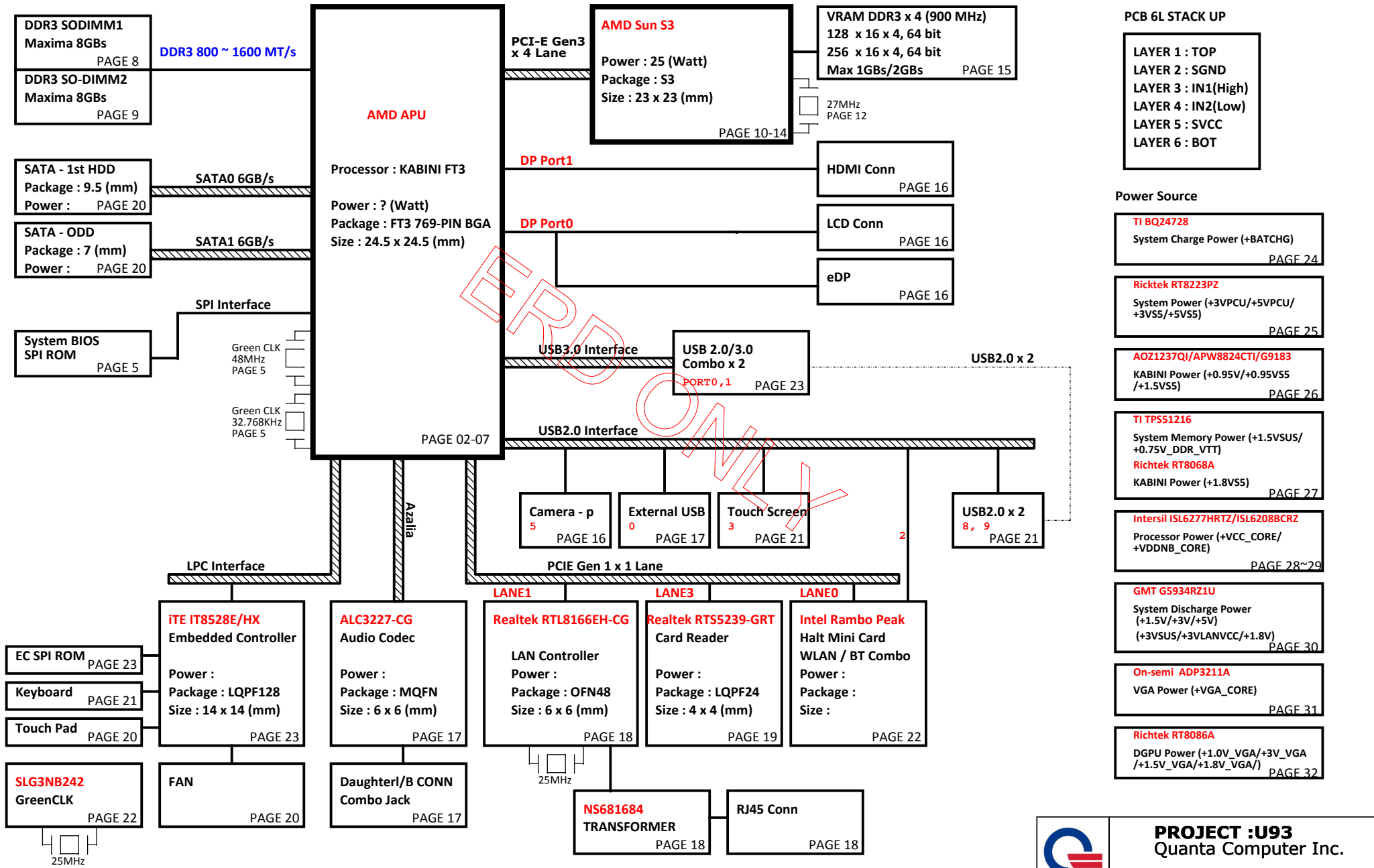
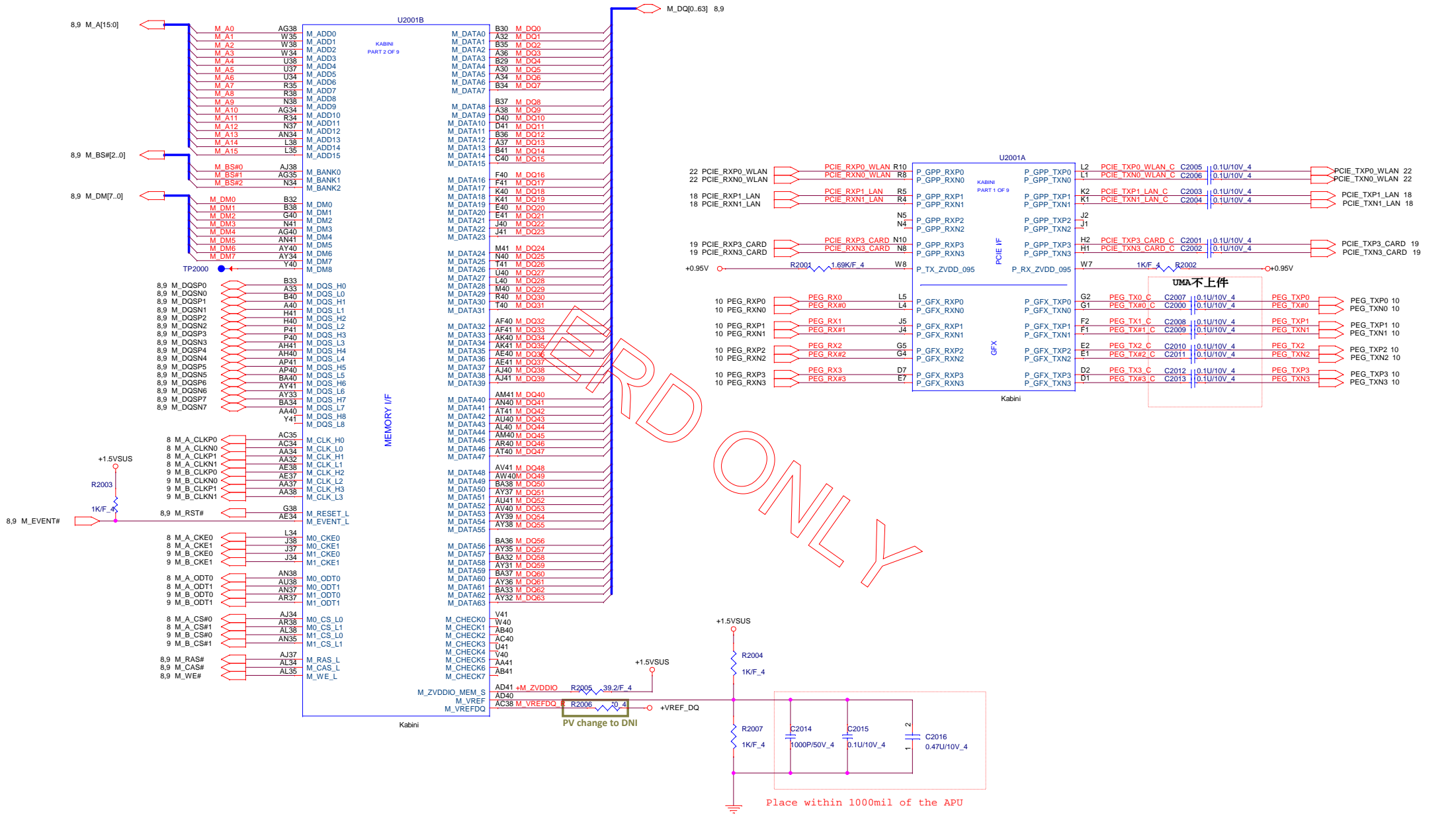


Lean G_AMD KABINI DIS/UMA (14"/15.6")

Ultra/Slim ⁰¹





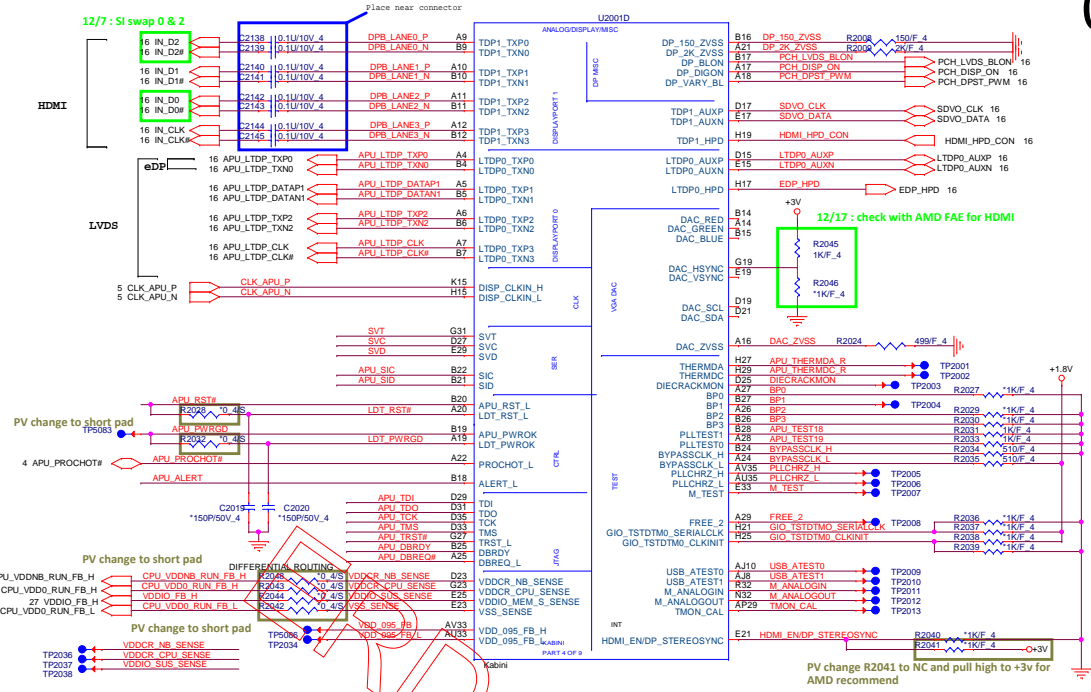
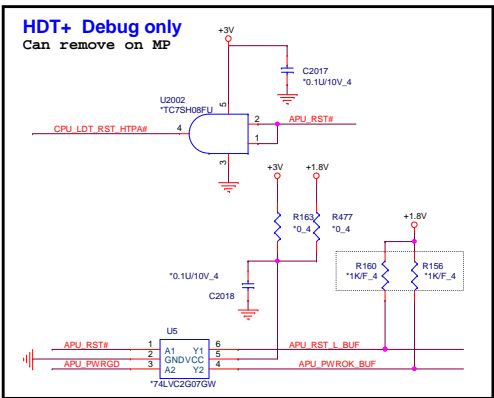
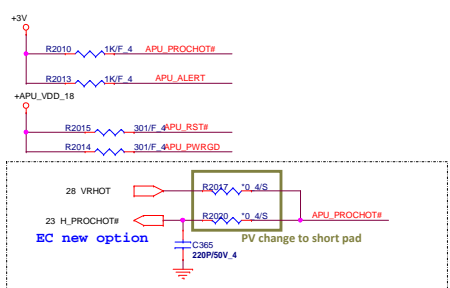
FORN ONLY

Place within 1000mil of the APU

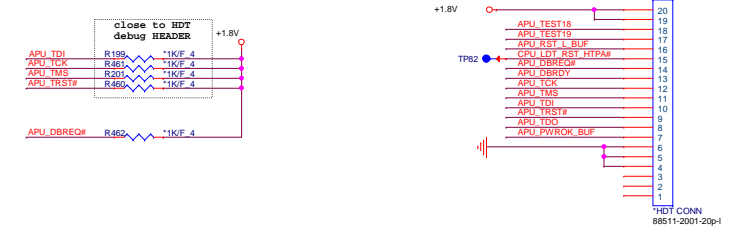
6,8,9,27,30,32 +1.5VSUS
8,9 +VREF_DQ
5,6,26 +0.95V



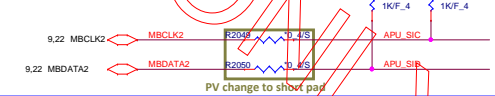
	INT PROJECT :U93 Quanta Computer Inc.		Rev 1A
	Size MEM/PCIE (1/6)		
Date: Monday, May 27, 2013		Sheet 2 of 32	



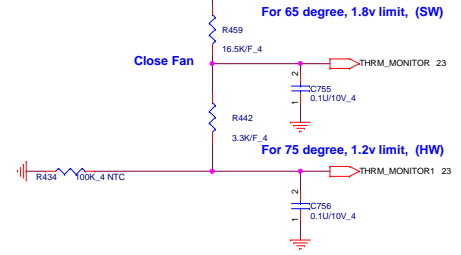
HDT+ Connector for Debug only



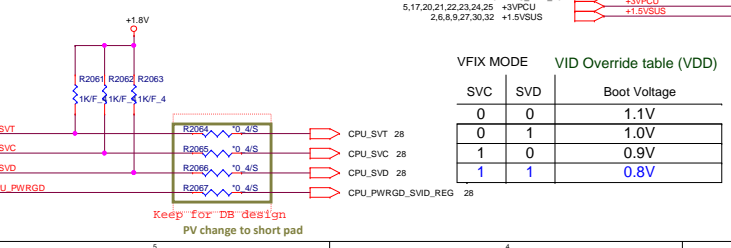
Thermal Sensor

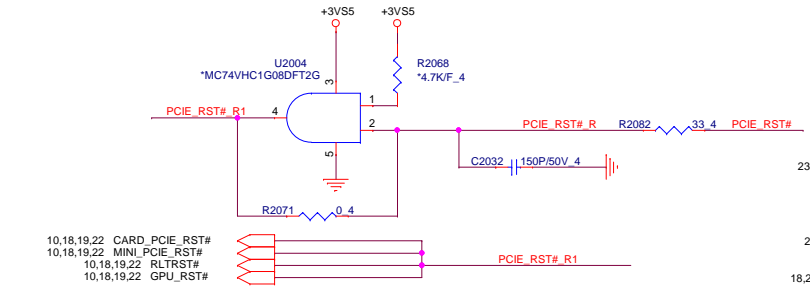


IO Thrm Protect

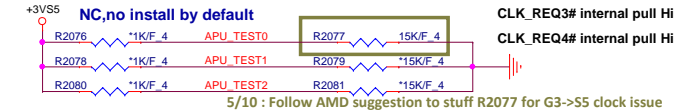


Serial VID

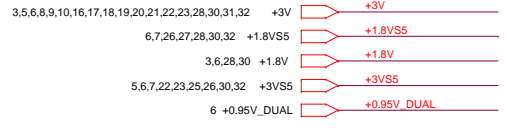
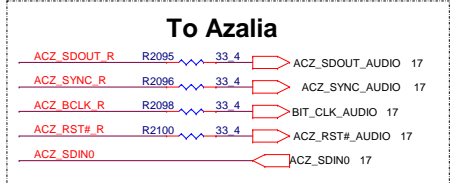
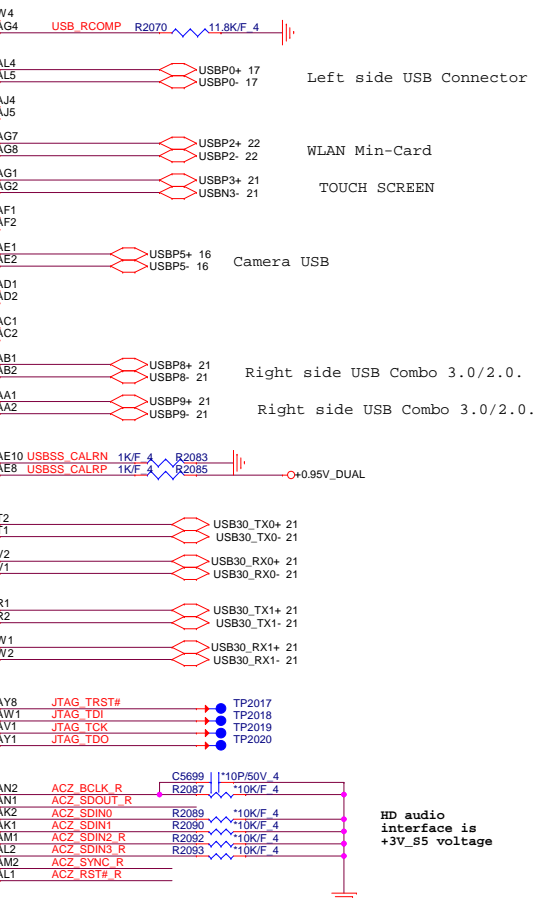
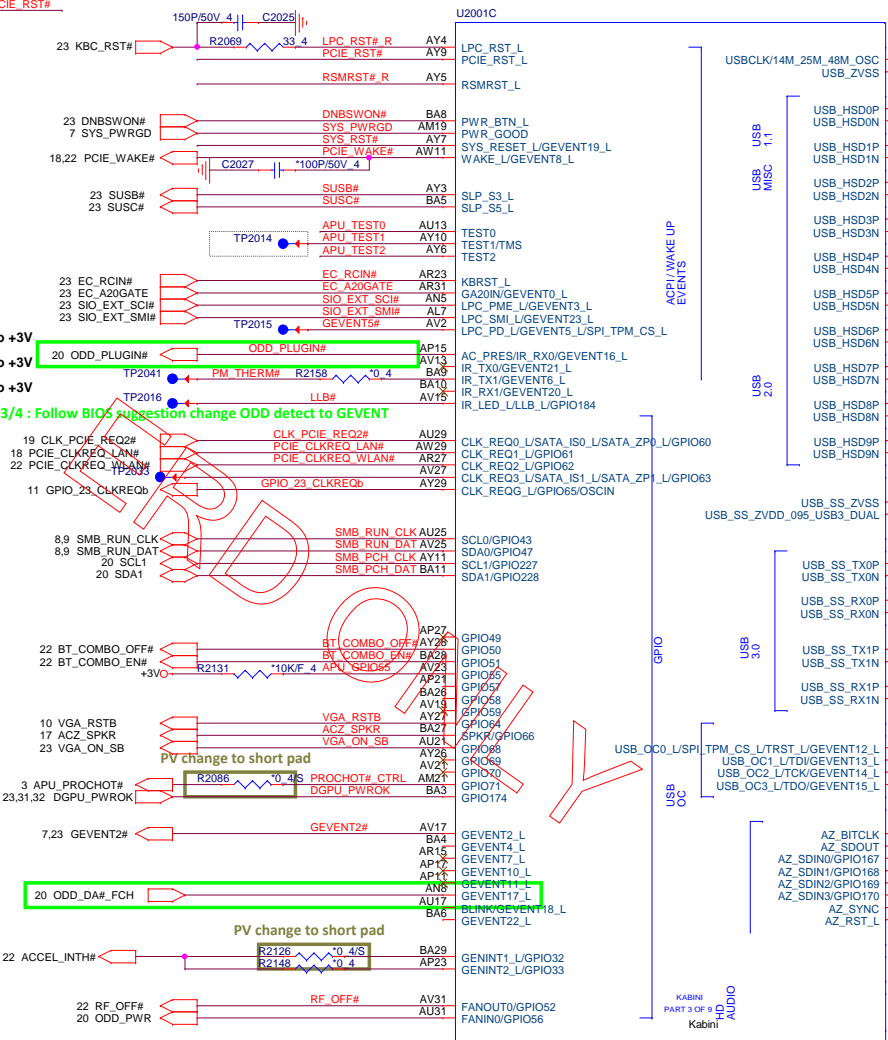
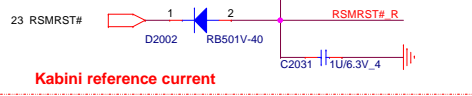
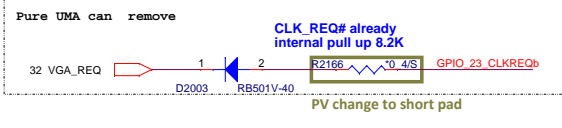
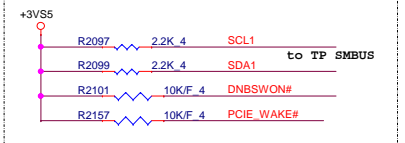
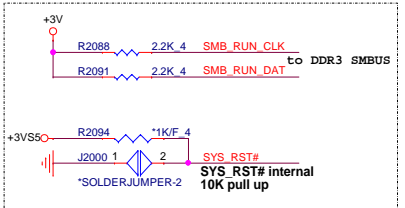




- 10,18,19,22 CARD_PCIE_RST#
- 10,18,19,22 MINI_PCIE_RST#
- 10,18,19,22 RLTRST#
- 10,18,19,22 GPU_RST#



TEST2	TEST1	TEST0	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted. FCH JTAG pins are overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins.
0	0	1	Reserved
0	1	X	Reserved
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins.
1	TMS	1	Use on ATE only Yuba JTAG enabled

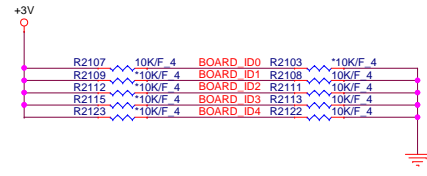
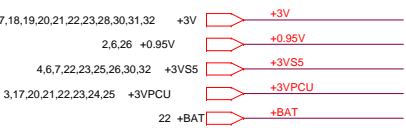
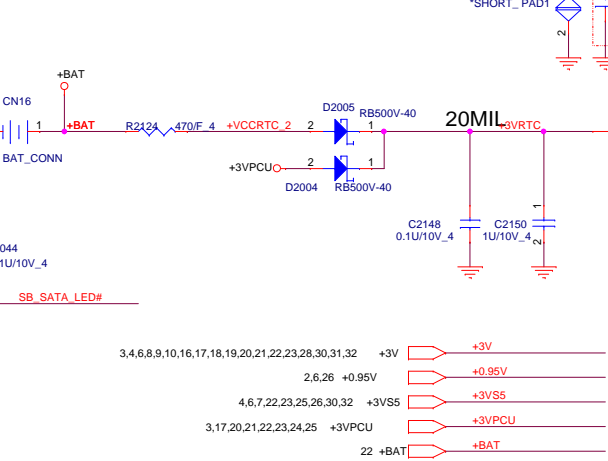
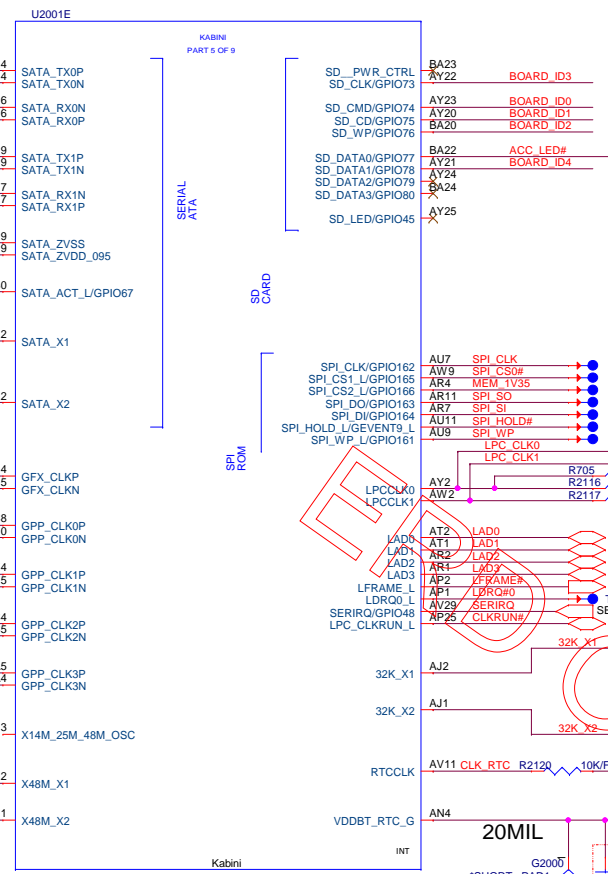
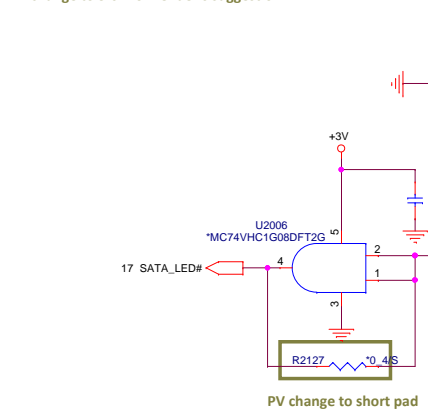
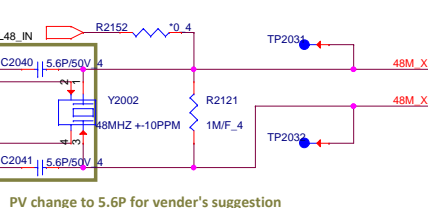
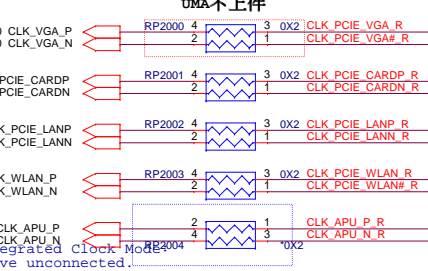
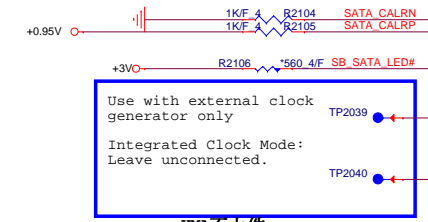
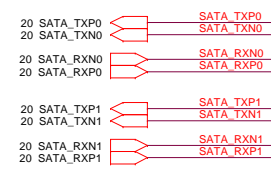


PROJECT :U93
Quanta Computer Inc.

Size: Document Number: **GPIO/USB/AZ (3/6)** Rev: 1A

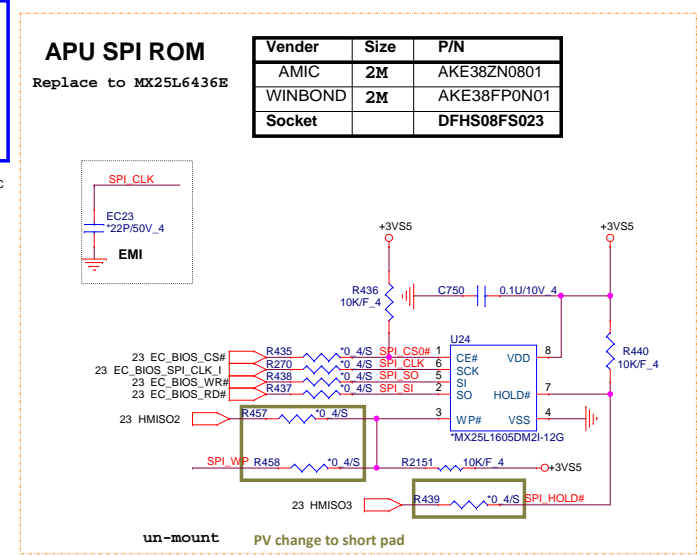
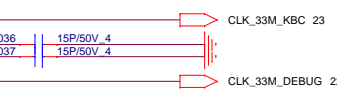
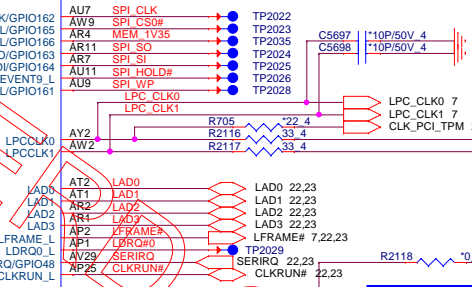
Date: Monday, May 27, 2013 Sheet: 4 of 32

SATA HDD
SATA ODD



BOARD ID SETTING

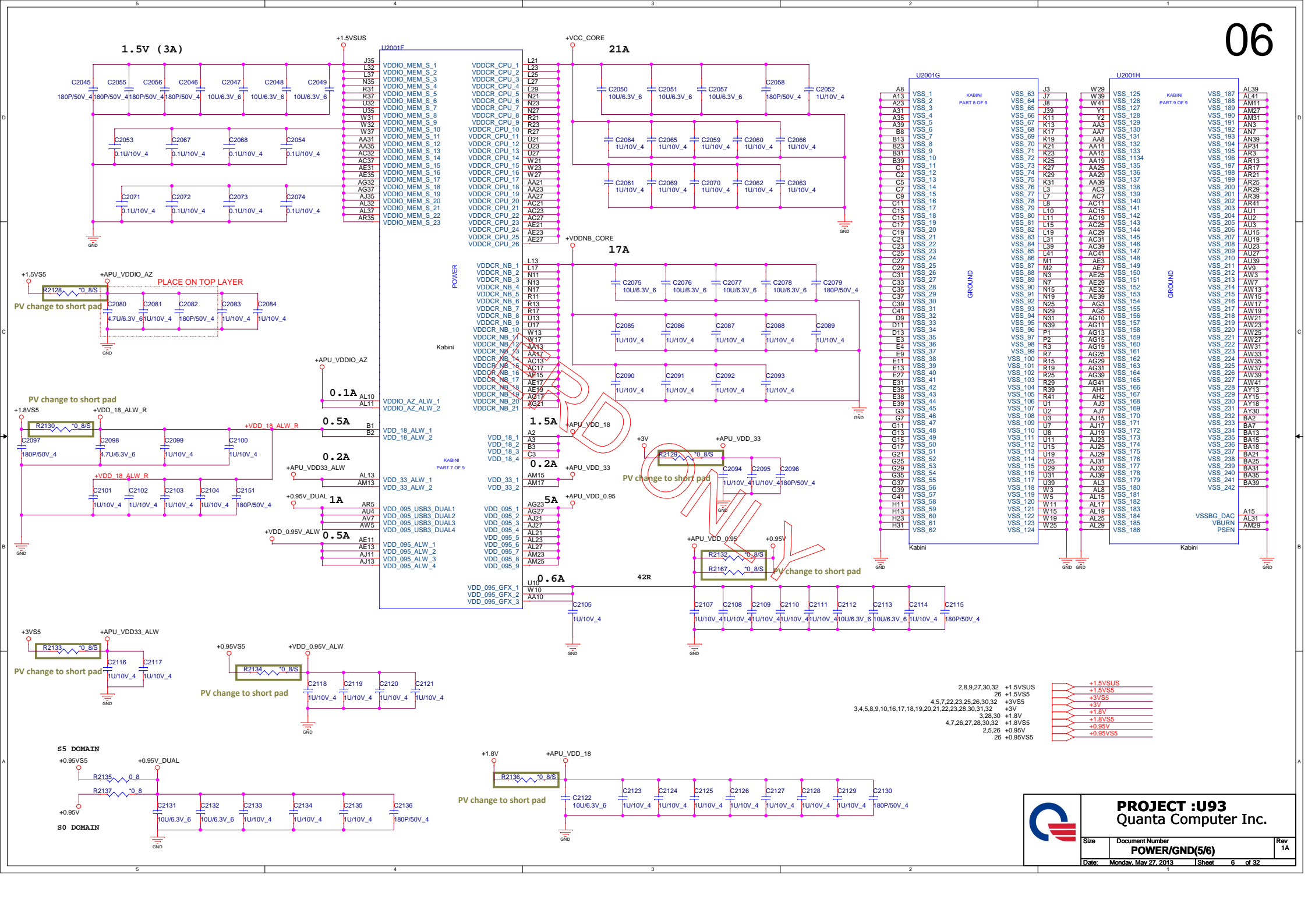
Model	BOARD_ID0	BOARD_ID1	BOARD_ID2	BOARD_ID3	BOARD_ID4
14" UMA	0	0	0	0	0
15" UMA	0	1	0	0	0
14" DIS	1	0	0	0	0
15" DIS	1	1	0	0	0



un-mount PV change to short pad

PROJECT :U93
Quanta Computer Inc.

Size	Document Number	Rev
	SATA/CLK (4/6)	1A
Date:	Thursday, May 30, 2013	Sheet 5 of 32



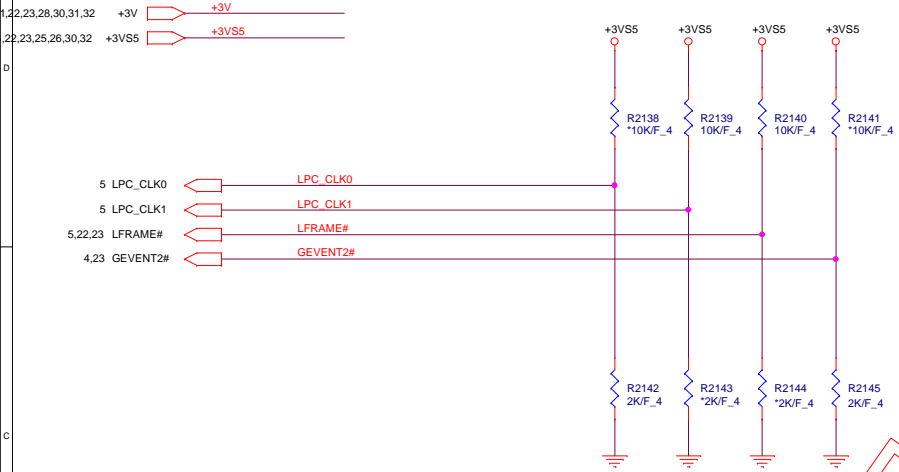
PROJECT :U93
Quanta Computer Inc.

Size	Document Number	Rev
	POWER/GND(5/6)	1A
Date:	Monday, May 27, 2013	Sheet 6 of 32

STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

DEBUG STRAPS

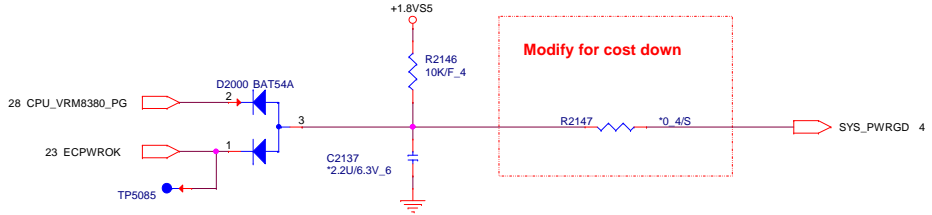


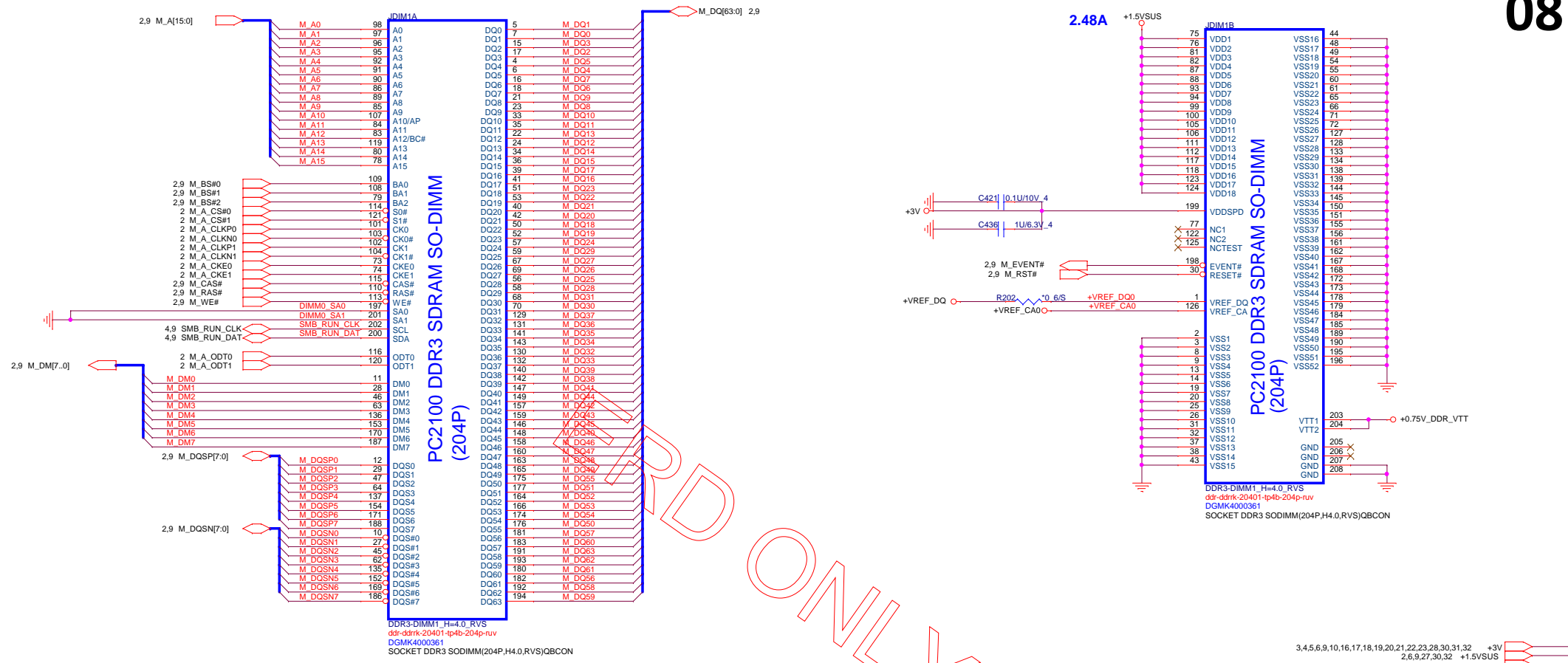
REQUIRED STRAPS

				LPC_CLK0	LPC_CLK1	LFRAME#	GEVENT2#
PULL HIGH				BOOT FAIL TIMER ENABLED	CLKGEN ENABLED DEFAULT	SPI ROM DEFAULT	1.8V SPI ROM
PULL LOW				BOOT FAIL TIMER DISABLED DEFAULT	CLKGEN DISABLED	LPC ROM	3.3V SPI ROM DEFAULT

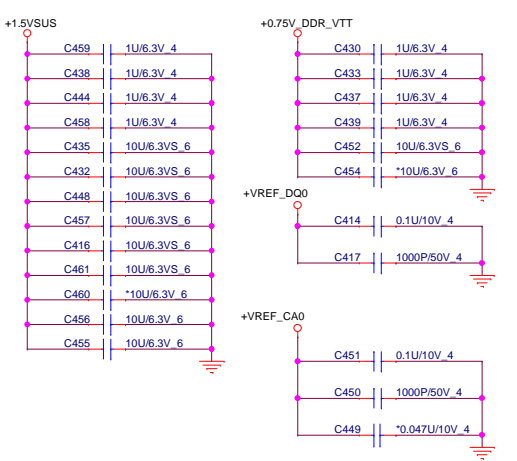
PROTOTYPE ONLY

SYS_PWRGD

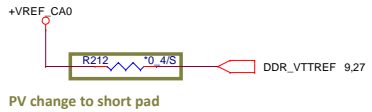
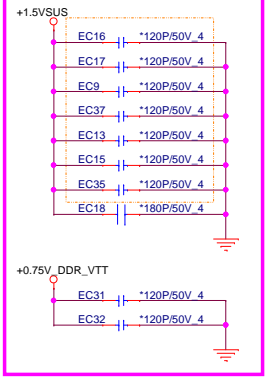




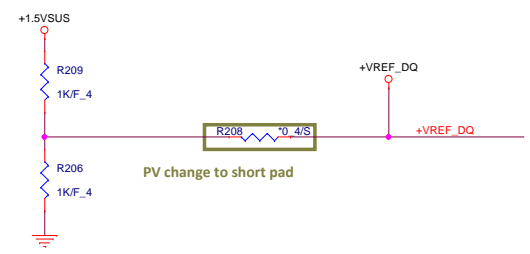
Place these Caps near So-Dimm0.



For EMI RESERVE

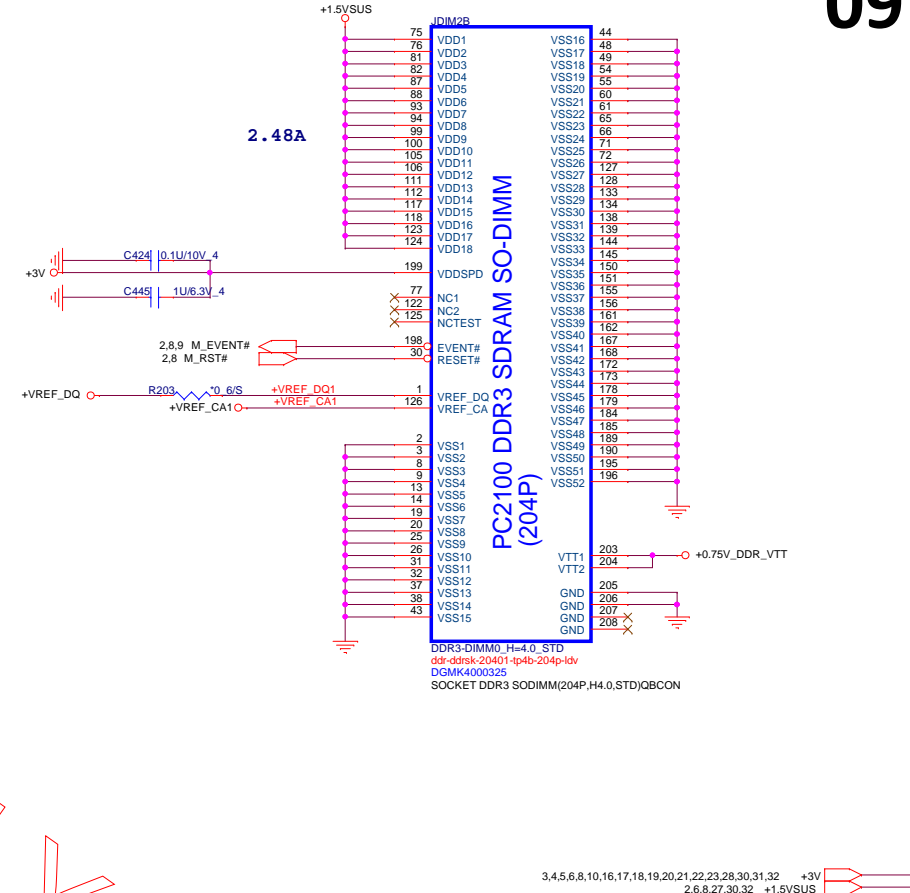
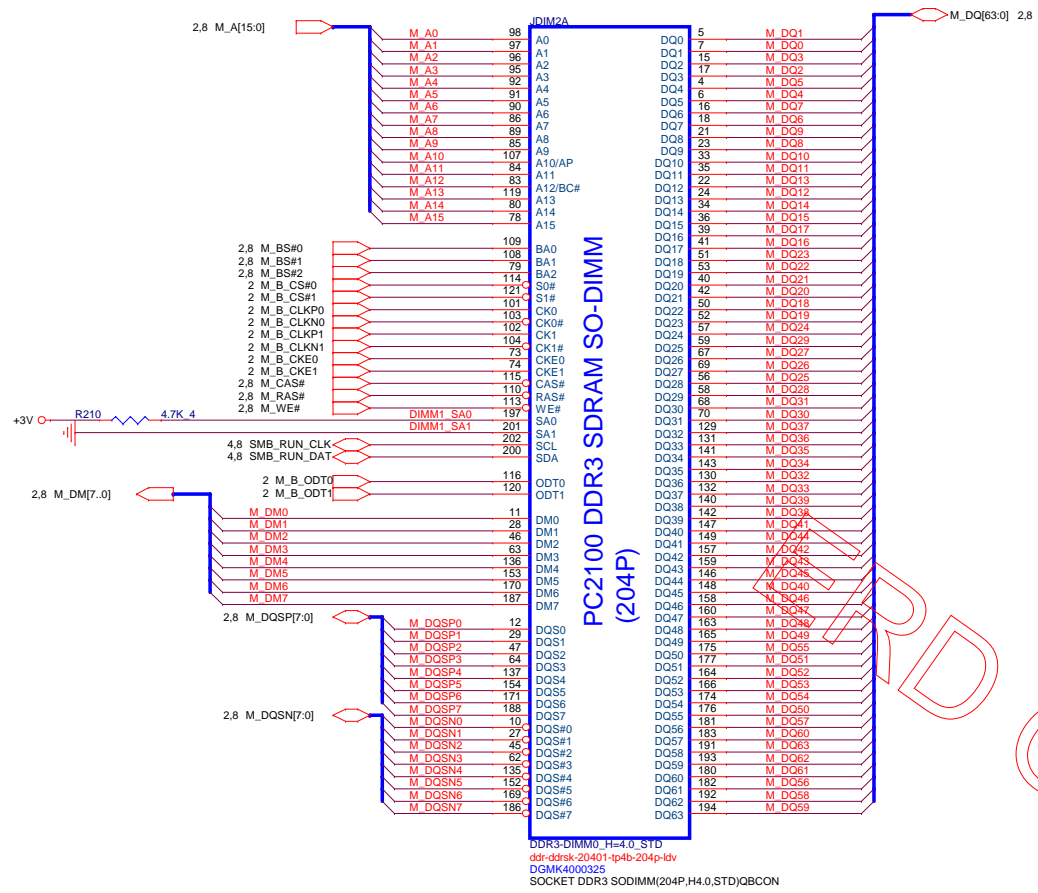


Reserved for AMD suggest



PROJECT :U93
Quanta Computer Inc.

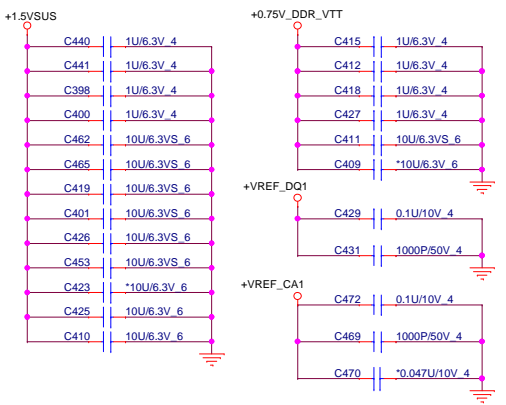
Size Custom	Document Number System Memory 1/2 (5.2H)	Rev 1A
Date: Monday, May 27, 2013	Sheet 8 of 32	



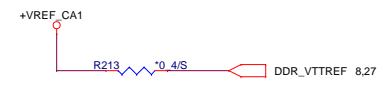
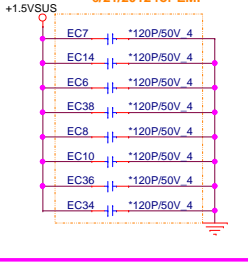
DDR3-DIMM0_H=4.0_STD
 ddr-ddrsk-20401-tp4b-204p-ldv
 DGMK4000325
 SOCKET DDR3 SODIMM(204P,H4.0,STD)QBCCN

3,4,5,6,8,10,16,17,18,19,20,21,22,23,28,30,31,32 +3V
 2,6,8,27,30,32 +1.5VSUS
 8,27 +0.75V_DDR_VTT

Place these Caps near So-Dimm1.

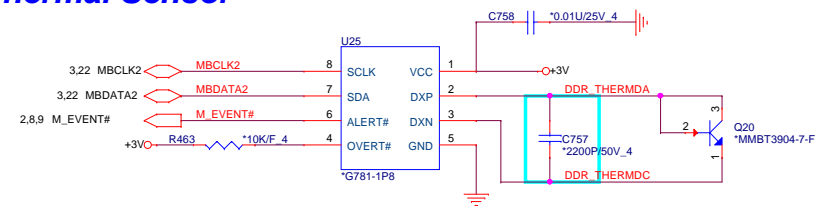


For EMI RESERVE
 6/21/2012 for EMI



Local Thermal Sensor

DDR3 Thermal Sensor

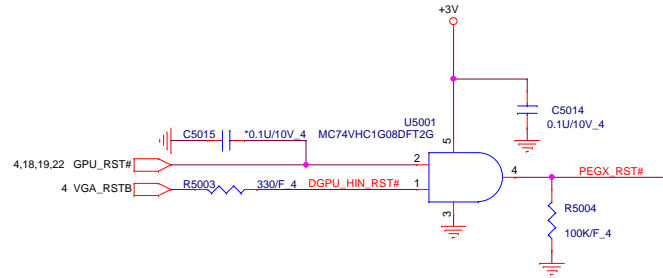
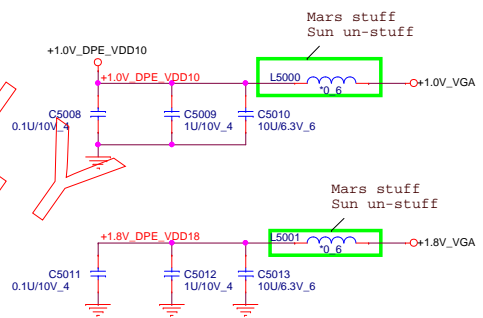
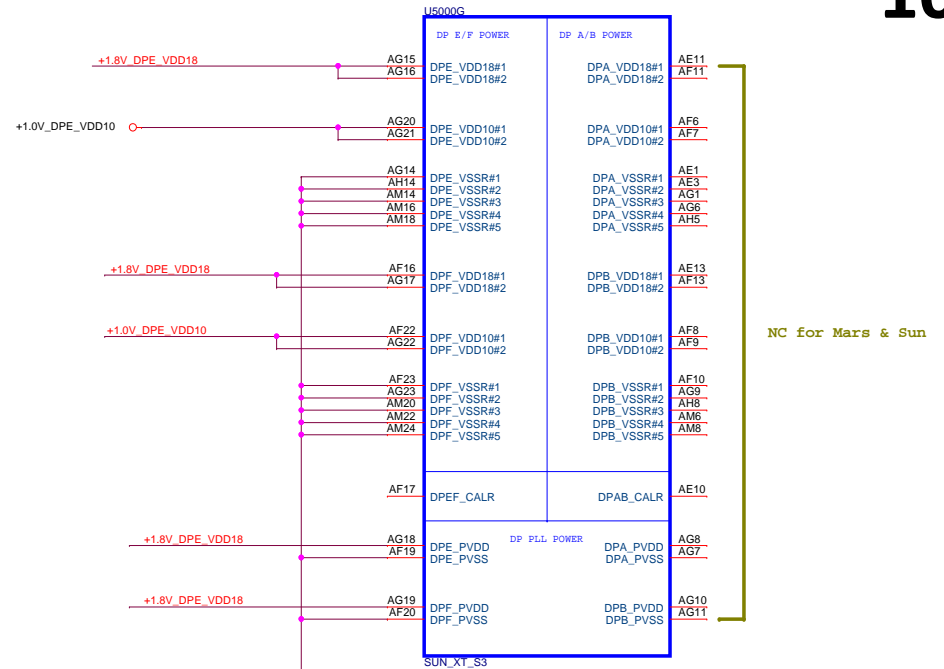
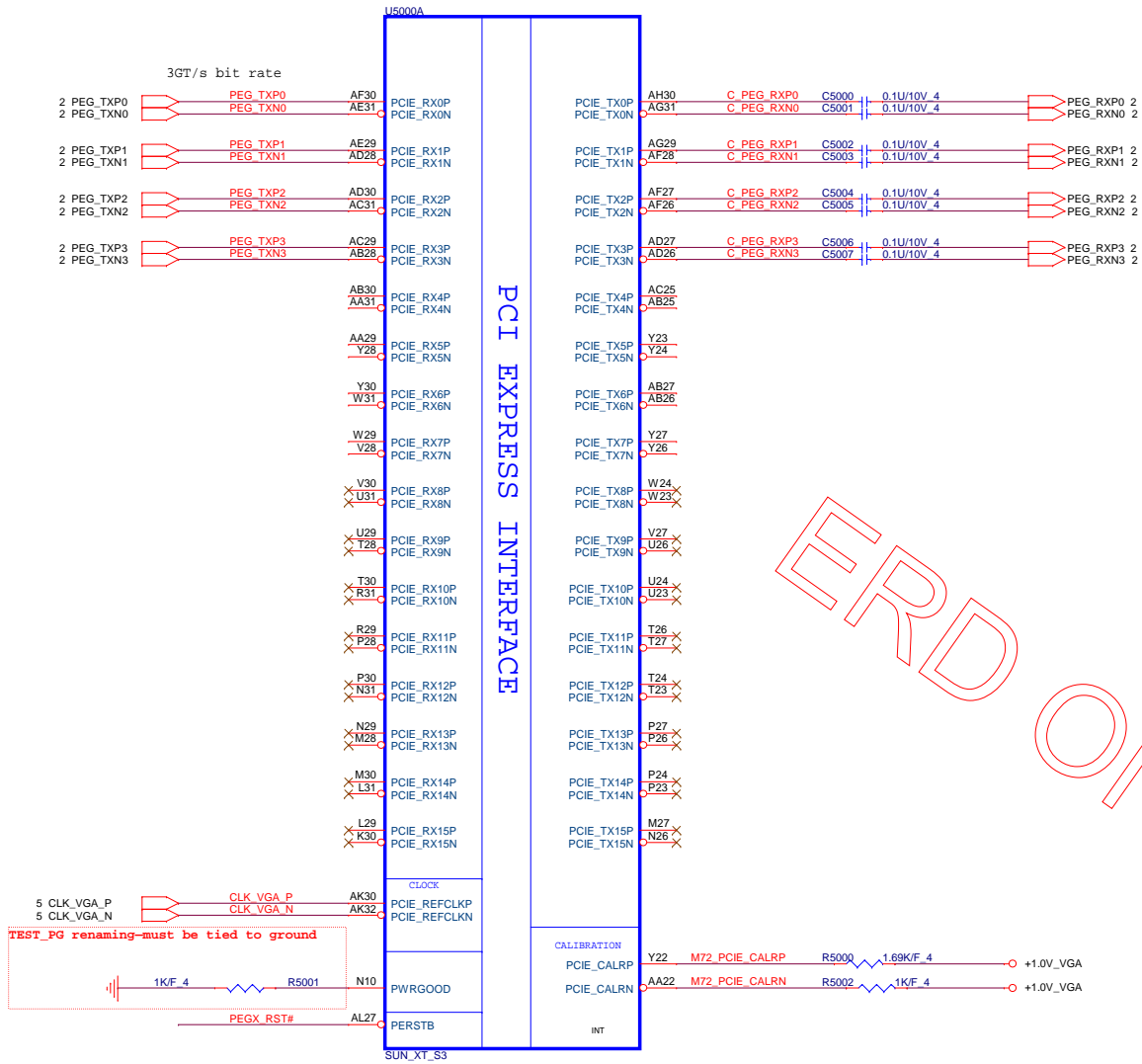


If use internal thermal IC, C9007 use 0ohm.

Main:AL000781039 G781-1P8(9Ah)
 2nd:AL001412005 EMC1412-2-ACZL-TR(9Ah)

Main:AL001412003 EMC1412-1-ACZL-TR(98h)
 2nd:AL000431014 TMP431ADGKR(98h)

		PROJECT :U93	
		Quanta Computer Inc.	
Size	Document Number	Rev	
Custom	System Memory 2/2 (9.2H)	1A	
Date:	Monday, May 27, 2013	Sheet	9 of 32



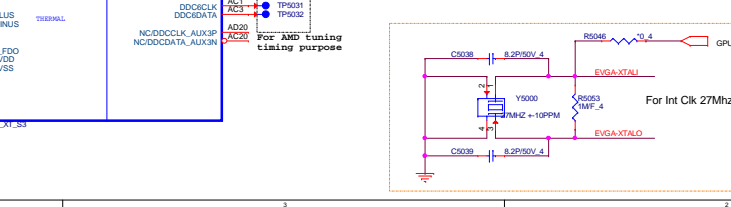
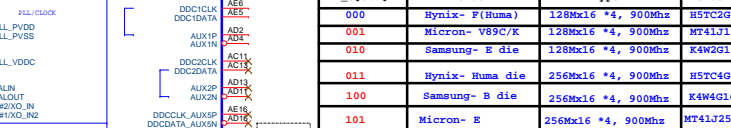
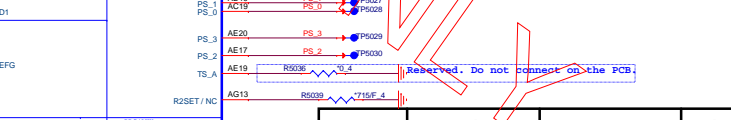
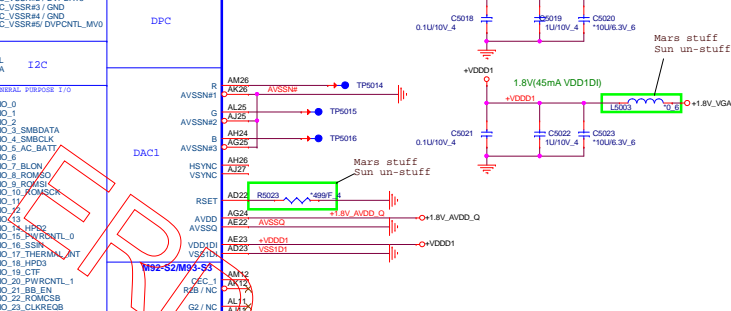
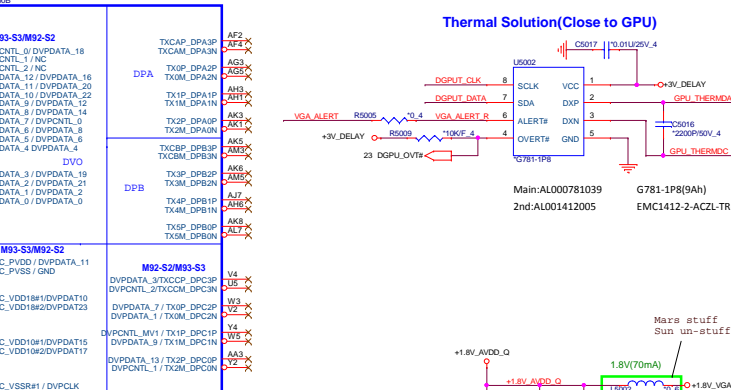
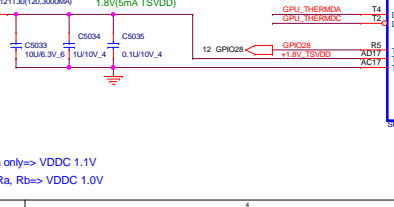
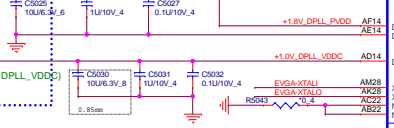
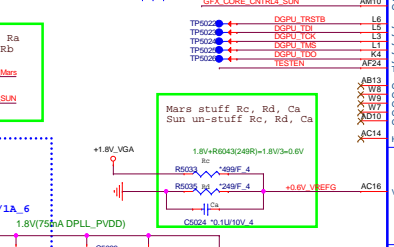
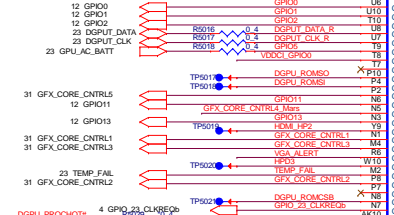
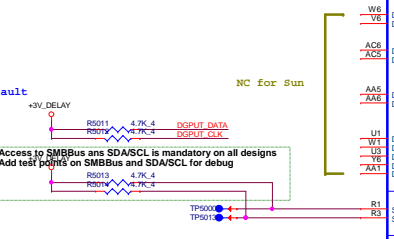
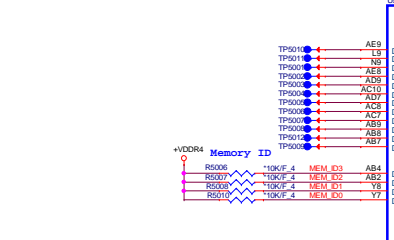
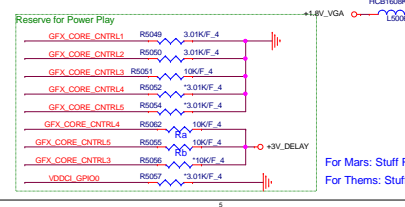
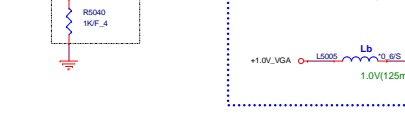
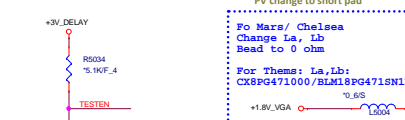
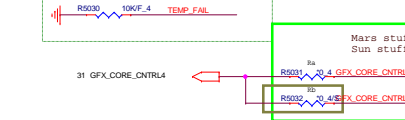
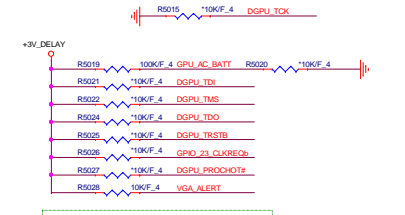
+1.0V_VGA 11,13,32
 +1.8V_VGA 11,13,22,32

PROJECT :U93
Quanta Computer Inc.

Size Custom	Document Number Sun S3 PCIe Interface	Rev 1A
Date: Saturday, June 15, 2013 Sheet 10 of 32		

ERD ONLY

Table with 7 columns: PWRCTRL5, PWRCTRL4, PWRCTRL3, PWRCTRL2, PWRCTRL1, V-CORE, and values from 0 to 1.175V.



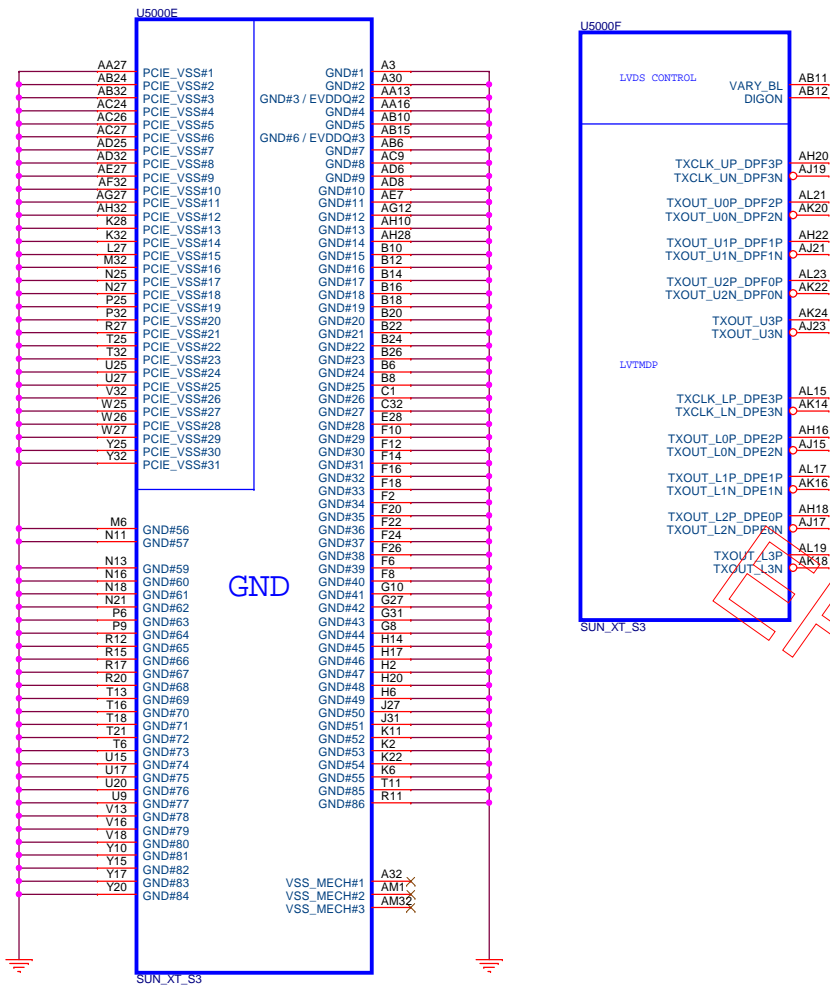
MLPS Implementation section with bullet points, a capacitor/resistor divider lookup table, and a circuit diagram for PS0, PS1, PS2, PS3.

Table with 5 columns: Pin/Blt, Name, Description, Default, Legacy. Lists various pins and their configurations.

Table with 6 columns: PS_3[3:1], Vendor, Type, Vendor P/N, R5045, R5048. Lists component specifications for PS pins.

Circuit diagram for a 27Mhz oscillator with a 10MHz crystal and buffer.

PROJECT :U93 Quanta Computer Inc. including a QR code, logo, and document information.



CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS
 ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
 0= DO NOT INSTALL RESISTOR
 1 = INSTALL 3K RESISTOR
 X = DESIGN DEPENDANT
 NA = NOT APPLICABLE

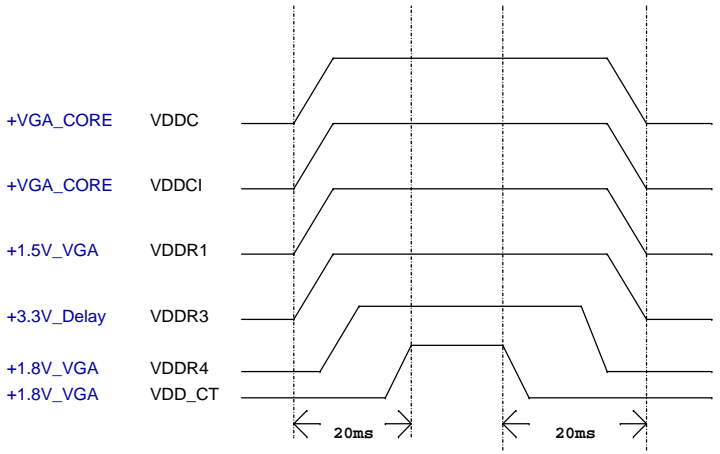
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	0
RSVD	GPIO2	RESERVED	X
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:1]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1] AUD[0]	HSYNC VSYNC	SEE DATABOOK FOR DETAIL SEE DATABOOK FOR DETAIL	0 0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21	H2SYNC	GENERICC	GPIO8	GPIO2
--------	--------	----------	-------	-------

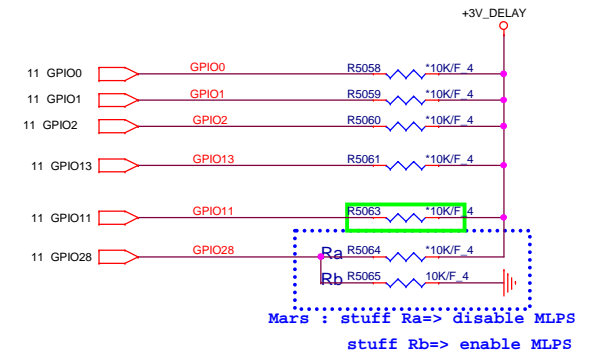
Power Up/Down Sequence



Memory Aperture size(Seymour)

GPIO9 BIOSROM	GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0
0	256M	0	1
0	64M	0	0
0	32M	0	1
0	512M	1	0
0	1G	1	1
0	2G	1	0
0	4G	1	1

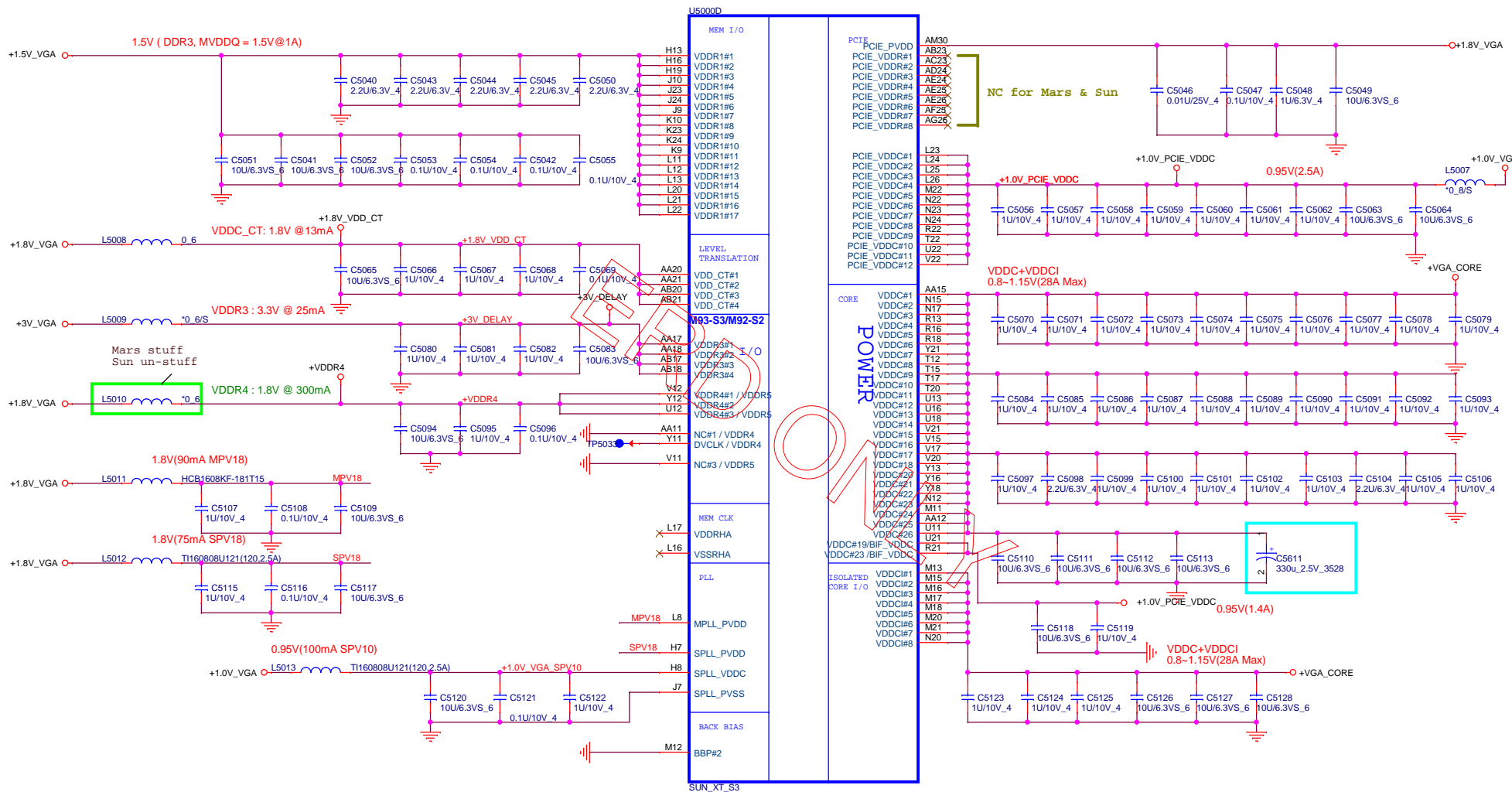
It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.



PROJECT :U93
 Quanta Computer Inc.

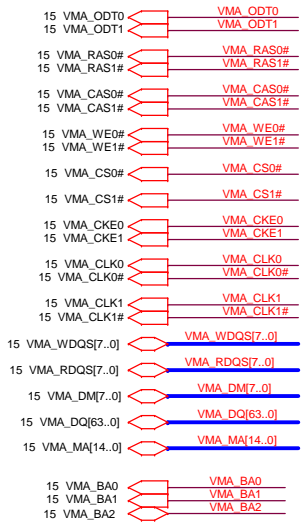
Size Custom	Document Number Sun S3 GND / LVDS/ Straps	Rev 1A
Date: Saturday, June 15, 2013		Sheet 12 of 32

+3V_DELAY 11,13

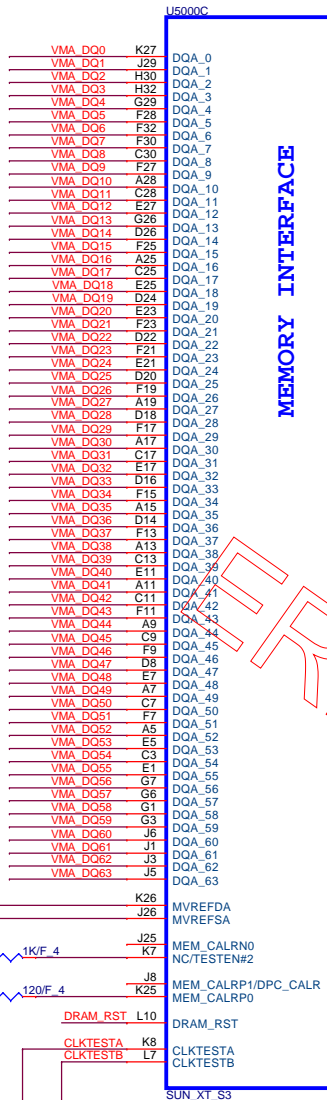


- ➔ +1.5V_VGA 14,15,32
- ➔ +1.8V_VGA 10,11,22,32
- ➔ +1.0V_VGA 10,11,32
- ➔ +VGA_CORE 31,32
- ➔ +3V 3,4,5,6,8,9,10,16,17,18,19,20,21,22,23,28,30,31,32
- ➔ +5V 16,17,20,21,30

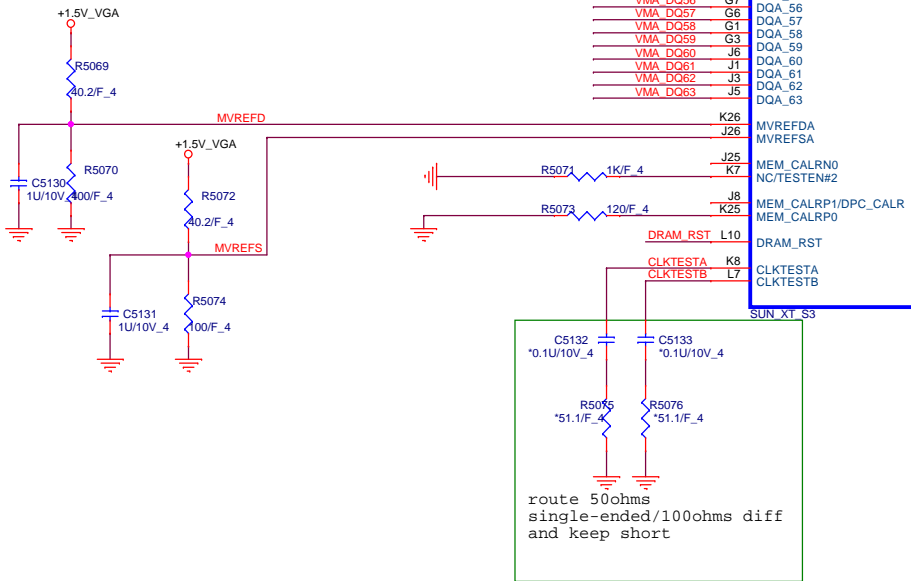
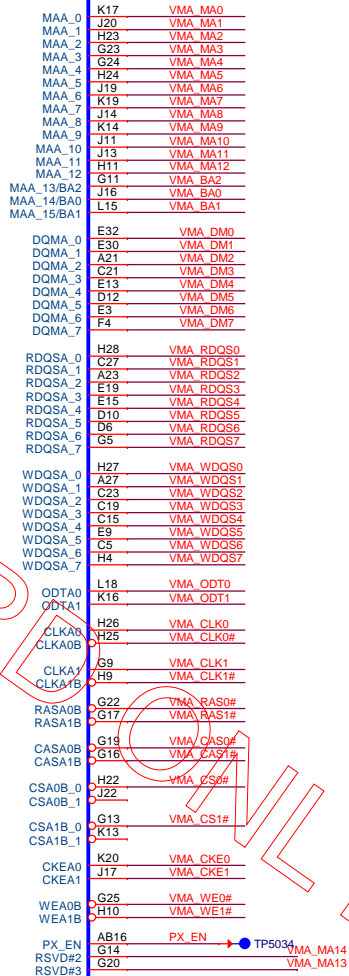
	PROJECT :U93	
	Quanta Computer Inc.	
Size Custom	Document Number Sun S3 Power_and_NC	Rev 1A
Date: Saturday, June 15, 2013	Sheet 13 of 32	



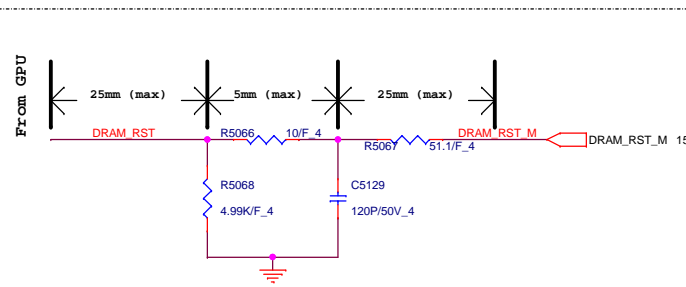
support 1gbit
VRAM (64M X 16)



MEMORY INTERFACE



route 50ohms
single-ended/100ohms diff
and keep short



Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

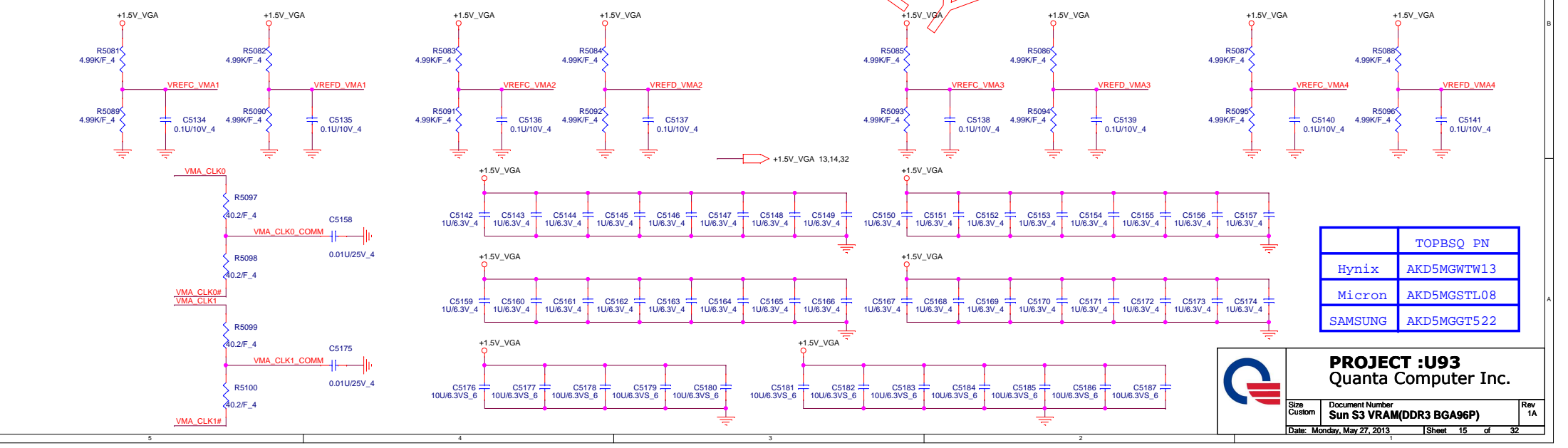
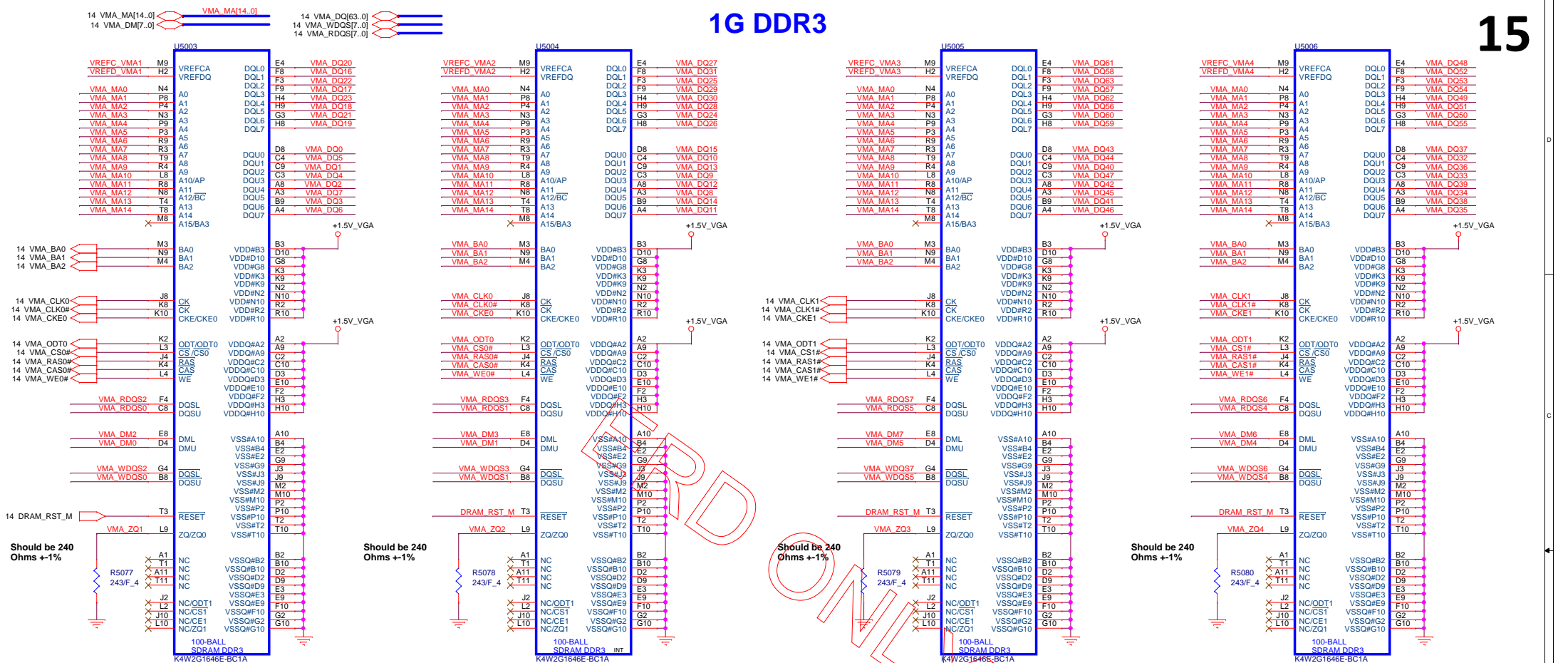
This basic topology should be used for DRAM_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.



PROJECT :U93
Quanta Computer Inc.

Size Custom	Document Number Sun S3 MEM Interface	Rev 1A
Date: Saturday, June 15, 2013	Sheet 14 of 32	

1G DDR3

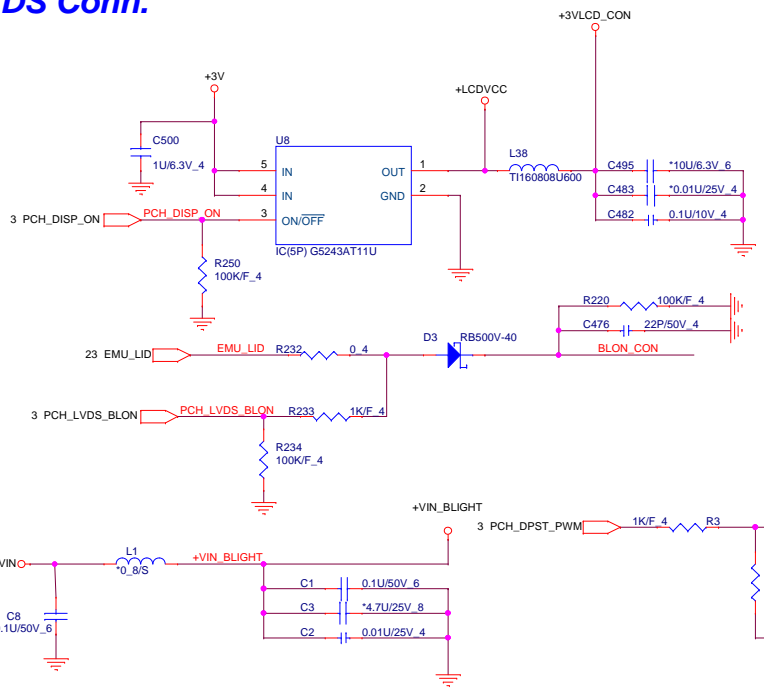


	TOPBSQ PN
Hynix	AKD5MGWTW13
Micron	AKD5MGSTL08
SAMSUNG	AKD5MGGT522

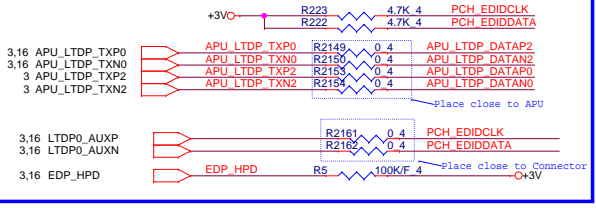
PROJECT :U93
Quanta Computer Inc.

Size Custom	Document Number Sun S3 VRAM(DDR3 BGA96P)	Rev 1A
Date: Monday, May 27, 2013	Sheet 15 of 32	

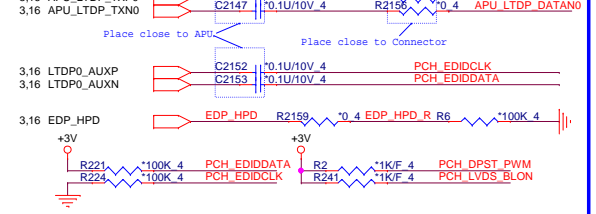
LVDS Conn.



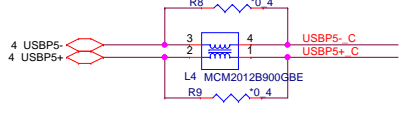
For LVDS only : stuff



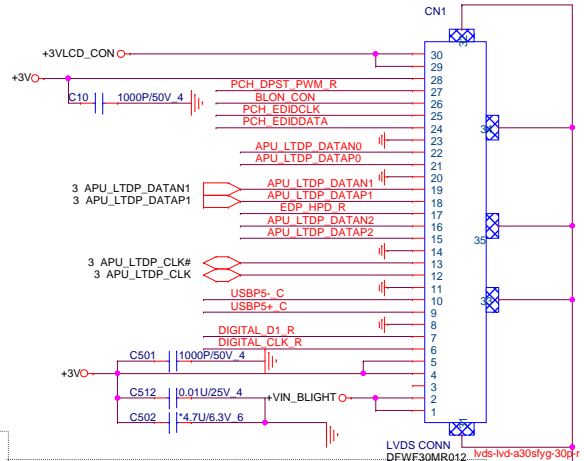
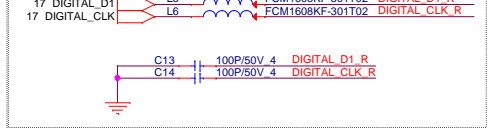
For EDP Only: stuff



USB CAMERA

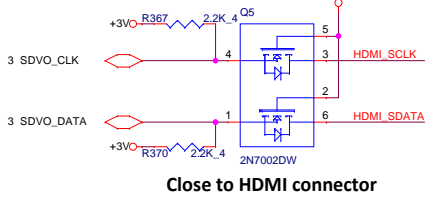


D_MIC



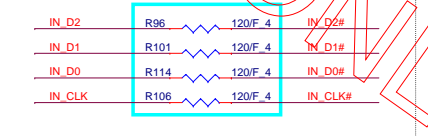
HDMI Conn.

HDMI SMBus Isolation

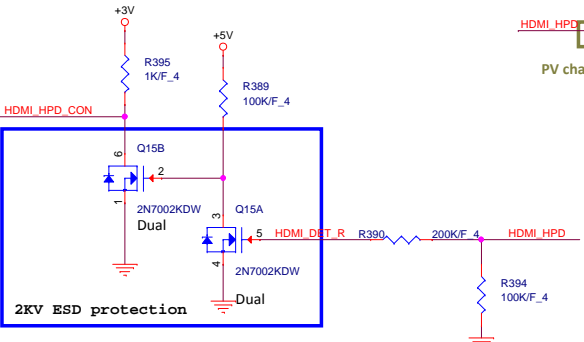


Close to HDMI connector

EMI Solution

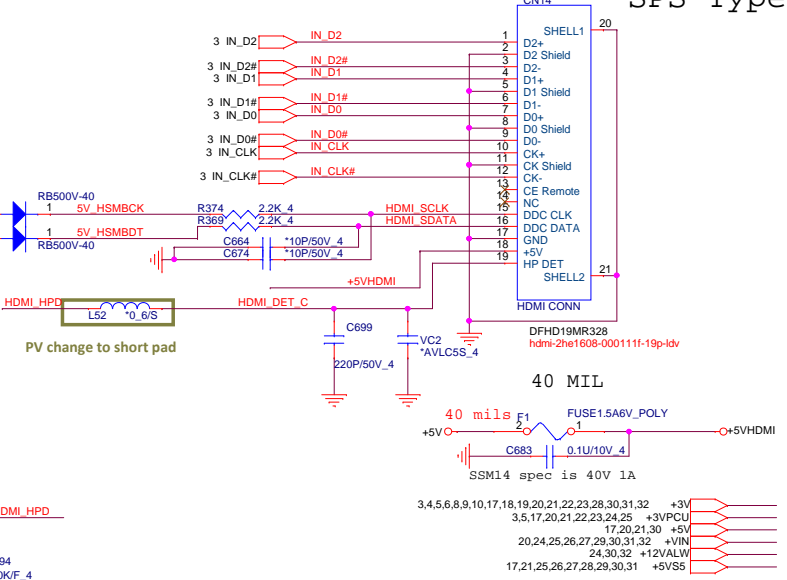


HDMI HPD SENSE



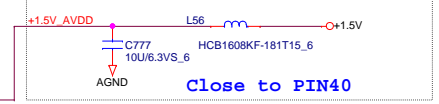
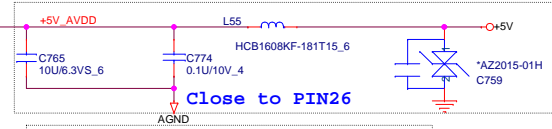
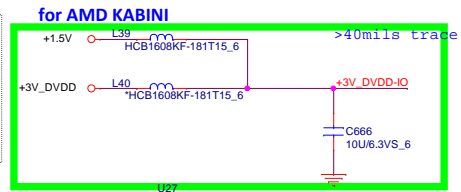
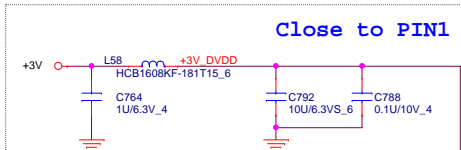
2KV ESD protection

SPS Type



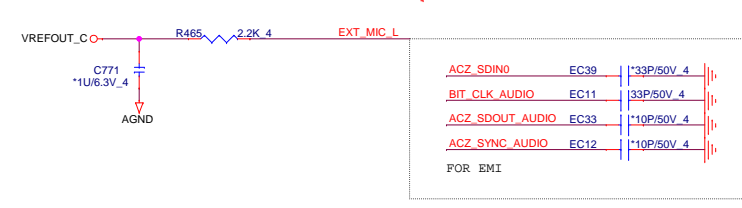
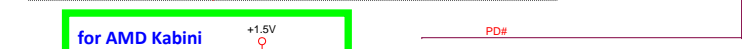
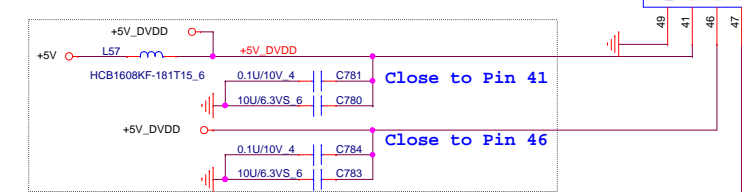
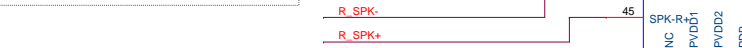
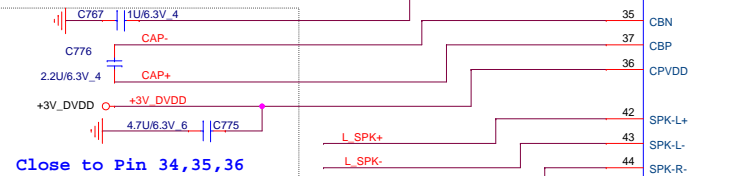
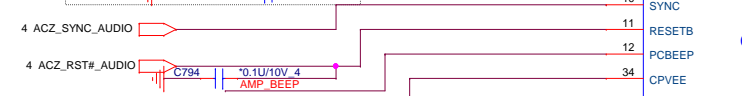
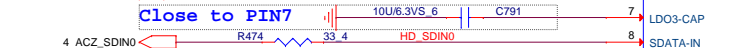
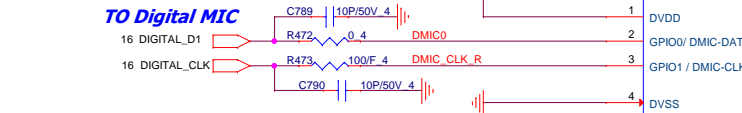
PROJECT :U93
Quanta Computer Inc.

Size Custom	Document Number LCD Connector (LVDS)	Rev 1A
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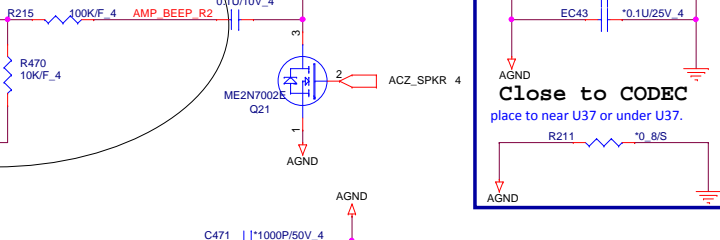
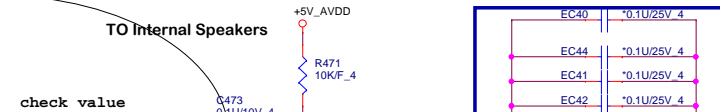
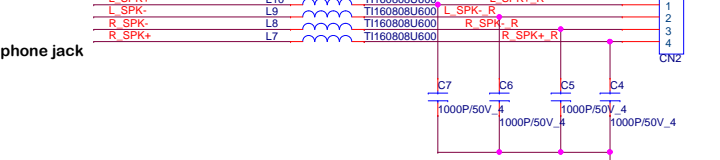
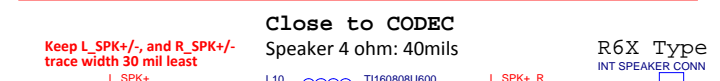
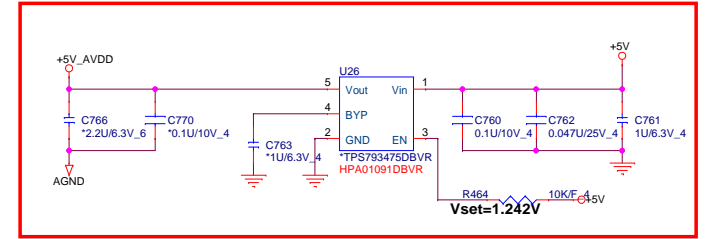
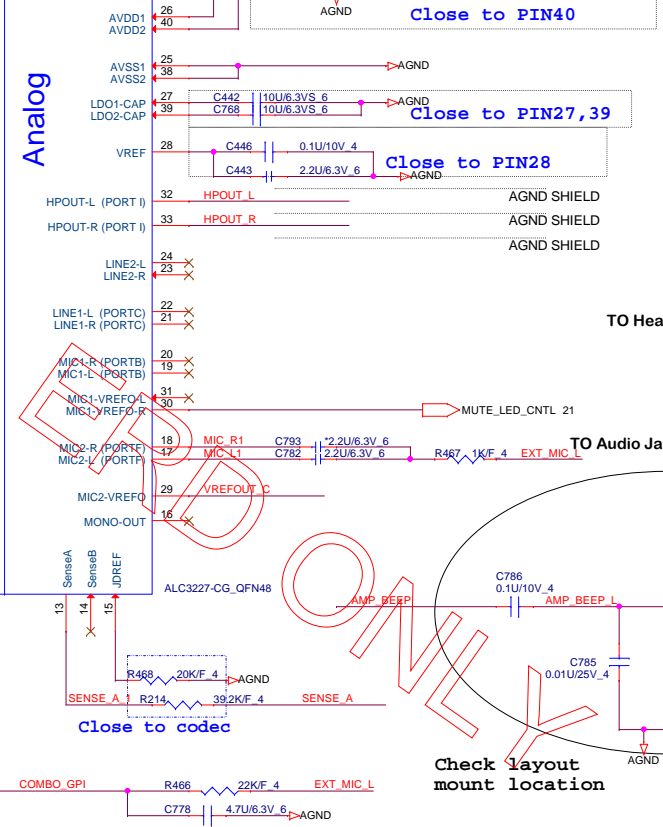
- 16,20,21,30 +5V
- 3,4,5,6,8,9,10,16,18,19,20,21,22,23,28,30,31,32 +3V
- 22,28,30 +1.5V

TO Digital MIC

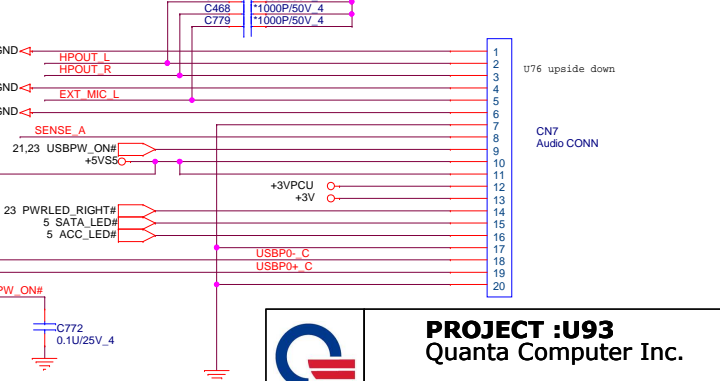
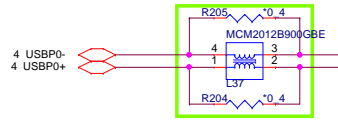


Analog

Digital



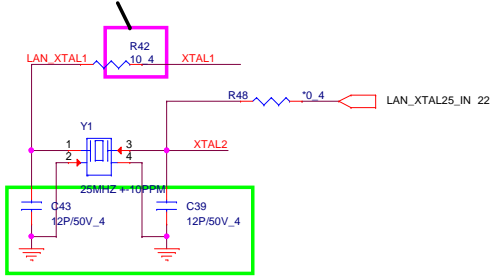
USB 2.0 AND AUDIO COMBO JACK



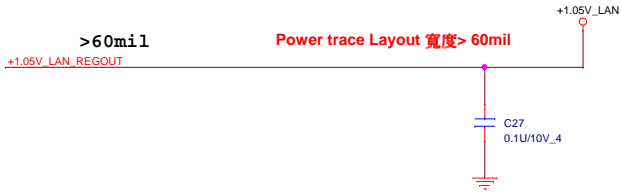
PROJECT :U93
Quanta Computer Inc.

Size Custom	Document Number Azalia ALC3227	Rev 1A
Date: Tuesday, June 04, 2013	Sheet 17	of 32

For EMI 0 ~ 22 ohm

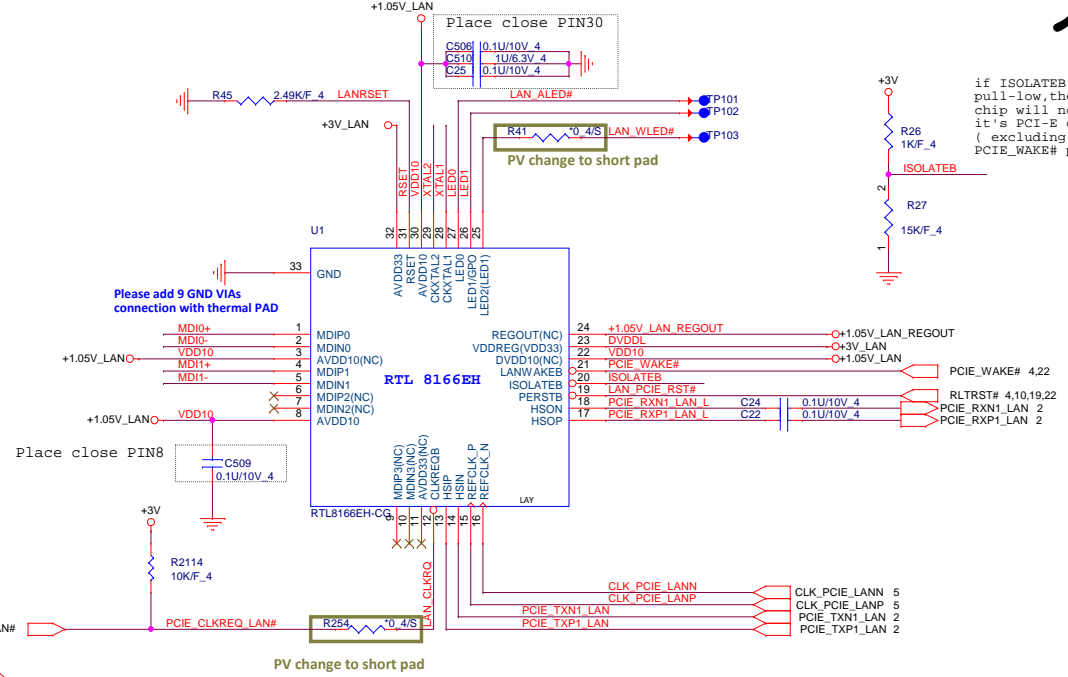
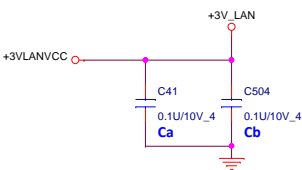


SI change to 12p



>60mil Power trace Layout 宽度 > 60mil

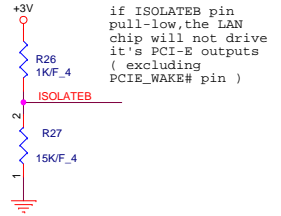
Place close PIN23 and PIN32



Please add 9 GND VIAS connection with thermal PAD

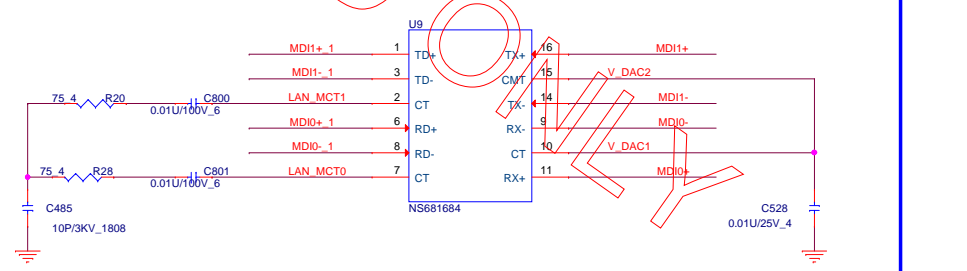
Place close PIN8

PV change to short pad

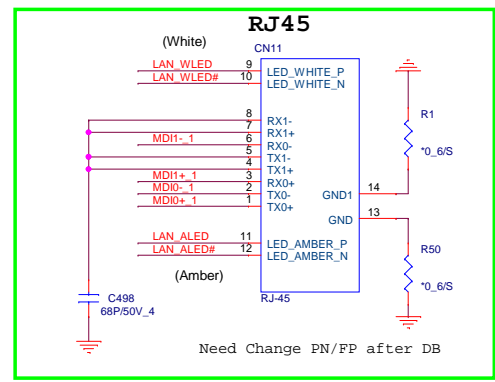


if ISOLATEB pin pull-low, the LAN chip will not drive it's PCI-E outputs (excluding PCI-E_WAKE# pin)

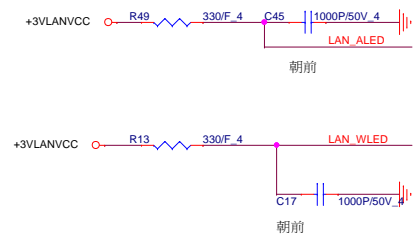
ERRD



LAN conn



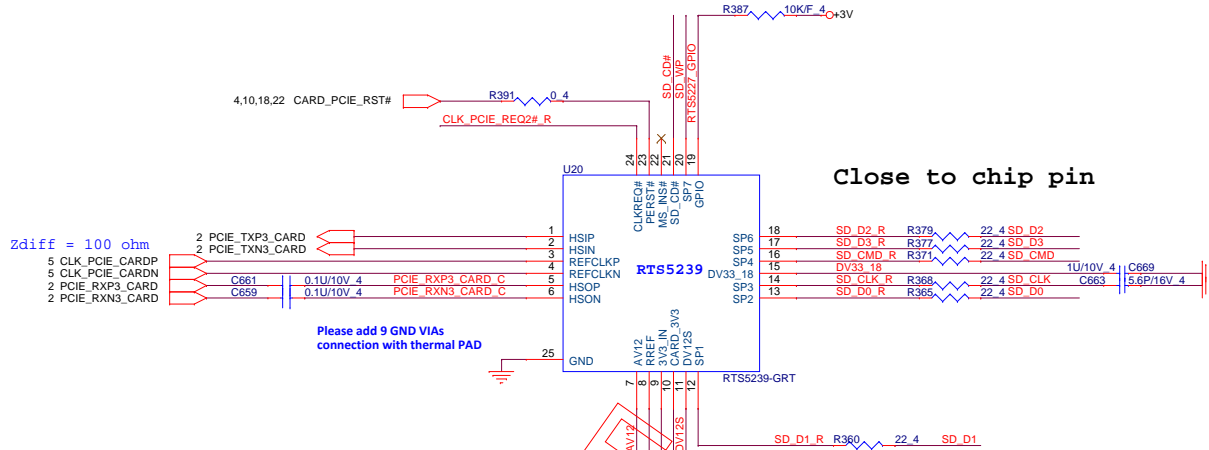
Need Change PN/FP after DB



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Quanta Computer Inc.

Size Custom	Document Number RTL 8166EH/RJ45	Rev 1A
Date: Tuesday, June 04, 2013	Sheet 18 of 32	

4 CLK_PCIE_REQ2# CLK_PCIE_REQ2# R392 0.4/S CLK_PCIE_REQ2# R



Close to chip pin

Zdiff = 100 ohm

- 2 PCIE_TXP3_CARD
- 2 PCIE_TXN3_CARD
- 5 CLK_PCIE_CARDP
- 5 CLK_PCIE_CARDN
- 2 PCIE_RXP3_CARD
- 2 PCIE_RXN3_CARD

Please add 9 GND VIAs connection with thermal PAD

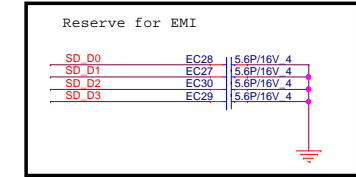
R363 need close to Chip

Close to chip pin

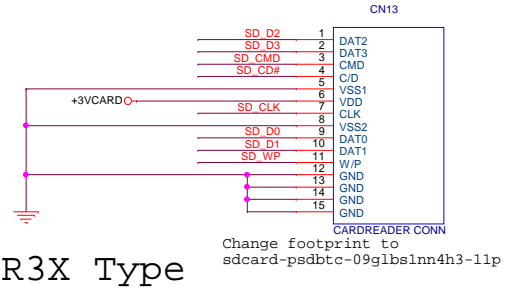
CLOSE CONN

SP1	SD_D1	MS_D1
SP2	SD_D0	MS_D0
SP3	SD_CLK	MS_D0
SP4	SD_CMD	MS_D2
SP5	SD_D3	MS_D3
SP6	SD_D2	MS_CLK
SP7	SD_WP	MS_BS

Share Pin



Reserve for EMI
SD / MMC
CARD READER



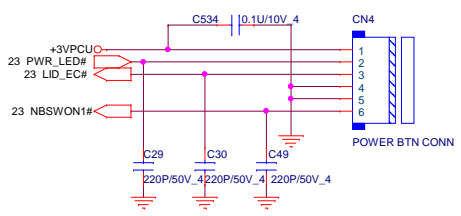
R3X Type

PROTOTYPE ONLY

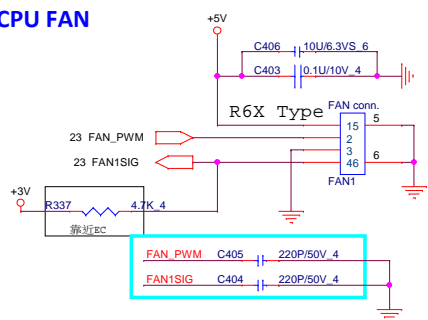
	PROJECT :U93 Quanta Computer Inc.		Rev 1A	
	Size Custom	Document Number RTS5239 & CR SOCKET		
	Date: Tuesday, June 04, 2013	Sheet 19 of 32		

Power Button Connector

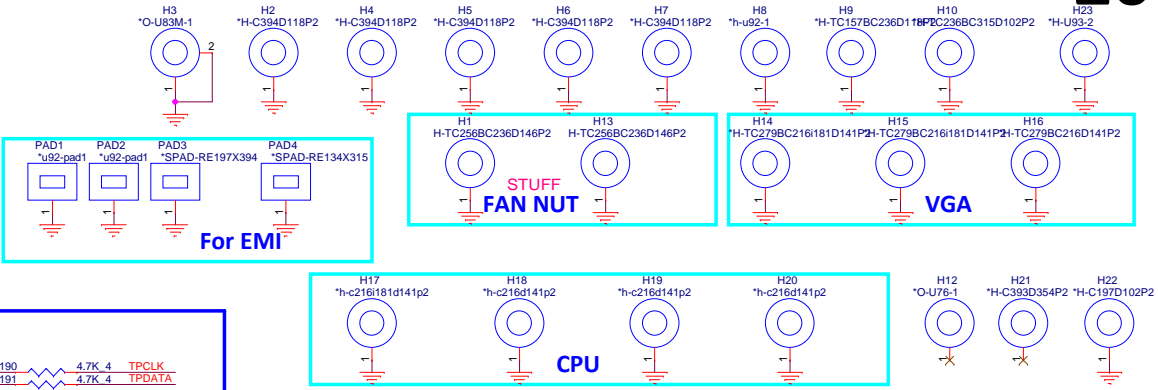
Pin1 : +3VPCU(LIDSWITCH PWR)
 Pin2 : POWER LED
 Pin3 : LIDSWITCH
 Pin4 : GND
 Pin5 : GND
 Pin6 : POWERON#



CPU FAN

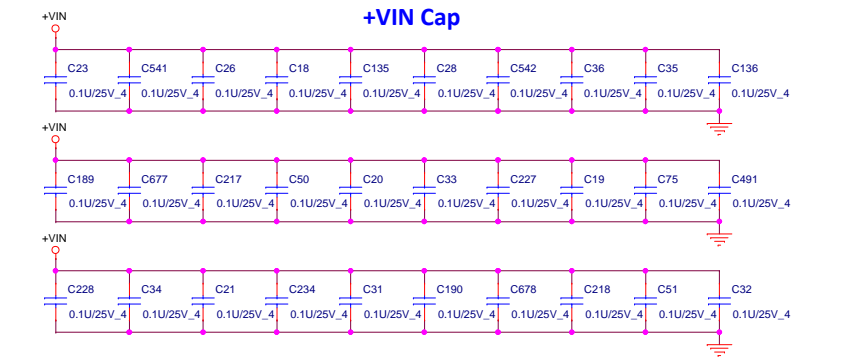
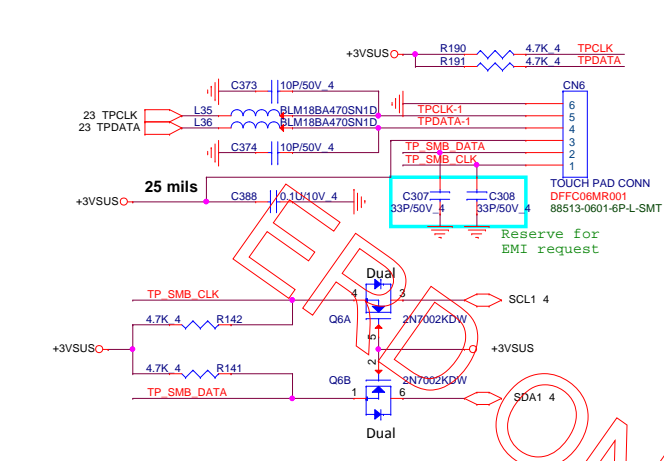
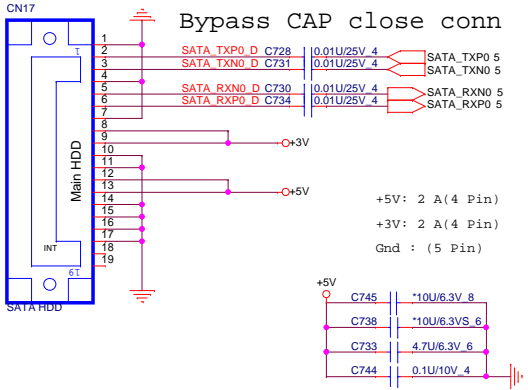


Hole



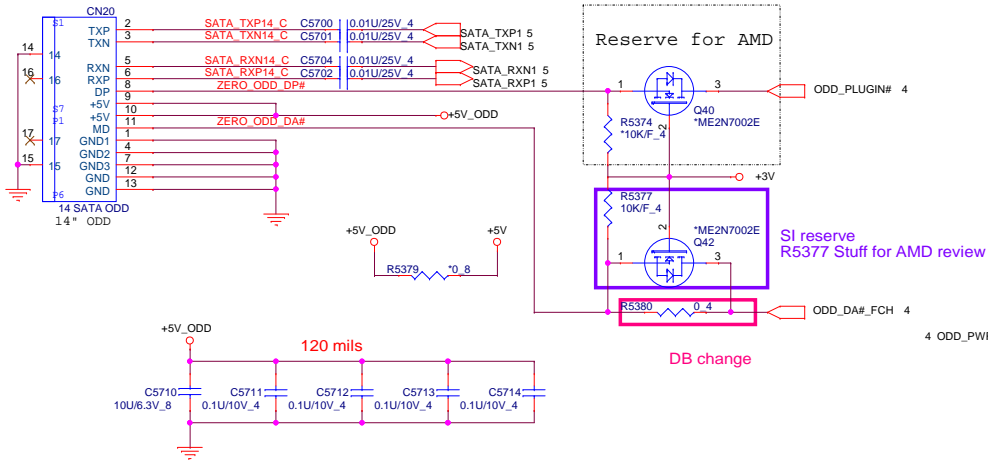
SATA HDD Connector(Cable type)

Bypass CAP close conn



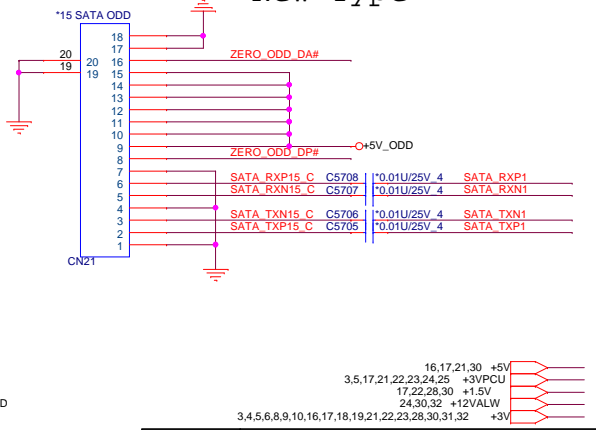
SATA ODD CONNECTOR

14" SATA ODD Bypass CAP close conn



15" SATA ODD

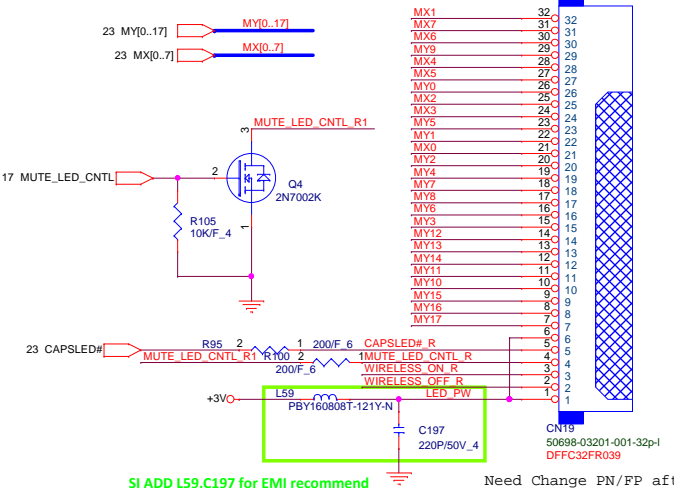
New Type



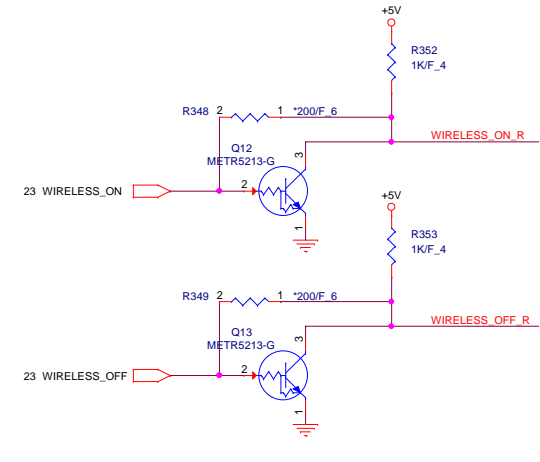
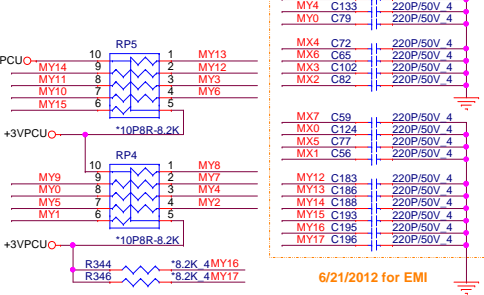
PROJECT :U93
 Quanta Computer Inc.

Size Custom	Document Number SATA HDD/ODD/MSATA CONN	Rev 1A
Date: Monday, May 27, 2013	Sheet 20 of	32

KEYBOARD Con.



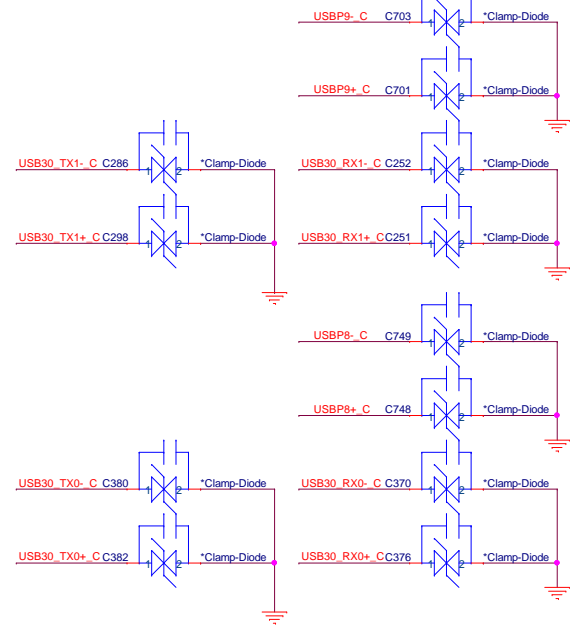
KEYBOARD PULL-UP



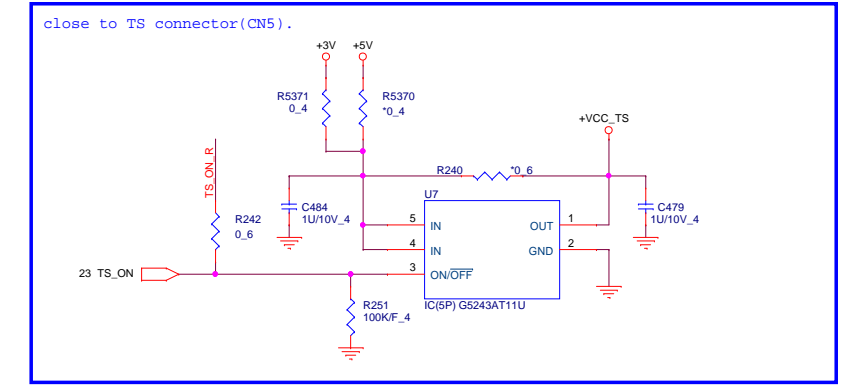
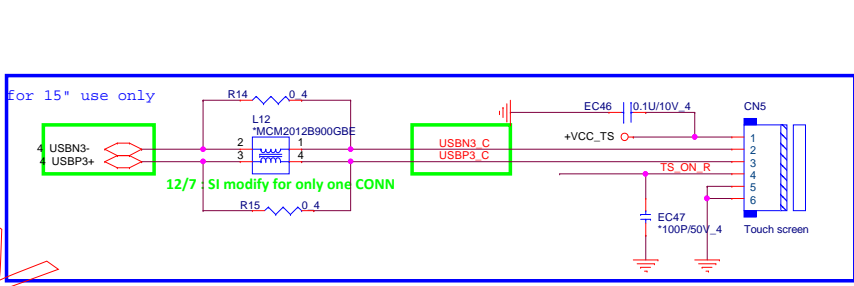
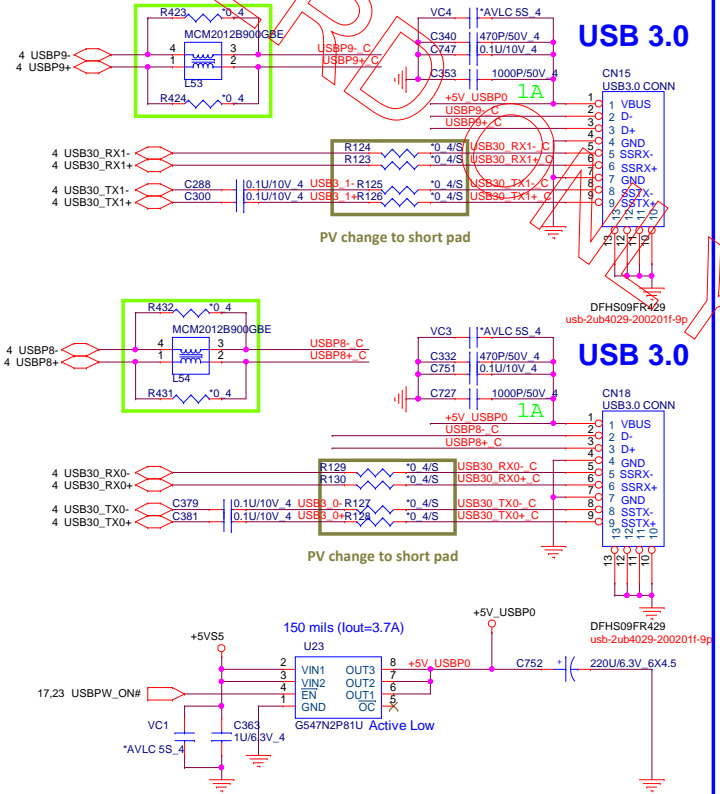
SI ADD L59,C197 for EMI recommend
 Need Change PN/FP after DB

NM9 Type

USB 2.0/3.0 Combo

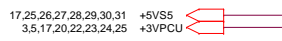


SPS Type

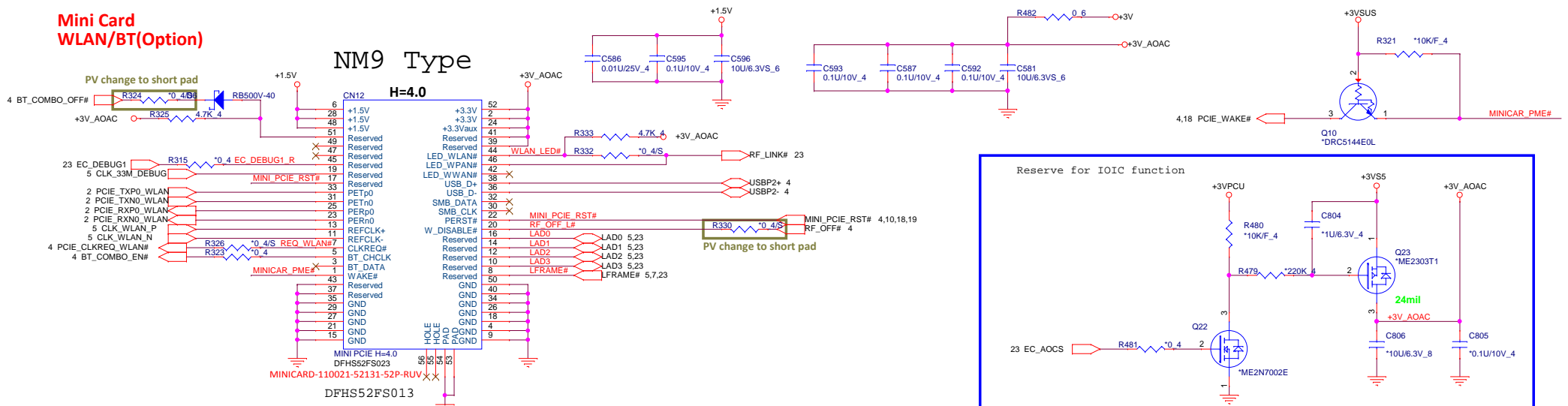


PROJECT :U93
 Quanta Computer Inc.

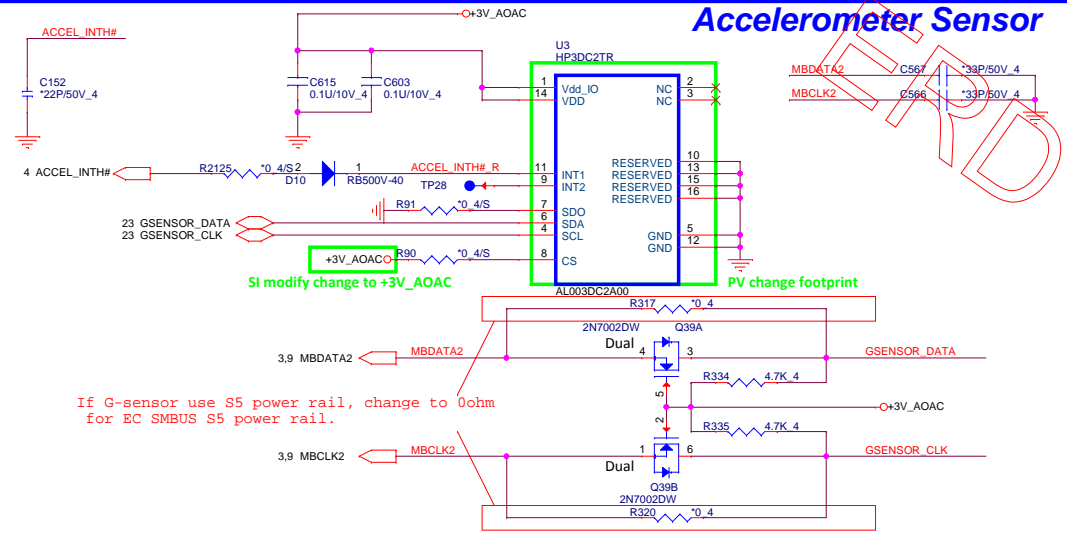
Size Custom	Document Number USB 3.0/KB/Green CLK	Rev 1A
Date: Monday, June 03, 2013	Sheet 21 of 32	



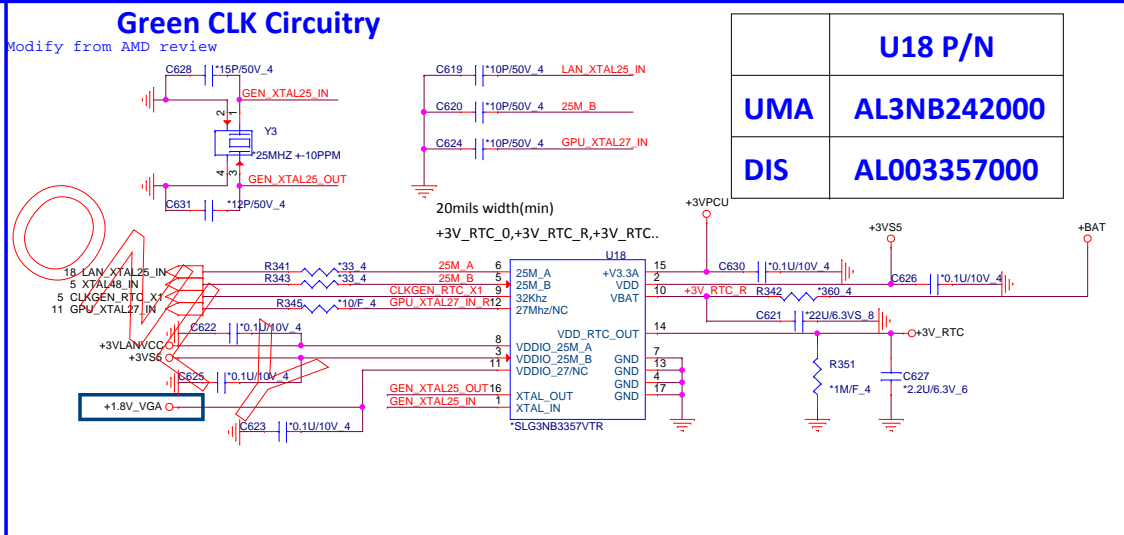
Mini Card WLAN/BT(Optional)



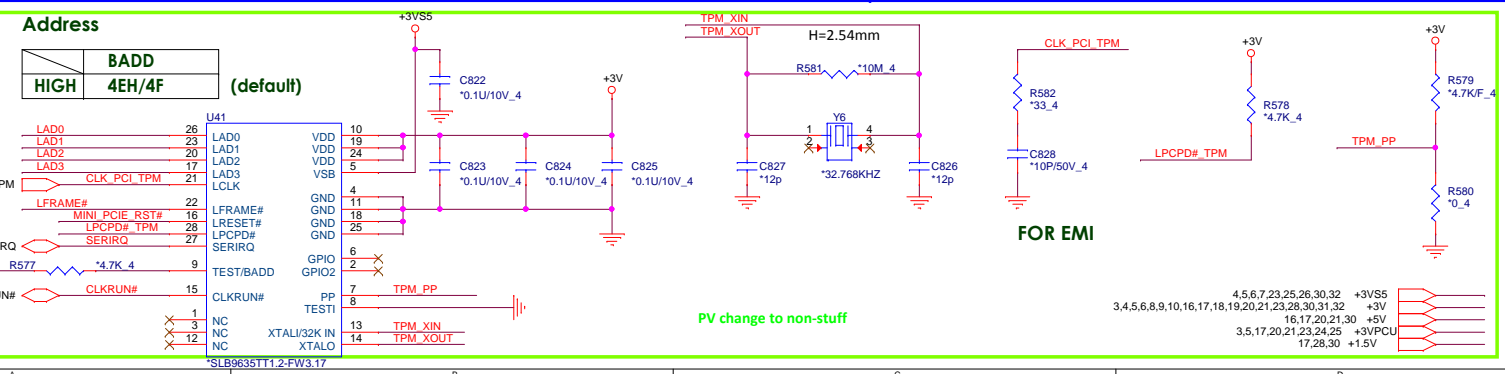
Accelerometer Sensor



Green CLK Circuitry



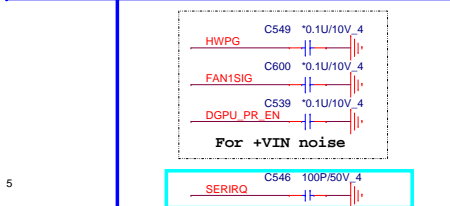
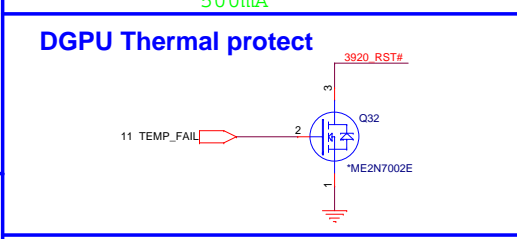
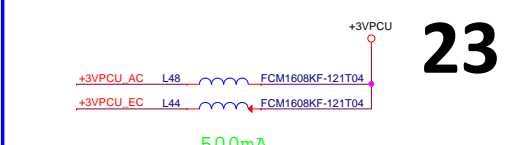
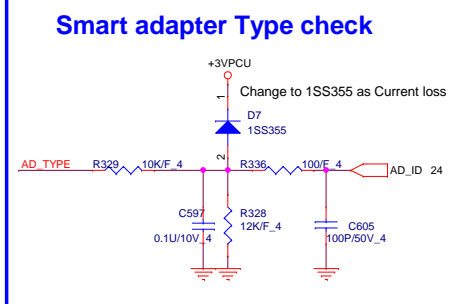
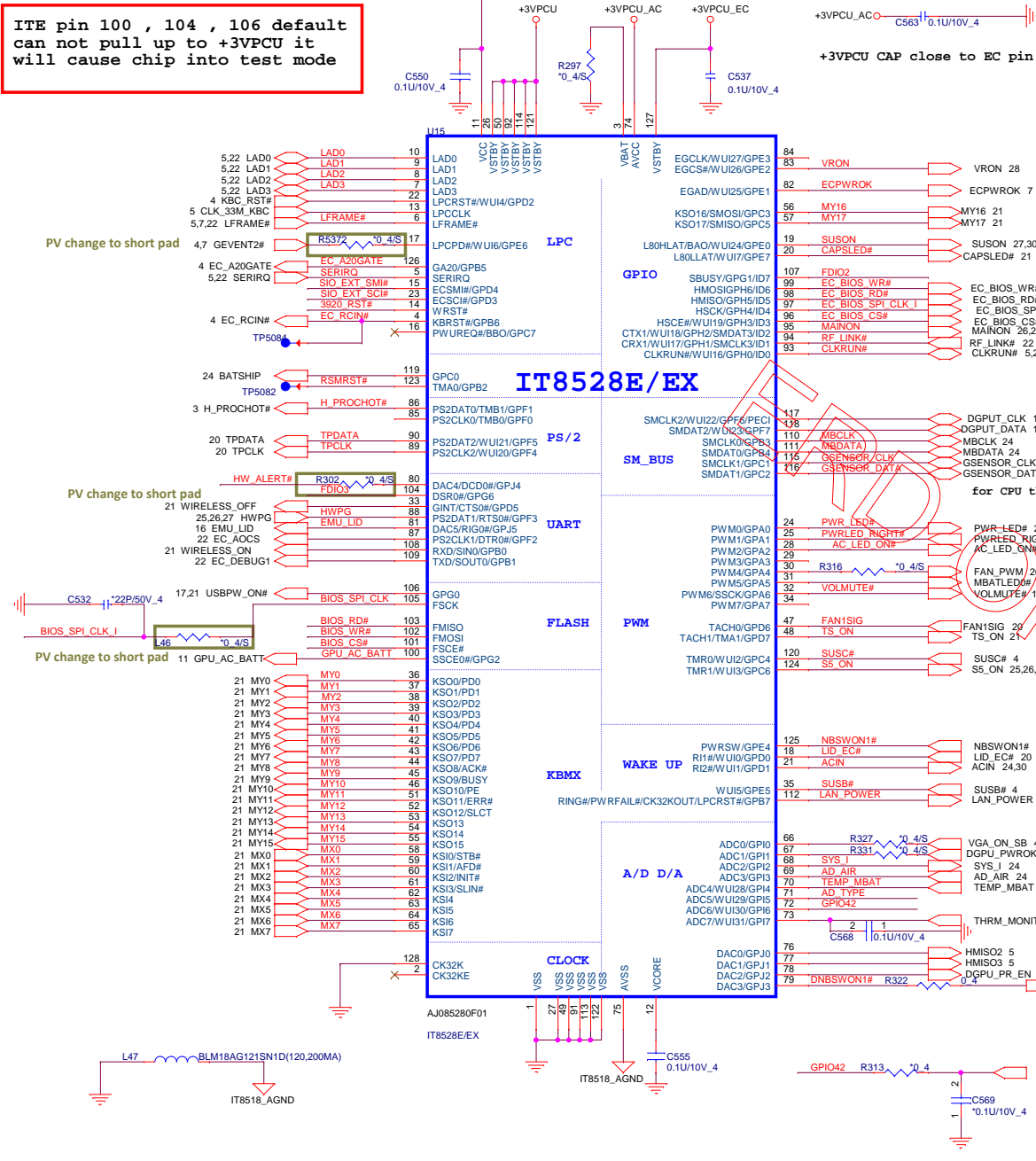
TPM (1.2)



PROJECT :U93		
Quanta Computer Inc.		
Size	Document Number	Rev
Custom	MINI-PCIE/LED	1A
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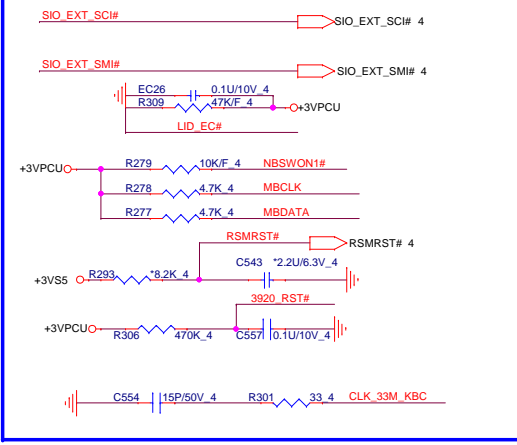
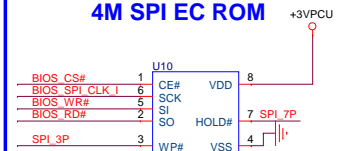


ITE pin 100, 104, 106 default can not pull up to +3VPCU it will cause chip into test mode

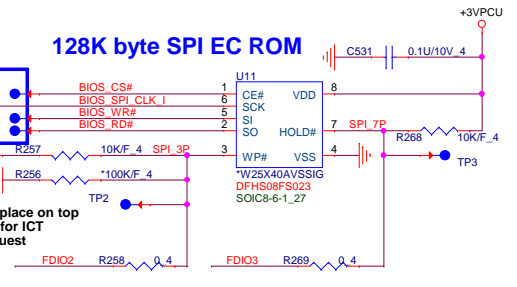
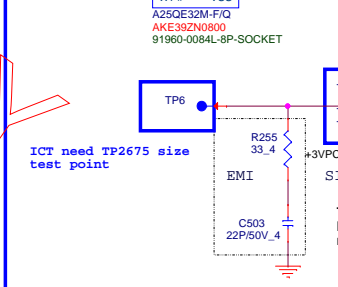


Vender	Size	P/N
AIT	4M	AKE39ZN0800
EON	4M	AKE39ZN0Q03
WND	4M	AKE39FN0N01
Socket		DFHS08FS023

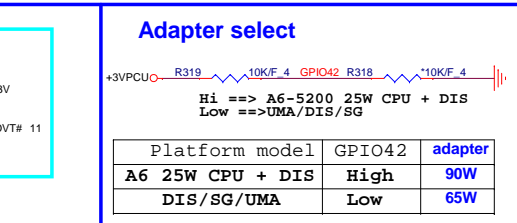
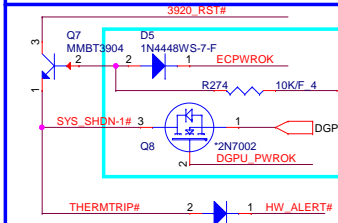
For GPU thermal for Battery charge/discharge



for CPU thermal & G sensor



from power button

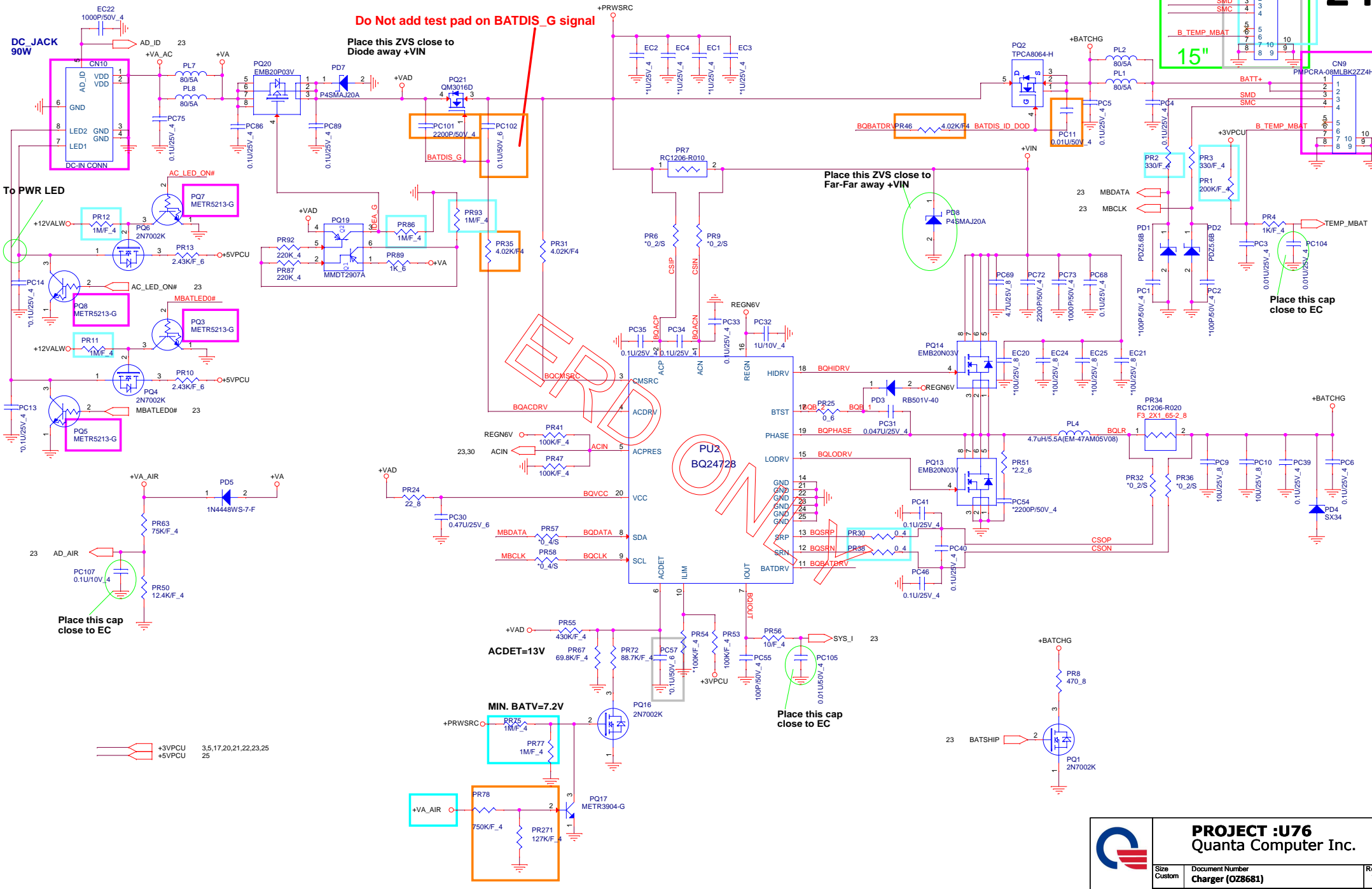


Platform model	GPIO42	adapter
A6 25W CPU + DIS	High	90W
DIS/SG/UMA	Low	65W

ADD VGA TEMP_FAIL function is active Hi

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Do Not add test pad on BATDIS_G signal

Place this ZVS close to Diode away +VIN

Place this ZVS close to Far-Far away +VIN

Place this cap close to EC

Place this cap close to EC

Place this cap close to EC

+3VPCU 3,5,17,20,21,22,23,25
 +5VPCU 25

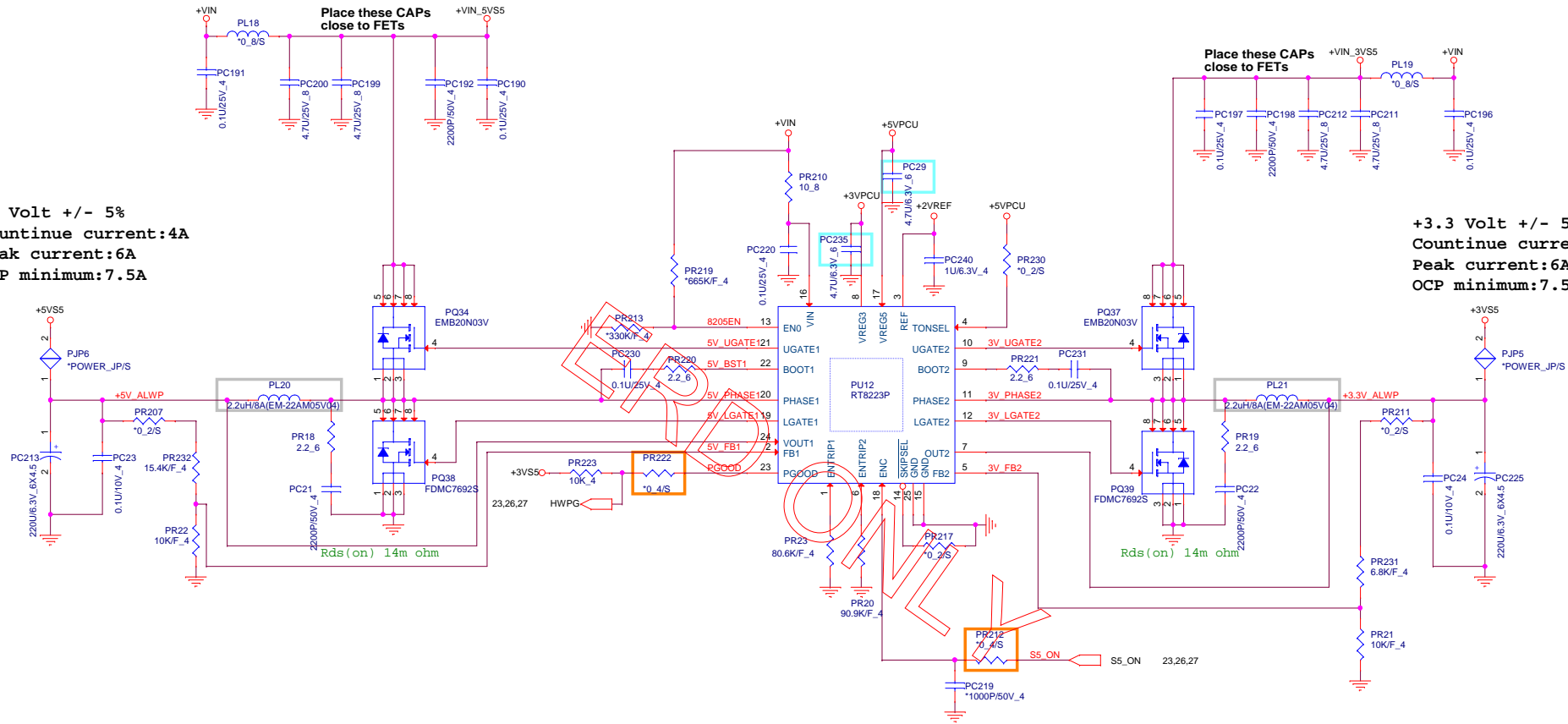



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 Quanta Computer Inc.

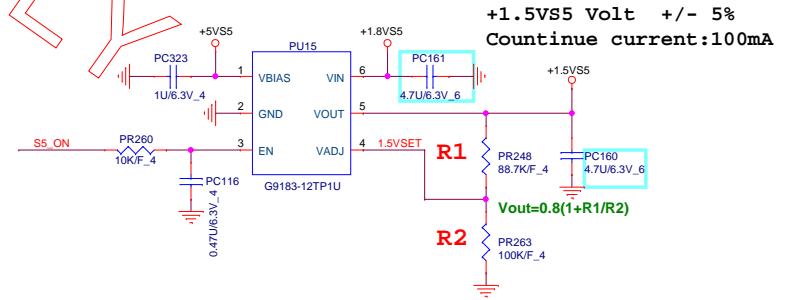
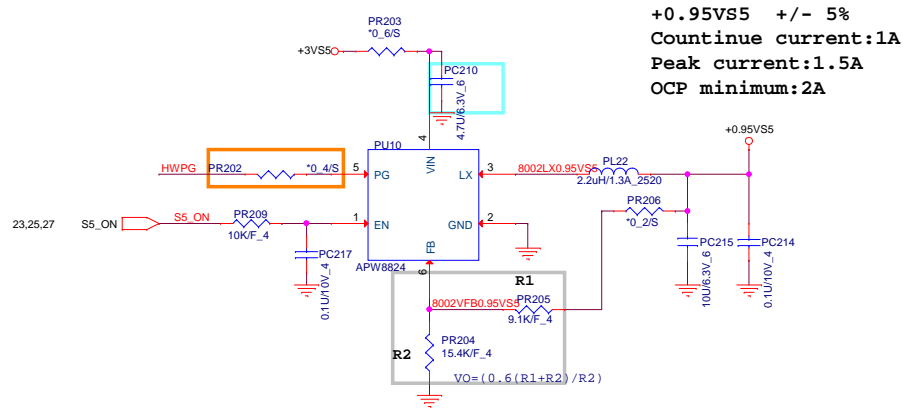
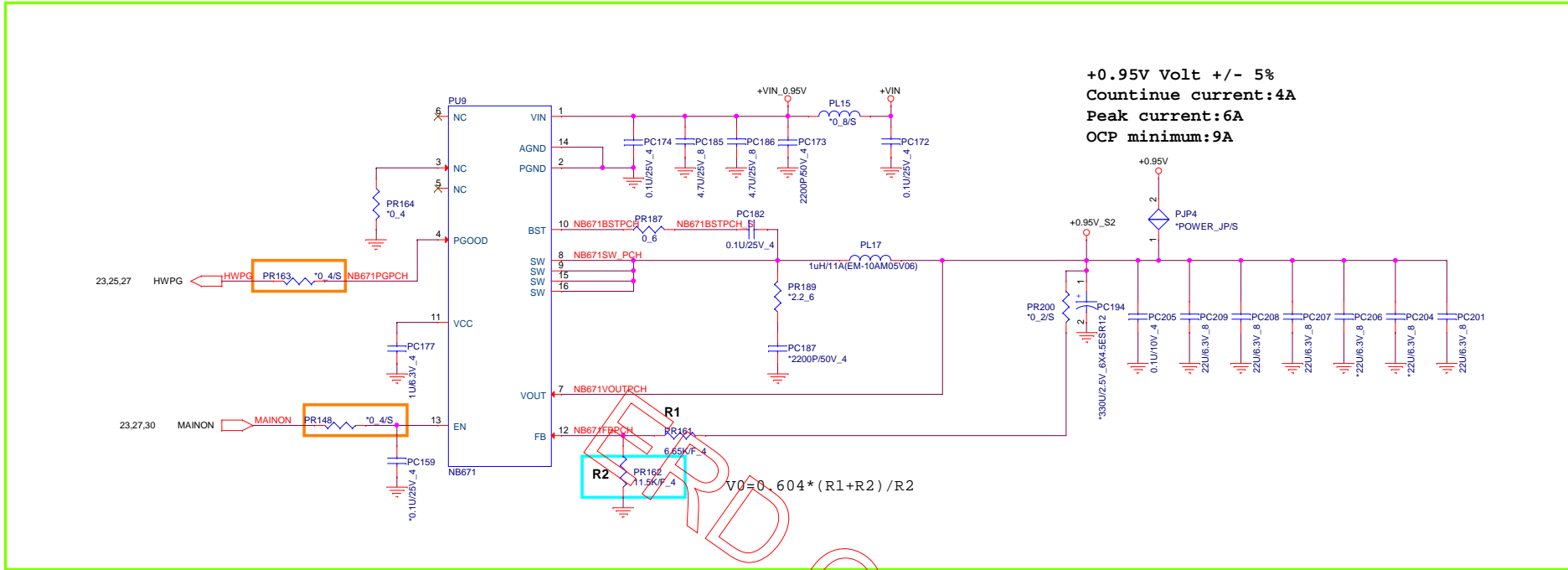
Size Custom	Document Number Charger (028681)	Rev 1A
Date: Monday, May 27, 2013	Sheet 24	of 32

+5 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

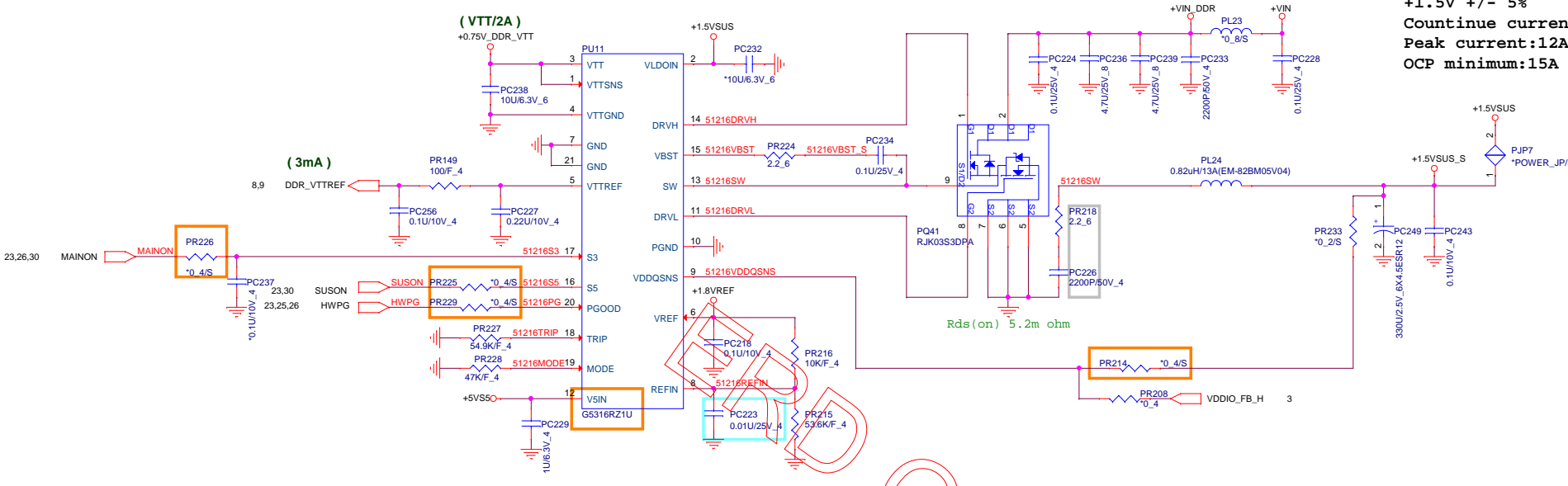


	PROJECT :U76 Quanta Computer Inc.		
	Size Custom	Document Number 3/5VPCU(RT8223P)	Rev 1A
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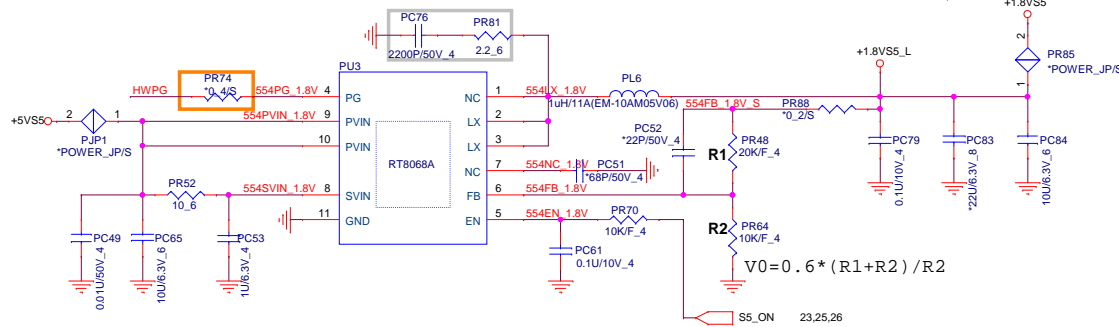
+1.5VSUS 2.6,8,9,30,32

+1.5V +/- 5%
Countinue current:10A
Peak current:12A
OCp minimum:15A




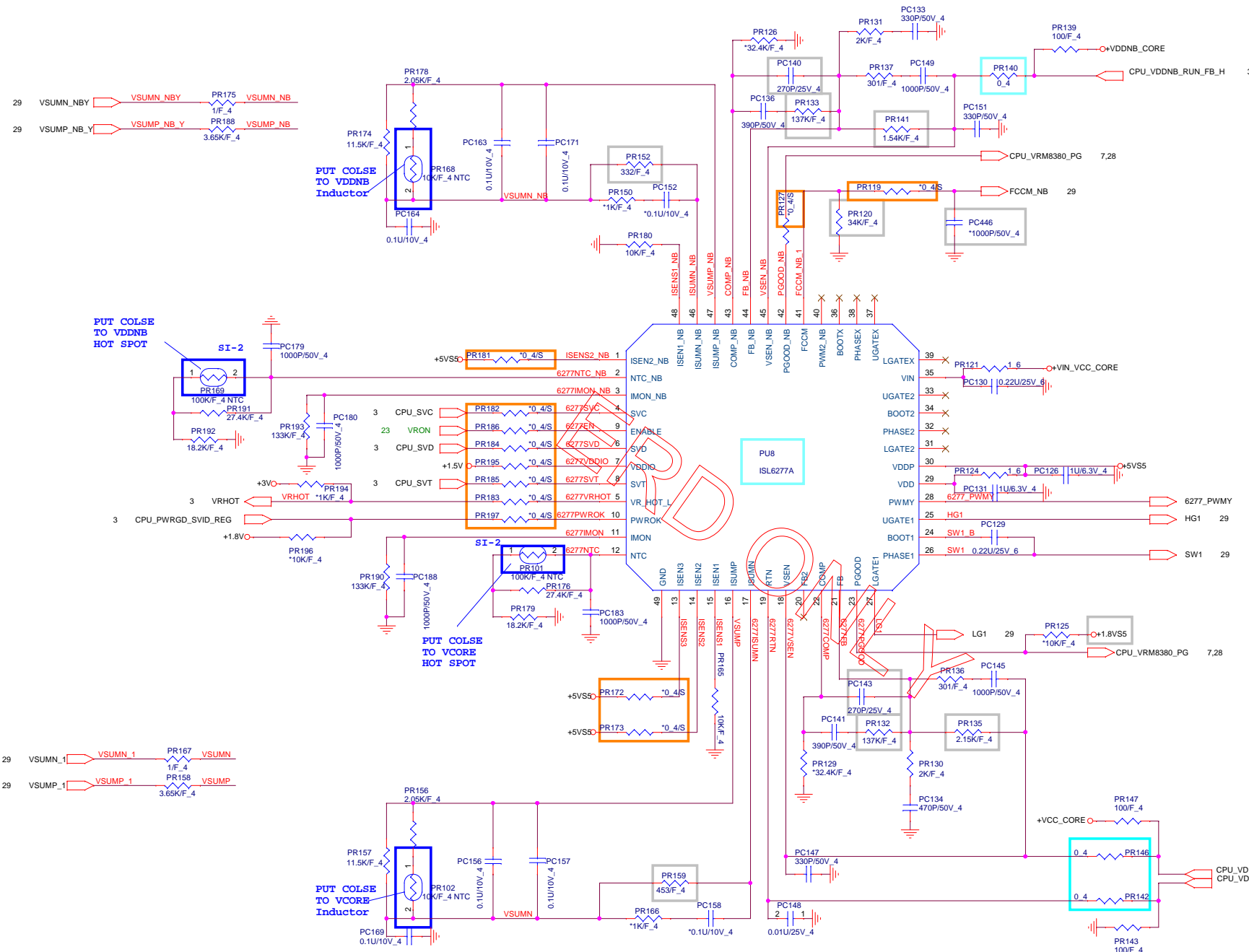
ONLY

1.8V +/- 3%
Countinue current:2A
Peak current:3A
OCp minimum:4A



$$V0 = 0.6 * (R1 + R2) / R2$$

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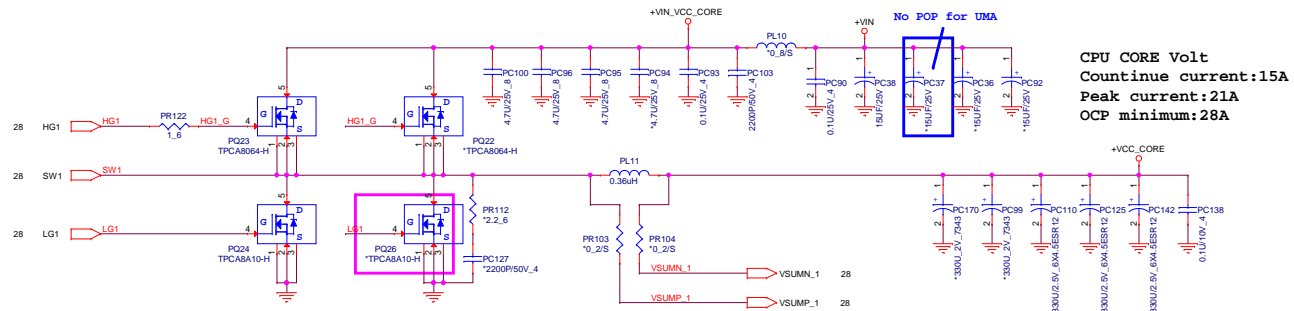
PUT COLSE TO VDDNB HOT SPOT

PUT COLSE TO VDDNB Inductor

PUT COLSE TO VCORE HOT SPOT

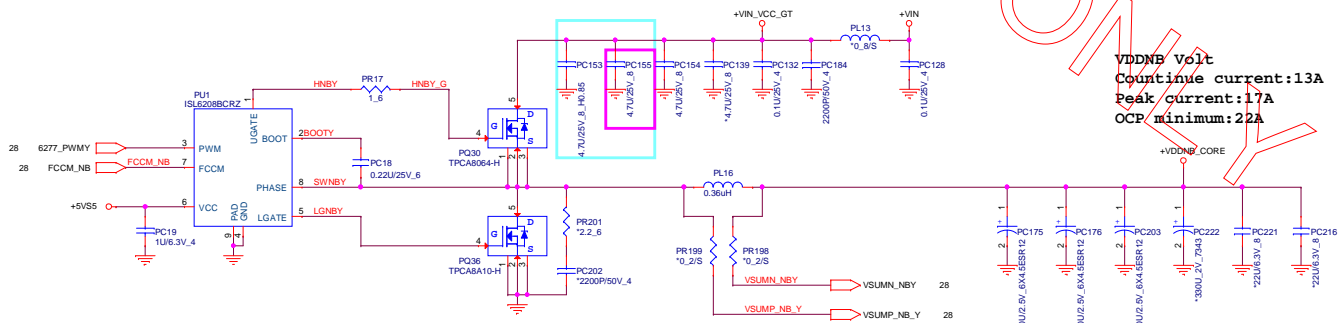
PUT COLSE TO VCORE Inductor

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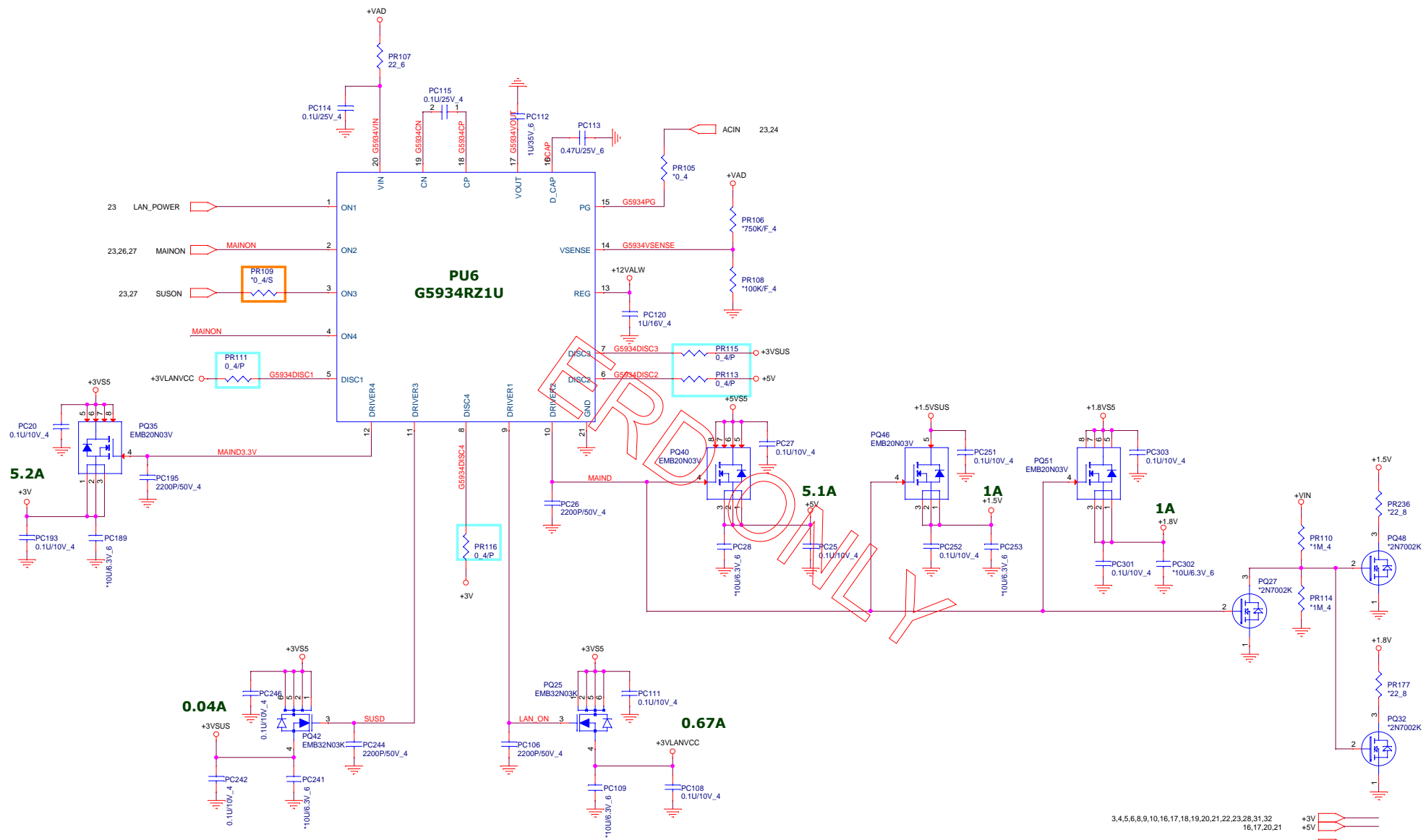


CPU CORE Volt
 Countinue current:15A
 Peak current:21A
 OCP minimum:28A


ERD ONLY



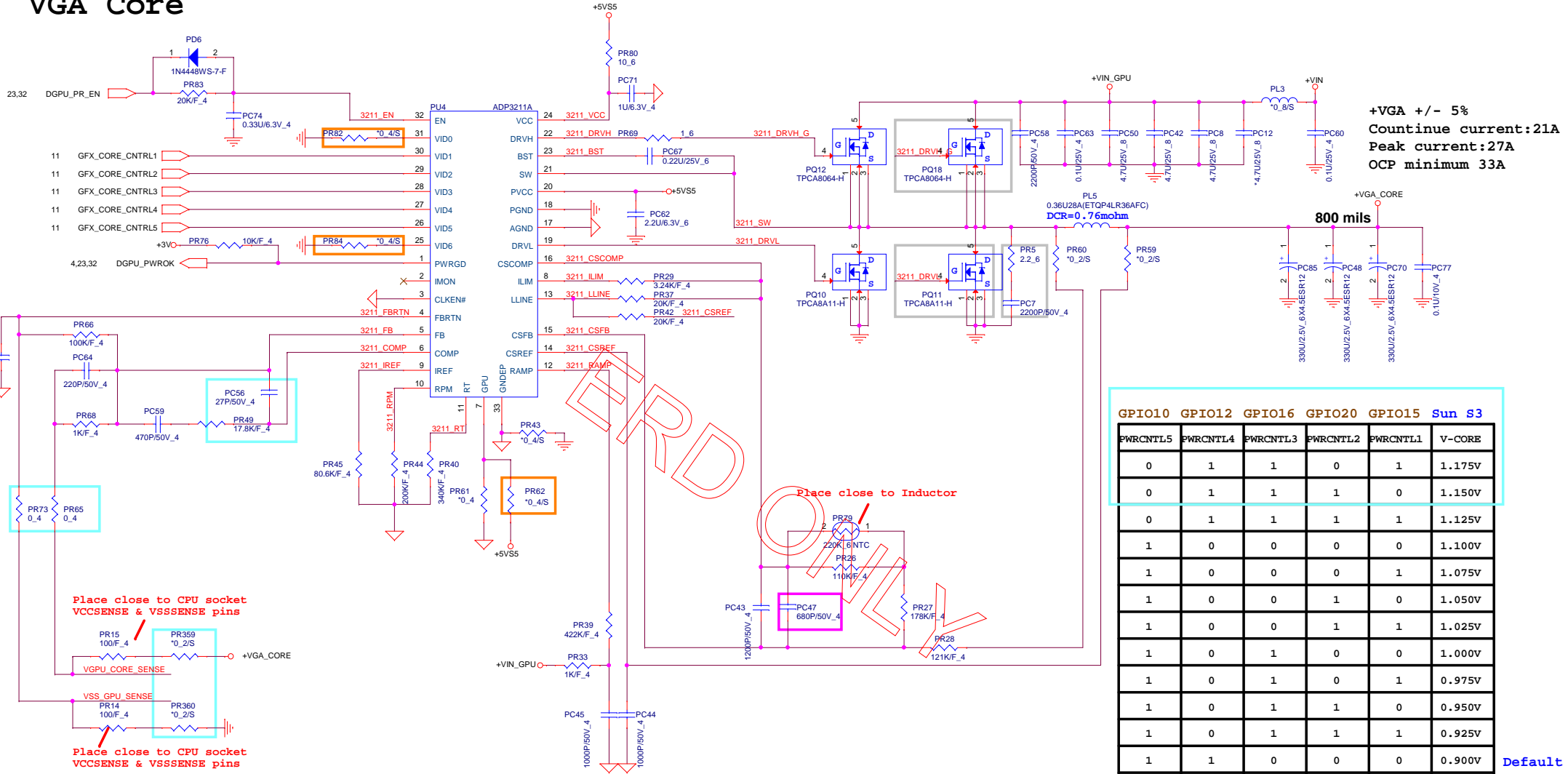
VDDNB Volt
 Countinue current:13A
 Peak current:17A
 OCP minimum:22A



- 3,4,5,6,8,9,10,16,17,18,19,20,21,22,23,28,31,32 +3V
- 16,17,20,21 +5V
- 16,20,24,25,26,27,29,31,32 +VIN
- 4,5,6,7,22,23,25,26,32 +3VS5
- 17,21,25,26,27,28,29,31 +5VS5
- 24,32 +12VALW
- 18,22 +3VLANVCC
- 8,9,27 +0.75V_DDR_VTT

	PROJECT :U76	
	Quanta Computer Inc.	
Size Custom	Document Number Dis-charge IC (SLG55448V)	Rev 1A
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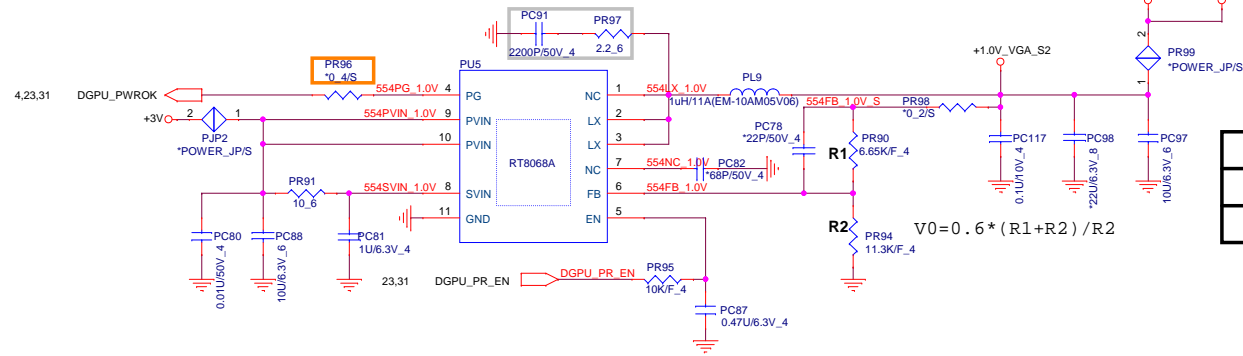
VGA Core



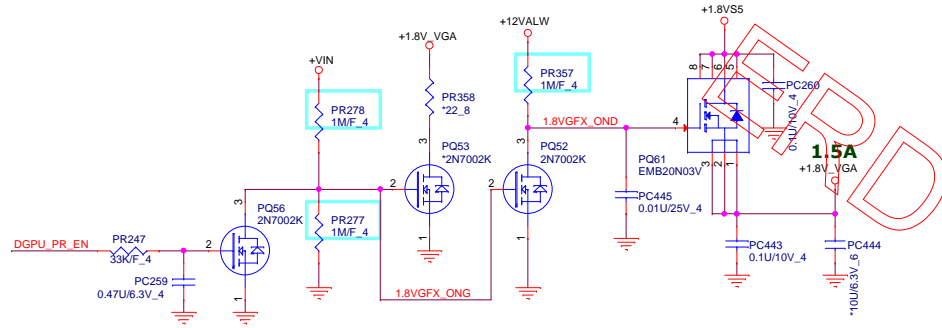
PROJECT :U76
Quanta Computer Inc.

Size Custom	Document Number +VGA CORE NCP3218G)	Rev 1A
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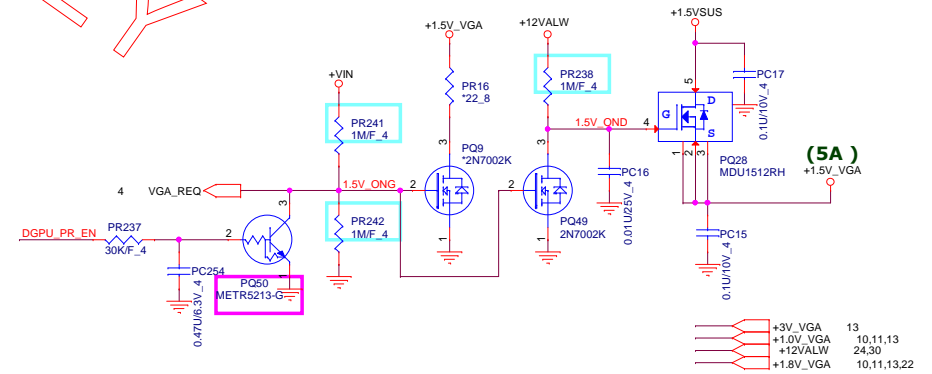
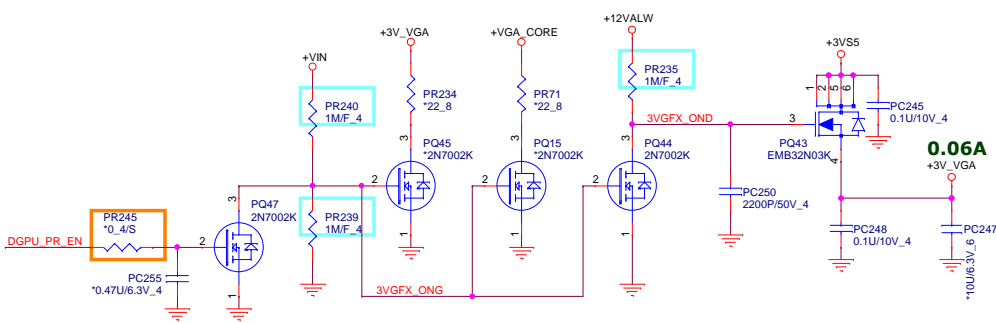
+0.95V +/- 3%
 Countinue current:2A
 Peak current:3A
 OCP minimum:4A



R2 Value	P/N	1.0V_VGA
10K	CS31002FB26	1.0V
11.3K	CS31132FB07	0.95V



PROTOTYPE ONLY



- +3V_VGA 13
- +1.0V_VGA 10,11,13
- +12VALW 24,30
- +1.8V_VGA 10,11,13,22

PROJECT :U76
 Quanta Computer Inc.

Size Custom	Document Number +VGA POWER	Rev 1A
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