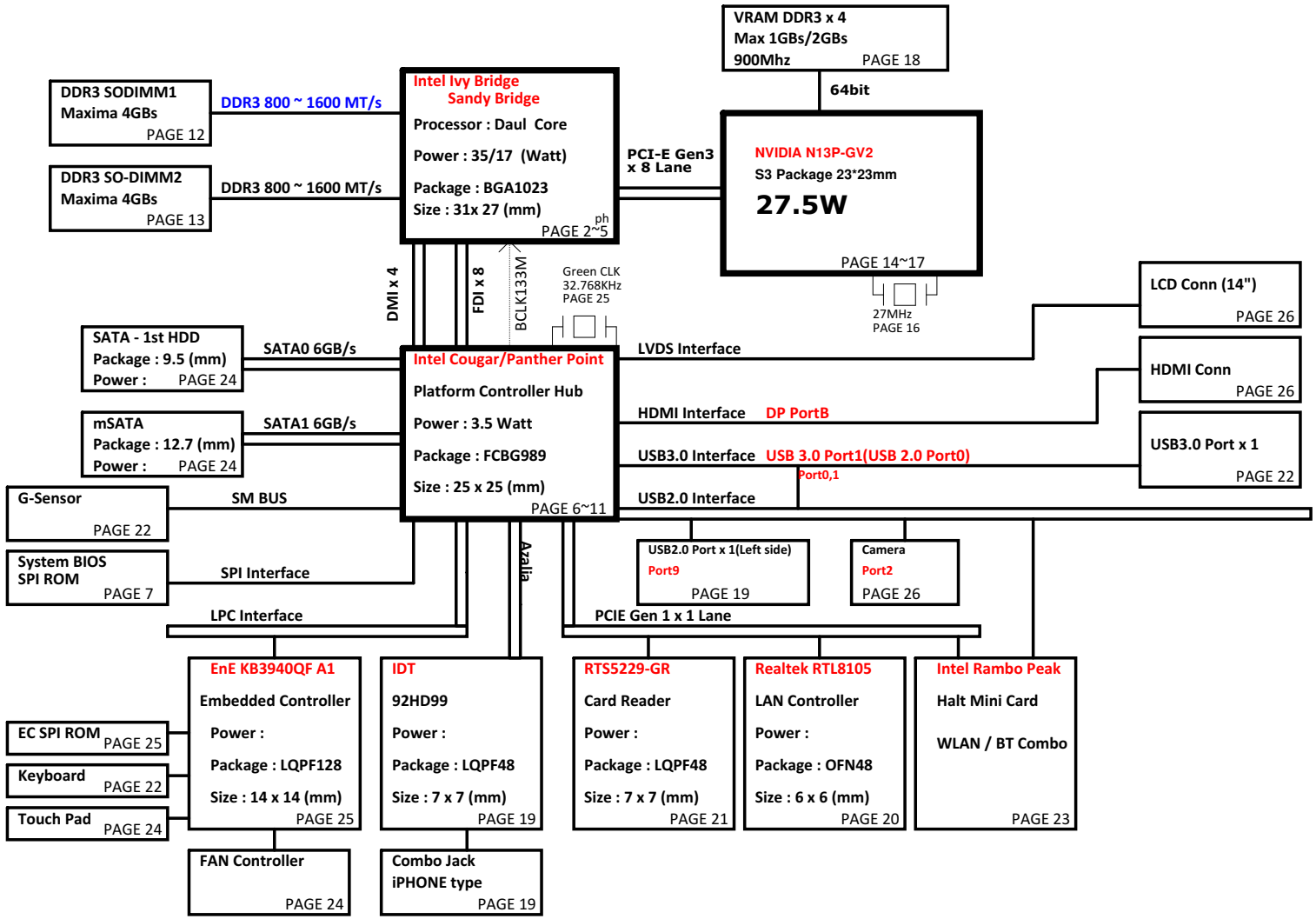
Volks DIS/UMA (14"/15.6") Ultra/Slim
Intel Chief River Platform Block Diagram

01



PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT

Power Source

BQ24738
System Charge Power (+BATCHG)

Ricktek RT8223P
System Power (+3VPCU/+5VPCU/ +3VS5/+5VS5)

NCP6132/NCP5911/RT8240P/ TPS51462RGER
Processor Power (+VCC_CORE/ +1.05_VTT/+VCCSA)

SLG55448V
System Discharge Power (+1.5V/+3V/+5V)

Richtek RT8207
System Memory Power (+1.5VSUS/ +0.75V_DDR_VTT)

NCP3218G
GPU core power(+VGACORE)

NB5

PROJECT : VOLKS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	1A

Date: Wednesday, May 23, 2012 Sheet 1 of 37

Ivy Bridge Processor (DMI,PEG,FDI)

02

PEG_COMP connect to PIN G3&G4 W:4mils/S:15mils/L: 60mils.
PEG_COMP connect to PIN G1 W:12mils/S:15mils/L: 500mils.

U20A

DMI
Intel(R) FDI
PCI EXPRESS -- GRAPHICS
eDP

IC,IVB_2CBGA,0P7

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

PEG x8

CPU RESET#

SM_DRAMPWROK Processor Input.

DDR3 DRAM RESET

for DS3

Processor pull-up (CPU)

Placement close to EC.

CPU XDP

SM_RCOMP[0] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[1] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[2] W:15mils/S:20mils/L: 500mils,

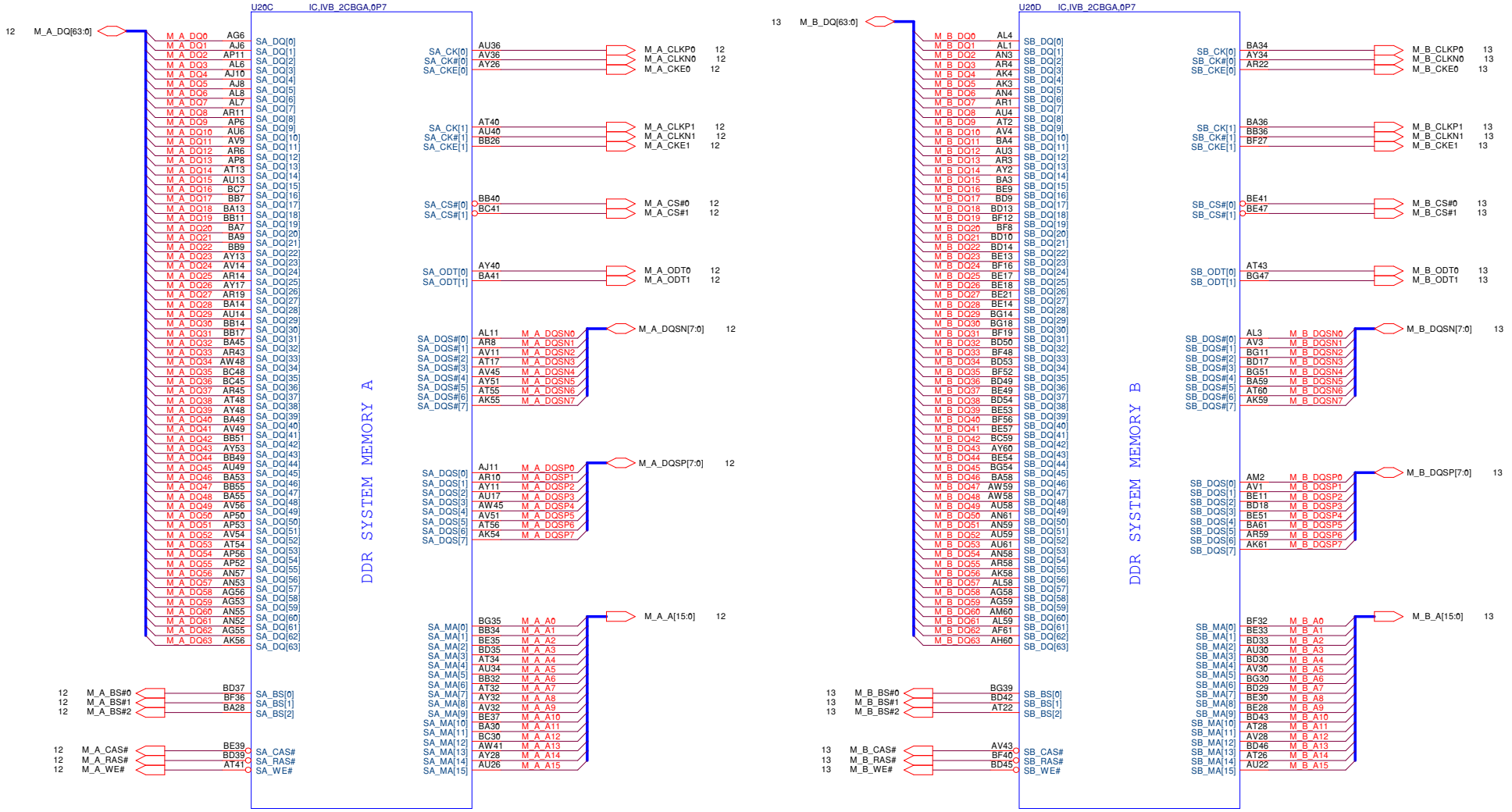
For iFDIM Trigger Point

Connect a Test Point on BPM# 6 signal, very close to processor.

Connect a Test Point on BPM# 7 signal, very close to processor.

PROJECT :	VOLKS
	Quanta Computer Inc.
NB5	Size: Custom; Document Number: Processor 1/4 (Host/GPU); Rev: 1A
	Date: Wednesday, May 23, 2012; Sheet 2 of 37

Ivy Bridge Processor (DDR3)



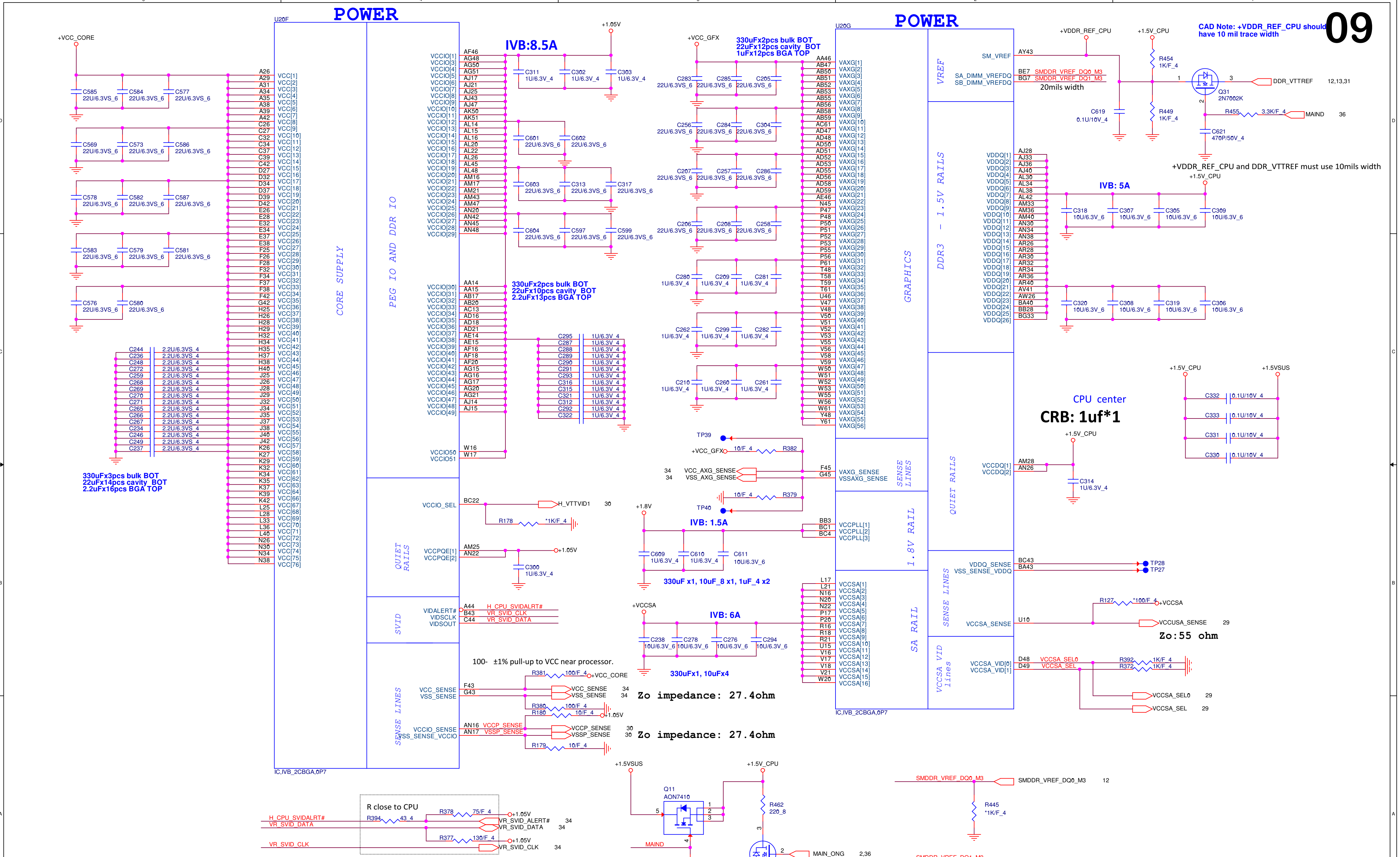
NB5

PROJECT : VOLKS

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Processor 2/5 (DDR3 I/F)	1A

Date: Wednesday, May 23, 2012 Sheet 3 of 37



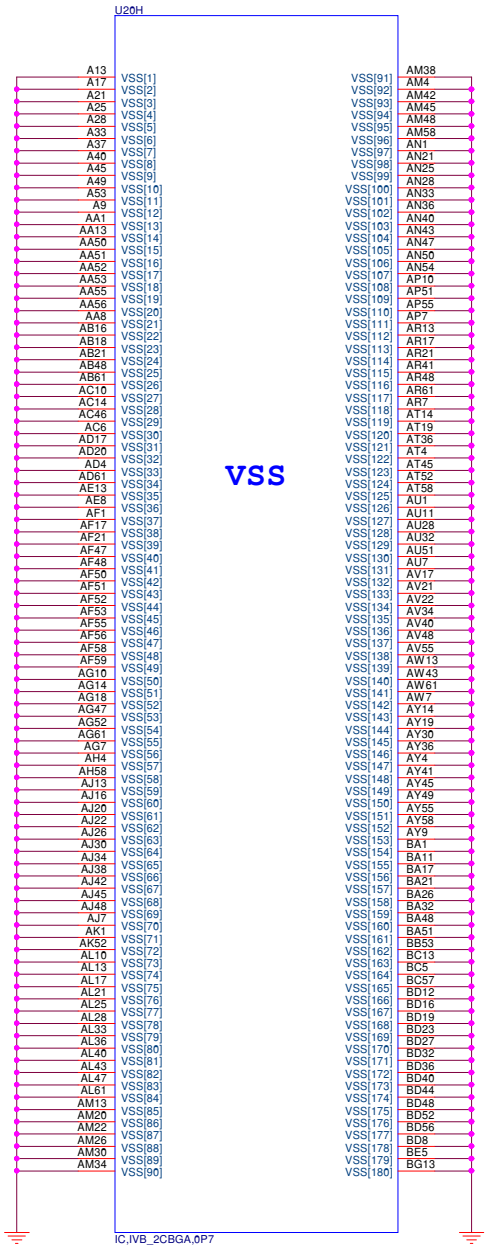
PROJECT : VOLKS

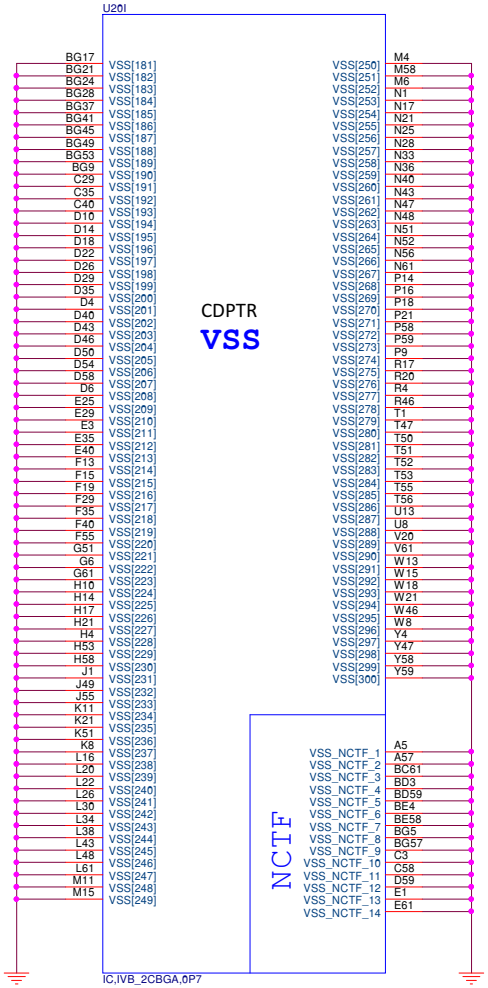
Quanta Computer Inc.

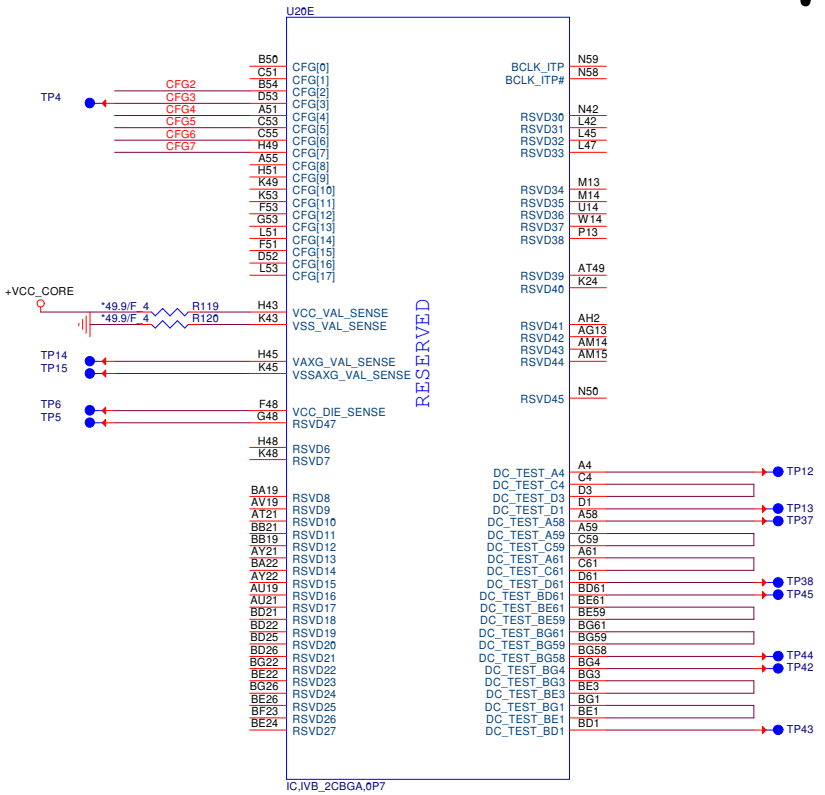
NB5

Size	Document Number	Rev
Custom	Processor 3/4 (POWER)	1A

Date: Wednesday, May 23, 2012 Sheet 4 of 37







CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Processor Strapping

The CFG signals have a default value of '1' if noterminated on the board.

	1	0
CFG2 (PCIe Static x16 Lane Numbering Reversal.)	Normal Operation(Default)	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

NB5

PROJECT : VOLKS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Processor 4/4 (RSV,Ground)	1A

Date: Wednesday, May 23, 2012 | Sheet 5 of 37

Cougar Point/Panther Point (DMI,FDI,PM)

Cougar Point/Panther Point (LVDS,DDI)

06

U18C
CPT_PPT_Rev_0p7

U18D
CPT_PPT_Rev_0p7

PCH Pull-high/low(CLG)

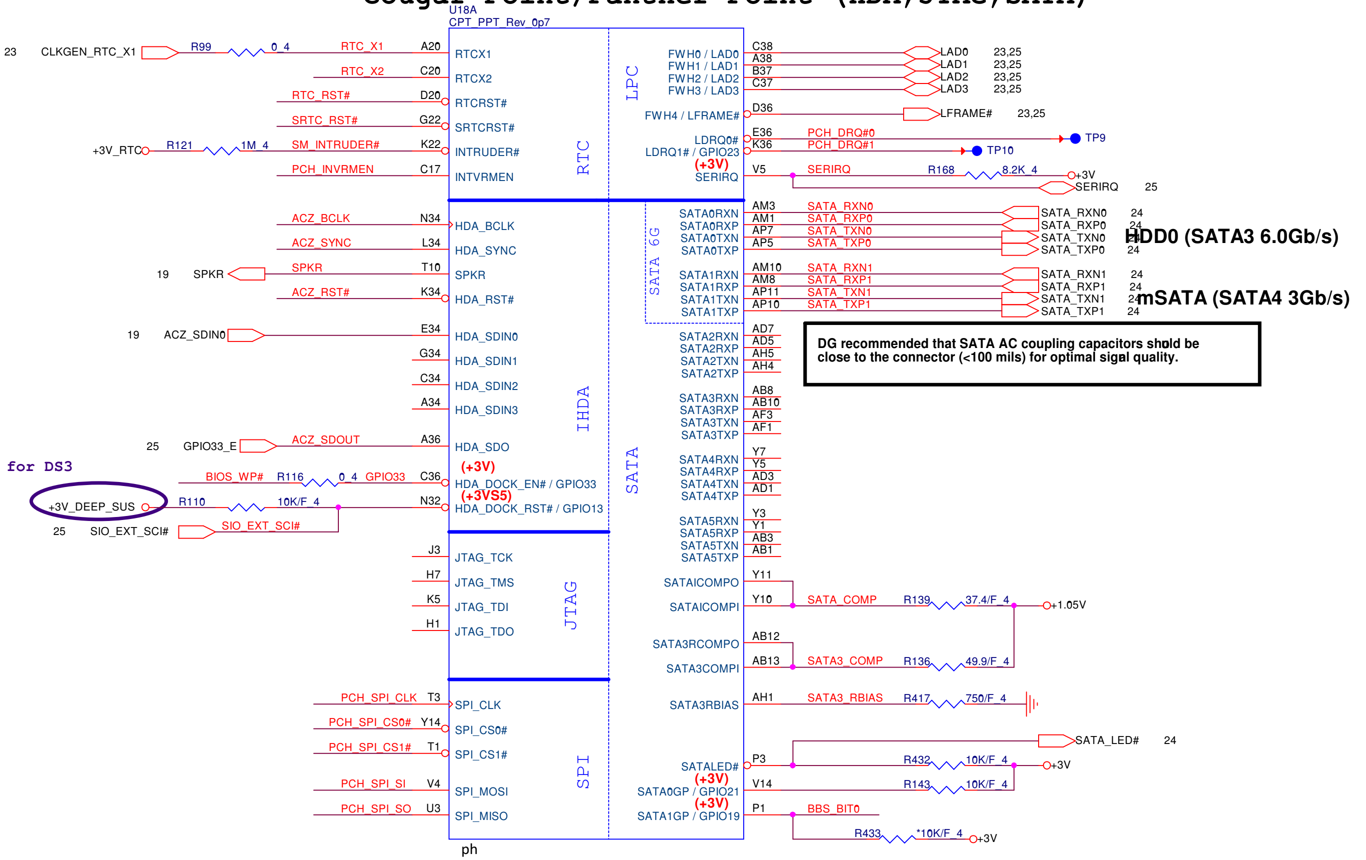
for DS3

System PWR_OK(CLG)

On Die DSW VR Enable
High = Enable (Default)
Low = Disable

PROJECT : VOLKS
Quanta Computer Inc.
NB5
Size: Custom | Document Number: PCH 1/6 (Host/Display) | Rev: 1A
Date: Wednesday, May 23, 2012 | Sheet 6 of 37

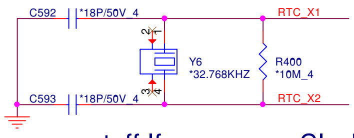
Cougar Point/Panther Point (HDA,JTAG,SATA)



U18A
CPT_PPT_Rev_0p7
23 CLKGEN_RTC_X1 R99 0_4 RTC_X1 A20 RTCX1
RTC_X2 C20 RTCX2
RTC_RST# D20 RTCRST#
SRTC_RST# G22 SRTCRST#
+3V_RTC R121 1M_4 SM_INTRUDER# K22 INTRUDER#
PCH_INVRMEN C17 INTVRMEN
RTC
ACZ_BCLK N34 HDA_BCLK
ACZ_SYNC L34 HDA_SYNC
19 SPKR SPKR T10 SPKR
ACZ_RST# K34 HDA_RST#
19 ACZ_SDIN0 E34 HDA_SDIN0
G34 HDA_SDIN1
C34 HDA_SDIN2
A34 HDA_SDIN3
25 GPIO33_E ACZ_SDOUT A36 HDA_SDO
for DS3
BIOS_WP# R116 0_4 GPIO33 C36 (+3V) HDA_DOCK_EN# / GPIO33
+3V_DEEP_SUS R110 10K/F_4 N32 (+3VS5) HDA_DOCK_RST# / GPIO13
25 SIO_EXT_SCI# SIO_EXT_SCI#
IHDA
J3 JTAG_TCK
H7 JTAG_TMS
K5 JTAG_TDI
H1 JTAG_TDO
JTAG
PCH_SPI_CLK T3 SPI_CLK
PCH_SPI_CS0# Y14 SPI_CS0#
PCH_SPI_CS1# T1 SPI_CS1#
PCH_SPI_SI V4 SPI_MOSI
PCH_SPI_SO U3 SPI_MISO
SPI
ph
LPC
FWH0 / LAD0 C38 LAD0 23,25
FWH1 / LAD1 A38 LAD1 23,25
FWH2 / LAD2 B37 LAD2 23,25
FWH3 / LAD3 C37 LAD3 23,25
FWH4 / LFRAME# D36 LFRAME# 23,25
LDRQ0# E36 PCH_DRQ#0 TP9
LDRQ1# / GPIO23 K36 PCH_DRQ#1 TP10
(+3V) SERIRQ V5 SERIRQ R168 8.2K_4 +3V
SERIRQ 25
SATA 6G
SATA0RXN AM3 SATA_RXN0 SATA_RXN0 24
SATA0RXP AM1 SATA_RXP0 SATA_RXP0 24
SATA0TXN AP7 SATA_TXN0 SATA_TXN0 24
SATA0TXP AP5 SATA_TXP0 SATA_TXP0 24
HDD0 (SATA3 6.0Gb/s)
SATA1RXN AM10 SATA_RXN1 SATA_RXN1 24
SATA1RXP AM8 SATA_RXP1 SATA_RXP1 24
SATA1TXN AP11 SATA_TXN1 SATA_TXN1 24
SATA1TXP AP10 SATA_TXP1 SATA_TXP1 24
mSATA (SATA4 3Gb/s)
SATA2RXN AD7
SATA2RXP AD5
SATA2TXN AH5
SATA2TXP AH4
DG recommended that SATA AC coupling capacitors shold be close to the connector (<100 mils) for optimal sigal quality.
SATA3RXN AB8
SATA3RXP AB10
SATA3TXN AF3
SATA3TXP AF1
SATA4RXN Y7
SATA4RXP Y5
SATA4TXN AD3
SATA4TXP AD1
SATA5RXN Y3
SATA5RXP Y1
SATA5TXN AB3
SATA5TXP AB1
SATA
SATAICOMPO Y11
SATAICOMPI Y10 SATA_COMP R139 37.4/F_4 +1.05V
SATA3RCOMPO AB12
SATA3COMPI AB13 SATA3_COMP R136 49.9/F_4
SATA3RBIAS AH1 SATA3_RBIAS R417 750/F_4
SATA_LED# 24
SATALED# P3 R432 10K/F_4 +3V
(+3V) SATA0GP / GPIO21 V14 R143 10K/F_4
(+3V) SATA1GP / GPIO19 P1 BBS_BIT0
R433 *10K/F_4 +3V

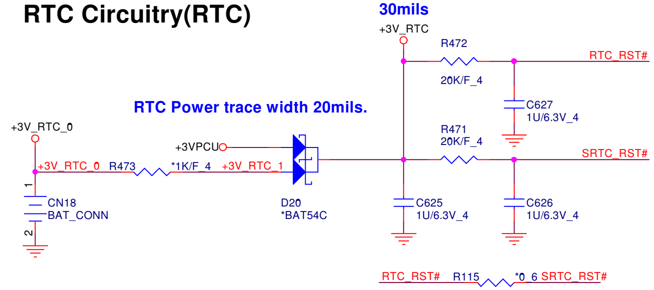
07

RTC Clock 32.768KHz

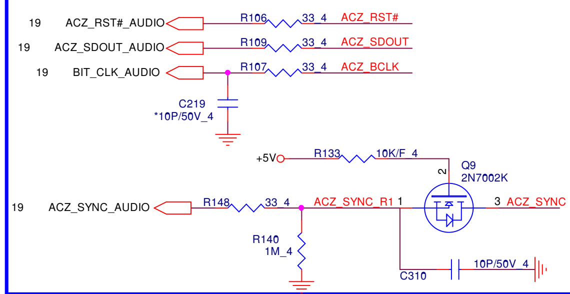


no stuff If use green Clock

RTC Circuitry(RTC)



HDA Bus(CLG)

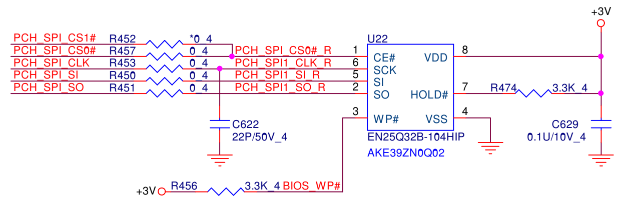


PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V R152 *1K/F_4 SPKR
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R363 *1K/F_4 PCI_GNT3# 8 +3V R364 10K/F_4
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC R122 330K_4 PCH_INVRMEN
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 R104 *1K/F_4 ACZ_SDOUT ACZ_SDOUT 25
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location: 1 / 1 / SPI 0 / 0 / LPC	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1# R419 *1K/F_4 BBS_BIT0 R354 *1K/F_4 BBS_BIT1 8
GPIO19 Different from Calpella	Boot BIOS Selection 0 [bit-0]	PWROK		
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V R416 *1K/F_4 NV_ALE 8
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm	+1.8V R415 2.2K_4 R414 1K/F_4 NV_CLE 9 H_SNB_IVB# 2
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	for DS3 +3V_DEEP_SUS R135 1K/F_4 ACZ_SYNC
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	+3V_DEEP_SUS R105 *1K/F_4 ACZ_SDOUT
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	
GPIO28 Different from Calpella	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	

PCH SPI ROM(CLG)

Vender	Size	P/N
EON	4MB	AKE39ZN0Q02 (EN25Q32B-104HIP)
MX	4MB	AKE39FP0Z02 (MX25L3206EM2I-12G)
AMIC	4MB	AKE39F-0800 (A25LQ32AM-F/Q)
Socket		DFHS08FS023



+3V
PCH_SPI_CS1# R452 *0_4
PCH_SPI_CS0# R457 0_4 PCH_SPI_CS0#_R 1
PCH_SPI_CLK R453 0_4 PCH_SPI1_CLK_R 6
PCH_SPI_SI R450 0_4 PCH_SPI1_SI_R 5
PCH_SPI_SO R451 0_4 PCH_SPI1_SO_R 2
U22
CE# SCK SI SO WP# VDD HOLD# VSS
8 7 3 4
R474 3.3K_4
C622
22P/50V_4
EN25Q32B-104HIP
AKE39ZN0Q02
C629
0.1U/10V_4
+3V R456 3.3K_4 BIOS_WP#

+3V 6,8,9,10,12,13,14,16,19,20,21,22,23,24,25,26,30,32,34,36
+5V 10,19,21,22,23,24,26,36
+1.8V 4,10,31
+1.05V 2,4,6,8,10,21,23,30,33,34
+3VS5 6,10,23,28,30,33,36
+3VPCU 21,22,23,24,25,26,27,28
+3V_RTC 6,10,23

NB5

PROJECT : VOLKS
Quanta Computer Inc.

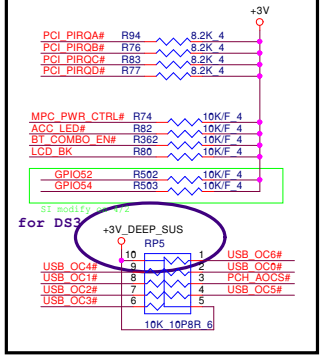
Size	Document Number	Rev
Custom	PCH 2/6 (HDA/RTC/SATA/SPI)	1A
Date: Wednesday, May 23, 2012	Sheet 7 of 37	

Cougar Point-M/Panther Point (PCI,USB,NVRAM)

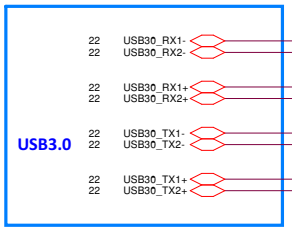
Cougar Point-M/Panther Point (PCI-E,SMBUS,CLK)

08

PCI/USBOC# Pull-up(CLG)

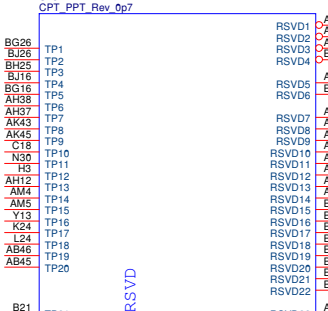


USB3.0

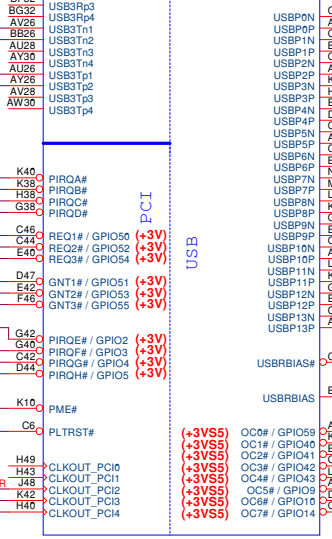


20111130 Modify USB3.0 for HM70

RSVD

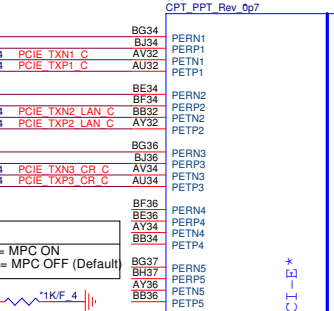


USB

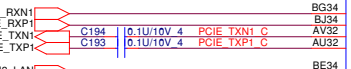


PCI

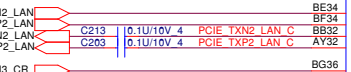
PCIE-E*



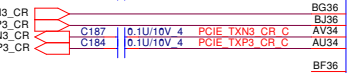
WLAN



LAN



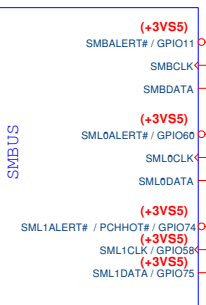
Cardreader



MPC Switch Control	
MPC_PWR_CTRL#	Low = MPC ON High = MPC OFF (Default)

MPC_PWR_CTRL# R75 *1K/F_4

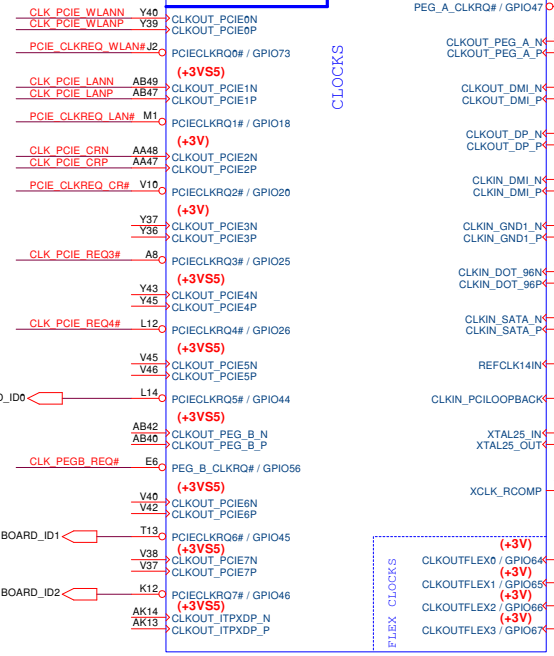
SMBUS



PV , HP request Image sensor SMBus reserve to PCH

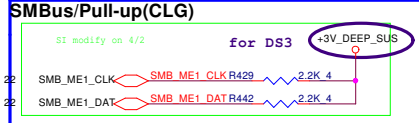
Controller Link

CLOCKS

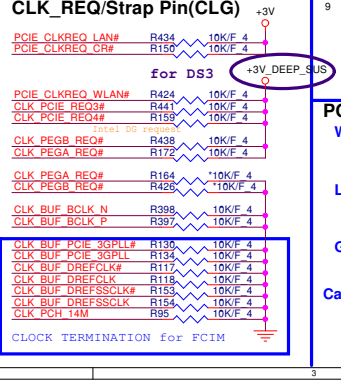


FLEX CLOCKS

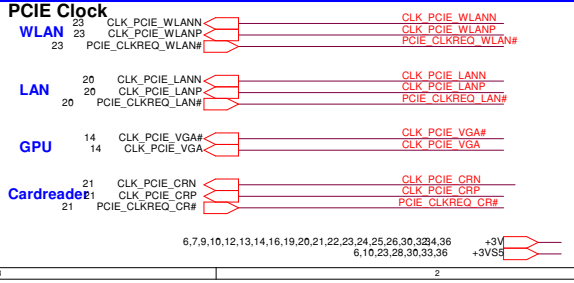
SMBus/Pull-up(CLG)



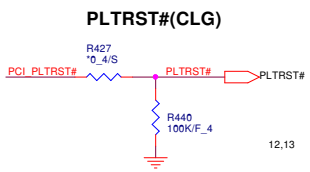
CLK_REQ/Strap Pin(CLG)

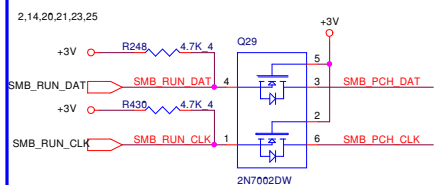


PCIE Clock

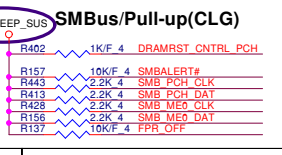


PLTRST#(CLG)





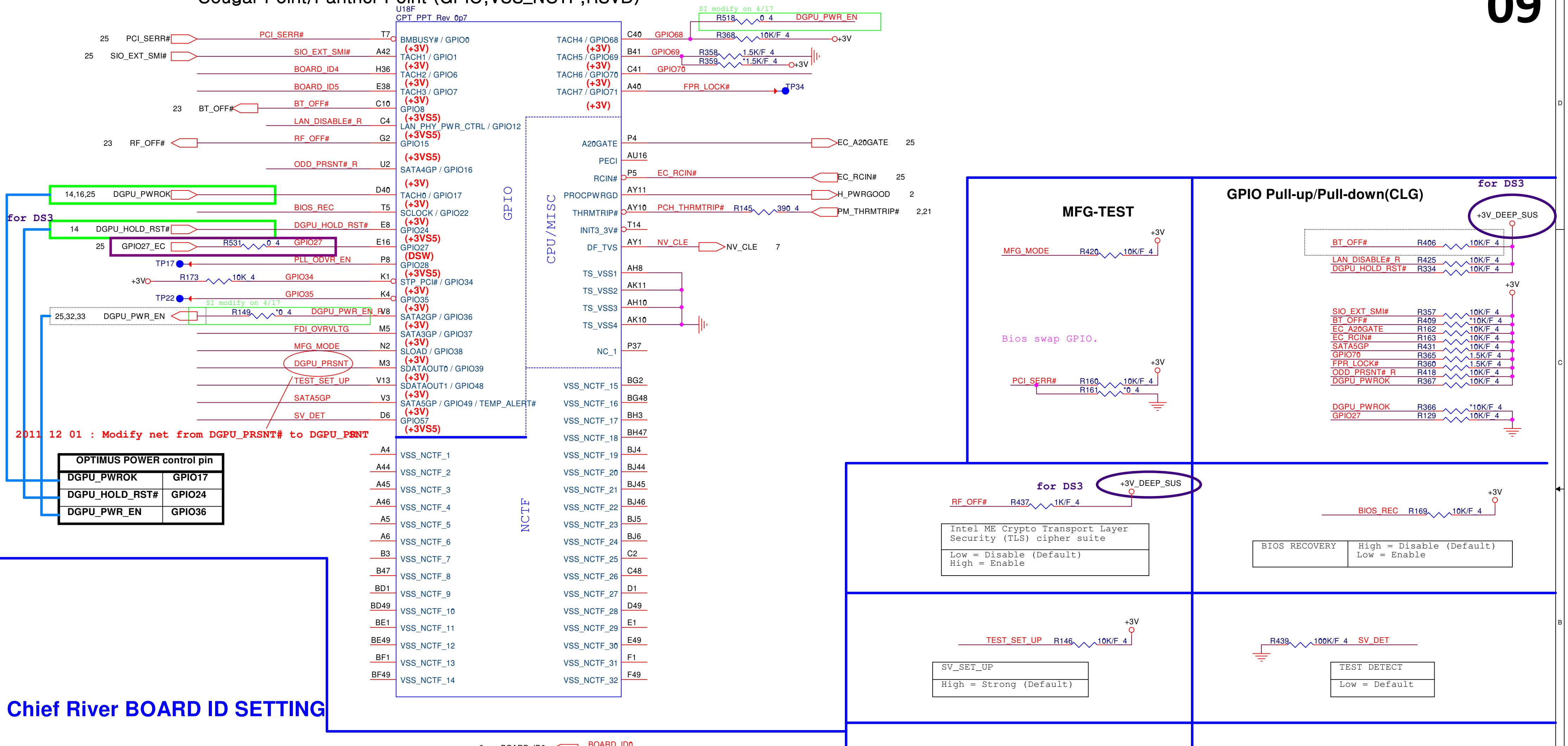
SMBus/Pull-up(CLG)



NB5	PROJECT : VOLKS Quanta Computer Inc.		
	Size: Custom	Document Number: PCH 3/6 (Clock/PCI/PCIE/USB)	Rev: 1A
	Date: Wednesday, May 23, 2012	Sheet: 8 of 37	

Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)

09



OPTIMUS POWER control pin	
DGPU_PWROK	GPIO17
DGPU_HOLD_RST#	GPIO24
DGPU_PWR_EN	GPIO36

Chief River BOARD ID SETTING

Model	BOARD_ID5	BOARD_ID4 14": 0 15": 1	BOARD_ID3 HM70: 0 HM77: 1	BOARD_ID2	BOARD_ID1 1G: 0 2G: 1	BOARD_ID0 UMA: 0 DIS: 1
U33 UMA	0	0	0	0	0	0
U33 DIS 128*16 VRAM	0	0	0	0	0	1
U33 DIS 256X16 VRAM	0	0	0	0	1	1
	0	0	0	1	1	1
U33 HM77	0	0	1	X	X	X
U33 HM70	0	0	0	X	X	X

	SG	UMA
Stuff	Ra	Rb
NC	Rb	Ra

6,7,8,10,12,13,14,16,19,20,21,22,23,24,25,26,30,32,34,36 +3V
6,10,23,28,30,33,36 +3VS5

PROJECT : VOLKS
Quanta Computer Inc.
NB5

Size	Document Number	Rev
Custom	PCH 4/6 (GPIO)	1A

Date: Wednesday, May 23, 2012 Sheet 9 of 37

Cougar Point/Panther Point (POWER)

Cougar Point/Panther Point (POWER)

U18J
CPT_PPT_Rev_0p7
POWER

U18G
CPT_PPT_Rev_0p7
POWER

Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
MISC
CPU
RTC
HDA
VCC CORE
VCCIO
CRT
LVDS
HVCMOS
DMI
DFT / SPI
FDI

3mA (10mils)
VCCASW:803mA (40mils)
160mA (20mils)
65mA (10mils)
8mA (10mils)
55mA (10mils)
95mA (10mils)
V_PROC_IO=2mA (10mils)
VCCRTC<1mA (10mils)
for DS3
VCCSUS3_3:65mA(15mils)
VCC5REFSUS=1mA
1mA (10mils)
119mA (15mils)
266mA (20mils)
70mA
350mA
30mA
1.01A (60mils)
10mA (10mils)
VCCCore:1.73 A (100mils)
VCCIO:3.799 A (140mils)
178m A (20mils)
(Mobile 1.5V)
160mA (15mils)
20mA (10mils)
6.3mA (10mils)
1mA (10mils)
60mA (10mils)
SG & UMA : Ra
DIS : Rb
42mA (10mils)
2 mA (10mils)
10mA (10mils)
V5REF= 1mA

PROJECT : VOLKS
Quanta Computer Inc.
NB5
Size: Custom
Document Number: PCH 5/6 (Power)
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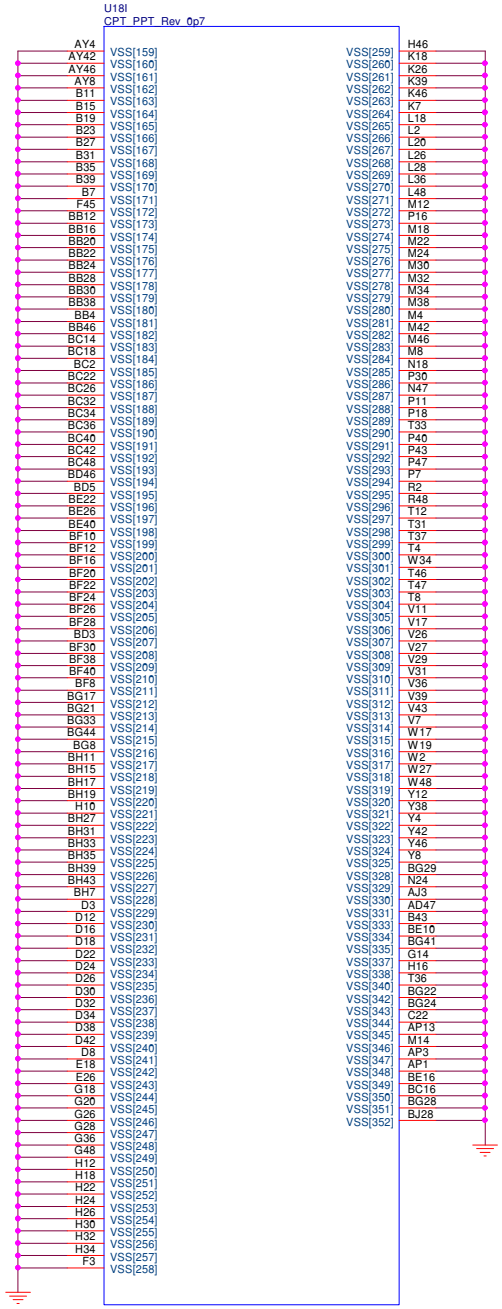
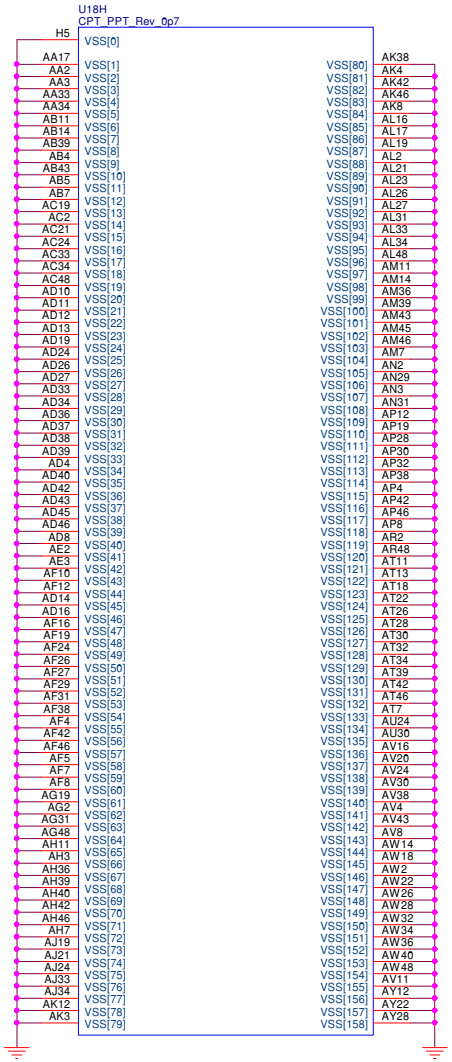
Cougar Point/Panther Point (GND)



Cougar Point/Panther Point (GND)



PROJECT : VOLKS

Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	PCH 6/6 (Ground)	1A

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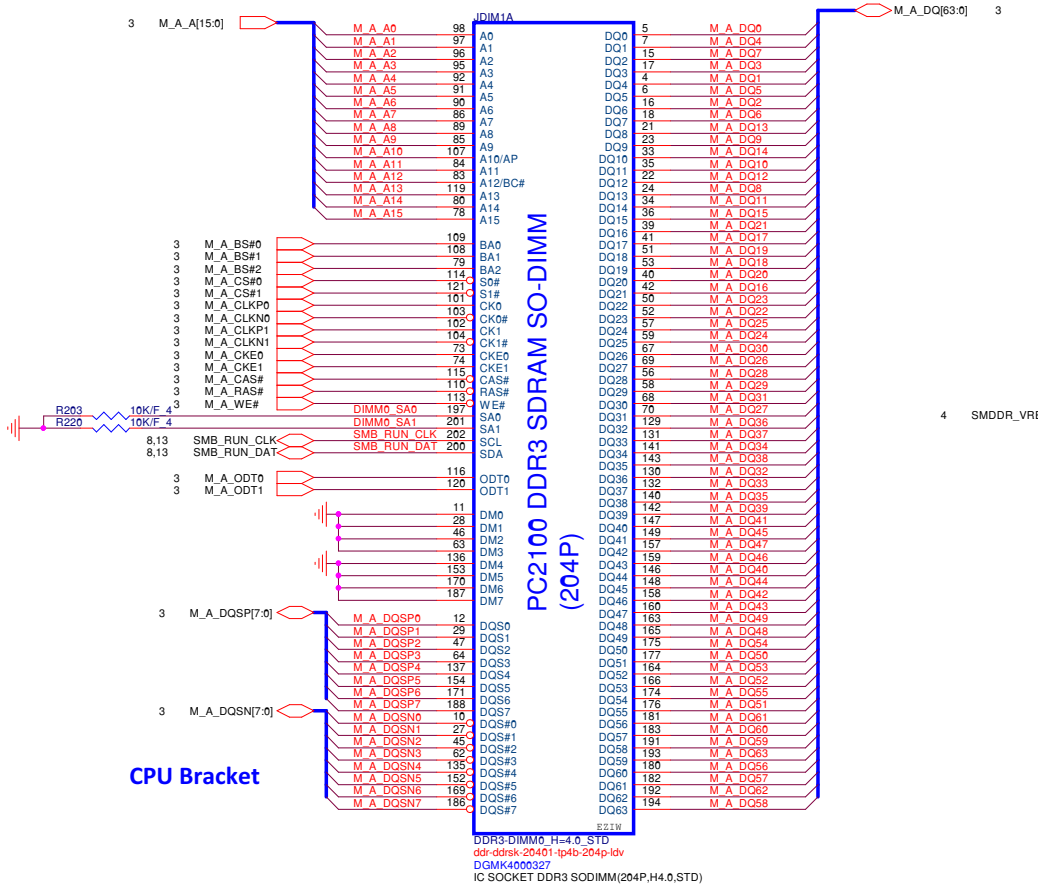
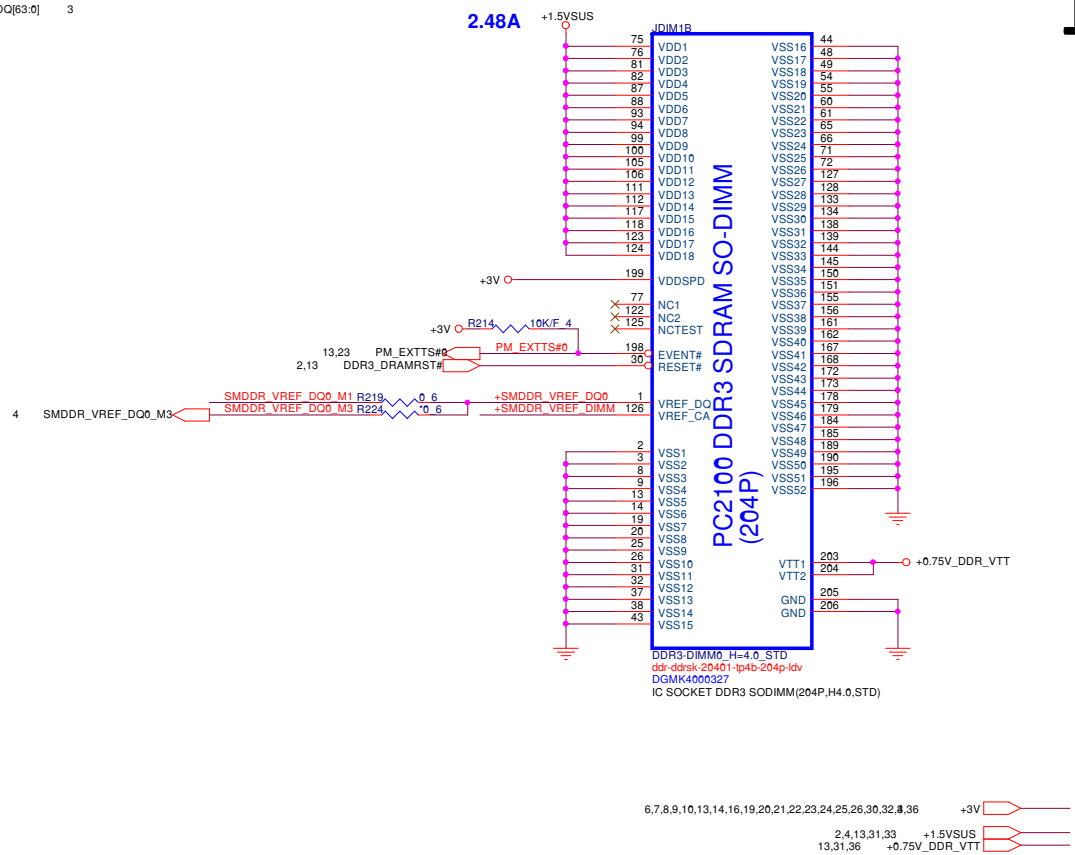
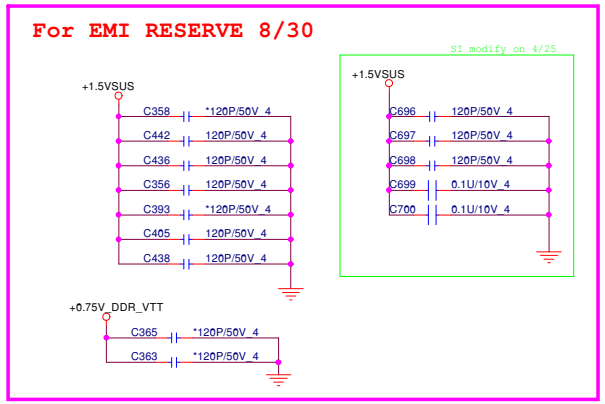
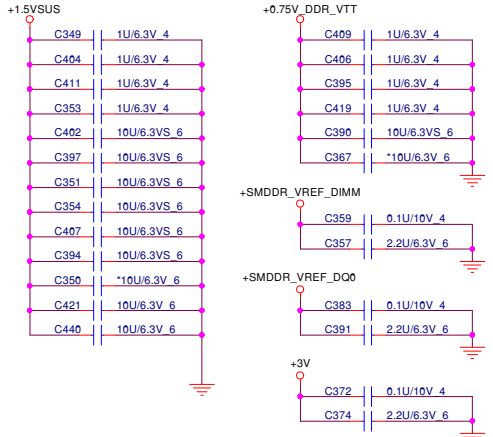
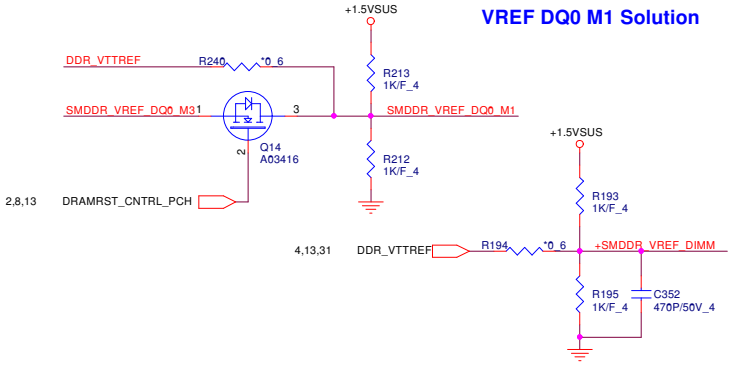


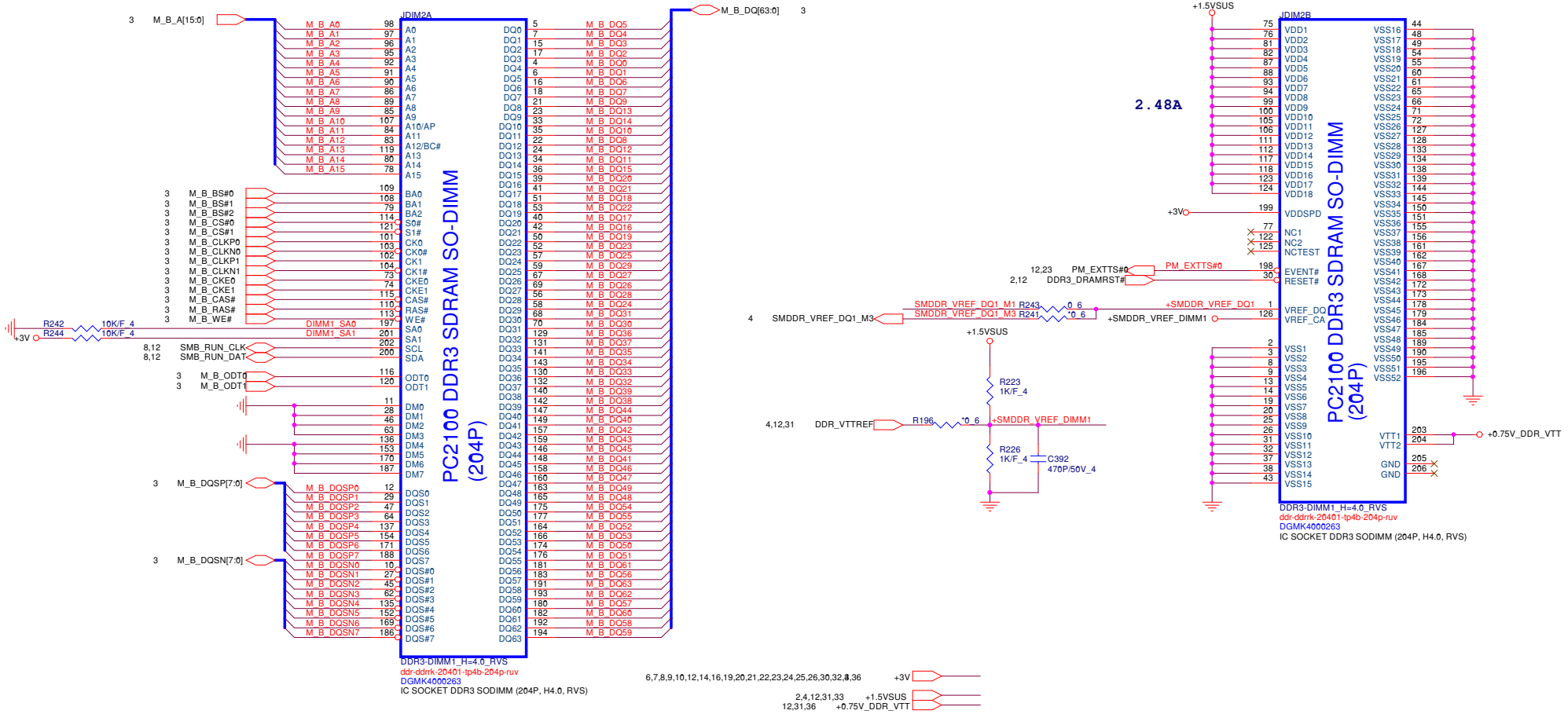




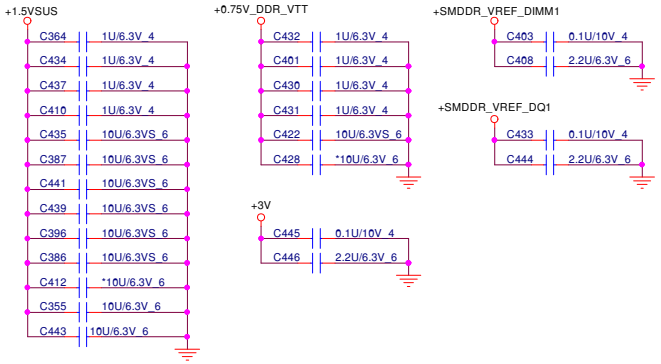




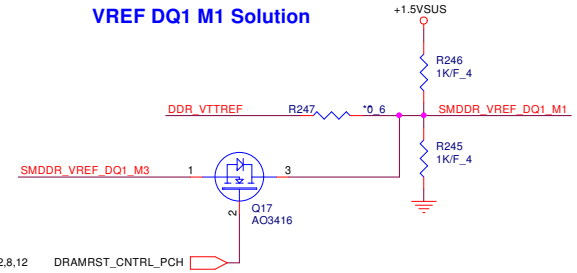
NB5	PROJECT : VOLKS Quanta Computer Inc.		
	Size: Custom	Document Number: System Memory 1/2 (5.2H)	Rev: 1A
	Date: Wednesday, May 23, 2012	Sheet: 12of	37



Place these Caps near So-Dimm1.



VREF DQ1 M1 Solution



NB5	PROJECT : VOLKS Quanta Computer Inc.	
Size: Custom	Document Number: System Memory 2/2 (9.2H)	Rev: 1A
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N13P-GV2-S-A2 (GB2-64)
Max point NVCLK = 937.5 , MCLK = 900
TDP point NVCLK = 800 , MCLK = 900

PEX_IOVDD + PEX_IOVDDQ = 1.042A

PEX_PLL_HVDD + PEX_SVDD_3V3 = 143mA

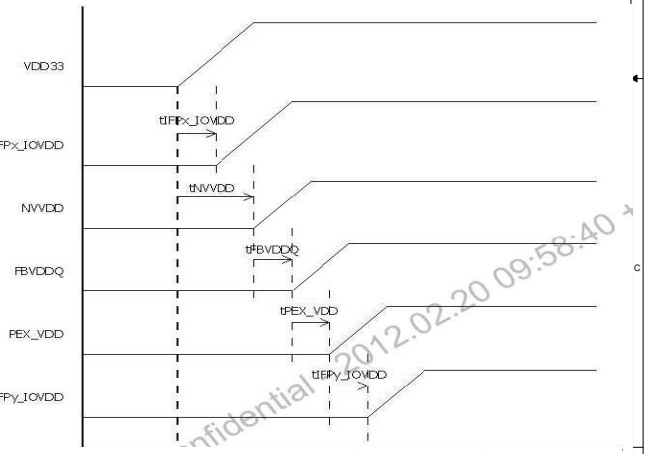
PEX_PLLVDD = 130mA

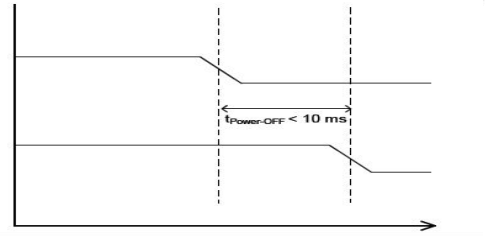
NVDD = 32.22 ~ 26.66 A

VDD33 = 56mA

power up sequence

power down sequence





PROJECT : VOLKS			
Quanta Computer Inc.			
Size: Custom	Document Number: N13P-GV2(PCIEI/F)		Rev: 1A
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U15B
bga595-nvidia-n13p-gv2-s-a2
COMMON

R39 10K/F_4 FB_CLAMP F3

NC	GF119
FB_CLAMP	GF117

2/14 FBA

FBA_ODT_L FBA_CMD2 R4 10K/F_4
FBA_ODT_H FBA_CMD18 R56 10K/F_4
FBA_RST# FBA_CMD5 R3 10K/F_4
FBA_CKE_L FBA_CMD3 R34 10K/F_4
FBA_CKE_H FBA_CMD19 R73 10K/F_4

T19 FBA_CMD1
T13 FBA_CMD17
T20 FBA_CMD31

For debug only

+1.5V_GFX R30 60.4/F_4 FBA_DEBUG0 F22
+1.5V_GFX R29 60.4/F_4 FBA_DEBUG1 J22

18 VMA_CLK0 VMA_CLK0 D24
18 VMA_CLK0# VMA_CLK0# D25
18 VMA_CLK1 VMA_CLK1 N22
18 VMA_CLK1# VMA_CLK1# M22

FB_PLLAVDD = 55mA

+1.05V_GFX
L7 FBMA-10-160808-300T +FB_PLLAVDD F16
30 ohm/100MHz
ESR=0.03ohm
P22
H22
C65 0.1U/10V_4
C48 0.1U/10V_4
C45 0.1U/10V_4
C128 22U/6.3VS_6

FB_DLLAVDD	GF119
FB_PLLAVDD	GF117

FB_DLLAVDD = 15mA

ph

18 VMA_DQ[63..0]
18 VMA_DM[7..0]
18 VMA_WDQS[7..0]
18 VMA_RDQS[7..0]

FBVDDQ + FBVDD = 3.116A

U15D
bga595-nvidia-n13p-gv2-s-a2
COMMON
12/14 FBVDDQ

+1.5V_GFX
C47 0.1U/10V_4
C43 0.1U/10V_4
C35 0.1U/10V_4
C46 0.1U/10V_4
C44 1U/6.3V_4
C40 1U/6.3V_4
C32 4.7U/6.3V_6
C60 10U/6.3V_6
C52 10U/6.3V_6

FB_CAL_PD_VDDQ D22 FB_CAL_PD_VDDQ R26 40.2/F_4 +1.5V_GFX
FB_CAL_PU_GND C24 FB_CAL_PU_GND R28 42.2/F_4
FB_CALTERM_GND B25 FB_CAL_TERM_GND R27 51.1/F_4

FB_VREF_PROBE D23 +FB_VREF1 T10

U15F
bga595-nvidia-n13p-gv2-s-a2
COMMON
13/14 GND

14,16,33 +1.05V_GFX
16,17,18,33 +1.5V_GFX

PROJECT :	VOLKS
Quanta Computer Inc.	
Size: Custom	Document Number: N11M-GE2(MEMORY/GND)
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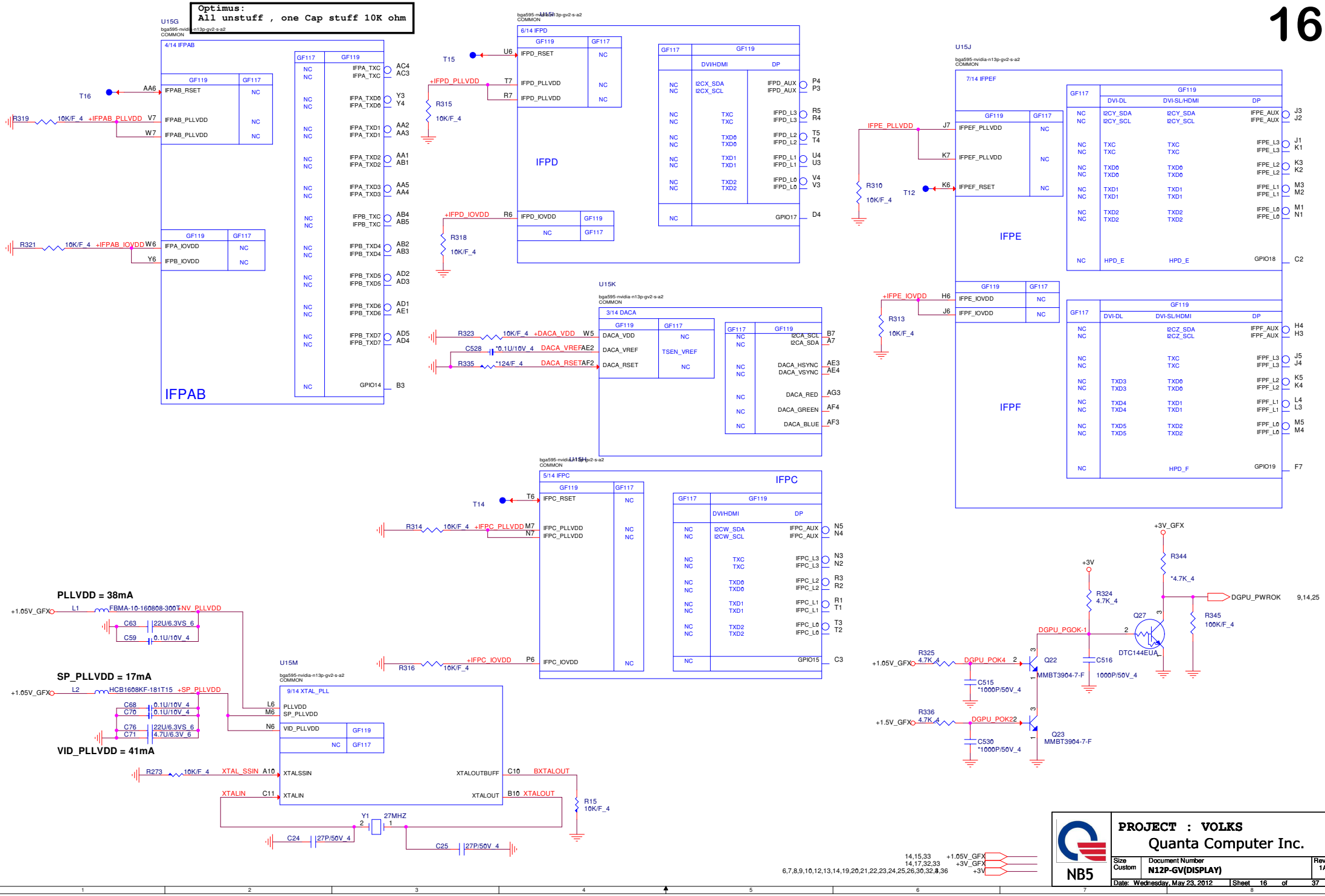
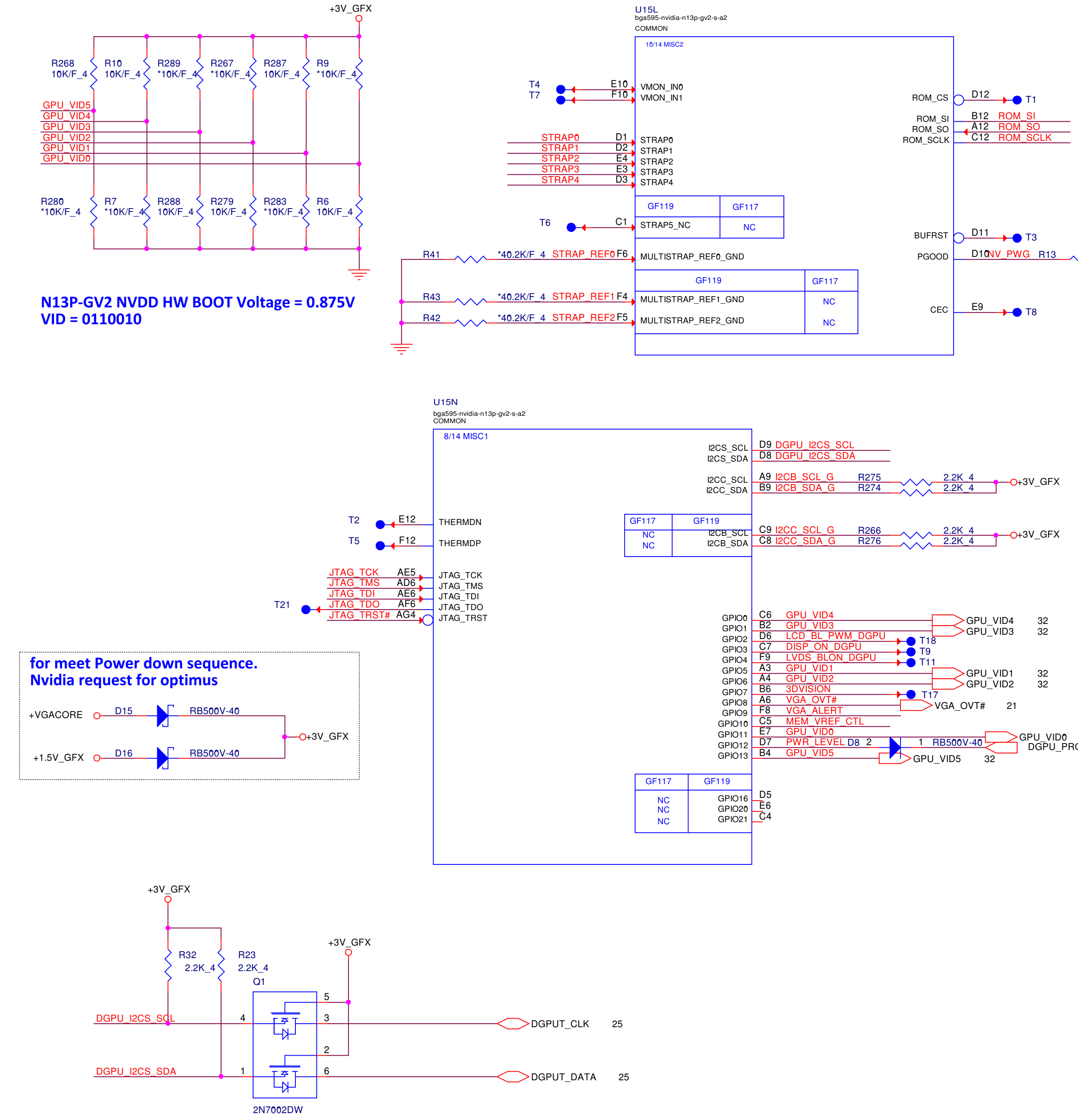
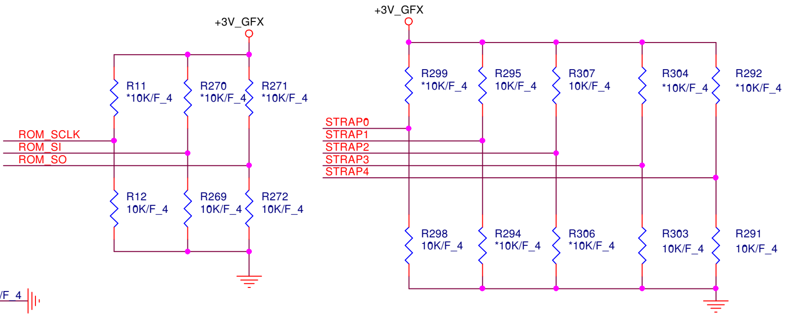
Optimus:
All unstuff , one Cap stuff 10K ohm







Binary Strap Mode Mapping

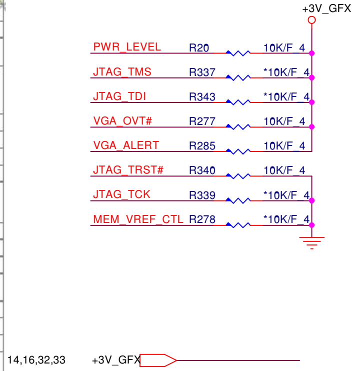
Strap Pin name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10Kohm	Pull-down to GND
ROM_SI	SUB_VENDOR	10Kohm	Pull-UP to 3V3 if VBIOS ROM Exists Pull-down to GND if no VBIO ROM
ROM_SO	VGA_DEVICE	10Kohm	Pull-down to GND (no dispaly)
STRAP0	RAMCFG[0]	10Kohm	USER defined
STRAP1	RAMCFG1]	10Kohm	USER defined
STRAP2	RAMCFG[2]	10Kohm	USER defined
STRAP3	RAMCFG[3]	10Kohm	USER defined
STRAP4	PCIE_MAX_SPEED	10Kohm	Pull-down to GND

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	QBCON P/N	HP P/N
		Reserved			
	(MP)				
0011	DDR3 256Mx16x4, 64bit, 2Gb,900MHz	Hynix	H5TQ4G63MFR-11C	AKD5PGWTW00	AKD5PGWTW01
0101	DDR3 256Mx16x4, 64bit, 2Gb,900MHz	Micron	MT41K256M16HA-107G:E	AKD5PGSTL01	AKD5PGSTL02
1100	DDR3 128Mx16x4, 64bit, 1Gb,900MHz	Hynix	H5TQ2G63DFR-11C	AKD5MGWTW12	AKD5MGWTW13
0101	DDR3 128Mx16x4, 64bit, 1Gb,900MHz	Samsung	K4W2G1646C-HC11	AKD5MGWT513	AKD5MGWT508
	(OOC)				
0001	DDR3 256Mx16x4, 64bit, 2Gb,900MHz	Samsung	K4W4G1646B-HC11	AKD5MGWT518	AKD5MGWT517
0100	DDR3 256Mx16x4, 64bit, 2Gb,900MHz	Hynix	H5TQ4G63AFR-11C	applying	applying
1011	DDR3 128Mx16x4, 64bit, 1Gb,900MHz	Samsung	K4W2G1646E-BC11	AKD5MGGT521	AKD5MGGT522

GB2-64 and GB4-128 GPIO Desdription

GPIO pin Name	Normal Function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	GPU_VID4	O	GPU Core VDD VID4	Strap to boot NVVDD
GPIO1	GPU_VID3	O	GPU Core VDD VID3	Strap to boot NVVDD
GPIO2	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control	100 K pull-down
GPIO3	LCD_VCC or PSI	O	Panel Power Enable or Phase Shedding	LCD_VCC: 100k pull-down PSI: 10k pull-up or pull-down; stuff as needed to disable phase shedding by default
GPIO4	LCD_BLEN	O	Panel Backlight Enable	100 K pull-down
GPIO5	GPU_VID1	O	GPU Core VDD VID1	Strap to boot NVVDD
GPIO6	GPU_VID2	O	GPU Core VDD VID2	Strap to boot NVVDD
GPIO7	3DVision	O	3D Vision Left/Right signal	100 K pull-down
GPIO8	OVERT	I/O	Active Low Thermal Catastrophic Over Temperature	100 K pull-up
GPIO9	ALERT	I/O	Active Low Thermal Alert	100 K pull-up
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 K pull-down
GPIO11	GPU_VID0	O	GPU Core VDD VID0	Strap to boot NVVDD
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100 K pull-up
GPIO13	GPU_VID5	O	GPU Core VDD VID5	Strap to boot NVVDD
GPIO14	HPD_AB	I	Hot Plug Detect for IFPAB	See Figure 76
GPIO15	HPD_C	I	Hot Plug Detect for IFPC	See Figure 76
GPIO16	PSI or MEM_VDD_CTL	O	Phase Shedding or Memory VDD VID	PSI: 10k pull-up or pull-down; stuff as needed to disable phase shedding by default MEM_VDD_CTL: Strap to boot FBVDD/Q
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	See Figure 76
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	See Figure 76
GPIO19	HPD_F	I	Hot Plug Detect for IFPF	See Figure 76
GPIO20	Reserved			
GPIO21	Reserved			



PROJECT : VOLKS

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Custom	N12P-GV(GPIO/STRAPS)	1A

CHANNEL A: 256MB/512MB DDR3

15 VMA_DQ[63..0]
15 VMA_DM[7..0]
15 VMA_WDQS[7..0]
15 VMA_RDQS[7..0]

U1 — VRAM _DDR3 — 96-BALL SDRAM DDR3 — ph
U14 — VRAM _DDR3 — 96-BALL SDRAM DDR3
U3 — VRAM _DDR3 — 96-BALL SDRAM DDR3
U17 — VRAM _DDR3 — 96-BALL SDRAM DDR3

VREFC_VMA1 / VREFD_VMA1
VREFC_VMA3 / VREFD_VMA3

FBA_CMD9, FBA_CMD11, FBA_CMD8, FBA_CMD25, FBA_CMD10, FBA_CMD24, FBA_CMD22, FBA_CMD7, FBA_CMD21, FBA_CMD6, FBA_CMD29, FBA_CMD23, FBA_CMD28, FBA_CMD20, FBA_CMD4, FBA_CMD14

FBA_CMD12, FBA_CMD27, FBA_CMD26

VMA_CLK0, VMA_CLK0#, FBA_CMD3

VMA_CLK1, VMA_CLK1#, FBA_CMD19

FBA_CMD2, FBA_CMD0, FBA_CMD30, FBA_CMD15, FBA_CMD13

FBA_CMD18, FBA_CMD16

VMA_WDQS2, VMA_RDQS2
VMA_WDQS1, VMA_RDQS1
VMA_WDQS5, VMA_RDQS5
VMA_WDQS7, VMA_RDQS7

VMA_DM2, VMA_DM0
VMA_DM3
VMA_DM5, VMA_DM4
VMA_DM7, VMA_DM6

VMA_WDQS0, VMA_RDQS0
VMA_WDQS3, VMA_RDQS3
VMA_WDQS4, VMA_RDQS4
VMA_WDQS6, VMA_RDQS6

FBA_CMD5

VMA_ZQ1
VMA_ZQ2
VMA_ZQ3
VMA_ZQ4

+1.5V_GFX

R33 240/F_4
R265 240/F_4
R72 240/F_4
R330 240/F_4

R5 162/F_4 VMA_CLK0, VMA_CLK0#

R263 1.33K/F_4, R264 1.33K/F_4, C481 0.1U/10V_4, VREFC_VMA1
R301 1.33K/F_4, R305 1.33K/F_4, C498 0.1U/10V_4, VREFD_VMA1
R71 162/F_4 VMA_CLK1, VMA_CLK1#
R328 1.33K/F_4, R329 1.33K/F_4, C520 0.1U/10V_4, VREFC_VMA3
R350 1.33K/F_4, R349 1.33K/F_4, C552 0.1U/10V_4, VREFD_VMA3

Left
C37 0.1U/10V_4
C33 0.1U/10V_4
C12 1U/6.3V_4
C10 1U/6.3V_4

C483 1U/6.3V_4
C500 1U/6.3V_4
C480 0.1U/10V_4
C497 0.1U/10V_4

C161 0.1U/10V_4
C85 0.1U/10V_4
C160 1U/6.3V_4
C162 1U/6.3V_4

C521 0.1U/10V_4
C522 0.1U/10V_4
C523 0.1U/10V_4
C551 1U/6.3V_4
C553 1U/6.3V_4
C555 10U/6.3V_6

Right
C14 1U/6.3V_4
C34 1U/6.3V_4
C9 10U/6.3V_6
C36 0.1U/10V_4
C13 0.1U/10V_4
C11 0.1U/10V_4

C479 1U/6.3V_4
C496 0.1U/10V_4
C482 0.1U/10V_4
C484 0.1U/10V_4
C478 10U/6.3V_6
C499 1U/6.3V_4

C159 0.1U/10V_4
C83 0.1U/10V_4
C82 1U/6.3V_4
C86 0.1U/10V_4
C84 1U/6.3V_4
C163 10U/6.3V_6

C518 0.1U/10V_4
C550 0.1U/10V_4
C519 1U/6.3V_4
C554 1U/6.3V_4

15,16,17,33 +1.5V_GFX

NB5

PROJECT : VOLKS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 VRAM(BGA96)	1A
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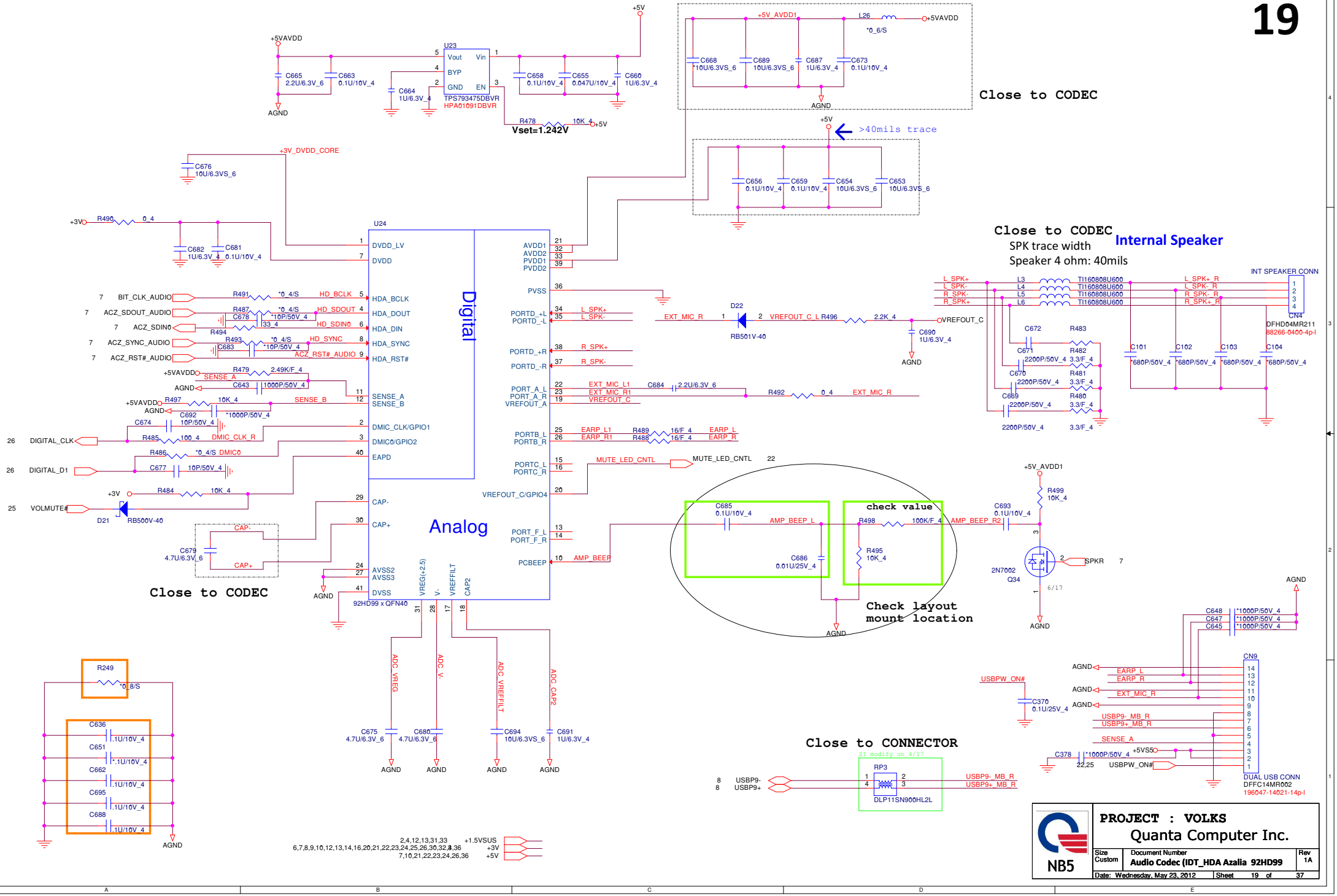
U23
TPS793475DBVR
HPA01091DBVR
Vset=1.242V
Close to CODEC
>40mils trace
U24
92HD99 x QFN40
Digital
Analog
Close to CODEC
SPK trace width
Speaker 4 ohm: 40mils
Internal Speaker
INT SPEAKER CONN
DFHD04MR211
88266-0400-4p-l
check value
Check layout
mount location
Close to CONNECTOR
DUAL USB CONN
DFFC14MR002
196047-14021-14p-l
PROJECT : VOLKS
Quanta Computer Inc.
NB5
Document Number
Audio Codec (IDT_HDA Azalia 92HD99
Rev 1A
Date: Wednesday, May 23, 2012
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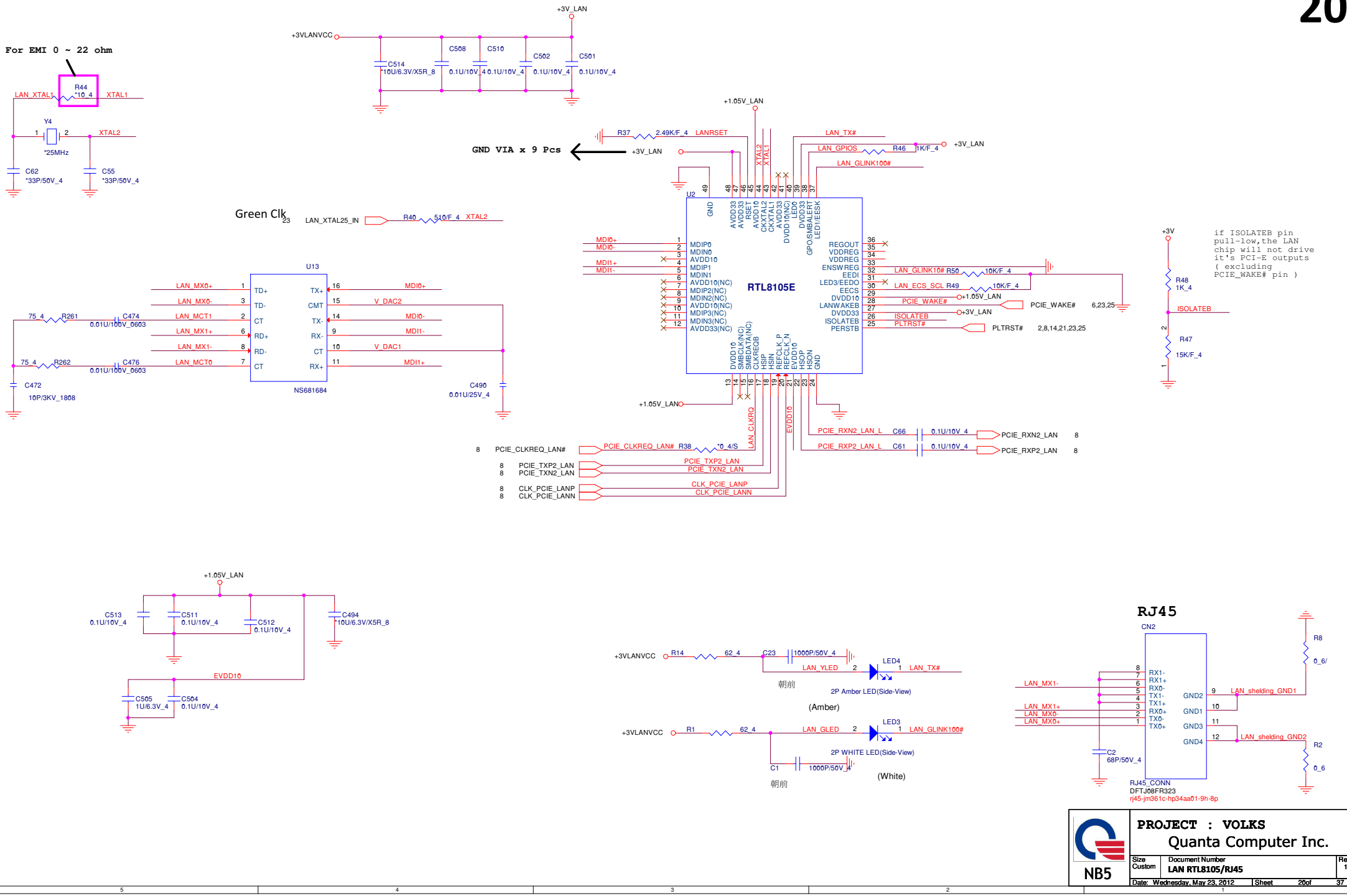

NB5	PROJECT : VOLKS Quanta Computer Inc.	
Size: Custom	Document Number: LAN RTL8105/RJ45	Rev: 1A
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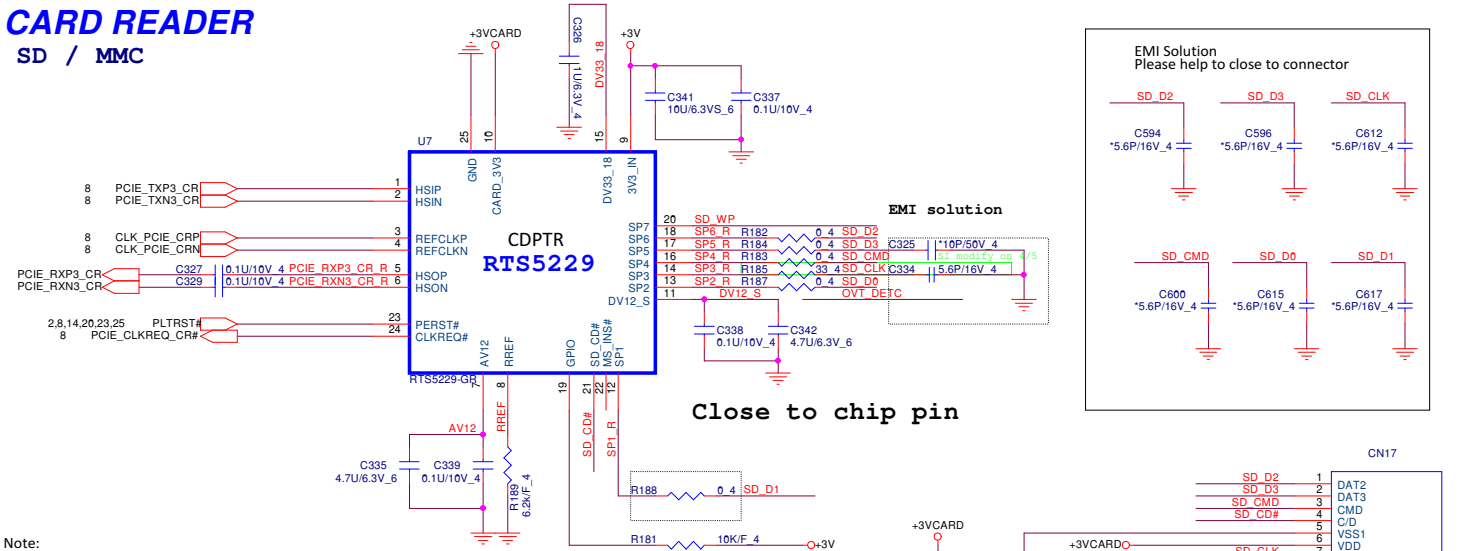
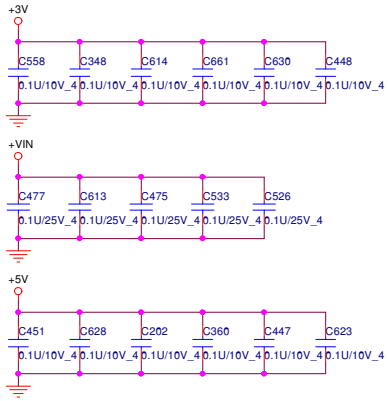
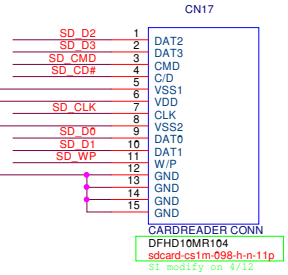
CARD READER

SD / MMC

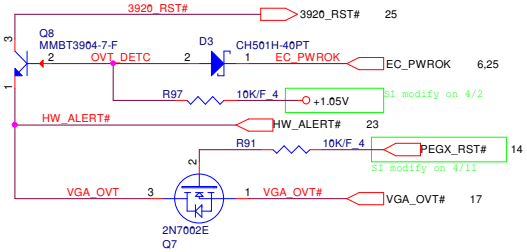


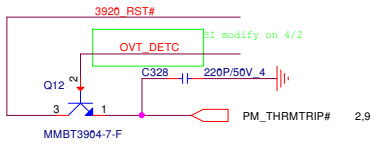


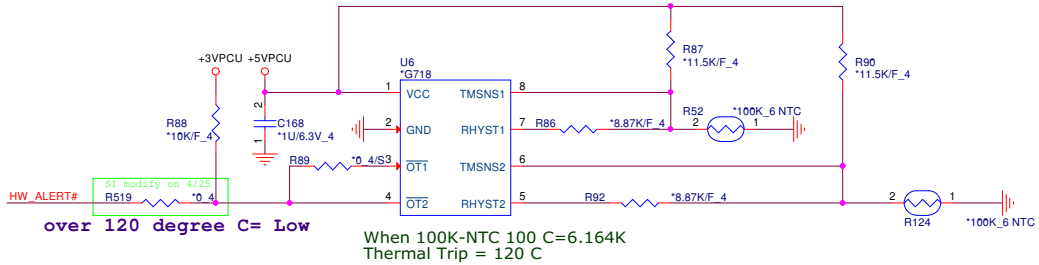


Note:
1. R5194, R5196, R5197, R5198, R5199, R5200 close to U37 pin
2. C5265, C5202 close to U37 pin7
3. C1021, C1022 close to U37 pin11
4. C1089, C1090 close to U37 pin9
5. C1019 close to U37 pin15
6. C1026, C1027 close to CN27 pin11
7. C1025 close to CN27 pin4

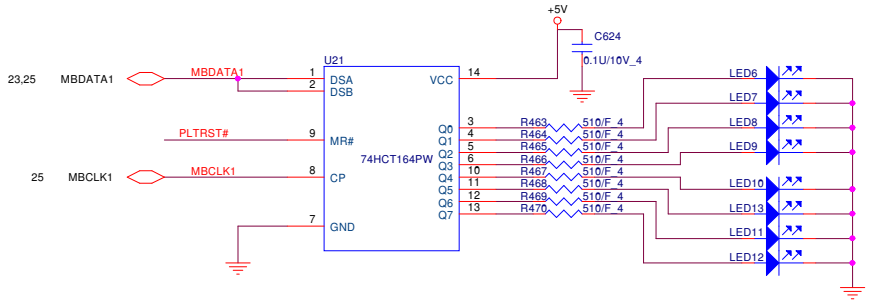
Thermal HW protect







80 port

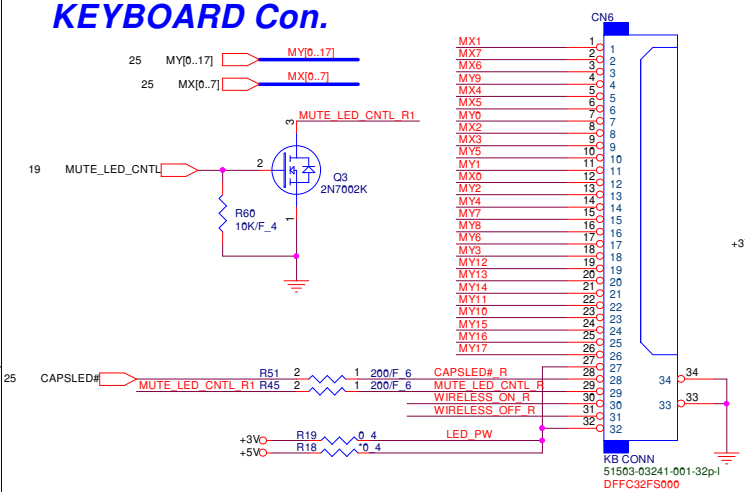


NB5

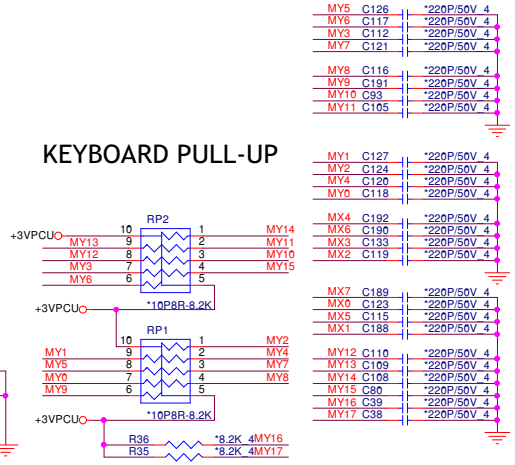
PROJECT : VOLKS
Quanta Computer Inc.

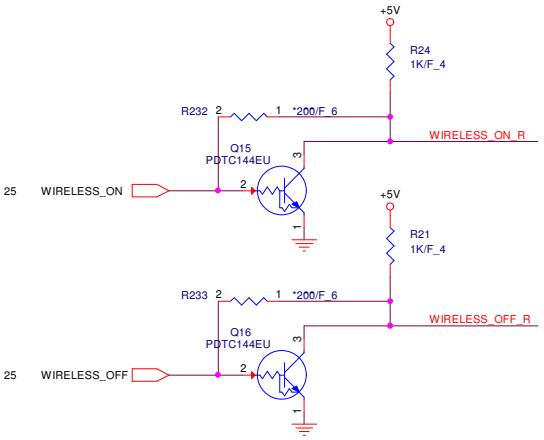
Size	Document Number	Rev
Custom	Card Reader control (RTS5229-GR)	1A
Date: Wednesday, May 23, 2012	Sheet 21of 37	

KEYBOARD Con.

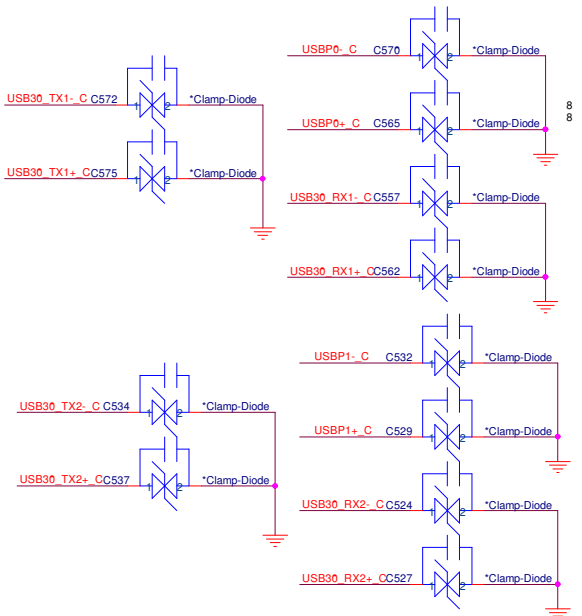


KEYBOARD PULL-UP

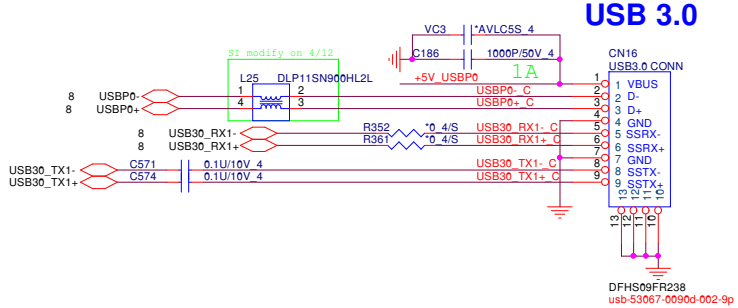




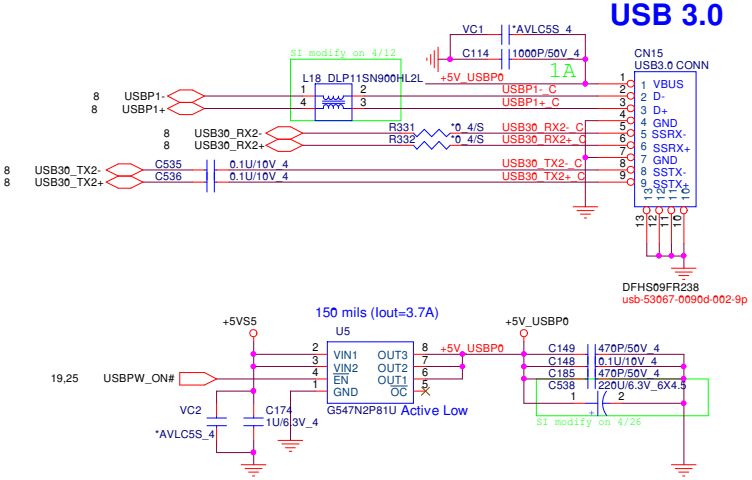
USB 2.0/3.0 Combo



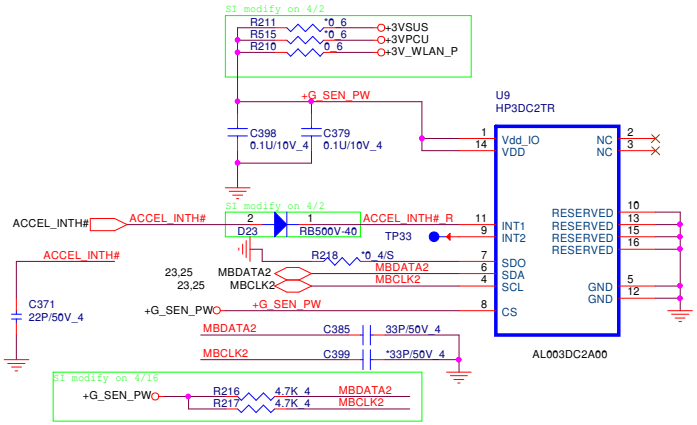
USB 3.0

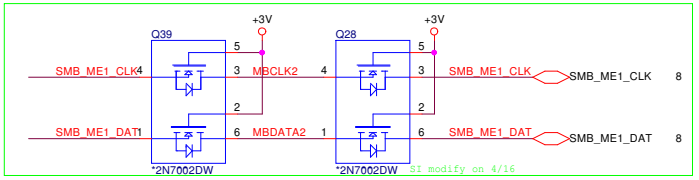


USB 3.0



Accelerometer Sensor





6,19,28,29,30,31,32,34,35,36
7,21,23,24,25,26,27,28
+5VS5
+3VPCU

PROJECT : VOLKS
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	USB 3.0/KB/Green CLK	1A
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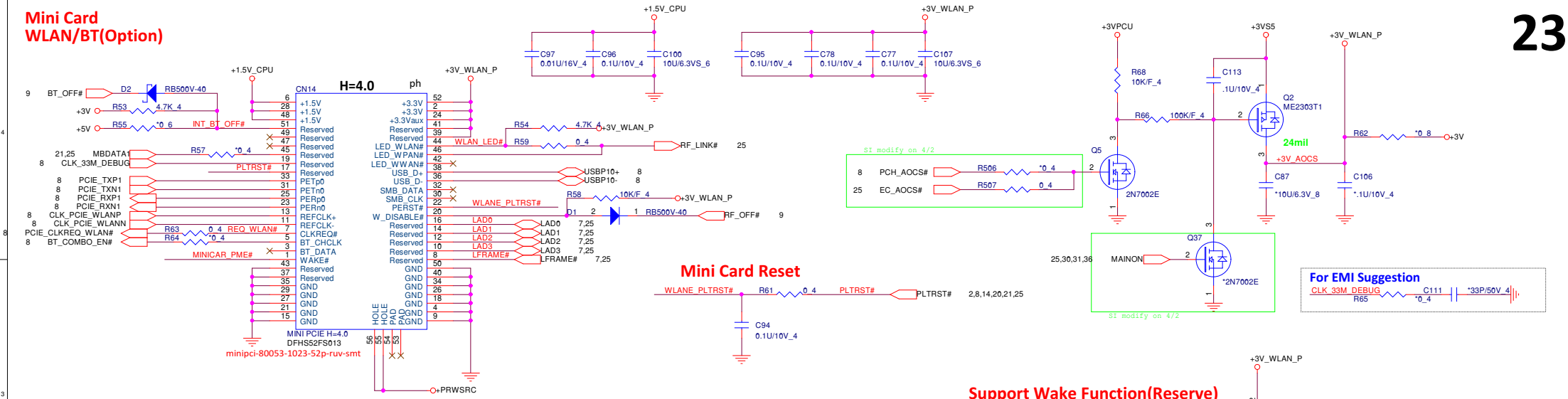
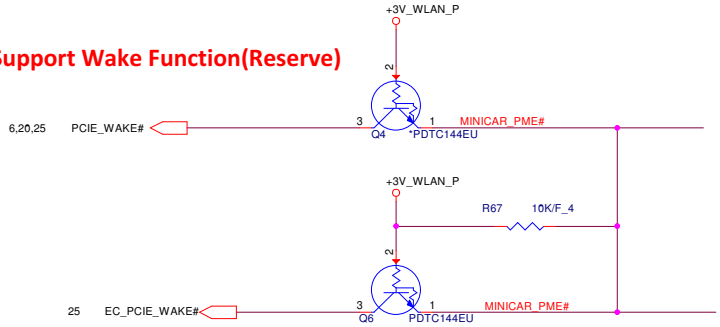
Mini Card WLAN/BT(Option)



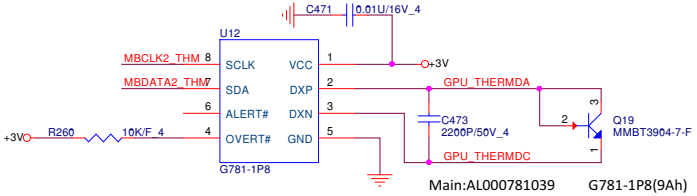
Mini Card Reset

Support Wake Function(Reserve)



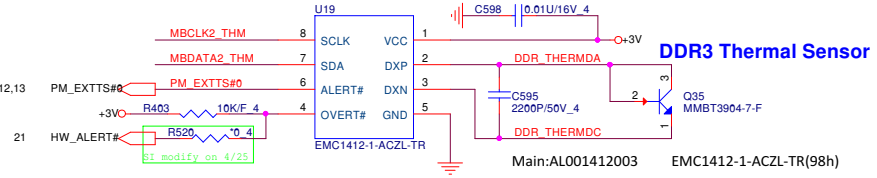
Local Thermal Sensor

GPU Thermal Sensor



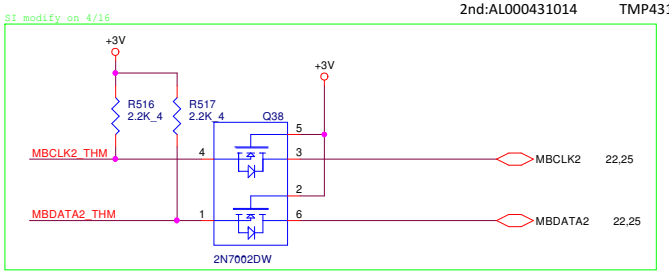
Main:AL000781039 G781-1P8(9Ah)
2nd:AL001412005 EMC1412-2-ACZL-TR(9Ah)

CPU Thermal Sensor



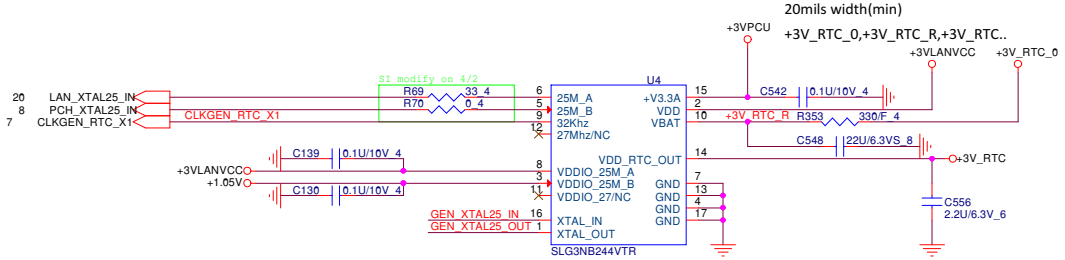
DDR3 Thermal Sensor

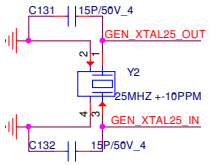
Main:AL001412003 EMC1412-1-ACZL-TR(98h)
2nd:AL000431014 TMP431ADGKR(98h)

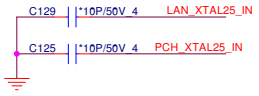


Green CLK Circuitry

20mils width(min)
+3V_RTC_0,+3V_RTC_R,+3V_RTC..





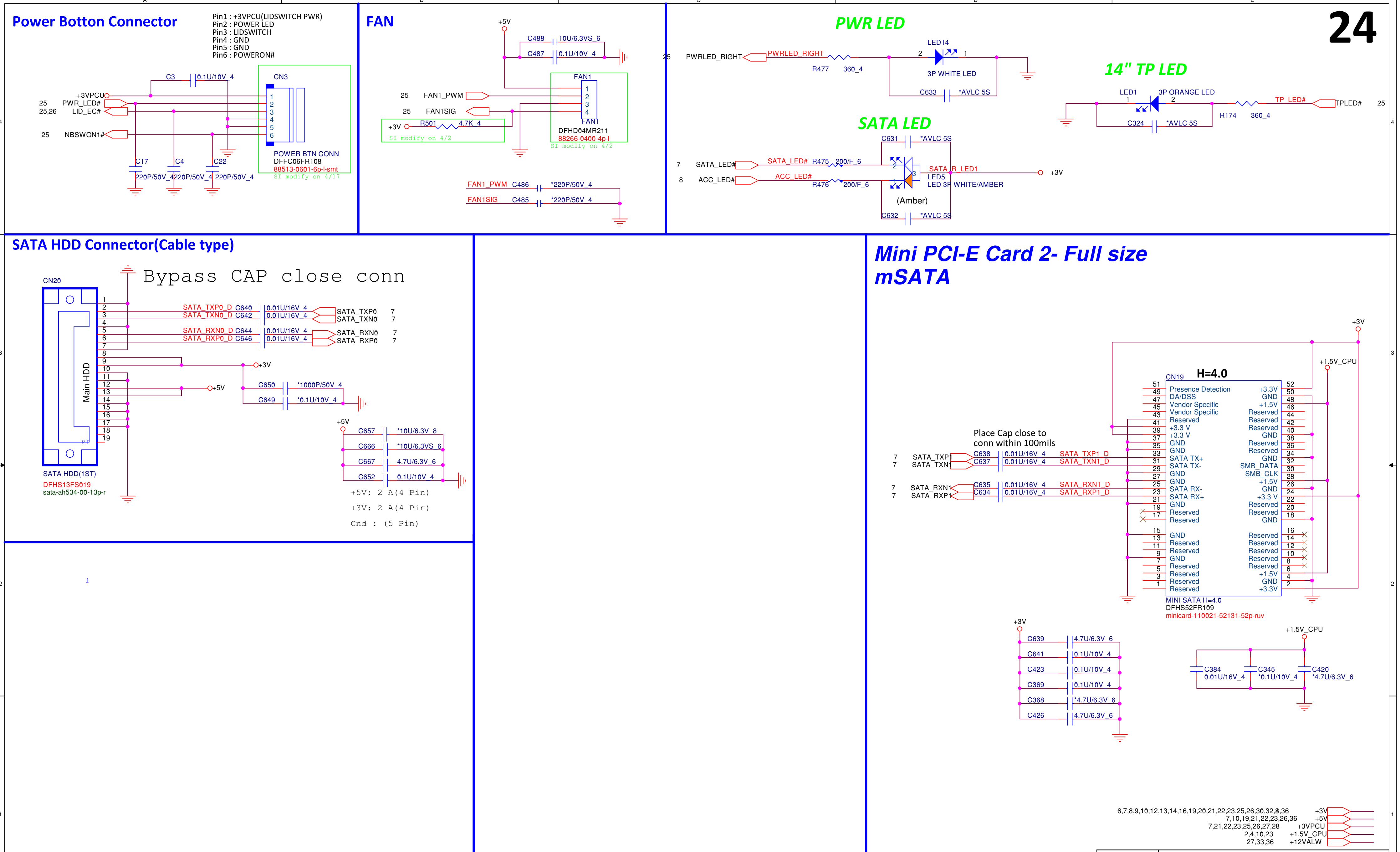


+PRWSRC

NB5

PROJECT : VOLKS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MINI-PCIE/LED	1A
Date: Wednesday, May 23, 2012	Sheet 23of 37	



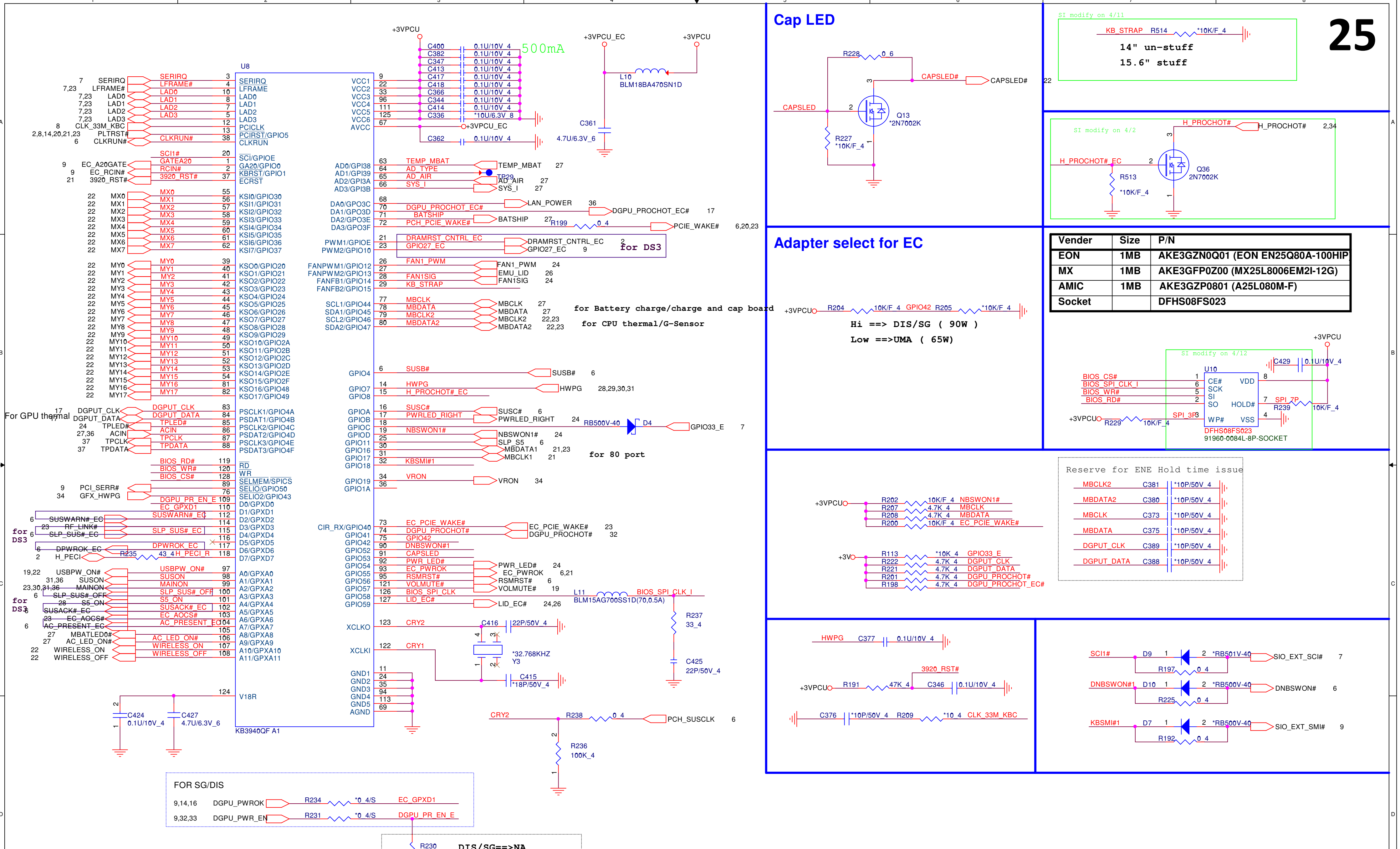
PROJECT : VOLKS

Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	SATA HDD/ODD/MSATA CONN	1A

Date: Wednesday, May 23, 2012 Sheet 24 of 37



Vender	Size	P/N
EON	1MB	AKE3GZN0Q01 (EON EN25Q80A-100HIP
MX	1MB	AKE3GFP0Z00 (MX25L8006EM2I-12G)
AMIC	1MB	AKE3GZP0801 (A25L080M-F)
Socket		DFHS08FS023

PROJECT : VOLKS

Quanta Computer Inc.

NB5

Size: Custom | Document Number: EC (KB3940 A1)/ROM | Rev: 1A

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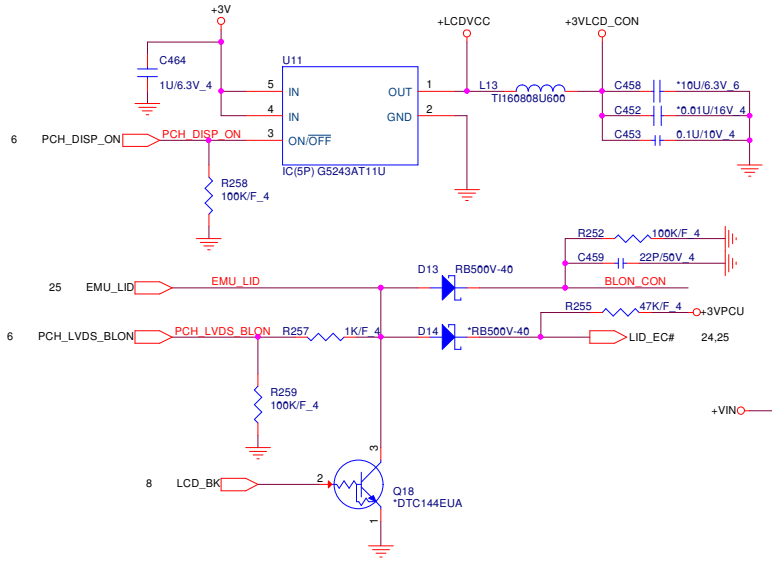
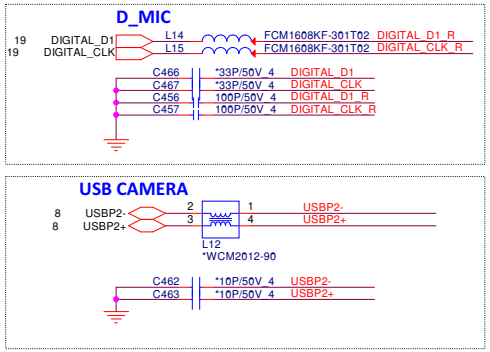
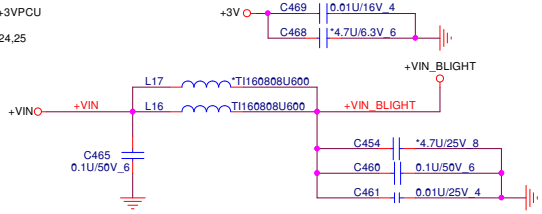
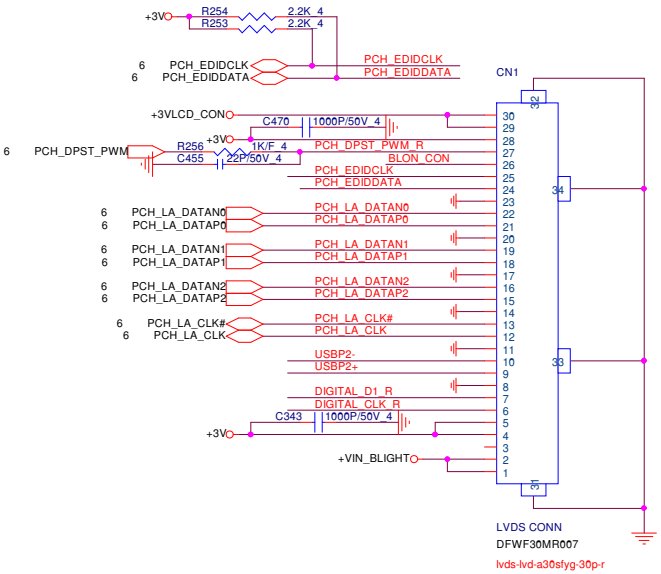
LVDS Conn.

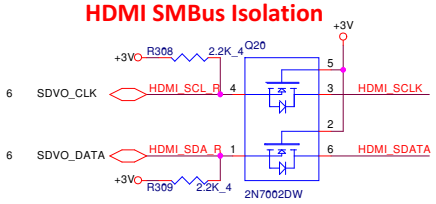


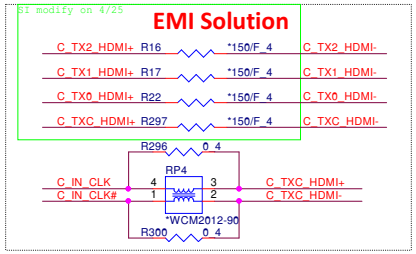


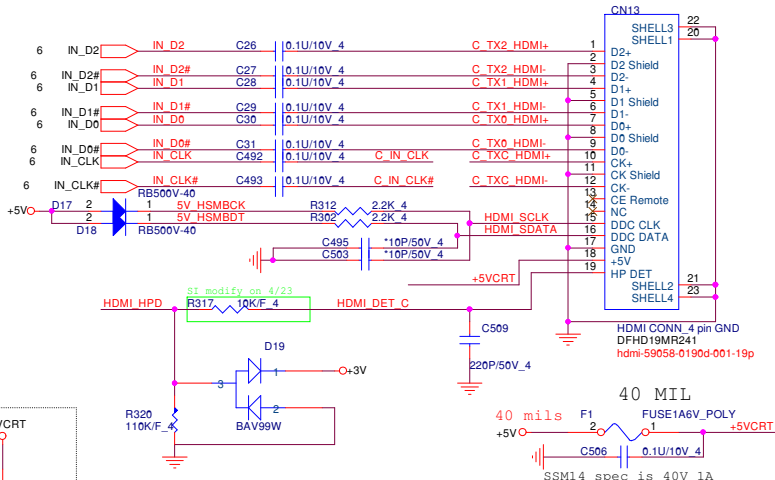


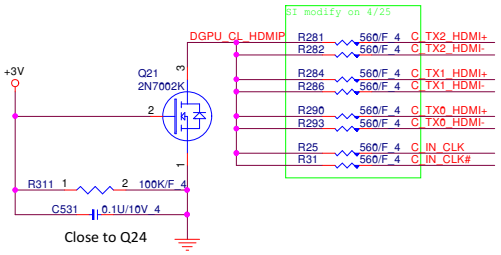


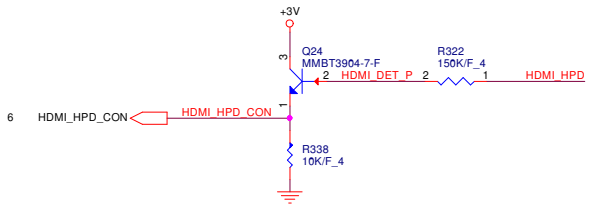
HDMI Conn.

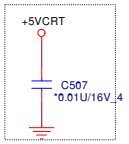


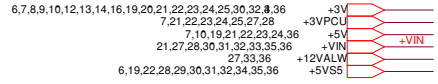










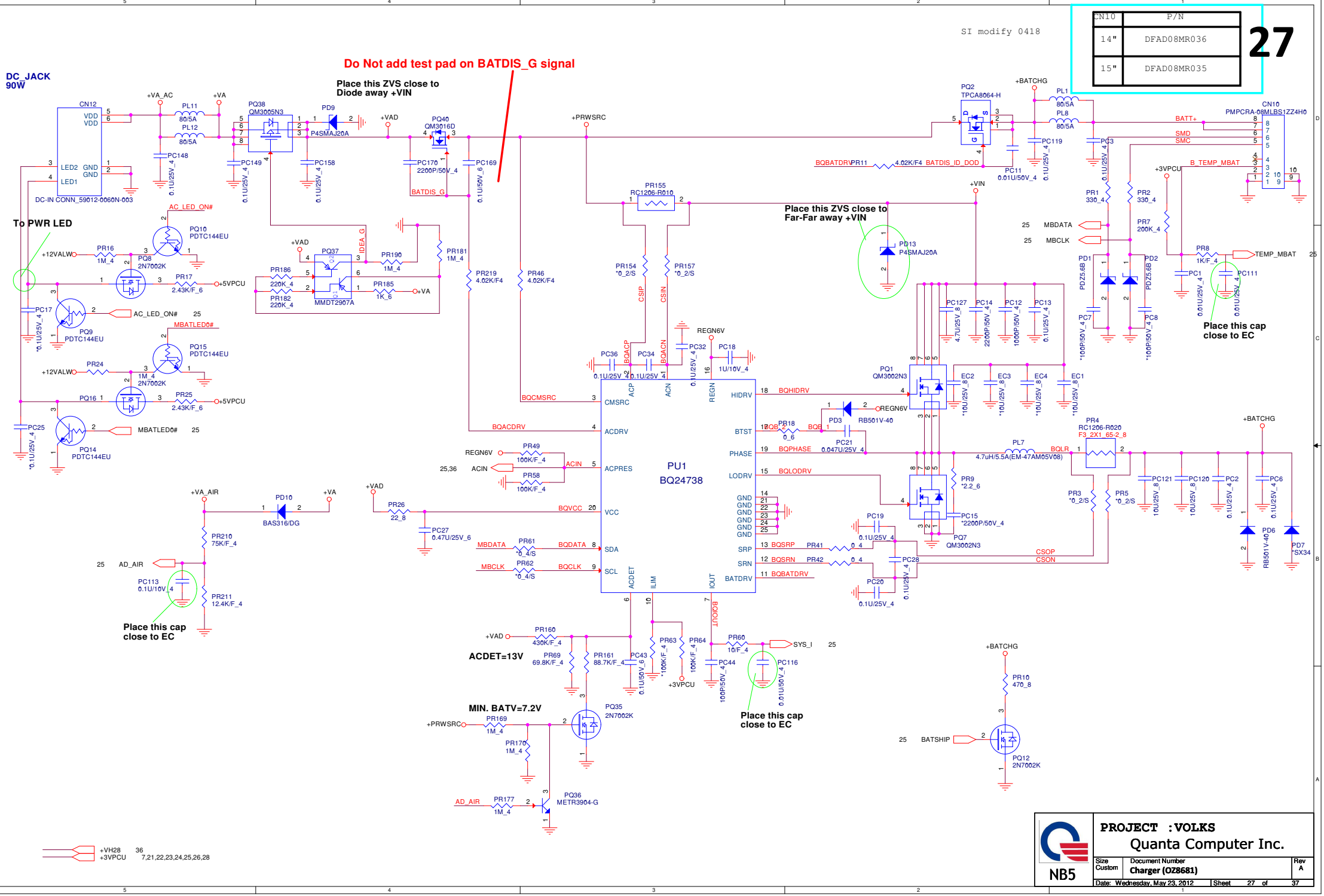


6,7,8,9,10,12,13,14,16,19,20,21,22,23,24,25,30,32,33,36 +3V
7,21,22,23,24,25,27,28 +3VPCU
7,10,19,21,22,23,24,36 +5V
21,27,28,30,31,32,33,35,36 +VIN
27,33,36 +12VALW
6,19,22,28,29,30,31,32,34,35,36 +5VS5

NB5

PROJECT : VOLKS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD Connector (LVDS)	1A
Date: Wednesday, May 23, 2012	Sheet 26of 37	


SI modify 0418
CN10 | P/N
14" | DFAD08MR036
15" | DFAD08MR035
27
Do Not add test pad on BATDIS_G signal
DC_JACK
90W
Place this ZVS close to Diode away +VIN
Place this ZVS close to Far-Far away +VIN
To PWR LED
Place this cap close to EC
Place this cap close to EC
Place this cap close to EC
ACDET=13V
MIN. BATV=7.2V
PU1
BQ24738
PROJECT : VOLKS
Quanta Computer Inc.
NB5
Size Custom
Document Number
Charger (OZ8681)
Rev A
Date: Wednesday, May 23, 2012
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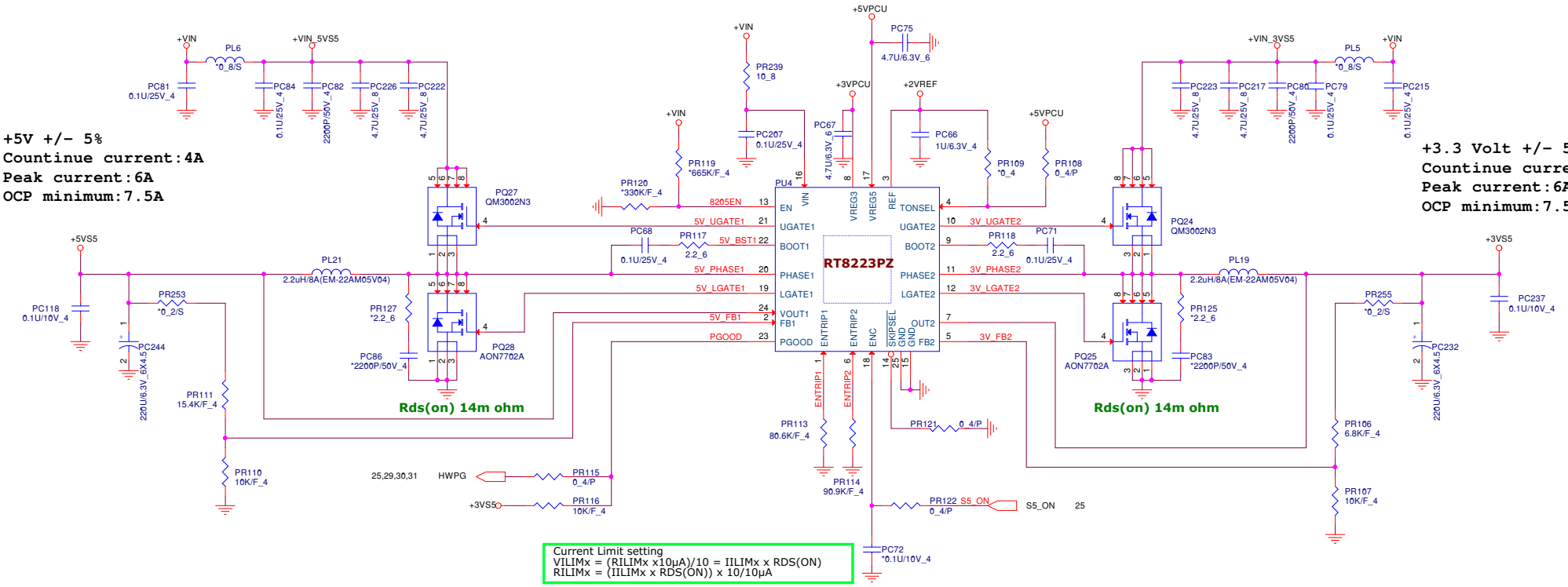
DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

+5V +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A



Current Limit setting
VILIMx = (RILIMx x10μA)/10 = IILIMx x RDS(ON)
RILIMx = (IILIMx x RDS(ON)) x 10/10μA

TONSEL= VREG5
Vout1=400kHz/Vout2=500kHz

21,26,27,30,31,32,33,35,36 +VIN
6,10,23,30,33,36 +3VS5
6,19,22,29,30,31,32,34,35,36 +5VS5
7,21,22,23,24,25,26,27 +3VPCU

NB5

PROJECT :VOLKS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	3/5VS5 (RT8223P)	A
Date: Wednesday, May 23, 2012	Sheet 28 of 37	

TPS51462RGER/AL051462000

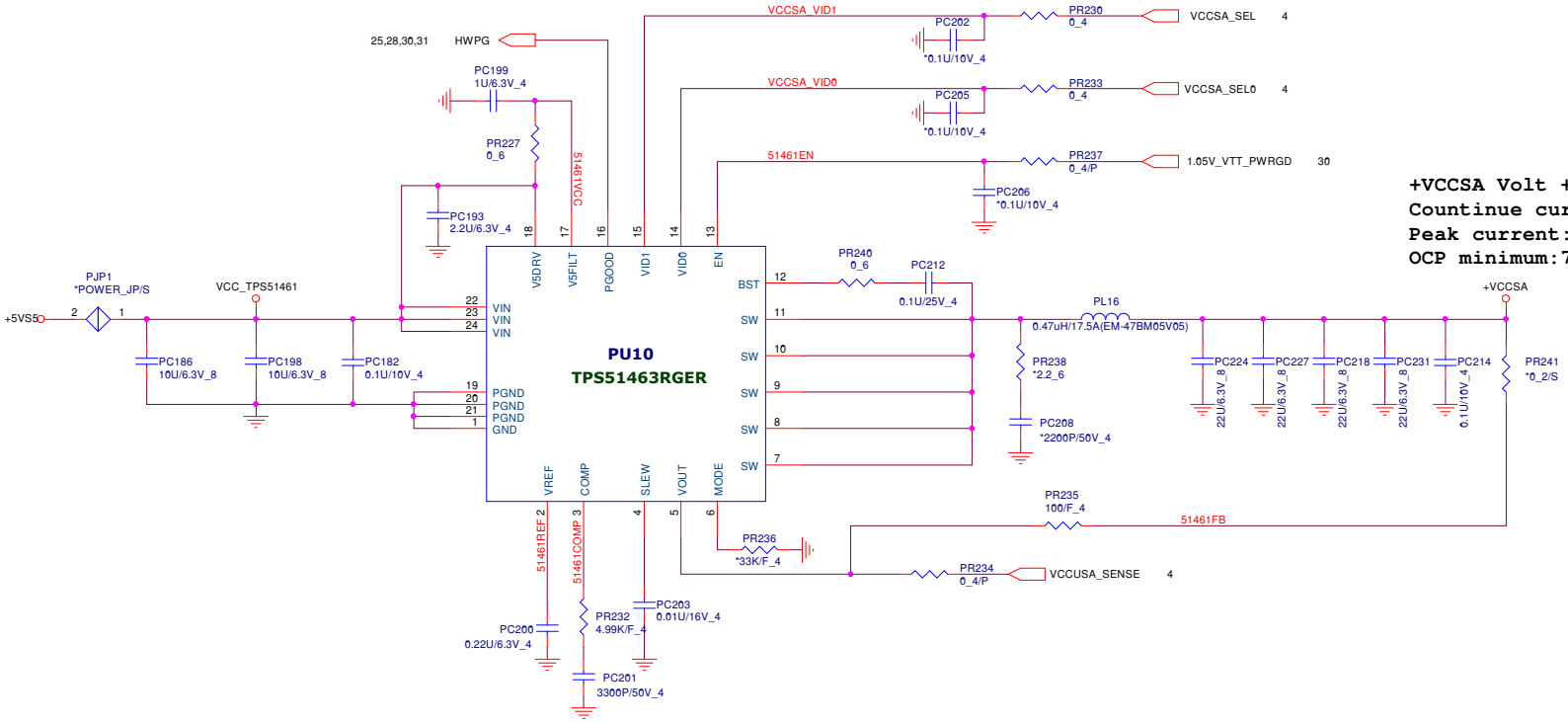
For CPU SV system agent voltage slew rate of 0.5 -10 mV/µs

SEL0	SEL1	+VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

TPS51463RGER/AL051463000

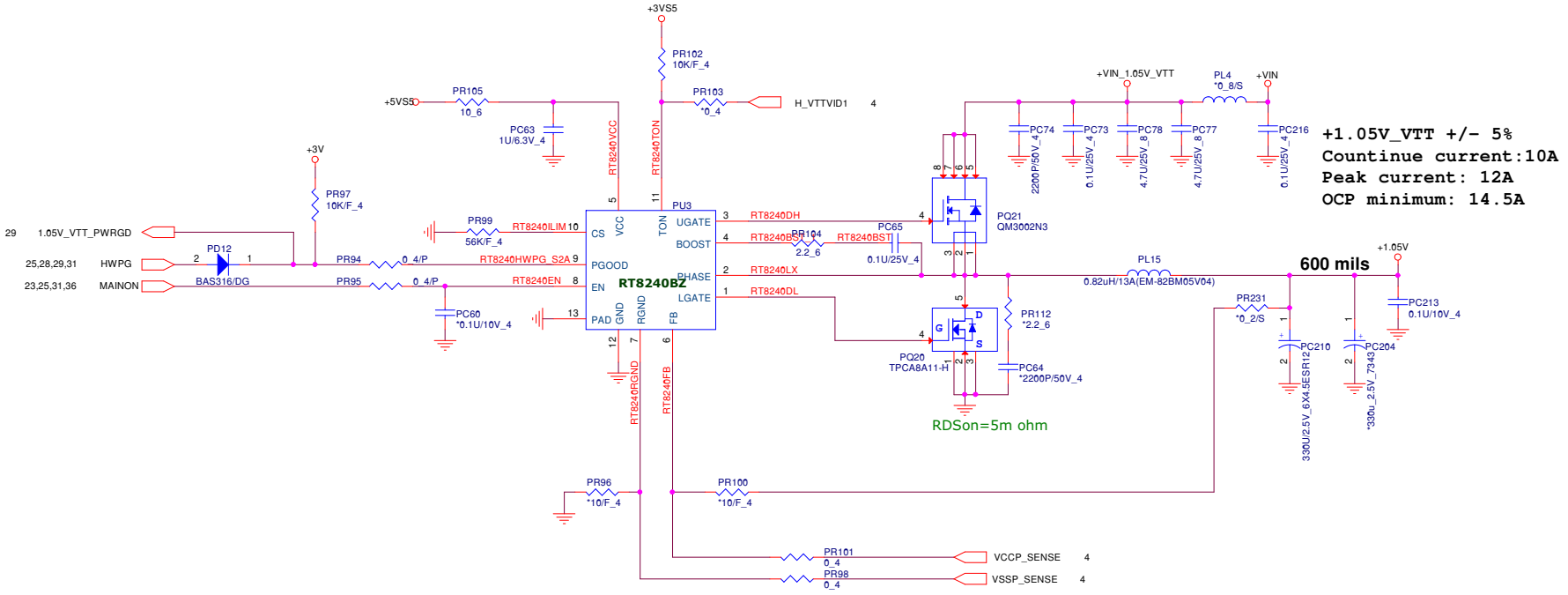
For CPU ULV system agent voltage slew rate of 0.5 -10 mV/µs

SEL0	SEL1	+VCCSA
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V



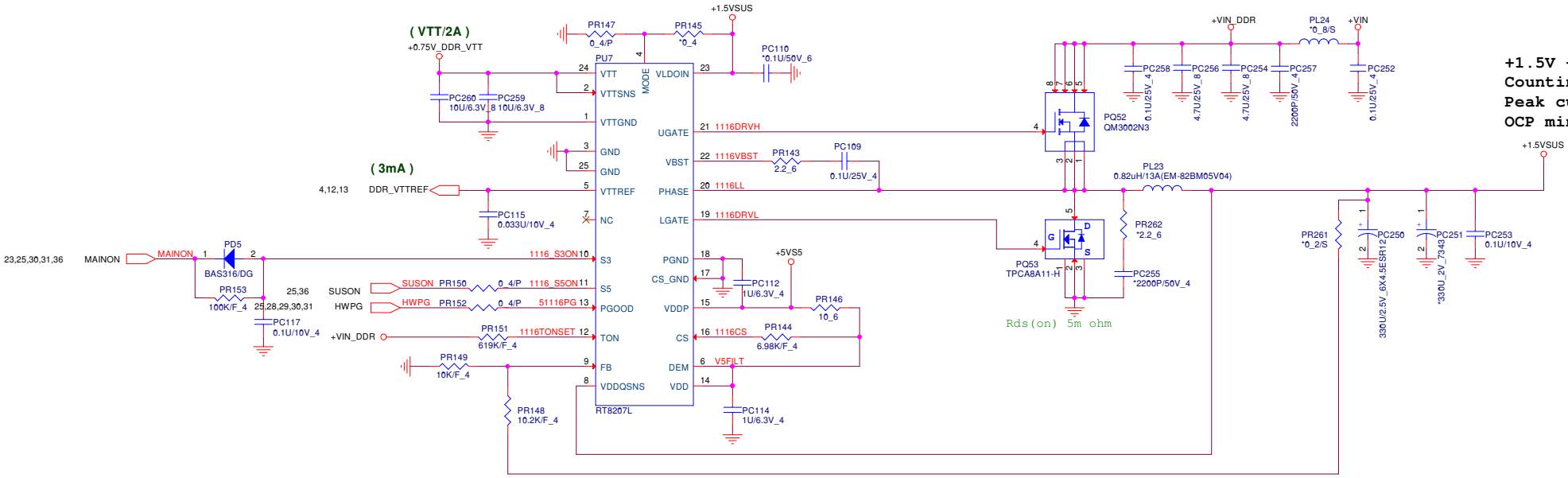
+VCCSA Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7A

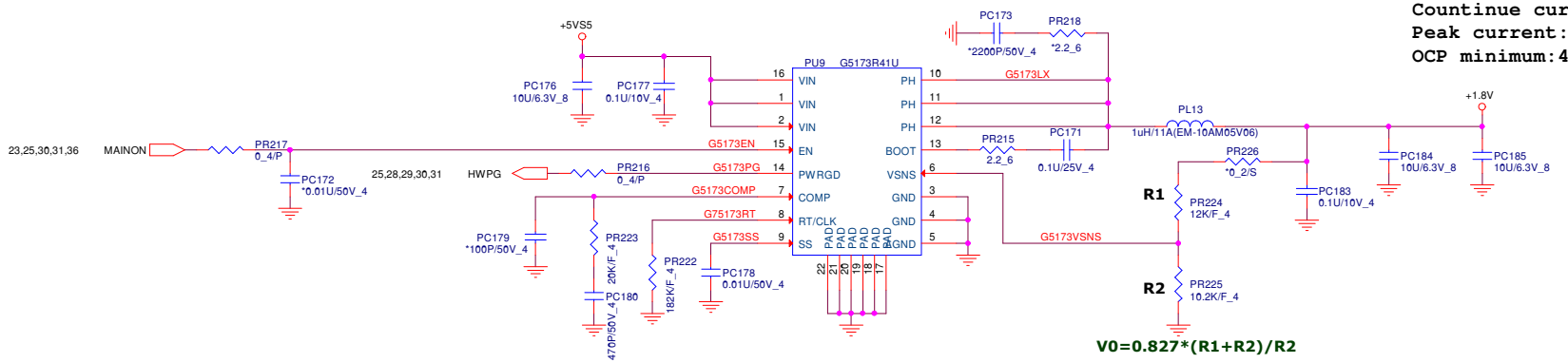
NB5	PROJECT : VOLKS Quanta Computer Inc.	
	Size: Custom Document Number: +VCCSA (TPS51462RGER)	Rev: A
	Date: Wednesday, May 23, 2012 Sheet 29of 37	



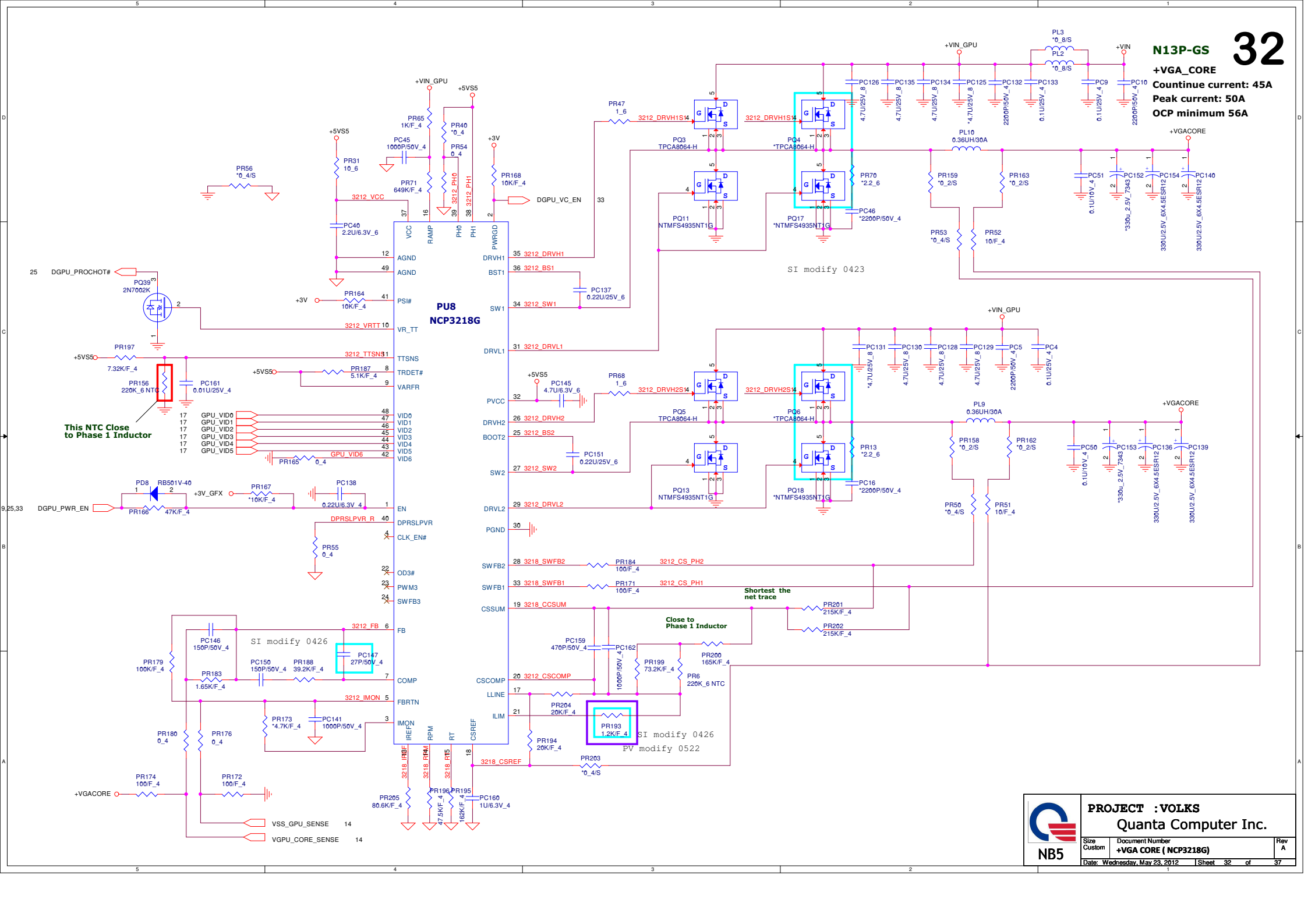
+1.05V_VTT +/- 5%
Countinue current:10A
Peak current: 12A
OCP minimum: 14.5A

NB5	PROJECT : VOLKS Quanta Computer Inc.		
	Size: Custom	Document Number: +1.05V (RT8240B)	Rev: A
	Date: Wednesday, May 23, 2012	Sheet 30of 37	





NB5	PROJECT :VOLKS Quanta Computer Inc.	
	Size: Custom Document Number: DDR3 (RT8207)	Rev: A
	Date: Wednesday, May 23, 2012	Sheet 31 of 37


32
N13P-GS
+VGA_CORE
Countinue current: 45A
Peak current: 50A
OCP minimum 56A
PU8
NCP3218G
SI modify 0423
SI modify 0426
PV modify 0522
This NTC Close to Phase 1 Inductor
Close to Phase 1 Inductor
Shortest the net trace
PROJECT : VOLKS
Quanta Computer Inc.
NB5
+VGA CORE (NCP3218G)
Wednesday, May 23, 2012
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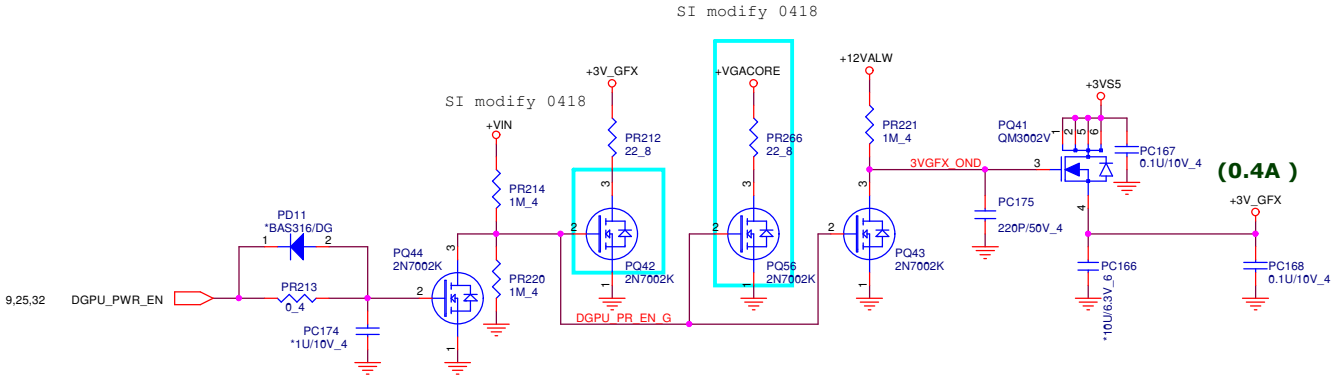
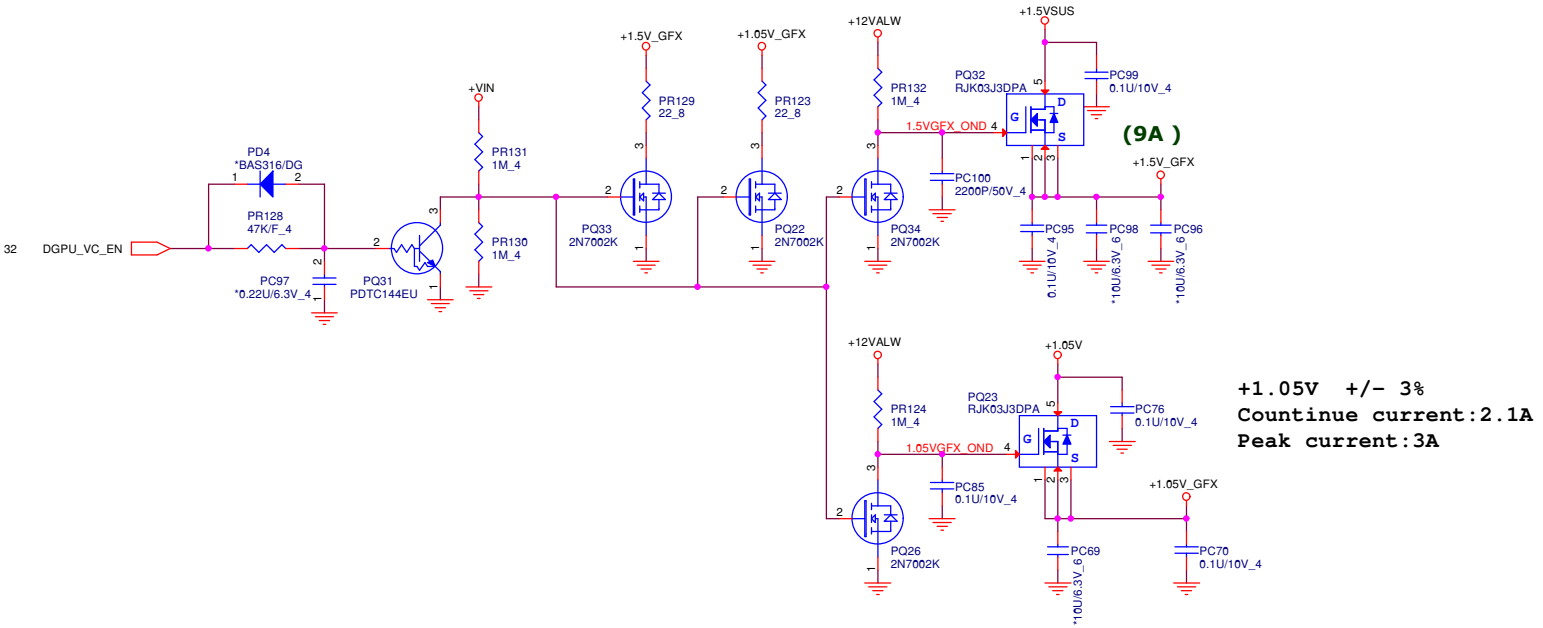
VGA

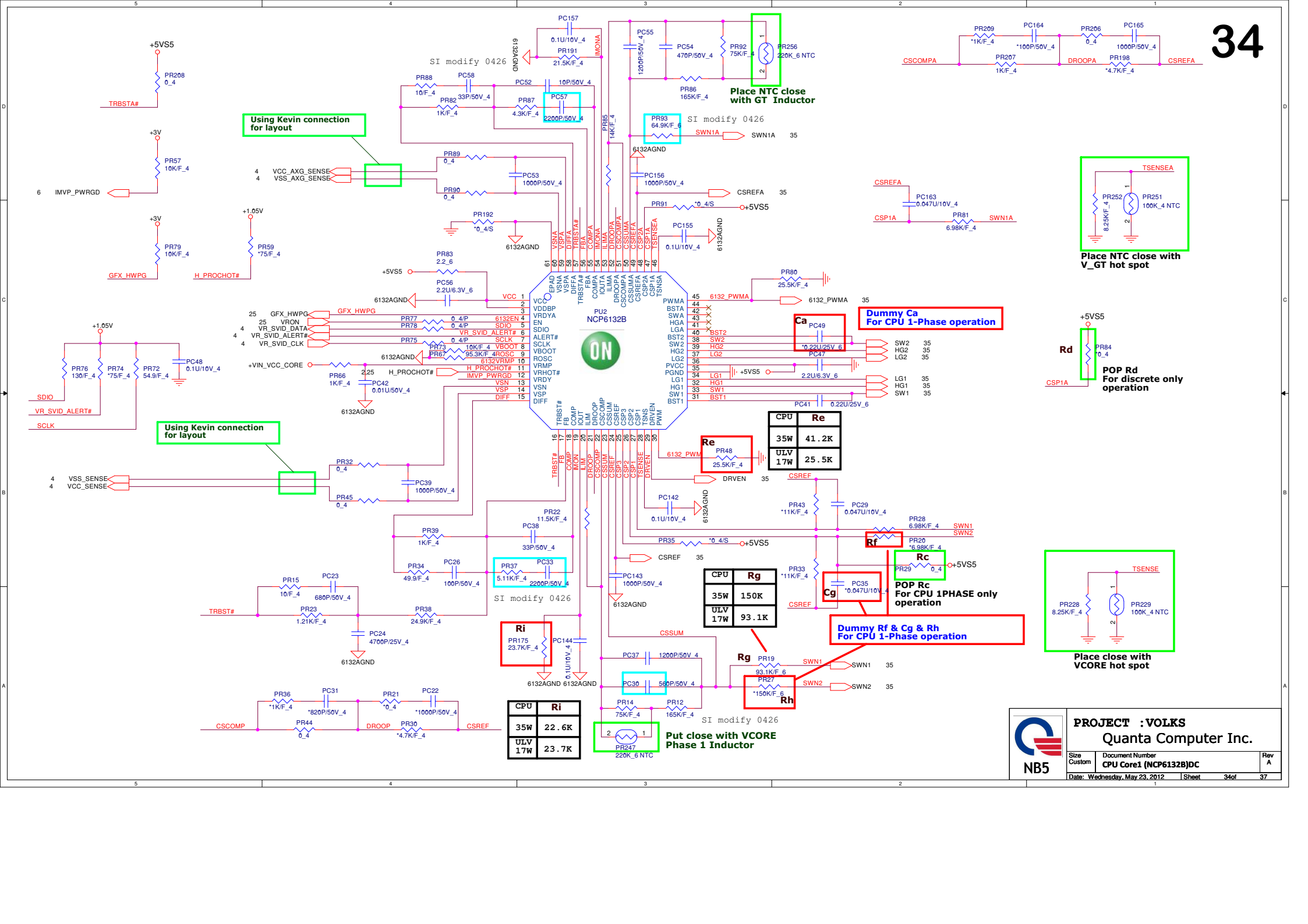
2,4,12,13,31 +1.5VSUS
6,10,23,28,30,36 +3VS5
14,16,17,32 +3V_GFX
15,16,17,18 +1.5V_GFX
14,15,16 +1.05V_GFX
27,36 +12VALW
2,4,6,7,8,10,21,23,30,34 +1.05V





+1.05V +/- 3%
Countinue current:2.1A
Peak current:3A

NB5	PROJECT :VOLKS Quanta Computer Inc.	
Size: Custom	Document Number: +VGA POWER	Rev: A
Date: Wednesday, May 23, 2012	Sheet 33 of 37	


34
PU2
NCP6132B
Using Kevin connection for layout
Using Kevin connection for layout
Place NTC close with GT Inductor
Dummy Ca For CPU 1-Phase operation
Place NTC close with V_GT hot spot
POP Rd For discrete only operation
POP Rc For CPU 1PHASE only operation
Dummy Rf & Cg & Rh For CPU 1-Phase operation
Place close with VCORE hot spot
Put close with VCORE Phase 1 Inductor
SI modify 0426
SI modify 0426
SI modify 0426
SI modify 0426
CPU Re
35W 41.2K
ULV 17W 25.5K
CPU Rg
35W 150K
ULV 17W 93.1K
CPU Ri
35W 22.6K
ULV 17W 23.7K
PROJECT : VOLKS
Quanta Computer Inc.
NB5
Size Custom
Document Number CPU Core1 (NCP6132B)DC
Rev A
Date: Wednesday, May 23, 2012
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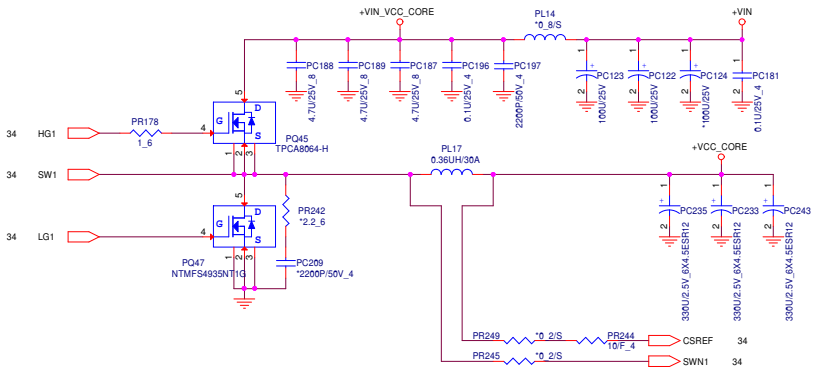
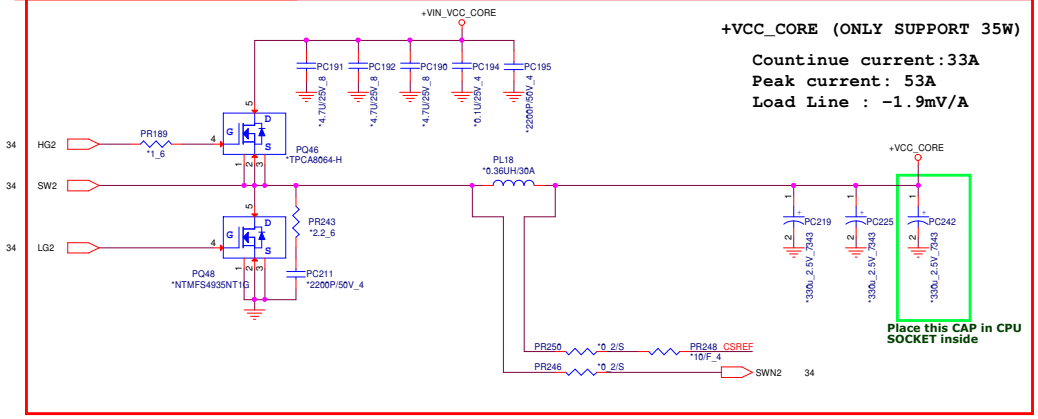


Dummy This Schematic
For CPU 1-Phase operation



+VCC_CORE (ONLY SUPPORT 35W)

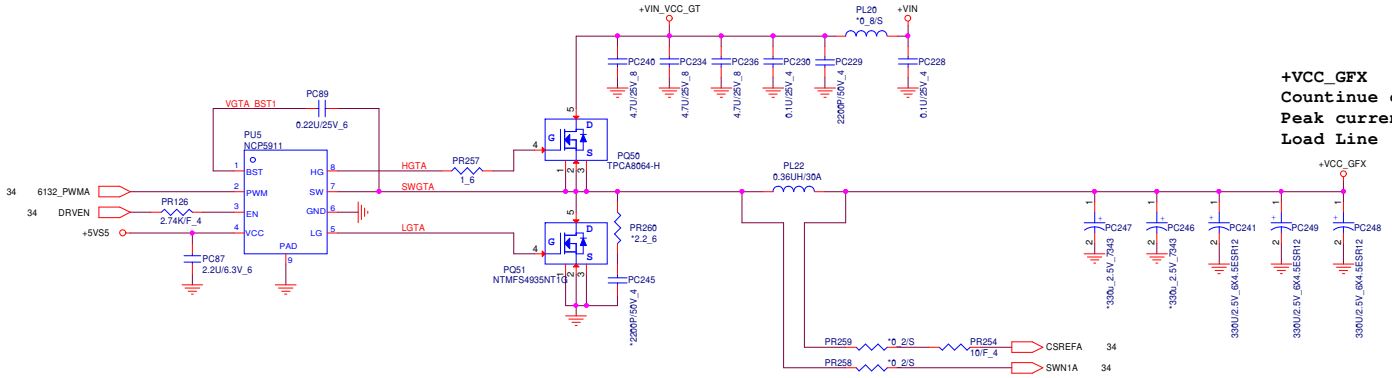
Countine current:33A
Peak current: 53A
Load Line : -1.9mV/A

+VCC_CORE (ONLY SUPPORT 35W)

Countine current:32A
Peak current: 53A
Load Line : -1.9mV/A

+VCC_CORE (ULV 17W)

Countine current:16A
Peak current: 33A
Load Line : -2.9mV/A



+VCC_GFX
Countine current:21.5A
Peak current: 33A
Load Line : -3.9mV/A

NB5	PROJECT : VOLKS Quanta Computer Inc.	
	Size: C Document Number: CPU Core2 (NCP5911)DC	Rev: A
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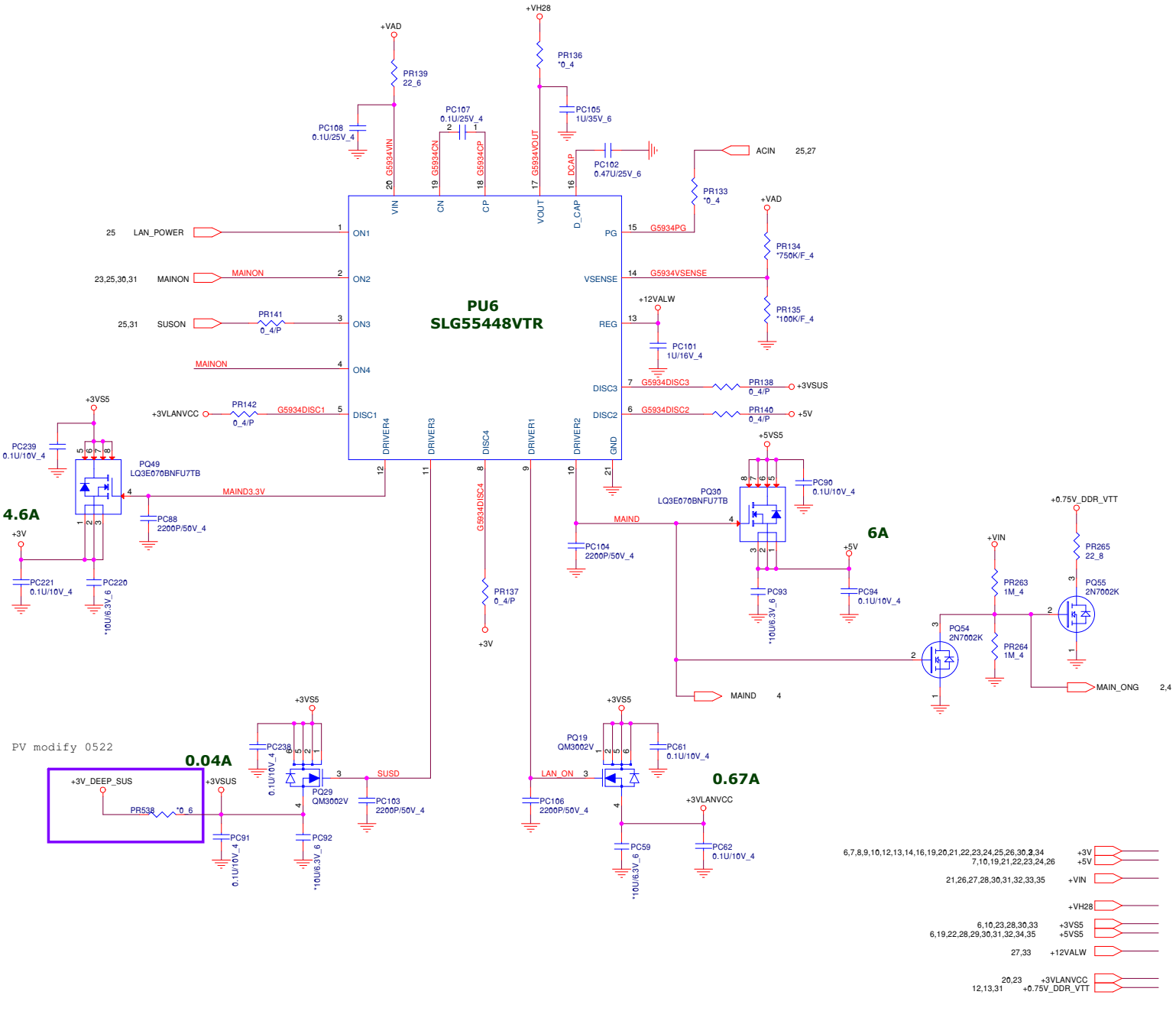

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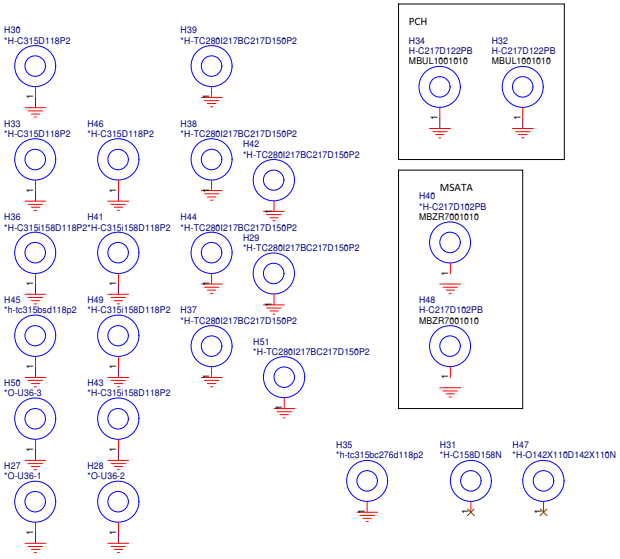
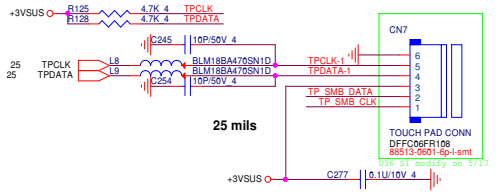
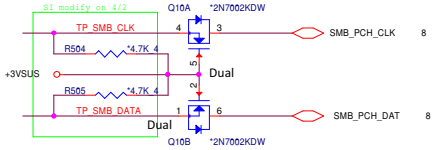
15" Hole



Touch Pad Connector





NB5	PROJECT : VOLKS Quanta Computer Inc.	
Size: C	Document Number: Hole	Rev: A
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