

Compal confidential

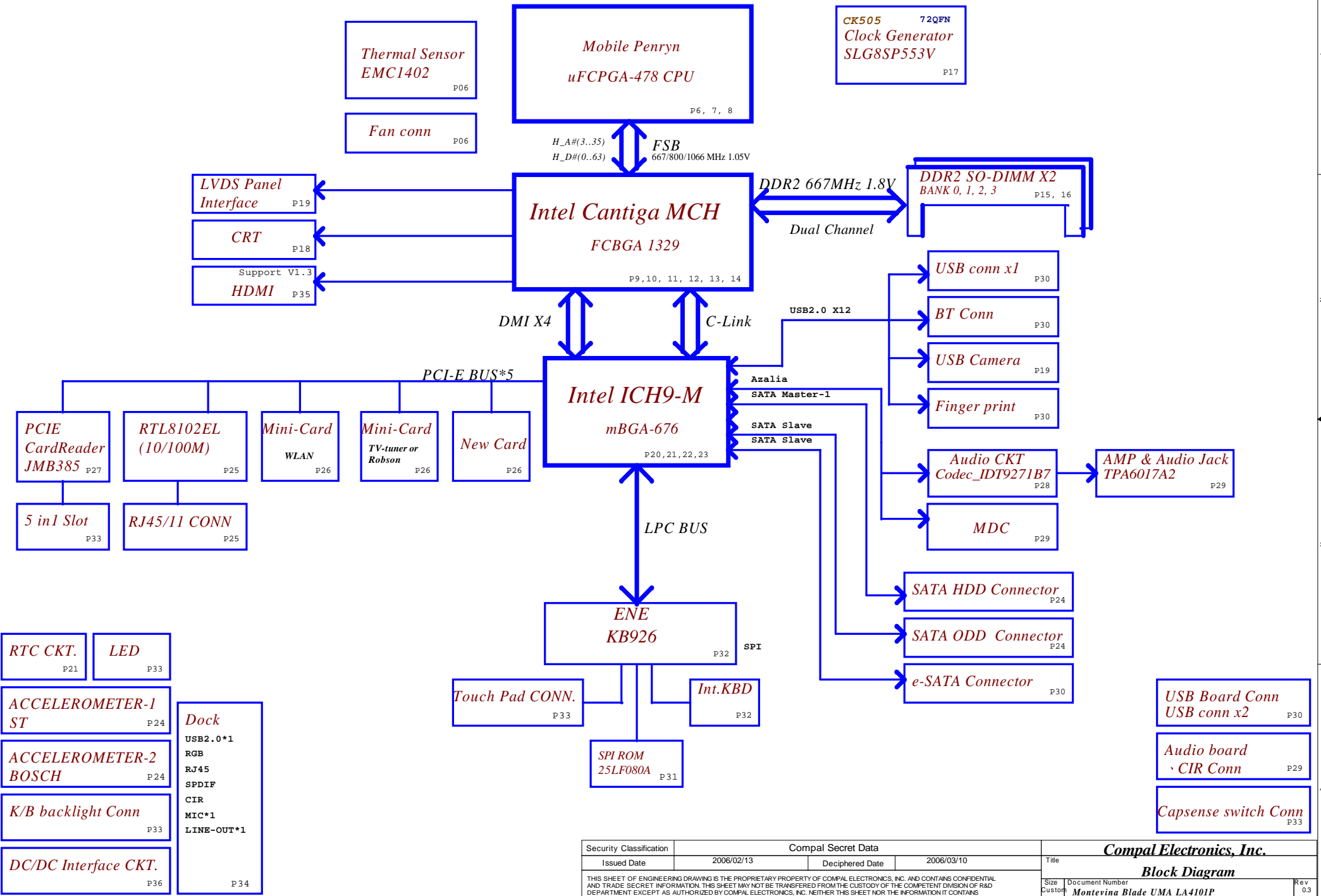
Schematics Document

Mobile Penryn uFCPGA with Intel
Cantiga_GM+ICH9-M core logic

2008-01-01

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2007/08/28	Deciphered Date	2006/03/10	Title		
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				Custom	Montevina Blade UMA LA410P	0.3
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Montevina Consumer 14" UMA



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				Custom	Montevina Blade UMA LA4101P	0.3
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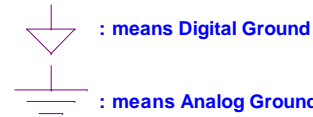
Block Diagram

Voltage Rails

O MEANS ON X MEANS OFF

power plane	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +2.5VS +1.8VS
State				
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :



@ :	means just reserve , no build
45 @ :	means need be mounted when 45 level assy or rework stage.
DEBUG@ :	means just reserve for debug.
BATT @ :	means need be mounted when 45 level assy or rework stage.
CONN@ :	means ME part
ESATA @ :	means just reserve for ESATA
GS @ :	means just reserve for G sensor
FP @ :	means just reserve for Finger Print
Multi @ :	means just reserve for Multi Bay
NewC@ :	means just reserve for New card
DOCK@ :	means just reserve for Docking
Main@ :	means just reserve for Main stream
OPP@ :	means just reserve for OPP
2MiniC@ :	means just reserve for 2nd Mini card slot

USB assignment:

USB-0	Right side
USB-1	Right side
USB-2	Left side(with ESATA)
USB-3	Dock
USB-4	Camera
USB-5	WLAN
USB-6	Bluetooth
USB-7	Finger Printer
USB-8	MiniCard(WWAN/TV)
USB-9	Express card
USB-10	X
USB-11	X

PCIe assignment:

PCIe-1	TV /WWAN/Robeson
PCIe-2	X
PCIe-3	WLAN
PCIe-4	GLAN (Realtek)
PCIe-5	Card reader
PCIe-6	New Card

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	Thermal Sensor	SODIMM	CLK CHIP	MINI CARD	LCD	Cap sensor board	NEW CARD	G sensor
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X	V	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X	X	V	V
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V	X	X	X

43154432L01 : Main@/DEBUG@/DOCK@/NewC@/FP@/ESATA@/GS@/Multi@/2MiniC@
 43154432L02 : Main@/DEBUG@/DOCK@/NewC@/FP@/ESATA@/GS@/2MiniC@
 43154432L03 : Main@/DEBUG@/DOCK@/NewC@/FP@/2MiniC@
 43154432L04 : OPP@/DEBUG@
 43154432L05 : OPP@/DEBUG@

I2C / SMBUS ADDRESSING

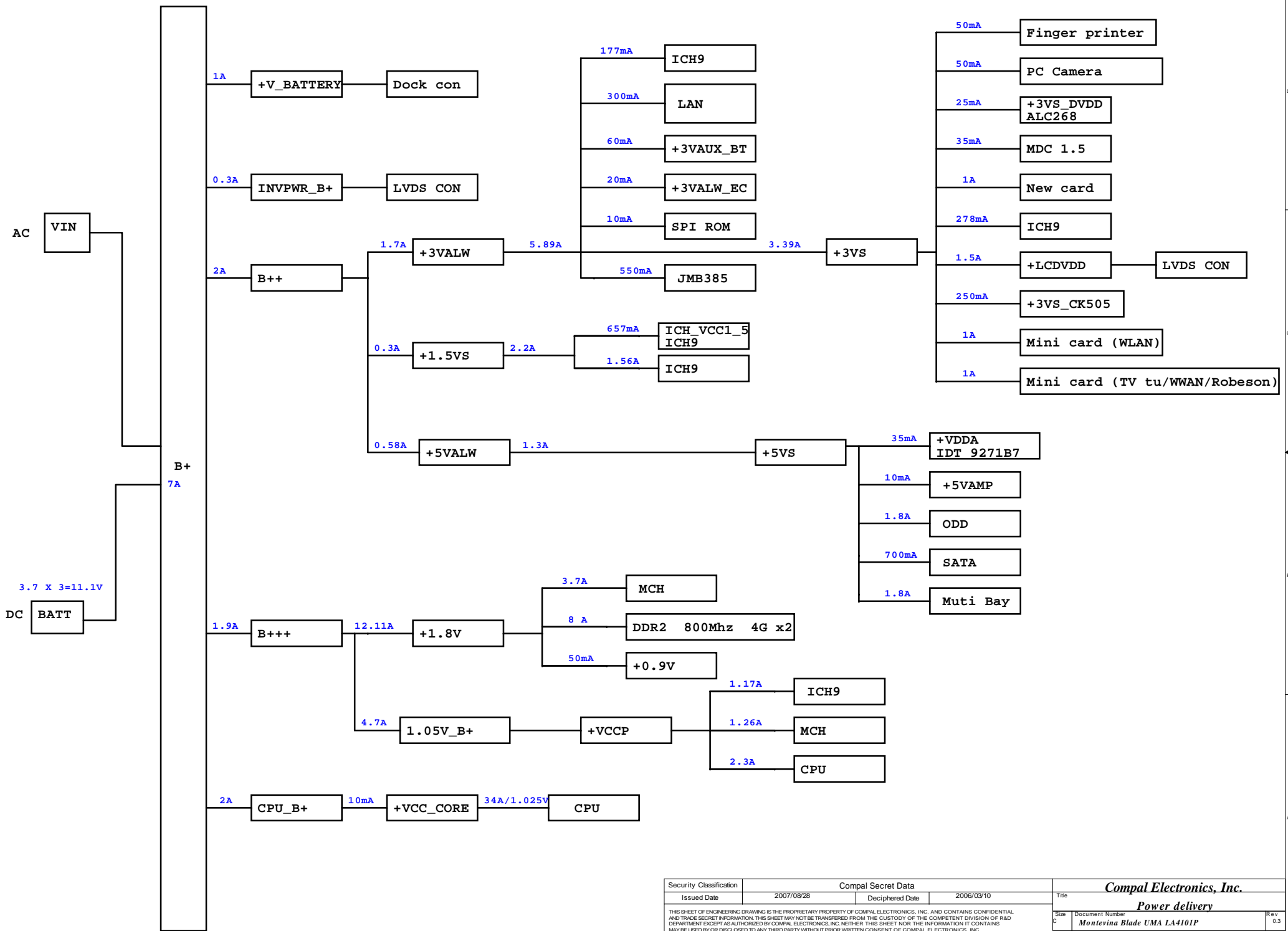
DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

43154432L01 : UMA GM PA FF (SI-1)
 43154432L02 : UMA GM PR FF (SI-1)
 43154432L03 : UMA GL PR FF-
 43154432L04 : UMA GM OPP (SI-1)
 43154432L05 : UMA GL OPP

Cantiga GM45 B0(QR32) : SA00001P930
 ICH9M A2 ES2 Base : SA00002AN10

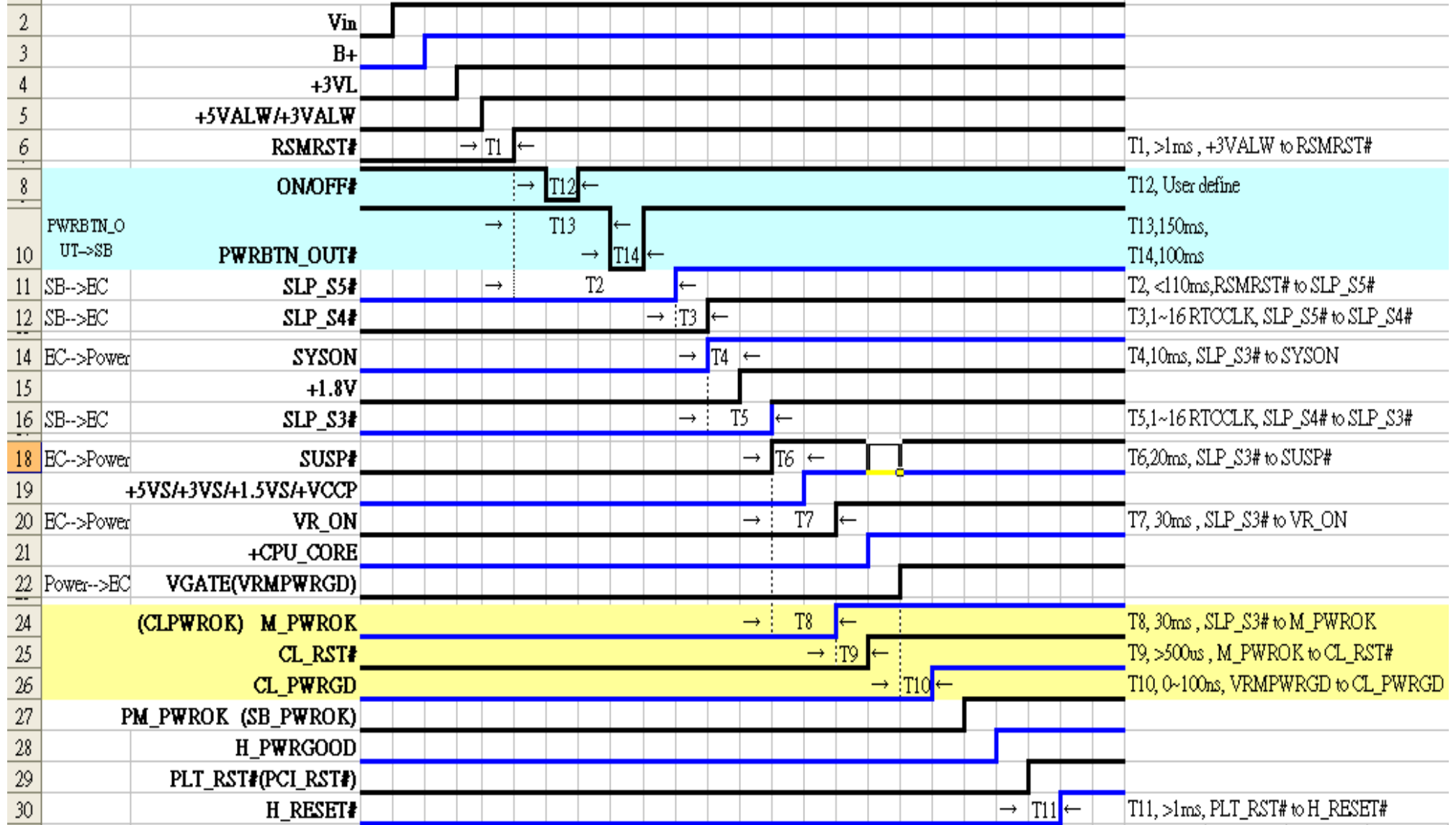
DA600007100 --->Main
 DAZ03V00100 --->OPP

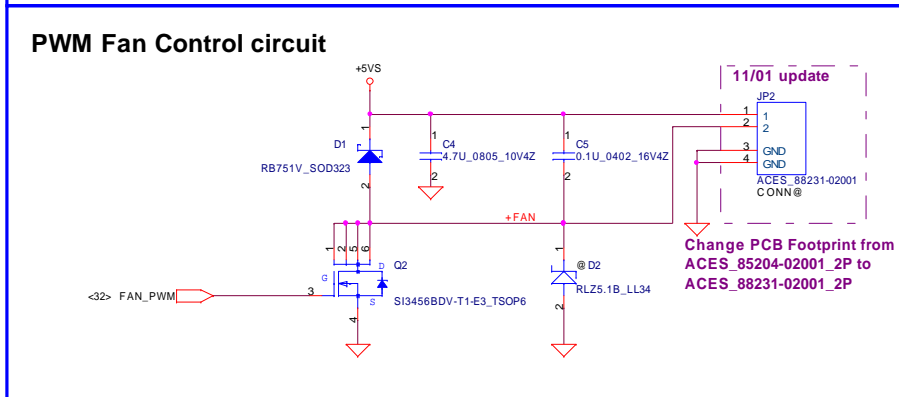
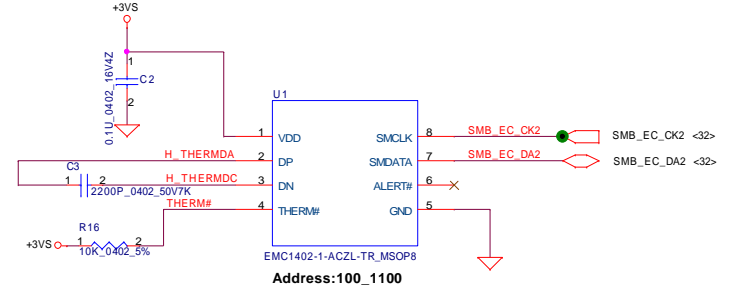
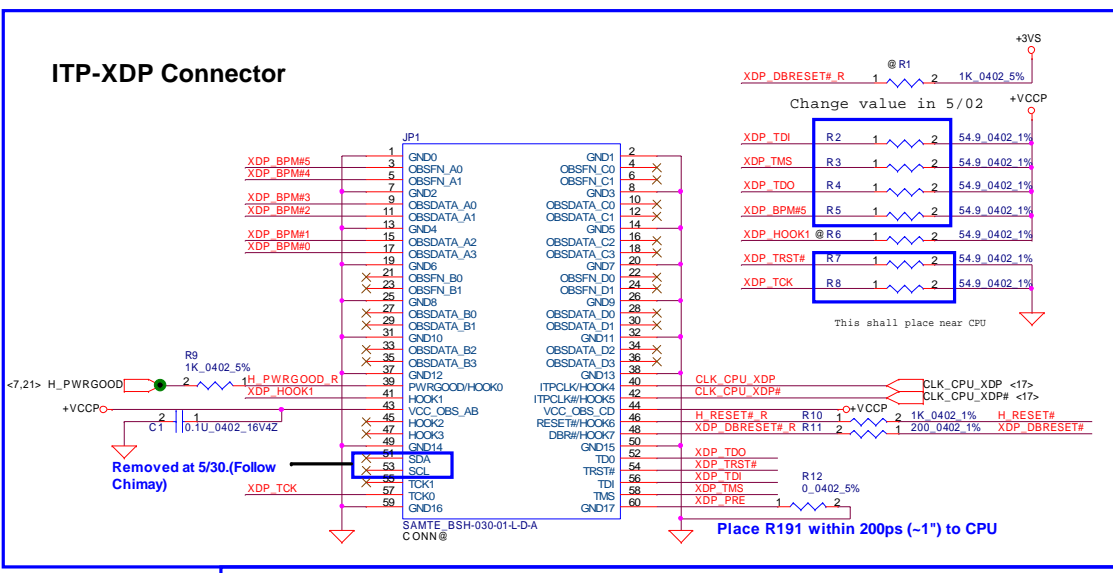
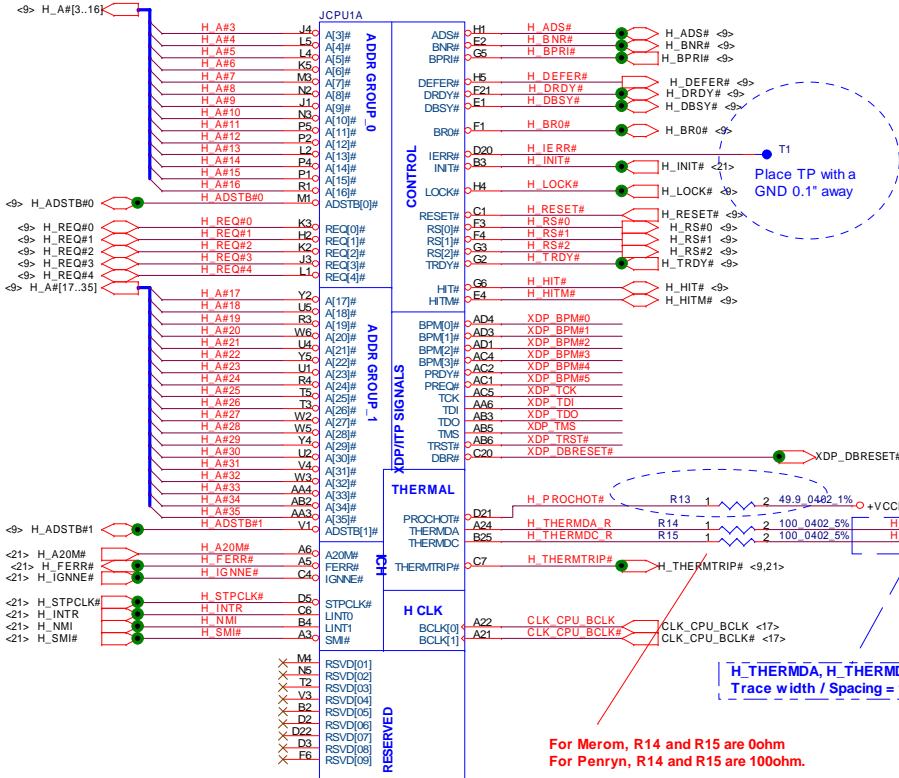
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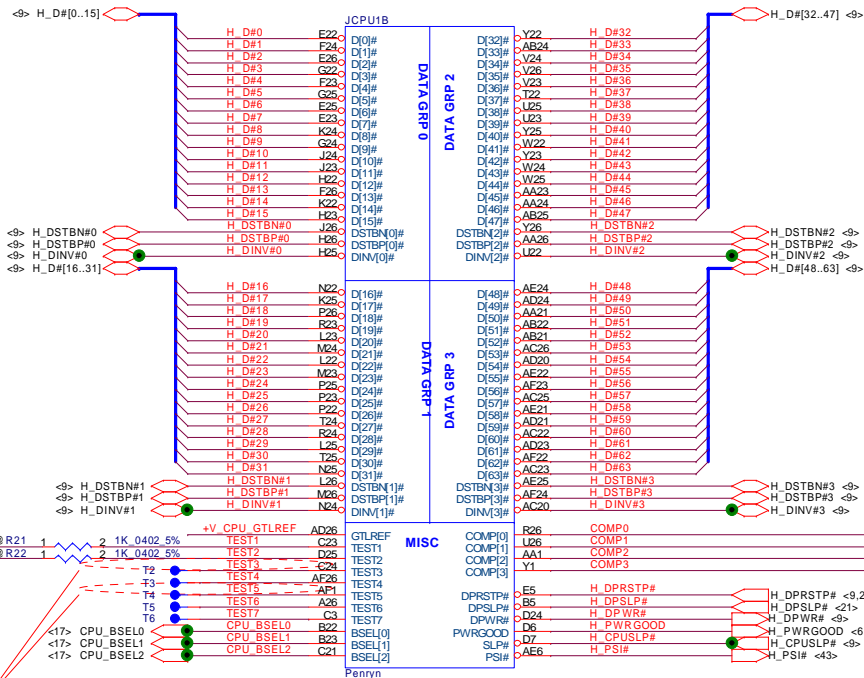
JAL50 power sequence AC mode

96.09.03.

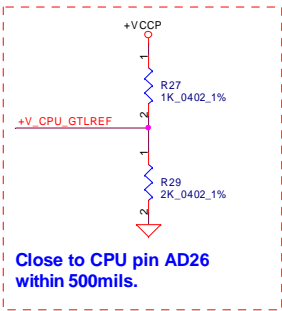




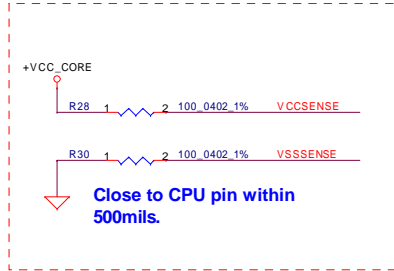
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Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



Length match within 25 mils. The trace width/space/other is 20/7/25.



* Route the TEST3 and TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

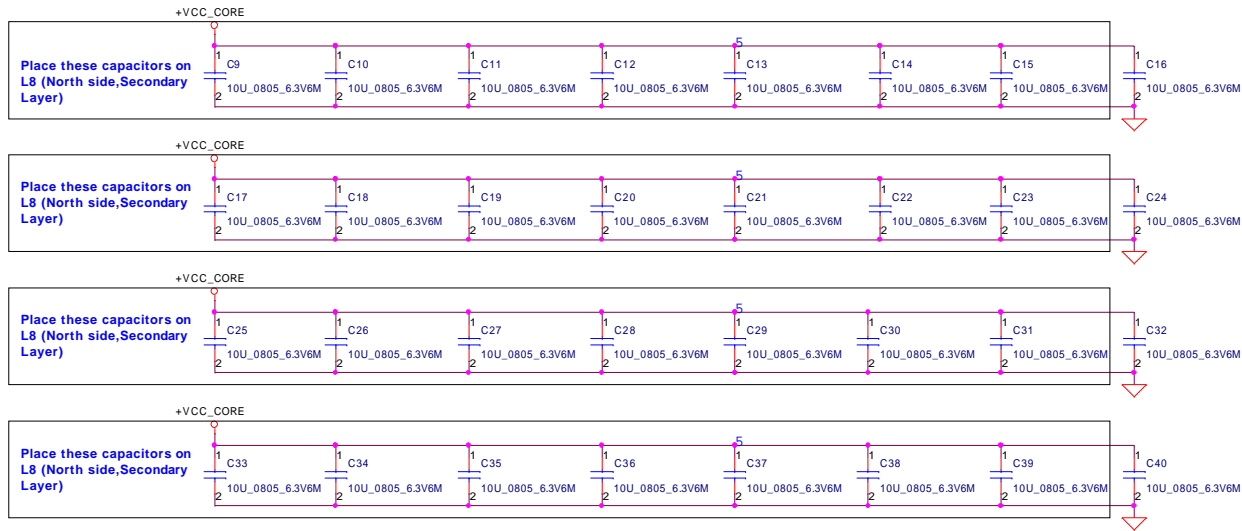
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

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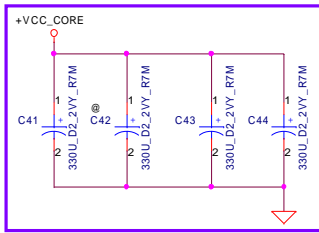
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Penryn(2/3)-AGTL+RTP-XDP <td>Size</td> <td>Document Number</td>		Size	Document Number
Custom	Montevina Blade UMA LA4100	Date	Rev
Saturday, January 05, 2008	11/07/08	7	0.3

JCPU1D		
A4	VSS0011	P6
A8	VSS0021	P21
A11	VSS0031	P24
A14	VSS0041	D2
A16	VSS0051	R5
A19	VSS0061	R22
A23	VSS0071	R25
A27	VSS0081	T1
B2	VSS0091	T4
B8	VSS0101	T23
B11	VSS0111	T26
B13	VSS0121	U8
B16	VSS0131	U21
B19	VSS0141	U24
B21	VSS0151	V2
B24	VSS0161	V5
C5	VSS0171	V22
C8	VSS0181	V25
C11	VSS0191	W1
C14	VSS0201	W4
C16	VSS0211	W23
C19	VSS0221	W26
C2	VSS0231	V6
C22	VSS0241	V21
C25	VSS0251	V24
D1	VSS0261	AA2
D4	VSS0271	AA5
D8	VSS0281	AA25
D11	VSS0291	AA8
D13	VSS0301	AA11
D16	VSS0311	AA12
D19	VSS0321	AA14
D23	VSS0331	AA16
D26	VSS0341	AA19
E3	VSS0351	AA22
E6	VSS0361	AA25
E8	VSS0371	AB1
E11	VSS0381	AB4
E14	VSS0391	AB8
E16	VSS0401	AB11
E19	VSS0411	AB13
E21	VSS0421	AB16
E24	VSS0431	AB19
F5	VSS0441	AB23
F8	VSS0451	AB26
F11	VSS0461	AC3
F13	VSS0471	AC8
F16	VSS0481	AC11
F19	VSS0491	AC14
F2	VSS0501	AC16
F22	VSS0511	AC21
F25	VSS0521	AC24
G4	VSS0531	AD2
G1	VSS0541	AD5
G26	VSS0551	AD8
H3	VSS0561	AD11
H6	VSS0571	AD13
H21	VSS0581	AD19
H24	VSS0591	AD22
J2	VSS0601	AD25
J5	VSS0611	AE1
J22	VSS0621	AE4
J25	VSS0631	AE8
K1	VSS0641	AE11
K4	VSS0651	AE14
K23	VSS0661	AE16
K26	VSS0671	AE19
L3	VSS0681	AE23
L6	VSS0691	A2
L21	VSS0701	AF6
L24	VSS0711	AF9
M2	VSS0721	AF11
M5	VSS0731	AF13
M22	VSS0741	AF16
M25	VSS0751	AF19
N1	VSS0761	AF21
N4	VSS0771	A25
N23	VSS0781	AF25
N26	VSS0791	
P3	VSS0801	
	VSS0811	
	VSS1631	

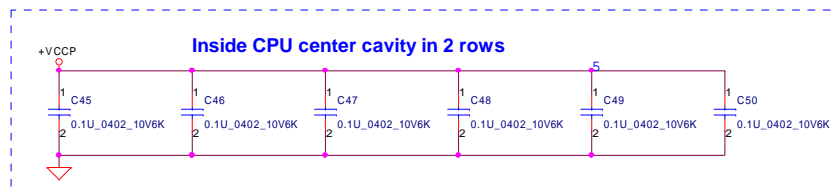


Mid Frequency Decoupling

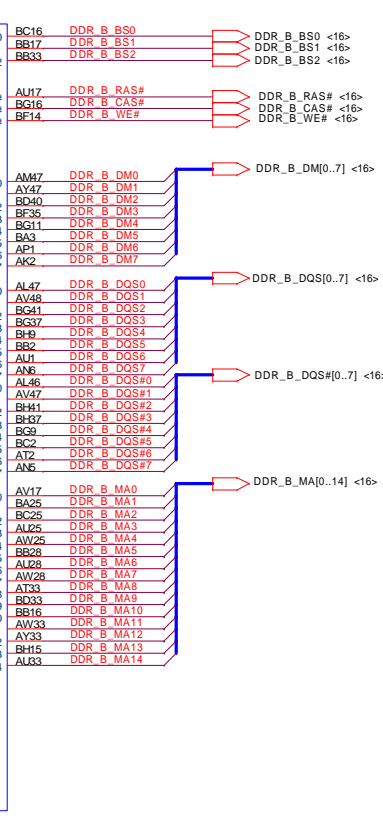
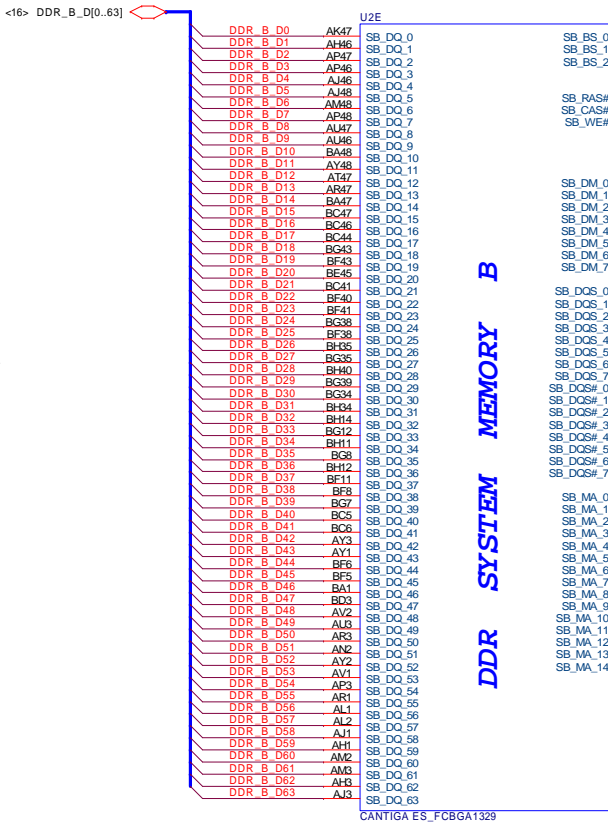
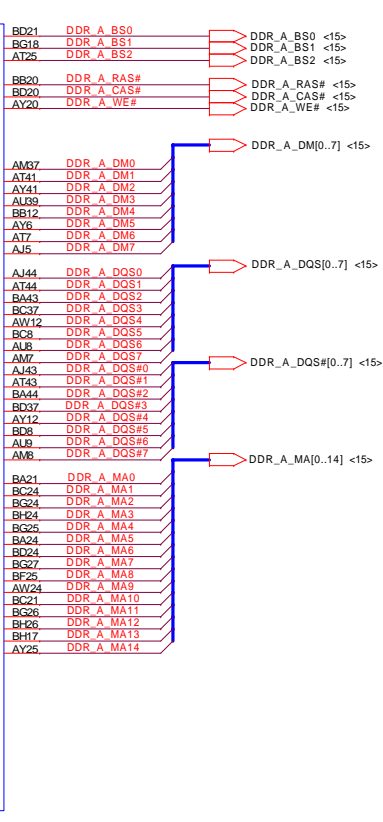
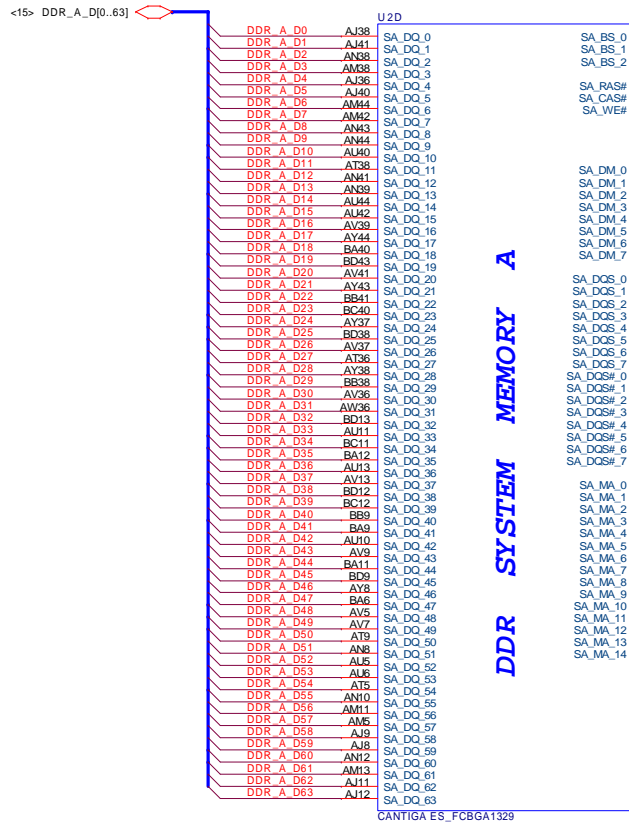
Near CPU CORE regulator
ESR <= 1.5m ohm
Capacitor > 1980uF



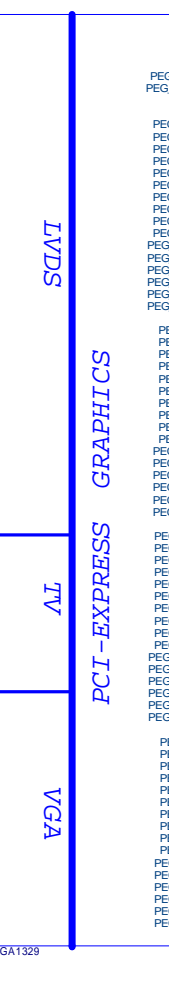
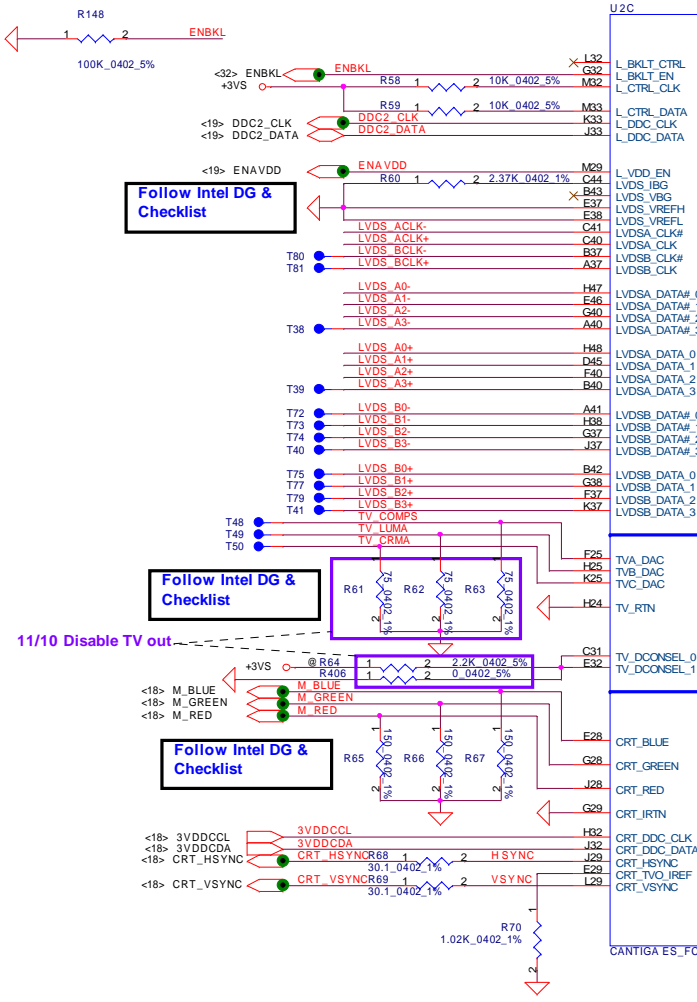
11/21 Change ESR=7m ohm



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				Penryn(3/3)-AGTL+/ITP-XDP		
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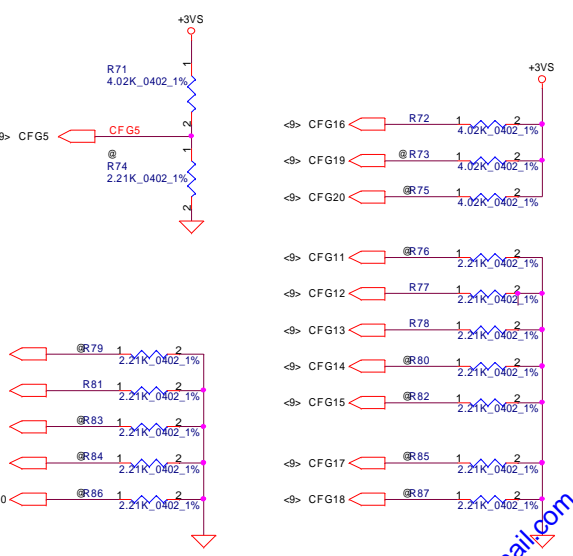
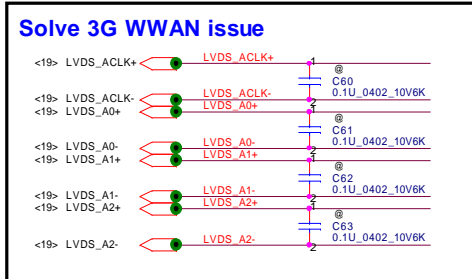


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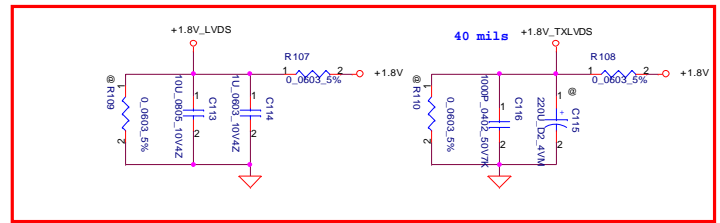
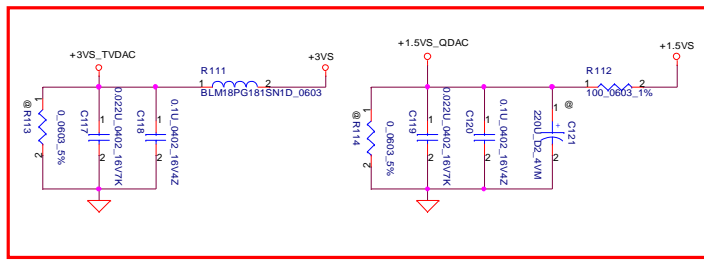
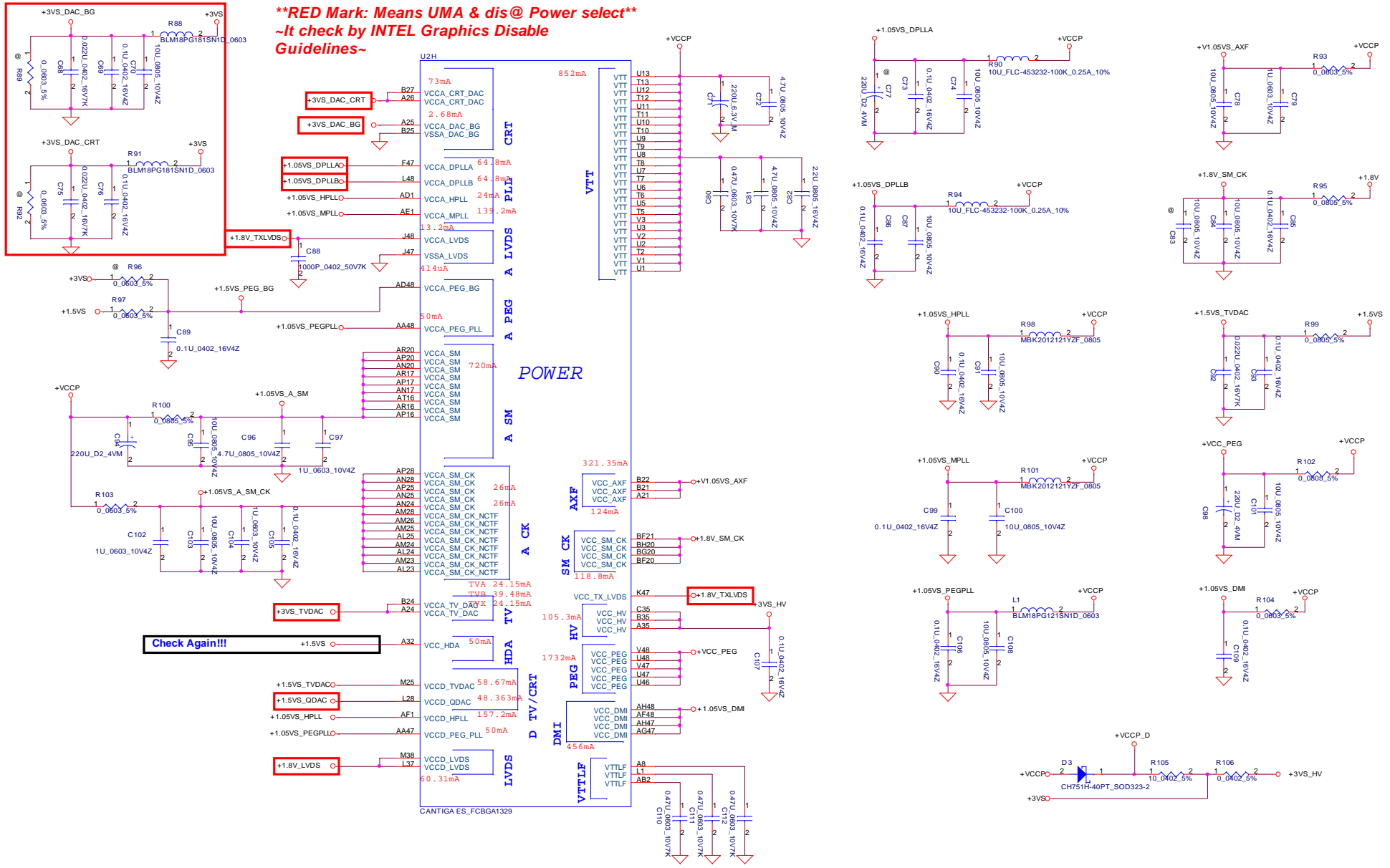


Strap Pin Table

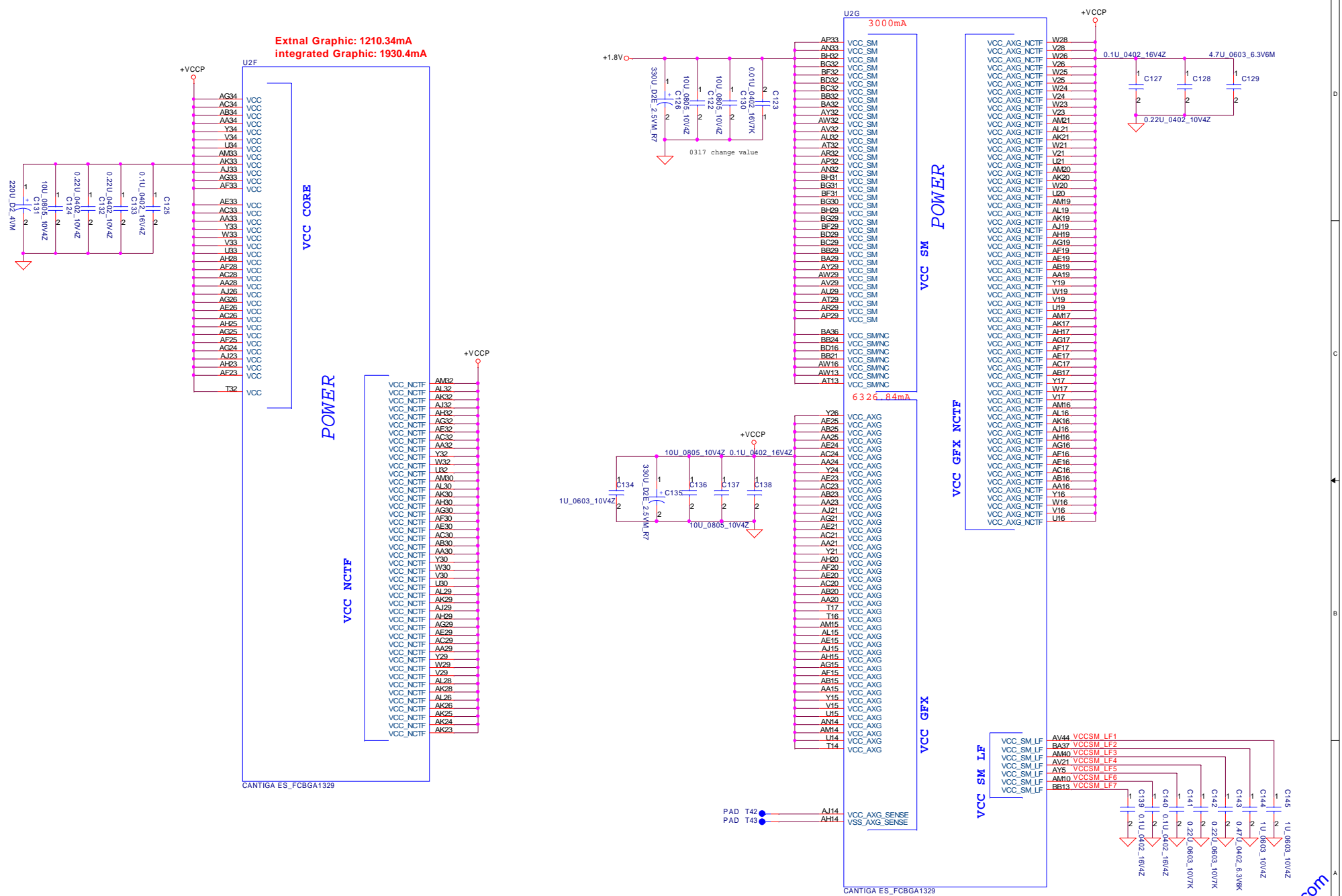
CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 = (TLS)chiper suite with no confidentiality 1 = (TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation, Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.



****RED Mark: Means UMA & dis@ Power select****
~It check by INTEL Graphics Disable
Guidelines~

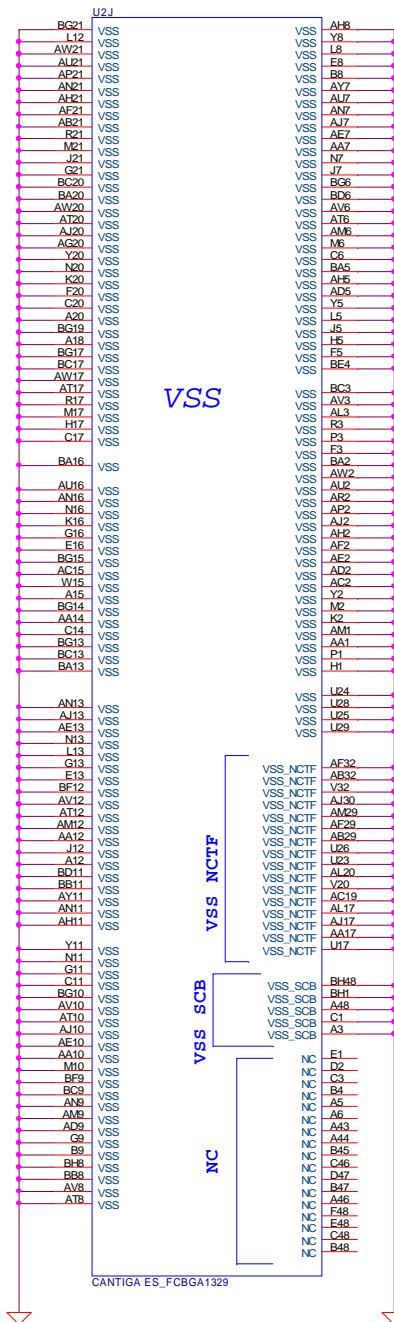
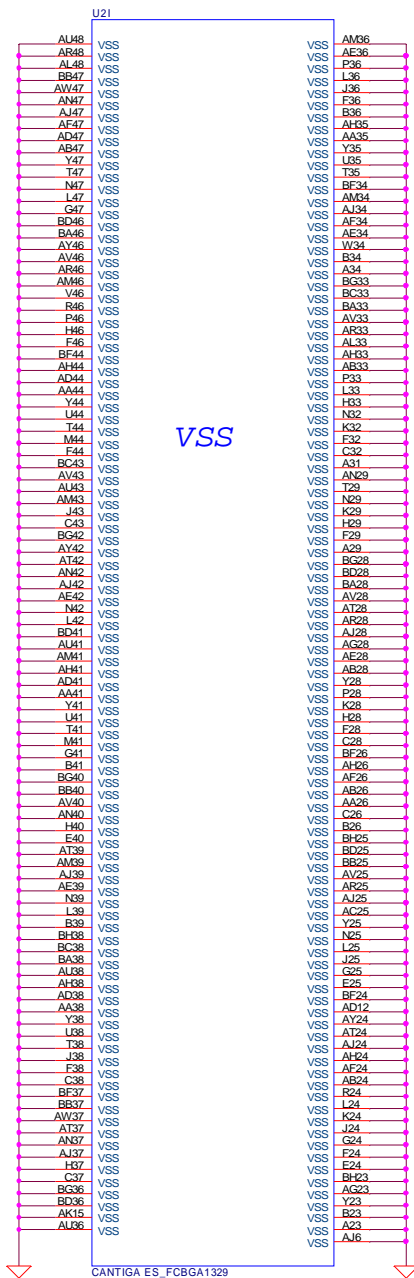


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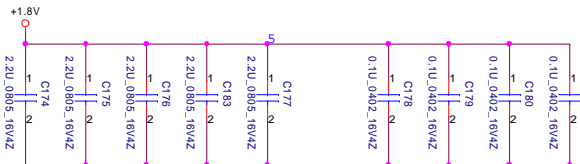
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Cantiga(5/6)-PWR/GND		Rev 0.3	
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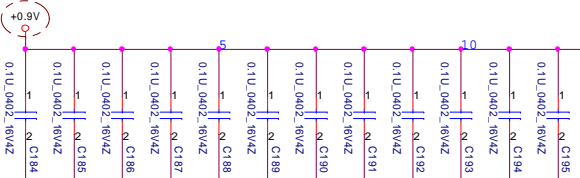
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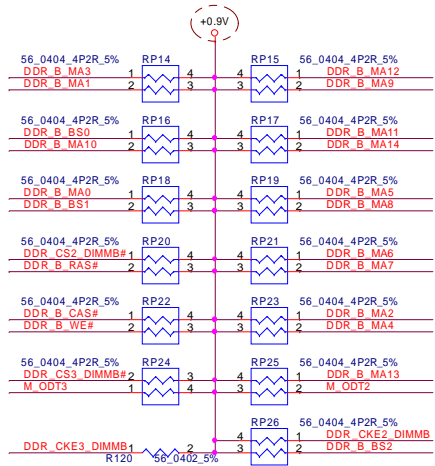
Layout Note:
Place near JP10



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



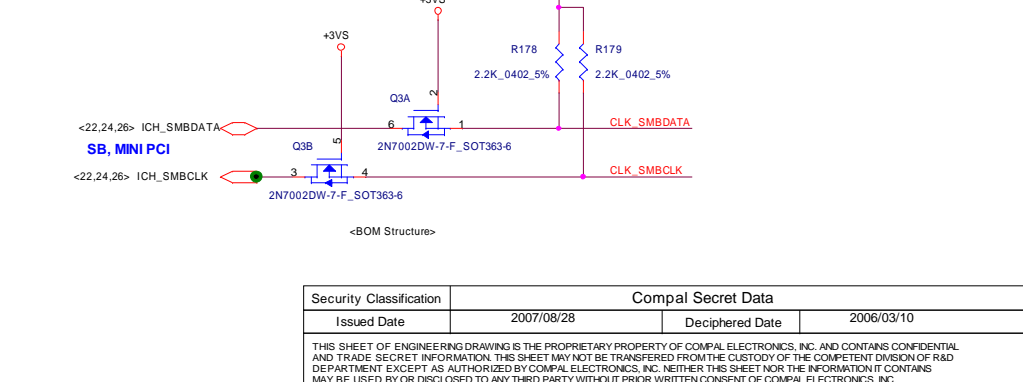
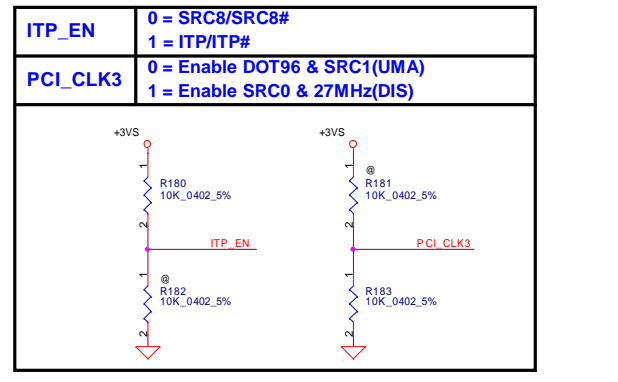
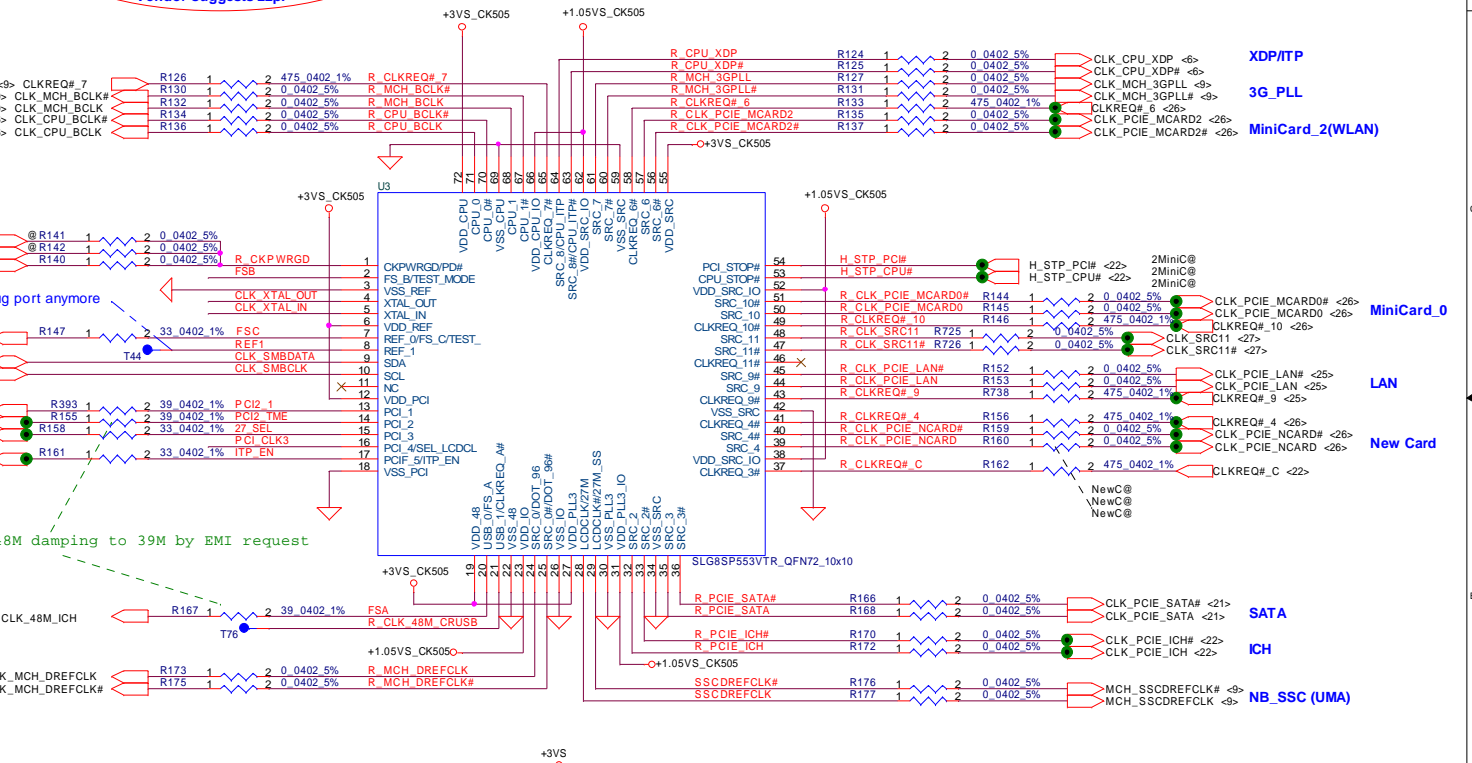
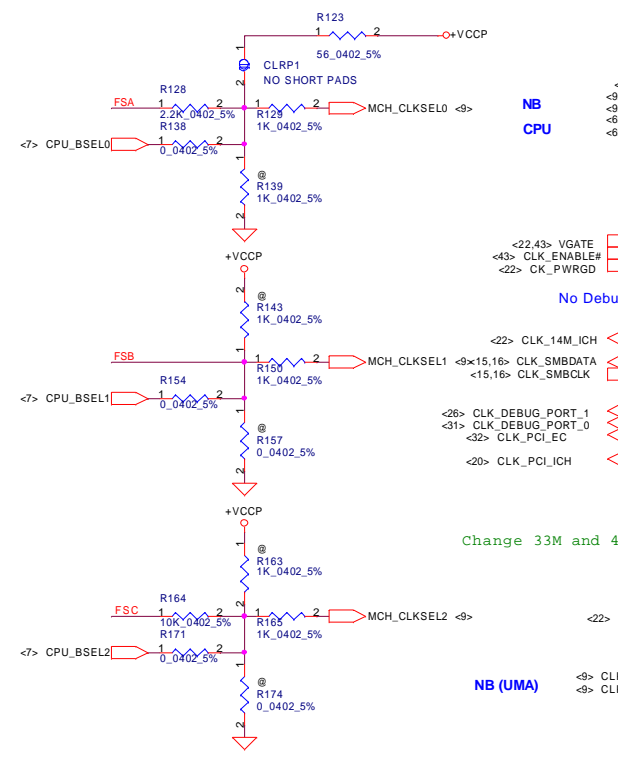
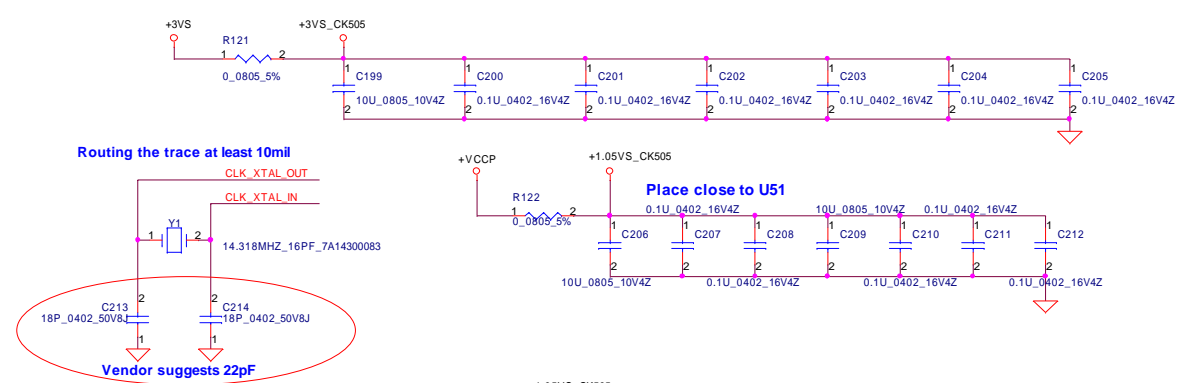
Layout Note:
Place these resistor closely JP3, all trace length Max=1.5"



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Date:	Saturday, January 05, 2008	Sheet	16	of 46

FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1						

Reserved



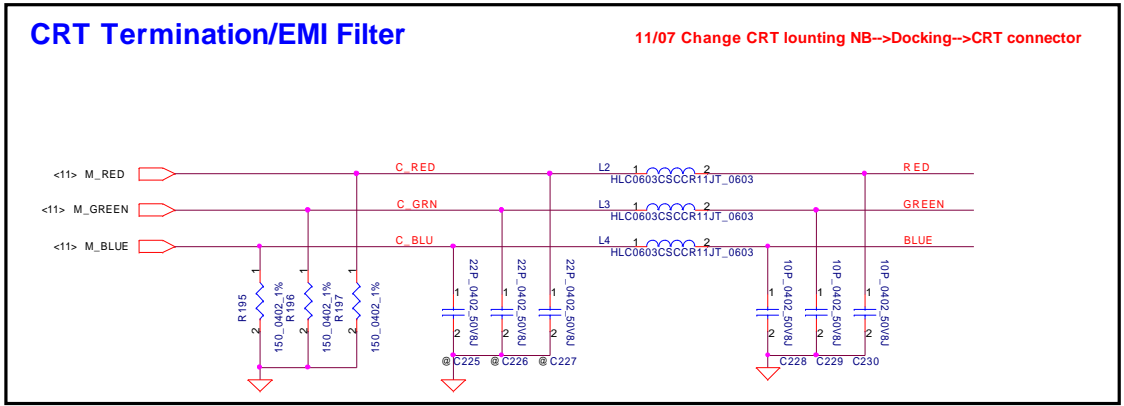
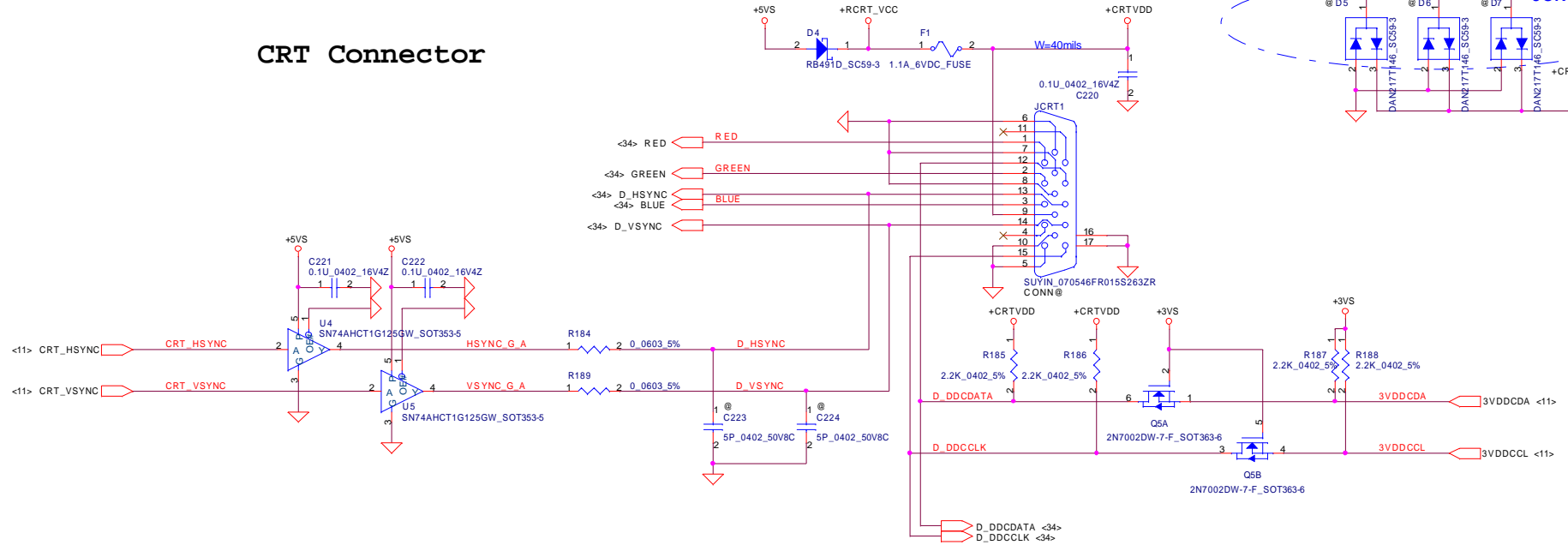
@C215	5P_0402_50V8C	2	1	CLK_48M_ICH
@C216	4.7P_0402_50V8C	2	1	CLK_14M_ICH
@C217	4.7P_0402_50V8C	2	1	CLK_PCI_ICH
@C218	4.7P_0402_50V8C	2	1	CLK_PCI_EC
@C219	5P_0402_50V8C	2	1	CLK_DEBUG_PORT_0

Security Classification	Compal Secret Data	
Issued Date	2007/08/28	Deciphered Date
		2006/03/10

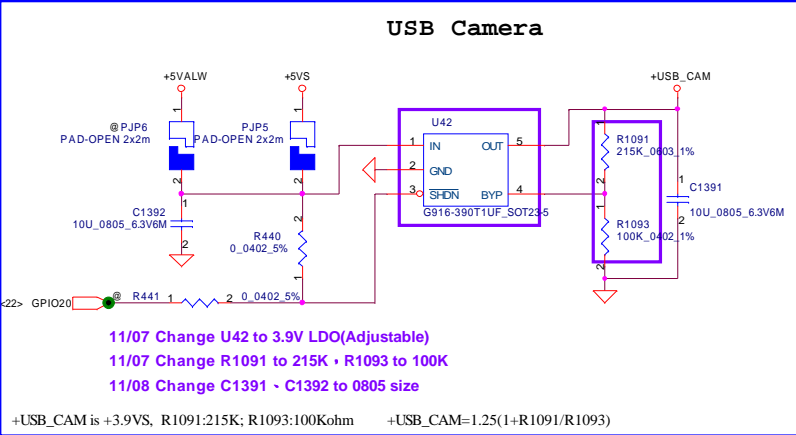
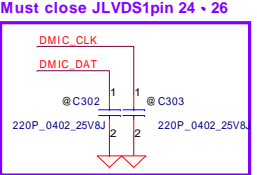
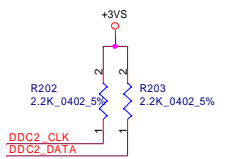
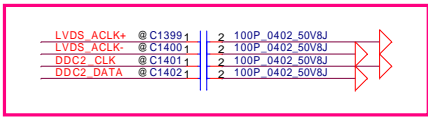
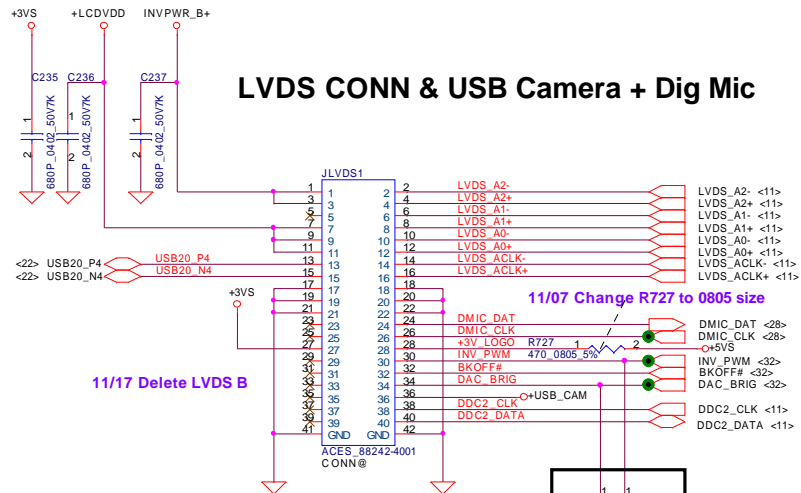
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Compal Electronics, Inc.	
Clock Generator CK505	
Size	Document Number
	Montevina Blade VBA LA4101P
Date:	Saturday, January 05, 2008
Sheet	17 of 46

CRT Connector

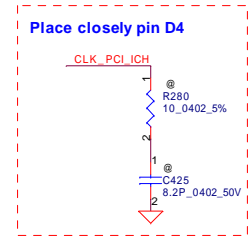
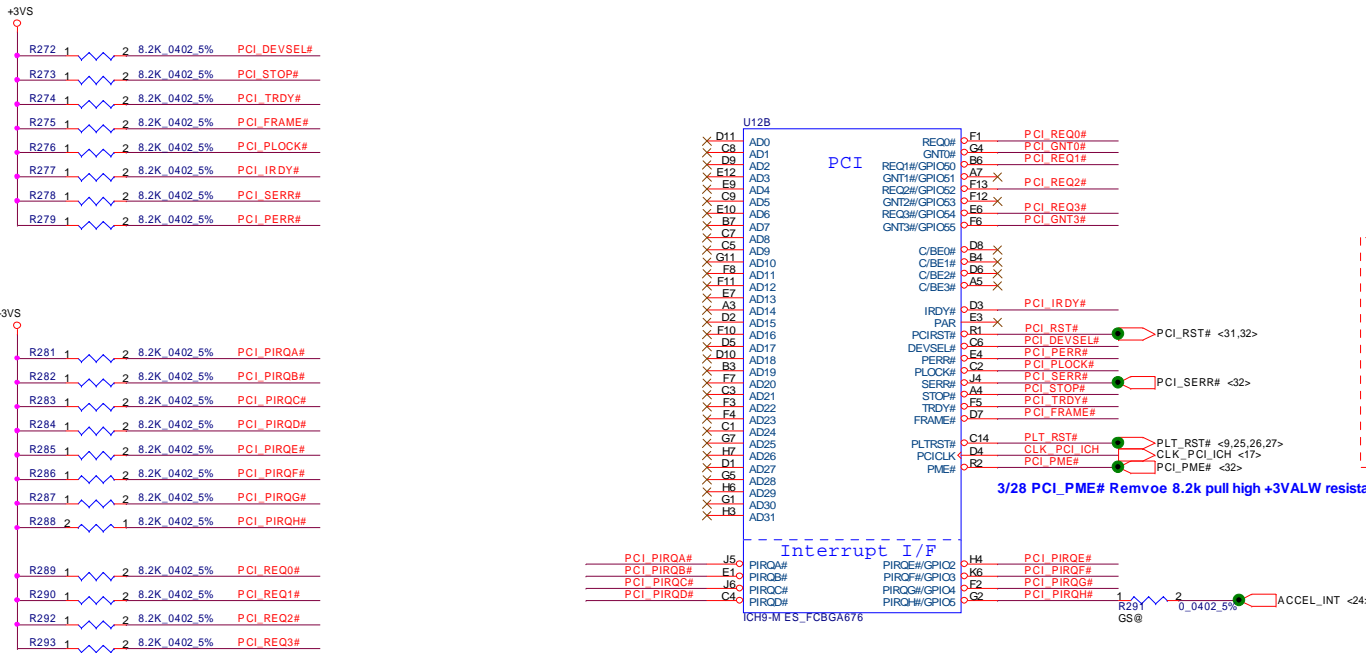


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				Montevina Blade UMA LA4101P	
				Date:	Saturday, January 05, 2008
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Date:	Saturday, January 05, 2008	Sheet	19	of 46

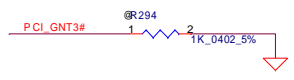
Compal Electronics, Inc.
LCD CONN



3/28 PCI_PME# Remove 8.2K pull high +3VALW resistance.

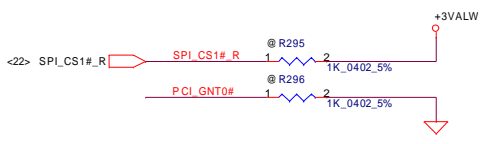
A16 swap override Strap

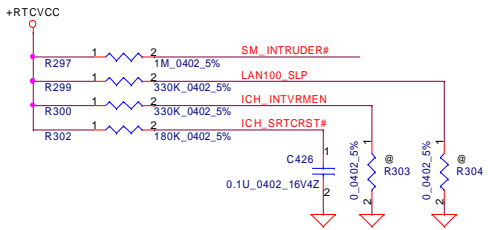
PCI_GNT3#	Low= A16 swap override Enable High= Default *
-----------	--



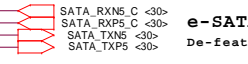
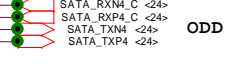
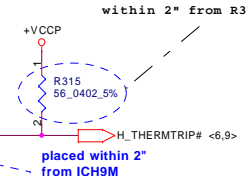
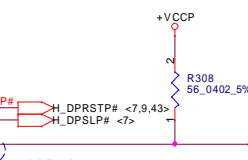
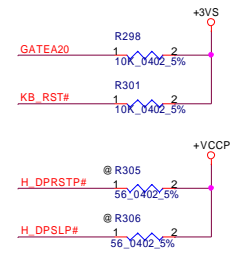
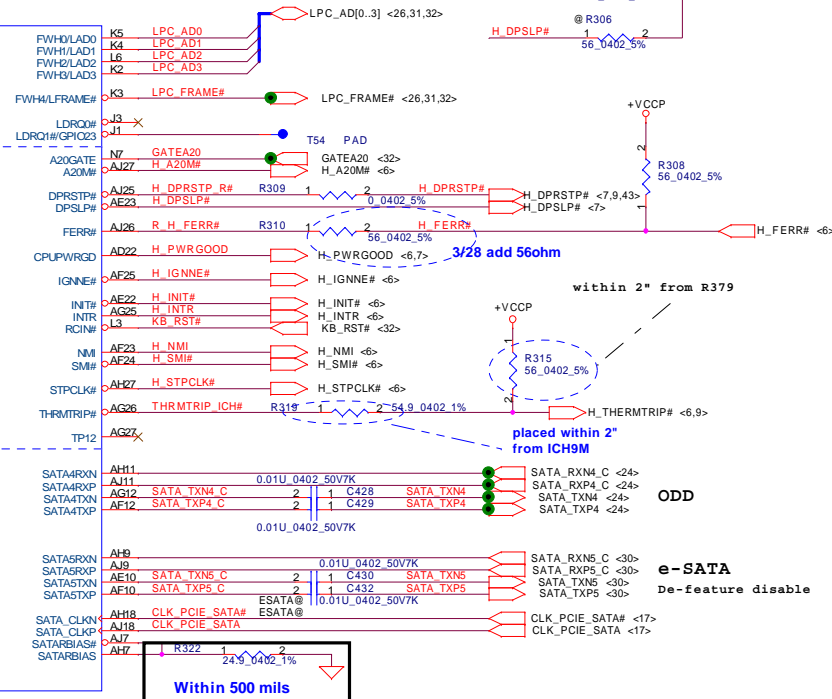
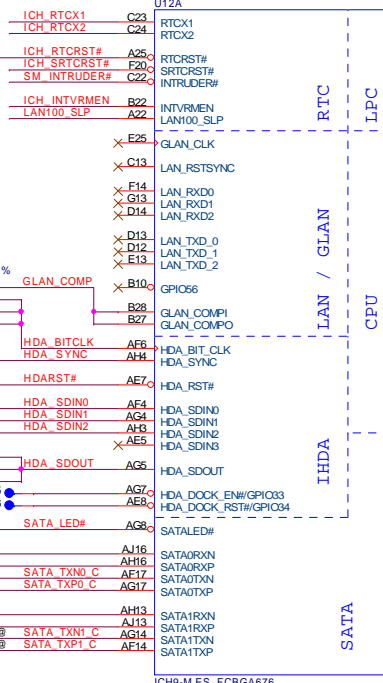
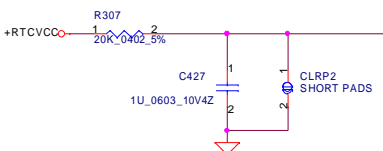
Boot BIOS Strap

PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

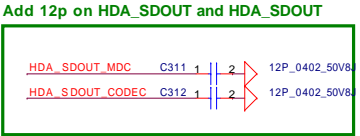
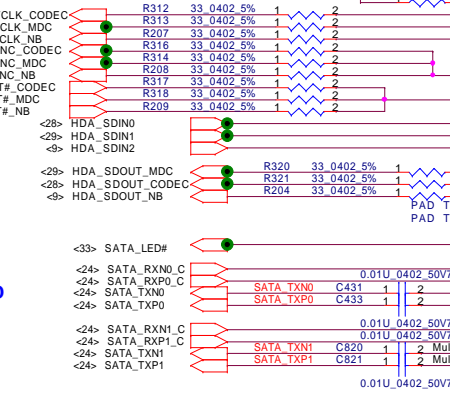




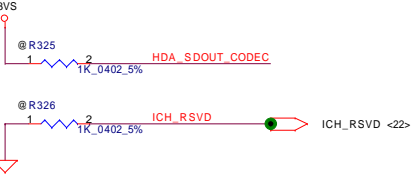
ICH8M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)
ICH8M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)	
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)



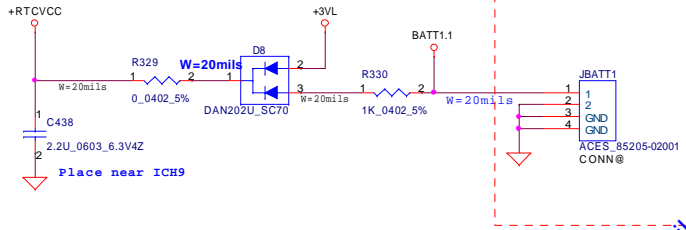
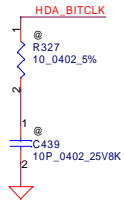
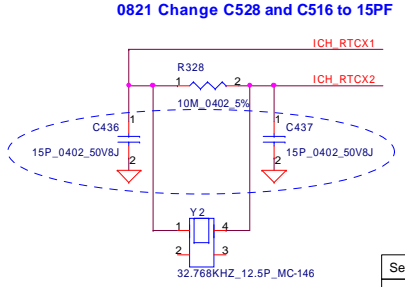
P-HDD



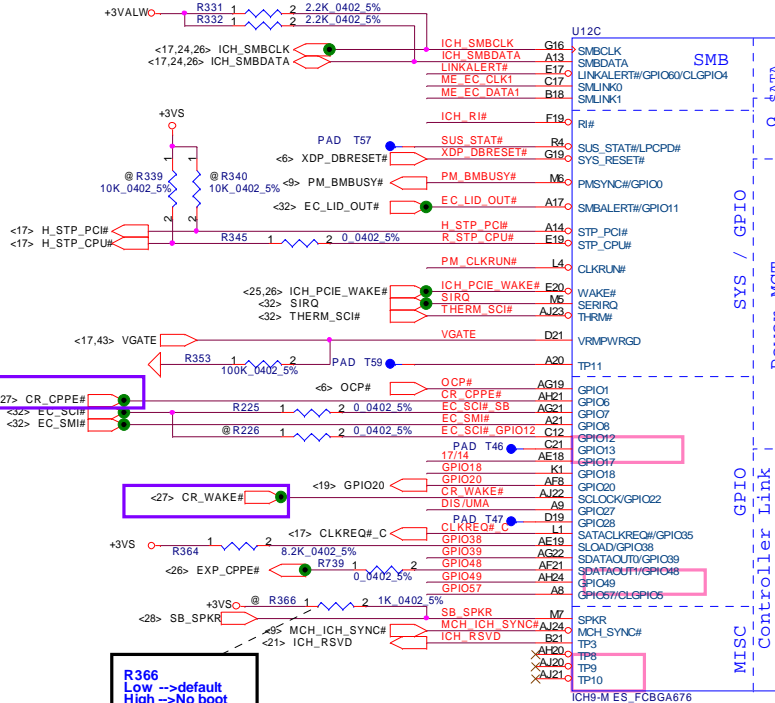
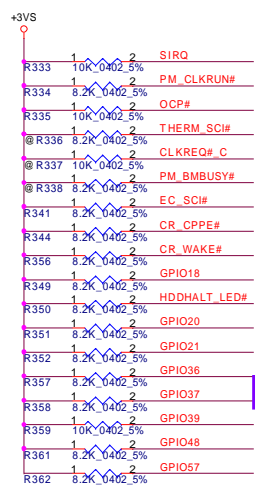
XOR CHAIN ENTRANCE STRAP:RSVD



ICH_RSVD	HDA_SDO_CODEC
0	0
0	1
1	0
1	1



Compal Electronics, Inc.
 ICH9(2/4) LAN, HD, IDE, LPC
 Rev 0.3
 Date: Saturday, January 05, 2008
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R366 Low -> default High -> No boot

11/17 Swap PCIE LAN and New card

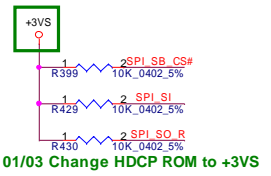
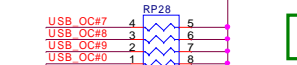
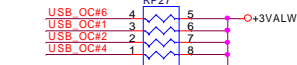
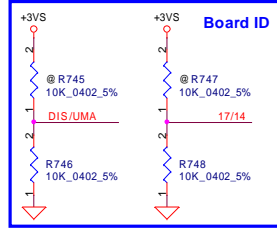
WLAN

LAN

Card Reader

New Card

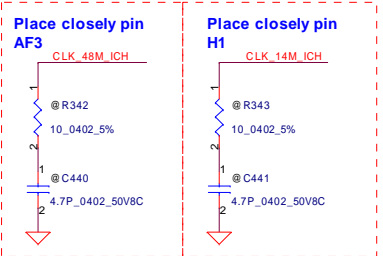
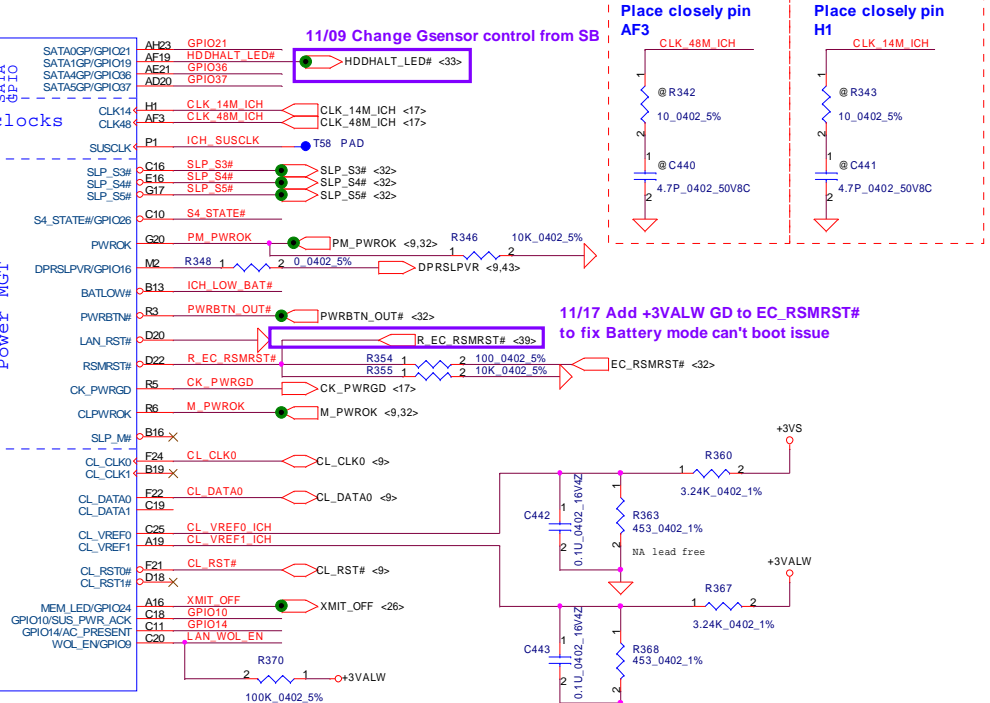
11/20 Add HDCP ROM for ICH9M



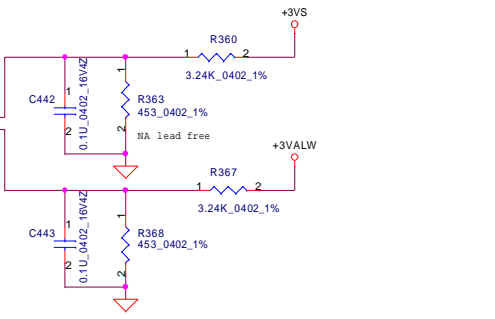
01/03 Change HDCP ROM to +3VS



Within 500 mils



11/17 Add +3VALW GD to EC_RSMRST# to fix Battery mode can't boot issue



Within 500 mils

- USB-0 Right side
- USB-1 Right side
- USB-2 Left side(with ESATA)
- USB-3 Dock
- USB-4 Camera
- USB-5 WLAN
- USB-6 Bluetooth
- USB-7 Finger Printer
- USB-8 MiniCard(WWAN/TV)
- USB-9 Express card

Security Classification	Compal Secret Data	
Issued Date	2007/08/28	Deciphered Date
		2006/03/10

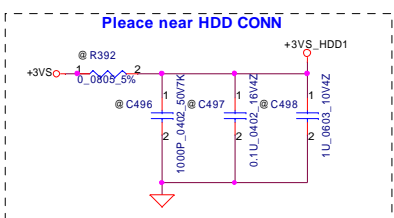
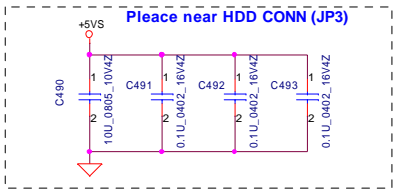
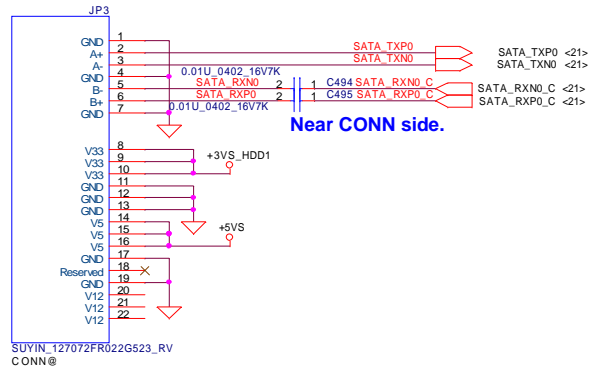
Compal Electronics, Inc.

ICH9(3/4) DMI,USB,GPIO,PCIE

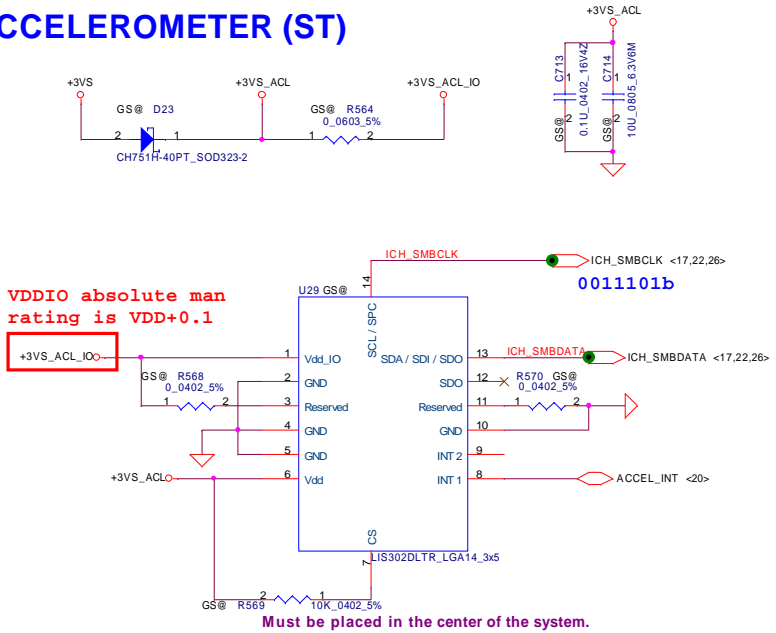
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Title	ICH9(3/4) DMI,USB,GPIO,PCIE	
Size	Document Number	Rev
Custom	Montevina Blade UMA LA4101P	0.3
Date:	Saturday, January 05, 2008	Sheet 22 of 46

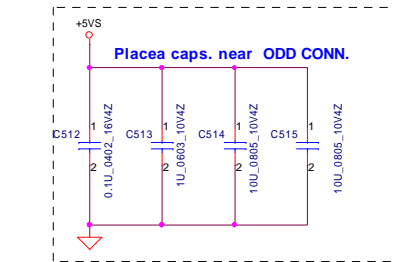
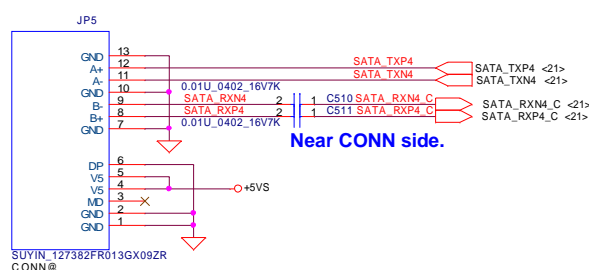
HDD Connector



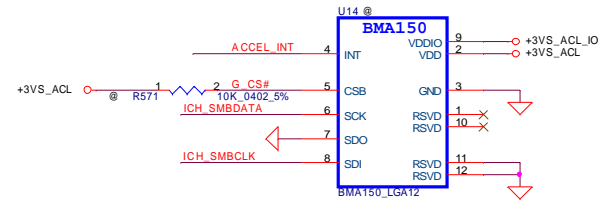
ACCELEROMETER (ST)



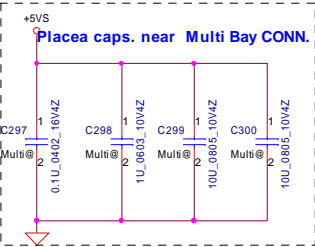
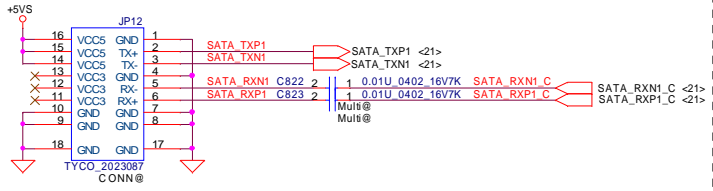
CD-ROM Connector



ACCELEROMETER (Bosch)



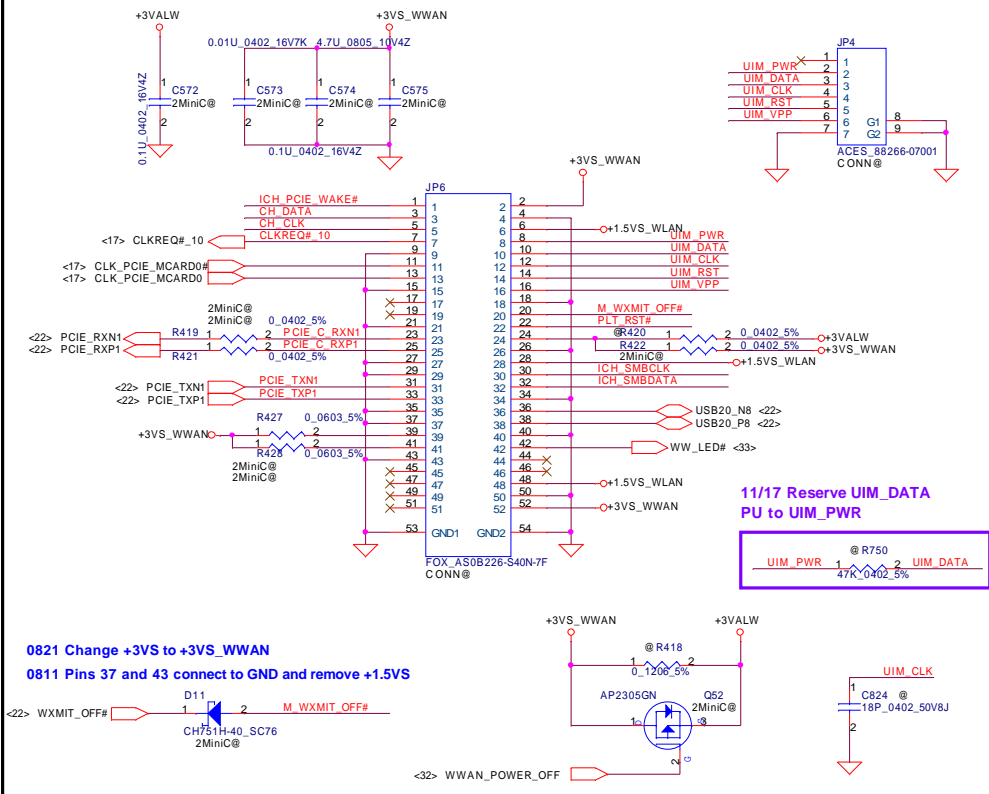
Multi Bay



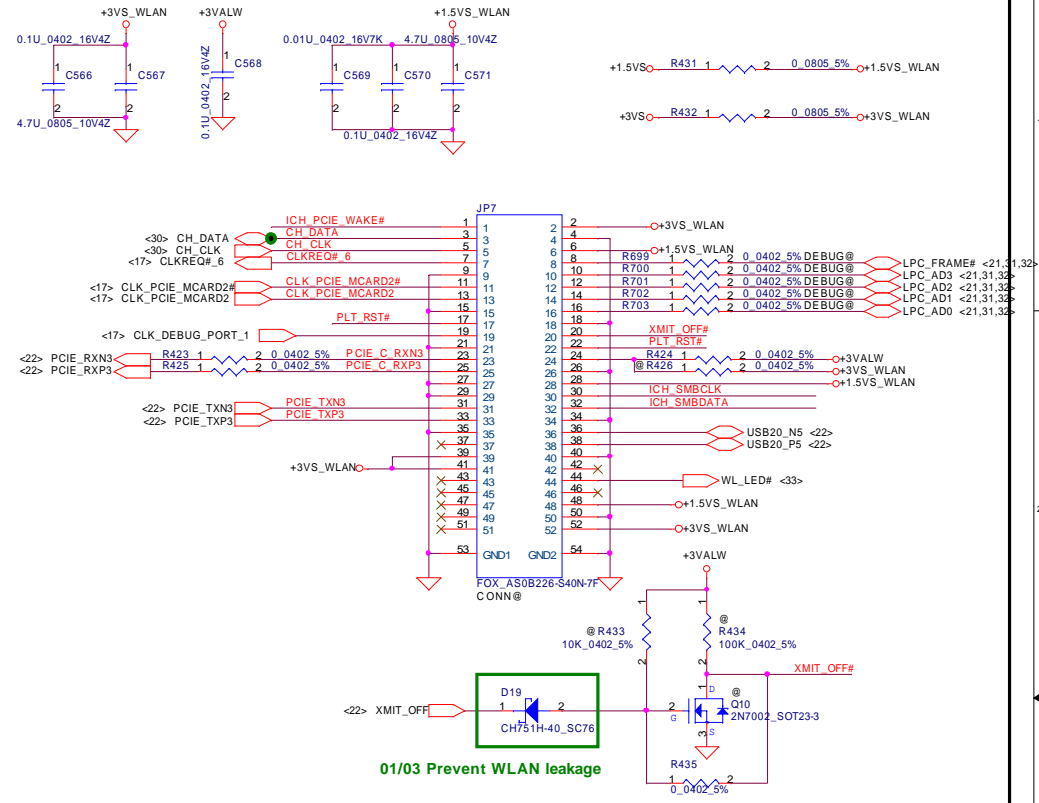
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Issued Date	2007/08/28	Deciphered Date
		2006/03/10
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Compal Electronics, Inc.	
HDD & CDROM	
Size	Document Number
Custom	Montevina Blade UMA LA410P
Date:	Saturday, January 05, 2008
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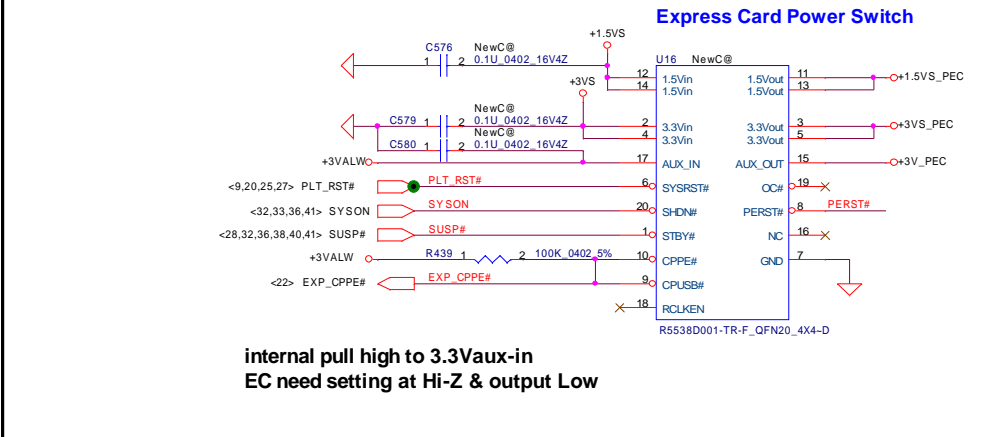
Mini Card 0--TV tuner/WWAN/Robson SIM card Connector



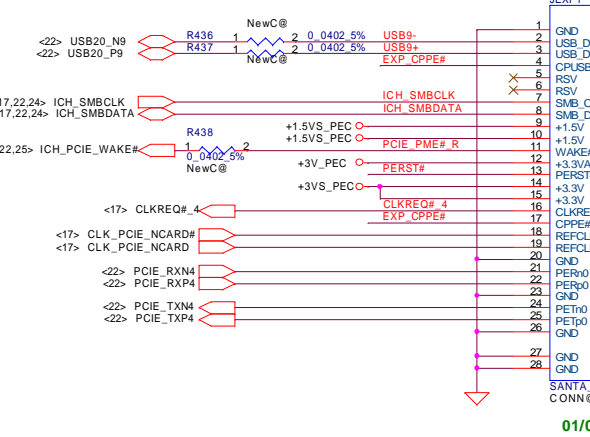
Mini Card 2---WLAN



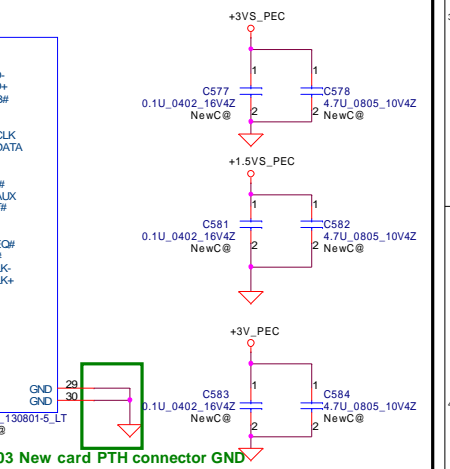
New Card



Close to JEXP



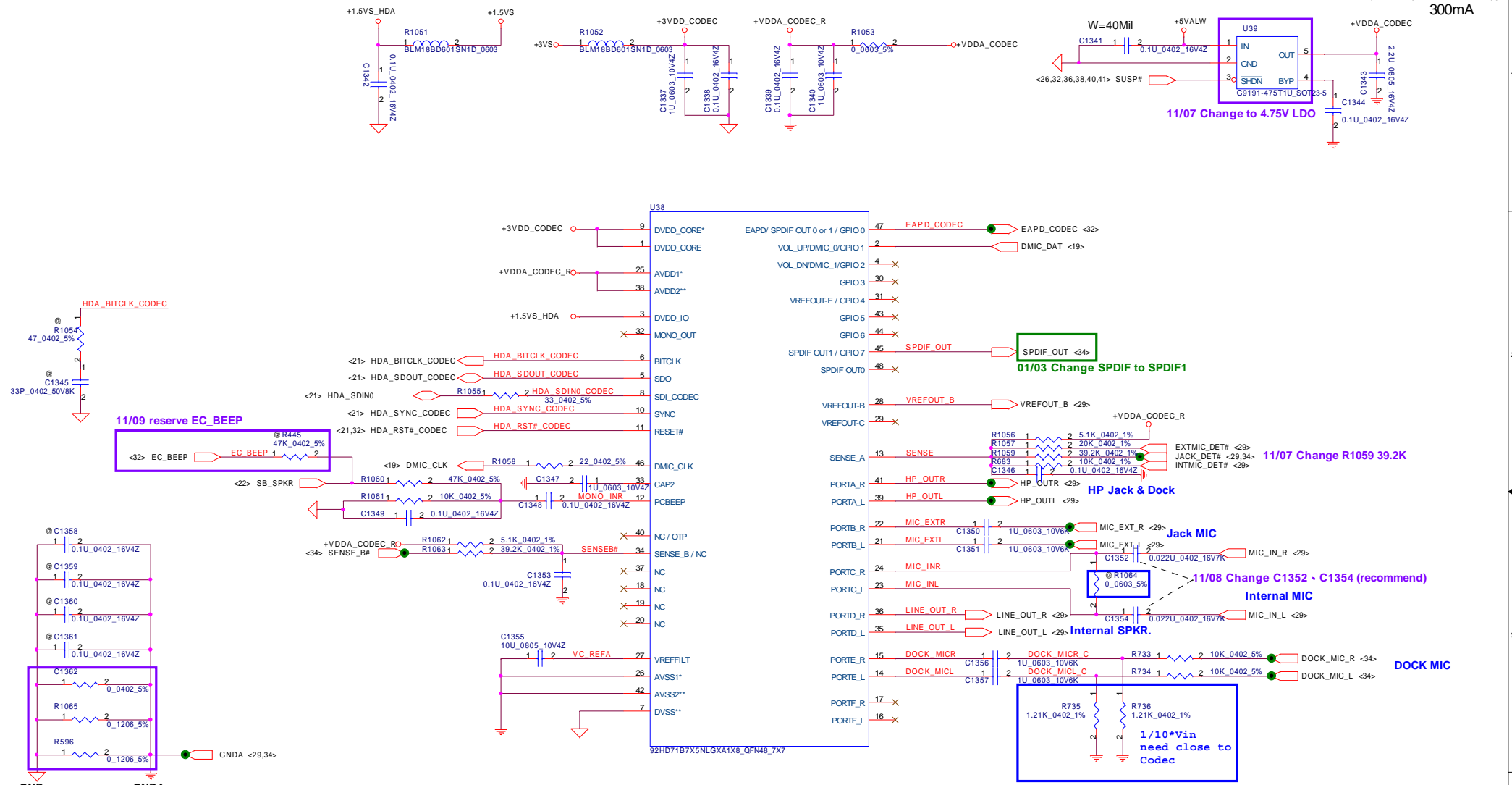
Near to Express Card slot.



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					Montevina Blade UMA LA4101P	0.3
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CODEC POWER

(4.75V(4.56~4.94V))
300mA

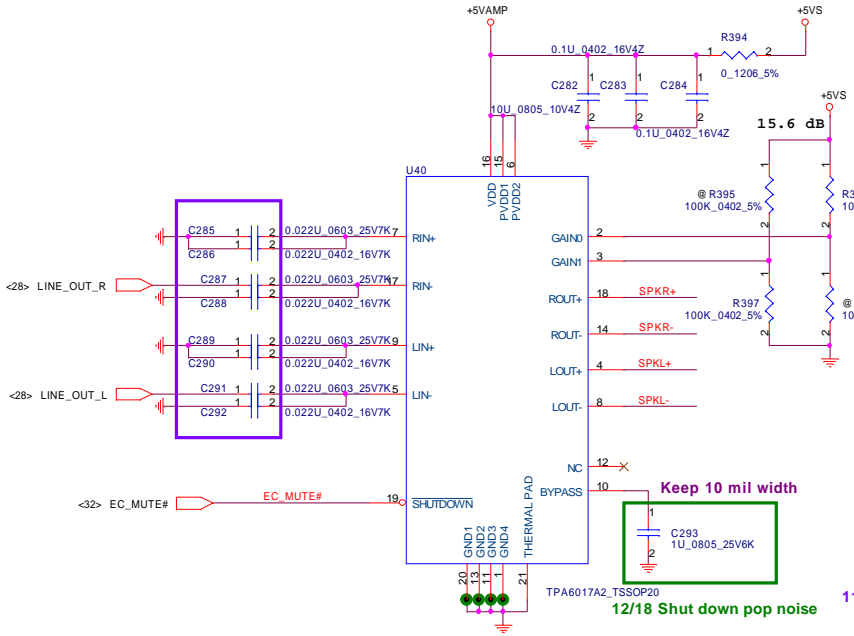


11/07 Stuff 0 Ohm for AGND and GND

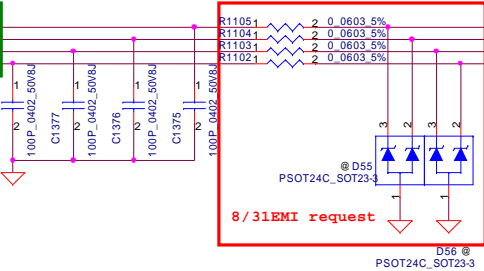
SENSE A		SENSE B	
Port	Resistor	Port	Resistor
A	39.2K	E	39.2K
B	20K	F	20K
C	10K	G	10K
D	5.11K	H	5.11K

Security Classification	Compal Secret Data			Title	Codec_IDT9271B7		
Issued Date	2007/08/28	Deciphered Date	2006/07/26	Size	Document Number	Rev	
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				Date:	Saturday, January 05, 2008	Sheet	28

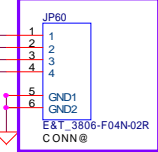
GAIN0	GAIN1	Av (inv)
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB



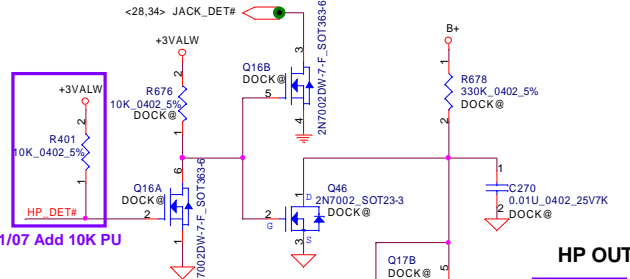
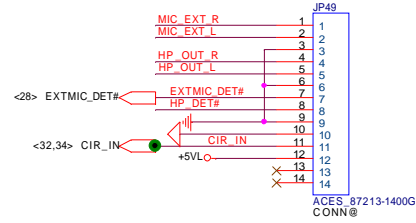
SPKR+
SPKR-
SPKL+
SPKL-



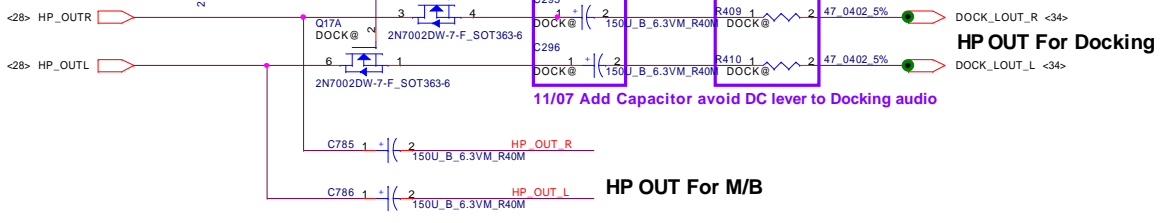
SPEAKER



Audio/B & CIR

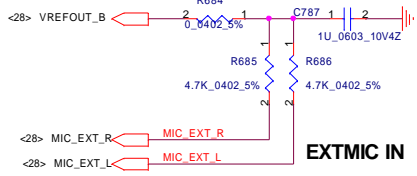
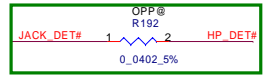


HP OUT

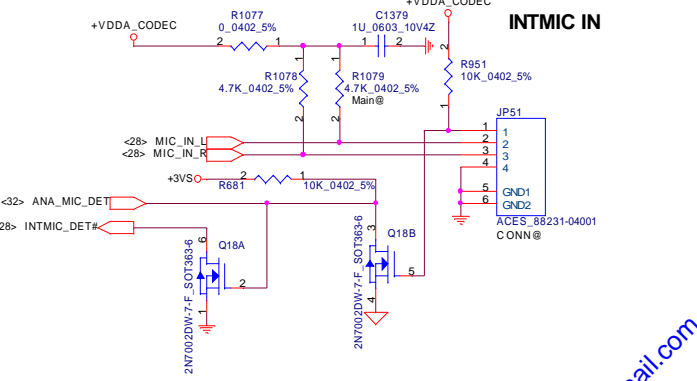


HP OUT For Docking

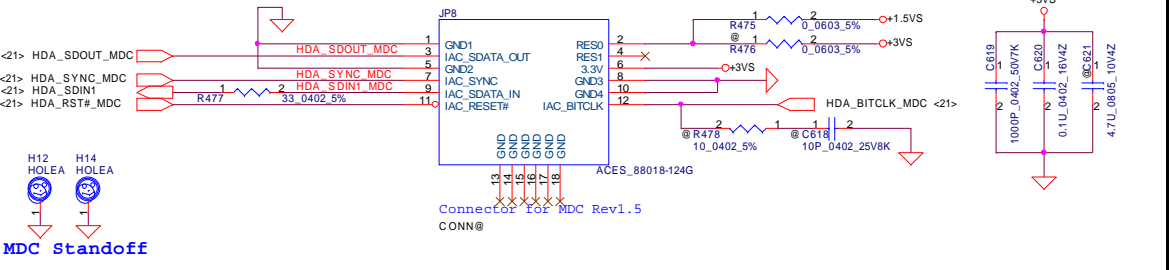
HP OUT For M/B



INTMIC IN

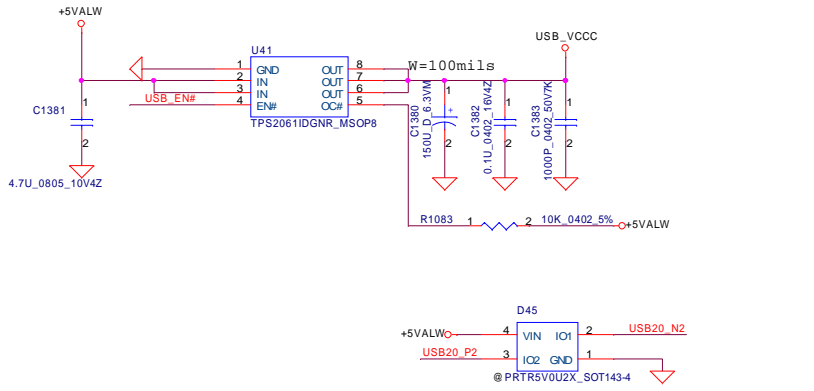


MDC 1.5 Conn.

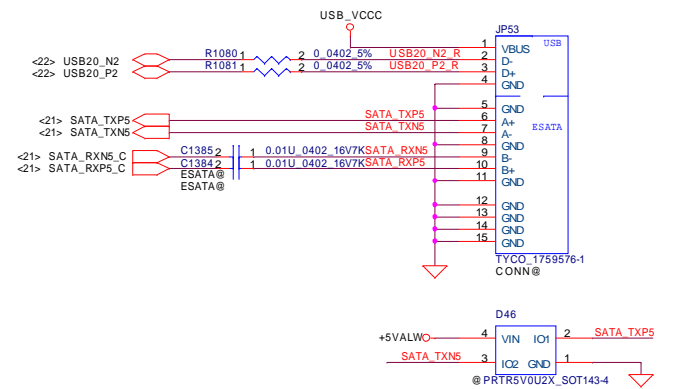


Security Classification	Compal Secret Data		Title	AMP & Audio Jack	
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Date:	Saturday, January 05, 2008	Sheet	29	of	46

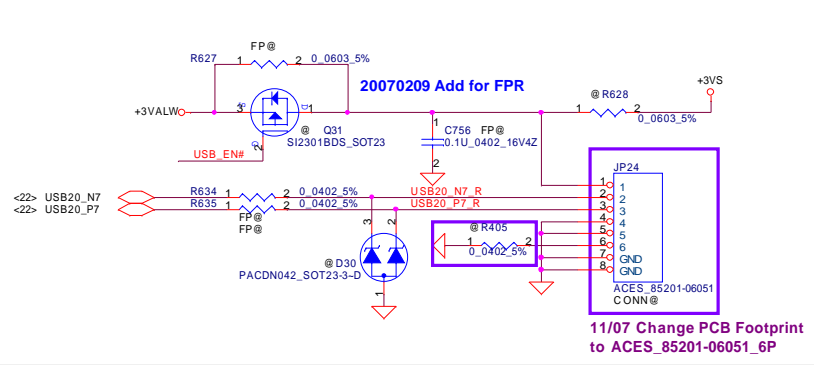
Left side USB Connector



Left side ESATA/USB combination Connector

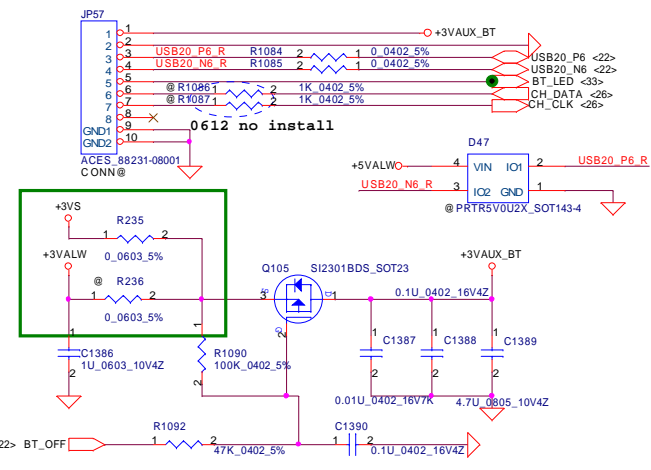


Finger printer

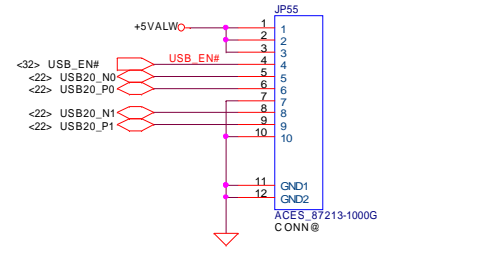


BT Connector

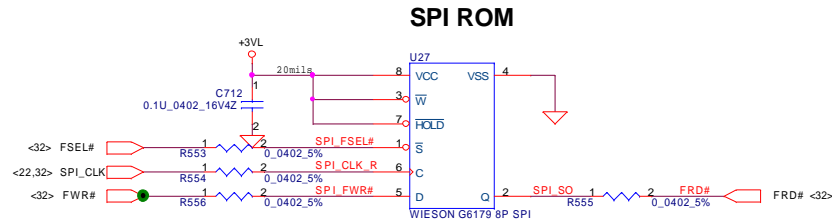
Need change to New version



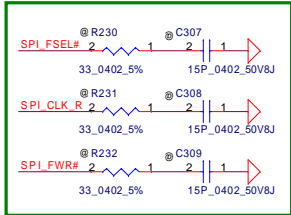
USB cable connector for Right side



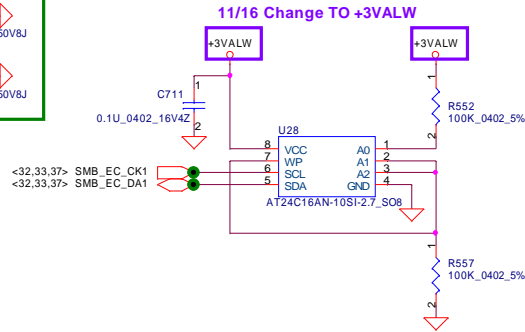
Security Classification	Compal Secret Data			Title	
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				Size	Document Number
Date:	Saturday, January 05, 2008	Sheet	30	of	46



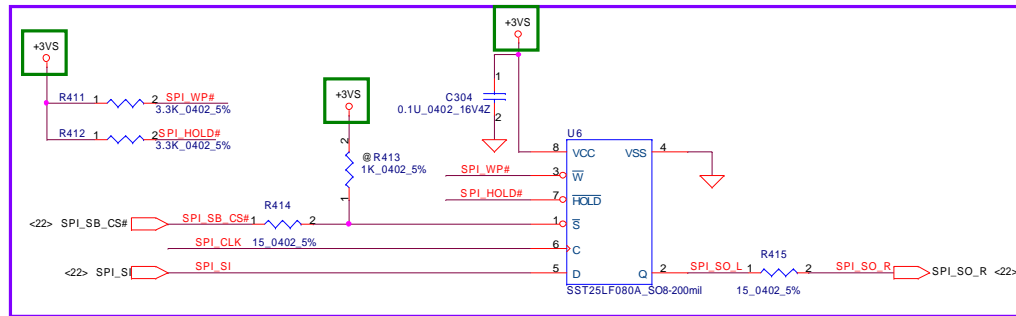
SP07000F500 S SOCKET WIESON G6179-100000 8P SPIFLASH
WIESO_G6179-100000_8P



12/27EMI request



11/16 Change TO +3VALW

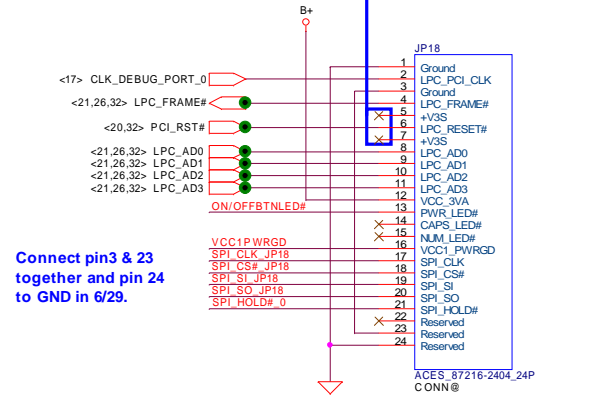


11/17 Add SB HDPC ROM

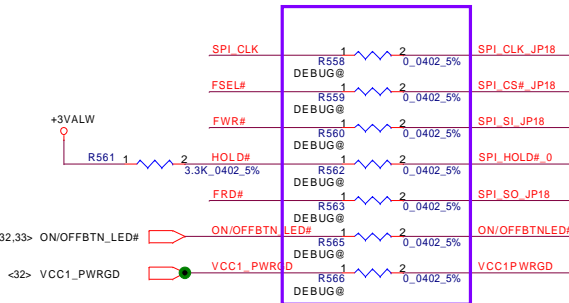
01/03 Change HDPC ROM to +3VS

LPC Debug Port

Change from +3VL to +3VS. 6/9
Removed +3VS. 6/13



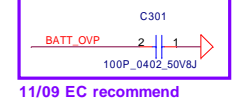
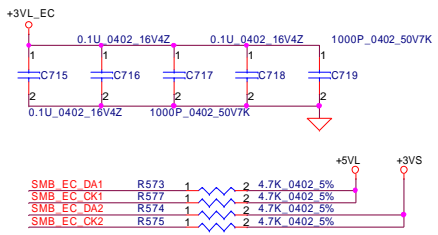
Connect pin3 & 23
together and pin 24
to GND in 6/29.



11/07 Add 0 Ohm for debug port

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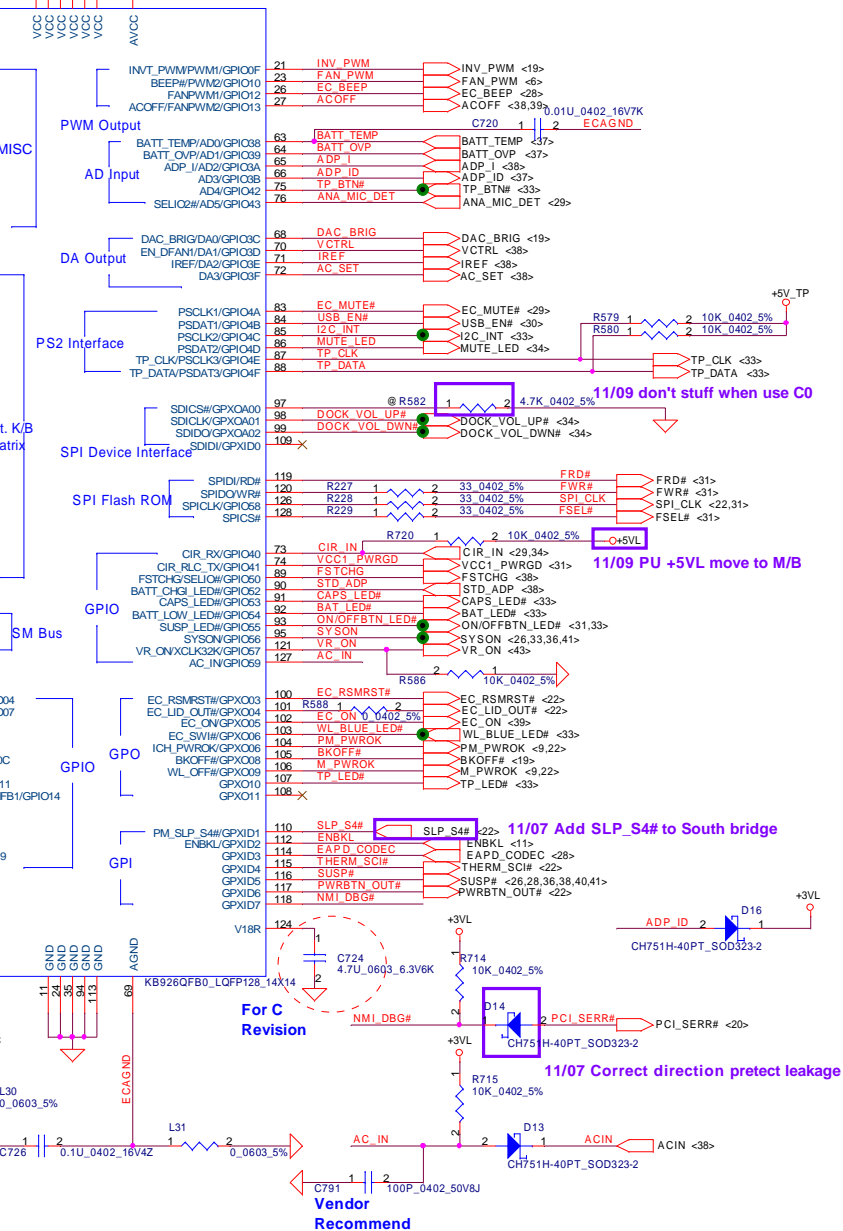
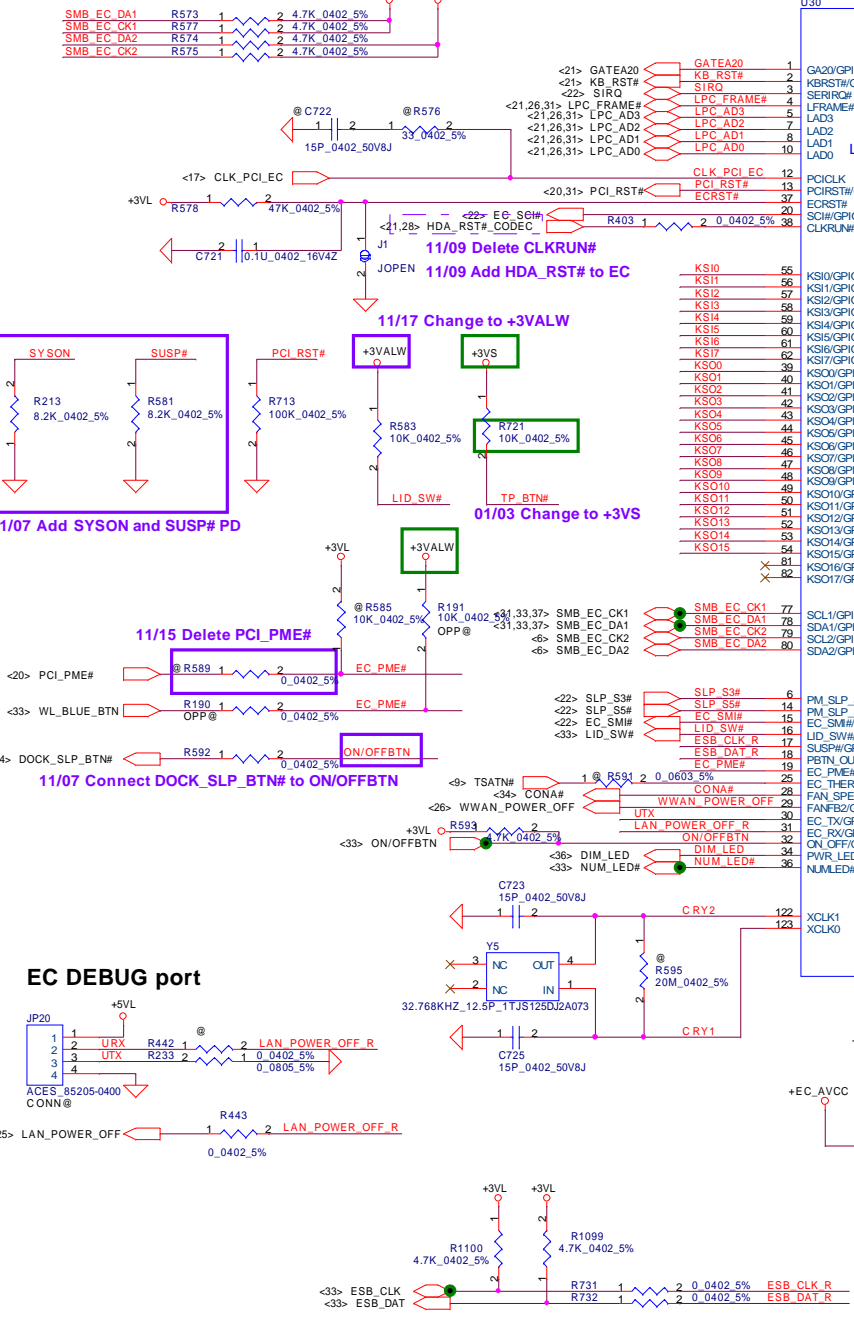
Compal Electronics, Inc.		
Title BIOS ROM		
Size	Document Number	Rev
	Montevina Blade LA4101P	0.3
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11/09 EC recommend

For EMI

KS015 @ C792	1	2	100P_0402_50V8J
KS010 @ C793	1	2	100P_0402_50V8J
KS011 @ C794	1	2	100P_0402_50V8J
KS014 @ C795	1	2	100P_0402_50V8J
KS013 @ C796	1	2	100P_0402_50V8J
KS012 @ C797	1	2	100P_0402_50V8J
KS03 @ C798	1	2	100P_0402_50V8J
KS06 @ C799	1	2	100P_0402_50V8J
KS08 @ C800	1	2	100P_0402_50V8J
KS07 @ C801	1	2	100P_0402_50V8J
KS04 @ C802	1	2	100P_0402_50V8J
KS02 @ C803	1	2	100P_0402_50V8J
KS10 @ C804	1	2	100P_0402_50V8J
KS01 @ C805	1	2	100P_0402_50V8J
KS05 @ C806	1	2	100P_0402_50V8J
KS13 @ C807	1	2	100P_0402_50V8J
KS12 @ C808	1	2	100P_0402_50V8J
KS00 @ C809	1	2	100P_0402_50V8J
KS15 @ C810	1	2	100P_0402_50V8J
KS14 @ C811	1	2	100P_0402_50V8J
KS09 @ C812	1	2	100P_0402_50V8J
KS16 @ C813	1	2	100P_0402_50V8J
KS17 @ C814	1	2	100P_0402_50V8J
KS11 @ C815	1	2	100P_0402_50V8J

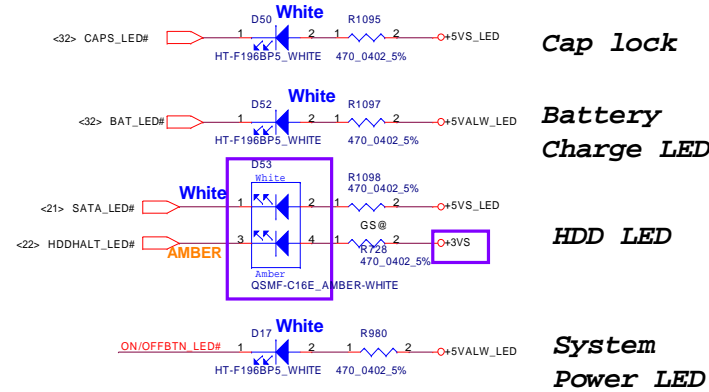


KS015 @ J19	1	1	100P_0402_50V8J
KS010	2	2	100P_0402_50V8J
KS011	3	3	100P_0402_50V8J
KS014	4	4	100P_0402_50V8J
KS013	5	5	100P_0402_50V8J
KS03	6	6	100P_0402_50V8J
KS06	7	7	100P_0402_50V8J
KS08	8	8	100P_0402_50V8J
KS07	9	9	100P_0402_50V8J
KS04	10	10	100P_0402_50V8J
KS02	11	11	100P_0402_50V8J
KS10	12	12	100P_0402_50V8J
KS01	13	13	100P_0402_50V8J
KS05	14	14	100P_0402_50V8J
KS13	15	15	100P_0402_50V8J
KS12	16	16	100P_0402_50V8J
KS00	17	17	100P_0402_50V8J
KS15	18	18	100P_0402_50V8J
KS14	19	19	100P_0402_50V8J
KS09	20	20	100P_0402_50V8J
KS16	21	21	100P_0402_50V8J
KS17	22	22	100P_0402_50V8J
KS11	23	23	100P_0402_50V8J
KS11	24	24	100P_0402_50V8J

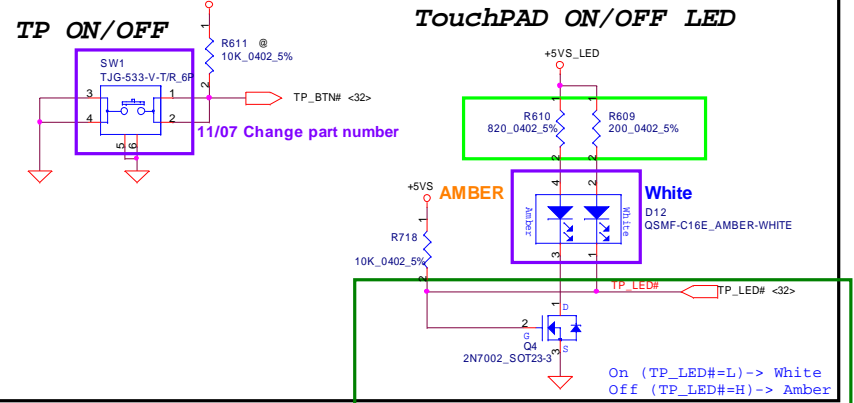
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Compal Electronics, Inc.			
EC KB926/KB Conn.			
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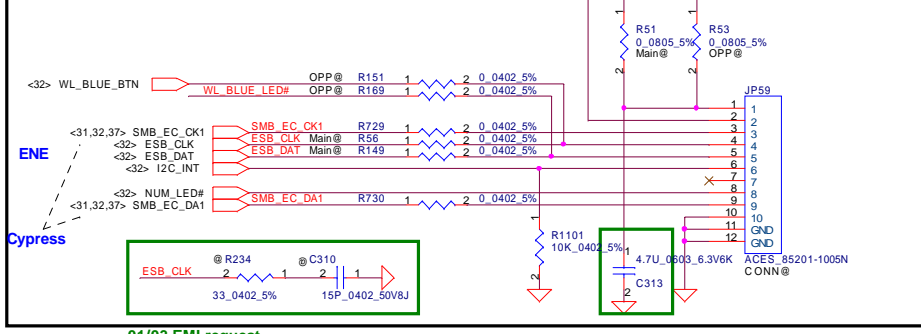
System LED



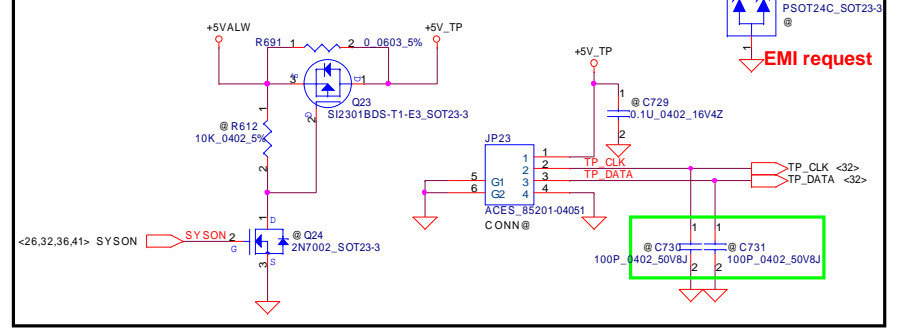
T/P Board (Include T/P_ON/OFF)



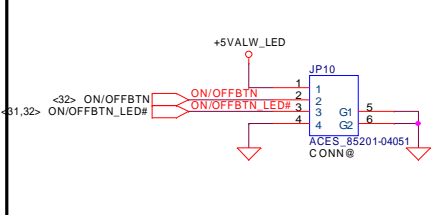
Capacitor Sensor Conn



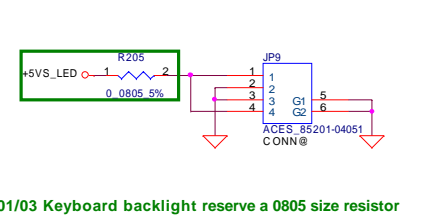
T/P Board Conn



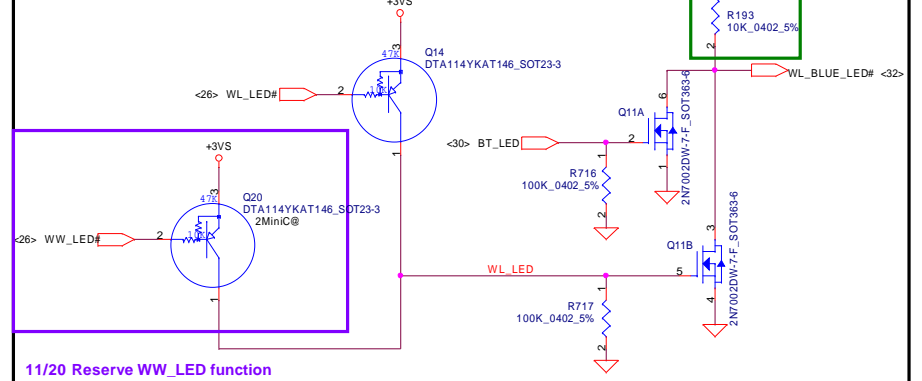
ON/OFF Button Connector



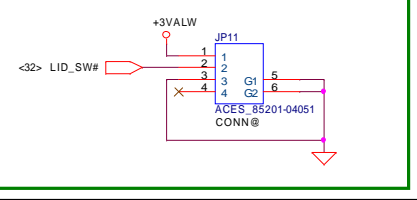
Keyboard backlight Conn



Mini card LED



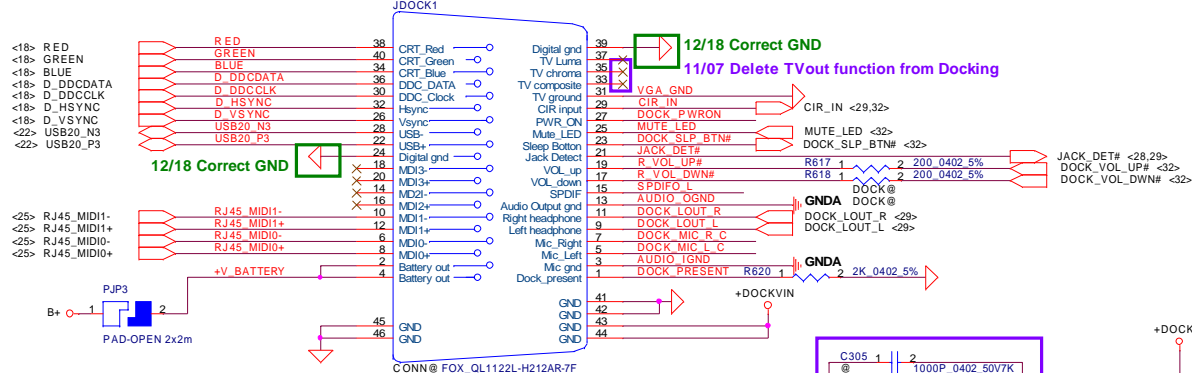
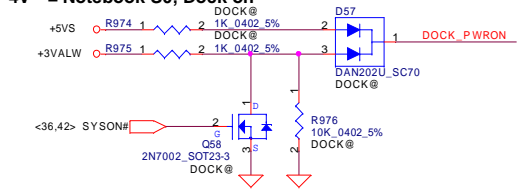
Lid Switch Connector



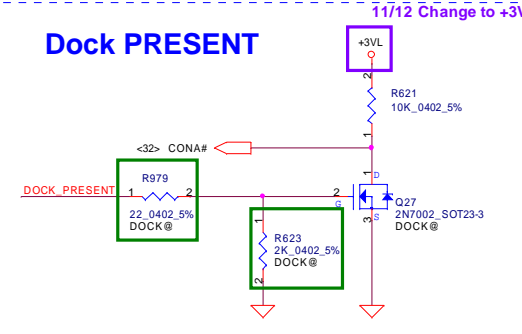
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	Montevina Blade LA4101P	Saturday, January 05, 2008		0.3
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Atlas/ Saturn Dock

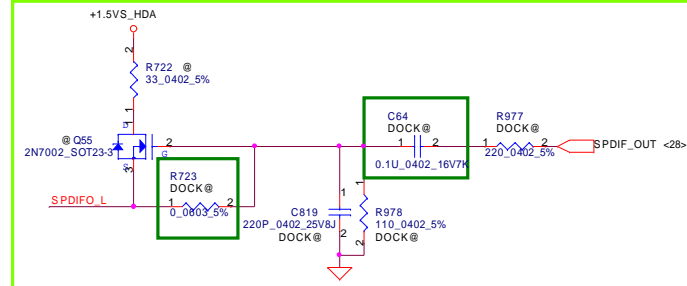
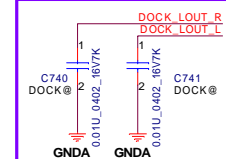
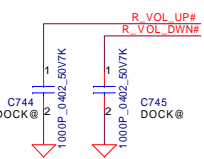
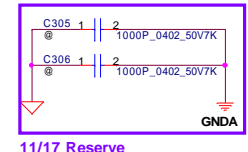
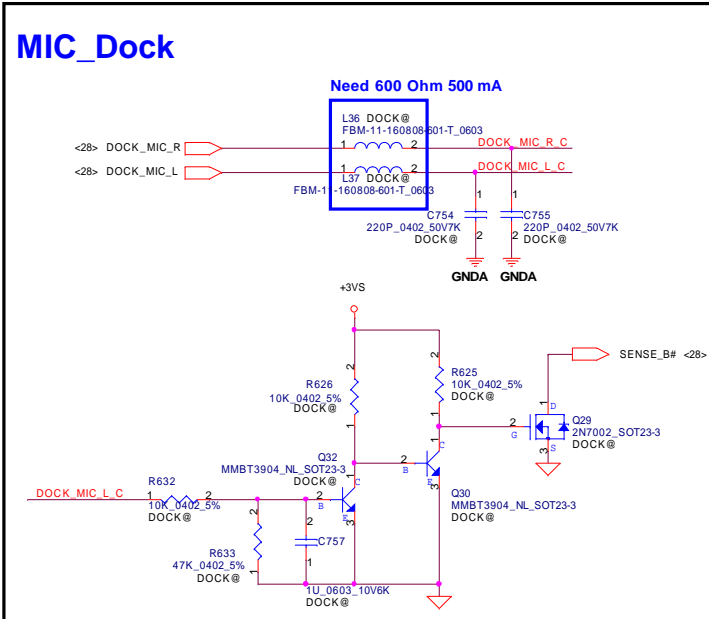
DOCK_PWR_ON Spec
0V = Notebook S4/S5, Dock off
2.5V = Notebook S3, Dock on
4V = Notebook S0, Dock on



Dock PRESENT



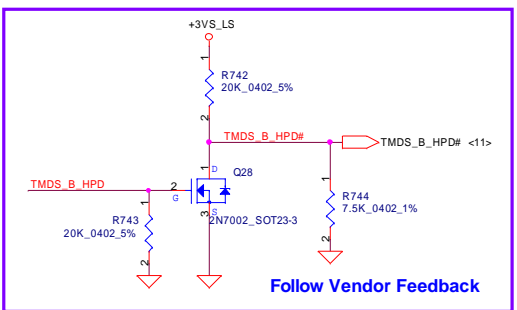
MIC_Dock



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Size	Document Number		Rev		
Customer	Montevina Blade UMA LA4101P		0.3		
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Follow Intel Feedback putting 2.2K ohm

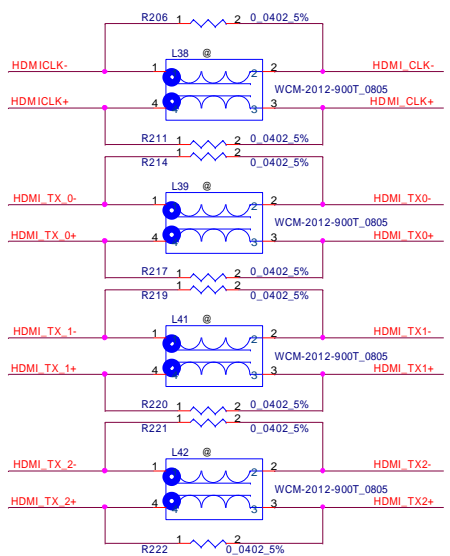
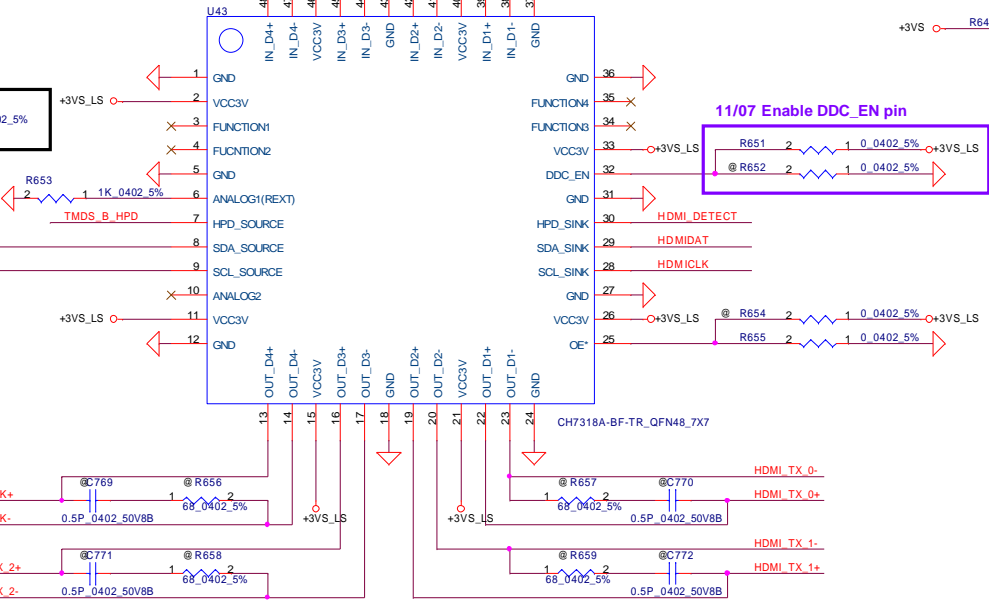
<9> HDMIDAT_NB
<9> HDMICKL_NB



Follow Vendor Feedback

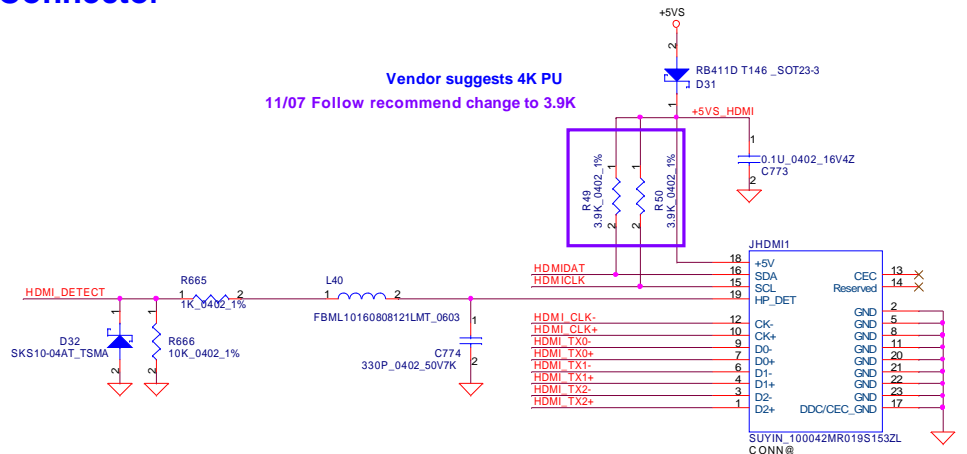
11/07 correct TMDS_B_HPD# connection to North bridge

<11> TMDS_B_DATA2#
<11> TMDS_B_DATA2
<11> TMDS_B_CLK#
<11> TMDS_B_CLK
+3VS_LS
+3VS_LS
TMDS_B_DATA1 <11>
TMDS_B_DATA1# <11>
TMDS_B_DATA0 <11>
TMDS_B_DATA0# <11>

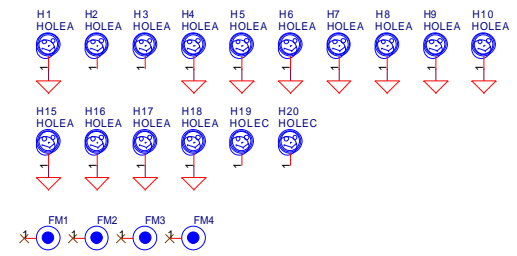
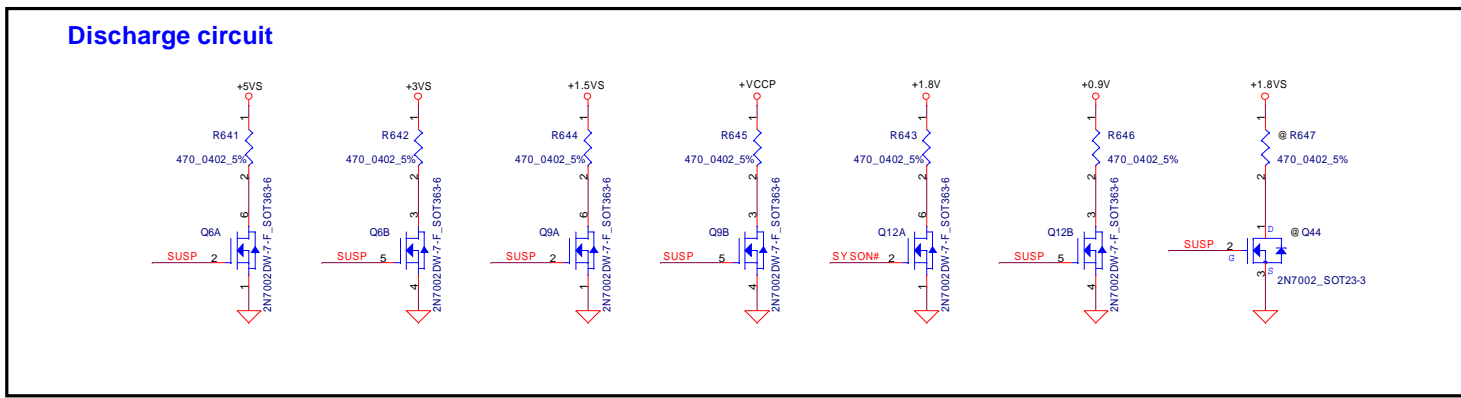
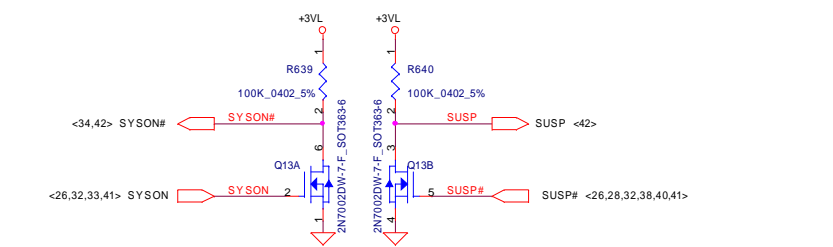
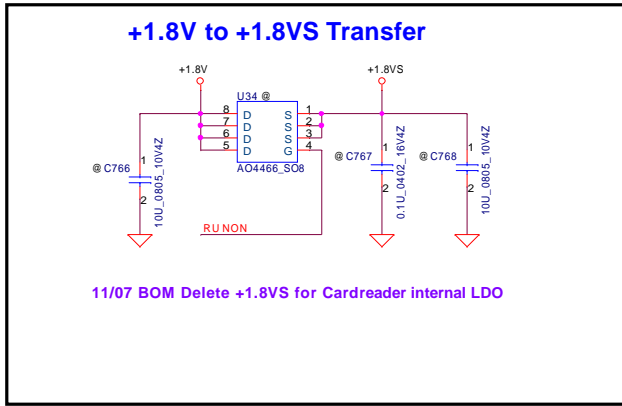
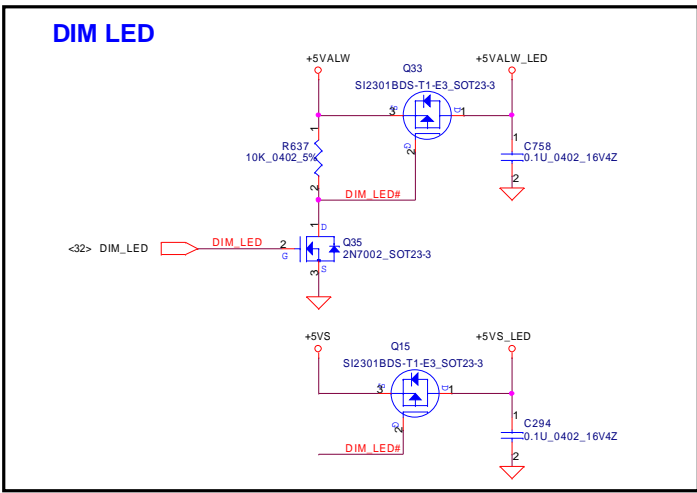
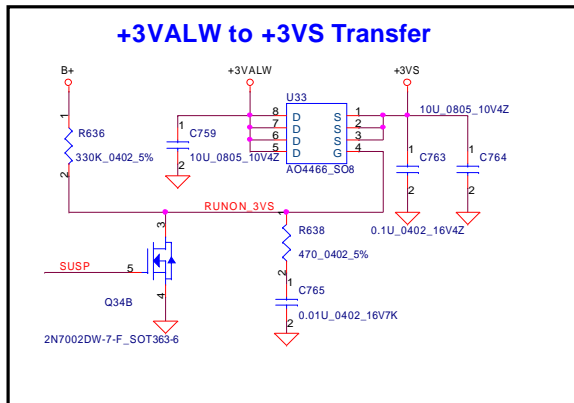
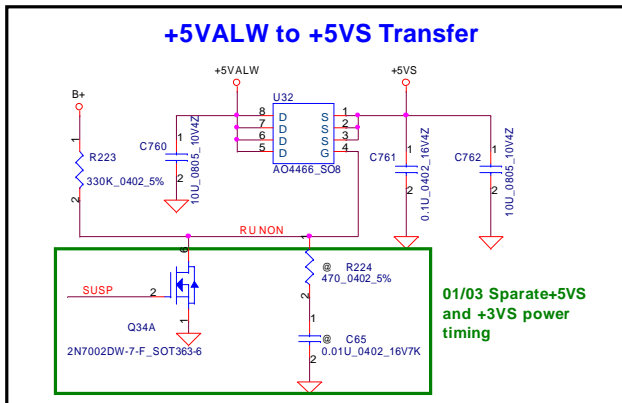


01/03 Reserver 0 ohm co lay with common choke

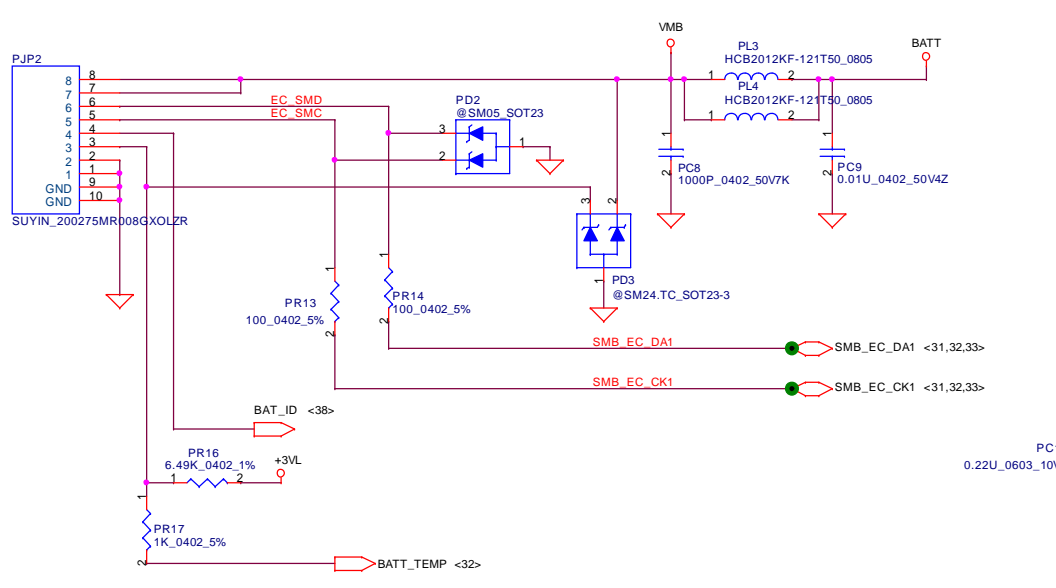
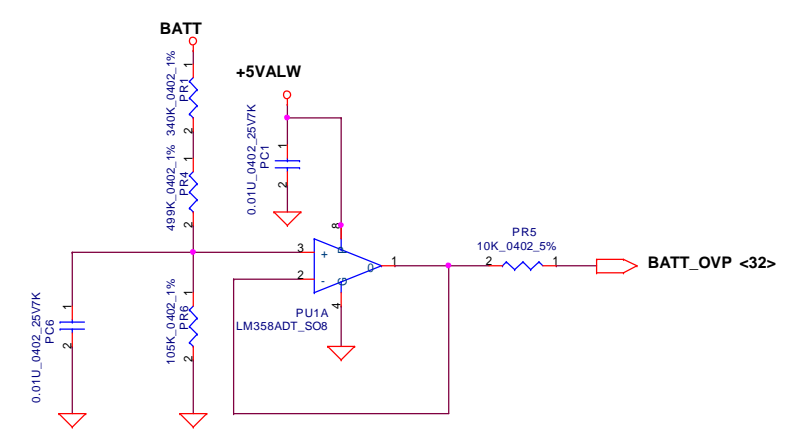
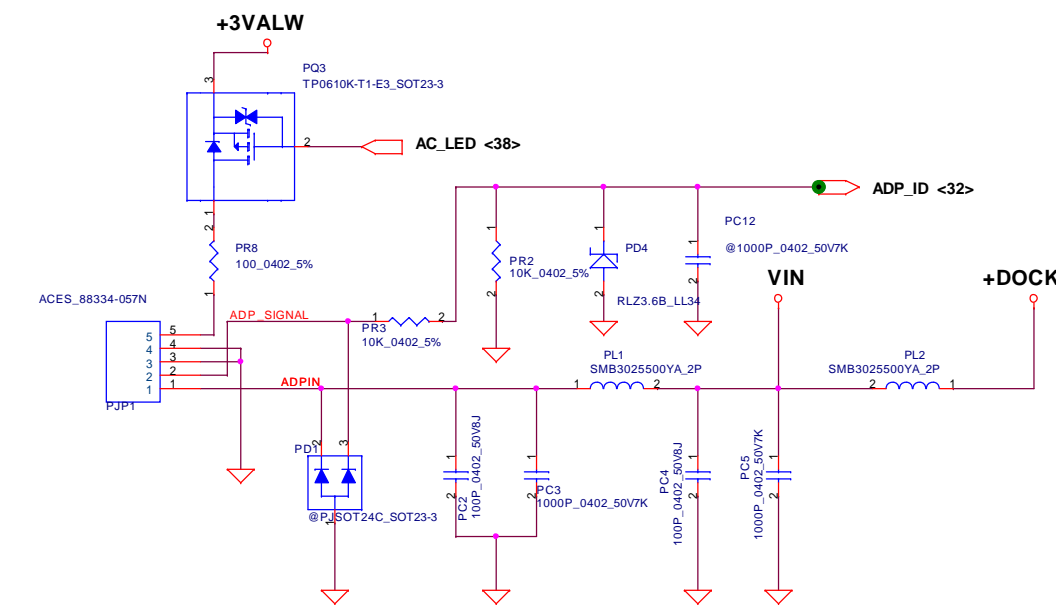
HDMI Connector



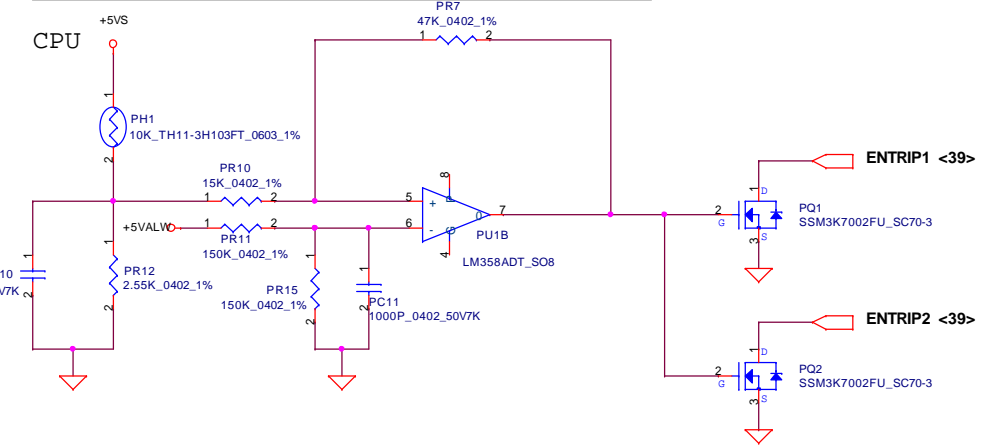
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Custom	Montevina Blade UMA LA410P				



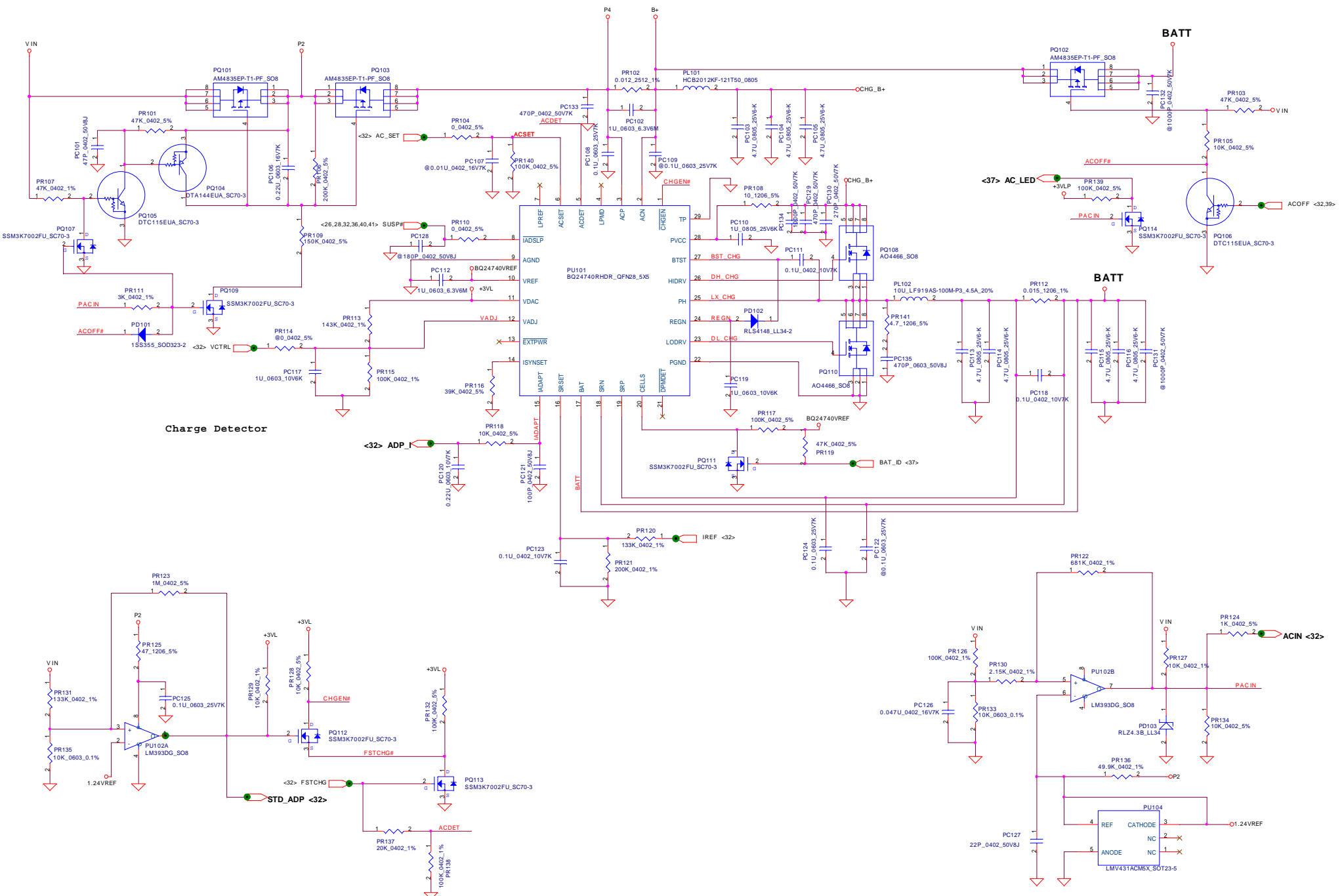
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PH1 under CPU bottom side :
 CPU thermal protection at 90 +/-3 degree C
 Recovery at 47 +/-3 degree C

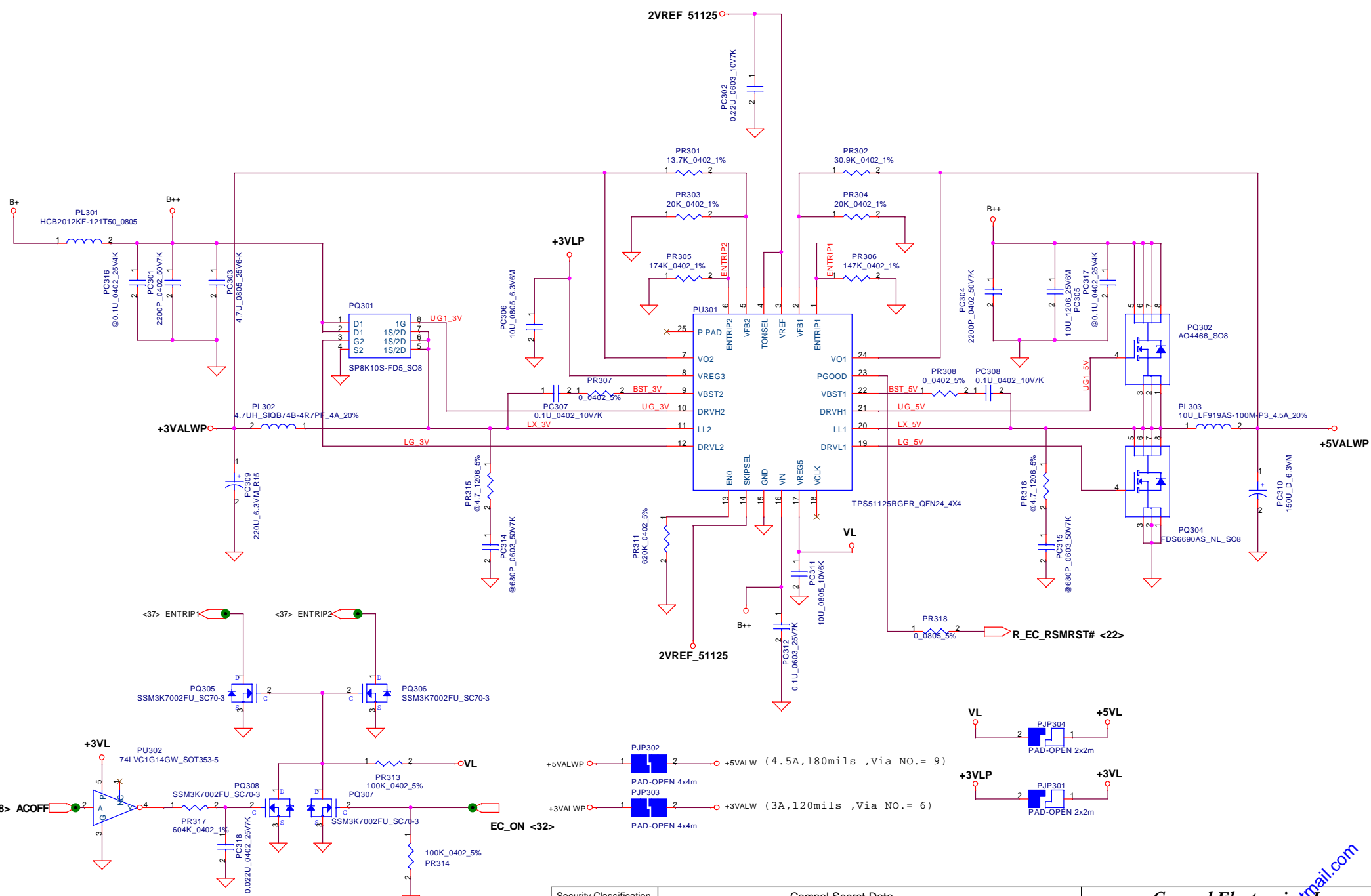


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Issued Date	2007/05/29	Deciphered Date	2008/05/29	DC Connector/CPU OTP	
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Charge Detector

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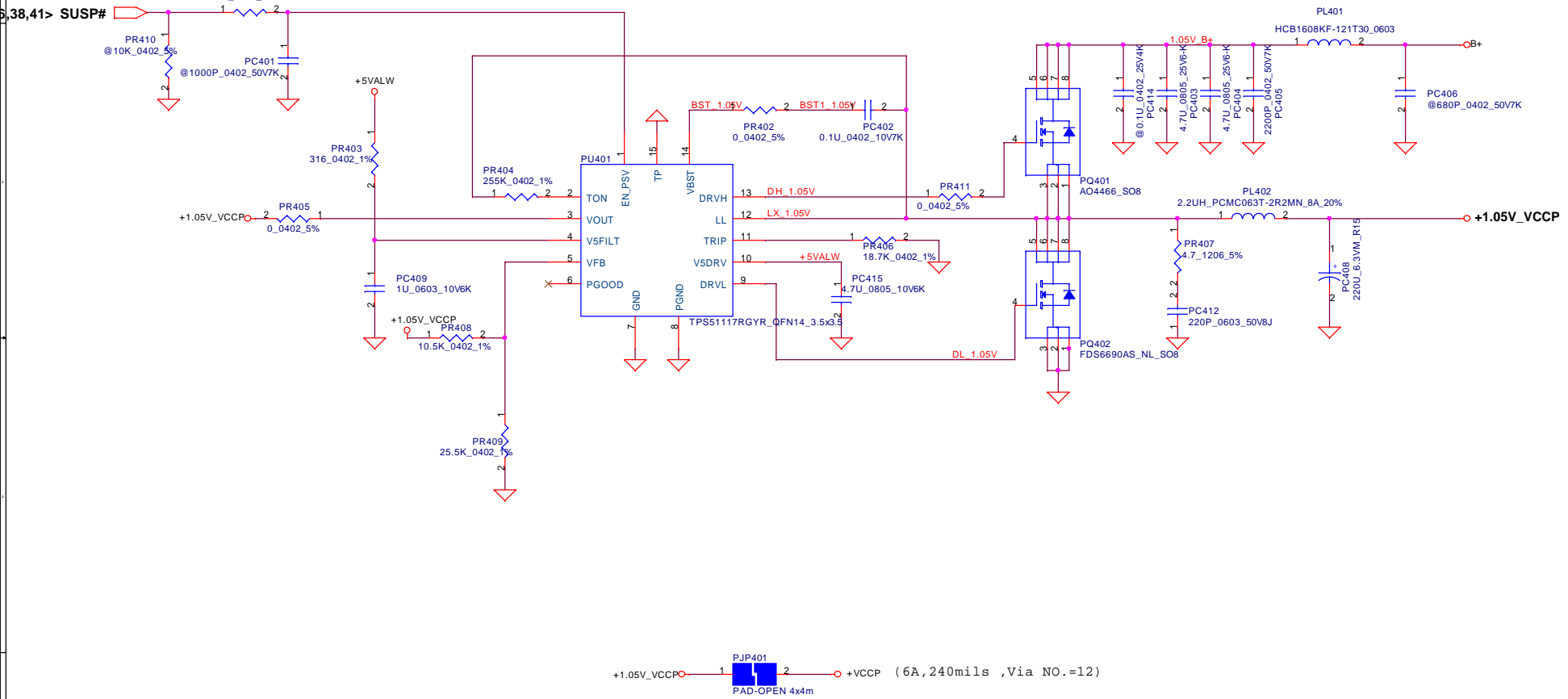
Title			Compal Electronics Inc.	
Size			3.3VALWP/5VALWP	
Document Number			Montevina Block UMA LA4101P	
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32,38> ACOFF

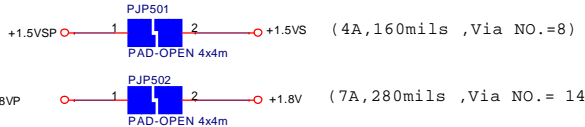
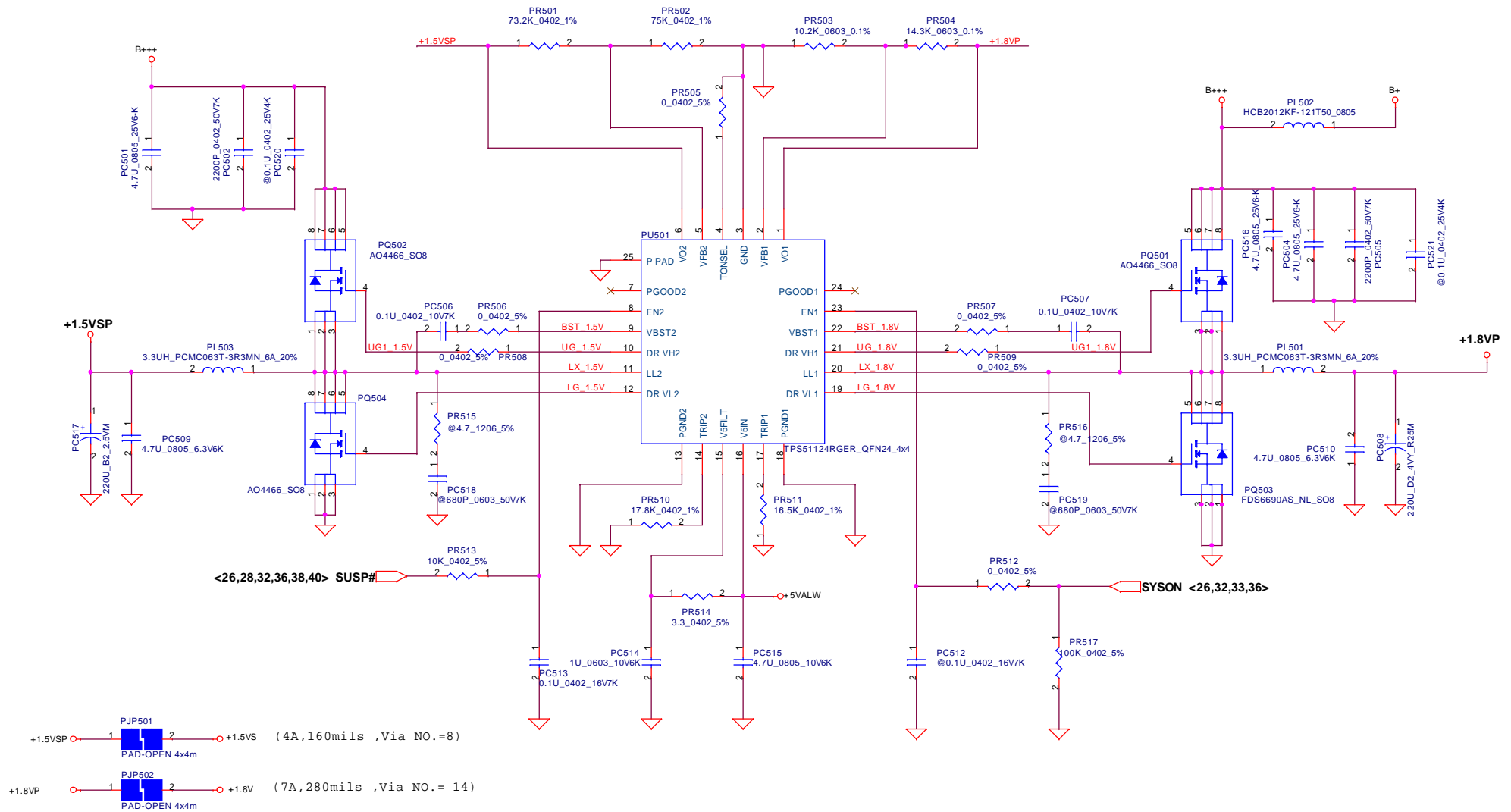
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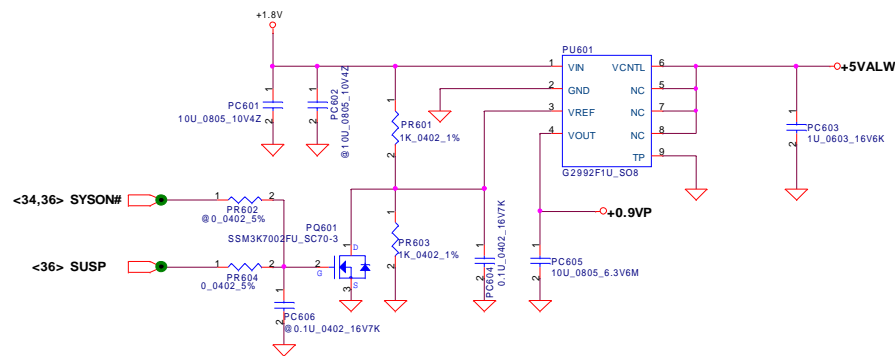


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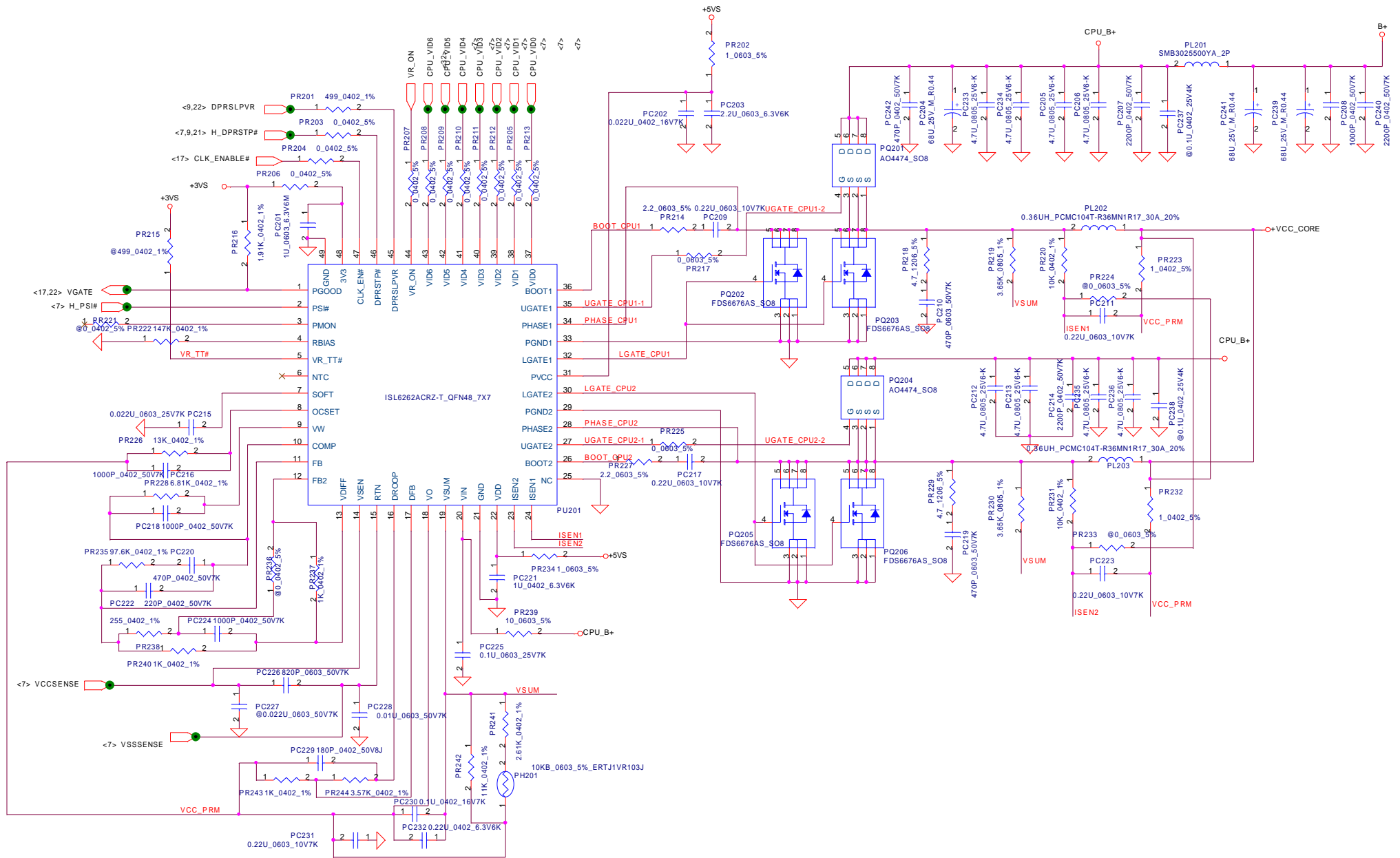


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Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
1	Transation Fail	08	C41、C42、C43、C44 Change ESR=7m ohm	11/21	SI-1
2	Disable TV out function from Docking	11、34	R61、R62、R63 change to 75 Ohm、TV_DCONSEL_0、TV_DCONSEL_1 connect to GND	11/07	SI-1
3	Update Connetor Library		CRT(JCRT1)、HDMI(JHDMI1)、ESATA(JP53)、Finger print(JJP24)、FAN(JP2)、Speaker(JP60)、Multi bay(JP12)、Dual LED(D53、D12)	11/17	SI-1
4	Delete LVDS B channel	11、19	Schematic Delete	11/17	SI-1
5	USB camera Footprint error	19	Change U42 to G916-390T1UF SOT23, it adjustable mode, R1091=215K、R1093=100K	11/07	SI-1
6	Reserve Card reader D3E function	22、27	GPIO6= CR_CPPE#、GPIO22=CR_WAKE#	11/17	SI-1
7	Swap PCIE LAN and New card	22	Swap PCIE4 and PICE6	11/17	SI-1
8	Add HDCP ROM for ICH9M	22、31	Add HDCP ROM for ICH9M	11/17	SI-1
9	Change G sensor control from SB、LED drive by +5VS	22、33	Change G sensor control from SB	11/17	SI-1
10	Avoid Battery mode can't boot issue	22、39	Add +3VALW GD to EC_RSMRST# to fix Battery mode can't boot issue	11/17	SI-1
11	Add G sensor ST and Bosch	24	Add G sensor ST and Bosch	11/17	SI-1
12	Change LAN solution (Marvell to Realtek)	25	Change LAN solution (Marvell to Realtek)	11/17	SI-1
13	LAN can't work	25	U46 Change to correct transformer type	11/17	SI-1
14	Cardreader schematic review and update, add D3E function	27	R709-->10K、R402-->8.2K、R704-->Stuff、R705-->@、U37-->@、Cardreader LED-->+5VS、add D3E function	11/17	SI-1
15	Jack can't detect normal	28	R1059 change from 39.2 to 39.2K	11/17	SI-1
16	Speaker work un normal	28	Add and Stuff C1362、R1065、R596	11/17	SI-1
17	HP audio team recommend	28、29	C285-C292、C1352、C1354 change to 0.022U、Amp output setup to 15.6 dB、Reserve C305、C306 for GNDA and GND	11/17	SI-1
18	Audio jack can't detect normal	29	Add Pull up resistor R401 to +3VALW	11/17	SI-1
19	Docking HP audio test fail	29	Add C295、BC296 to avoid DC level, and add R409、R410 to reduce HP out level	11/17	SI-1
20	Leakage problem	32	Correct direction prectect leakage	11/07	SI-1
21	EC pin define update	32	Delete EC_PME#、SYSON PU、SUSP# PU、LID_SW# change to +3VALW、Delete CLKRUN#、R582->@ for C0 chip、CIR PU+5VL、add 100P to BATT_OVP(EC recommend)	11/07	SI-1
22	Can't Hibernation(SLP_S4#)	32	Connect SLP_S4# to SB	11/17	SI-1
23	EC can't receive docking present	34	CONA# change +3VL	11/12	SI-1
24	HDMI can't detect	35	DDC_EN must enable、TMDS_B_HPD# inverse	11/07	SI-1
25	LVDS power on timing	19	C238 change to 0.047u to meet TI timing	01/03	SI-2
26	Prevent WWAN nosie	21	Add 12p on HDA_SDOOUT and HDA_SDOOUT	01/03	SI-2
27	Power leakage	21、31	Change HDCP ROM to +3VS power plane	01/03	SI-2
28	Prevent WLAN leakage	26	Add Diode prevent WLAN leakage	01/03	SI-2

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Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
29	New card PTH connector GND	26	New card PTH connector GND	01/03	SI-2
30	Change Cardreader LED control	27	Change Cardreader LED control	01/03	SI-2
31	Change SPDIF to SPDIF1	28	Change to SPDIF1	01/03	SI-2
32	Shut down pop noise	29	Change C293 to 1U	01/03	SI-2
33	Change BT power to +3VS	30	Change BT power to +3VS	01/03	SI-2
34	EMI Request	31	SPI_FSEL#、SPI_CLK_R、SPI_FWR# reserver RC	01/03	SI-2
35	Reserver 0 ohm co lay with common choke	35	Reserver 0 ohm co lay with common choke	01/03	SI-2
36	Sparate+5VS and +3VS power timing	36	Sparate+5VS and +3VS power timing	01/03	SI-2
37	Keyboard backlight reserve a 0805 size resistor	33	Keyboard backlight reserve a 0805 size resistor	01/03	SI-2
38	Change Lid switch connector type	33	Change Lid switch connector type	01/03	SI-2
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Version Change List (P. I. R. List) for Power Circuit

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	37	DC Connector /CPU_OTP	11/06	Compal	Add PD4 & PC12	Add PD4 & PC12	
2	39	3.3VALWP/5VALWP	11/06	Compal	for Layout	Change PQ301 cancel PQ303	
3	38	Charger	11/06	Compal	EMI solution	Add pc128	
4	43	+CPU_CORE	11/06	Compal	EMI solution	Add PC240	
5	39	3.3VALWP/5VALWP	11/14	Compal	for Layout	Change PL303 and PC310	
6	38	Charger	12/31	Compal	EMI solution	Add PC129, PC130, PC131, PC132, PC133	
7	43	+CPU_CORE	12/31	Compal	EMI solution	Add PC242	
8	39	3.3VALWP/5VALWP	12/31	Compal	PWR request	Add PU302, control signal changed to ACOFF	
9							
10							
11							
12							
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14							

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