

# Compal Confidential

## *Hadid M/B LA8554P Schematics Document*

*Intel Ivy Bridge ULV Processor with DDRIII memory down+ Panther Point*

*Date : 2012/5/23*

*Version 3.0*

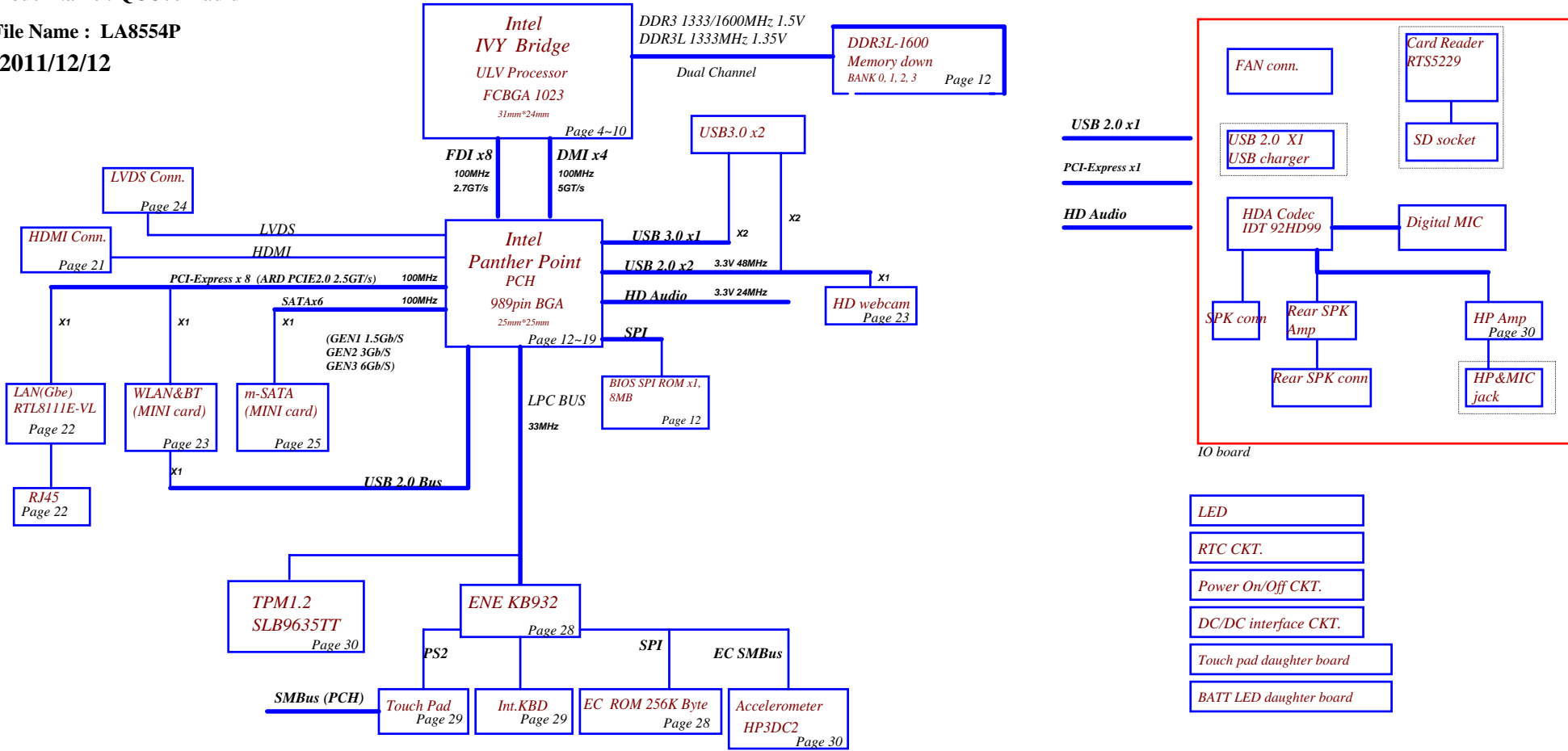
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Model Name : QCU00 Hadid

File Name : LA8554P

2011/12/12



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# QCU00 (LA-8554P Ver:0.1)

## Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS_VCCP	+V1.05SP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+VCCP	+VCCP (1.05V ) power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII (1.35V OR 1.5V)	ON	ON	OFF
+1.5VS	+1.5VS switched power rail	ON	OFF	OFF
+1.8VS	(+5VALW ) to 1.8V switched power rail to PCH	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+LAN_IO	+3VALW to +LAN_IO power rail for LAN	ON	ON	ON*
+3V_PCH	+3VALW to +3V_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5V_PCH	+5VALW to +5V_PCH power rail for PCH (Short resistor)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	B+ to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

### EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

### PCH SM Bus address

Device	Address
DDR DIMM0	
Mini Card2	
Mini Card3	
TP module	

### EC SM Bus2 address

Device	Address
PCH (Reserve)	1010 0110b
G-sensor	0101001b

### SMBUS Control Table

	SOURCE	BATT	Charger	HP Amp	MINI3	SODIMM	EC_SMB_CK2 EC_SMB_DA2	EC_SMB_CK1 EC_SMB_DA1	G-Sensor	TP
EC_SMB_CK1 EC_SMB_DA1	KB932	V	V						V	
EC_SMB_CK2 EC_SMB_DA2	KB932			V						
PCH_SMBCLK PCH_SMBDATA	PCH				V					V
PCH_SML1CLK PCH_SML1DATA	PCH					V				

CLKOUT	DESTINATION
PCI0	PCH_LPBACK
PCI1	PCI_LPC
PCI2	None
PCI3	None
PCI4	None

SATA	DESTINATION
SATA0	None
SATA1	m-SATA,JMINI2
SATA2	None
SATA3	None
SATA4	None
SATA5	None


### USB Port Table


USB 2.0	USB 1.1	Port	1 External USB Port
EHCI1	UHCI0	0	USB2.0 (left side)
		1	USB2.0 (Right side)
	UHCI2	2	
		3	
		4	
		5	
EHCI2	UHCI4	6	
		7	
	UHCI5	8	Camera
		9	BT
		10	
		11	
UHCI6	12		
	13		

USB 3.0	Port	1 External USB Port
	1	USB3.0 (left)
	2	
	3	
	4	

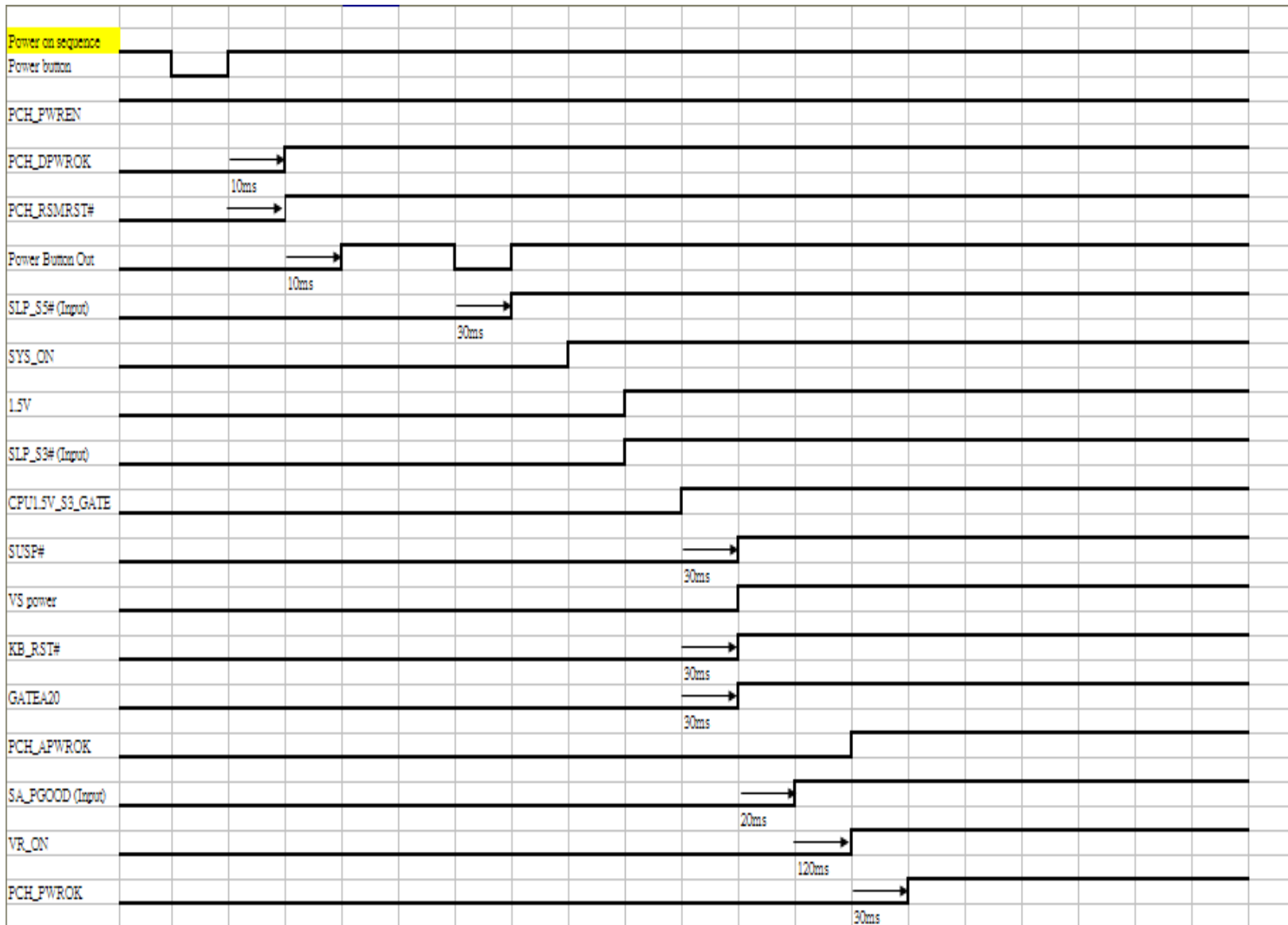
CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	10/100/1G LAN	CLKOUTFLEX0	None
	CLKOUT_PCIE1	WLAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	None	CLKOUTFLEX2	None
	CLKOUT_PCIE3	CARD READER	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

Symbol Note :

 : means Digital Ground

 : means Analog Ground

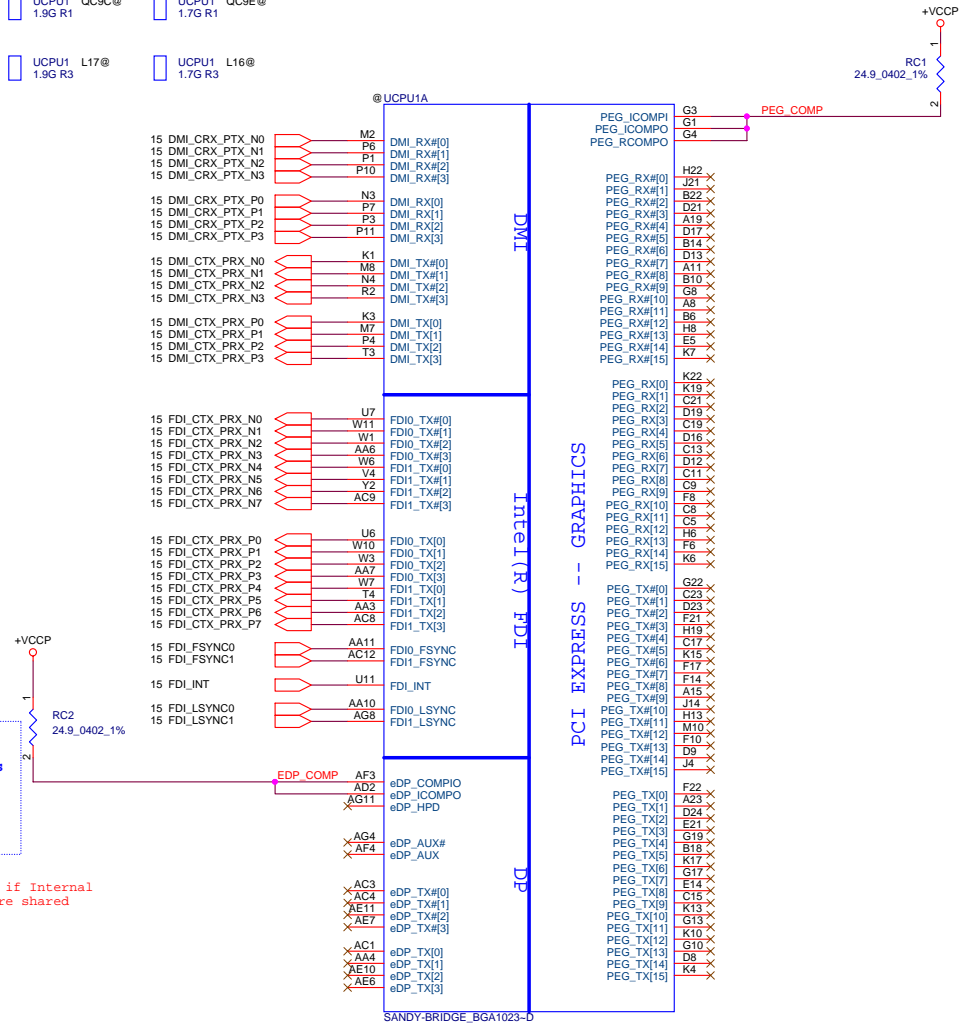
Option	@	CONN@		
UMA	X	X	V	



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- UCPU1 QBP8@ 1.5G R1
- UCPU1 QBP7@ 1.7G R1
- UCPU1 QC52@ 2.0G R1
- UCPU1 QC9B@ 2.0G R1
- UCPU1 L18@ 2.0G R3
- UCPU1 QBTP@ 1.5G R3
- UCPU1 QC53@ 1.9G R1
- UCPU1 QC9C@ 1.9G R1
- UCPU1 L17@ 1.9G R3
- UCPU1 QBP5@ 1.7G R1
- UCPU1 QC55@ 1.8G R1
- UCPU1 QC9E@ 1.7G R1
- UCPU1 L16@ 1.9G R3
- UCPU1 QBTO@ 1.7G R1
- UCPU1 QC56@ 1.7G R1

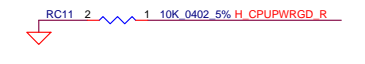
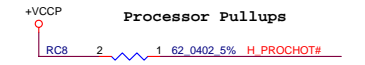
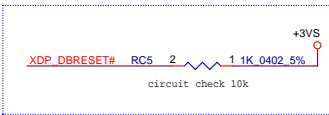
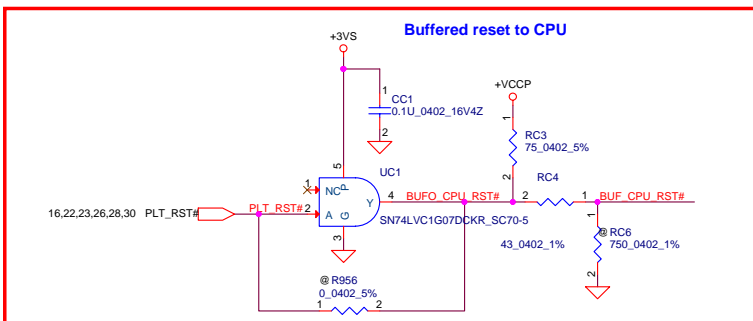
PEG\_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms  
 PEG\_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms



eDP\_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

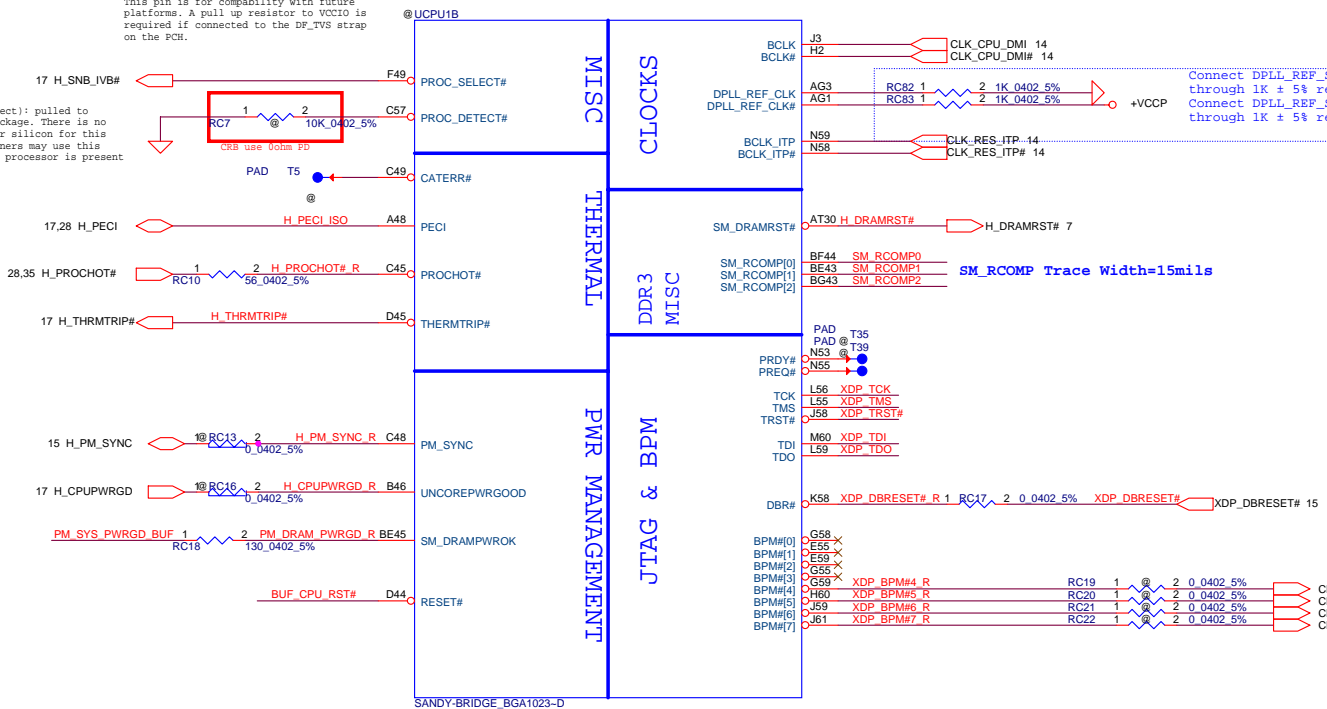
NOTE: eDP\_COMPIO and eDP\_ICOMPO should not be left floating even if Internal Graphic is disabled since they are shared with other interfaces

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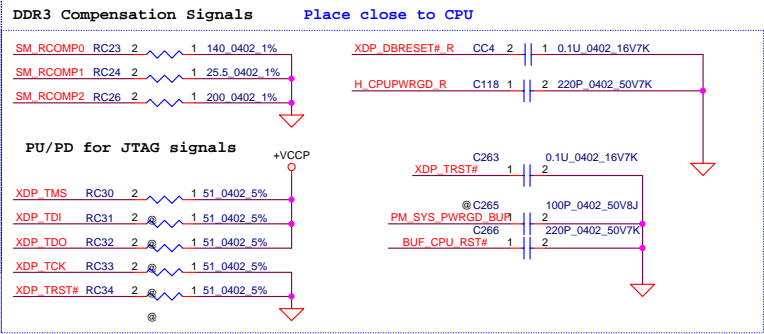
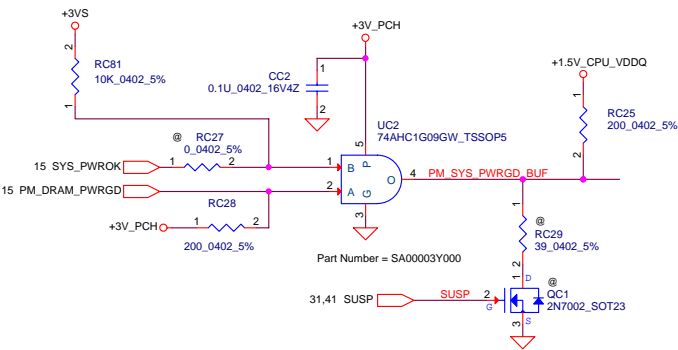
PROC\_DETECT (Processor Detect): pulled to ground on the processor package. There is no connection to the processor silicon for this signal. System board designers may use this signal to determine if the processor is present

This pin is for compatibility with future platforms. A pull up resistor to VCCIO is required if connected to the DP\_TVS strap on the FCH.



Connect DPPLL\_REF\_SSCLK on Processor to GND through 1K ± 5% resistor.  
Connect DPPLL\_REF\_SSCLK# on Processor to VCCP through 1K ± 5% resistor

SM\_RCOMP Trace Width=15mils

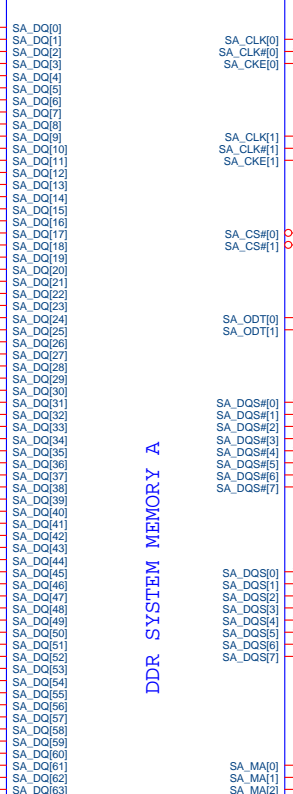


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12 DDR\_A\_D[0..63]

UCPU1C



DDR SYSTEM MEMORY A

SANDY-BRIDGE\_BGA1023-D

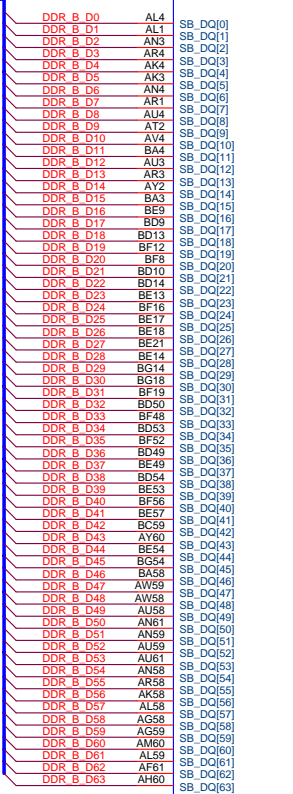
12 DDR\_A\_BS0  
12 DDR\_A\_BS1  
12 DDR\_A\_BS2

12 DDR\_A\_CAS#  
12 DDR\_A\_RAS#  
12 DDR\_A\_WE#



12 DDR\_B\_D[0..63]

UCPU1D

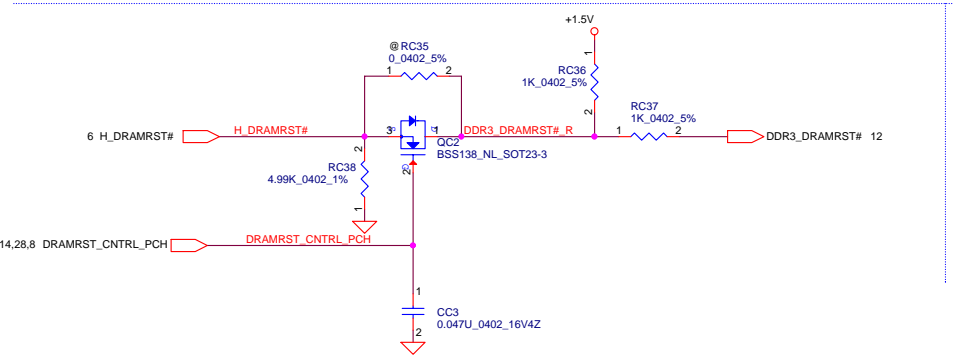
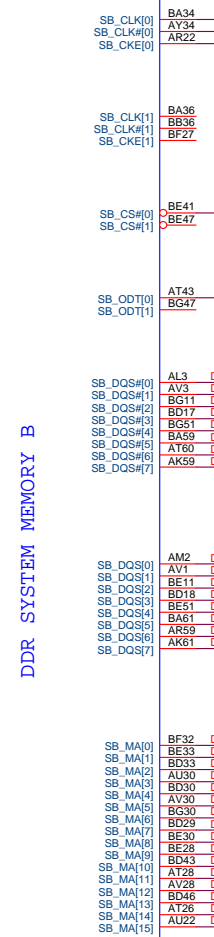


DDR SYSTEM MEMORY B

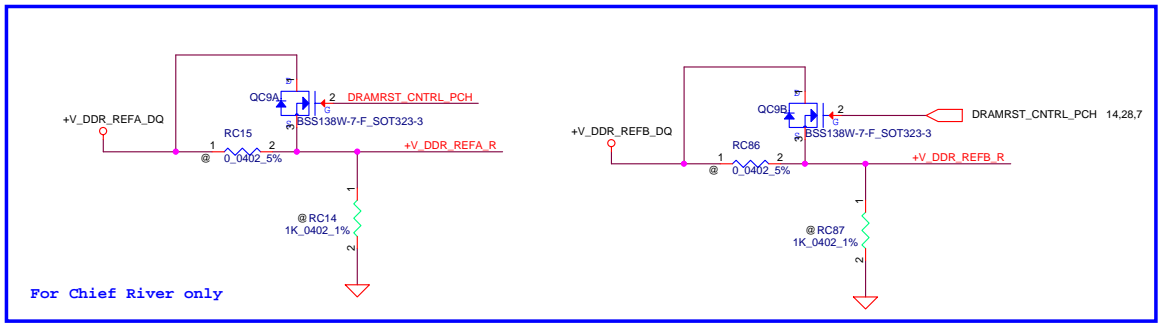
SANDY-BRIDGE\_BGA1023-D

12 DDR\_B\_BS0  
12 DDR\_B\_BS1  
12 DDR\_B\_BS2

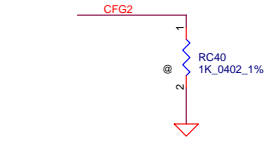
12 DDR\_B\_CAS#  
12 DDR\_B\_RAS#  
12 DDR\_B\_WE#



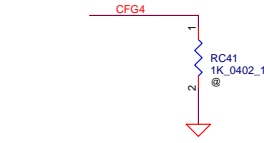
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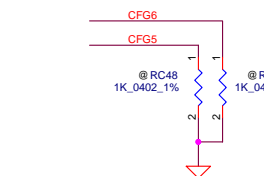
CFG Straps for Processor



PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	* 1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed



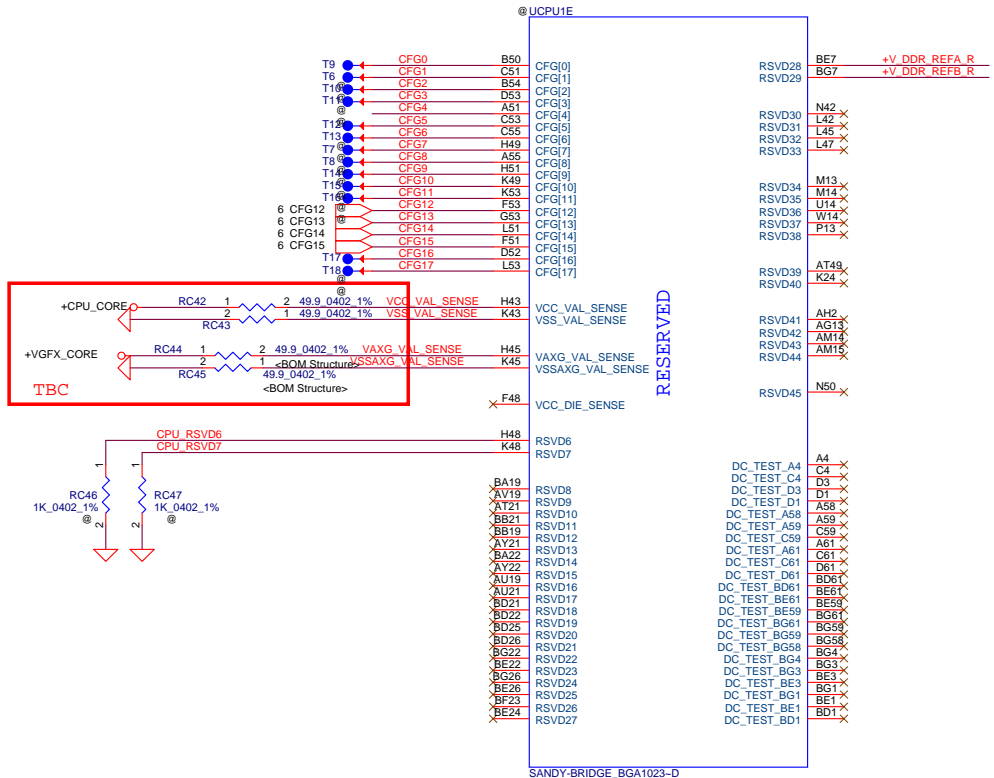
Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



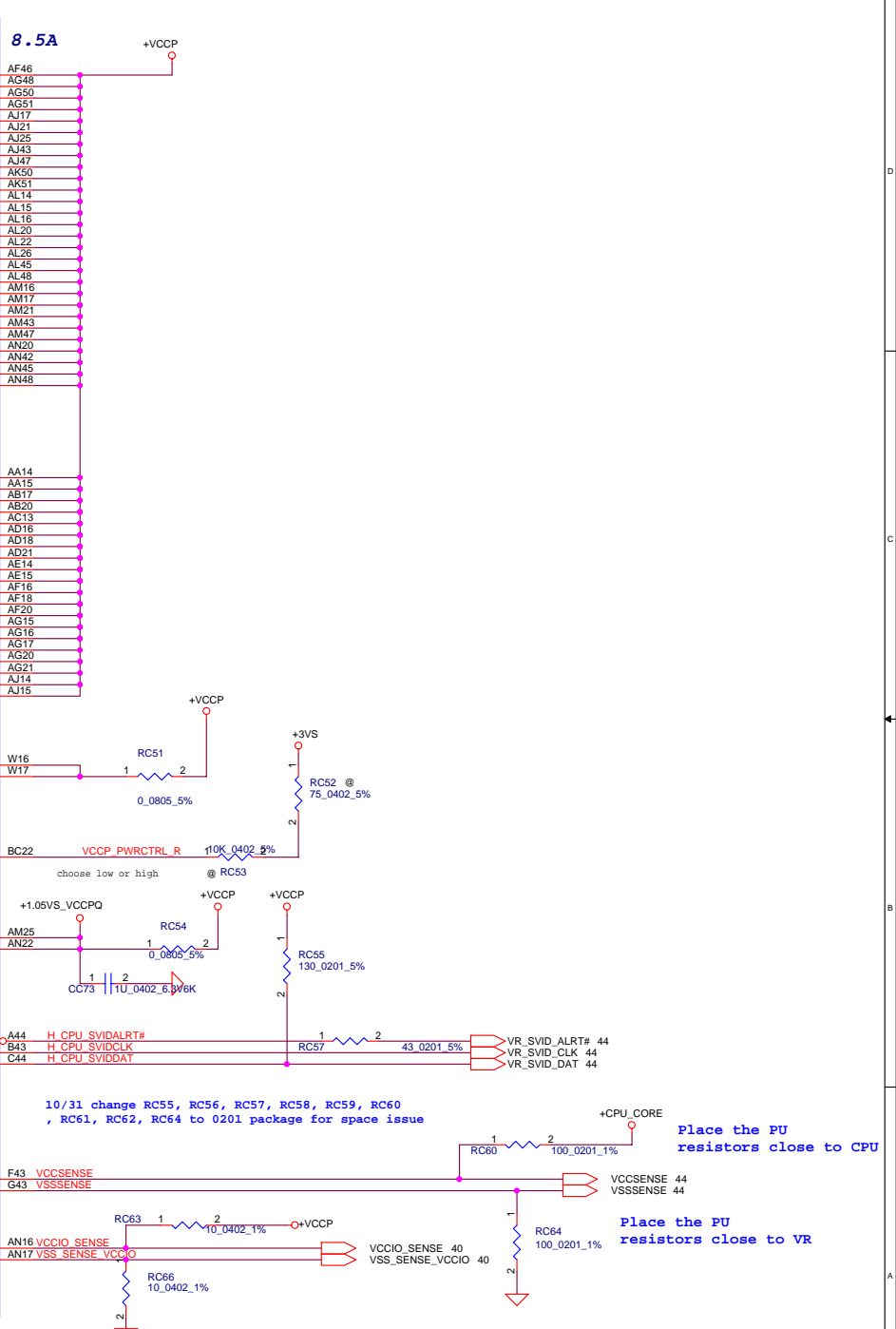
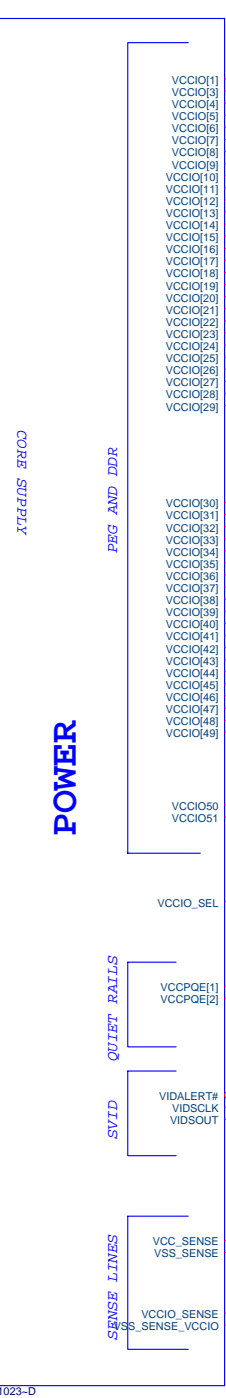
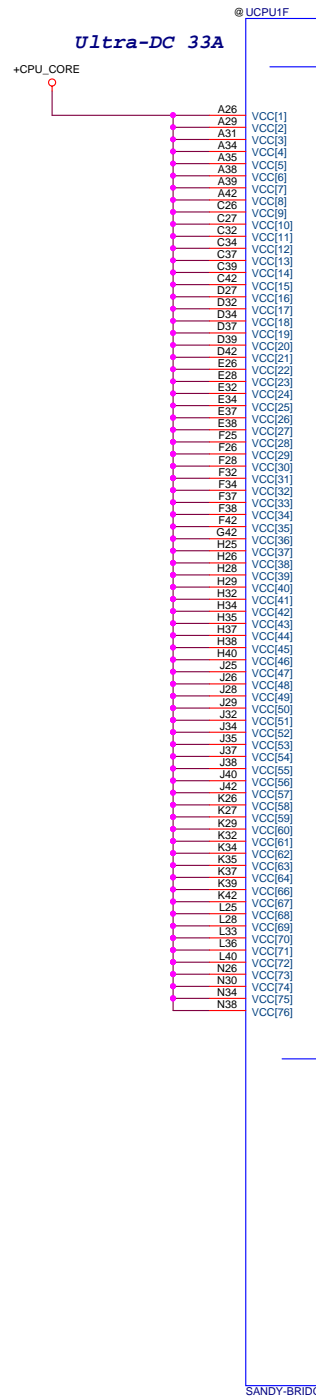
PCIe Port Bifurcation Straps	
CFG[6:5]	* 00 = 1 x 8, 2 x 4 PCI Express 01 = reserved 10 = 2 x 8 PCI Express 11 = 1 x 16 PCI Express



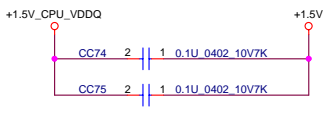
PEG DEFER TRAINING	
CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training







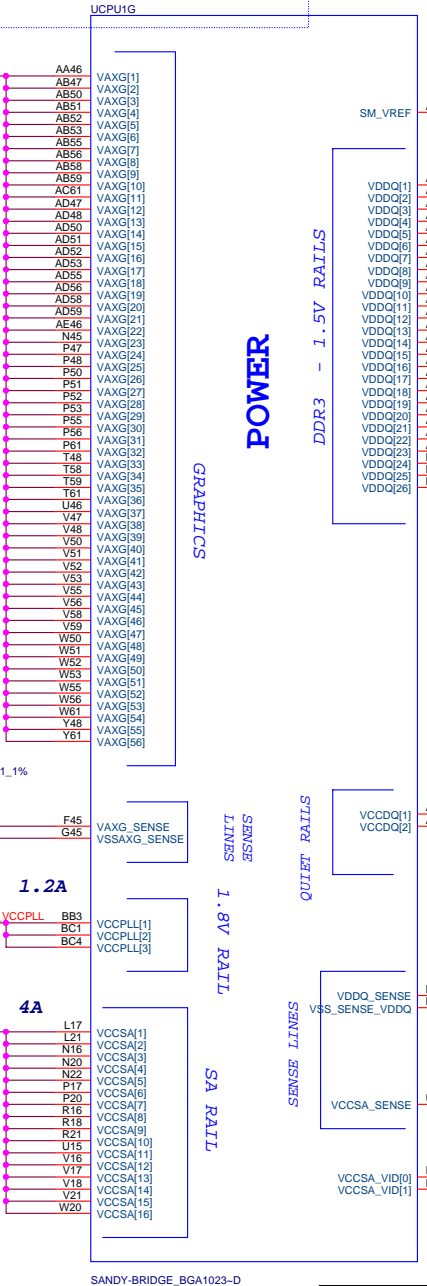
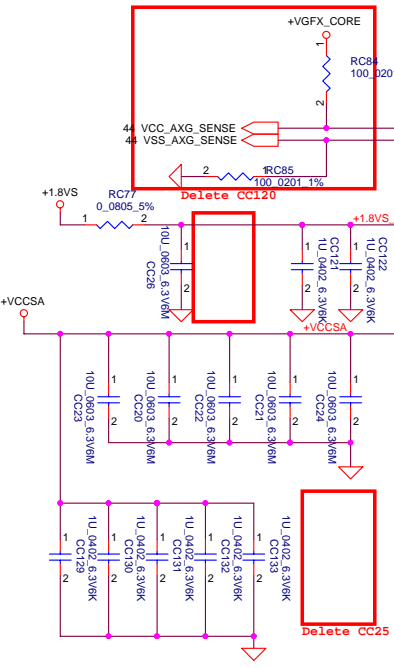
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- Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,
- VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed



12/6 Base on Intel review result, change to 100 ohm



**POWER**

**GRAPHICS**

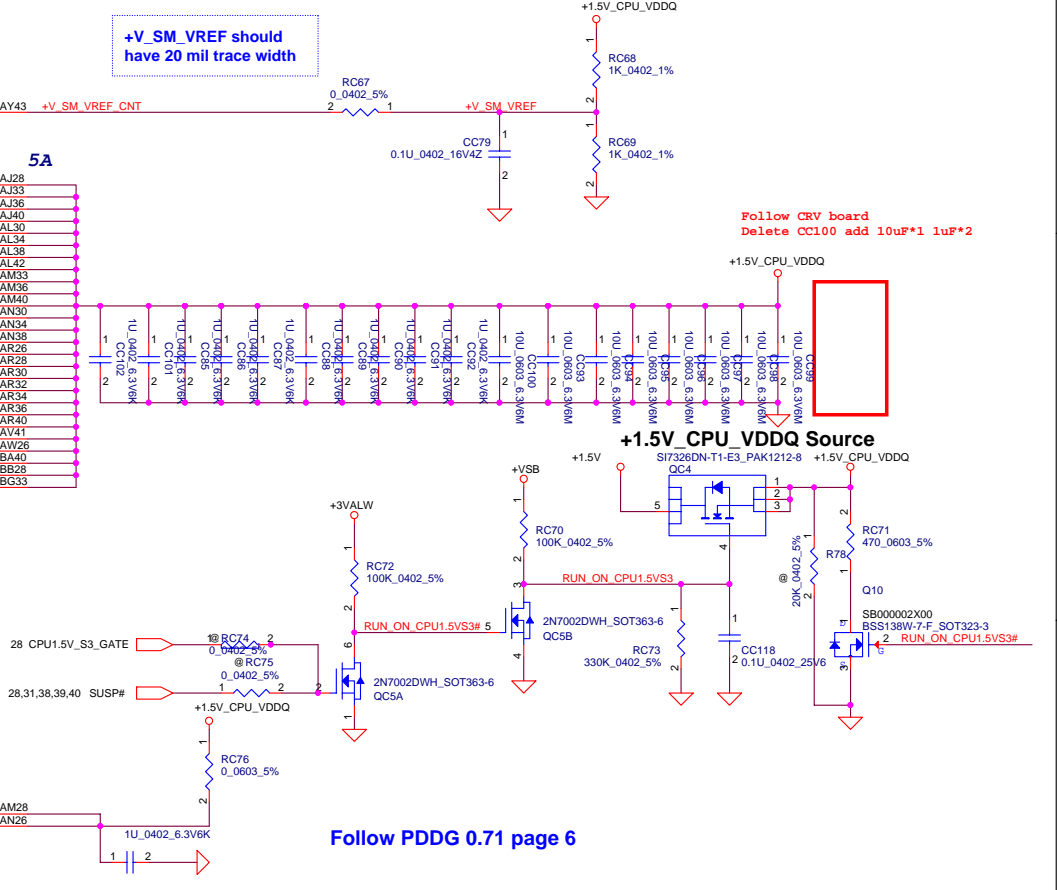
**DDR3 - 1.5V RAILS**

**QUIET RAILS**

**SENSE LINES**

**SA RAIL**

+V\_SM\_VREF should have 20 mil trace width

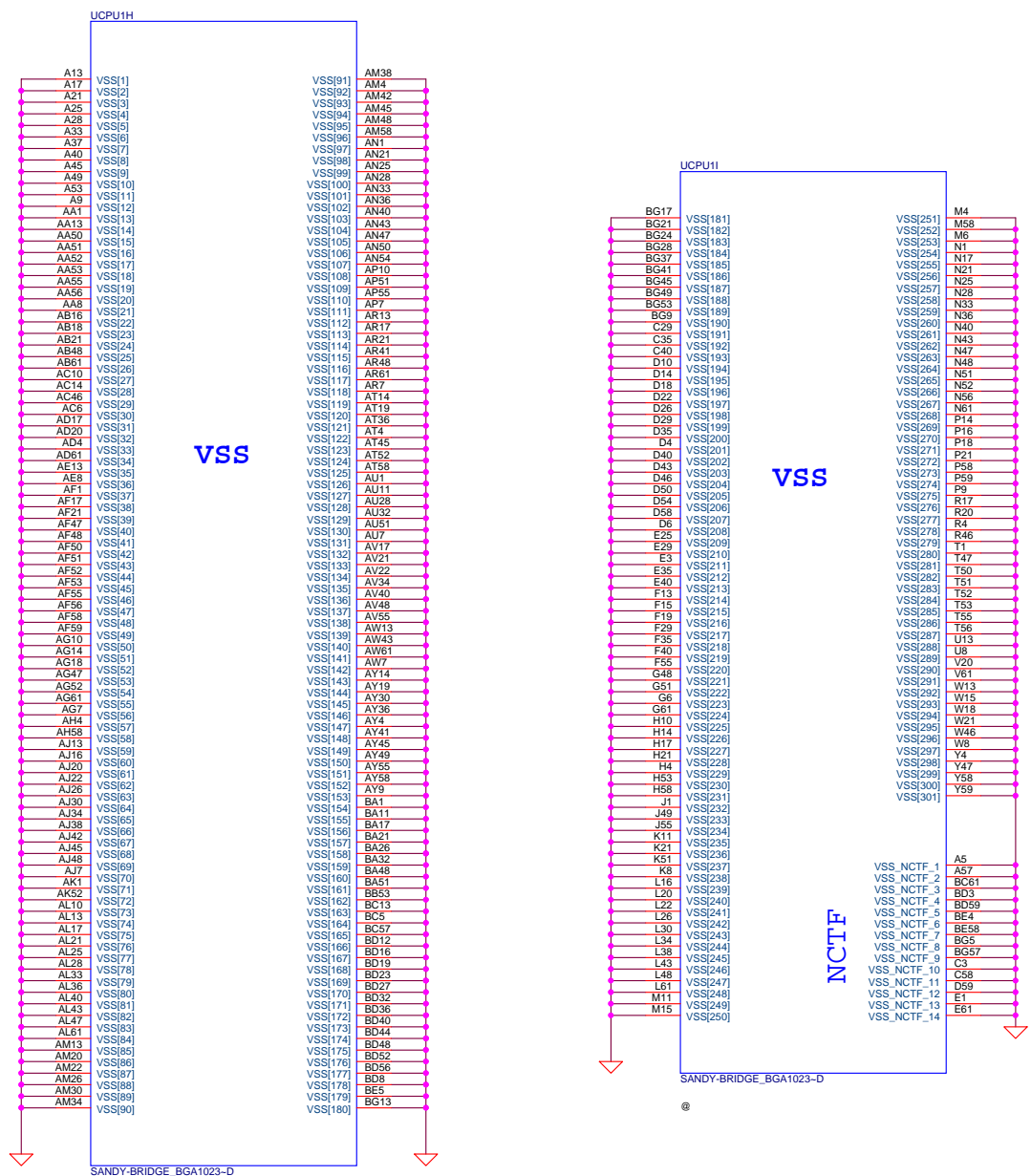


Follow CRV board Delete CC100 add 10uF\*1 1uF\*2

Follow PDDG 0.71 page 6

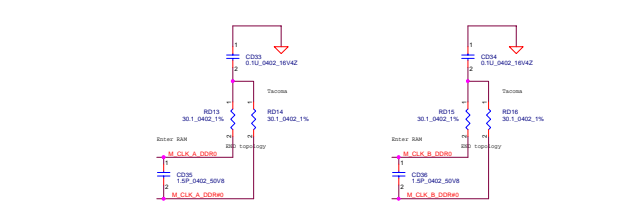
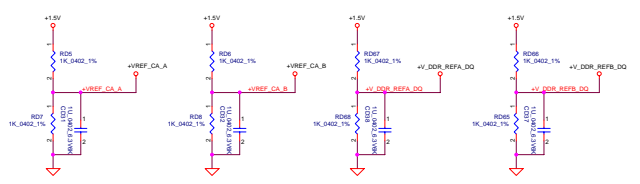
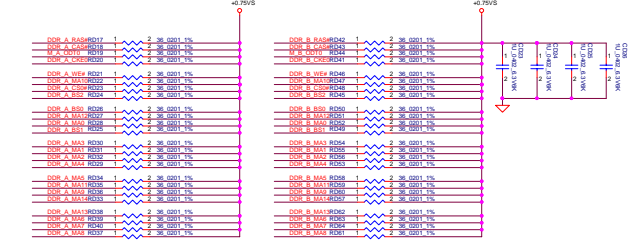
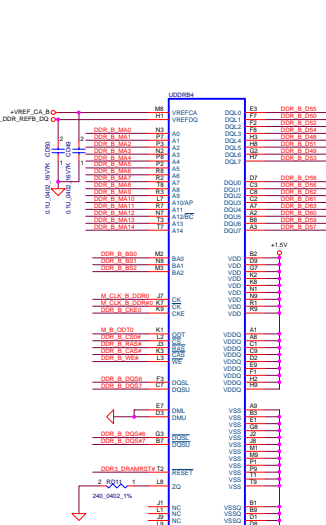
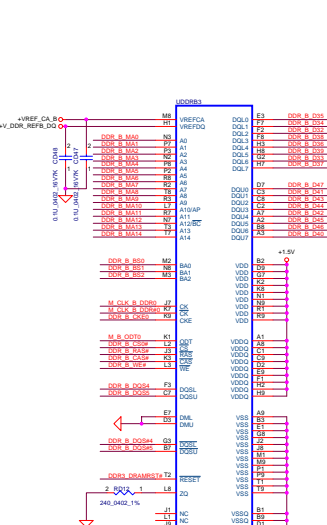
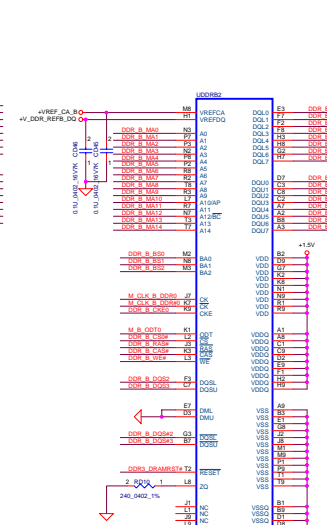
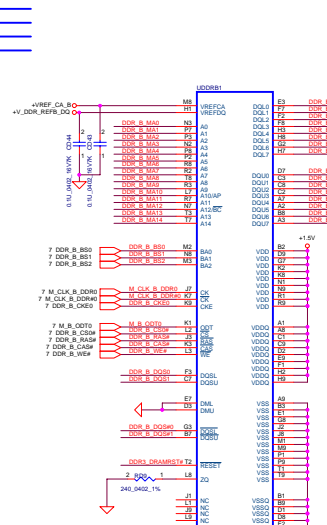
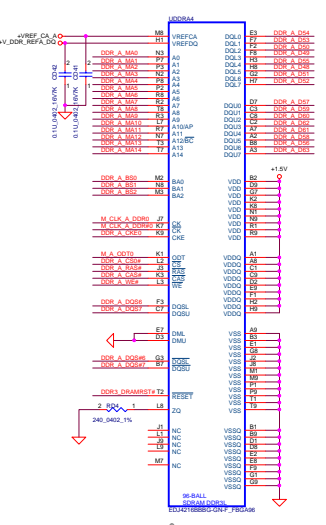
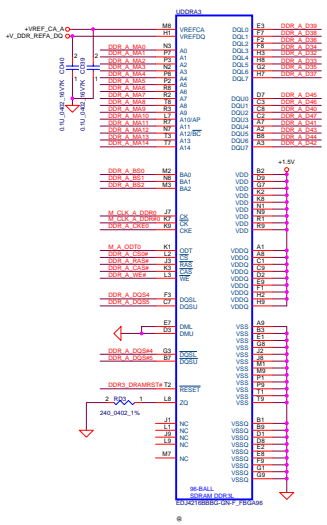
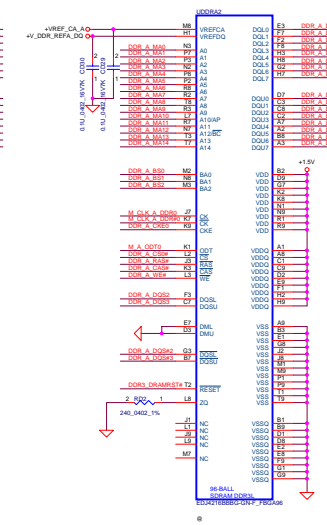
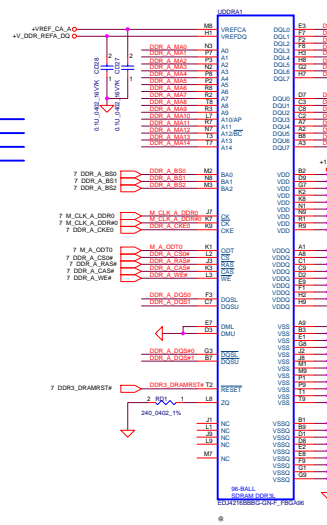
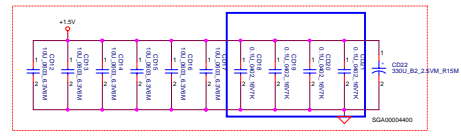
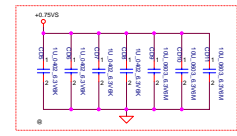
VCCSA				
VID0	VID1	Vout	Sandy	Ivy
0	0	0.9V	V	V
0	1	0.8V	V	V
1	0	0.725V	X	V
1	1	0.675V	X	V

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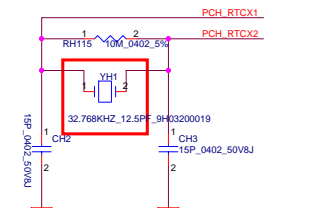


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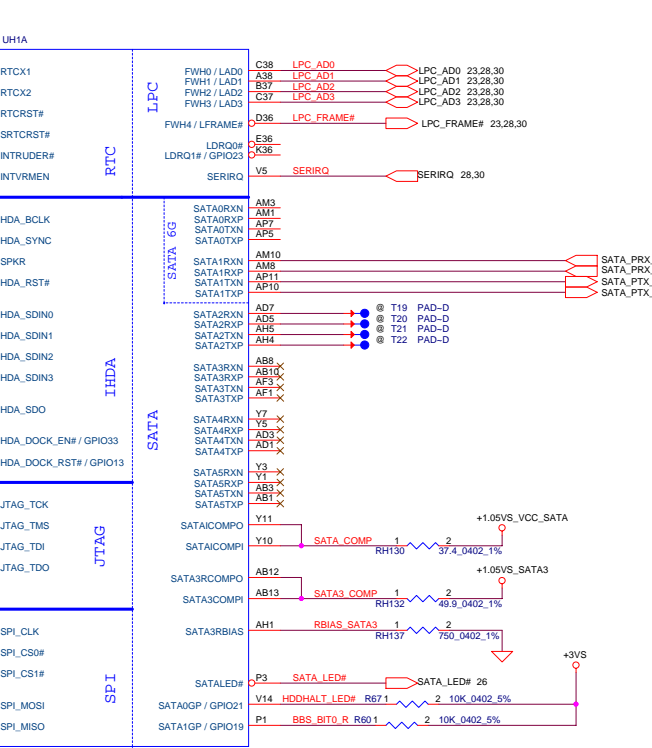
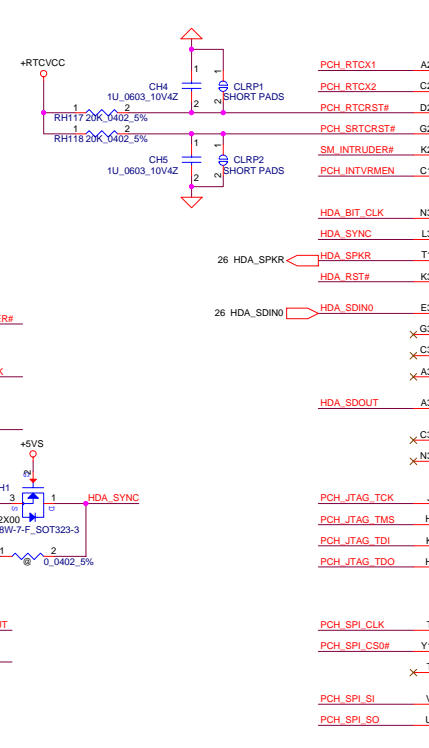
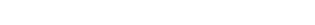
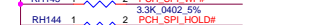
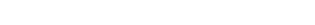
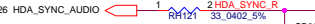
**Layout Note:**  
Place near memory group



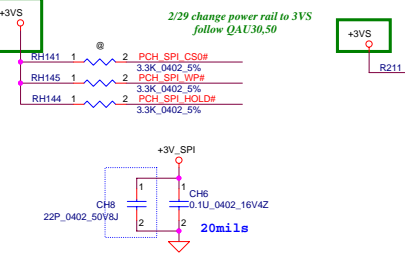
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4019HW					



1/13 Change dimension to standard part

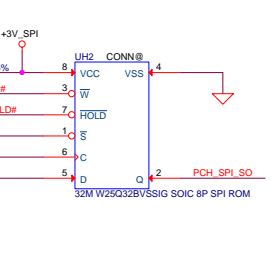


**SPI ROM FOR BIOS&ME ( 8MByte )**

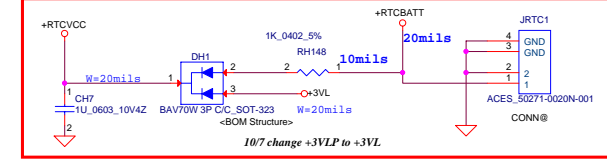


11/01 add CH8 for RF request

**8MByte SPI ROM PN SA000039A00**

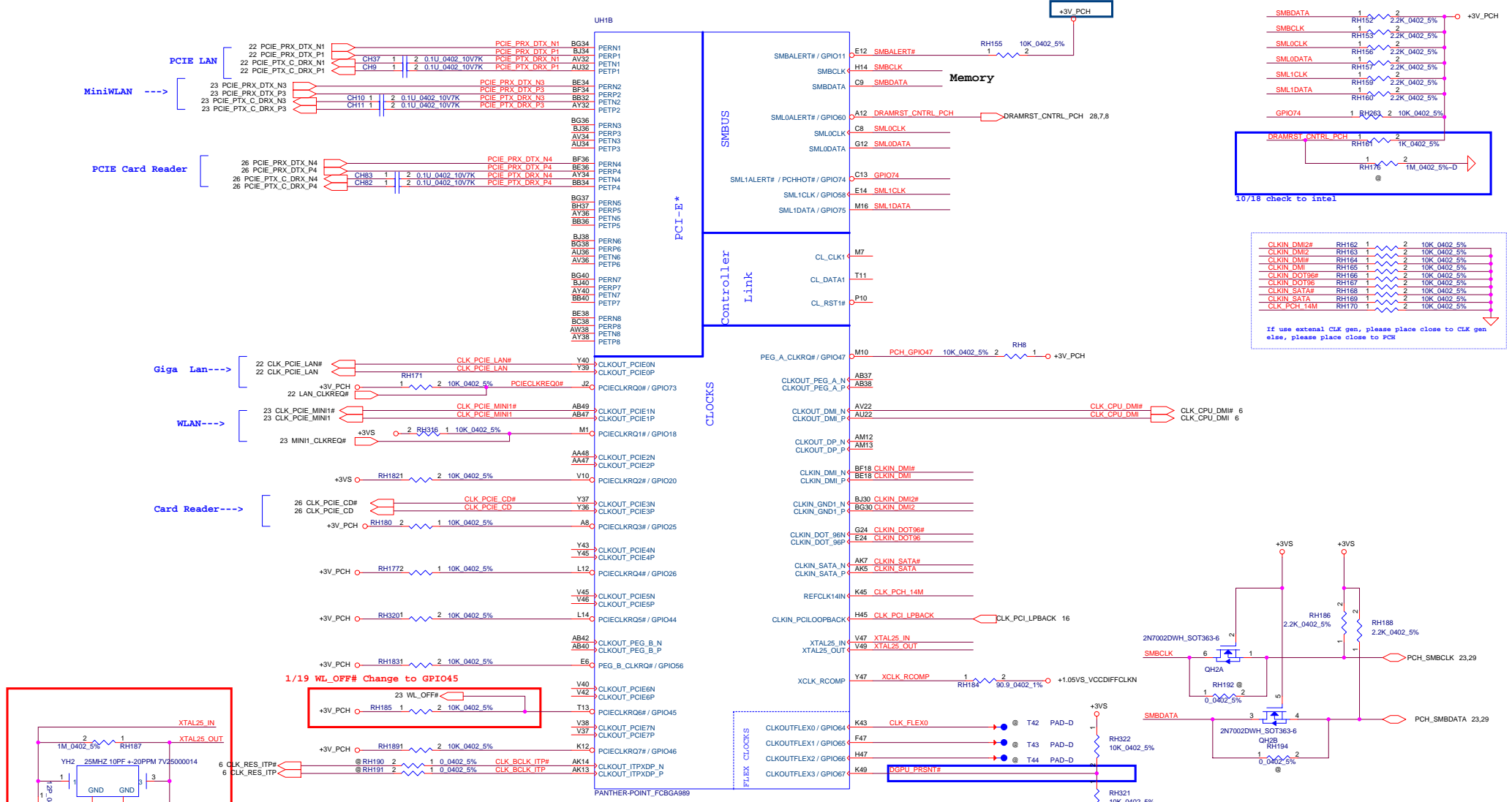


**RTC Battery**

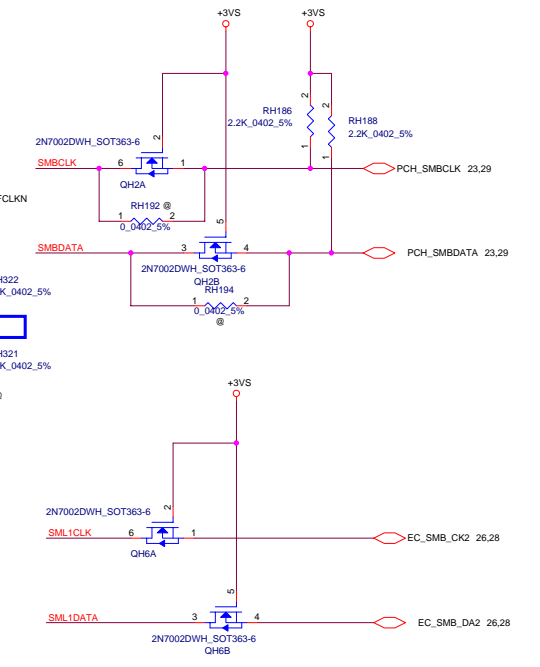
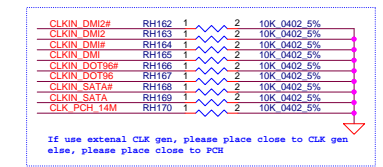
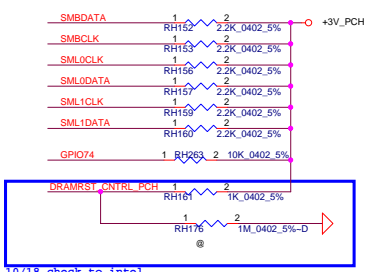
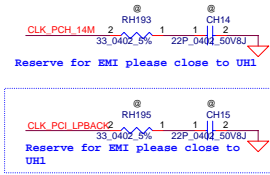
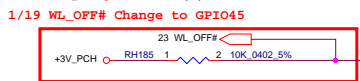
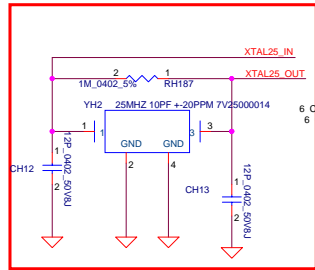


1/5 Modify PIN define

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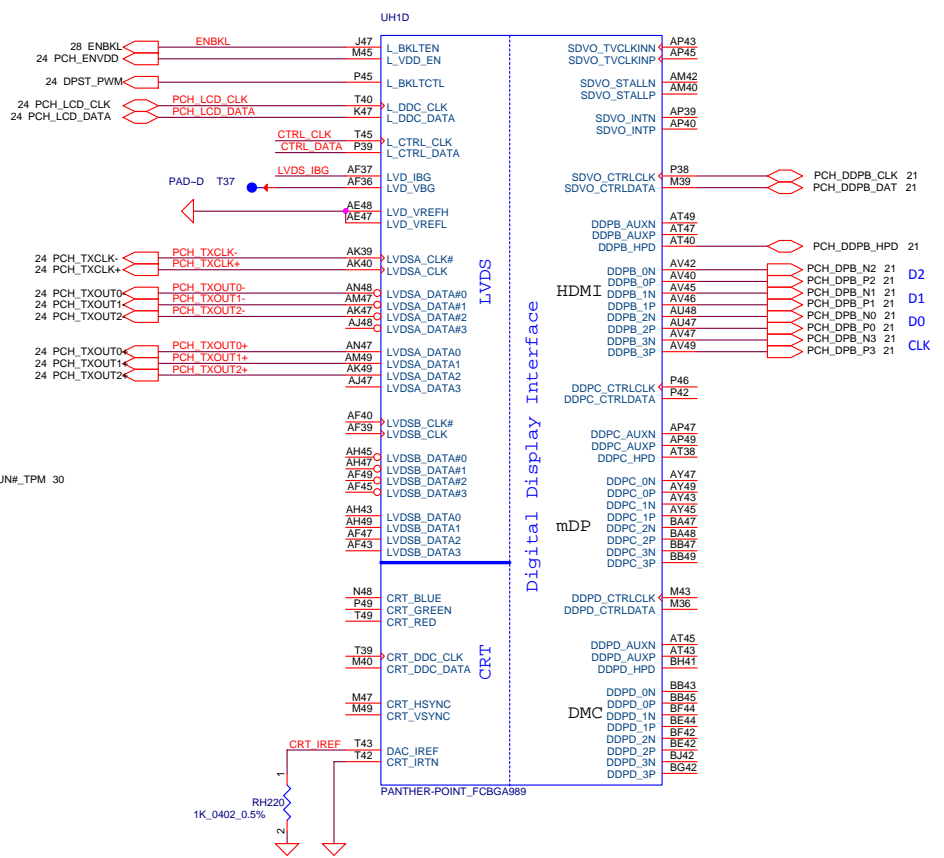
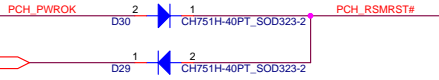
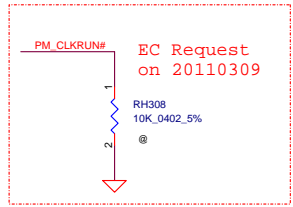
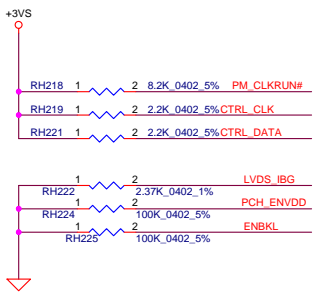
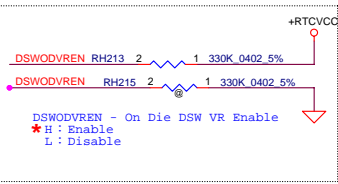
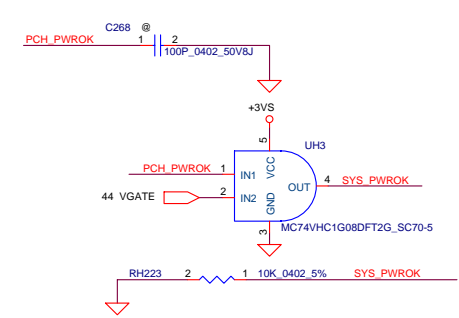
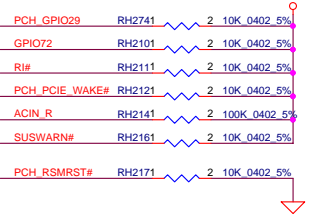
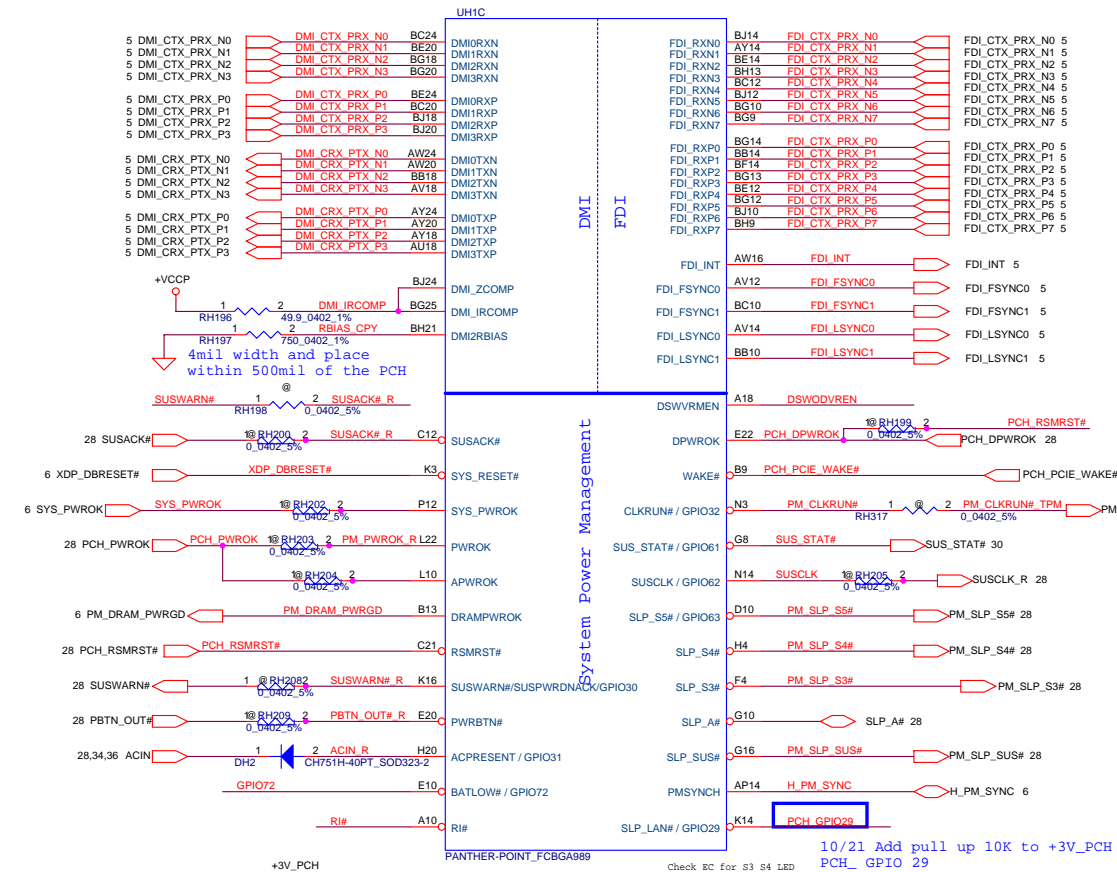


1/13 YH2 Change dimension to standard part

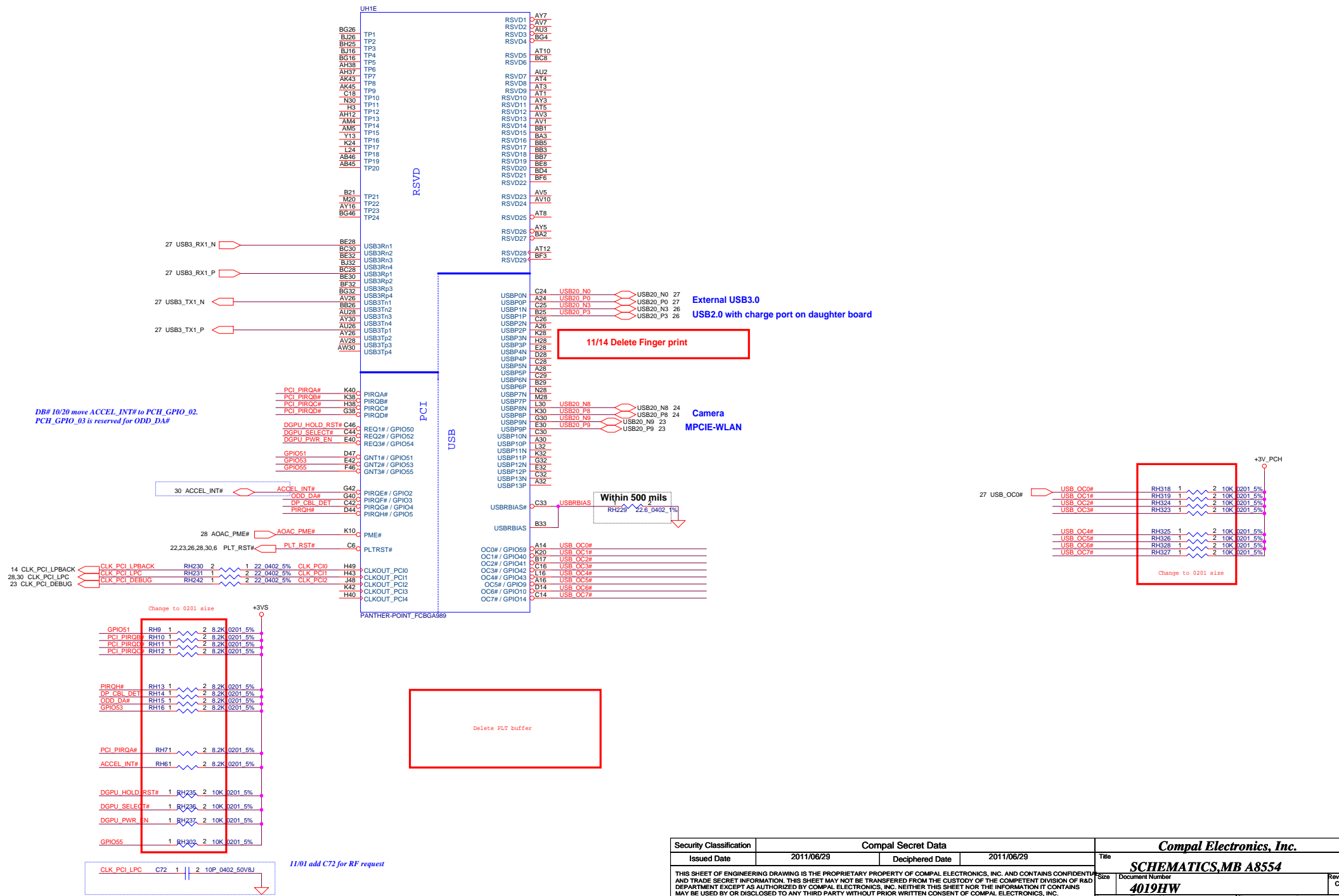


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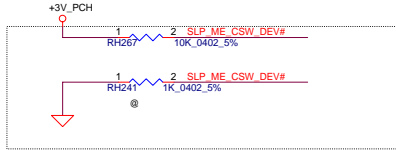


GPI028

On-Die PLL Voltage Regulator

This signal has a weak internal pull up

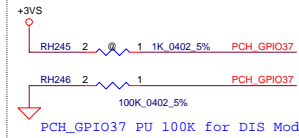
- \* H : On-Die voltage regulator enable
- L : On-Die PLL Voltage Regulator disable



10/21 Common BT\_ON is GPIO 34  
(Route to GPIO 38 currently), GPIO 38 pull  
high 10K to 3VS only

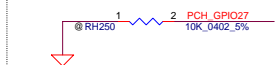
PCH\_GPIO37  
FDI TERMINATION VOLTAGE OVERRIDE

- \* LOW - Tx, Rx terminated to same voltage (DC Coupling Mode)

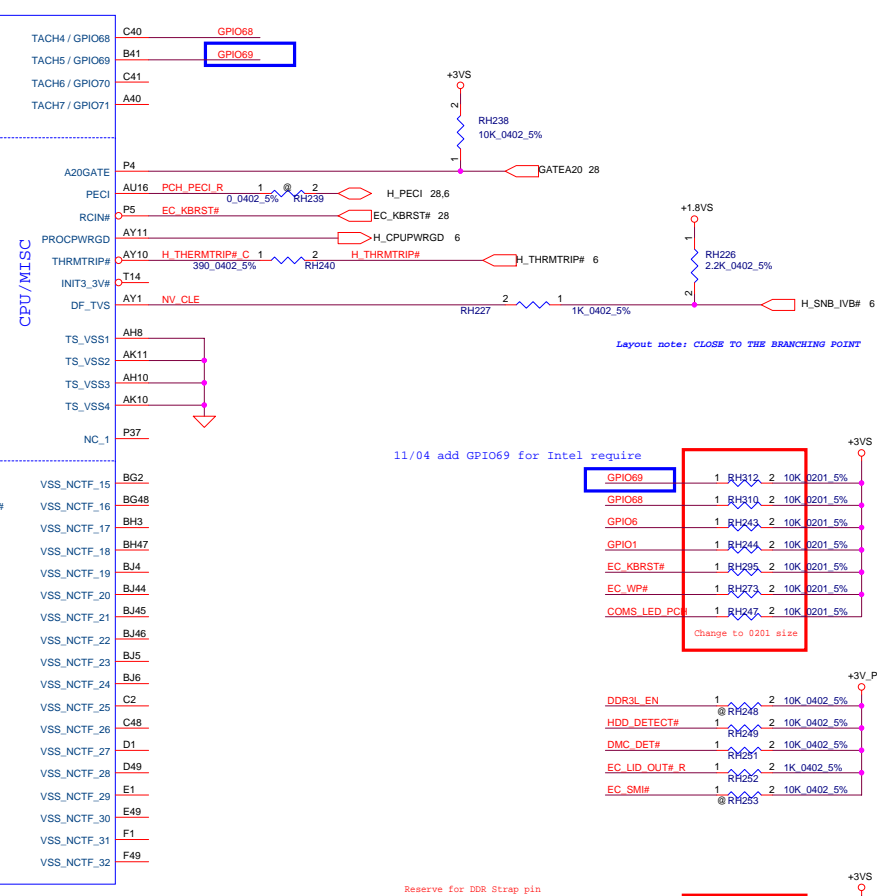
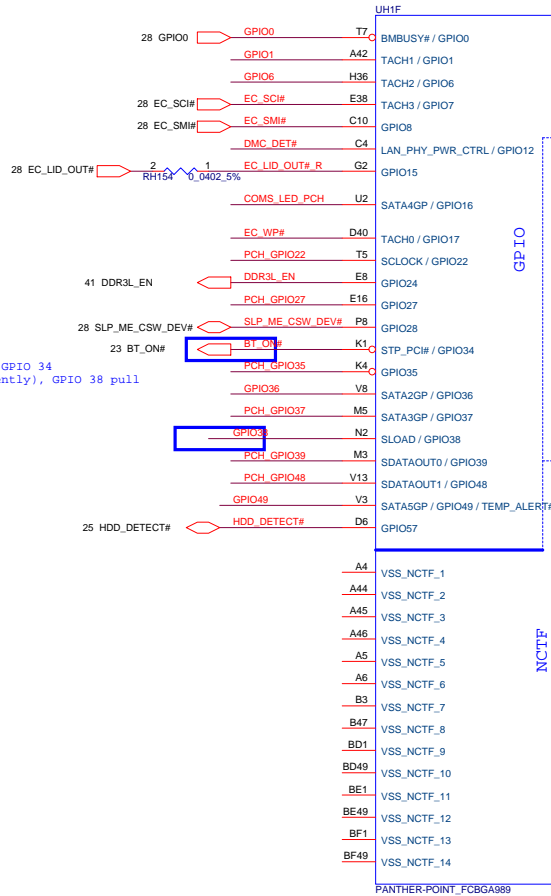
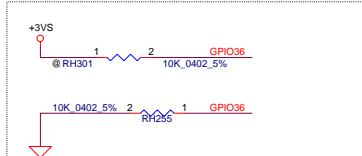


GPI027  
PCH\_GPIO27 (Have internal Pull-High)

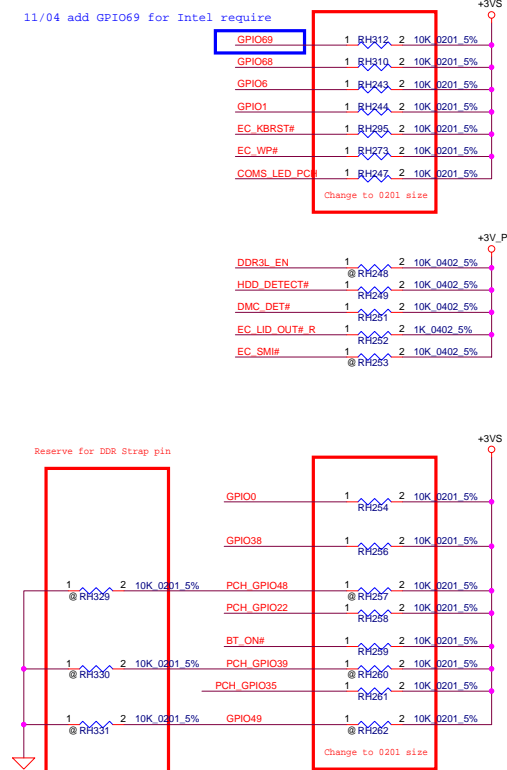
- \* High: VCCVRM VR Enable
- Low: VCCVRM VR Disable



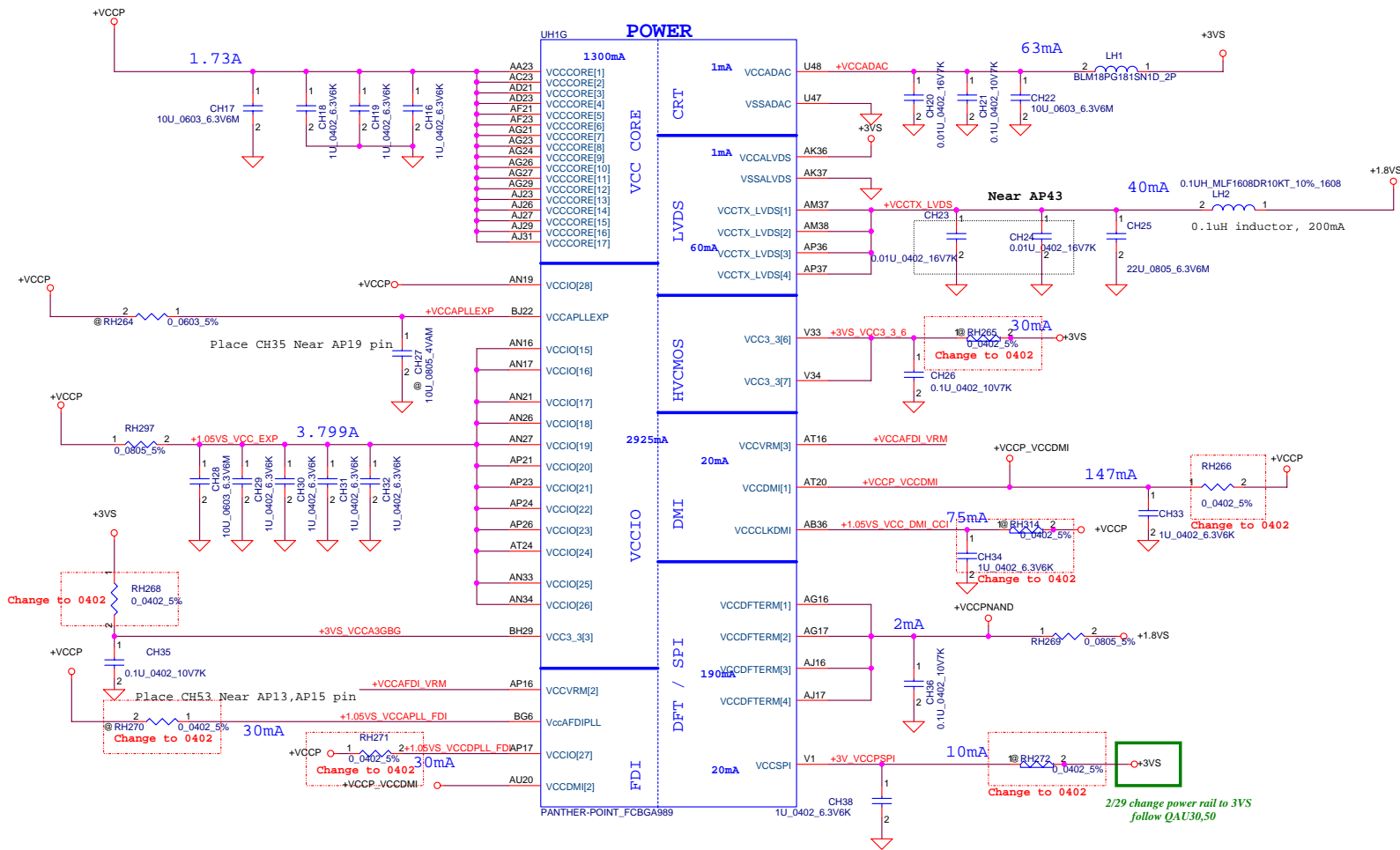
10/23 reserve GPIO 36 pull up resistor and add pull down resistor



DDR strap pin Vendor/PN	GPIO39	GPIO48	GPIO49
Samsung SA00005Q100 256M16/1600 K4B4G1646B-HCKO FBGA	RH330 0	RH329 0	RH331 0
Hynix SA00005G100 256M16/1600 H5TQ4G63MFR-PBC FBGA	RH330 0	RH329 0	RH262 1
Elpida SA00005HT10 256M16/1600 EJ742162B8B-GN-F 96P	RH330 0	RH257 1	RH331 0
Samsung SA00005J000 256M16/1600 K4B4G1646B-HYK0 FBGA	RH330 0	RH257 1	RH262 1
Hynix SA00005AV00 256M16/1600 H5TC4G63MFR-PBA 96P	RH260 1	RH329 0	RH331 1
	RH260 1	RH329 0	RH262 1



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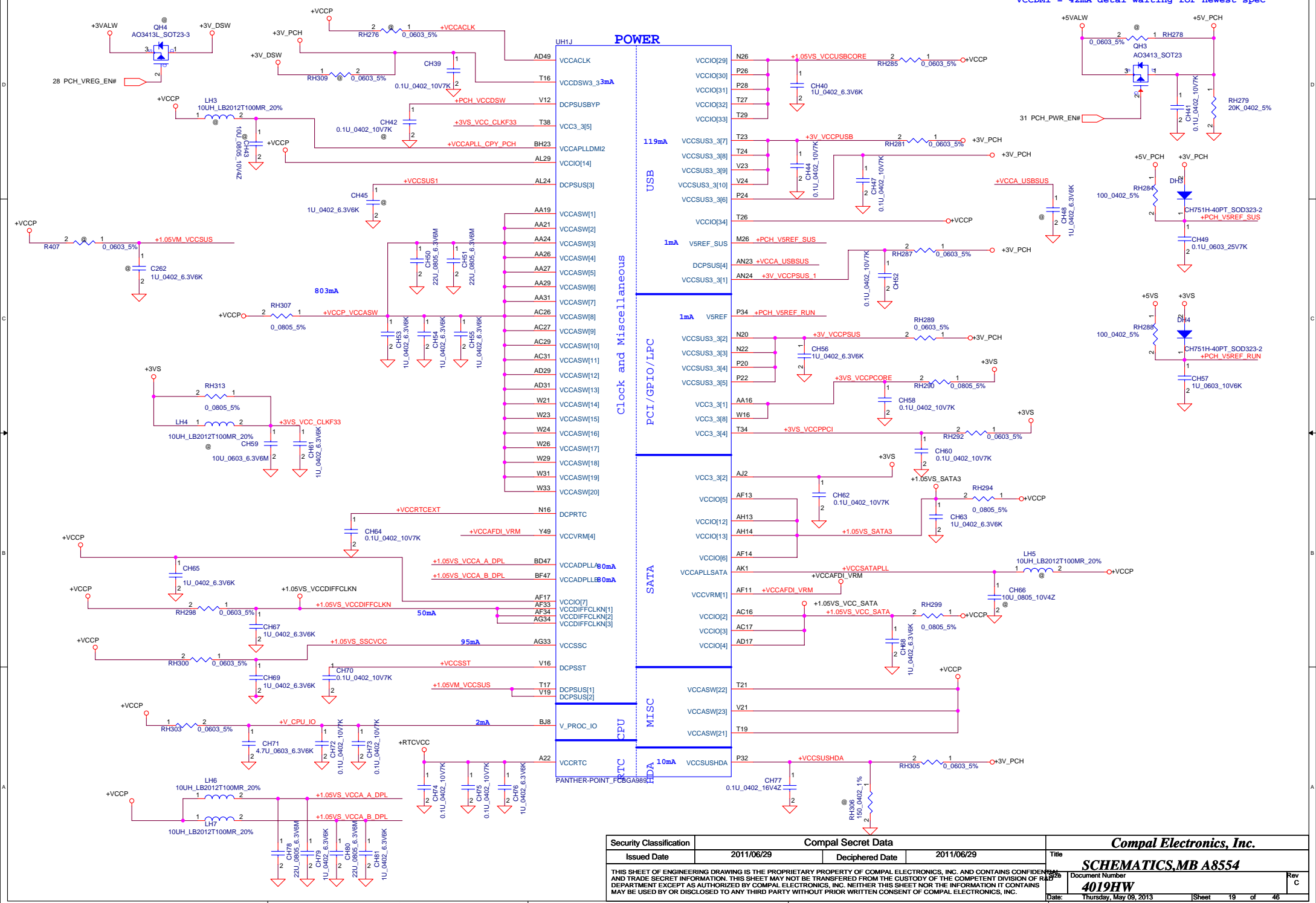
**Table B-6. Measured I<sub>CC</sub> (Mobil)**

Voltage Rail	Voltage (V)	50 Inmax Current Integrated Graphics? (A)
V <sub>PRDQ</sub> _I <sub>D</sub>	1.05 / 1.0	0.002
VSREF	5	0.001
VSREF_Sus	5	0.001
Vcc3_3	3.3	0.178
VccADAC <sup>1</sup>	3.3	0.063
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore (Internal Suspend VR mode using INTVRMEN)	1.05	1.73
VccCore (External Suspend VR mode using INTVRMEN)	1.05	1.61
VccDMI	1.1	0.047

**Table B-6. Measured I<sub>CC</sub> (Mobil)**

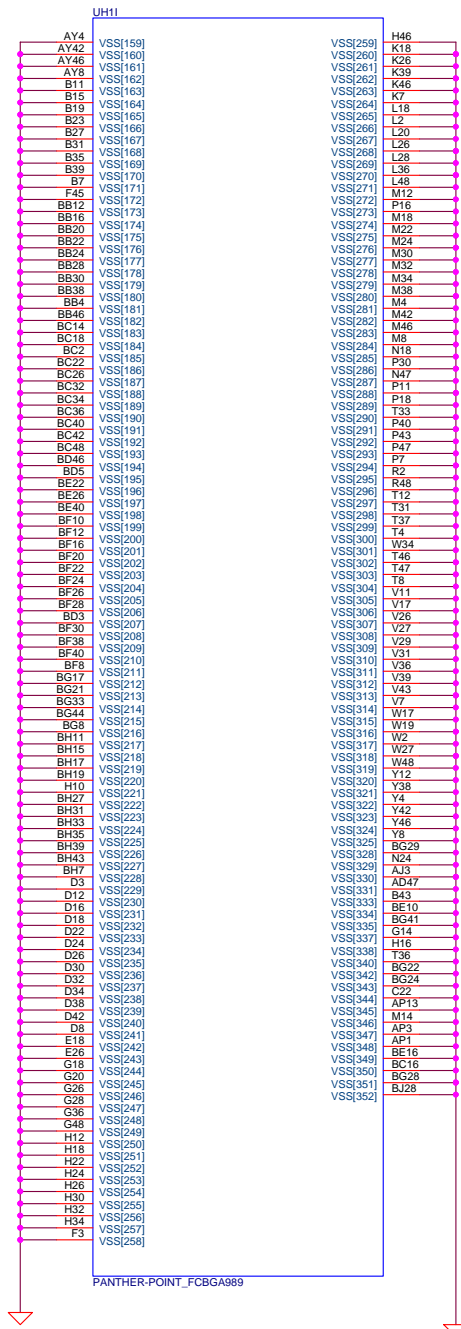
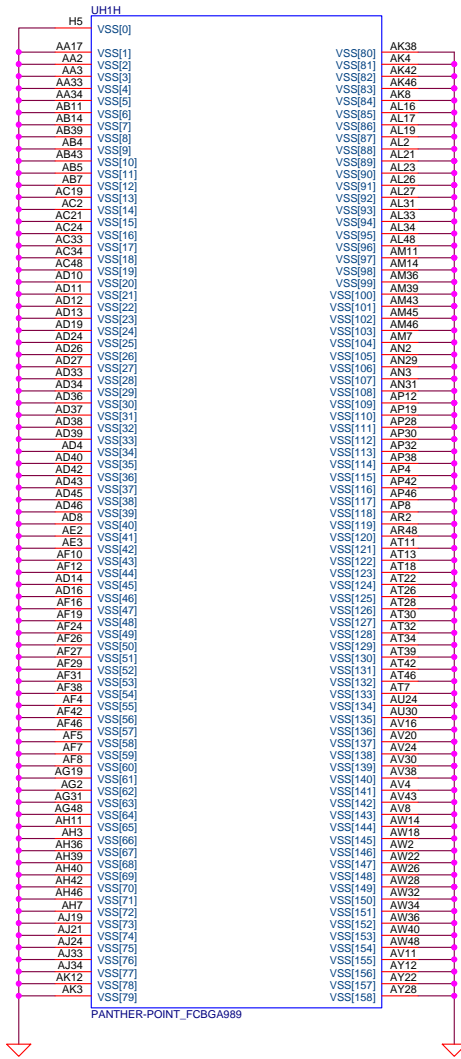
Voltage Rail	Voltage (V)	50 Inmax Current Integrated Graphics? (A)
VccI <sub>D</sub> <sup>2</sup>	1.05	3.799
VccASW	1.05	0.803
VccSPI	3.3	0.01
VccDSW3_3	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	N/A
VccSus3_3 (Internal Suspend VR mode using INTVRMEN)	3.3	0.085
VccSus3_3 (External Suspend VR mode using INTVRMEN)	3.3	0.065
VccSusHDA	3.3	0.01
VccVRM	1.5	0.147
VccClkDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.050
VccALVDS	3.3	0.001
VccTX_LVDS <sup>1</sup>	1.8	0.040
DepSus (External Suspend VR mode using INTVRMEN) <sup>4</sup>	1.05	0.12

VCC3\_3 = 266mA detail waiting for newest spec  
 VCCDMI = 42mA detail waiting for newest spec

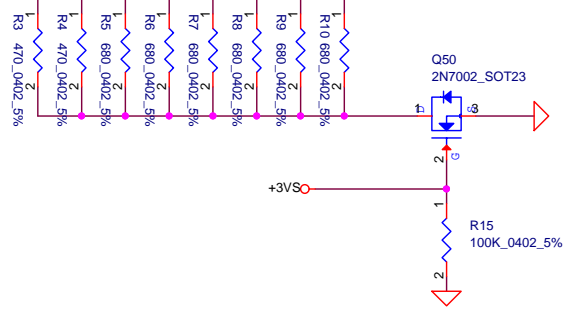
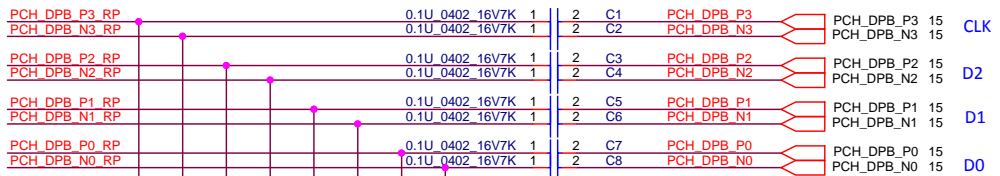


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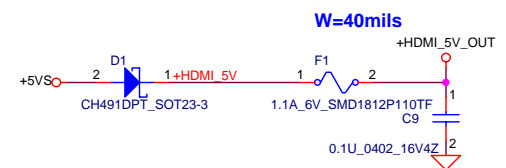
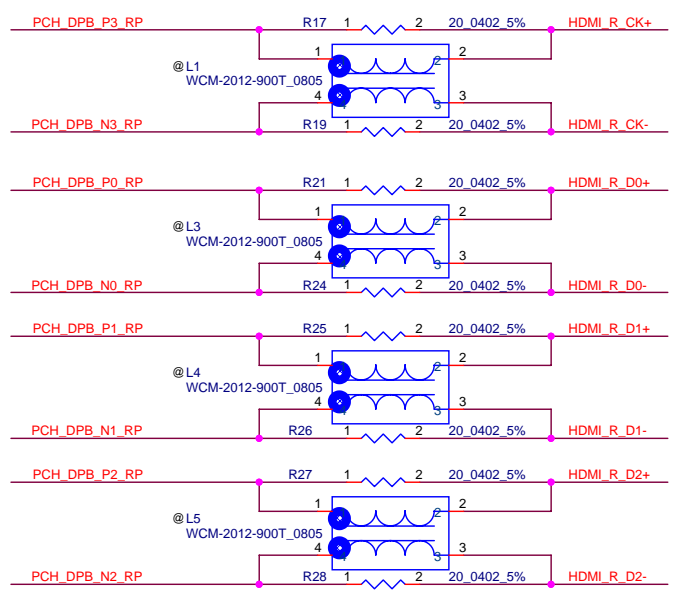
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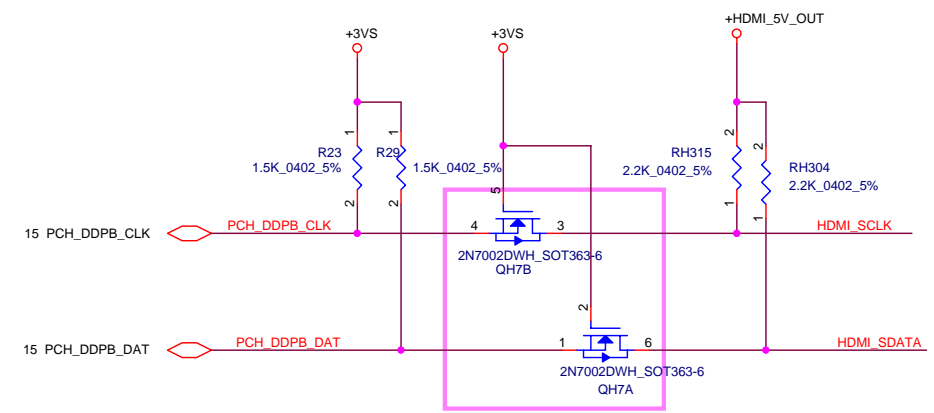
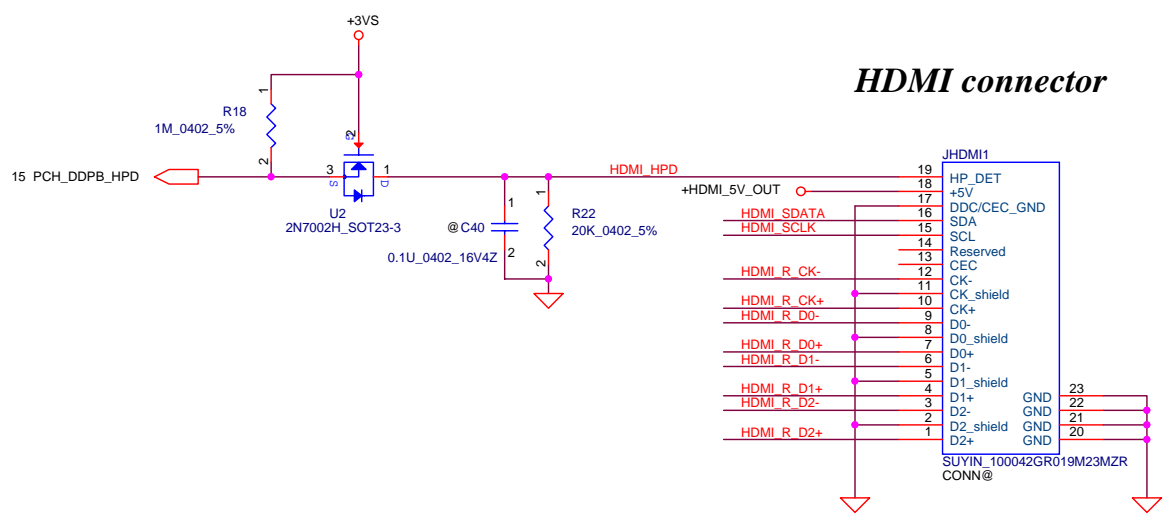
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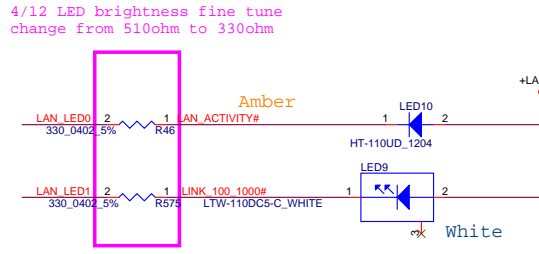
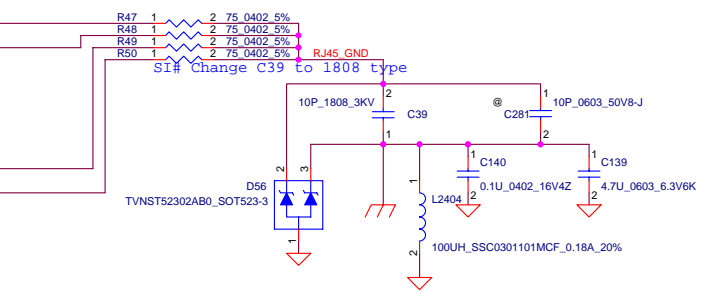
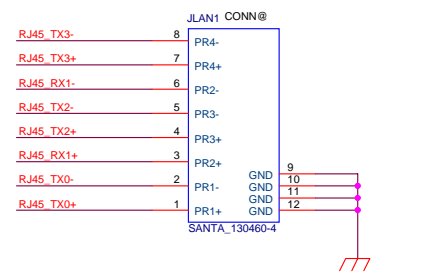
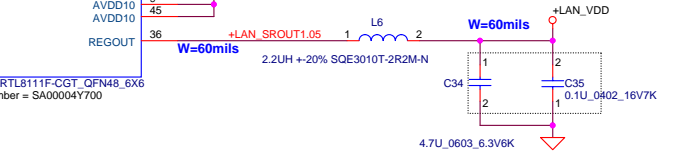
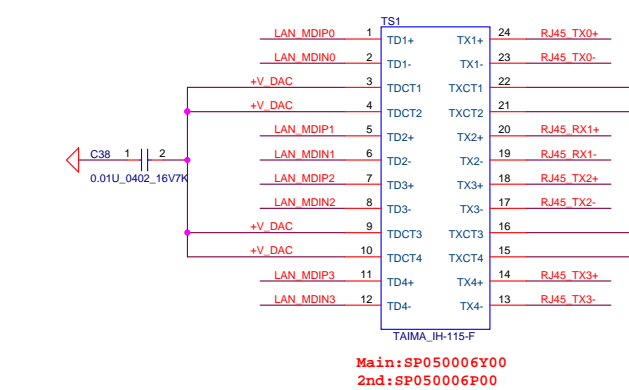
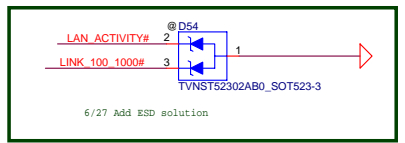
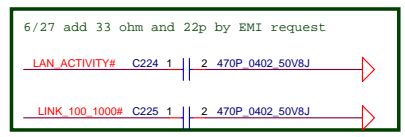
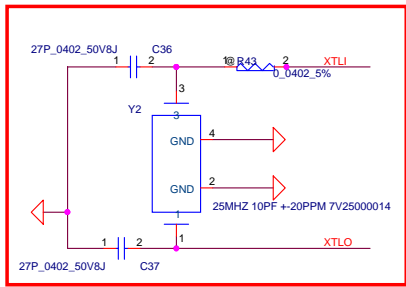
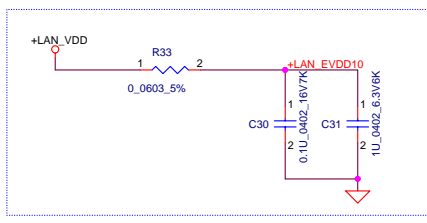
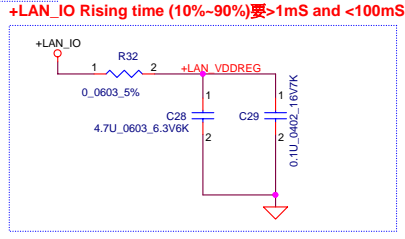
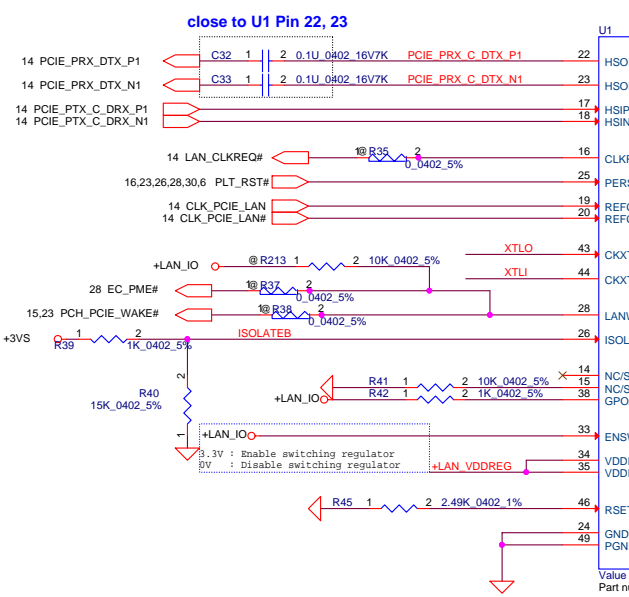
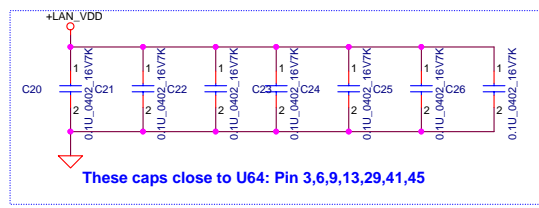
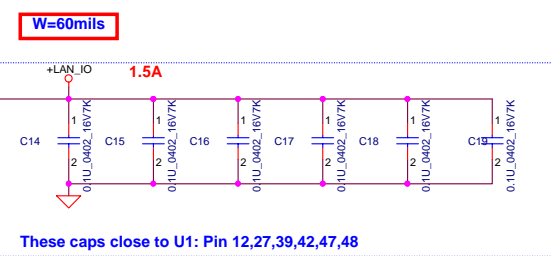
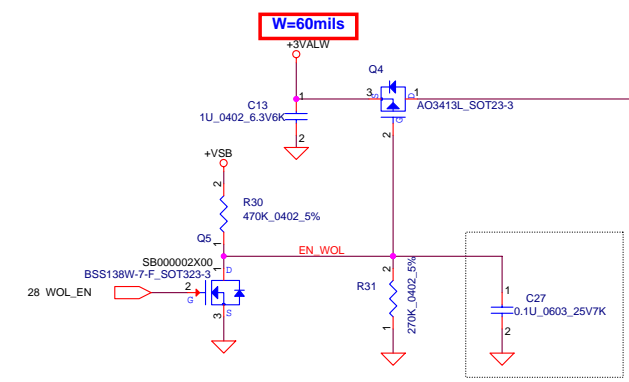
SM070001310 400ma 90ohm@100mhz DCR 0.3



### HDMI connector



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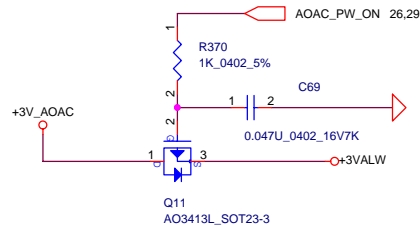
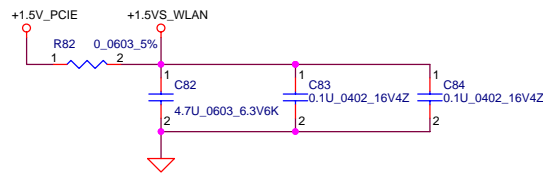
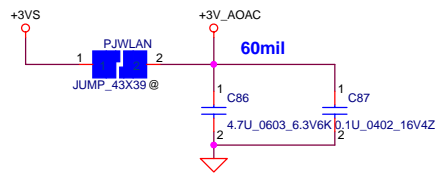
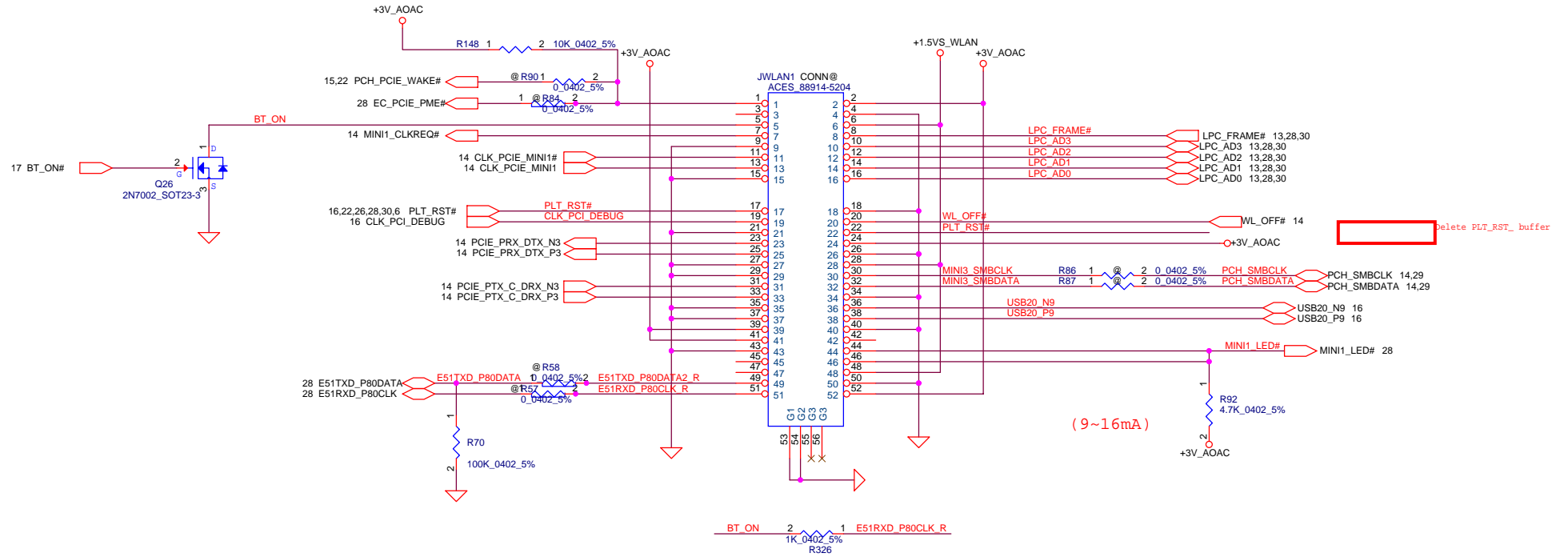


Main: SP050006Y00  
2nd: SP050006P00

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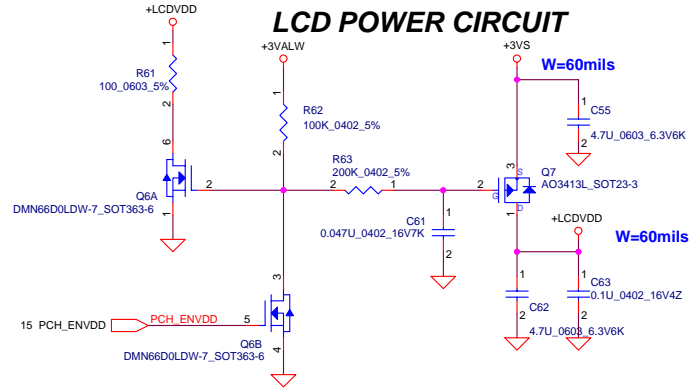
10/13 JMINI2 change symbol to DC040008B00

**Temp Footprint: ACES\_50711\_0520W-001\_52P-T**

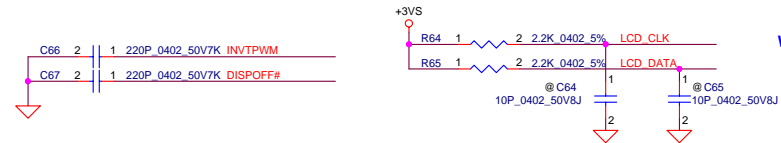
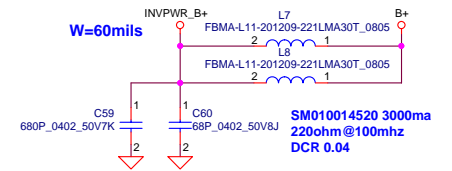
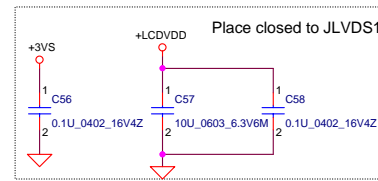
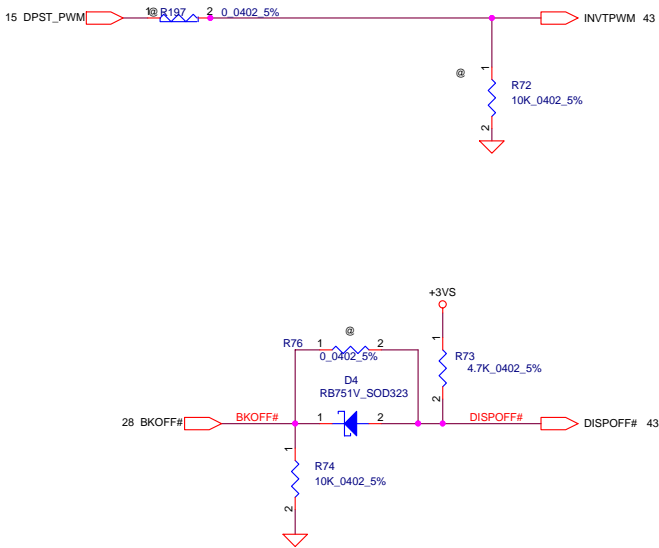


Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

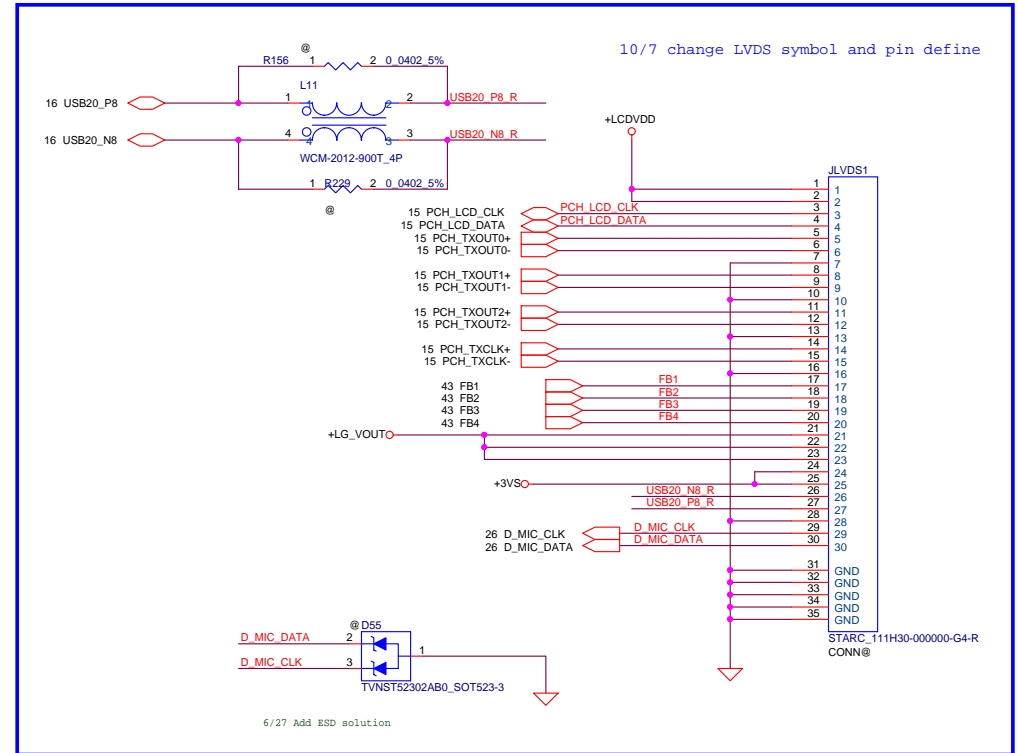




**1/5 Delete INVT\_PWM**



### LCD/LED PANEL Conn.



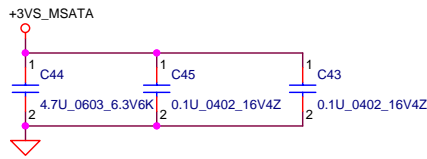
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Compal Electronics, Inc.

**SCHEMATICS, MB A8554**

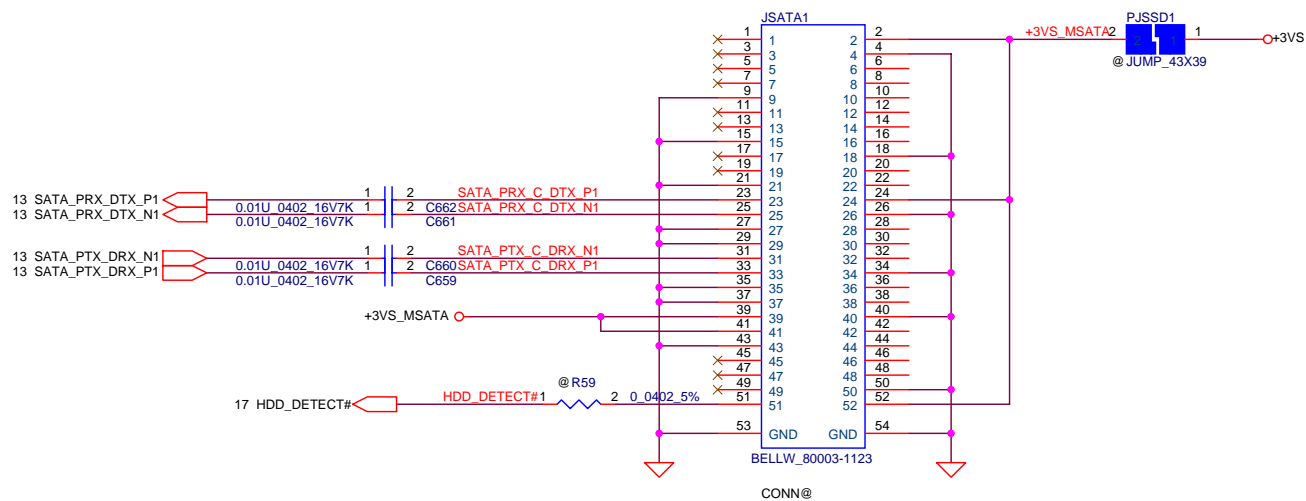
**4019HW**



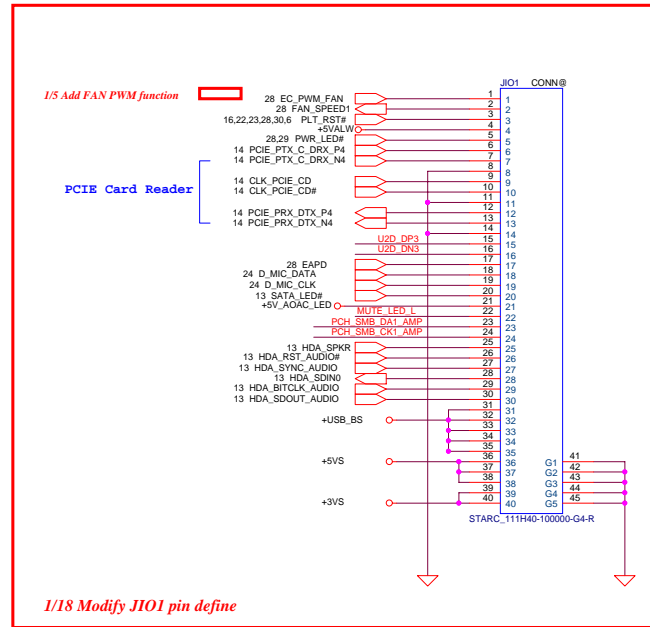
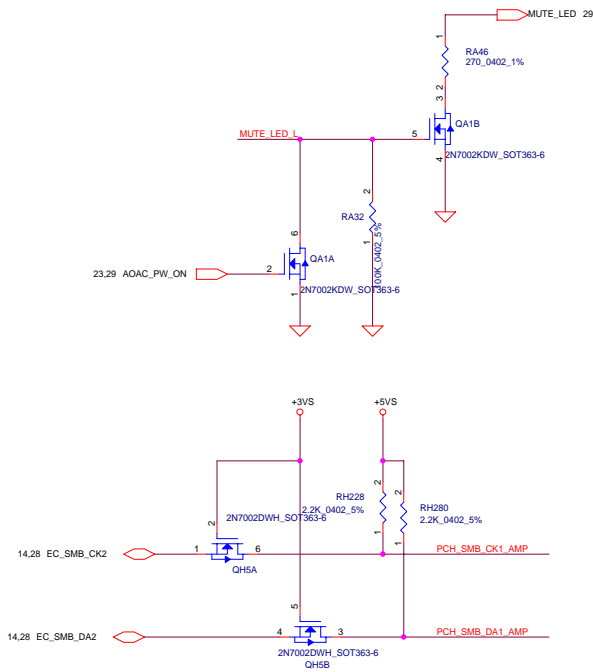


**mSATA Conn.**

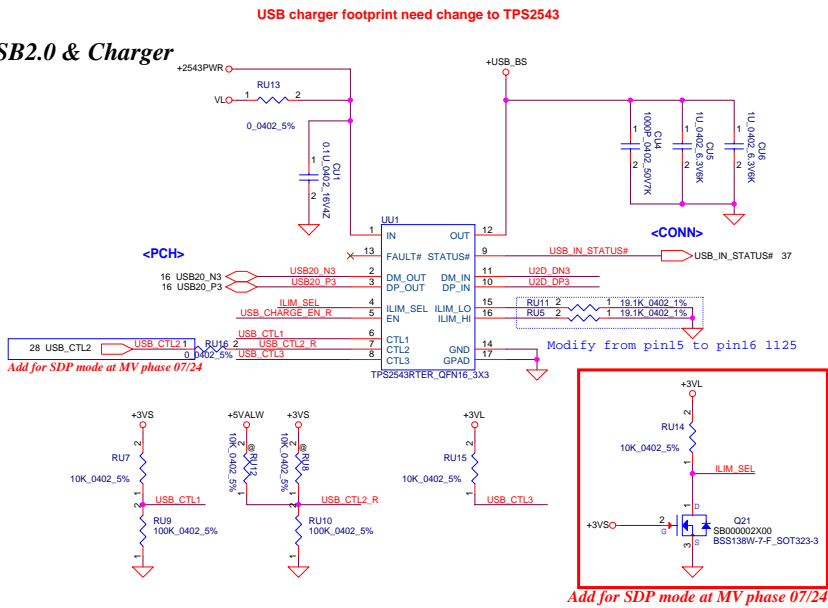
10/27 JMINI2 change symbol to SP070000A00



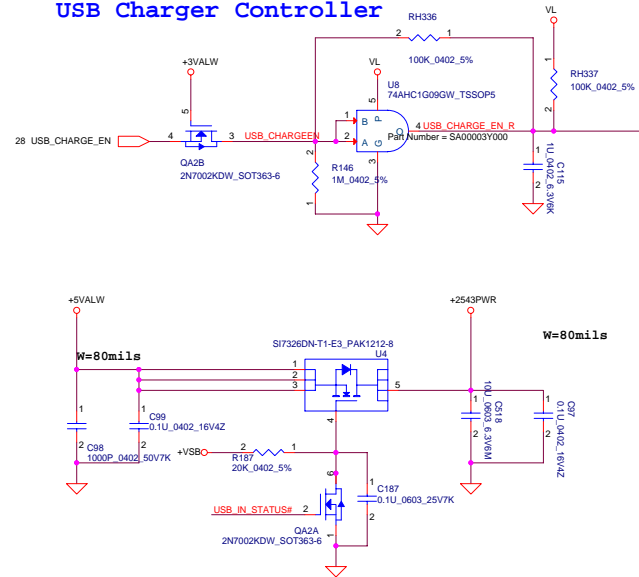
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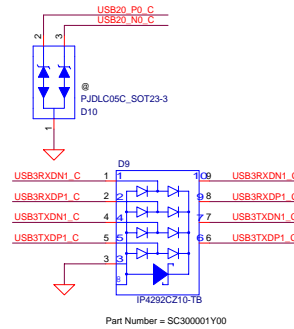
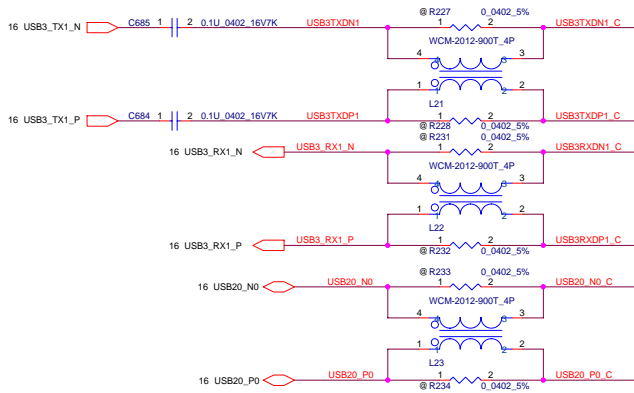
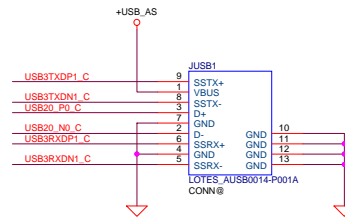
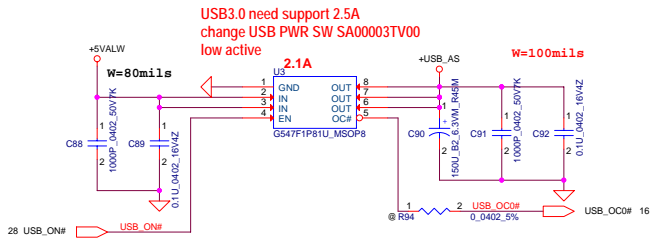
### USB2.0 & Charger



### USB Charger Controller



State	S0				S3				S4, S5			
Mode	SDP				DCP(Mouse/KB wake)				DCP(Power wake)			
Control Pin	CTL1	CTL2	CTL3	ILIM_SEL	CTL1	CTL2	CTL3	ILIM_SEL	CTL1	CTL2	CTL3	ILIM_SEL
	1	1	1	0	0	1	1	1	0	0	1	1

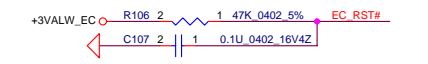
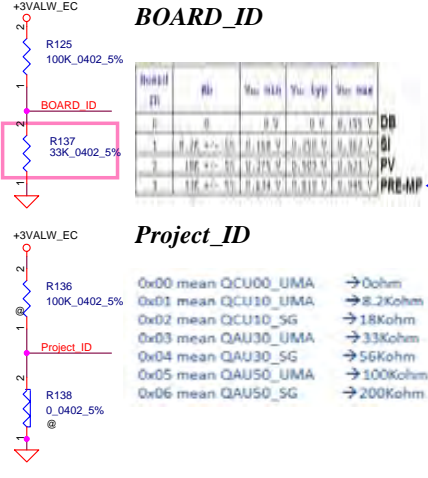


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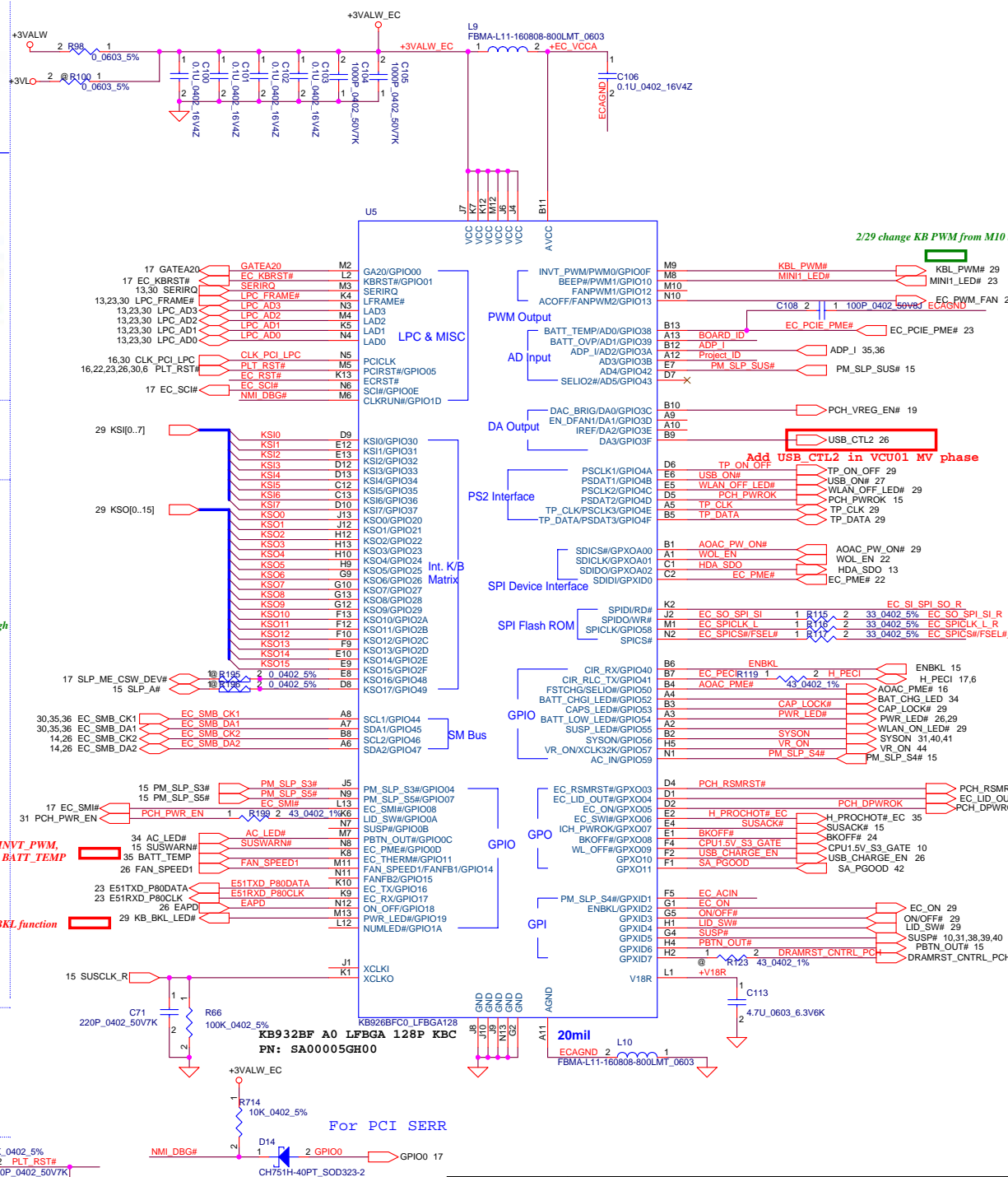
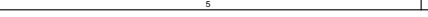
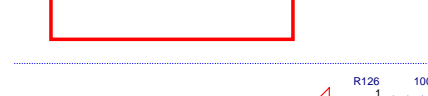
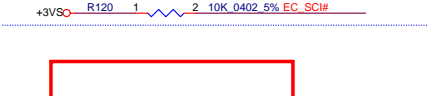
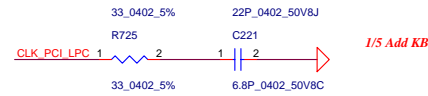
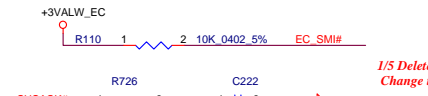
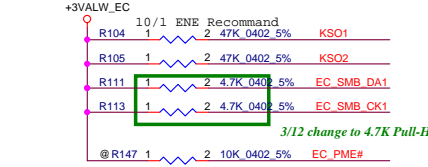
# BOARD\_ID

# Project\_ID

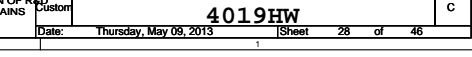
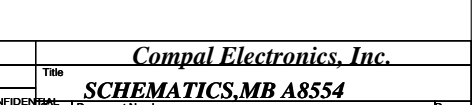
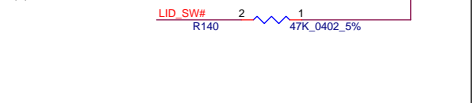
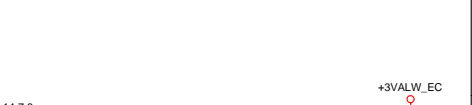
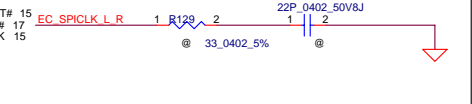
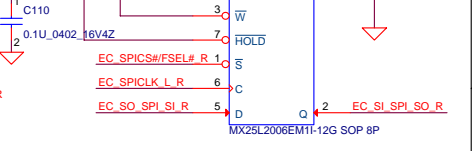
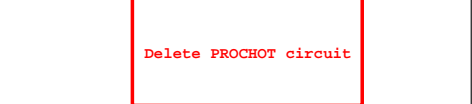
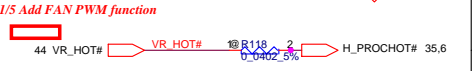
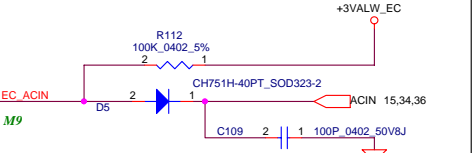
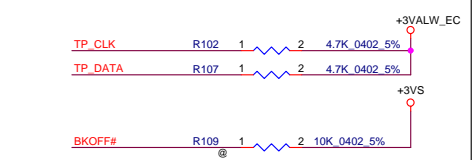
0x00	mean	QCU00_UMA	→	0ohm
0x01	mean	QCU10_UMA	→	2.2Kohm
0x02	mean	QCU10_SG	→	18Kohm
0x03	mean	QAU30_UMA	→	33Kohm
0x04	mean	QAU30_SG	→	56Kohm
0x05	mean	QAU50_UMA	→	100Kohm
0x06	mean	QAU50_SG	→	200Kohm



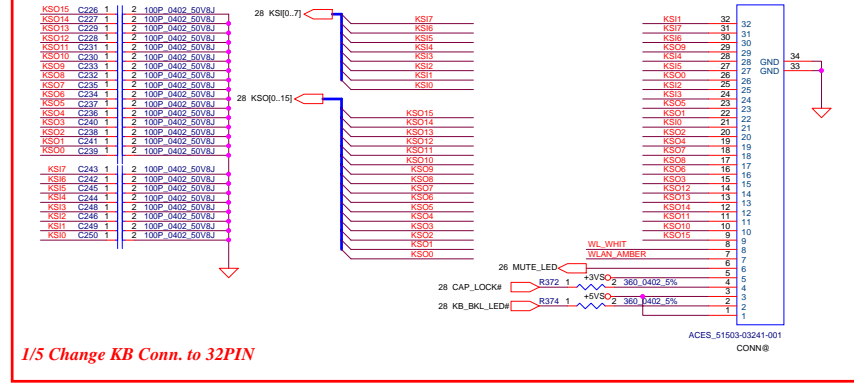
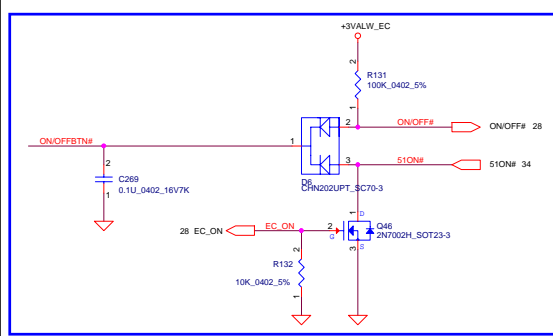
PV# 9/13 change power rail form +3VALW->+3VALW\_EC



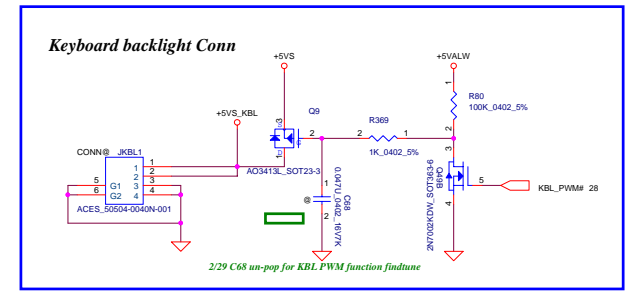
For PCI SERR  
NMI\_DBG# → GPIO0 17



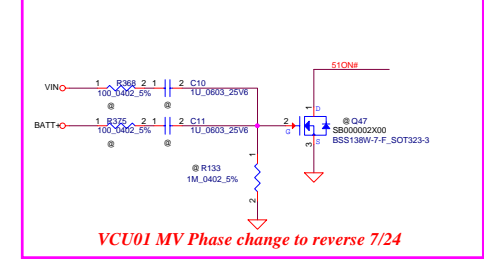
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1/5 Change KB Conn. to 32PIN

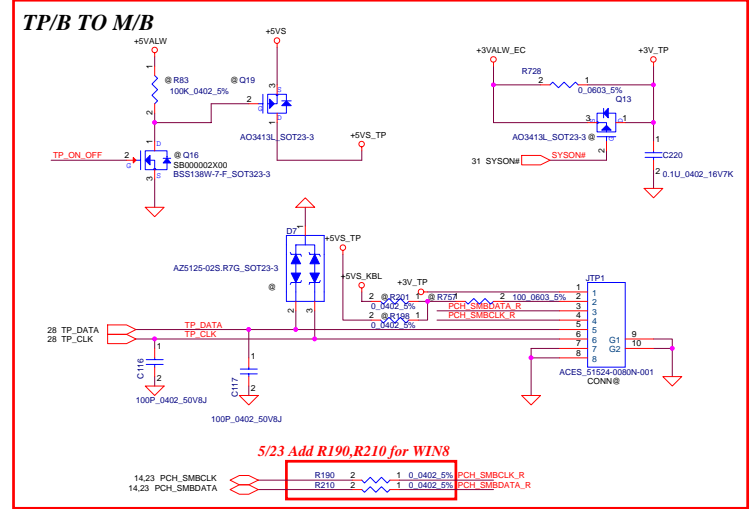
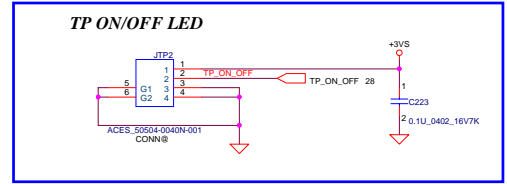
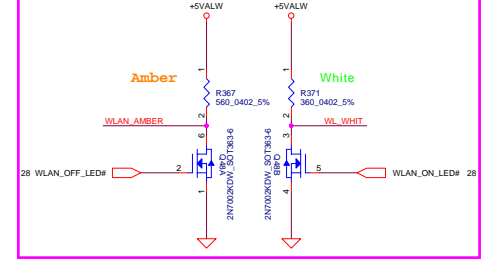


4/13 Add AC/battery plug-in detect circuit

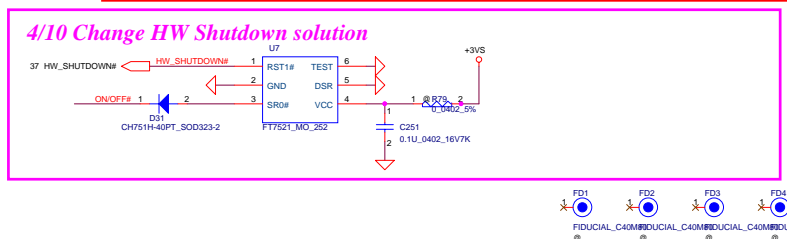
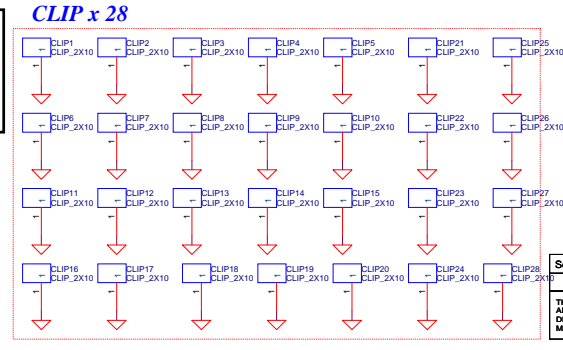
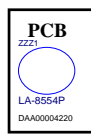
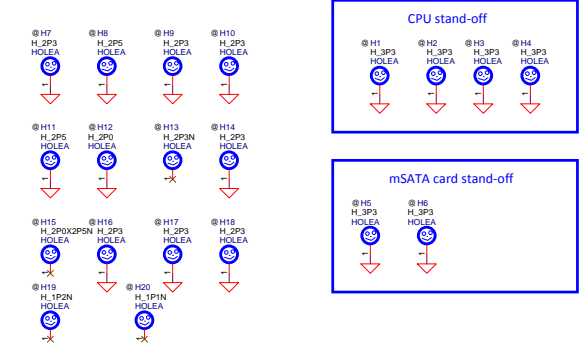
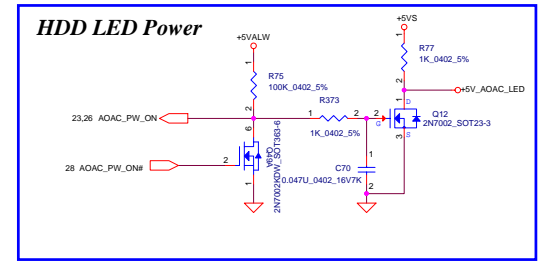
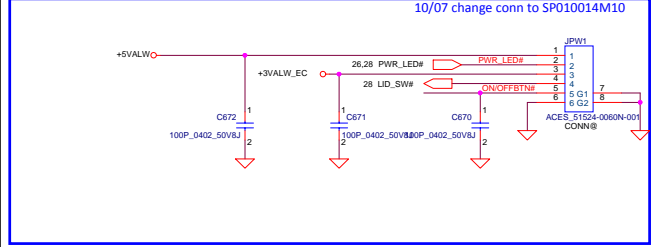


VCU01 MV Phase change to reverse 7/24

4/12 change power rail to +5VALW



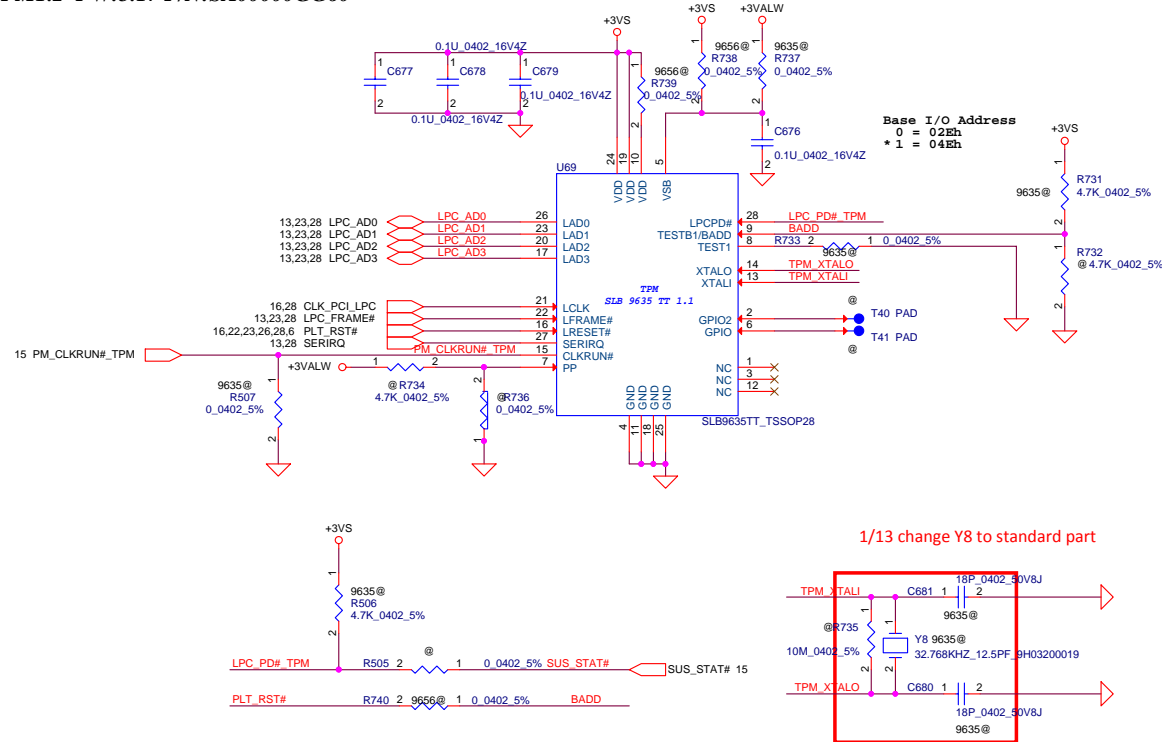
Power On/Off board Conn.



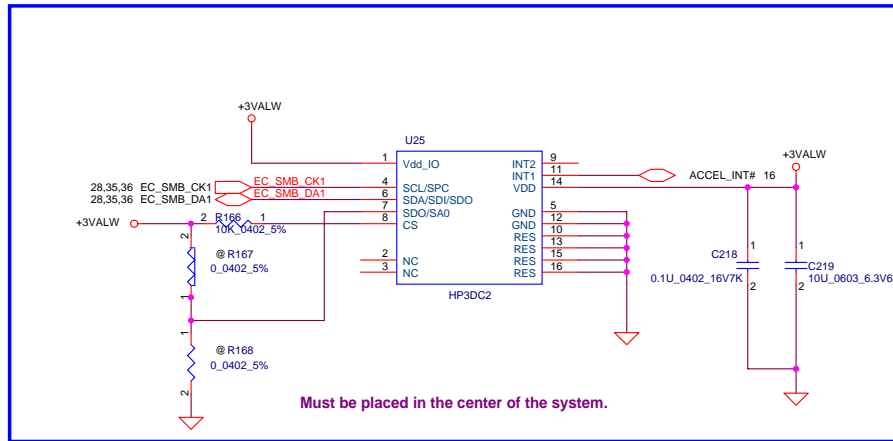
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4/9 Modify Circuit, 9635 & 9656 co-lay for WIN8 SKU

TPMI.2 FW:3.19 P/N:SA00000GG70  
 TPMI.2 FW:3.17 P/N:SA00000GG60

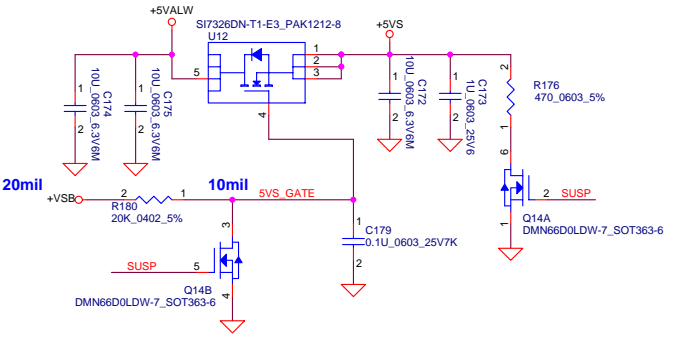


ACCELEROMETER

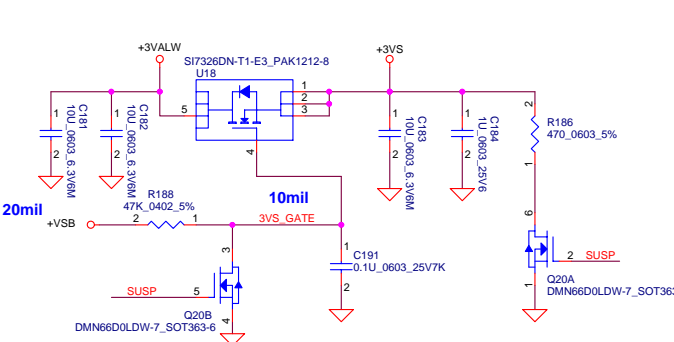


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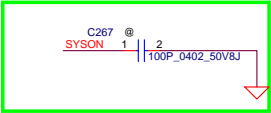
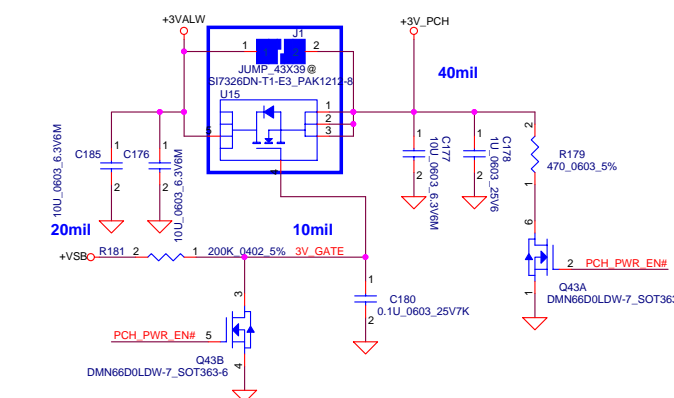
**+5VALW TO +5VS**



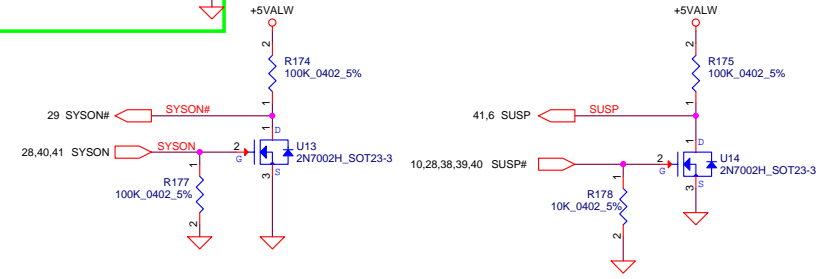
**+3VALW TO +3VS**



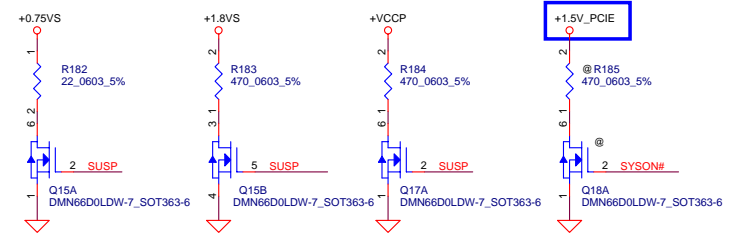
**+3VALW TO +3VALW(PCH AUX Power)**  
Short J1 for PCH VCCSUS3.3



Reserve C267 100pF by ESD request



**10/06 change +1.5V to +1.5\_PCIE**



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QA Z60 Strap pin Table		@:un_install	
Netname	setting	BOM config	
CPU	CFG2	1	RC40 @ 1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed
	CFG4	1	RC41 @ 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port
	CFG[6:5]	0 1	RC49 RC48 @ 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
	CFG7	1	RC50 @ 1: (Default) PEG Train immediately following xRESETB de assertion 0: PEG Wait for BIOS for training
PCH	PCH_INTVRMEN	H	RH124 RH126 @ H : Integrated VRM enable L : Integrated VRM disable
	HDA_SPKR	L	RH139 @ H:No Reboot L:Default
	HDA_SYNC	H	RH149 This signal has a weak internal pull-down On Die PLL VR is supplied by H:1.5V when sampled high L:1.8V when sampled low Needs to be pulled High for Huron River platform
	HDA_SDOUT	L	RH140 @ ME debug mode , this signal has a weak internal PD L=>security measures defined in the Flash Descriptor will be in effect (default) H=>Flash Descriptor Security will be overridden
	DSWODVREN	H	RH213 RH215 @ On Die DSW VR Enable H : Enable L : Disable
	SLP_ME_CSW_DEV#	H	RH267 RH241 @ On-Die PLL Voltage Regulator This signal has a weak internal pull up H : On-Die voltage regulator enable L : On-Die PLL Voltage Regulator disable
	PCH_GPIO37	L	RH245 @ RH246 FDI TERMINATION VOLTAGE OVERRIDE L: Tx, Rx terminated to same voltage(DC Coupling Mode)
GPIO27	H	RH250 @ PCH_GPIO27 (Have internal Pull-High) H: VCCVRM VR Enable L: VCCVRM VR Disable	

2

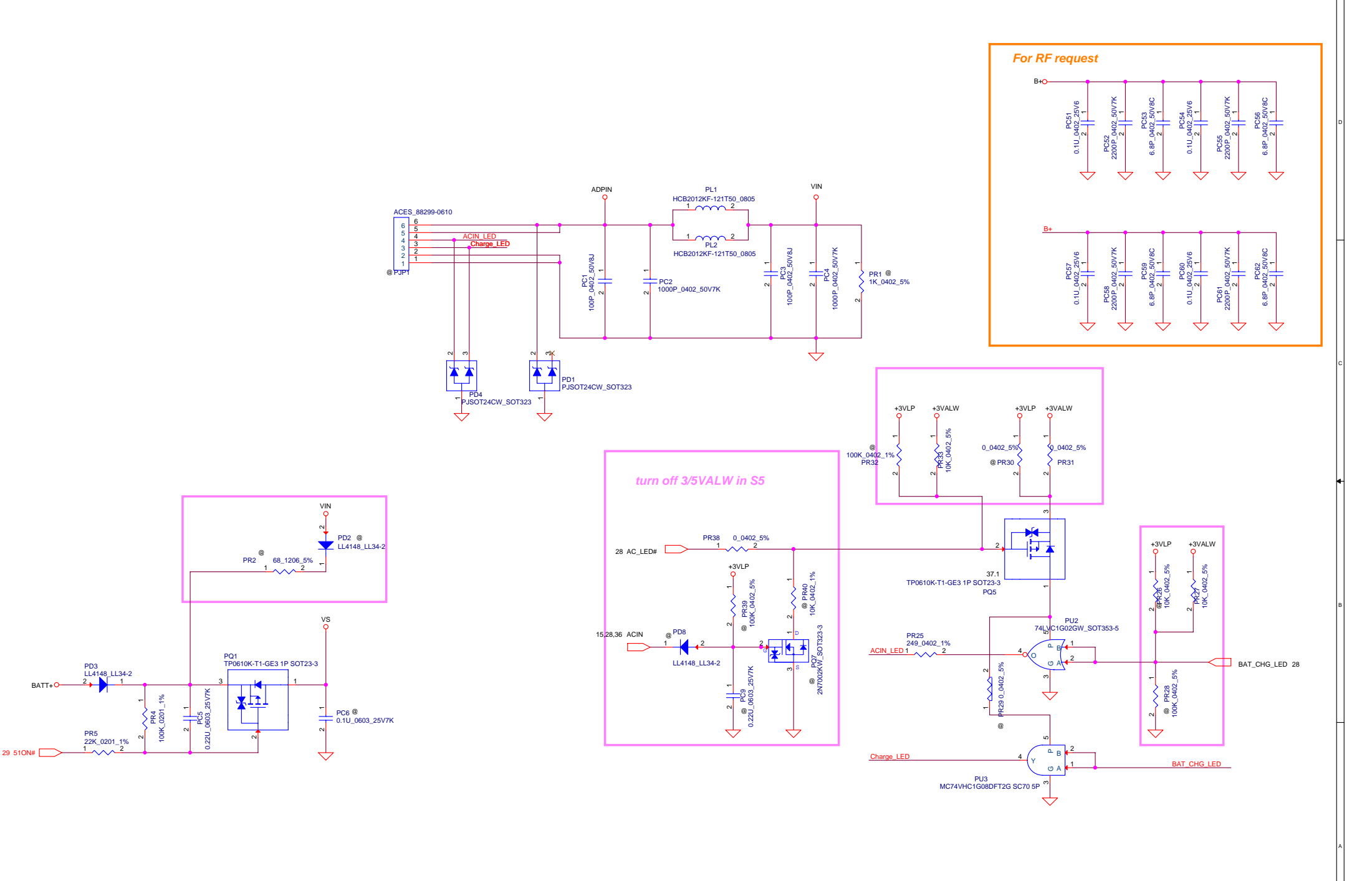
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	SCHEMATICS, MB A8554	
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	xx	xxx	2011/02/XX	XXXX XXXX	XXXX		Rev01

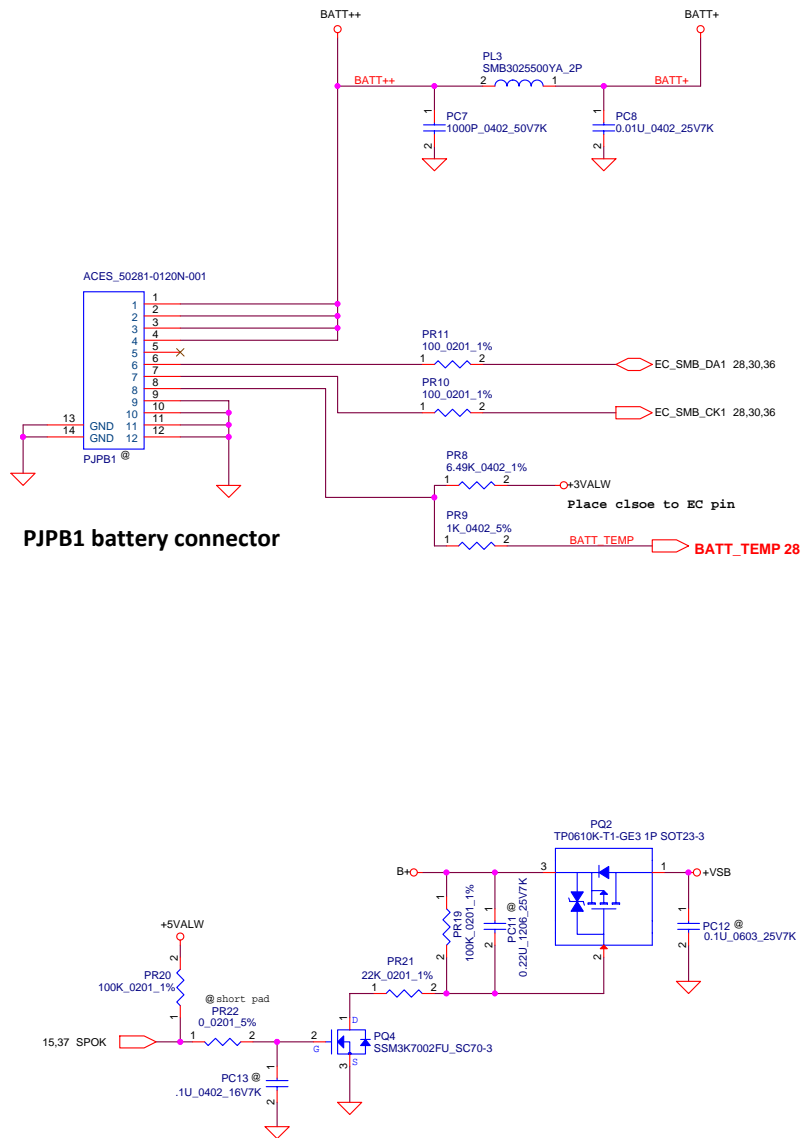
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**PJPB1 battery connector**

For KB930 --> Keep PU1 circuit  
(Vth = 0.825V)

For KB9012 --> Remove PU1 circuit, but keep PR25  
PH1, PR15, PQ3, PR17, PR18, PR16  
VCIN0\_PH-->NTC\_V  
VCIN1\_PH-->Turbo\_V

PH1 under CPU bottom side :  
CPU thermal protection at 97+/-3 degree C  
Recovery at 55 +/-3 degree C

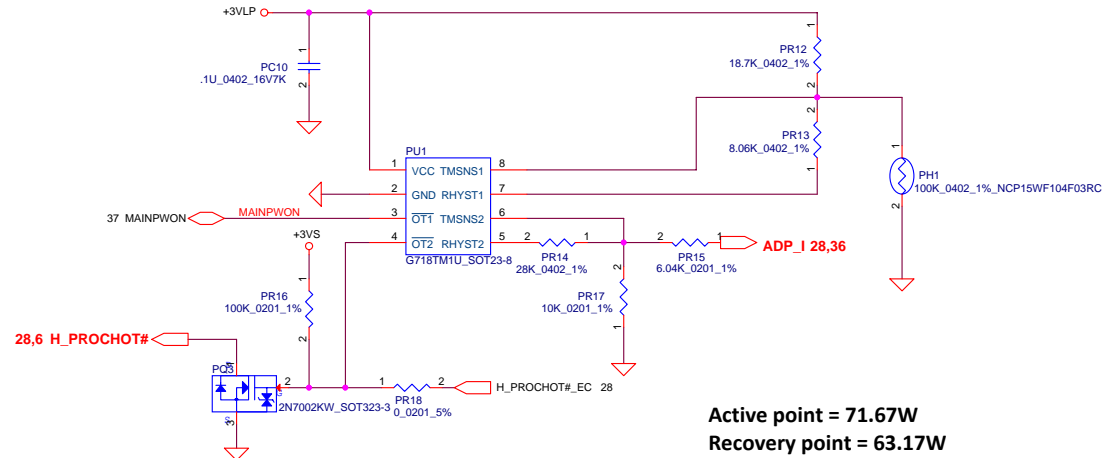
$$R_{set} = 3 * R_{tmh}$$

$$R_{hyst} = (R_{set} * R_{tml}) / (3 * R_{tml} - R_{set})$$

$$R_{tmh} \text{ at } 97C = 6.24K, R_{tml} \text{ at } 55C = 27.16K$$

$$R_{set} = 3 * 6.24K = 18.72K \rightarrow 18.7K$$

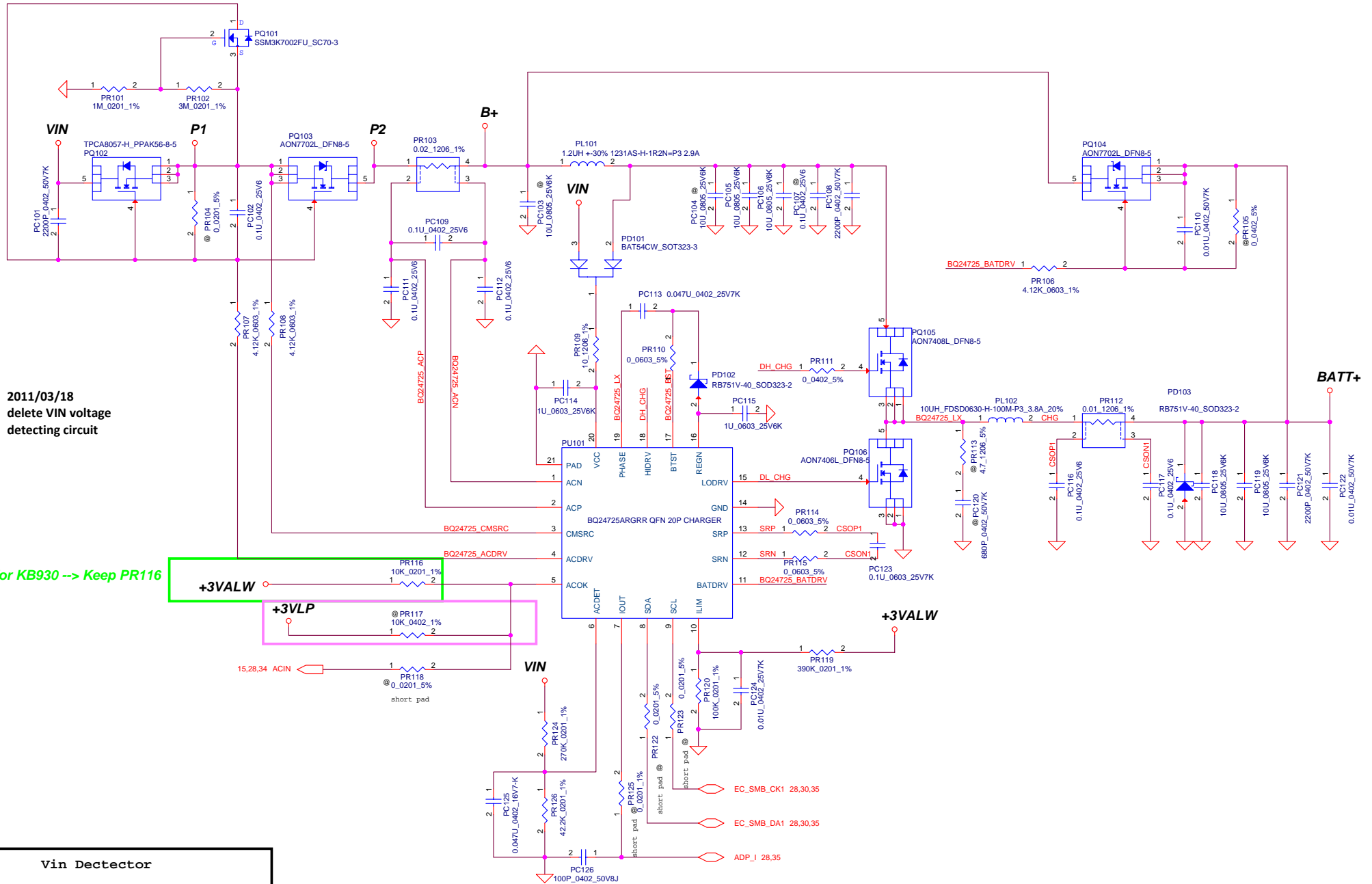
$$R_{hyst} = (18.7K * 27.16K) / (3 * 27.16K - 18.7K) = 8.09k \rightarrow 8.06k$$



Active point = 71.67W  
Recovery point = 63.17W

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for reverse input protection

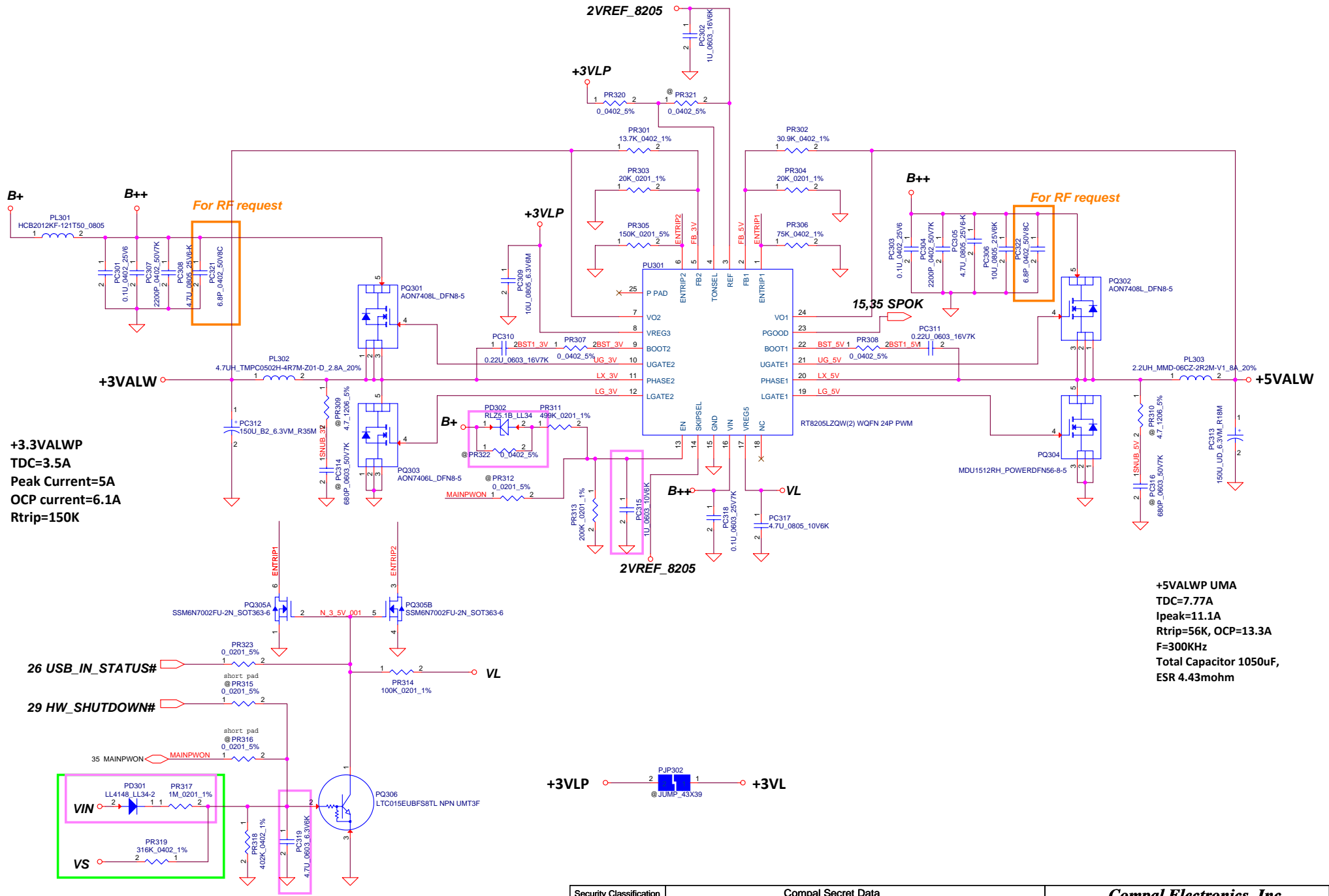


2011/03/18  
delete VIN voltage  
detecting circuit

For KB930 --> Keep PR116

Vin Detector			
	Min.	Typ	Max.
L-->H		17.75V	
H-->L		17.38V	
ILIM and external DPM 3.37A			

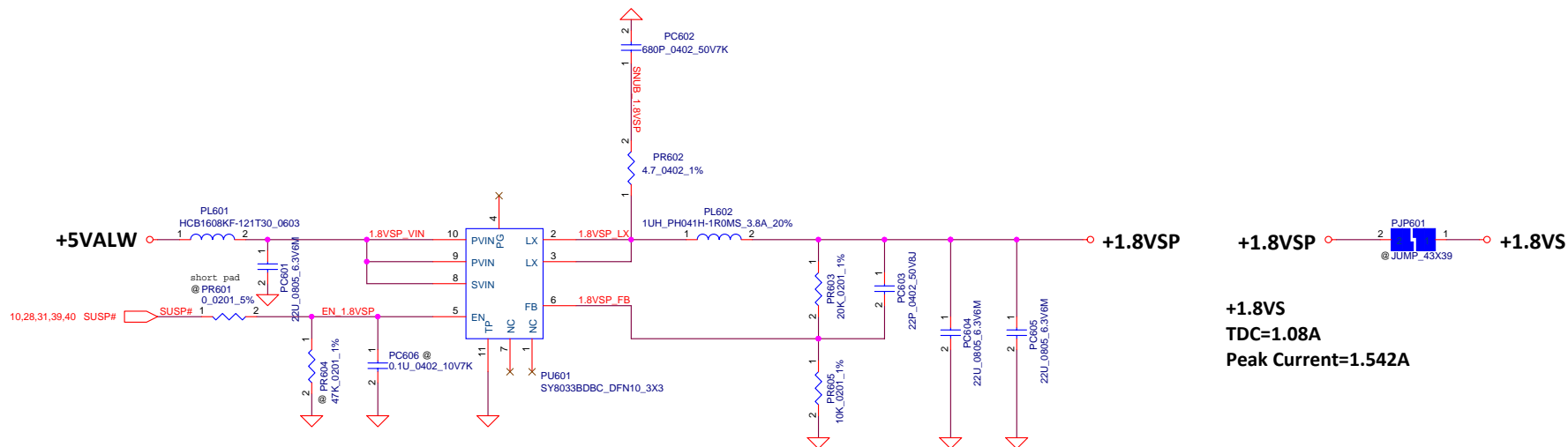
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**+3.3VALWP**  
**TDC=3.5A**  
**Peak Current=5A**  
**OCP current=6.1A**  
**Rtrip=150K**

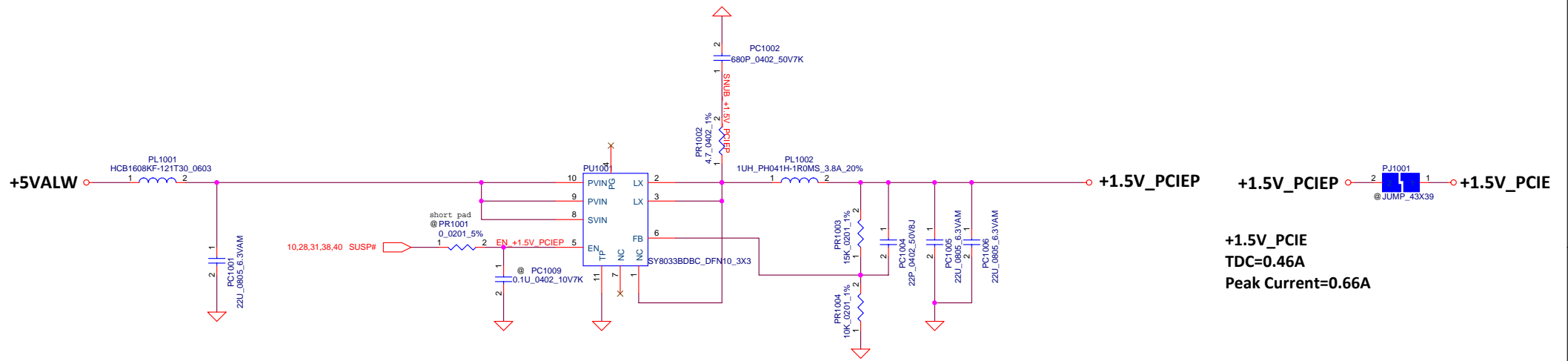
**+5VALWP UMA**  
**TDC=7.77A**  
**Ipeak=11.1A**  
**Rtrip=56K, OCP=13.3A**  
**F=300KHz**  
**Total Capacitor 1050uF,**  
**ESR 4.43mohm**

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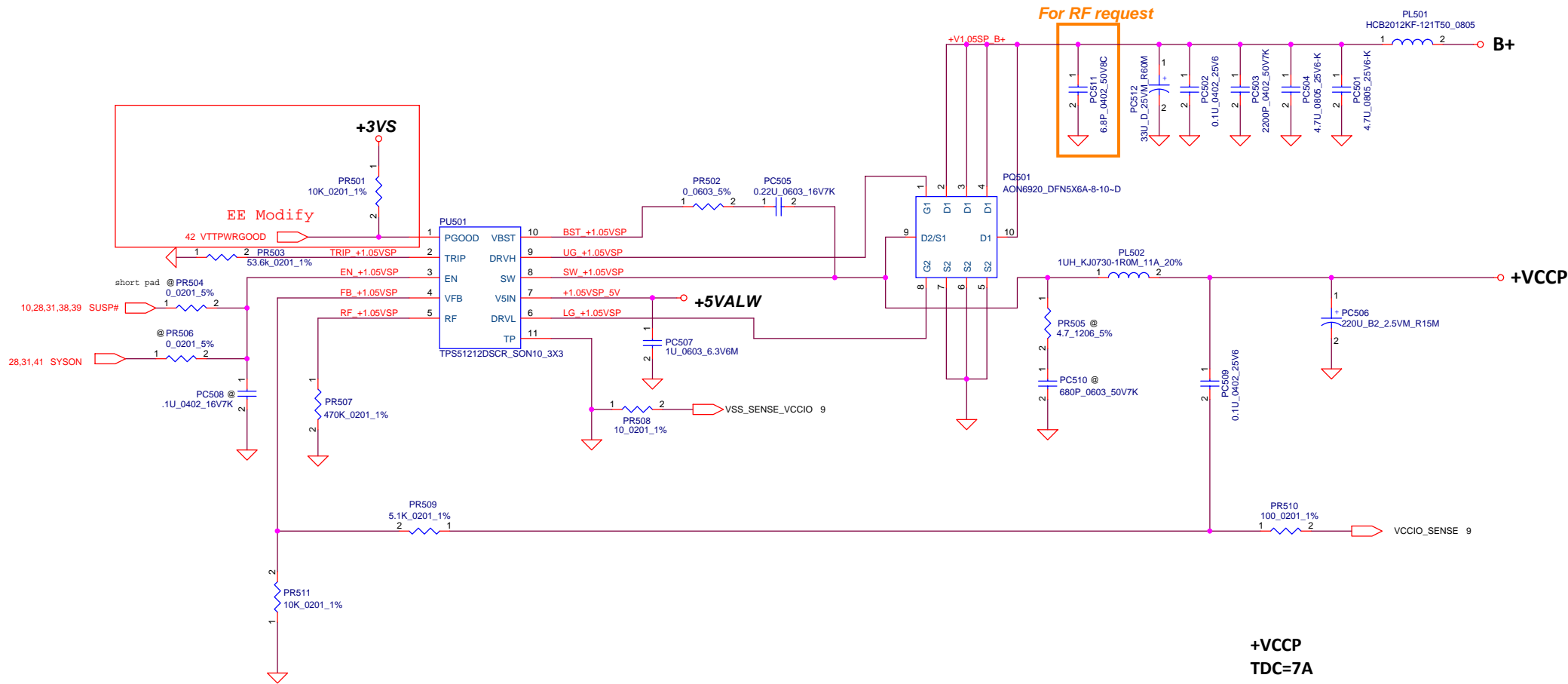


**+1.8VSP**  
**+1.8VS**  
**TDC=1.08A**  
**Peak Current=1.542A**

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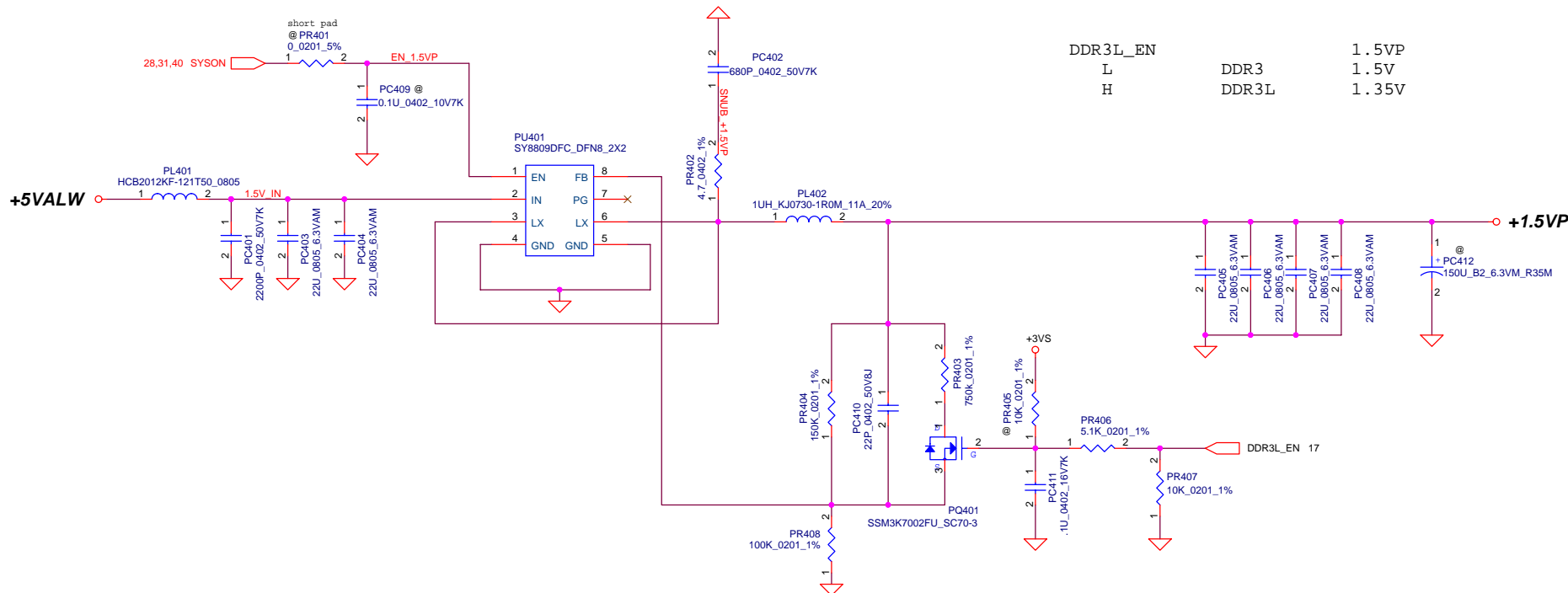
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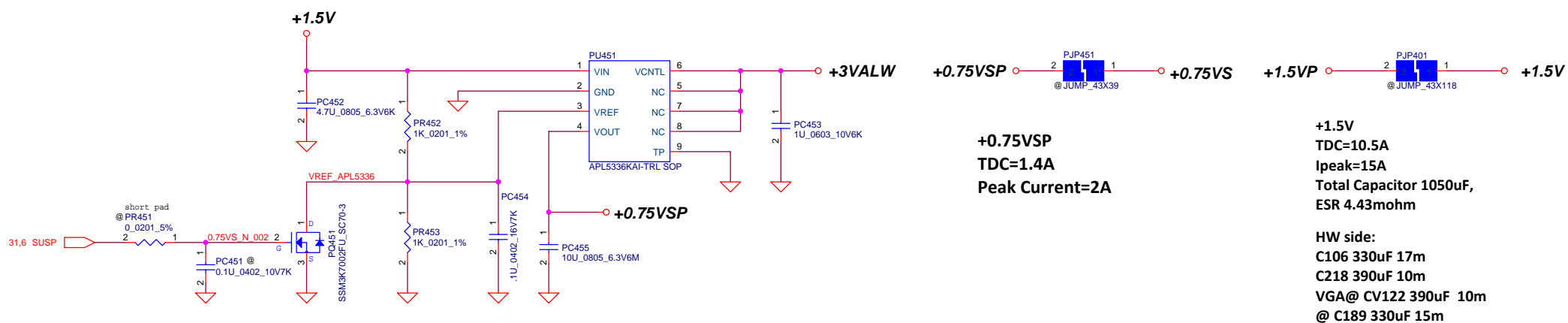
**+VCCP**  
**TDC=7A**  
**Peak Current=9A**  
**OCp current=11.9A**  
**Rtrip =53.6k**

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DDR3L\_EN  
L      DDR3      1.5VP  
H      DDR3L    1.35V



+0.75VSP @ JUMP\_43X39      +0.75VS  
+1.5VP @ JUMP\_43X118      +1.5V

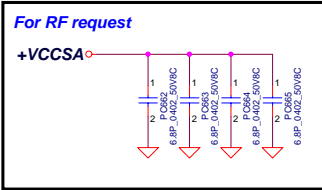
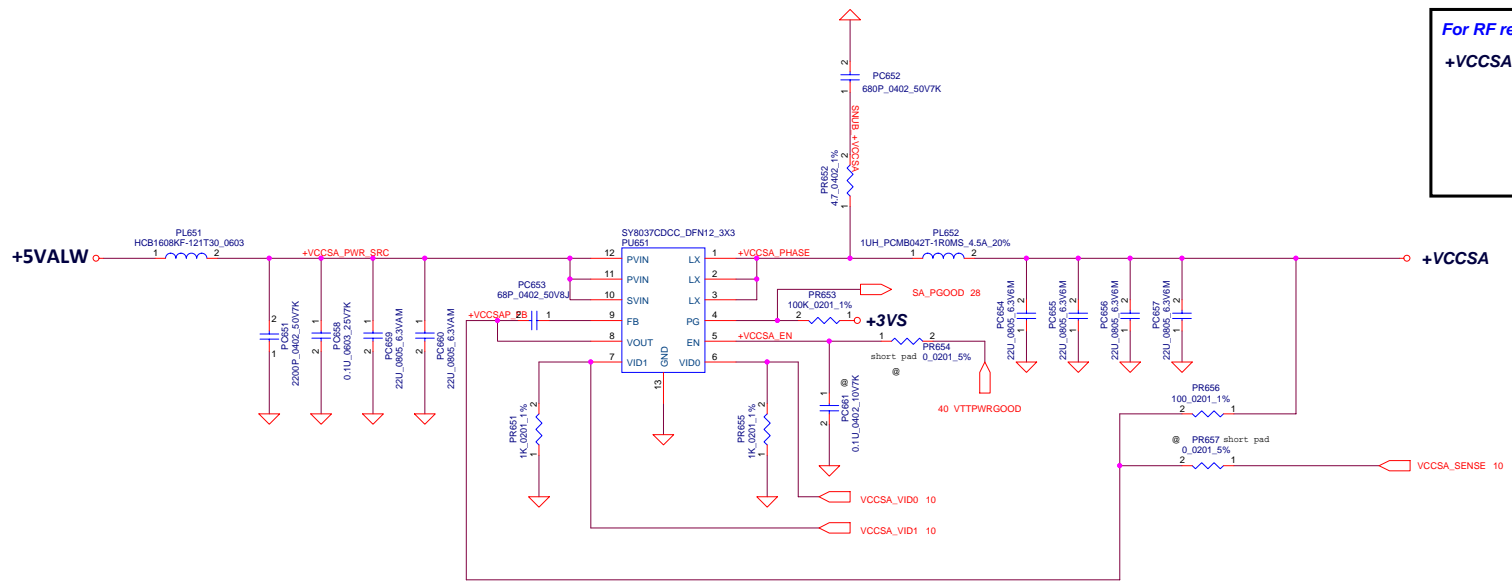
**+0.75VSP**  
**TDC=1.4A**  
**Peak Current=2A**

**+1.5V**  
**TDC=10.5A**  
**Ipeak=15A**  
**Total Capacitor 1050uF,**  
**ESR 4.43mohm**

**HW side:**  
**C106 330uF 17m**  
**C218 390uF 10m**  
**VGA@ CV122 390uF 10m**  
**@ C189 330uF 15m**

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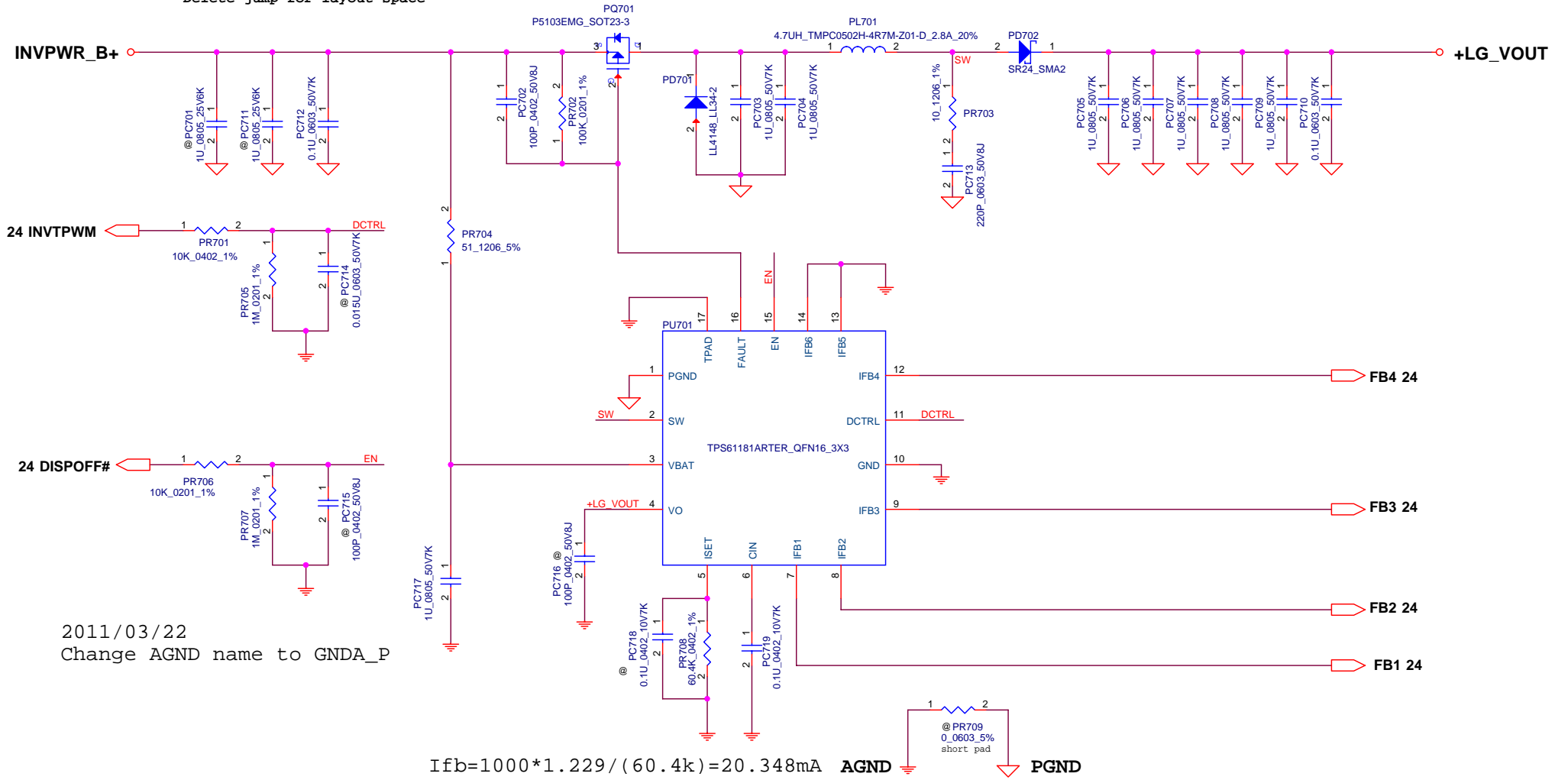
The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.



+VCCSA  
TDC=4.2A  
Ipeak=6A

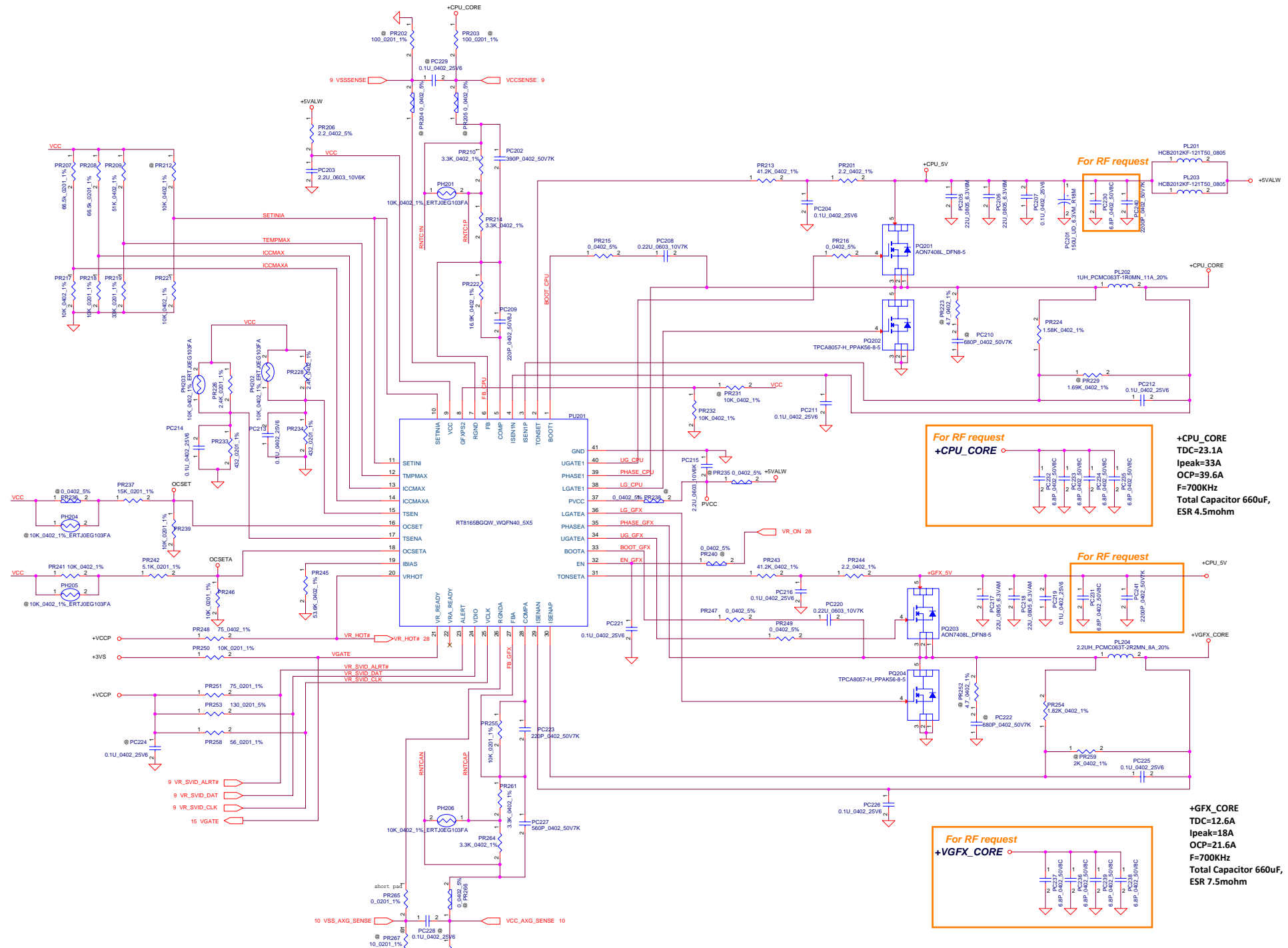
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2011/03/23  
Delete jump for layout space



2011/03/22  
Change AGND name to GNDA\_P

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For RF request

For RF request

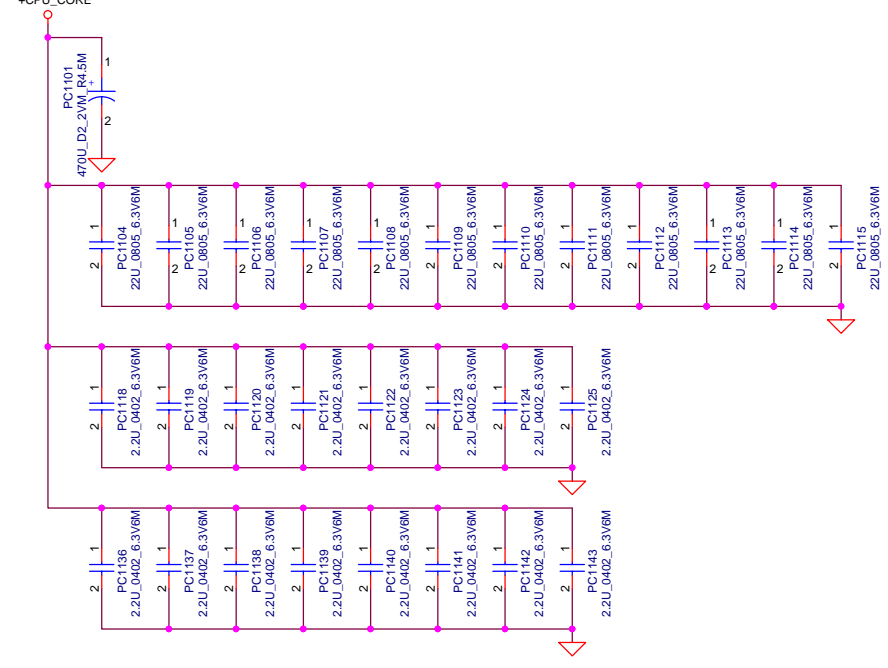
For RF request

**+CPU\_CORE**  
 TDC=23.1A  
 Ipeak=33A  
 OCP=39.6A  
 F=700KHz  
 Total Capacitor 660uF,  
 ESR 4.5mohm

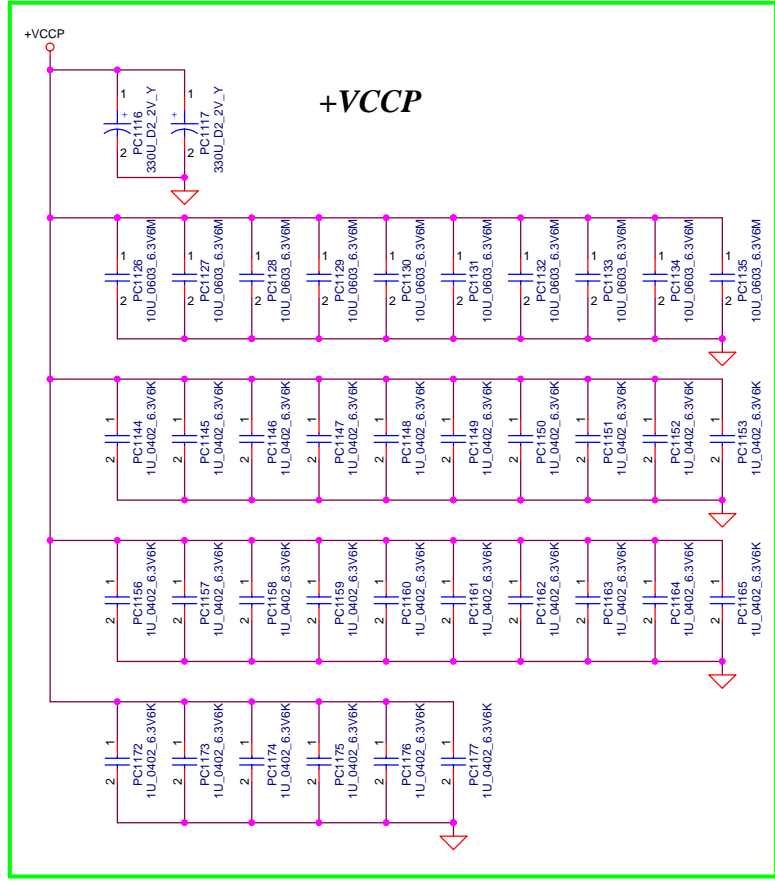
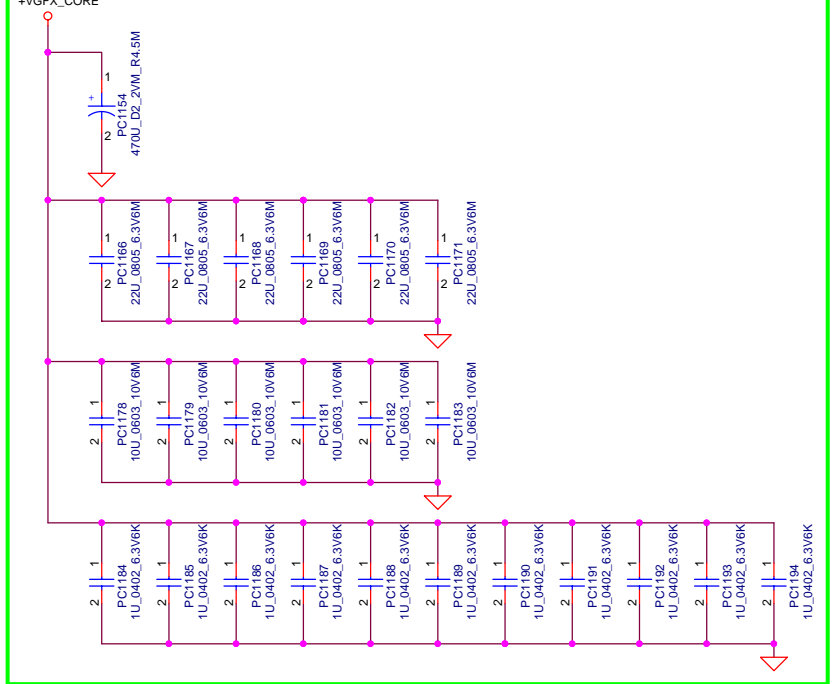
**+VGFX\_CORE**  
 TDC=12.6A  
 Ipeak=18A  
 OCP=21.6A  
 F=700KHz  
 Total Capacitor 660uF,  
 ESR 7.5mohm

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### +CPU\_CORE



### +VGFX\_CORE



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Item	FIXED ISSUE	Reason for change	Rev	PG#	Modify list	B.Ver#	Phase
1	some projects cannot meet S5 power consumption in AC Mode	turn off S5 3/5VALW in AC Mode		36,34,37	1.add pd8 LL4148_LL34-2,pr39 100K_0402_5%,pr40 10K_0402_1%, pc9 0.22U_0603_25V7K, pg7 2N7002KW_SOT323-3, pr32 100K_0402_1%, pr30 0_0402_5%,pr28 100K_0402_5%, pd2 LL4148_LL34-2, pr2 68_1206_5%, pr117 10K_0402_1%, pr322 0_0402_5% 2.remove pr33 10K_0402_5%, pr31 0_0402_5%, pr27 10K_0402_5%, pr 116 10K_0201_1%, pd302 RLZ5.1B_LL34, pc315 1U_0603_10V6K, pc319 4.7U_0603_6.3V6K, pd301 LL4148_LL34-2, pr317 1M_0201_1%		PV
2	spec of panel output current has changed to 61.5mA(max)	change panel drive output current to 60mA		43	1.change pr708 from 52.3K_0402_1% to 60.4K_0402_1%		PV
3	HW think Hadid has passed ErP-lot6, so it's not necessary to turn off 3/5VALW in S5 status of AC mode.	turn on S5 3/5VALW in AC Mode		36,34,38	1.remove pd8 LL4148_LL34-2,pr39 100K_0402_5%,pr40 10K_0402_1%, pc9 0.22U_0603_25V7K, pg7 2N7002KW_SOT323-3, pr32 100K_0402_1%, pr30 0_0402_5%,pr28 100K_0402_5%, pd2 LL4148_LL34-2, pr2 68_1206_5%, pr117 10K_0402_1%, pr322 0_0402_5% 2.add pr33 10K_0402_5%, pr31 0_0402_5%, pr27 10K_0402_5%, pr 116 10K_0201_1%, pd302 RLZ5.1B_LL34, pc315 1U_0603_10V6K, pc319 4.7U_0603_6.3V6K, pd301 LL4148_LL34-2, pr317 1M_0201_1%		MV
4							
5							
6							
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15							

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