Compal Confidential

2014 S-series(400series) Rolo/Reeses/Raisinet

INTEL Sharkbay & Crescent bay ULT –U processor with DDR3L

Date : 2014/02/18

Version 0.5

Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

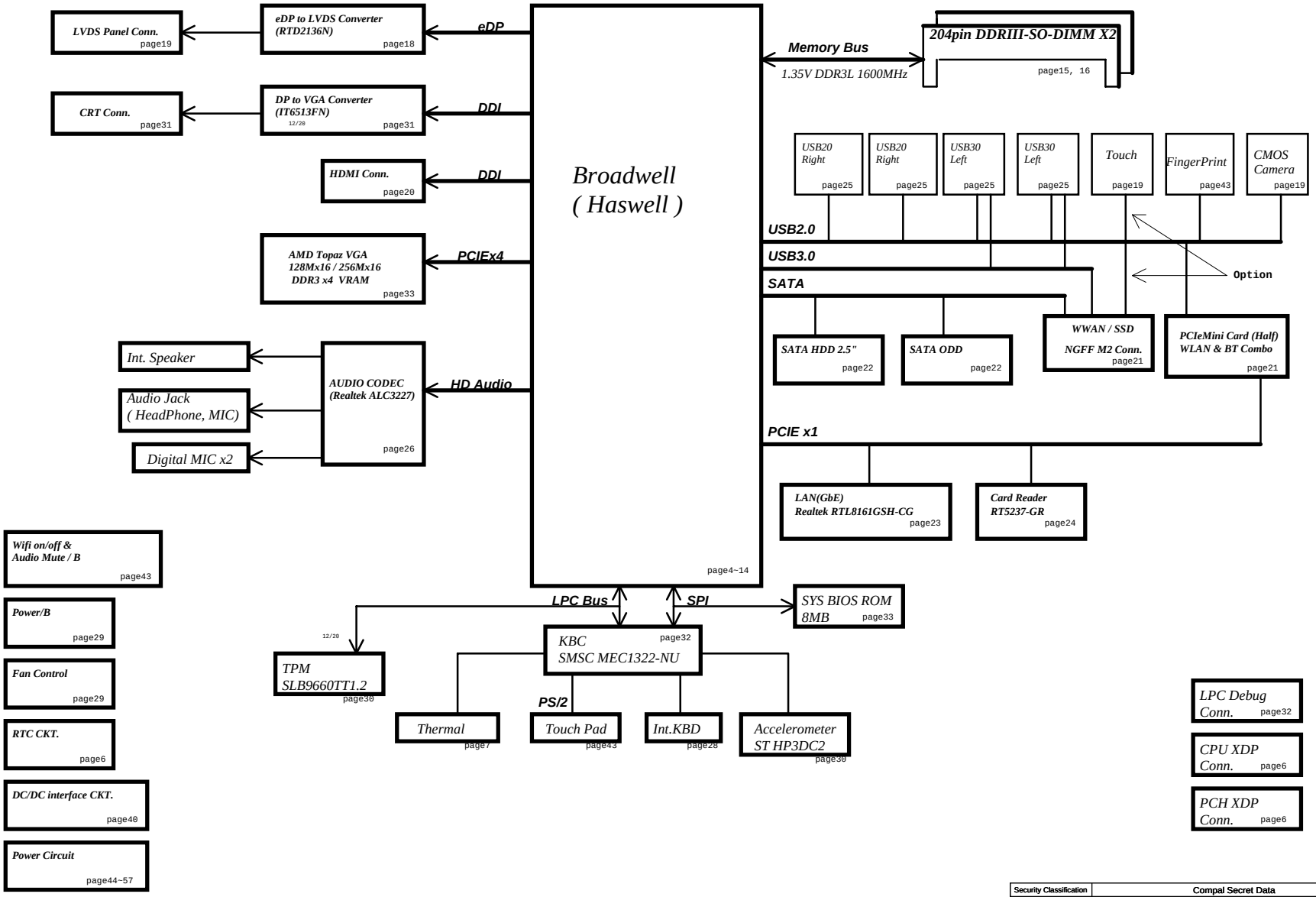
Compal Electronics, Inc.		
Title: Cover Page		
Size: B	Document Number: LA-B181P	Rev: 0.5
Date: Tuesday, March 25, 2014	Sheet 1 of 62	

Compal Confidential

Model Name :

Intel Broadwell U / Haswell Block Diagram

Project Name :



CPU DC/DC TPS51622ARSMR 50~51	
INPUTS	OUTPUTS
B+	VCC_VORE

SYSTEM DC/DC RT8243AZQW 47	
INPUTS	OUTPUTS
B+	3VDS/5VDS

SYSTEM DC/DC RT8207MZQW 48	
INPUTS	OUTPUTS
B+	1.35V_VDDQ 0.675VS

SYSTEM DC/DC SY8206DQNC 49	
INPUTS	OUTPUTS
B+	1.05VS

SYSTEM DC/DC SY8003DFC 52	
INPUTS	OUTPUTS
B+	1.5VS

SYSTEM DC/DC RT8880BGQW 54~55	
INPUTS	OUTPUTS
B+	+VGA_CORE

SYSTEM DC/DC SY8003DFC 56	
INPUTS	OUTPUTS
B+	+1.8VS_VGA

SYSTEM DC/DC SY8003DFC 57	
INPUTS	OUTPUTS
B+	+0.95VS_VGA

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/29	Deciphered Date 2011/06/29	Title: Block Diagrams
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Size: Custom; Document Number: LA-B181P; Rev: 0.5
			Date: Tuesday, March 25, 2014; Sheet 2 of 62

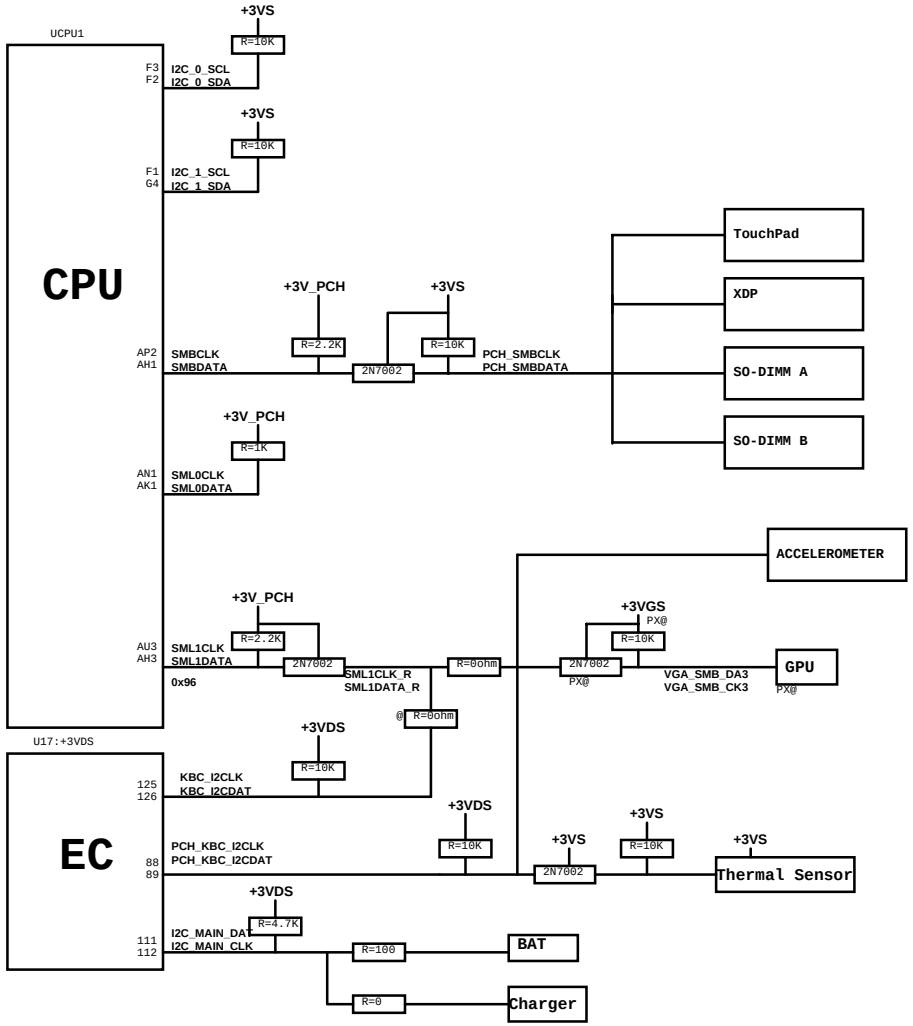
@ is NO SMT part (empty)
short@ : short pad , don't pop.
@EMI@,@ESD@,@RF@ : Reserve , don't pop.

RF@ : RF team request, must add.
EMI@ : EMI team request, must add.
ESD@ : ESD team request, must add.

LVDS@ : Support LVDS panel.
eDP@ : Support eDP panel.

WWAN@ : For WWAN function.

PX@ : GPU BOM config.



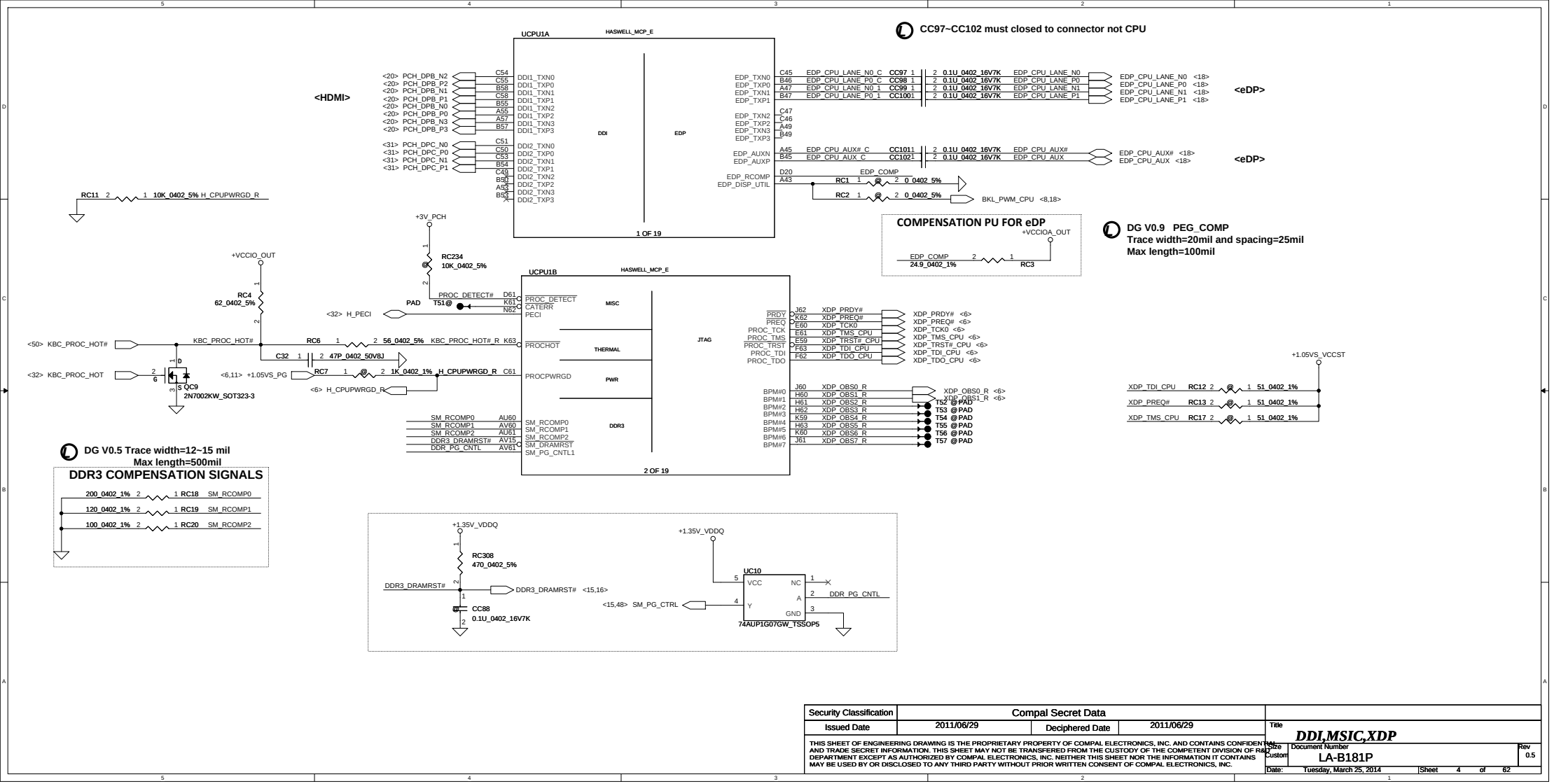
<USB2.0 port>

USB2.0 port	DESTINATION CS
0	USB 2.0(Right side)
1	USB 2.0(Right side)
2	USB 2.0(Left side)
3	WLAN/BT
4	Finger Print
5	WWAN (Option) Touch
6	Camera
7	USB 2.0(Left side)

<PCI-E,SATA,USB3.0>

Lane#	PCI-E		SATA	USB3.0	DESTINATION CS
1				0	USB3.0
2				1	USB3.0
3	1			2	WWAN (M.2)
4	2			3	Card reader(PCI-E)
5	3				10/100/1000 LAN
6	4				WLAN (M.2)
7	5				GPU(DIS only)
8					GPU(DIS only)
9					GPU(DIS only)
10					GPU(DIS only)
11	6	L3	3		2.5"HDD
12		L2	2		ODD
13		L1	1		
14		L0	0		SSD(NGFF)

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/29	Deciphered Date	2011/06/29
Title: Notes List			
Size: Custom	Document Number: LA-B181P		Rev: 0.5
Date: Tuesday, March 25, 2014	Sheet 3 of 62		

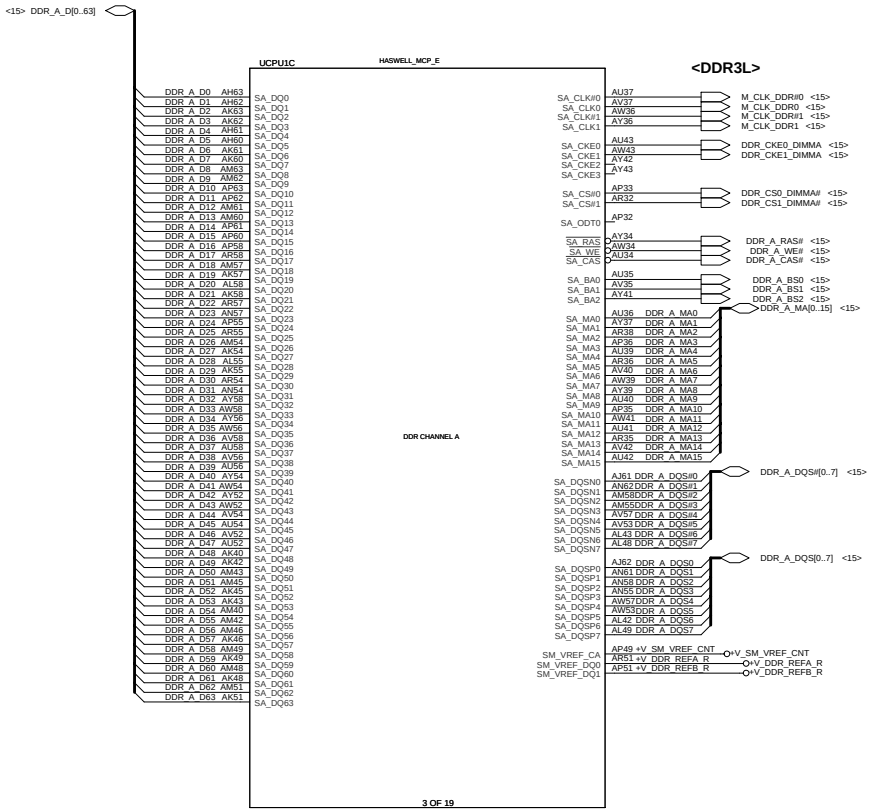


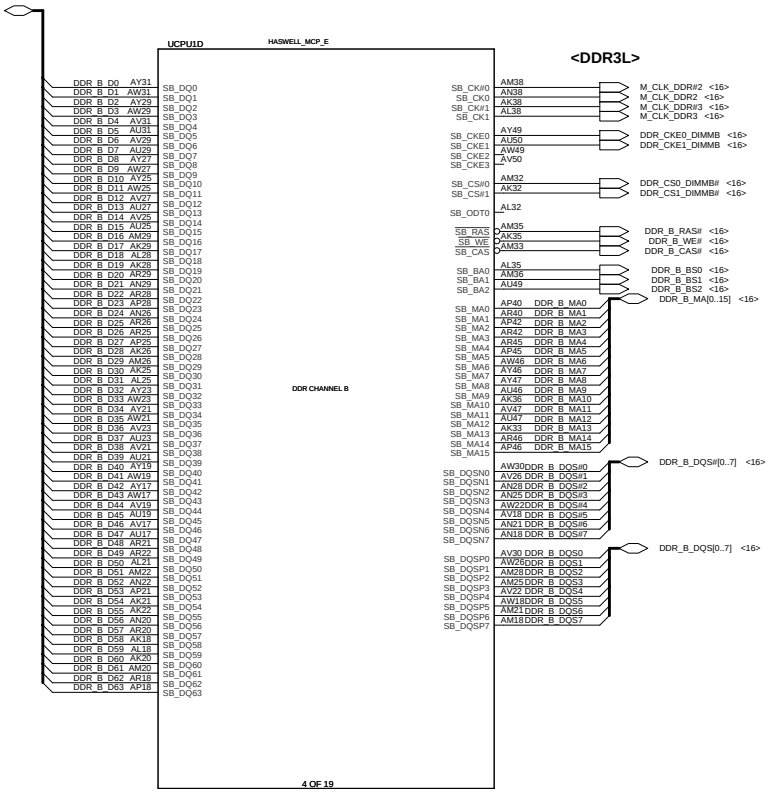
Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Title: *DDI,MSIC,XDP*

Size	Document Number	Rev
Custom	LA-B181P	0.5

Date: Tuesday, March 25, 2014 | Sheet 4 of 62

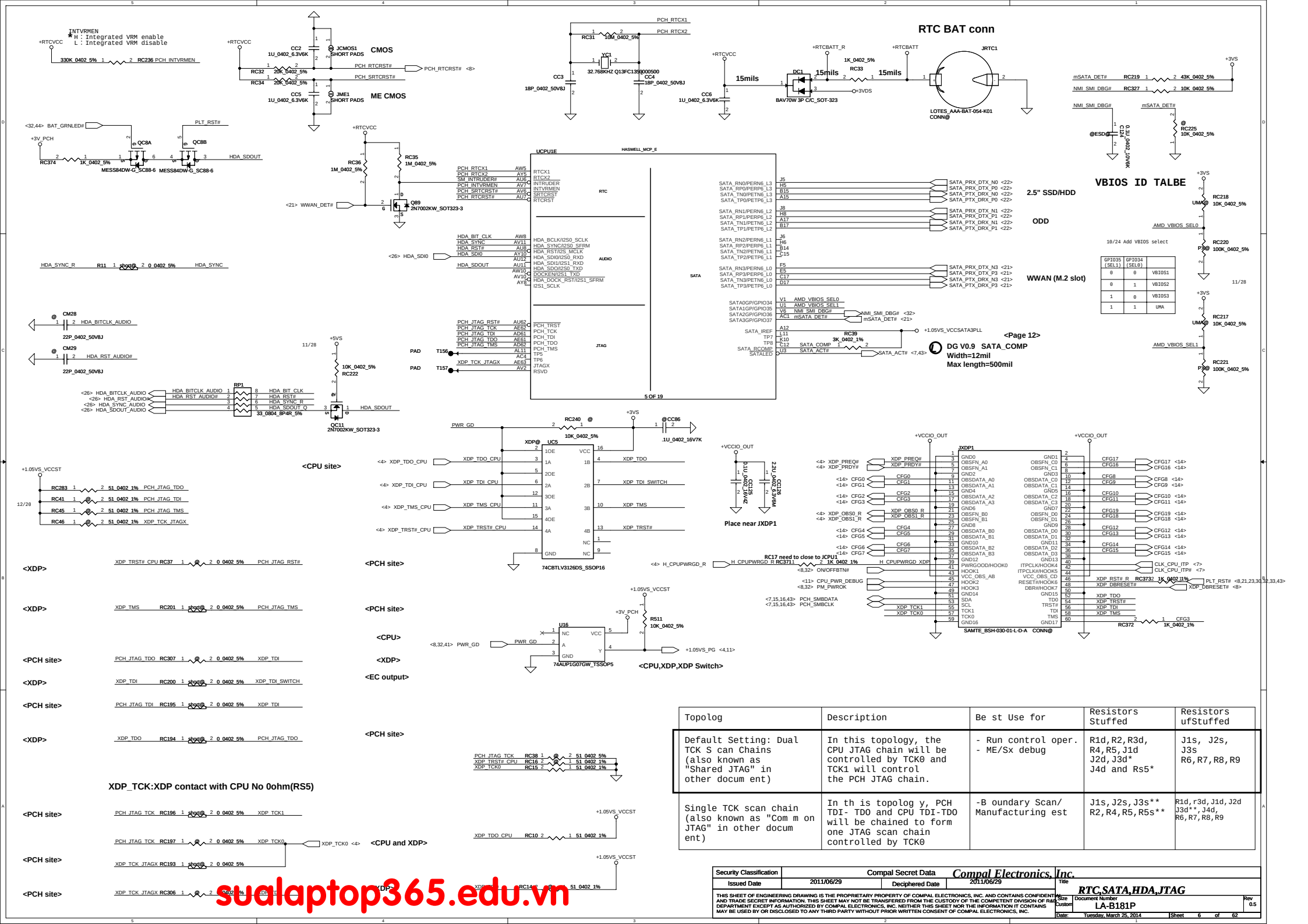




Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Title	DDRIII		
Size	Document Number		Rev
Custom	LA-B181P		0.5
Date:	Tuesday, March 25, 2014	Sheet 5 of 62	

Compal Electronics, Inc.

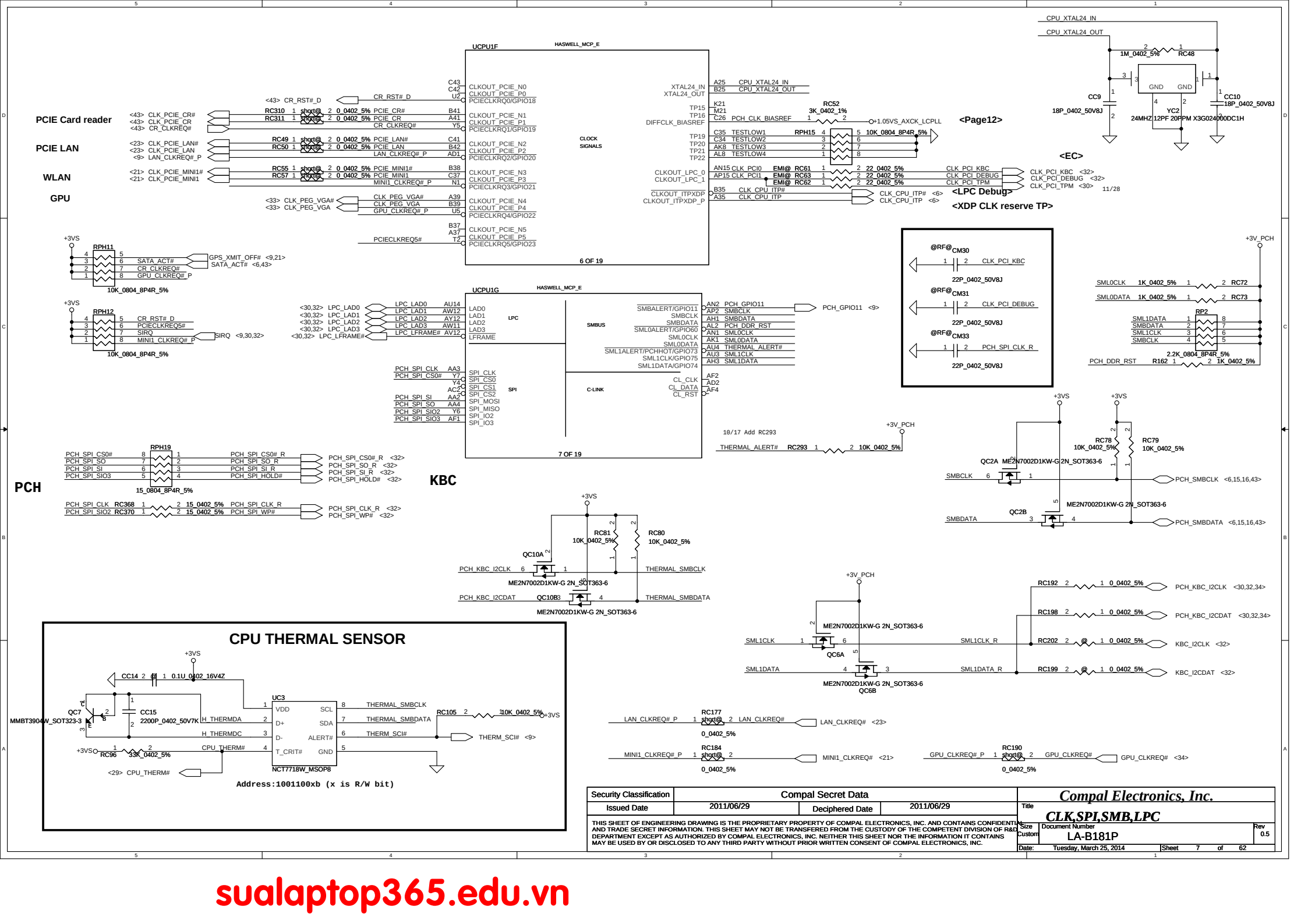


Topolog	Description	Be st Use for	Resistors Stuffed	Resistors ufStuffed
Default Setting: Dual TCK S can Chains (also known as "Shared JTAG" in other docum ent)	In this topology, the CPU JTAG chain will be controlled by TCK0 and TCK1 will control the PCH JTAG chain.	- Run control oper. - ME/Sx debug	R1d,R2,R3d, R4,R5,J1d J2d,J3d* J4d and Rs5*	J1s, J2s, J3s R6,R7,R8,R9
Single TCK scan chain (also known as "Com m on JTAG" in other docum ent)	In th is topolog y, PCH TDI- TDO and CPU TDI-TDO will be chained to form one JTAG scan chain controlled by TCK0	-B oundary Scan/ Manufacturing est	J1s,J2s,J3s** R2,R4,R5,R5s**	R1d,r3d,J1d,J2d J3d**,J4d, R6,R7,R8,R9

Security Classification	Compal Secret Data	Compal Electronics, Inc.
Issued Date 2011/06/29	Deciphered Date 2011/06/29	Title RTC,SATA,HDA,JTAG

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Size	Document Number	Rev
Custom	LA-B181P	0.5
Date: Tuesday, March 25, 2014	Sheet 6 of 62	



Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

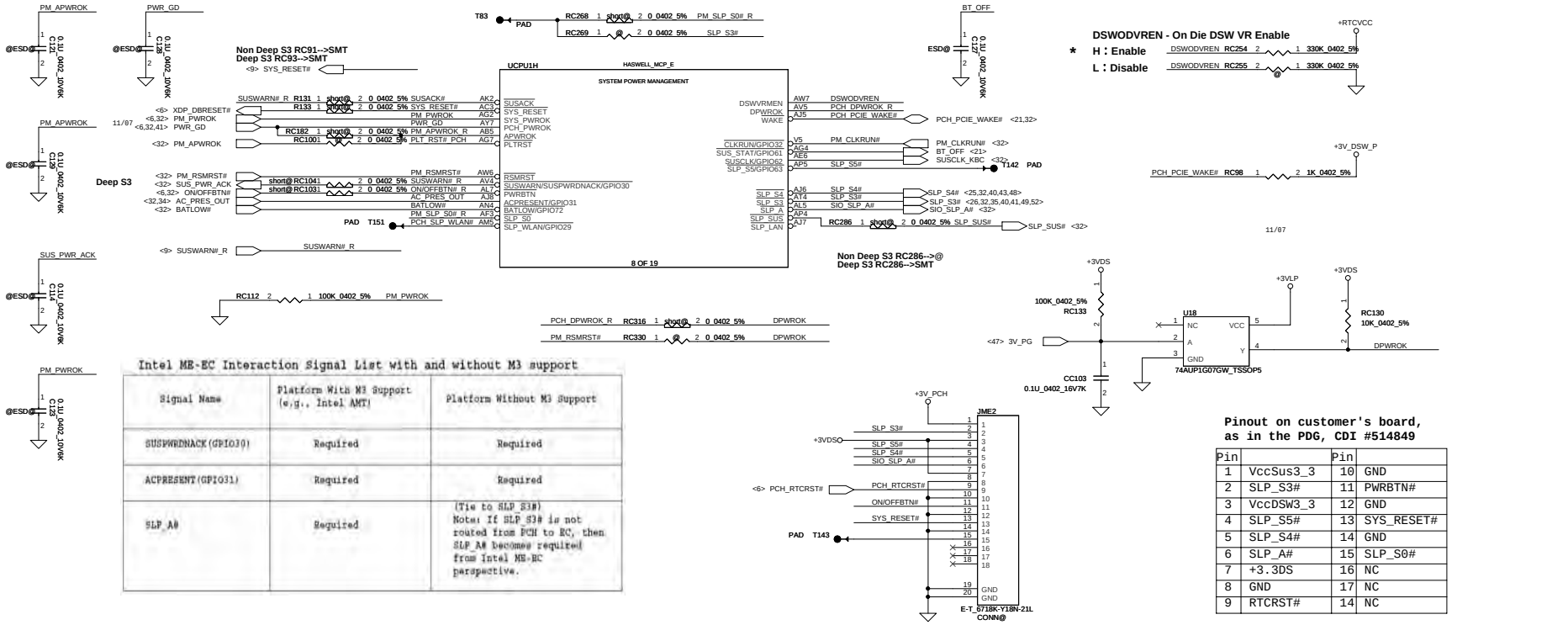
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

Title: CLK,SPI,SMB,LPC

Size: Custom | Document Number: LA-B181P | Rev: 0.5

Date: Tuesday, March 25, 2014 | Sheet 7 of 62

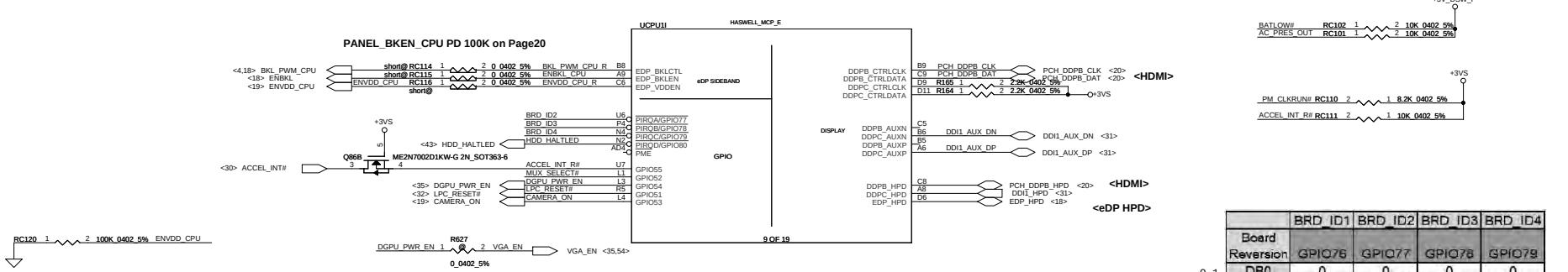


Intel ME-EC Interaction Signal List with and without M3 support

Signal Name	Platform With M3 Support (e.g., Intel AMT)	Platform Without M3 Support
SUSWRDNACK(GPIO30)	Required	Required
ACPRESENT(GPIO31)	Required	Required
SLP_A#	Required	(Tie to SLP_S3#) Note: If SLP_S3# is not routed from PCH to EC, then SLP_A# becomes required from Intel ME-EC perspective.

Pinout on customer's board, as in the PDG, CDI #514849

Pin		Pin	
1	VccSus3_3	10	GND
2	SLP_S3#	11	PWRBTN#
3	VccDSW3_3	12	GND
4	SLP_S5#	13	SYS_RESET#
5	SLP_S4#	14	GND
6	SLP_A#	15	SLP_S0#
7	+3.3DS	16	NC
8	GND	17	NC
9	RTCRST#	14	NC



Board Reversion	BRD_ID1 GPIO76	BRD_ID2 GPIO77	BRD_ID3 GPIO78	BRD_ID4 GPIO79
0.1 DB0	0	0	0	0
DB1	0	0	0	1
0.2 DB2	0	0	1	0
0.3	0	0	1	1
0.4 SI1	0	1	0	0
SI1B	0	1	0	1
SI2	0	1	1	0
	0	1	1	1
0.5 PV1	1	0	0	0
	1	0	0	1
	1	0	1	0
	1	0	1	1
MV	1	1	0	0
	1	1	0	1
	1	1	1	0
	1	1	1	1

Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.			
Title	PM,GPIO,DDI		
Size: Custom	Document Number: LA-B181P		Rev: 0.5
Date: Tuesday, March 25, 2014	Sheet 8 of 62		

UCPU1J
HASWELL_MCP_E
10 OF 19

DG V0.9 PCH_OPIRCOMP
Width=12mil,spacing=12mil
Max length=500mil

Boot BIOS Strap

	PCH_GPIO86	Boot BIOS Location
*	0	SPI

PCH Strap

Boot BIOS Strap Bit (BBS)	GSPI0_MOSI/GPIO86
* SPI	0
LPC	1

Platform ID

12/20

PLT_ID1	RC266	1	2 10K_0402_5%
PLT_ID2	RC272	1	2 10K_0402_5%
PLT_ID3	RC273	1	2 10K_0402_5%
PLT_ID1	RC275	1	@ 2 10K_0402_5%
PLT_ID2	RC276	1	@ 2 10K_0402_5%
PLT_ID3	RC277	1	@ 2 10K_0402_5%

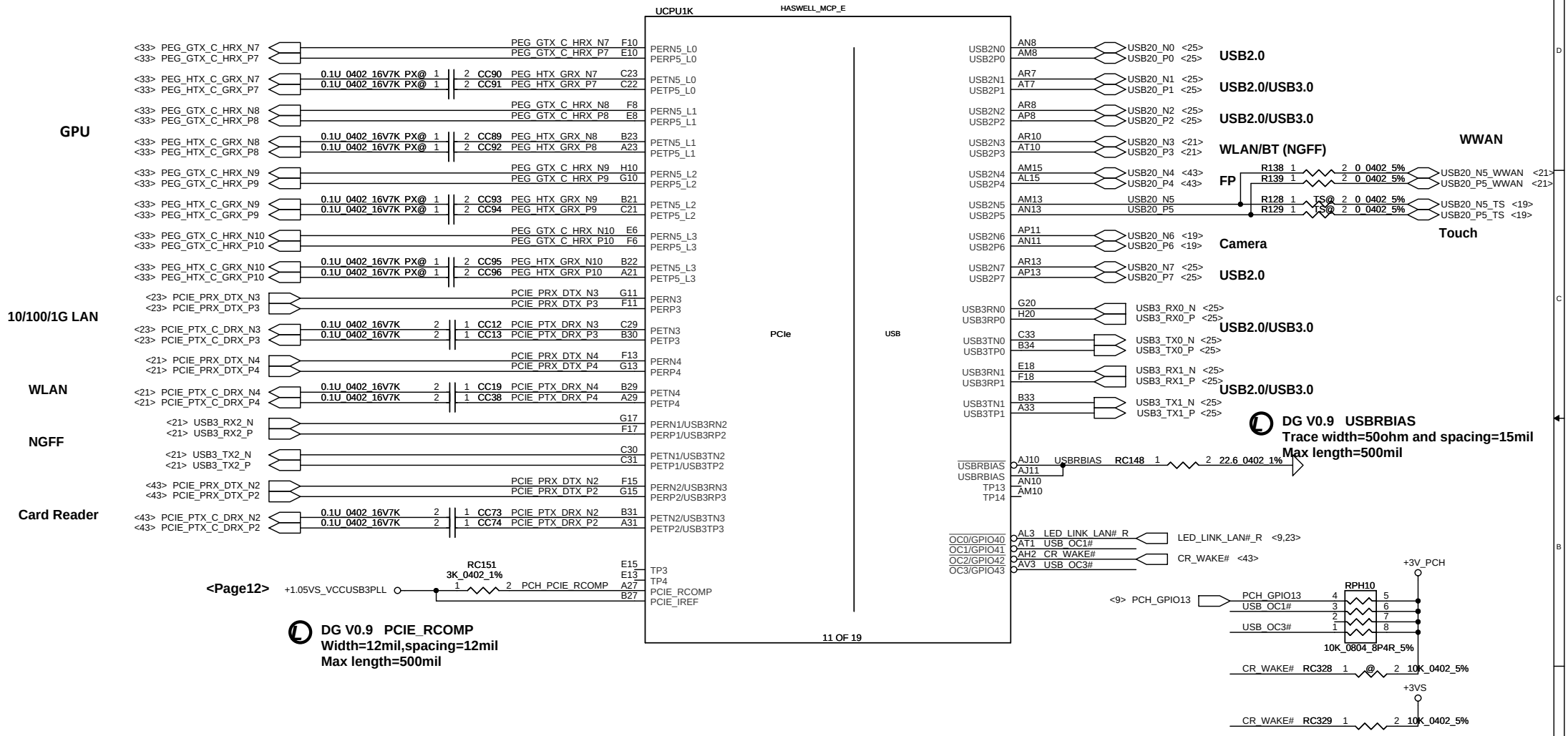
TOUCH_RST#	RC274	1	2 10K_0402_5%
DOCKID1	RC284	1	2 10K_0402_5%
SC_PWRSV#	RC287	1	2 10K_0402_5%
ODD_DA#	RC289	1	2 10K_0402_5%
PCH_GPIO4	RC290	1	2 10K_0402_5%
TOUCH_DET#	RC291	1	2 10K_0402_5%
EC_SCI#	RC292	1	2 10K_0402_5%
SDIO_CLK	RC299	1	2 10K_0402_5%
FPR_OFF	RC305	1	2 10K_0402_5%
SDIO_D1	RC309	1	2 10K_0402_5%
SDIO_D3	RC312	1	2 10K_0402_5%
PCH_GPIO76	RC126	1	2 10K_0402_5%
GSPI0_CLK	RC315	1	2 10K_0402_5%
GSPI0_MISO	RC317	1	2 10K_0402_5%
GSPI1_CS#	RC318	1	2 10K_0402_5%
GSPI1_CLK	RC319	1	2 10K_0402_5%
GSPI1_MISO	RC320	1	2 10K_0402_5%
GSPI1_MOSI	RC321	1	2 10K_0402_5%

Security Classification	Compal Secret Data	
Issued Date	2011/06/29	Deciphered Date 2011/06/29

Title: GPIO,UART,I2C

Size	Document Number	Rev
Custom	LA-B181P	0.5

Date: Tuesday, March 25, 2014 Sheet 9 of 62



Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Title	PCIE,USB		
Size: B	Document Number: LA-B181P		Rev: 0.5
Date: Tuesday, March 25, 2014	Sheet 10 of 62		

+VCC_CORE@10000mA

SVID ALERT

+1.05VS_VCCST

RC154 75_0402_5%

<50> VR_SVID_ALRT# — RC155 1 — 2 43_0402_1% H_CPU_SVIDALRT#

DG V0.5 H_CPU_SVIDALRT#
RC154 close to CPU<300mil
Max length=1000~2000mil

SVID DATA

+1.05VS_VCCST

RC156 130_0402_1%

<50> VR_SVID_DAT — VR_SVID_DAT

DG V0.5 VIDSOUT
RC156 close to CPU<500mil
Max length=1000~2000mil

+1.05VS — RC294 1 — @ — 2 0_0402_5% — +VCCIO_OUT

VCC_SENSE

+VCC_CORE — RC157 100_0402_1% — VCCSENSE

<50> VCCSENSE

+VCCIO_OUT
+VCCIOA_OUT

<50> VR_SVID_CLK
<50> VR_SVID_DAT
<50> VR12.5_VR_ON — RC301 RF@ 0_0402_5% — <4,6> +1.05VS_PG — VR12.6PG_MCP

@RF@ C421 33P_0402_50V8J

CPU_PWR_DEBUG

UCPU1L — HASWELL_MCP_E — HSW ULT POWER — 12 OF 19

+1.35V_VDDQ	L59	RSVD	
	J58	RSVD	
2500mA	AH26	VDDQ	
	AJ31	VDDQ	
	AJ33	VDDQ	
	AJ37	VDDQ	
	AN33	VDDQ	
	AP43	VDDQ	
	AR48	VDDQ	
	AY35	VDDQ	
	AY40	VDDQ	
	AY44	VDDQ	
	AY50	VDDQ	
	F59	VCCIN	
	N58	RSVD	
	AC58	RSVD	
	E63	VCCSENSE	
	AB23	VCC_SENSE	
	A59	RSVD	
	E20	VCCIO_OUT	
	AD23	VCCIOA_OUT	
	AA23	RSVD	
	AE59	RSVD	
	AE59	RSVD	
H_CPU_SVIDALRT#	L62	VIDALERT	
VR_SVID_CLK	N63	VIDSCLK	
VR_SVID_DAT	L63	VIDSOUT	
	B59	VCCST_PWRGD	
	F60	VR_EN	
VR12.6PG_MCP	C59	VR_READY	
	D63	VSS	
CPU_PWR_DEBUG	H59	PWR_DEBUG	
	P62	VSS	
	P60	RSVD_TP	
	P61	RSVD_TP	
	N59	RSVD_TP	
	N61	RSVD_TP	
	T59	RSVD_TP	
	AD60	VSS	
	AD59	VSS	
	AA59	VSS	
	AE60	VSS	
	AC59	VSS	
	AG58	VSS	
	U59	VSS	
	V59	VSS	
+1.05VS_VCCST	AC22	VCCST	
600mA	AE22	VCCST	
	AE23	VCCST	
	AB57	VCC	
	AD57	VCC	
	AG57	VCC	
	C24	VCC	
	C28	VCC	
	C32	VCC	

+VCC_CORE	C36	VCC	
	C40	VCC	
	C44	VCC	
	C48	VCC	
	C52	VCC	
	C56	VCC	
	E23	VCC	
	E25	VCC	
	E27	VCC	
	E29	VCC	
	E31	VCC	
	E33	VCC	
	E35	VCC	
	E37	VCC	
	E39	VCC	
	E41	VCC	
	E43	VCC	
	E45	VCC	
	E47	VCC	
	E49	VCC	
	E51	VCC	
	E53	VCC	
	E55	VCC	
	E57	VCC	
	F24	VCC	
	F28	VCC	
	F32	VCC	
	F36	VCC	
	F40	VCC	
	F44	VCC	
	F48	VCC	
	F52	VCC	
	F56	VCC	
	G23	VCC	
	G25	VCC	
	G27	VCC	
	G29	VCC	
	G31	VCC	
	G33	VCC	
	G35	VCC	
	G37	VCC	
	G39	VCC	
	G41	VCC	
	G43	VCC	
	G45	VCC	
	G47	VCC	
	G49	VCC	
	G51	VCC	
	G53	VCC	
	G55	VCC	
	G57	VCC	
	H23	VCC	
	J23	VCC	
	K23	VCC	
	K57	VCC	
	L22	VCC	
	M23	VCC	
	M57	VCC	
	P57	VCC	
	U57	VCC	
	W57	VCC	

+1.05VS_VCCST — RC166 150_0402_5% — CPU_PWR_DEBUG — CPU_PWR_DEBUG <6> — 10K_@RC167 10K_0402_5%

+1.05VS — RC2231 short@ 0_0805_5% — +1.05VS_VCCST

CC771 22U_0805_6.3V6M — CC72 1U_0402_6.3V6K — 1U_0402_6.3V6K

11/07

VR12.5_VR_ON — RC288 10K_0402_5% — VR12.6PG_MCP — <50> VR12.6PG_MCP

+1.35V_VDDQ

CC20 2.2U_0402_6.3V6M — CC21 2.2U_0402_6.3V6M — CC22 2.2U_0402_6.3V6M — CC23 2.2U_0402_6.3V6M

CC24 330U_2.5V_M — CC25 330U_2.5V_M

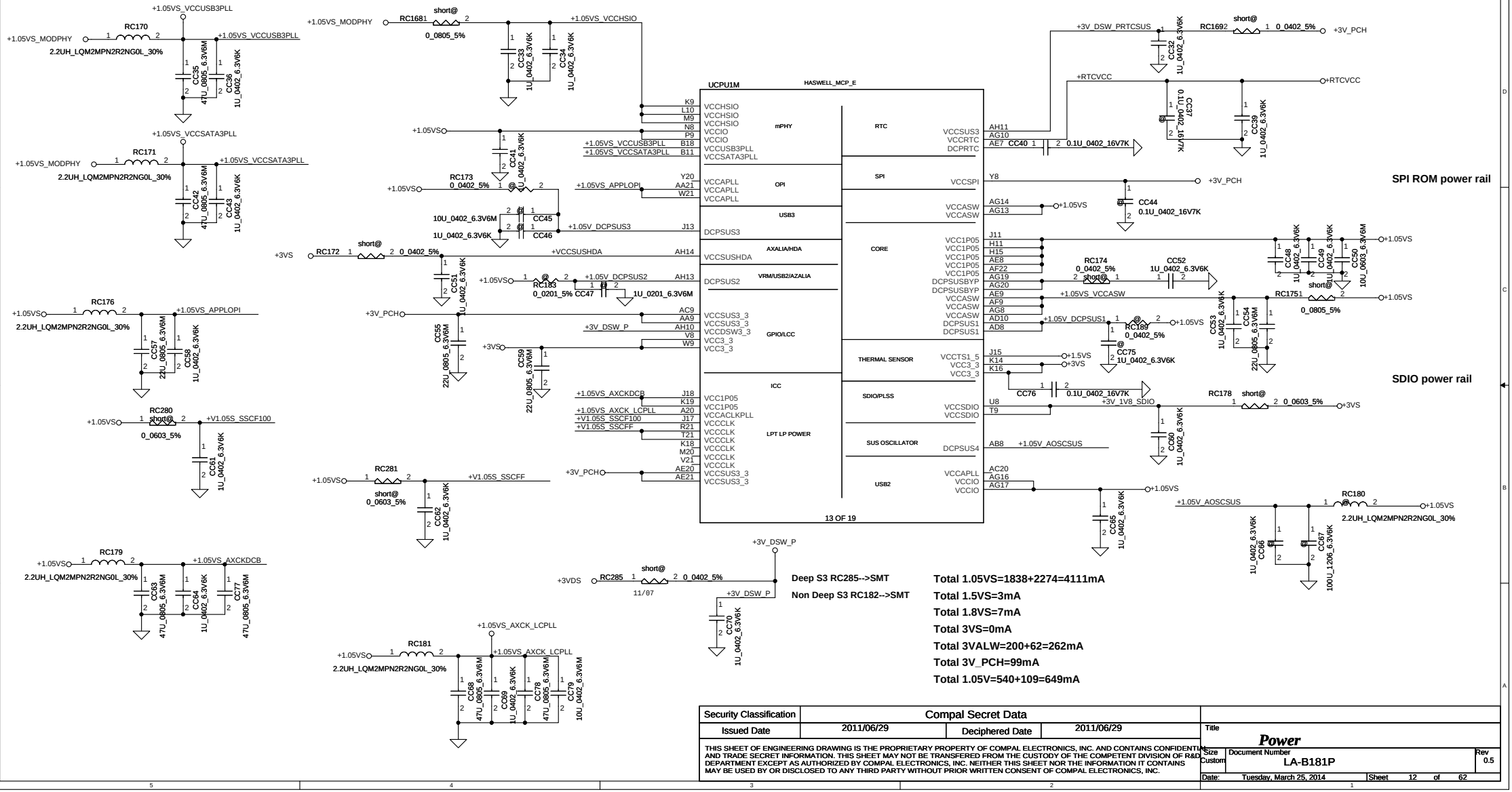
10U_0603_6.3V6M: CC26, CC27, CC28, CC29, CC30, CC31

Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: Power

Size: Custom	Document Number: LA-B181P	Rev: 0.5
Date: Tuesday, March 25, 2014	Sheet 11 of 62	

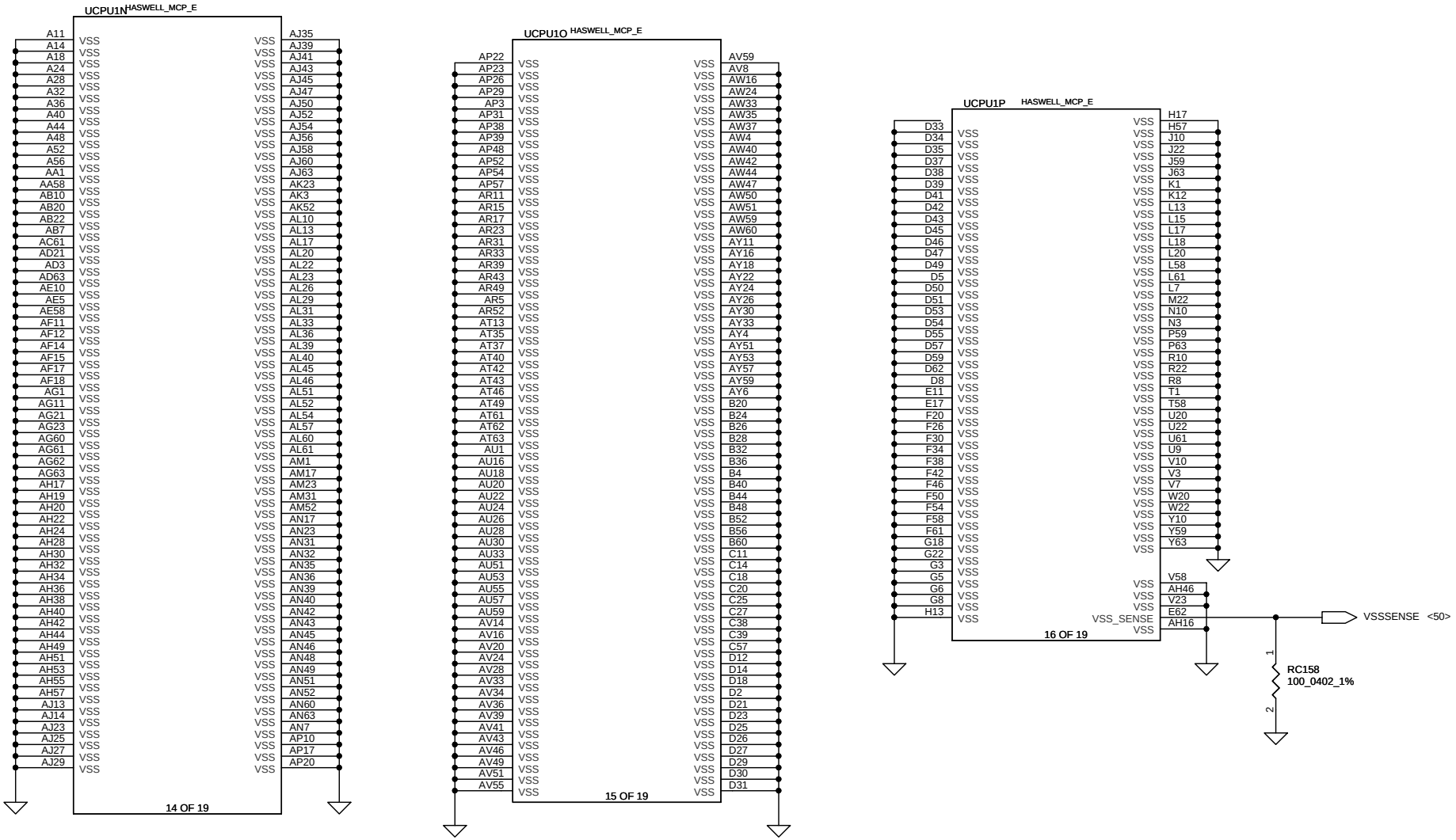


Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Title: **Power**

Size	Document Number	Rev
Custom	LA-B181P	0.5

Date: Tuesday, March 25, 2014 Sheet 12 of 62



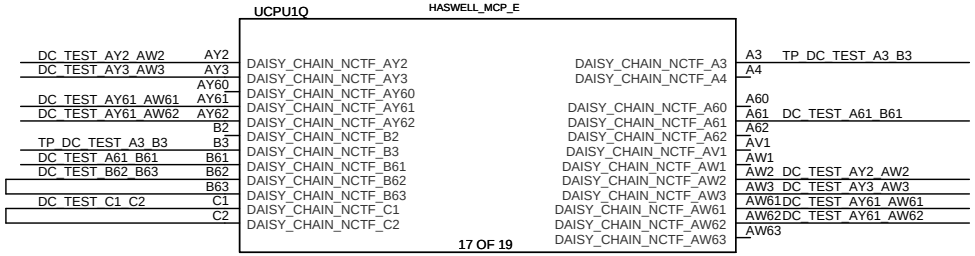
Security Classification	Compal Secret Data		
Issued Date	2010/05/27	Deciphered Date	2011/05/11

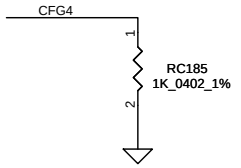
Compal Electronics, Inc.

Title: GND/VSSSEN

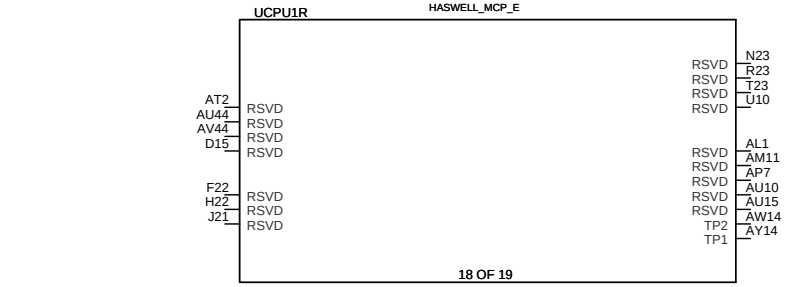
Size | Document Number: LA-B181P | Rev: 0.5

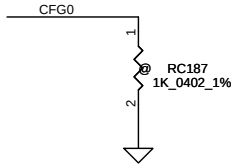
Date: Tuesday, March 25, 2014 | Sheet 13 of 62

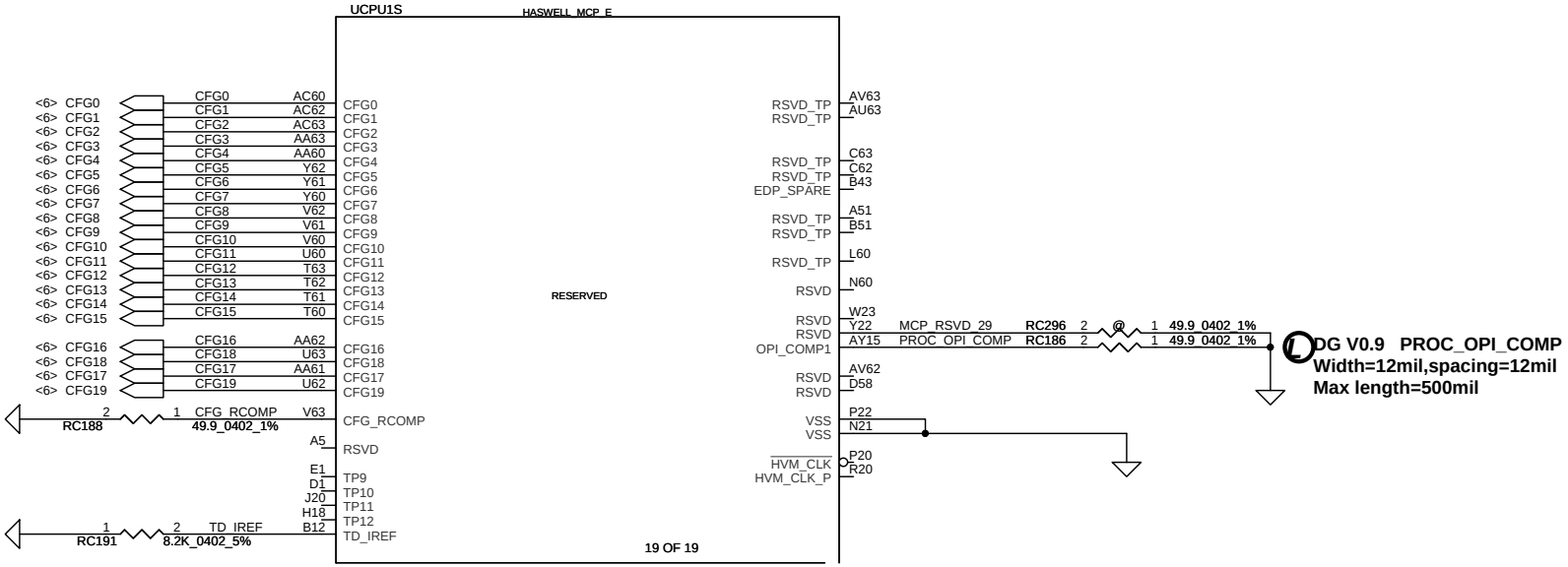




Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port







DG V0.9 PROC_OPI_COMP
Width=12mil,spacing=12mil
Max length=500mil

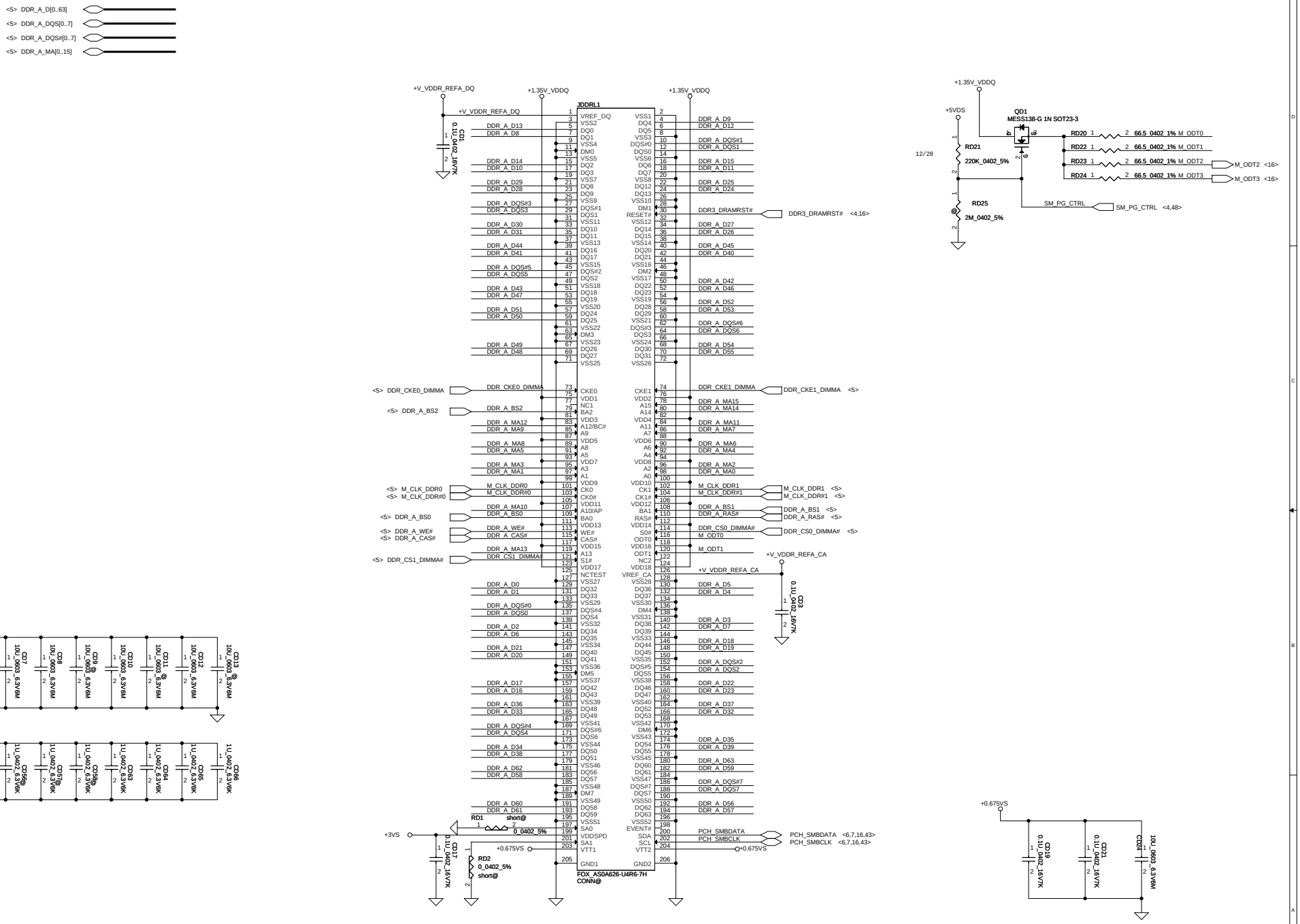
Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: RSVD/CFG

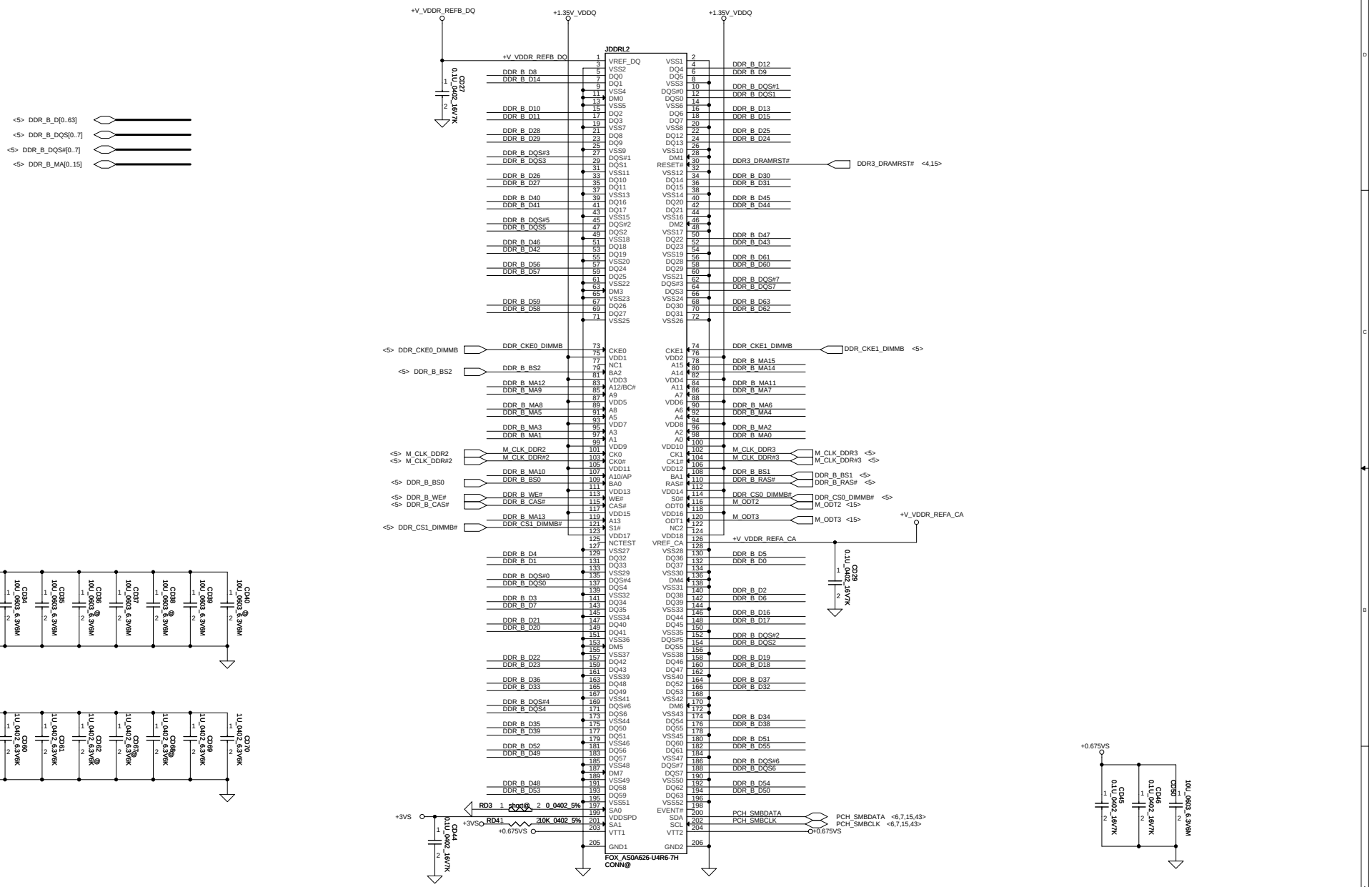
Size	Document Number	Rev
	LA-B181P	0.5

Date: Tuesday, March 25, 2014 Sheet 14 of 62



Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Title	DDR3L DIMM0		
Size C	Document Number LA-B181P		Rev 0.5
Date: Tuesday, March 25, 2014	Sheet 15 of 62		



Security Classification	Compal Secret Data		
Issued Date	2010/05/27	Deciphered Date	2011/05/11

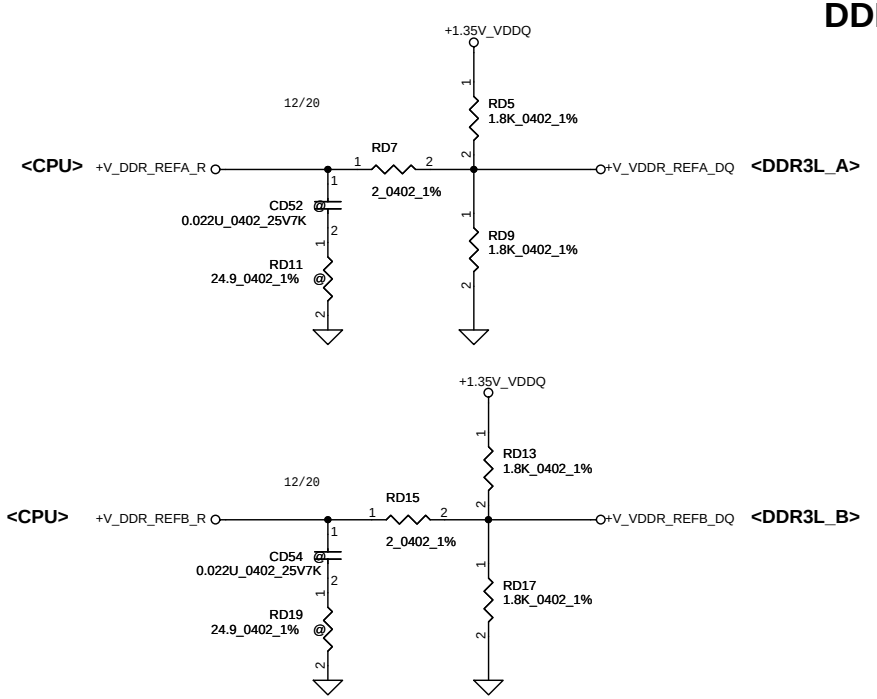
Compal Electronics, Inc.

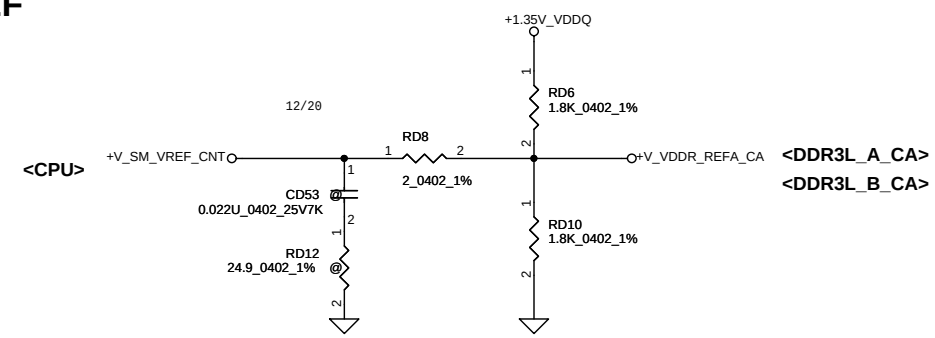
Title: DDR3L DIMM1

Size	Document Number	Rev
	LA-B181P	0.5

Date: Tuesday, March 25, 2014 | Sheet 16 of 62

DDR3L VREF





Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: DDR3L VREF

Size	Document Number	Rev
	LA-B181P	0.5

Date: Tuesday, March 25, 2014 Sheet 17 of 62

JPHW7 need to short

+3VS — 80mil — @JPHW7 (JUMP_43X79) — 80mil — +3VS_RT

Layout note
Close to Pin3

+DP_V33 — 10U_0603_6.3V6M, 0.1U_0402_16V4Z (CT38, CT39, CT40)

Layout note
Close to LT5 Close to Pin18 Close to Pin13

+SWR_VDD — 10U_0603_6.3V6M, 0.1U_0402_16V4Z (CT29, CT30, CT31, CT32, CT33)

Layout note
Close to Pin11 Close to Pin27 Close to Pin7

+SWR_V12 — 10U_0603_6.3V6M, 0.1U_0402_16V4Z (CT34, CT35, CT36, CT37)

※ROM only mode : PIN 47 4.7k pull low, Pin 48 4.7k pull high.
EP mode : PIN 47 4.7k pull high, Pin 48 4.7k pull low.
EEPROM : PIN 47 4.7k pull high, Pin 48 4.7k pull high.
〈 ※Default mode 〉

+3VS_RT — RT27@ 4.7K_0402_5% — MIIC_SDA — PIN47
+3VS_RT — RT28 4.7K_0402_5% — MIIC_SCL — RT29 4.7K_0402_5% — PIN48 — RT30@ 4.7K_0402_5%

SWR / LDO Mode select

	LDO	SWR
2132S	Do not support	mount LT7
2132R	Use 0 ohm	mount LT7

※ If use 2132R, please select LDO mode as default.

RTD2136N

UT1 LVDS@

+3VS_RT — PVCC
+SWR_VDD 100mil — SWR_VDD
DP_V33
+SWR_V12 — RT31 4.7UH_1098AS-4R7M_1.3A_20% — +SWR_LX — SWR_LX
SWR_VCCK
VCCK
DP_V12

PWR

LANE0P / LANE0N ← <4> EDP_CPU_LANE_P0 / N0
LANE1P / LANE1N ← <4> EDP_CPU_LANE_P1 / N1
AUX-CH_P / AUX-CH_N ← <4> EDP_CPU_AUX / AUX#
DP_HPD ← <8> EDP_HPD, RT34 1K_0402_1%, RT35 100K_0402_5%

LVDS DP

PWMIN ← <4,8> BKL_PWM_CPU, PAD-D TT1, RT36 12K_0402_1%
TESTMODE
DP_REXT
MIIC_SCL / MIIC_SDA
CIICSCL / CIICSDA ← @TT2 CIICSCL, @TT3 CIICSDA

OTHERS

DP_GND
GND
PAD

GND

RTD2136N-CGT_QFN_48 — EDP/LVDS_CTRL

TXOC+ / TXOC-	35 / 36	LVDS_A_CLKP / LVDS_A_CLKN → LVDS_A_CLKP <19> / LVDS_A_CLKN <19>
TXO0+ / TXO0-	41 / 42	LVDS_A_TXP0 / LVDS_A_TXN0 → LVDS_A_TXP0 <19> / LVDS_A_TXN0 <19>
TXO1+ / TXO1-	39 / 40	LVDS_A_TXP1 / LVDS_A_TXN1 → LVDS_A_TXP1 <19> / LVDS_A_TXN1 <19>
TXO2+ / TXO2-	37 / 38	LVDS_A_TXP2 / LVDS_A_TXN2 → LVDS_A_TXP2 <19> / LVDS_A_TXN2 <19>
TXO3+ / TXO3-	33 / 34	TT4 PAD-D, TT5 PAD-D
TXEC+ / TXEC-	25 / 26	LVDS_B_CLKP / LVDS_B_CLKN → LVDS_B_CLKP <19> / LVDS_B_CLKN <19>
TXE0+ / TXE0-	31 / 32	LVDS_B_R_TXOUT0+ / TXOUT0-
TXE1+ / TXE1-	29 / 30	LVDS_B_R_TXOUT1+ / TXOUT1-
TXE2+ / TXE2-	27 / 28	LVDS_B_R_TXOUT2+ / TXOUT2-
TXE3+ / TXE3-	23 / 24	TT6 PAD-D, TT7 PAD-D
MIICSCL1 / MIICSDA1	46 / 45	LCD_EDID_CLK / LCD_EDID_DATA → LCD_EDID_CLK <19> / LCD_EDID_DATA <19>
PANEL_VCC	20	DP_ENVDD → DP_ENVDD <19>
PWMOUT	19	INVTPWM → INVTPWM <19>
BL_EN	44	TS_BKOFF#

+SWR_VDD — UT5 @ CAT24C64WI-GT3_SO8 — LCD_EDID_CLK, LCD_EDID_DATA

+3VS_RT — LCD_EDID_CLK RT32 4.7K_0402_5% — LCD_EDID_DATA RT33 4.7K_0402_5%

+SWR_VDD — RT37 4.7K_0402_5% CIICSCL — RT38 4.7K_0402_5% CIICSDA

DP_ENVDD — RT39 100K_0402_5%

RP38 eDP@
EDP_CPU_LANE_P0 / N0 / P1 / N1 → EDP_CPU_R_LANE_P0 / N0 / P1 / N1
0_0804_8P4R_5% <to connector>

RP39 eDP@
EDP_CPU_R_LANE_P1 / N1 / P0 / N0 → LVDS_B_TXOUT1+ / 1- / 0+ / 0-
0_0804_8P4R_5%

EDP_CPU_AUX RT43 eDP@ 0_0402_5% EDP_CPU_R_AUX RT45 eDP@ 0_0402_5% LVDS_B_TXOUT2+
EDP_CPU_AUX# RT44 eDP@ 0_0402_5% EDP_CPU_R_AUX# RT46 eDP@ 0_0402_5% LVDS_B_TXOUT2-

LVDS_B_R_TXOUT1+ RT53 LVDS@ 0_0402_5% LVDS_B_TXOUT1+ → LVDS_B_TXOUT1+ <19>
LVDS_B_R_TXOUT1- RT54 LVDS@ 0_0402_5% LVDS_B_TXOUT1- → LVDS_B_TXOUT1- <19>
LVDS_B_R_TXOUT0+ RT55 LVDS@ 0_0402_5% LVDS_B_TXOUT0+ → LVDS_B_TXOUT0+ <19>
LVDS_B_R_TXOUT0- RT56 LVDS@ 0_0402_5% LVDS_B_TXOUT0- → LVDS_B_TXOUT0- <19>

LVDS_B_R_TXOUT2+ RT47 LVDS@ 0_0402_5% LVDS_B_TXOUT2+ → LVDS_B_TXOUT2+ <19>
LVDS_B_R_TXOUT2- RT48 LVDS@ 0_0402_5% LVDS_B_TXOUT2- → LVDS_B_TXOUT2- <19>

EDP_HPD RT49 eDP@ 0_0402_5% EDP_HPD_PANEL RT51 eDP@ 0_0402_5% EDP_HPD_PANEL_R → EDP_HPD_PANEL_R <19>
BKL_PWM_CPU RT50 eDP@ 0_0402_5% INVTPWM
<LVDS panel>

	PIN15
2132S	TL_ENVDD
2132R	+LCD_VDD *

* Version R internal Power Switch, can output 1A, Rds(on)=0.2 ohm

PIN16	Accept voltage input (high level)
2132S	3.3V
2132R	1.5~3.3V

* Version R has internal level shifter, remove level shifter circuit on AMD platform

INVTPWM — LVDS@ R163 100K_0402_5%

RT41 @ 0_0402_5%
RT42 eDP@ 100K_0402_5%
+3VS — CT41 0.1U_0402_16V7K
TS_BKOFF# — LVDS@ — IN1 / IN2 / VCC / GND / OUT — EC_TS_BKOFF# <19>
<8> ENBKL → ENBKL
UT6 MC74VHC1G08DFT2G_SC70-5
RT52 eDP@ 0_0402_5%

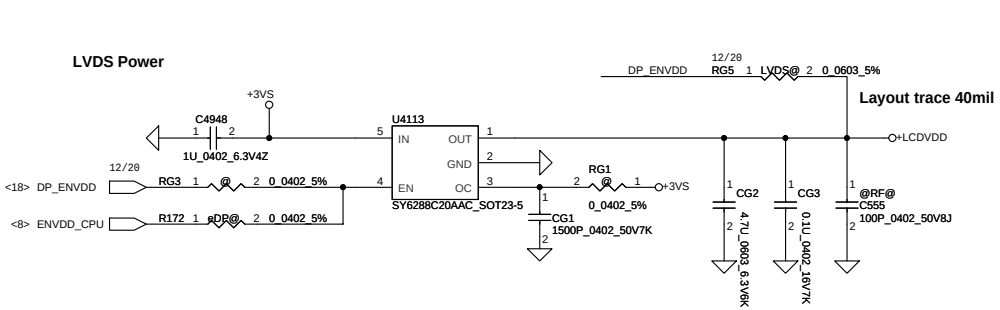
<RTS2132>
<PCH CTRL>
<LVDS Panel>
PD 100K on LVDS page

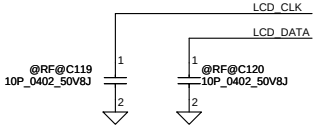
Different between 2132S and 2132R	
2132S	2132R
1. Support SWR mode	1. Support LDO mode and SWR mode 2. Internal ROM 3. Support LCD_VDD(internal Power switch) 4. Integrates Level shifter

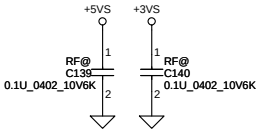
Security Classification	Compal Secret Data		
Issued Date	2013/3/1	Deciphered Date	2015/3/1

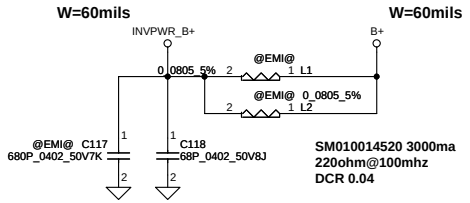
Compal Electronics, Inc.

Title: *LVDS Translator-RTD2132R*
Size: — Document Number: LA-B181P — Rev: 0.5
Date: Tuesday, March 25, 2014 — Sheet 18 of 62

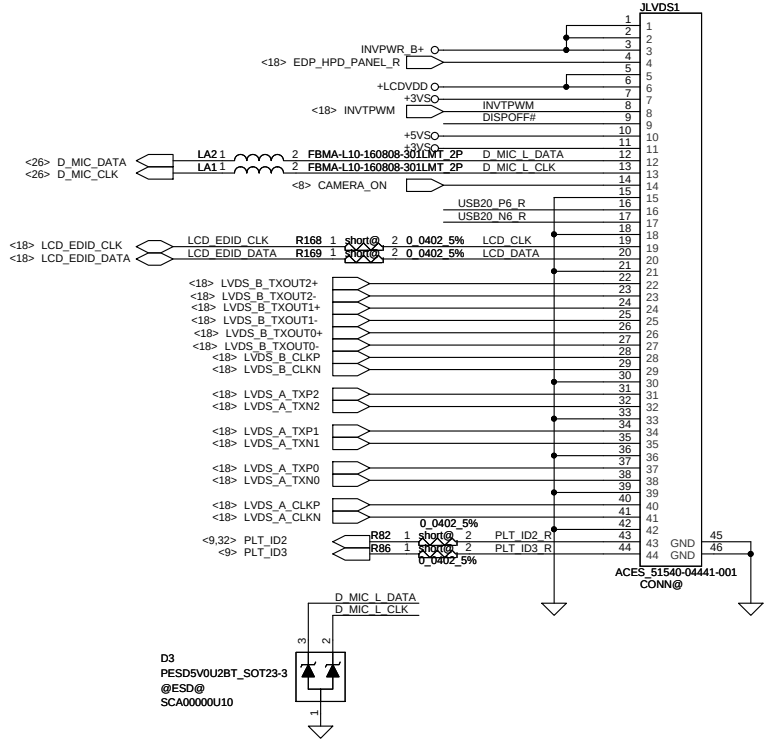




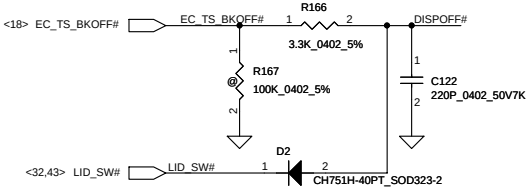


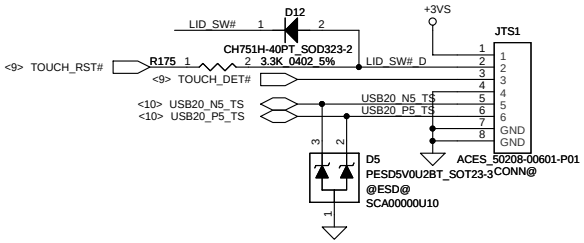


LCD/LED PANEL Conn.

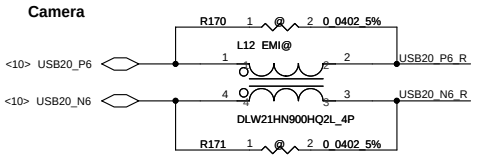


Touch





Camera



	GPIO92 PLT_ID2	GPIO93 PLT_ID3
Rolo 14"	0	1
Reeses 15"	1	0
Raisinet 17"	1	1

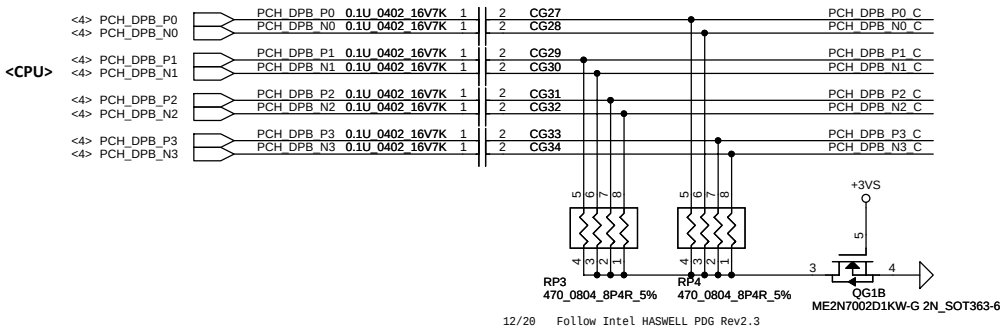
Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

Compal Electronics, Inc.

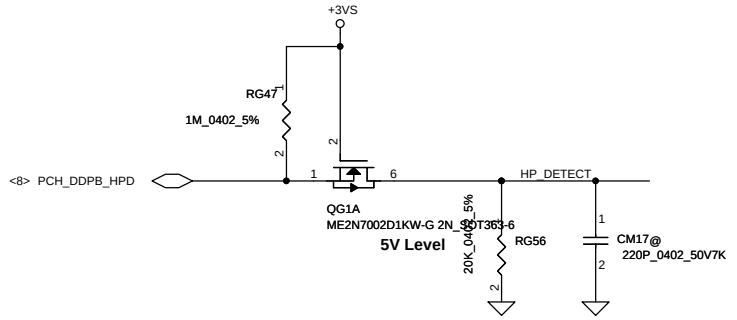
Title: LVDS Connector

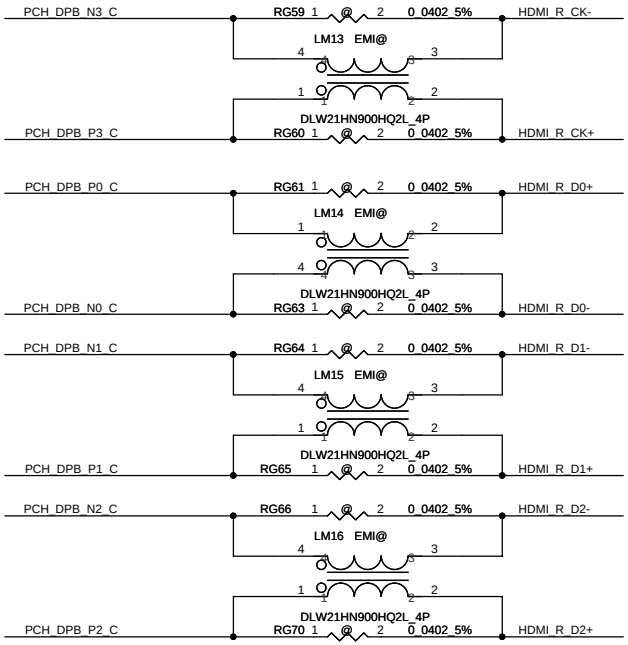
Size: | Document Number: LA-B181P | Rev: 0.5

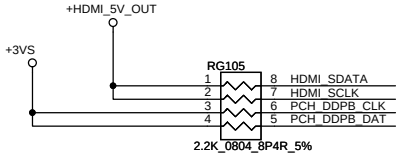
Date: Tuesday, March 25, 2014 | Sheet 19 of 62

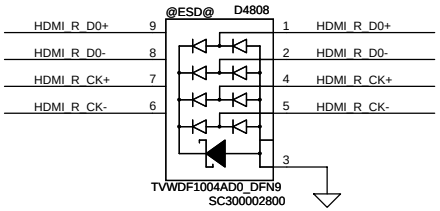


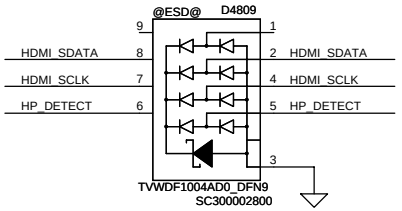
12/20 Follow Intel HASWELL PDG Rev2.3

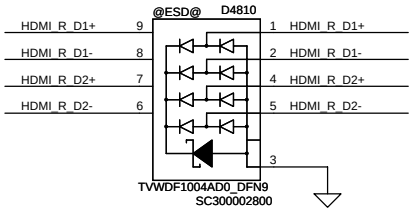


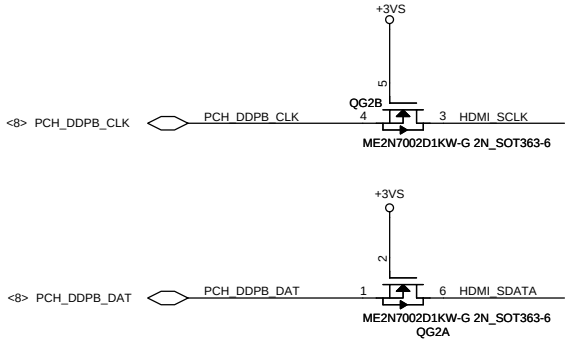






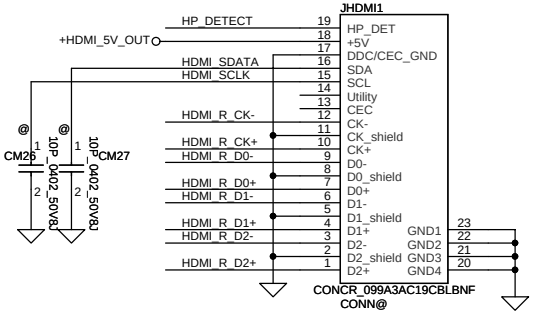


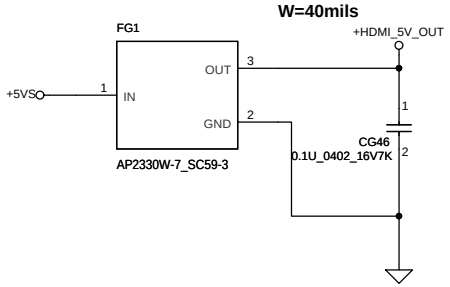




5V PULL UP IN CONNECTER SIDE

HDMI Conn.

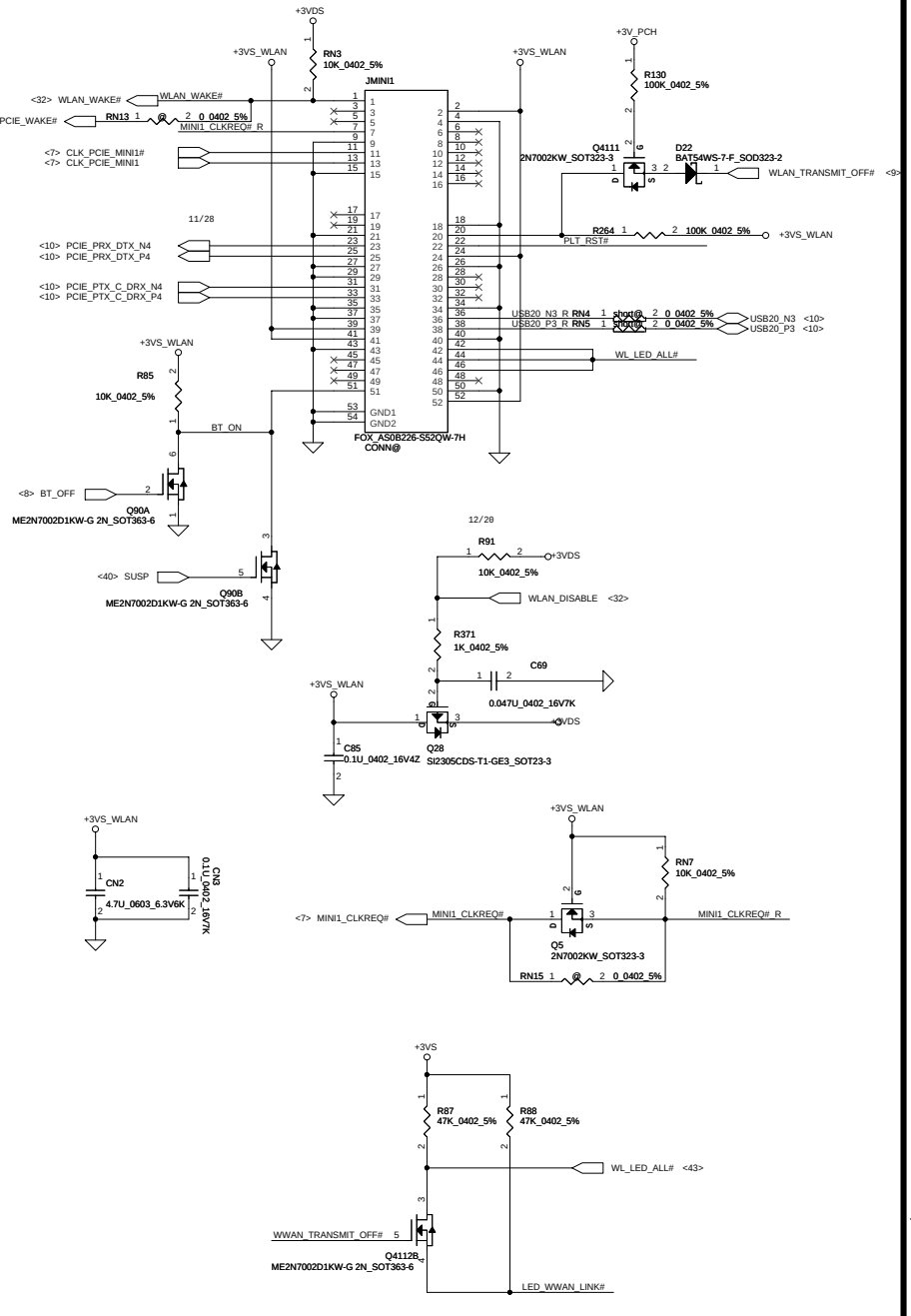




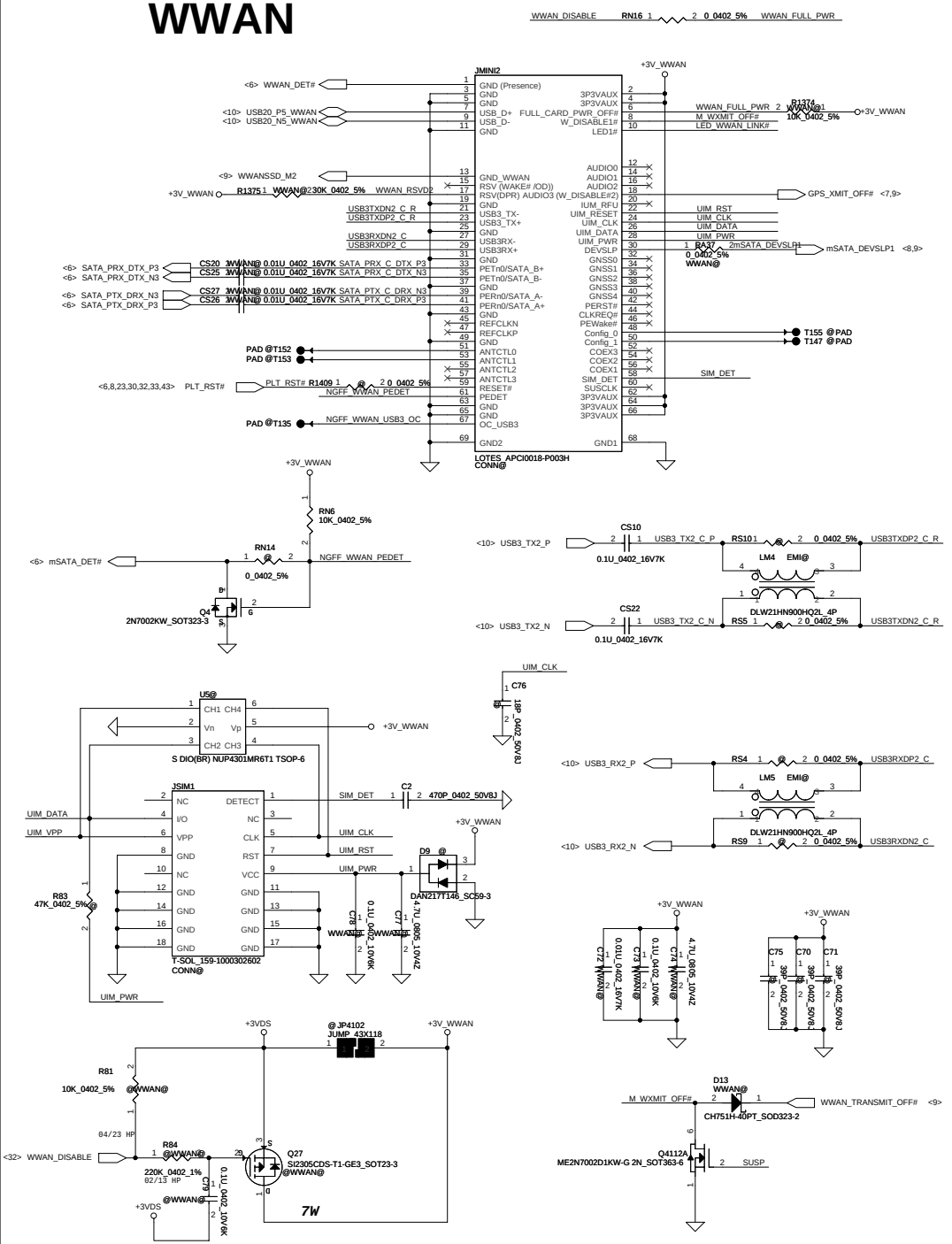
Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.	
Title	HDMI Conn/Level shift
Size	Document Number: LA-B181P
Rev	0.5
Date: Tuesday, March 25, 2014	Sheet 20 of 62

WLAN



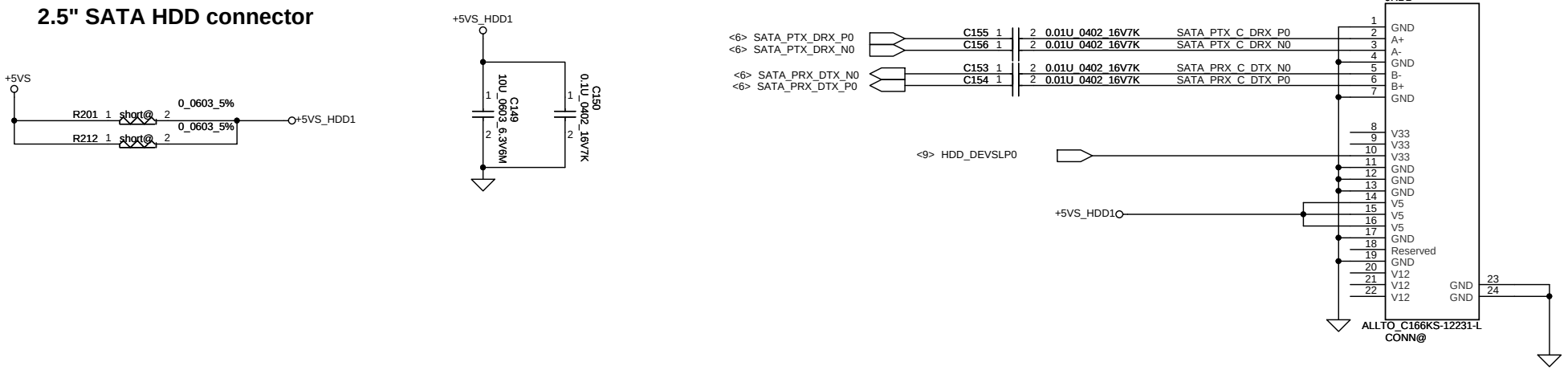
WWAN

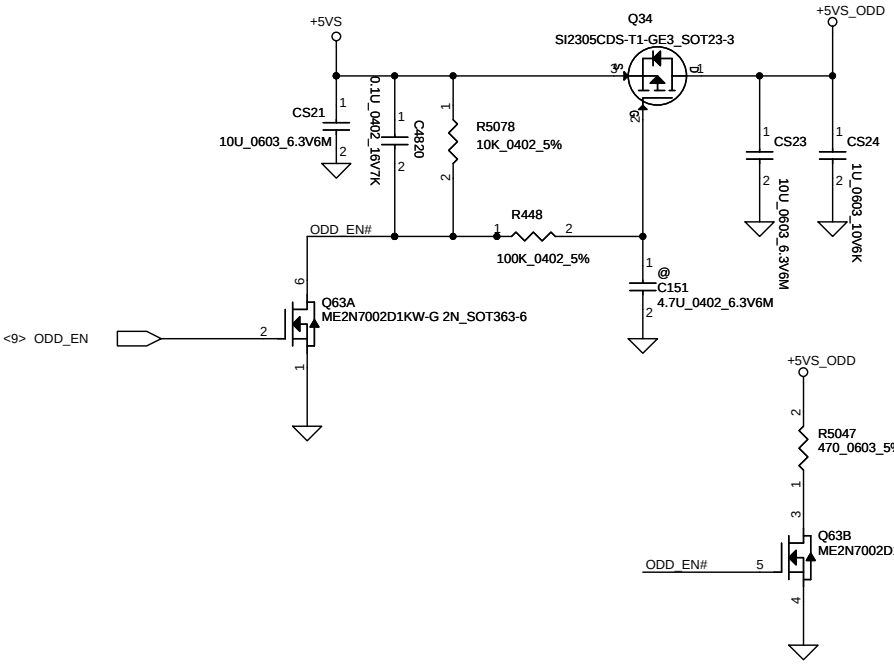


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/02/26	Deciphered Date	2015/07/08

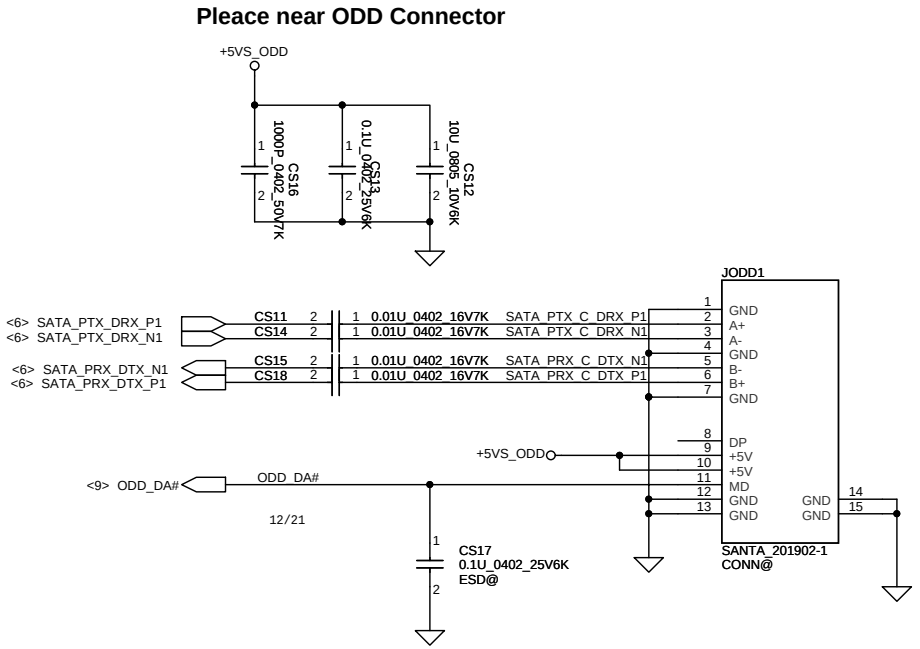
Title	WLAN		
Size	Document Number		Rev
	LA-B181P		0.5
Date:	Tuesday, March 25, 2014	Sheet	21 of 62

2.5" SATA HDD connector





Please near ODD Connector



12/20 Customer change GPIO table

Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: ODD/SATA Conn

Size: B | Document Number: LA-B181P | Rev: 0.5

Date: Tuesday, March 25, 2014 | Sheet 22 of 62

+LAN_VDD_3V3 Rising time need>0.5mS and <100mS

CL8& CL9 close to UL1: Pin 23

CL22 & CL23 close to UL1: Pin 11,32

CL24 close to UL1: Pin 32

CL25 close to UL1: Pin 11

CL12 & CL13 close LL2

CL17 & CL18 close UL1 Pin22

CL19 & CL20 close UL1 Pin30

Place CL14~CL16 close UL1 Pin 3, 8 , 22

+LAN_VDD_3V3=40mil

+VDDREG=40mil

+LAN_REGOUT=60mil

SP050005L00 Footprint

RJ-45 CONN.

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/02/26	Deciphered Date 2011/06/29	Title: LAN RTL8161GSH
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Size: Document Number: LA-B181P Rev: 0.5
			Date: Tuesday, March 25, 2014 Sheet 23 of 62

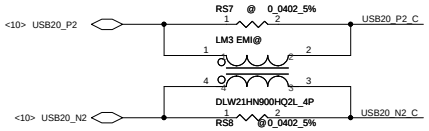
Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

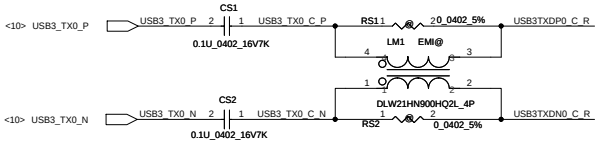
Title: ***Card Reader RTS5237***

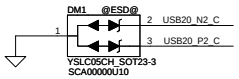
Size	Document Number	Rev
Custom	LA-B181P	0.5

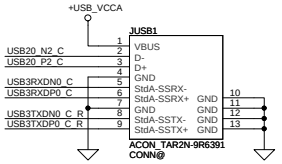
Date: Tuesday, March 25, 2014 | Sheet 24 of 62

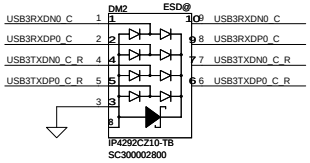
USB3.0

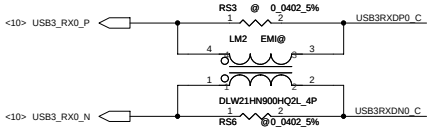




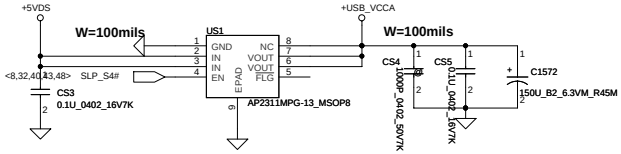


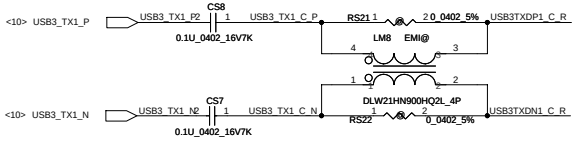


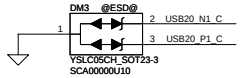


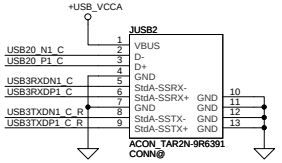


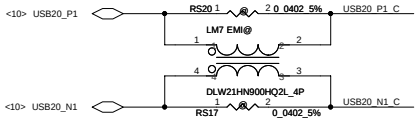
USB3.0 need support 2.5A
change USB PWR SW SA00003TV00
low active

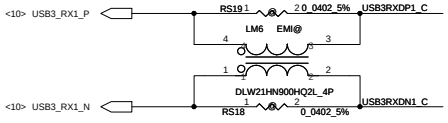


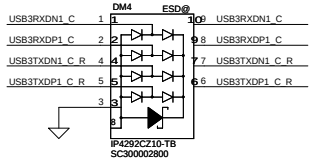




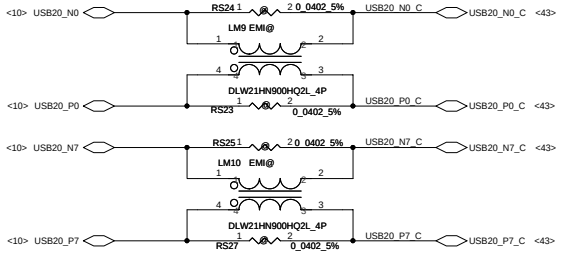




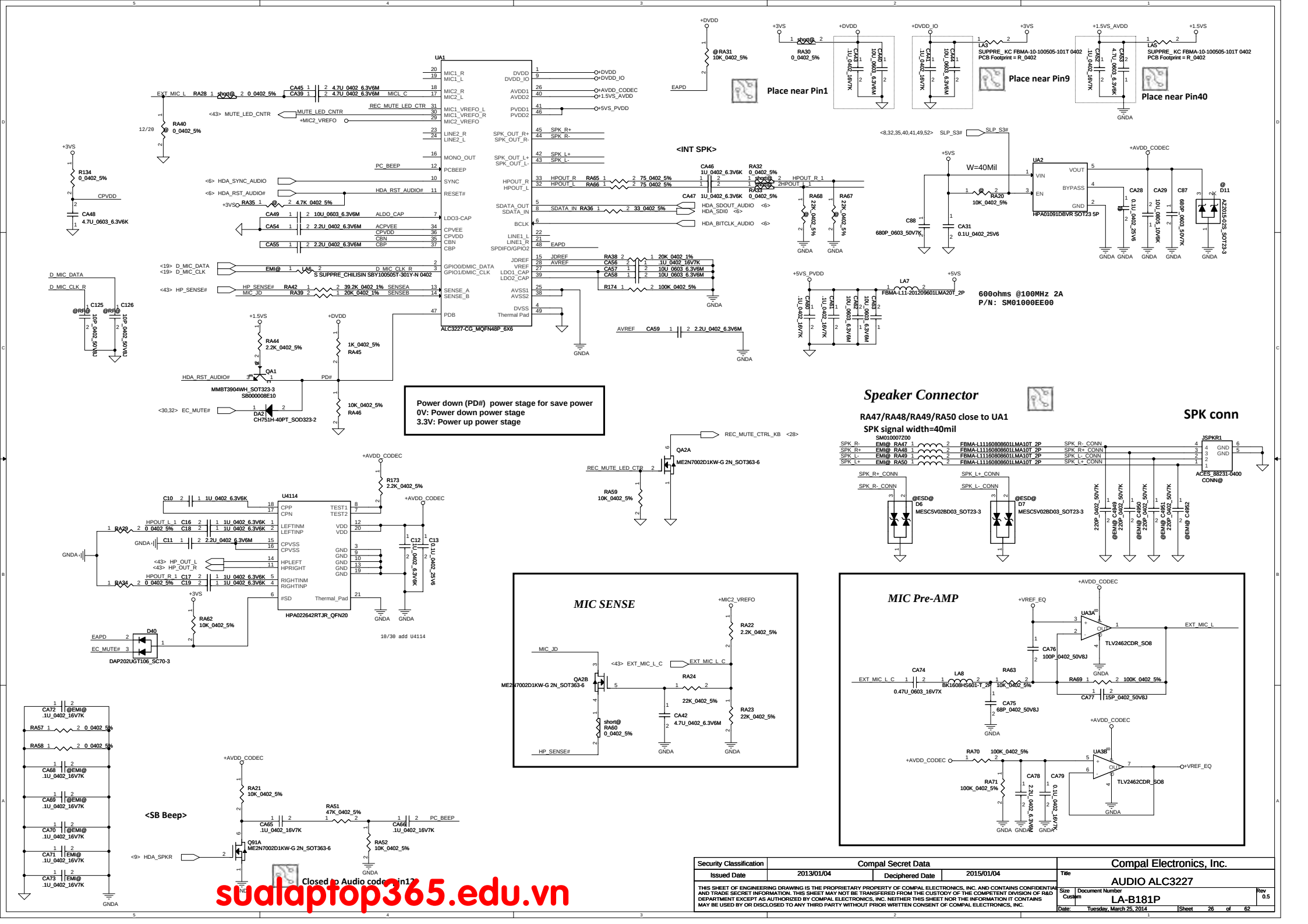




USB2.0



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/02/26	Deciphered Date 2015/07/08	Title: USB 3.0
			Size: C; Document Number: LA-B181P; Rev: 0.5
			Date: Tuesday, March 25, 2014; Sheet 25 of 62



Security Classification	Compal Secret Data		
Issued Date	2013/01/04	Deciphered Date	2015/01/04

Compal Electronics, Inc.

Title: AUDIO ALC3227

Size: Custom | Document Number: LA-B181P | Rev: 0.5

Date: Tuesday, March 25, 2014 | Sheet 26 of 62

Security Classification	Compal Secret Data		
Issued Date	2012/03/23	Deciphered Date	2012/10/21

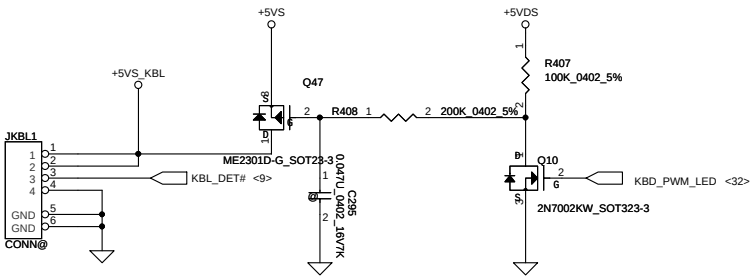
Compal Electronics, Inc.

Title: Audio SPK Conn/Jack/MIC

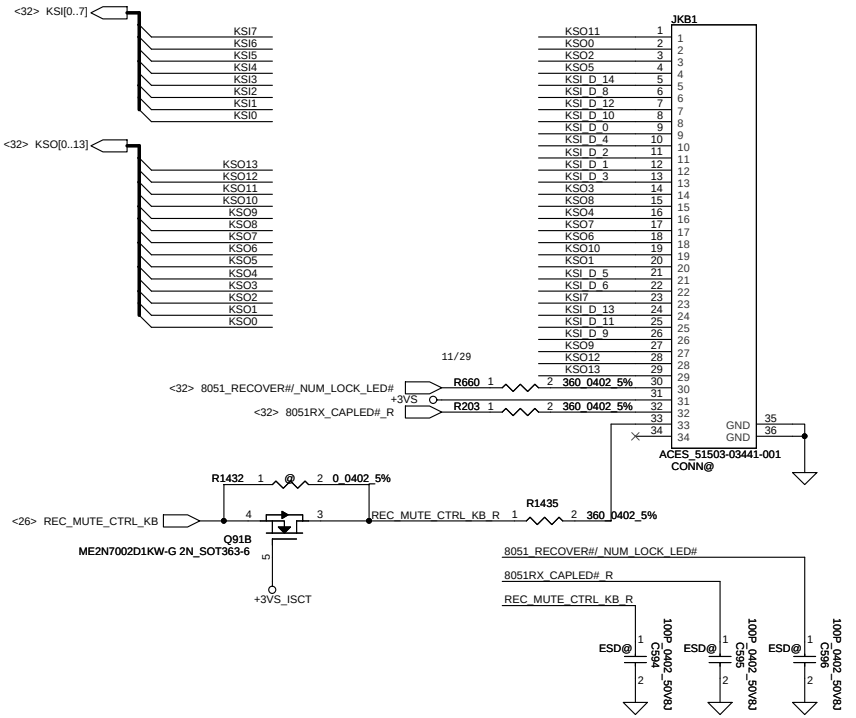
Size	Document Number	Rev
C	LA-B181P	0.5

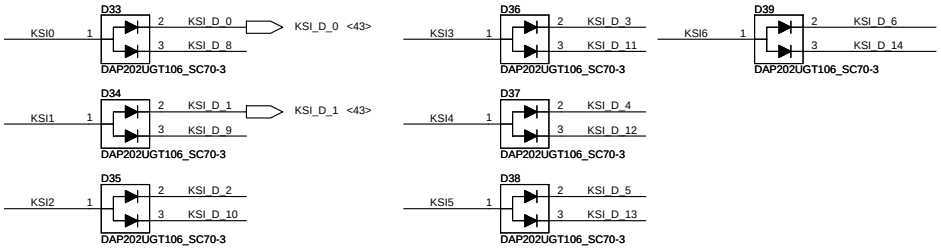
Date: Tuesday, March 25, 2014 | Sheet 27 of 62

KB backlight Conn



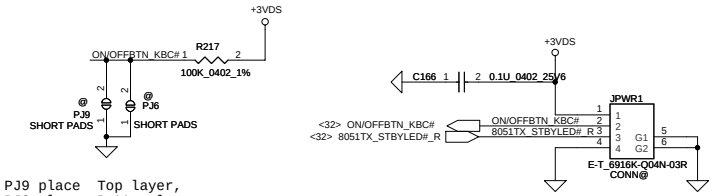
Keyboard conn





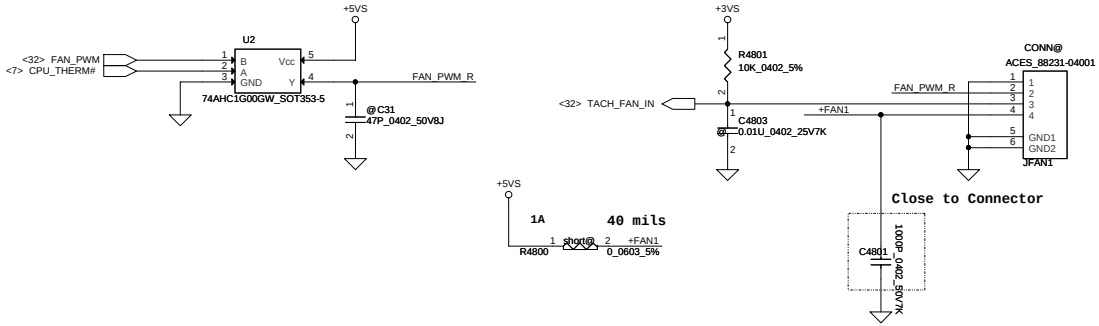
Compal Electronics, Inc.	
Title	KB/TP
Size: Custom	Document Number: LA-B181P
Rev	0.5
Date: Tuesday, March 25, 2014	Sheet 28 of 62

Power Button Connector



PJ9 place Top layer,
PJ6 place Bottom layer

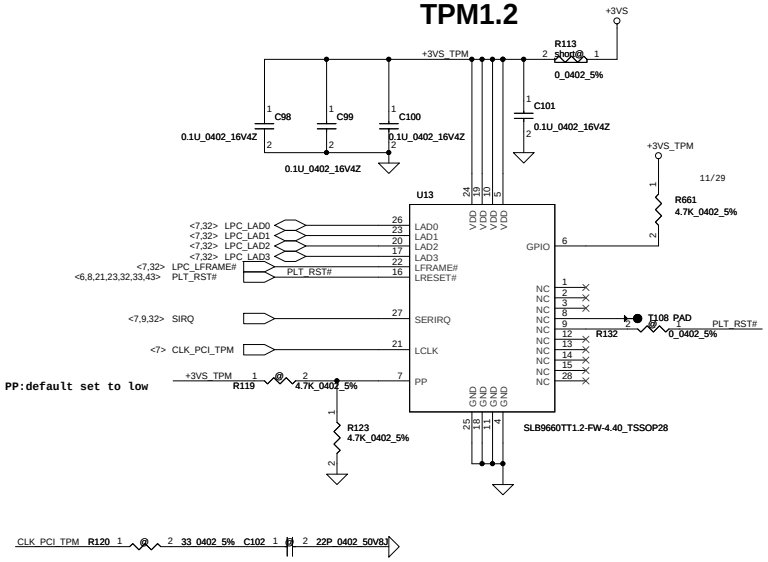
Fan Control Circuit



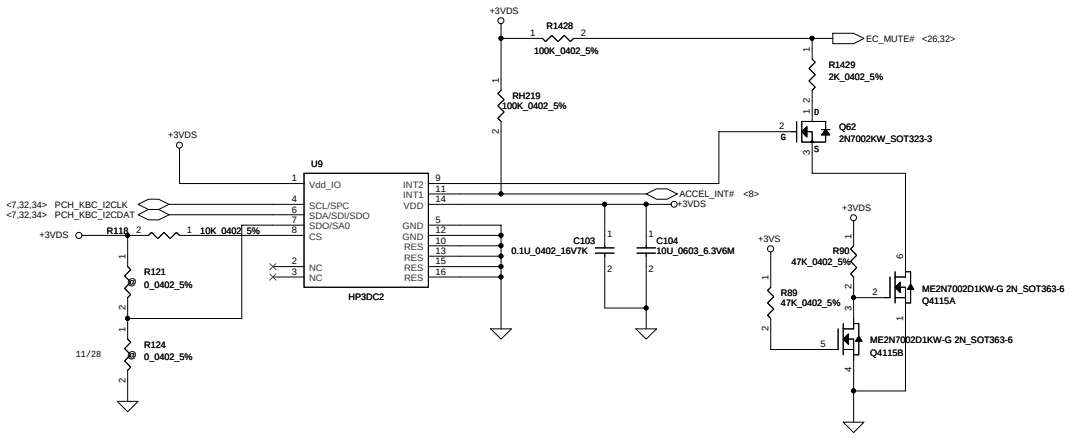
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/02/26	Deciphered Date 2015/07/08	Title PWRBTN/FAN

Size Custom	Document Number LA-B181P		Rev 0.5
Date: Tuesday, March 25, 2014	Sheet 29 of 62		

TPM1.2

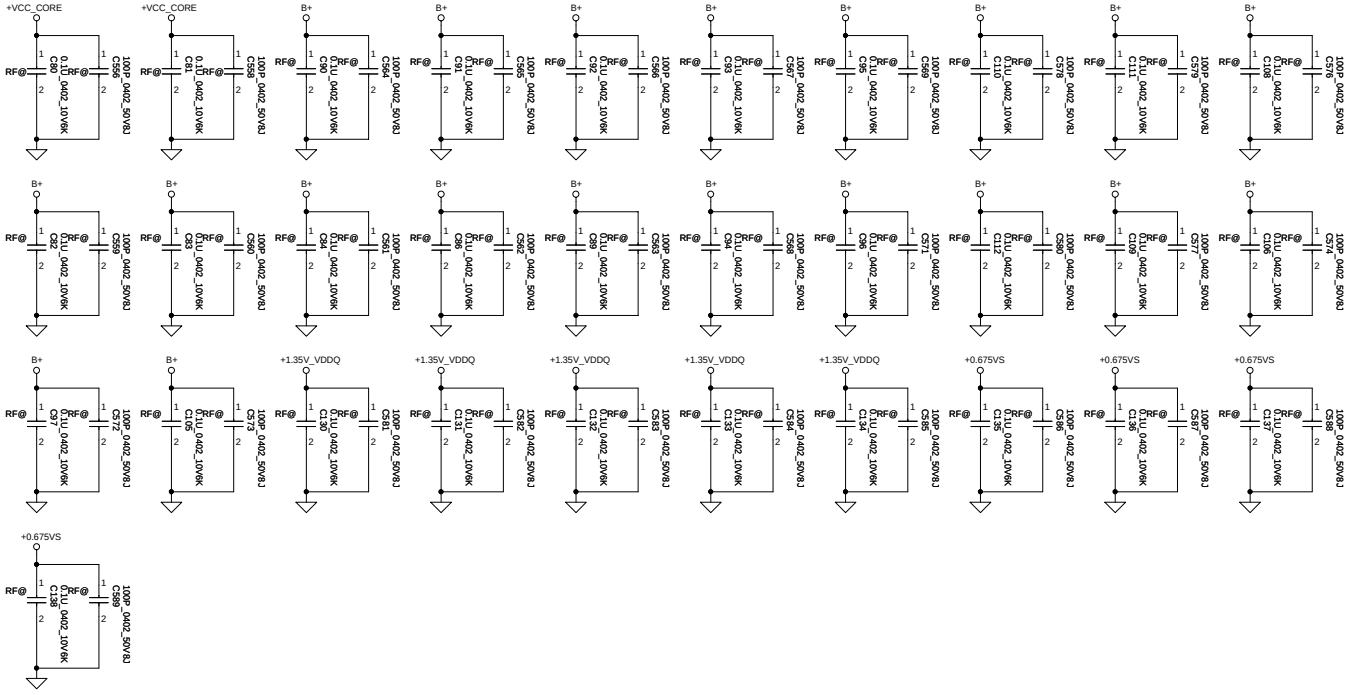


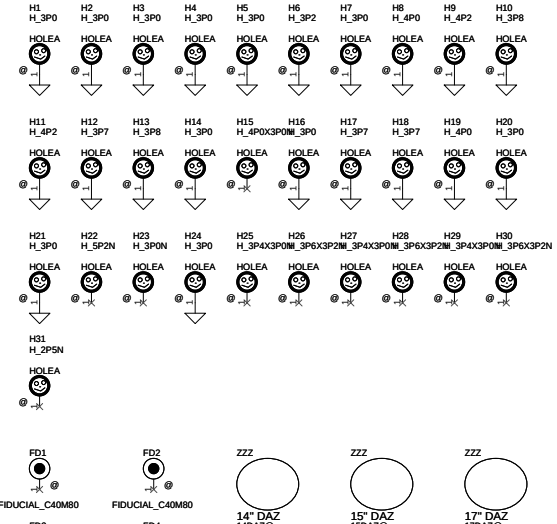
ACCELEROMETER



CLK_PCI_TPM R120 33_0402_5% C102 22P_0402_50V8J

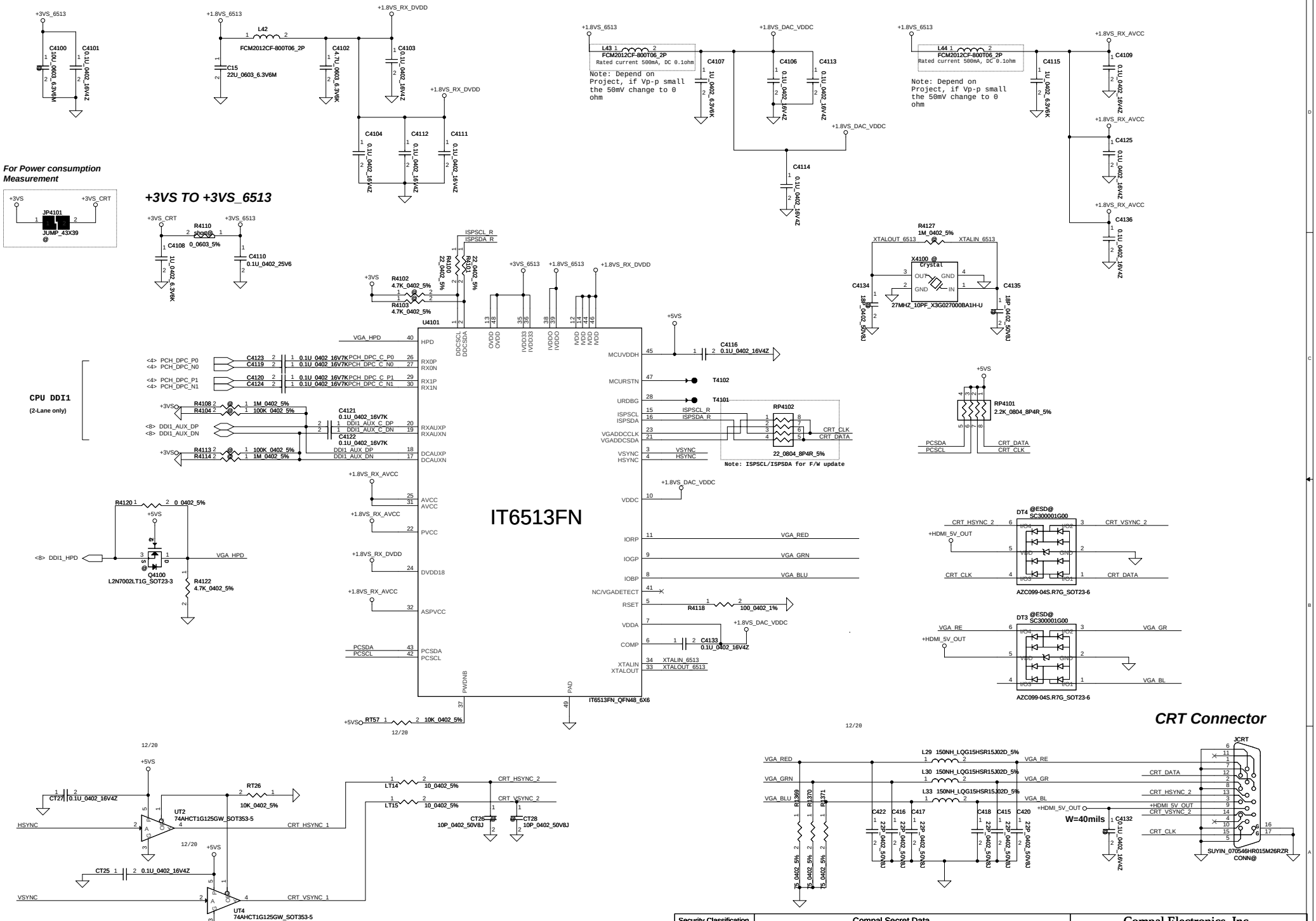
RF CAP

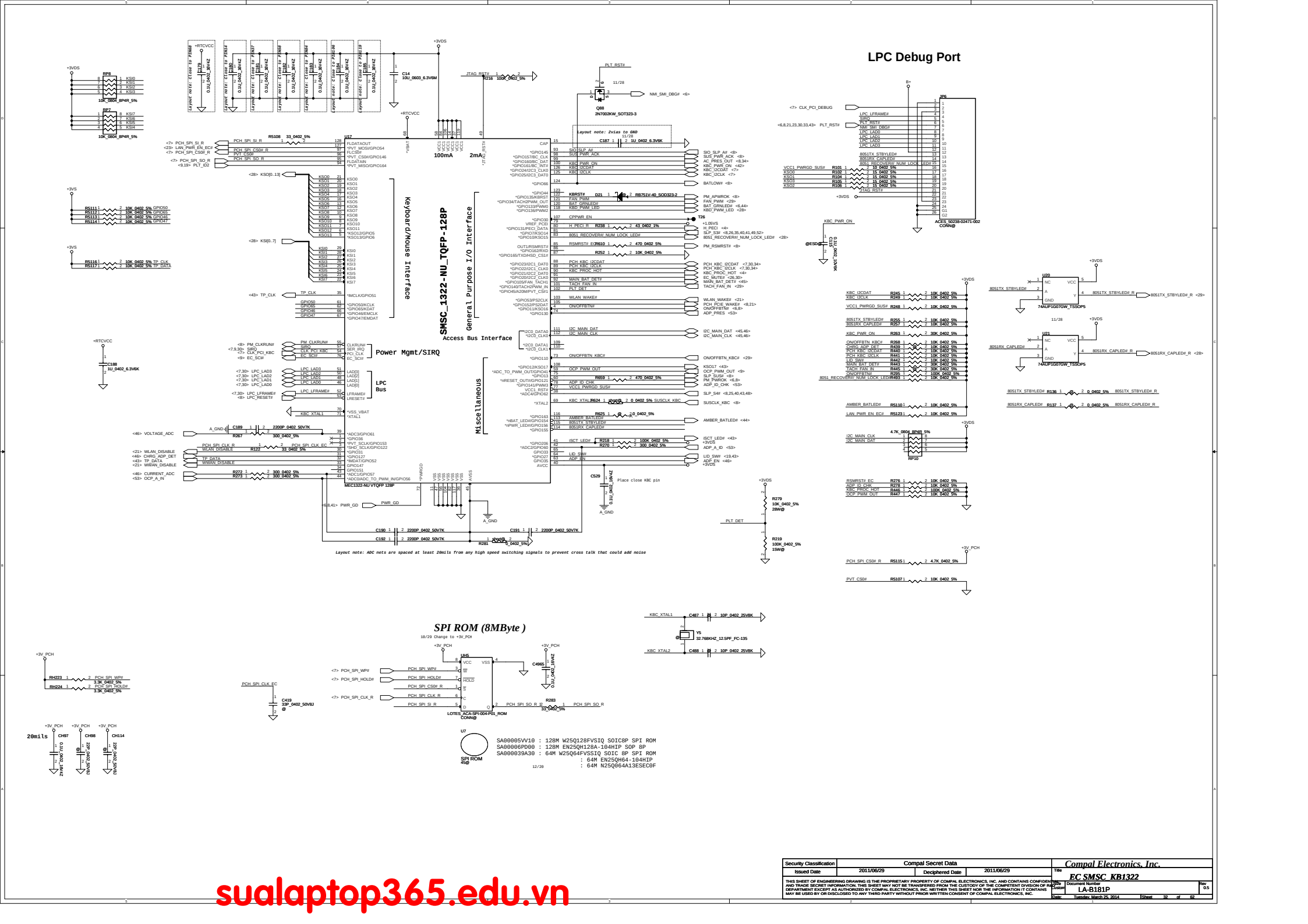


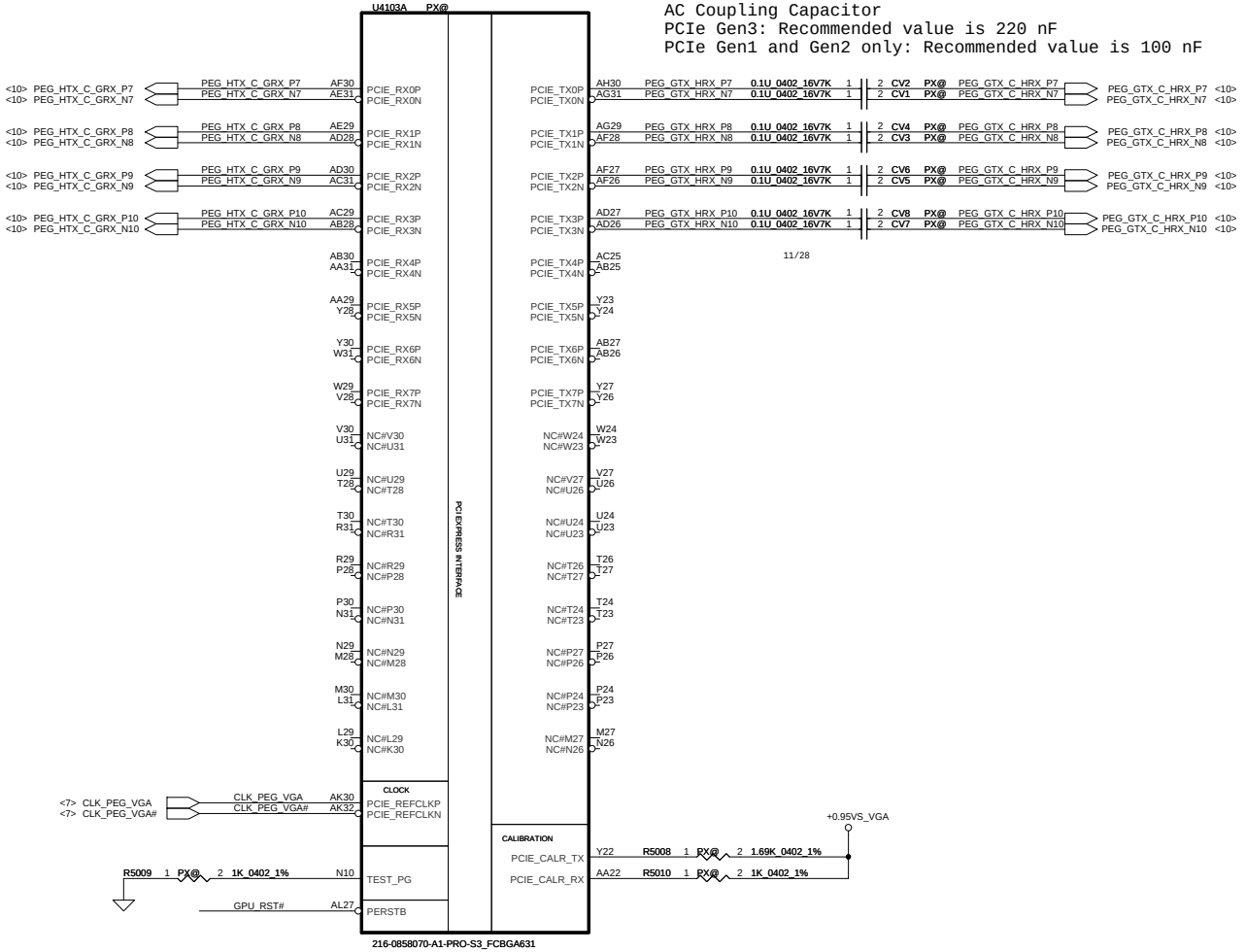


Security Classification	Compal Secret Data		
Issued Date	2013/02/26	Deciphered Date	2015/07/08

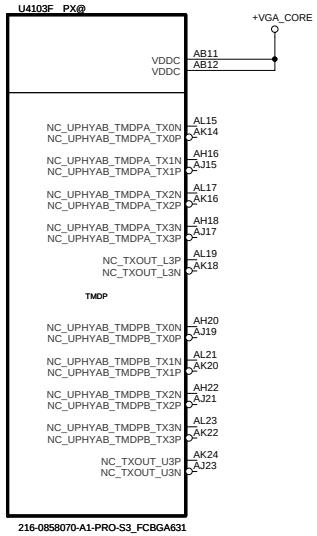
Compal Electronics, Inc.			
Title	LED/Screw hole		
Size	Document Number	LA-B181P	Rev 0.5
Date:	Tuesday, March 25, 2014	Sheet 30 of 62	

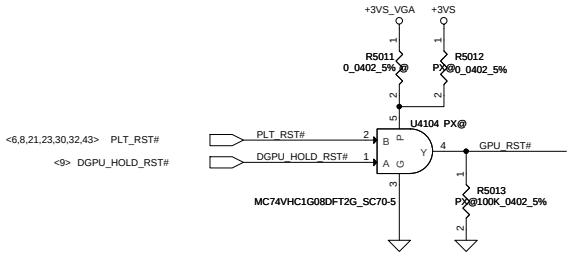


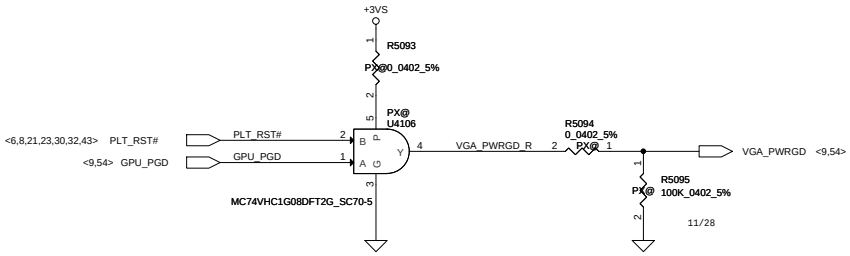




No Use GPU Display Port outpud







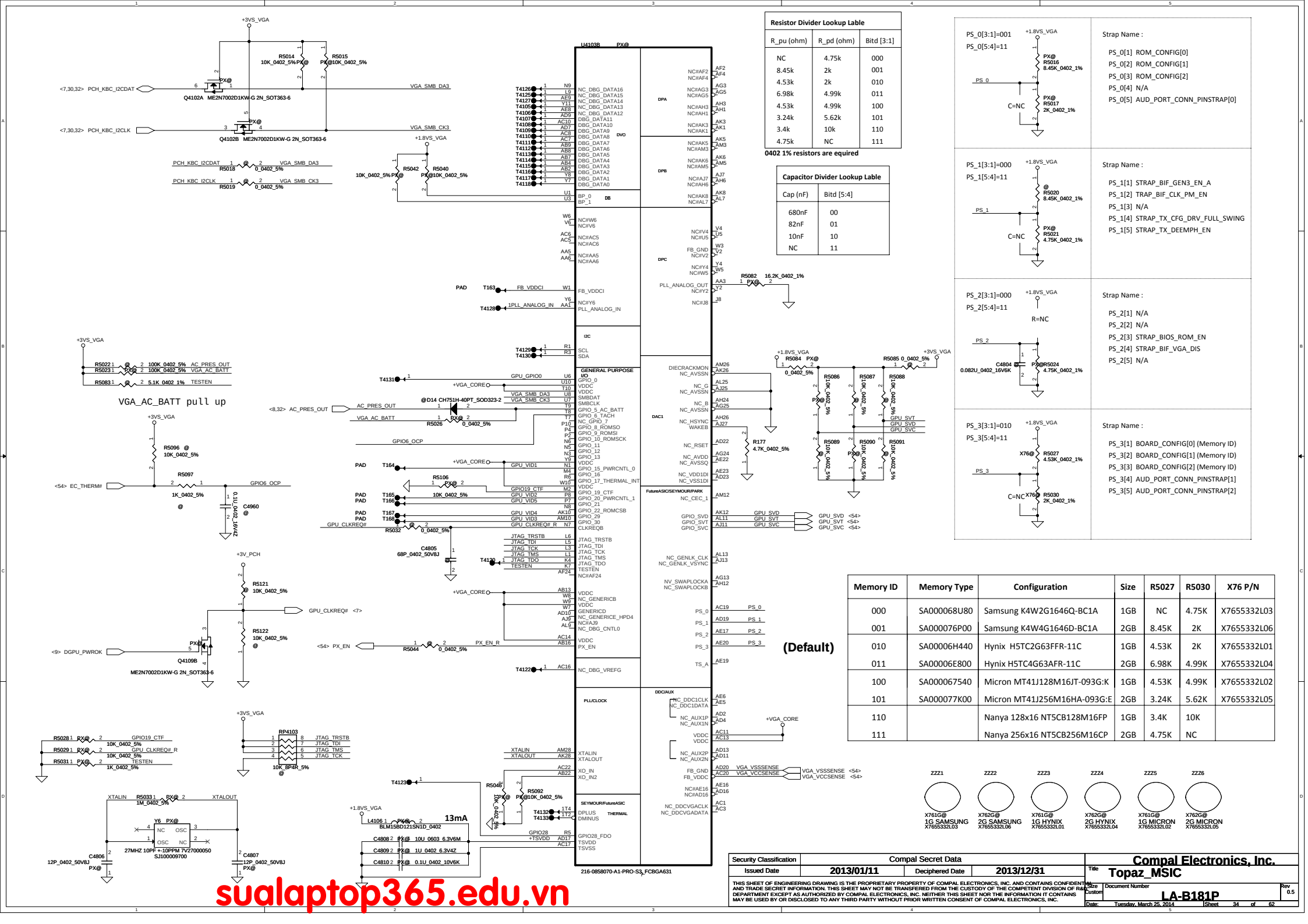
Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

Compal Electronics, Inc.

Title: Topaz_PCIE/DP

Size: Custom | Document Number: LA-B181P | Rev: 0.5

Date: Tuesday, March 25, 2014 | Sheet 33 of 62



Resistor Divider Lookup Lable		
R_pu (ohm)	R_pd (ohm)	Bitd [3:1]
NC	4.75k	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

0402 1% resistors are equired

Capacitor Divider Lookup Lable	
Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11

PS_0[3:1]=001, PS_0[5:4]=11 — PS_0 — R5016 8.45K_0402_1% / R5017 2K_0402_1% — C=NC

Strap Name :
- PS_0[1] ROM_CONFIG[0]
- PS_0[2] ROM_CONFIG[1]
- PS_0[3] ROM_CONFIG[2]
- PS_0[4] N/A
- PS_0[5] AUD_PORT_CONN_PINSTRAP[0]

PS_1[3:1]=000, PS_1[5:4]=11 — PS_1 — R5020 8.45K_0402_1% / R5021 4.75K_0402_1% — C=NC

Strap Name :
- PS_1[1] STRAP_BIF_GEN3_EN_A
- PS_1[2] TRAP_BIF_CLK_PM_EN
- PS_1[3] N/A
- PS_1[4] STRAP_TX_CFG_DRV_FULL_SWING
- PS_1[5] STRAP_TX_DEEMPH_EN

PS_2[3:1]=000, PS_2[5:4]=11 — R=NC — PS_2 — C4804 0.082U_0402_16V6K — R5024 4.75K_0402_1%

Strap Name :
- PS_2[1] N/A
- PS_2[2] N/A
- PS_2[3] STRAP_BIOS_ROM_EN
- PS_2[4] STRAP_BIF_VGA_DIS
- PS_2[5] N/A

PS_3[3:1]=010, PS_3[5:4]=11 — PS_3 — X76@ R5027 4.53K_0402_1% / C=NC X76@ R5030 2K_0402_1%

Strap Name :
- PS_3[1] BOARD_CONFIG[0] (Memory ID)
- PS_3[2] BOARD_CONFIG[1] (Memory ID)
- PS_3[3] BOARD_CONFIG[2] (Memory ID)
- PS_3[4] AUD_PORT_CONN_PINSTRAP[1]
- PS_3[5] AUD_PORT_CONN_PINSTRAP[2]

Memory ID	Memory Type	Configuration	Size	R5027	R5030	X76 P/N
000	SA000068U80	Samsung K4W2G1646Q-BC1A	1GB	NC	4.75K	X7655332L03
001	SA000076P00	Samsung K4W4G1646D-BC1A	2GB	8.45K	2K	X7655332L06
010	SA00006H440	Hynix H5TC2G63FFR-11C	1GB	4.53K	2K	X7655332L01
011	SA00006E800	Hynix H5TC4G63AFR-11C	2GB	6.98K	4.99K	X7655332L04
100	SA000067540	Micron MT41J128M16JT-093G:K	1GB	4.53K	4.99K	X7655332L02
101	SA000077K00	Micron MT41J256M16HA-093G:E	2GB	3.24K	5.62K	X7655332L05
110		Nanya 128x16 NT5CB128M16FP	1GB	3.4K	10K	
111		Nanya 256x16 NT5CB256M16CP	2GB	4.75K	NC	

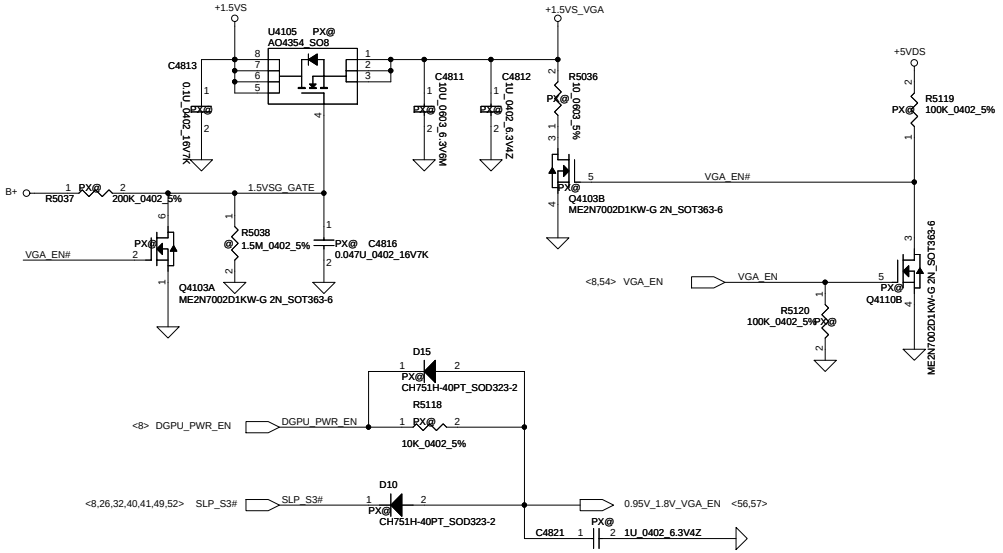
ZZZ1 X761G@ 1G SAMSUNG X7655332L03
ZZZ2 X762G@ 2G SAMSUNG X7655332L06
ZZZ3 X761G@ 1G HYNIX X7655332L01
ZZZ4 X762G@ 2G HYNIX X7655332L04
ZZZ5 X761G@ 1G MICRON X7655332L02
ZZZ6 X762G@ 2G MICRON X7655332L05

Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

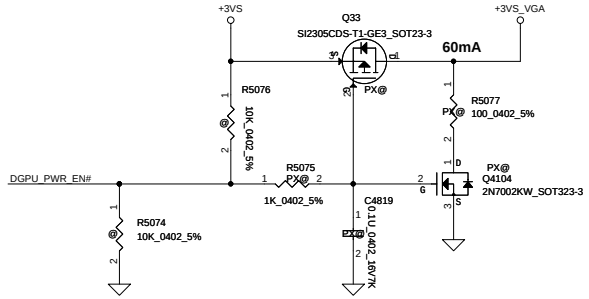
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

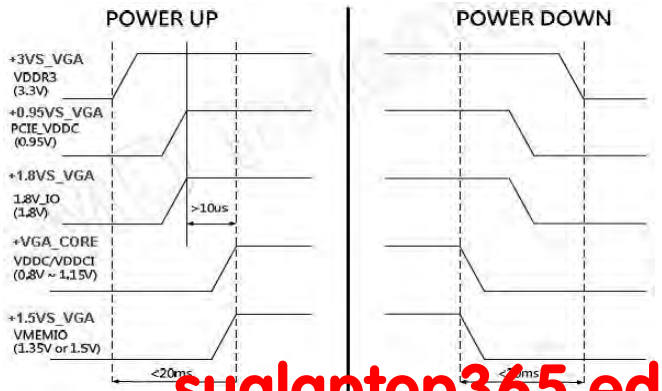
Compal Electronics, Inc.
Title: Topaz_MSIC
Size: Custom | Document Number: LA-B181P | Rev: 0.5
Date: Tuesday, March 25, 2014 | Sheet 34 of 62

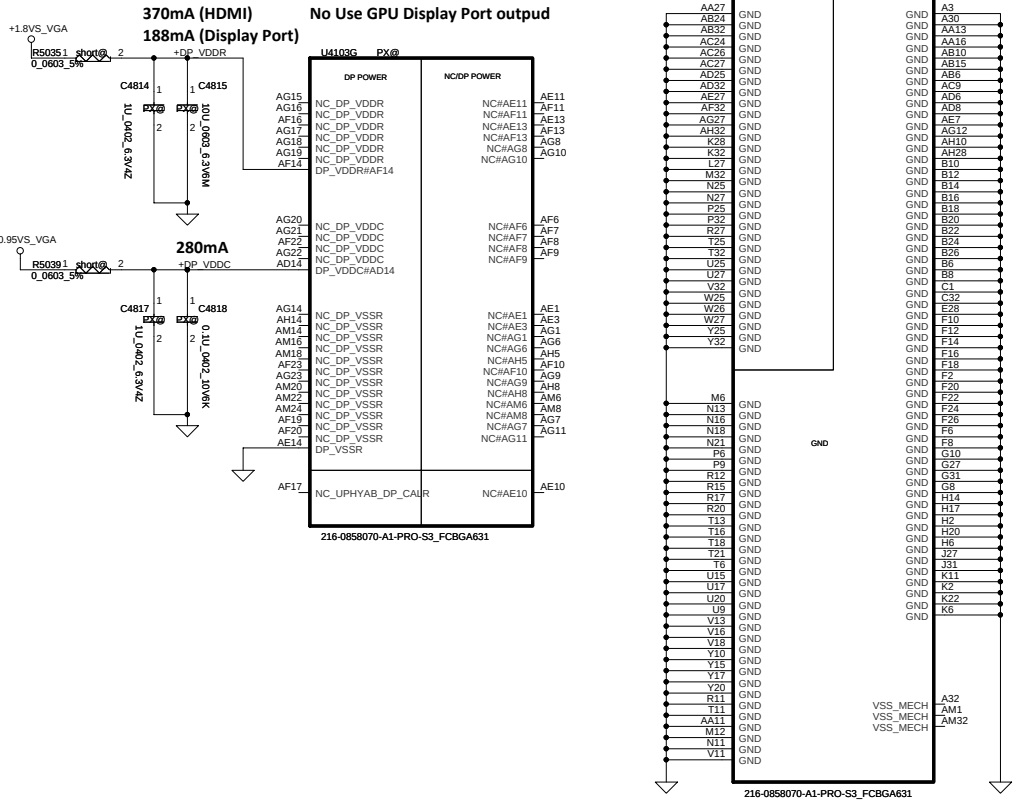
+1.5VS to +1.5VS_VGA (2.096A)

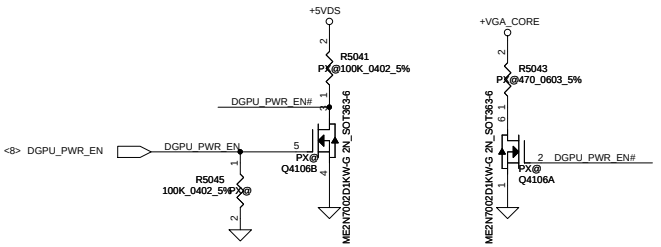


+3VS to +3VS_VGA (25mA)









Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

Compal Electronics, Inc.

Title: **Topaz_Power/GND**

Size: Custom | Document Number: **LA-B181P** | Rev: 0.5

Date: Tuesday, March 25, 2014 | Sheet 35 of 62

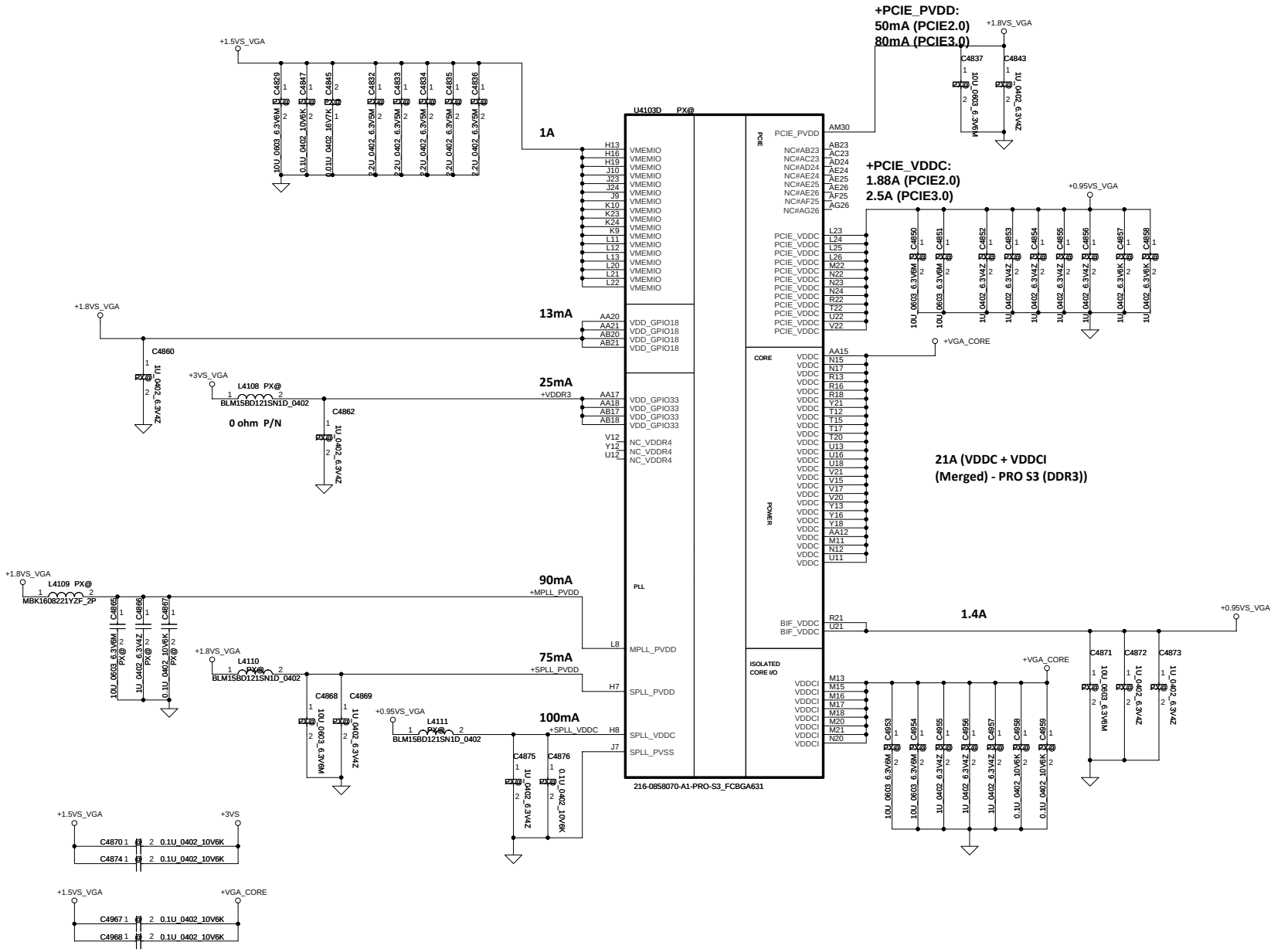
+VGA_CORE		10uF	1uF	0.1uF
VDDC	TBD	5 (1@)	10 (2@)	0
VDDCI	3.5A	1	3	0

+0.95VS_VGA		10uF	1uF	0.1uF
PCIE_VDDC	2.5A	2 (1@)	5 (1@)	0
BIF_VDDC	1.4A	0	0	0
SPLL_VDDC	100mA	1	1	1

+1.5VS_VGA		10uF	1uF	0.1uF
VDDR1	1.5A	3	5	5

+1.8VS_VGA		10uF	1uF	0.1uF
PCIE_PVDD	100mA	1	1	1
MPLL_PVDD	130mA	1	1	1
SPLL_PVDD	75mA	1	1	1
VDDR4	(300mA)	0	0	0
VDD_CT	13mA	1	1	1
+TSVDD	13mA	1	1	1
+DP_VDDR		0	0	0
+DP_VDDC		0	0	0

+3VS_VGA		10uF	1uF	0.1uF
VDDR3	25mA	0	2 (1@)	1



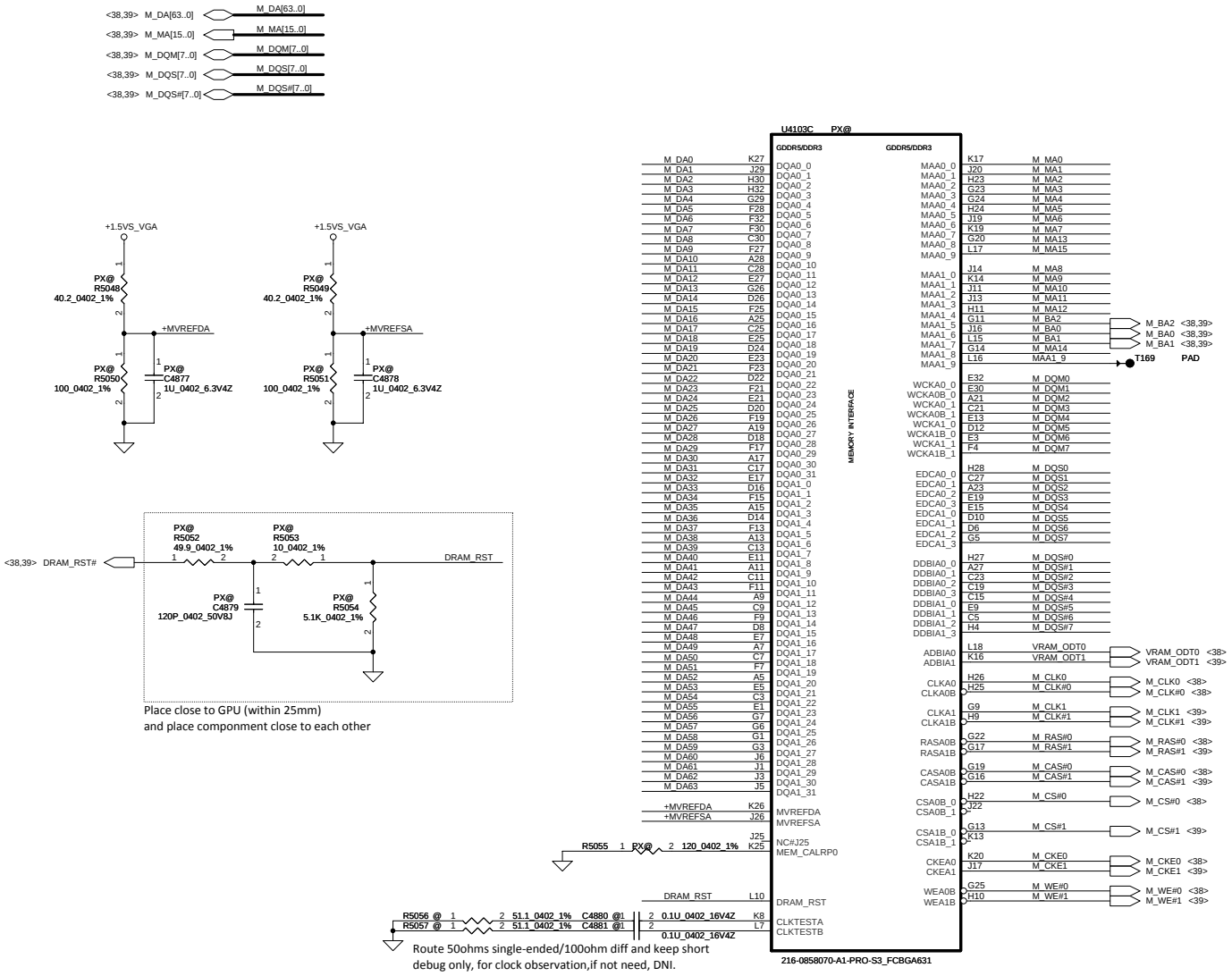
Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

Compal Electronics, Inc.

Title: Topaz_Power

Size: Custom | Document Number: LA-B181P | Rev: 0.5

Date: Tuesday, March 25, 2014 | Sheet 36 of 62



Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

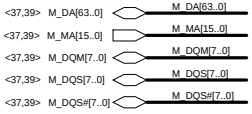
Compal Electronics, Inc.

Title: Topaz_MEM

Size: Custom | Document Number: LA-B181P | Rev: 0.5

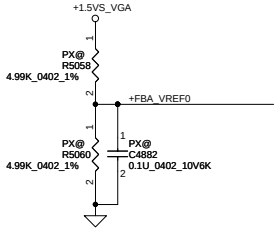
Date: Tuesday, March 25, 2014 | Sheet 37 of 62

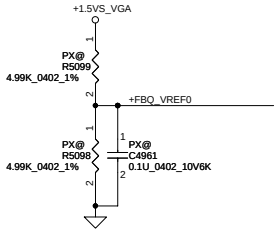
Memory Partition A - Lower 32 bits

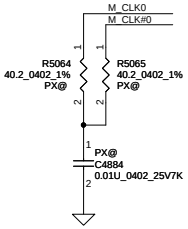


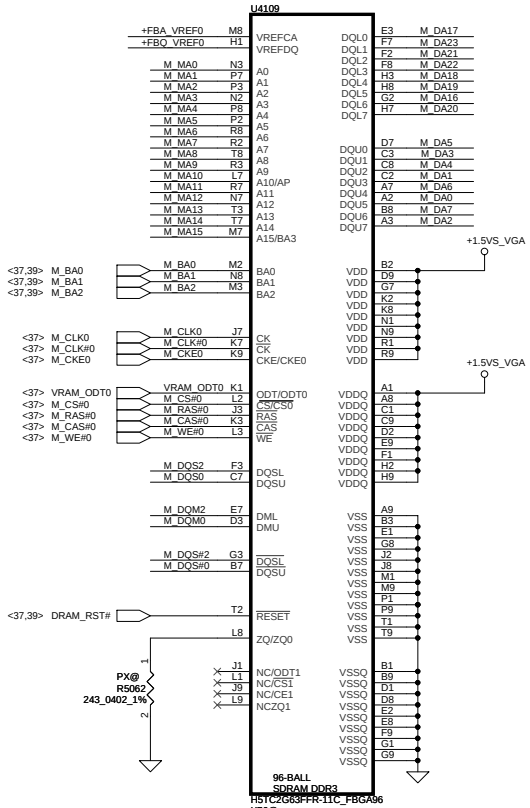
UH1 @Hynix

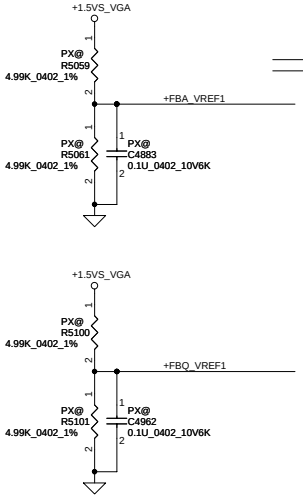
UM1 @Micron

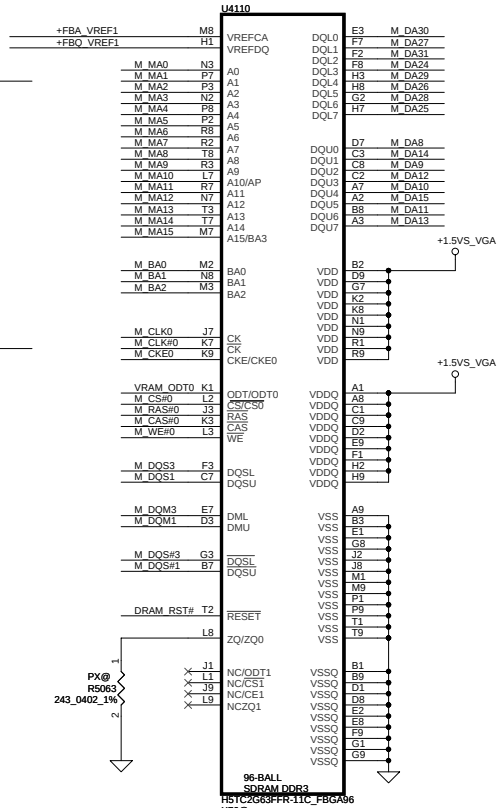


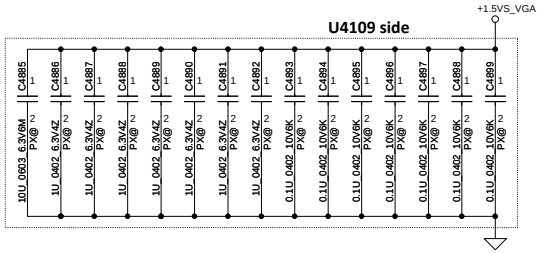


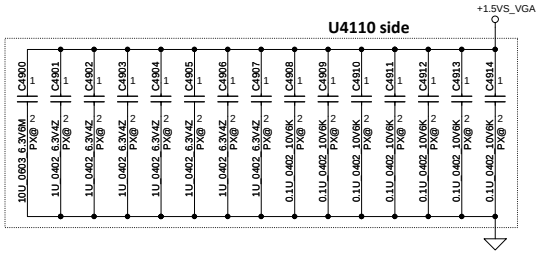












Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

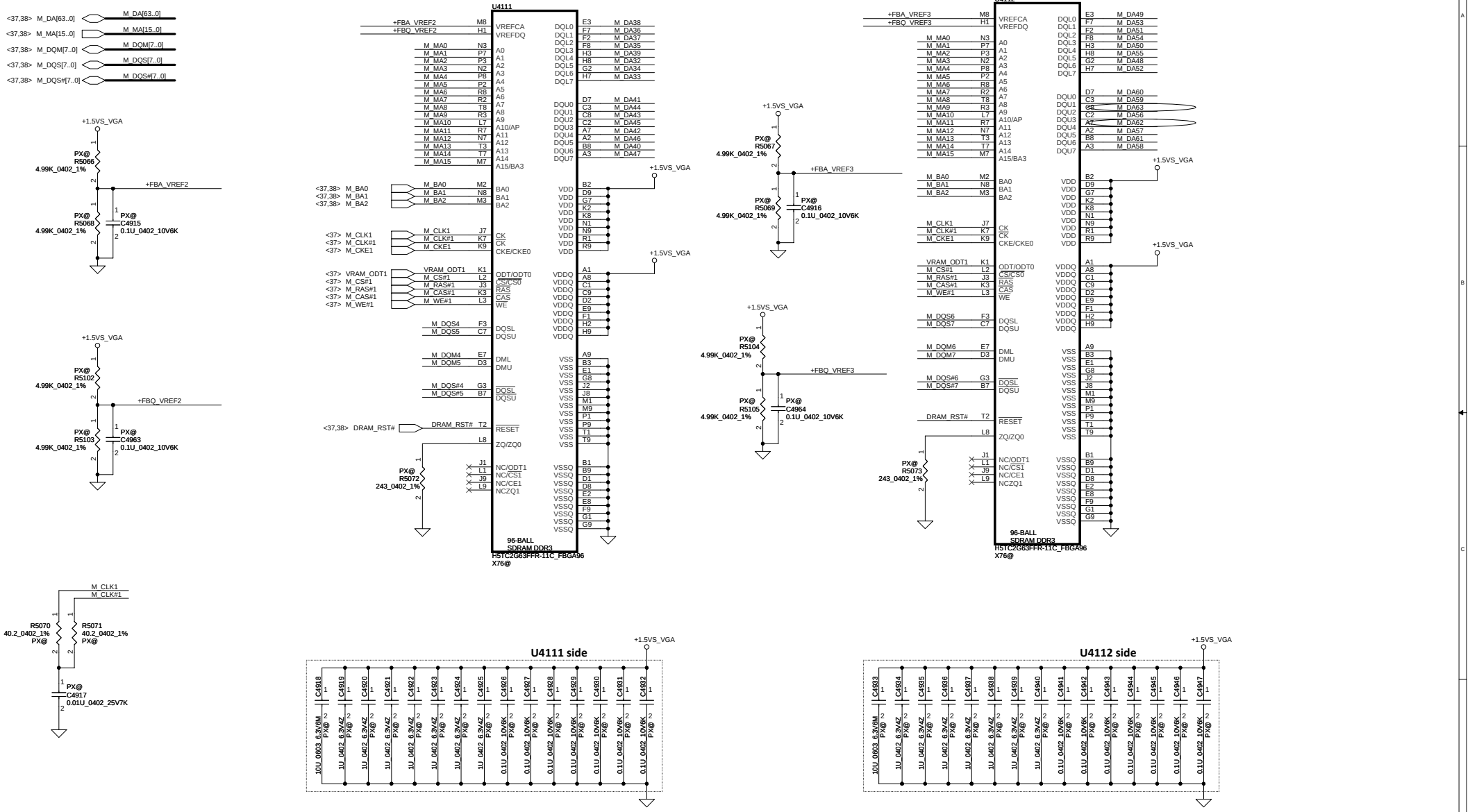
Compal Electronics, Inc.

Title: Topaz_VRAM A Lower

Size: Custom | Document Number: LA-B181P | Rev: 0.5

Date: Tuesday, March 25, 2014 | Sheet 38 of 62

Memory Partition A - Upper 32 bits



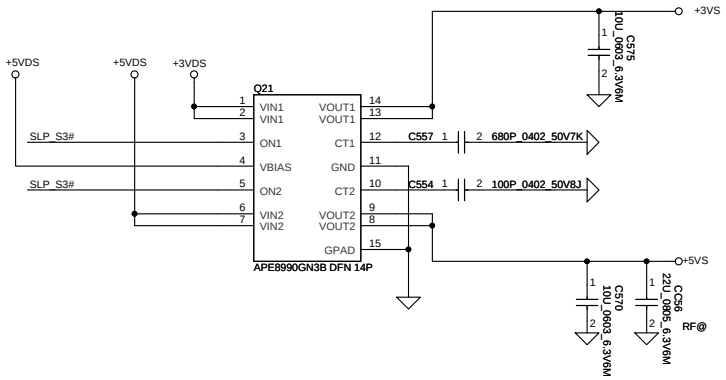
Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

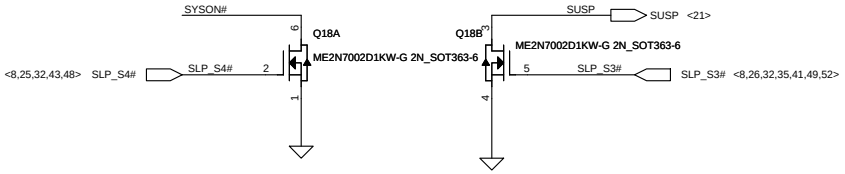
Compal Electronics, Inc.

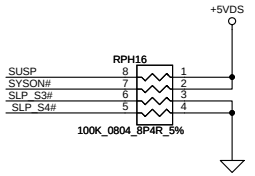
Title: **Topaz_VRAM A Upper**

Size: Custom | Document Number: **LA-B181P** | Rev: 0.5

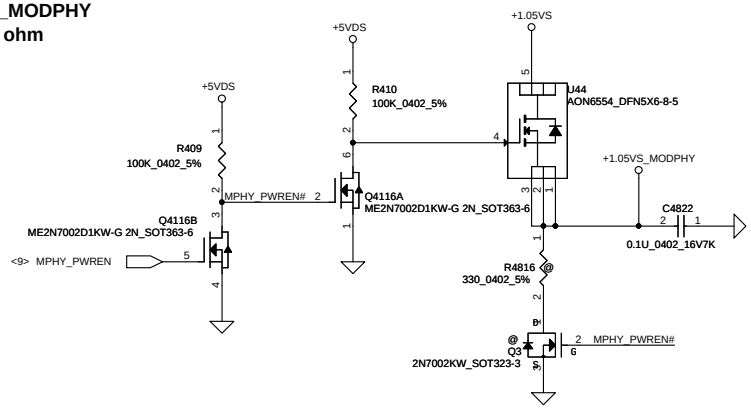
Date: Tuesday, March 25, 2014 | Sheet 39 of 62







CPU +V1.05DX_MODPHY
Max Rdson <6m ohm
1840mA



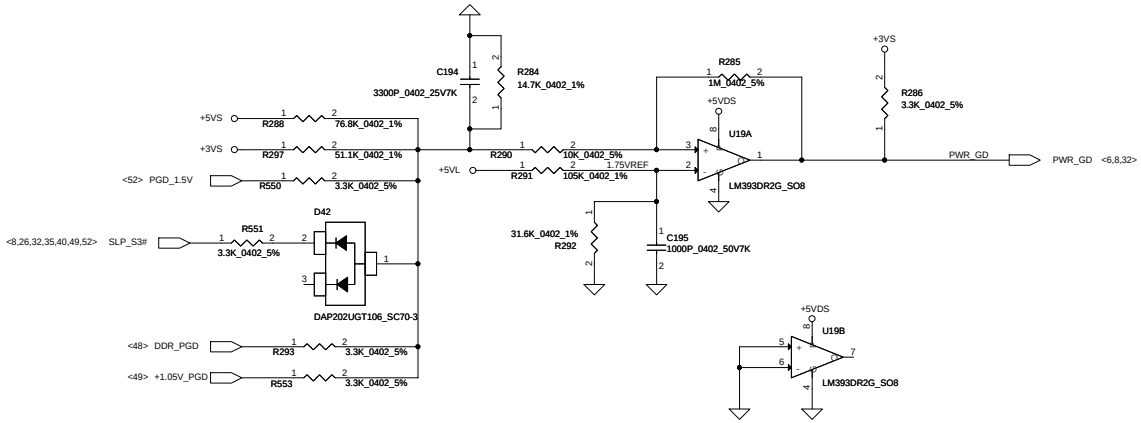
Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: DC Interface

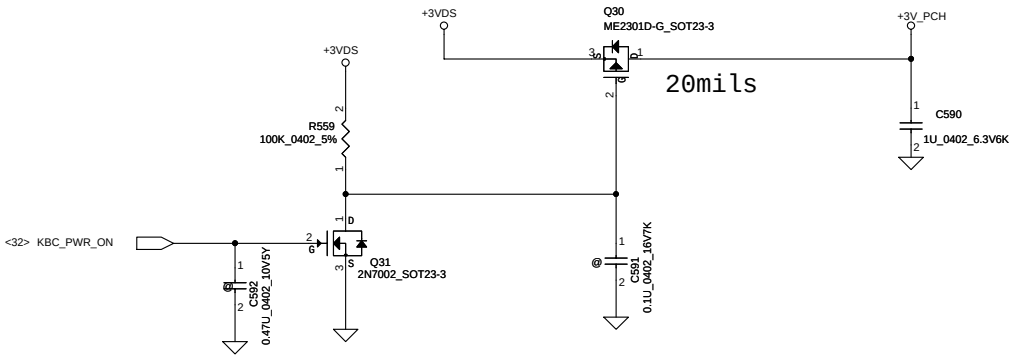
Size	Document Number	Rev
Custom	LA-B181P	0.5

Date: Tuesday, March 25, 2014 | Sheet 40 of 62



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: WAKE and RST-1

Size: C	Document Number: LA-B181P		Rev: 0.5
Date: Tuesday, March 25, 2014	Sheet 41 of 62		



Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: DC DC Device-1

Size	Document Number	Rev
Custom	LA-B181P	0.5

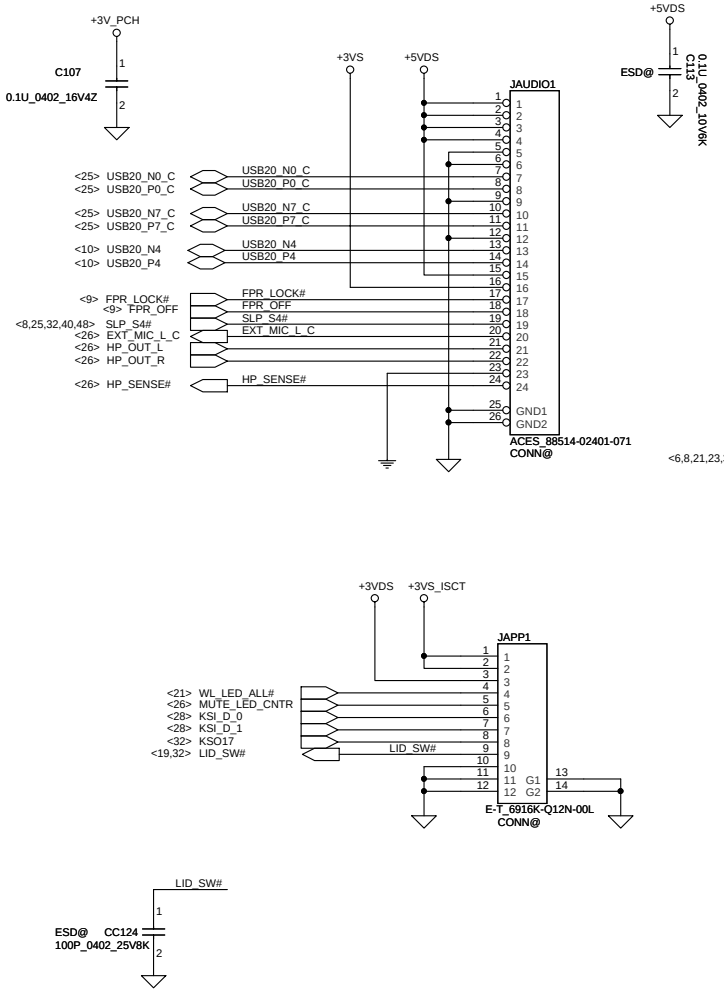
Date: Tuesday, March 25, 2014 Sheet 42 of 62

Audio Board

USB CONN

Finger printer

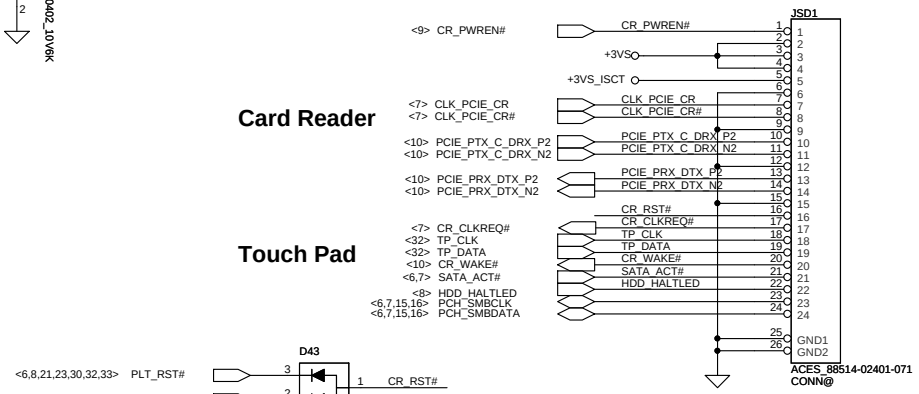
Combo Jack

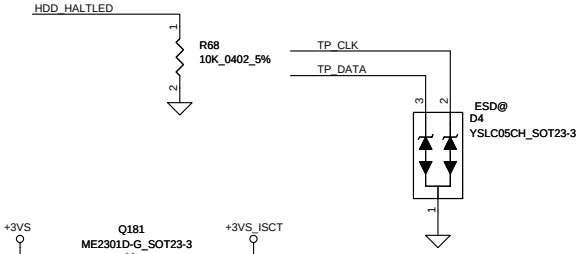


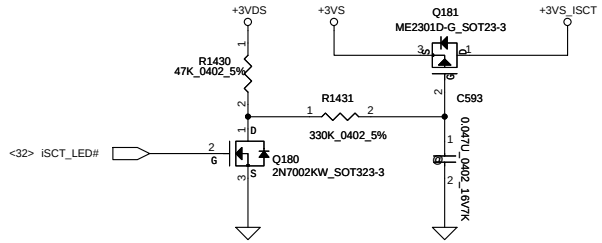
Card Reader Board

Card Reader

Touch Pad







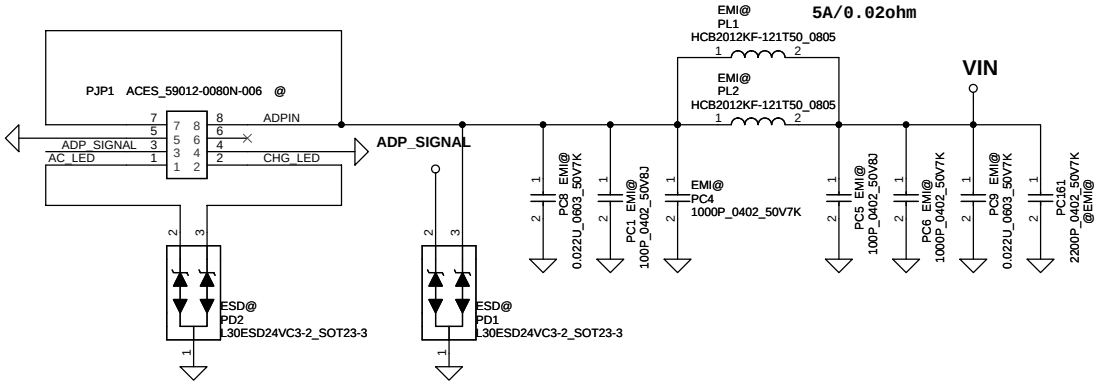
Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

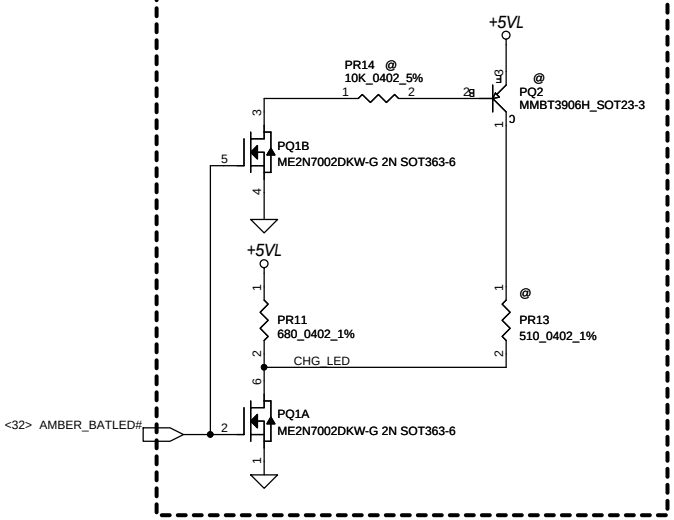
Compal Electronics, Inc.

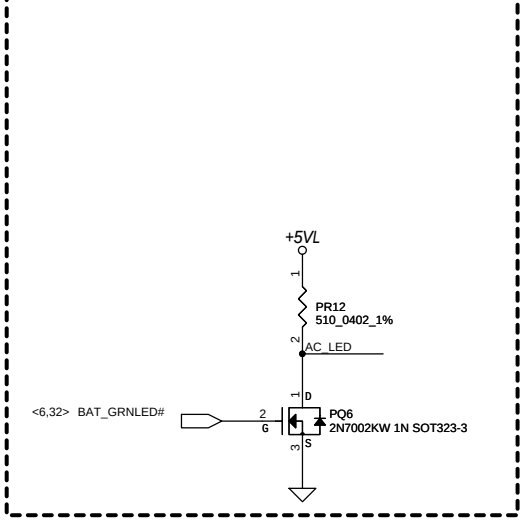
Title: DC DC Device-1

Size	Document Number	Rev
Custom	LA-B181P	0.5

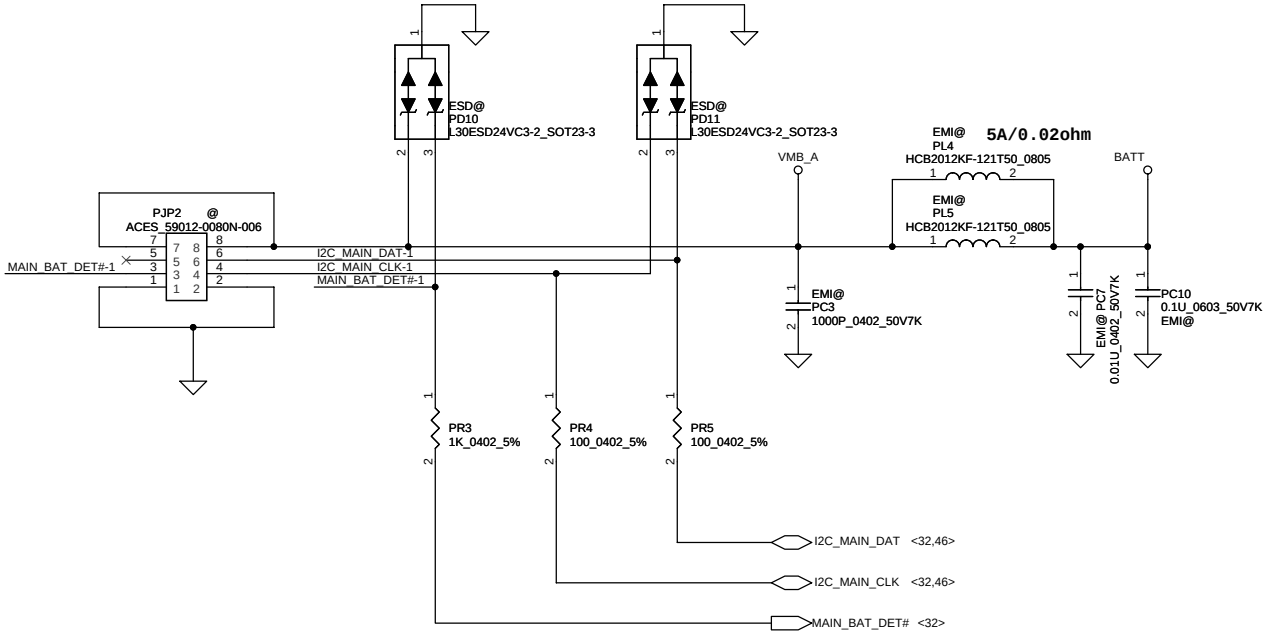
Date: Tuesday, March 25, 2014 Sheet 43 of 62



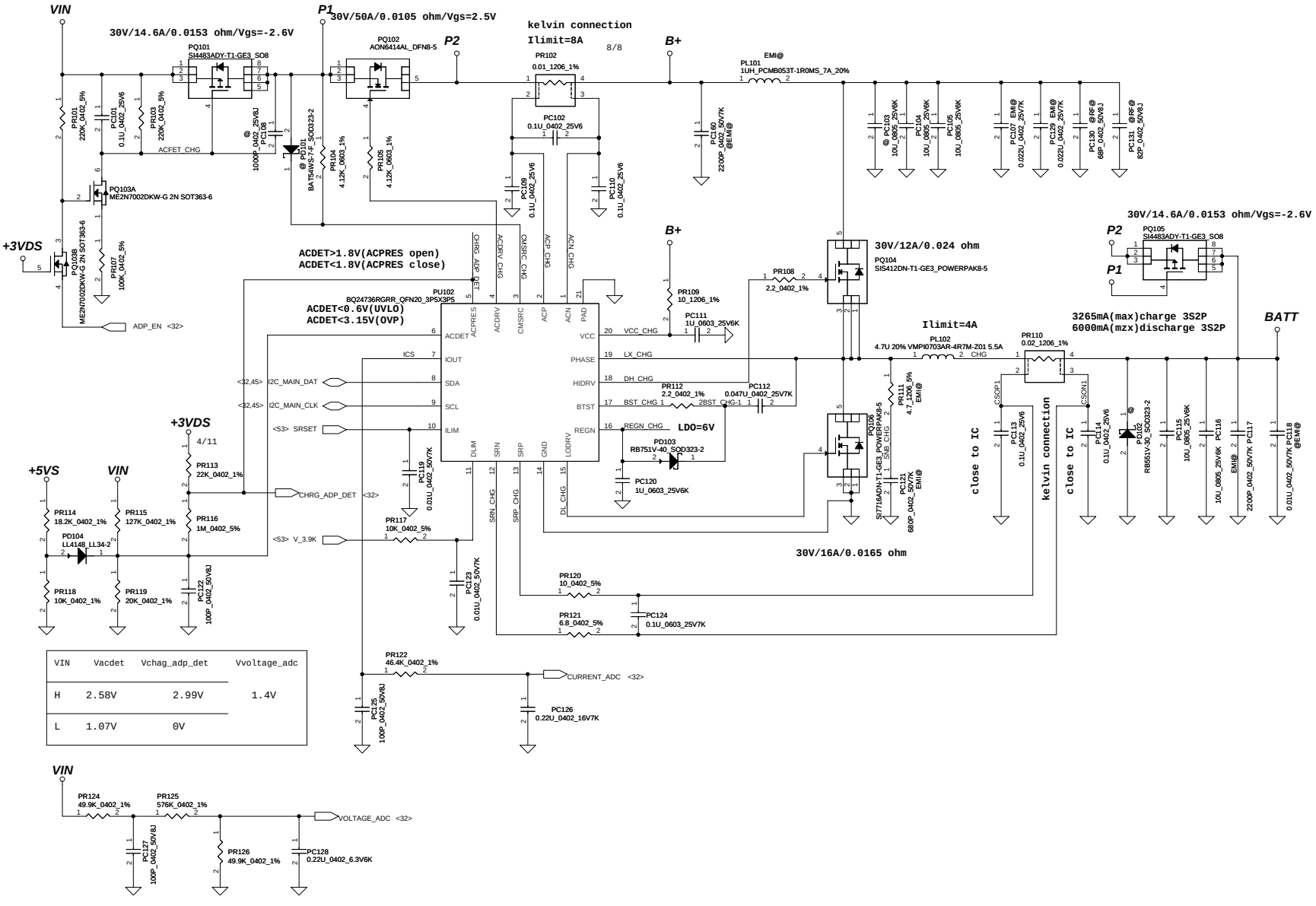




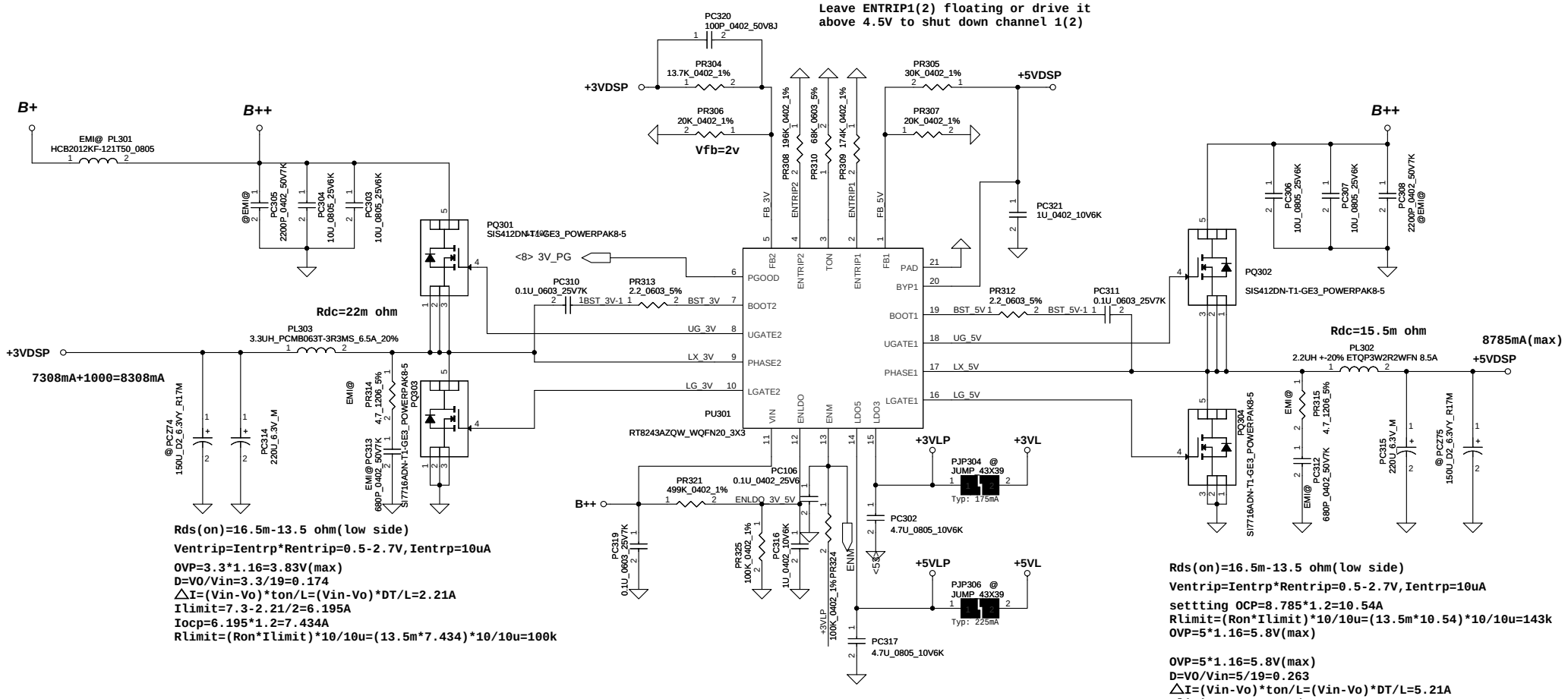
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/09/09	Deciphered Date	2016/09/30
Title	DC Conn		
Size	Document Number		Rev
	LA-B181P		0.5
Date:	Tuesday, March 25, 2014	Sheet 44 of 62	



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/09/09	Deciphered Date	2016/09/30
Title	BATT Conn		
Size	Document Number		Rev
	LA-B181P		0.5
Date:	Tuesday, March 25, 2014	Sheet	45 of 62



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/09/09	Deciphered Date	2016/09/30
Title	CHARGER		
Size	Document Number LA-B181P		Rev 0.5
Date: Tuesday, March 25, 2014	Sheet 46 of 62		



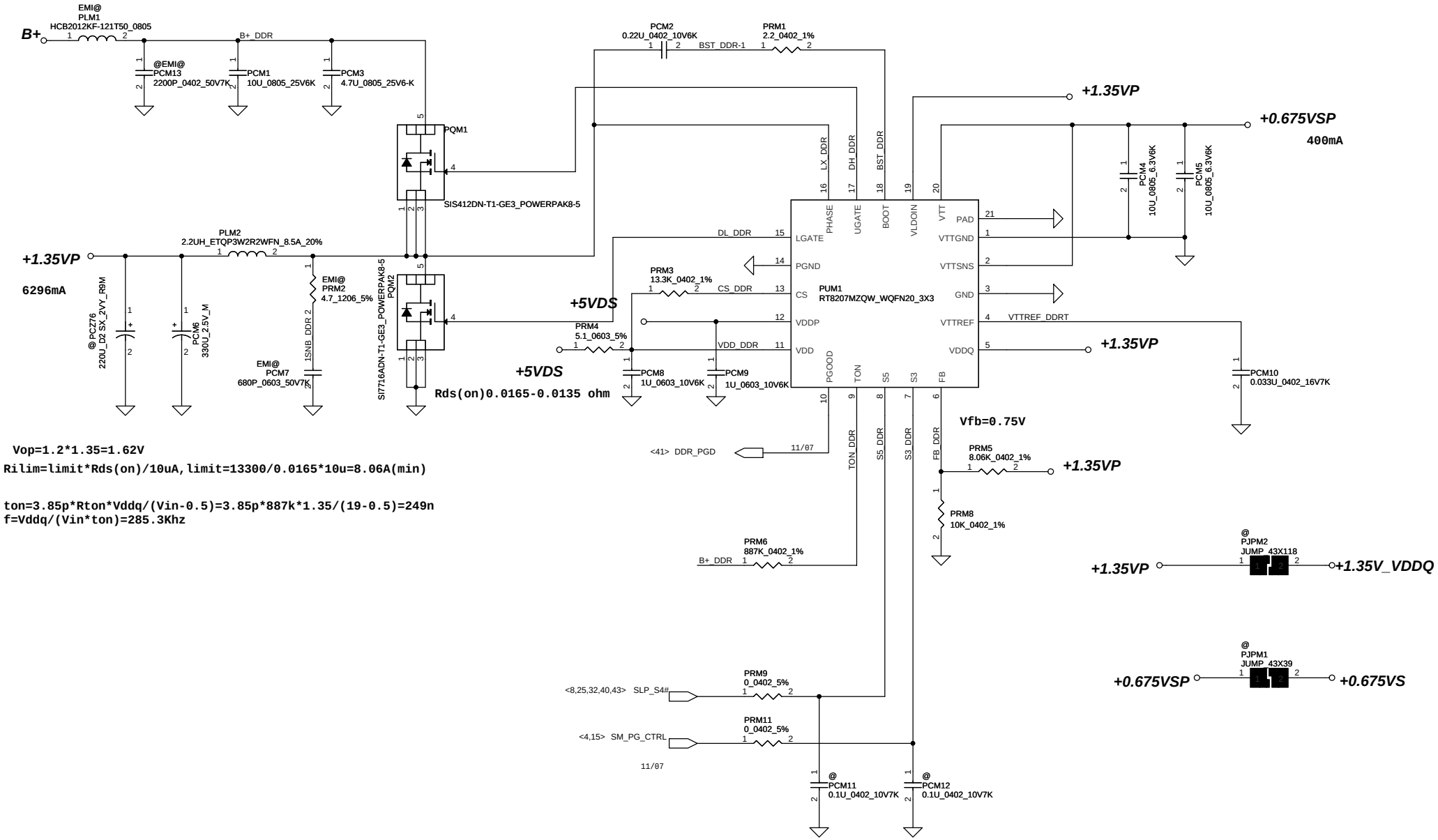
Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2016/09/30

Compal Electronics, Inc.

Title: 3VDSP/5VDSP

Size: Custom | Document Number: LA-B181P | Rev: 0.5

Date: Tuesday, March 25, 2014 | Sheet 47 of 62



Vop=1.2*1.35=1.62V

Rilim=limit*Rds(on)/10uA,limit=13300/0.0165*10u=8.06A(min)

ton=3.85p*Rton*Vddq/(Vin-0.5)=3.85p*887k*1.35/(19-0.5)=249n

f=Vddq/(Vin*ton)=285.3Khz

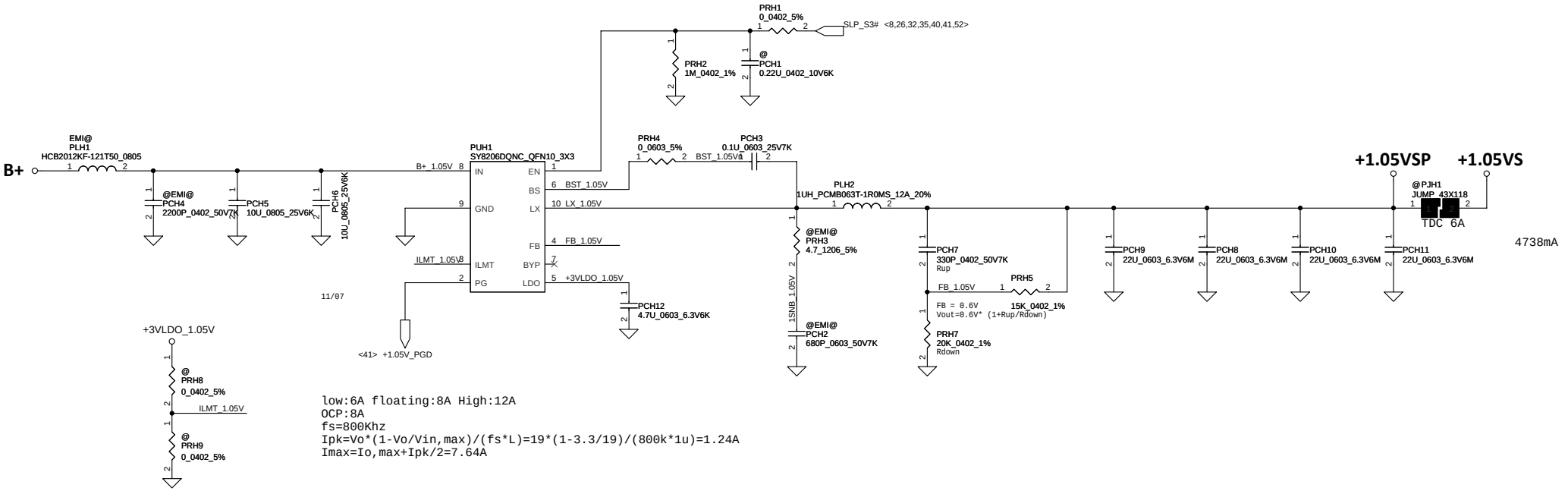
Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2016/09/30

Compal Electronics, Inc.

Title: +1.35V/+0.675VS

Size: Custom | Document Number: LA-B181P | Rev: 0.5

Date: Tuesday, March 25, 2014 | Sheet 48 of 62



Compal Electronics, Inc.

Title	*+1.05VS*	
Size	Document Number: **LA-B181P**	Rev: 0.5
Date: Tuesday, March 25, 2014	Sheet 49 of 62	

PRZ5:Vo-usr=1.7*(150/(150+9.53))=1.598V
Vusr=540mV
PRZ11:disable OSR&PT,Rosr=150k

PRZ10:setting fs R=150==>1Mhz

Ramp setting:
PRZ9=100K type:160mV
PRZ9>=150K type:40mV

boot voltage setting:
Vb-ram=1V==>2V
Vb-ram=0V==>1.7V
Vb-ram>1.525V==>0V

Iccmax=32A(15w),Iccmax=40A(28w)
IccTDC=10A(15w),IccTDC=16A(28w)
IccDyn=27A(15w),IccDyn=32A(28w)

OCP voatge seeting:
PRZ8=39K ==>18.9mV
Vimon=1.7V

Rp_n=10.74k Rcs(eff)=0.6m ohm
1.7V=10*(1+Rimon/39k)*0.6m*32,Rimon=345k

ALERT goes low,THERM=1.08V
VR_HOT goes low,THERM=1.1V

slew rate(15w,150K)=96mV/uS,slew rate(28w,100K)=84mV/uS
address selection(15w):1.7*100/(100+150)=0.68V
address selection(28w):1.7*100/(100+100)=0.85V

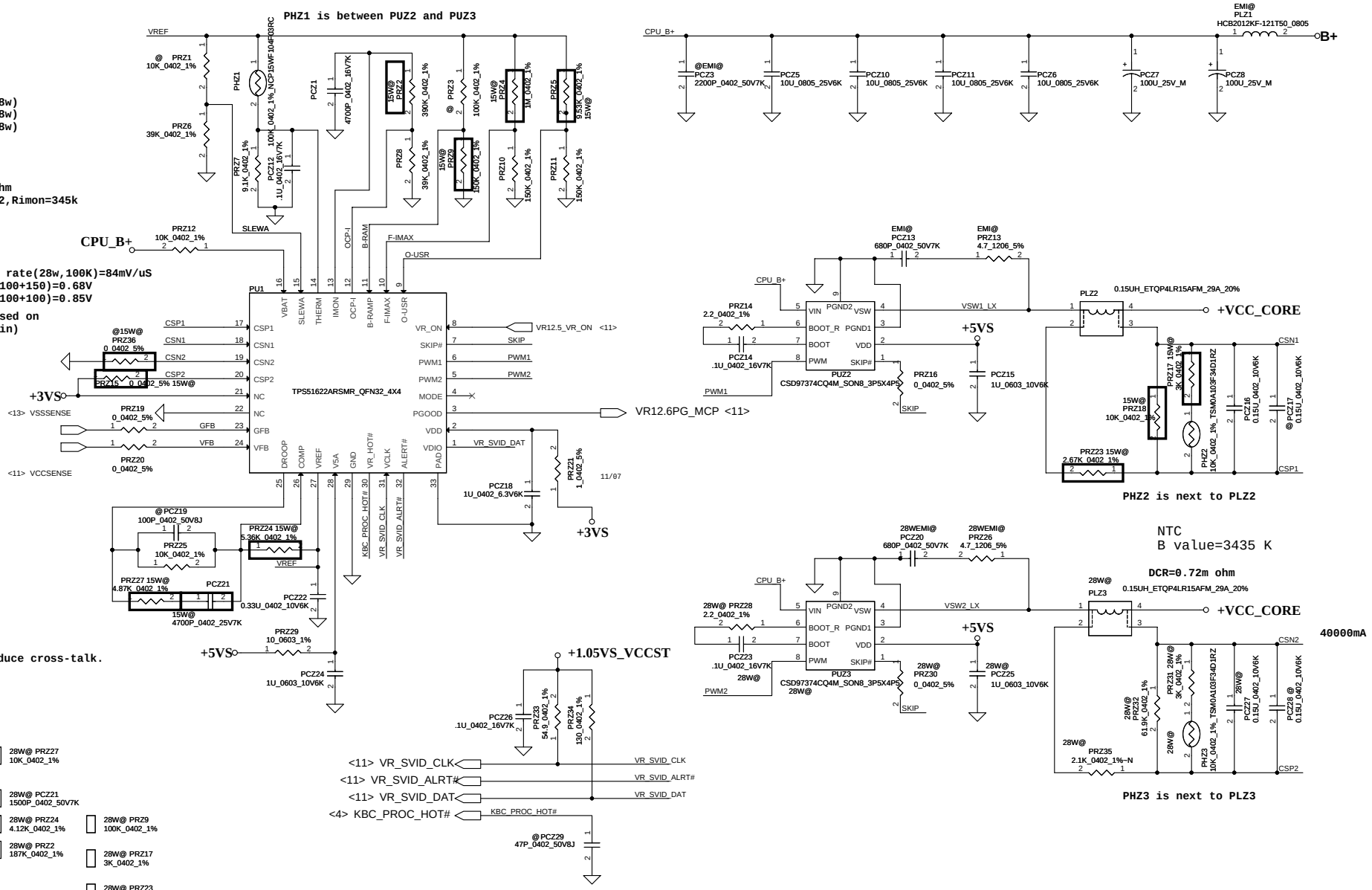
On-tome(ton):ON-time is fixed based on the input voltage (at the VBAT pin)

Vssense and Vccsense need to be difference pair

Droop:Error amplifier output.

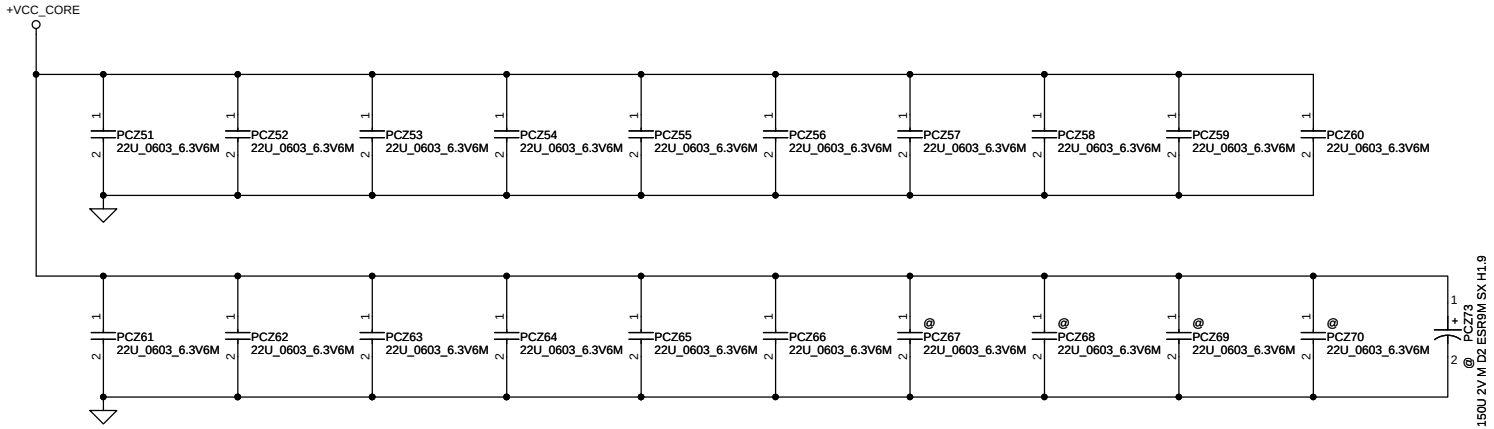
ALERT between VCLK and VDIO to reduce cross-talk.

PHZ1 is between PUZ2 and PUZ3

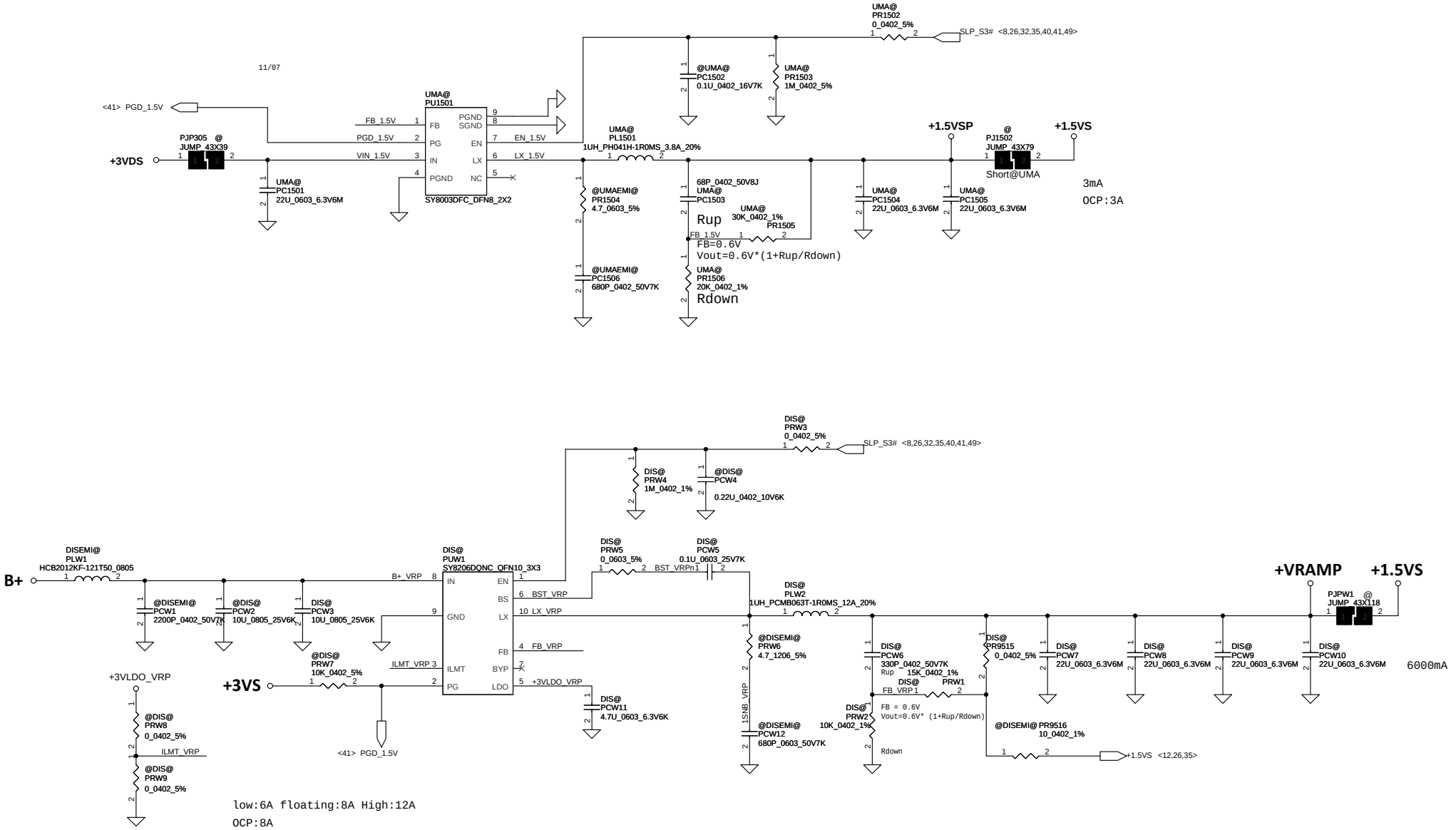


Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2016/09/30

Compal Electronics, Inc.			
Title	+CPU_CORE		
Size	Document Number	LA-B181P	Rev 0.5
Date: Tuesday, March 25, 2014	Sheet 50 of 62		



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/09/09	Deciphered Date	2016/09/30
Title	PROCESSOR DECOUPLING		
Size	Document Number		Rev
	LA-B181P		0.5
Date:	Tuesday, March 25, 2014	Sheet	51 of 62



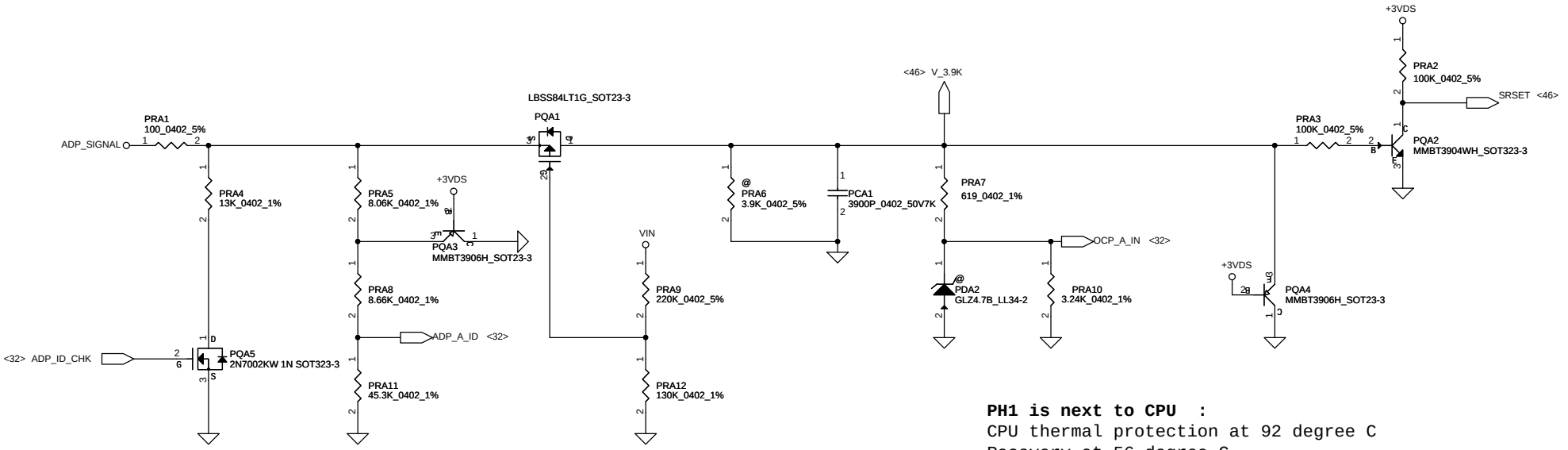
Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2016/09/30

Compal Electronics, Inc.

Title: +1.5VS

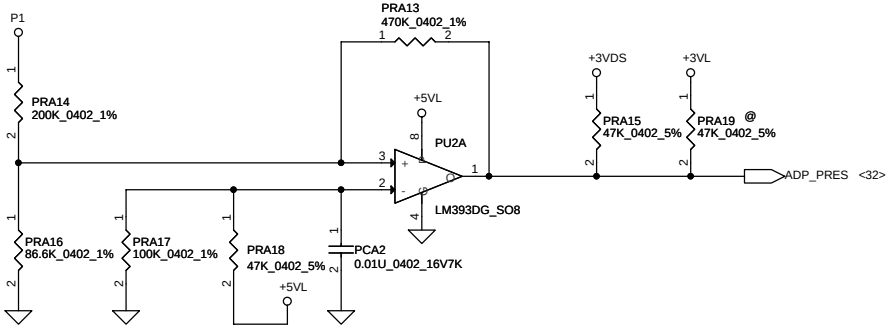
Size: | Document Number: LA-B181P | Rev: 0.5

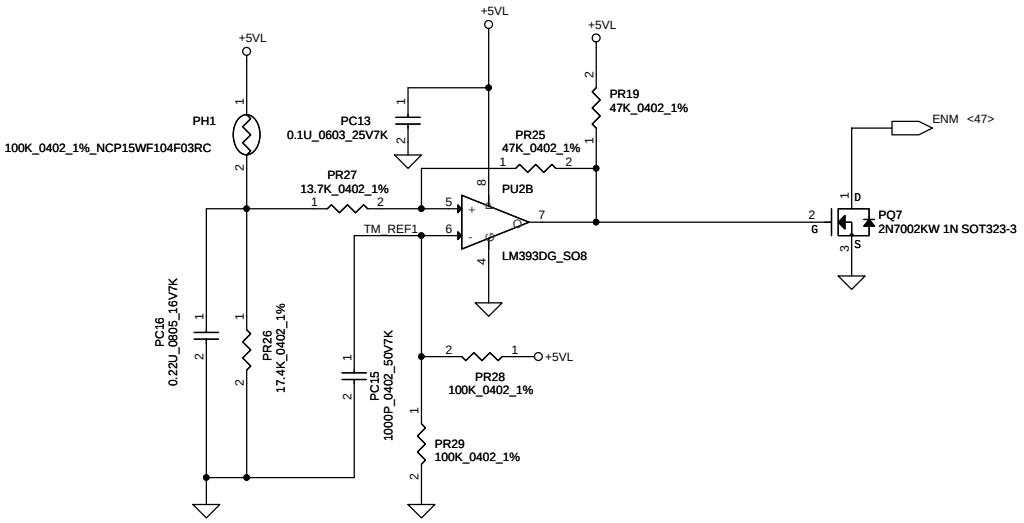
Date: Tuesday, March 25, 2014 | Sheet 52 of 62



MEMO:PRA4 and PQA5 are not mount

PH1 is next to CPU :
CPU thermal protection at 92 degree C
Recovery at 56 degree C

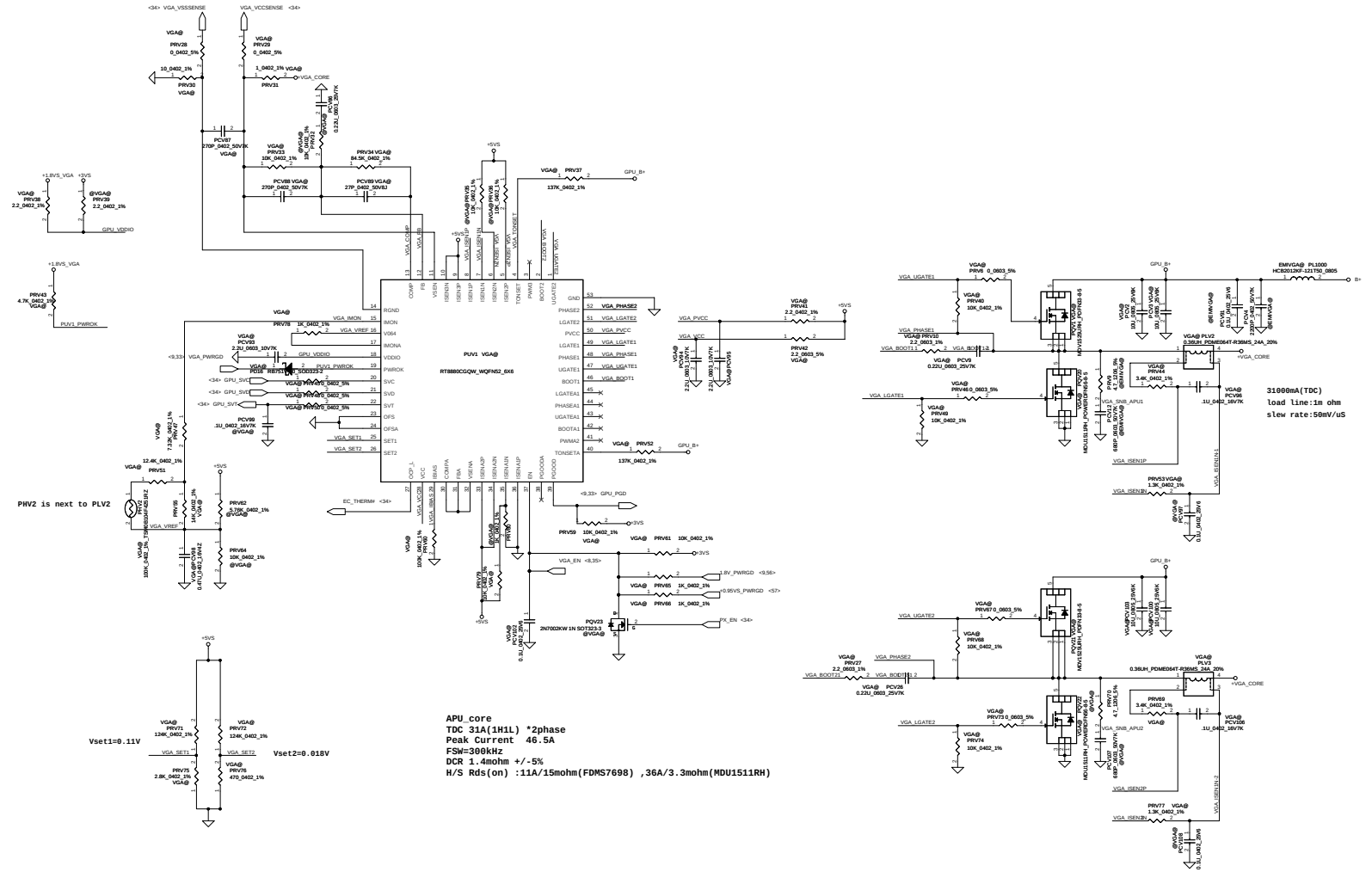




Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2016/09/30

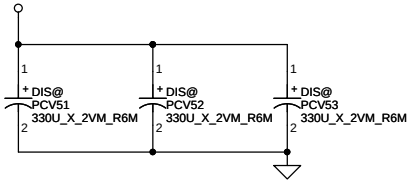
Compal Electronics, Inc.

Title	ADP_OCP
Size	
Document Number	LA-B181P
Rev	0.5
Date:	Tuesday, March 25, 2014
Sheet	53 of 62

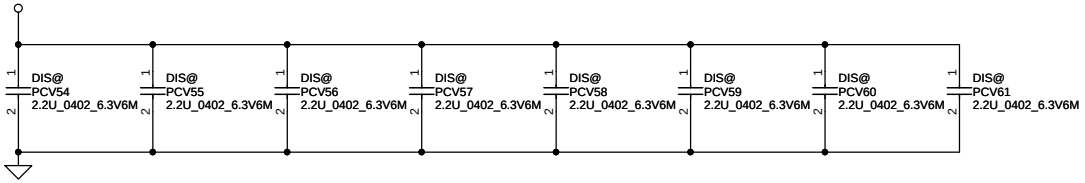


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/03/19	Deciphered Date	2013/03/19
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Title: RT8880AGQW
			Size: Document Number: LA-B181P Rev: 0.5
			Date: Tuesday, March 25, 2014 Sheet 54 of 60

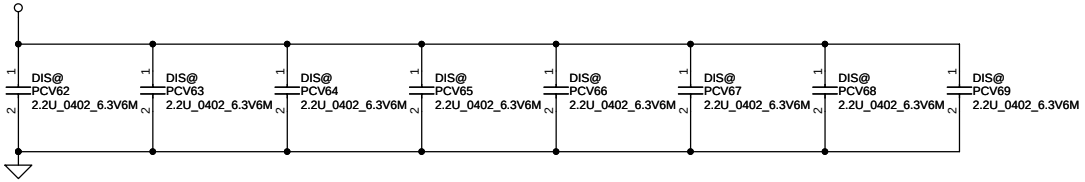
+VGA_CORE



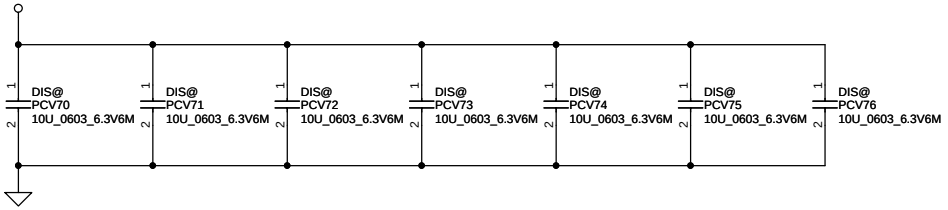
+VGA_CORE



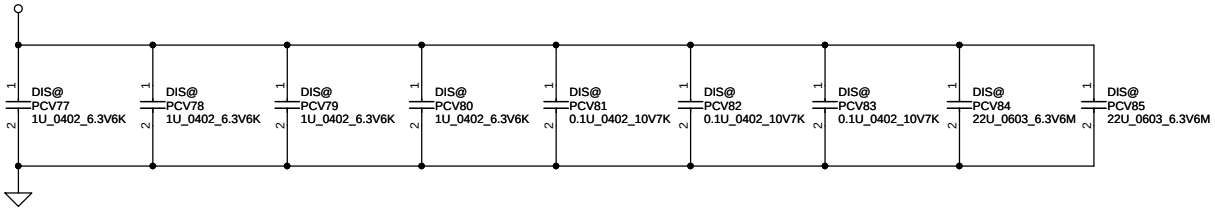
+VGA_CORE



+VGA_CORE



+VGA_CORE



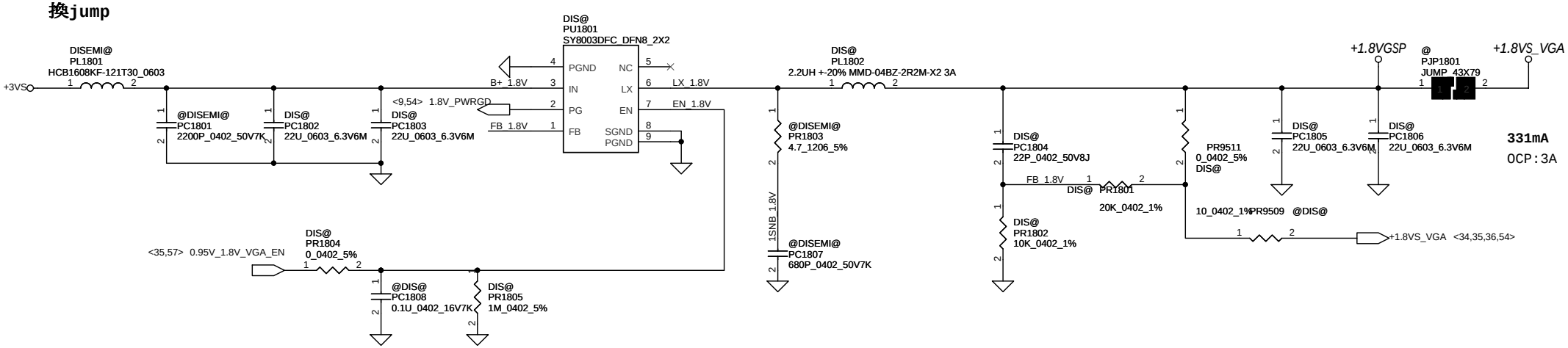
Security Classification	Compal Secret Data		
Issued Date	2012/04/03	Deciphered Date	2016/09/30

Compal Electronics, Inc.

Title: *VGA CHIP DECOUPLING*

Size | Document Number: **LA-B181P** | Rev: 0.5

Date: Tuesday, March 25, 2014 | Sheet 55 of 62



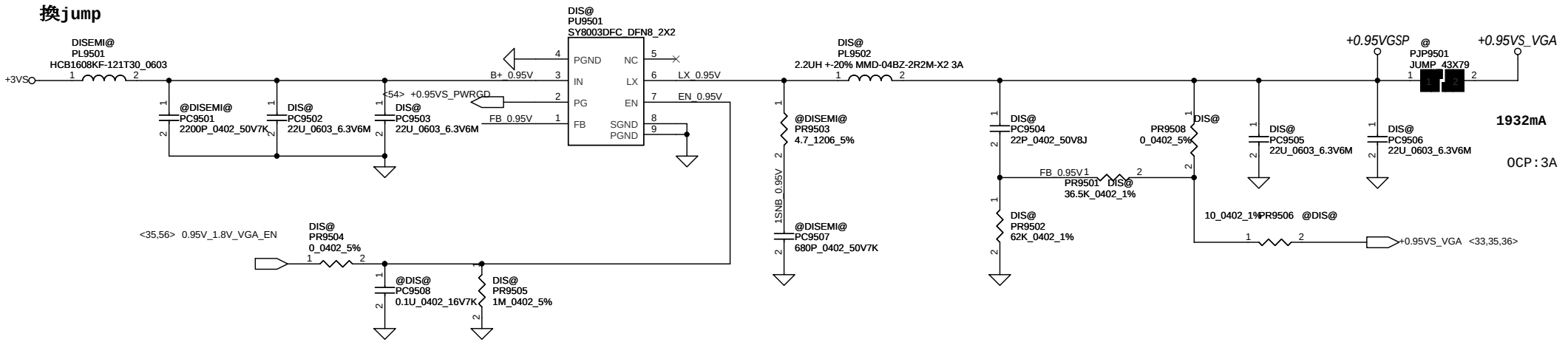
Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2016/09/30

Compal Electronics, Inc.

Title: *+1.8VS_VGA*

Size: B | Document Number: LA-B181P | Rev: 0.5

Date: | Sheet 56 of 62



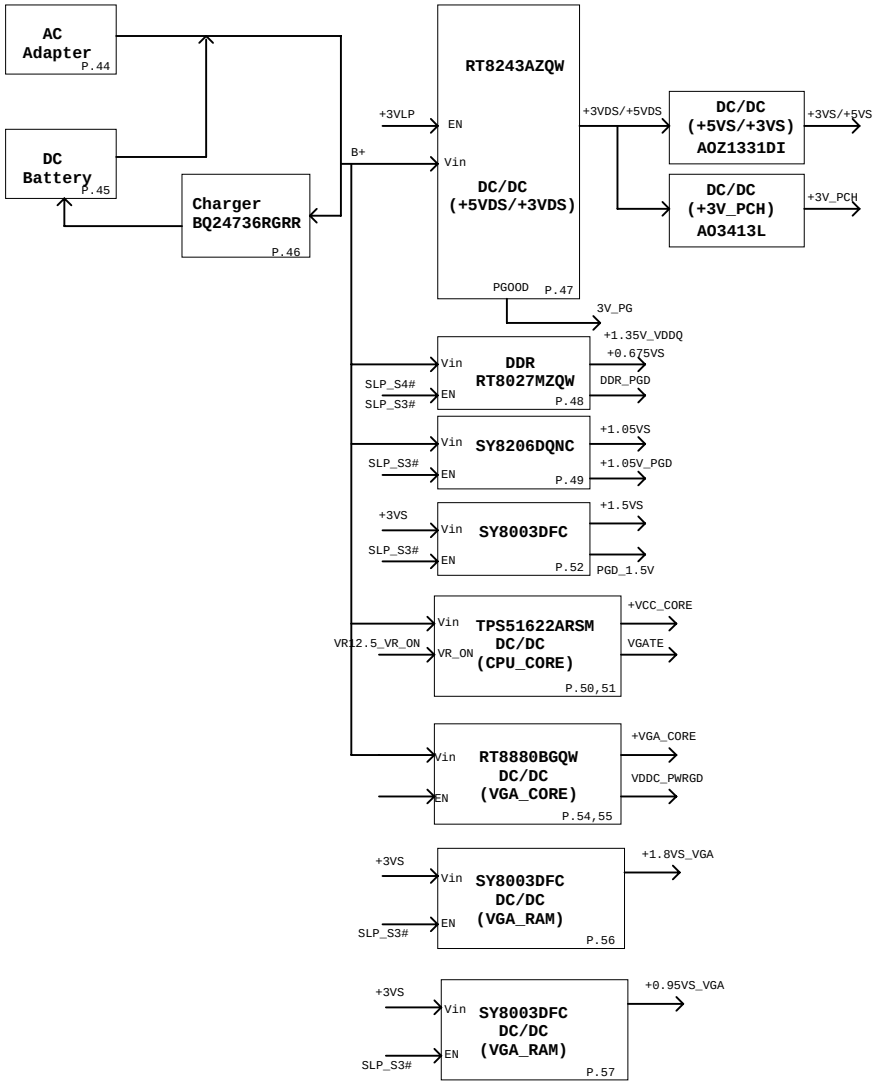
Security Classification	Compal Secret Data		
Issued Date	2013/09/09	Deciphered Date	2016/09/30

Compal Electronics, Inc.

Title: *+0.95VS_VGA*

Size: B | Document Number: **LA-B181P** | Rev: 0.5

Date: | Sheet 57 of 62



CPU DC/DC TPS51622ARSMR 50~51	
INPUTS	OUTPUTS
B+	VCC_VORE

SYSTEM DC/DC RT8243AZQW 47	
INPUTS	OUTPUTS
B+	3VDS/5VDS

SYSTEM DC/DC RT8207MZQW 48	
INPUTS	OUTPUTS
B+	1.35V_VDDQ 0.675VS

SYSTEM DC/DC SY8206DQNC 49	
INPUTS	OUTPUTS
B+	1.05VS

SYSTEM DC/DC SY8003DFC 52	
INPUTS	OUTPUTS
B+	1.5VS

SYSTEM DC/DC RT8880BGQW 54~55	
INPUTS	OUTPUTS
B+	+VGA_CORE

SYSTEM DC/DC SY8003DFC 56	
INPUTS	OUTPUTS
B+	+1.8VS_VGA

SYSTEM DC/DC SY8003DFC 57	
INPUTS	OUTPUTS
B+	+0.95VS_VGA

Security Classification	Compal Secret Data		
Issued Date	2012/04/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.

Title: Power Block Diagram

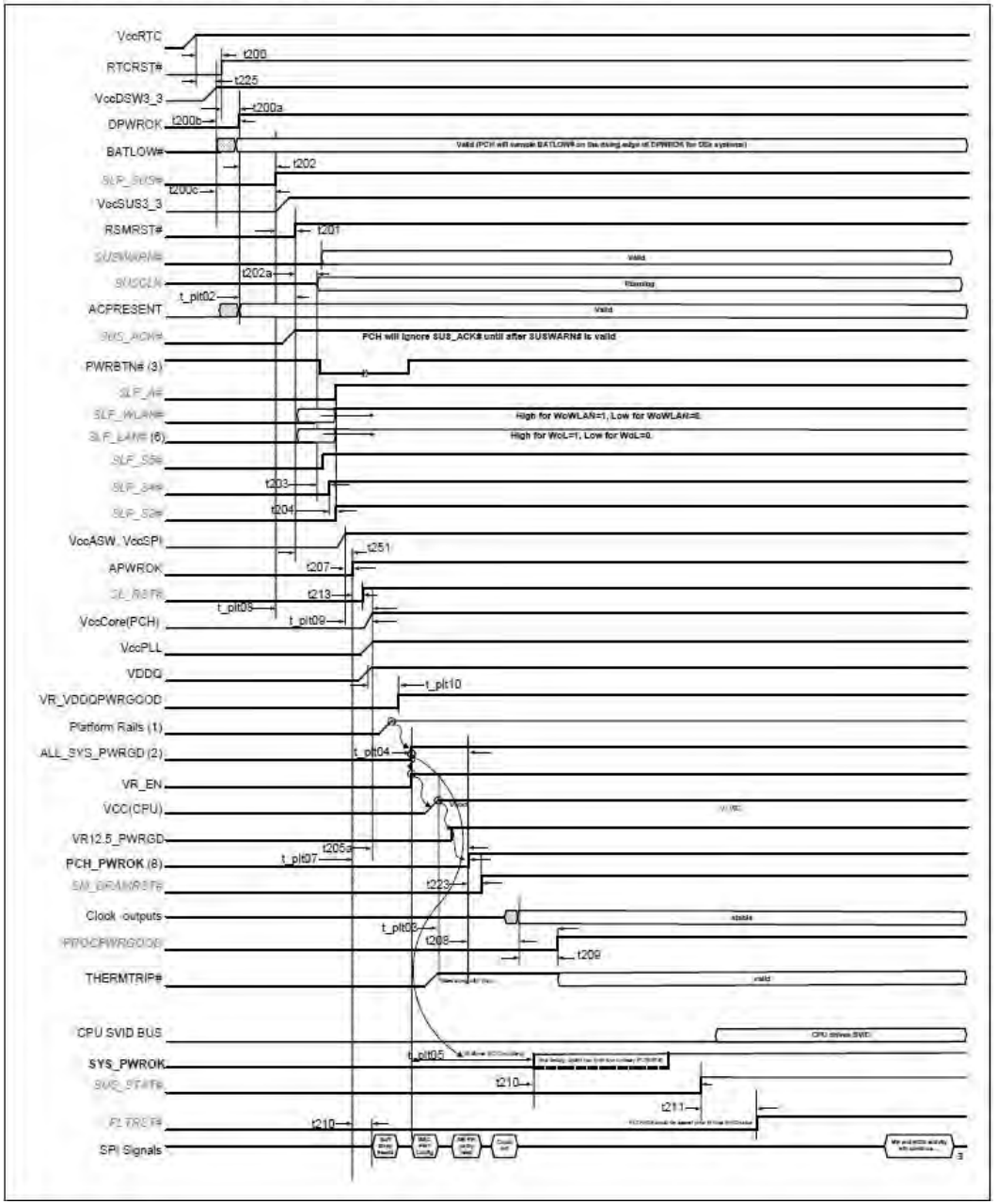
Size: Document Number: LA-8181P

Rev: 0.5

Date: Tuesday, March 25, 2014 Sheet 58 of 60

Power ON Sequence

Timing Diagram for G3 to S0/M0 [Deep Sx Platform]



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/02/26	Deciphered Date	2015/07/08
Title	Power ON Sequence		
Size C	Document Number LA-B181P		Rev 0.5
Date: Tuesday, March 25, 2014	Sheet 59 of 62		

Version change list (P.I.R. List)

Item	Date	Fixed Issue	Reason for change	Modify List	Phase
1	20131030		Delete 1.PQ307 2.charger air line power circuit 3.change AON7506 to SI7716(PQ106) 4.change NDS0610 to LBSS84L 5.change AON7506 to SI7716 6.change 47U 6.3V to 22U 6.3V (PCH8,PCH9) 7.PR9512 mount	1.customer request 2.customer request 3.customer common part 4.compal change 5.customer common part 6.vender reveiw	DB0 DB0 DB0 DB0
2	20131031		1.10U_0805_25V==>2200p_0402_50V not mount(PC160) 2.PC107,PR111,PC121,PC305,PR314 PC313,PC308,PR315,PC312,PCH4,PCZ3,PRZ13,PCZ13 PCZ20,PCZ26,PCW1,PCV4,PRV70,PCV107 3.change 147K_0402_1% to 237K_0402_1% (PRV34) change 560P_0402_50V7K to 470P_0402_50V7 (PCV88) change 10.7K_0402_1% to 22.6K_0402_1%(PRV47) change 9.76K_0402_1% to 5.6K_0402_1%(PRV51) change 15K_0402_1% to 19.1K_0402_1%(PRV55) change 910K_0402_5% to 20.5K_0402_1%(PRV75) change 910k_0402_1% to 910_0402_1%(PRV53) change 3.48K_0402_1% to 3.4K_0402_1%(PRV69) change 910k_0402_1% to 910_0402_1%(PRV77) 4.remove PR9510,PR9512,PR9514,PR9513 5.remove PC318,PRH10,PRW10,PCW13 6. PRH8,PRW8 not mount 7.22u/0805 6.3V to 22u/0603 6.3V PC1504,PC1501 PC1505,PC1802,PC1803,PC1805,PC1806,PC9502,PC9503, PC9505,PC9506,PCH9,PCH10,PCH11,PCH8 8.0.22U_0402_6.3V6K to 0.22U_0603_50V7K (PC128)	1.EMI feedback 2.EMI feedback 3.power vender feedback 4.power change fb sense 5.for compal module design 6.current limit design	DB0 DB0 DB0 DB1 DB1 DB1 DB1 DB1 DB1 SI1 SI1 SI1
3	20131101		1.remove PRW11	1.HW request	
4	20131112		1.not mount PRW7 2.change 0_0402_1% to 0_0402_5%(PR1502,PR1804, PR9504,PR9508,PR9511,PR9515)	2.AMD request	
5	20131202		1.not mount PRZ36,PRV32 and PCV86 2.PC128 change 0.22U_0603_25V to 0.22U_0402_6.3V6K 3.add PD16,PRV43 4.add PRV45,PRV48,PCV99 and PRV50	1.PWR request 2.PWR request 3. customer request 4.richtek request	SI1 SI1 SI2
					SI2

Security Classification	Compal Secret Data		
Issued Date		Deciphered Date	

Compal Electronics, Inc.		
Title: PIR List		
Size: B	Document Number: LA-B181P	Rev: 0.5
Date: Tuesday, March 25, 2014	Sheet 60 of 62	

Version change list (P.I.R. List)

Item	Date	Fixed Issue	Reason for change	Modify List	Phase
6	20131210		add PRV78 1K_0402_1% PRV62 5.76K_0402_1% PRV64 10K_0402_1% PRV80 1K_0402_1% PRV79 10K_0402_1% PRV52 137K_0402_1%	RITCHTEK issue request	DB0 DB0 DB0 ~~DB0~~
	20131221		PRM2 Change 4.7_1206_5% to 0_1206_5% PCM7 Change 680P_0603_50V7K to 1000P_0603_50V7K PR314 not mount==>mount PC313 not mount==>mount PR315 not mount==>mount PC312 not mount==>mount PCZ13 not mount==>mount PRZ13 not mount==>mount PCZ20 not mount==>mount(28W) PRZ26 not mount==>mount(28W)	EMI request	DB0 DB0 DB0 DB1 ~~DB1~~
	20131226		PRV31 Change 10_0402_1% to 1_0402_1% PRV34 Change 127K_0402_1% to 84.5K_0402_1% PRV47 Change 22.6K_0402_1% to 7.32K_0402_1% PRV51 Change 5.6K_0402_1% to 12.4K_0402_1% PRV55 Change 19.1K_0402_1% to 14K_0402_1% PRV75 Change 20.5K_0402_1% to 2.8K_0402_1% PRV77 Change 910_0402_1% to 1.3K_0402_1% PRV53 Change 910_0402_1% to 1.3K_0402_1% PC128 Change 0.22U_0603_6.3V to 0.22U_0402_6.3V	RITCHTEK issue request	DB1 DB1 DB1 DB1 SI1
	20140102		PRM2 Change 0_1206_5% to 4.7_1206_5% PCM7 Change 1000P_0603_50V7K to 680P_0603_50V7K PUV1 change RT8880BGQW to RT8880CGQW	EMI request RITCHTEK request	SI1 ~~SI1~~
	20140103		PR14,PQ2 and PR13 are not mount. PR11 Change 330_0402_1% to 680_0402_1%	Customer request	
	20140106		PRV80 mount==>not mount PRV79 not mount==>mount	RITCHTEK issue request	
	20140213		add PC8,PC9 and PC10 mount PR111,PC121,PC107 and PC129 PC107 2200P_0402_50V7K==>0.022_0402 25V PC129 0.1U_0402_50V7K==>0.022_0402_25V	EMC request EMC request	
	20140214		add PC161 2200P_0402_50V7K not mount	EMC request	SI1 SI1 SI2 SI2

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: PIR List
Size: B	Document Number: LA-B181P		Rev: 0.5
Date: Tuesday, March 25, 2014	Sheet 61 of 62		

ZPL40/50/70 from DB to DB-R LA-B181P REV:0.1 -> 0.2 Modify <2013.11.28.~ 2013.12.03>

Rev.	Item	Date	Impact	Page	Change Cause	Modify Description
0.2	1	11/28	CKT, LAYOUT	6	-Design issue	-Change RC222 pin 1 connection from +3VS to +5VS
0.2	2	11/28	CKT, LAYOUT	7	-Follow CHICLET	-Move TPM LPC CLK from port 0 to port 1
0.2	3	11/28	CKT	8	-DGPU_PWR_EN voltage level uncorrect issue	-Uninstall RC125
0.2	4	11/28	CKT, LAYOUT	9	-DGPU power on sequence	-Change RC121 to 100K and add CC127 to timing delay.
0.2	5	11/28	CKT, LAYOUT	18	-Footprint uncorrect issue	-Modify UT6 footprint to SC70-5
0.2	6	11/28	CKT, LAYOUT	21	-No used.	-Remove CLK_PCI_DEBUG from JMINI1 pin 19
0.2	7	11/28	CKT	23	-Q35 can't turn on issue	-Uninstall RL26
0.2	8	11/28	CKT	30	-Follow HP BIOS code request	-Uninstall R124
0.2	9	11/28	CKT, LAYOUT	32	-Avoid leakage issue.	-Swap Q88 pin 1 and pin 3
0.2	10	11/28	CKT, LAYOUT	32	-Footprint uncorrect issue	-Modify C187 footprint to 0402 package
0.2	11	11/28	CKT, LAYOUT	33	-Design issue	-Swap GPU PEG RX bus P/N signal and CV1~CV8 change to 0.22u
0.2	12	11/29	CKT, LAYOUT	28	-Current limit	-Add R660
0.2	13	11/29	CKT, LAYOUT	30	-Vendor request	-U13 pin 6 add external 4.7K PU to +3VS_TPM
0.2	14	11/29	CKT	32	-Follow CHICLET	-Change R255, R257, and R493 to 10Kohm -Delete QC12 and add buffer U20 and U21.
0.2	15	12/02	CKT, LAYOUT	6	-Follow CHICLET	QC8.3 net name from HDA_SDOUT_AUDIO change to HDA_SDOUT
0.2	16	12/02	CKT, LAYOUT	32	-Follow CHICLET	add R101, R102, R104, R105, R106
0.2	17	12/02	CKT, LAYOUT	23	-leakage issue and FAR suggest	1.swap QL2 pin 1 and pin 3 2.install RL40 3.Reserve 2 resistor (RL48, RL49) connection QL2.2 to +3VS and +LAN_VDD_3V3.
0.2	18	12/02	CKT, LAYOUT	34	-Follow 2013 RRR	-Add D14
0.2	19	12/02	CKT	35	-DGPU power on sequence	-Uninstall R5076, R5074
0.2	20	12/03	CKT, LAYOUT	40	-Follow CHICLET	-change +1.05VS_MODPHY switch circuit

ZPL40/50/70 from DB-R to SI LA-B181P REV:0.2 -> 0.3 Modify <2013.12.04~ 2013.12.17>

0.3	1	12/04	CKT, LAYOUT	29	-Follow 2013 RRR	-update FAN control circuit delete Q4108, R5080 and add U2, C31
0.3	2	12/05	CKT	35	-DGPU power on sequence	-C4816 from 0.01u change to 0.022u
0.3	3	12/05	CKT	9	-DGPU power on sequence	-Change RC121 to 0ohm and uninstall CC127 (BIOS code control timing)
0.3	4	12/05	CKT	10, 33	-For PCIe Gen2	-change CC89, CC90, CC91, CC92, CC93, CC94, CC95, CC96, CV1, CV2, CV3, CV4, CV5, CV6, CV7, CV8 from 0.22u to 0.1u
0.3	5	12/06	CKT	12	-Follow CHICLET	-Change RC174 from 5.11ohm to 0ohm
0.3	6	12/06	CKT	11	-Follow INTEL schematic	-Change RC156 from 110ohm to 130ohm install
0.3	7	12/06	CKT, LAYOUT	29	-Platform ID identify	-add R82, R86
0.3	8	12/06	CKT, LAYOUT	32		-reserve R136, R137 co-lay with U20, U21
0.3	9	12/06	CKT, LAYOUT	40		-reserve R135 co-lay with Q185
0.3	10	12/09	CKT, LAYOUT	43	-No leakage issue	-remove Q57
0.3	11	12/09	CKT	26	-Follow CHICLET	-RA36 from 22ohm change to 33ohm
0.3	12	12/09	CKT, LAYOUT	17	-Follow INTEL schematic	-Install CD52, CD53, CD54, RD11, RD12, RD19 and re-placement RD7, RD8, RD15
0.3	13	12/09	CKT, LAYOUT	11	-Follow INTEL schematic	-Re-placement RC154
0.3	14	12/09	CKT, LAYOUT	12	-Follow INTEL schematic	-Add RC183, CC47, RC189, CC75
0.3	15	12/10	CKT, LAYOUT	10	-For WWAN , Touch share USB port	-Add R138, R139
0.3	16	12/10	CKT, LAYOUT	4	-Follow CHICLET	-Add C32
0.3	17	12/11	CKT, LAYOUT	8	-Follow INTEL schematic	-reserve RC330
0.3	18	12/11	CKT, LAYOUT	21	-solve SIM card can't detect issue	-delete R5079 , Q4107 and add C2
0.3	19	12/13	CKT, LAYOUT	9	-Follow Runt	-R103 change to test point T184
0.3	20	12/13	CKT	8	-solve DGPU power issue	-Install RC125
0.3	21	12/13	CKT, LAYOUT	21	-Follow Runt	-Q90 , Q4113 from two single MOS change to daul MOS (Q90)
0.3	22	12/13	CKT, LAYOUT	22	-ODD power issue	-Add Q63
0.3	23	12/13	CKT, LAYOUT	23	-LAN power issue	-delete JHW1 , RL26
0.3	24	12/13	CKT, LAYOUT	21	-no need	-delete R205 , C292
0.3	25	12/13	CKT	25	-For V drop test	-C1572 from 100u change to 150u
0.3	26	12/13	CKT, LAYOUT	9	-Hp request	-ODD_DA# form GPIO14 change to GPIO3
0.3	27	12/13	CKT, LAYOUT	21	-For GPIO initial status	-add R91
0.3	28	12/14	CKT, LAYOUT	12	-solve power ripple	-add CC77 , CC78 , CC79
0.3	29	12/16	CKT, LAYOUT	9	-reserve for MPHY sequence	-add RC377

ZPL40/50/70 from DB-R to SI LA-B181P REV:0.3 -> 0.4 Modify <2013.12.18~ 2013.12.25>

0.4	1	12/20	CKT	9	-Follow HP request	-Install RC272, RC273
0.4	2	12/20	CKT, LAYOUT	15	-Follow Intel PDG	-Remove RD26, Install RD21
0.4	3	12/20	CKT, LAYOUT	16	-Follow Intel PDG	-Unnstall CD52, CD53, CD54, RD11, RD12, RD19 and re-placement RD7, RD8, RD15
0.4	4	12/20	CKT, LAYOUT	19	-Follow Vendor request	-Reserve RG5
0.4	5	12/20	CKT	19	-Follow HP request	-Change R82, R86 to 0 ohm
0.4	6	12/20	CKT	20	-Follow Intel PDG	-Change RP3 and RP4 to 470 ohm
0.4	7	12/20	CKT	21	-Compal Request	-Install R91
0.4	8	12/20	CKT, LAYOUT	22	-Customer modify GPIO table.	-Remove Q84, R954. Change JODD1 pin 11 netname to ODD_DA#
0.4	9	12/20	CKT	23	-Prepare leakage issue when S3, S5	-Uninstall RL40, QL2, RL49, RL48 install RL34
0.4	10	12/20	CKT	24	-Vendor Request	-Reserve RA40, U4101 pin 37 add RT57 10K PU to +5VS
0.4	11	12/20	CKT	31	-Vendor Request	-Remove R1363, R1365, R1367, C421, C423, C414, L31, L32, L34, R1364, R1366, and R1368. Modify CRT pi filter
0.4	12	12/20	CKT, LAYOUT	40	-Follow Compal common design	-Modify MPHY Power circuit
0.4	13	12/23	CKT, LAYOUT	30	-Follow RF team request	-Install C80, C556, C81, C558 -Reserve C90, C564, C91, C565, C92, C566, C93, C567, C95, C569, C110, C578, C111, C579, C108, C576, C82, C559, C83, C560, C84, C561, C86, C562, C89, C563, C94, C568, C96, C571, C112, C580, C109, C577, C106, C574, C97, C572, C105, C573, C130, C581, C131, C582, C132, C583, C133, C584, C134, C585, C135, C586, C136, C587, C137, C588, C138, C589
0.4	14	12/24	CKT, LAYOUT		-Follow ESD team request	-Install C113, C127 -Reserve C114, C115, C116, C121, C123, C124, C128, C129

ZPL40/50/70 from SI to PV-1 LA-B181P REV:0.3 -> 0.4 Modify <2014.02.05~2014.>

0.5	1	02/05	CKT	21	-Double pull hugh	-RN3 change to @
0.5	2	02/05	CKT	18, 19	-For LVDS SKU	-R163, RG3 change to LVDS@
0.5	3	02/05	CKT	19	-For eDP SKU	-R172 change to eDP@
0.5	4	02/05	CKT	19	-For Lid Switch issue	-R166, R175 change to 3.3K
0.5	5	02/05	CKT, LAYOUT	22	-For ODD issue	-add R448, reserve C151
0.5	6	02/05	CKT, LAYOUT			-1. QA2, QA3 combine to dual mos QA2A, QA2B 2. Q91, Q182 combine to dual mos Q91A, Q91B 3. Q86, Q87 combine to dual mos Q86A, Q86B 4. Q63 change to Q63A, Q63B 5. Q4112, Q4114 combine to dual mos Q4112A, Q4112B
0.5	7	02/10	CKT, LAYOUT	35	-For GPU Power Sequence	-add D15 and move R5075, C4819
0.5	8	02/10	CKT, LAYOUT	28	-Follow ESD team request	-add C594, C595, C596
0.5	9	02/10	LAYOUT	31		-Move U4101 circuit close to JCRT
0.5	10	02/11	CKT, LAYOUT	40	-SLG59M1470VTR is single source issue	-modify U44 circuit
0.5	11	02/12	CKT	33	-Improve VGA_PWRGD signal quality	-R5094 from 8.25K change to 0ohm
0.5	12	02/13	CKT, LAYOUT	11, 19	-Follow RF team request	-add C139, C140, C421
0.5	13	02/14	CKT, LAYOUT		-Follow HP request	-1. FPR_OFF from GPIO11 change to GPIO65 2. change JAUDIO1.16 from +3V_PCH to +3VS 3. disconnect EC pin125 and CPU pinAJ5 rename EC pin125 "PCH_PCIE_WAKE#" to "EC_GPIO25" and add R249 pull up to +3VDS 4. RN13 un-install 5. connector EC pin103 to JMINI1 pin1 (WLAN_WAKE#), JMINI2 pin15 change to NC 6. connector EC pin105 to CPU pinAJ5 (PCH_PCIE_WAKE#) 7. change RN3 pull up power rail from +3VS_WLAN to +3VDS and install RN3 8. add JP4102 between +3VDS and +3V_WWAN

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/11/5	Deciphered Date	2010/12/01
Title	HW_PIR1		
Size	Document Number		Rev
Custom	LA-B181P		0.5
Date:	Tuesday, March 25, 2014	Sheet	62 of 62