2012 S-Series Richie 13.3"
UMA/DIS Muxless Schematic

Intel Chief River Platform
Ivy Bridge (rPGA989)
Panther Point PCH

REV:-1
2012-03-15

DY:No stuff
DIS_PX:Only DIS install

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Cover Page***		
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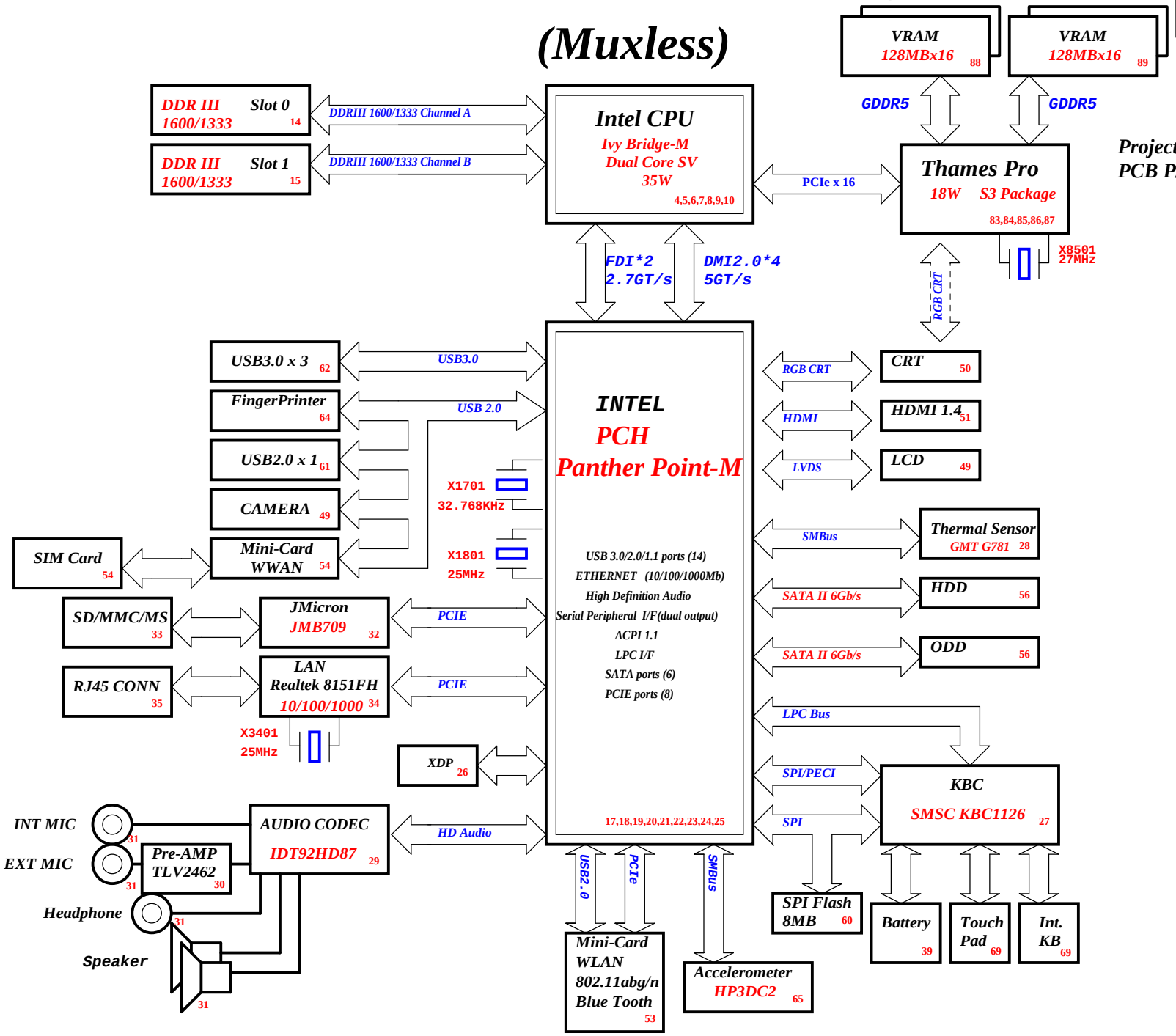
S-Series Richie Block Diagram (Muxless)



Project code:91.4RS01.001
PCB P/N:11241

SYSTEM DC/DC TPS51461RGER 48	
INPUTS	OUTPUTS
DCBATOUT	+VCCSA

CPU DC/DC ISL95832HRTZ 42~44	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS51211DSCR 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0

SYSTEM DC/DC TPS51123RGER 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC TPS51216RUKR 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

GFX DC/DC ISL95832HRTZ 42~44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

VGA UP1527QQDD 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

CHARGER BQ24736RGRR 40	
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC RT8068AZQWID 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

SYSTEM DC/DC FDMC7696 93	
INPUTS	OUTPUTS
1D5V_S3	1V_VGA_S0

Switches	
INPUTS	OUTPUTS
1D5V_S3 5V_S5 3D3V_S5	1D5V_S0 5V_S0 3D3V_S0

PCB 8 LAYER

L1:	Top
L2:	GND
L3:	Signal
L4:	Signal
L5:	VCC
L6:	Signal
L7:	GND
L8:	Bottom

PCB LAYER

L1:Top	L5:Vcc
L2:GND	L6:Signal
L3:Signal	L7:GND
L4:Signal	L8:Bottom

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Title: Block Diagram

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PCH Strapping

Chief River Schematic Checklist Rev0.72

Name	Schematics Notes
SPKR	The signal has a weak internal pull-down. Note: the internal pull-down is disabled after PLTRST# deasserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Cougar Point will disable the TCO Timer system reboot feature).
INIT3_3V#	This signal has a weak internal pull-up. Note: The internal pull-up is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled low. Leave as "No Connect".
INTVRMEN	Integrated 1.05 V VRM Enable / Disable. Integrated 1.05 V VRMs is enabled when high NOTE: This signal should always be pulled high External 1.05 V VRM Enable / Disable. Integrated 1.05 V VRMs is enabled when Low. NOTE: This signal should be pulled down to GND through 330 kOhms resistor
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Used as GPIO only. Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3 power rail.
DF_TVS	This signal is a strap for selecting DMI and FDI termination voltage. For Ivy Bridge processor only implementation: DF_TVS needs to be pulled up to VccDFTERM power rail through 2.2 kOhms ±5% resistor. For future processor compatibility: It needs to be connected to PROC_SELECT through a 1.0 kOhms ±5% series resistor. The PROC_SELECT signal would need a 2.2 kOhms ±5% pull-up resistor to PCH VccDFTERM.
SATA1GP/ GPIO19	This Signal has a weak internal pull-up. Note: the internal pull-up is disabled after PLTRST# deasserts. This field determines the destination of accesses to the BIOS memory range. Also controllable via Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 1 strap. Bit11 Bit 10 Boot BIOS Destination 0 1 Reserved 1 0 PCI 1 1 SPI 0 0 LPC NOTE: If option 00 LPC is selected BIOS may still be placed on LPC, but all platforms with Cougar Point require SPI flash connected directly to the Cougar Point's SPI bus with a valid descriptor in order to boot. NOTE: Booting to PCI is intended for debut/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or via Boot BIOS Destination Bit will not affect SPI accesses initiated by Management Engine or Integrated GbE LAN. NOTE: PCI Boot BIOS destination is not supported on mobile.
SATA2GP/ GPIO36	Reserved. This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled high when strap is sampled.
SATA3GP/ GPIO37	Reserved This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled high when strap is sampled.
HDA_DOCK_EN# /GPIO33	High Definition Audio Dock Enable: This signal controls the external Intel HD Audio docking isolation logic. This is an active-low-signal. When deasserted the external docking switch is in isolate mode. When asserted the external docking switch electrically connects the Intel? HD Audio dock signals to the corresponding Cougar Point signals. This signal can instead be used as GPIO33.
HDA_SDO	Signal has a weak internal pull-down. If strap is sampled low, the security measures defined in the Flash Descriptor will be in effect (default). If sampled high, the Flash Descriptor Security will be overridden. This strap should only be asserted high via external pull-up in manufacturing/debug environments ONLY. Note: The weak internal pull-down is disabled after PLTRST# deasserts. Asserting the HDA_SDO high on the rising edge of RSMRST# will also halt Intel Management Engine after chipset bring up and disable runtime Intel Management Engine features. This is a debug mode and must not be asserted after manufacturing/ debug.
HDA_SYNC	This signal has a weak internal pull-down. On Die PLL VR is supplied by 1.5 V from VCCVRM when sampled high, 1.8 V from VCCVRM when sampled low. Needs to be pulled High for Chief River platform.
GPIO15	TLS Confidentiality Low (0) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality This signal has a weak internal pull-down. NOTE: The weak internal pull-down is disabled after RSMRST# deasserts. NOTE: A strong pull-up may be needed for GPIO functionality
L_DDC_DATA	LVDS Detected. When '1'- LVDS is detected; When '0'- LVDS is not detected. This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts.
SDVO_CTRLDATA	Port B Detected When '1'- Port B is detected; When '0'- Port B is not detected. This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts.
DDPC_CTRLDATA	Port C Detected. When '1'- Port C is detected; When '0'- Port C is not detected This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts
DDPD_CTRLDATA	Port D Detected. When '1'- Port D is detected; When '0'- Port D is not detected This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts.
DSWVRMEN	Deep S4/S5 Well On-Die Voltage Regulator Enable If strap is sampled high, the Integrated Deep S4/S5 Well (DSW) On-Die VR mode is enabled.
GPIO28	The On-Die PLL voltage regulator is enabled when sampled high. When sampled low the On-Die PLL Voltage Regulator is disabled. If not used, 8.2-kΩ to 10-kΩ pull-up to +V3.3A power-rail. Note: This signal has a weak internal pull-up. The internal pull-up is disabled after RSMRST# deasserts.
GPIO29/ SLP_LAN#	GPIO29 is multiplexed with SLP_LAN#. If Intel LAN is implemented on the platform, SLP_LAN# must be used to control the power to the PHY LAN (no other implementation is supported). If integrated Intel LAN is not supported on the platform, GPIO29 can be used as a normal GPIO. A soft strap determines the functionality of GPIO29, either as SLP_LAN# or GPIO. By default, the soft strap enables SLP_LAN# functionality on the pin. If the soft trap is changed to enable GPIO functionality, then SLP_LAN# functionality is no longer available, and the signal can be used as a normal GPIO (default to GPI).

Processor Strapping

Chief River Schematic Checklist Rev0.72

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[0]		Connect a series 1K ohm resistor on the critical CFG[0] trace in a manner which does not introduce any stubs to CFG[0] trace. Route as needed from the opposite side of this series isolation resistor to the debug port. ITP will drive the net to GND.	
CFG[2] CFG2 is for the 16x	**PCIe Static x16 Lane Numbering Reversal.**	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed	1
CFG[4]	**Display Port Presence strap**	1:Disabled - No Physical Display Port attached to Embedded DisplayPort 0:Enabled - An external Display Port device is connected to the Embedded Display Port Pull down to GND through a 1KΩ ± 5% resistor to enable port	1
CFG[6:5]	**PCIE Port Bifurcation Straps**	00 = 1 x 8, 2 x 4 PCI Express 01 = reserved 10 = 2 x 8 PCI Express 11 = 1 x 16 PCI Express	11
CFG[17:7]	**Reserved configuration lands. A test point may be placed on the board for these lands.**		

PCIe Routing

LANE1	X
LANE2	X
LANE3	Card Reader
LANE4	Mini Card1(WLAN)
LANE5	X
LANE6	LAN
LANE7	X
LANE8	X

Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_S0 VCCSA 0D75V_S0 VCC_CORE VCC_GFXCORE VGA_CORE 1D8V_VGA_S0 3D3V_VGA_S0 1D5V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 1.0V 0.9 - 0.675V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
1D5V_S3 DDR_VREF_S3	5V 1.5V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	9V-14.1V 9V-19.5V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and 3D3V_S5 in Sx

USB 2.0 Table

Pair	Device
0	FREE
1	USB 3.0 I/O CONN. 1
2	USB 3.0 I/O CONN. 2
3	USB 3.0 I/O CONN. 3
4	FREE
5	BT WLAN combo
6	FREE
7	FREE
8	Fingerprint
9	USB 2.0 I/O CONN. 1
10	Camera
11	FREE
12	WWAN
13	FREE

USB3.0 Table

USB	
Pair	Device
1	FREE
2	I/O CONN. 1
3	I/O CONN. 2
4	I/O CONN. 3

SATA Table

SATA	
Pair	Device
0	HDD
1	ODD
2	N/A
3	N/A
4	N/A
5	N/A

SMBus ADDRESSES

I²C / SMBus Addresses Device	Ref Des	Chief River CRV Address	Hex	Bus
DIMM1 DIMM2 Touch-Pad				PCH_SMB_CLK/PCH_SMB_DATA PCH_SMB_CLK/PCH_SMB_DATA PCH_SMB_CLK/PCH_SMB_DATA
N/A				PCH_SML0_CLK/PCH_SML0_DATA
KBC G781_Thermal IC GPU_Thames PRO G-Sensor		 1001100 0X41 0X52		PCH_SML1CLK/PCH_SML1DATA PCH_SML1CLK/PCH_SML1DATA PCH_SML1CLK/PCH_SML1DATA PCH_SML1CLK/PCH_SML1DATA

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

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CPU(1/7)

IVY BRIDGE PROCESSOR (DMI,DP,PEG,FDI)

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

DP Compensation, within 500mil

1D05V_S0 — R402 1 — 24D9R2F-L-GP — DP_COMP (A18) — 4mil / 12mil

NOTE: EDP_HPD
Select a Fast FET similar to 2N7002E whose rise/ fall time is less than 6 ns.
If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.
This signal can be left as no connect if entire eDP interface is disabled.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

PEG Compensation

1D05V_S0 — R401 1 — 24D9R2F-L-GP — PEG_COMP (J22)

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

CPU1A — IVY-BRIDGE — 1 OF 9

DMI: DMI_TXN[3:0] (B27, B25, A25, B24) → DMI_RX#0..3; DMI_TXP[3:0] (B28, B26, A24, B23) → DMI_RX0..3; DMI_RXN[3:0] (G21, E22, F21, D21) → DMI_TX#0..3; DMI_RXP[3:0] (G22, D22, F20, C21) → DMI_TX0..3

Intel(R) FDI: FDI_TX_N[7:0] (A21, H19, E19, F18, B21, C20, D18, E17) → FDI0_TX#0..3, FDI1_TX#0..3; FDI_TX_P[7:0] (A22, G19, E20, G18, B20, C19, D19, F17) → FDI0_TX0..3, FDI1_TX0..3; FDI_FSYNC0 (J18), FDI_FSYNC1 (J17) → FDI0_FSYNC, FDI1_FSYNC; FDI_INT (H20); FDI_LSYNC0 (J19), FDI_LSYNC1 (H17) → FDI0_LSYNC, FDI1_LSYNC

eDP: EDP_COMPIO (A18), EDP_ICOMPO (A17), EDP_HPD (B16); EDP_AUX (C15), EDP_AUX# (D15); EDP_TX0 (C17), EDP_TX1 (F16), EDP_TX2 (C16), EDP_TX3 (G15); EDP_TX#0 (C18), EDP_TX#1 (E16), EDP_TX#2 (D16), EDP_TX#3 (F15)

PCI EXPRESS* - GRAPHICS

PEG_ICOMPI (J22), PEG_ICOMPO (J21), PEG_RCOMPO (H22)

PEG_RX#0..15: K33, M35, L34, J35, J32, H34, H31, G33, G30, E35, E34, E32, D33, D31, B33, C32 → PEG_RXN15..0 → PEG_RXN[0..15] 83

PEG_RX0..15: J33, L35, K34, H35, H32, G34, G31, F33, F30, E35, E33, E32, D34, E31, C33, B32 → PEG_RXP15..0 → PEG_RXP[0..15] 83

PEG_TX#0..15: M29, M32, M31, L32, L29, K31, K28, J30, J28, H29, G27, F29, F27, D28, F26, E25 → PEG_C_TXN15..0 → DIX_PXC401..416 → SCD22U16V2KX-GP → PEG_TXN15..0 → PEG_TXN[0..15] 83

PEG_TX0..15: M28, M33, M30, L31, L28, K30, K27, J29, J27, H28, G28, E28, F28, D27, E26, D25 → PEG_C_TXP15..0 → DIX_PXC417..432 → SCD22U16V2KX-GP → PEG_TXP15..0 → PEG_TXP[0..15] 83

GP

62.10040.821
1ST = 62.10055.551
2nd = 62.10055.321
3rd = 62.10055.731

BOM Note:1st/2nd/3rd Add in BOM

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU(1/7): DMI/PEG/FDI**

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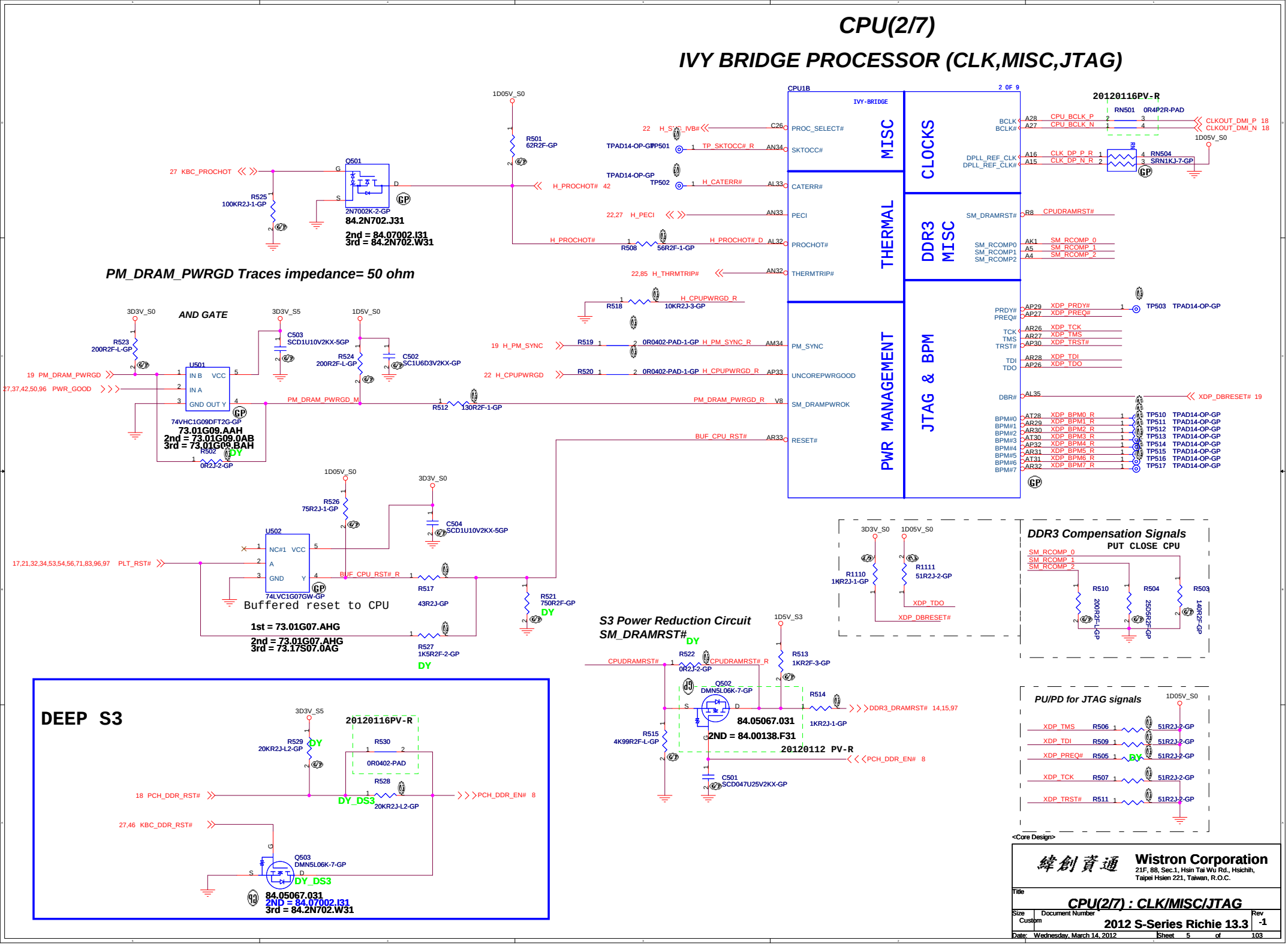
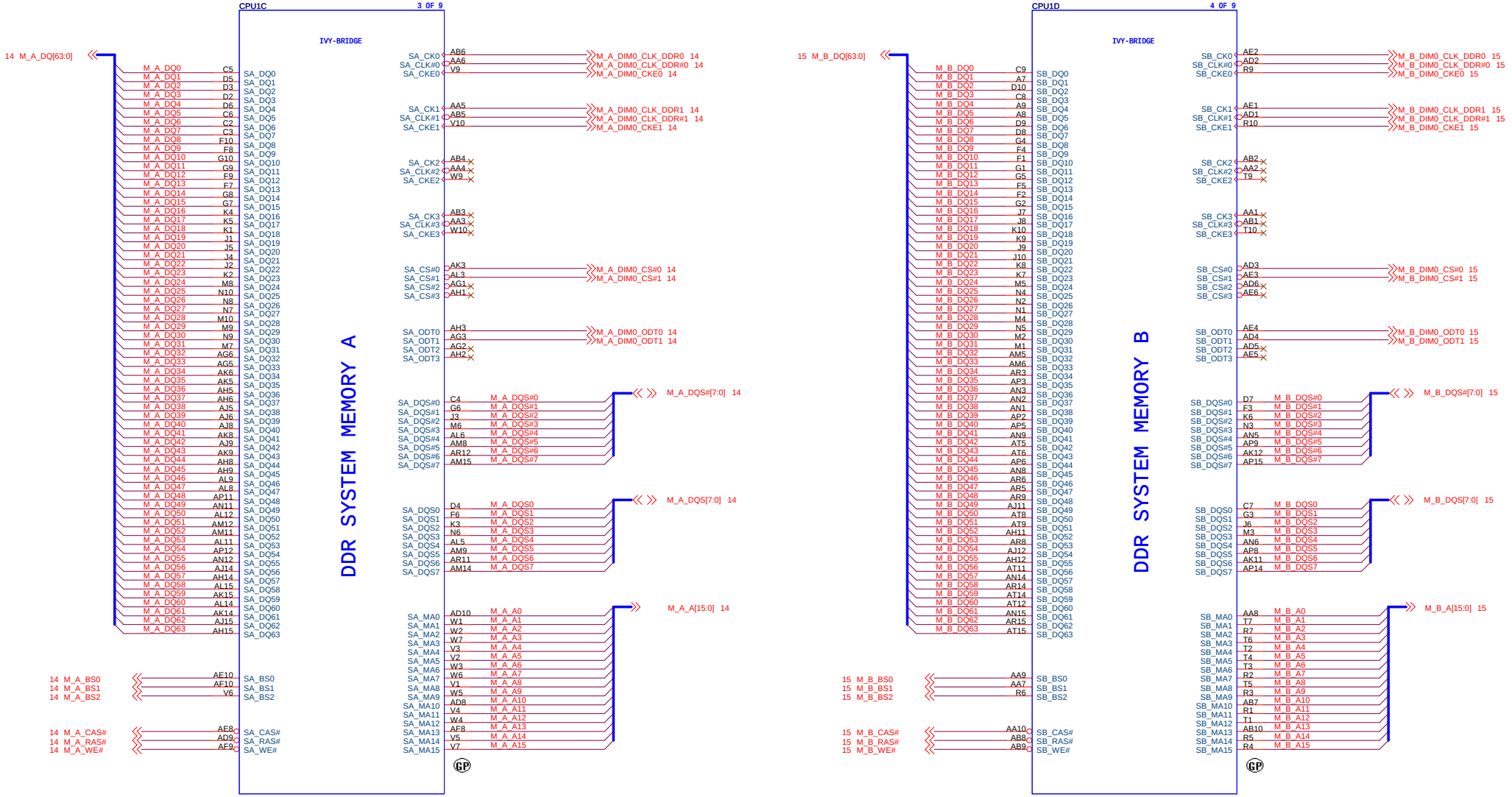
CPU(2/7)

IVY BRIDGE PROCESSOR (CLK,MISC,JTAG)



CPU(3/7)

IVY BRIDGE PROCESSOR (DDR3)



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Title: **CPU(3/7) : DDR3**

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CPU(4/7)

IVY BRIDGE PROCESSOR (POWER)

POWER

CPU1F — 6 OF 9 — IVY-BRIDGE

PROCESSOR CORE POWER

53A

VCC_CORE

Place Bottom

Place Top

C713 SC22U6D3V5MX-2GP, C722 SC22U6D3V5MX-2GP, C727 SC10U6D3V3MX-GP, C736 SC22U6D3V5MX-2GP, C714 SC22U6D3V5MX-2GP

C735 SC22U6D3V5MX-2GP, C721 SC22U6D3V5MX-2GP, C726 SC10U6D3V3MX-GP, C728 SC22U6D3V5MX-2GP, C723 SC22U6D3V5MX-2GP

C742 SC22U6D3V5MX-2GP, C701 SC10U6D3V5KX-1GP, C741 SC10U6D3V5KX-1GP, C703 SC22U6D3V5MX-2GP, C709 SC10U6D3V3MX-GP

C738 SC10U6D3V5KX-1GP, C702 SC10U6D3V5KX-1GP, C706 SC10U6D3V5KX-1GP, C707 SC10U6D3V5KX-1GP, C708 SC10U6D3V5KX-1GP

C740 SC22U6D3V5MX-2GP, C739 SC22U6D3V5MX-2GP, C704 SC22U6D3V5MX-2GP, C712 SC22U6D3V5MX-2GP, C710 SC22U6D3V5MX-2GP, C711 SC22U6D3V5MX-2GP

VCC1 AG35, VCC2 AG34, VCC3 AG33, VCC4 AG32, VCC5 AG31, VCC6 AG30, VCC7 AG29, VCC8 AG28, VCC9 AG27, VCC10 AG26, VCC11 AF35, VCC12 AF34, VCC13 AF33, VCC14 AF32, VCC15 AF31, VCC16 AF30, VCC17 AF29, VCC18 AF28, VCC19 AF27, VCC20 AF26, VCC21 AD35, VCC22 AD34, VCC23 AD33, VCC24 AD32, VCC25 AD31, VCC26 AD30, VCC27 AD29, VCC28 AD28, VCC29 AD27, VCC30 AD26, VCC31 AC35, VCC32 AC34, VCC33 AC33, VCC34 AC32, VCC35 AC31, VCC36 AC30, VCC37 AC29, VCC38 AC28, VCC39 AC27, VCC40 AC26, VCC41 AA35, VCC42 AA34, VCC43 AA33, VCC44 AA32, VCC45 AA31, VCC46 AA30, VCC47 AA29, VCC48 AA28, VCC49 AA27, VCC50 AA26, VCC51 Y35, VCC52 Y34, VCC53 Y33, VCC54 Y32, VCC55 Y31, VCC56 Y30, VCC57 Y29, VCC58 Y28, VCC59 Y27, VCC60 Y26, VCC61 V35, VCC62 V34, VCC63 V33, VCC64 V32, VCC65 V31, VCC66 V30, VCC67 V29, VCC68 V28, VCC69 V27, VCC70 V26, VCC71 U35, VCC72 U34, VCC73 U33, VCC74 U32, VCC75 U31, VCC76 U30, VCC77 U29, VCC78 U28, VCC79 U27, VCC80 U26, VCC81 R35, VCC82 R34, VCC83 R33, VCC84 R32, VCC85 R31, VCC86 R30, VCC87 R29, VCC88 R28, VCC89 R27, VCC90 R26, VCC91 P35, VCC92 P34, VCC93 P33, VCC94 P32, VCC95 P31, VCC96 P30, VCC97 P29, VCC98 P28, VCC99 P27, VCC100 P26

PROCESSOR UNCORE POWER

8.5A

1D05V_S0

C729 SC10U6D3V3MX-GP, C730 SC10U6D3V3MX-GP, C731 SC22U6D3V5MX-2GP, C732 SC10U6D3V3MX-GP, C715 SC10U6D3V3MX-GP, C716 SC22U6D3V5MX-2GP, C717 SC22U6D3V5MX-2GP, C718 SC10U6D3V3MX-GP, C733 SC10U6D3V3MX-GP, C734 SC10U6D3V3MX-GP, C719 SC10U6D3V3MX-GP, C720 SC22U6D3V5MX-2GP

VCCIO1 AH13, VCCIO2 AH10, VCCIO3 AG10, VCCIO4 AC10, VCCIO5 Y10, VCCIO6 P10, VCCIO7 U10, VCCIO8 L10, VCCIO9 J14, VCCIO10 J13, VCCIO11 J12, VCCIO12 J11, VCCIO13 H14, VCCIO14 H12, VCCIO15 H11, VCCIO16 G14, VCCIO17 G13, VCCIO18 G12, VCCIO19 F14, VCCIO20 F13, VCCIO21 F12, VCCIO22 F11, VCCIO23 E14, VCCIO24 E12, VCCIO25 E11, VCCIO26 D14, VCCIO27 D13, VCCIO28 D12, VCCIO29 D11, VCCIO30 C14, VCCIO31 C13, VCCIO32 C12, VCCIO33 C11, VCCIO34 B14, VCCIO35 B12, VCCIO36 A14, VCCIO37 A13, VCCIO38 A12, VCCIO39 A11, VCCIO40 J23

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

Route these three net together

VIDALERT# AJ29 H_CPU_SVIDALRT# R705 1 43R2J-GP VR_SVID_ALERT# 42

VIDSCLK AJ30 H_CPU_SVIDCLK H_CPU_SVIDCLK 42

VIDSOUT AJ28 H_CPU_SVIDDAT H_CPU_SVIDDAT 42

R703 1 130R2F-1-GP 1D05V_S0

reserve PAD for ESD

DY 0R2J-2-GP D701, DY 0R2J-2-GP D702

VCC_CORE

PUT CLOSE CPU

R706 100R2F-L1-GP-U

VCC_SENSE AJ35 VCCSENSE VCCSENSE 42

VSS_SENSE AJ34 VSSSENSE VSSSENSE 42

R704 100R2F-L1-GP-U

VCCIO_SENSE B10 VTT_SENSE 45

VSS_SENSE_VCCIO A10 VSSP_SENSE 45

R707 10R2F-L-GP, R708 10R2F-L-GP 1D05V_S0

PUT CLOSE CPU

Differential Sense feedback

<Core Design>

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Title: CPU(4/7) : PWR

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CPU(5/7)

IVY BRIDGE PROCESSOR (GRAPHICS POWER)

33A

POWER

VCC_GFXCORE

Under Socket and Closed to CPU

C820 SC22U6D3V5MX-2GP, C821 SC22U6D3V5MX-2GP, C822 SC22U6D3V5MX-2GP, C823 SC10U6D3V5KX-1GP, C824 SC22U6D3V5MX-2GP, C825 SC22U6D3V5MX-2GP

VCC_GFXCORE

Closed to CPU Socket

C826 SC10U6D3V5KX-1GP, C827 SC22U6D3V5MX-2GP, C828 SC22U6D3V5MX-2GP, C829 SC22U6D3V5MX-2GP, C830 SC22U6D3V5MX-2GP, C831 SC22U6D3V5MX-2GP

CPU1G — IVY-BRIDGE — 7 OF 9

GRAPHICS

VAXG1 AT24, VAXG2 AT23, VAXG3 AT21, VAXG4 AT20, VAXG5 AT18, VAXG6 AT17, VAXG7 AR24, VAXG8 AR23, VAXG9 AR21, VAXG10 AR20, VAXG11 AR18, VAXG12 AR17, VAXG13 AP24, VAXG14 AP23, VAXG15 AP21, VAXG16 AP20, VAXG17 AP18, VAXG18 AP17, VAXG19 AN24, VAXG20 AN23, VAXG21 AN21, VAXG22 AN20, VAXG23 AN18, VAXG24 AN17, VAXG25 AM24, VAXG26 AM23, VAXG27 AM21, VAXG28 AM20, VAXG29 AM18, VAXG30 AM17, VAXG31 AL24, VAXG32 AL23, VAXG33 AL21, VAXG34 AL20, VAXG35 AL18, VAXG36 AL17, VAXG37 AK24, VAXG38 AK23, VAXG39 AK21, VAXG40 AK20, VAXG41 AK18, VAXG42 AK17, VAXG43 AJ24, VAXG44 AJ23, VAXG45 AJ21, VAXG46 AJ20, VAXG47 AJ18, VAXG48 AJ17, VAXG49 AH24, VAXG50 AH23, VAXG51 AH21, VAXG52 AH20, VAXG53 AH18, VAXG54 AH17

SENSE LINES

VAXG_SENSE AK35 — VCCGT_SENSE 42
VSSAXG_SENSE AK34 — VSSGT_SENSE 42

R820 100R2F-L1-GP-U — VCC_GFXCORE
R819 100R2F-L1-GP-U

VREF

SM_VREF AL1 — +V_SM_VREF_CNT

B4:VREF_DQ CHA
D1:VREF_DQ CHB

SA_DIMM_VREFDQ B4 — DDR_VREF_S3_B4
SB_DIMM_VREFDQ D1 — DDR_VREF_S3_D1

R815 1KR2F-3-GP DY, R816 1KR2F-3-GP DY

C801 SC2D2U10V2ZY-2GP DY, C802 SC2D2U10V2ZY-1GP DY

DDR3 -1.5V RAILS

VDDQ1 AE7, VDDQ2 AE4, VDDQ3 AE1, VDDQ4 AC7, VDDQ5 AC4, VDDQ6 AC1, VDDQ7 Y7, VDDQ8 Y4, VDDQ9 Y1, VDDQ10 U7, VDDQ11 U4, VDDQ12 U1, VDDQ13 P7, VDDQ14 P4, VDDQ15 P1

C803 SC10U6D3V3MX-GP, C804 SC10U6D3V5KX-1GP, C805 SC10U6D3V5KX-1GP, C806 SC10U6D3V5KX-1GP, C807 SC10U6D3V5KX-1GP, C808 SC10U6D3V5KX-1GP

12~16A

1D5V_S0

330U*1 10U*6

TC803 ST330U2D5VBM-1-GP
80.3371V.A2L
2nd = 77.22771.00L
20120131PVR

SA RAIL

VCCSA1 M27, VCCSA2 M26, VCCSA3 L26, VCCSA4 J26, VCCSA5 J25, VCCSA6 J24, VCCSA7 H26, VCCSA8 H25

6A

VCCSA

C813 SC10U6D3V5KX-1GP, C814 SC10U6D3V5KX-1GP, C815 SC10U6D3V5KX-1GP, TC802 SF330U2D5VDM-1GP DY

1st = 77.23371.13L
2ND = 79.33719.L01

VCCSA

R0801 need be close to pin H23.

R801 100R2J-2-GP DY

VCCSA_SENSE H23 — VCCUSA_SENSE — VCCUSA_SENSE 48

1.8V RAIL

1.5A

1D8V_S0

VCCPLL1 B6, VCCPLL2 A6, VCCPLL3 A2

C819 SC10U6D3V5KX-1GP DY, C816 SC10U6D3V5KX-1GP, C817 SC1U10V2KX-1GP, C818 SC1U10V2KX-1GP

MISC

VCCSA_VID0 C22 — H_FC_C22
VCCSA_VID1 C24 — VCCSA_SEL

H_FC_C22 48
VCCSA_SEL 48

R804 1KR2J-1-GP, R806 1KR2J-1-GP

VCCIO_SEL A19 — H_VCCP_SEL

SNB: No Connect
IVB: VSS

R817 0R2J-2-GP DY — H_SNB_IVB#_PWRCTRL 45

R818 0R2J-2-GP DY

H_VCCP_SEL	Voltage
1	1.05V
0	1.0V

S3 Power Reduction Circuit Processor VREF_DQ Implementation

1D5V_S3 — R821 1KR2F-3-GP DY — R822 1KR2F-3-GP DY

DDR_VREF_S3 — 20120112_PV-R — R807 0R0402-PAD

+V_SM_VREF — 84.05067.031
1st = 84.2N702.J31
2ND = 84.07002.I31
3rd = 84.2N702.W31

R811 0R2J-2-GP DY

Q801 DMN5L06K-7-GP

+V_SM_VREF_CNT — R803 100KR2J-1-GP DY

R802 0R2J-2-GP DY

5 PCH_DDR_EN# — 20120112_PV-R — R823 0R0402-PAD

C832 SC470P50V2KX-3GP

19,27,29,34,35,36,37,45,46,47,48,92,93 PM_SLP_S3#

CAD Note: +V_SM_VREF should have 10 mil trace width

M3 - Processor Generated SO-DIMM VREF_DQ

VCCGT_SENSE
VSSGT_SENSE

D801 0R2J-2-GP DY, D802 0R2J-2-GP DY

reserve PAD for ESD

20120112 PV-R

14 M_VREF_DQ_DIMM0
15 M_VREF_DQ_DIMM1

1st = 84.05067.031
2nd = 84.00138.F31
3rd = 84.05067.031

PCH_DDR_EN# — Q802 AP2302GN-HF-GP — R810 0R2J-2-GP DY

DDR_VREF_S3_B4
DDR_VREF_S3_D1

Q803 AP2302GN-HF-GP — R814 0R2J-2-GP DY

5 PCH_DDR_EN#

1st = 84.05067.031
2nd = 84.00138.F31
3rd = 84.05067.031

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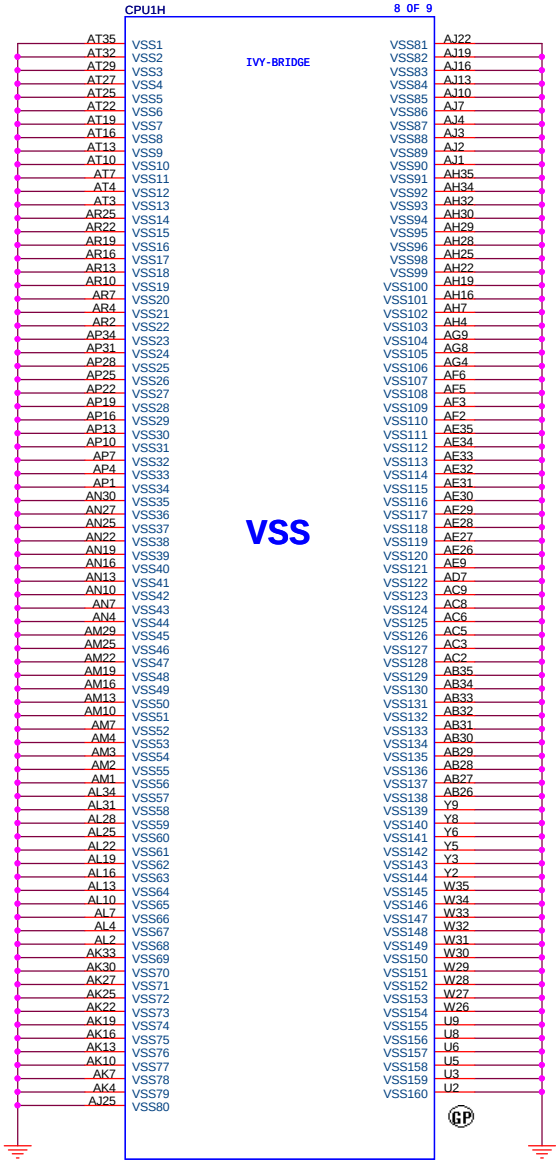
Title: CPU(5/7) : GFX/PWR

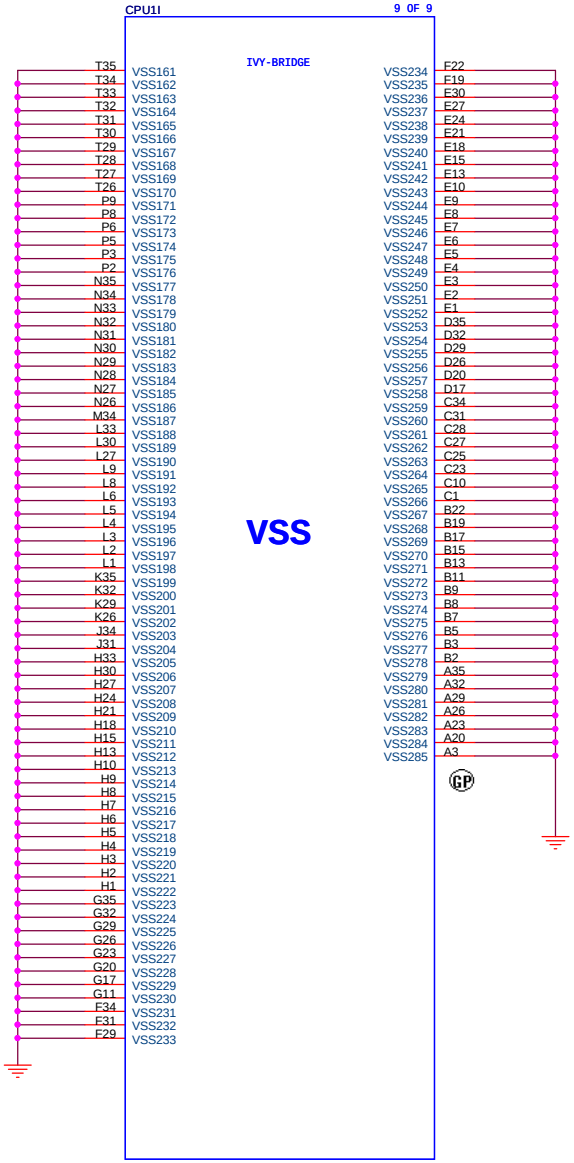
Size: Custom | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

Date: Wednesday, March 14, 2012 | Sheet 8 of 103

CPU(6/7)

IVY BRIDGE PROCESSOR (GND)





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Title: CPU(6/7) : GND

Size	Document Number	Rev
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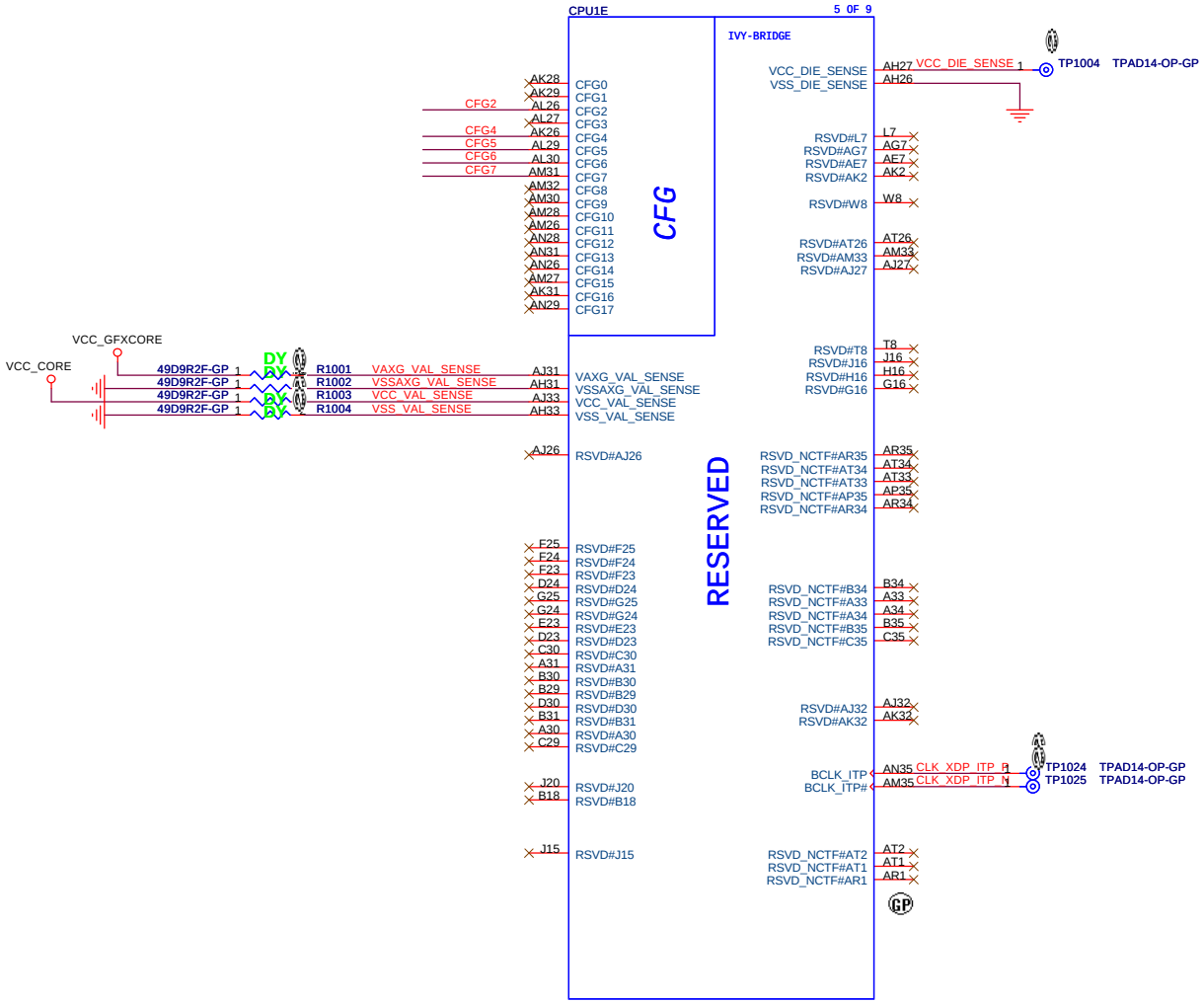
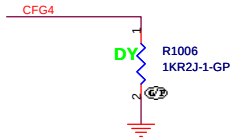
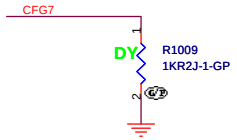
CPU(7/7)

IVY BRIDGE PROCESSOR (RESERVED)

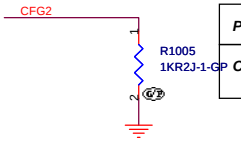




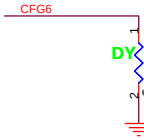
Display Port Presence Strap	0:Enable eDP
CFG4	1:(Default) Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

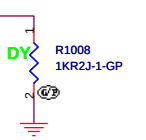


PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



PEG Static Lane Reversal	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed





PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

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Title: CPU(7/7): CFG/RSVD/DDR3_VREF

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

Date: Wednesday, March 14, 2012 Sheet 10 of 103

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Title: CPU XDP

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

Date: Wednesday, March 14, 2012 | Sheet 11 of 103

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Title: ***RESERVED***

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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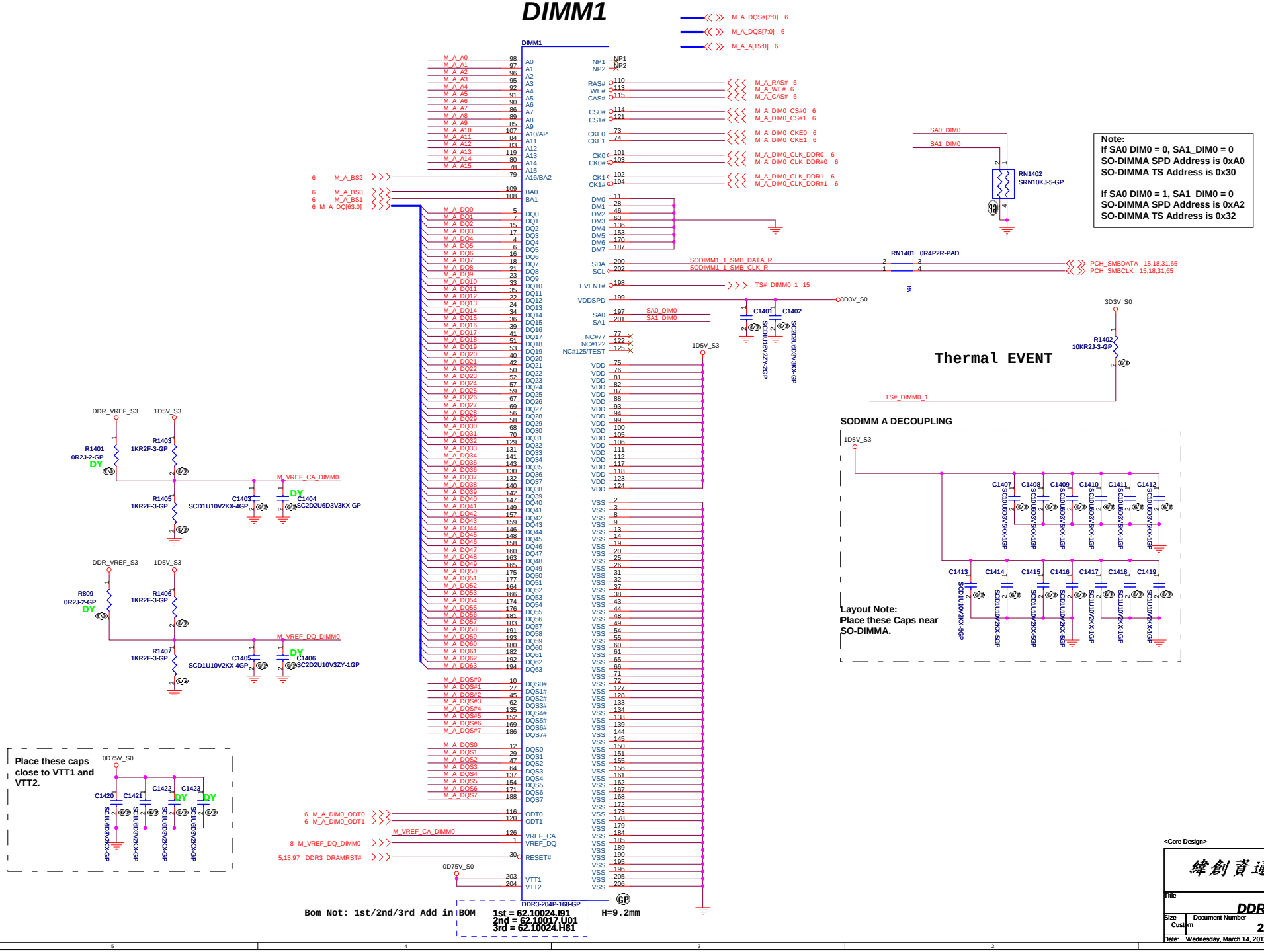
DIMM1



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Title	DDR3 SO-DIMM1		
Size: Custom	Document Number: 2012 S-Series Richie 13.3	Rev: -1	
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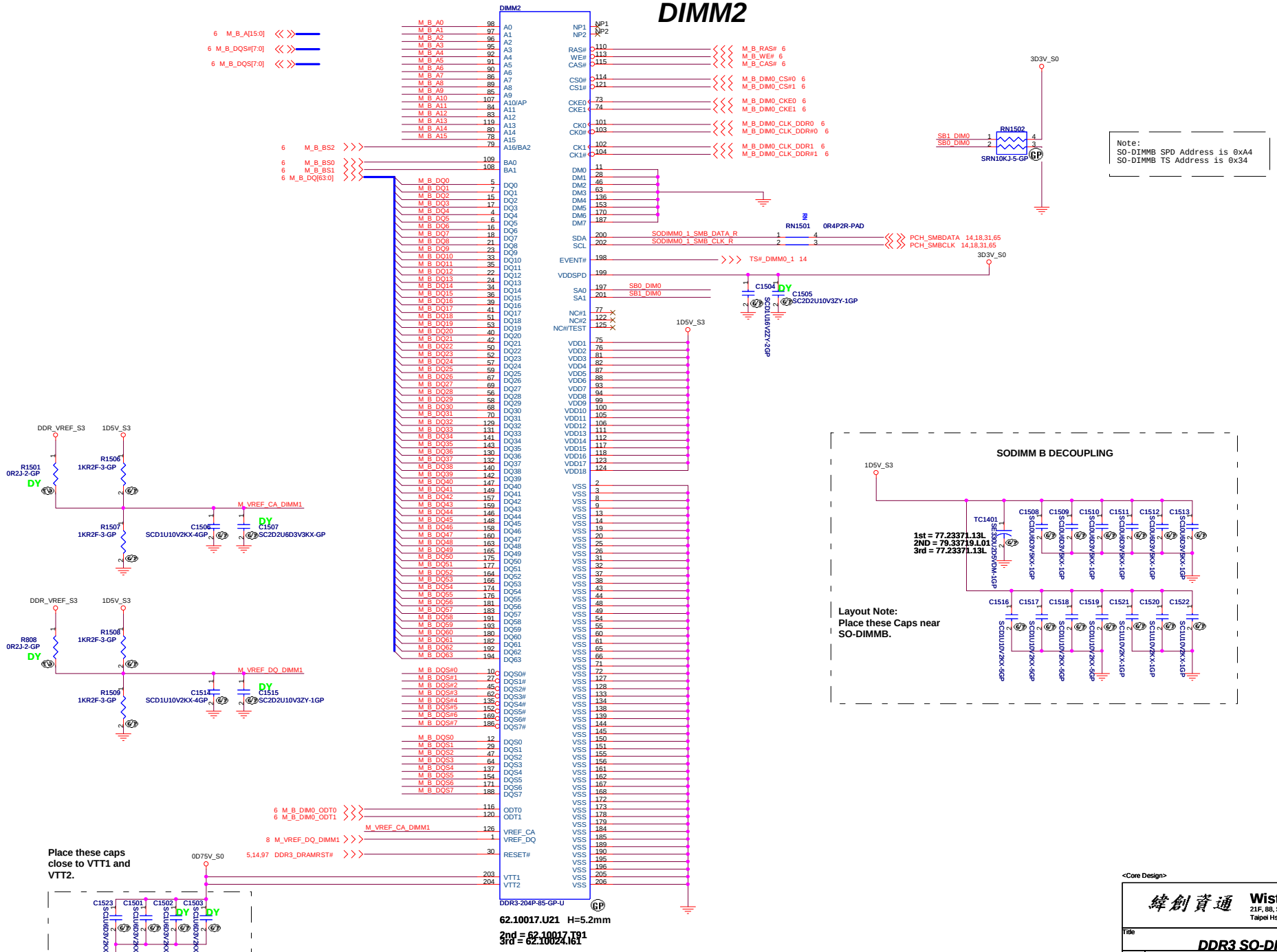
DIMM2



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Title: **DDR3 SO-DIMM2**

Size	Document Number	Rev
Custom	2012 S-Series Richie 13.3	-1

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Title: ***RESERVED***

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PCH(1/9)

INTVRMEN- Integrated
SUS 1.05V VRM Enable
High - Enable internal VRs

PCH1A 1 OF 10

RTC_X1 A20 RTCX1
RTC_X2 C20 RTCX2
RTC_RST# D20 RTCRST#
SRTC_RST# G22 SRTCRST#
54,97 INTRUDER# K22 INTRUDER#
PCH_INTVRMEN C17 INTVRMEN

LPC_AD[3:0] 27,71
FWH0/LAD0 C38 LPC_AD0
FWH1/LAD1 A38 LPC_AD1
FWH2/LAD2 B37 LPC_AD2
FWH3/LAD3 C37 LPC_AD3
FWH4/LFRAME# D36 LPC_FRAME# R 1 R1726 22R2J-2-GP LPC_FRAME# 27,71
LDRQ0# E36
LDRQ1#/GPIO23 K36 PCH_GPIO23 1 TP1701 TPAD14-OP-GP
SERIRQ V5 SIRQ 27,71

RTC_AUX_S5 R1709 1MR2J-1-GP
R1710 330KR2J-L1-GP PCH_INTVRMEN

29,97 HDA_SDOUT_CODEC
29,97 HDA_RST#_CODEC
29 HDA_SYNC_CODEC
29 HDA_SPKR
RN1701 SRN33J-7-GP
R1711 1 2 0R0402-PAD
20120112 PV-R

HDA_BIT_CLK N34 HDA_BCLK
HDA_SYNC L34 HDA_SYNC
PCH_HDA_SPKR T10 SPKR
PCH_HDA_RST# K34 HDA_RST#
HDA_SYNC_C
E34 HDA_SDIN0
G34 HDA_SDIN1
C34 HDA_SDIN2
A34 HDA_SDIN3
HDA_SDO_R
HDA_SDO A36 HDA_SDO

29 HDA_SDIN0_CODEC
68 HDD_HALTLED
1KR2J-1-GP R1712 1
HDD_HALTLED_R C36 HDA_DOCK_EN#/GPIO33
ISO_PREP# N32 HDA_DOCK_RST#/GPIO13

PCH_JTAG_TCK_BUF J3 JTAG_TCK
PCH_JTAG_TMS H7 JTAG_TMS
PCH_JTAG_TDI K5 JTAG_TDI
PCH_JTAG_TDO H1 JTAG_TDO

60 PCH_SPI_CLK T3 SPI_CLK
60 PCH_SPI_CS#0 Y14 SPI_CS0#
27,71 SPI_CS1# T1 SPI_CS1#
60 PCH_SPI_MOSI V4 SPI_MOSI
60 PCH_SPI_MISO U3 SPI_MISO

PANTHER-GP-NF

SATA0RXN AM3 SATA_RXN0 56
SATA0RXP AM1 SATA_RXP0 56
SATA0TXN AP7 SATA_TXN0 56
SATA0TXP AP5 SATA_TXP0 56 HDD
SATA1RXN AM10 SATA_RXN1 56
SATA1RXP AM8 SATA_RXP1 56
SATA1TXN AP11 SATA_TXN1 56
SATA1TXP AP10 SATA_TXP1 56 ODD
SATA2RXN AD7
SATA2RXP AD5
SATA2TXN AH5
SATA2TXP AH4
SATA3RXN AB8
SATA3RXP AB10
SATA3TXN AF3
SATA3TXP AF1
SATA4RXN Y7
SATA4RXP Y5
SATA4TXN AD3
SATA4TXP AD1
SATA5RXN Y3
SATA5RXP Y1
SATA5TXN AB3
SATA5TXP AB1
SATAICOMPO Y11
SATAICOMPI Y10 SATA_COMP R1713 1 2 37D4R2F-GP 1D05V_S0
SATA3RCOMPO AB12
SATA3COMPI AB13 SATA3_COMP R1714 1 2 49D9R2F-GP 1D05V_S0
SATA3RBIAS AH1 RBIAS_SATA3 1 R1715 750R2F-GP
NEED TO PLACE CLOSE TO PCH
SATALED# P3 SATA_LED# R1716 10KR2J-3-GP 3D3V_S0 SATA_LED# 68
SATA0GP/GPIO21 V14 SATA0GP_GPIO21 22
SATA1GP/GPIO19 P1 SATA_ODD_DET# 56

3D3V_S5
R1725 1KR2J-1-GP
BAT_GRNLED# S
BAT_GRNLED# D
10KR2J-3-GP R1701
27,82 BAT_GRNLED# G
84.00084.F31
2nd = 84.BSS84.B31
BSS84-7-F-GP Q1701

10KR2J-3-GP R1702
5,21,32,34,53,54,56,71,83,96,97 PLT_RST# G
84.00084.F31
2nd = 84.BSS84.B31
BSS84-7-F-GP Q1702

3D3V_S5
R1724 1KR2J-1-GP HDA_SYNC
R1729 1 10KR2J-3-GP ISO_PREP#

For Flash Descriptor Security Override HW strap

RTC Battery

RTC1 PWR GND NP1 NP2
BAT-060003HA0J2M213ZL-GP-U
62.70014.001
2nd = 62.70001.061
20120314 MV
20120315 MV

+RTC_VCC R1720 1 1KR2J-1-GP RTC_PWR
3D3V_AUX_S5 U1701 CH715FGP-GP-U
C1705 SC1U10V3ZY-6GP
RTC_AUX_S5
83.R0304.D81
2ND = 83.00040.E81
20120210PV-R

NO REBOOT STRAP

No Reboot Strap R710	
HDA_SPKR	Low = Default High = No Reboot

3D3V_S0 R1722 10KR2J-3-GP HDA_SPKR DY
R1723 10KR2J-3-GP SIRQ

5V_S0 RN1702 SRN10KJ-5-GP
HDA_SDO_G U1704 2N7002KDW-GP
HDA_SYNC_C HDA_SYNC HDA_SDO HDA_SDO_R
84.2N702.A3F
2nd = 84.2N702.E3F
3rd = 84.2N702.F3F

3D3V_S5
PCHXDP R1717 210R2F-L-GP PCH_JTAG_TMS
PCHXDP R1718 210R2F-L-GP PCH_JTAG_TDO
PCHXDP R1719 210R2F-L-GP PCH_JTAG_TDI
RN1703
PCHXDP PCH_JTAG_TDO PCH_JTAG_TDI PCH_JTAG_TMS
SRN100J-4-GP
PCHXDP R1721 51R2J-2-GP PCH_JTAG_TCK_BUF
R1727 DY 1KR2J-1-GP HDD_HALTLED_R
R1728 20KR2J-L2-GP HDA_SDO

LAYOUT NOTE:
JTAG_TMS TERMINATIONS NEED TO BE PLACED NEAR PCH
JTAG_TDI TERMINATIONS NEED TO BE PLACED NEAR PCH
JTAG_TDO TERMINATIONS NEED TO BE PLACED NEAR XDP
JTAG_TCK TERMINATIONS NEED TO BE PLACED NEAR PCH

X1701 X-32D768KHZ-34GPU
C1702 7pF20PPM SC6P50V2CN-1GP
C1703 SC6P50V2CN-1GP
82.20312MV
82.30001.661
2ND = 82.30001.B21

R1706 10MR2J-L-GP
R1705 20KR2J-L2-GP
C1701 SC1U10V2KX-1GP
R1707 DY 330KR2J-L1-GP PCH_INTVRMEN
R1708 20KR2J-L2-GP
C1704 SC1U10V2KX-1GP
G1701 GAP-OPEN

<Core Design>

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Title: PCH(1/9) : HDA/JTAG/SATA
Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1
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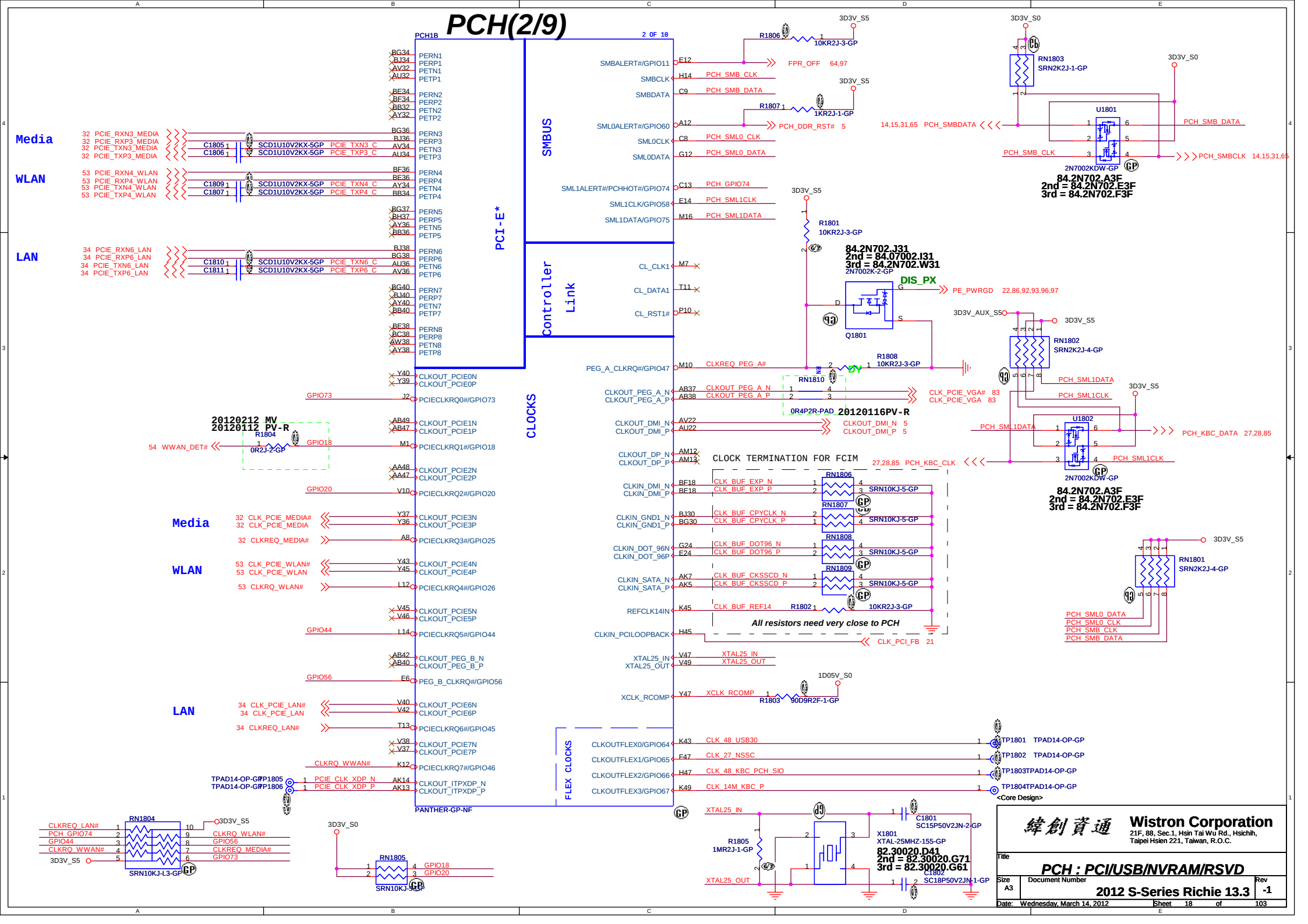
PCH(2/9)


PCH1B
2 OF 10
PCI-E*
SMBUS
Controller Link
CLOCKS
FLEX CLOCKS
PANTHER-GP-NF
Media
WLAN
LAN
PERN1 PERP1 PETN1 PETP1
PERN2 PERP2 PETN2 PETP2
PERN3 PERP3 PETN3 PETP3
PERN4 PERP4 PETN4 PETP4
PERN5 PERP5 PETN5 PETP5
PERN6 PERP6 PETN6 PETP6
PERN7 PERP7 PETN7 PETP7
PERN8 PERP8 PETN8 PETP8
SMBALERT#/GPIO11
SMBCLK
SMBDATA
SML0ALERT#/GPIO60
SML0CLK
SML0DATA
SML1ALERT#/PCHHOT#/GPIO74
SML1CLK/GPIO58
SML1DATA/GPIO75
CL_CLK1
CL_DATA1
CL_RST1#
PEG_A_CLKRQ#/GPIO47
CLKOUT_PCIE0N CLKOUT_PCIE0P
CLKOUT_PCIE1N CLKOUT_PCIE1P
CLKOUT_PCIE2N CLKOUT_PCIE2P
CLKOUT_PCIE3N CLKOUT_PCIE3P
CLKOUT_PCIE4N CLKOUT_PCIE4P
CLKOUT_PCIE5N CLKOUT_PCIE5P
CLKOUT_PCIE6N CLKOUT_PCIE6P
CLKOUT_PCIE7N CLKOUT_PCIE7P
CLKOUT_PEG_A_N CLKOUT_PEG_A_P
CLKOUT_PEG_B_N CLKOUT_PEG_B_P
CLKOUT_DMI_N CLKOUT_DMI_P
CLKOUT_DP_N CLKOUT_DP_P
CLKOUT_ITPXDP_N CLKOUT_ITPXDP_P
CLKIN_DMI_N CLKIN_DMI_P
CLKIN_GND1_N CLKIN_GND1_P
CLKIN_DOT_96N CLKIN_DOT_96P
CLKIN_SATA_N CLKIN_SATA_P
REFCLK14IN
CLKIN_PCILOOPBACK
XTAL25_IN XTAL25_OUT
XCLK_RCOMP
CLOCK TERMINATION FOR FCIM
All resistors need very close to PCH
CLKOUTFLEX0/GPIO64
CLKOUTFLEX1/GPIO65
CLKOUTFLEX2/GPIO66
CLKOUTFLEX3/GPIO67
GPIO73 GPIO18 GPIO20 GPIO56 GPIO44
PCIECLKRQ0#/GPIO73
PCIECLKRQ1#/GPIO18
PCIECLKRQ2#/GPIO20
PCIECLKRQ3#/GPIO25
PCIECLKRQ4#/GPIO26
PCIECLKRQ5#/GPIO44
PEG_B_CLKRQ#/GPIO56
PCIECLKRQ6#/GPIO45
PCIECLKRQ7#/GPIO46
CLKRQ_WWAN#
20120212 MV
20120112 PV-R
20120116PV-R
84.2N702.J31
2nd = 84.07002.I31
3rd = 84.2N702.W31
84.2N702.A3F
2nd = 84.2N702.E3F
3rd = 84.2N702.F3F
82.30020.D41
2nd = 82.30020.G71
3rd = 82.30020.G61
DIS_PX
0R4P2R-PAD
SRN10KJ-5-GP
SRN10KJ-L3-GP
SRN2K2J-1-GP
SRN2K2J-4-GP
2N7002K-2-GP
2N7002KDW-GP
SCD1U10V2KX-5GP
SC15P50V2JN-2-GP
SC18P50V2JN-1-GP
XTAL-25MHZ-155-GP
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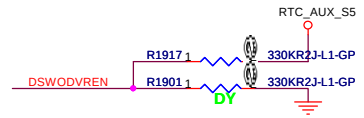
PCH : PCI/USB/NVRAM/RSVD
2012 S-Series Richie 13.3
Wednesday, March 14, 2012
Sheet 18 of 103

PCH(3/9)

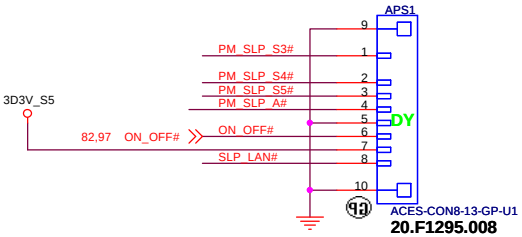
DSWODVREN - On Die DSW VR Enable	
HIGH (R1917 STUFFED, R1901 UNSTUFFED	Enabled (DEFAULT)
LOW (R1901 STUFFED, R1917 UNSTUFFED	Disabled



Intel ME-EC Interaction Signal List with and without M3 support

Signal Name	Platform With M3 Support (e.g., Intel AMT)	Platform Without M3 Support
SUSPWRDNACK(GPIO30)	Required	Required
ACPRESENT(GPIO31)	Required	Required
SLP_A#	Required	(Tie to SLP_S3#) Note: If SLP_S3# is not routed from PCH to EC, then SLP_A# becomes required from Intel ME-EC prespecrive.

AMT/ME COMPLIANCY TEST CONN.



<Core Design>

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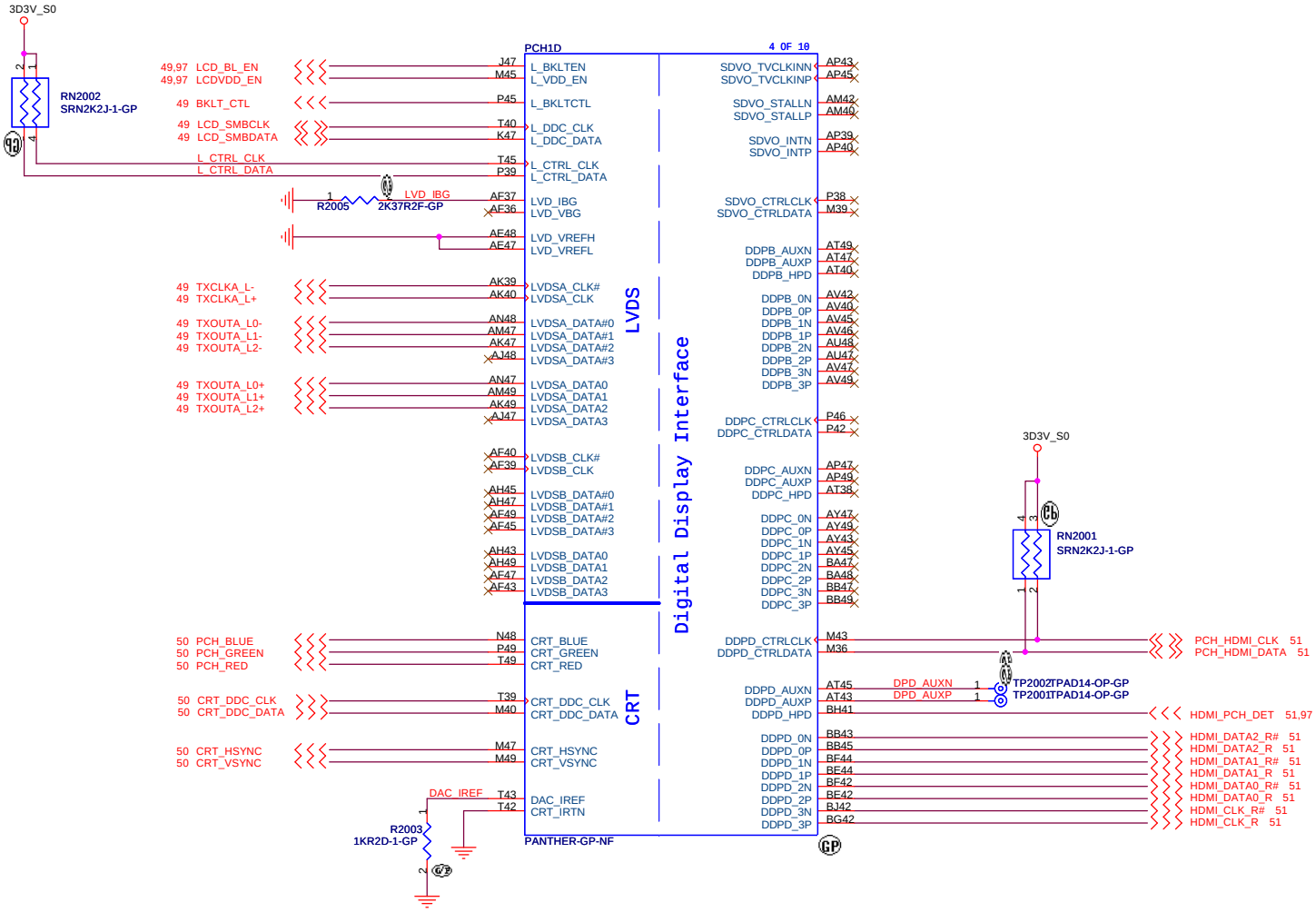
Title: PCH(3/9) : DMI/FDI/PM

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

Date: Wednesday, March 14, 2012 Sheet 19 of 103

PCH(4/9)



<Core Design>

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Title: **PCH(4/9) : LVDS/CRT/DDI**

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

Date: Wednesday, March 14, 2012 Sheet 20 of 103

PCH(5/9)

GPIO Table

S 2012 Chief River	PCH GPIO 52
Richie U&D (13 inches)	1
Rocky U&D (14 inches)	1
Rocky U&D (15/17 inches)	0

Boot BIOS Strap

GNT1#/GPIO51	SATA1GP#/GPIO19	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI(Default)

USB 3.0/2.0 Port Pairing

USB 3.0 Port	USB 2.0 Port
Port 1	Port 0
Port 2	Port 1
Port 3	Port 2
Port 4	Port 3

USB3.0 Table

USB	
Pair	Device
1	FREE
2	I/O CONN. 1
3	I/O CONN. 2
4	I/O CONN. 3

USB2.0 Table

USB	
Pair	Device
0	FREE
1	USB 3.0 I/O CONN. 1
2	USB 3.0 I/O CONN. 2
3	USB 3.0 I/O CONN. 3
4	FREE
5	BT WLAN combo
6	FREE
7	FREE
8	Fingerprint
9	USB 2.0 I/O CONN. 1
10	Camera
11	FREE
12	WWAN
13	FREE

PCH1E — 5 OF 10

RSVD: RSVD1 AY7, RSVD2 AV7, RSVD3 AU3, RSVD4 BG4, RSVD5 AT10, RSVD6 BC8, RSVD7 AU2, RSVD8 AT4, RSVD9 AT3, RSVD10 AT1, RSVD11 AY3, RSVD12 AT5, RSVD13 AV3, RSVD14 AV1, RSVD15 BB1, RSVD16 BA3, RSVD17 BB5, RSVD18 BB3, RSVD19 BB7, RSVD20 BE8, RSVD21 BD4, RSVD22 BF6, RSVD23 AV5, RSVD24 AV10, RSVD25 AT8, RSVD26 AY5, RSVD27 BA2, RSVD28 AT12, RSVD29 BE3

TP: TP1 BG26, TP2 BJ26, TP3 BH25, TP4 BJ16, TP5 BG16, TP6 AH38, TP7 AH37, TP8 AK43, TP9 AK45, TP10 C18, TP11 N30, TP12 H3, TP13 AH12, TP14 AM4, TP15 AM5, TP16 Y13, TP17 K24, TP18 L24, TP19 AB46, TP20 AB45, TP21 B21, TP22 M20, TP23 AY16, TP24 BG46

USB3RN1 BE28, USB3RN2 BC30, USB3RN3 BE32, USB3RN4 BJ32, USB3RP1 BC28, USB3RP2 BE30, USB3RP3 BE32, USB3RP4 BG32, USB3TN1 AV26, USB3TN2 BB26, USB3TN3 AU28, USB3TN4 AY30, USB3TP1 AU26, USB3TP2 AY26, USB3TP3 AV28, USB3TP4 AW30

62 USB3_RXN2, 62 USB3_RXN3, 62 USB3_RXN4, 62 USB3_RXP2, 62 USB3_RXP3, 62 USB3_RXP4, 62 USB3_TXN2, 62 USB3_TXN3, 62 USB3_TXN4, 62 USB3_TXP2, 62 USB3_TXP3, 62 USB3_TXP4

USBP0N C24, USBP0P A24, USBP1N C25, USBP1P B25, USBP2N C26, USBP2P A26, USBP3N K28, USBP3P H28, USBP4N E28, USBP4P D28, USBP5N C28, USBP5P A28, USBP6N C29, USBP6P B29, USBP7N N28, USBP7P M28, USBP8N L30, USBP8P K30, USBP9N G30, USBP9P E30, USBP10N C30, USBP10P A30, USBP11N L32, USBP11P K32, USBP12N G32, USBP12P E32, USBP13N C32, USBP13P A32

USB_PN1 62, USB_PP1 62, USB_PN2 62, USB_PP2 62, USB_PN3 62, USB_PP3 62 — **USB 3.0 Conn. 1 / USB 3.0 Conn. 2 / USB 3.0 Conn. 3**

USB_PN5 53, USB_PP5 53 — **BT WLAN combo**

USB_PN8 64, USB_PP8 64, USB_PN9 61, USB_PP9 61, USB_PN10 49, USB_PP10 49 — **Fingerprint / USB 2.0 Conn. 1 / Camera**

USB_PN12 54, USB_PP12 54 — **WWAN**

USBRBIAS# C33 — USB_BIAS — R2101 1 — 22D6R2F-L1-GP

USBRBIAS B33

PCI: INT_PIRQA# K40, INT_PIRQB# K38, INT_PIRQC# H38, INT_PIRQD# G38, PIRQA#, PIRQB#, PIRQC#, PIRQD#, REQ1#/GPIO50, REQ2#/GPIO52, REQ3#/GPIO54, GNT1#/GPIO51, GNT2#/GPIO53, GNT3#/GPIO55, PIRQE#/GPIO2, PIRQF#/GPIO3, PIRQG#/GPIO4, PIRQH#/GPIO5, PME#, PLTRST#

PCH_GPIO50 C46, PCH_GPIO51 D47, PCH_GPIO2 G42, PME# K10, PCI_PLTRST# C6

CLKOUT_PCI0 H49, CLKOUT_PCI1 H43, CLKOUT_PCI2 J48, CLKOUT_PCI3 K42, CLKOUT_PCI4 H40

CLK_PCI_SIO_R, CLK_PCI_FB_R, CLK_OUT_PCI2, CLK_OUT_PCI3, CLK_PCI_KBC_R

OC0#/GPIO59 A14, OC1#/GPIO40 K20, OC2#/GPIO41 B17, OC3#/GPIO42 C16, OC4#/GPIO43 L16, OC5#/GPIO9 A16, OC6#/GPIO10 D14, OC7#/GPIO14 C14

OC0# GPIO59, OC1# GPIO40, OC2# GPIO41, OC3# GPIO42, OC4# GPIO43, OC5# GPIO9, OC7# GPIO14, LANLINK_STATUS 35

PANTHER-GP-NF

3D3V_S0 — R2113 1 — 10KR2J-3-GP — PCH_GPIO51; R2109 1 — 10KR2J-3-GP — PCH_GPIO51; DY

3D3V_S0 — DY — R2112 1 — 10KR2J-3-GP — PE_GPIO0

3D3V_S0 — R2110 1 — 10KR2J-3-GP — DY — CAMERA_ON; RN2101 1,2,3,4 — ACCEL_INT, NMI_SMI_DBG#

RN2102 — SRN8K2J-2-GP — INT_PIRQA#, INT_PIRQD#, INT_PIRQB#, INT_PIRQC# — PE_GPIO1, PCH_GPIO2, PLT_DET_R, PCH_GPIO50 — 3D3V_S0

20120112 PV-R

27,69 PLT_DET; 92,93 PE_GPIO1 — R2106 1,2 — 0R0402-PAD — PLT_DET_R

49 CAMERA_ON; 83 PE_GPIO0

3D3V_S5 — 56,96 SATA_ODD_DA#; 27,71 NMI_SMI_DBG#; 65 ACCEL_INT

R2102 1 — DY — PME# — 10KR2J-3-GP

27,97 CLK_PCI_KBC; 18 CLK_PCI_FB — R2103 1,2 — 22R2J-2-GP; R2105 1,2 — 22R2J-2-GP — TPAD14-OP-GP — TP2108; TPAD14-OP-GP — TP2106; R2107 1,2 — 22R2J-2-GP — 71,97 CLK_PCI_DEBUG

3D3V_S5 — U2101 — AND GATE — A, B, VCC, GND, Y — U74LVC1G08G-AL5-R-GP-U — 73.01G08.EHG / 2nd = 73.7SZ08.EAH / 3rd = 73.01G08.L04

PCI_PLTRST# — PLT_RST# — PLT_RST# 5,17,32,34,53,54,56,71,83,96,97

R2104 0R2J-2-GP 1,2 — DY

R2108 100KR2J-1-GP 1,2 — DY

3D3V_S5 — RN2104 — SRN10KJ-6-GP — OC4# GPIO43, OC1# GPIO40, OC2# GPIO41, OC3# GPIO42

3D3V_S5 — RN2103 — SRN10KJ-6-GP — OC5# GPIO9, LANLINK_STATUS, OC7# GPIO14, OC0# GPIO59

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Title: PCH(5/9) : PCI/USB/NVM

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

Date: Wednesday, March 14, 2012 | Sheet 21 of 103

PCH(6/9)

VRAM ID TABLE

PCH_GPIO39	PCH_GPIO38	VENDER
0	1	Samsung
1	0	Hynix
1	1	Elpida
0	0	UMA

GDDR5/DDR3 TABLE

20110822SI

2012 Chief River	PCH GPIO 12
Richie U&D (13 inches)	0 (13") GDDR5
Rocky U&D (14 inches)	1(14",15",17")DDR3
Rocky U&D (15/17 inches)	1(14",15",17")DDR3

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

PROC_SELECT	
DMI & FDI Termination Voltage	
DF_TVS	SNB: "1" IVB: "0"

PCH1F — 6 OF 10 — PANTHER-GP-NF

GPIO: BMBUSY#/GPIO0, TACH1/GPIO1, TACH2/GPIO6, TACH3/GPIO7, GPIO8, LAN_PHY_PWR_CTRL/GPIO12, GPIO15, SATA4GP/GPIO16, TACH0/GPIO17, SCLOCK/GPIO22, GPIO24, GPIO27, GPIO28, STP_PCI#/GPIO34, GPIO35, SATA2GP/GPIO36, SATA3GP/GPIO37, SLOAD/GPIO38, SDATAOUT0/GPIO39, SDATAOUT1/GPIO48, SATA5GP/GPIO49/TEMP_ALERT#, GPIO57

CPU/MISC: TACH4/GPIO68, TACH5/GPIO69, TACH6/GPIO70, TACH7/GPIO71, A20GATE, PECI, RCIN#, PROCPWRGD, THRMTRIP#, INIT3_3V#, DF_TVS, TS_VSS1, TS_VSS2, TS_VSS3, TS_VSS4, NC_1, VSS_NCTF_15#BG2, VSS_NCTF_16#BG48, VSS_NCTF_17#BH3, VSS_NCTF_18#BH47

NCTF: VSS_NCTF_1#A4, VSS_NCTF_2#A44, VSS_NCTF_3#A45, VSS_NCTF_4#A46, VSS_NCTF_5#A5, VSS_NCTF_6#A6, VSS_NCTF_7#B3, VSS_NCTF_8#B47, VSS_NCTF_9#BD1, VSS_NCTF_10#BD49, VSS_NCTF_11#BE1, VSS_NCTF_12#BE49, VSS_NCTF_13#BF1, VSS_NCTF_14#BF49, VSS_NCTF_19#BJ4, VSS_NCTF_20#BJ44, VSS_NCTF_21#BJ45, VSS_NCTF_22#BJ46, VSS_NCTF_23#BJ5, VSS_NCTF_24#BJ6, VSS_NCTF_25#C2, VSS_NCTF_26#C48, VSS_NCTF_27#D1, VSS_NCTF_28#D49, VSS_NCTF_29#E1, VSS_NCTF_30#E49, VSS_NCTF_31#F1, VSS_NCTF_32#F49

NCTF TEST PIN: A4, A44, A45, A46, A5, A6, B3, B47, BD1, BD49, BE1, BE49, BF1, BF49, BG2, BG48, BH3, BH47, BJ4, BJ44, BJ45, BJ46, BJ5, BJ6, C2, C48, D1, D49, E1, E49, F1, F49

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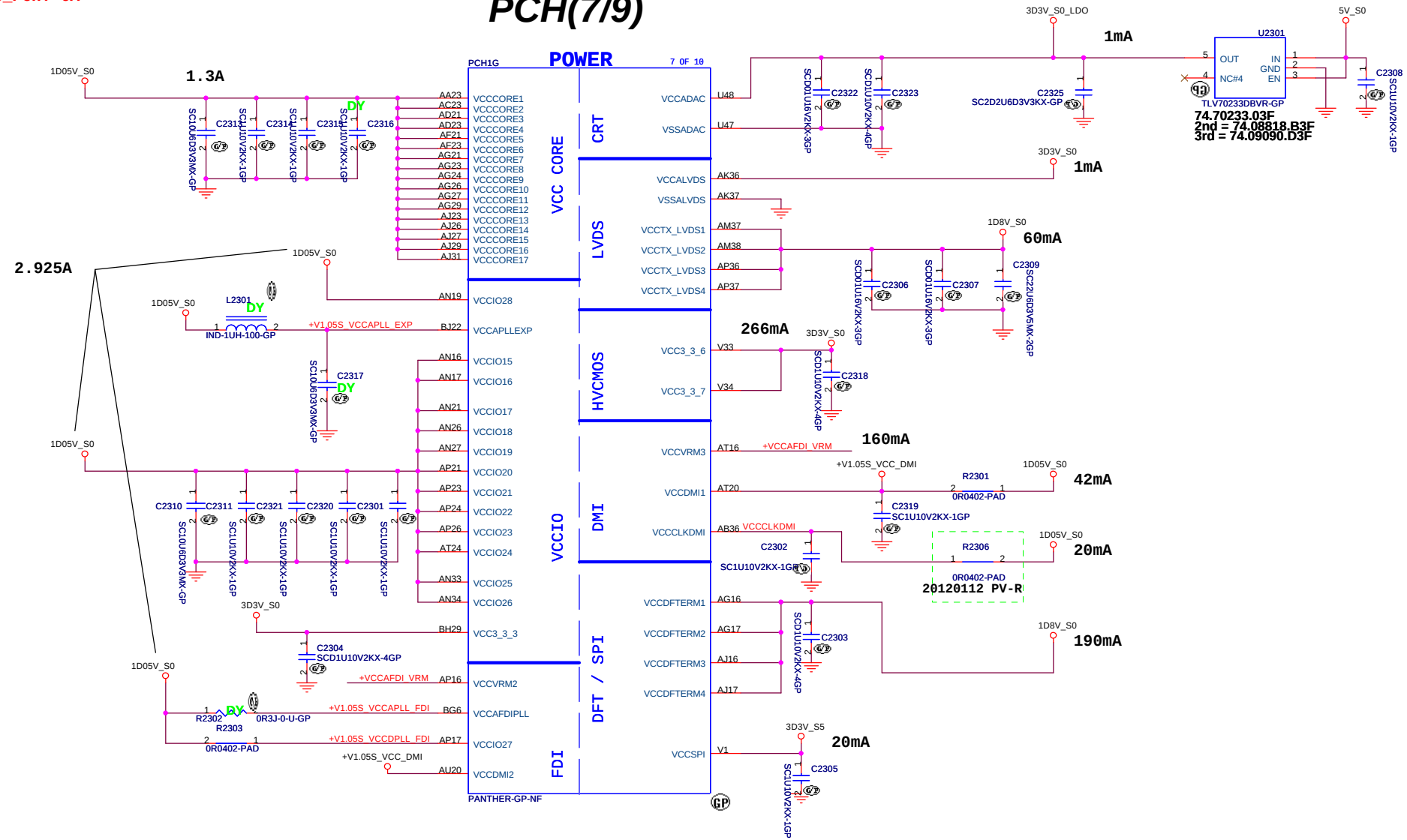
Title: PCH(6/9) : GPIO/NTCF/RSVD

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

Date: Wednesday, March 14, 2012 | Sheet 22 of 103

VCC_PCH: 6A

PCH(7/9)



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Title: PCH(7/9) : PWR1

Size	Document Number	Rev
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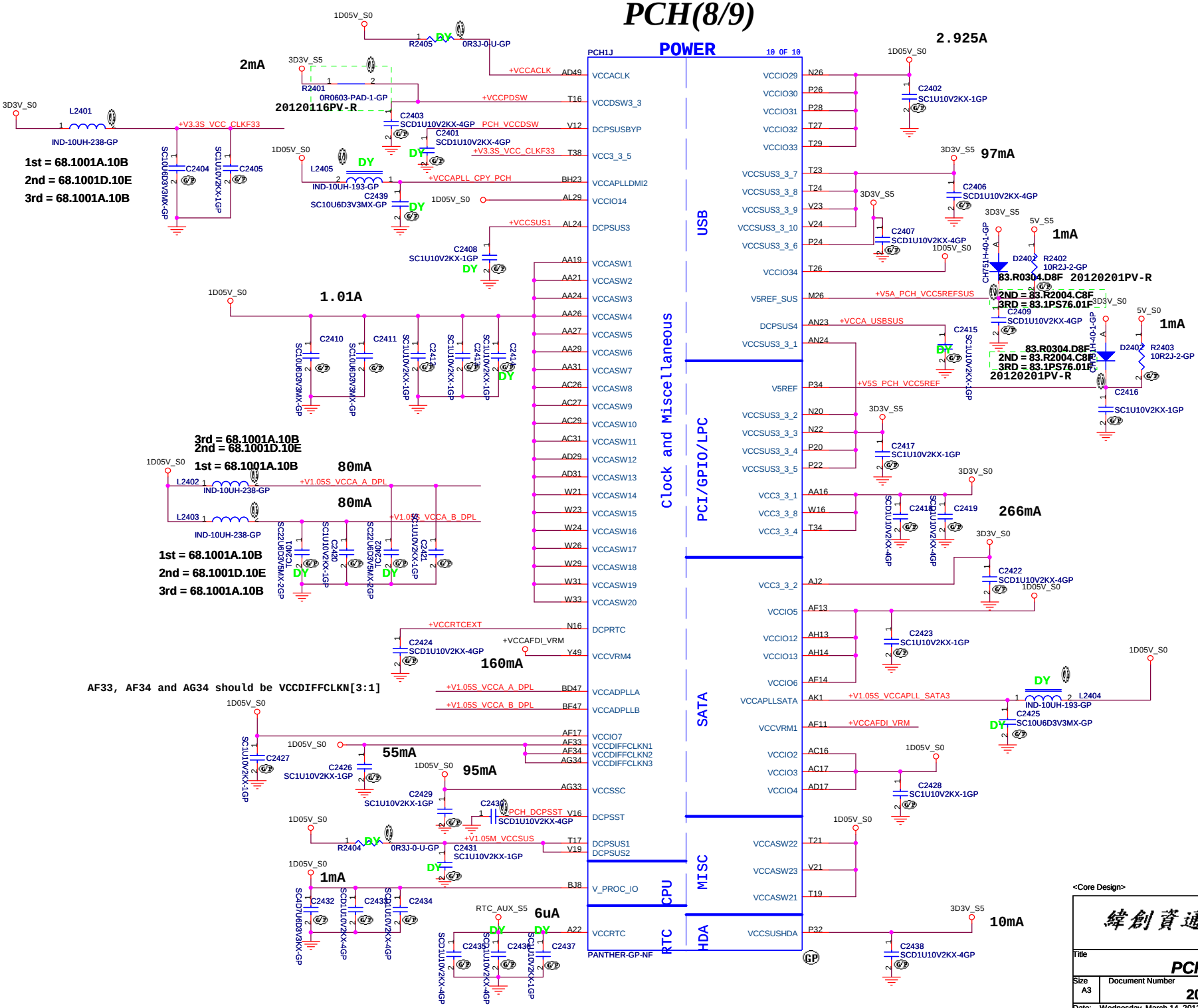
PCH(8/9)



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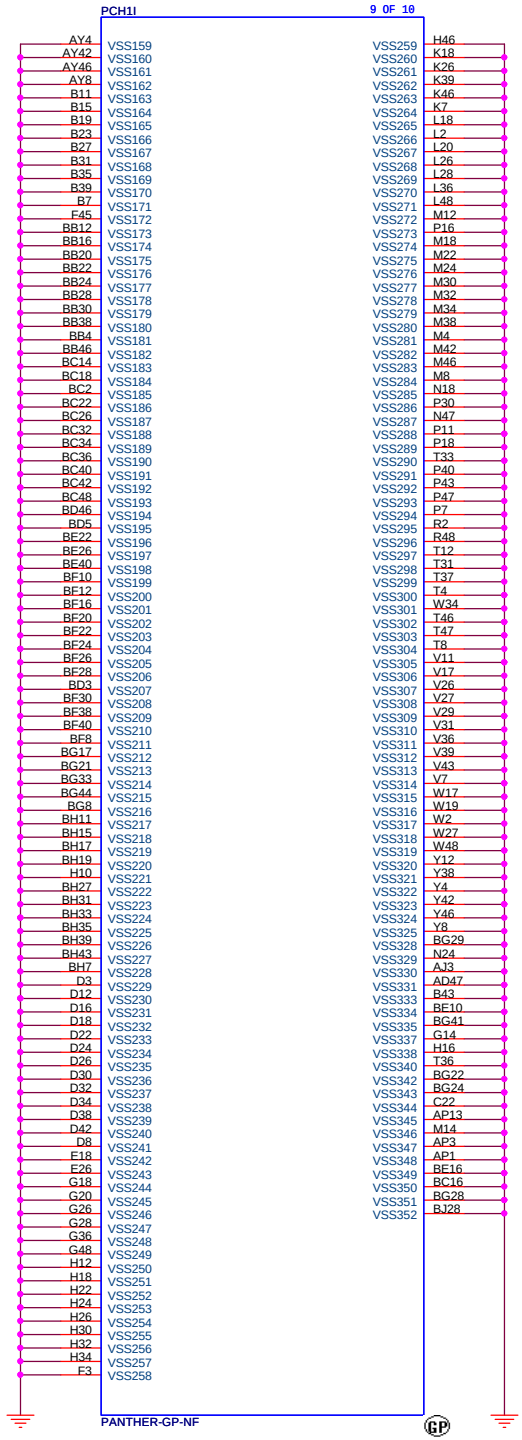
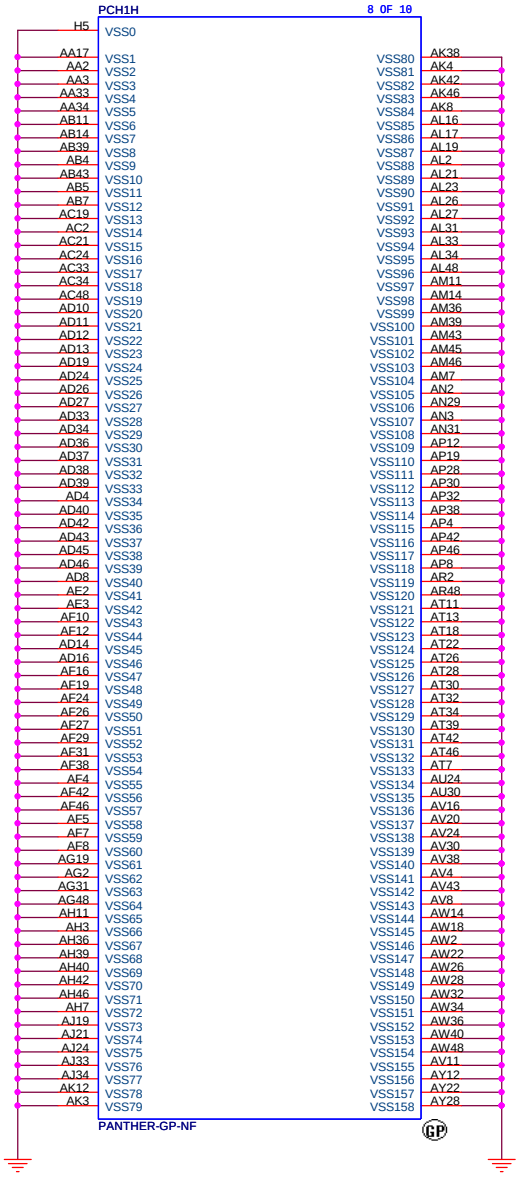
Title	PCH(8/9) : PWR2
Size: A3	Document Number: 2012 S-Series Richie 13.3
Rev: -1	
Date: Wednesday, March 14, 2012	Sheet 24 of 103

PCH(9/9)





<Core Design>

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Title: PCH(9/9) : GND

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<Core Design>

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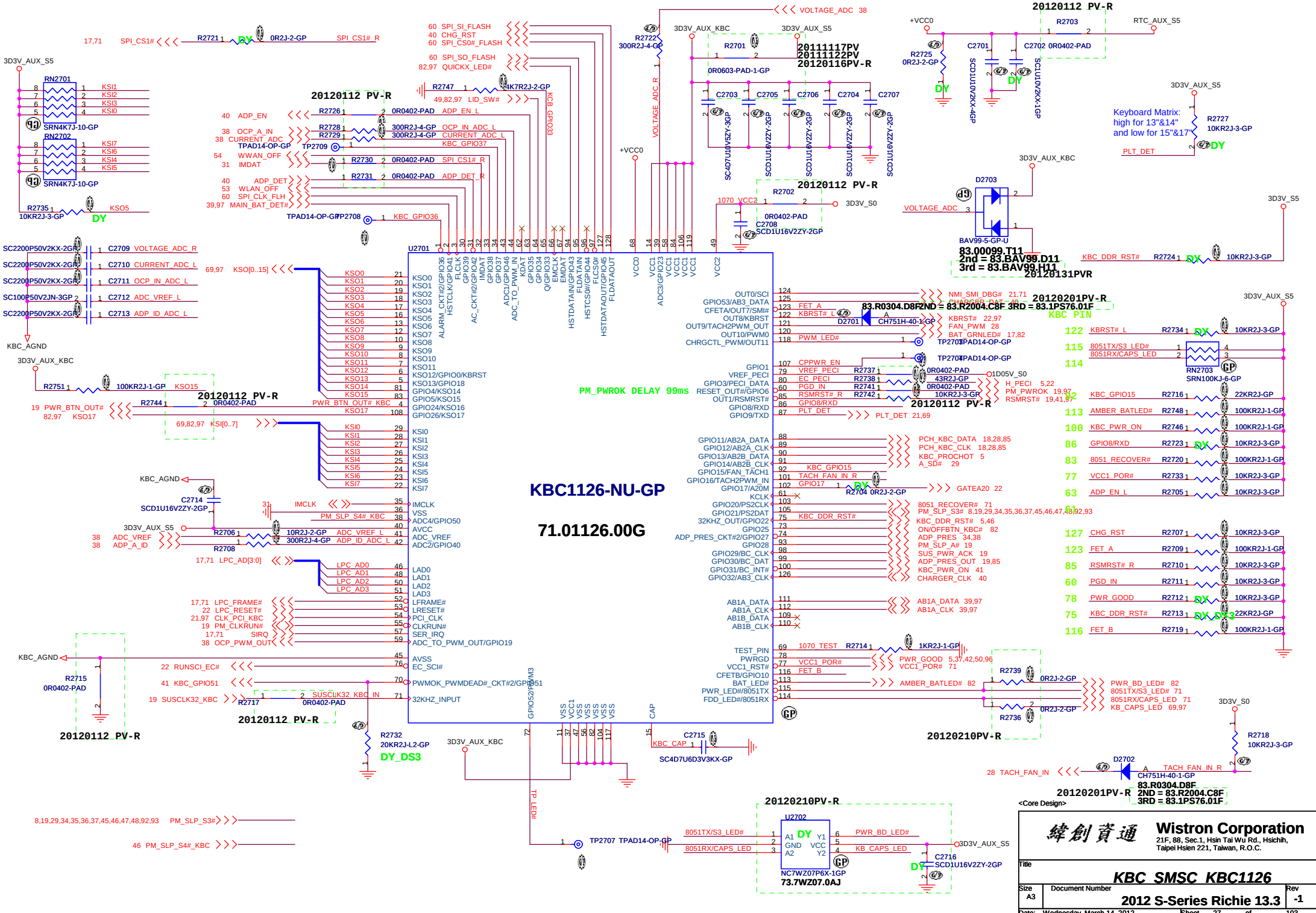
Title: PCH XDP

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

Date: Wednesday, March 14, 2012 | Sheet 26 of 103


KBC1126-NU-GP
71.01126.00G
PM_PWROK DELAY 99ms
KBC PIN
Keyboard Matrix:
high for 13"&14"
and low for 15"&17"
20120112 PV-R
20111117PV
20111122PV
20120116PV-R
20120131PVR
20120201PV-R
20120210PV-R
83.00099.T11
2nd = 83.BAV99.D11
3rd = 83.BAV99.H11
83.R0304.D8F
2ND = 83.R2004.C8F
3RD = 83.1PS76.01F
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KBC_SMSC_KBC1126
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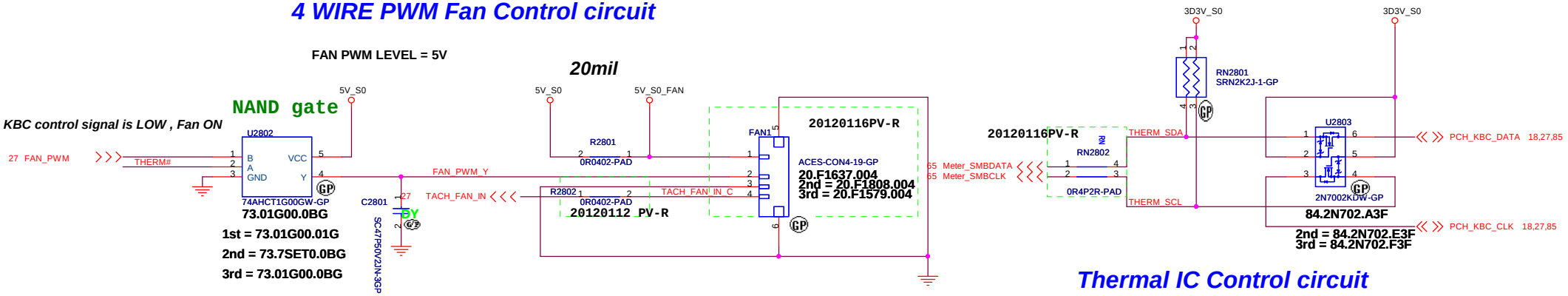
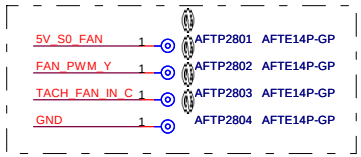
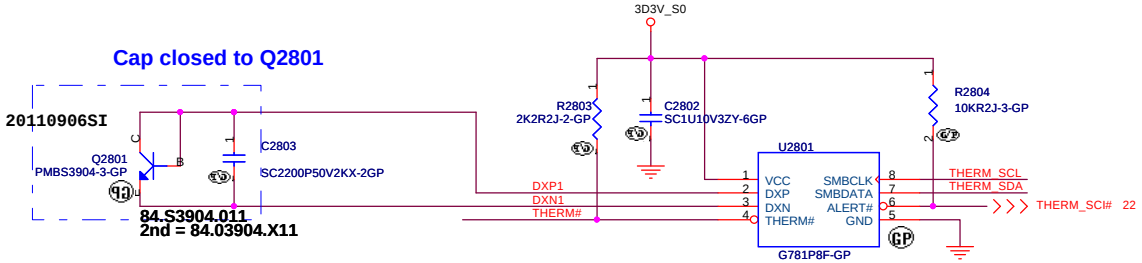
4 WIRE PWM Fan Control circuit



A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

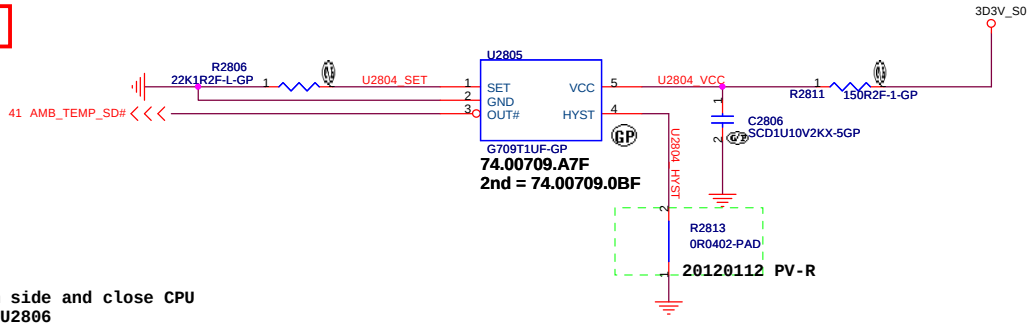


Thermal IC Control circuit



T8 H/W Shutdown Control circuit

Degree	Rset
95	25.5K
90	22.1K
85	18.7K



Layout: PUT U2805 Bottom side and close CPU
PUT R2806 Close U2806

<Core Design>

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Title: Thermal G781 / FAN

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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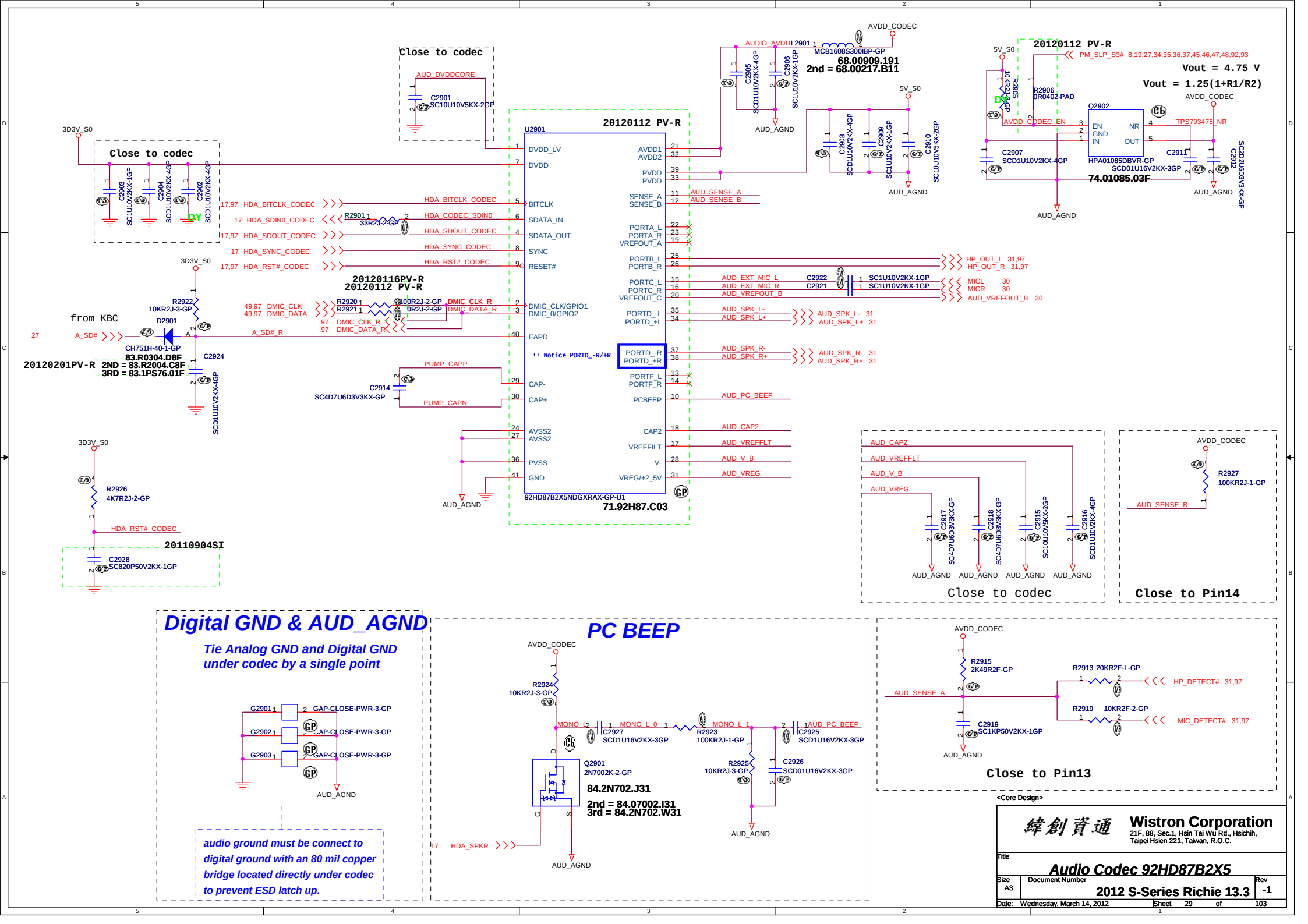
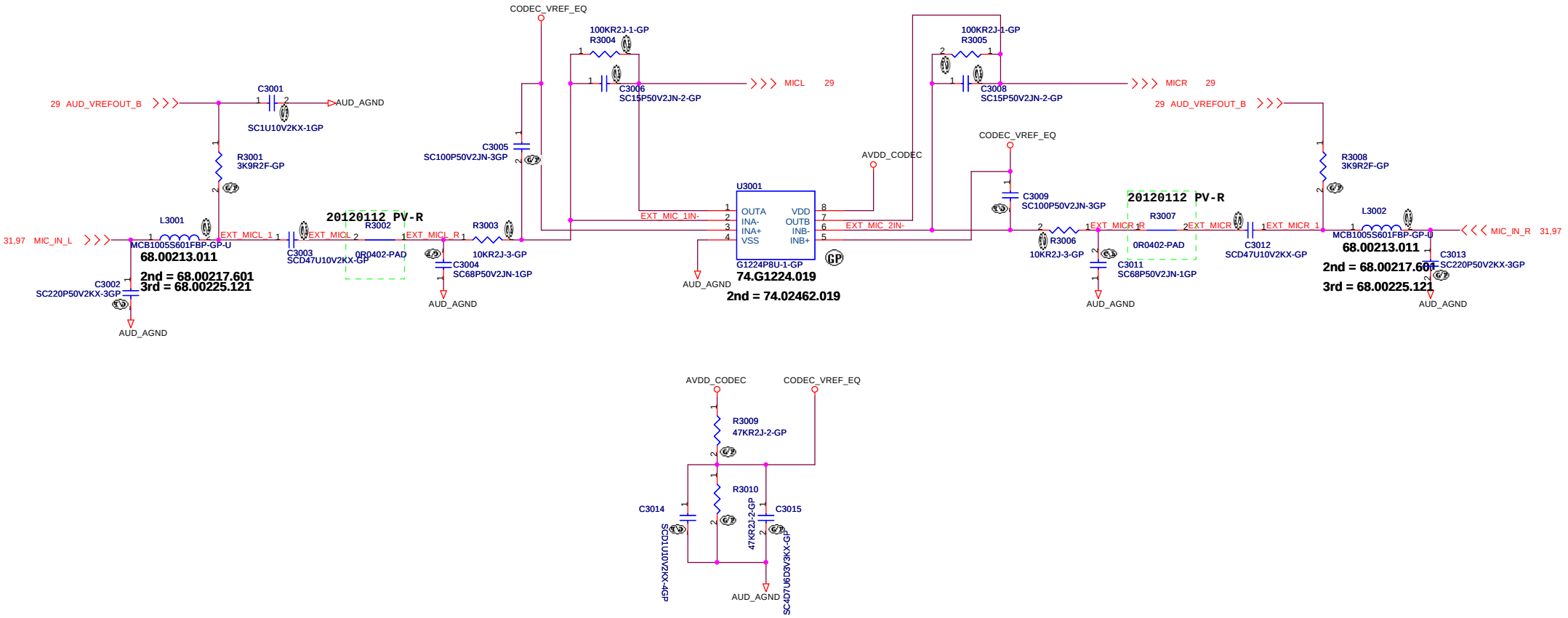

Close to codec
AUD_DVDDCORE
C2901
SC10U10V5KX-2GP
U2901
20120112 PV-R
DVDD_LV
DVDD
BITCLK
SDATA_IN
SDATA_OUT
SYNC
RESET#
DMIC_CLK/GPIO1
DMIC_0/GPIO2
EAPD
!! Notice PORTD_-R/+R
CAP-
CAP+
AVSS2
AVSS1
PVSS
GND
AVDD1
AVDD2
PVDD
PVDD
SENSE_A
SENSE_B
PORTA_L
PORTA_R
VREFOUT_A
PORTB_L
PORTB_R
PORTC_L
PORTC_R
VREFOUT_C
PORTD_-L
PORTD_+L
PORTD_-R
PORTD_+R
PORTF_L
PORTF_R
PCBEEP
CAP2
VREFFILT
V-
VREG/+2_5V
92HD87B2X5NDGXRAX-GP-U1
71.92H87.C03
HDA_BITCLK_CODEC
HDA_CODEC_SDIN0
HDA_SDOUT_CODEC
HDA_SYNC_CODEC
HDA_RST#_CODEC
R2901
33R2J-2-GP
20120116PV-R
20120112 PV-R
DMIC_CLK_R
DMIC_DATA_R
R2920
R2921
100R2J-2-GP
0R2J-2-GP
from KBC
D2901
CH751H-40-1-GP
83.R0304.D8F
20120201PV-R 2ND = 83.R2004.C8F
3RD = 83.1PS76.01F
R2922
10KR2J-3-GP
C2924
SCD1U10V2KX-4GP
A_SD#
A_SD#_R
PUMP_CAPP
PUMP_CAPN
C2914
SC4D7U6D3V3KX-GP
AUD_AGND
3D3V_S0
R2926
4K7R2J-2-GP
HDA_RST#_CODEC
20110904SI
C2928
SC820P50V2KX-1GP
AVDD_CODEC
AUDIO_AVDD
L2901
MCB1608S300IBP-GP
68.00909.191
2nd = 68.00217.B11
C2905
C2906
SCD1U10V2KX-4GP
SCD1U10V2KX-1GP
5V_S0
C2908
C2909
C2910
SC10U10V5KX-2GP
AUD_SENSE_A
AUD_SENSE_B
HP_OUT_L
HP_OUT_R
AUD_EXT_MIC_L
AUD_EXT_MIC_R
AUD_VREFOUT_B
C2922
C2921
SC1U10V2KX-1GP
MICL
MICR
AUD_SPK_L-
AUD_SPK_L+
AUD_SPK_L-
AUD_SPK_L+
AUD_SPK_R-
AUD_SPK_R+
AUD_SPK_R-
AUD_SPK_R+
AUD_PC_BEEP
AUD_CAP2
AUD_VREFFLT
AUD_V_B
AUD_VREG
20120112 PV-R
PM_SLP_S3# 8,19,27,34,35,36,37,45,46,47,48,92,93
Vout = 4.75 V
Vout = 1.25(1+R1/R2)
R2905
10KR2J-3-GP
R2906
0R0402-PAD
Q2902
AVDD_CODEC_EN
EN
GND
IN
NR
OUT
TPS793475_NR
HPA01085DBVR-GP
74.01085.03F
C2907
SCD1U10V2KX-4GP
C2911
SCD01U16V2KX-3GP
C2912
SC22U6D3V3KX-GP
Close to codec
AUD_CAP2
AUD_VREFFLT
AUD_V_B
AUD_VREG
C2917
C2918
C2915
C2916
SC4D7U6D3V3KX-GP
SC10U10V5KX-2GP
SCD1U10V2KX-4GP
Close to codec
AVDD_CODEC
R2927
100KR2J-1-GP
AUD_SENSE_B
Close to Pin14
Digital GND & AUD_AGND
Tie Analog GND and Digital GND
under codec by a single point
G2901
G2902
G2903
GAP-CLOSE-PWR-3-GP
audio ground must be connect to
digital ground with an 80 mil copper
bridge located directly under codec
to prevent ESD latch up.
PC BEEP
R2924
10KR2J-3-GP
MONO_L2
MONO_L_0
C2927
SCD1U16V2KX-3GP
Q2901
2N7002K-2-GP
84.2N702.J31
2nd = 84.07002.I31
3rd = 84.2N702.W31
MONO_L_1
R2923
100KR2J-1-GP
AUD_PC_BEEP
C2925
SCD1U16V2KX-3GP
R2925
10KR2J-3-GP
C2926
SCD01U16V2KX-3GP
HDA_SPKR
R2915
2K49R2F-GP
R2913 20KR2F-L-GP
HP_DETECT# 31,97
R2919 10KR2F-2-GP
MIC_DETECT# 31,97
C2919
SC1KP50V2KX-1GP
Close to Pin13
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Audio Codec 92HD87B2X5
Size A3
Document Number
2012 S-Series Richie 13.3
Rev -1
Date: Wednesday, March 14, 2012
Sheet 29 of 103

Pre-AMP. for External MIC



<Core Design>

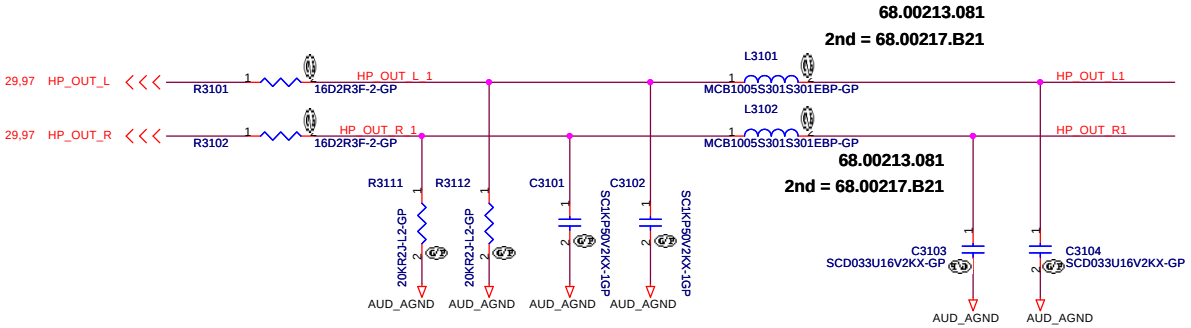
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***External MIC Pre-Amp***

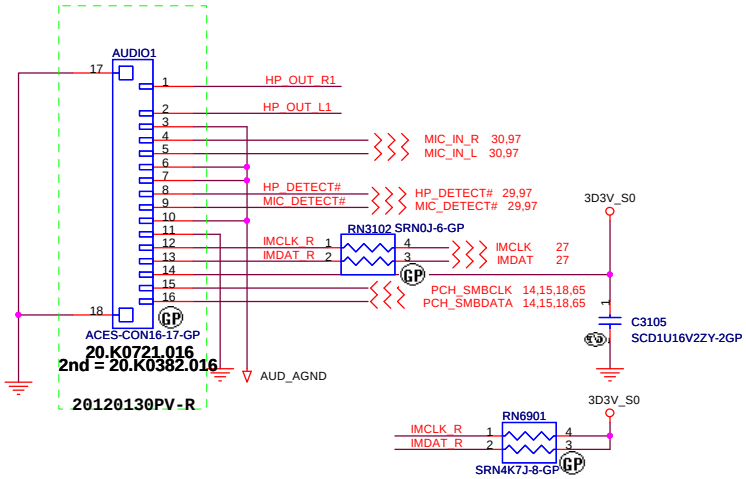
Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

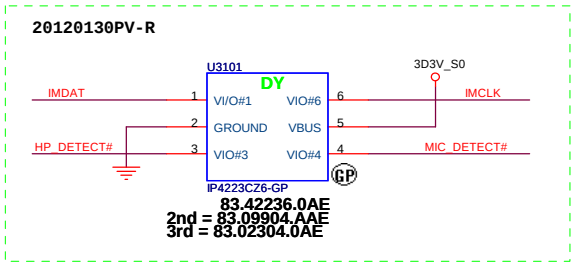
Date: Wednesday, March 14, 2012 Sheet 30 of 103

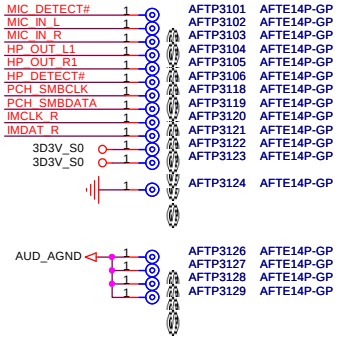
HeadPhone OUT



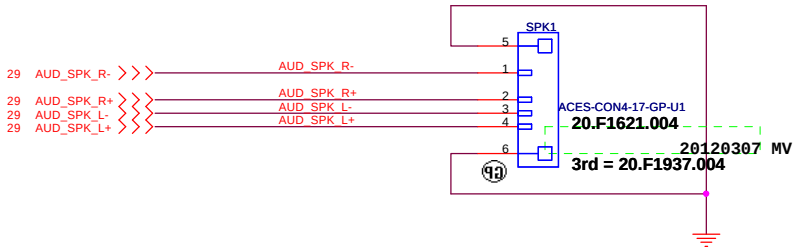
Audio Board +Touch Pad Connector

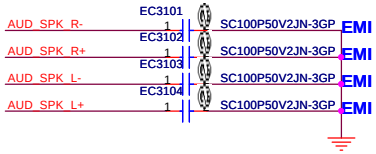


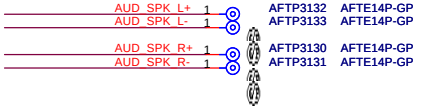




Speaker Connector







<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO Connector

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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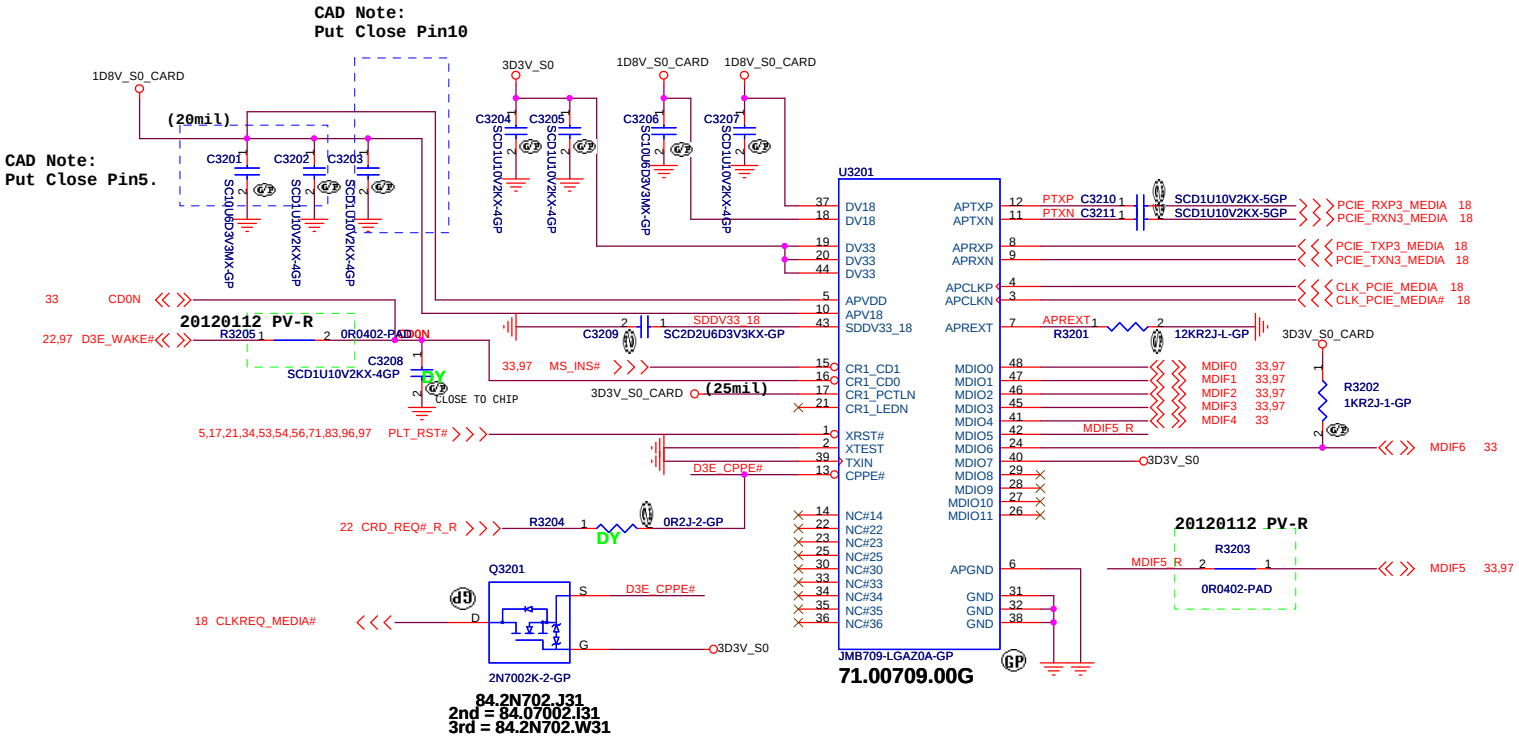
CardReader JMicron JMB709



D3E Detection Table

D3E_CPPE#	Status
H	D3E mode
L	Normal mode

CR1_CDxN Detection Table

CR1_CDxN		Card Type
1	0	
H	H	(No Card)
H	L	SD Card/MMC
L	H	MemoryStick
L	L	XD Card

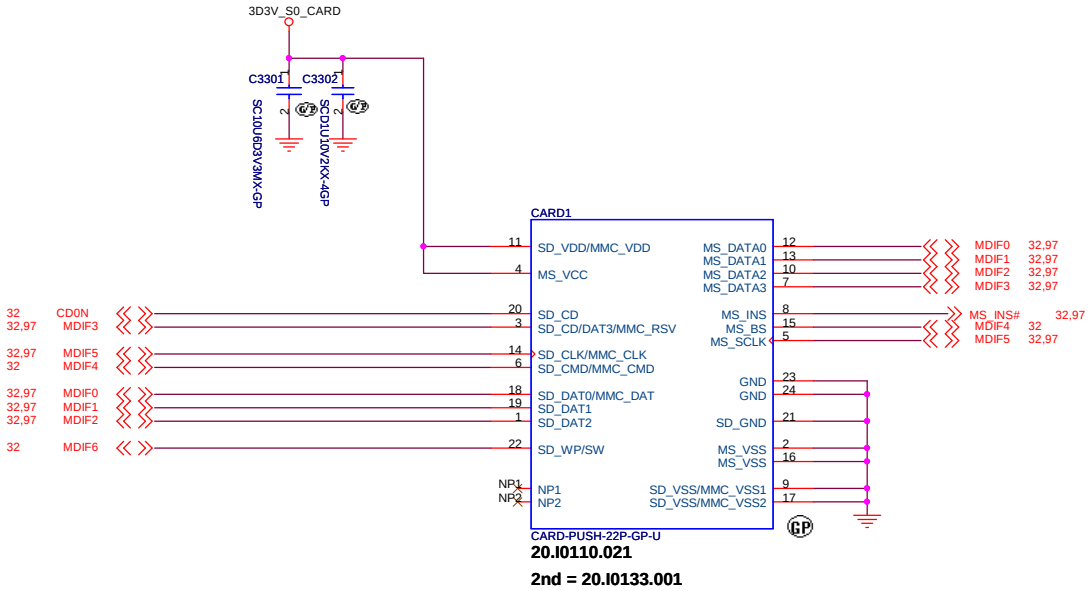
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Card Reader-JMB 709**

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

Date: Wednesday, March 14, 2012 Sheet 32 of 103



20.I0110.021

2nd = 20.I0133.001

Pin Name	Default Mode	SD/MMC Card	MS Card
MDIO0	SD/MMC/MS	SD1_DAT0	MS1_DAT0
MDIO1		SD1_DAT1	MS1_DAT1
MDIO2		SD1_DAT2	MS1_DAT2
MDIO3		SD1_DAT3	MS1_DAT3
MDIO4		SD1_CMD	MS1_BS
MDIO5		SD1_CLK	MS1_CLK
MDIO6		SD1_WP	
MDIO7			
MDIO8		MMC_DAT4	MS1_DAT4
MDIO9		MMC_DAT5	MS1_DAT5
MDIO10		MMC_DAT6	MS1_DAT6
MDIO11		MMC_DAT7	MS1_DAT7
CR1_LEDN		SD1_LED#	MS1_LED#
CR1_PCTLN		SD1_PCTL#	MS1_PCTL#
CR1_CD0		SD1_CD#	
CR1_CD1			MS1_CD#

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***SD/MS/MMC CONNECTOR***

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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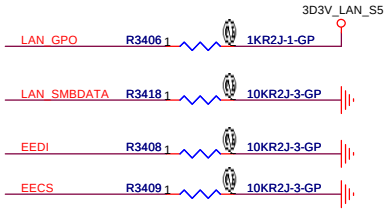
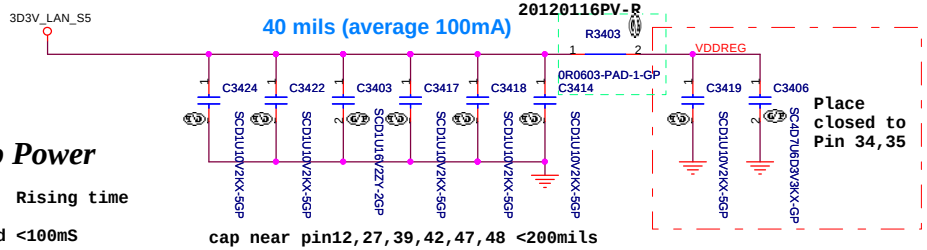
LAN CHIP-RTL8151FH

USE EFuse No ASF

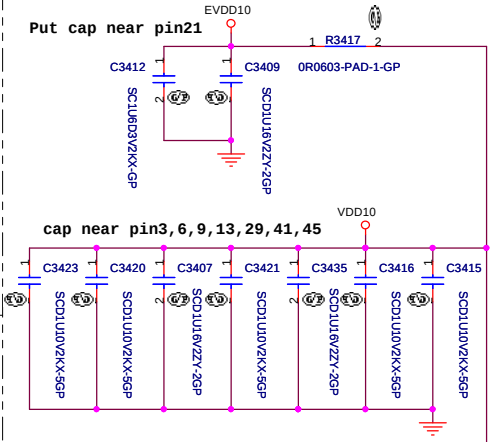


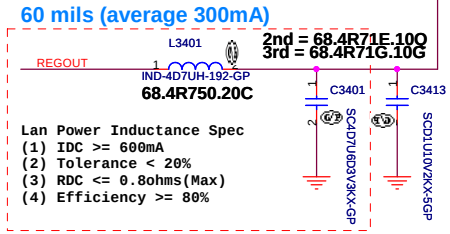
LanChip Power

+3.3V_LAN_S5 Rising time (10%~90%)
Spec >1mS and <100mS



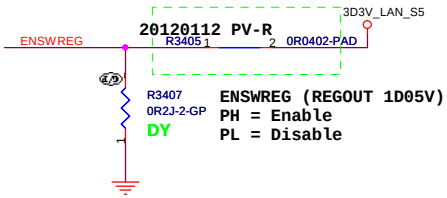
Regout power plane(1D05V)

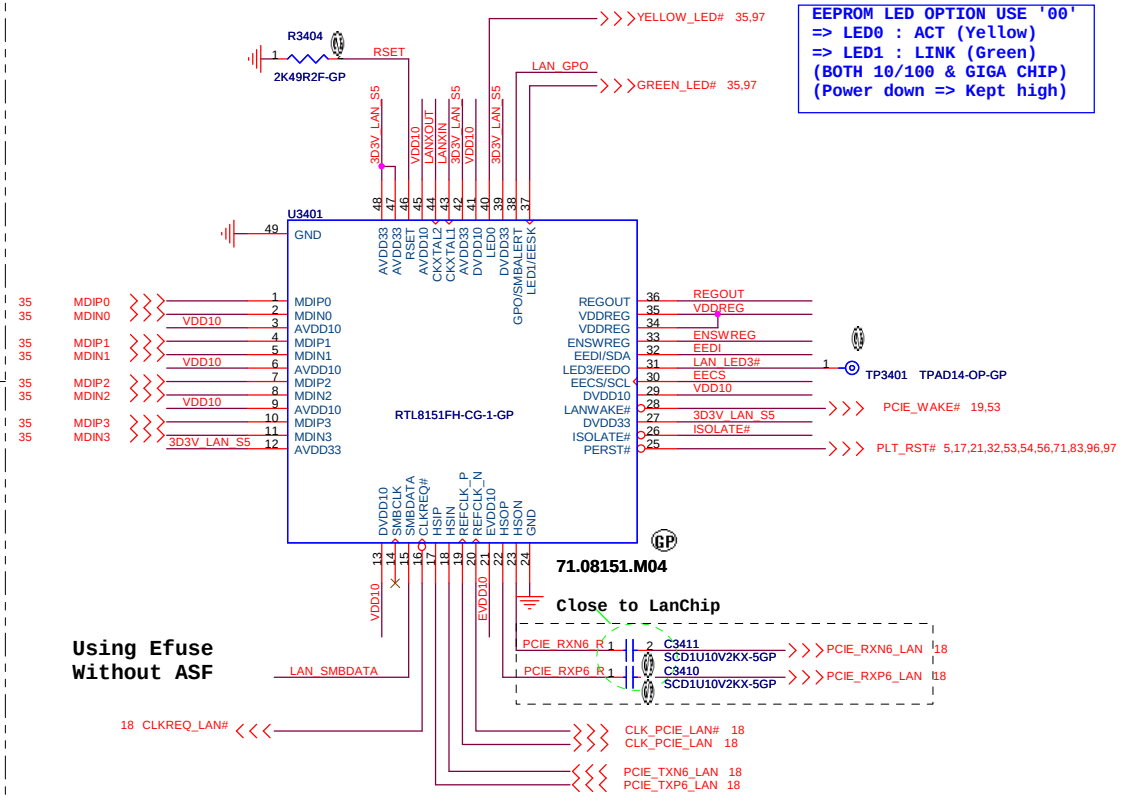


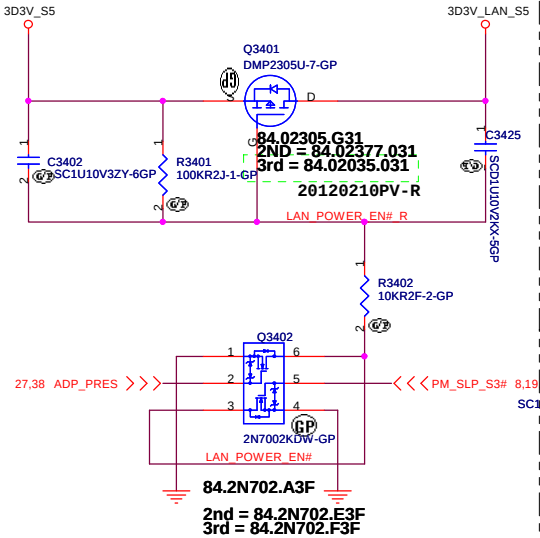


Put 4D7U L + 4D7U cap near pin36 <200mils
(2nd = 78.22610.81L)

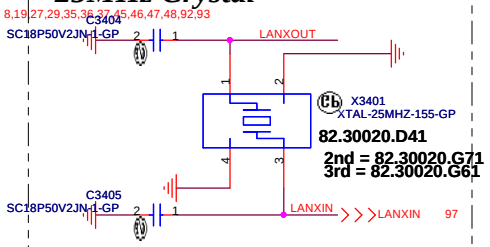
Regout Switch



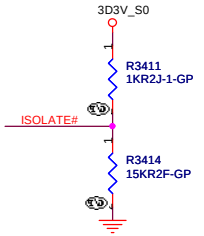




25MHz Crystal



Isolate Strap Pin



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Lan Realtek 8151FH

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

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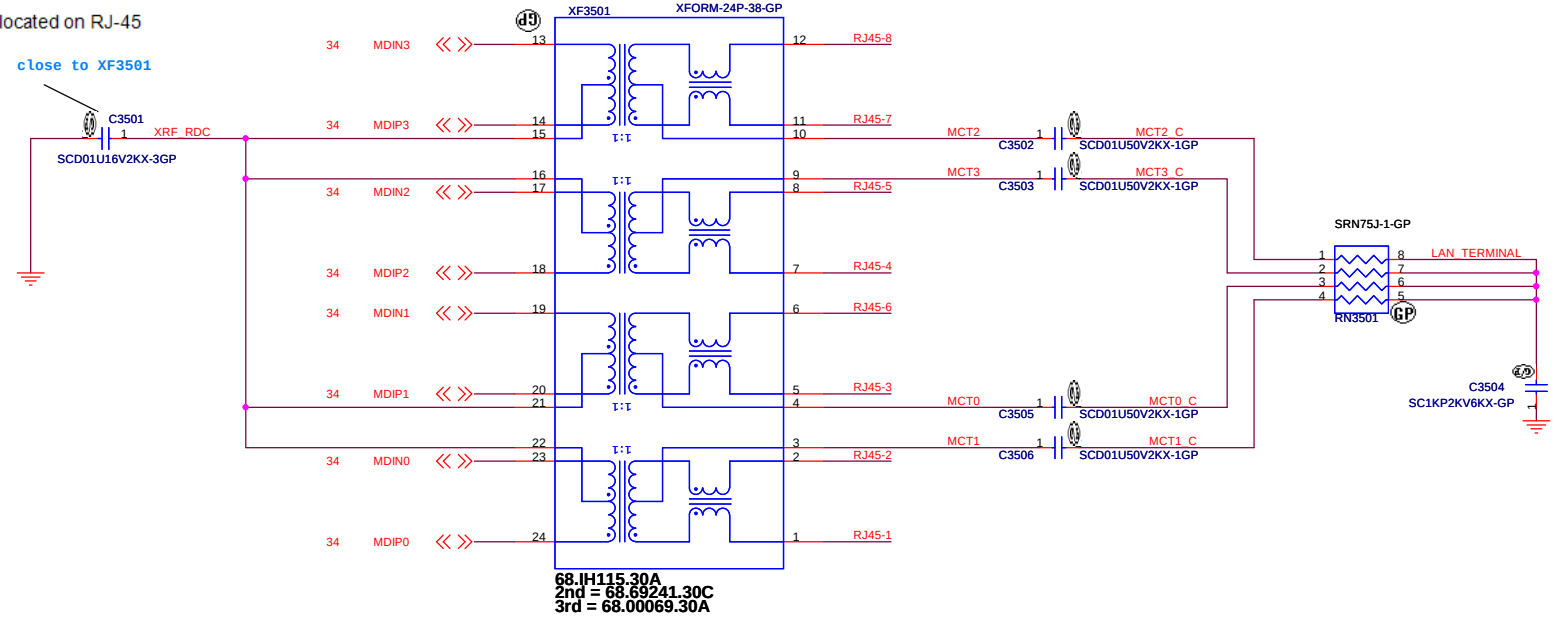
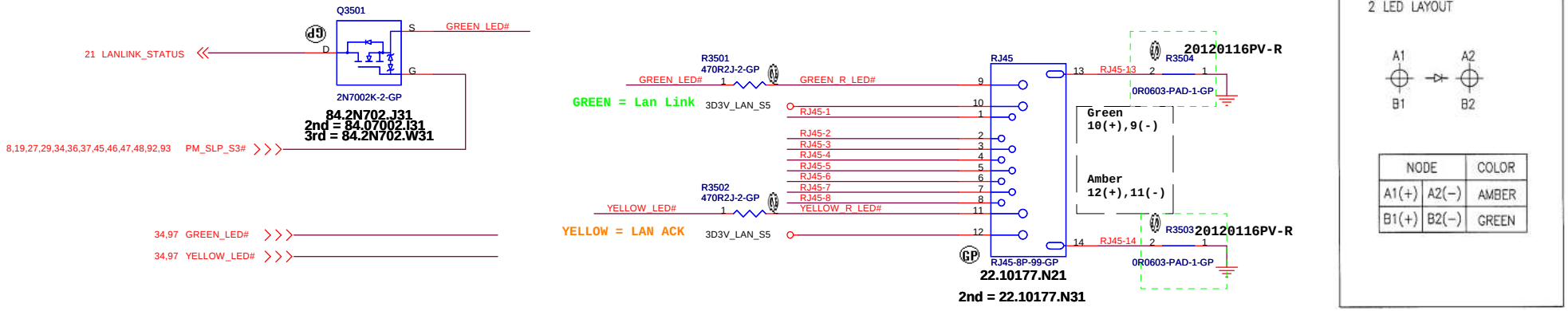
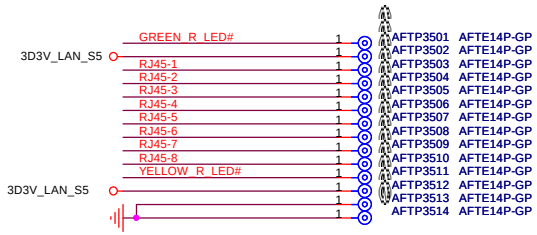
White LED for connectivity and Amber LED for activity located on RJ-45 connector



RJ45 Connector





(1)route on bottom as differential pairs.
(2)Tx+/Tx- are pairs. Rx+/Rx- are pairs.
(3)No vias, No 90 degree bends.
(4)pairs must be equal lengths.
(5)6mil trace width,12mil separation.
(6)36mil between pairs and any other trace.
(7)Must not cross ground moat,
except RJ-45 moat.

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN RJ45

Size	Document Number	Rev
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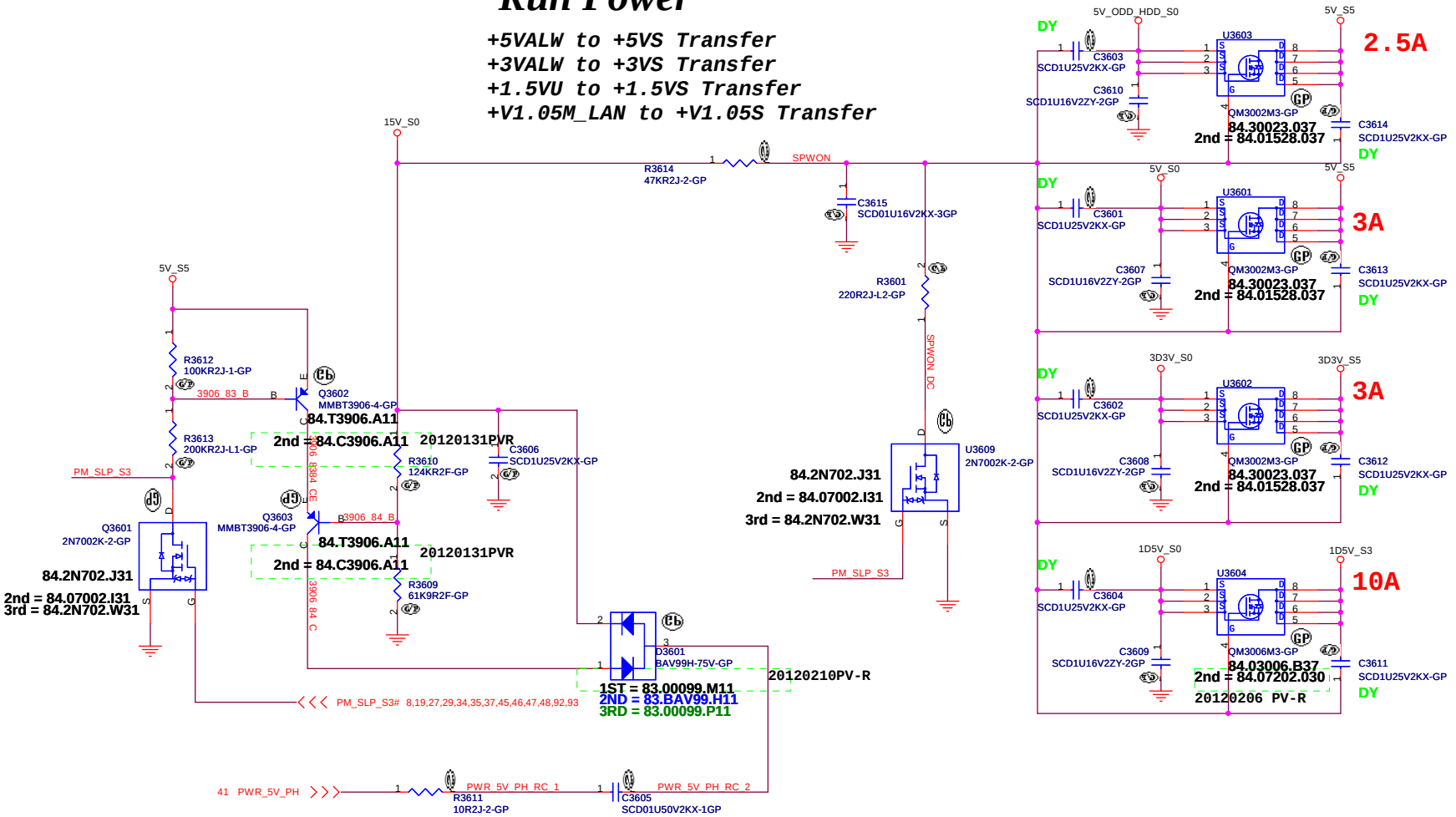
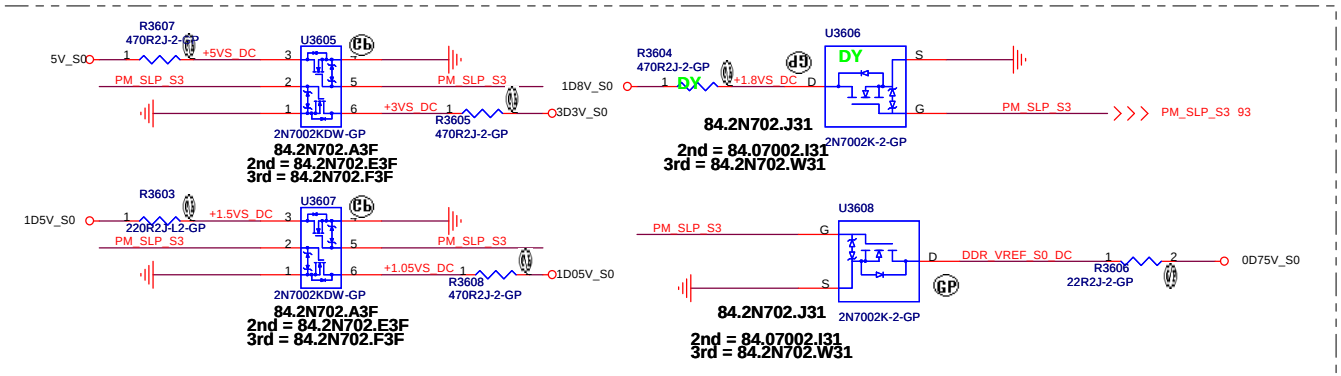
Run Power

+5VALW to +5VS Transfer
+3VALW to +3VS Transfer
+1.5VU to +1.5VS Transfer
+V1.05M_LAN to +V1.05S Transfer





<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

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A3	2012 S-Series Richie 13.3	-1

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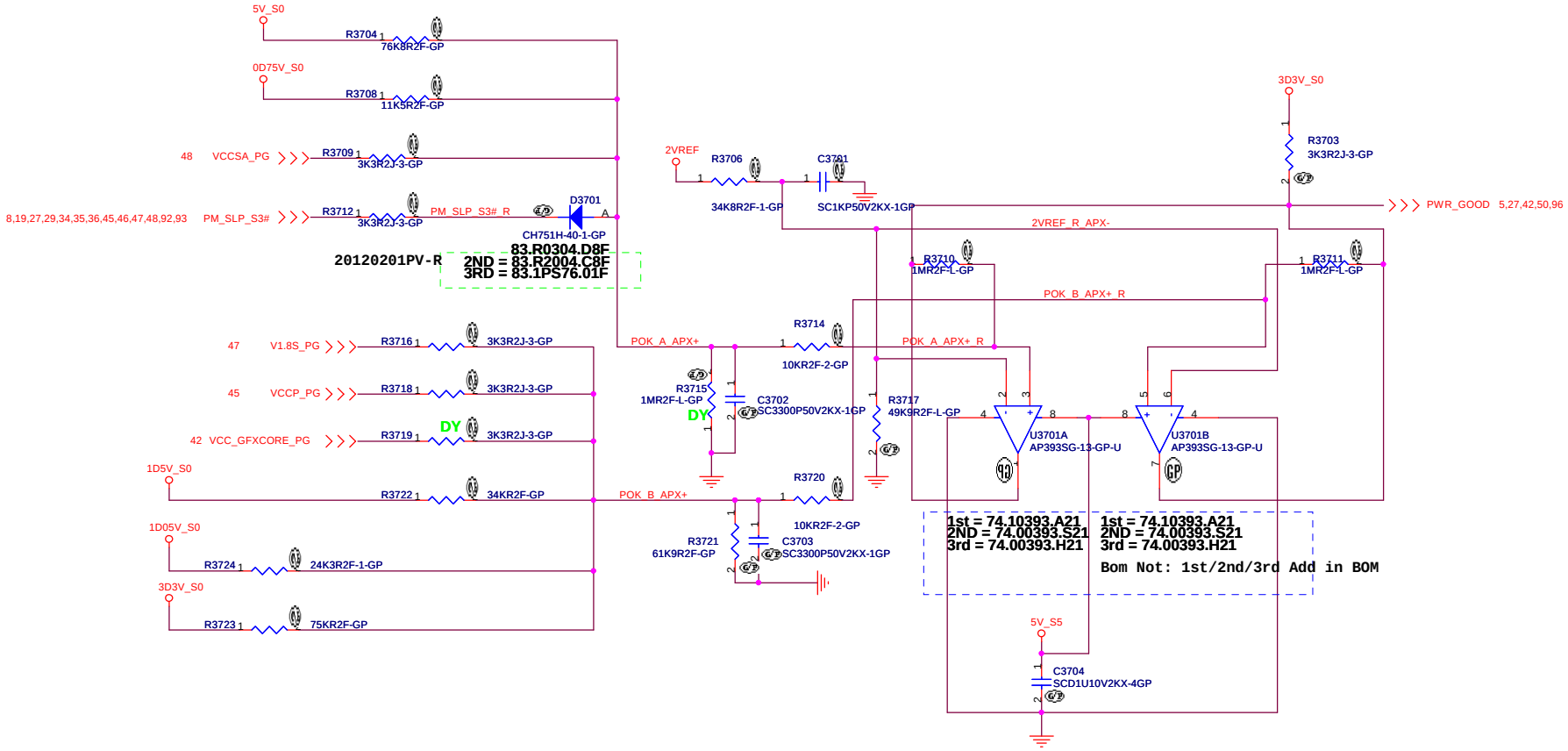
POK

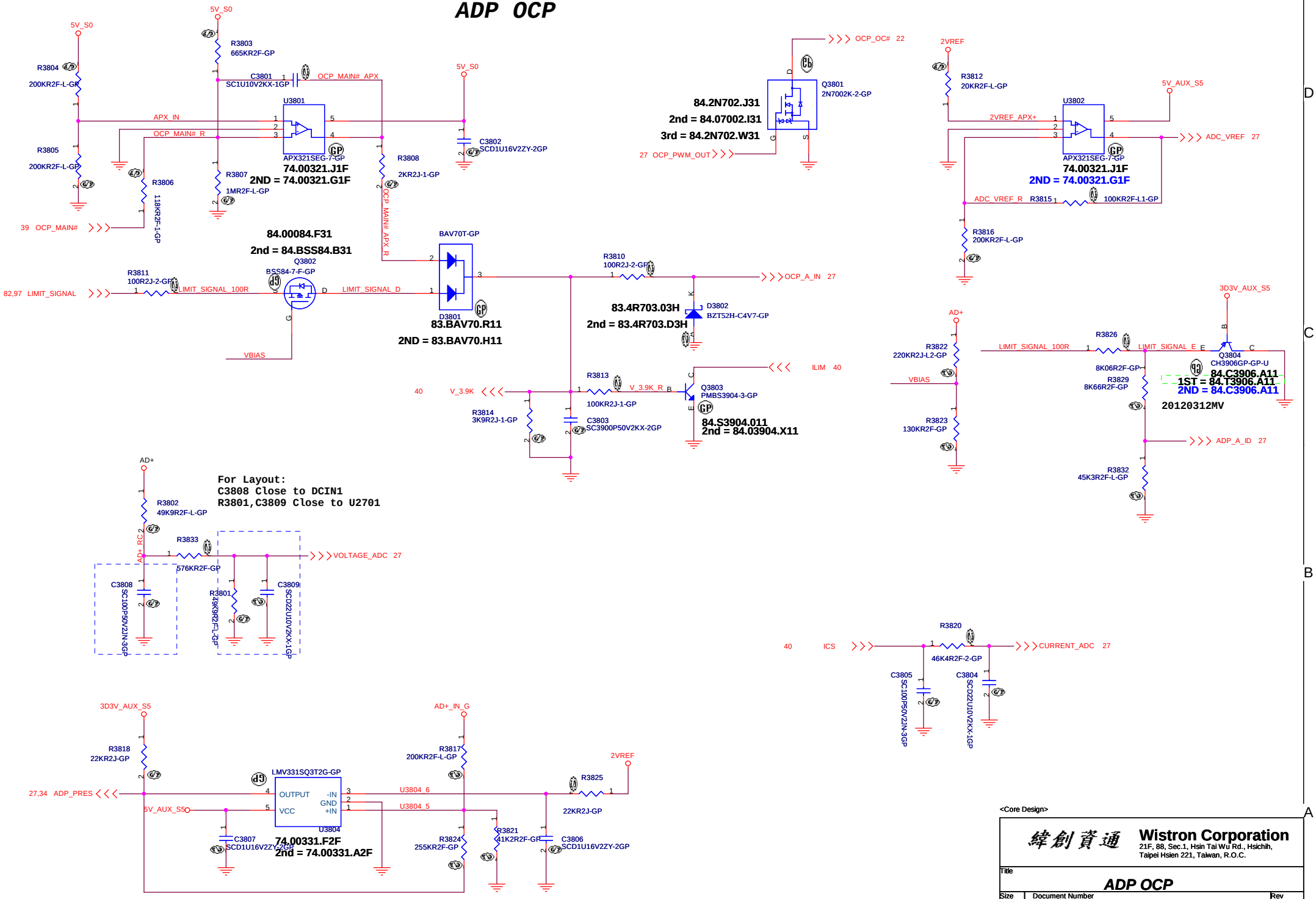


<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	POK	
Size A3	Document Number 2012 S-Series Richie 13.3	Rev -1
Date: Wednesday, March 14, 2012	Sheet 37 of 103	

ADP OCP



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ADP OCP

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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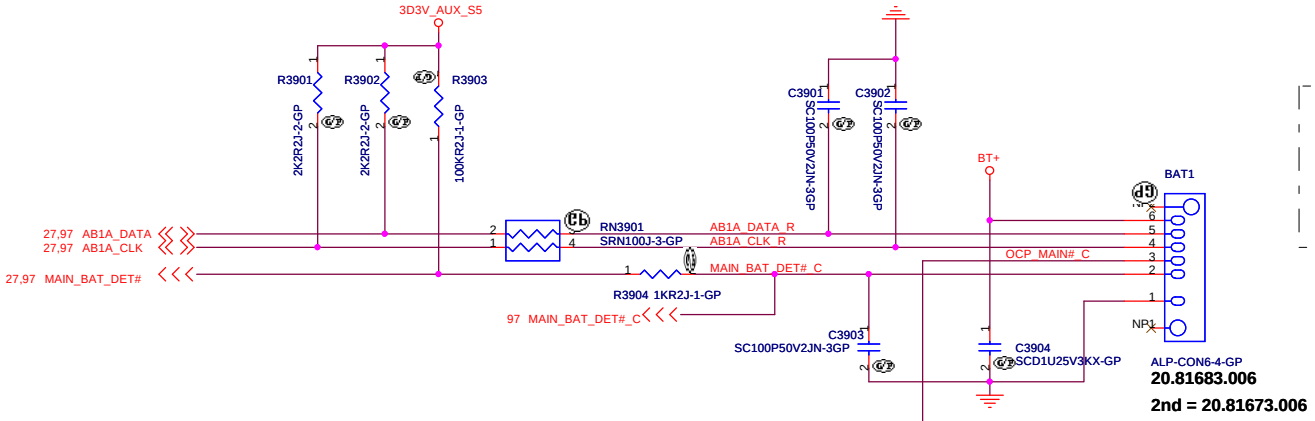
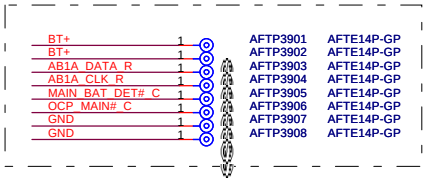
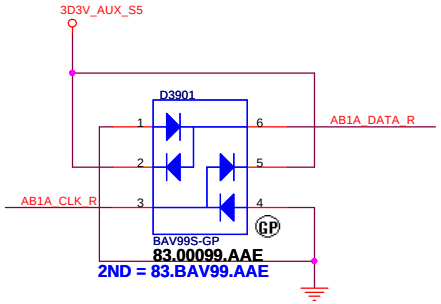
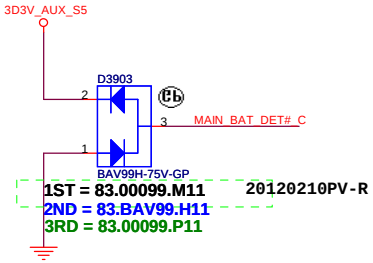
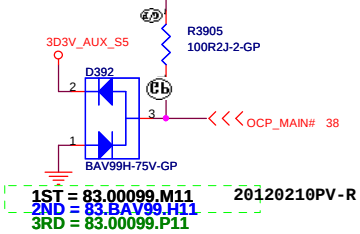
Battery Connector







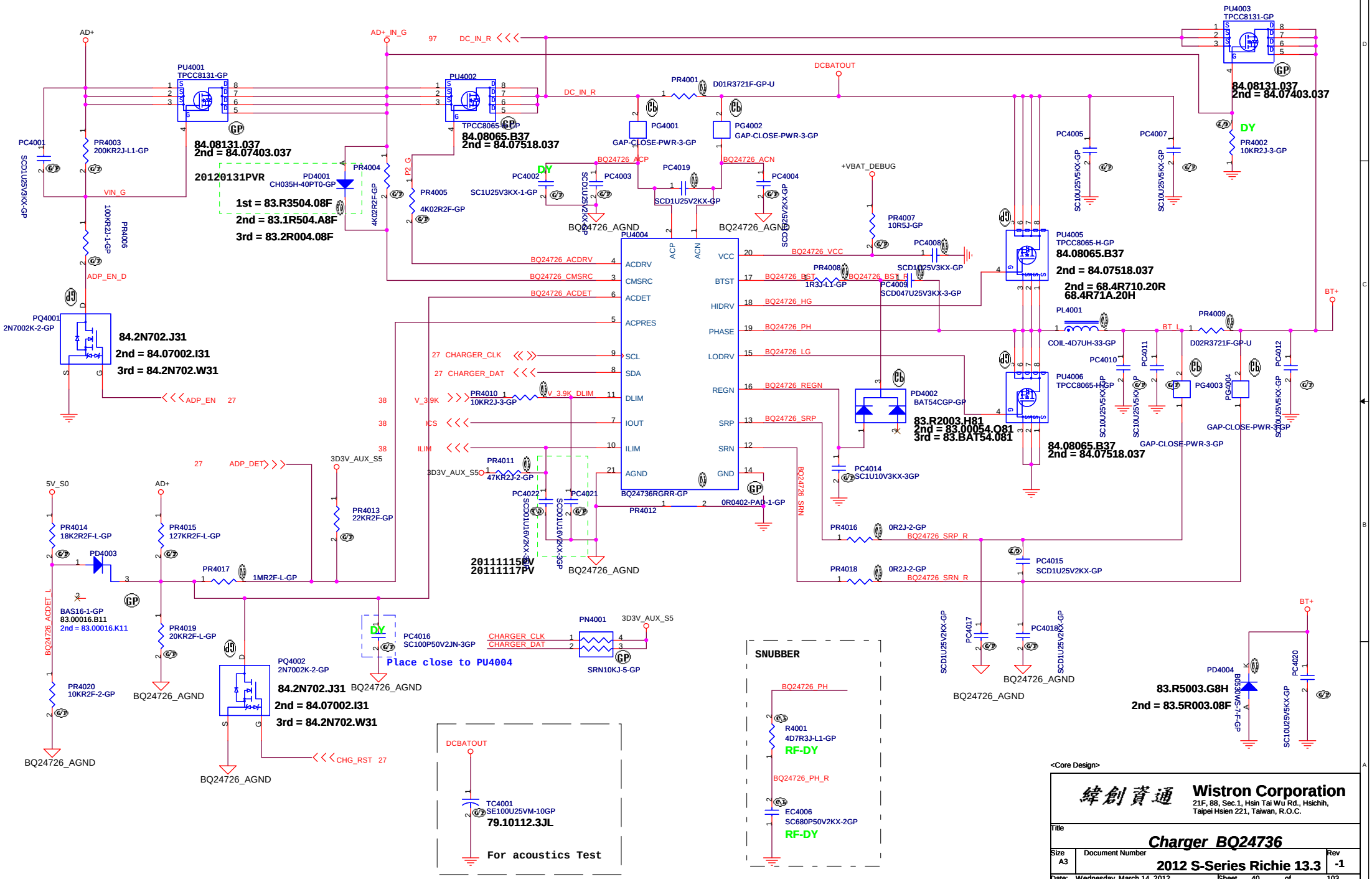




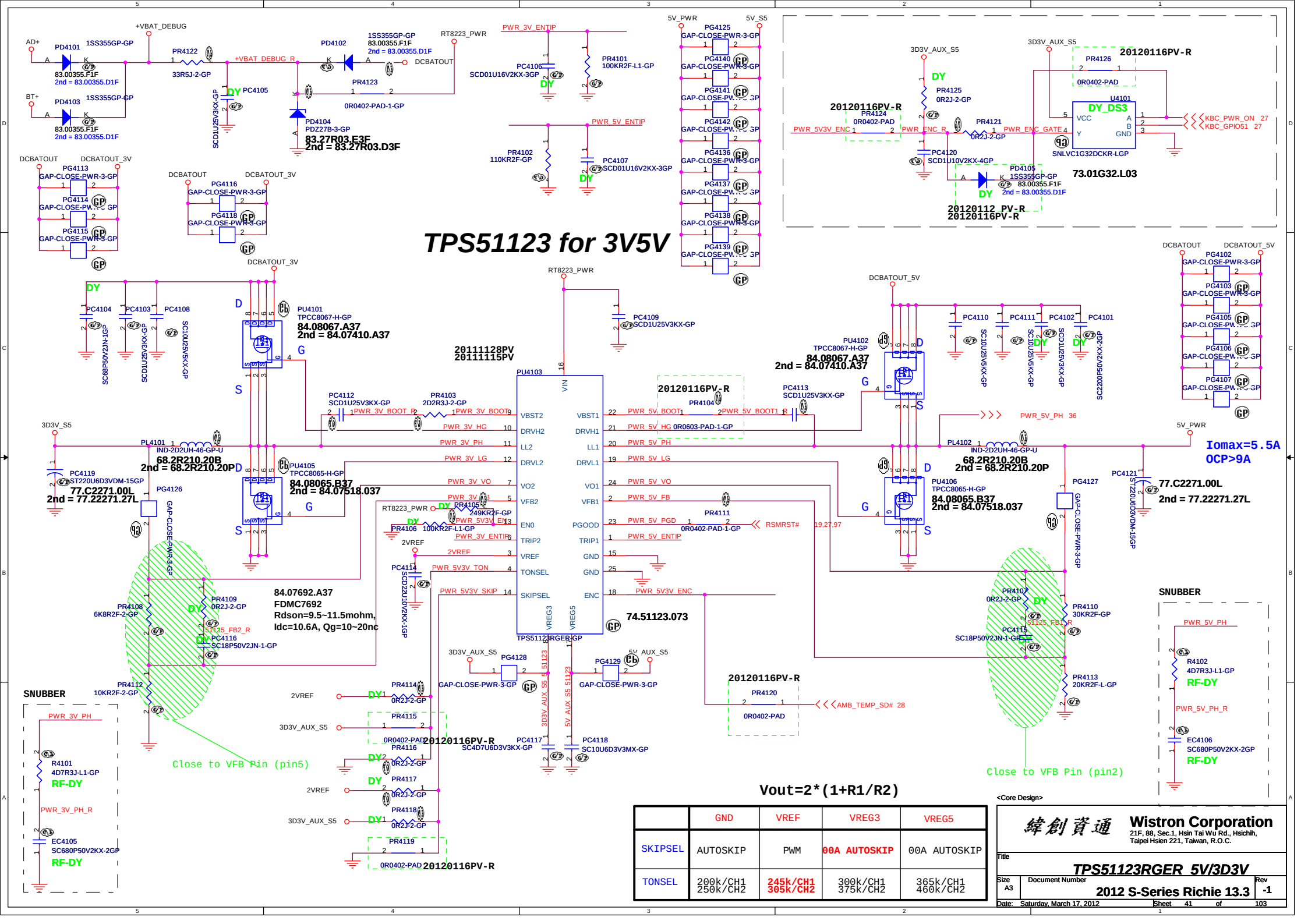
<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: ***BATT CONN***		
Size: A3	Document Number: **2012 S-Series Richie 13.3**	Rev: -1
Date: Wednesday, March 14, 2012	Sheet 39 of 103	

BQ24736 for CHARGER



TPS51123 for 3V5V



	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

<Core Design>

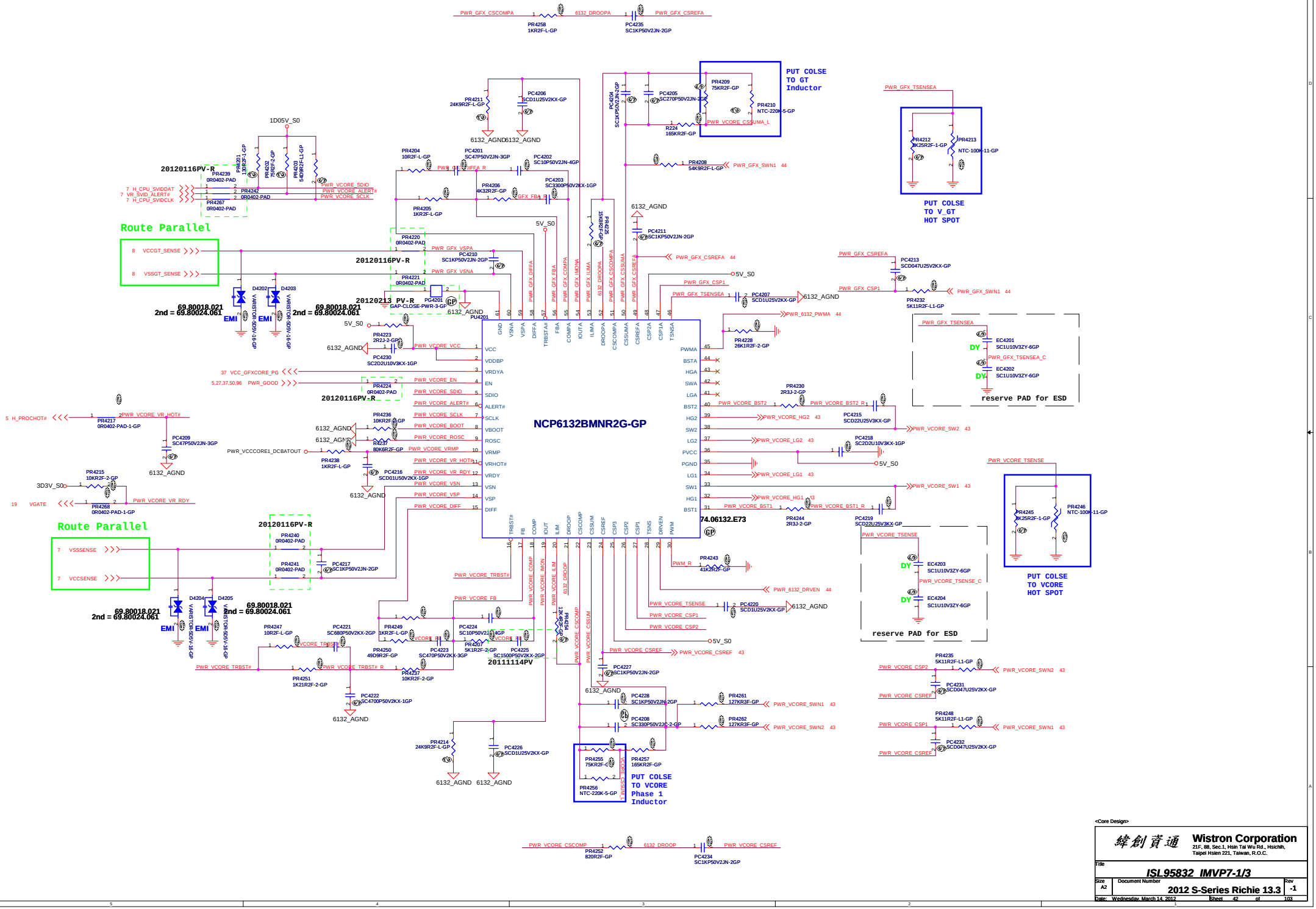
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51123RGER 5V/3D3V

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

Date: Saturday, March 17, 2012 | Sheet 41 of 103

SSID = CPU.Regulator



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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL95832 IMVP7-1/3

Size	Document Number	Rev
A2	2012 S-Series Richie 13.3	-1

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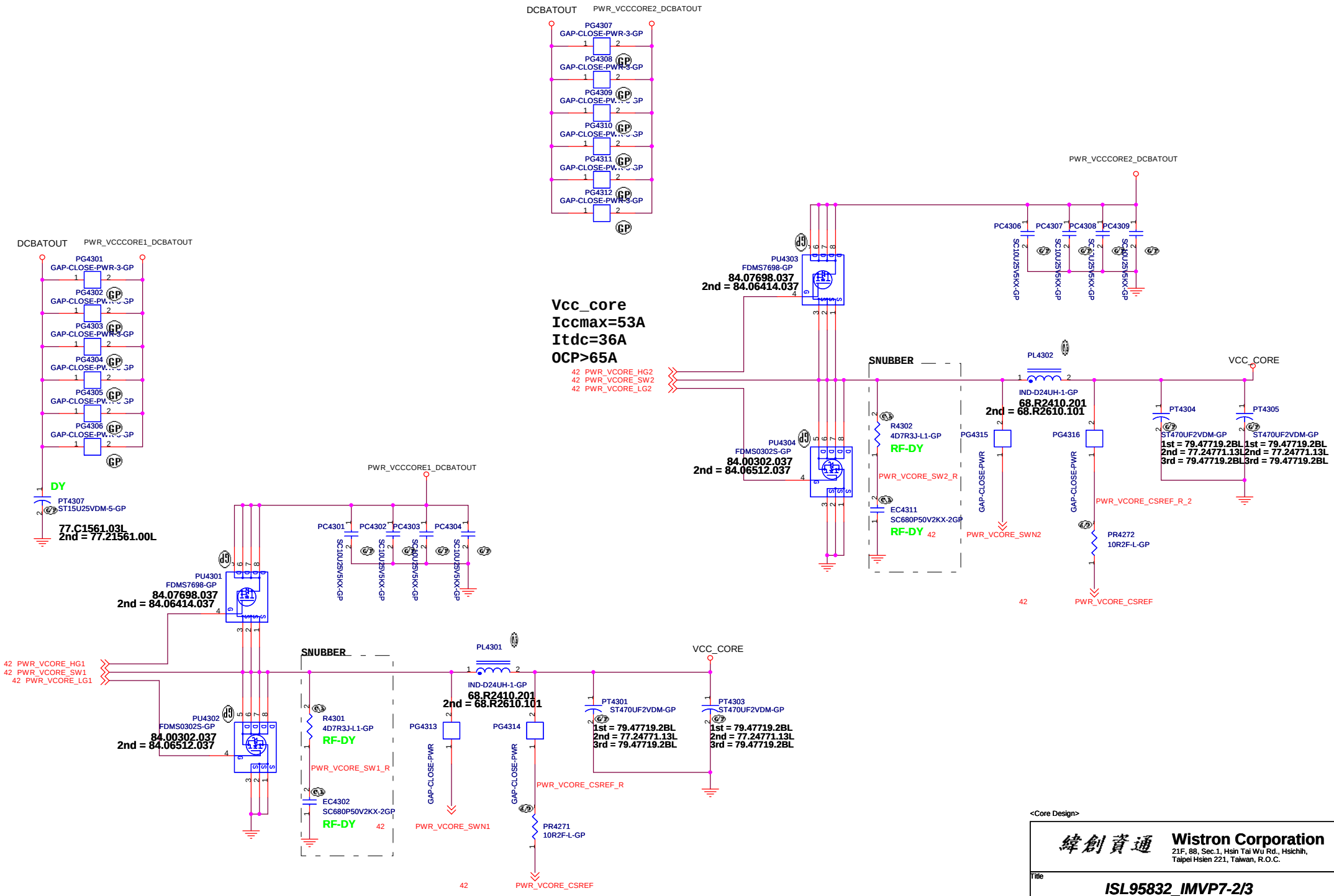

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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL95832_IMVP7-2/3

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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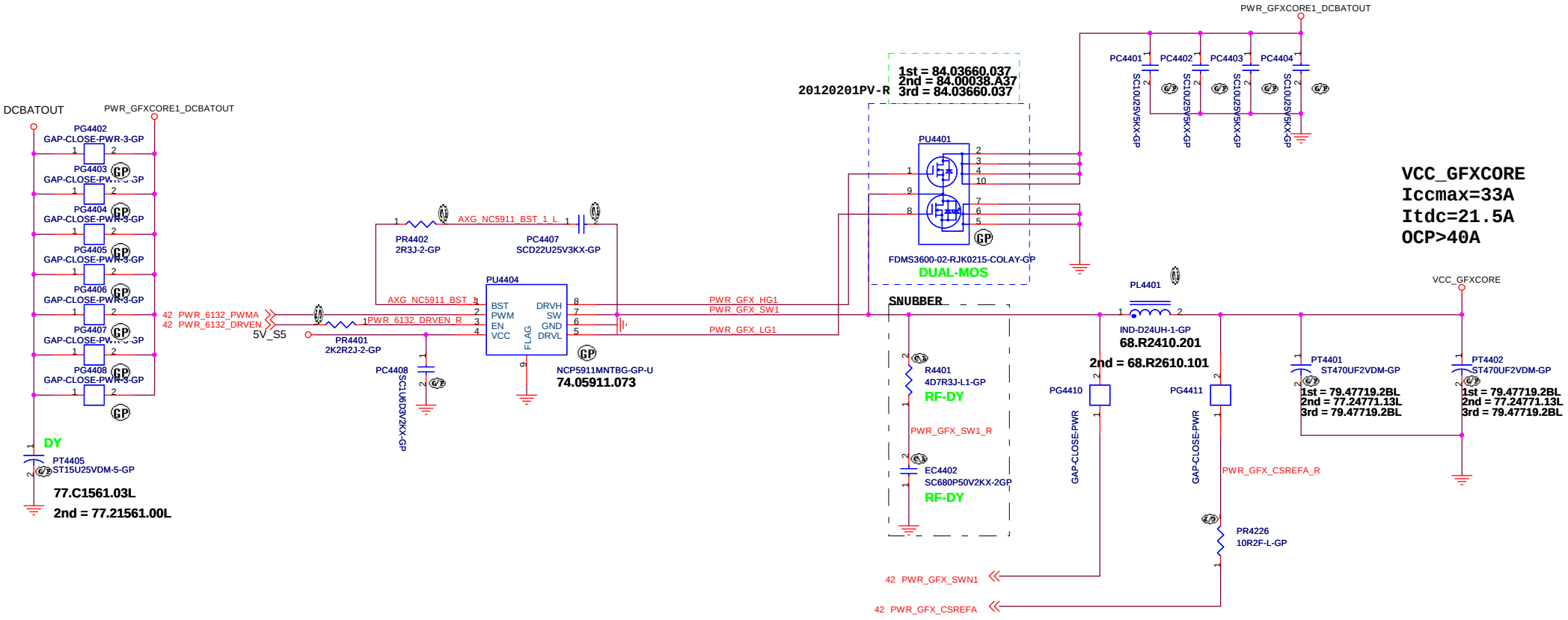
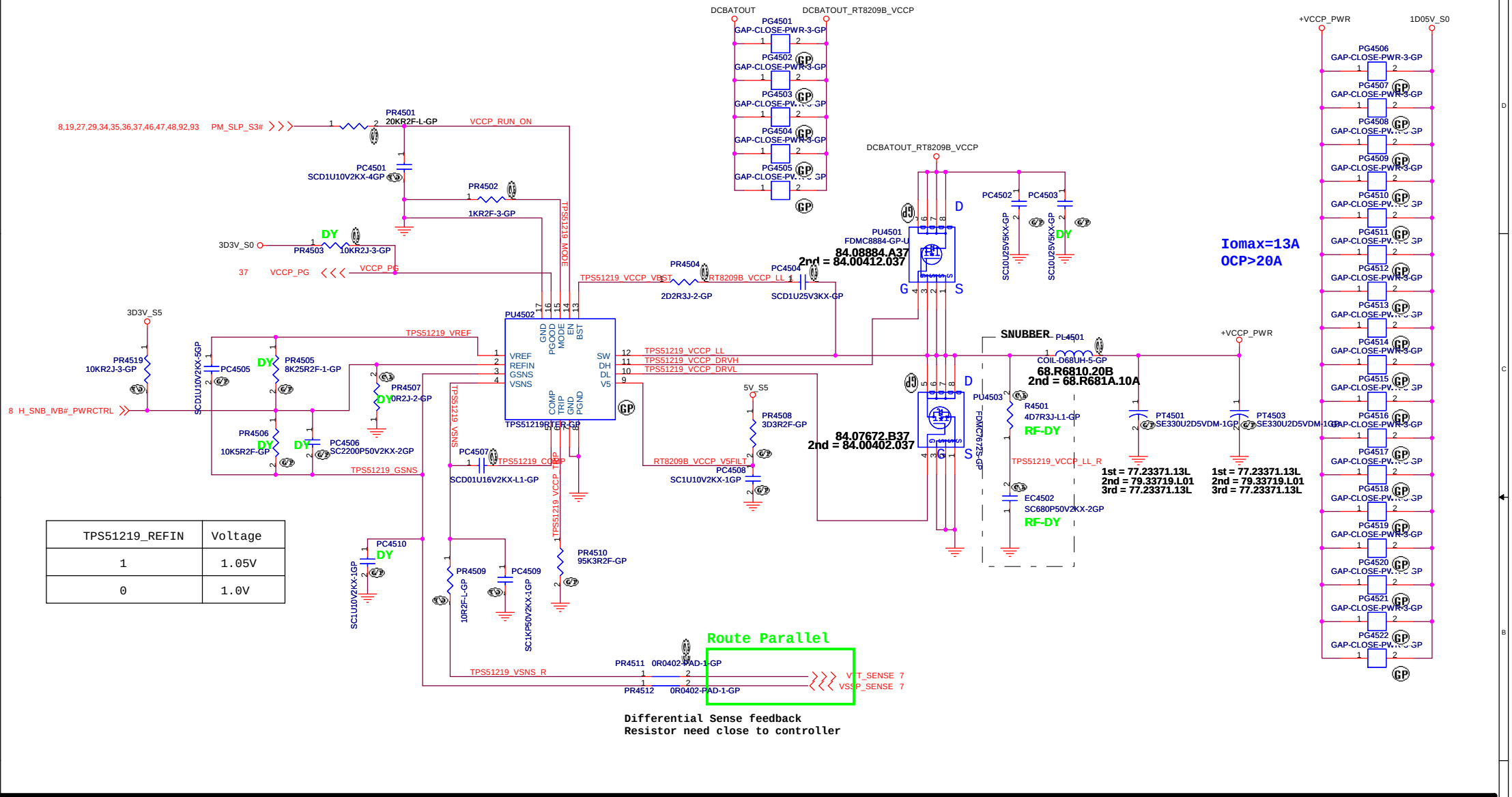


<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ISL95832_IMVP7-3/3		
Size: A3	Document Number: 2012 S-Series Richie 13.3	Rev: -1
Date: Monday, March 19, 2012	Sheet 44 of 103	



TPS51219_REFIN	Voltage
1	1.05V
0	1.0V

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51218_1D05V / 1D0V

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

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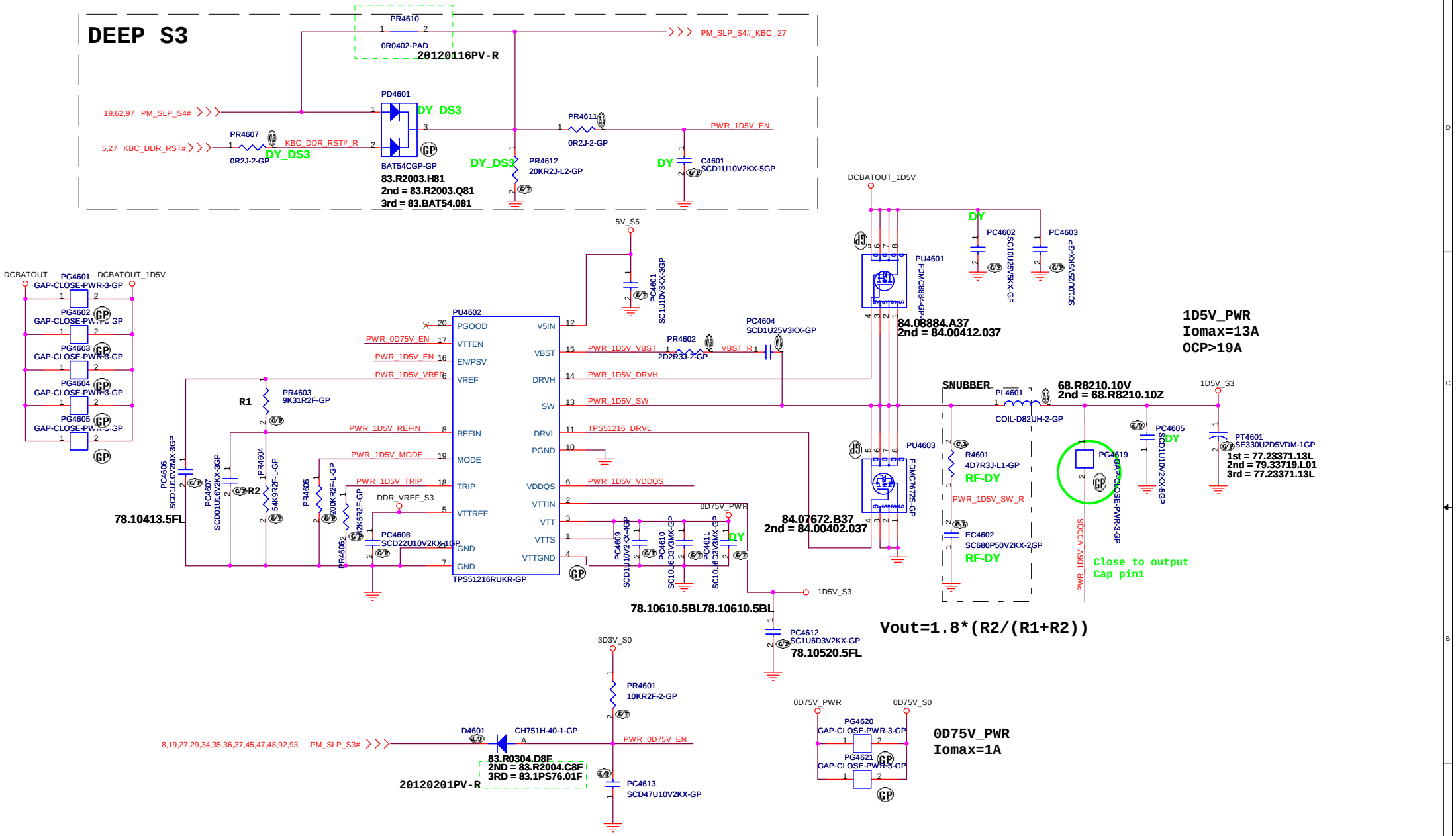

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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: UP1561_1D5V&0D75V

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

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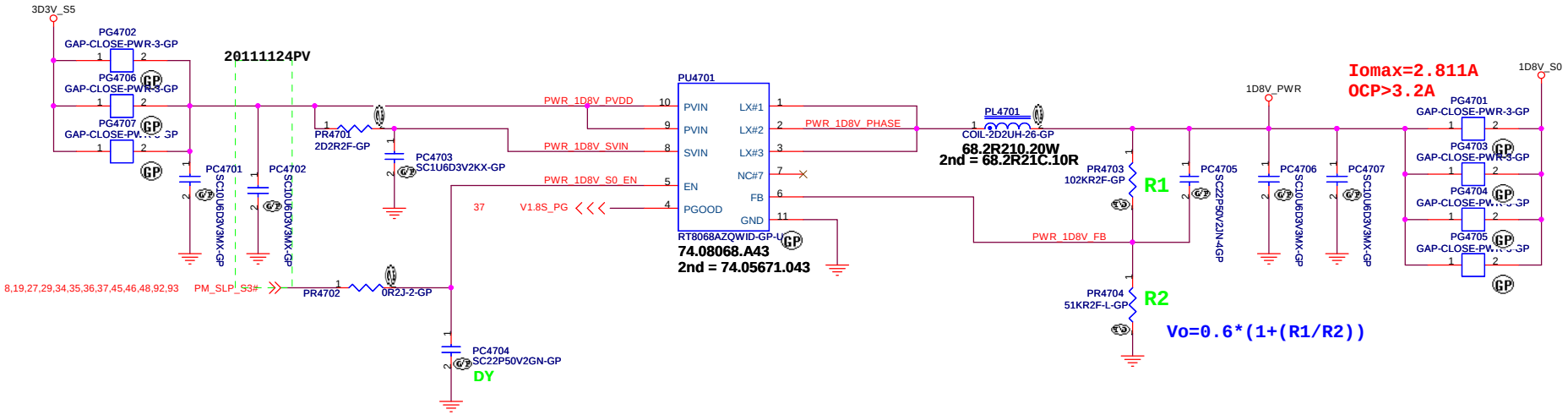
RT8068A for 1D8V_S0



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 1D8V_S0

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

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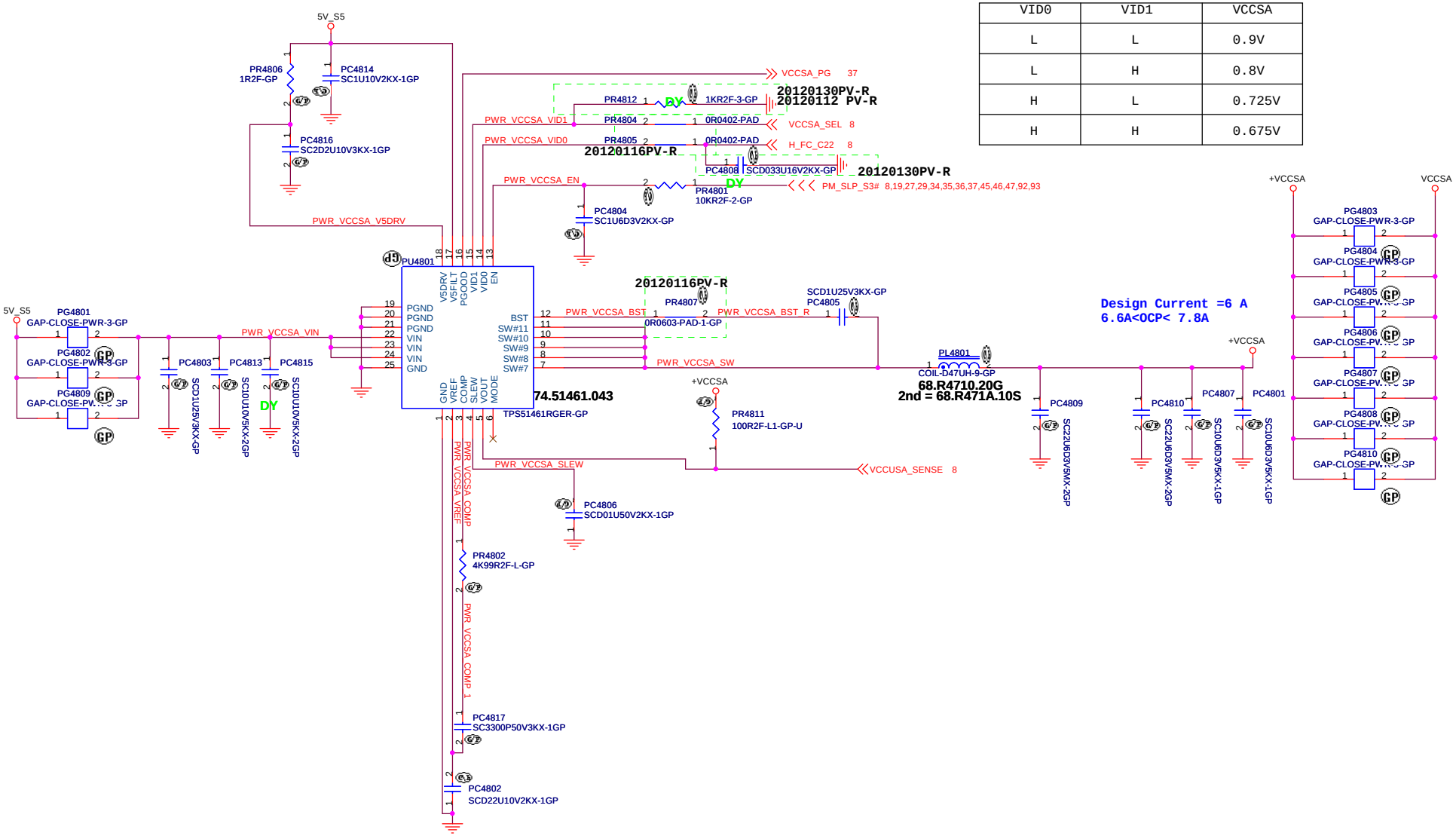
TPS51461 for VCCSA

VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***ISL95870A VCCSA***

Size	Document Number	Rev
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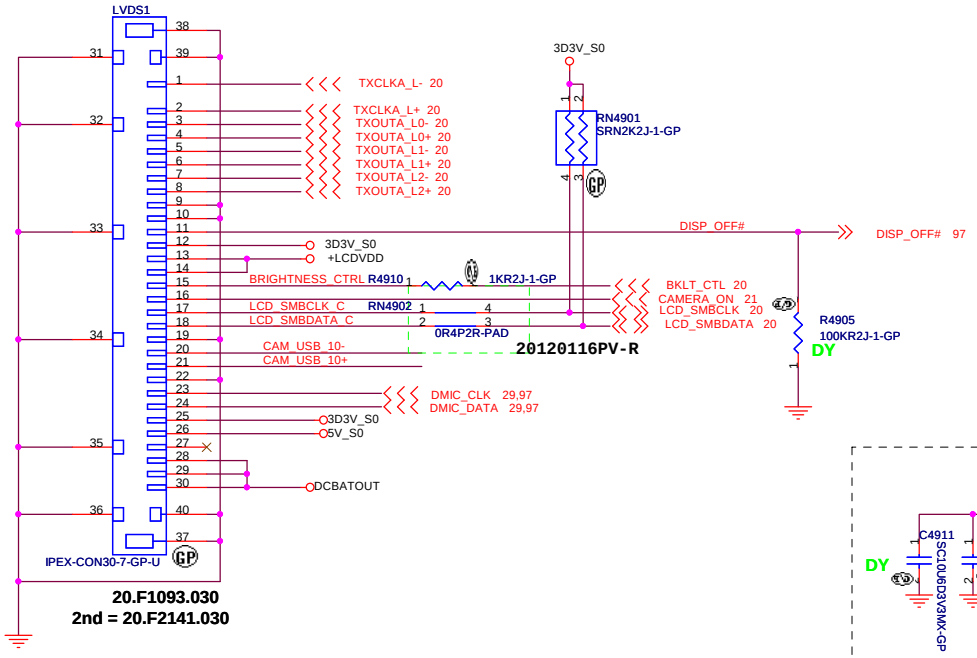
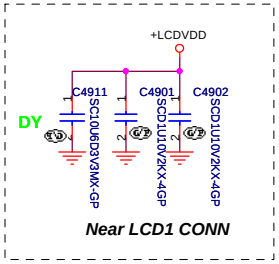
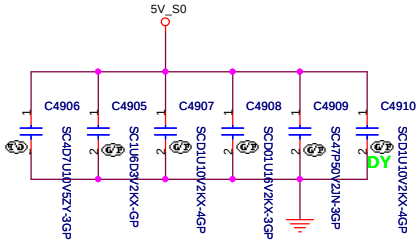
LCD Connector

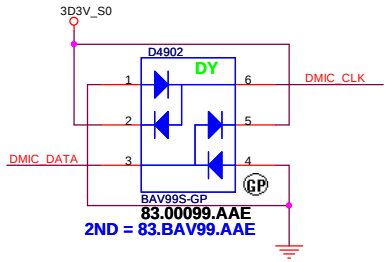
CARMER PINDEFINE

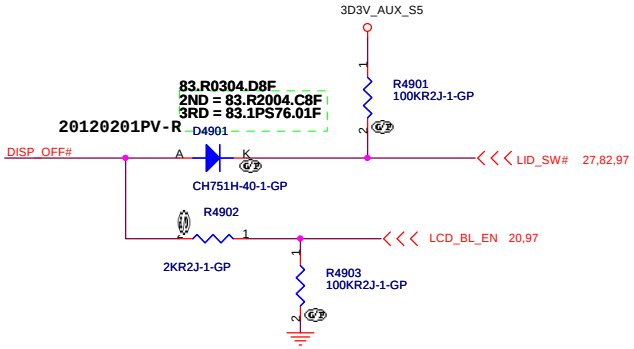
No.	Signal
1	DMIC_CLK
2	DMIC_DATA
3	GND
4	3.3V_MIC
5	5V_KBL
6	EN
7	VCC_5V
8	GND
9	D+
10	D-



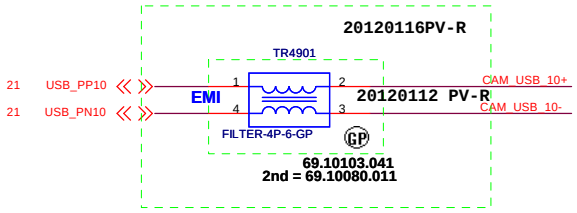




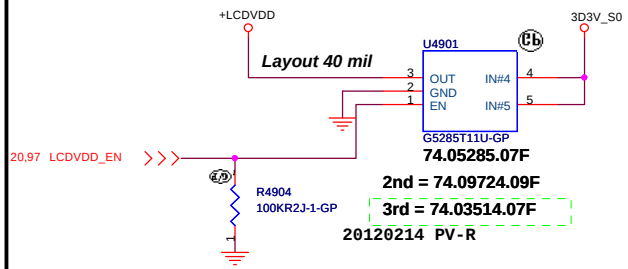




CAMERA



LCD POWER CIRCUIT



LED BACKLIGHT CONVERTER POWER

<Core Design>

緯創資通 Wistron Corporation
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Title: LCD Connector

Size	Document Number	Rev
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CRT Connector

CRT1
Transmission line
characteristic
impedance for RGB
signals Zo = 37.5 Ohm

Place these resistors as
the closest components to
connector CRT1

Transmission line characteristic
impedance Zo= 50 Ohm

Transmission line characteristic
impedance Zo = 50 Ohm

CRT RGB

68.00084.B61
2nd = 68.00245.051
3rd = 68.00226.141

MUX_R — L5001 BLM18BB470SN1D-GP — MUX_L_R — R5011 0R2J-2-GP — CRT_R
MUX_G — L5002 BLM18BB470SN1D-GP — MUX_L_G — R5012 0R2J-2-GP — CRT_G
MUX_B — L5003 BLM18BB470SN1D-GP — MUX_L_B — R5013 0R2J-2-GP — CRT_B

R1: R5001 R5002 R5003 75R2F-2-GP

C5001 C5002 C5003 SC22P50V2JN-4GP
C5004 C5005 C5006 SC22P50V2JN-4GP
C5007 C5008 C5009 SC22P50V2JN-4GP

DY DY DY 20120112 PV-R 20120116PV-R

DDC&HSYNC&VSYNC

5V_S0 — F5001 FUSE-1D1A6V-4GP-U — 1.1A/8V — +5VS_CRT_F2

Q5002 DMP2305U-7-GP
84.02305.G31
2nd = 84.02377.031
3rd = 84.02035.031
20120210PV-R
69.50007.691
2nd = 69.50007.771
3rd = 69.60040.011

CRTVDD_EN# 1
R5020 10KR2J-3-GP
R5019 10KR2J-3-GP
CRTVDD_EN#

5V_S0_CRT
C5020 SC4D7U10V5ZY-3GP DY
C5022 SCD1U16V2ZY-2GP

Q5001 2N7002K-2-GP
84.2N702.J31
2nd = 84.07002.I31
3rd = 84.2N702.W31

5,27,37,42,96 PWR_GOOD

C5019 SCD1U16V2ZY-2GP DY

CRT1
NC#4 NC#11
VCC_CRT
DDCDATA_ID1 DDCCLK_ID3
CRT_RED CRT_GREEN CRT_BLUE
VSYNC HSYNC
GND GND GND GND GND GND GND GND
D-SUB-15-123-GP
20.20938.015
2nd = 20.20984.015

DDC_DATA_CON
DDC_CLK_CON
CRT_R
CRT_G
CRT_B
CRT_VSYNC_CON_1
CRT_HSYNC_CON_1

RN5001 SRN2K2J-1-GP
C5023 C5021 SC22P50V2JN-4GP DY
C5024 C5025 SC33P50V2JN-3GP DY

3D3V_S0 — RN5007 SRN10KJ-5-GP — M_HSYNC M_VSYNC

20120116PV-R
20 PCH_RED — R5006 0R0402-PAD — MUX_R
20 PCH_GREEN — R5007 0R0402-PAD — MUX_G
20 PCH_BLUE — R5008 0R0402-PAD — MUX_B

5V_S0_CRT — C5016 SCD1U16V2ZY-2GP

73.1G125.D0G
2nd = 73.07125.0AG
3rd = 73.1G125.0JH
U5001 U74AHCT1G125G-AL5-R-GP-U
OE# VCC A GND Y

M_HSYNC
M_VSYNC

20120116PV-R
RN5002 0R4P2R-PAD
20 CRT_HSYNC
20 CRT_VSYNC

U5002 U74AHCT1G125G-AL5-R-GP-U
73.1G125.D0G
2nd = 73.07125.0AG
3rd = 73.1G125.0JH

5V @ ext. CRT side
RN5003 SRN33J-5-GP
HSYNC_5
VSYNC_5
CRT_HSYNC_CON_1
CRT_VSYNC_CON_1

C5018 C5017 SC10P50V2JN-4GP DY

3D3V_S0 — RN5004 SRN2K2J-1-GP

20120116PV-R
2011102PV
20120116PV-R
RN5008 0R4P2R-PAD
20 CRT_DDC_DATA
20 CRT_DDC_CLK

CRT_DDC_DATA_R
CRT_DDC_CLK_R

Q5003 2N7002KDW-GP
DDC_DATA_CON
DDC_CLK_CON

84.2N702.A3F
2nd = 84.2N702.E3F
3rd = 84.2N702.F3F

5V_S0_CRT — D5004 BAV99S-GP DY
83.00099.AAE
2ND = 83.BAV99.AAE
CRT_VSYNC_CON_1
CRT_HSYNC_CON_1

AFTP5001 AFTE14P-GP
AFTP5002 AFTE14P-GP
AFTP5003 AFTE14P-GP
AFTP5004 AFTE14P-GP
AFTP5005 AFTE14P-GP
AFTP5006 AFTE14P-GP
AFTP5007 AFTE14P-GP
AFTP5009 AFTE14P-GP
AFTP5011 AFTE14P-GP
AFTP5008 AFTE14P-GP
AFTP5010 AFTE14P-GP
AFTP5012 AFTE14P-GP

5V_S0_CRT — D5005 BAV99S-GP DY
83.00099.AAE
2ND = 83.BAV99.AAE
DDC_CLK_CON
DDC_DATA_CON

3D3V_S0 — D5006 BAV99S-GP DY
83.00099.AAE
2ND = 83.BAV99.AAE
CRT_R
CRT_G

3D3V_S0 — D5003 BAV99-5-GP DY
83.00099.T11
2nd = 83.BAV99.D11
3rd = 83.BAV99.H11
CRT_B

3D3V_S0 — C5010 SCD1U10V2KX-4GP DY

20120131PVR

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT Connector
Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1
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HDMI Connector

HDMI CONN

20120130PV-R

TR5101
HDMI_CLK_R_C 1 2 HDMI_CLK_R_C_CON
HDMI_CLK_R_C# 4 3 HDMI_CLK_R_C#_CON
COIL-90OHM-100MHZ-3-GP
68.11900.20A
2nd = 69.10098.031
3rd = 69.10118.021

TR5103
HDMI_DATA1_R_C 1 2 HDMI_DATA1_R_C_CON
HDMI_DATA1_R_C# 4 3 HDMI_DATA1_R_C#_CON
COIL-90OHM-100MHZ-3-GP
68.11900.20A
2nd = 69.10098.031
3rd = 69.10118.021

TR5102
HDMI_DATA0_R_C 1 2 HDMI_DATA0_R_C_CON
HDMI_DATA0_R_C# 4 3 HDMI_DATA0_R_C#_CON
COIL-90OHM-100MHZ-3-GP
68.11900.20A
2nd = 69.10098.031
3rd = 69.10118.021

TR5104
HDMI_DATA2_R_C 1 2 HDMI_DATA2_R_C_CON
HDMI_DATA2_R_C# 4 3 HDMI_DATA2_R_C#_CON
COIL-90OHM-100MHZ-3-GP
68.11900.20A
2nd = 69.10098.031
3rd = 69.10118.021

HDMI_PLL_GND
DY R5123 0R2J-2-GP
Q5103 2N7002K-2-GP
3D3V_S0
DY R5113 100KR2J-1-GP
84.2N702.J31
2nd = 84.07002.I31
3rd = 84.2N702.W31

HDMI1
SKT-HDMI23-54-GP
22.10296.721
2nd = 22.10296.761
HDMI_DATA2_R_C_CON
HDMI_DATA2_R_C#_CON
HDMI_DATA1_R_C_CON
HDMI_DATA1_R_C#_CON
HDMI_DATA0_R_C_CON
HDMI_DATA0_R_C#_CON
HDMI_CLK_R_C_CON
HDMI_CLK_R_C#_CON
DDC_CLK_HDMI
DDC_DATA_HDMI
5V_S0_CRT
C5102 SCD1U10V2KX-5GP

Close to PCH

20 HDMI_CLK_R#
20 HDMI_CLK_R
C5103 C5104 SCD1U10V2KX-5GP
HDMI_CLK_R_C#
HDMI_CLK_R_C

20 HDMI_DATA0_R#
20 HDMI_DATA0_R
C5105 C5106 SCD1U10V2KX-5GP
HDMI_DATA0_R_C#
HDMI_DATA0_R_C

20 HDMI_DATA1_R#
20 HDMI_DATA1_R
C5110 C5107 SCD1U10V2KX-5GP
HDMI_DATA1_R_C#
HDMI_DATA1_R_C

20 HDMI_DATA2_R#
20 HDMI_DATA2_R
C5108 C5109 SCD1U10V2KX-5GP
HDMI_DATA2_R_C#
HDMI_DATA2_R_C

Close to HDMI Connector

RN5106 SRN680J-GP
RN5107 SRN680J-GP
HDMI_PLL_GND

HPD_HDMI_CON
3D3V_S0
HDMI_HPD_B
R5111 150KR2J-L1-GP
Q5102 PMBS3904-1-GP
84.03904.L06
2nd = 84.03904.X11
DY R5110 200KR2J-L1-GP
HDMI_HPD_R
R5128 0R0402-PAD
HDMI_PCH_DET 20,97
R5112 20KR2F-L-GP
20120116PV-R

5V_S0_CRT
3D3V_S0
RN5101 SRN2K2J-1-GP
Q5104 2N7002KDW-GP
20 PCH_HDMI_CLK
20 PCH_HDMI_DATA
DDC_CLK_HDMI
DDC_DATA_HDMI
84.2N702.A3F
2nd = 84.2N702.E3F
3rd = 84.2N702.P3F

Routing Guidelines:
CTRLDATA must be routed longer than CTRLCLK within 1000 mils (25.4 mm).
The total delay on CTRLDATA should be longer than CTRLCLK.

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Conn
Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1
Date: Wednesday, March 14, 2012 | Sheet 51 of 103

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)***

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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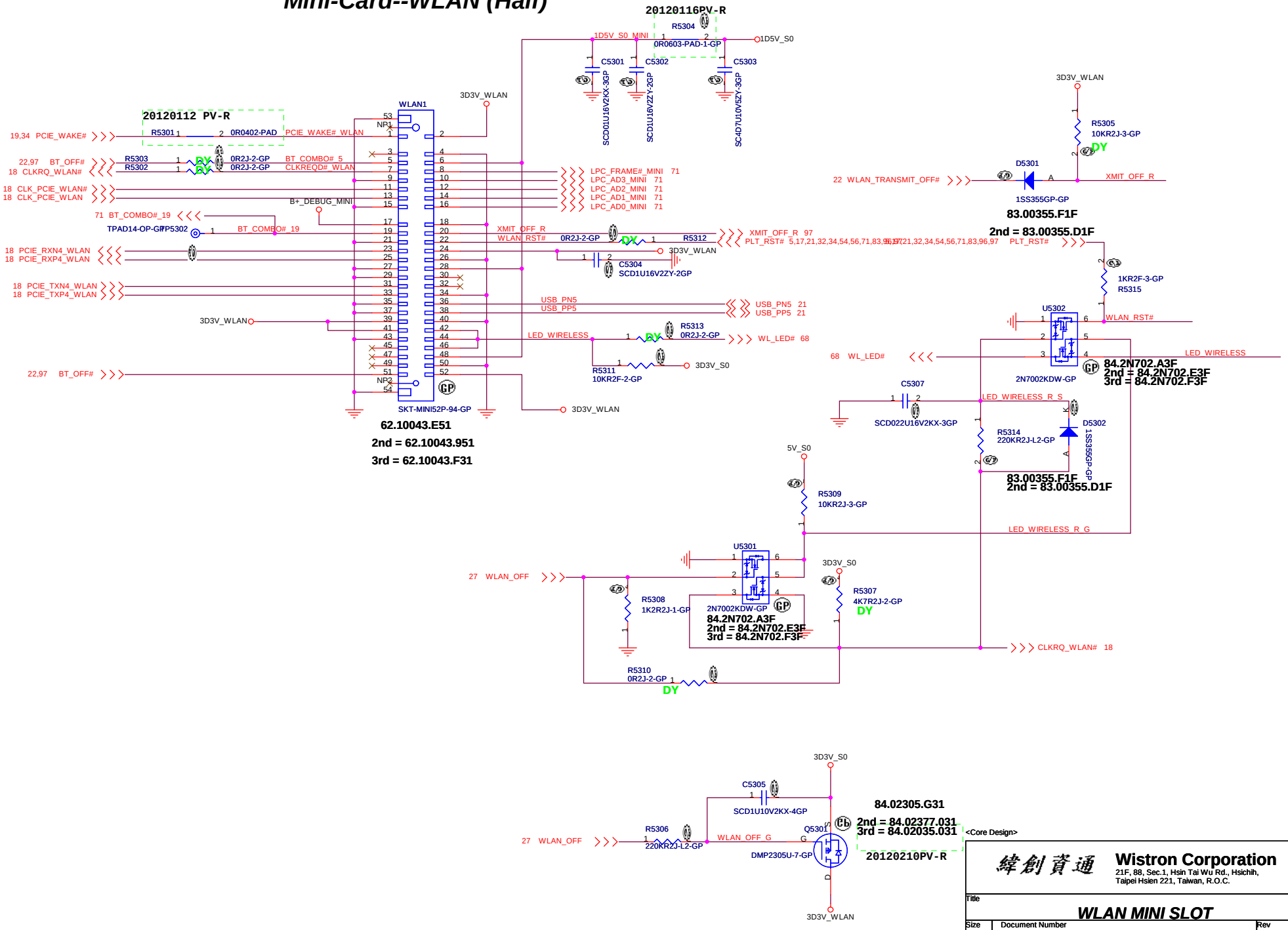
WLAN Connector

Mini-Card--WLAN (Half)



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	**WLAN MINI SLOT**	
Size: A3	Document Number: 2012 S-Series Richie 13.3	Rev: -1
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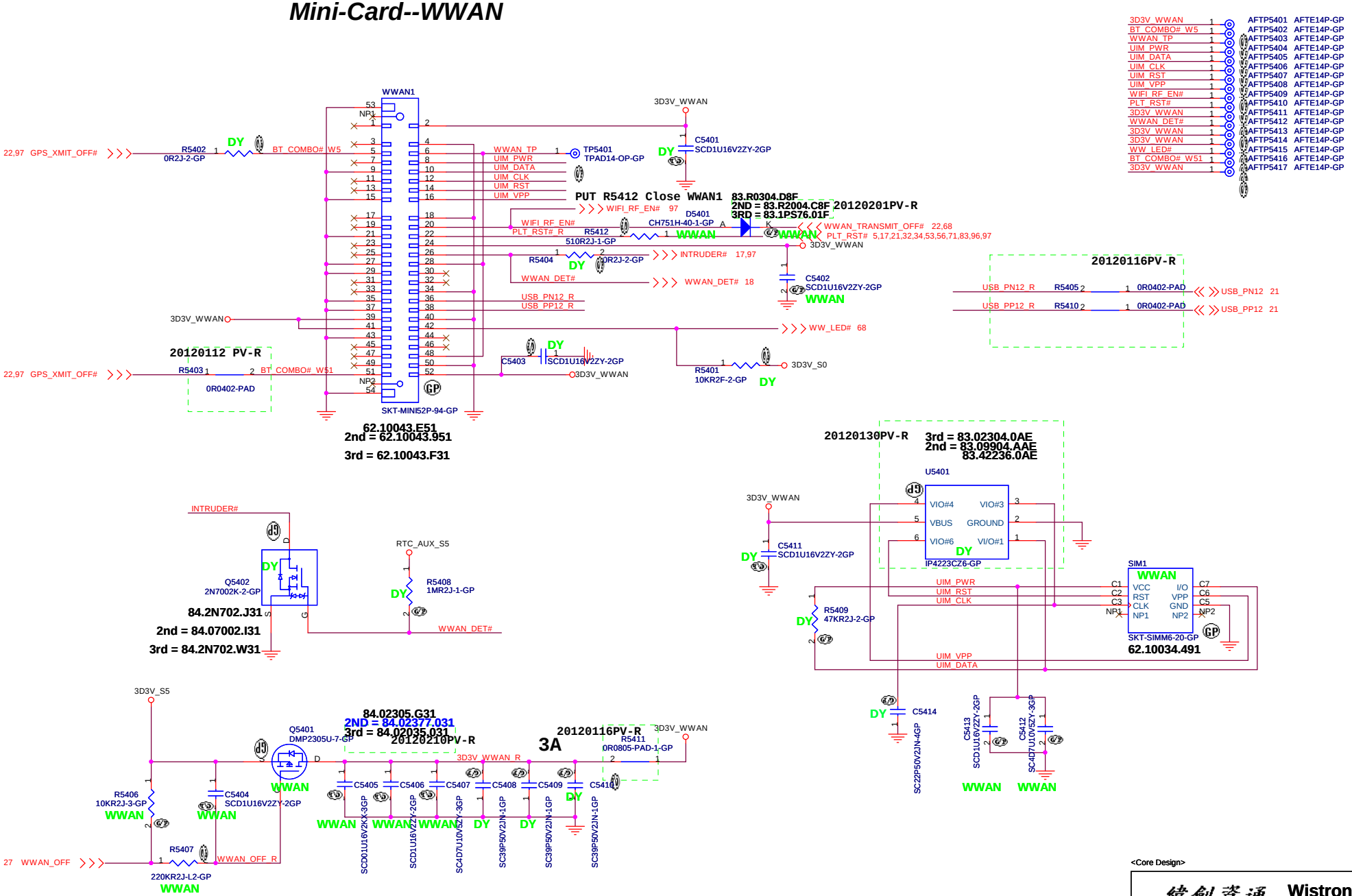
WWAN Connector

Mini-Card--WWAN



Title: WWAN MINI SLOT/SIM

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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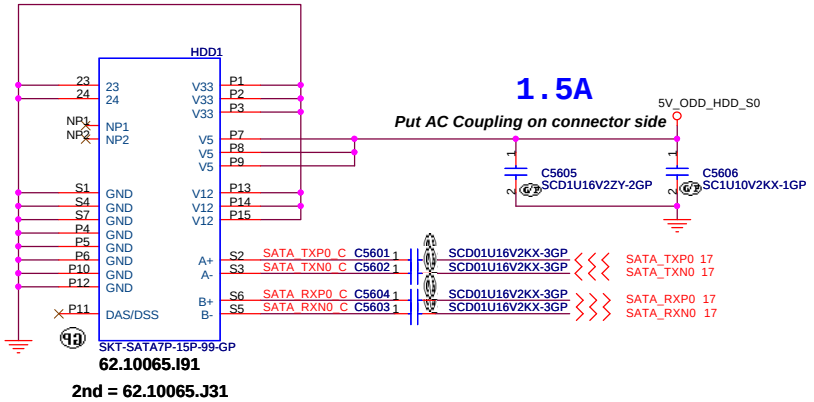
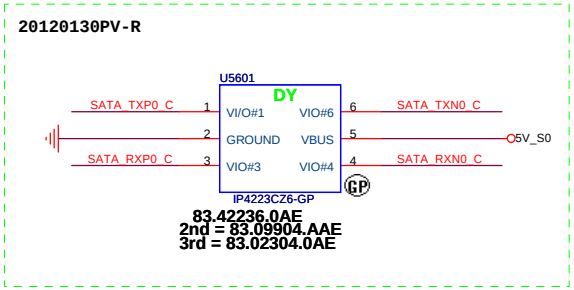
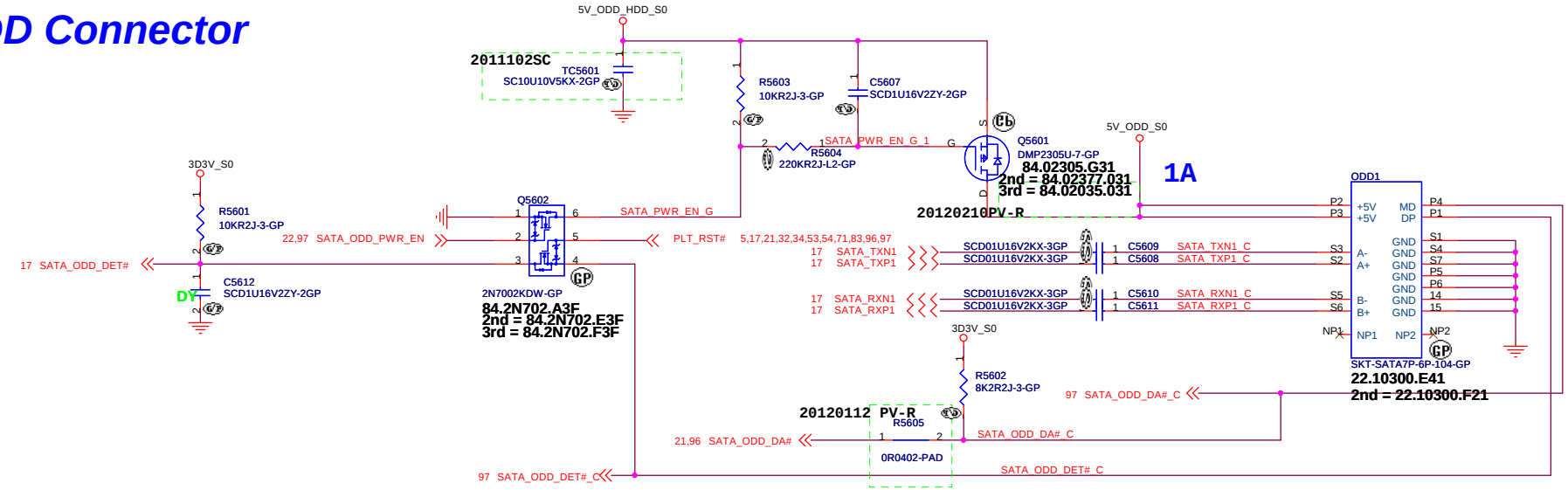
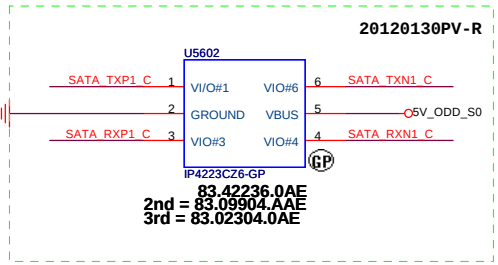
HDD Connector





ODD Connector





<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD

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A3	2012 S-Series Richie 13.3	-1

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<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)***

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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(Blanking)

<Core Design>

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Title: ***(Reserved)***

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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(Blanking)

<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
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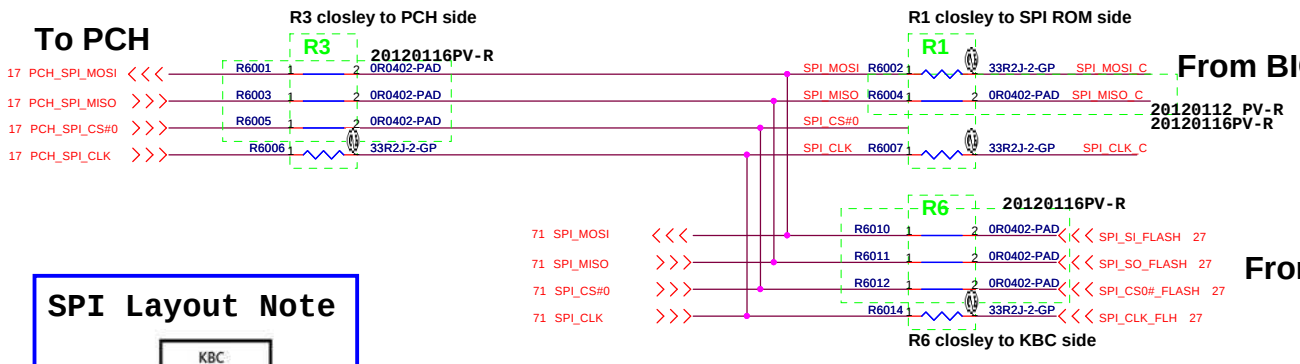
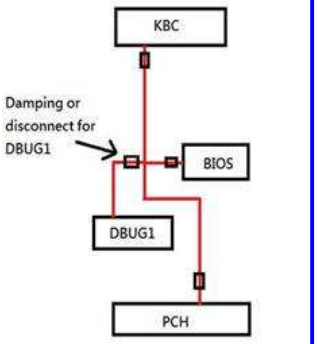
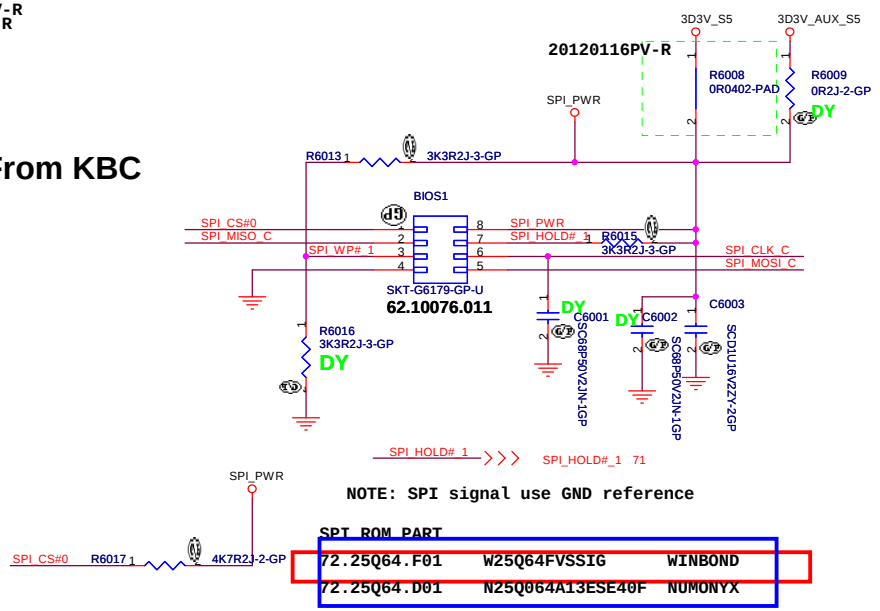
SSID = Flash.ROM



SPI Layout Note



SYSTEM SPI ROM Socket



NOTE: SPI signal use GND reference

SPI ROM PART

72.25Q64.F01	W25Q64FVSSIG	WINBOND
72.25Q64.D01	N25Q064A13ESE40F	NUMONYX

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

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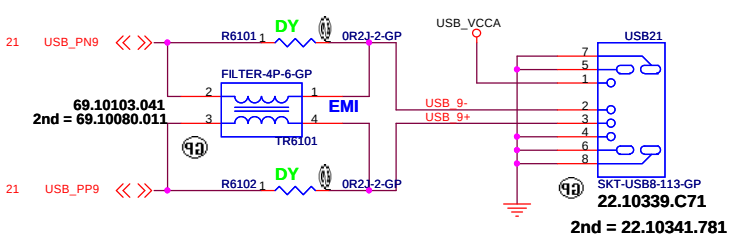
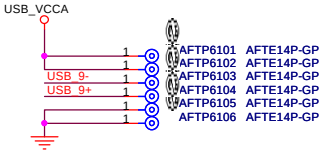
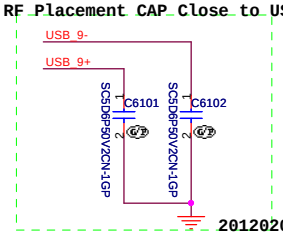
Right Side USB 2.0 Connector

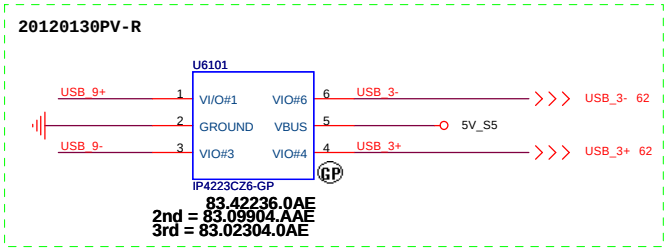
Right Side USB 2.0





For RF Placement CAP Close to USB21





<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB Power SW**

Size	Document Number	Rev
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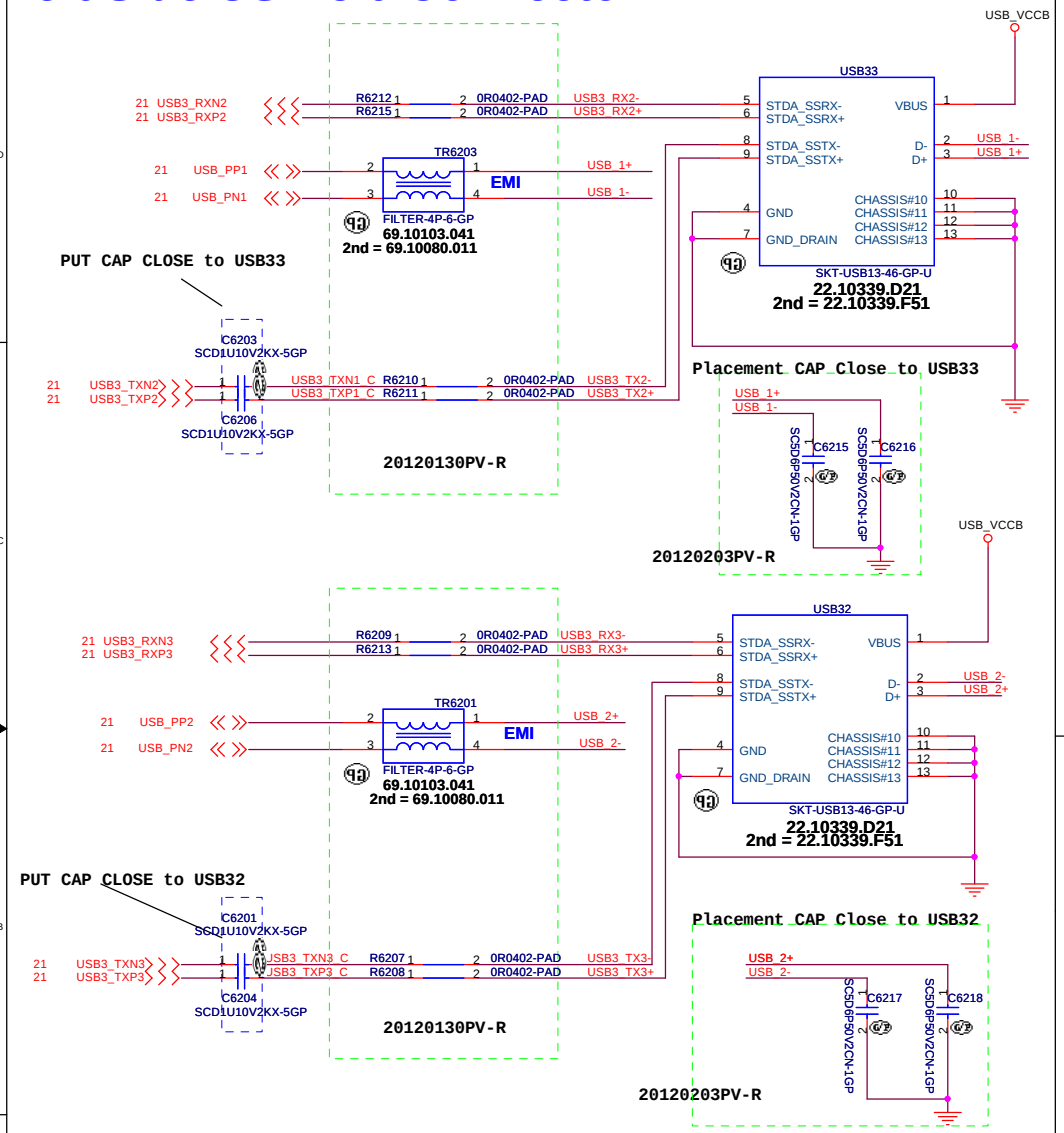
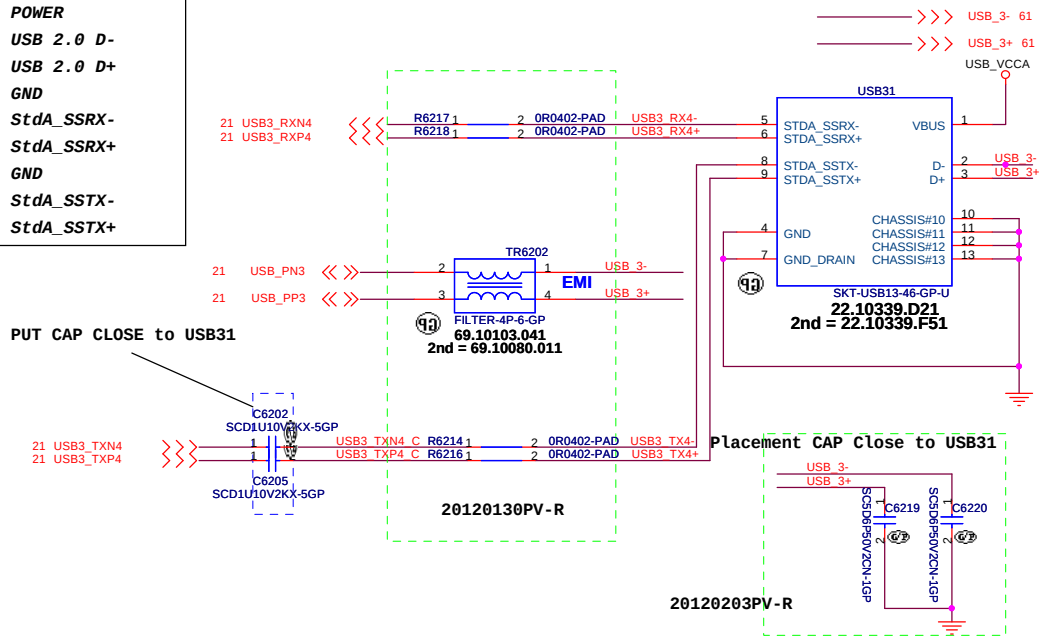
Left Side USB 3.0 Connector

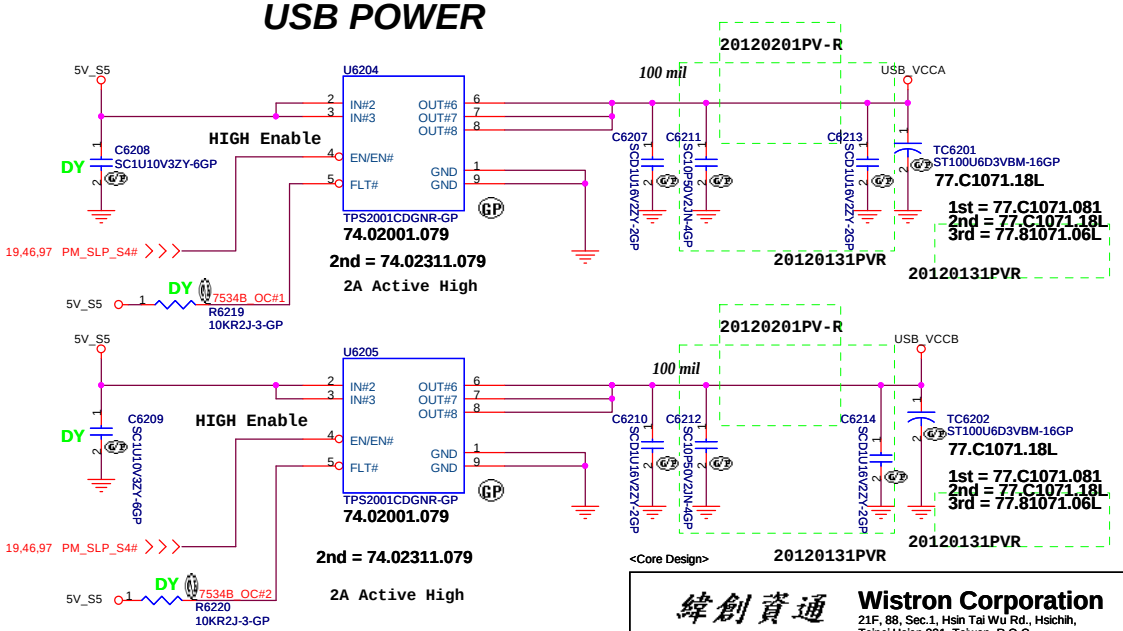


USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX-
6	StdA_SSRX+
7	GND
8	StdA_SSTX-
9	StdA_SSTX+

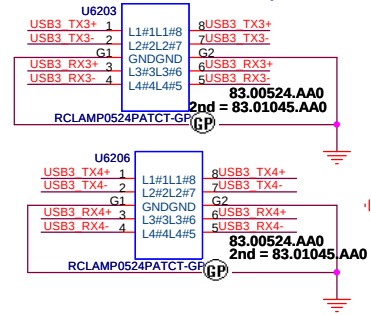
Right Side USB 3.0 Connector



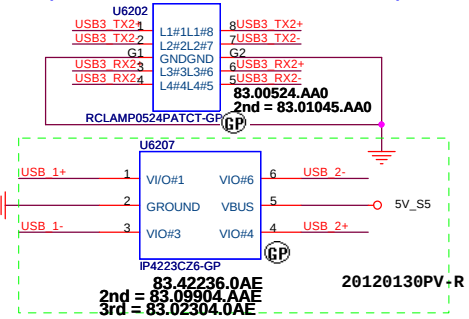
USB POWER



Ultra Low Capacitance TVS Arrays (Pin5.6.7.8 No Internal Connection)



Ultra Low Capacitance TVS Arrays (Pin5.6.7.8 No Internal Connection)



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Title	USB3.0		
Size A3	Document Number 2012 S-Series Richie 13.3		Rev -1
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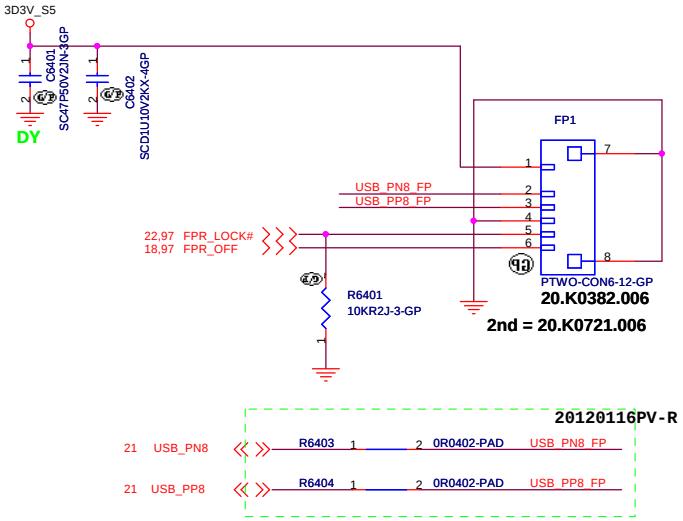
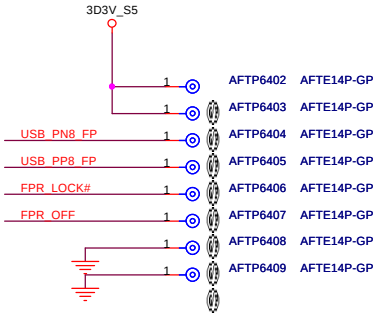
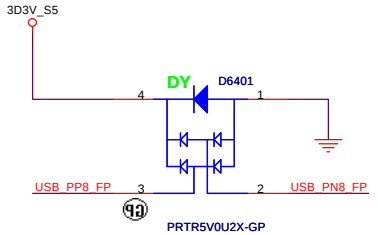
Finger Printer Connector







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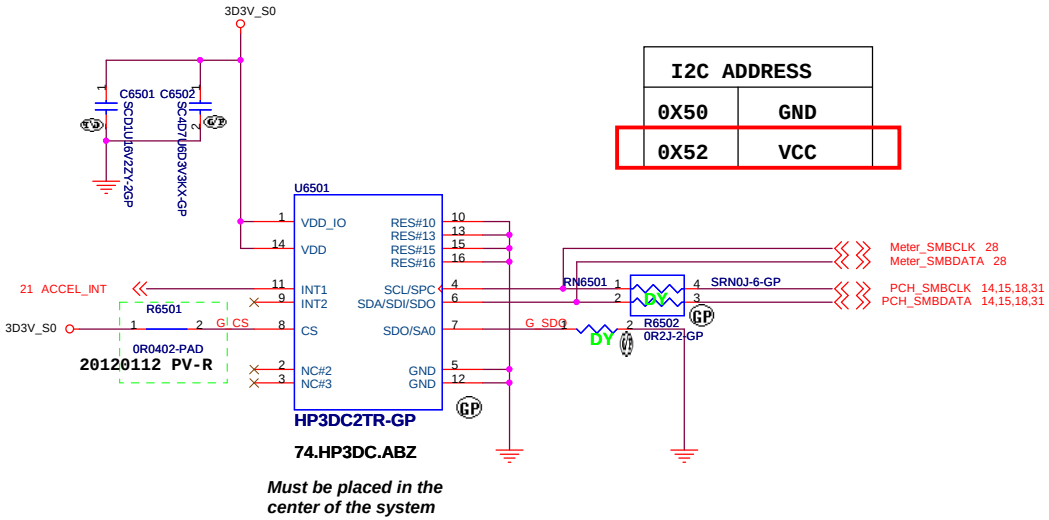
ACCELEROMETER



I2C ADDRESS	
0X50	GND
0X52	VCC

Must be placed in the center of the system

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Title: ACCELEROMETER

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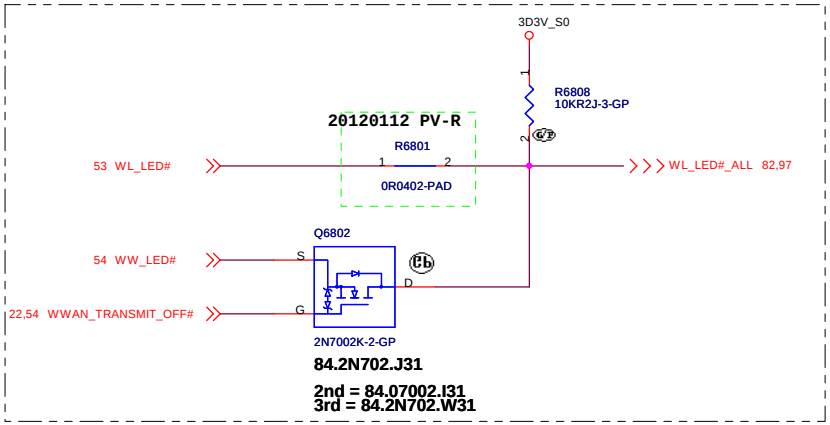
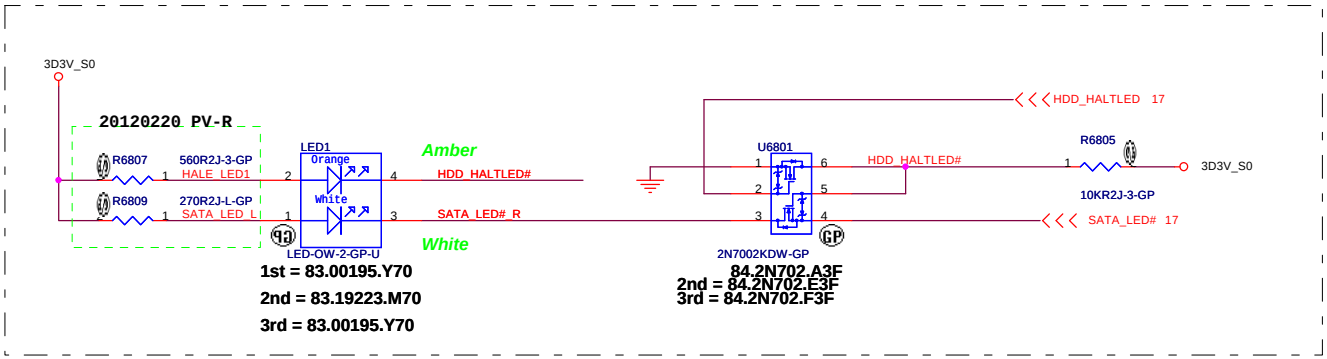
WLAN / WWAN POWER LED



HDD LED



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Title: LED Control

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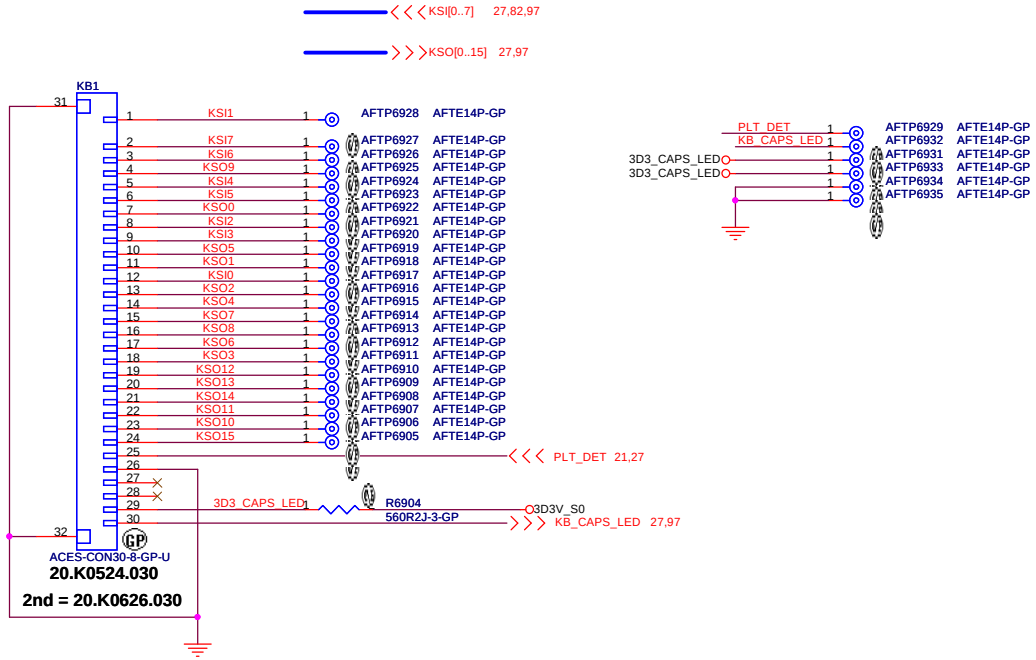
Keyboard Connector



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Title: ***Key Board/Touch Pad***

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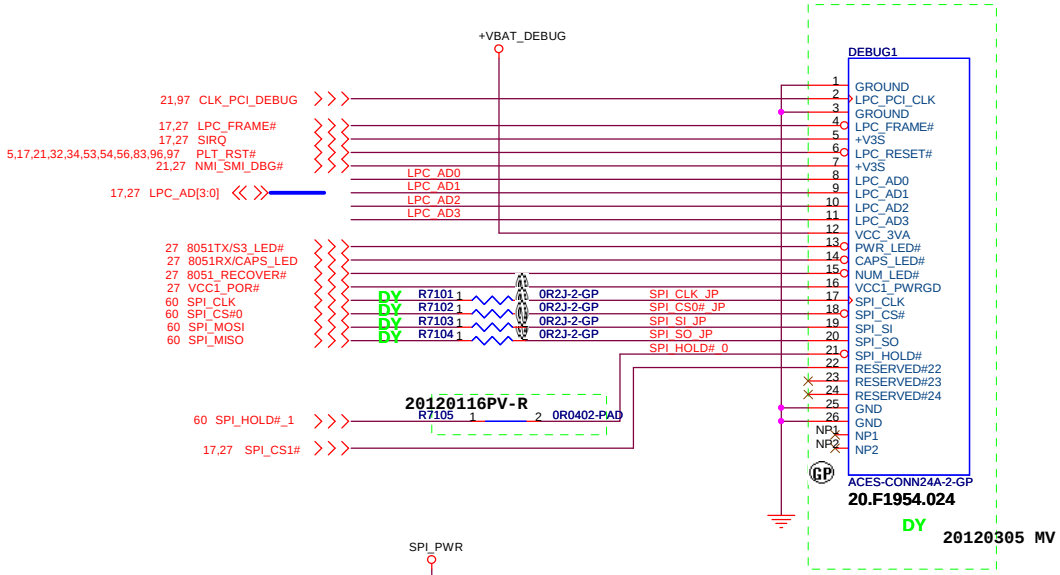
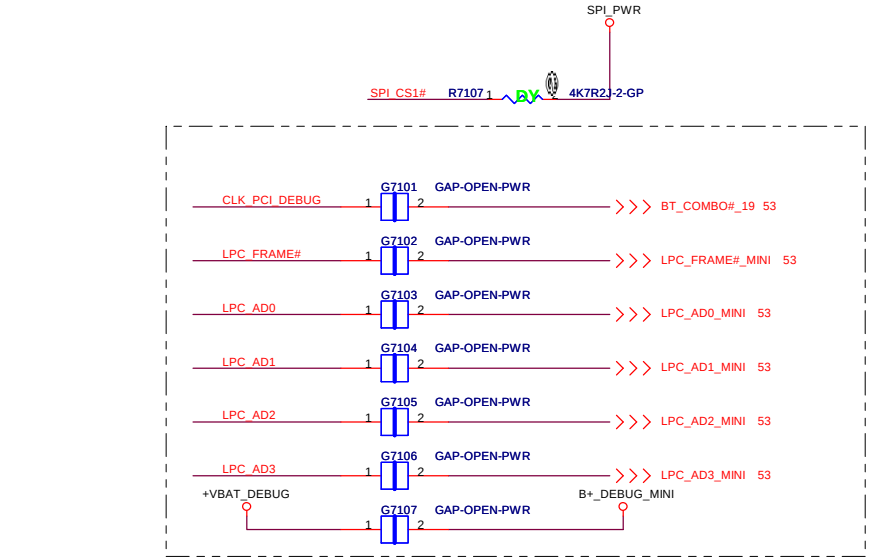
24 PIN LPC DEBUG CONN.





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Title: ***Reserved***

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Title: ***Reserved***

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Title: ***TPM***

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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Title: ***Reserved***

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A3	2012 S-Series Richie 13.3	-1

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Title: ***Reserved***

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Title: ***Reserved***

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A3	2012 S-Series Richie 13.3	-1

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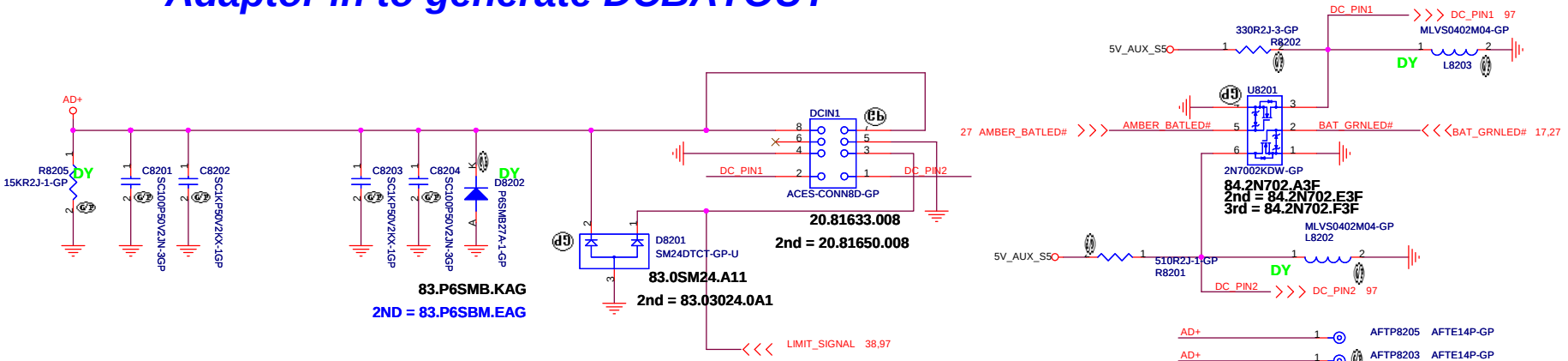
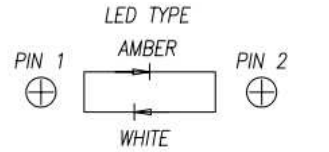
Adaptor in to generate DCBATOUT

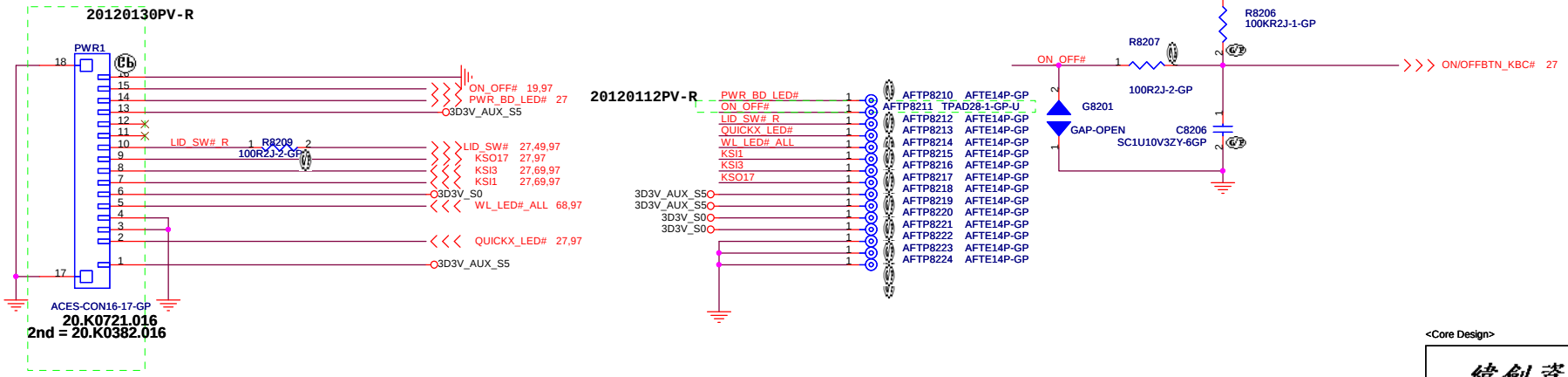




NODE		COLOR
PIN1(+)	PIN2(−)	AMBER
PIN1(−)	PIN2(+)	WHITE

	KBC pin 120 BAT_GRNLED#	KBC pin 113 AMBER_BATLED#
Amber	High	Low
White	Low	High
LED OFF	Low	Low

Power Button +Quick Lanch board



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Title: **POWER Button/ DCIN Connector**

Size	Document Number	Rev
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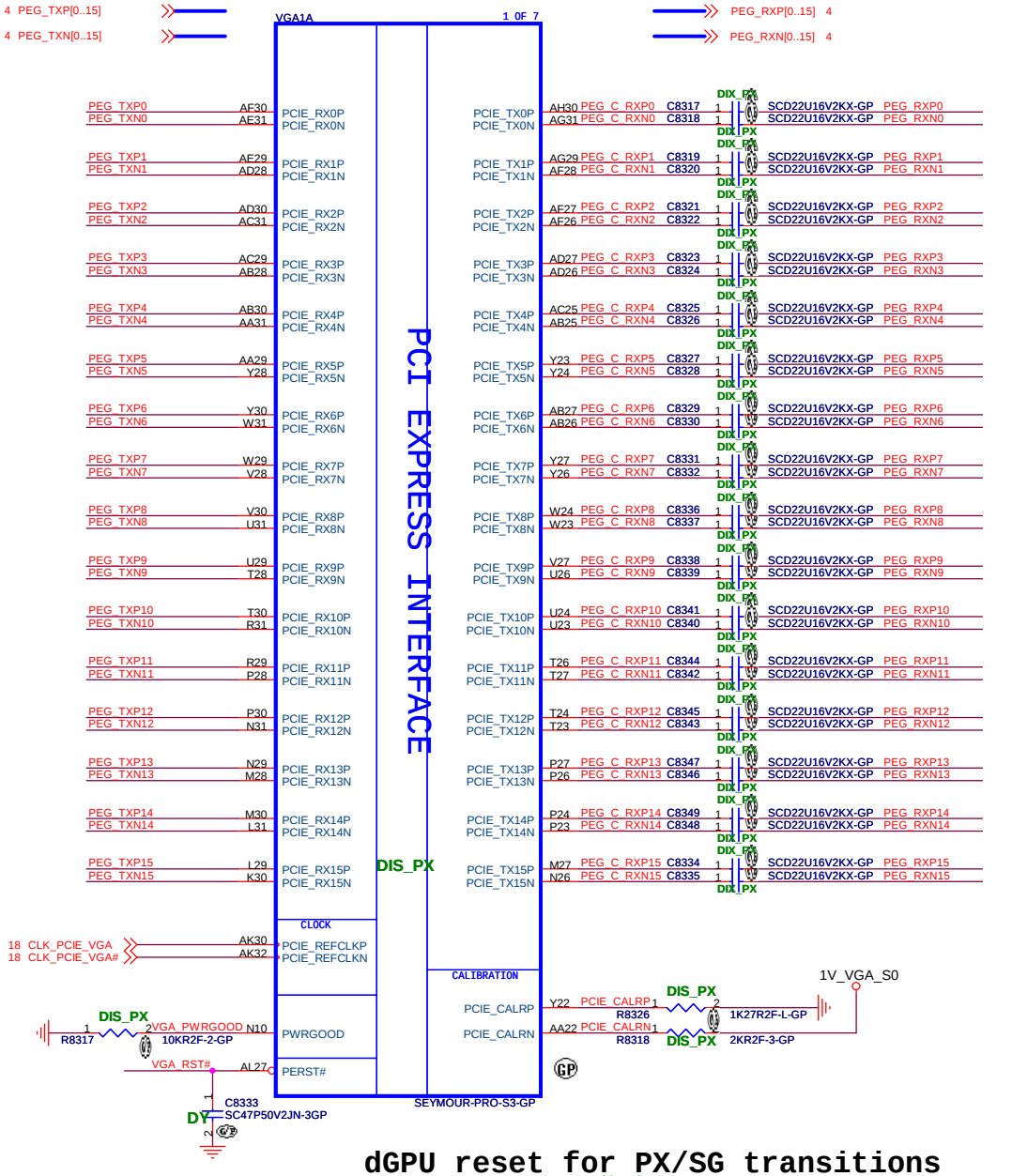
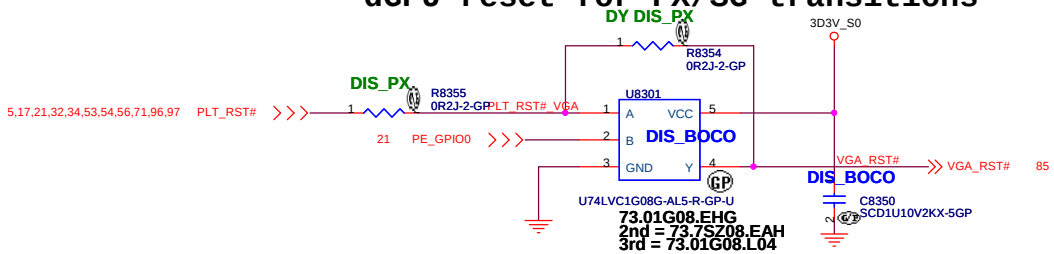


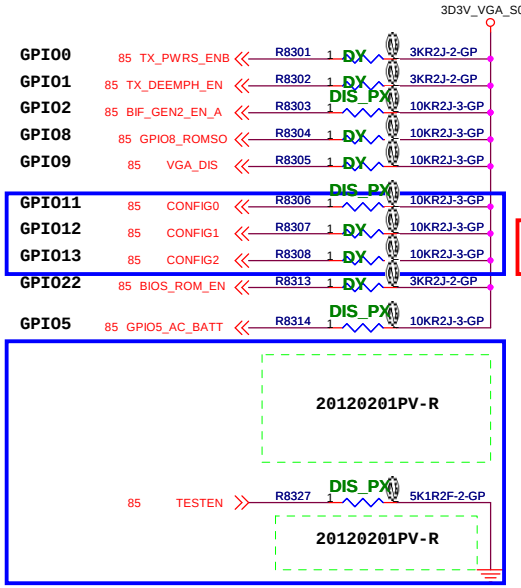


CONFIGURATION STRAPS

ALLOW FOR PULL-UP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMEND	PLATFORM SETTING
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	X	1
BIF_GEN2_EN_A	GPIO2	0:Advertises the PCIe device as 2.5GT/s capable at power on. 1:Advertises the PCIe device as 5.0GT/s capable at power on.	0	0
GPIO5_AC_BATT	GPIO5	AC (Performance mode) = 3.3 V Battery saving mode = 0.0 V	?	0
GPIO8_ROMSO	GPIO8	RESERVED	0	0
VGA_DIS	GPIO9	0:VGA Controller capacity enabled 1:The device won't be recognized as the system's VGA controller	0	0
ROMIDCFG[2:0]	GPIO[13:11]	BIOS_ROM_EN=1, Config[2:0] defines the ROM type BIOS_ROM_EN=0, Config[2:0] defines the primary memory aperture size	X X X	0 0 1 (256MB)
GPIO21_BB_EN	GPIO21	RESERVED	0	0
BIOS_ROM_EN	GPIO_22_ROMCSB	0:Disable external BIOS ROM device 1:Enable external BIOS ROM device	X	0
VIP_DEVICE_STRAP_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver that it sense whether or not a VIP device is connected on the VIP Host interface.	X	0
RSVD	H2SYNC	RESERVED	0	0
RSVD	GENERICC	RESERVED	0	0
AUD[1]	HSYNC	AUD[1:0]:11-Audio for both DisplayPort and HDMI	X	1
AUD[0]	VSYNC		X	1



GPIO_13	GPIO_12	GPIO_11	Memory Aperture Size
0	0	1	512MB/256MB memory aperture (Default)
1	1	0	reserved

JTAG SIGNAL OPTION

Signal	Normal mode	Debug mode	pilot run mode
TESTEN	"1"(PU)	"1"(PU)	"0"(PD)
JTAG_TRST#	"0"(PD)	"1"(PU)	NC
JTAG_TCK	CLK	"1"(PU)	NC
JTAG_TMS	"1"(PU)	"1"(PU)	NC

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Title: GPU PCIE/STRAPPING(1/5)

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

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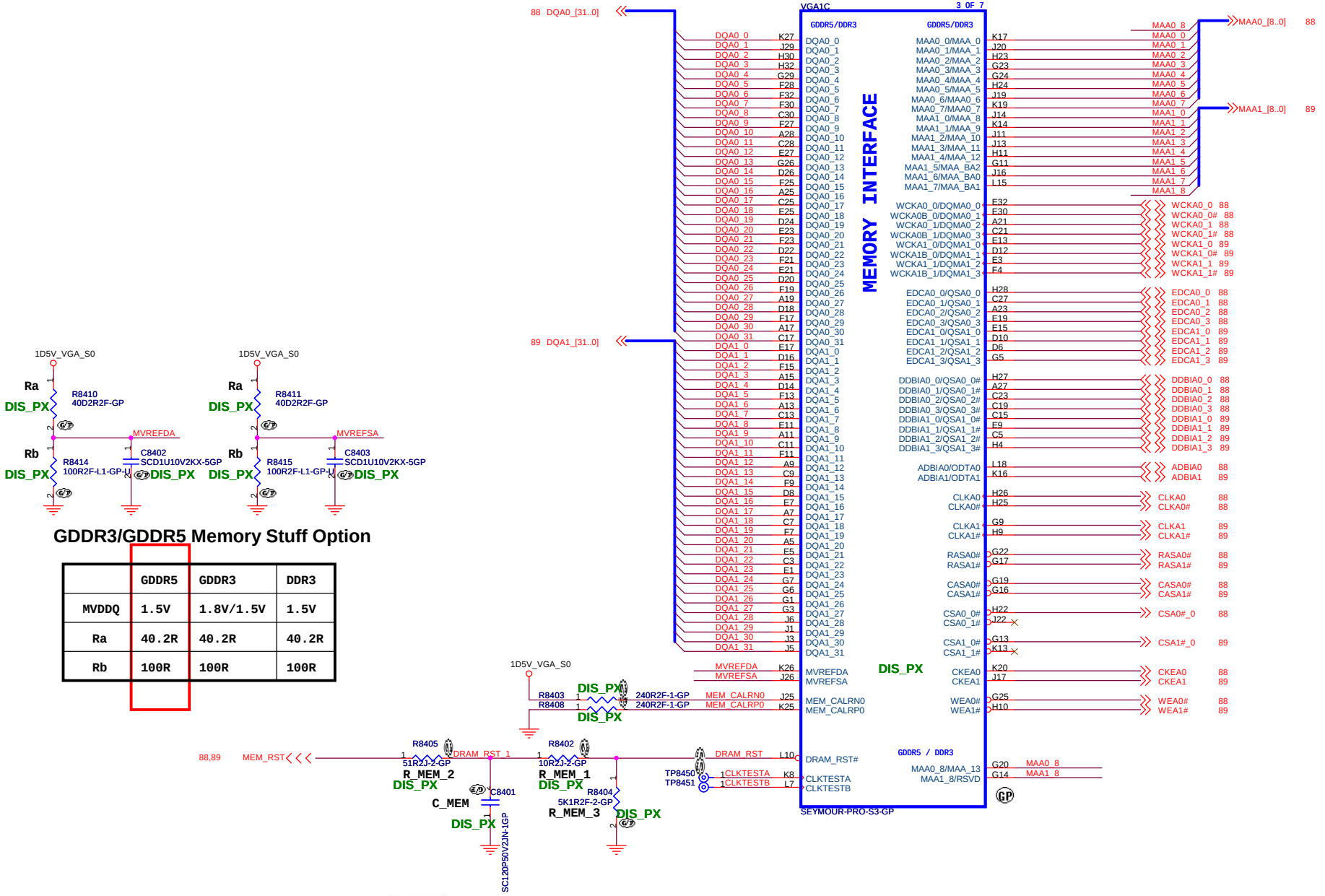
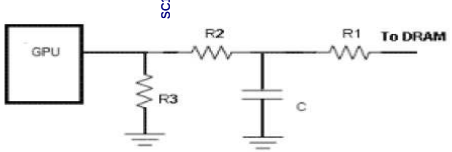


GDDR3/GDDR5 Memory Stuff Option

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R



C	R1	R2	R3
120 pF	51 Ω	10 Ω	5 kΩ

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Title: GPU Memory(2/5)

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

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VRAM ID TABLE

MEM ID3	MEM ID2	MEM ID1	MEM ID0	MEM ID VALUE	Vendor & PN	DIE Ver
NC	NC	0	0	0	Samsung(128X16) K4G20325FC-HC04	C
NC	NC	1	0	2	Samsung(128X16) K4G20325FD-FC04	D
NC	NC	0	1	1	Hynix(128MX16) H5GQ2H24MFR-T2C	M
NC	NC	1	1	3	Hynix(128MX16) H5GQ2H24AFR-T2C	A
NC	NC	0	0	0	Elpida(128MX16) EDW2032BBBG-50-F	B
NC	NC	NC	NC	NC	UMA	

Reserve Pul-High Resistor for MEM_ID2/MEM_ID3

0= Old Die
1= New Die

VBIOS 1 : Samsung
VBIOS 2 : Hynix
VBIOS 3 : Elpida

GPU Power ID Table

GPU SIDE		UP1527QQDD
GPIO_15_PWRCNTL_0	GPIO_20_PWRCNTL_1	VGA_CORE
0	0	1V
1	0	0.9V

LVDS Interface

VGA1F 6 OF 7

LVDS CONTROL: VARY_BL, DIGON

LVTMDP: TXCLK_UP_DPF3P/N, TXOUT_U0P_DPF2P/N, TXOUT_U1P_DPF1P/N, TXOUT_U2P_DPF0P/N, TXOUT_U3P/N, TXCLK_LP_DPE3P/N, TXOUT_L0P_DPE2P/N, TXOUT_L1P_DPE1P/N, TXOUT_L2P_DPE0P/N, TXOUT_L3P/N

SEYMOUR-PRO-S3-GP

CTF setpoint is 118°C, and is programmed during ASIC initialization.

Intel is H_THERMTRIP#

SSEL1 (Pin 3)	SSEL0 (Pin 7)	Spread Percent (%) SSCLK (Pin 5)
Low (VSS)	Low (VSS)	Spread Off (No Spread)
Low (VSS)	Middle (Floating)	-0.50%
Low (VSS)	High (VDD)	-2.5%
Middle (Floating)	Low (VSS)	-0.25%
Middle (Floating)	Middle (Floating)	-0.75%
Middle (Floating)	High (VDD)	-1.0%
High (VDD)	Low (VSS)	-1.5%
High (VDD)	Middle (Floating)	-2.0%
High (VDD)	High (VDD)	-3.0%

Recommended Clock-Input Configurations

Memory Type	Description
DDR3	27-MHz (± 30 ppm) crystal connected to XTALIN/XTALOUT, or 27-MHz (1.8 V) oscillator connected to XTALIN.
GDDR5	27-MHz (3.3 V) oscillator connected to XO_IN, and 100-MHz (3.3 V) oscillator connected to XO_IN2. (By default, this clock should not be spread since internal spreading is used.)

CAD NOTE: EC5803,EC8504 Close VGA1

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Title: GPU_DP/LVDS/CRT/GPIO(3/5)

Size: A2 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

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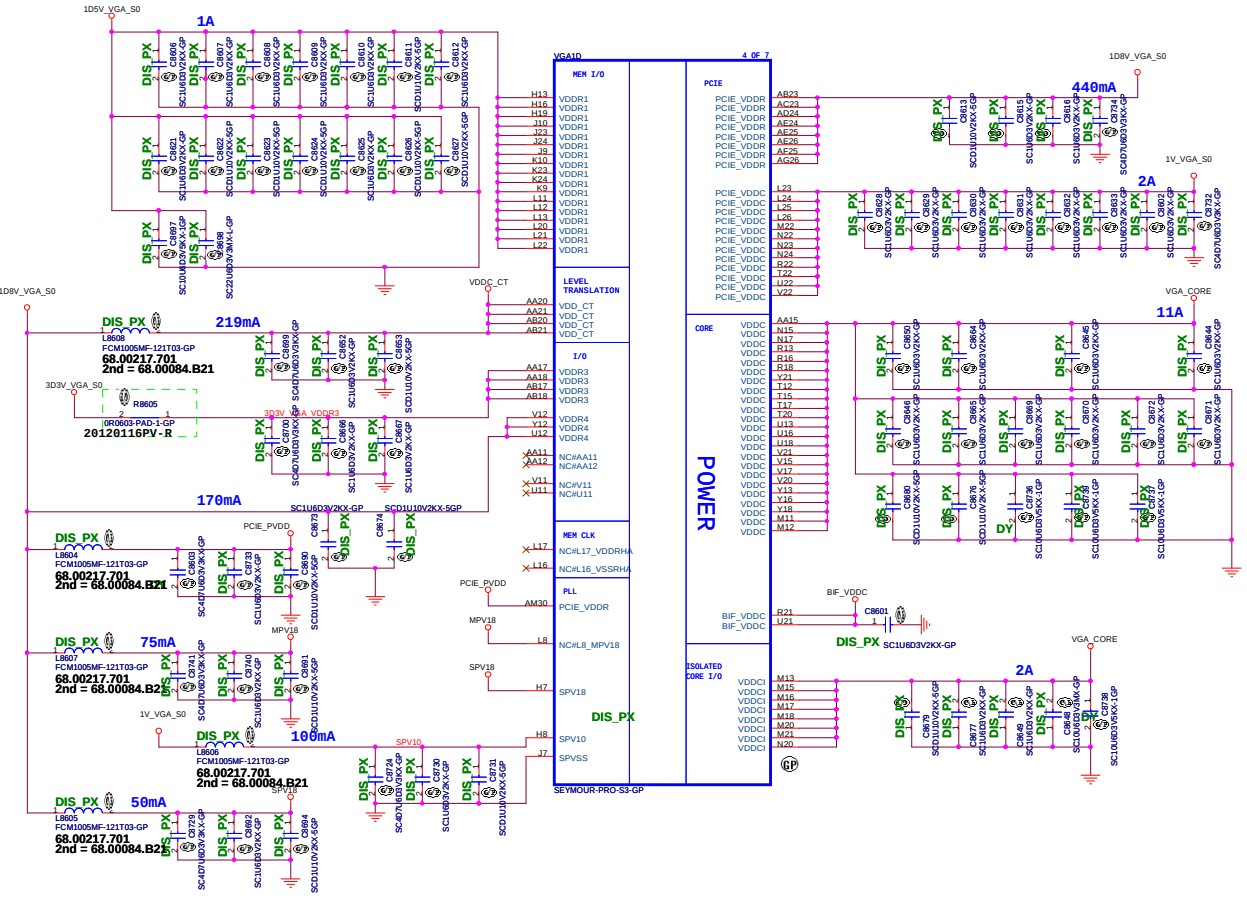

	PX_EN	8209A_EN/DEM_VGA	PX_MODE	PX_EN#	PX_EN##	BIF_VDDC
Non-BACO	0	1	1	0	1	VGA_Core
BACO	1	0	0	1	0	1V_VGA

PX_EN# = High, BIF_VDDC = 1V_VGA_S0
PX_EN## = High, BIF_VDDC = VGA_CORE

PX_EN	Mode	BIF_VDDC
0	Normal	VGA_Core
1	BACO	1V_VGA

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Title: GPU_POWER(4/5)

Size: A2 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

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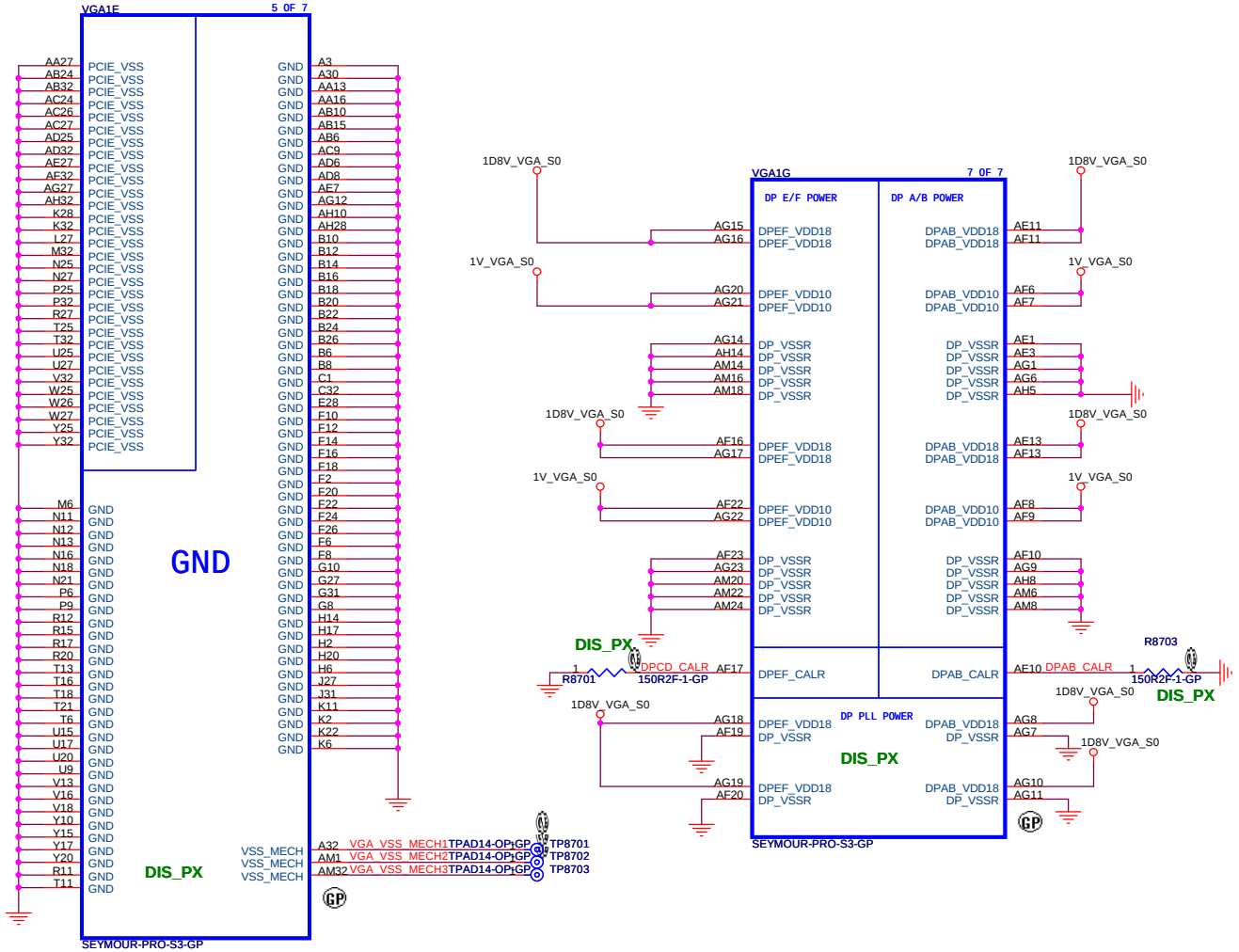

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Title: GPU_DPPWR/GND(5/5)

Size	Document Number	Rev
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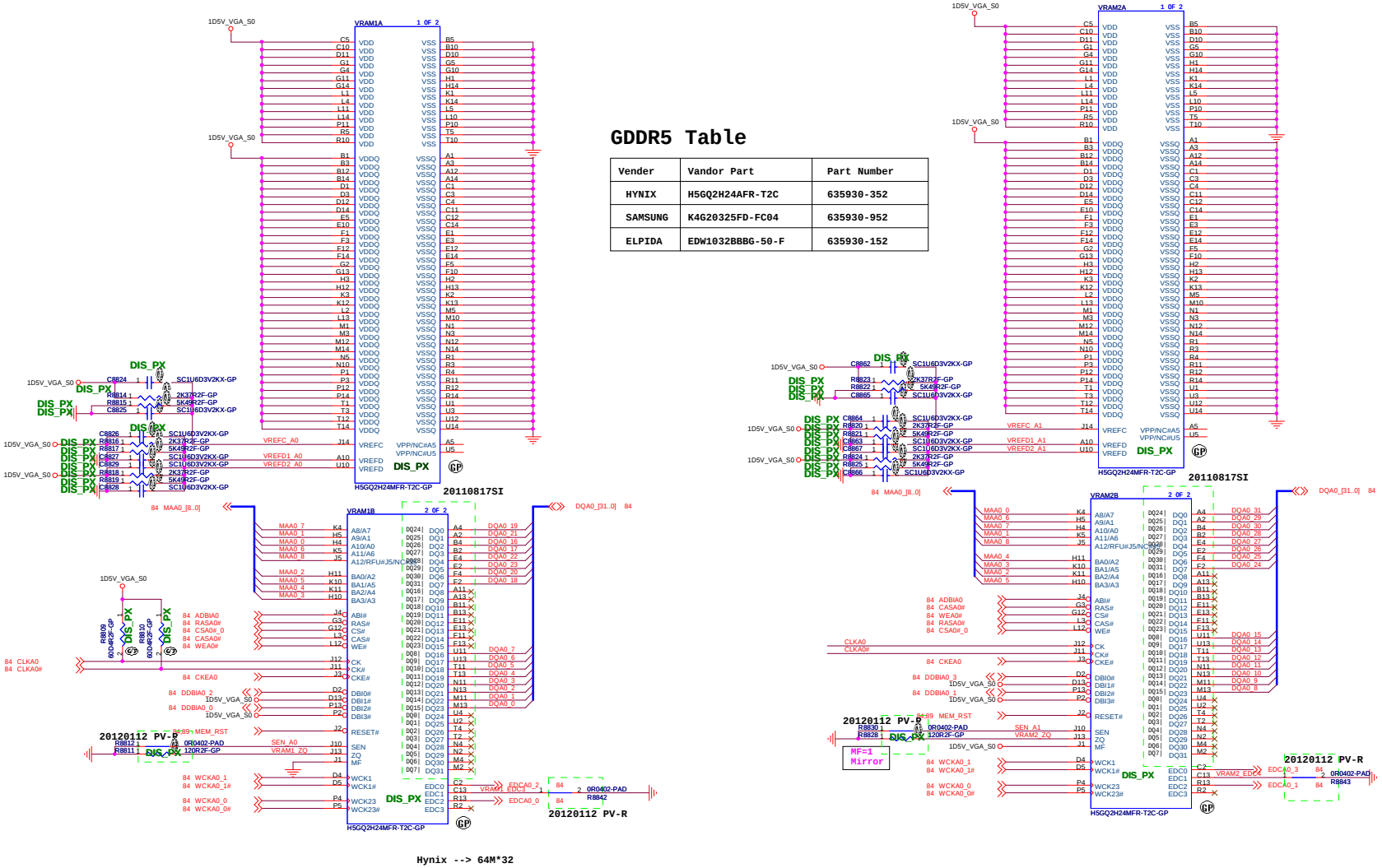
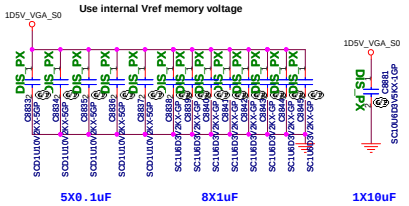
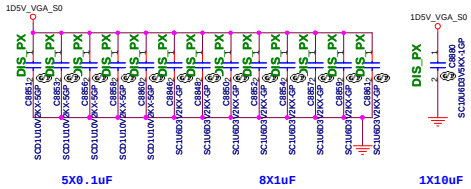
GDDR5 Table

Vender	Vandor Part	Part Number
HYNIX	H5GQ2H24AFR-T2C	635930-352
SAMSUNG	K4G20325FD-FC04	635930-952
ELPIDA	EDW1032BBBG-50-F	635930-152







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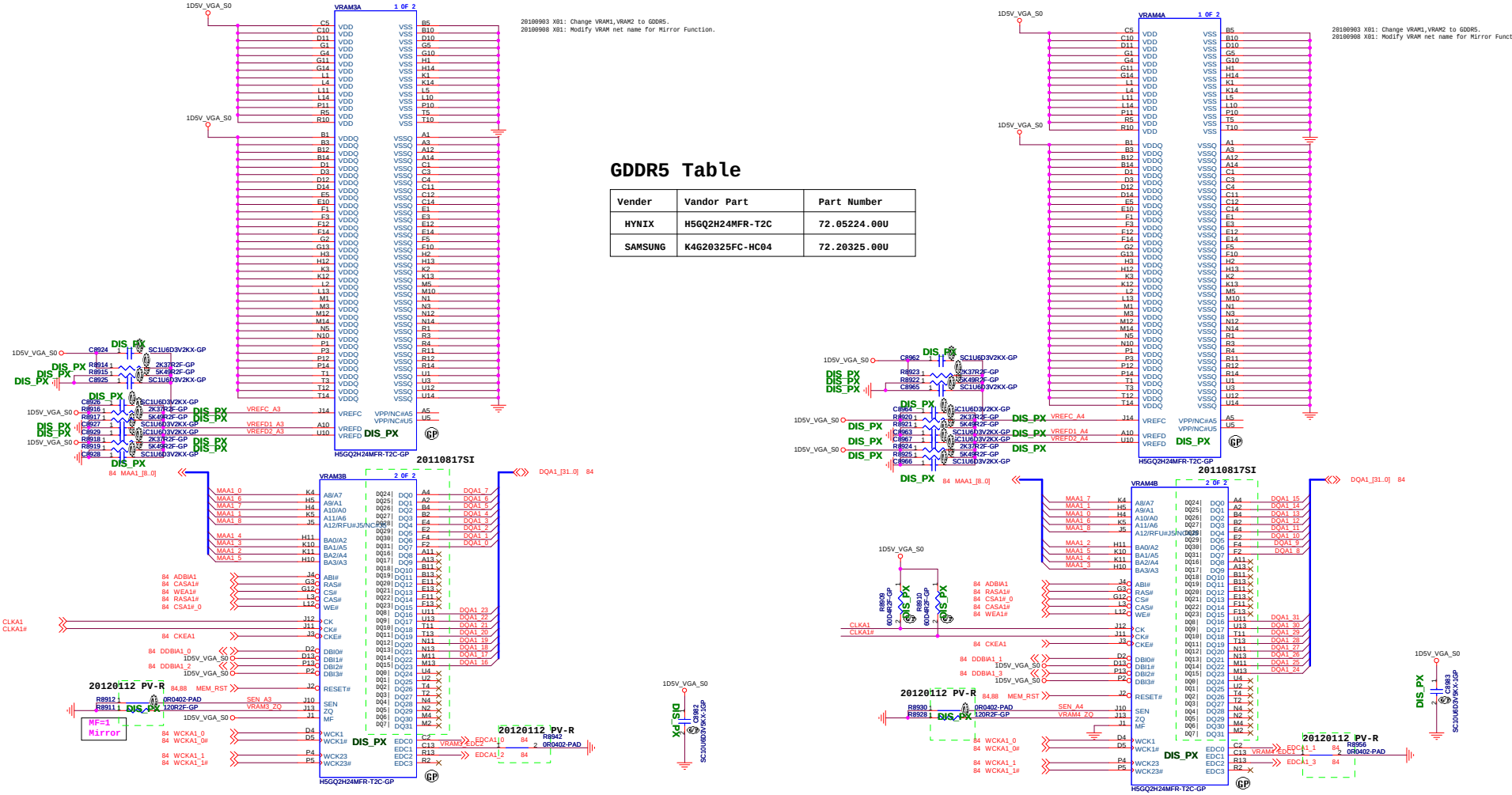
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM1,2 (1/4)

Size: A2 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

Date: Wednesday, March 14, 2012 | Sheet 88 of 103



GDDR5 Table

Vender	Vandor Part	Part Number
HYNIX	H5GQ2H24MFR-T2C	72.05224.00U
SAMSUNG	K4G20325FC-HC04	72.20325.00U

<Core Design>

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Title: GPU-VRAM3,4 (2/4)

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A2	2012 S-Series Richie 13.3	-1

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Title: *(Reserved) GPU-VRAM5,6 (3/4)*

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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Title: ***(Reserved) GPU-VRAM7,8 (4/4)***

Size	Document Number	Rev
A3	**2012 S-Series Richie 13.3**	-1

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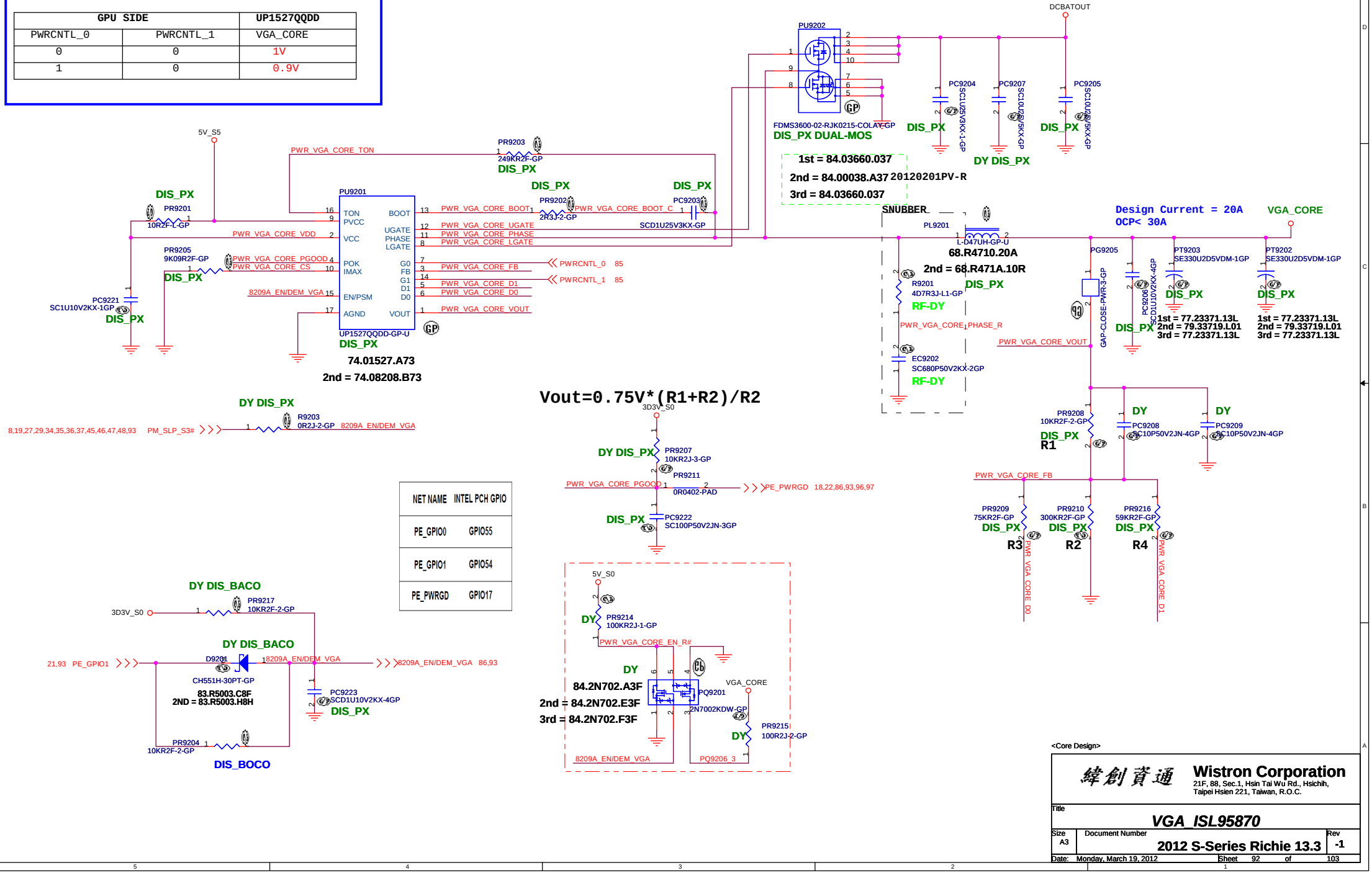
+VGA_CORE

GPU Power ID Table

Thames Pro S3 GDDR5

GPU SIDE		UP1527QQDD
PWRCNTL_0	PWRCNTL_1	VGA_CORE
0	0	1V
1	0	0.9V



<Core Design>

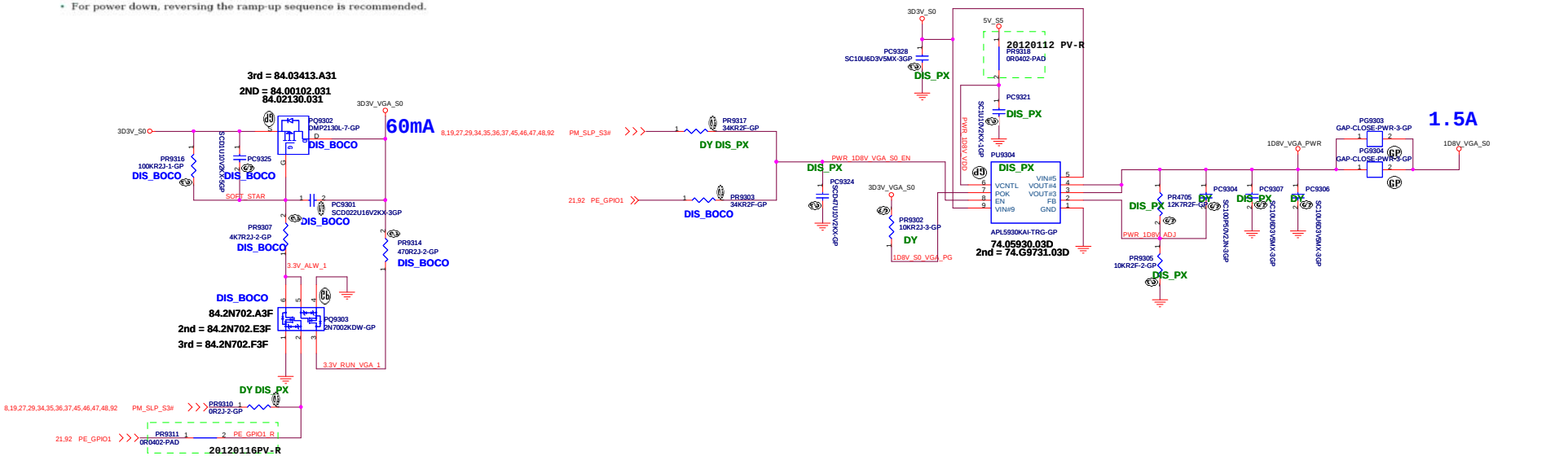
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: VGA_ISL95870		
Size: A3	Document Number: 2012 S-Series Richie 13.3	Rev: -1
Date: Monday, March 19, 2012	Sheet 92 of 103	

5.3 Power-Up/Down Sequence

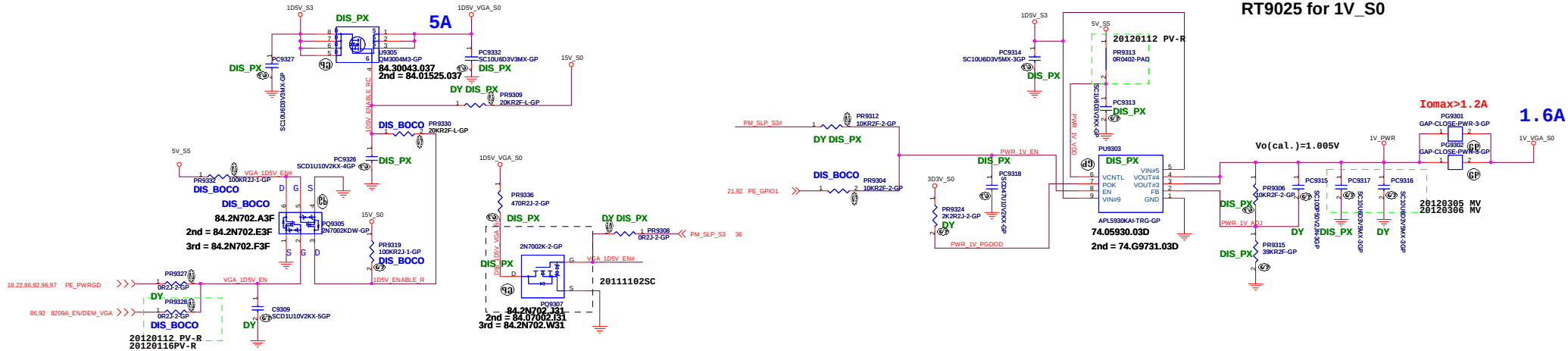
Seymour has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies, except for **VDDR3**, must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. There is no timing requirement on the ramp up of **VDDR3** relative to other power rails.
- The external pull-up resistors on the **DDC/AUX** signals (if applicable) should ramp up before or after both **VDDC** and **VDD_CT** have ramped up.
- **VDDC** and **VDD_CT** should not ramp up simultaneously. For exmaple, **VDDC** should reach 90% before **VDD_CT** starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.

3D3V_VGA_S0 > VGA_CORE > 1V_VGA_S0 > 1D5V_VGA_S0 > 1D8V_VGA_S0



1D5V_VGA_S0



<Variant Name>

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Title: ***DISCRETE VGA POWER***

Size	Document Number	Rev
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Title: ***Reserved***

Size	Document Number	Rev
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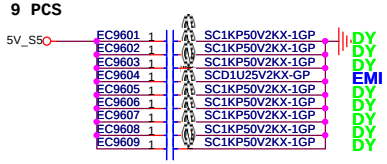
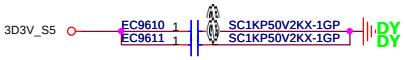
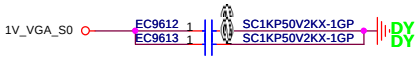
5V_S5 9 PCS



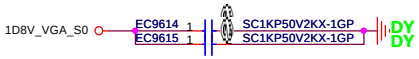
1D8V_PWR 2 PCS



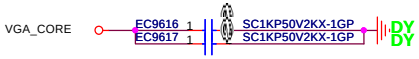
1V_VGA_S0 2 PCS



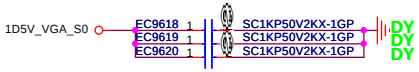
1D8V_VGA_S0 2 PCS



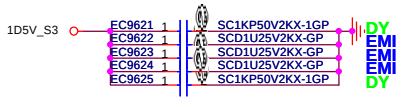
VGA_CORE 2 PCS



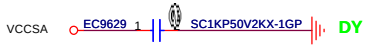
1D5V_VGA_S0 2 PCS



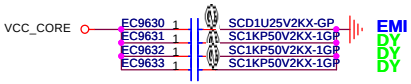
1D5V_S3 8 PCS



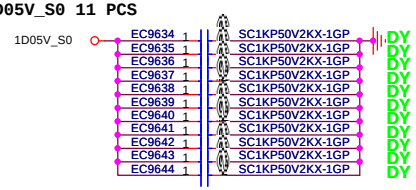
VCCSA 1 PCS



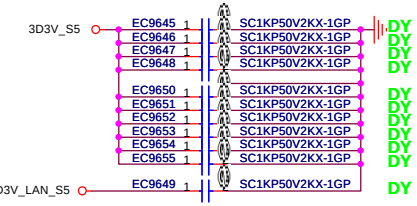
VCC_CORE 4 PCS



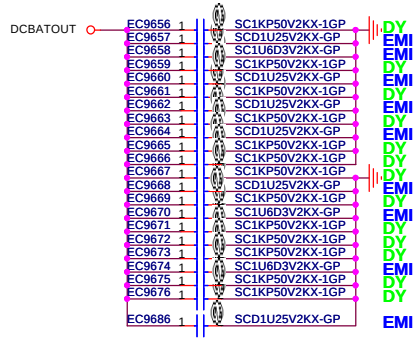
1D05V_S0 11 PCS

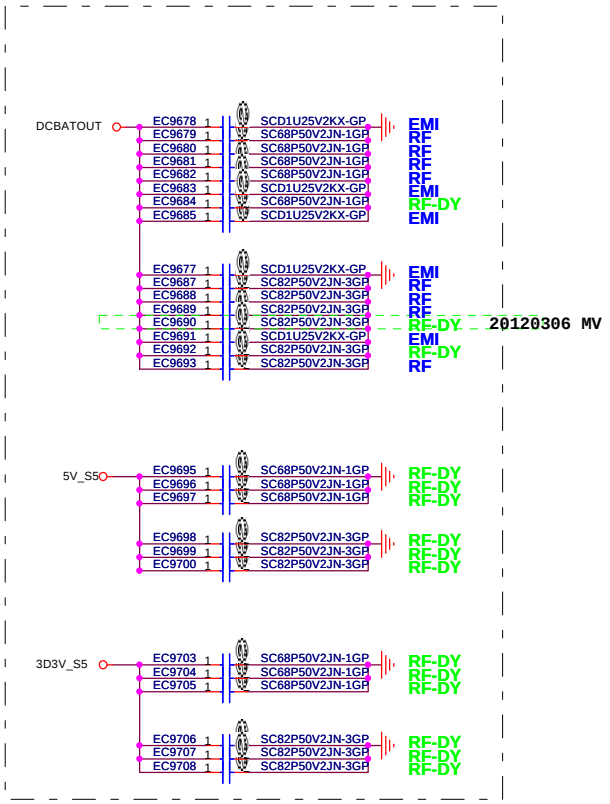


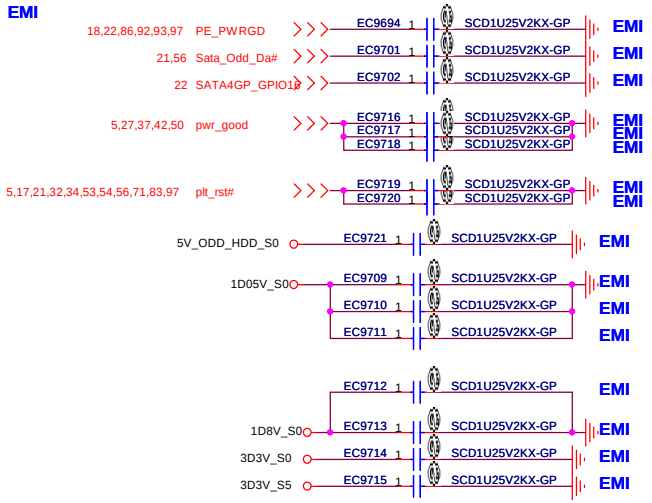
3D3V_S5 11 PCS



DCBATOUT 21 PCS







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PAGE 14_DIMM1 EMI CAP

5,14,15 DDR3_DRAMRST# — EC1428 — SC1KP50V2KX-1GP — DY

PAGE 15_DIMM1 EMI CAP

5,14,15 DDR3_DRAMRST# — EC1524 — SC1KP50V2KX-1GP — DY

PAGE 17_PCH(1/9)

17,29 HDA_BITCLK_CODEC — EC1701 — SC22P50V2JN-4GP — DY
17,29 HDA_SDOUT_CODEC — EC1702 — SC22P50V2JN-4GP — DY

PAGE 27_KBC

22,27 KBrst# — EC2701 — SC1KP50V2KX-1GP — DY
19,27 Pm_Pwrok — EC2702 — SC1KP50V2KX-1GP — DY
19,27,41 Rsmrst# — EC2703 — SC1KP50V2KX-1GP — DY

PAGE 29_AUDIO CODEC EMI CAP

17,29 HDA_RST#_CODEC — EC2901 — SC1KP50V2KX-1GP — DY

PAGE 31_AUDIO CONNECTOR EMI CAP

30,31 MIC_IN_R — EC3111 — SC100P50V2JN-L-GP — DY
30,31 MIC_IN_L — EC3112 — SC100P50V2JN-L-GP — DY
29,31 HP_OUT_L — EC3113 — SC100P50V2JN-L-GP — DY
29,31 HP_OUT_R — EC3114 — SC100P50V2JN-L-GP — DY — AUD_AGND

20120130PV-R

AVDD_CODEC — EC3115 — SC1U6D3V2KX-GP — AUD_AGND — DY
5V_S0 — EC3107 — SCD1U16V2ZY-2GP — DY

DY — EC3108 — SC1KP50V2KX-1GP — AUD_AGND
DY — EC3109 — SC1KP50V2KX-1GP
DY — EC3110 — SC1KP50V2KX-1GP

PAGE 32_Card Reader EMI CAP

32,33 MDIF5 — EC3201 — SC22P50V2JN-4GP — DY

CLOSE U3201 PIN1

5,17,21,32,34,53,54,56,71,83,96 PLT_RST# — EC3212 — SC100P50V2JN-L-GP — DY

PAGE 33_SD/MS/MMC CONNECTOR EMI CAP

CLOSE CARD1

22,32 D3E_WAKE — EC3307 — SC1KP50V2KX-1GP — DY
32,33 MS_INS# — EC3308 — SC1KP50V2KX-1GP — DY
32,33 MDIF2 — EC3306 — SC22P50V2JN-4GP — DY
32,33 MDIF1 — EC3305 — SC22P50V2JN-4GP — DY
32,33 MDIF0 — EC3304 — SC22P50V2JN-4GP — DY
32,33 MDIF3 — EC3303 — SC22P50V2JN-4GP — DY

PAGE 34_Lan RTL8111E EMI CAP

CLOSE U3401 Pin25

5,17,21,32,34,53,54,56,71,83,96 PLT_RST# — EC3401 — SCD1U25V2KX-GP — EMI

PAGE 35_LAN RJ45 EMI CAP

34,35 GREEN_LED# — EC3502 — SCD1U16V2ZY-2GP — DY
34,35 YELLOW_LED# — EC3501 — SCD1U16V2ZY-2GP — DY

PAGE 39_BATT CONN EMI CAP

27,39 AB1A_DATA — EC3901 — SC22P50V2JN-4GP — DY
27,39 AB1A_CLK — EC3902 — SC22P50V2JN-4GP — DY
27,39 MAIN_BAT_DET# — EC3903 — SC1KP50V2KX-1GP — DY
39 MAIN_BAT_DET#_C — EC3904 — SC1KP50V2KX-1GP — DY

PAGE 49_LVDS EMI CAP

20,49 LCDVDD_EN — EC4911 — SC1KP50V2KX-1GP — DY
49 DISP_OFF# — EC4912 — SC1KP50V2KX-1GP — DY
27,49,82 LID_SW# — EC4913 — SC1KP50V2KX-1GP — DY
20,49 LCD_BL_EN — EC4914 — SC1KP50V2KX-1GP — DY
29,49 DMIC_DATA — EC4904 — SC33P50V2JN-3GP — DY
29,49 DMIC_CLK — EC4905 — SC33P50V2JN-3GP — DY

PUT CLOSE R4911

DCBATOUT — EC4915 — SCD1U50V3KX-GP — DY
+LCDVDD — EC4916 — SCD1U16V2ZY-2GP — DY
3D3V_S0 — EC4903 — SC1U6D3V2KX-GP — DY
EC4902 — SC1U6D3V2KX-GP — DY
EC4901 — SC1U6D3V2KX-GP — DY

PAGE 50_CRT EMI CAP

5V_S0 — EC5011 — SCD1U50V3KX-GP — DY

PAGE 51_HDMI EMI CAP

20,51 HDMI_PCH_DET — EC5101 — SC1KP50V2KX-1GP — DY

PAGE 53_WLAN SLOT EMI CAP

5,17,21,32,34,53,54,56,71,83,96 PLT_RST# — EC5303 — SC100P50V2JN-L-GP — DY
53 XMIT_OFF_R — EC5301 — SC1KP50V2KX-1GP — DY
22,53 BT_OFF# — EC5302 — SC1KP50V2KX-1GP — DY

PAGE 54_WLAN SLOT EMI CAP

CLOSE WWAN1

22,54 GPS_XMIT_OFF# — EC5401 — SC1KP50V2KX-1GP — DY
17,54 INTRUDER# — EC5402 — SC1KP50V2KX-1GP — DY
54 WIFI_RF_EN# — EC5403 — SC1KP50V2KX-1GP — DY
5,17,21,32,34,53,54,56,71,83,96 PLT_RST# — EC5404 — SC100P50V2JN-L-GP — DY

PAGE 56_HDD/ODD EMI CAP

5V_S0 — EC5601 — SC1U10V3ZY-6GP — DY
22,56 SATA_ODD_PWR_EN — EC5615 — SC1KP50V2KX-1GP — DY
56 SATA_ODD_DET#_C — EC5613 — SC1KP50V2KX-1GP — DY
56 SATA_ODD_DA#_C — EC5614 — SC1KP50V2KX-1GP — DY

PAGE 61_USB2.0 EMI CAP

CLOSE USB21

USB_VCCA — EC6102 — SCD1U16V2ZY-2GP — DY

PAGE 62_USB3.0 EMI CAP

USB_VCCA — EC6202 — SC1U10V3ZY-6GP — DY
USB_VCCB — EC6201 — SC1U10V3ZY-6GP — DY
EC6203 — SC1U10V3ZY-6GP — DY

PAGE 64_FINGER PRINT EMI CAP

22,64 FPR_LOCK# — EC6404 — SC1KP50V2KX-1GP — DY
18,64 FPR_OFF — EC6405 — SC1KP50V2KX-1GP — DY

PAGE 82_DCIN EMI CAP

38,82 LIMIT_SIGNAL — EC8206 — SC1KP50V2KX-1GP — EMI
82 DC_PIN1 — EC8209 — SC1U25V3KX-1-GP — EMI
82 DC_PIN2 — EC8210 — SC1U25V3KX-1-GP — EMI
27,82 QUICKX_LED# — EC8212 — SC1KP50V2KX-1GP — EMI
19,82 ON_OFF# — EC8213 — SC1KP50V2KX-1GP — EMI
27,49,82 LID_SW# — EC8214 — SC1KP50V2KX-1GP — EMI
68,82 WL_LED#_ALL — EC8215 — SCD1U16V2ZY-2GP — DY

AD+ — EC8202 — SC1U25V3KX-1-GP — DY
EC8201 — SC1U25V3KX-1-GP — EMI

CLOSE PWR1

27,69,82 KSI1 — EC8216 — SC1KP50V2KX-1GP — EMI
27,69,82 KSI3 — EC8217 — SC1KP50V2KX-1GP — EMI
27,82 KSO17 — EC8218 — SC1KP50V2KX-1GP — EMI

3D3V_S0 — EC8207 — SC1KP50V2KX-1GP — EMI
EC8211 — SCD1U25V2KX-GP — EMI
3D3V_AUX_S5 — EC8205 — SC1KP50V2KX-1GP — EMI
EC8208 — SCD1U25V2KX-GP — EMI

PAGE 40-48,92_POWER EMI CAP

CLOSE TO PU4005 — DCBATOUT — EC4001 — SCD1U25V2KX-GP — EMI
CLOSE TO PU4301 — DCBATOUT — EC4301 — SCD1U50V3KX-GP — DY
CLOSE TO PU4303 — DCBATOUT — EC4303 — SCD1U50V3KX-GP — DY
CLOSE TO PU4401 — DCBATOUT — EC4401 — SCD1U25V2KX-GP — EMI
CLOSE TO PU4501 — DCBATOUT — EC4501 — SCD1U50V3KX-GP — DY
CLOSE TO PU4601 — DCBATOUT — EC4601 — SCD1U50V3KX-GP — DY
CLOSE TO PU4701 — DCBATOUT — EC4701 — SCD1U25V2KX-GP — EMI
CLOSE TO PU4801 — DCBATOUT — EC4801 — SCD1U25V2KX-GP — EMI
CLOSE TO PU9202 — DCBATOUT — EC9201 — SCD1U50V3KX-GP — DY

PAGE 62_USB3.0 CAP

CLOSE USB31 — USB_VCCA — EC6215 — SCD1U16V2ZY-2GP — DY
CLOSE USB32 — USB_VCCB — EC6214 — SCD1U16V2ZY-2GP — DY
CLOSE USB33 — USB_VCCB — EC6213 — SCD1U16V2ZY-2GP — DY

19,46,62 PM_SLP_S4# — EC6212 — SC1KP50V2KX-1GP — DY

CLOSE U6205

19,46,62 PM_SLP_S4# — EC6211 — SC1KP50V2KX-1GP — DY

PAGE 69_KEYBOARD/TOUCH PAD EMI CAP

20120112 PV-R

SRC1KP50VM-GP EC6904 — KSI3 KSO5 KSO1 KSI0 — EMI
SRC1KP50VM-GP EC6903 — KSO2 KSO4 KSO7 KSO8 — EMI
SRC1KP50VM-GP EC6906 — KSO6 KSO3 KSO12 KSO13 — EMI
SRC1KP50VM-GP EC6905 — KSO14 KSO11 KSO10 KSO15 — EMI
SRC1KP50VM-GP EC6901 — KSI1 KSI7 KSI6 KSO9 — EMI
SRC1KP50VM-GP EC6902 — KSI4 KSI5 KSO0 KSI2 — EMI

KSI[0..7] 27,69,82
KSO[0..15] 27,69

27,69 KB_CAPS_LED — EC6907 — SC100P50V2JN-L-GP — DY

PAGE 82_DCIN EMI CAP

CLOSE PWR1

27,69,82 KSI1 — EC8216 — SC1KP50V2KX-1GP — EMI
27,69,82 KSI3 — EC8217 — SC1KP50V2KX-1GP — EMI
27,82 KSO17 — EC8218 — SC1KP50V2KX-1GP — EMI

3D3V_S0 — EC8207 — SC1KP50V2KX-1GP — EMI
EC8211 — SCD1U25V2KX-GP — EMI
3D3V_AUX_S5 — EC8205 — SC1KP50V2KX-1GP — EMI
EC8208 — SCD1U25V2KX-GP — EMI

EC2904/EC2903 CLOSE U2901

21,27 CLK_PCI_KBC — EC2101 — SC12P50V2JN-3GP — RF-DY
21,71 CLK_PCI_DEBUG — EC2102 — SC12P50V2JN-3GP — RF-DY

29 DMIC_CLK_R — EC2904 — SC220P50V2KX-3GP — EMI
29 DMIC_DATA_R — EC2903 — SC220P50V2KX-3GP — EMI

18,22,86,92,93,96 PE_PWRGD

EC9207 SC4750V2JN-3GP EMI
EC9208 SC4750V2JN-3GP EMI

WLAN & WWAN

H1 ~ H16 --> ZZ.00PAD.D11
H17 ~ H22 --> ZZ.00PAD.N11
H23 ~ H26 --> 34.4Y824.001
H27 ~ H28 --> 34.4Q602.101

WWAN WWAN PCH

H23 H24 H25 H26 H27 H28
STF256R169H05-GP STF256R169H05-GP STF256R169H05-GP STF256R169H05-GP STF256R169H03-GP STF256R169H03-GP
34.4KD36.001 34.4KD36.001 34.4KD36.001 34.4KD36.001

H19 H20 H11 H12
HOLE276R178-GP HOLE276R178-GP HOLE256R115-GP HOLE256R115-GP
ZZ.00PAD.N11 ZZ.00PAD.N11 ZZ.00PAD.D11 ZZ.00PAD.D11

H30 H31 H1 H2 H3 H4
HOLE276R178-GP HOLE256R115-GP HOLE256R115-GP HOLE256R115-GP HOLE256R115-GP HOLE256R115-GP
ZZ.00PAD.N11 ZZ.00PAD.D11 ZZ.00PAD.D11 ZZ.00PAD.D11 ZZ.00PAD.D11 ZZ.00PAD.D11

H29 H17 H15 H16 H5 H8
HOLE256R115-GP HOLE276R178-GP HOLE276R178-GP HOLE276R178-GP HOLE256R115-GP HOLE256R115-GP
ZZ.00PAD.D11 ZZ.00PAD.N11 ZZ.00PAD.N11 ZZ.00PAD.N11 ZZ.00PAD.D11 ZZ.00PAD.D11

Put Caps near DIMMA1

1D5V_S3 — EC1425 EC1424 — SC68P50V2JN-1GP — RF-DY

Put Caps near DIMMA2

1D5V_S3 — EC1525 EC1526 — SC68P50V2JN-1GP — RF-DY

3D3V_LAN_S5 — EC3403 EC3405 EC3402 — SCD1U10V2KX-5GP SC82P50V2JN-3GP SC56P50V2JN-2GP — RF-DY

34 LANXIN — EC3404 — SC56P50V2JN-2GP — RF-DY

DCBATOUT — EC4003 EC4002 EC4004 EC4005 — SC68P50V2JN-1GP SC82P50V2JN-3GP SC2200P50V2KX-2GP SCD1U50V3KX-GP — RF-DY

DCBATOUT_3V — EC4101 EC4102 EC4103 EC4104 — SC68P50V2JN-1GP SC82P50V2JN-3GP SC2200P50V2KX-2GP SCD1U25V2KX-GP — RF-DY EMI

DCBATOUT_5V — EC4107 EC4108 EC4109 EC4110 — SCD1U25V2KX-GP SC82P50V2JN-3GP SC2200P50V2KX-2GP SCD1U50V3KX-GP — EMI RF-DY

PWR_VCCCORE1_DCBATOUT — EC4304 EC4305 EC4306 EC4307 — SC68P50V2JN-1GP SCD1U25V2KX-GP SC2200P50V2KX-2GP SCD1U50V3KX-GP — RF-DY EMI RF-DY

PWR_VCCCORE2_DCBATOUT — EC4312 EC4308 EC4309 EC4310 — SC68P50V2JN-1GP SCD1U25V2KX-GP SC2200P50V2KX-2GP SCD1U50V3KX-GP — RF-DY EMI RF-DY

PWR_GFXCORE1_DCBATOUT — EC4403 EC4404 EC4405 EC4406 — SC68P50V2JN-1GP SCD1U25V2KX-GP SC2200P50V2KX-2GP SCD1U50V3KX-GP — RF-DY EMI RF-DY

DCBATOUT_RT8209B_VCCP — EC4503 EC4504 EC4505 EC4506 — SC68P50V2JN-1GP SC82P50V2JN-3GP SC2200P50V2KX-2GP SCD1U25V2KX-GP — RE RE RF RF

DCBATOUT_1D5V — EC4603 EC4604 EC4605 EC4606 — SC68P50V2JN-1GP SC82P50V2JN-3GP SCD1U25V2KX-GP SCD1U25V2KX-GP — RF-DY RF-DY EMI EMI

+LCDVDD — EC4909 EC4908 — SC68P50V2JN-1GP SC1KP50V2KX-1GP — RF-DY RF-DY

3D3V_WLAN — EC5304 EC5305 EC5306 EC5307 — SC68P50V2JN-1GP SC82P50V2JN-3GP SC2200P50V2KX-2GP SCD1U50V3KX-GP — RF-DY RF-DY RF-DY RF-DY

1D5V_S0 — EC5309 EC5310 EC5311 EC5308 — SC68P50V2JN-1GP SC82P50V2JN-3GP SC2200P50V2KX-2GP SCD1U50V3KX-GP — RF-DY RF-DY RF-DY RF-DY

3D3V_WWAN — EC5405 EC5406 EC5407 EC5408 — SC68P50V2JN-1GP SC82P50V2JN-3GP SC2200P50V2KX-2GP SCD1U50V3KX-GP — RF-DY RF-DY RF-DY RF-DY

DCBATOUT — EC9203 EC9204 EC9205 EC9206 — SC68P50V2JN-1GP SCD1U25V2KX-GP SC2200P50V2KX-2GP SCD1U50V3KX-GP — RF-DY EMI RF-DY RF-DY

40 DC_IN_R AD+_IN_G — EC4007 EC4008 — SC1U25V3KX-1-GP SC1U25V3KX-1-GP — EMI EMI

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Title: UNUSED PARTS/EMI Capacitors
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Title

Change History

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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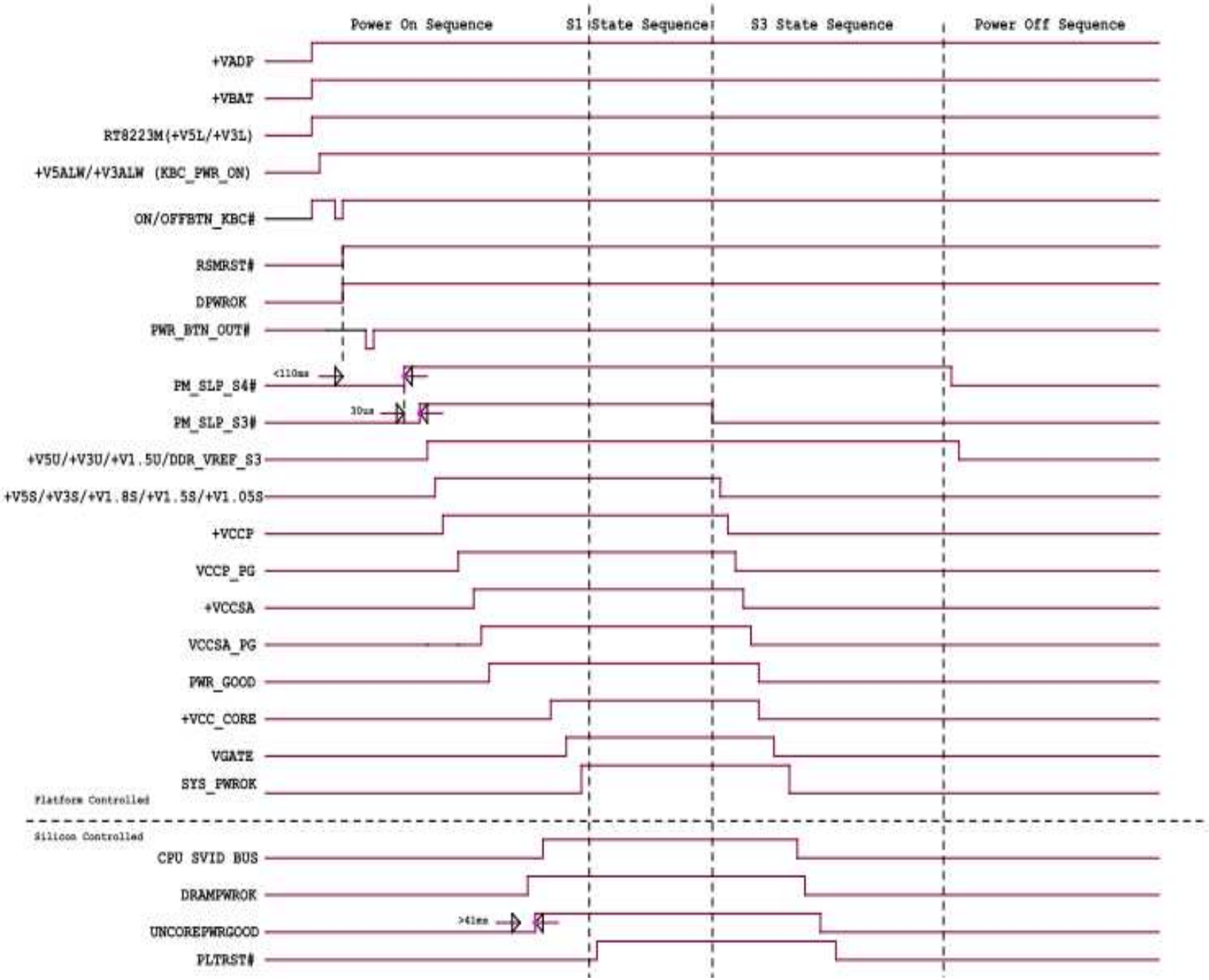
S-Series Power Sequence and Reset Signal Timing



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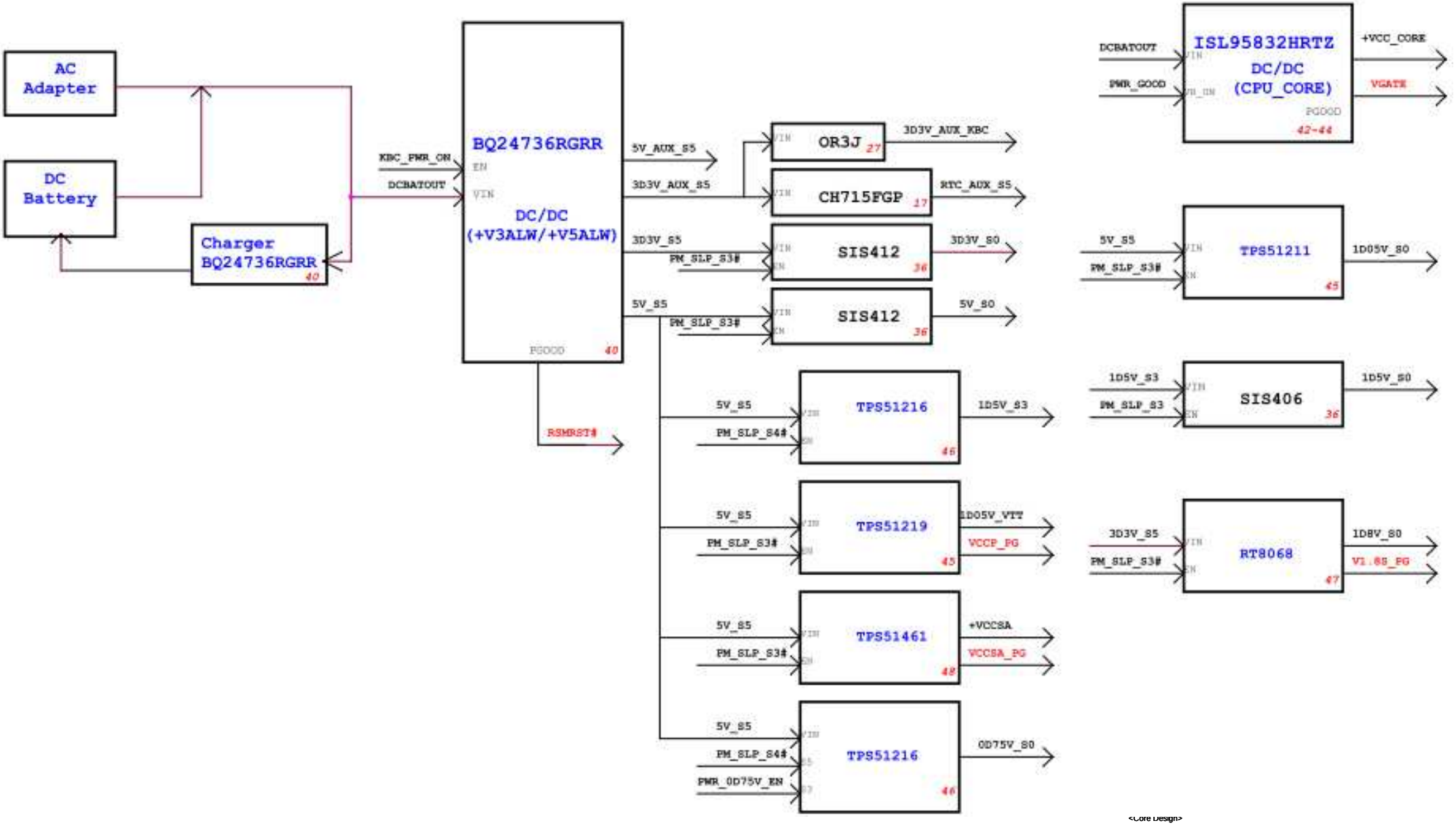
S-Series POWER BLOCK DIAGRAM



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Title: *Power Block Diagram*		
Size: A3	Document Number: 2012 S-Series Richie 13.3	Rev: -1
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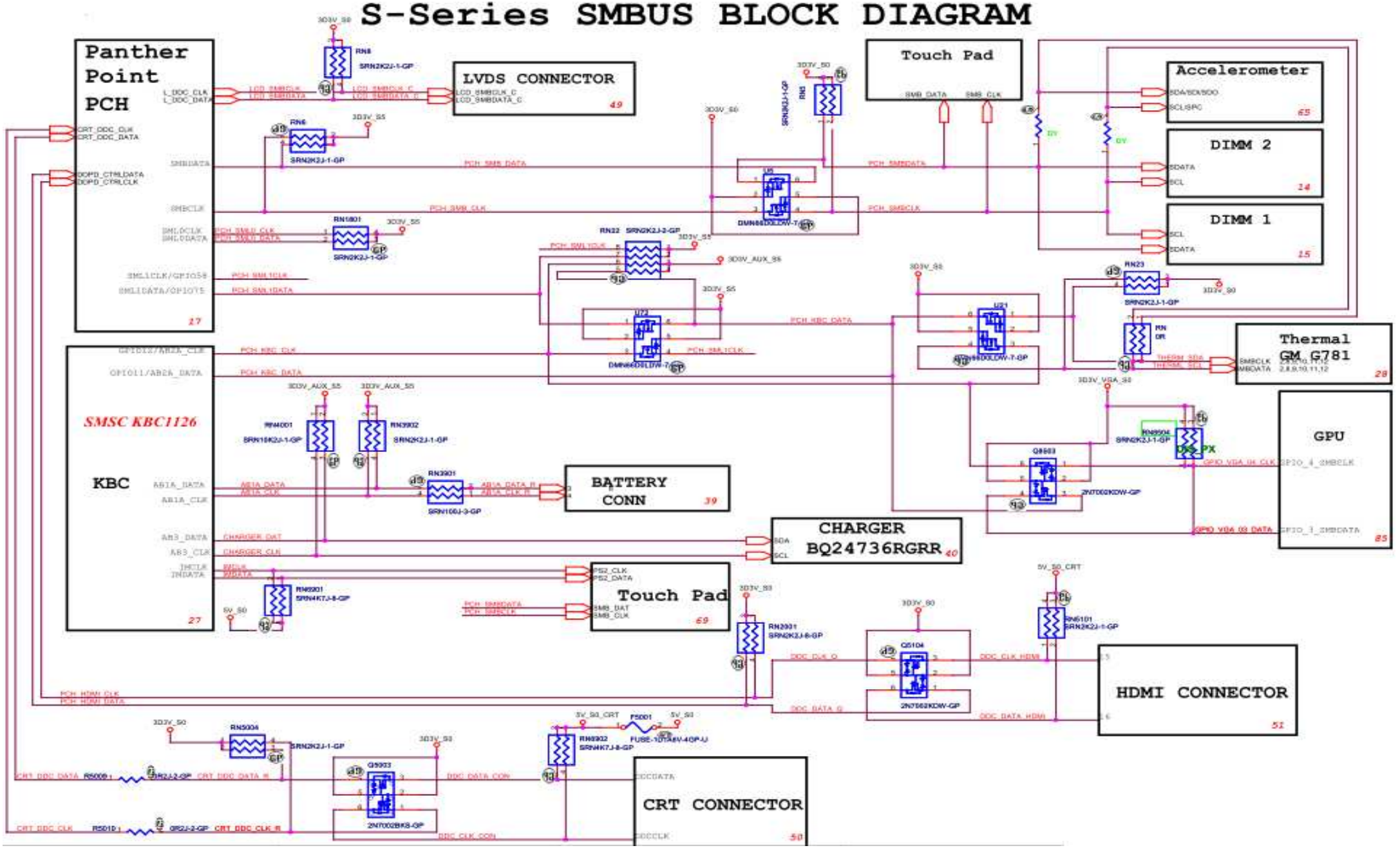
S-Series SMBUS BLOCK DIAGRAM



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Title	***SMBUS Block Diagram***	
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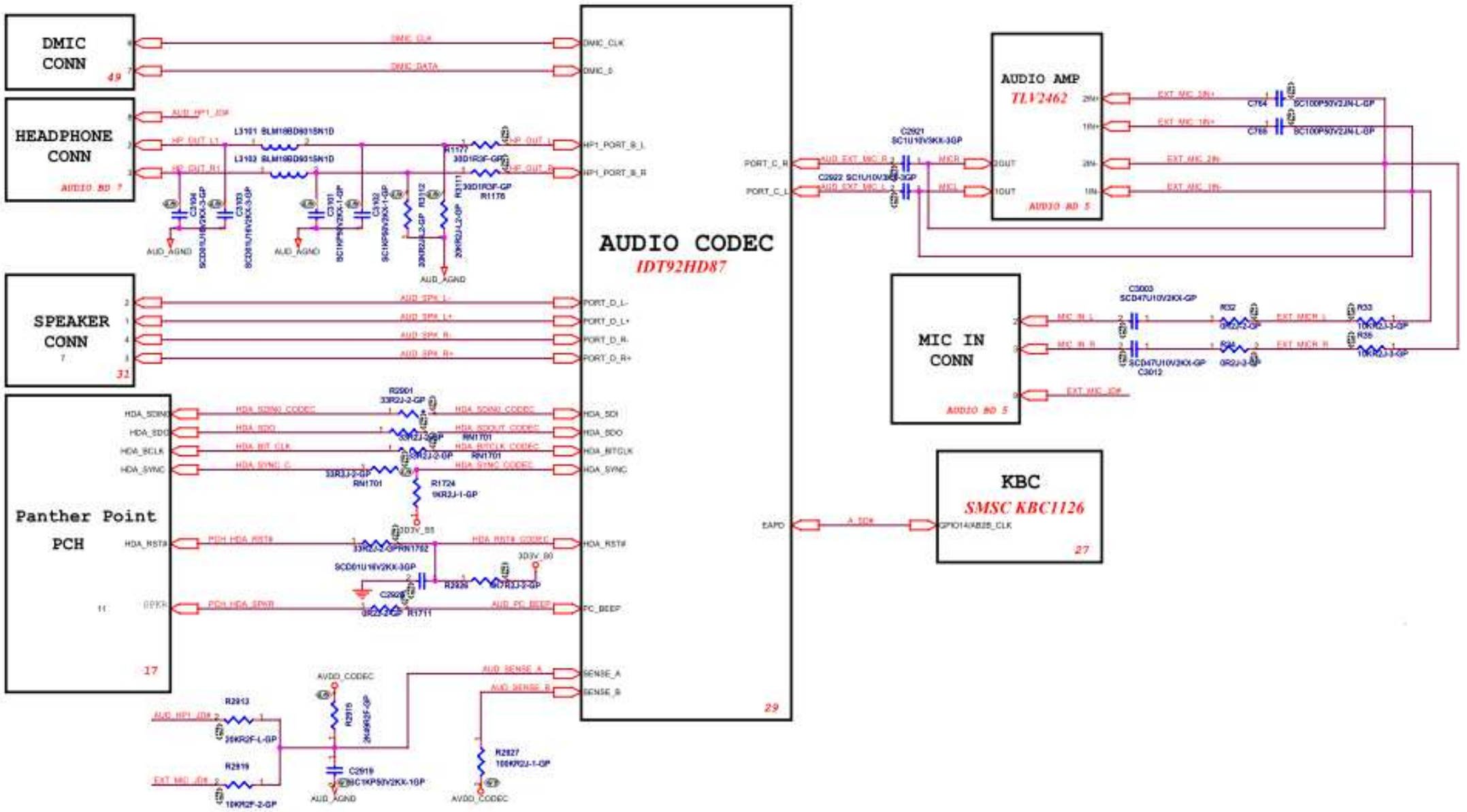
S-Series AUDIO BLOCK DIAGRAM



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