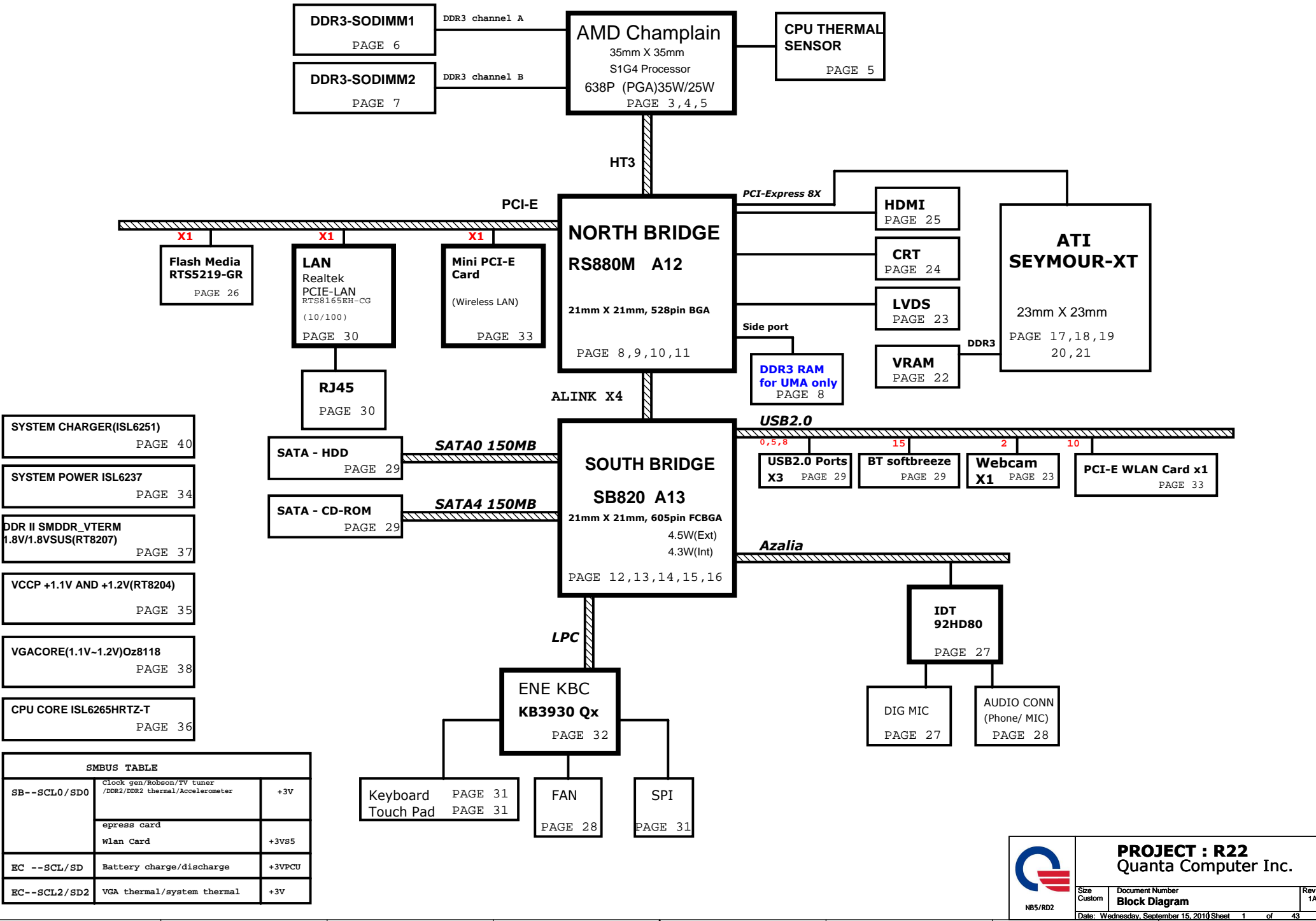


R22 SYSTEM DIAGRAM



01




- SYSTEM CHARGER(ISL6251) PAGE 40
- SYSTEM POWER ISL6237 PAGE 34
- DDR II SMD DR_VTERM 1.8V/1.8VSUS(RT8207) PAGE 37
- VCCP +1.1V AND +1.2V(RT8204) PAGE 35
- VGACORE(1.1V~1.2V)Oz8118 PAGE 38
- CPU CORE ISL6265HRTZ-T PAGE 36

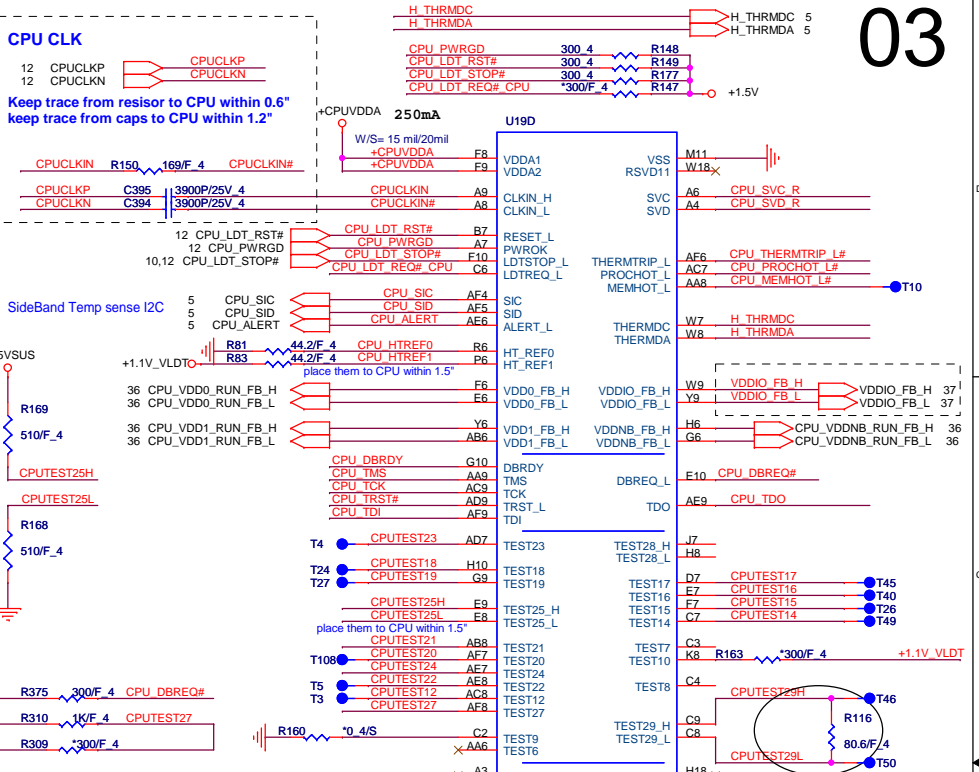
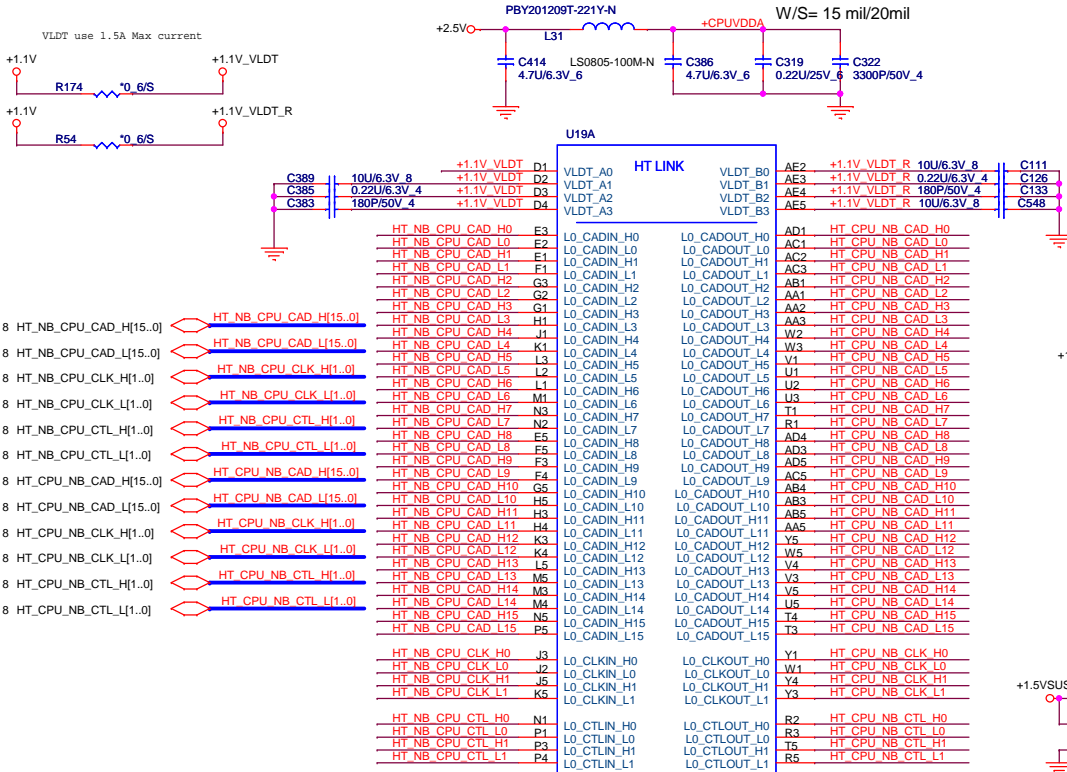
SMBUS TABLE		
SB--SCL0/SD0	Clock gen/Robson/TV tuner /DDR2/DDR2 thermal/Accelerometer	+3V
	epress card	
	wlan Card	+3VS5
EC --SCL/SD	Battery charge/discharge	+3VPCU
EC--SCL2/SD2	VGA thermal/system thermal	+3V

PROJECT : R22
Quanta Computer Inc.

Size Custom	Document Number Block Diagram	Rev 1A
Date: Wednesday, September 15, 2010 Sheet 1 of 43		

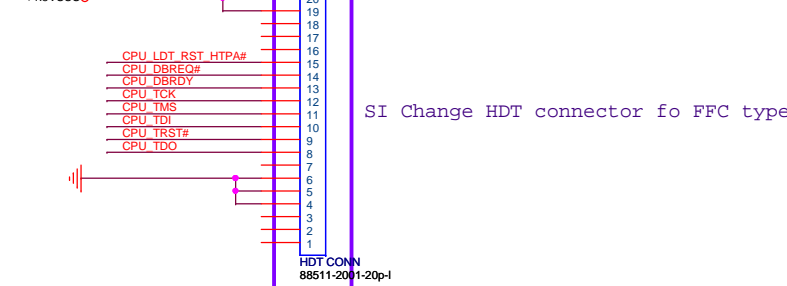
Use internal CLK GEN

 NB5/RD2	PROJECT : R22 Quanta Computer Inc.	
	Size Custom	Document Number Clock Generator
Date: Wednesday, September 15, 2014 Sheet 2 of 43		

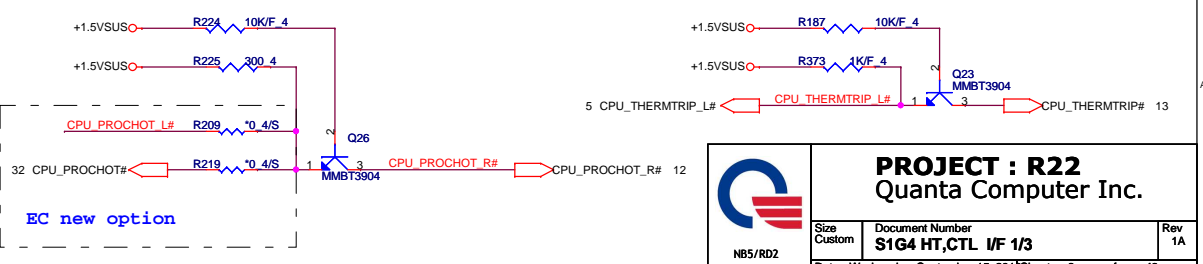
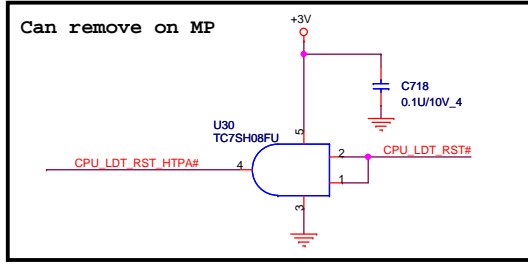
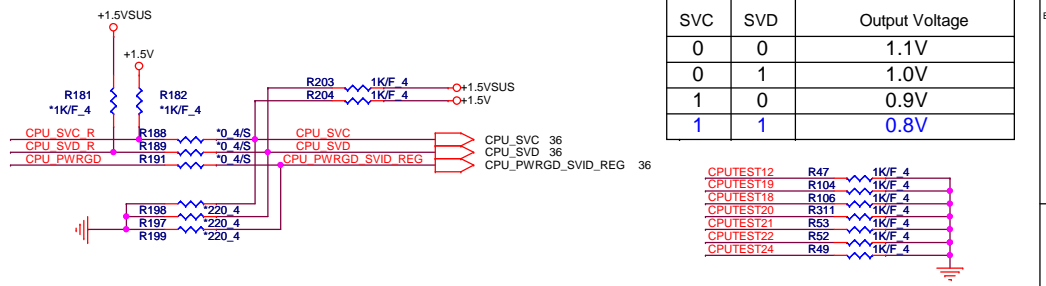


FOX PZ63826-284R-41F
 DG0*8000004 IC SOCKET SMD 638P S1(P1.27,H3.2)
 MLX 47296-4131
 DG0*8000003 IC SOCKET SMD 638P S1(P1.27,H3.2)
 TYC 4-1903401-2
 DG0*8000005 IC SOCKET SMD 638P S1(P1.27,H3.2)

HDT Connector



Serial VID

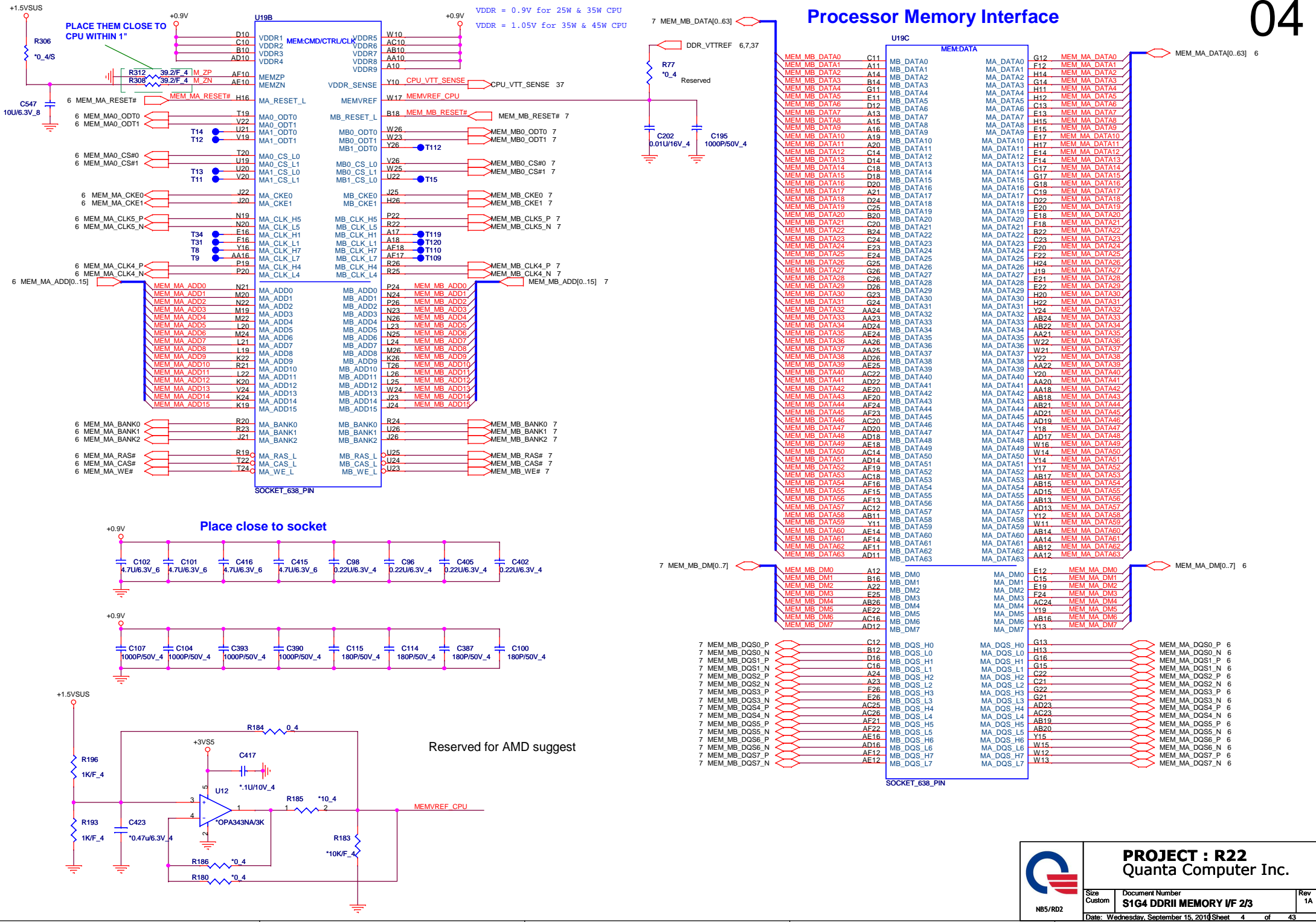


PROJECT : R22
Quanta Computer Inc.

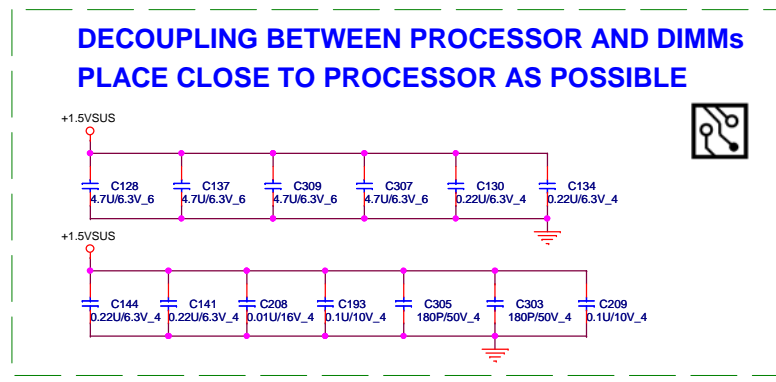
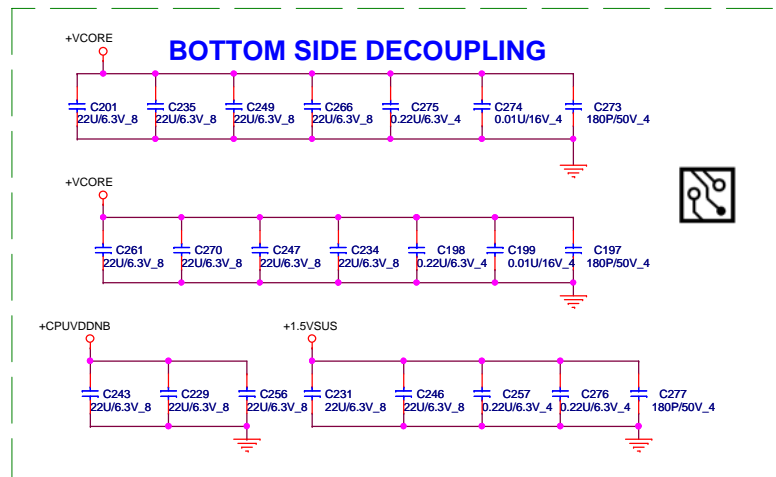
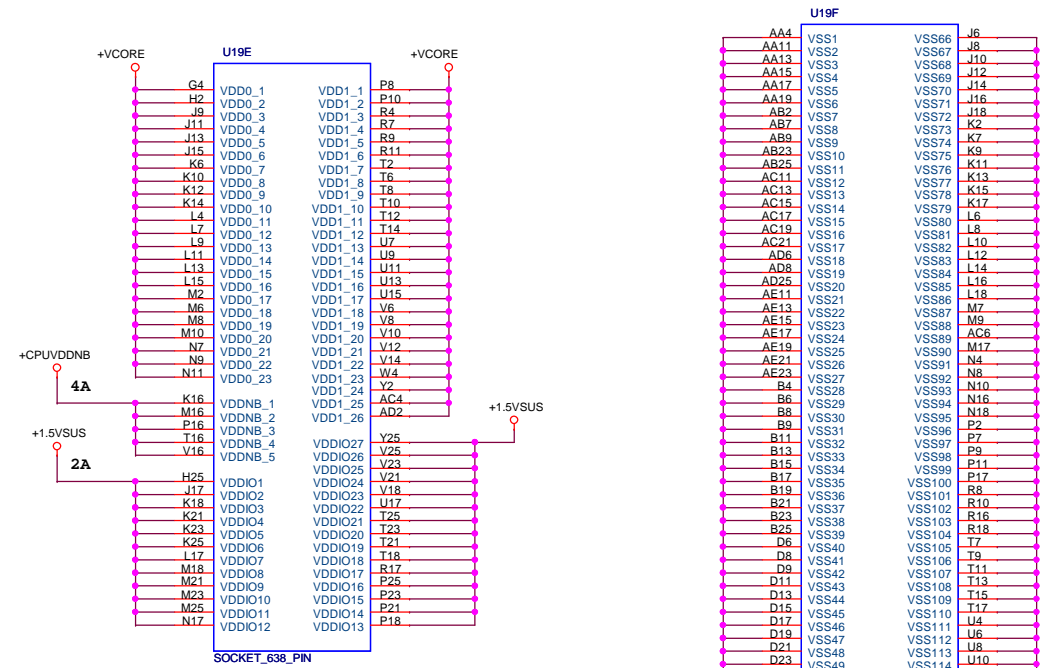
Size NB5/RD2	Document Number S1G4 HT,CTL I/F 1/3	Rev 1A
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Date: Wednesday, September 15, 2010 Sheet 3 of 43

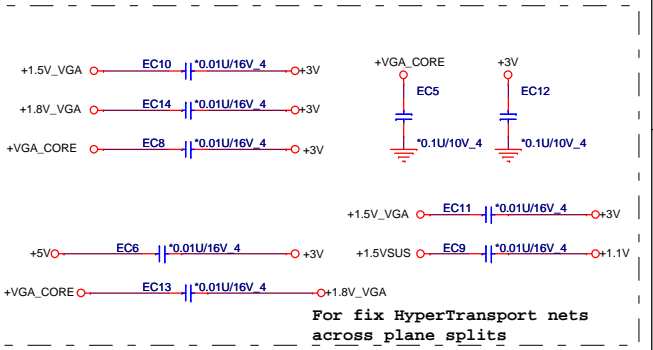
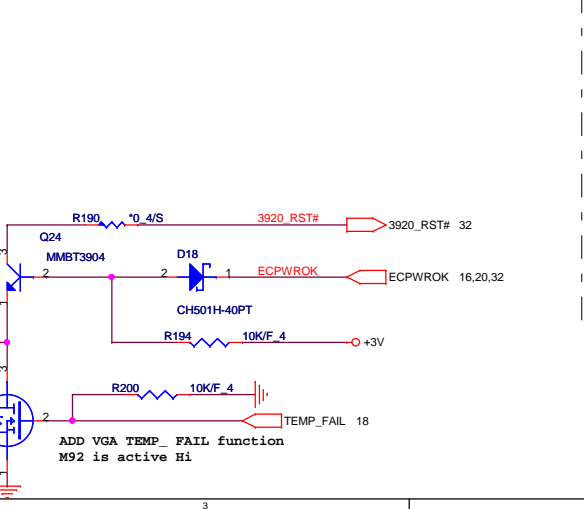
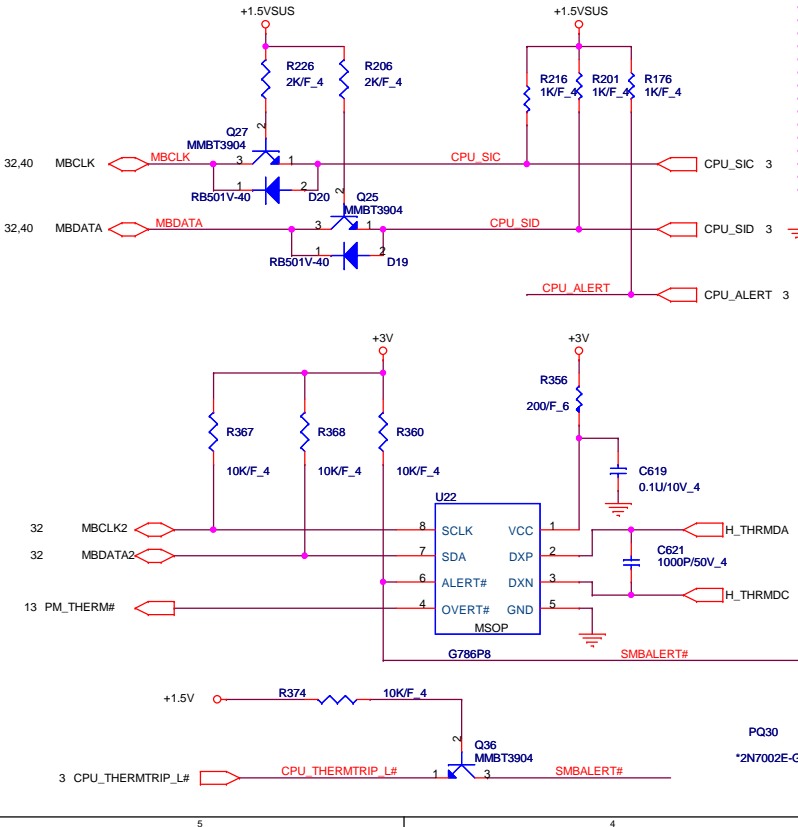
Processor Memory Interface




PROJECT : R22
Quanta Computer Inc.



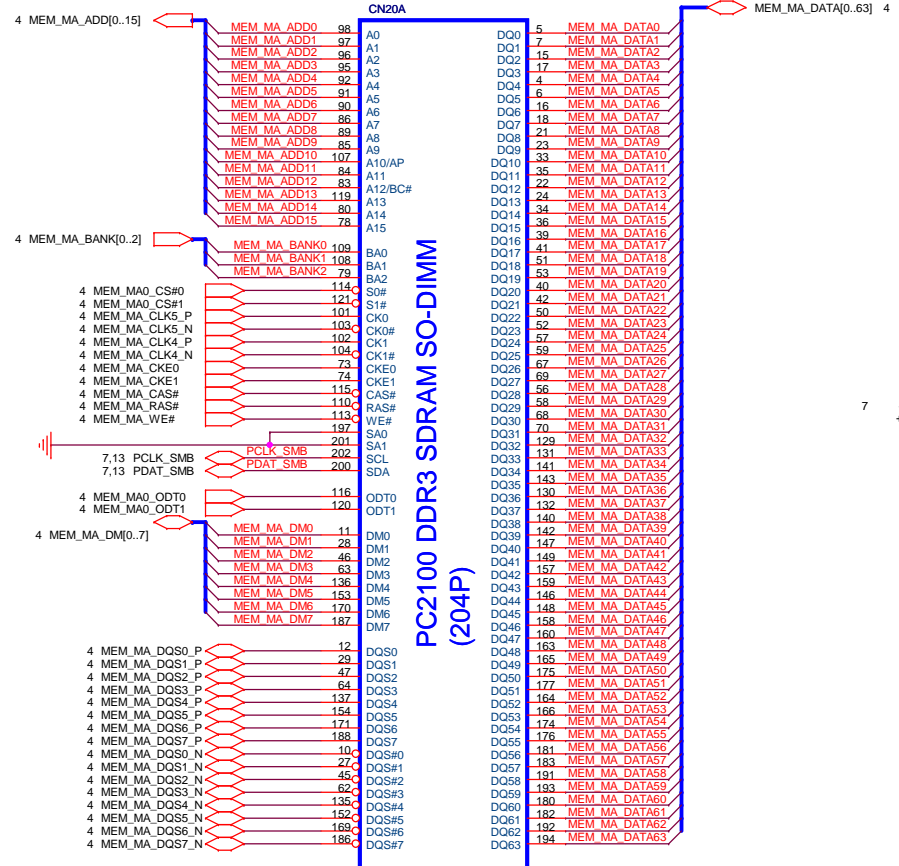
PROCESSOR POWER AND GROUND





PROJECT : R22
Quantal Computer Inc.

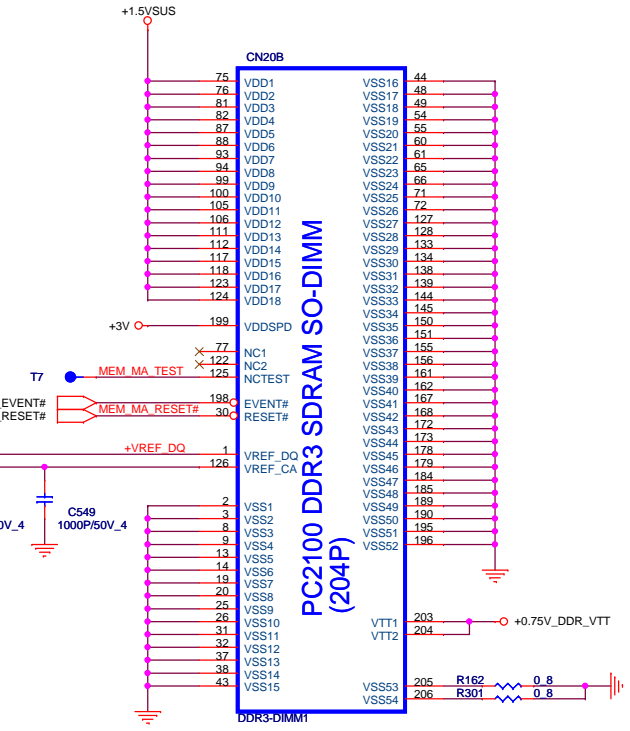
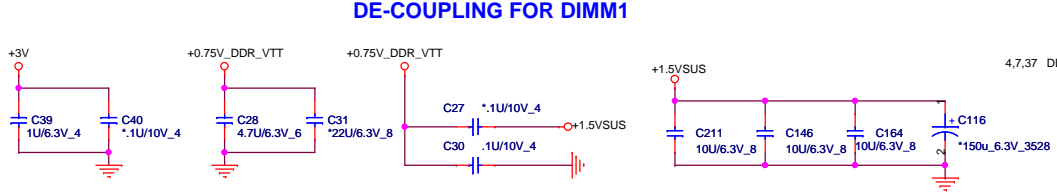
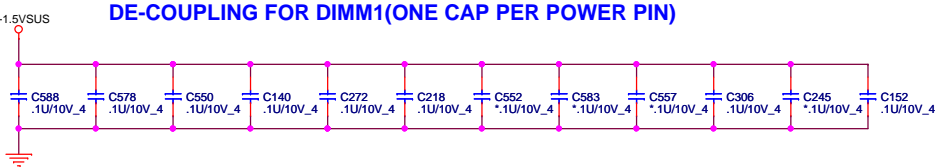
Size Custom	Document Number S1G4 PWR & GND 3/3	Rev 1A
Date: Wednesday, September 15, 2010 Sheet 5 of 43		



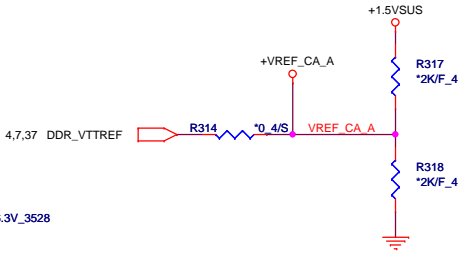
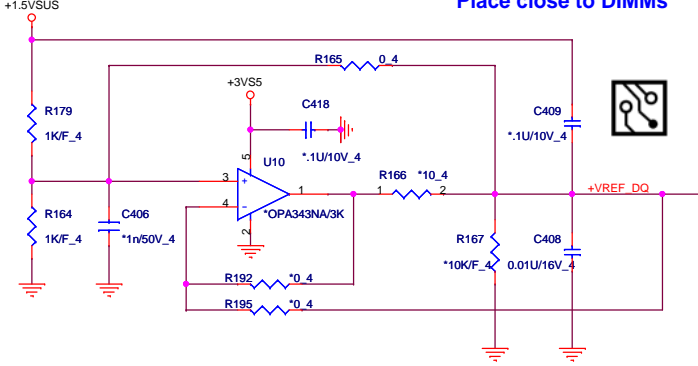
PC2100 DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM1
H=5.2 footprint: "ddr-c-2013289-204p"

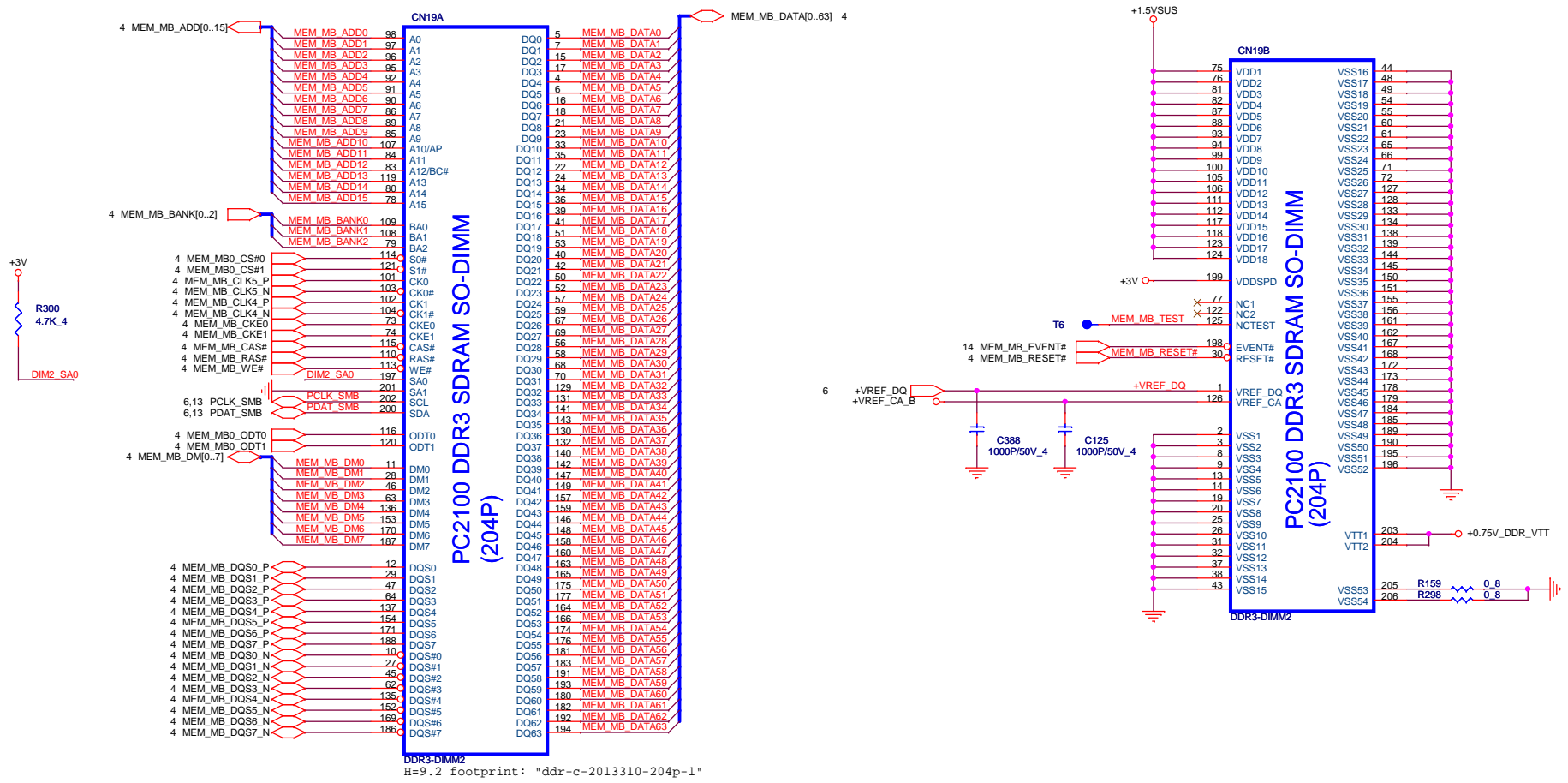
SO-DIMM BYPASS PLACEMENT :
Place these Caps near So-Dimm1.
No Vias Between the Trace of PIN to CAP.



Place close to DIMMs



PROJECT : R22
Quanta Computer Inc.

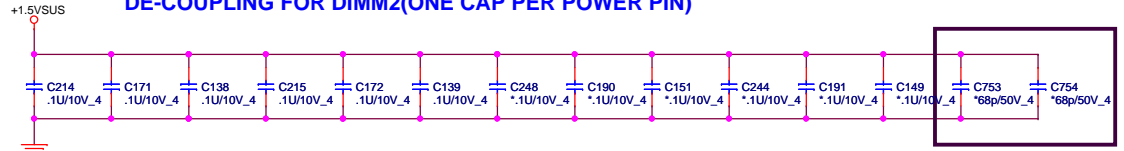


DDR3-DIMM2
H=9.2 footprint: "ddr-c-2013310-204p-1"

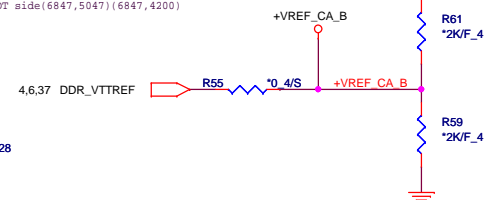
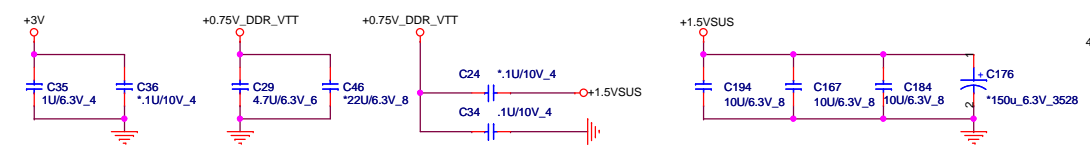
SO-DIMM BYPASS PLACEMENT :


- Place these Caps near So-Dimm1.
- No Vias Between the Trace of PIN to CAP.

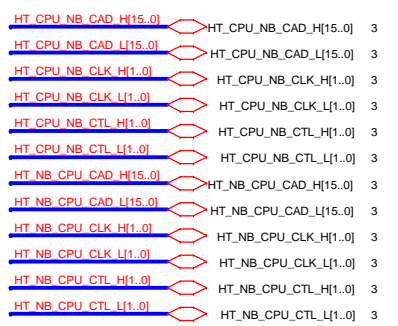
DE-COUPLING FOR DIMM2(ONE CAP PER POWER PIN)



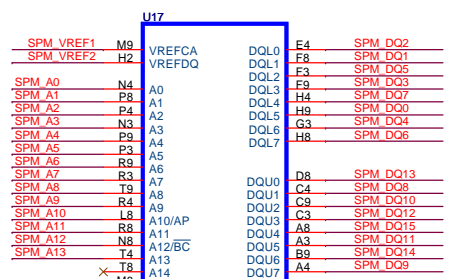
DE-COUPLING FOR DIMM2



 <p>NBS/RD2</p>	<p>PROJECT : R22 Quantas Computer Inc.</p>		
	<p>Size Custom</p>	<p>Document Number DDR3 SODIMMS TERMINATIONS</p>	<p>Rev 1A</p>
	<p>Date: Wednesday, September 15, 2010 Sheet 7 of 43</p>		

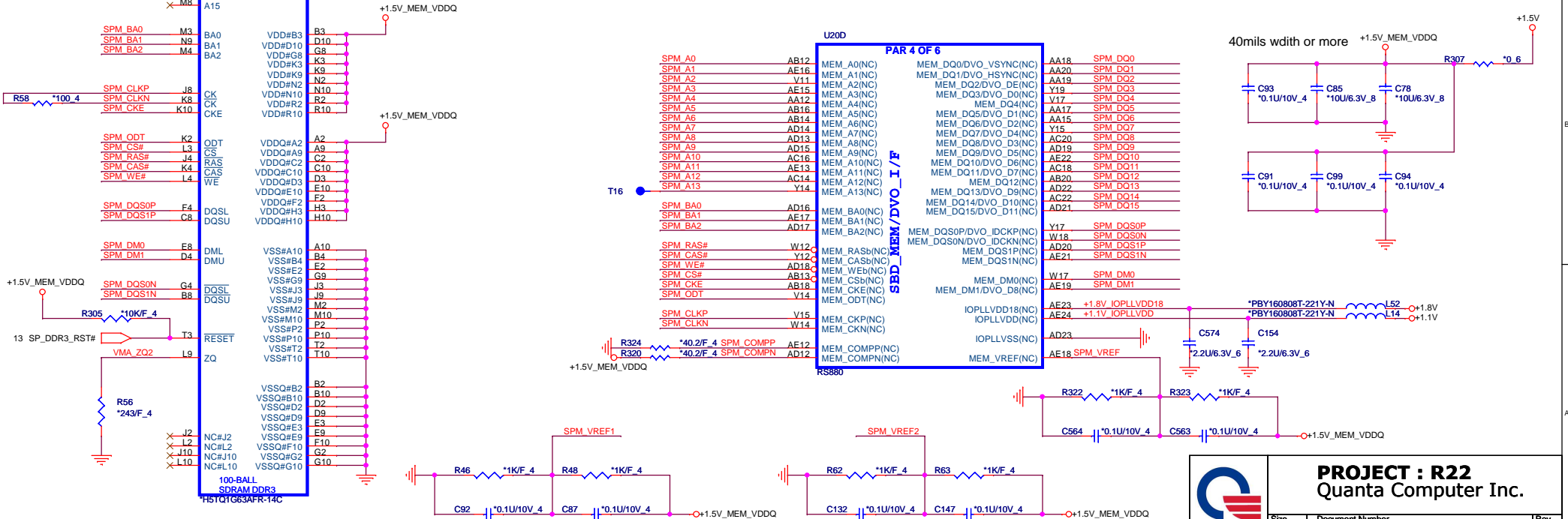


signals	RS880	RX880
HT_TXCALP	R430 301 ohm 1%	R430 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	R434 301 ohm 1%	R434 1.21k ohm 1%
HT_RXCALN		



HYPER TRANSPORT CPU I/F

This block is for UMA only , DIS can remove all component

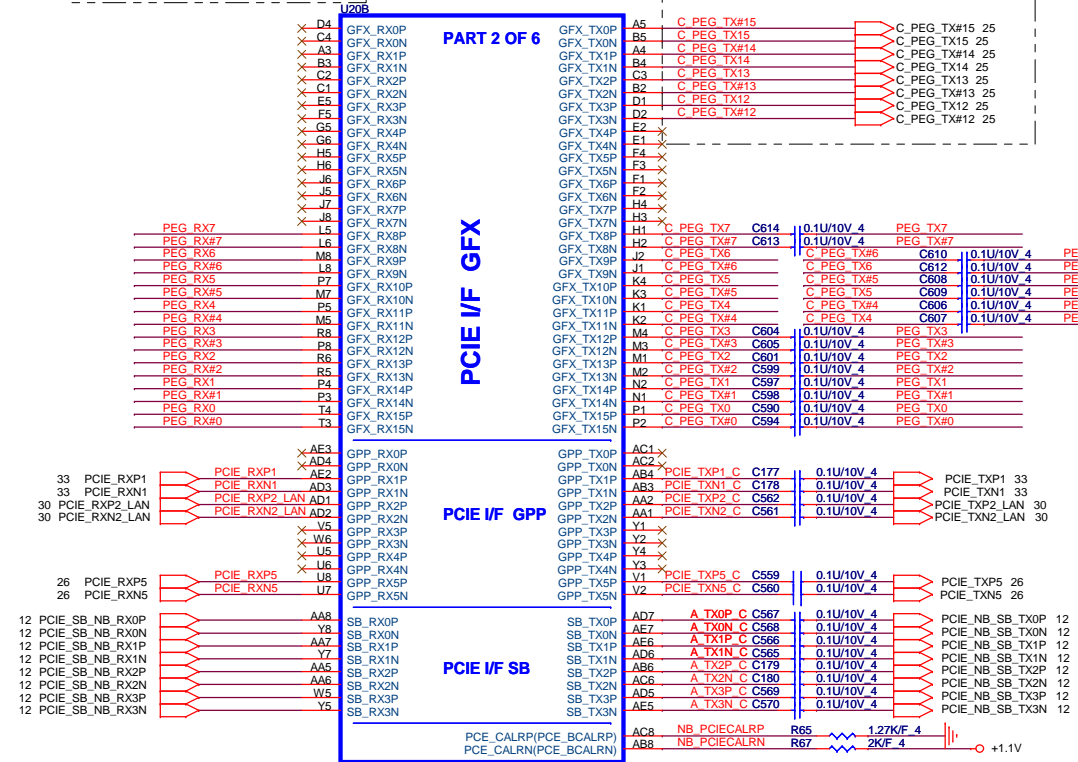


PROJECT : R22 Quanta Computer Inc.

UMA can remove all GFX_TX CAP

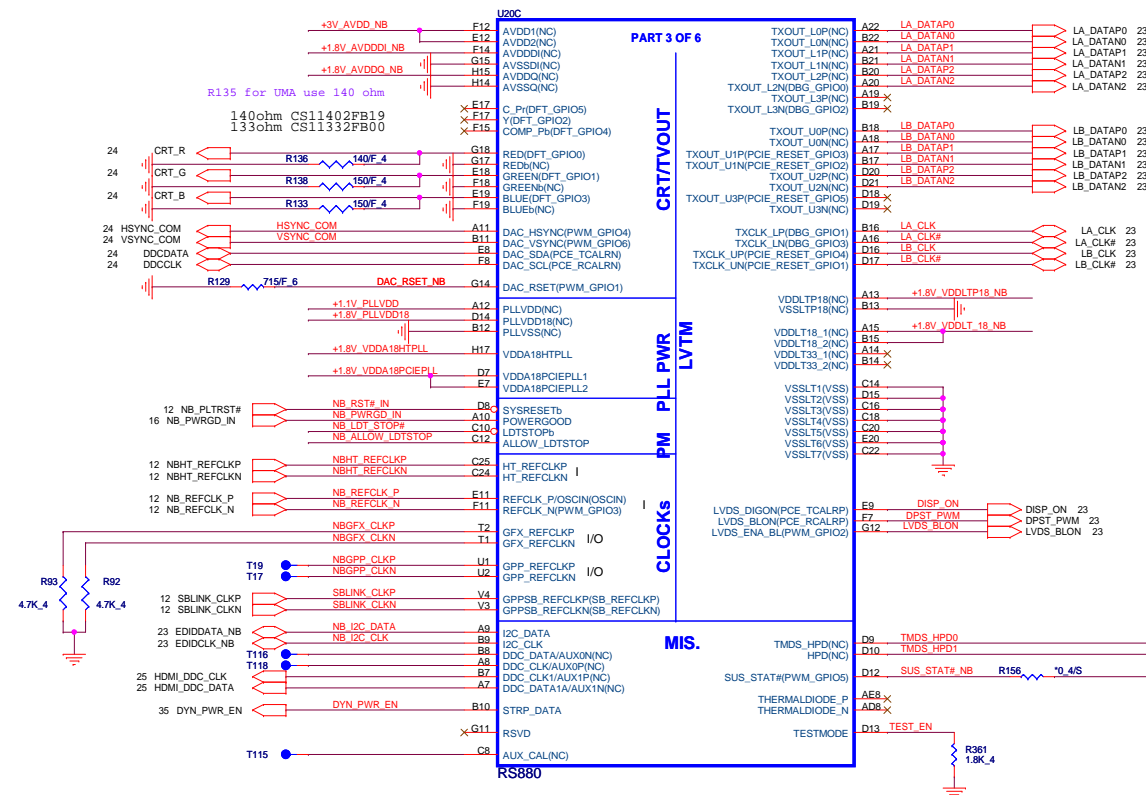
GFX_RX can remove at next stage for MUXLESS

To HDMI CONN



PROJECT : R22
Quanta Computer Inc.

Size Custom	Document Number RS880-PCIE I/F 2/5	Rev 1A
Date: Wednesday, September 15, 2010 Sheet 9 of 43		



STRAP_DEBUG_BUS_GPIO_ENABLEB

Enables the Test Debug Bus using GPIO.

RS880M	
1	Disable
0	Enable

VSYNC_COM R369 3K_4 +3V

RS880M: Enables Side port memory

RS880M:HSYNC#

Selects if Memory SIDE PORT is available or not
 1 = Memory Side port Not available
 0 = Memory Side port available

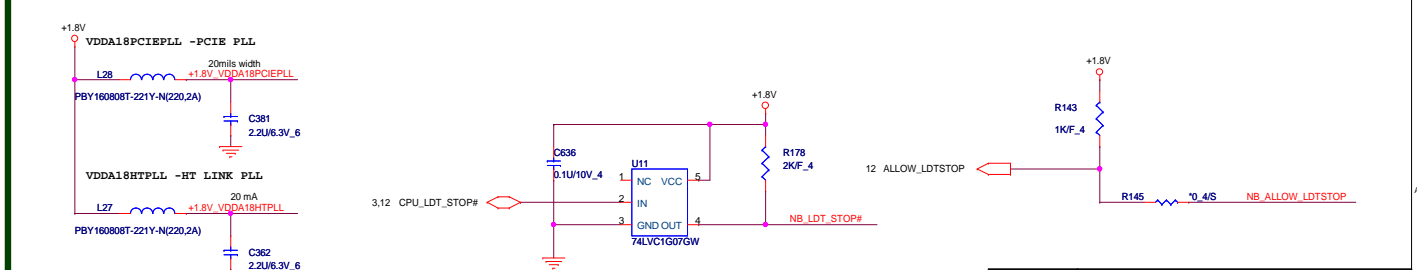
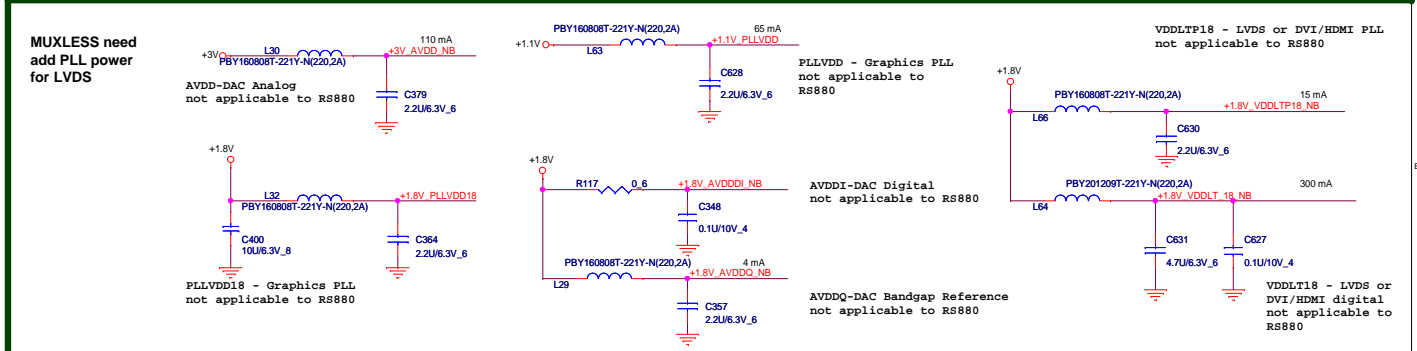
Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]

HSYNC_COM R365 3K_4 +3V
 R364 3K_4

For external EEPROM Debug only

RS780/RX780

DYN_PWR_EN R363 2Kf_4



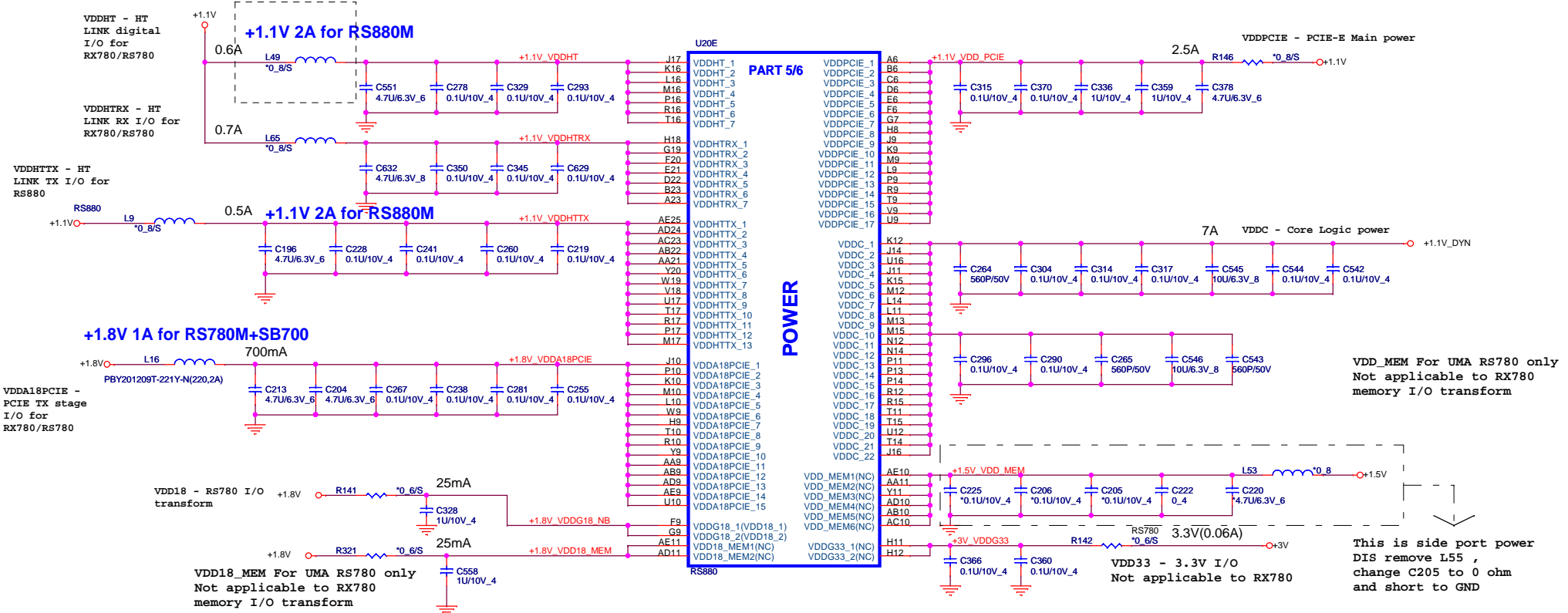
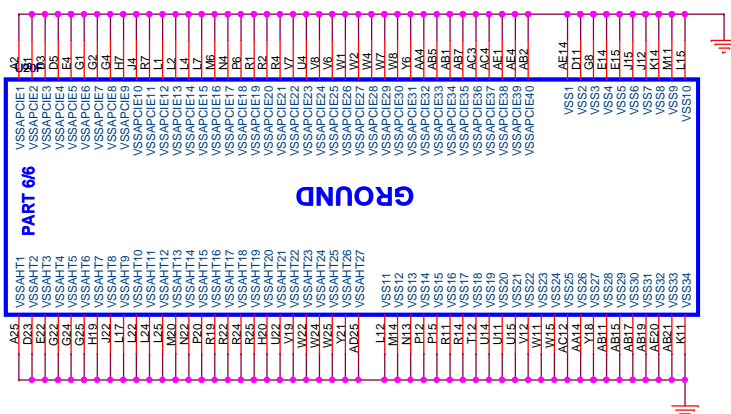
PROJECT : R22
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
	RS880-SYSTEM I/F 3/5	
Date: Wednesday, September 15, 2010 Sheet 10 of 43		

NBS/RDZ

RS880M POWER TABLE

PIN NAME	RS880M	PIN NAME	RS880M
VDDHT	+1.1V	IOPLLVD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVD	+1.1V
VDD18_MEM	+1.8V	PLLVD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDL18	+1.8V
IOPLLVD18	+1.8V	VDDL133	NC



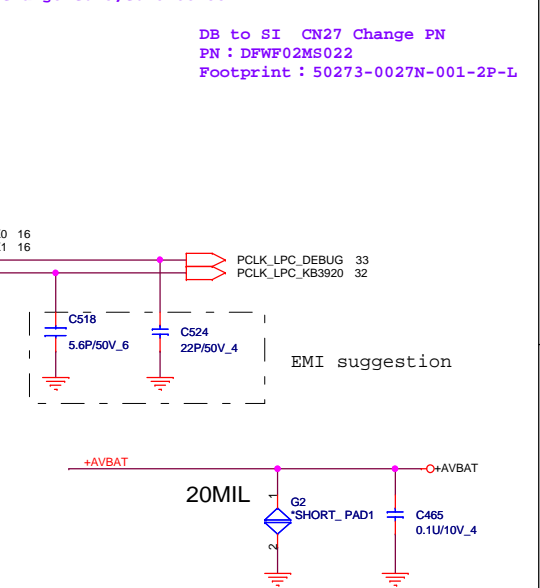
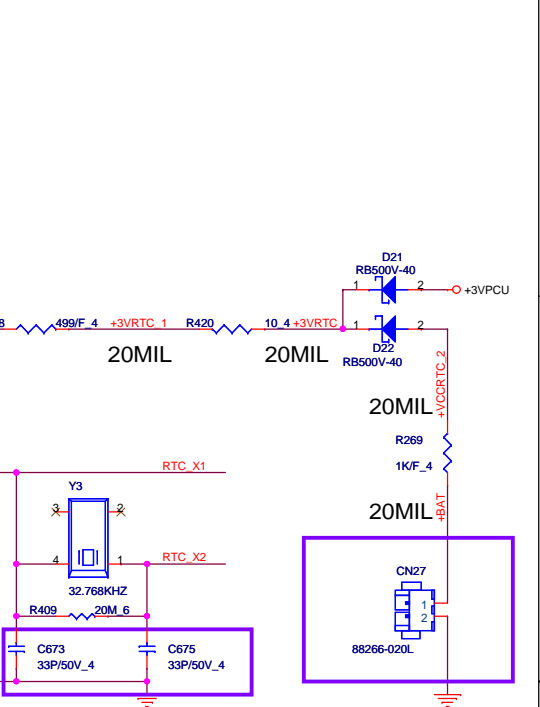
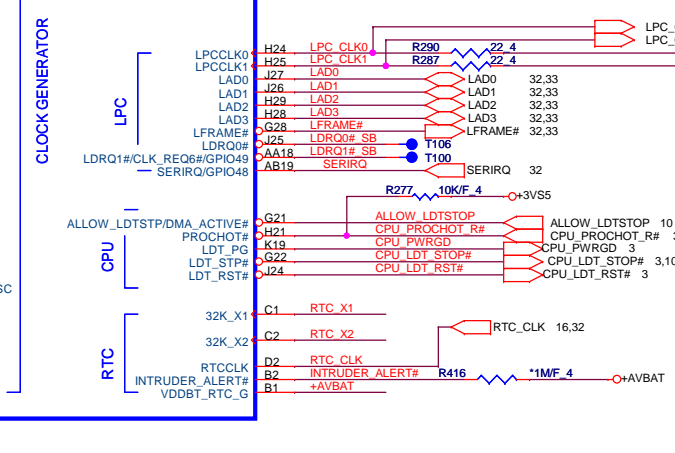
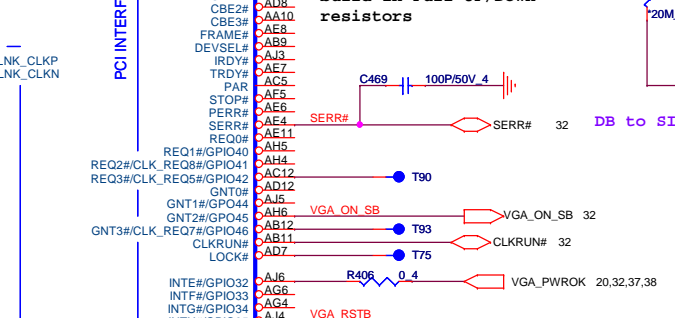
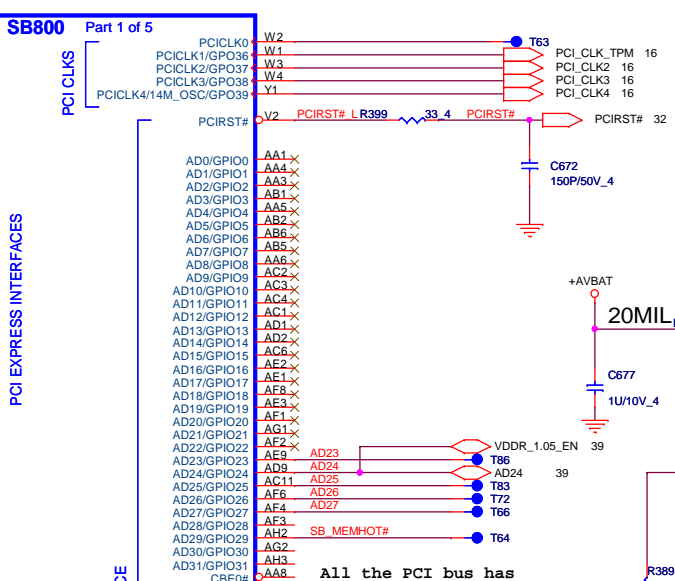
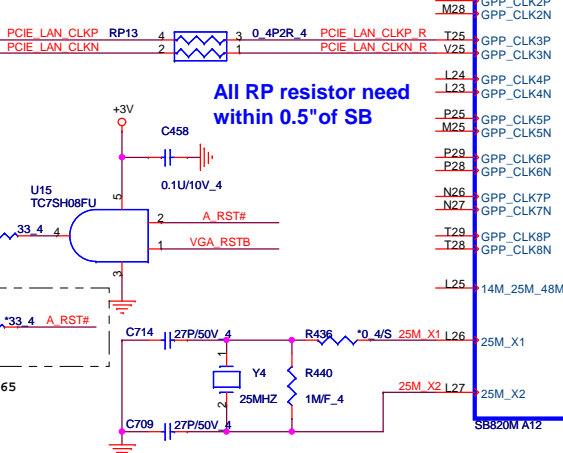
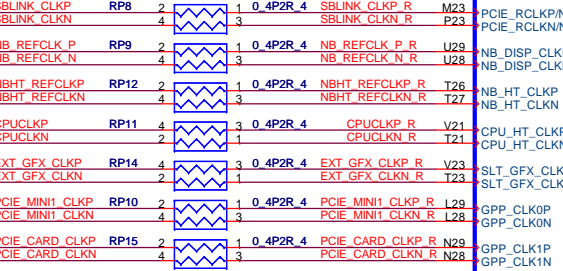
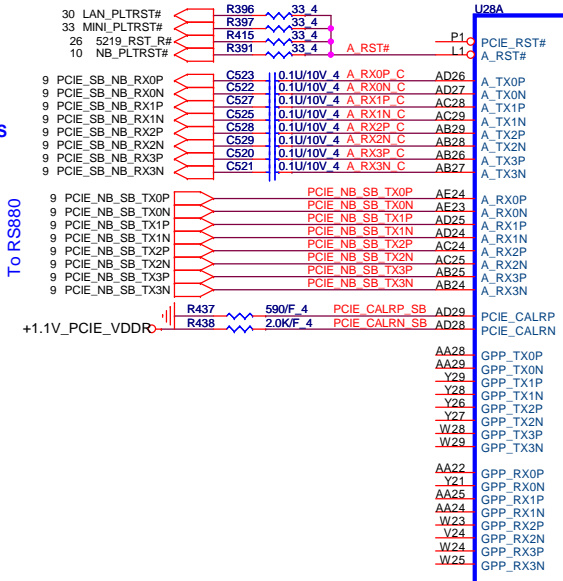
VDD_MEM For UMA RS780 only
Not applicable to RX780
memory I/O transform

This is side port power
DIS remove L55,
change C205 to 0 ohm
and short to GND



PROJECT : R22
Quanta Computer Inc.

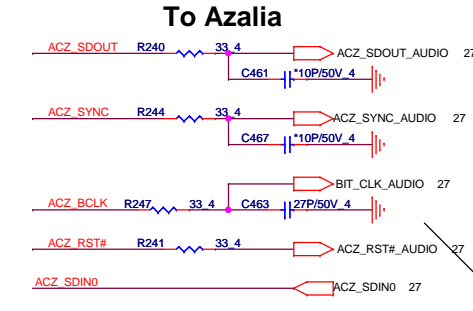
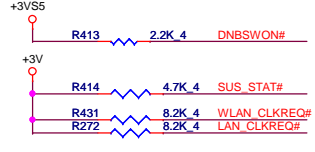
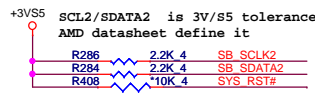
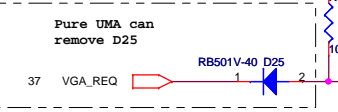
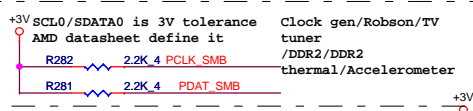
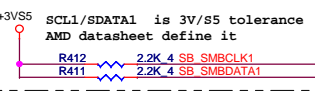
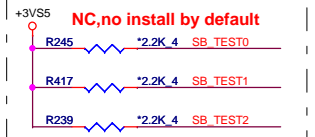
PLACE THESE
PCIE AC
COUPLING CAPS
CLOSE TO SB



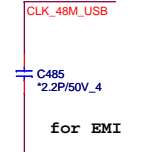
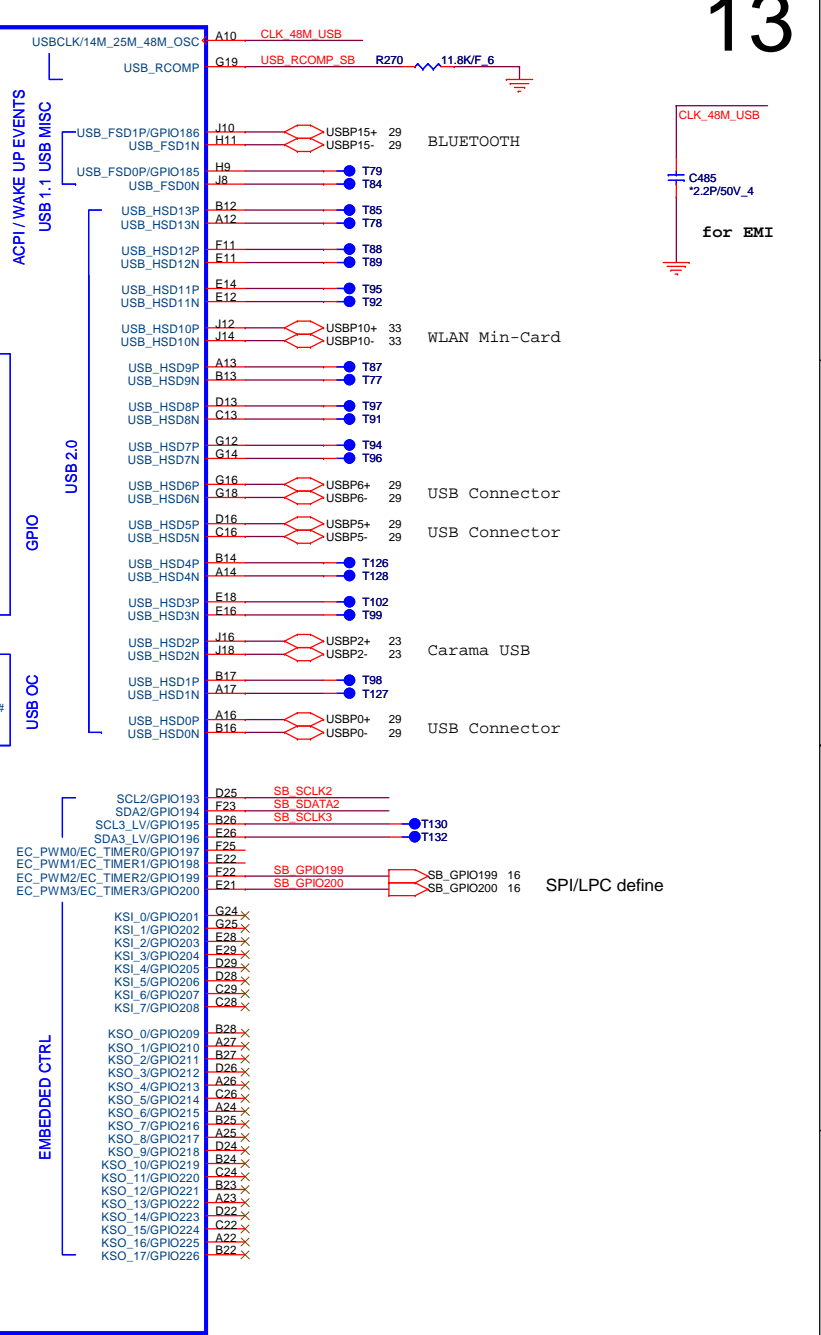
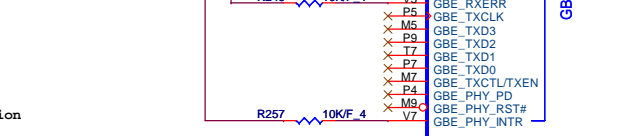
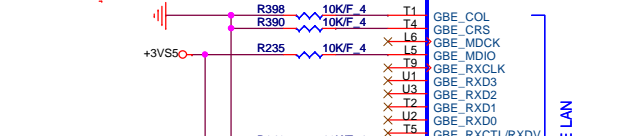
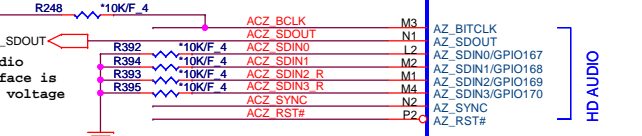
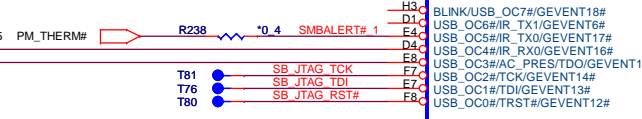
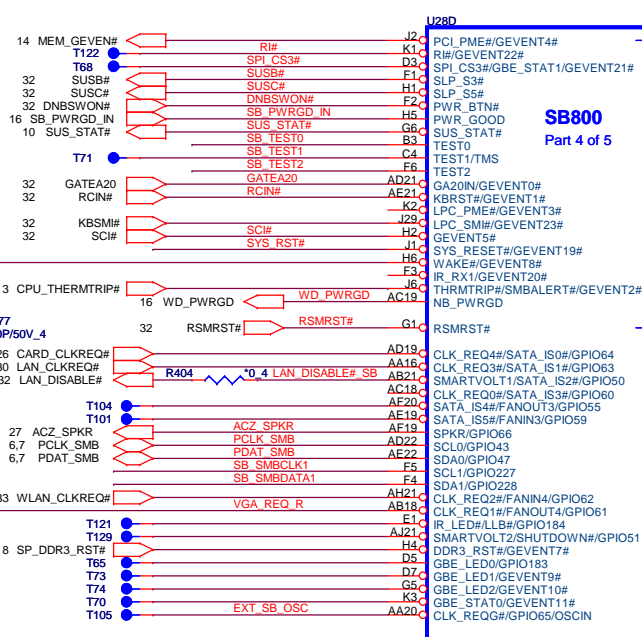
INTRUDER_ALERT# Left not connected (Southbridge has 50-kohm internal pull-up to VBAT).

PROJECT : R22
 Quanta Computer Inc.

Size Custom Document Number SB820-PCIE/PCI/CPU/LPC 1/4 Rev 1A
 Date: Wednesday, September 15, 2010 Sheet 12 of 43



For Zero ODD



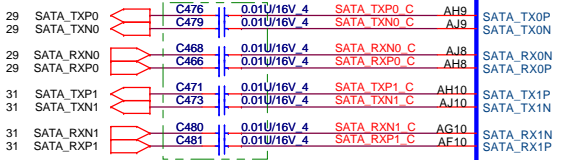
PROJECT : R22
Quantas Computer Inc.

SATA PORT 0,1,2,3
can support AHCI
mode

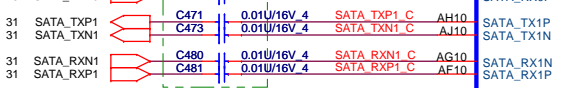
PLACE SATA AC COUPLING
CAPS CLOSE TO SB820

IF THERE IS NO IDE, TEST
POINTS FOR DEBUG BUS
IS MANDATORY

SATA1



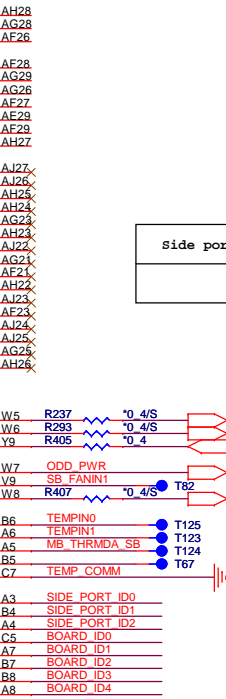
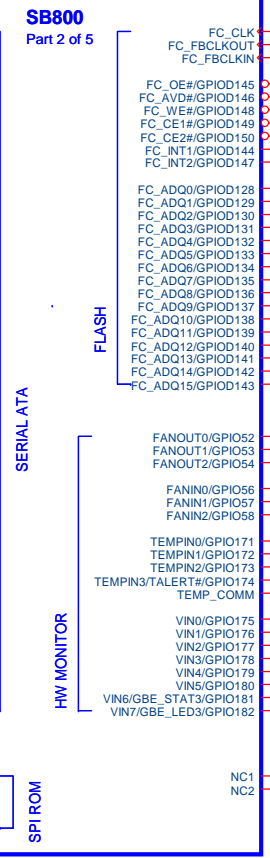
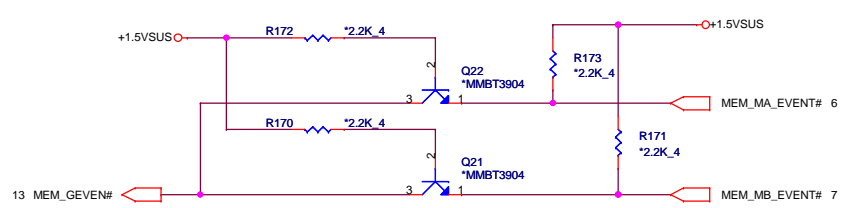
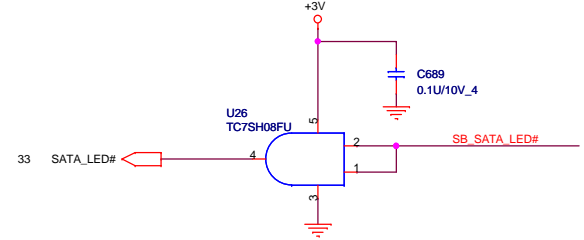
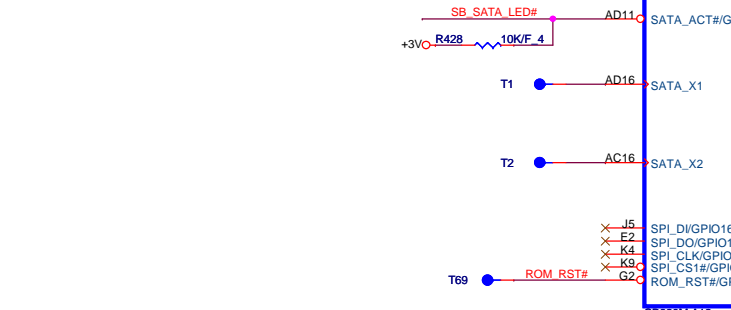
SATA ODD



NOTE:
R361 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK

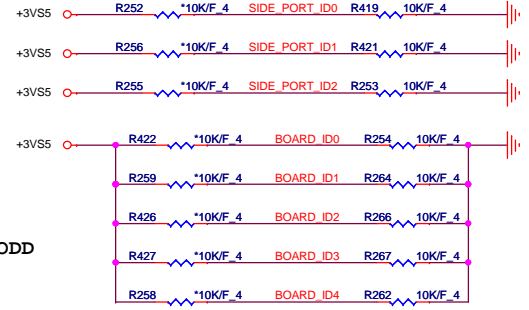
PLVDD_SATA--
SATA PLL
POWER

XTLVDD_SATA-- SATA
crystal power



SIDE_PORT_ID2	SIDE_PORT_ID1	SIDE_PORT_ID0	
1	0	0	Samsung
1	0	1	Hynix
0	0	0	No support side port

Side port IDE H/W setting



For Zero ODD

ID4	ID3	ID2	ID1	ID0	CONFIG	31- Level BOM	Item
0	0	0	0	0	UMA		1
0	0	0	1	0			2
0	0	1	0	0			3
0	0	1	1	0			4
0	1	0	1	0			5
0	1	1	1	0			6
1	0	0	1	0			7
1	0	1	1	0			8
0	0	0	0	1	SG / Muxless		9
0	0	1	0	1			10
1	0	0	1	1			11
1	0	1	1	1			12

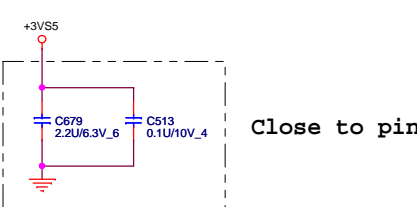
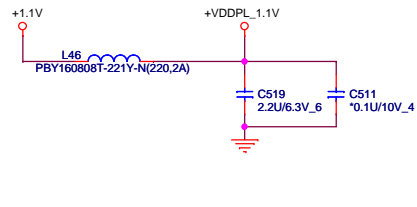
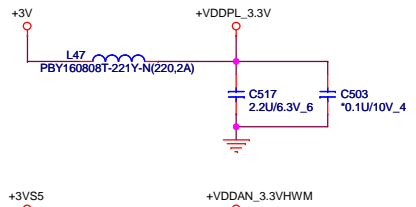
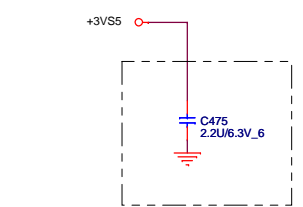
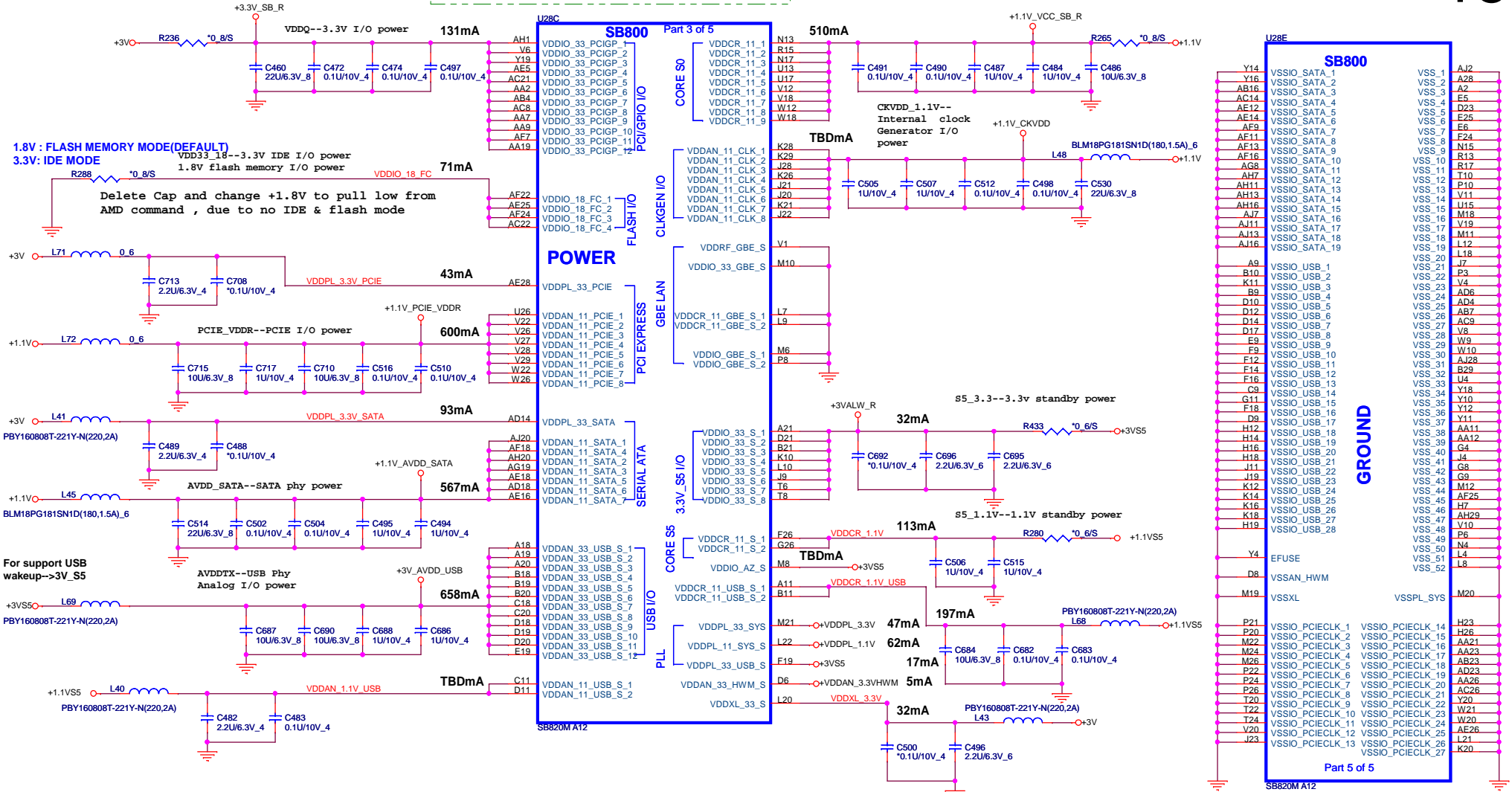
Item	Board ID Hardware setting
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	

PROJECT : R22
Quanta Computer Inc.

Size Custom Document Number **SB820-ACPI/GPIO/USB 2/4** Rev 1A

NB5/RD2 Date: Wednesday, September 15, 2010 Sheet 14 of 43

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

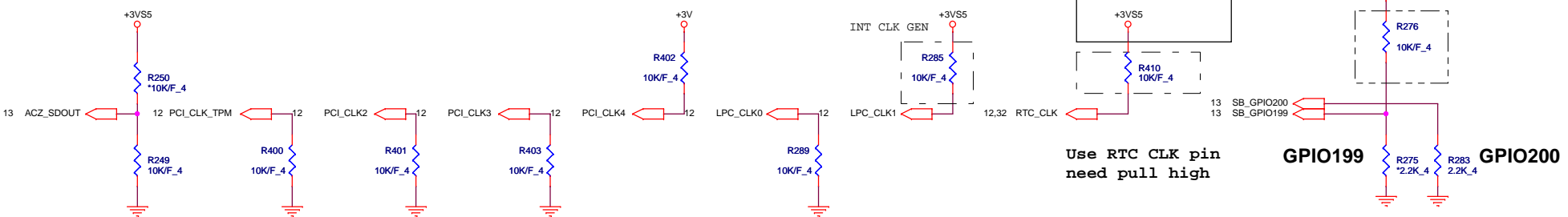


PROJECT : R22
Quantal Computer Inc.

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

internal have pull Hi 10K , confirm AMD ward this pull Hi not need

REQUIRED STRAPS



It must ready before RSMRST#

Use RTC CLK pin need pull high

GPIO199 GPIO200

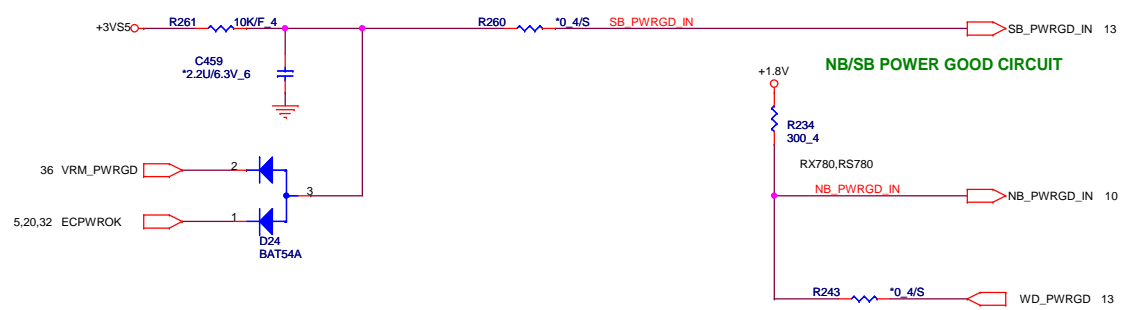
REQUIRED STRAPS

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM (Default) L,L = FWH ROM	

DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)

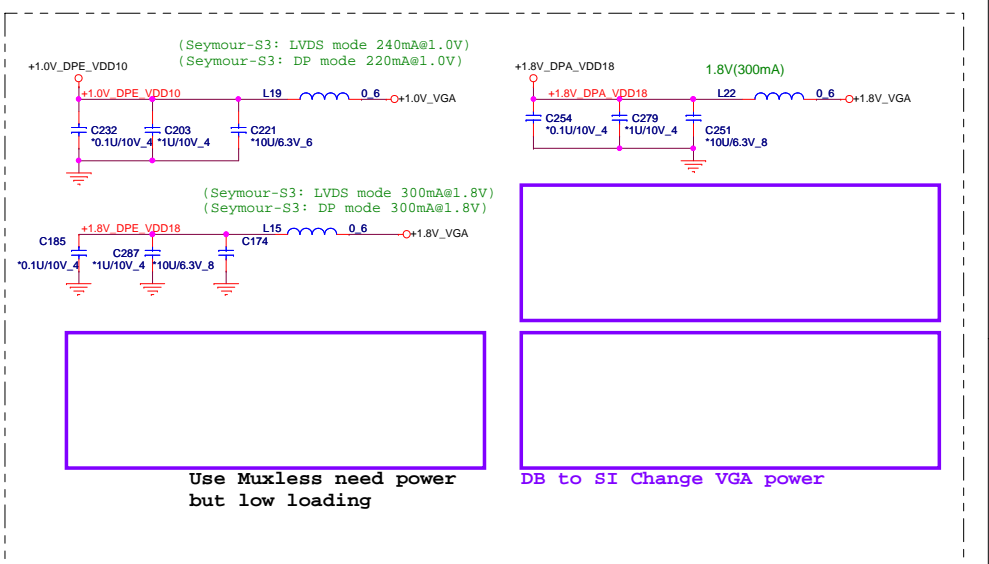
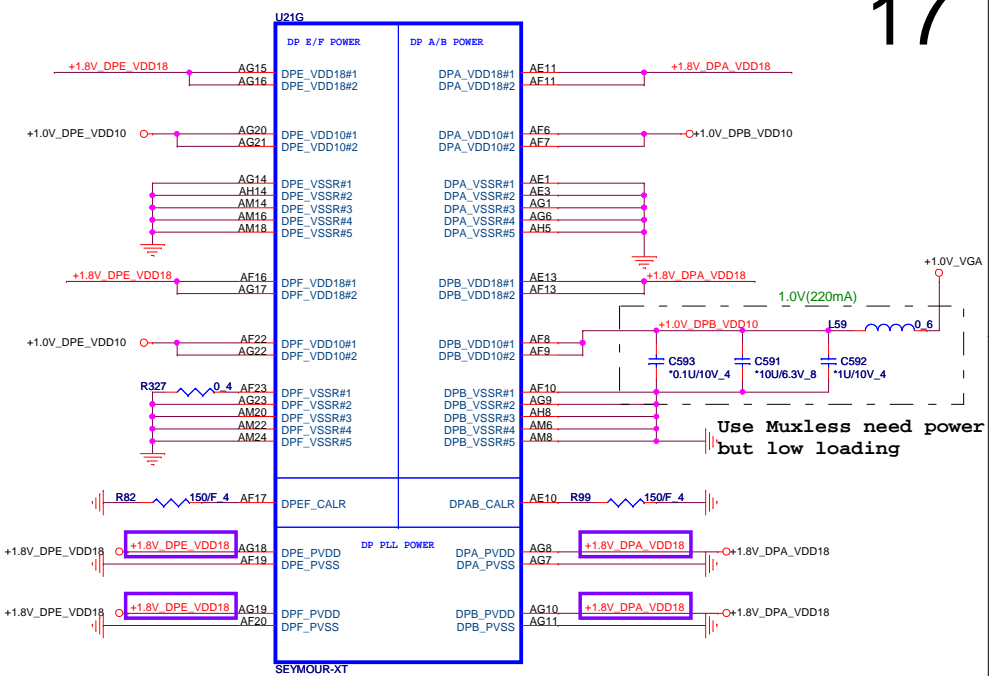
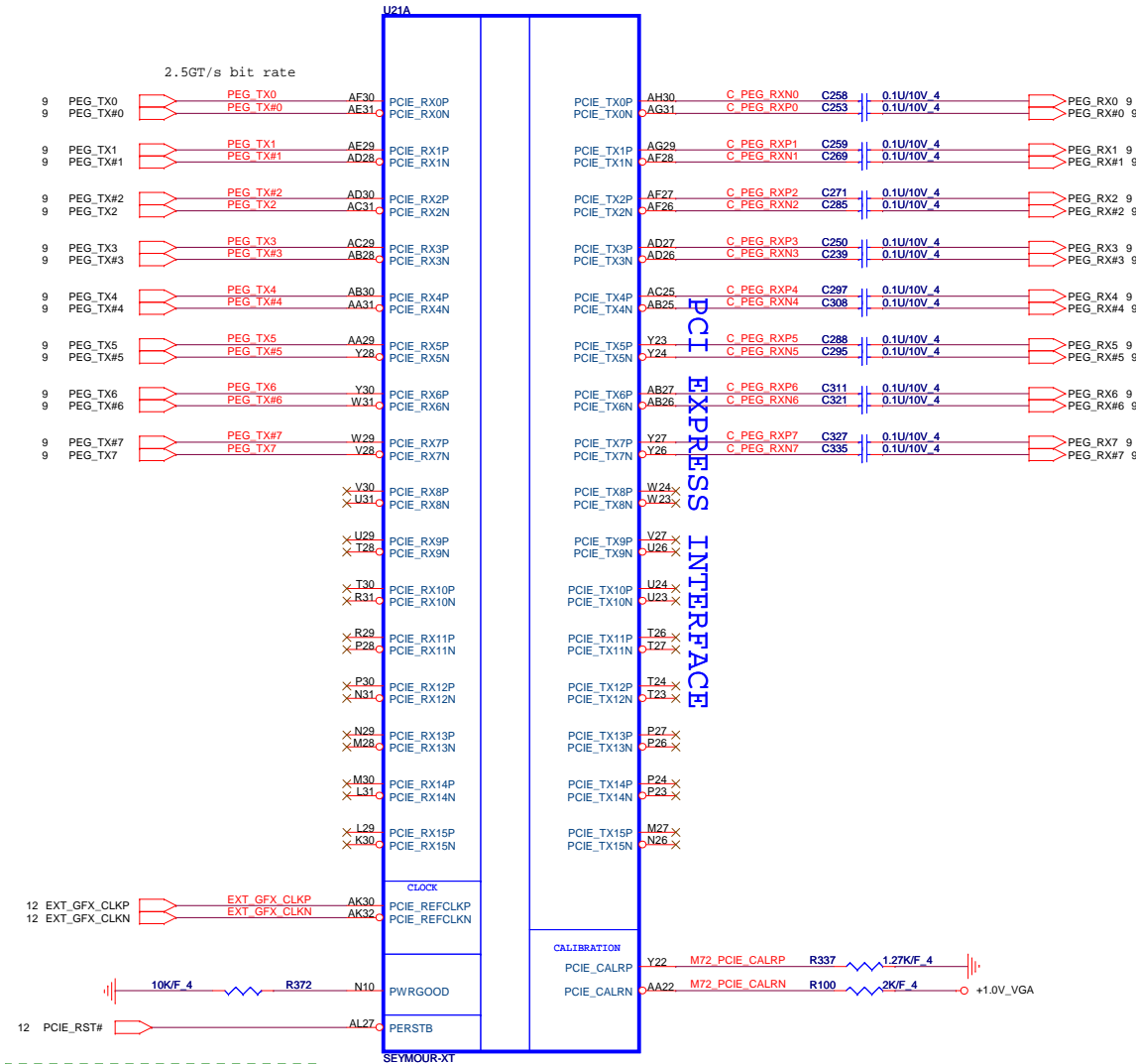


	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

AL17SZ17000 IC(5P) NL17SZ17DFT2G(SOT-353) SOT-353
ALUC1G17000 IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5) SOT23-5

PROJECT : R22
Quanta Computer Inc.

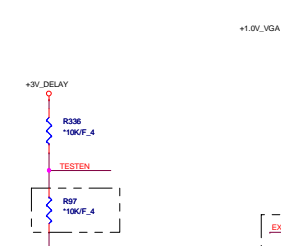
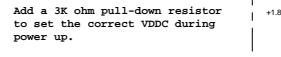
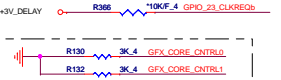
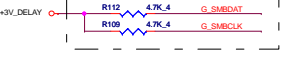
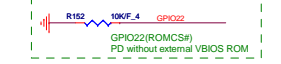
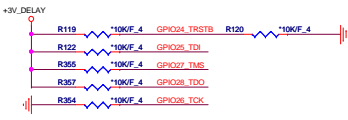
Size Custom Document Number **SB820-STRAPS** Rev 1A
Date: Wednesday, September 15, 2016 Sheet 16 of 43



100MHz (+/-300ppm) input frequency,
0-0.7V single-ended swing

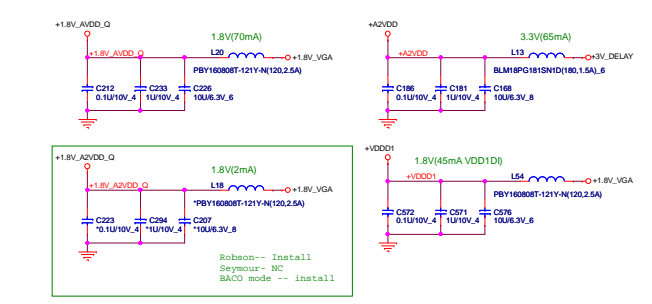
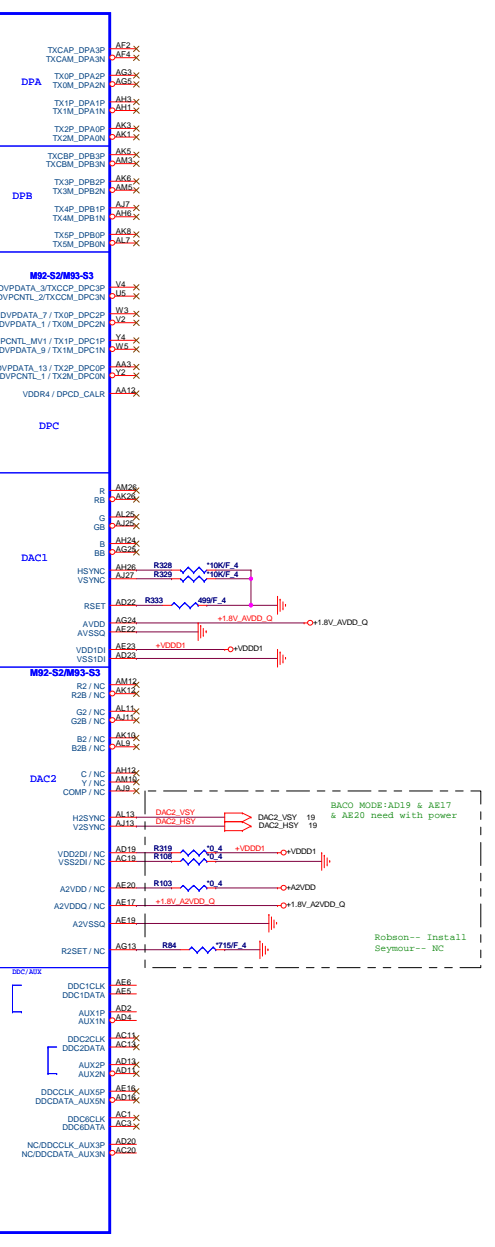
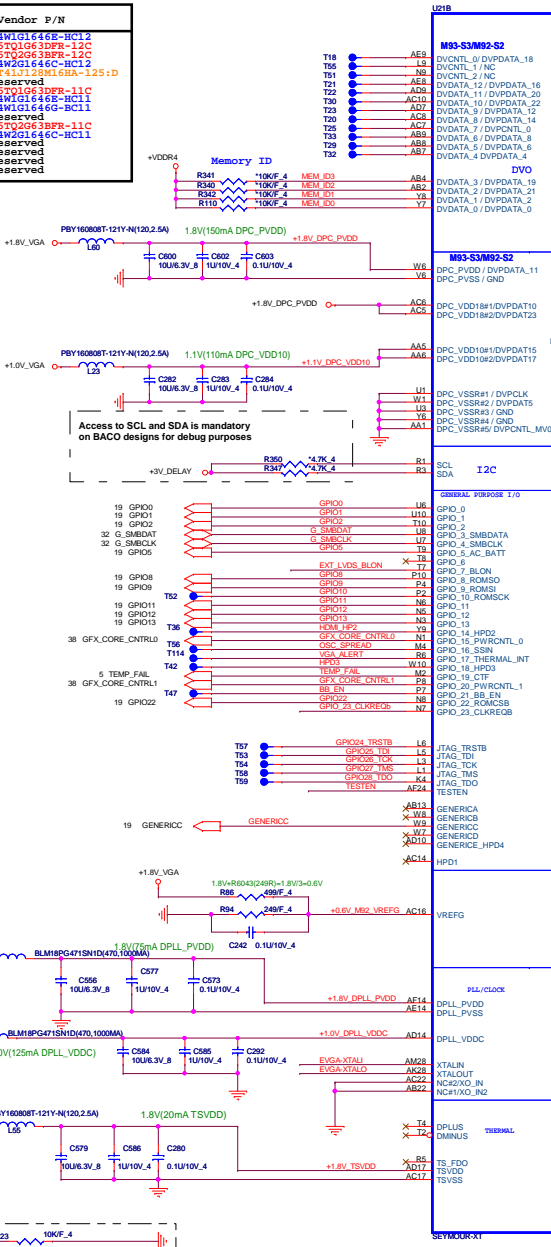
MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Samsung- E die	64*16-800MHZ	K4W1G1646E-HC12
0001	Hynix- Vega die	64*16-800MHZ	H5TQ1G63DFR-12C
0010	Hynix- Vega die	128*16-800MHZ	H5TQ2G63BFR-12C
0011	Samsung- C die	128*16-800MHZ	K4W2G1646C-HC12
0100	MICRON	Reserved	M7E931159H161A-125D
0101		Reserved	
0110	Hynix- Vega die	64*16-900MHZ	H5TQ1G63DFR-11G
0111	Samsung- G die	64*16-900MHZ	K4W1G1646G-HC11
1000	Samsung- G die	64*16-900MHZ	K4W1G1646G-HC11
1001		Reserved	
1010	Hynix- Vega die	128*16-900MHZ	H5TQ2G63BFR-11C
1011	Samsung- C die	128*16-900MHZ	K4W2G1646C-HC11
1100		Reserved	
1101		Reserved	
1110		Reserved	
1111		Reserved	

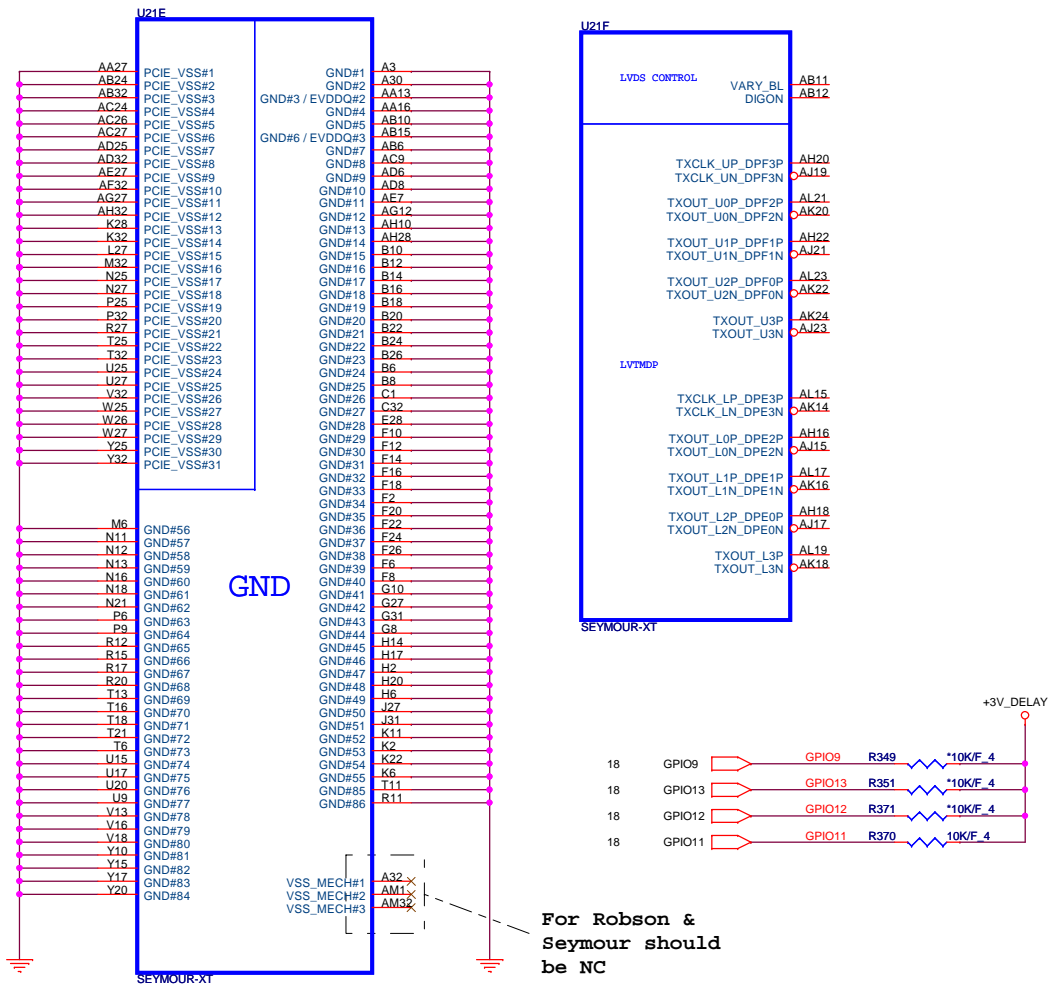
MEM_ID[3:0]	31 Level BOM	H/W setting
0000	TBD	TBD
0001	TBD	TBD
0010	TBD	TBD
0011	TBD	TBD
0100	TBD	TBD



Seymour uninstall to meet AP24 N/C

If no contact this pin to LVDS need pull low



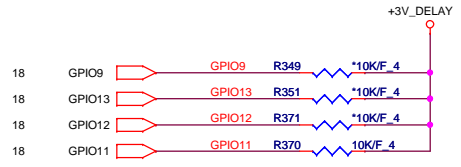


CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

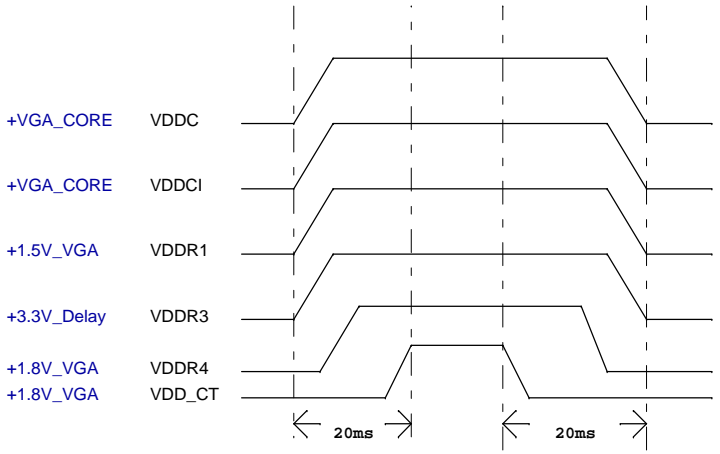
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:1]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSNC	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS
ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21	H2SYNC	GENERICC	GPIO8	GPIO2
--------	--------	----------	-------	-------



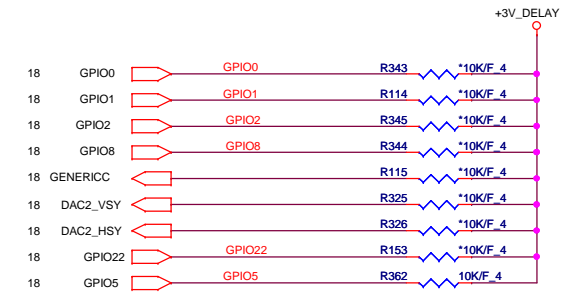
Power Up/Down Sequence



Memory Aperture size

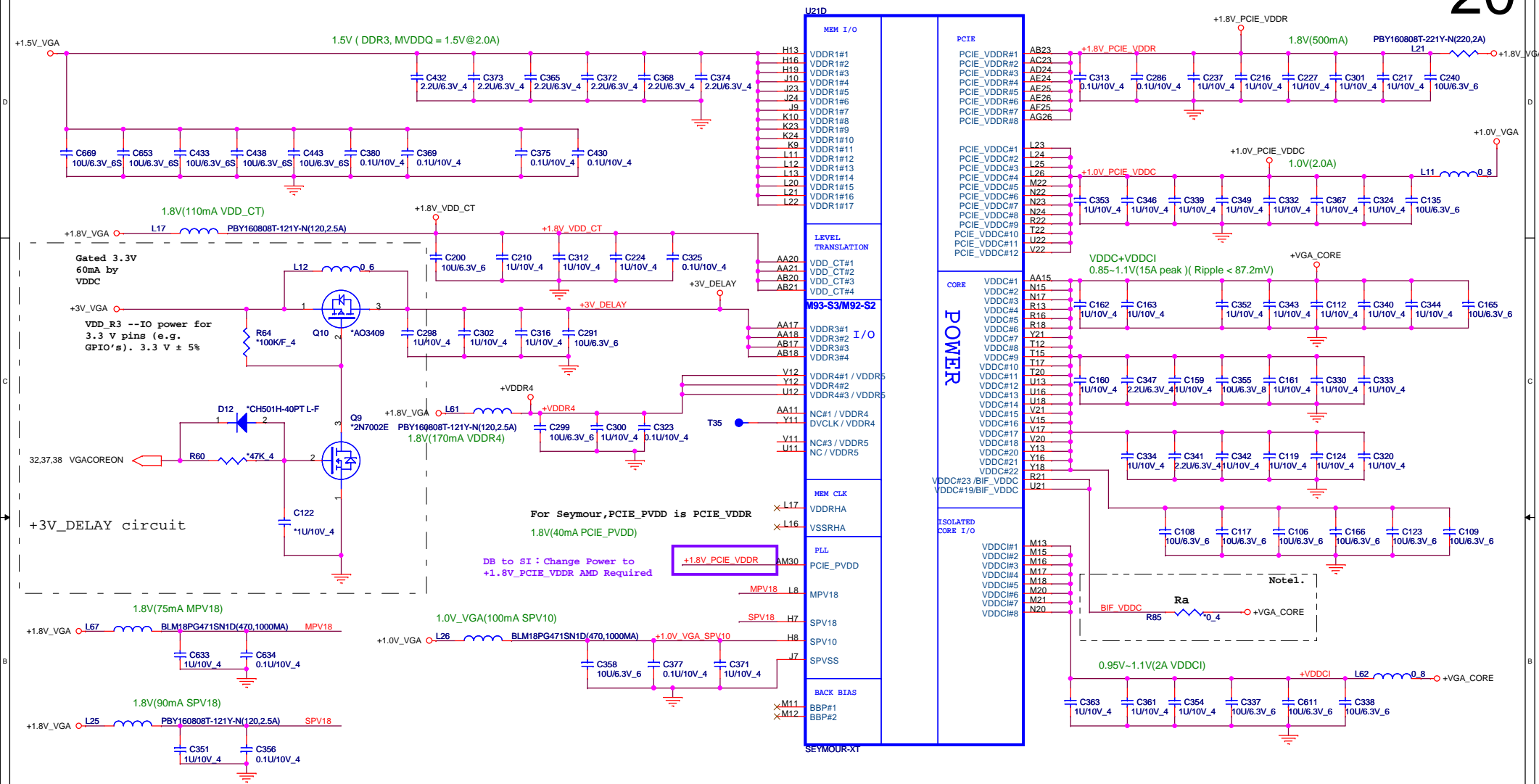
GPIO9	GPIO13	GPIO12	GPIO11
BIOSROM	ROMIDCFG2	ROMIDCFG1	ROMIDCFG0
0	128M	0	0
0	64M	0	1
0	32M	0	1
0	512M	1	0
0	1G	1	1
0	2G	1	1
0	4G	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

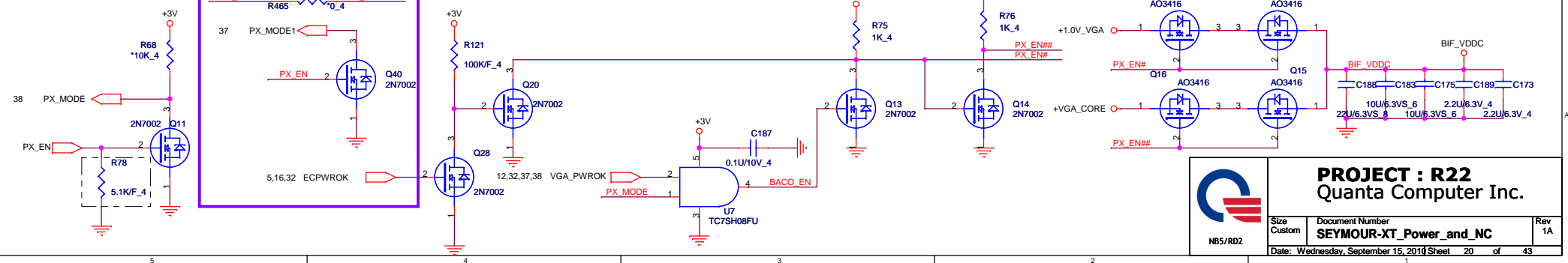


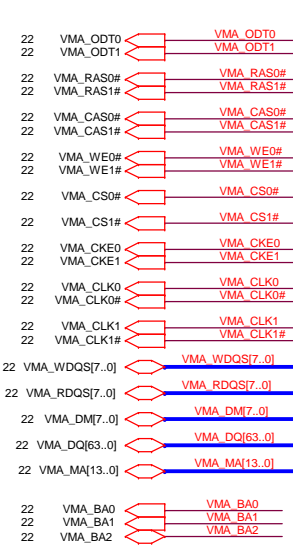
PROJECT : R22
Quantas Computer Inc.

Size Custom	Document Number	Rev 1A
SEYMOUR-XT GND / LVDS/ Straps		
Date: Wednesday, September 15, 2010 Sheet 19 of 43		

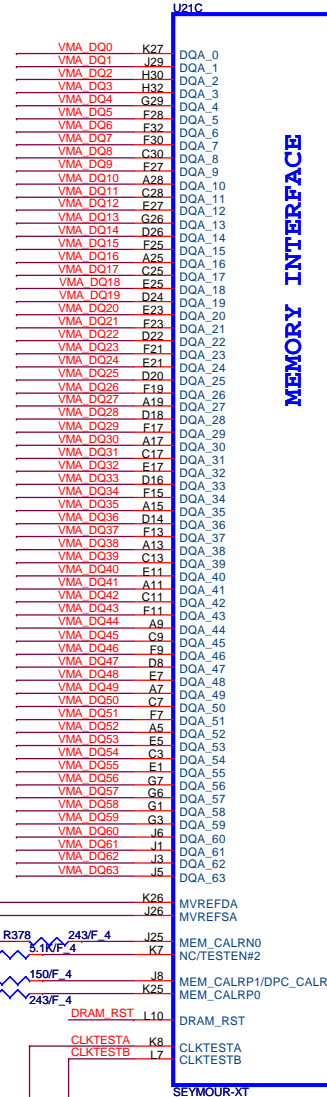


Support BACO Mode

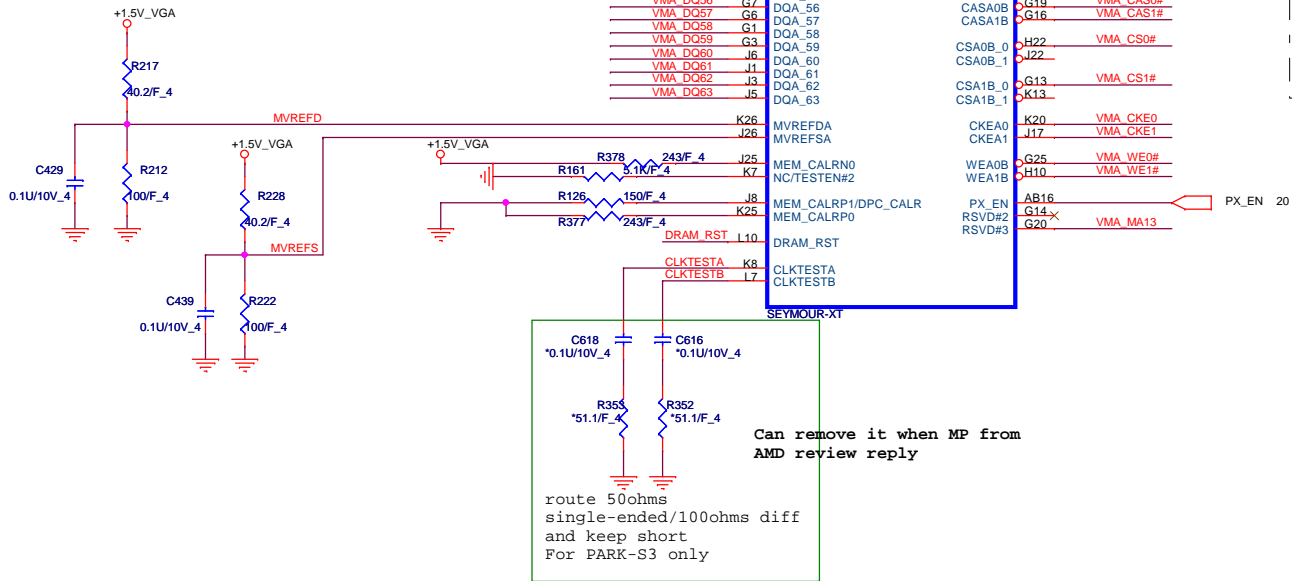
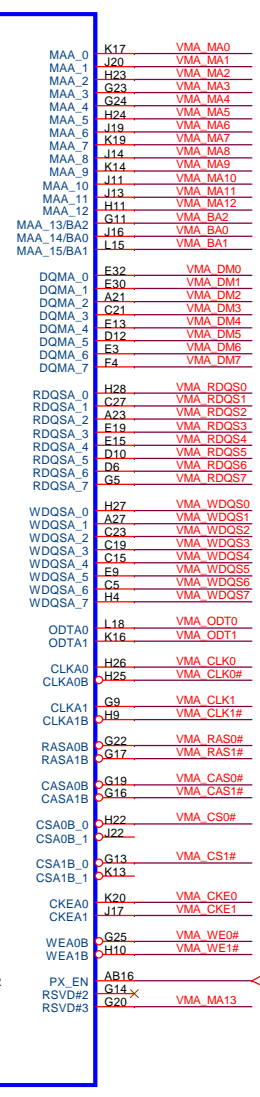




support 1gbt
VRAM (64M X 16)



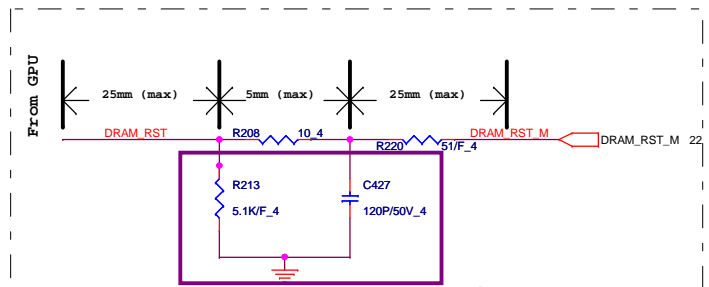
MEMORY INTERFACE



SEYMOUR-XT

Can remove it when MP from
AMD review reply

route 50ohms
single-ended/100ohms diff
and keep short
For PARK-S3 only



DB to SI : R213 & C427 exchange

Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

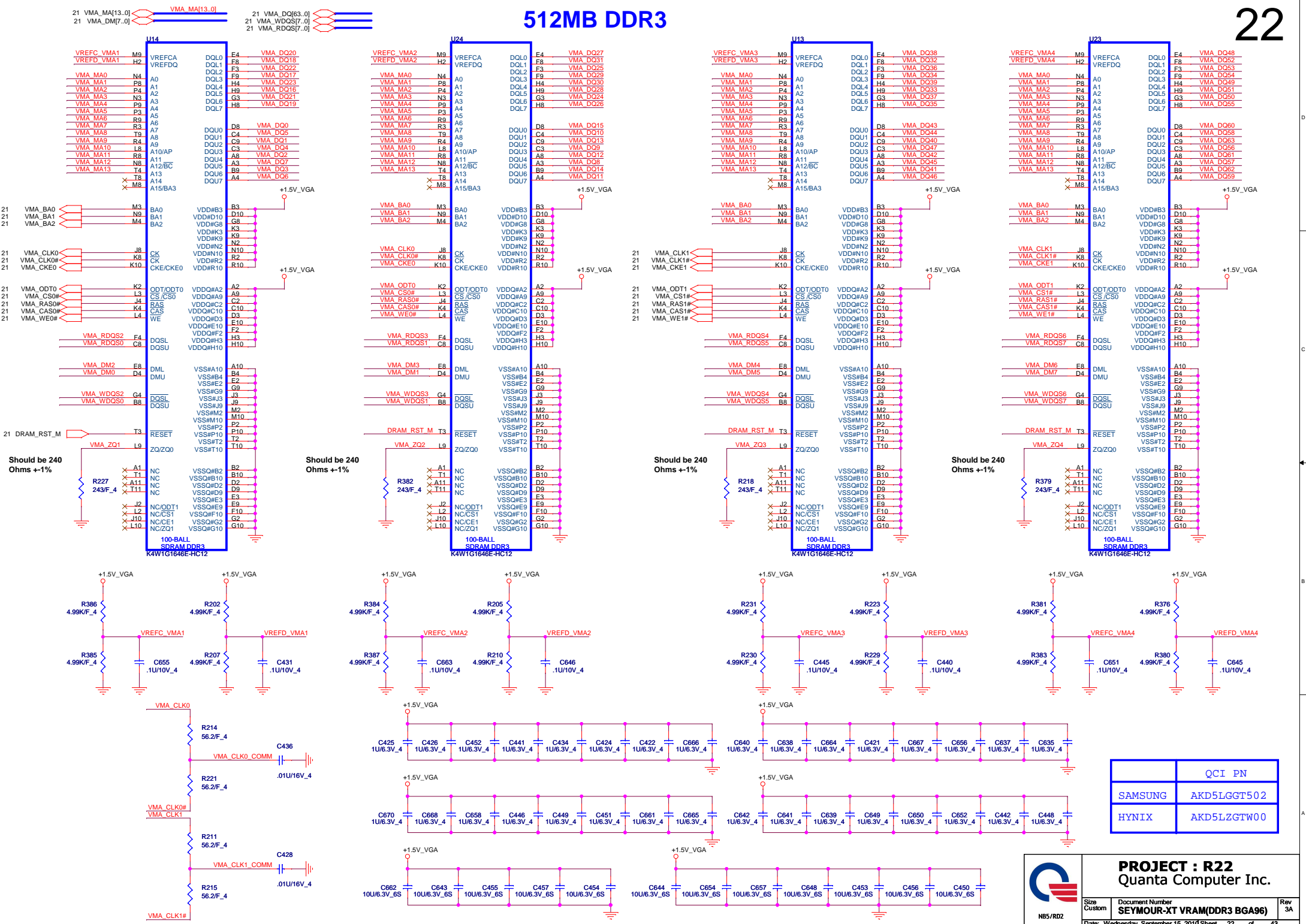
This basic topology should be used for DRAM_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.



PROJECT : R22
Quanta Computer Inc.

Size Custom	Document Number SEYMOUR-XT MEM Interface	Rev 1A
Date: Wednesday, September 15, 2010 Sheet 21 of 43		

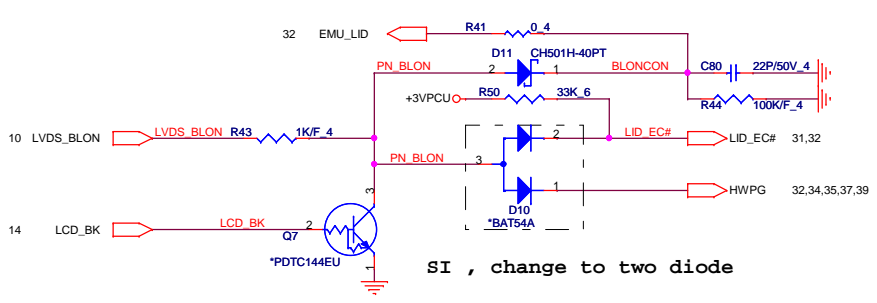
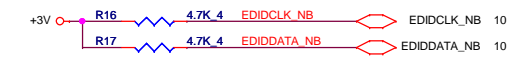
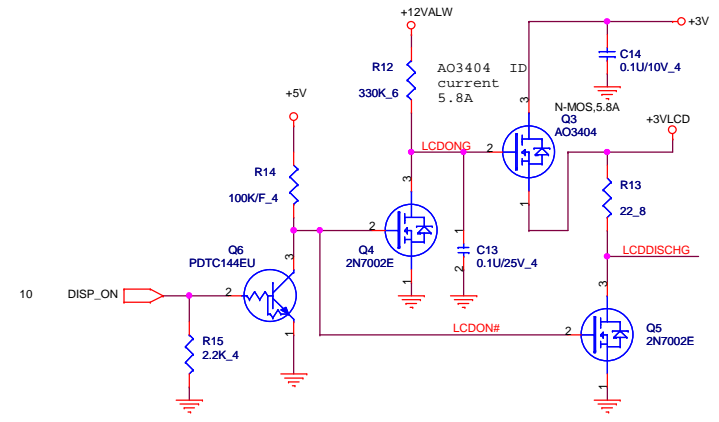
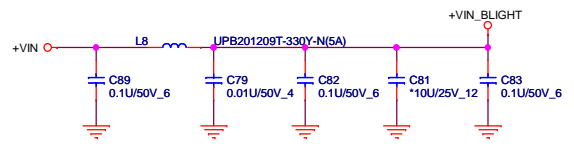
512MB DDR3



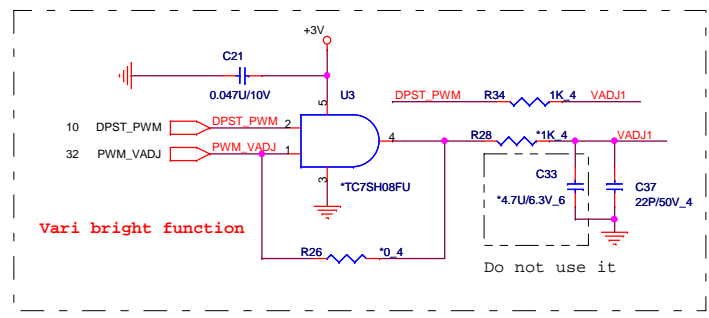
	QCI PN
SAMSUNG	AKD5LGGT502
HYNIX	AKD5LZGTW00



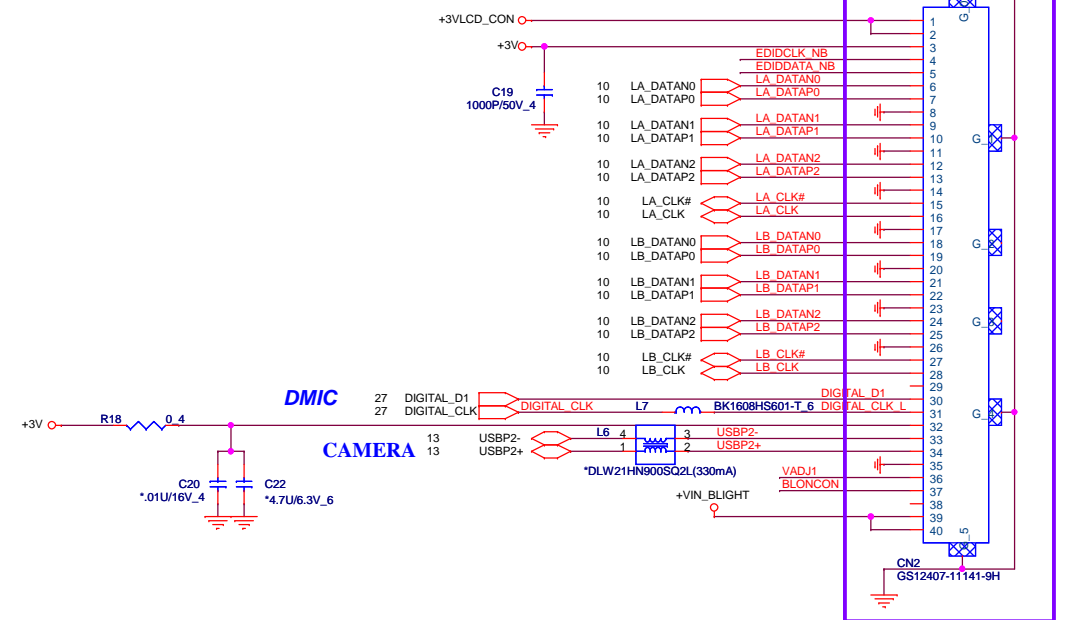
PROJECT : R22
Quanta Computer Inc.



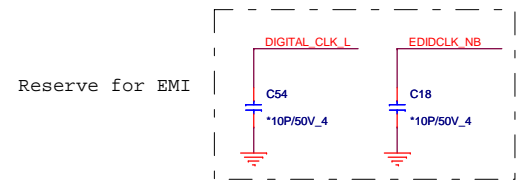
SI , change to two diode



Do not use it



CN2 Change PN DFHS40FS036



Reserve for EMI



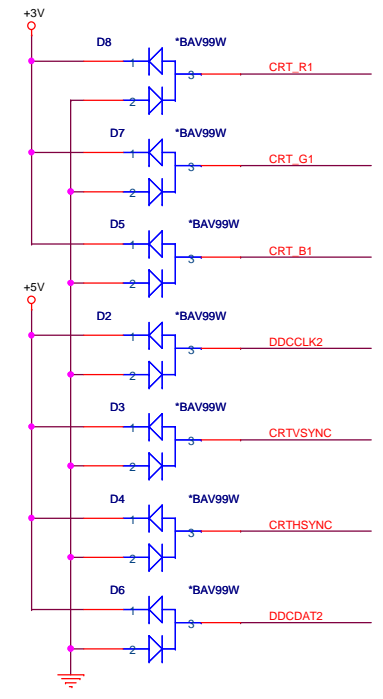
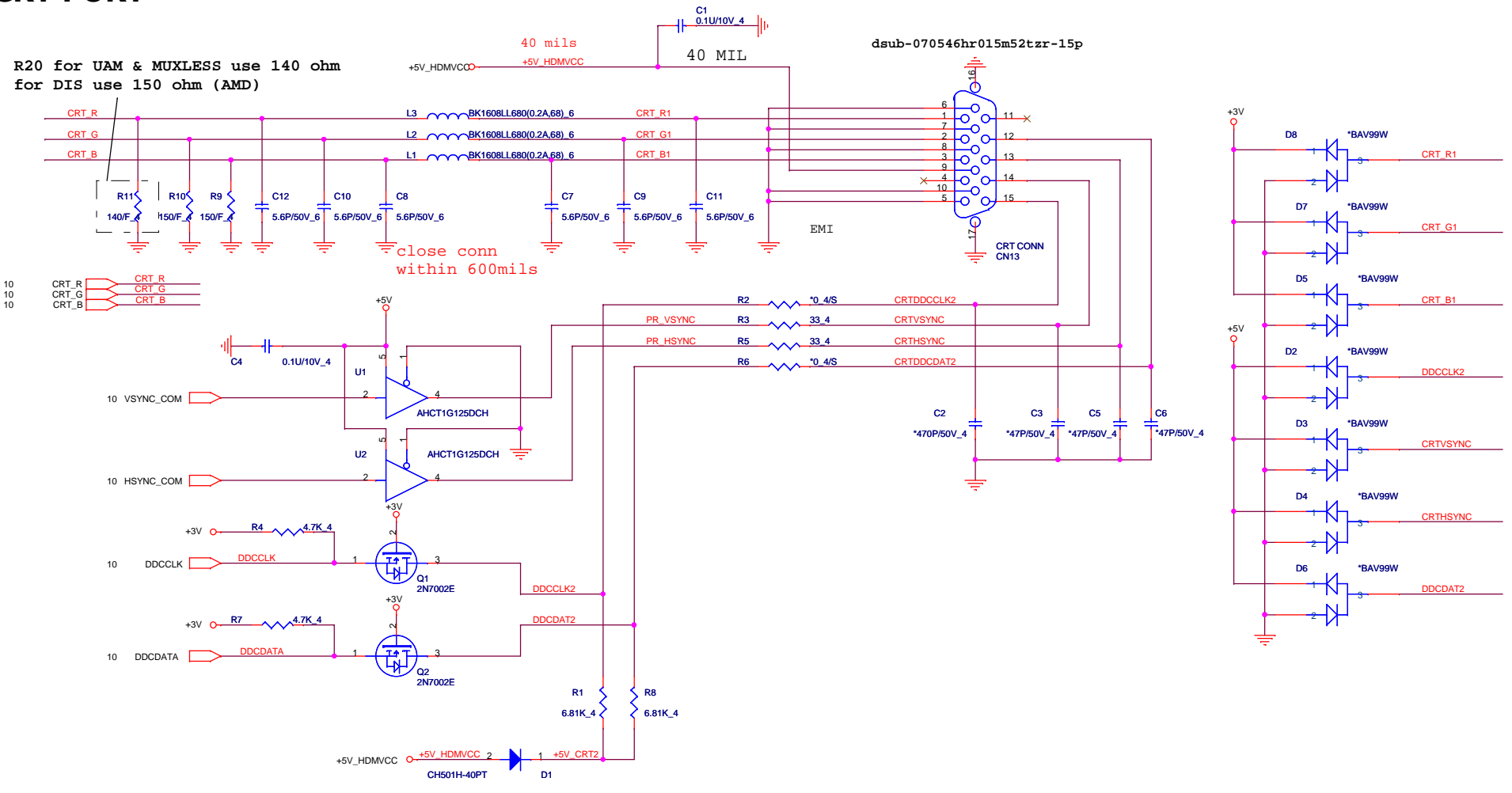
PROJECT : R22
Quanta Computer Inc.

Size Custom	Document Number LCD CONN	Rev 1A
Date: Wednesday, September 15, 2010 Sheet 23 of 43		

NB5/RD2

CRT PORT

R20 for UAM & MUXLESS use 140 ohm
for DIS use 150 ohm (AMD)



PROJECT : R22
Quanta Computer Inc.

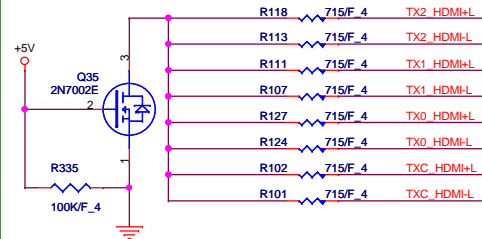
Size Custom	Document Number CRT	Rev 1A
Date: Wednesday, September 15, 2010 Sheet 24 of 43		

UMA/DISCRETE select for HDMI

From RS880M

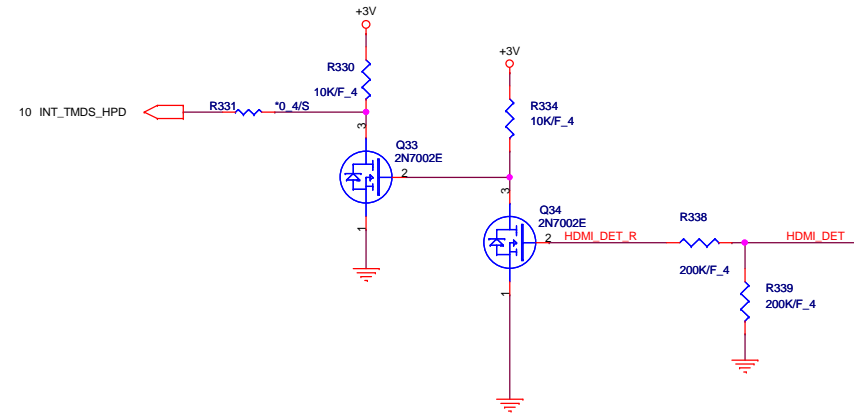
for Layout concern
,placement close
north bridge

9	C_PEG_TX15	C_PEG_TX15	C625	0.1U/10V_4	TX2_HDMI-L
9	C_PEG_TX#15	C_PEG_TX#15	C626	0.1U/10V_4	TX2_HDMI+L
9	C_PEG_TX14	C_PEG_TX14	C623	0.1U/10V_4	TX1_HDMI-L
9	C_PEG_TX#14	C_PEG_TX#14	C624	0.1U/10V_4	TX1_HDMI+L
9	C_PEG_TX#13	C_PEG_TX#13	C620	0.1U/10V_4	TX0_HDMI-L
9	C_PEG_TX13	C_PEG_TX13	C622	0.1U/10V_4	TX0_HDMI+L
9	C_PEG_TX#12	C_PEG_TX#12	C615	0.1U/10V_4	TXC_HDMI-L
9	C_PEG_TX12	C_PEG_TX12	C617	0.1U/10V_4	TXC_HDMI+L

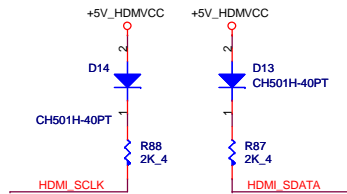


Close to HDMI Connector

HDMI HPD SENSE



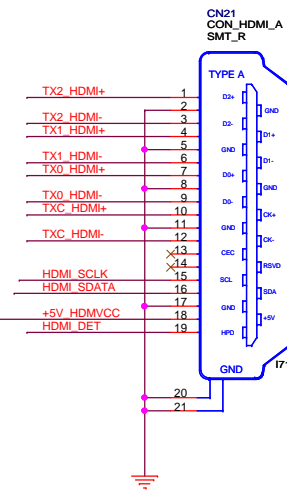
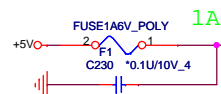
HDMI Connector



Add for EMI debug

TX2_HDMI-L	RP6	3	4	0_4P2R_4	TX2_HDMI-
TX2_HDMI+L	RP6	1	2	0_4P2R_4	TX2_HDMI+
TX1_HDMI-L	RP5	3	4	0_4P2R_4	TX1_HDMI-
TX1_HDMI+L	RP5	1	2	0_4P2R_4	TX1_HDMI+
TX0_HDMI-L	RP7	3	4	0_4P2R_4	TX0_HDMI-
TX0_HDMI+L	RP7	1	2	0_4P2R_4	TX0_HDMI+
TXC_HDMI-L	RP4	3	4	0_4P2R_4	TXC_HDMI-
TXC_HDMI+L	RP4	1	2	0_4P2R_4	TXC_HDMI+

Need add nearby HDMI CONN



hdmi-100042mr019s172z1-19p-v

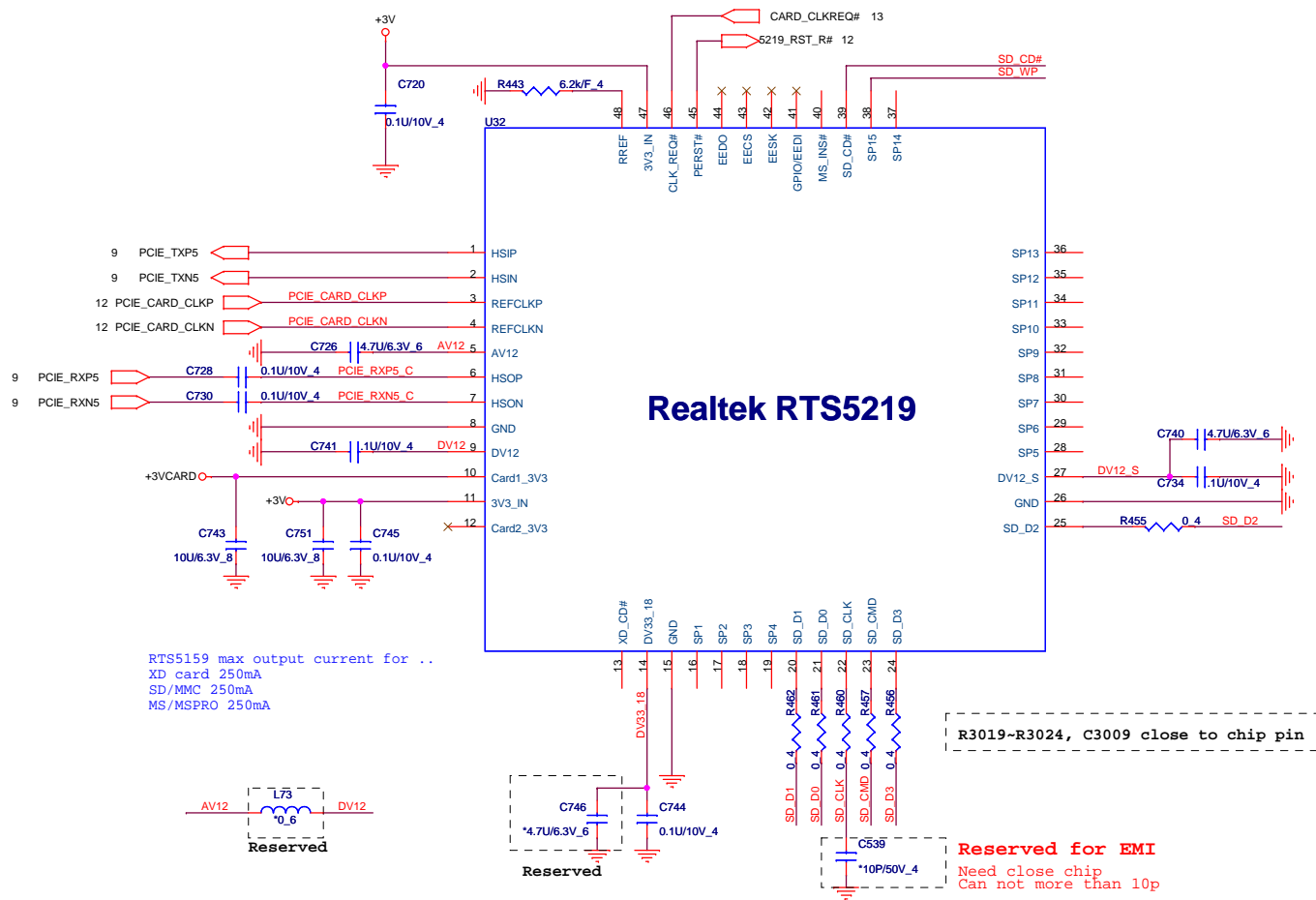
UMA HDMI I2C SELECT

Close to HDMI Connector

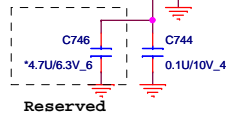
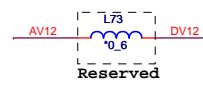


PROJECT : R22
Quanta Computer Inc.

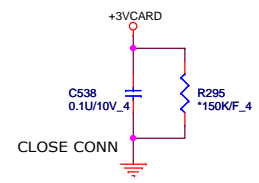
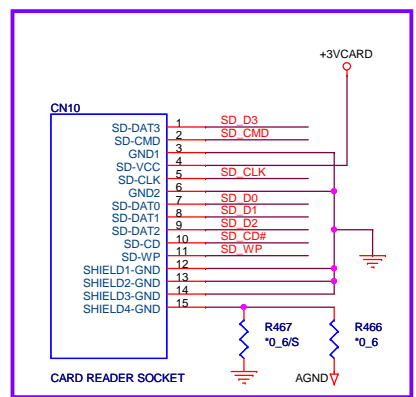
Size Custom	Document Number NBS/RD2	Rev 1A
Date: Wednesday, September 15, 2010 Sheet 25 of 43		




RTS5159 max output current for ...
 XD card 250mA
 SD/MMC 250mA
 MS/MSPRO 250mA



Reserved for EMI
 Need close chip
 Can not more than 10p



DB to SI Change Footprint to SDCARD-CS1S-038-11P-SMT For SMT issue

	PROJECT : R22 Quanta Computer Inc.	
	Size Custom NBS/RD2	Document Number RTS5219 & CR SOCKET
Date: Wednesday, September 15, 2010 Sheet 26 of 43		

3,5,6,7,10,11,12,13,14,15,16,20,23,24,25,26,28,29,30,31,32,33,38,39 +3V
 +4.75VAVDD
 5,20,23,24,25,28,29,31,33,39 +5V

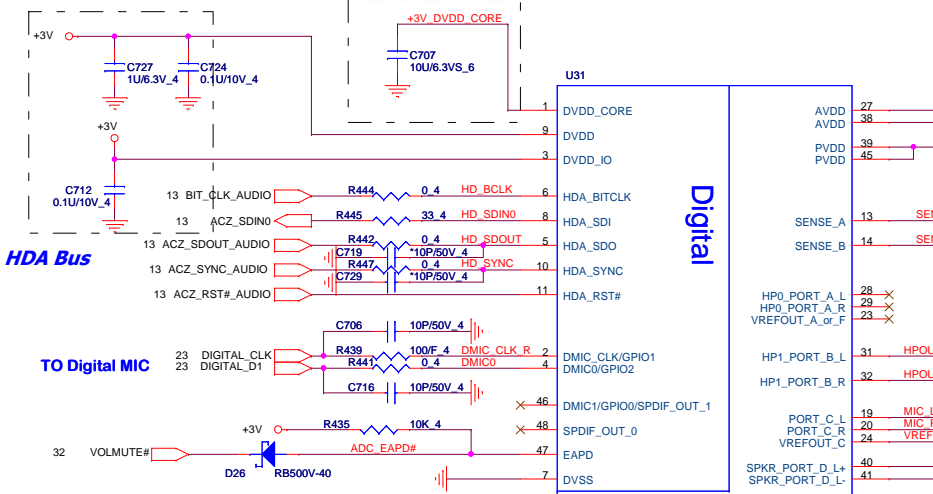
Close to CODEC

Close to CODEC

>40mils trace

Close to CODEC

Close to CODEC



HDA Bus

Digital

TO Digital MIC

TO Internal Speakers

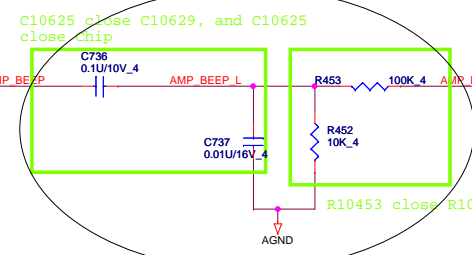
TO Headphone jack

TO Audio Jack MIC

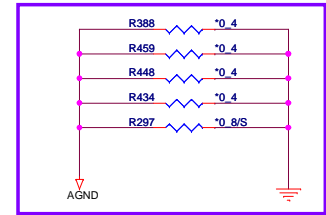
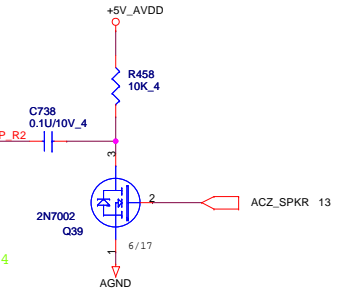
Close to CODEC

Analog

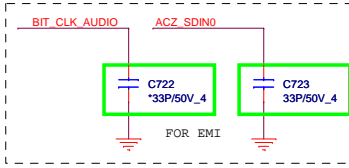
TO Internal Speakers



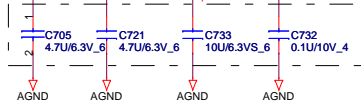
Check layout mount location



DB to SI : Reverse For EMI & ESD



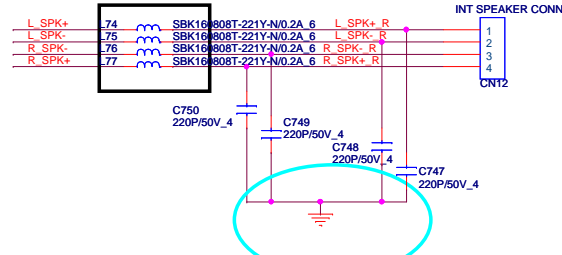
SI , check BIT_CLK_AUDIO double pull low




Close to CODEC

EMI Request

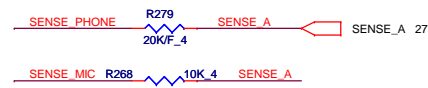
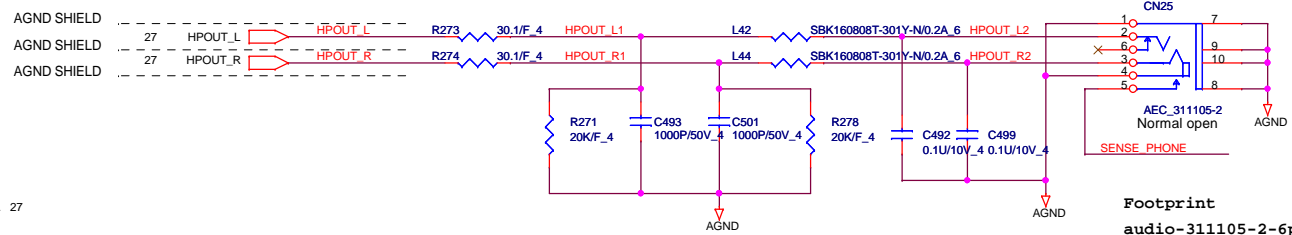
INT. SPEAKER



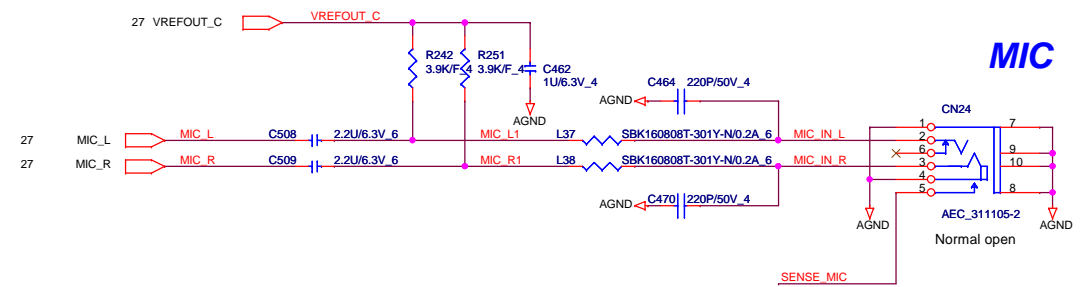
DB to SI : 9/14 for IDT recommend

			PROJECT : R22 Quanta Computer Inc.	
NBS/RD2			Date: Wednesday, September 15, 2010 Sheet 27 of 43	

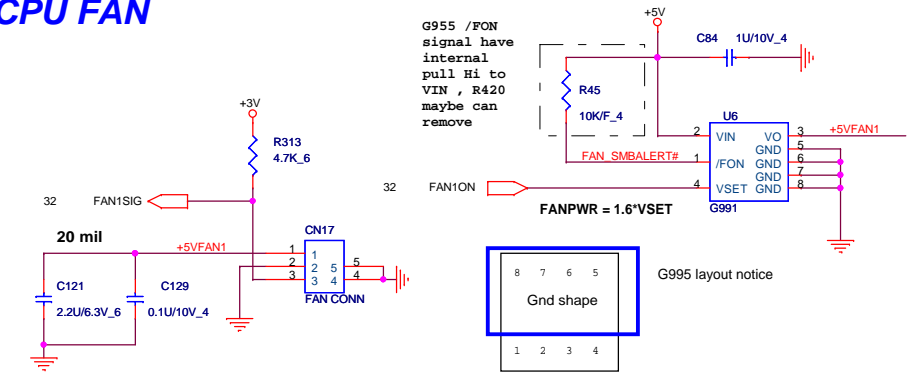
Line out



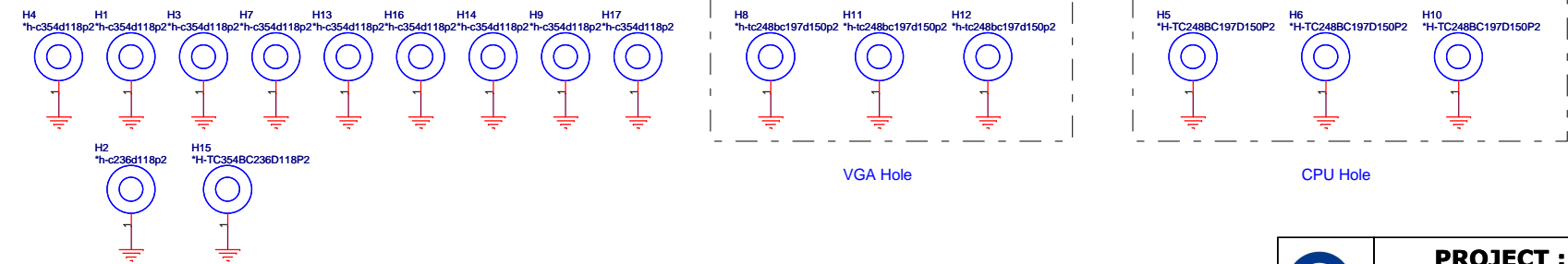
MIC



CPU FAN



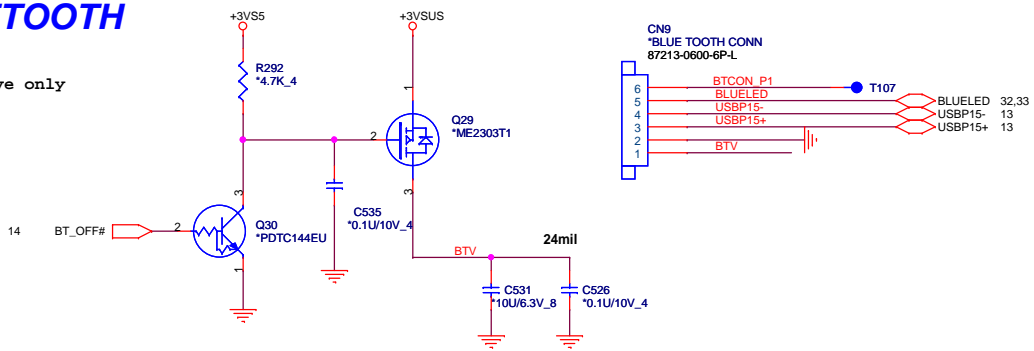
HOLE



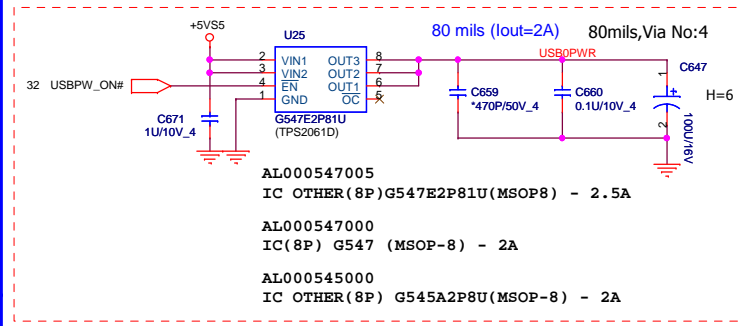
	PROJECT : R22 Quanta Computer Inc.	
	Size Custom Document Number AMP_TPA6017/CPU FAN/HOLE	Rev 1A
Date: Wednesday, September 15, 2010 Sheet 28 of 43		

BLUETOOTH

Reserve only

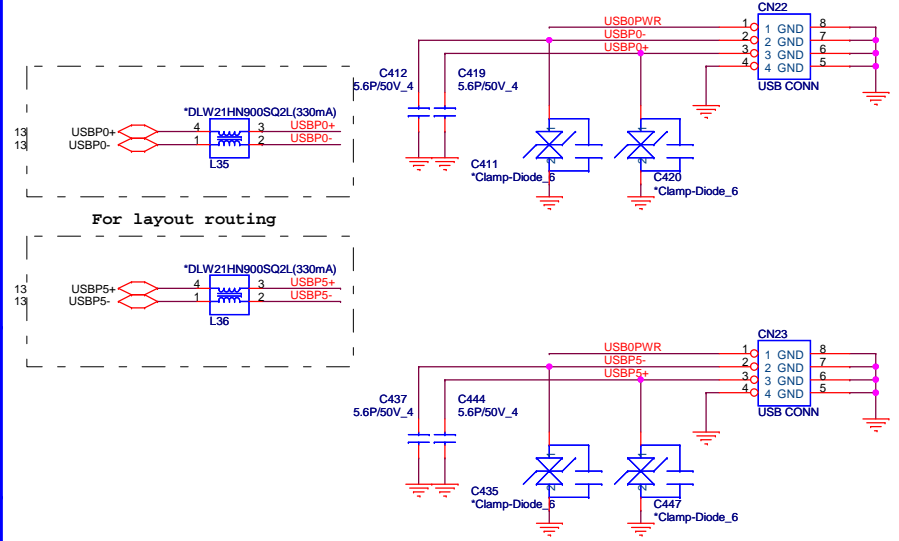
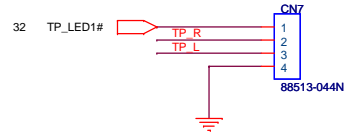
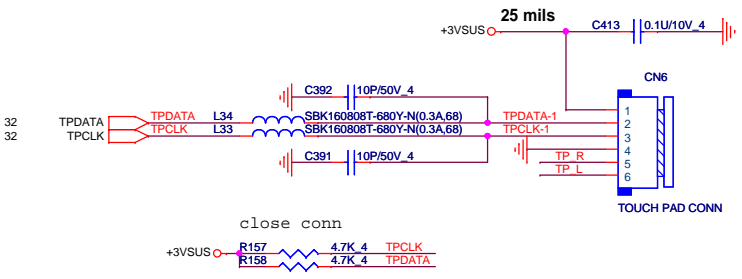


LEFT SIDE USBX2

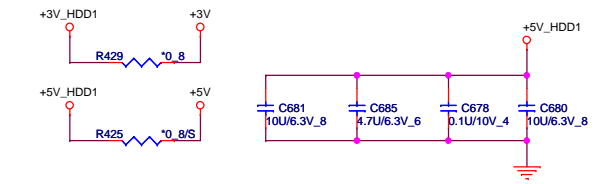
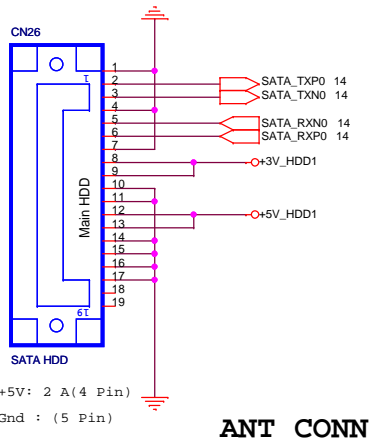


TOUCH PAD CONN

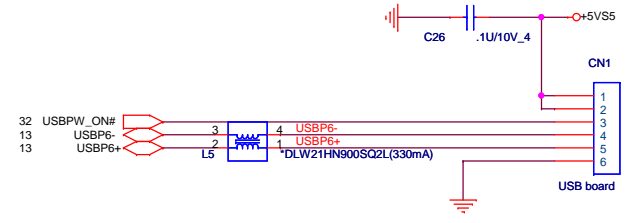
To TOUCH PAD SW board



SATA HDD CONNECTOR



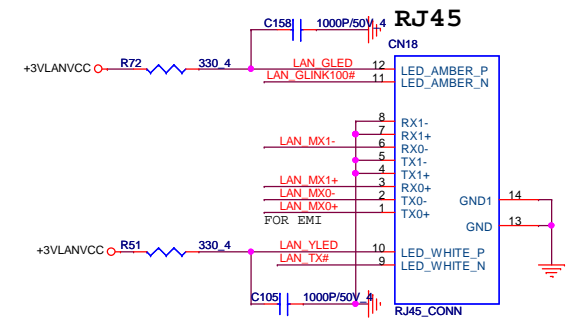
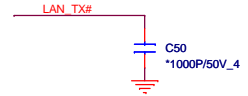
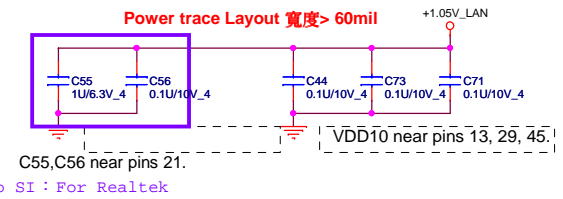
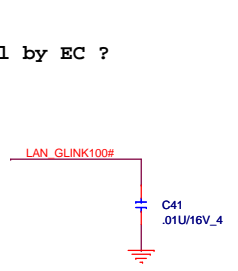
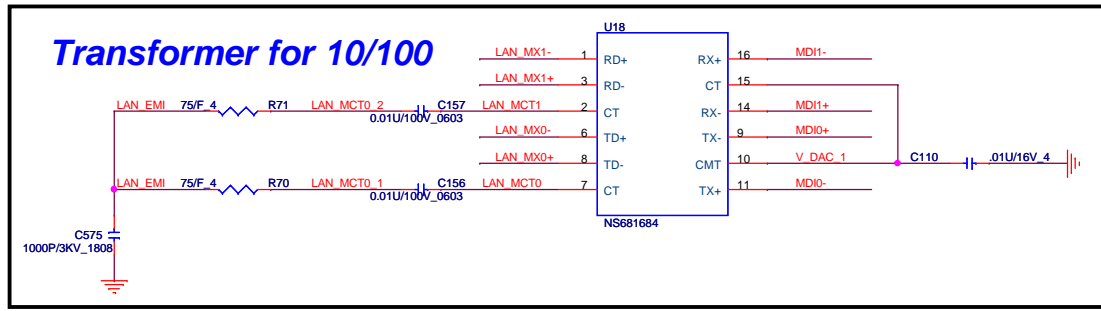
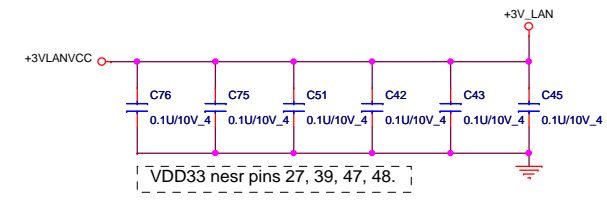
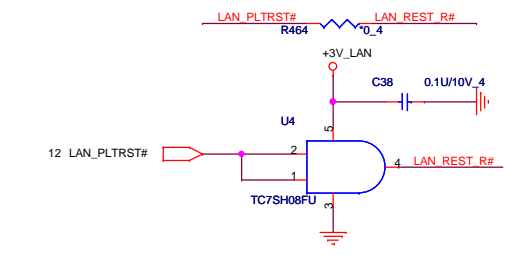
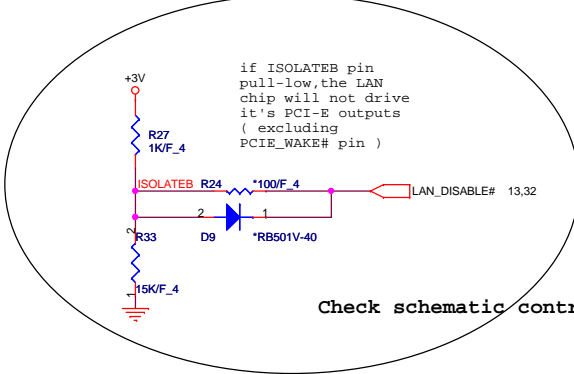
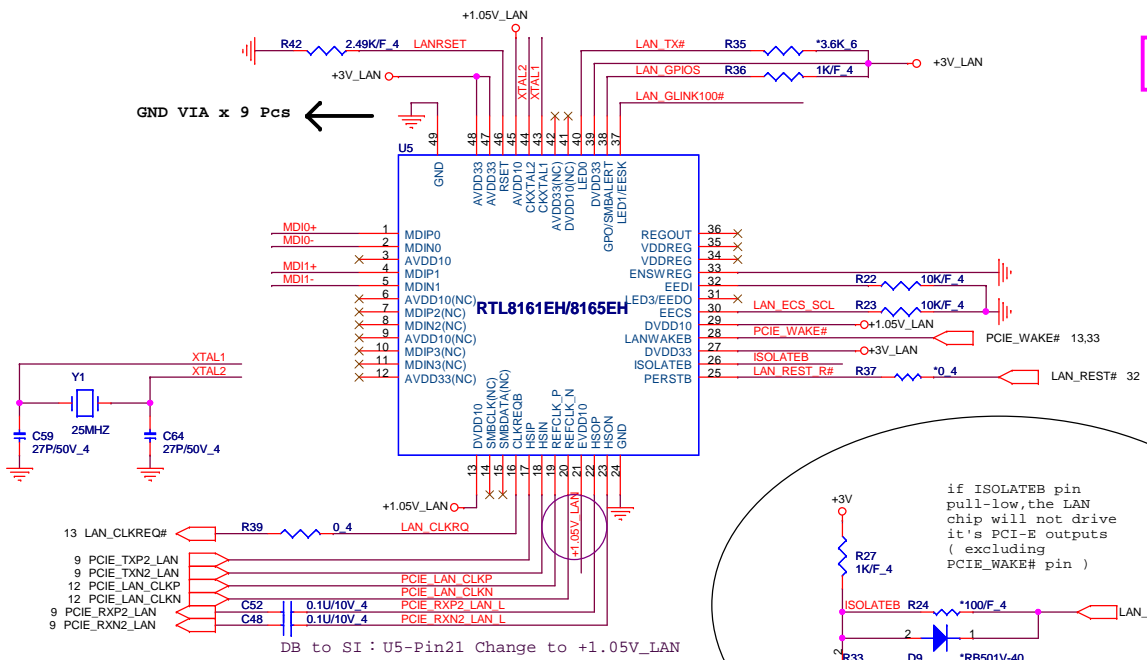
Right SIDE USBX1



PROJECT : R22
Quanta Computer Inc.

Size Custom	Document Number BT/USBX3/TP/HDD	Rev 1A
Date: Wednesday, September 15, 2010 Sheet 29 of 43		

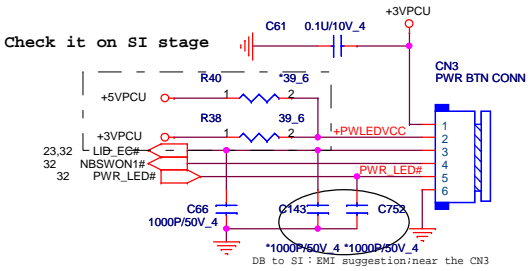
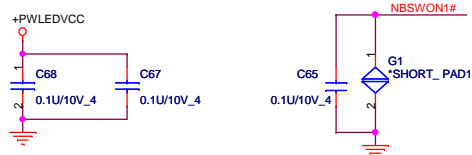
ANT CONN



Footprint : rj45-130452-u4-12p

	PROJECT : R22 Quanta Computer Inc.	
	Size Custom Document Number RTL8102EL/RJ45	Date: Wednesday, September 15, 2010 Sheet 30 of 43

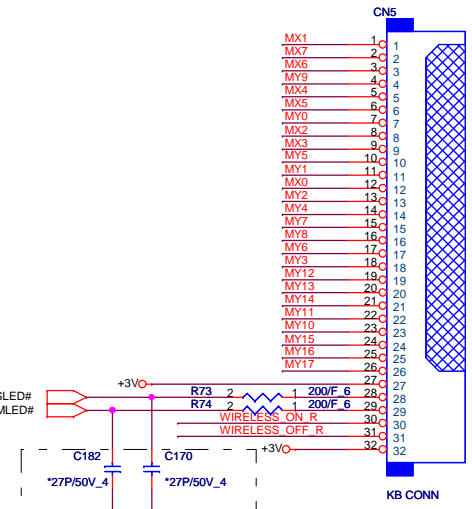
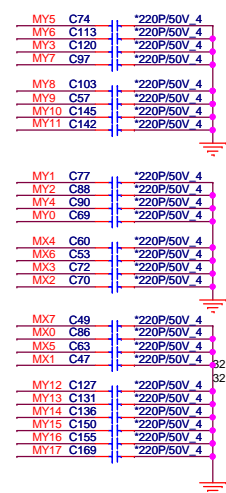
POWER BUTTON CONNECTOR



1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND

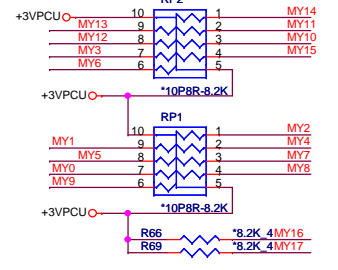
DB to SI : BNI suggestion: near the CN3

KEYBOARD CONN



Reserve for ESD

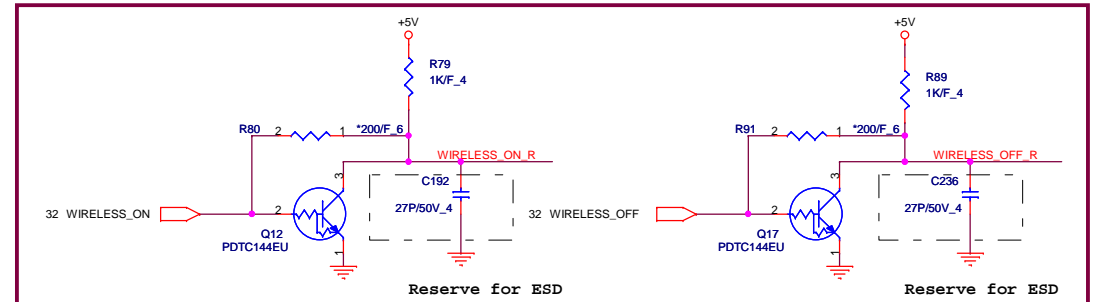
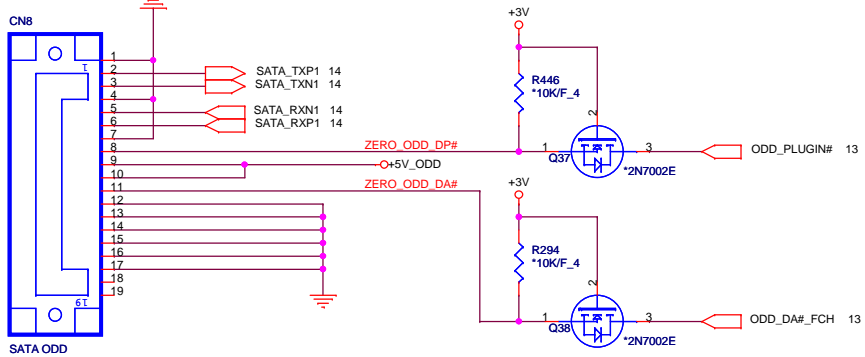
KEYBOARD PULL-UP



Reserve only

SATA CD-ROM

ANT CONN



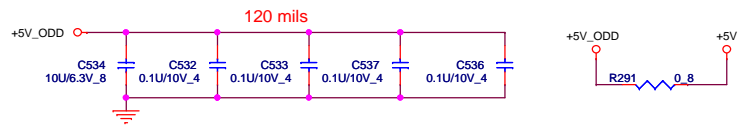
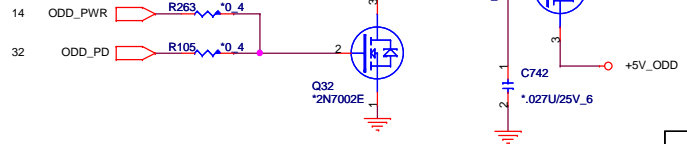
Reserve for ESD

Reserve for ESD

DB to SI : K/B RF LED Change

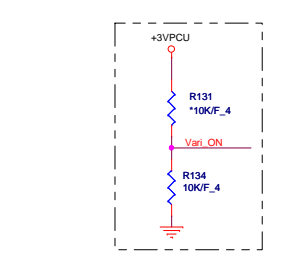
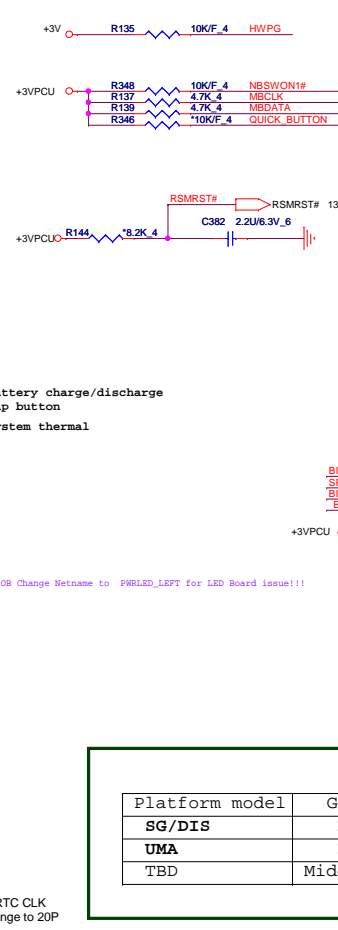
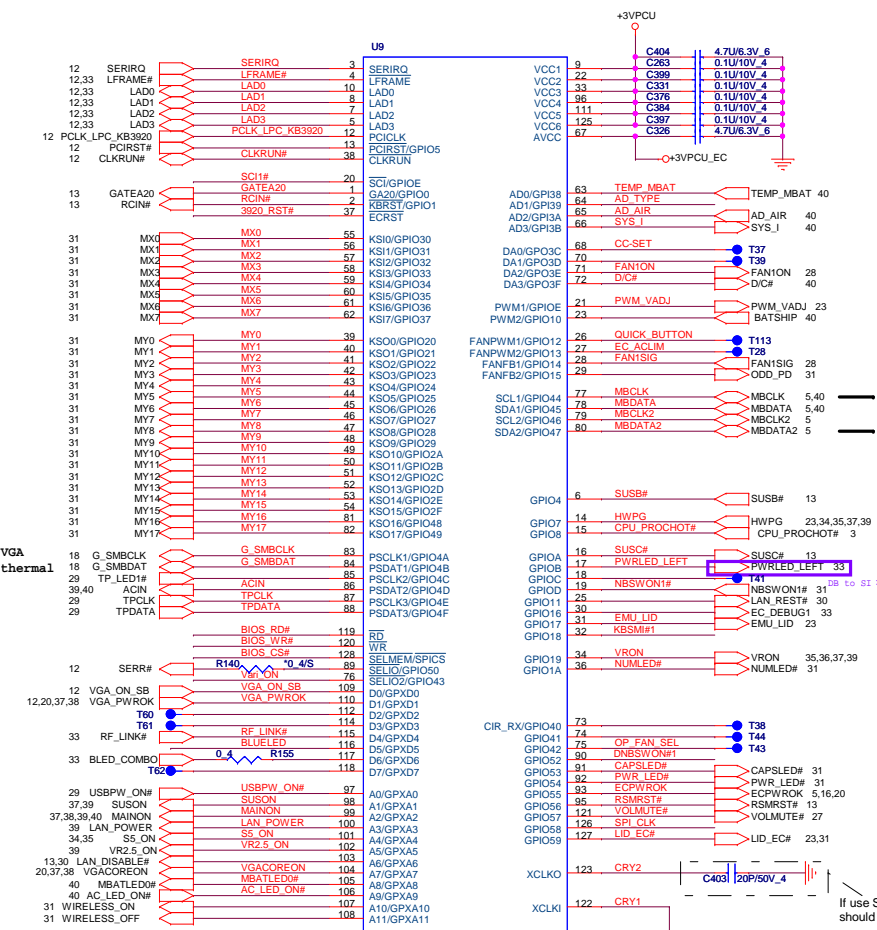
Zero Power ODD circuit

High : ODD power on
Low : ODD power down

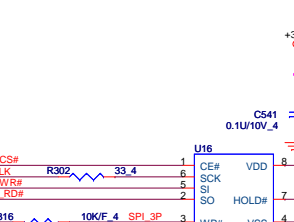


PROJECT : R22
Quanta Computer Inc.

Size Custom	Document Number KEYBOARD/SW_BOARD/ODD	Rev 1A
Date: Wednesday, September 15, 2010 Sheet 31 of 43		

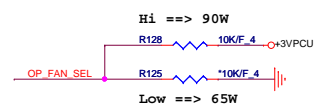


Enable Vari-bright need pull low

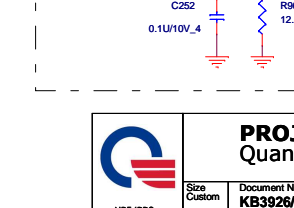
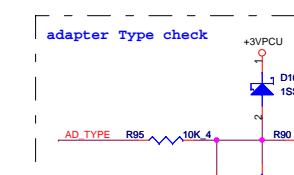
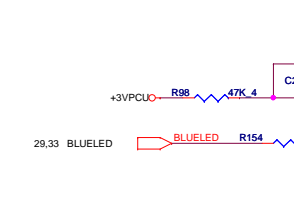
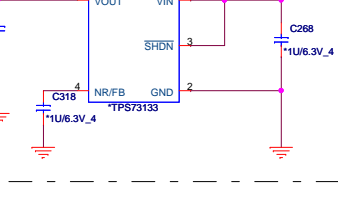
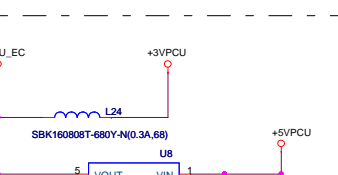
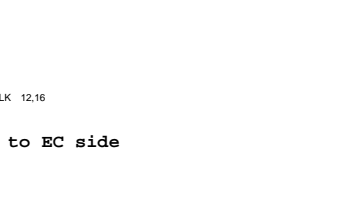
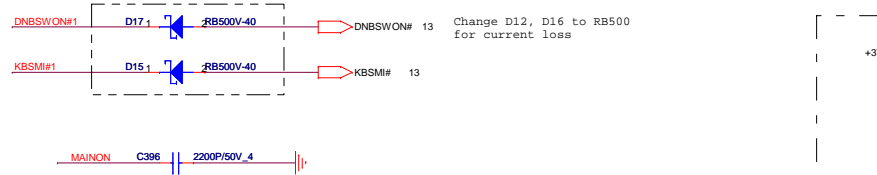
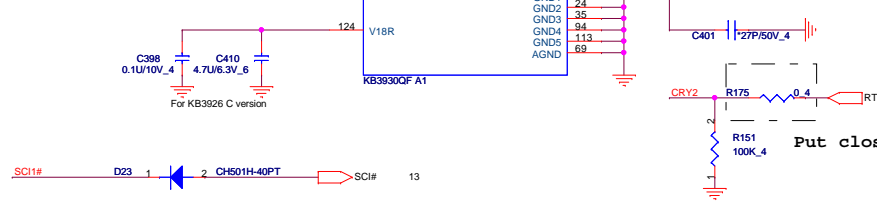


MAX AKE38FP0Z0 2M byte
WINBOND AKE38FP0N01 SPI
EON AKE38ZA0Q00 BIOS
SOCKET DFHS08FS023

Platform model	GPIO42
SG/DIS	High
UMA	Low
TBD	Middle (1.5V)

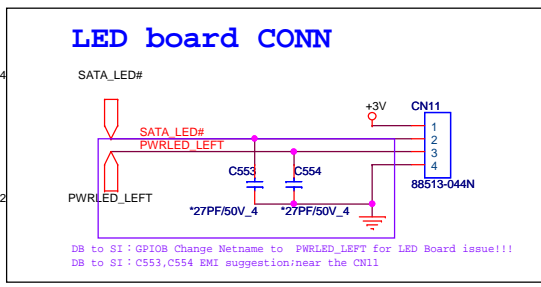
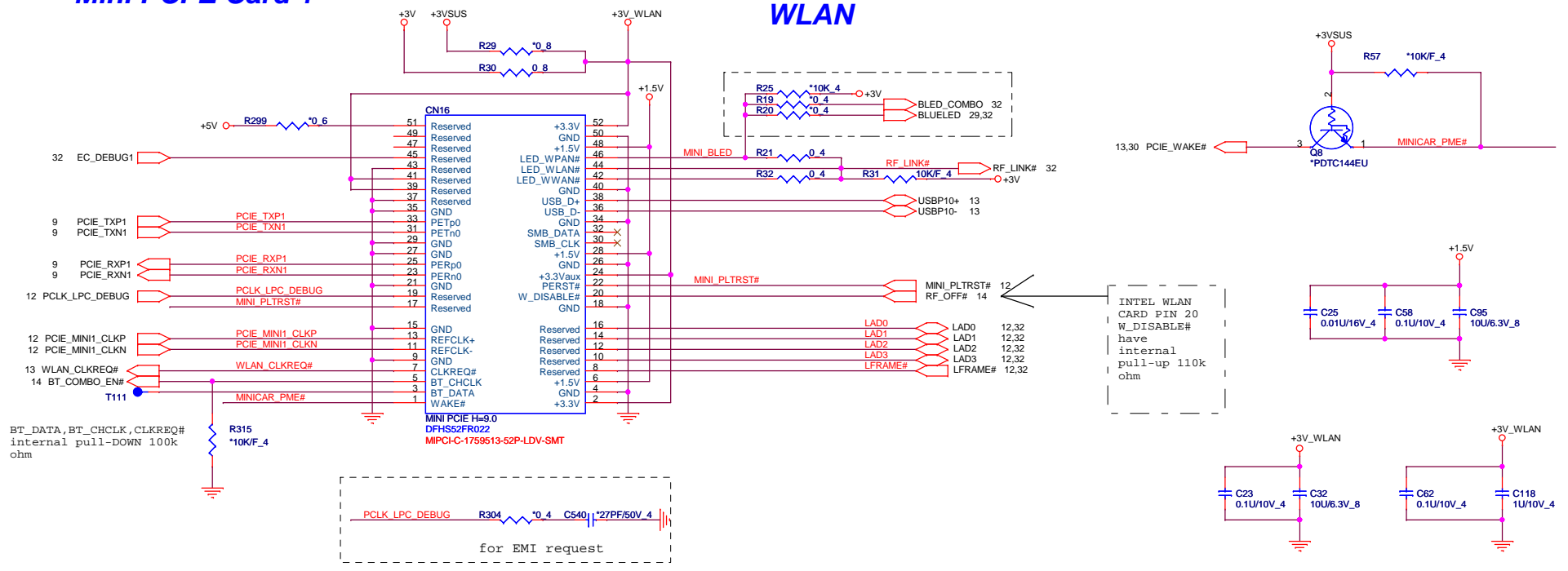


Hi ==> 90W
Low ==> 65W

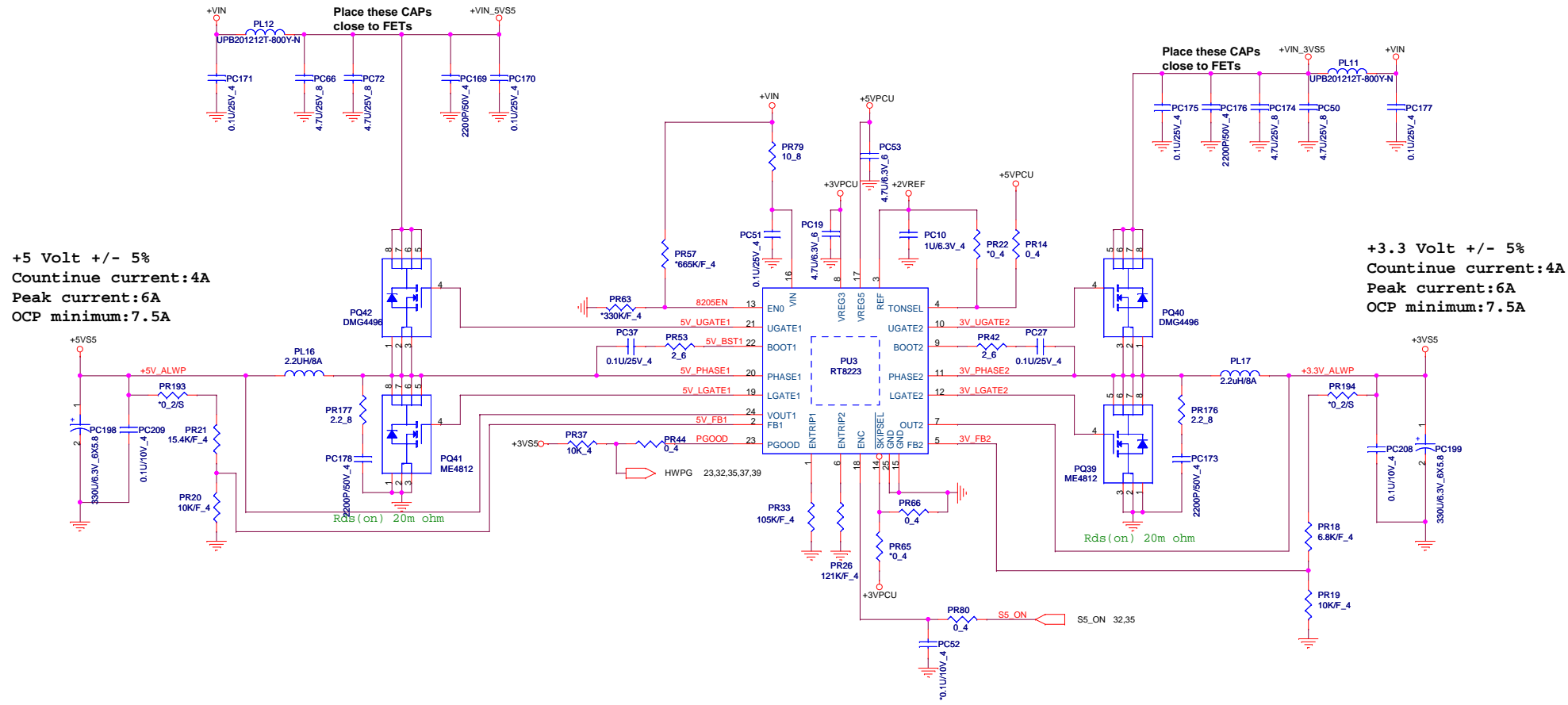


Mini PCI-E Card 1

WLAN




DC/DC +3VS5/+5VS5



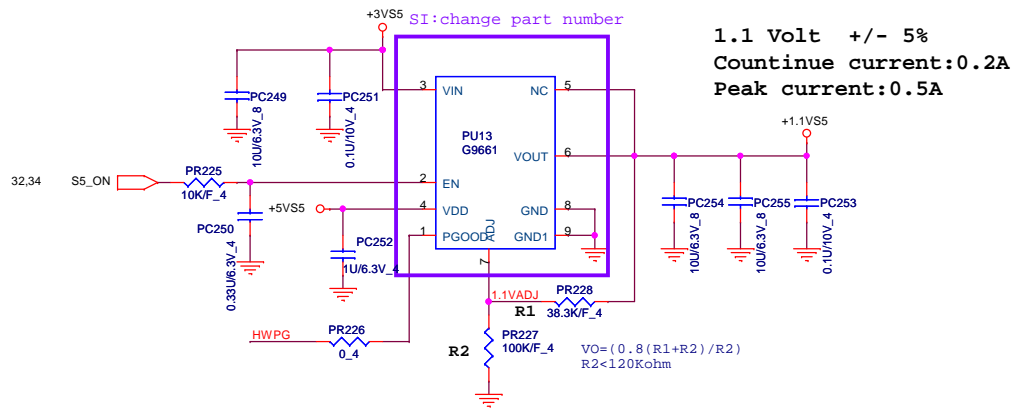
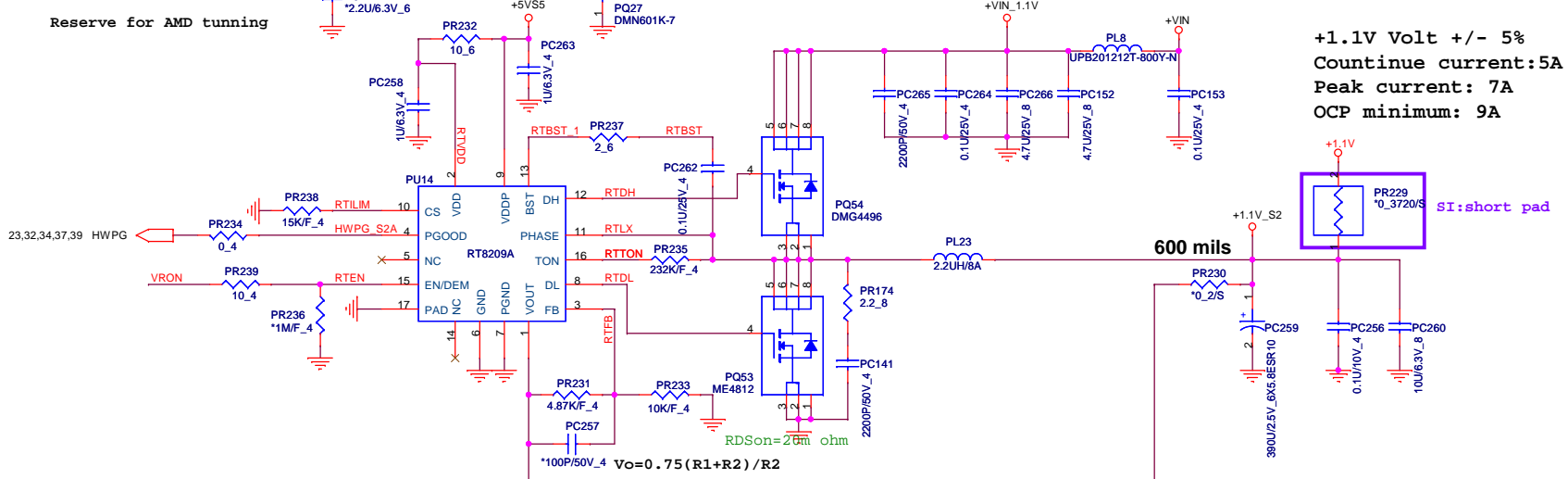
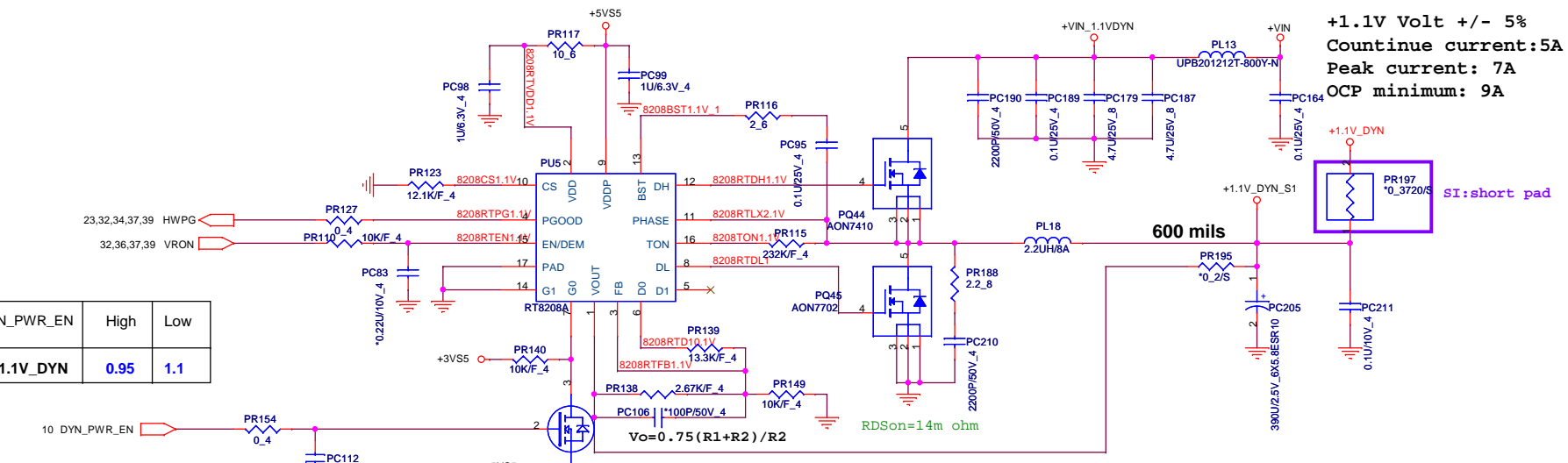
+5 Volt +/- 5%
 Countinue current:4A
 Peak current:6A
 OCP minimum:7.5A

+3.3 Volt +/- 5%
 Countinue current:4A
 Peak current:6A
 OCP minimum:7.5A

 PROJECT : R22 Quanta Computer Inc.		
Size Custom	Document Number +5V/+3V (RT8206B)	Rev 1A
Date: Wednesday, September 15, 2010 Sheet 34 of 43		

DYN_PWR_EN	High	Low
+1.1V_DYN	0.95	1.1

Reserve for AMD tuning



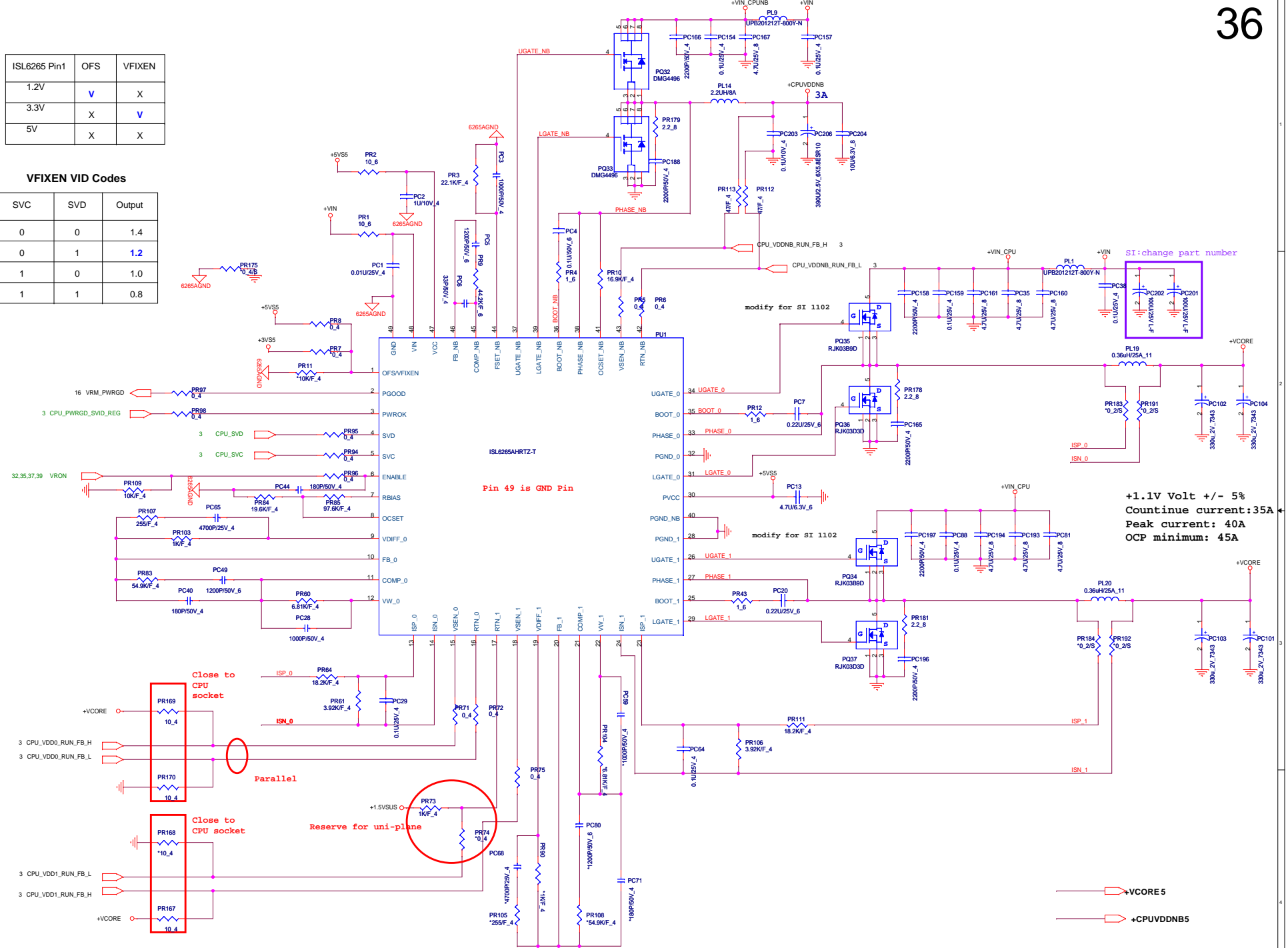
PROJECT : R22
Quanta Computer Inc.

Size Custom	Document Number VGA Core/4.1.8VGF/1.0VGF	Rev 1A
Date: Wednesday, September 15, 2010 Sheet 35 of 43		

ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

VFIXEN VID Codes

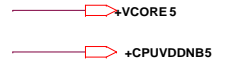
SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8

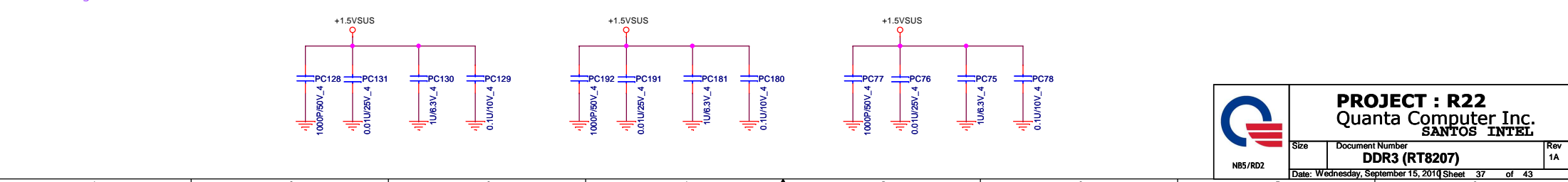
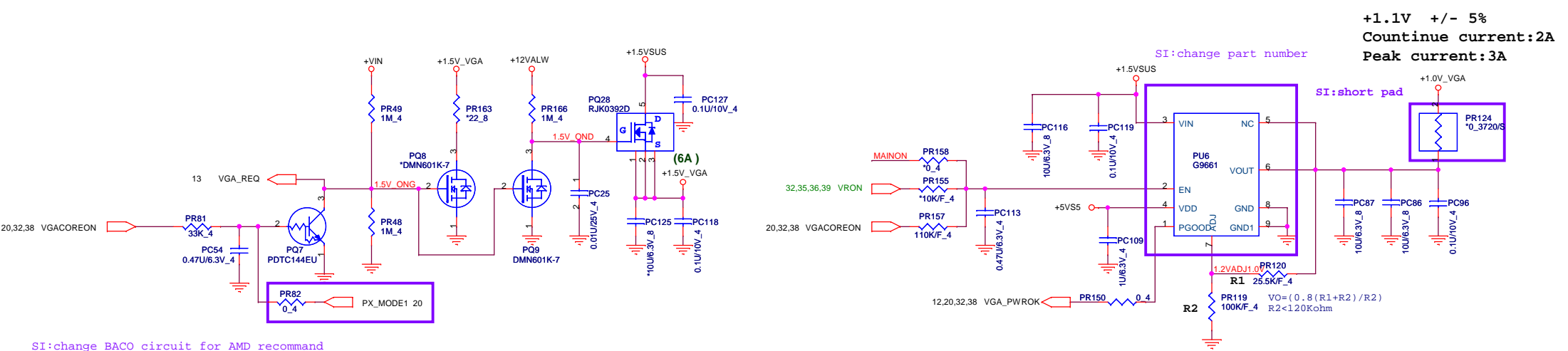
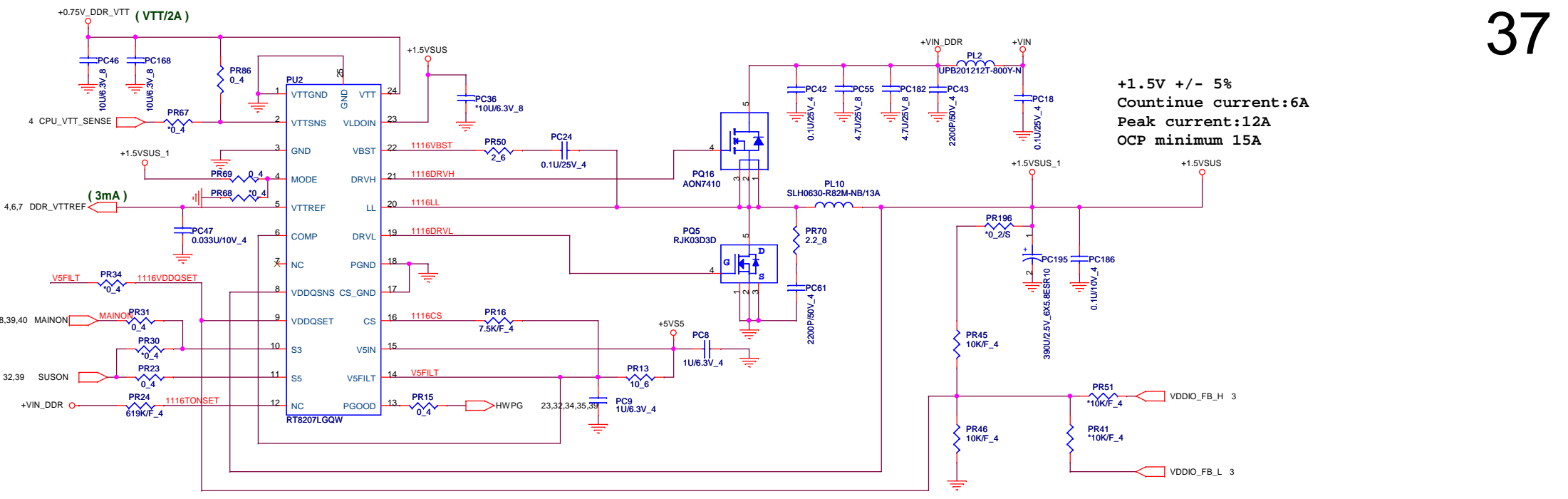


Pin 49 is GND Pin

+1.1V Volt +/- 5%
Continue current: 35A
Peak current: 40A
OCP minimum: 45A

Close to CPU socket
Parallel
Reserve for uni-plane

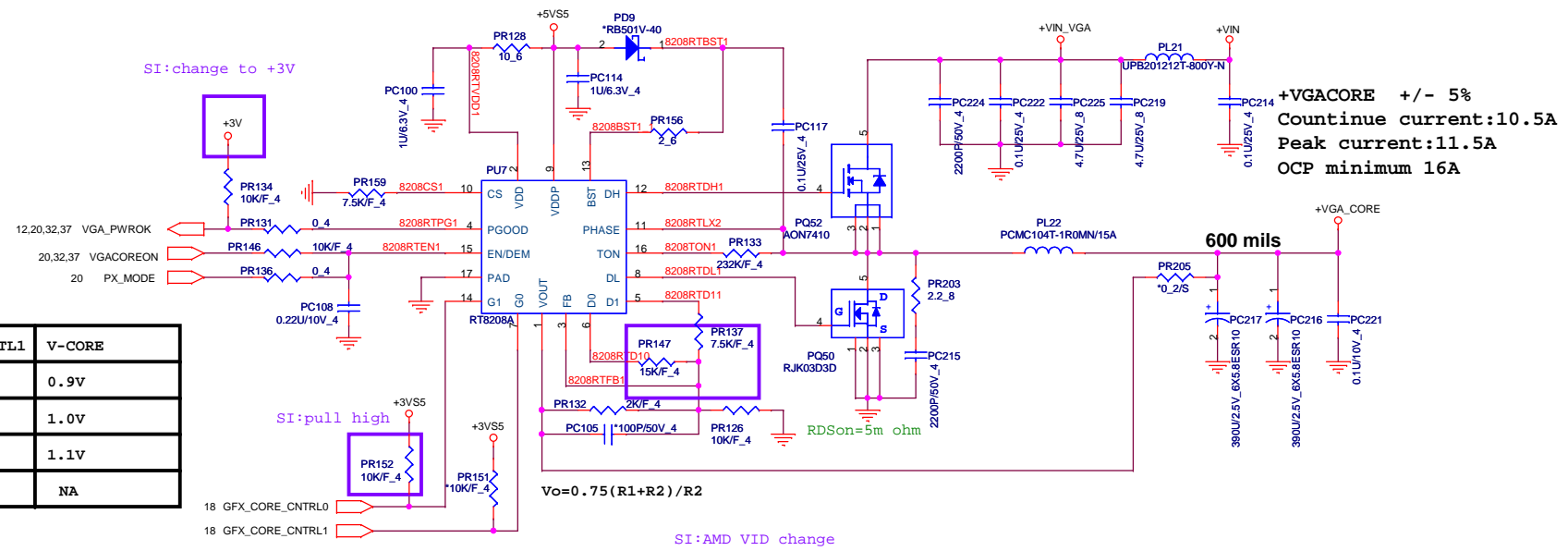




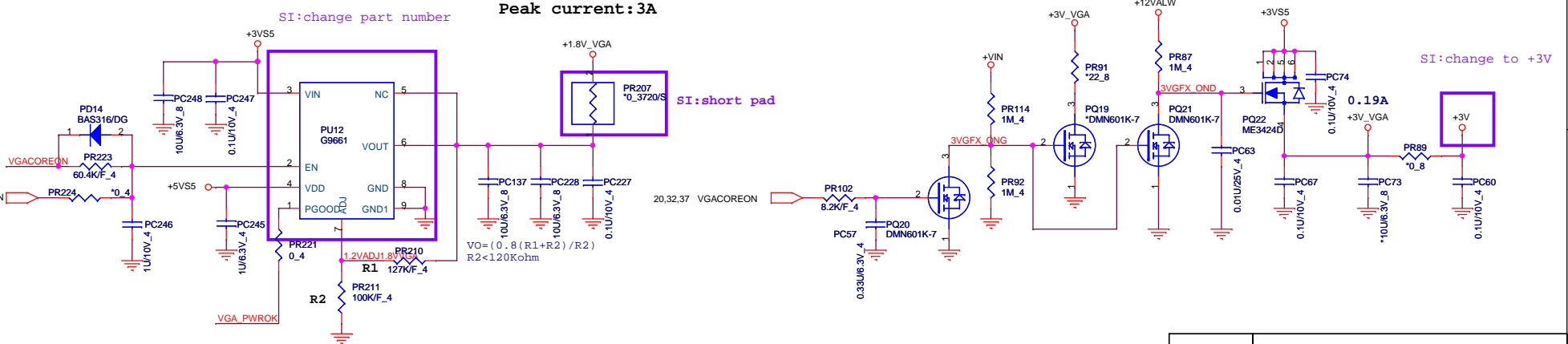
PROJECT : R22
Quanta Computer Inc.
SANTOS INTEL

Size	Document Number	Rev
NB5/RD2	DDR3 (RT8207)	1A
Date: Wednesday, September 15, 2010 Sheet 37 of 43		

Par-k-LP	PWRCNTL0	PWRCNTL1	V-CORE
L	0	0	0.9V
M	0	1	1.0V
H	1	0	1.1V
TBD	1	1	NA



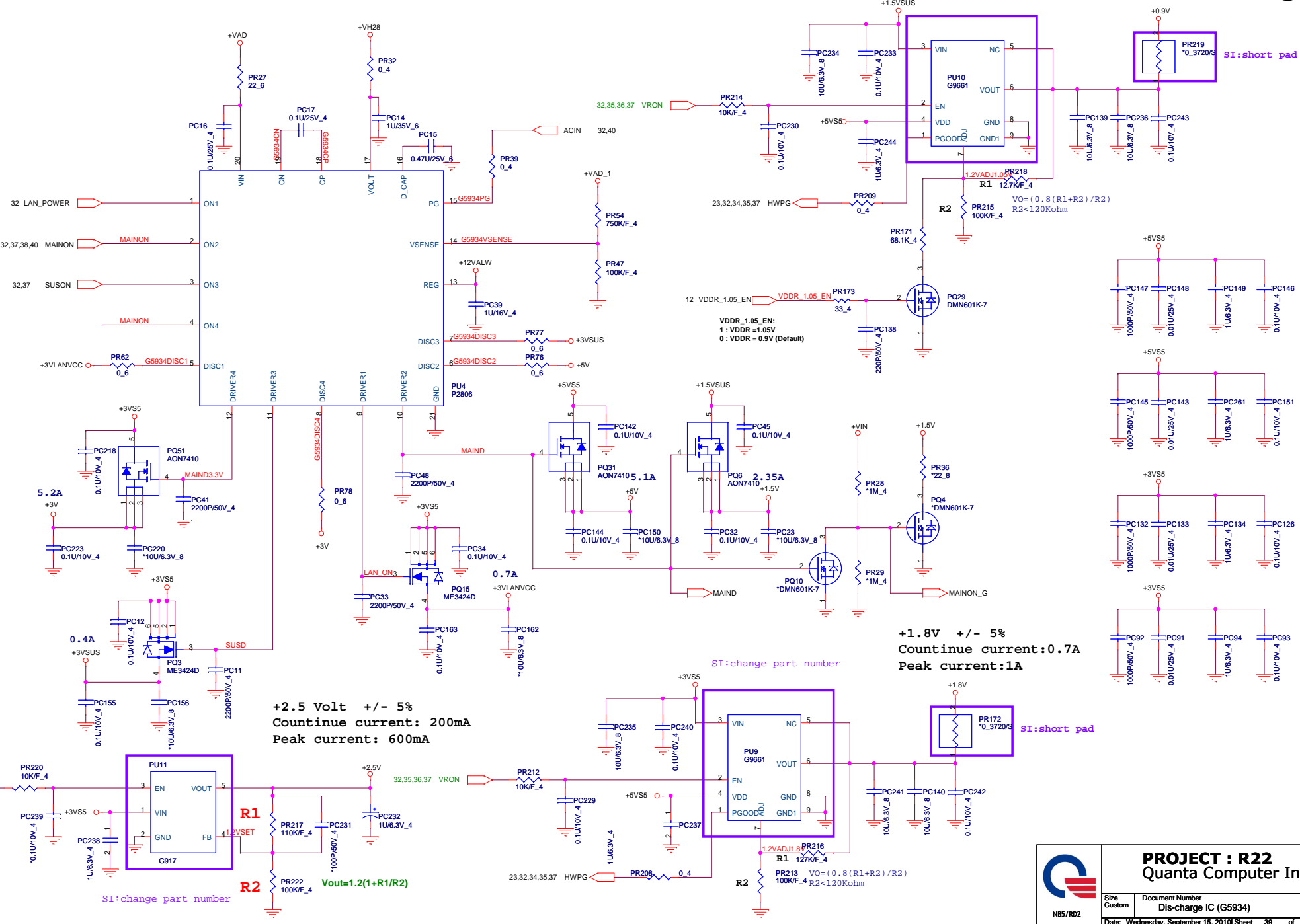
+1.8V +/- 5%
Continue current:1.2A
Peak current:3A



PROJECT : R22
Quanta Computer Inc.

+0.9V +/- 5%
Continue current: 1.5A
Peak current: 2A

39



+2.5 Volt +/- 5%
Continue current: 200mA
Peak current: 600mA

+1.8V +/- 5%
Continue current: 0.7A
Peak current: 1A

PROJECT : R22		
Quanta Computer Inc.		
Size Custom	Document Number Dis-charge IC (G5934)	Rev 1A
Date: Wednesday, September 15, 2010 Sheet 39 of 43		

D
C
B
A

D
C
B
A

SI-change part number & footprint

DC_JACK 90W

Place this ZVS close to Idea Diode

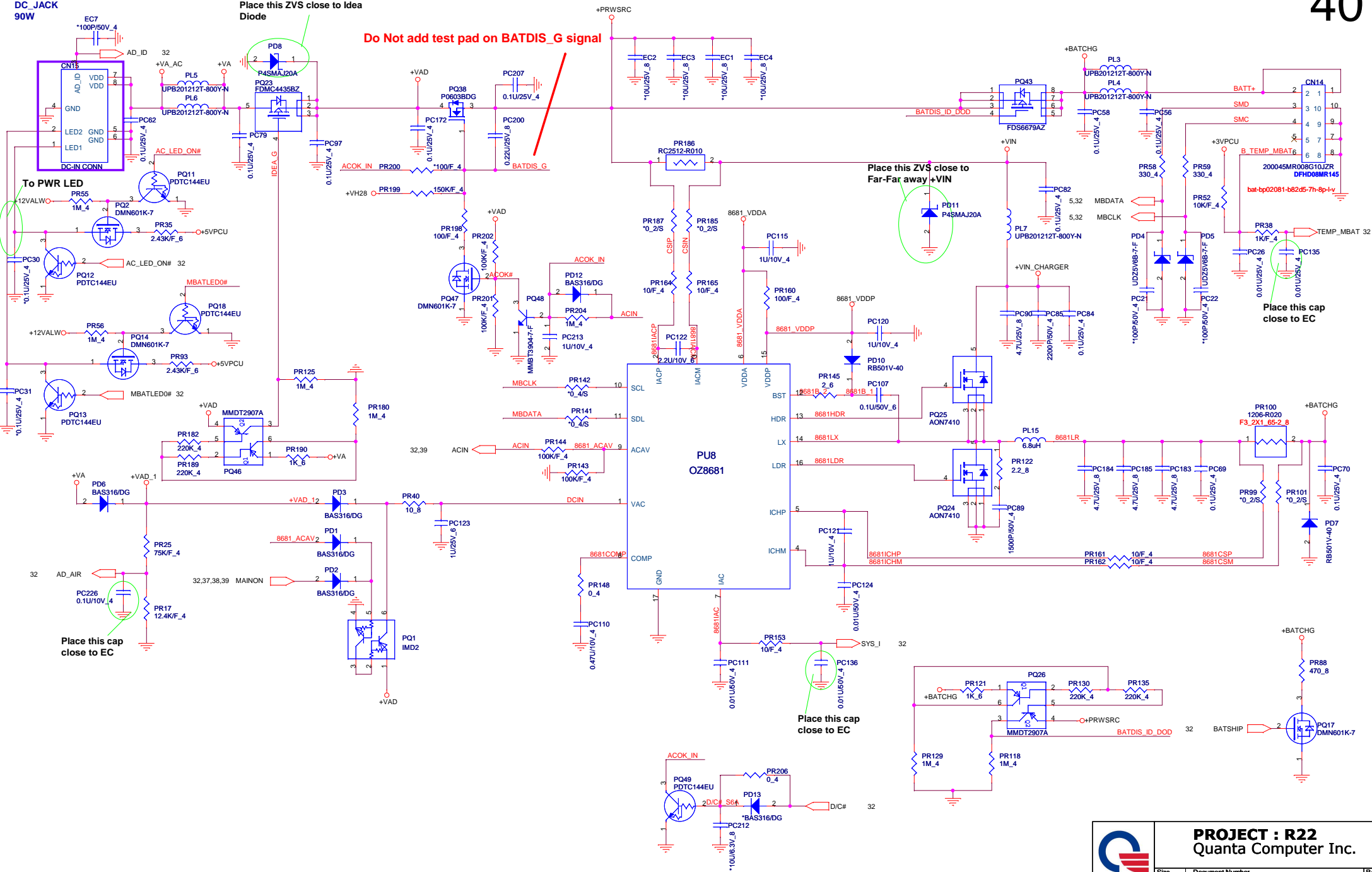
Do Not add test pad on BATDIS_G signal


Place this ZVS close to Far-Far away +VIN

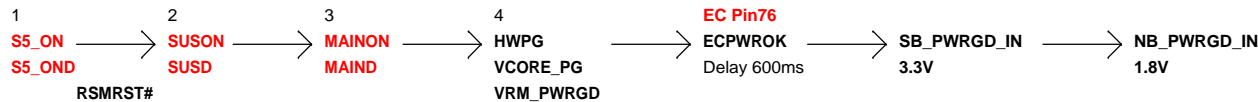
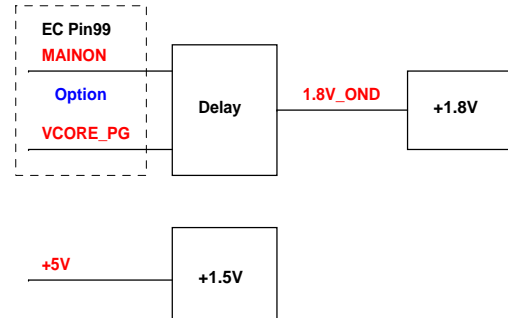
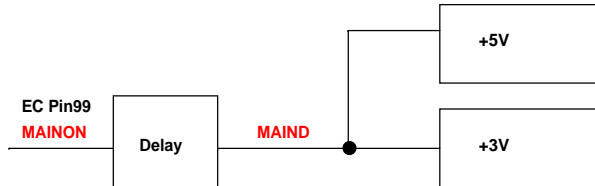
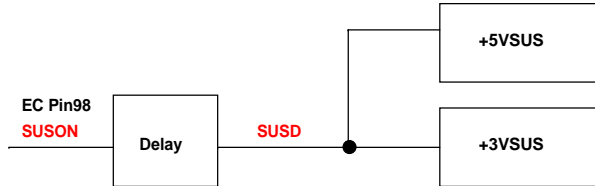
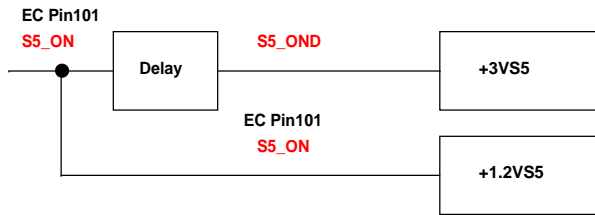
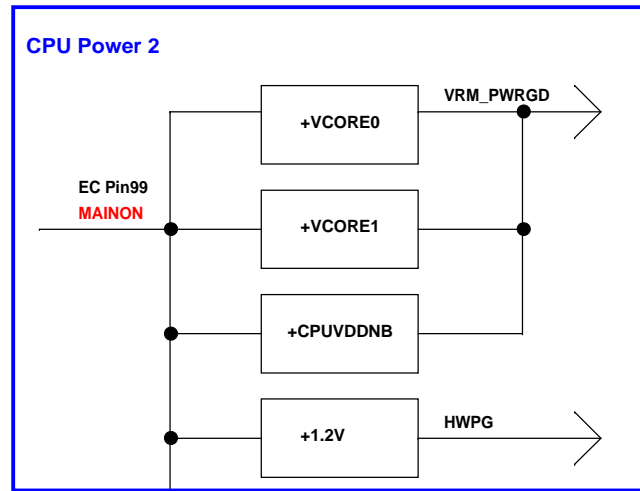
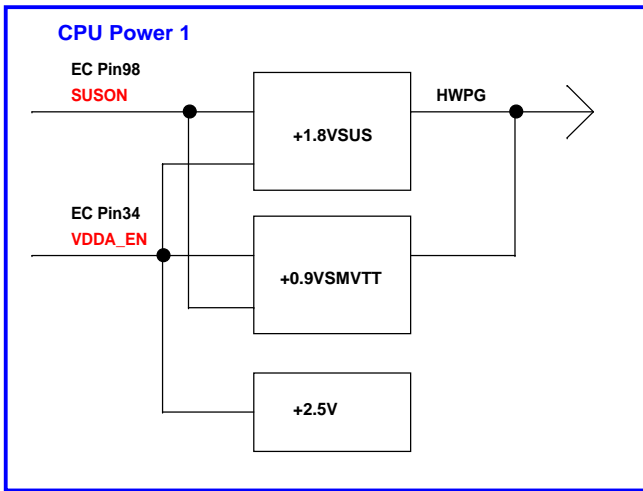
Place this cap close to EC

Place this cap close to EC

Place this cap close to EC



			PROJECT : R22	
			Quanta Computer Inc.	
Size	Document Number			Rev
Custom	CHARGER (ISL6251)			1A
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Power & Ground

Label	ACTIVE	Description	Control Signal
+VIN	S0, S3, S4, S5	AC ADAPTER (19V)	
+3VPCU	S0, S3, S4, S5	ALWAYS POWER (3V)	
+3V	S0		MAINON
+3VSUS	S0, S3		SUSON
+3VS5	S0, S3, S4, S5		S5_ON
+3VLANVCC	S0		LAN_POWER
+5VPCU	S0, S3, S4, S5	ALWAYS POWER (5V)	
+5V	S0		MAINON
+5V_VCC1			
+5VALW			
+10VALW			
+15VALW			
+1.8V	S0		+1.5_ON
+1.8VSUS	S0, S3		
+1.5V	S0		MAINON
+1.5VSUS	S0, S3	DDR CORE POWER	SUSON
+1.5VSUS_1			
+1.5V_VGA	S0	VGA , VRAM POWER	+1.5_ON
+1.2V	S0		VRON
+1.2VSUS	S0, S3		SUSON
+1.1V	S0	VDDPCIE - PCIE-E MAIN POWER	VRON
+1.1VS5	S0, S3, S4, S5	STANDBY POWER	S5_ON
+1.1V_DYN	S0	NB VDDC - CORE LOGIC POWER	DYN_PWR_EN
+1.05V	S0	HT POWER (1.05V)	VRON
+1.0V_VGA	S0	PARK DPX_VDD10 POWER	VRON
+2.5V	S0	CPU VDDA POWER	VR2.5_ON
+VCORE0	S0	CPU CORE POWER (?V)	VRON
+VCORE1	S0	CPU CORE POWER (?V)	VRON
+CPUVDDNB	S0	CPU VDDNB POWER	VRON
+0.75_DDR_VTT	S0	DDR COMMAND & CONTROL PULL UP POWER	SUSON
DDR_VTTREF	S0, S3	DDR REFERENCE POWER	SUSON
+VGA_CORE	S0	VGA CORE POWER	MAINON
+AVBAT	S0, S3, S4, S5	RTC & KBC POWER (3_3V)	

SMBUS

DEVICE	ADDRESS	BUS
CLOCK GENERATOR		
DDR3		
CPU THERMAL SENSOR		
CHARGER		

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

PCI DEVICES IRQ ROUTING

DEVICE	IDSEL #	REQ/GNT #	PCI_INT



PROJECT : R22
Quanta Computer Inc.

Size	Document Number	Rev 1A
Date: Wednesday, September 15, 2010 Sheet 42 of 43		

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