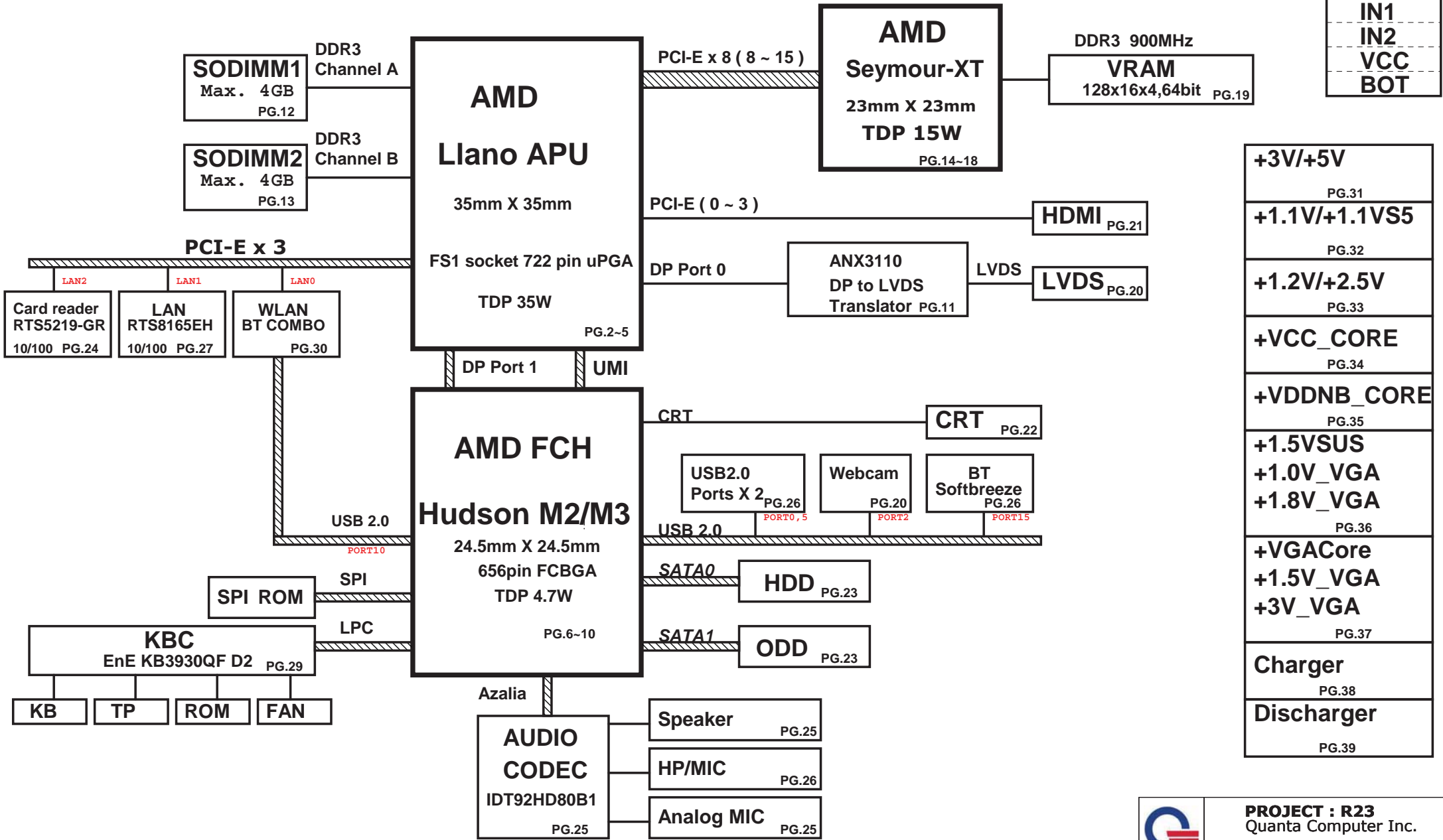



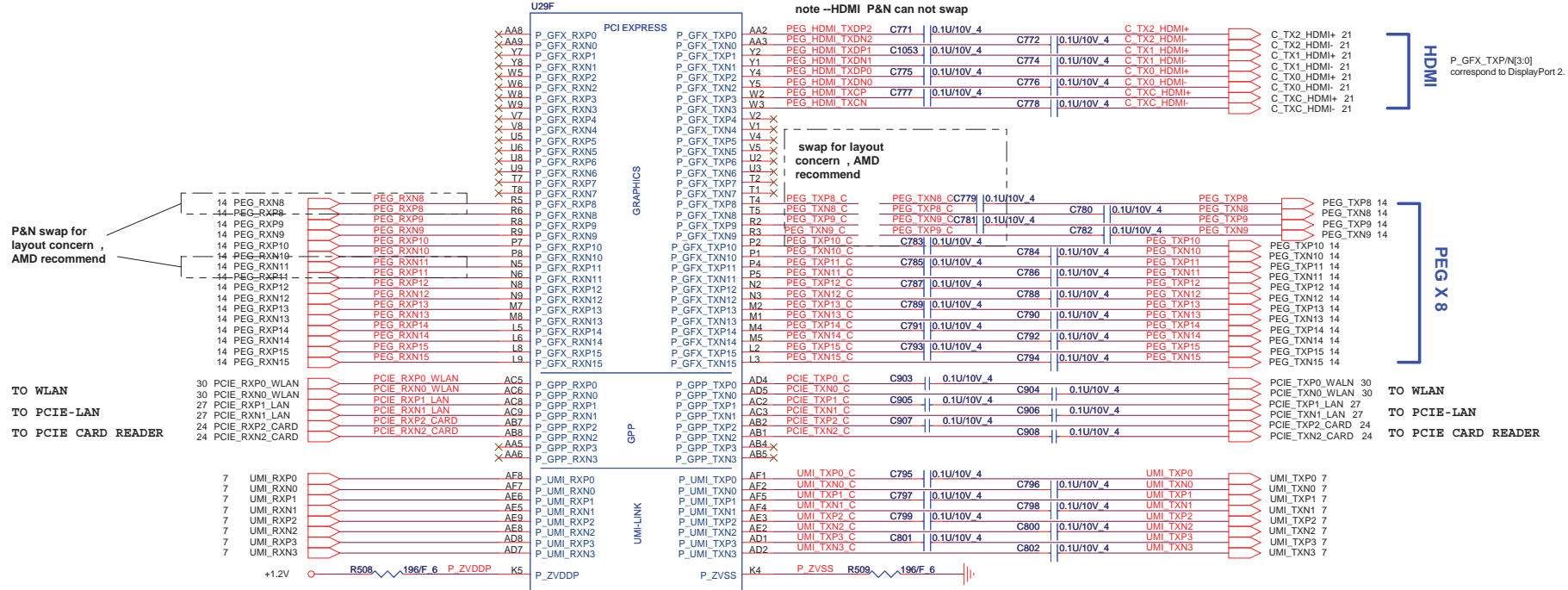
R23 AMD Sabin UMA/Muxless SYSTEM DIAGRAM

Stackup

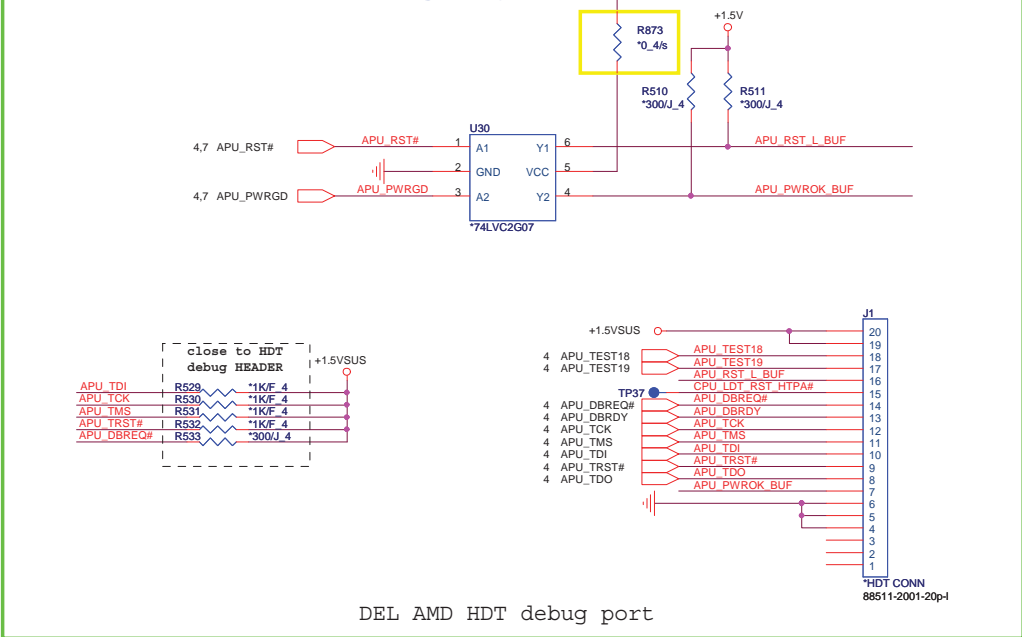
TOP
GND
IN1
IN2
VCC
BOT



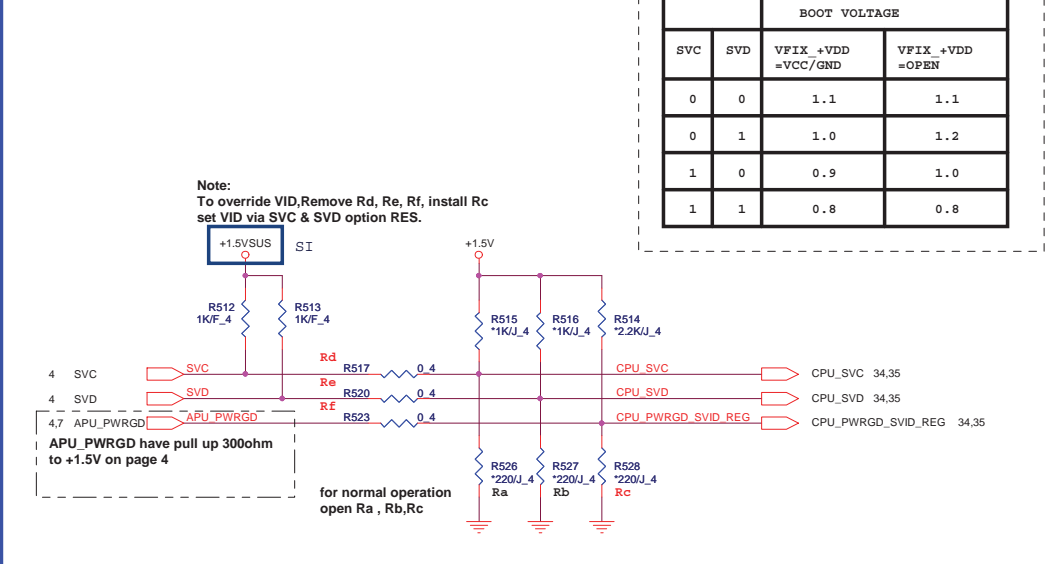
	PROJECT : R23		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number BLOCK DIAGRAM	
Date: Tuesday, May 03, 2011		Sheet 1 of 40	



HDT+ Connector for Debug only

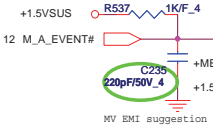
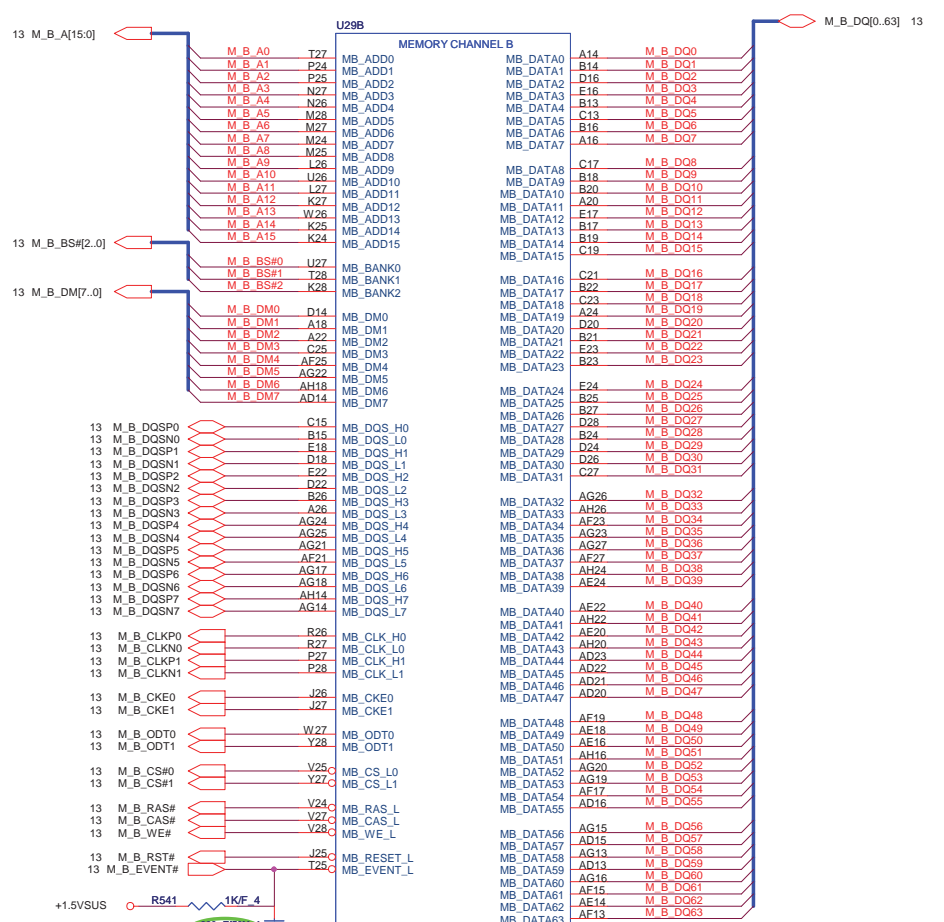
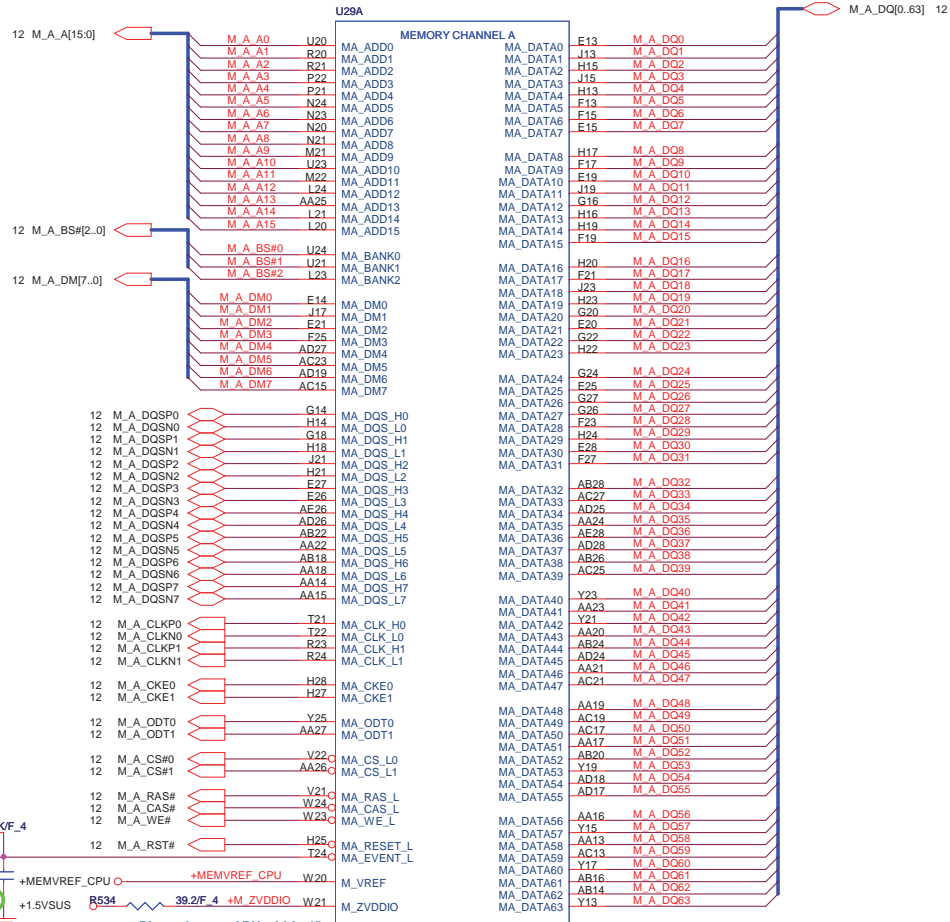


VID Override Circuit



Quanta Computer Inc.
PROJECT : R23

Size Document Number **Liano PCIE/UMI/GPP** Rev 1A
Date: Wednesday, May 04, 2011 Sheet 2 of 40

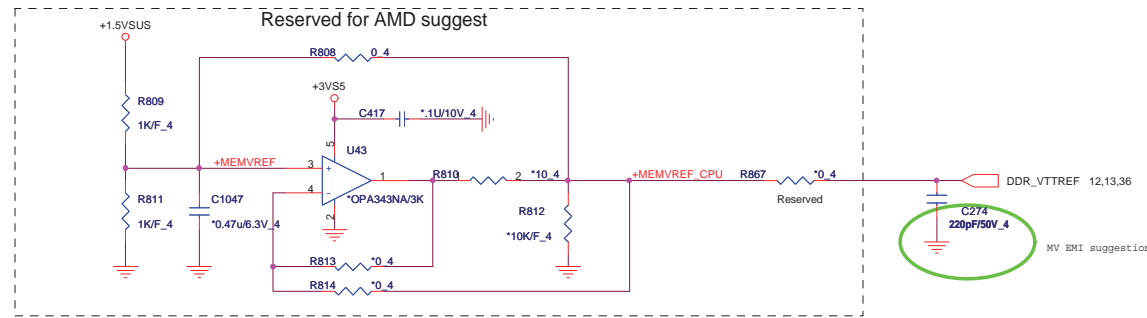


Place close to APU within 1" Soldermask openings for all bottom side vias/TpS under FS1



Llano APU

Llano APU

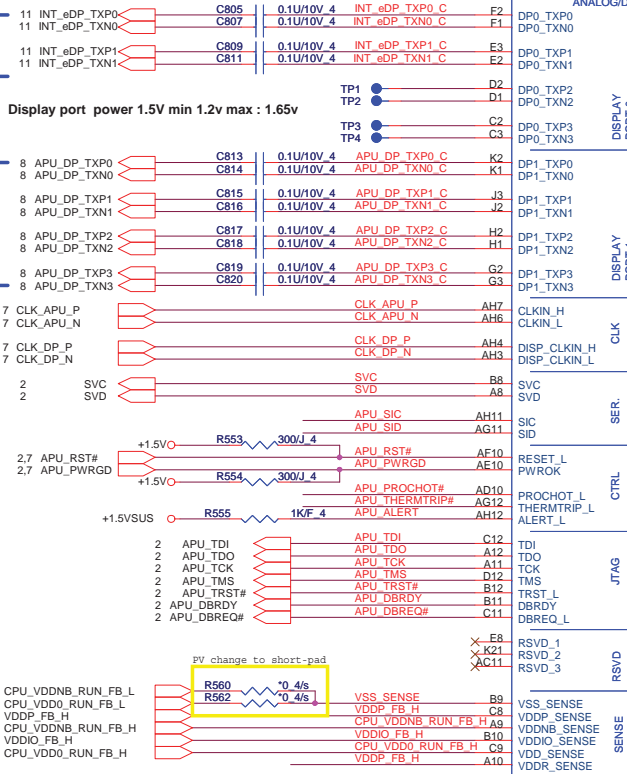


Quanta Computer Inc.
 PROJECT : R23

Size	Document Number	Rev
	Llano DDR3 MEM I/F	1A
Date:	Wednesday, May 04, 2011	Sheet 3 of 40

Place caps with APU < 1 inch route PCIe as 85ohm +/- 10%

DP0 output to eDP to LVDS converter

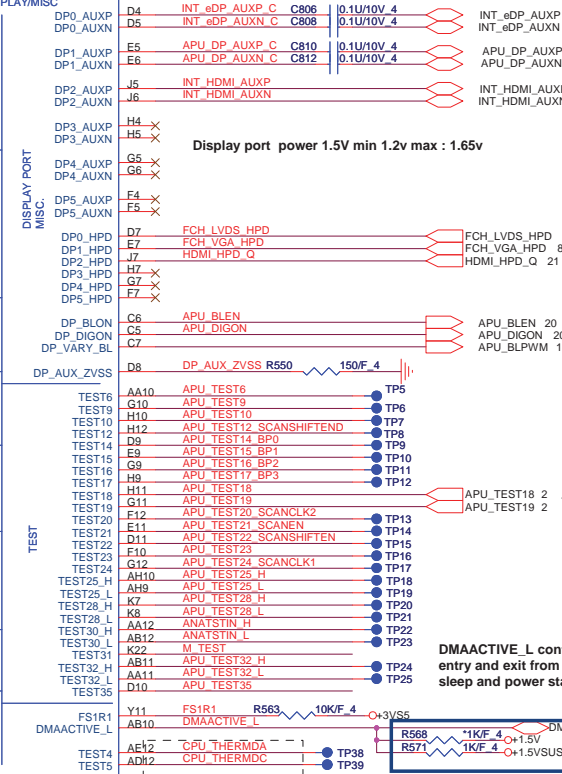


Display port power 1.5V min 1.2V max : 1.65v

DP1 output to Hudson-M2 for VGA translator interface

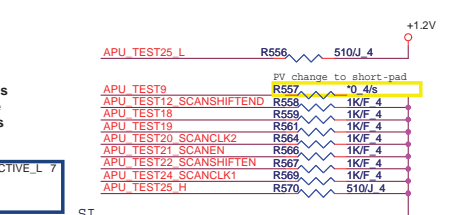
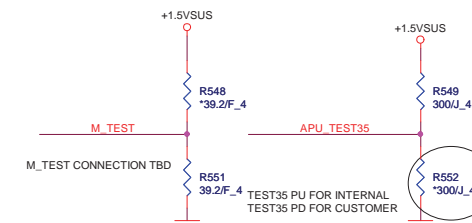
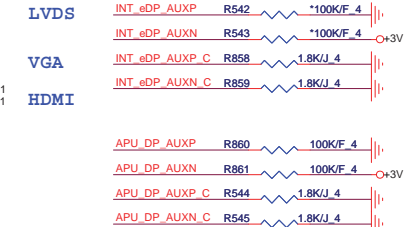
Note: CLK_APU_HCLKP/N is 100MHZ SSC

Note: CLK_DP_NSSCP/N is 100MHZ non-SSC

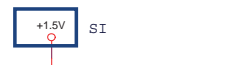


Display port power 1.5V min 1.2V max : 1.65v

DMAACTIVE_L controls entry and exit from the sleep and power states

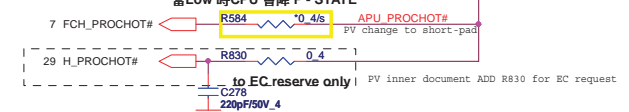


Llano APU

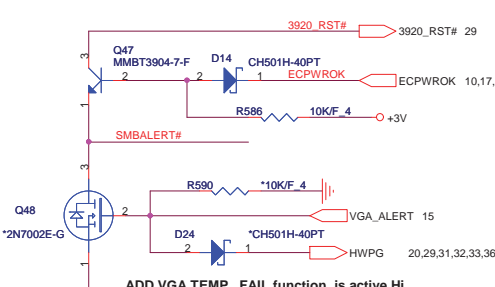


FS1R1 signals is for detect CPU TYPE and protect it. FS1R1 CPU this pin is N.C FS1R2 CPU this pin is LOW can remove it at MP

APU_PROCHOT# 可以當 input or output 當Low時CPU會降 P- STATE



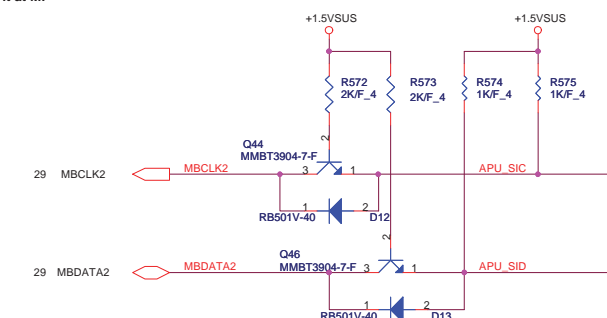
Thermal



over 120 degree C = Low

When 100K-NTC 100 C=6.164K Thermal Trip = 120 C

DEL Thermal IC circuit on MV

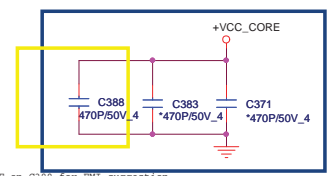


Quanta Computer Inc.
PROJECT : R23

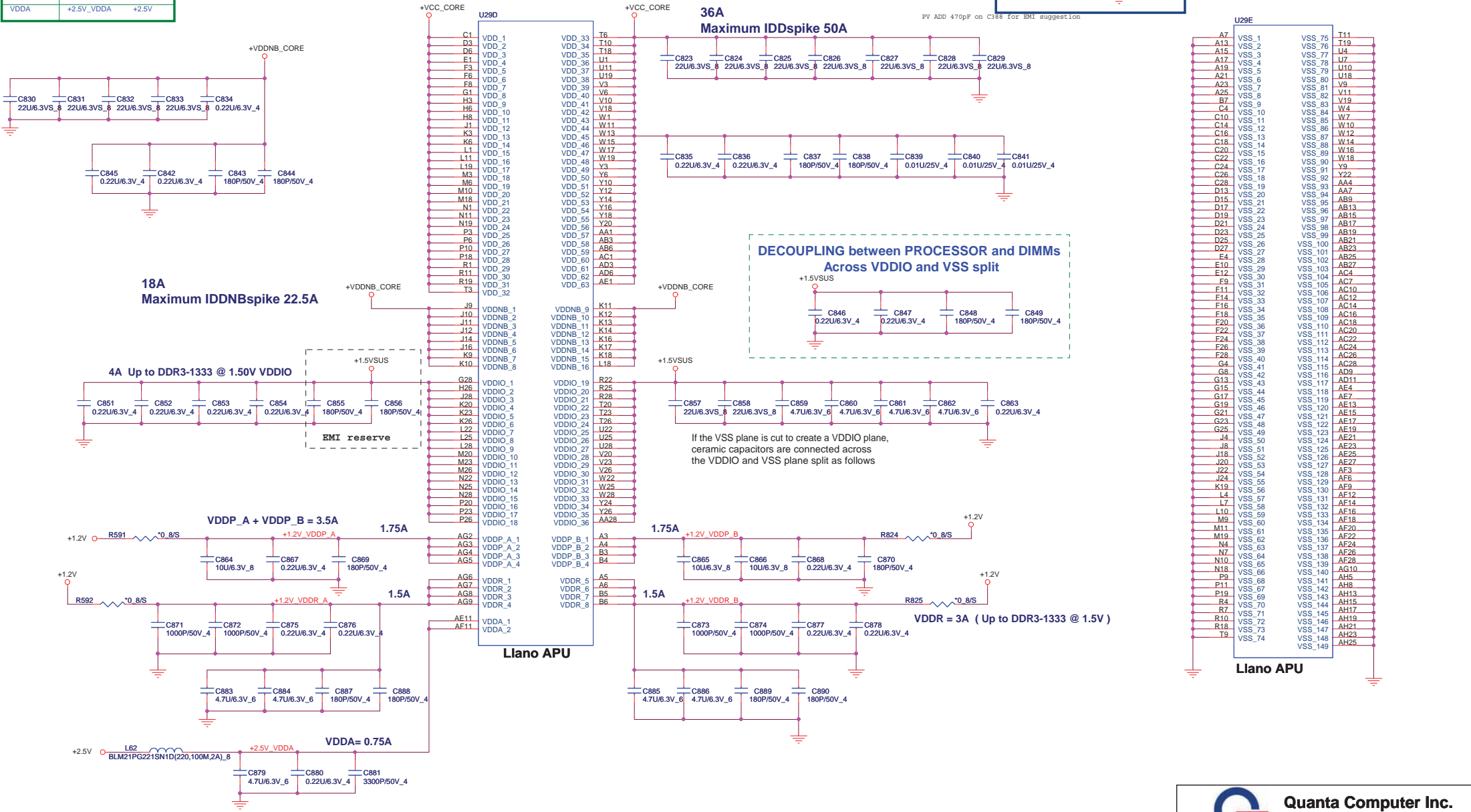
Size	Document Number	Llano Display/Misc	Rev 1A
Date: Wednesday, May 04, 2011	Sheet 4	of 40	

APU POWER TABLE

PIN NAME	NET NAME	VOLTAGE
VDD	+VCC_CORE	+1.1V
VDDNB	+VDDNB_CORE	??
VDDIO	+1.5VSUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V



SI EMI



18A
Maximum IDDNBspike 22.5A

36A
Maximum IDDspike 50A

DECOUPLING between PROCESSOR and DIMMs
Across VDDIO and VSS split

If the VSS plane is cut to create a VDDIO plane, ceramic capacitors are connected across the VDDIO and VSS plane split as follows

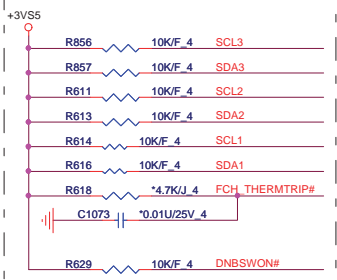
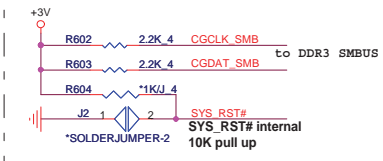
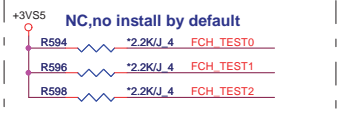
PV ADD 470pF on C388 for EMI suggestion

Liano APU

Liano APU

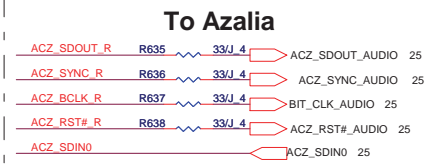
Quanta Computer Inc.
PROJECT : R23

Size	Document Number	Rev
	Liano POWER/GND	1A
Date:	Wednesday, May 04, 2011	Sheet 5 of 40

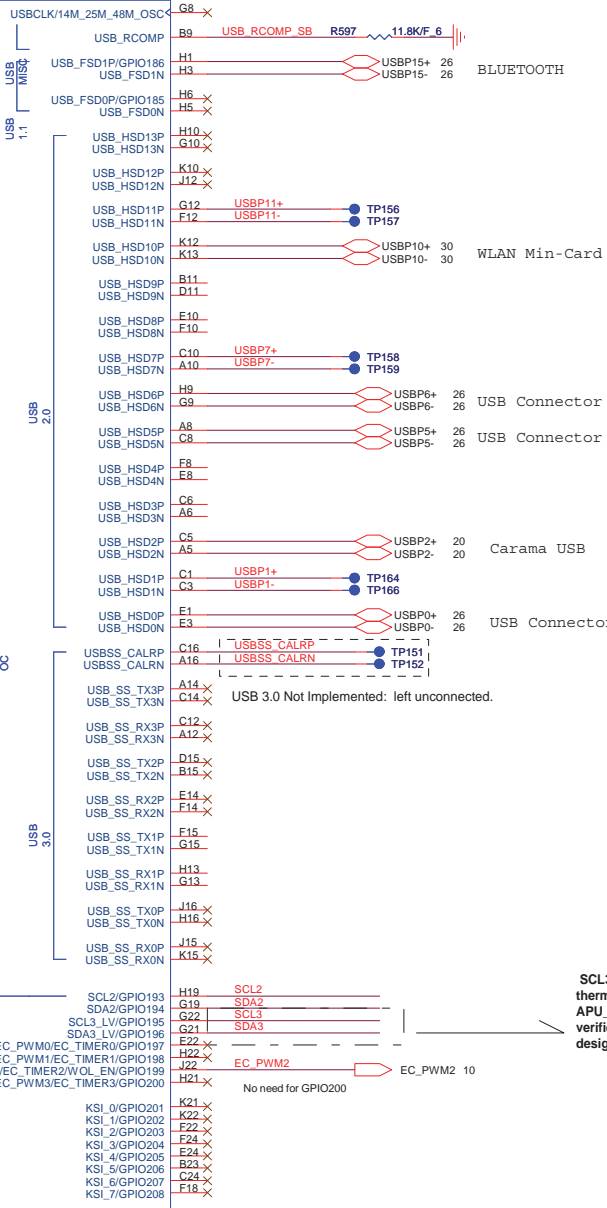
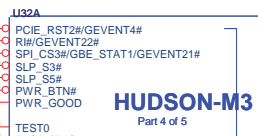
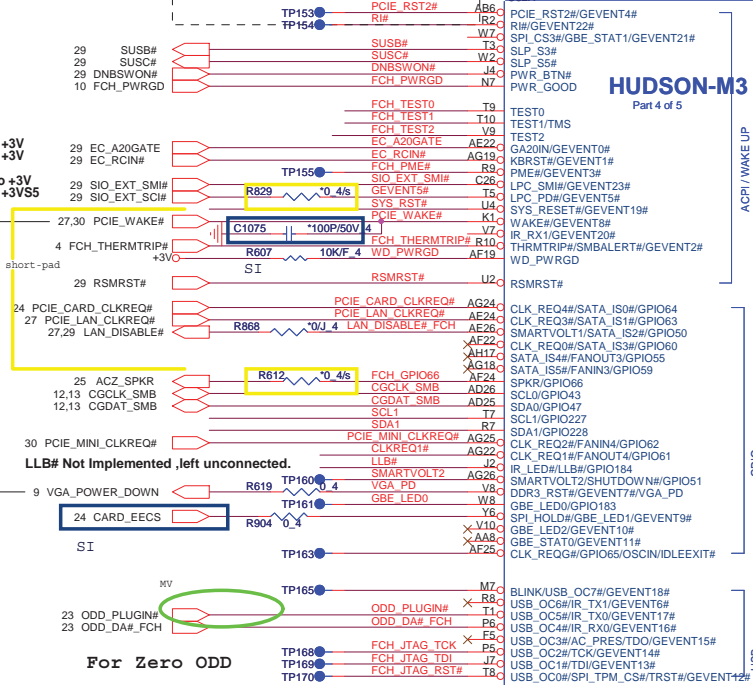


This pin is used to power down VGA DAC regulators when CRT no connected

GEVENT16# internal pull Hi 8.2K to +3V5S
GEVENT15# internal pull Hi 8.2K to +3V5S



remove PCIE_RST2# from AMD recommend

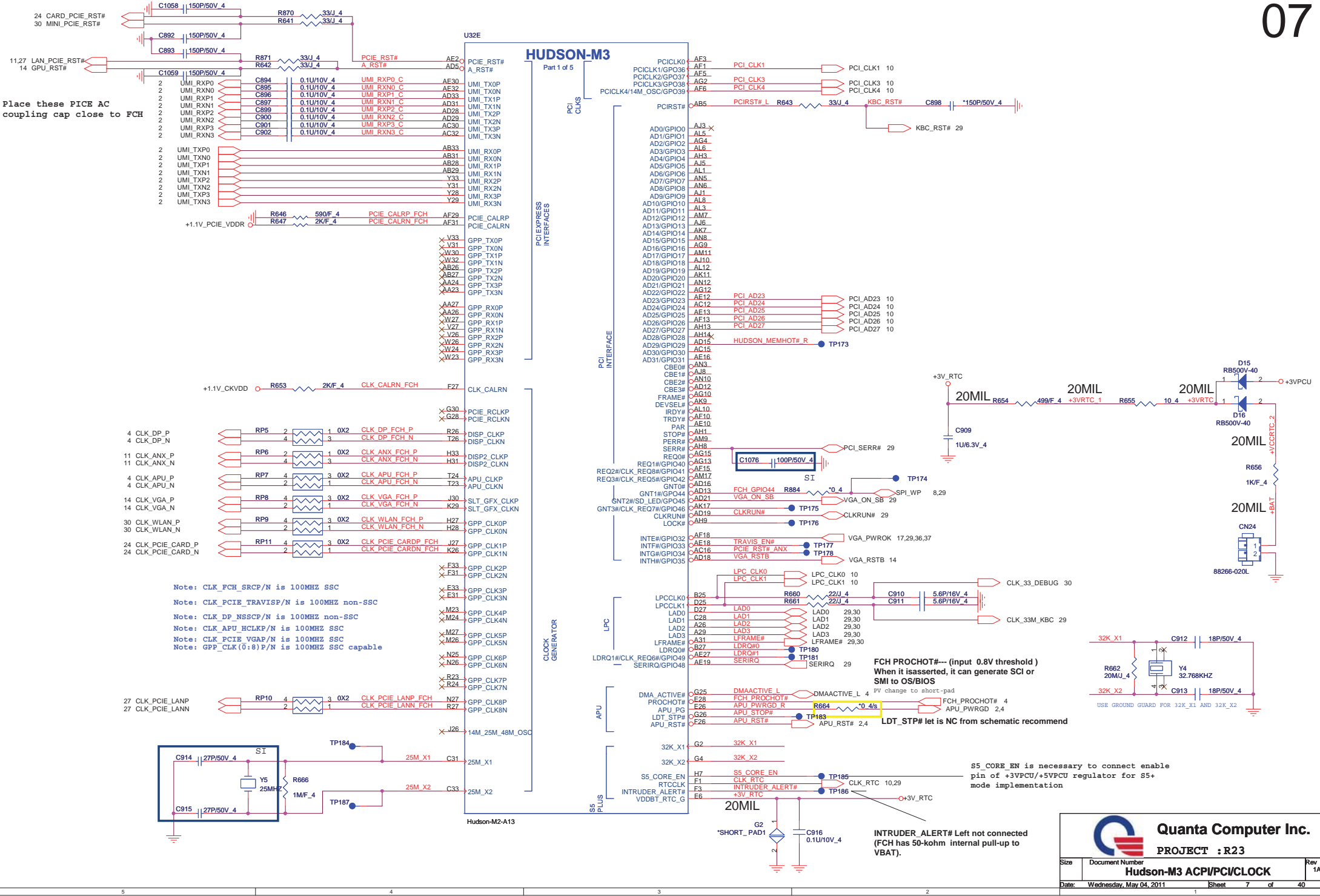


SCL3 of a TSI-capable APU's thermal bus, Pulled up to APU_VDDIO. Resistor value verified in the relevant APU design guide.

Hudson-M2-A13

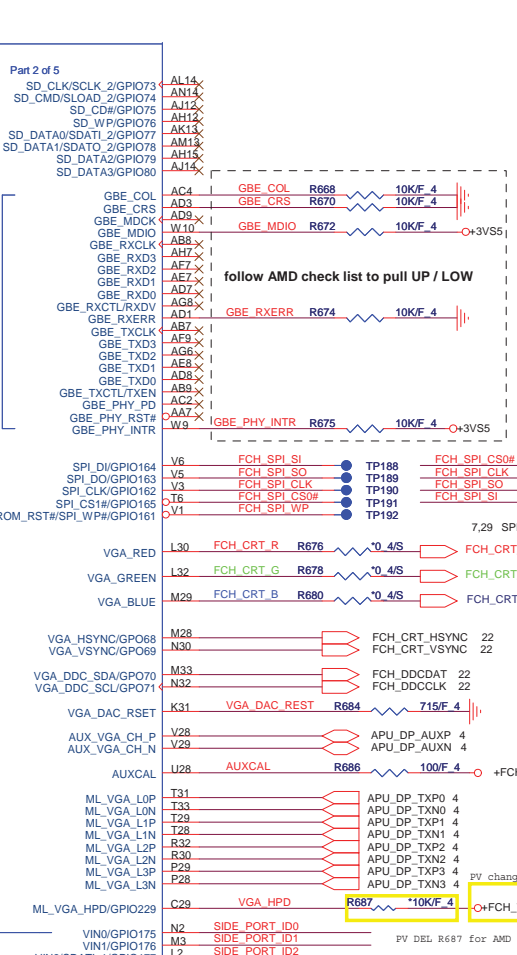
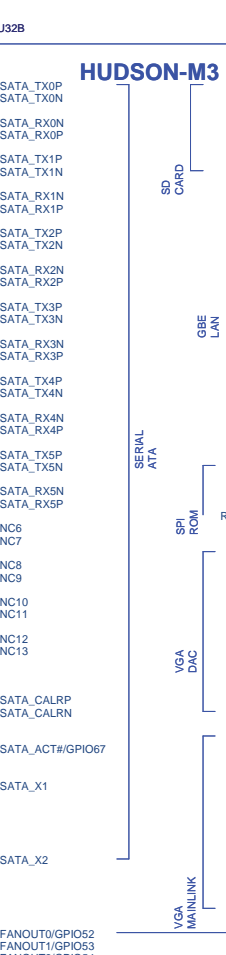
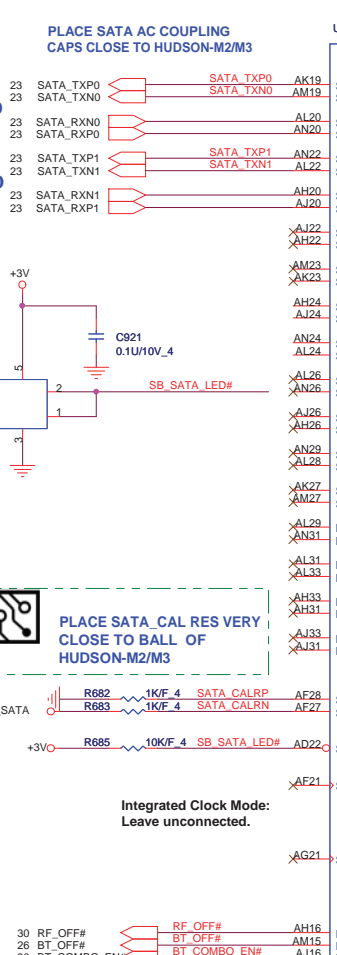
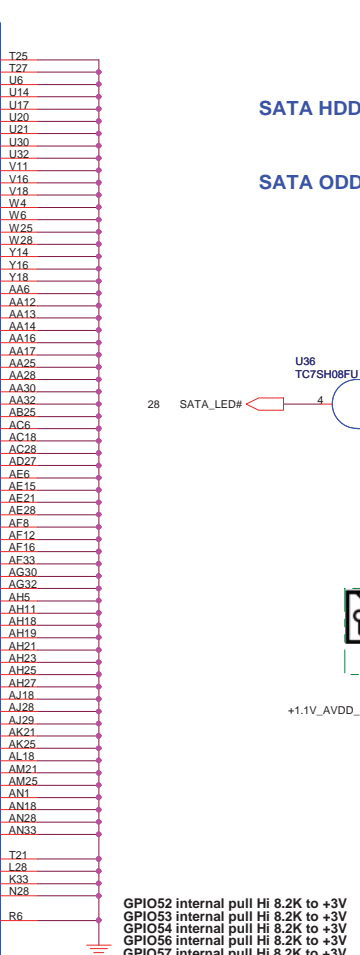
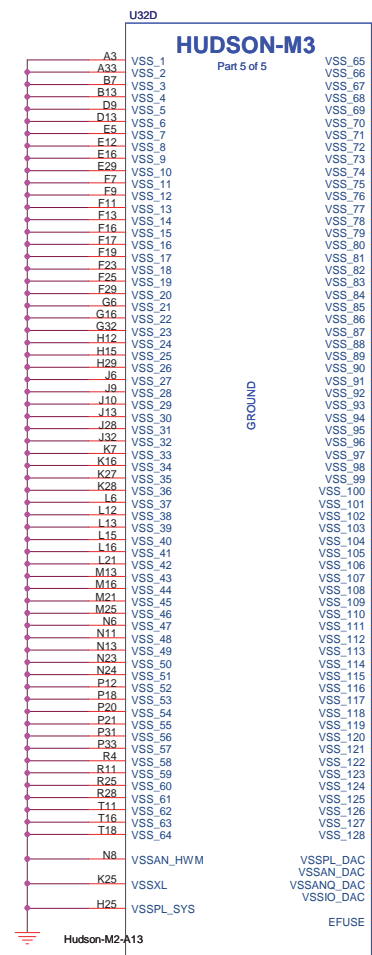
Quanta Computer Inc.
PROJECT : R23

Size	Document Number	Hudson-M3 GPIO/USB/AZ/RGMII	Rev	1A
Date:	Wednesday, May 04, 2011	Sheet	6	of 40

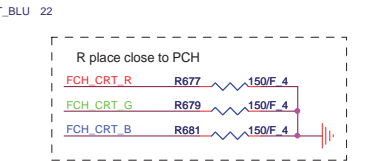
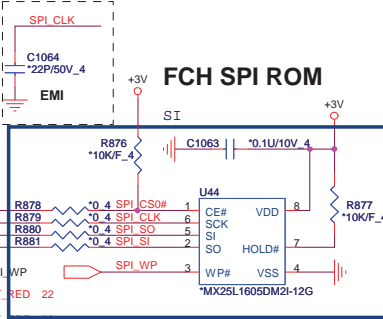


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PROJECT : R23

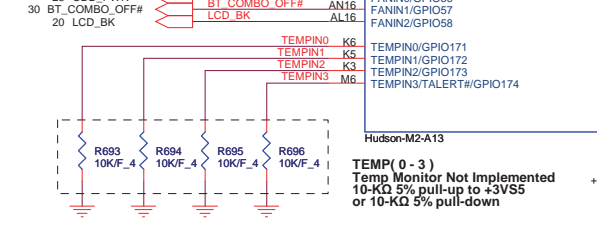
Size	Document Number	Rev
	Hudson-M3 ACP/PCI/CLOCK	1A
Date:	Wednesday, May 04, 2011	Sheet 7 of 40



Vender	Size	P/N
AMIC	2M	AKE382N0801
WINBOND	2M	AKE38FP0N01
Socket		DFHS08FS023



ID4	ID3	ID2	ID1	ID0	CONFIG	31- Level BOM	Item
0	0	0	0	0	UMA		1
0	0	0	1	0			2
0	0	1	0	0			3
0	0	1	1	0			4
0	1	0	1	0			5
0	1	1	1	0			6
1	0	0	1	0			7
1	0	1	1	0			8
0	0	0	0	1	SG / Muxless		9
0	0	1	0	1			10
1	0	0	1	1			11
1	0	1	1	1			12



SIDE_PORT_ID2	SIDE_PORT_ID1	SIDE_PORT_ID0	Manufacturer
0	0	0	Samsung
0	0	1	Hynix
0	1	0	NC
0	1	1	no support side port

Quanta Computer Inc.

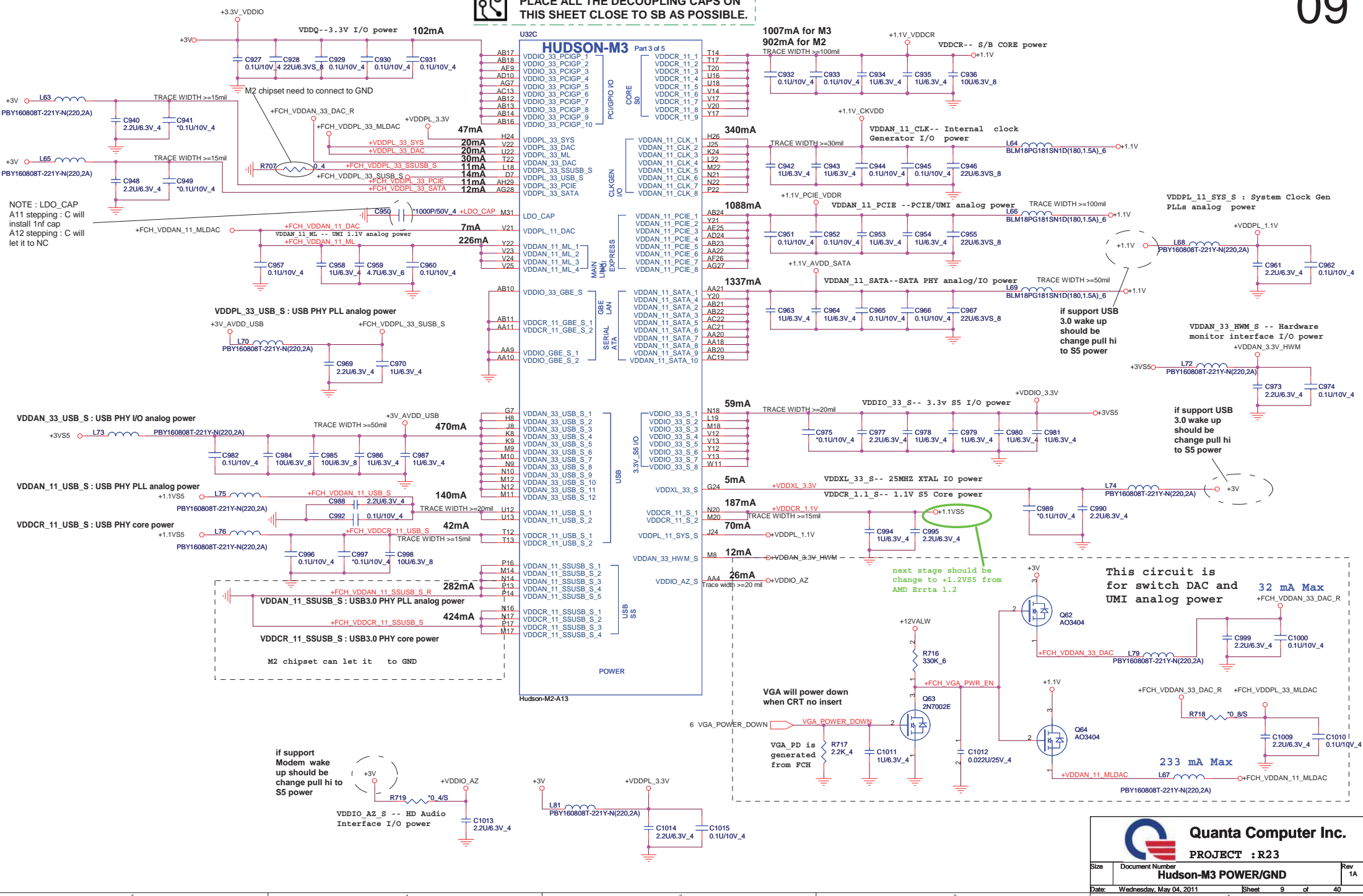
PROJECT : R23

Document Number: **Hudson-M3 SATA/HWM/SPI**

Date: Wednesday, May 04, 2011

Sheet 8 of 40

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.



NOTE : LDO_CAP
A11 stepping: C will
install 1nf cap
A12 stepping: C will
let it to NC

if support
Modem wake
up should be
change pull hi to
S5 power

if support USB
3.0 wake up
should be
change pull hi
to S5 power

if support USB
3.0 wake up
should be
change pull hi
to S5 power

This circuit is
for switch DAC and
UMI analog power
32 mA Max

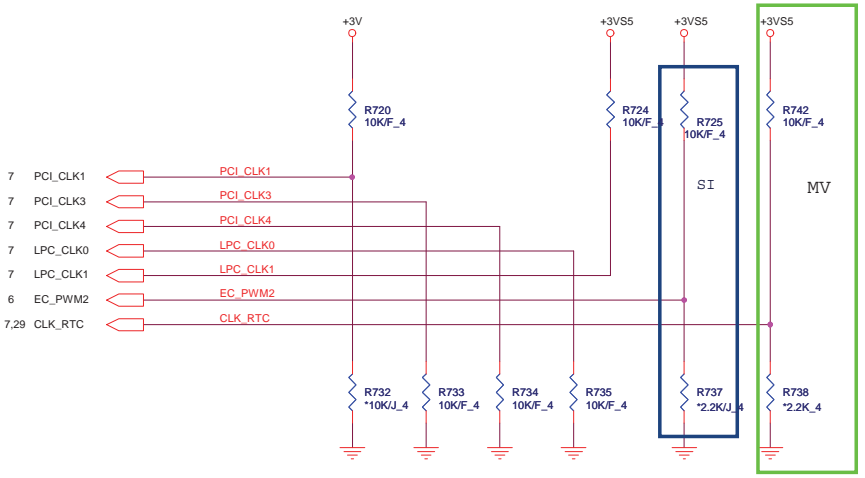
VGA will power down
when CRT no insert
VGA_PD is
generated
from FCH

Quanta Computer Inc.
PROJECT : R23

Size	Document Number	Rev
	Hudson-M3 POWER/GND	1A
Date:	Wednesday, May 04, 2011	Sheet 9 of 40

STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



REQUIRED STRAPS

	-----	PCI_CLK1	-----	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	CLK_RTC
PULL HIGH	-----	ALLOW PCIe Gen2 DEFAULT	-----	USE DEBUG STRAP	non_Fusion CLOCK MODE	AMD internal EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM DEFAULT	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	-----	FORCE PCIe Gen1	-----	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM	S5 PLUS MODE ENABLED

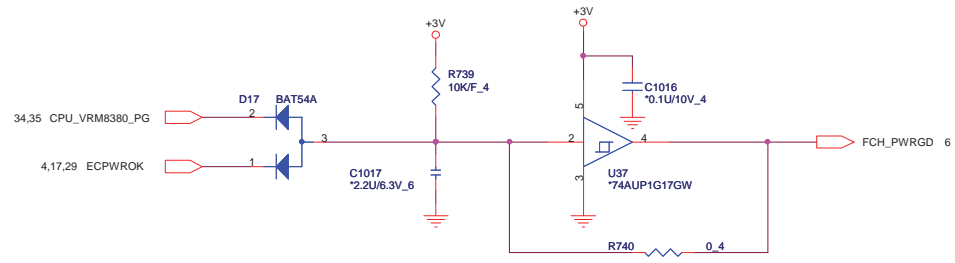
DEBUG STRAPS

FCH has 15K Internal Pull Up for PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIe STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIe STRAPS	ENABLE PCI MEM BOOT

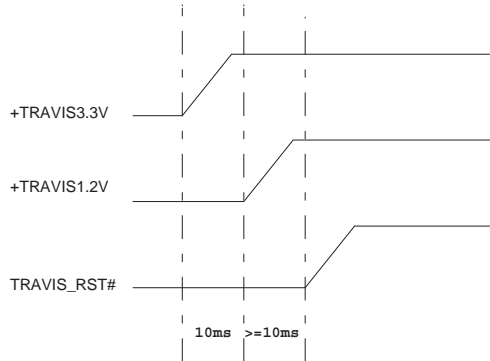
FCH_PWRGD



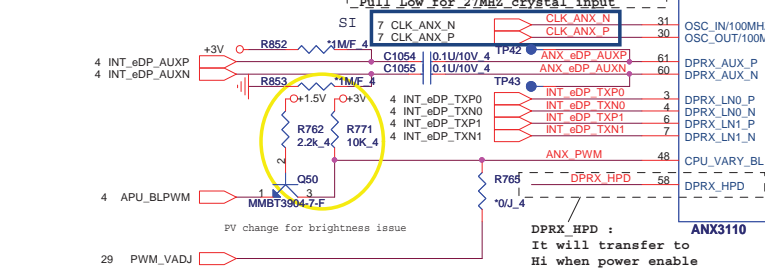
Quanta Computer Inc.
PROJECT : R23

Size	Document Number	Rev
	Hudson-M3 STRAP/PWRGD	1A
Date:	Wednesday, May 04, 2011	Sheet 10 of 40

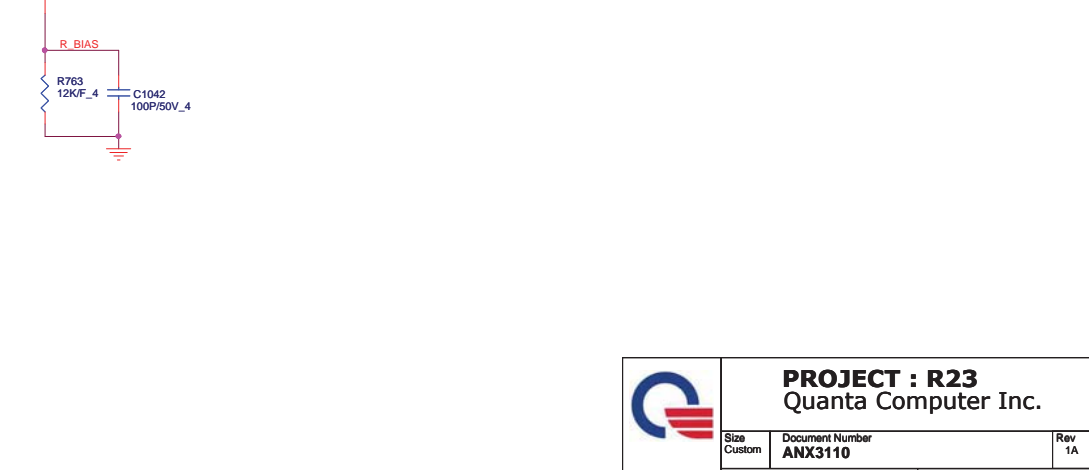
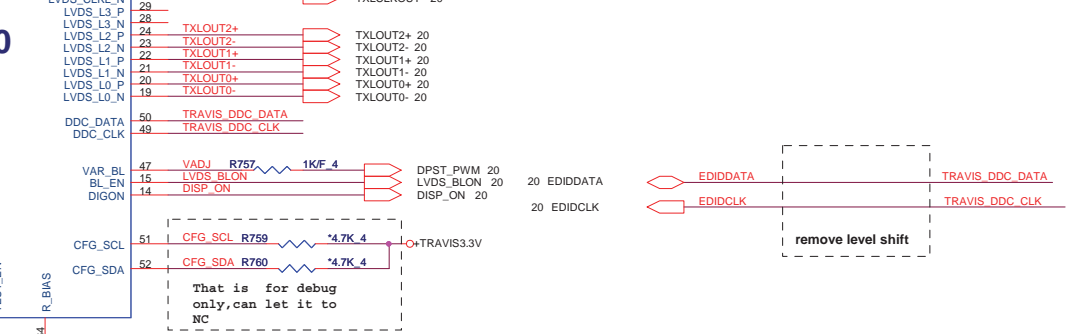
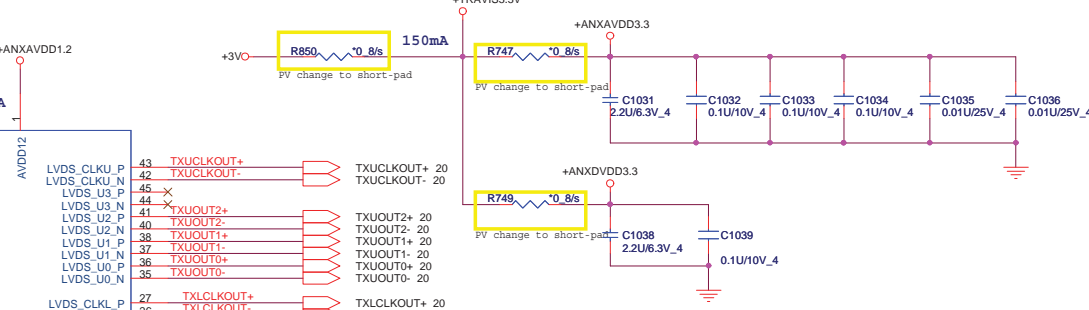
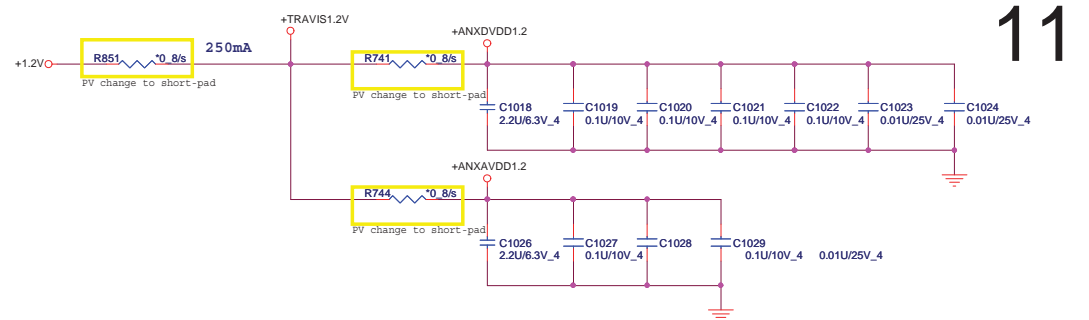
ANX3110 Power Up Sequence



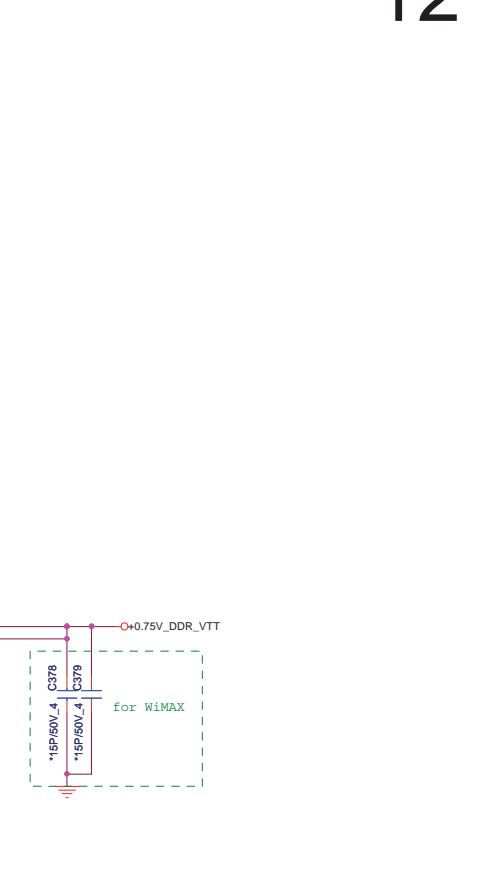
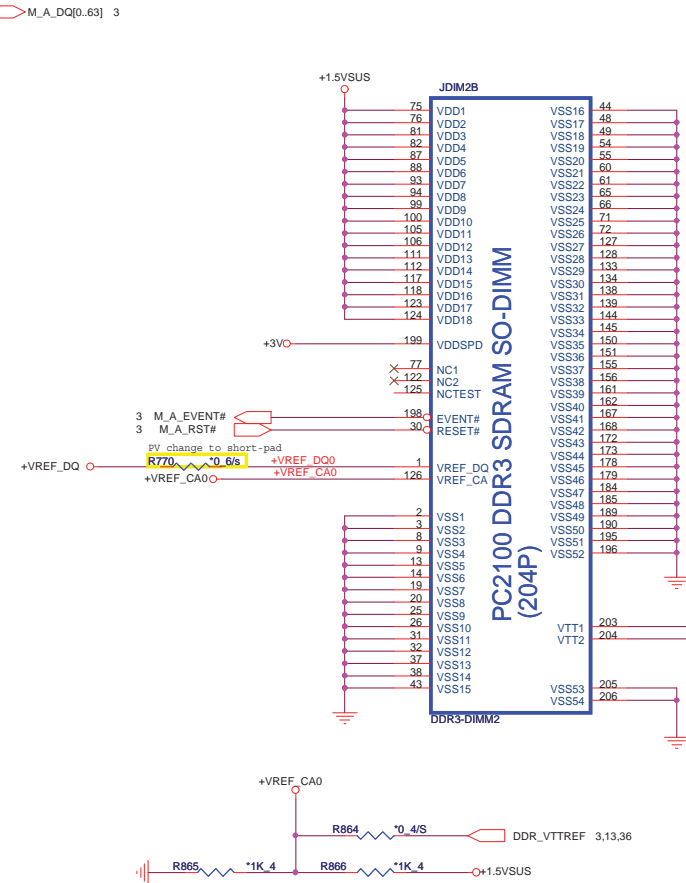
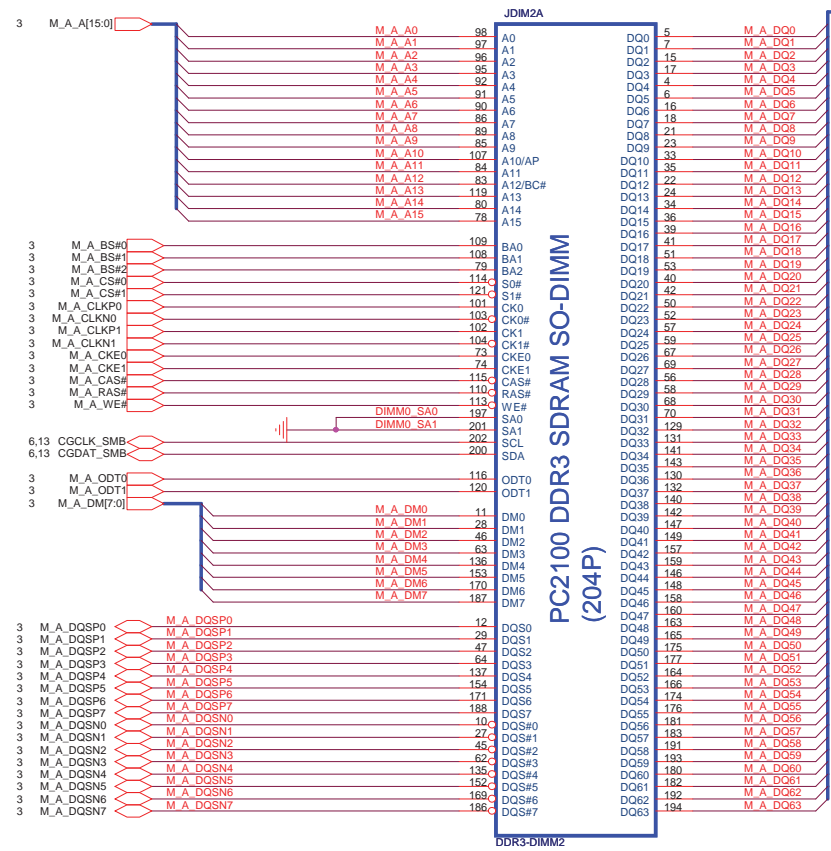
GPIO 0 : Define VAR_BL & BL_EN & DIGON H/W or S/W control power up timing
 Pull Hi for H/W mode
 ---chip have defined power up timing
 Pull Low for S/W mode -- APU through DPRX port to program it



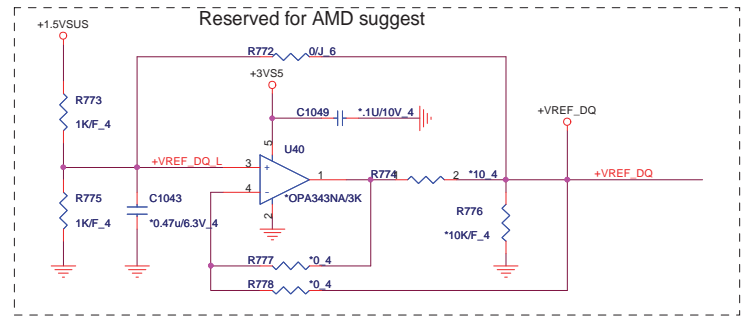
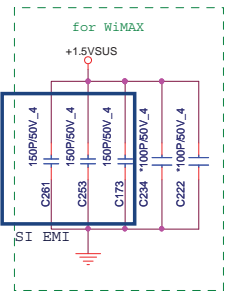
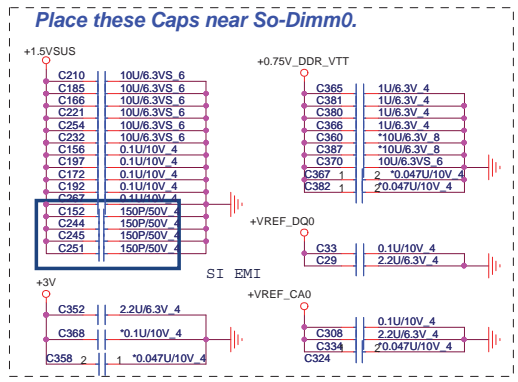
ANALOGIX ANX3110



PROJECT : R23 Quanta Computer Inc.		
Size Custom	Document Number ANX3110	Rev 1A
Date: Tuesday, May 03, 2011	Sheet 11 of 40	



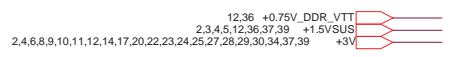
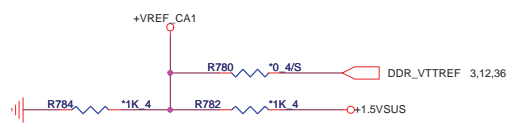
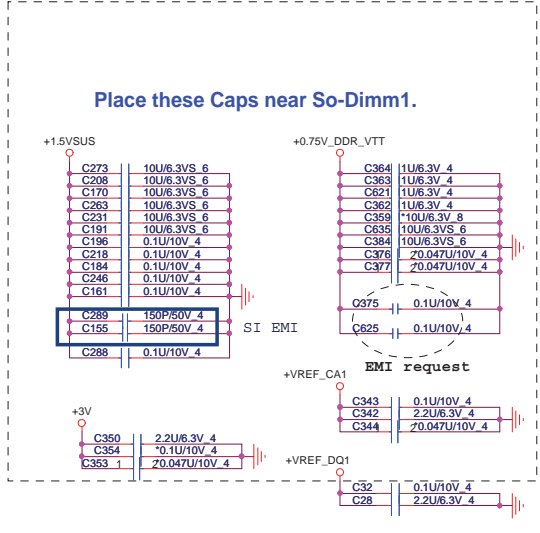
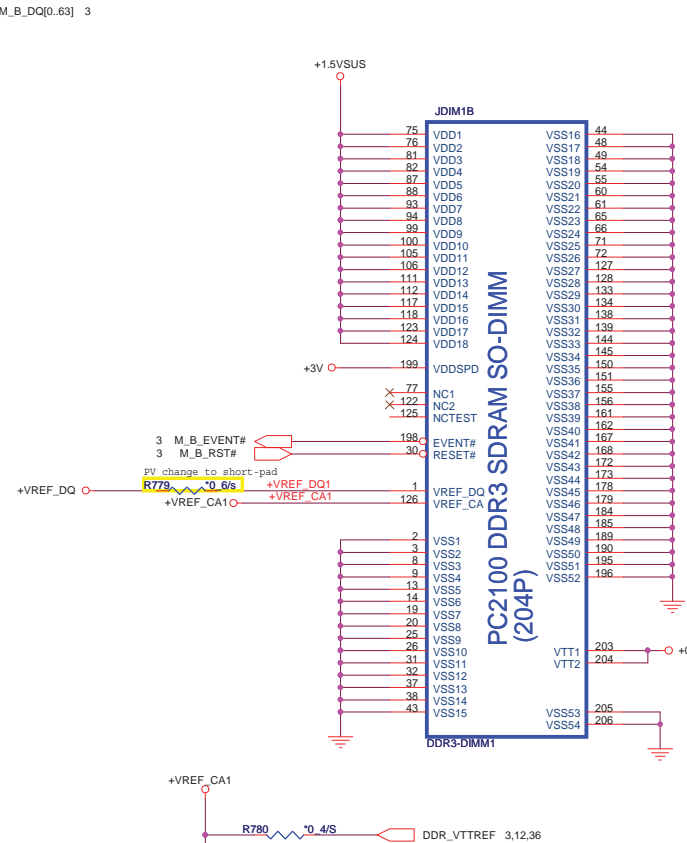
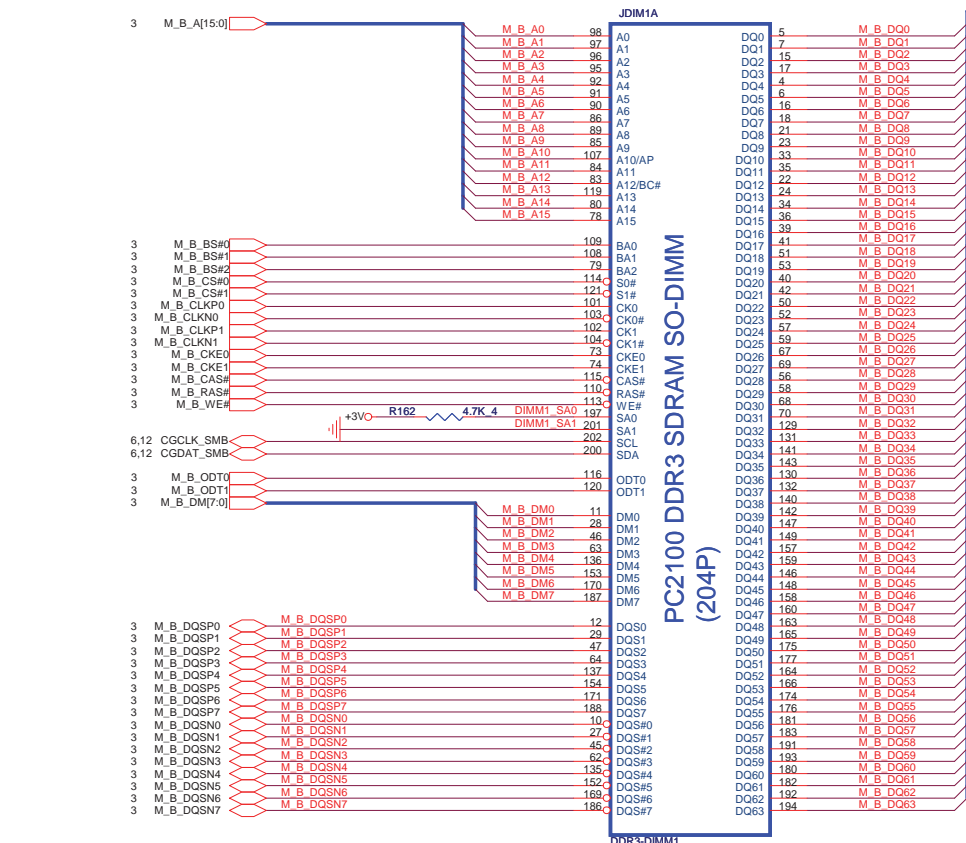
H9.2mm



13.36 +0.75V_DDR_VTT
 2.3,4,5,13,36,37,39 +1.5VSUS
 2,4,6,8,9,10,11,13,14,17,20,22,23,24,25,27,28,29,30,34,37,39 +3V

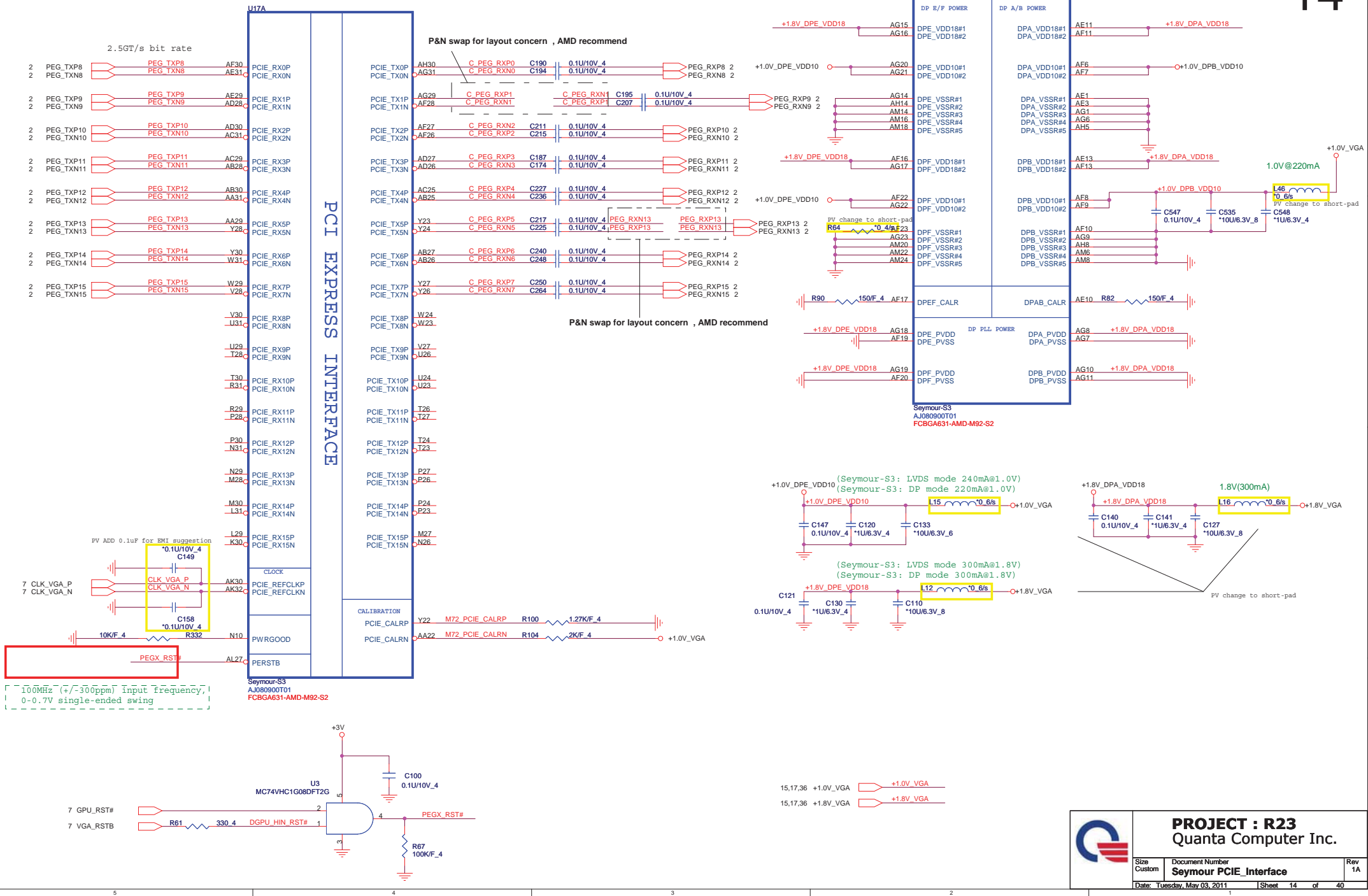
PROJECT : R23
 Quanta Computer Inc.

Size Custom Document Number **DDR3 DIMM-0** Rev 1A
 Date: Tuesday, May 03, 2011 Sheet 12 of 40

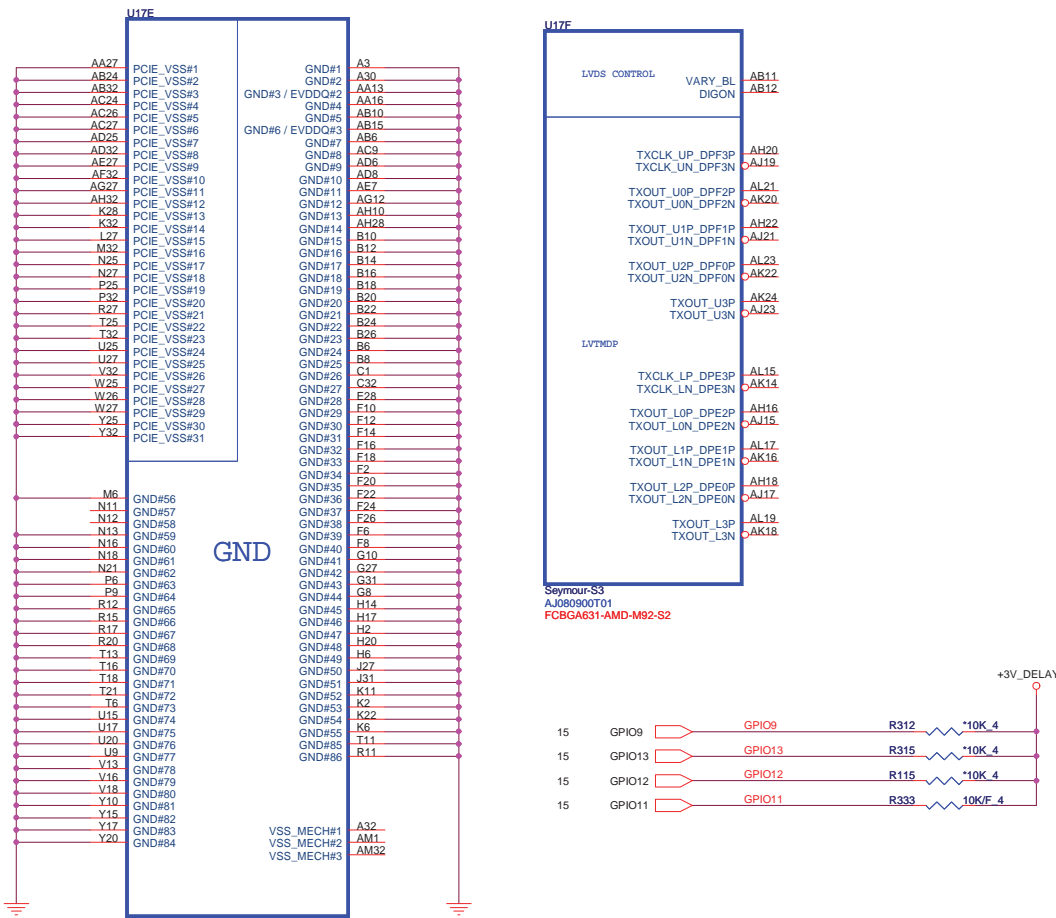


PROJECT : R23
Quanta Computer Inc.

Size Custom	Document Number DDR3 DIMM-1	Rev 1A
Date: Tuesday, May 03, 2011 Sheet 13 of 40		



PROJECT : R23 Quanta Computer Inc.		
Size Custom	Document Number	Rev 1A
Seymour_PCIE_Interface		
Date: Tuesday, May 03, 2011	Sheet 14	of 40



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

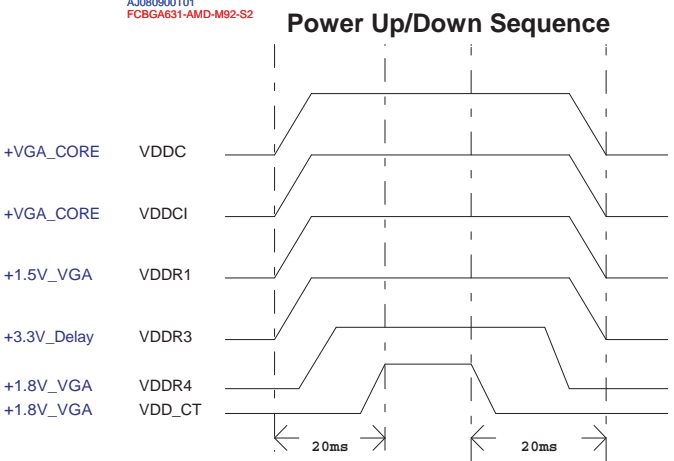
RECOMMENDED SETTINGS
 0= DO NOT INSTALL RESISTOR
 1= INSTALL 10K RESISTOR
 X = DESIGN DEPENDANT
 NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	Enable CLKREG# Power Management 0 - CLKREG# power management capability is disabled 1 - CLKREG# power management capability is enabled	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

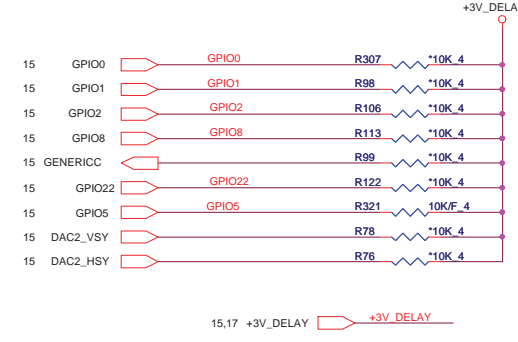
H2SYNC	GENERICC	
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET		
GPIO21_BB_EN		



Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

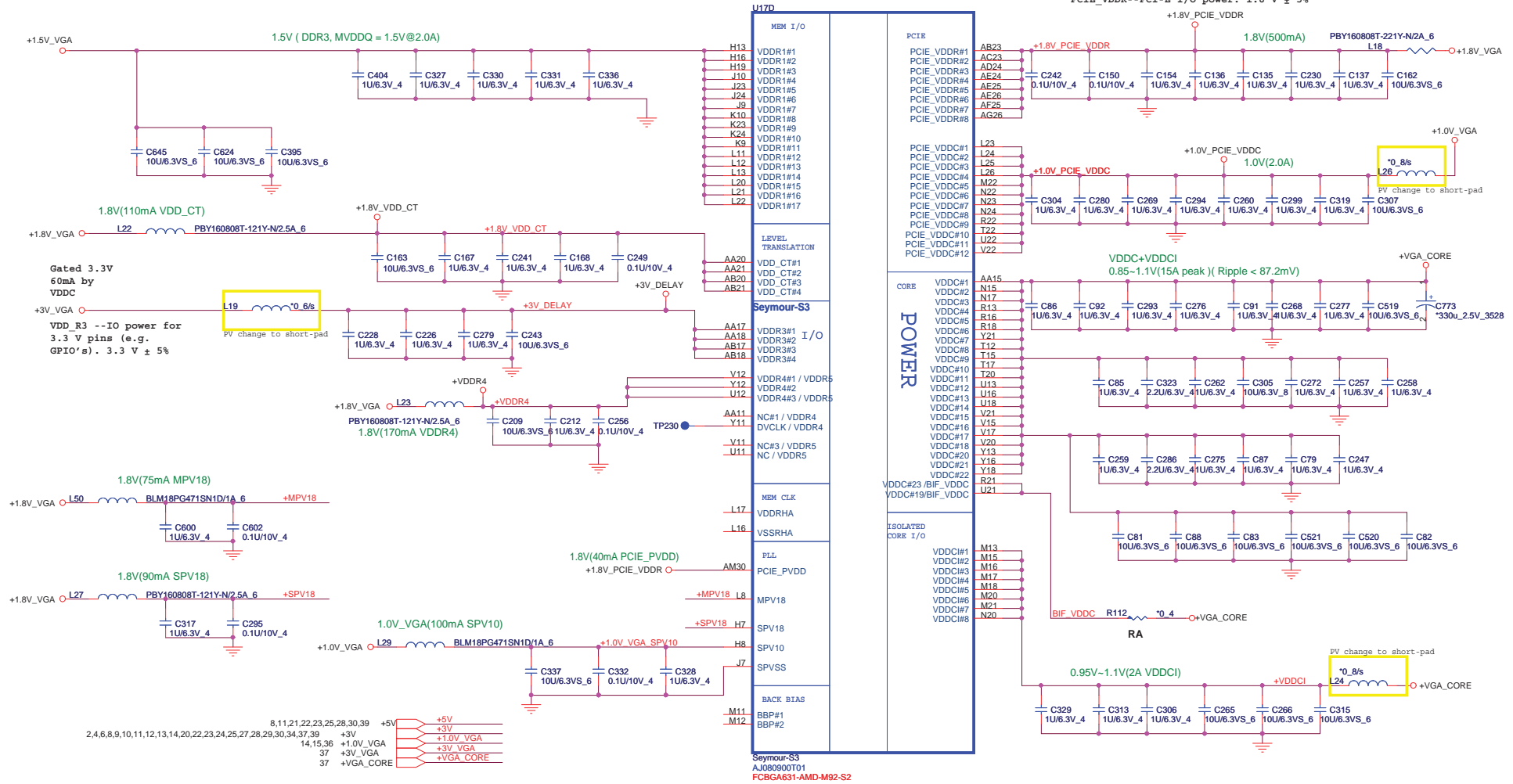
It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.



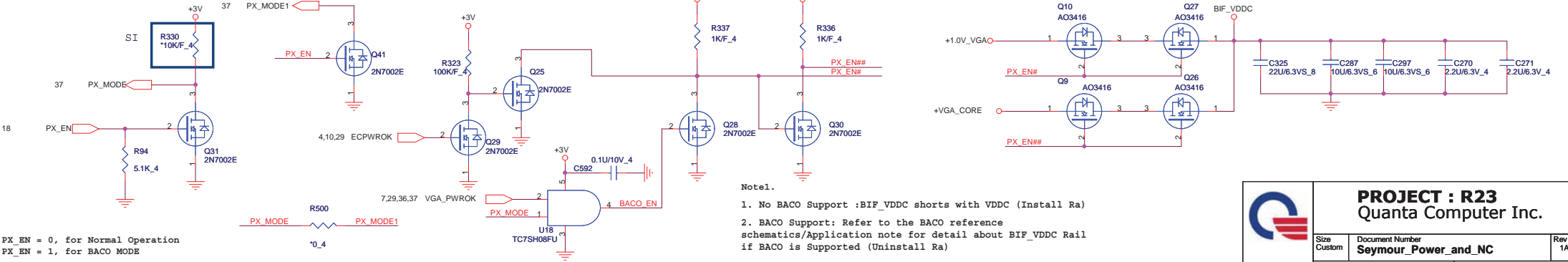
PROJECT : R23
Quanta Computer Inc.

Size Custom	Document Number Seymour GND / LVDS/ Straps	Rev 1A
Date: Tuesday, May 03, 2011	Sheet 16 of 40	

PCIE_VDDR--PCI-E I/O power. 1.8 V ± 5%

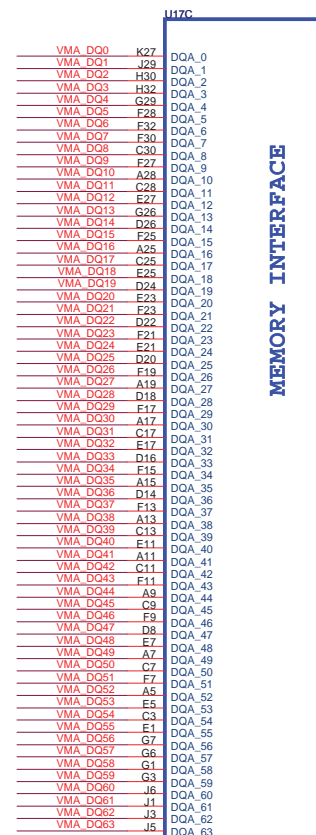
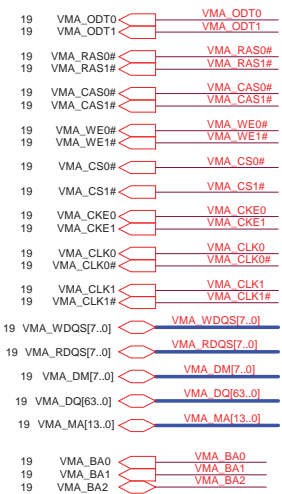


Support BACO Mode

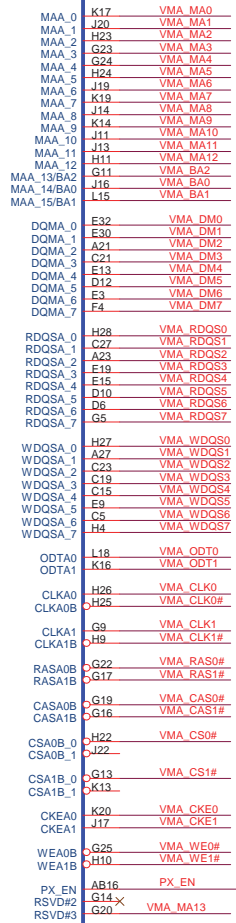


PROJECT : R23
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Seymour_Power_and_NC	1A
Date: Tuesday, May 03, 2011	Sheet 17 of 40	

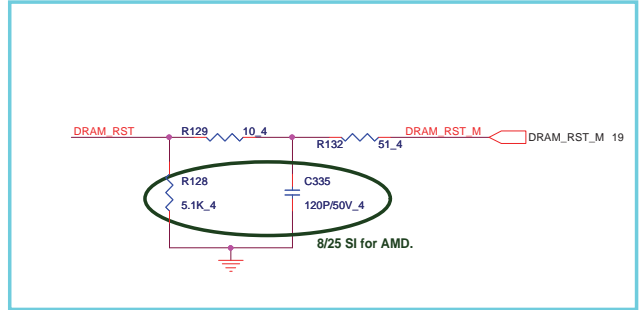
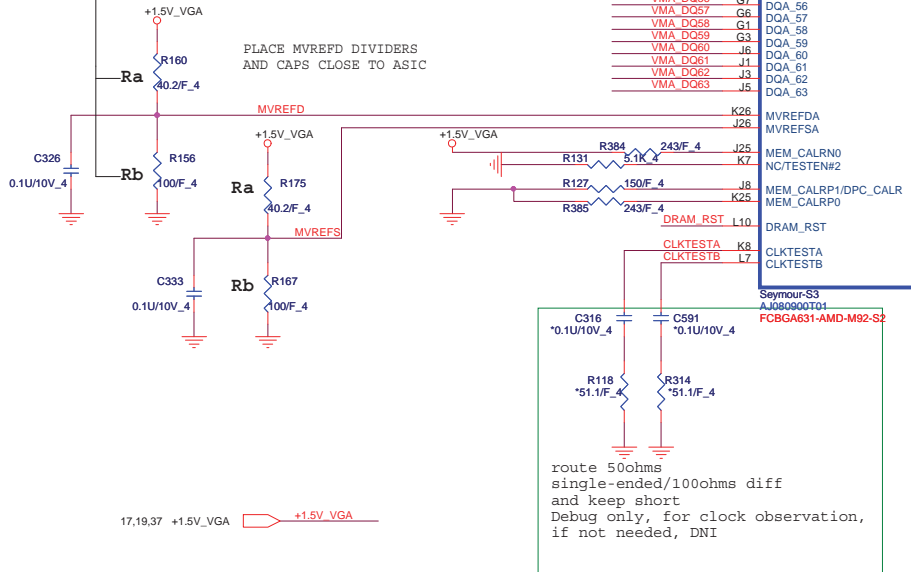


MEMORY INTERFACE



support 1Gbit
VRAM (64M X 16)

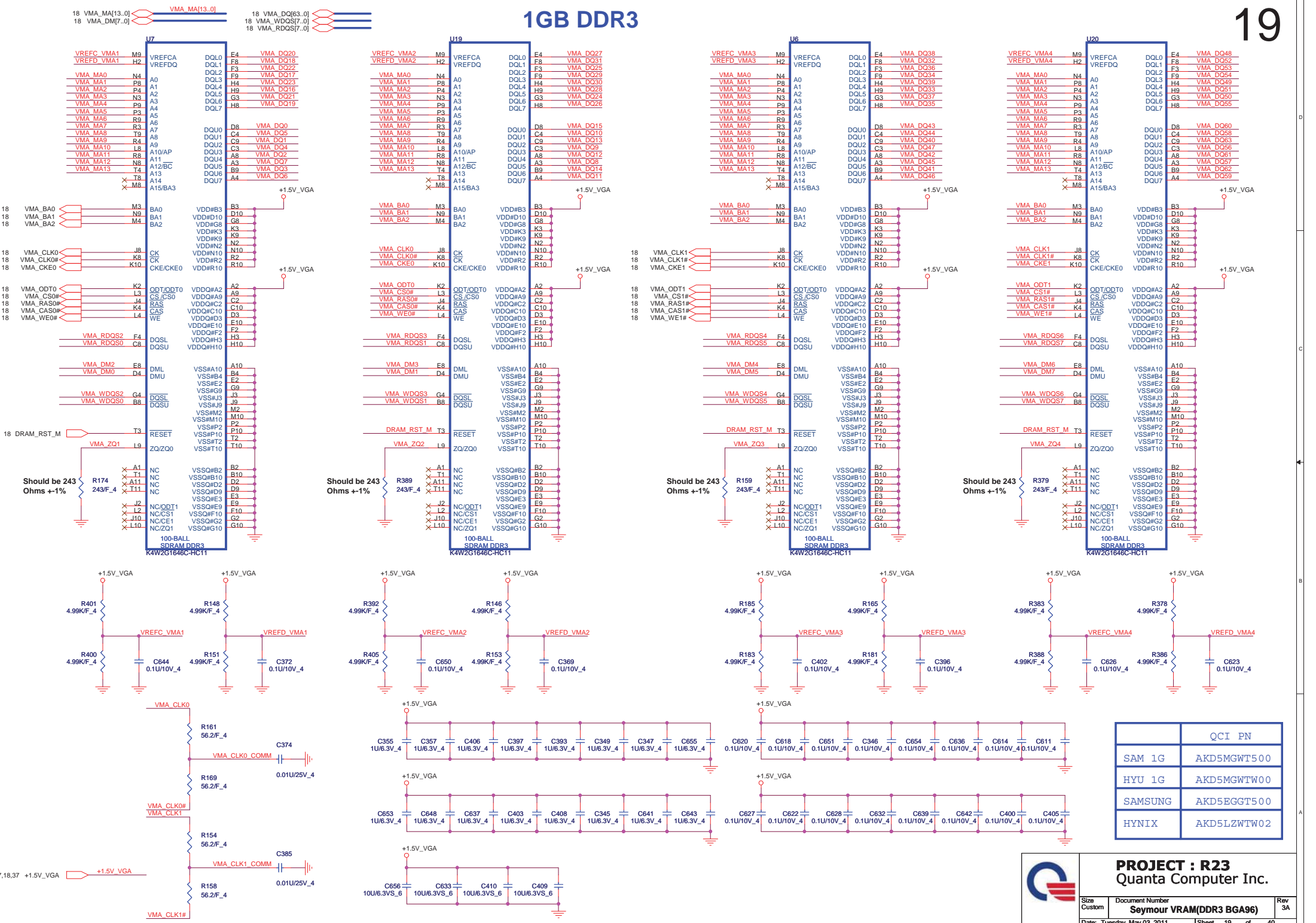
DIVIDER RESISTORS	GDDR5	DDR3
MVREF TO 1.8V (Ra)	40.2R	40.2R
MVREF TO GND (Rb)	100R	100R



PROJECT : R23
Quanta Computer Inc.

Size Custom	Document Number Seymour/MEM_Interface	Rev 1A
Date: Tuesday, May 03, 2011	Sheet 18	of 40

1GB DDR3

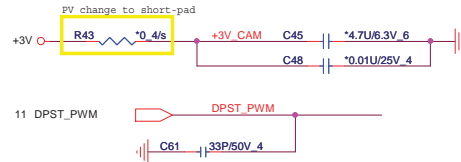
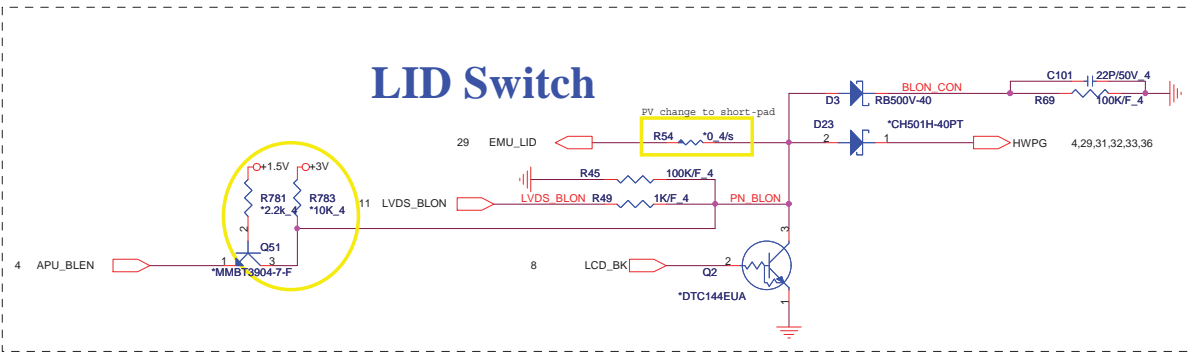


QCI PN	
SAM 1G	AKD5MGWT500
HYU 1G	AKD5MGWTW00
SAMSUNG	AKD5EGGT500
HYNIX	AKD5LZTWT02

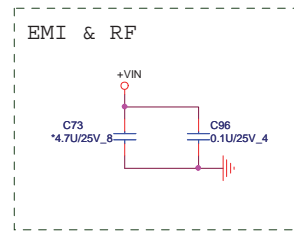
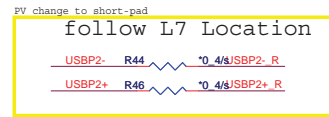
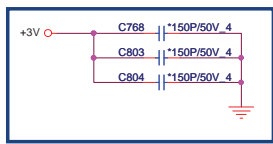
PROJECT : R23
Quanta Computer Inc.

Size Custom	Document Number	Rev 3A
	Seymour VRAM(DDR3 BGA96)	
Date: Tuesday, May 03, 2011	Sheet 19 of 40	

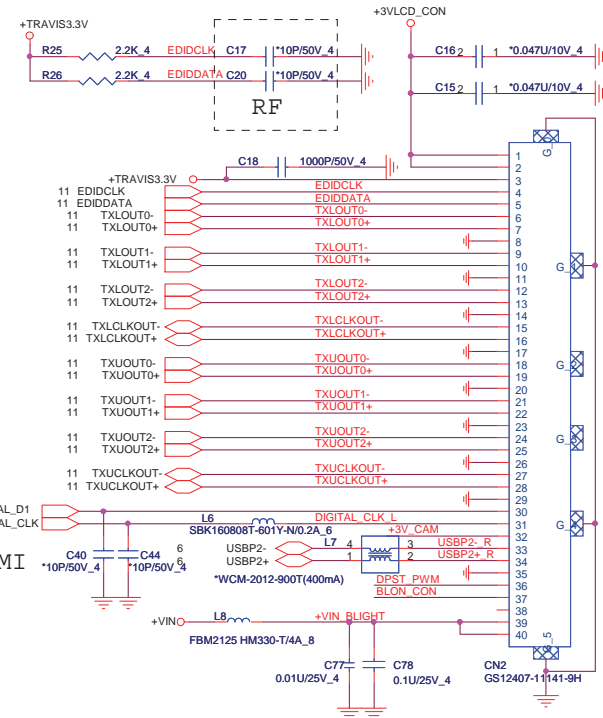
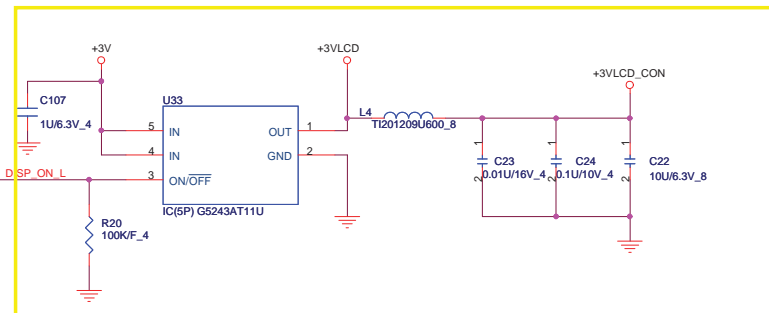
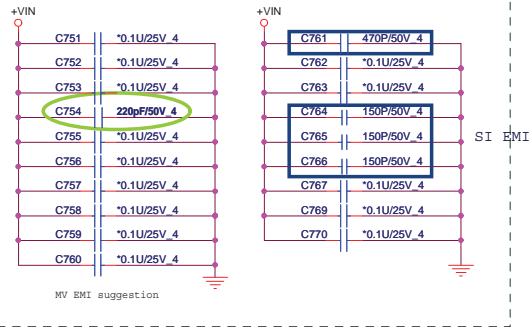
LID Switch



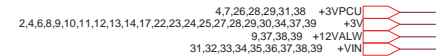
SI EMI



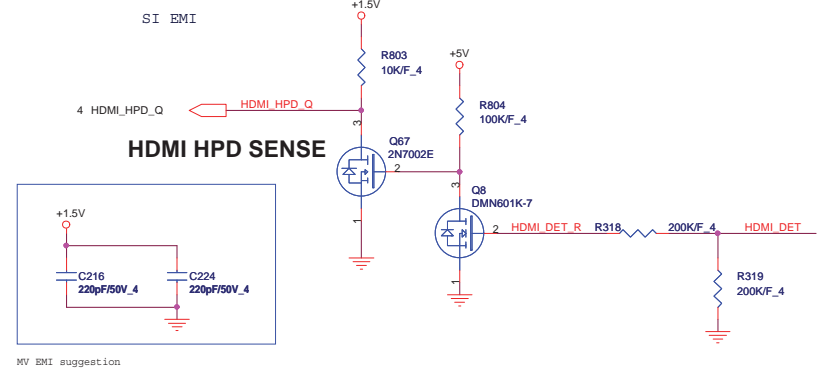
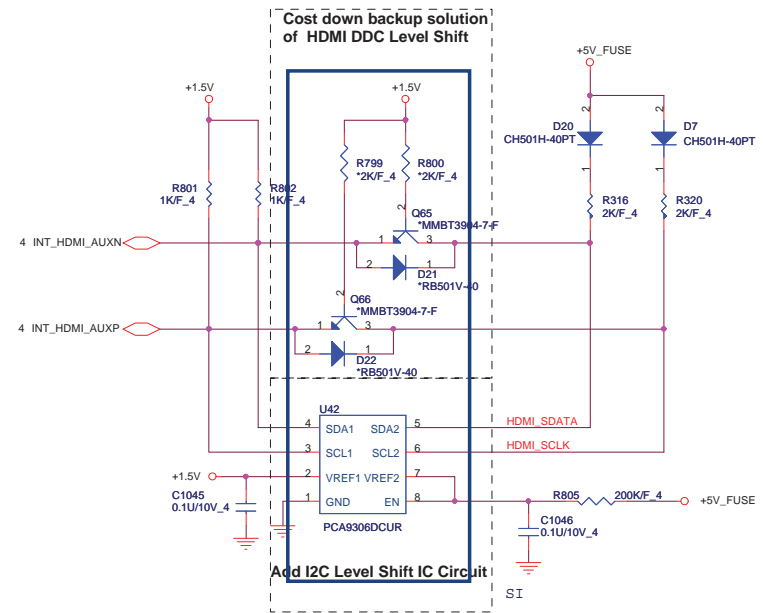
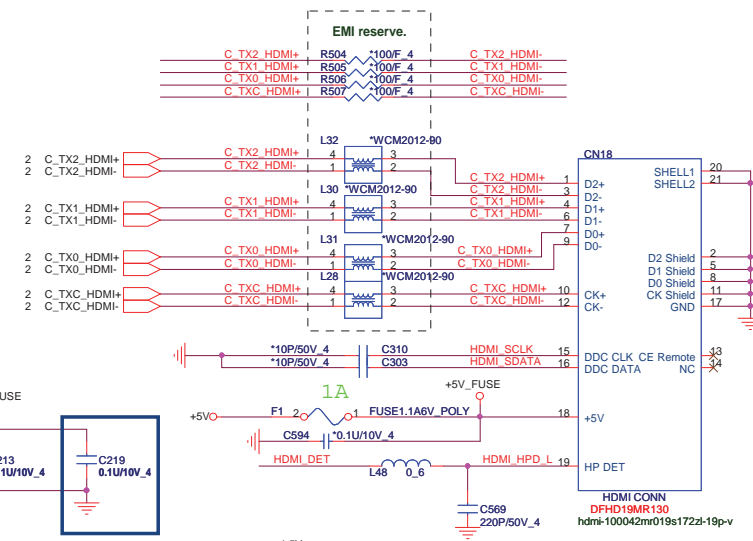
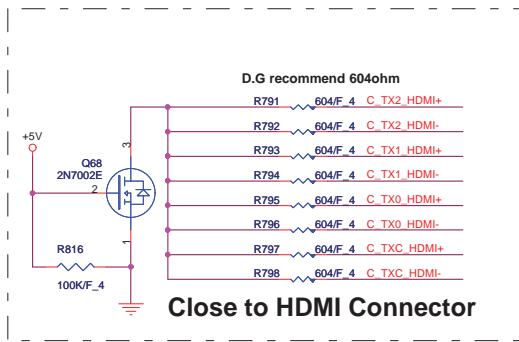
Coupling CAP.



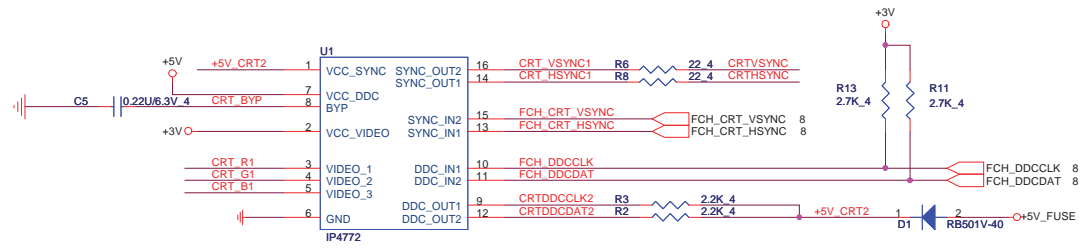
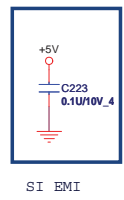
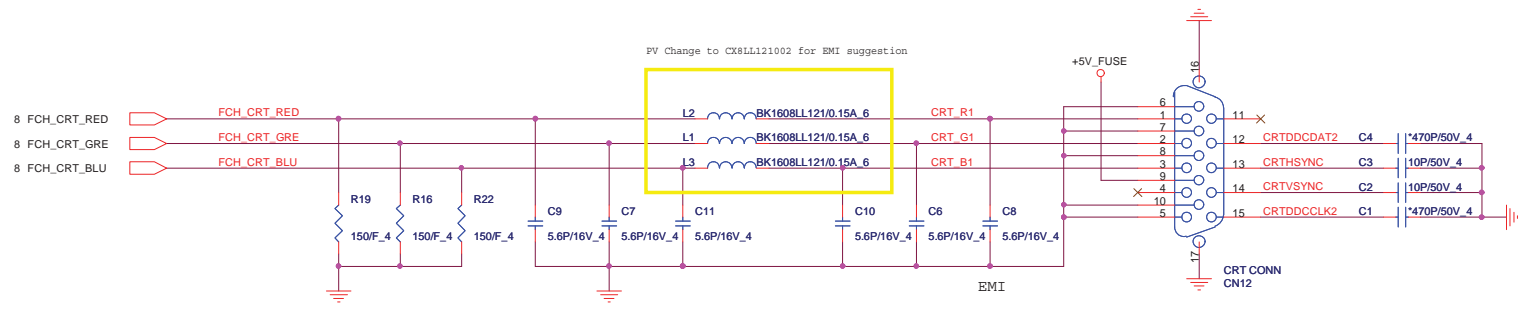
PV change for reduce circuit!



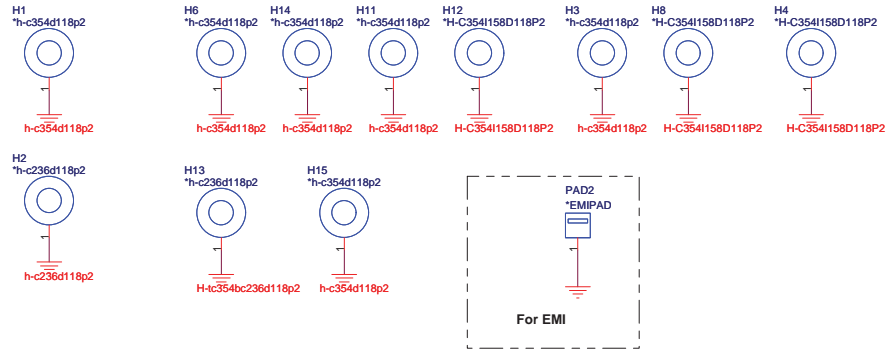
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		Quanta Computer Inc.	
Size Custom	Document Number	LCD CONN/LID/CAM	
Date: Tuesday, May 03, 2011	Sheet 20	Rev 1A	



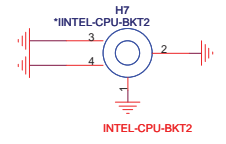
CRT PORT



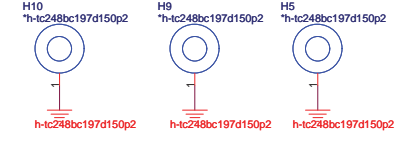
HOLE



CPU

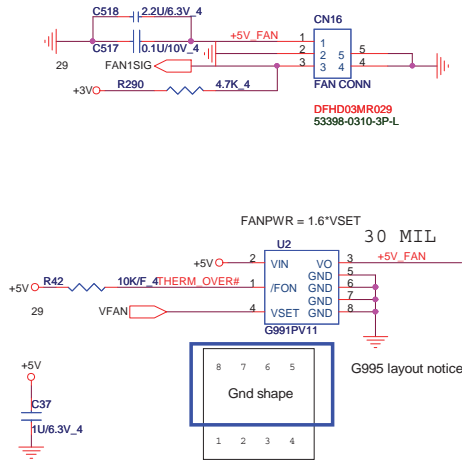


VGA

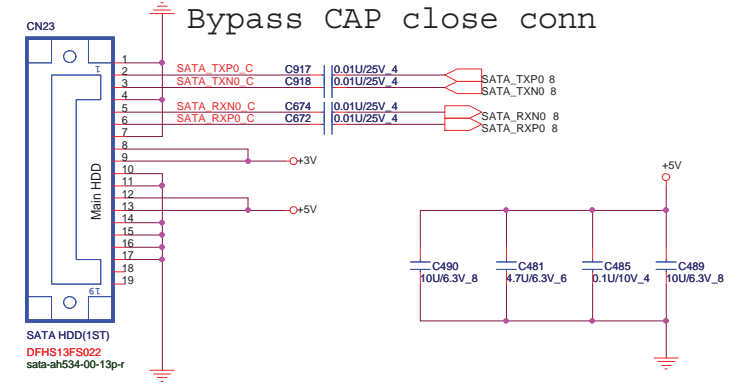


	PROJECT : R23	
	Quanta Computer Inc.	
	Size Custom	Document Number CRT,Hole
Date: Tuesday, May 03, 2011 Sheet 22 of 40		

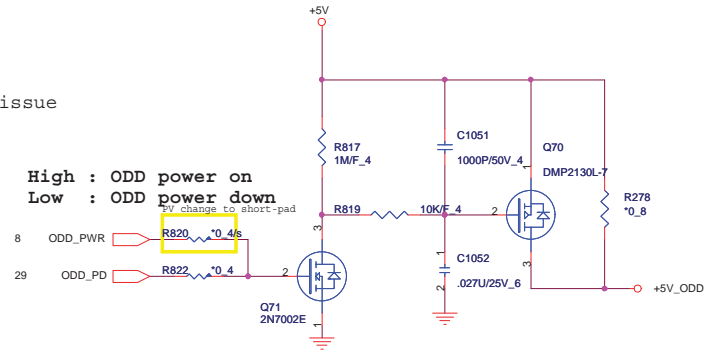
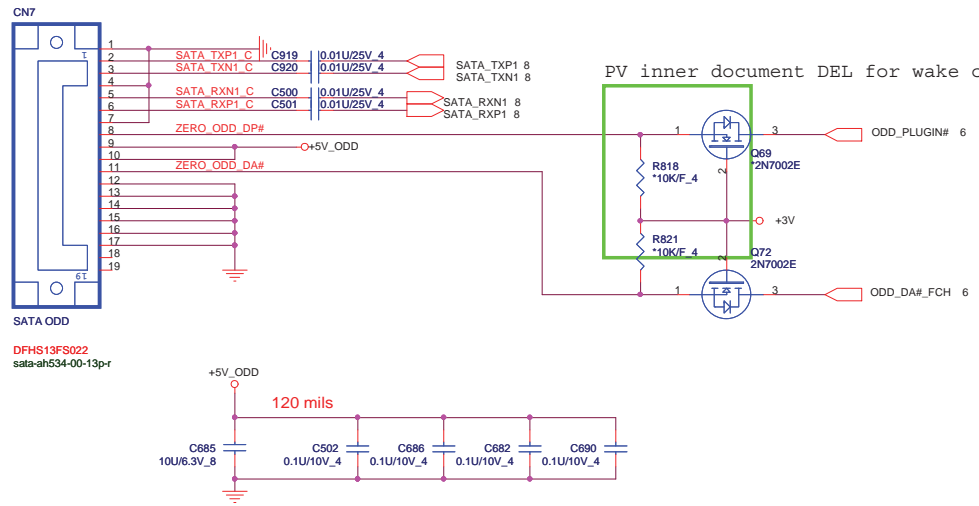
CPU FAN

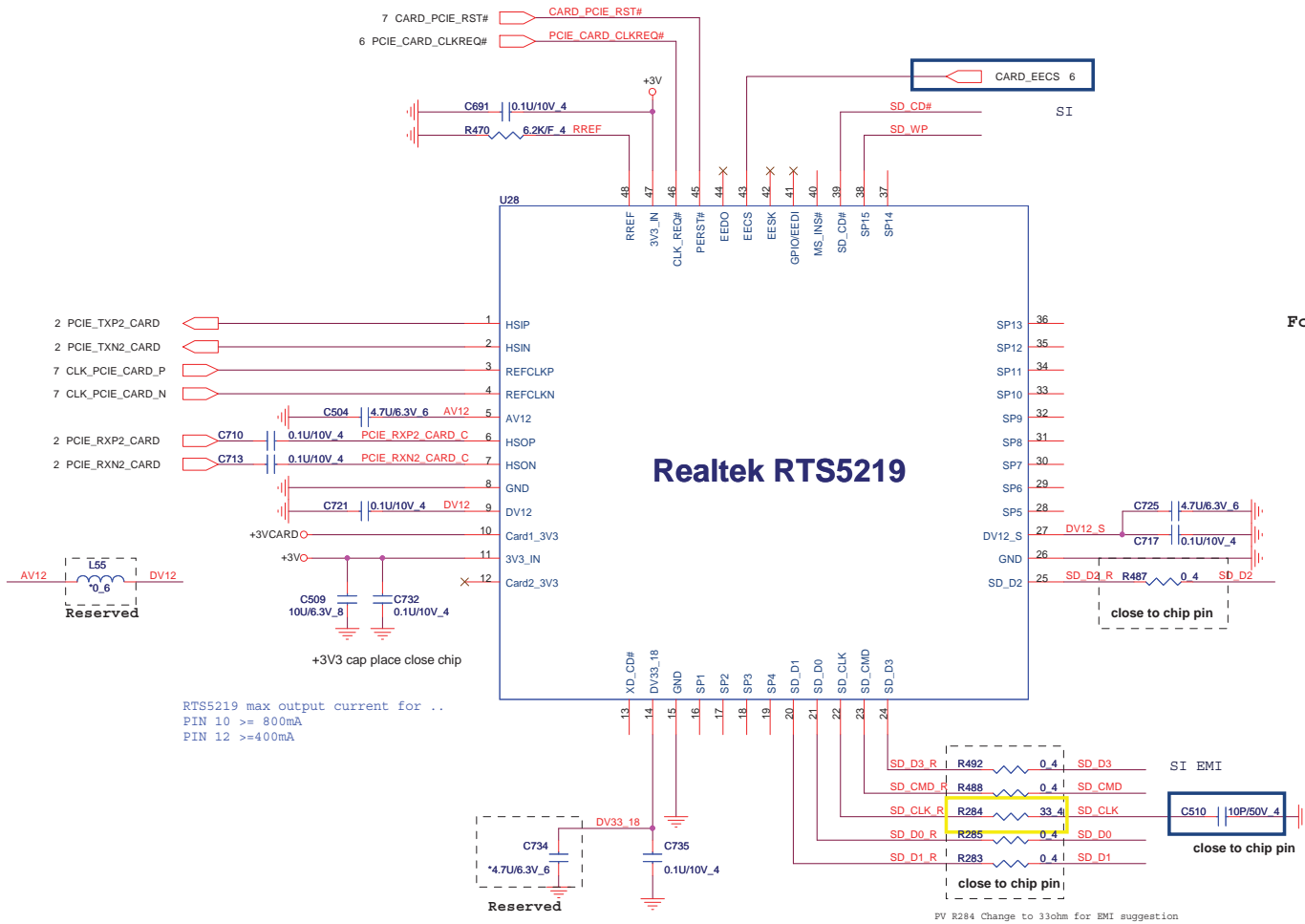


SATA HDD CONNECTOR

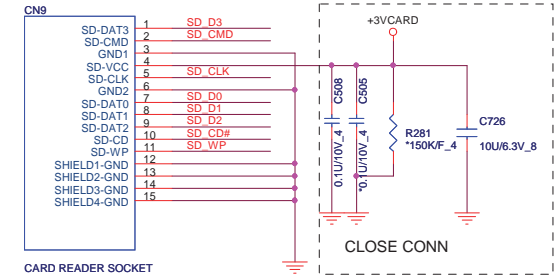


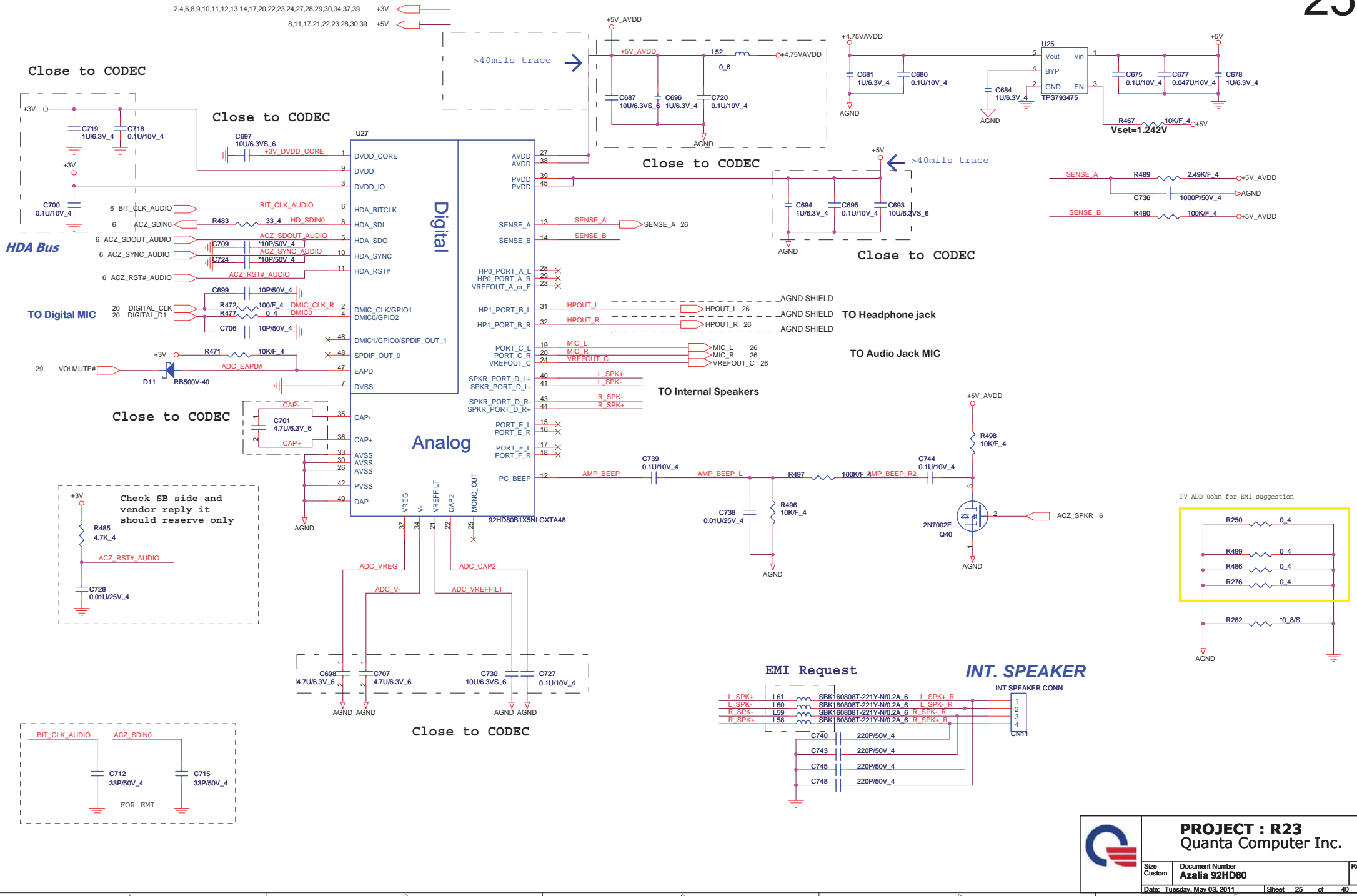
SATA ODD CONNECTOR SATA ODD





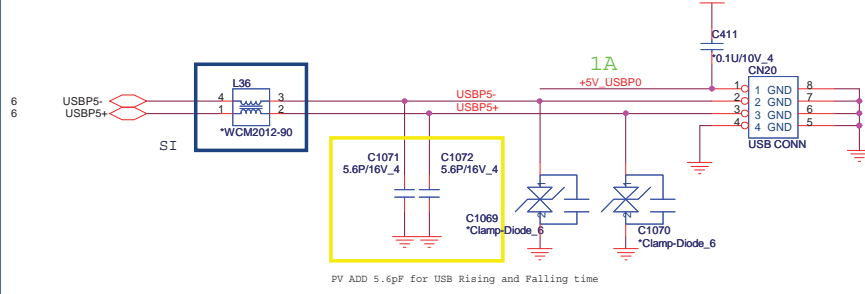
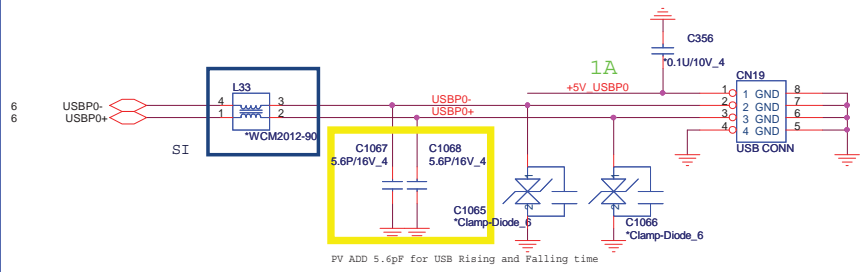
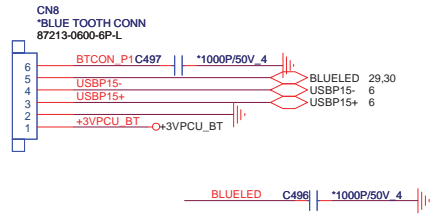
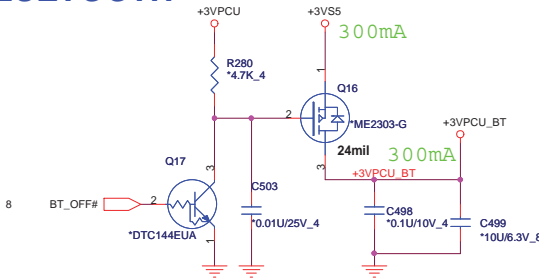
Footprint lqfp48-9x9-5-1_6h



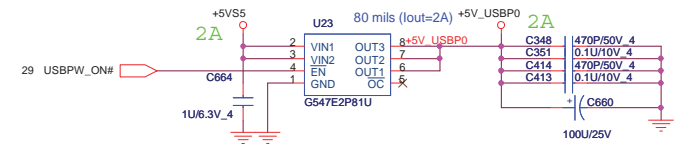


			PROJECT : R23 Quanta Computer Inc.	
			Size Custom Document Number Azalia 92HD80	Rev 1A
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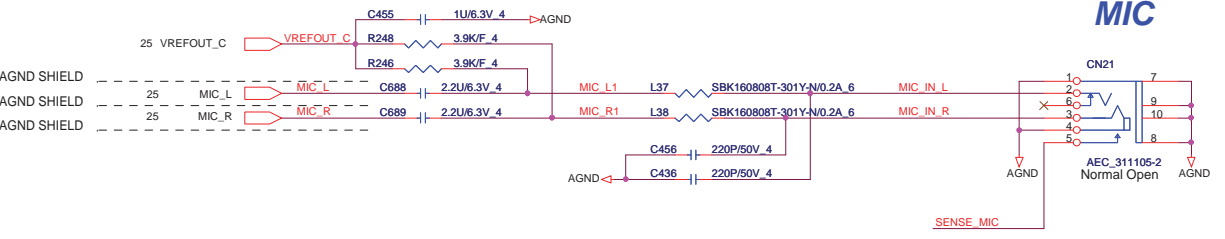
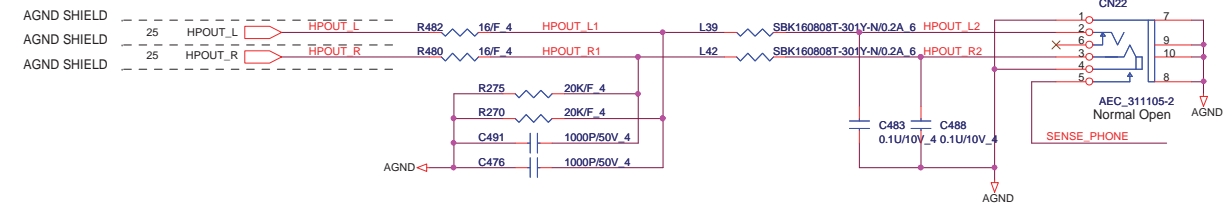
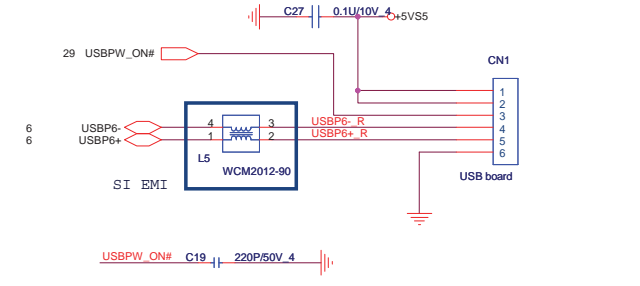
BLUETOOTH



LEFT SIDE USB2



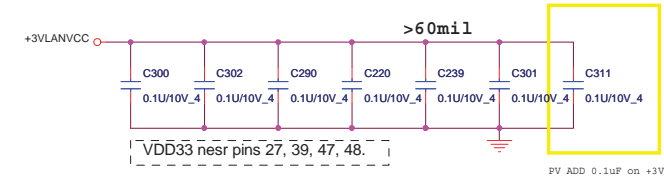
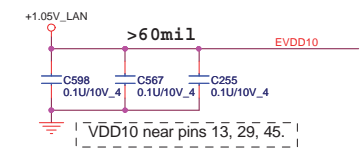
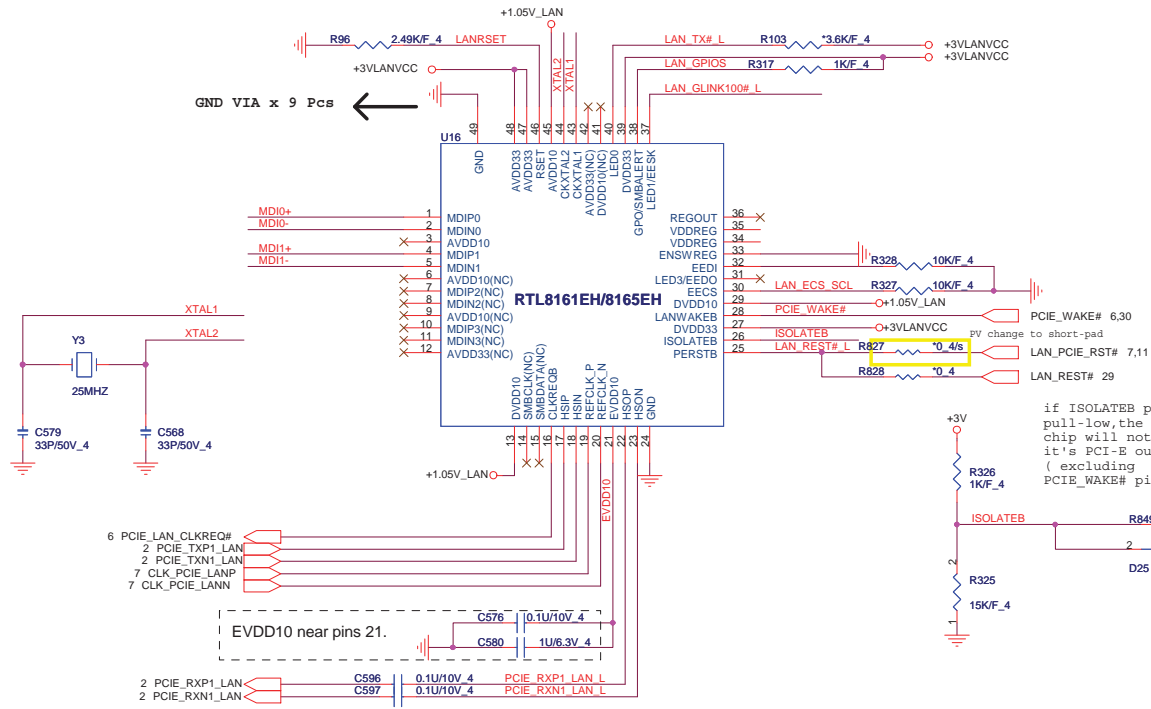
Right SIDE USB1



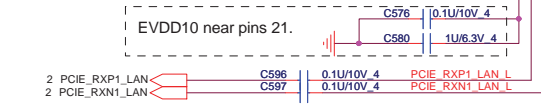
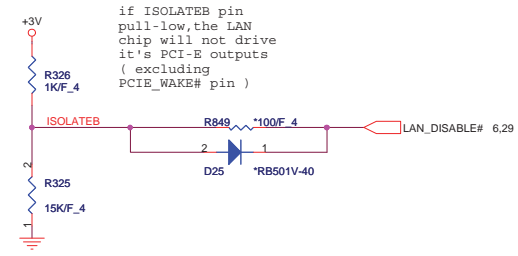
Line out

MIC

PROJECT : R23 Quanta Computer Inc.		
Size Custom	Document Number USB/BT/Audio Jack	Rev 1A
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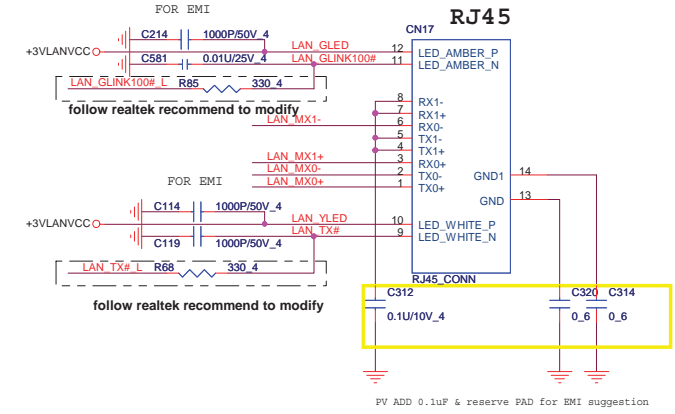
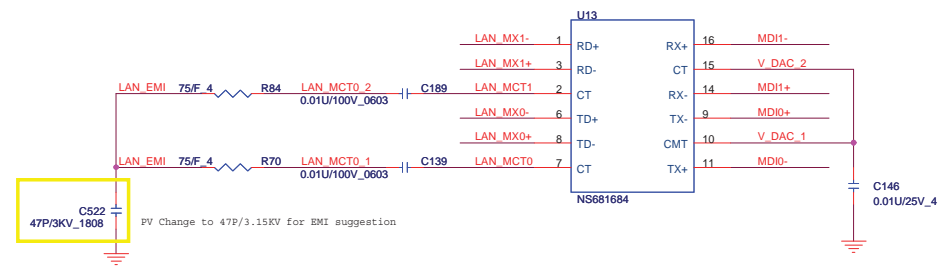


FV ADD 0.1uF on +3VLANVCC for EMI suggestion



Lan Con.

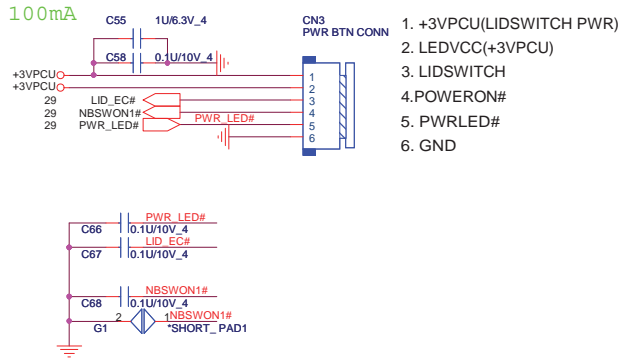
Transformer for 10/100



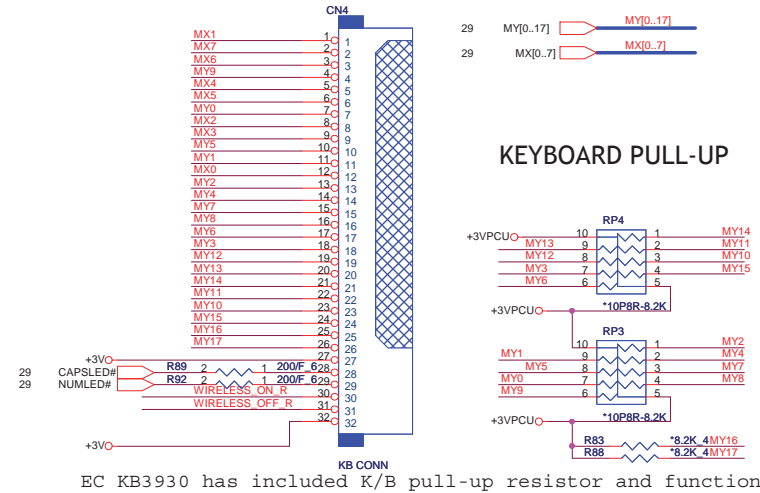
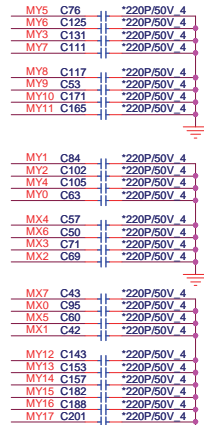
			PROJECT : R23 Quanta Computer Inc.	
			Size Custom Document Number RTL8165EH Date: Tuesday, May 03, 2011	Rev 1A Sheet 27 of 40



POWER BOTTON CONNECT

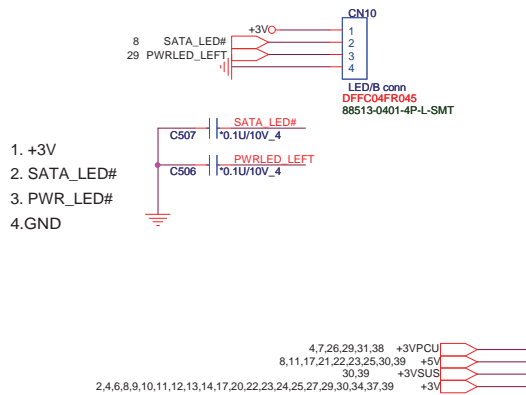


KEYBOARD Con.

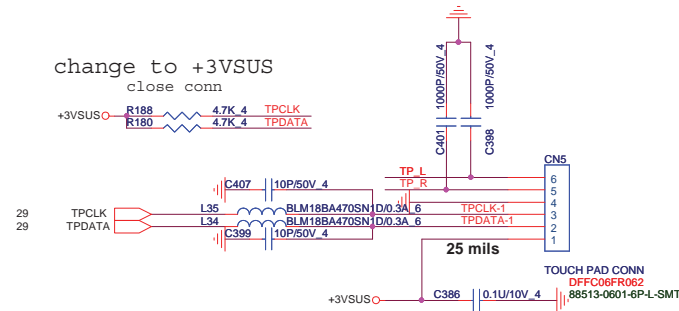


KEYBOARD PULL-UP

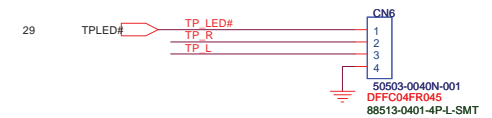
LED Con.

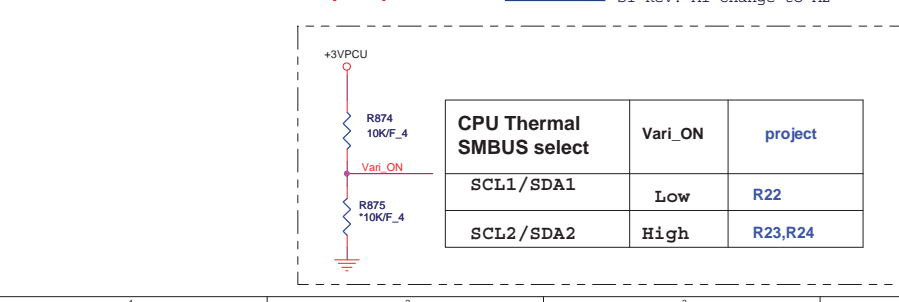
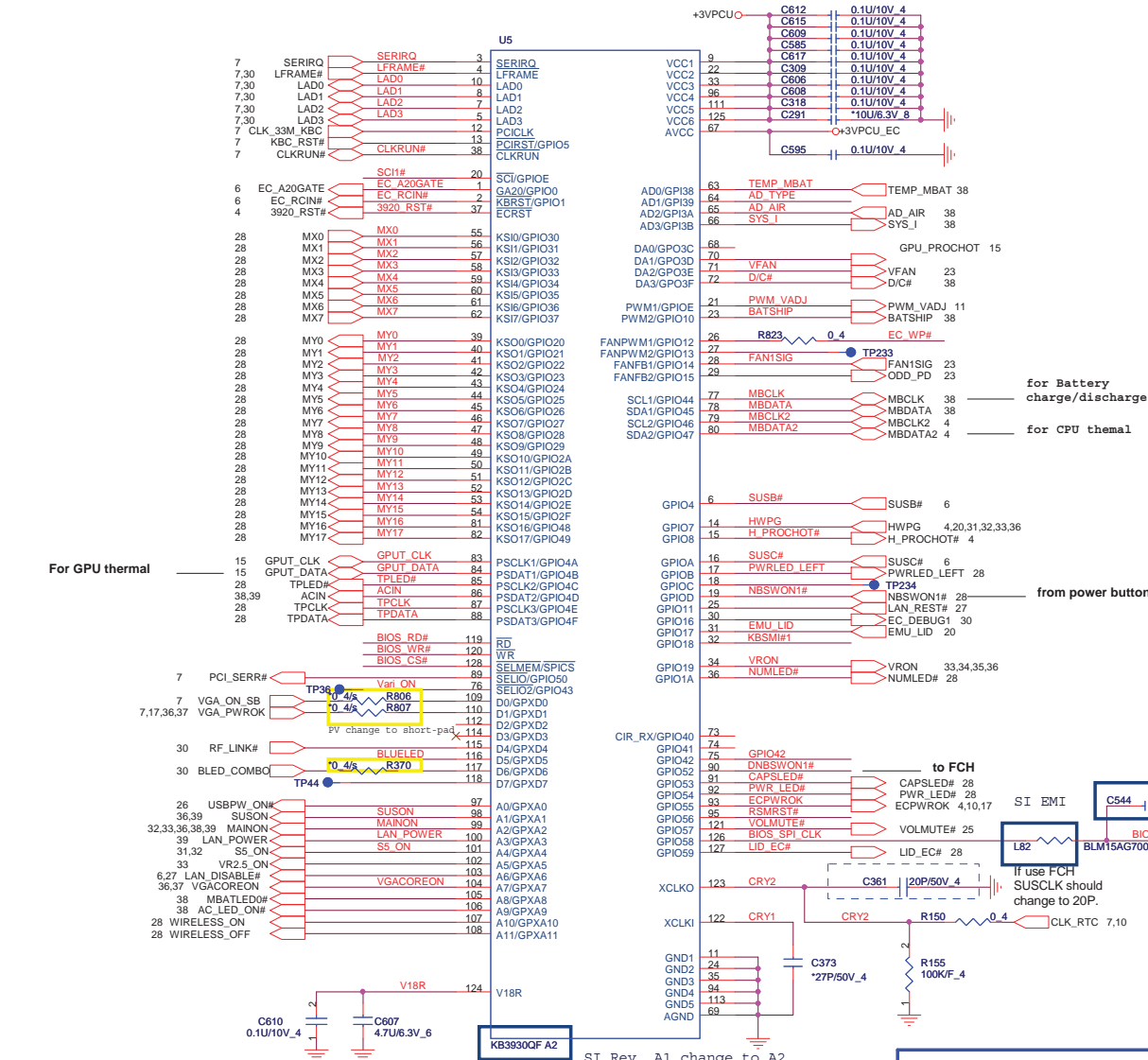
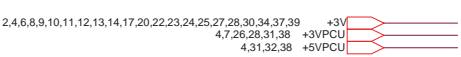


TOUCH PAD Con.

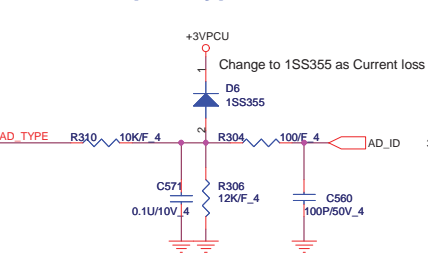


To TOUCH PAD SW board

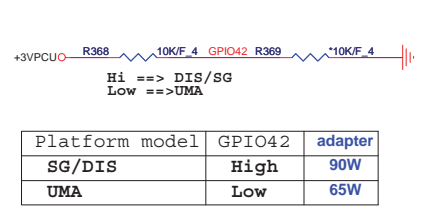




Smart adapter Type check

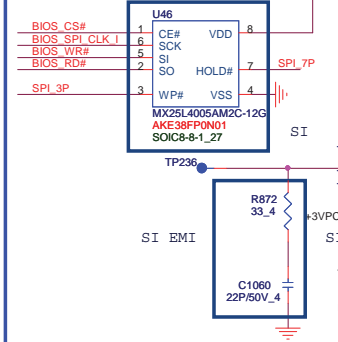


Adapter select

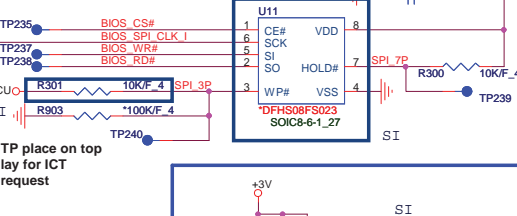


Vender	Size	P/N
AMIC	128K	AKE35ZN0801
EON	128K	AKE35FN0Q00
Socket		DFHS08FS023

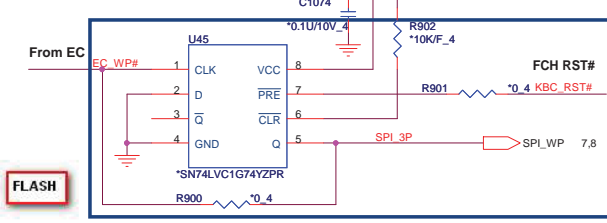
2M SPI EC ROM



128K byte SPI EC ROM



INPUTS				OUTPUTS	
PRE	CLR	CLK	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H (1)	H (1)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q ₀	Q̄ ₀



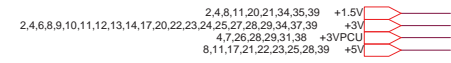
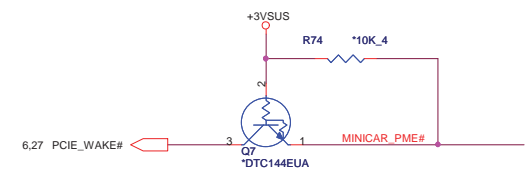
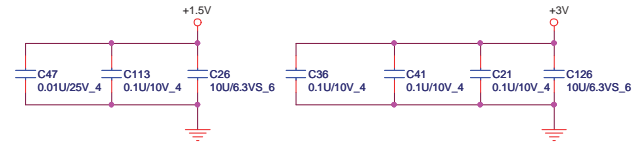
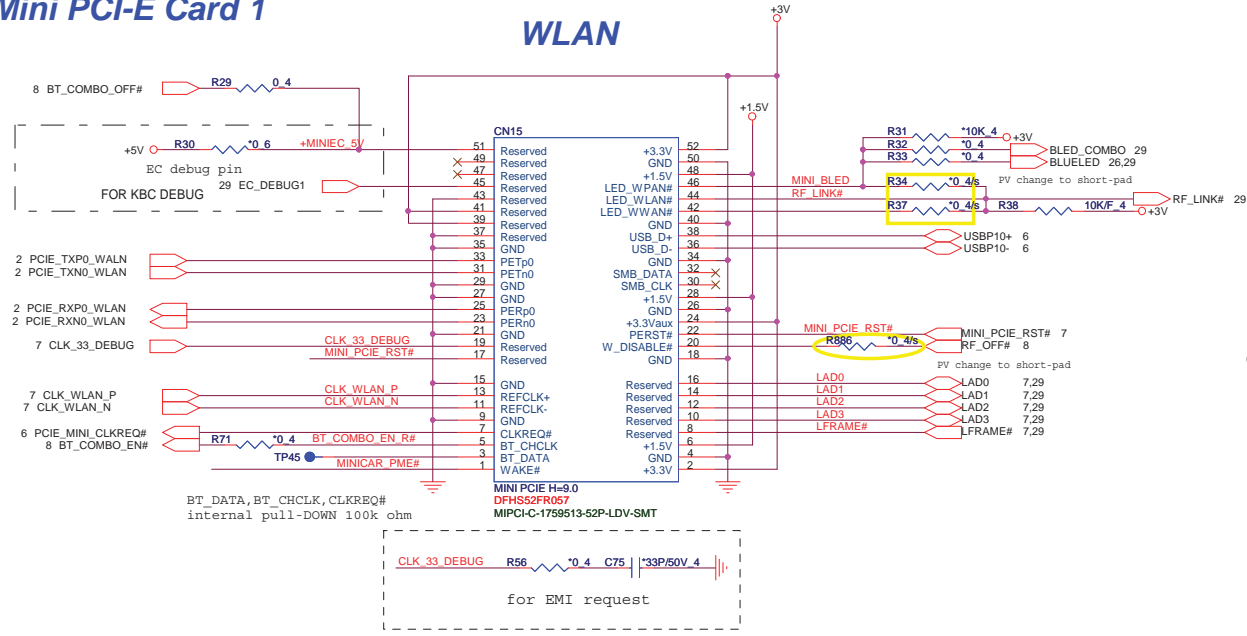
PROJECT : R23
Quanta Computer Inc.

Size Custom Document Number **EC (KB3926)/ROM** Rev 1A

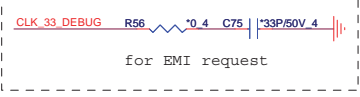
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Mini PCI-E Card 1

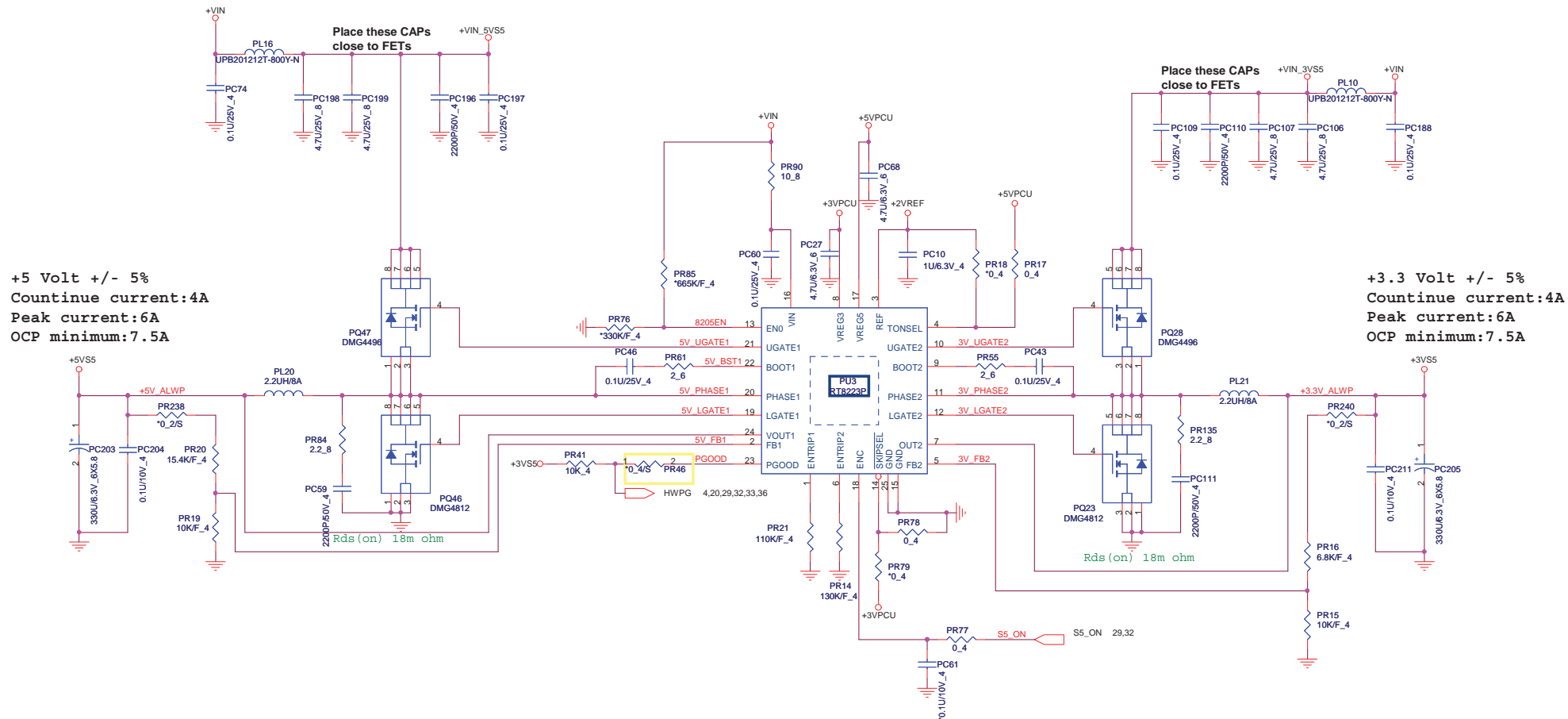
WLAN



BT_DATA, BT_CHCLK, CLKREQ#
internal pull-DOWN 100k ohm




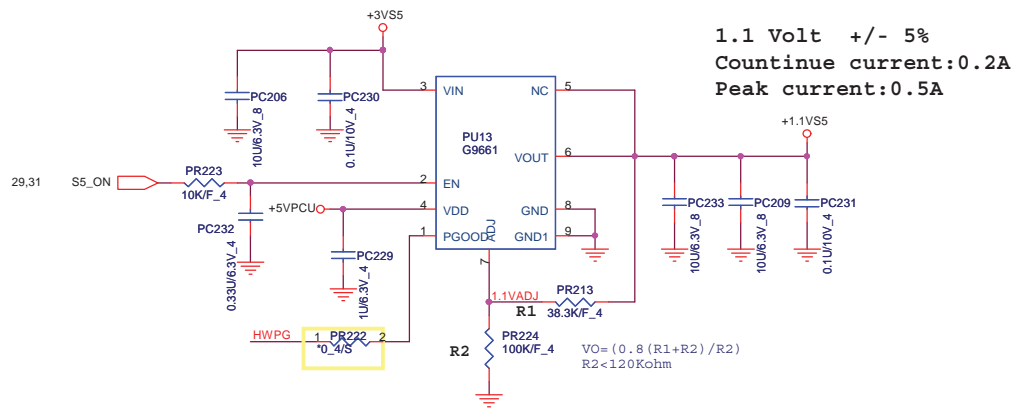
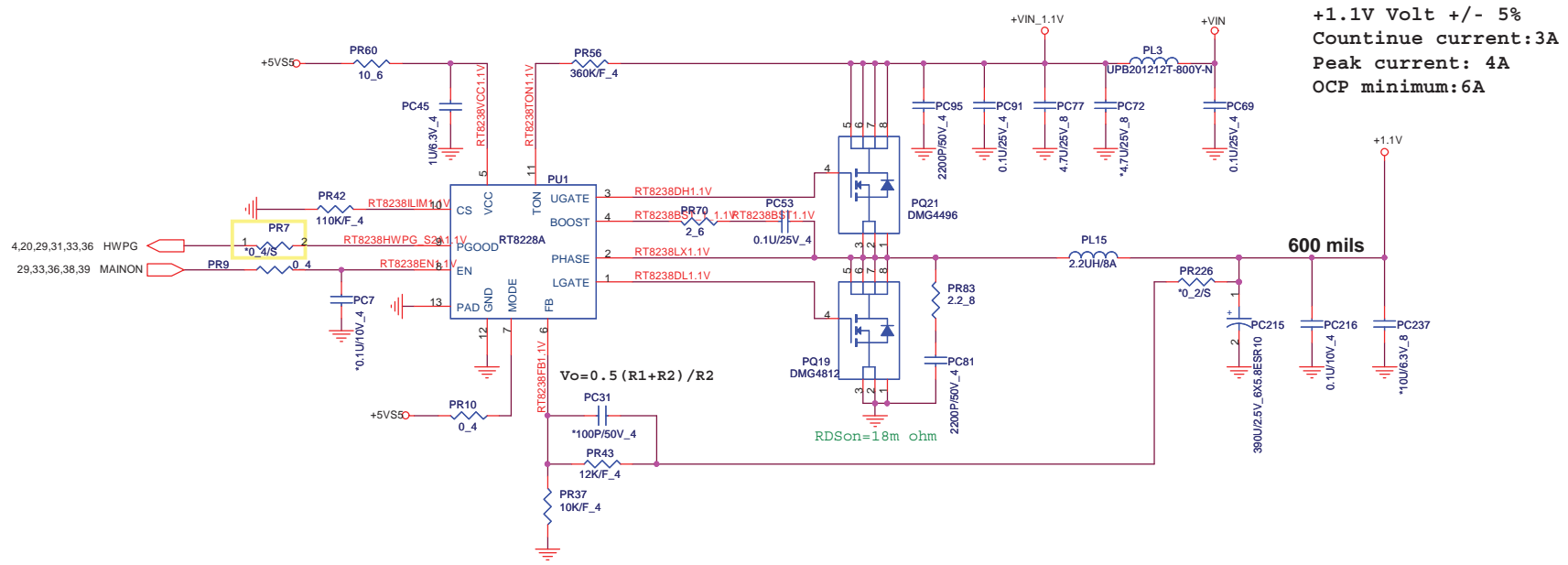
	PROJECT : R23		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number MINI PCI-E CONN X1	
Date: Tuesday, May 03, 2011		Sheet 30 of 40	

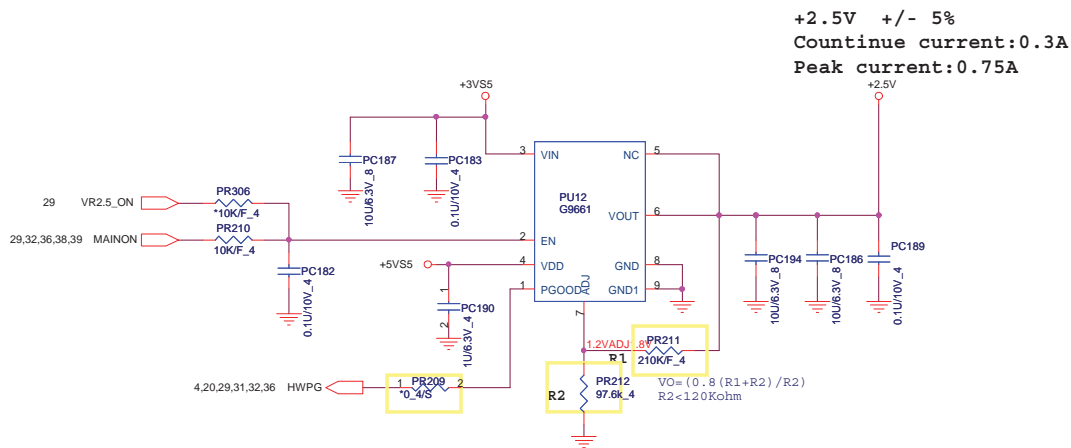
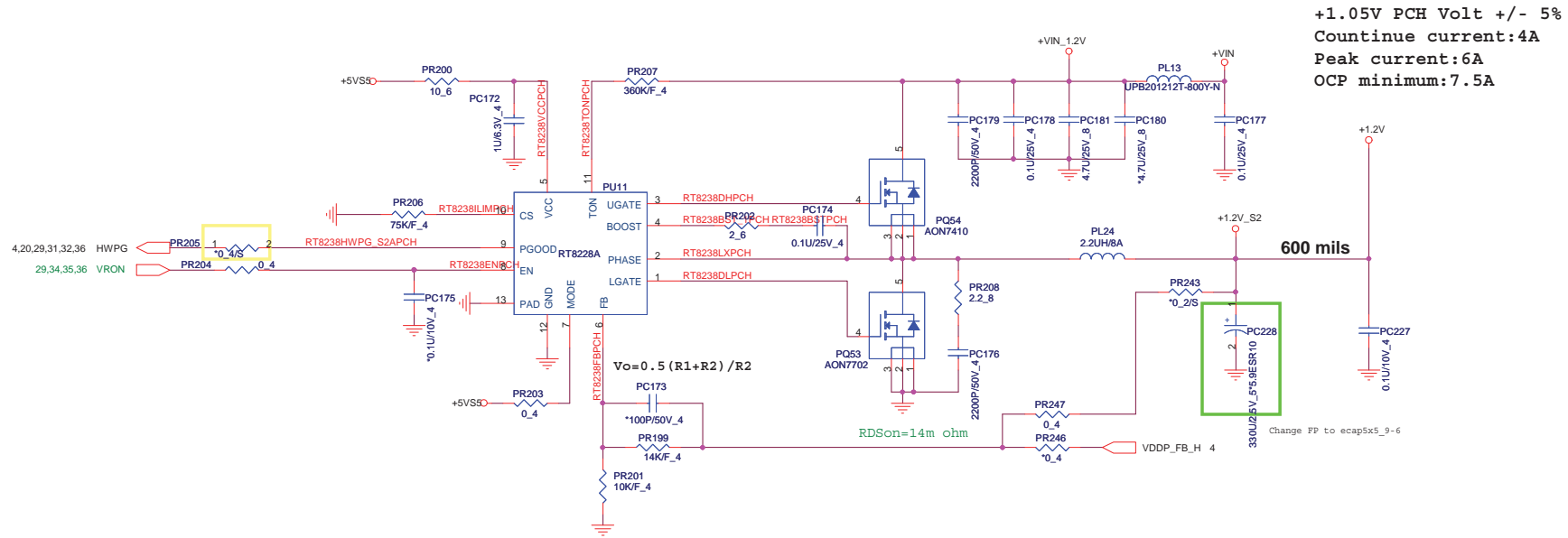



+5 Volt +/- 5%
 Countinue current:4A
 Peak current:6A
 OCP minimum:7.5A

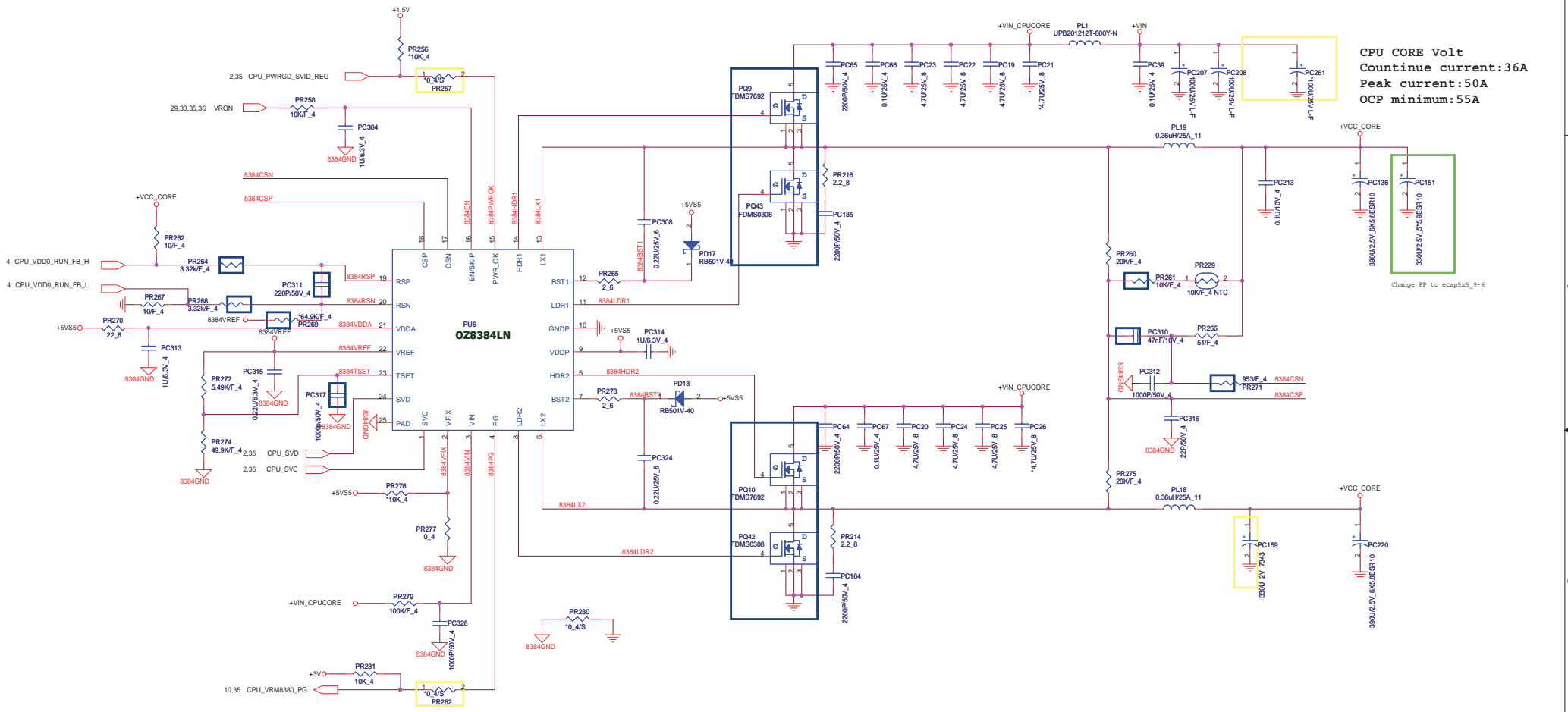
+3.3 Volt +/- 5%
 Countinue current:4A
 Peak current:6A
 OCP minimum:7.5A

 PROJECT : R23 Quanta Computer Inc.			
			Size Custom
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 PROJECT : R23 Quanta Computer Inc.		

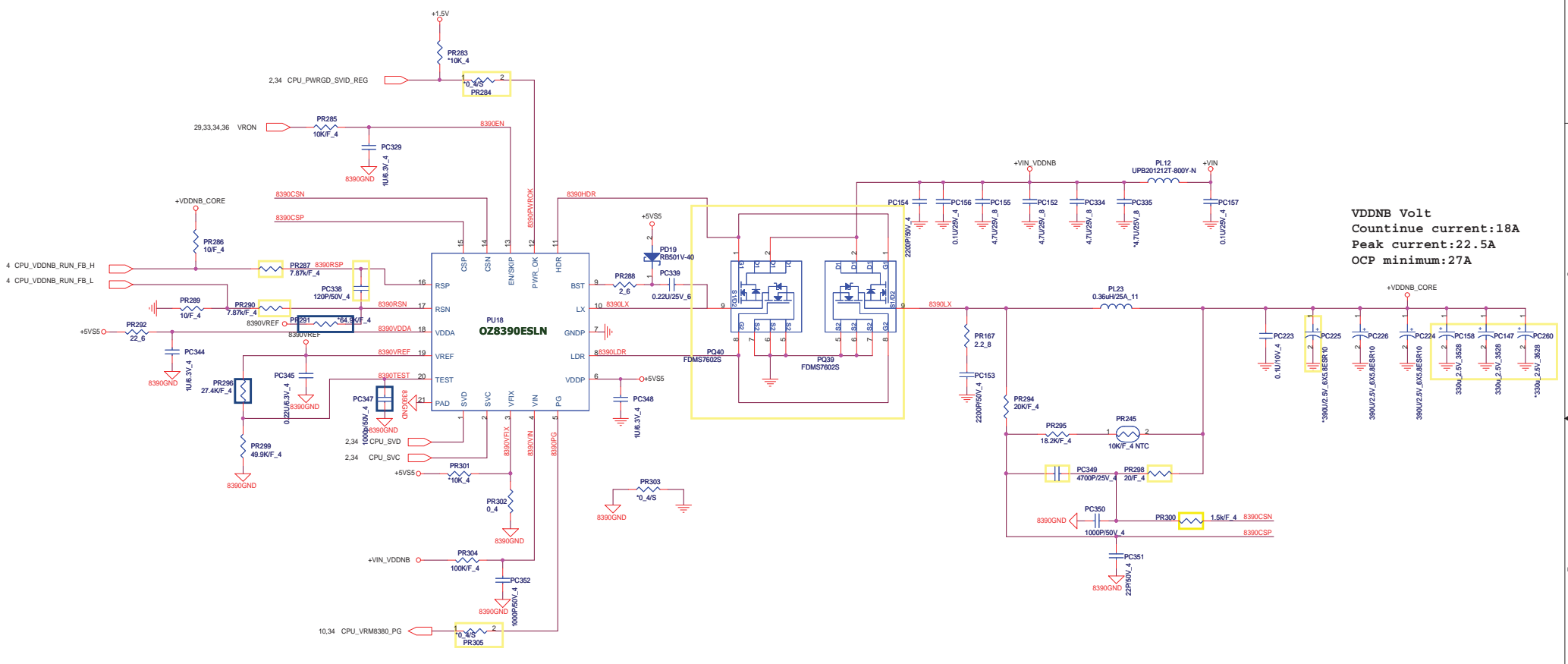


CPU CORE Volt
Countinue current:36A
Peak current:50A
OCP minimum:55A

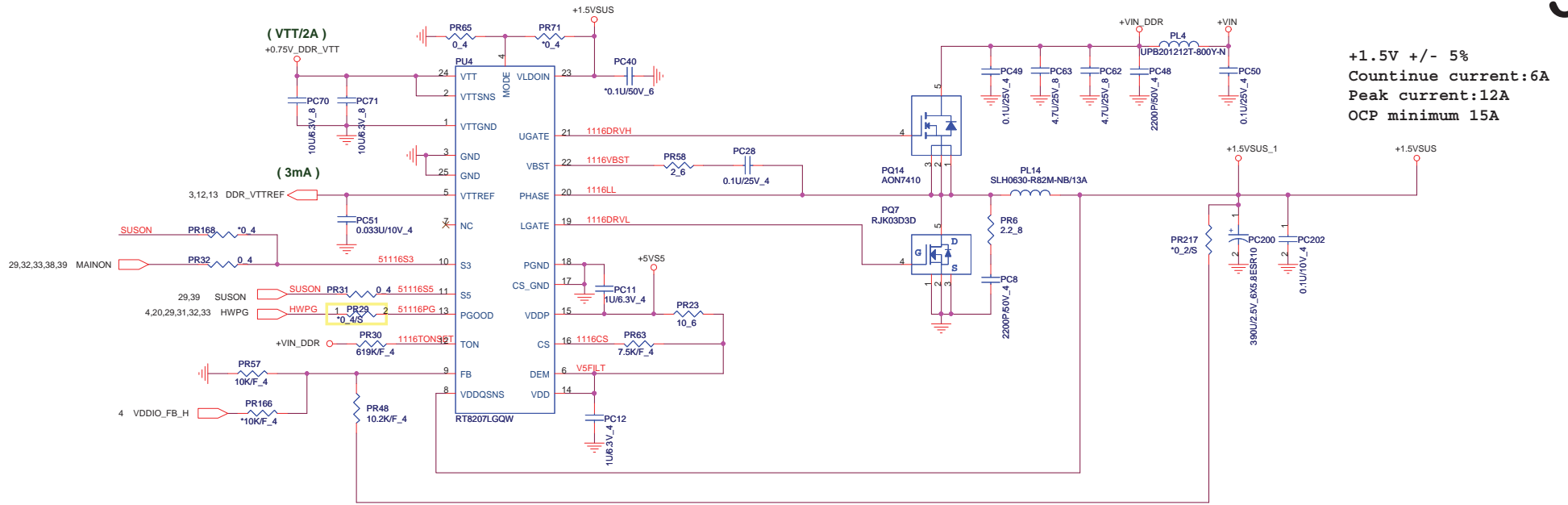


PROJECT : R23
Quanta Computer Inc.

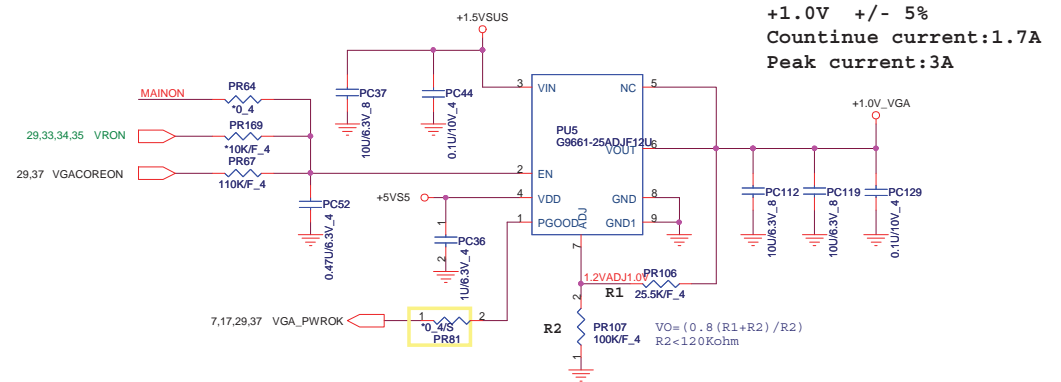
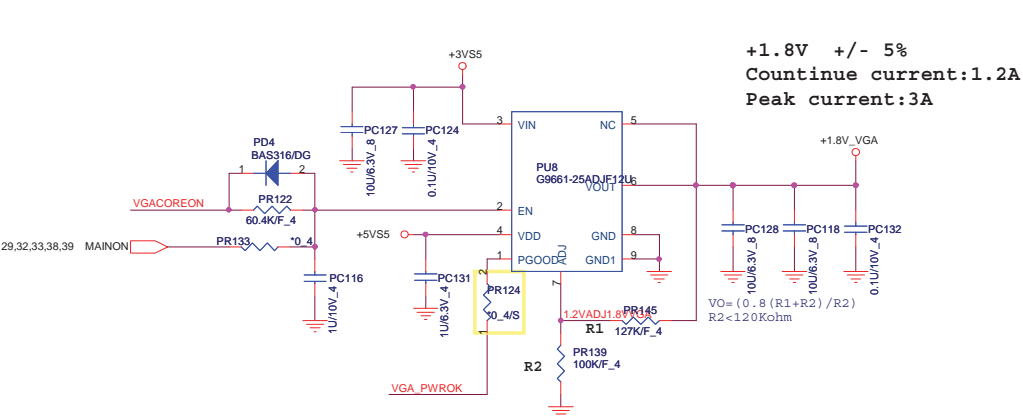
Size C	Document Number +1.1V VTT / PCH	Rev 1A
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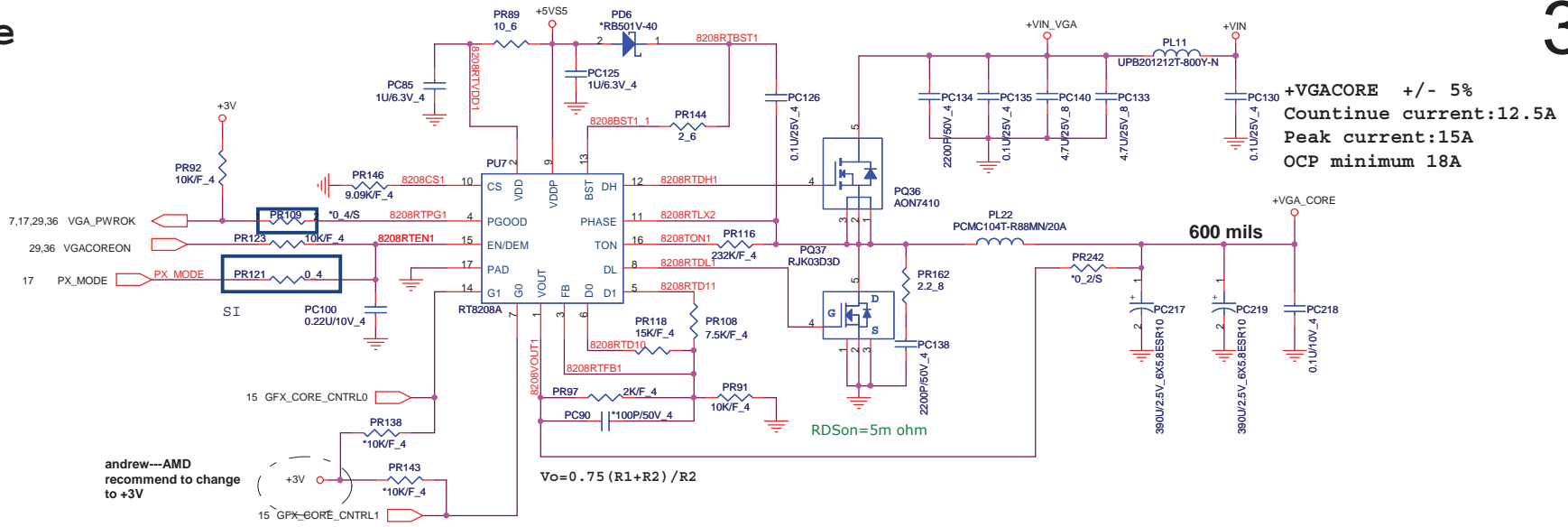
VDDNB Volt
 Countinue current:18A
 Peak current:22.5A
 OCP minimum:27A



SG & Discrete Only

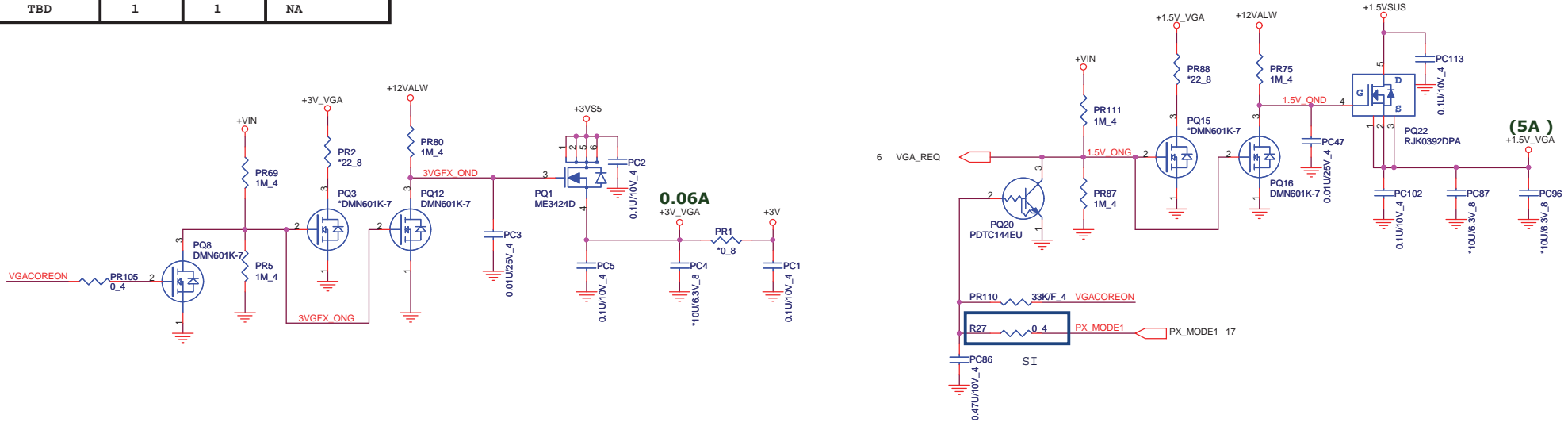


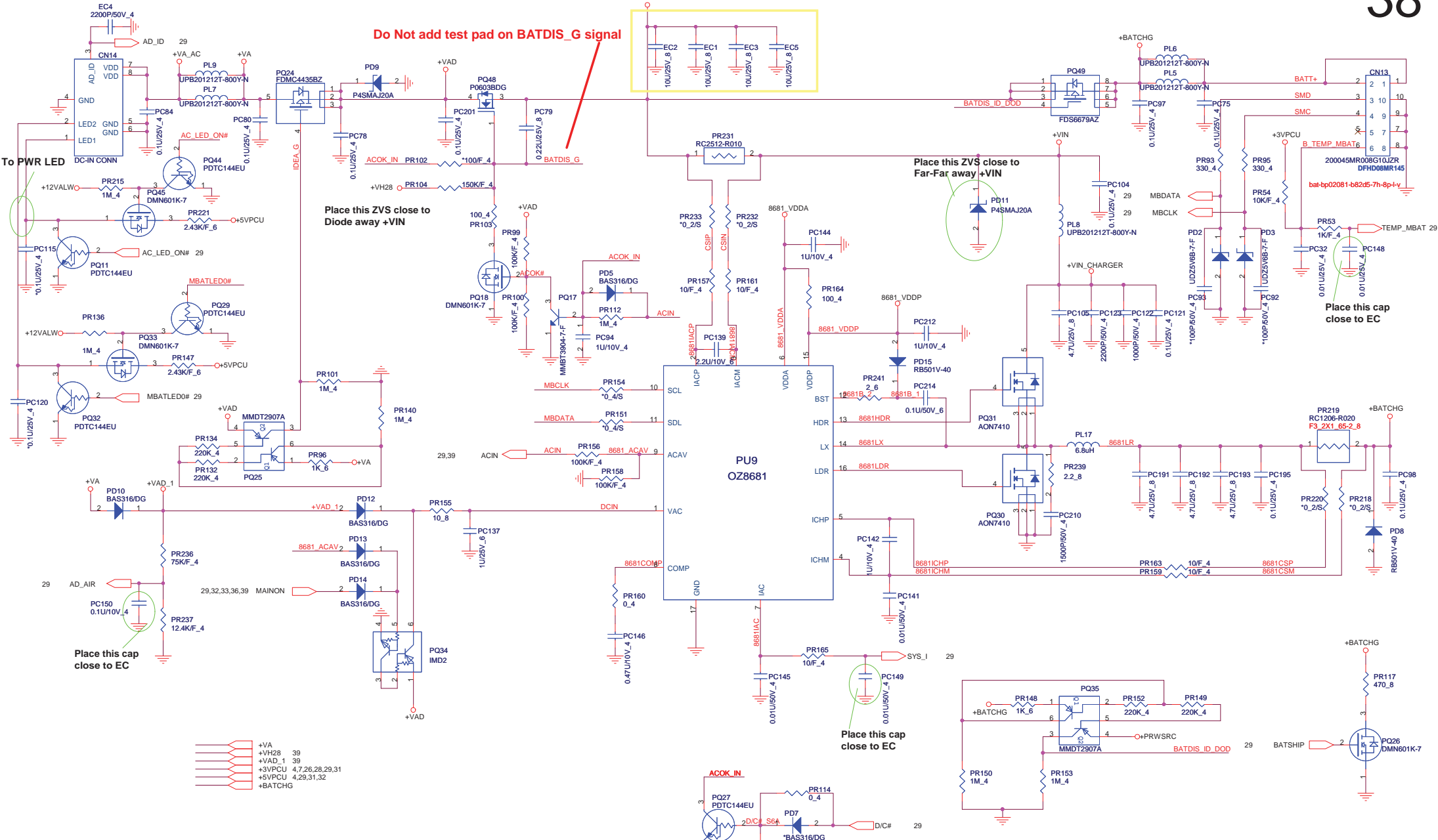
 PROJECT : R23 Quanta Computer Inc.		
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andrew---AMD
 recommend to change
 to +3V

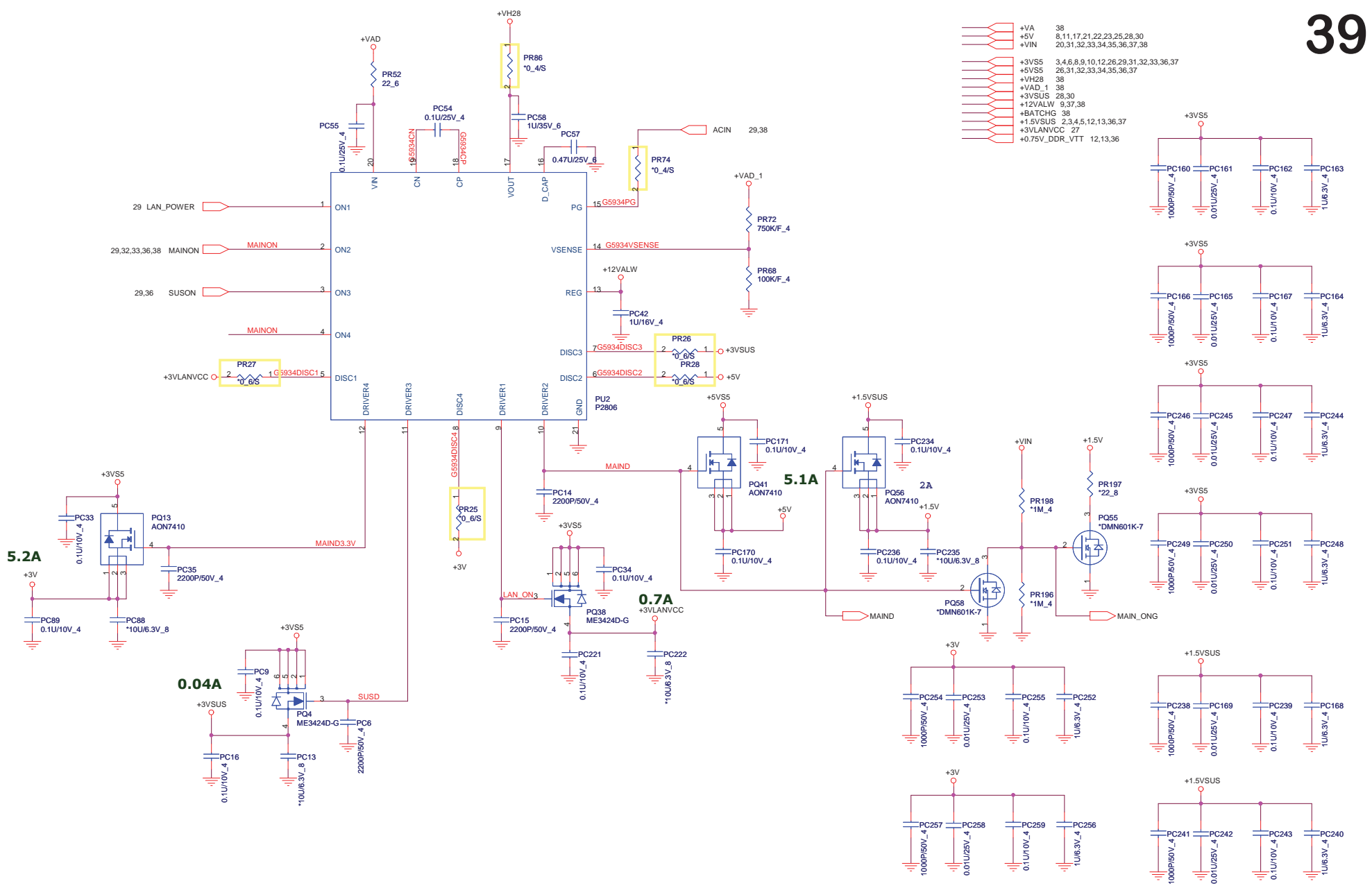
Seymour-XT	PWRCNTL0	PWRCNTL1	V-CORE
L	0	0	0.9V
M	0	1	1V
H	1	0	1.1V (Default)
TBD	1	1	NA






- +VA
- +VH28 39
- +VAD_1 39
- +3VPCU 4,7,26,28,29,31
- +5VPCU 4,29,31,32
- +BATCHG

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- +VA 38
- +5V 8,11,17,21,22,23,25,28,30
- +VIN 20,31,32,33,34,35,36,37,38
- +3VS5 3,4,6,8,9,10,12,26,29,31,32,33,36,37
- +5VS5 26,31,32,33,34,35,36,37
- +VH28 38
- +VAD_1 38
- +3VSUS 28,30
- +12VALW 9,37,38
- +BATCHG 38
- +1.5VSUS 2,3,4,5,12,13,36,37
- +3VLAVCC 27
- +0.75V_DDR_VTT 12,13,36

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