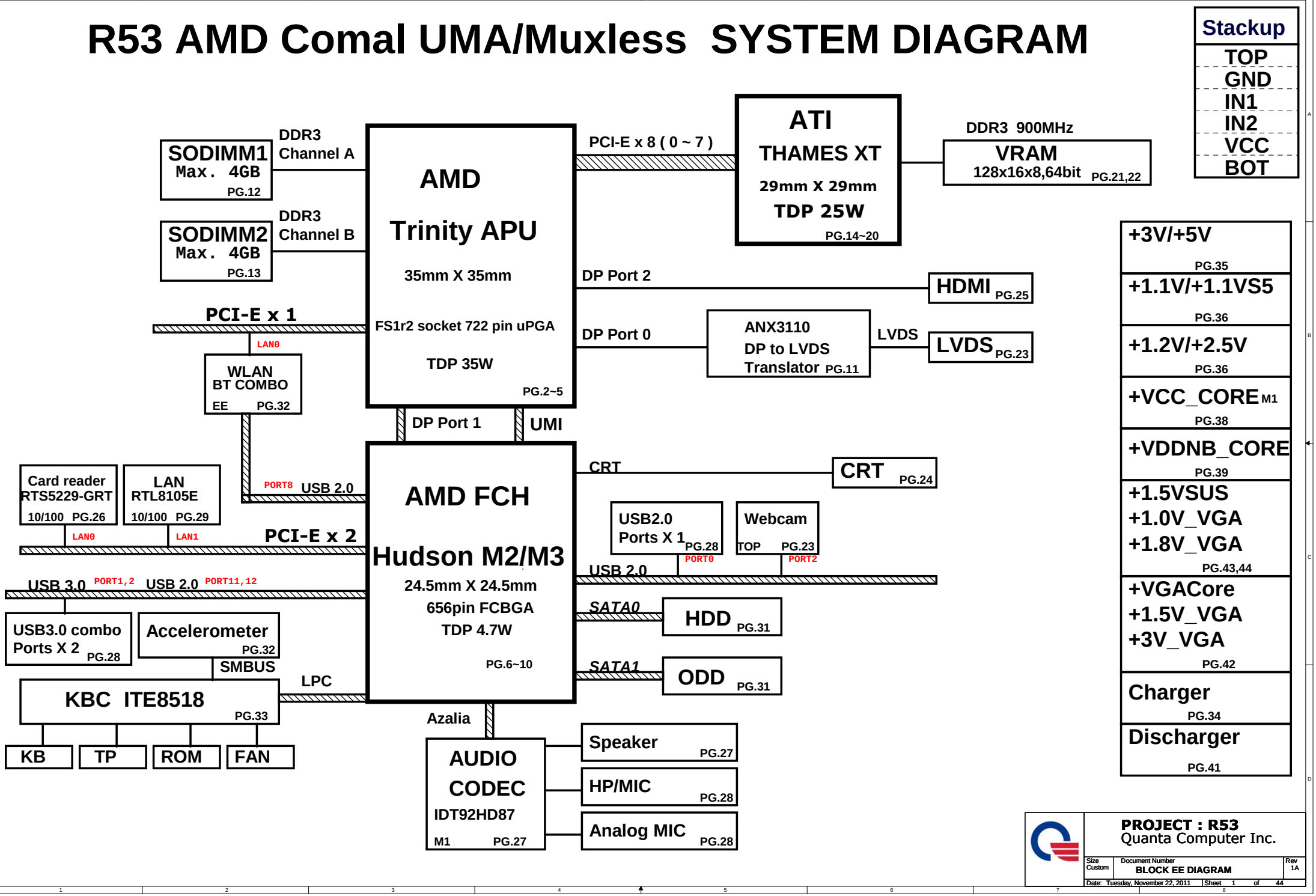
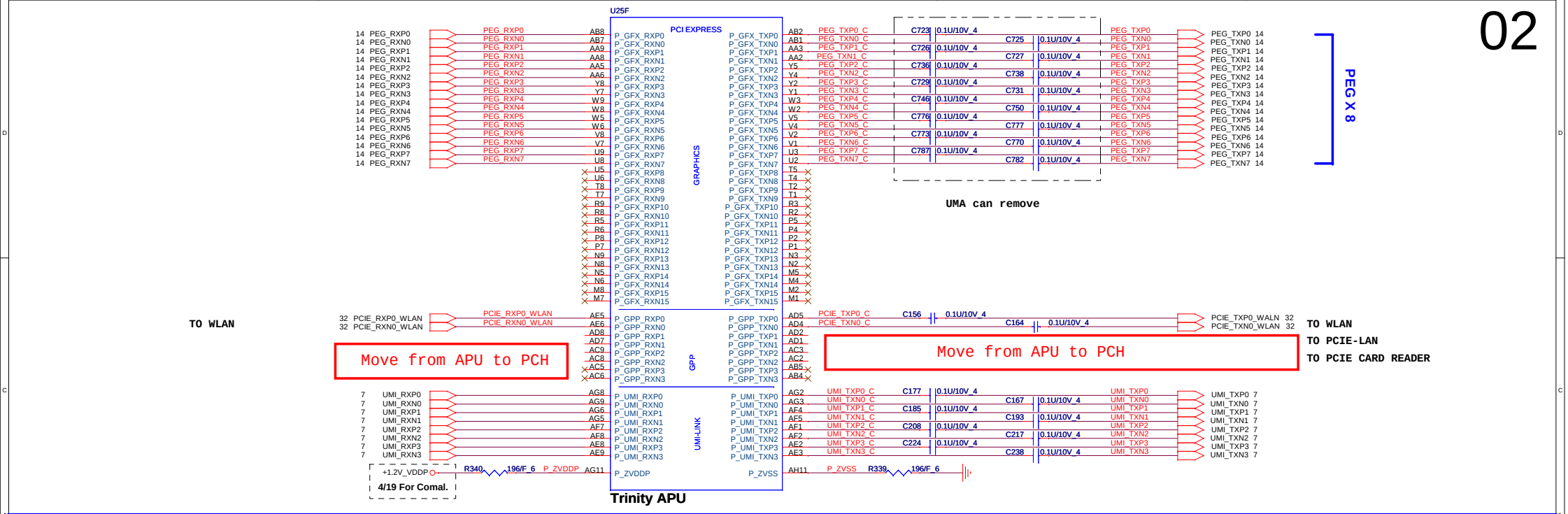
R53 AMD Comal UMA/Muxless SYSTEM DIAGRAM



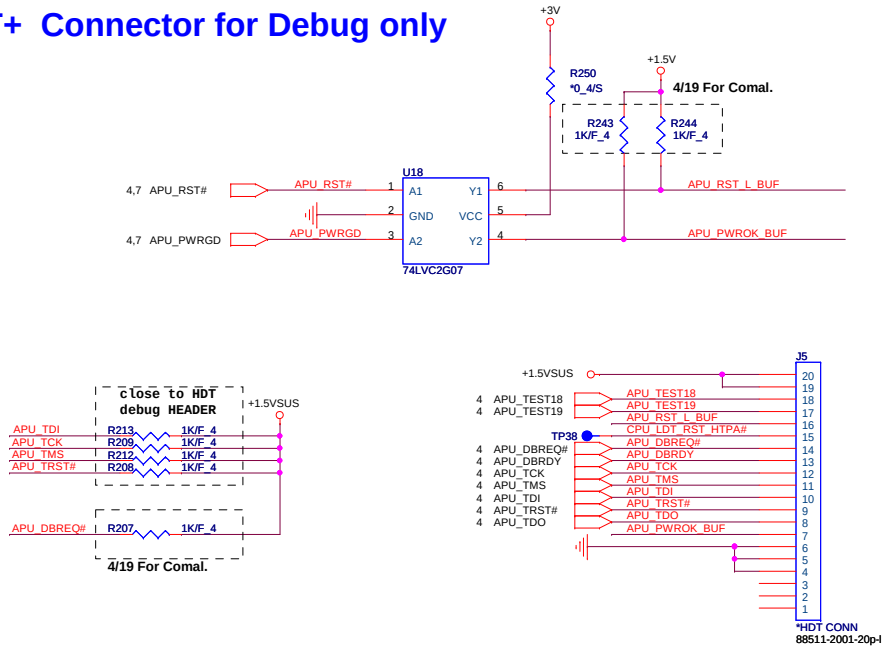
PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK EE DIAGRAM	1A

Date: Tuesday, November 22, 2011 Sheet 1 of 44



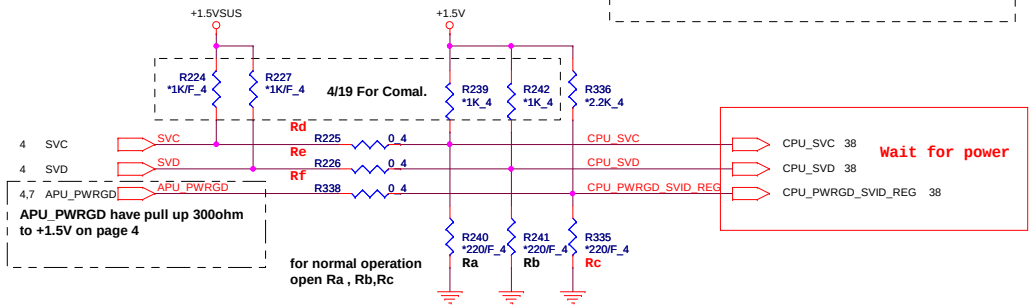
HDT+ Connector for Debug only



VID Override Circuit

	BOOT VOLTAGE		
SVC	SVD	VFIX_+VDD =VCC/GND	VFIX_+VDD =OPEN
0	0	1.1	1.1
0	1	1.0	1.2
1	0	0.9	1.0
1	1	0.8	0.8

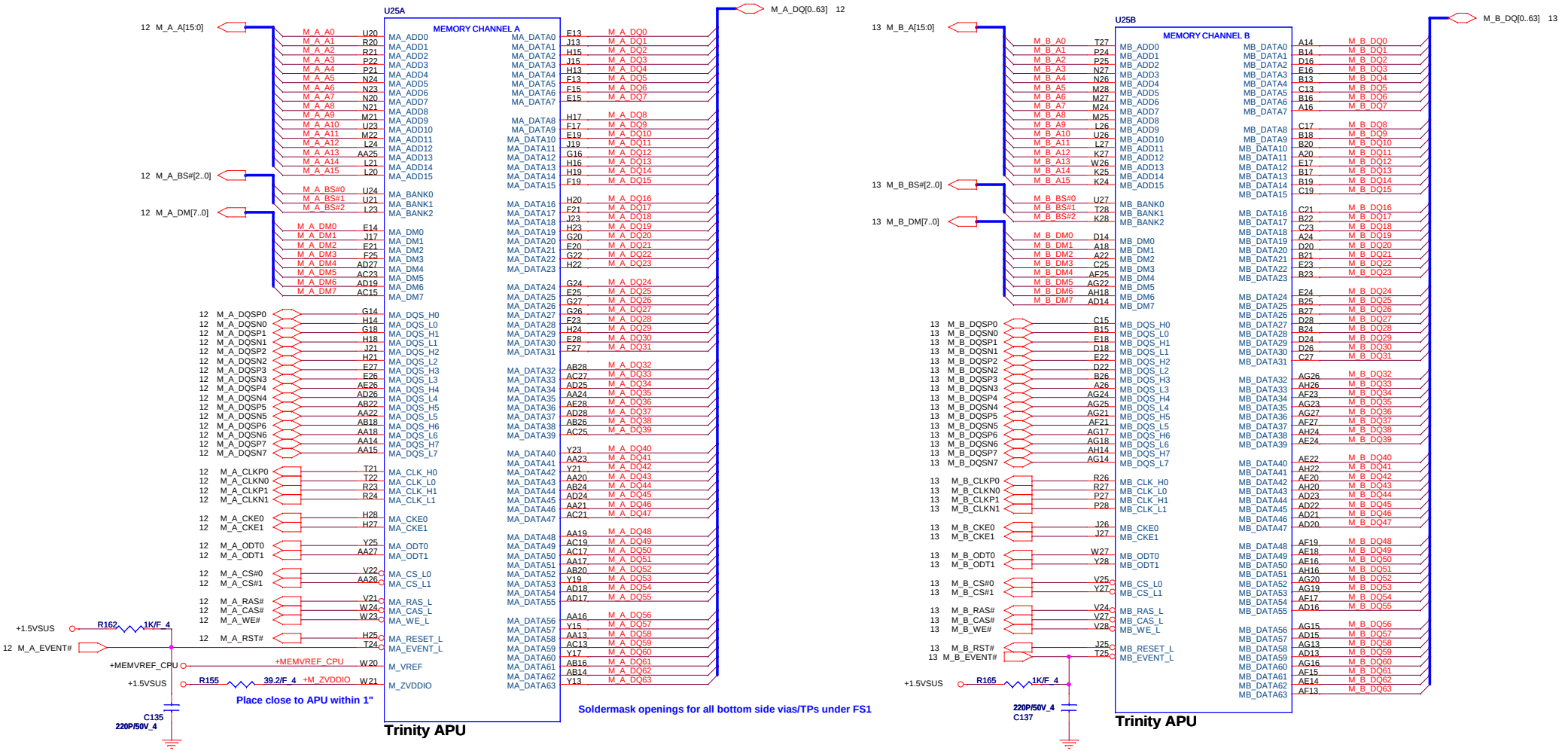
Note:
To override VID,Remove Rd, Re, Rf, install Rc
set VID via SVC & SVD option RES.

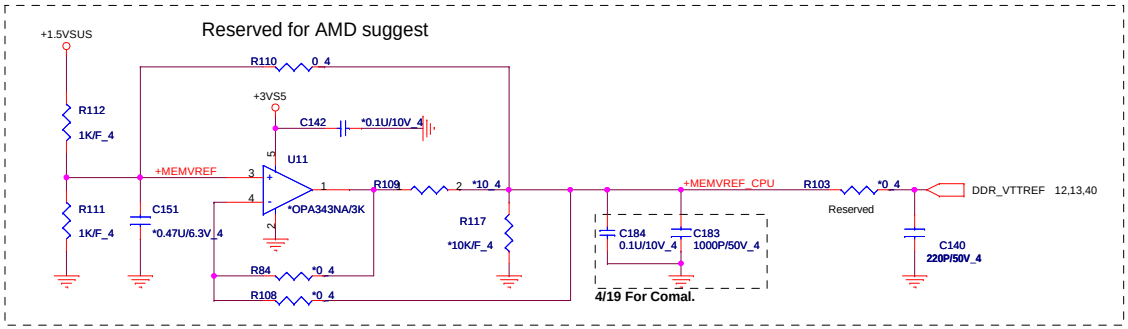


PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Llano PCIE/UMI/GPP	1A

Date: Monday, November 14, 2011 Sheet 2 of 44





PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Llano DDR3 MEM I/F	1A

Date: Monday, November 14, 2011 Sheet 3 of 44

Place caps with APU < 1 inch
route PCIE as 85ohm +/- 10%

DP0 output to
eDP to LVDS converter

Display port power 1.5V min 1.2v max : 1.65v

DP1 output to Hudson-M2
for VGA translator interface

4/19 HDMI change to DP2 for Comal.

DP2 output to
HDMI connector

note --HDMI P&N can not swap

Note: CLK_APU_HCLKP/N is 100MHZ SSC

Note: CLK_DP_NSSCP/N is 100MHZ non-SSC

4/19 For Comal.

4/19 For Comal.

4/19 For Comal.

4/19 For Comal,
close to APU.

Trinity APU

LVDS

VGA

HDMI

Display port power 1.5V min 1.2v max : 1.65v

SI,AMD no concern
so remove TP10,
TP17,TP18,TP16,TP23

To AMD HDT

M_TEST CONNECTION TBD

7/8 For Comal.

TEST35 PU FOR INTERNAL
TEST35 PD FOR CUSTOMER

DMAACTIVE_L controls
entry and exit from the
sleep and power states

AMD internal test only

FS1R1 signals is for detect CPU TYPE and protect it.
FS1R1 CPU this pin is N.C
FS1R2 CPU this pin is LOW
can remove it at MP

4/19 For Comal.

SI , PU SUS power
meet AMD design

Add R49 for verify this solution

reserve for leakage current verify

APU_PROCHOT# 可以當 input or output
當Low 時CPU 會降 P - STATE

to EC reserve only

Thermal

THERMTRIP# shutdown temperature 125度C

ADD VGA TEMP_ FAIL function is active Hi

over 120 degree C= Low

When 100K-NTC 100 C=6.164K
Thermal Trip = 120 C

PROJECT : R53
Quanta Computer Inc.
R23

Size	Document Number	Rev
	Llano Display/Misc	1A
Monday, November 14, 2011	Sheet	of

APU POWER TABLE

PIN NAME	NET NAME	VOLTAGE
VDD	+VCC_CORE	+1.1V
VDDNB	+VDDNB_CORE	??
VDDIO	+1.5VSUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V

SI , change to 22u for improve +VDDNB_CORE transient

4/19 For Comal.

C821 22U/6.3VS_8 C818 22U/6.3VS_8 C452 22U/6.3VS_8

C408 0.22U/10V_4 C465 0.22U/10V_4 C466 180P/50V_4 C468 180P/50V_4 C467 180P/50V_4

4/19 For Comal.

C346 22U/6.3VS_8 C380 22U/6.3VS_8 C397 180P/50V_4

SI , change to 22u for AMD ACE dynamic test,

36A

Maximum IDDspike 50A

C229 22U/6.3V_8 C271 22U/6.3V_8 C250 22U/6.3V_8 C669 22U/6.3V_8 C260 22U/6.3V_8

C286 22U/6.3V_8 C715 22U/6.3VS_8 C267 22U/6.3VS_8 C266 22U/6.3VS_8 C259 22U/6.3VS_8

4/19 For Comal.

C307 0.22U/10V_4 C306 0.22U/10V_4 C234 180P/50V_4 C239 180P/50V_4 C293 0.01U/25V_4 C304 0.01U/25V_4 C290 0.01U/25V_4

25A

Maximum IDDNBspike 33A

DECOUPLING between PROCESSOR and DIMMs Across VDDIO and VSS split

C207 0.22U/10V_4 C194 0.22U/10V_4 C195 180P/50V_4 C275 180P/50V_4

2.8A Up to DDR3-1333 @ 1.50V VDDIO

C242 0.22U/10V_4 C349 0.22U/10V_4 C255 0.22U/10V_4 C400 0.22U/10V_4 C285 0.22U/10V_4 C338 0.22U/10V_4

4/19 For Comal.

C190 180P/50V_4

4/19 For Comal.

C399 22U/6.3VS_8 C192 22U/6.3VS_8 C403 22U/6.3VS_8 C402 22U/6.3VS_8 C323 4.7U/6.3V_6 C310 4.7U/6.3V_6 C210 4.7U/6.3V_6 C398 4.7U/6.3V_6

If the VSS plane is cut to create a VDDIO plane, ceramic capacitors are connected across the VDDIO and VSS plane split as follows

VDDP = 5A

R334 *0_8/S

4/19 For Comal.

C707 22U/6.3VS_8 C674 10U/6.3V_8 C689 10U/6.3V_8 C679 10U/6.3V_8

C683 0.22U/6.3V_4 C684 0.22U/6.3V_4 C682 180P/50V_4 C685 180P/50V_4

VDDR = 3.3A (Up to DDR3-1333 @ 1.5V)

R333 *0_8/S

C673 10U/6.3V_8 C671 10U/6.3V_8 C676 10U/6.3V_8

C680 0.22U/6.3V_4 C203 0.22U/10V_4 C675 1000P/50V_4 C678 180P/50V_4 C681 180P/50V_4

VDDA= 0.75A

L17 PBY160808T-221Y-N(220,2A)

C204 4.7U/6.3V_6 C216 0.22U/10V_4 C226 3300P/50V_4

U25D

Trinity APU

U25E

Trinity APU

EMI suggestion

C96 470P/50V_4 C98 *470P/50V_4 C97 *470P/50V_4

PROJECT :	R53
Quanta Computer Inc.	
Size: Custom	Document Number: Llano POWER/GND
Rev: 1A	
Date: Friday, November 11, 2011	Sheet 5 of 44

NC,no install by default

R462 *2.2K_4 FCH_TEST0
R463 *2.2K_4 FCH_TEST1
R469 *2.2K_4 FCH_TEST2

+3V
R295 2.2K_4 CGCLK_SMB
R287 2.2K_4 CGDAT_SMB
to DDR3 SMBUS
SI2 , change power rail from +3V to +3VS5
+3VS5
R468 *1K_4
J6 1 2 SYS_RST#
*SOLDERJUMPER-2
SYS_RST# internal 10K pull up

GEVENT0# internal pull Hi 8.2K to +3V
GEVENT1# internal pull Hi 8.2K to +3V
GEVENT23# internal pull Hi 8.2K to +3V
GEVENT5# internal pull Hi 8.2K to +3VS5
PCIE_WAKE# no need to pull
Hi resistor from check list

CLK_REQ2# internal pull Hi 8.2K to +3V
CLK_REQ3# internal pull Hi 8.2K to +3V
CLK_REQ4# internal pull Hi 8.2K to +3V

+3VS5
R301 10K/F_4 SCL3
R298 10K/F_4 SDA3
R290 2.2K_4 SCL2
R296 2.2K_4 SDA2
R464 2.2K_4 SCL1
R465 2.2K_4 SDA1
R284 *4.7K_4 FCH_THERMTRIP#
C582 *0.01U/25V_4
R272 10K/F_4 DNBSWON#

SI2 , HP request Image sensor SMBUS reserve to FCH

This pin is used to power down VGA DAC regulators when CRT no connected

GEVENT16# internal pull Hi 8.2K to +3VS5
GEVENT15# internal pull Hi 8.2K to +3VS5

To Azalia

ACZ_SDOUT_R R454 33_4 ACZ_SDOUT_AUDIO 27
ACZ_SYNC_R R481 33_4 ACZ_SYNC_AUDIO 27
ACZ_BCLK_R R450 33_4 BIT_CLK_AUDIO 27
ACZ_RST#_R R479 33_4 ACZ_RST#_AUDIO 27
ACZ_SDIN0 ACZ_SDIN0 27

Pure UMA can remove
CLK_REQ# already internal pull up 8.2K
44 VGA_REQ 1 2 CLKREQ1#
D10 RB501V-40

remove PCIE_RST2# from AMD recommend

TP45 TP98 PCIE_RST2# RI#
33 SUSB# SUSC#
33 SUSC#
33 DNBSWON#
10 FCH_PWRGD
SUSB# SUSC# DNBSWON# FCH_PWRGD

4/19 For Comal.
TP51 FCH_TEST0 FCH_TEST1 FCH_TEST2
33 EC_A20GATE
33 EC_RCIN#
EC_A20GATE EC_RCIN#
TP50 FCH_PME#
33 SIO_EXT_SMI#
33 SIO_EXT_SCI#
R447 *0_4/S
SIO_EXT_SMI# GEVENT5# SYS_RST#
29,32 PCIE_WAKE#
C879 *100P/50V_4
PCIE_WAKE# FCH_THERMTRIP#
4 FCH_THERMTRIP#
+3V
R286 10K/F_4 WD_PWRGD
33 RSMRST#
RSMRST#
26 PCIE_CARD_CLKREQ#
29 PCIE_LAN_CLKREQ#
PCIE_CARD_CLKREQ# PCIE_LAN_CLKREQ#

27 ACZ_SPKR
12,13 CGCLK_SMB
12,13 CGDAT_SMB
30 SCL1
30 SDA1
32 PCIE_MINI_CLKREQ#
R505 *0_4/S
FCH_GPIO66 CGCLK_SMB CGDAT_SMB SCL1 SDA1 PCIE_MINI_CLKREQ# CLKREQ1#

LLB# Not Implemented ,left unconnected.
9 VGA_POWER_DOWN
R283 0_4
TP94 LLB#
TP64 SMARTVOLT2
VGA_PD
TP49 GBE_LED0
Remove Card EECS function form Vendor mail
SI
TP63

TP93 TP97 ODD_PLUGIN# ODD_DA#_FCH
31 ODD_PLUGIN#
31 ODD_DA#_FCH
4/19 For Comal.
TP48 TP99 TP95 TP46 FCH_JTAG_TCK FCH_JTAG_TDI FCH_JTAG_RST#
For Zero ODD

HD audio interface is +3V_S5 voltage
R484 *10K/F_4 ACZ_BCLK_R
R476 *10K/F_4 ACZ_SDOUT_R
R467 *10K/F_4 ACZ_SDIN0
R470 *10K/F_4 ACZ_SDIN1
R466 *10K/F_4 ACZ_SDIN2_R
ACZ_SDIN3_R
ACZ_SYNC_R
ACZ_RST#_R

TP60 TP59
32 BT_COMBO_OFF#
BT_COMBO_OFF#
14 VGA_RSTB
33 VGA_ON_SB
VGA_RSTB VGA_ON_SB

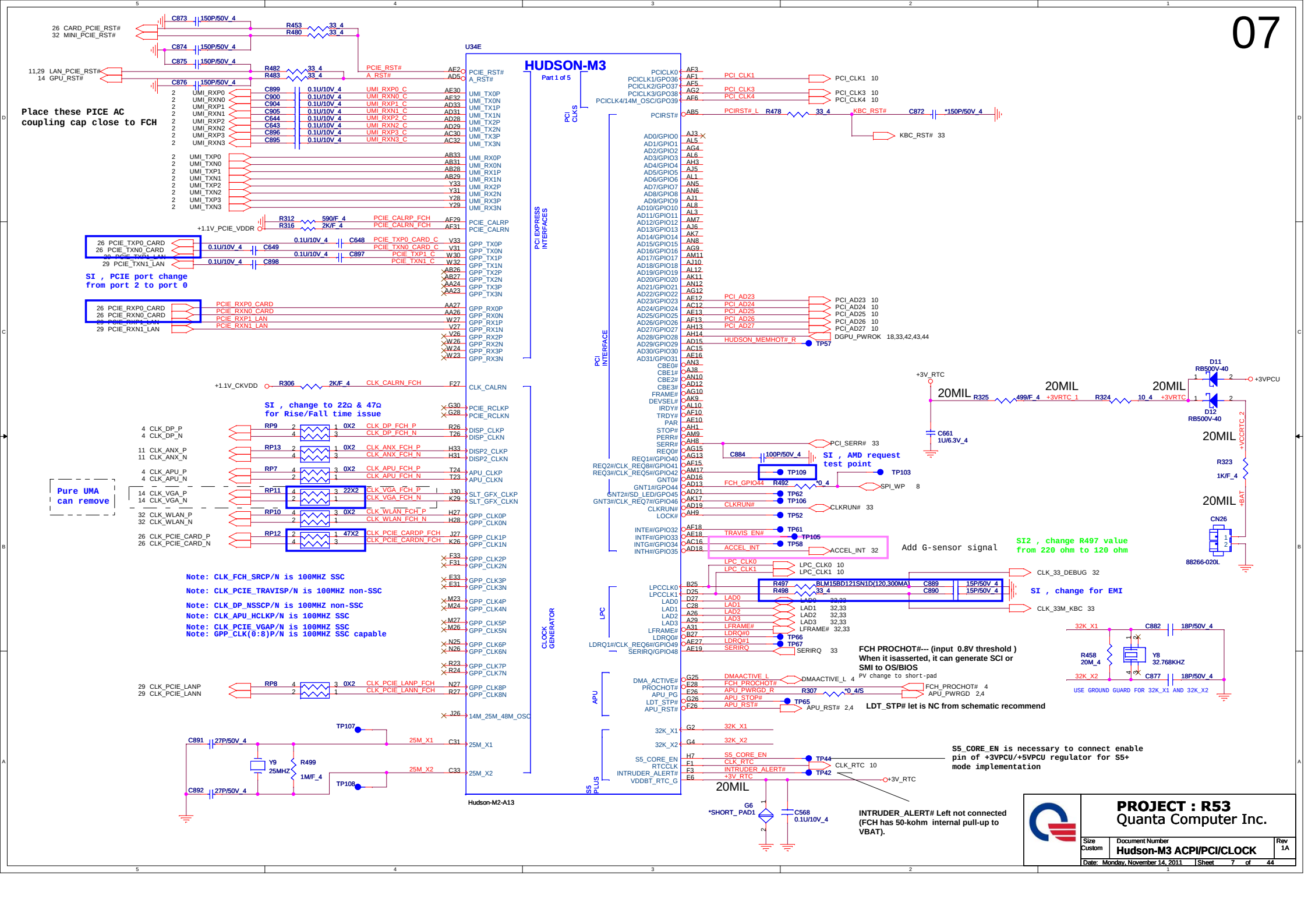
U34A
HUDSON-M3
Part 4 of 5

PCIE_RST2#/GEVENT4#
RI#/GEVENT22#
SPI_CS3#/GBE_STAT1/GEVENT21#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
TEST0
TEST1/TMS
TEST2
GA20IN/GEVENT0#
KBRST#/GEVENT1#
PME#/GEVENT3#
LPC_SMI#/GEVENT23#
LPC_PD#/GEVENT5#
SYS_RESET#/GEVENT19#
WAKE#/GEVENT8#
IR_RX1/GEVENT20#
THRMTRIP#/SMBALERT#/GEVENT2#
WD_PWRGD
RSMRST#
CLK_REQ4#/SATA_IS0#/GPIO64
CLK_REQ3#/SATA_IS1#/GPIO63
SMARTVOLT1/SATA_IS2#/GPIO50
CLK_REQ0#/SATA_IS3#/GPIO60
SATA_IS4#/FANOUT3/GPIO55
SATA_IS5#/FANIN3/GPIO59
SPKR/GPIO66
SCL0/GPIO43
SDA0/GPIO47
SCL1/GPIO227
SDA1/GPIO228
CLK_REQ2#/FANIN4/GPIO62
CLK_REQ1#/FANOUT4/GPIO61
IR_LED#/LLB#/GPIO184
SMARTVOLT2/SHUTDOWN#/GPIO51
DDR3_RST#/GEVENT7#/VGA_PD
GBE_LED0/GPIO183
SPI_HOLD#/GBE_LED1/GEVENT9#
GBE_LED2/GEVENT10#
GBE_STAT0/GEVENT11#
CLK_REQG#/GPIO65/OSCIN/IDLEEXIT#
BLINK/USB_OC7#/GEVENT18#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GEVENT17#
USB_OC4#/IR_RX0/GEVENT16#
USB_OC3#/AC_PRES/TDO/GEVENT15#
USB_OC2#/TCK/GEVENT14#
USB_OC1#/TDI/GEVENT13#
USB_OC0#/SPI_TPM_CS#/TRST#/GEVENT12#
AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO167
AZ_SDIN1/GPIO168
AZ_SDIN2/GPIO169
AZ_SDIN3/GPIO170
AZ_SYNC
AZ_RST#
PS2_DAT/SDA4/GPIO187
PS2_CLK/CEC/SCL4/GPIO188
SPI_CS2#/GBE_STAT2/GPIO166
PS2KB_DAT/GPIO189
PS2KB_CLK/GPIO190
PS2M_DAT/GPIO191
PS2M_CLK/GPIO192
KSO_0/GPIO209
KSO_1/GPIO210
KSO_2/GPIO211
KSO_3/GPIO212
KSO_4/GPIO213
KSO_5/GPIO214
KSO_6/GPIO215
KSO_7/GPIO216
KSO_8/GPIO217
KSO_9/GPIO218
KSO_10/GPIO219
KSO_11/GPIO220
KSO_12/GPIO221
KSO_13/GPIO222
KSO_14/XDB0/GPIO223
KSO_15/XDB1/GPIO224
KSO_16/XDB2/GPIO225
KSO_17/XDB3/GPIO226
USBCLK/14M_25M_48M_OSC
USB_RCOMP
USB_FSD1P/GPIO186
USB_FSD1N
USB_FSD0P/GPIO185
USB_FSD0N
USB_HSD13P
USB_HSD13N
USB_HSD12P
USB_HSD12N
USB_HSD11P
USB_HSD11N
USB_HSD10P
USB_HSD10N
USB_HSD9P
USB_HSD9N
USB_HSD8P
USB_HSD8N
USB_HSD7P
USB_HSD7N
USB_HSD6P
USB_HSD6N
USB_HSD5P
USB_HSD5N
USB_HSD4P
USB_HSD4N
USB_HSD3P
USB_HSD3N
USB_HSD2P
USB_HSD2N
USB_HSD1P
USB_HSD1N
USB_HSD0P
USB_HSD0N
USBSS_CALRP
USBSS_CALRN
USB_SS_TX3P
USB_SS_TX3N
USB_SS_RX3P
USB_SS_RX3N
USB_SS_TX2P
USB_SS_TX2N
USB_SS_RX2P
USB_SS_RX2N
USB_SS_TX1P
USB_SS_TX1N
USB_SS_RX1P
USB_SS_RX1N
USB_SS_TX0P
USB_SS_TX0N
USB_SS_RX0P
USB_SS_RX0N
SCL2/GPIO193
SDA2/GPIO194
SCL3_LV/GPIO195
SDA3_LV/GPIO196
EC_PWM0/EC_TIMER0/GPIO197
EC_PWM1/EC_TIMER1/GPIO198
EC_PWM2/EC_TIMER2/WOL_EN/GPIO199
EC_PWM3/EC_TIMER3/GPIO200
KSI_0/GPIO201
KSI_1/GPIO202
KSI_2/GPIO203
KSI_3/GPIO204
KSI_4/GPIO205
KSI_5/GPIO206
KSI_6/GPIO207
KSI_7/GPIO208
USB MISC
USB 1.1
ACPI / WAKE UP EVENTS
GPIO
USB 2.0
USB OC
USB 3.0
HD AUDIO
EMBEDDED CTRL

USB_RCOMP_SB R494 11.8K/F_6
USBP6+ USBP6- → USBP12+ 28 USBP12- 28 Left side USB Combo 3.0/2.0.
USBP5+ USBP5- → USBP11+ 28 USBP11- 28 Left side USB Combo 3.0/2.0.
USBP8+ 32 USBP8- 32 WLAN Min-Card
USBP7+ USBP7- → TP104 TP101
USBP2+ 23 USBP2- 23 Camera USB
USBP0+ 28 USBP0- 28 Right side USB 2.0 Connector
USBSS_CALRP R496 1K/F_4
USBSS_CALRN R495 1K/F_4
+FCH_VDD_11_SSUSB_S
USB 3.0 Not Implemented: left unconnected.
USBP30_TX2+ 28 USBP30_TX2- 28
USBP30_RX2+ 28 USBP30_RX2- 28
USBP30_TX1+ 28 USBP30_TX1- 28
USBP30_RX1+ 28 USBP30_RX1- 28
SCL2 SDA2 SCL3 SDA3
SCL3 of a TSI-capable APU's thermal bus,Pulled up to APU_VDDIO. Resistor value verified in the relevant APU design guide.
EC_PWM2 → EC_PWM2 10
No need for GPIO200

Hudson-M2-A13

PROJECT : R53
Quanta Computer Inc.
Size Custom | Document Number Hudson-M3 GPIO/USB/AZ/RGMII | Rev 1A
Date: Friday, November 11, 2011 | Sheet 6 of 44


HUDSON-M3
Part 1 of 5
U34E
Hudson-M2-A13
PCI EXPRESS INTERFACES
PCI INTERFACE
CLOCK GENERATOR
LPC
APU
S5 PLUS
PCI CLKS
Place these PICE AC coupling cap close to FCH
SI , PCIE port change from port 2 to port 0
SI , change to 22Ω & 47Ω for Rise/Fall time issue
Pure UMA can remove
SI , AMD request test point
Add G-sensor signal
SI2 , change R497 value from 220 ohm to 120 ohm
SI , change for EMI
Note: CLK_FCH_SRCP/N is 100MHZ SSC
Note: CLK_PCIE_TRAVISP/N is 100MHZ non-SSC
Note: CLK_DP_NSSCP/N is 100MHZ non-SSC
Note: CLK_APU_HCLKP/N is 100MHZ SSC
Note: CLK_PCIE_VGAP/N is 100MHZ SSC
Note: GPP_CLK(0:8)P/N is 100MHZ SSC capable
FCH PROCHOT#--- (input 0.8V threshold) When it isasserted, it can generate SCI or SMI to OS/BIOS
LDT_STP# let is NC from schematic recommend
S5_CORE_EN is necessary to connect enable pin of +3VPCU/+5VPCU regulator for S5+ mode implementation
INTRUDER_ALERT# Left not connected (FCH has 50-kohm internal pull-up to VBAT).
USE GROUND GUARD FOR 32K_X1 AND 32K_X2
PROJECT : R53
Quanta Computer Inc.
Hudson-M3 ACPI/PCI/CLOCK
Size Custom
Rev 1A
Date: Monday, November 14, 2011
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U34D

HUDSON-M3

Part 5 of 5

GROUND

Hudson-M2-A13

U34B

HUDSON-M3

Part 2 of 5

Hudson-M2-A13

PLACE SATA AC COUPLING CAPS CLOSE TO HUDSON-M2/M3

SATA HDD

SATA ODD

U23 *MC74VHC1G08DFT2G

C577 *0.1U/10V_4

SB_SATA_LED#

R288 0_4

PLACE SATA_CAL RES VERY CLOSE TO BALL OF HUDSON-M2/M3

R313 1K/F_4

R303 931/F_4

4/19 For Comal.

R294 *220/F_6 SB_SATA_LED#

Integrated Clock Mode: Leave unconnected.

Add GPIO for G-sensor LED control

GPIO52 internal pull Hi 8.2K to +3V
GPIO53 internal pull Hi 8.2K to +3V
GPIO54 internal pull Hi 8.2K to +3V
GPIO56 internal pull Hi 8.2K to +3V
GPIO57 internal pull Hi 8.2K to +3V
GPIO58 internal pull Hi 8.2K to +3V

TP102

R281 10K/F_4 R276 10K/F_4 R485 10K/F_4 R277 10K/F_4

TEMP(0 - 3)
Temp Monitor Not Implemented
10-KΩ 5% pull-up to +3VS5
or 10-KΩ 5% pull-down

6/7 for Comal.

ICT need TP2675 size test point

TP47 TP40 TP41 TP43 TP39

R455 10K/F_4

R456 *10K/F_4

R451 *10K/F_4

R452 *10K/F_4

R280 *10K/F_4

R503 *0_4/S

R510 *0_4/S

R509 *0_4/S

R314 715/F_4

R317 100/F_4

R311 *10K/F_4

VIN(0 - 7)
Voltage Monitor Not Implemented
10-KΩ 5% pull-up to +3VS5
or 10-KΩ 5% pull-down

SI , Q23,Q41 change to dual type MOS Q50

R444 10K/F_4 R445 *10K/F_4
R442 *10K/F_4 R443 10K/F_4
R449 *10K/F_4 R448 10K/F_4
R440 *10K/F_4 R460 10K/F_4
R438 *10K/F_4 R439 10K/F_4
R446 10K/F_4 R459 *10K/F_4
R441 10K/F_4 R461 *10K/F_4
R437 *10K/F_4 R457 10K/F_4

Vender	Size	P/N
AMIC	2M	AKE38ZN0801
WINBOND	2M	AKE38FP0N01
Socket		DFHS08FS023

FCH SPI ROM

SI , change power rail from +3V to +3VS5

C880 *22P/50V_4 EMI

C881 *0.1U/10V_4

R486 10K/F_4

R487 0_4 SPI_CS0#
R472 0_4 SPI_CLK
R471 0_4 SPI_SO
R489 0_4 SPI_SI
R493 *0_4

R473 *10K/F_4

R491 *10K/F_4

*MX25L1605DM2I-12G

R place close to PCH

FCH_CRT_R R502 150/F_4
FCH_CRT_G R501 150/F_4
FCH_CRT_B R504 150/F_4

Reserve for debug

VGA Hot-plug

R508 1K/F_4

R500 100K/F_4

Q50B 2N7002DW-7-F Dual

Q50A 2N7002DW-7-F Dual

R309 100K/F_4

ID4	ID3	ID2	ID1	ID0	CONFIG	31- Level BOM	Item
0	0	0	0	0	UMA		1
0	0	0	1	0			2
0	0	1	0	0			3
0	0	1	1	0			4
0	1	0	1	0			5
0	1	1	1	0			6
1	0	0	1	0			7
1	0	1	1	0			8
0	0	0	0	1	SG / Muxless		9
0	0	1	0	1			10
1	0	0	1	1			11
1	0	1	1	1			12

SIDE_PORT_ID2	SIDE_PORT_ID1	SIDE_PORT_ID0	
0	0	0	Samsung
0	0	1	Hynix
0	1	0	NC
0	1	1	no supprot side port

PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Hudson-M3 SATA/HWM/SPI	1A

Date: Friday, November 11, 2011 Sheet 8 of 44

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

SI, add for leakage issue

R539 0_8 Q46 *AO3416

+3V

33,34,36,40,41 MAINON

+3.3V_VDDIO

VDDQ--3.3V I/O power 102mA

C589 0.1U/10V_4 C570 22U/6.3V_8 C586 0.1U/10V_4 C581 0.1U/10V_4 C585 0.1U/10V_4

M2 chipset need to connect to GND
M3 remove

+FCH_VDDAN_33_DAC_R

+FCH_VDDPL_33_MLDAC

+VDDPL_3.3V

R291 *0_4

+FCH_VDDPL_33_SUSB_S

+FCH_VDDPL_33_SSUSB_S

+FCH_VDDPL_33_PCIE

+FCH_VDDPL_33_SATA

+3V L52 PBY160808T-221Y-N(220,2A) TRACE WIDTH >=15mil

C638 2.2U/6.3V_4 C639 *0.1U/10V_4

+3V L54 PBY160808T-221Y-N(220,2A) TRACE WIDTH >=15mil

C641 2.2U/6.3V_4 C632 *0.1U/10V_4

NOTE : LDO_CAP
A11 stepping : C will install 1nf cap
A12 stepping : C will let it to NC

C635 *1000P/50V_4 +LDO_CAP

+FCH_VDDAN_11_MLDAC

+FCH_VDDAN_11_DAC

VDDAN_11_ML -- UMI 1.1V analog power

+FCH_VDDAN_11_ML

C609 0.1U/10V_4 C617 1U/6.3V_4 C631 4.7U/6.3V_6 C613 0.1U/10_4

+3V +VDDPL_3.3V

L53 PBY160808T-221Y-N(220,2A)

C640 2.2U/6.3V_4 C615 0.1U/10V_4

VDDPL_33_USB_S : USB PHY PLL analog power

+3V_AVDD_USB +FCH_VDDPL_33_SUSB_S

L67 PBY160808T-221Y-N(220,2A)

C885 2.2U/6.3V_4 C886 1U/6.3V_4

VDDAN_33_USB_S : USB PHY I/O analog power

+3V_AVDD_USB

+3VS5 L68 PBY160808T-221Y-N(220,2A) TRACE WIDTH >=50mil

C574 0.1U/10V_4 C583 10U/6.3V_8 C887 10U/6.3V_8 C567 1U/6.3V_4 C575 1U/6.3V_4

VDDAN_11_USB_S : USB PHY PLL analog power

+1.1VS5 L70 PBY160808T-221Y-N(220,2A) +FCH_VDDAN_11_USB_S

C979 0.1U/10V_4 C572 2.2U/6.3V_4 C587 0.1U/10V_4

SI , AMD SR tool review need one more 0.1u

VDDCR_11_USB_S : USB PHY core power

+1.1VS5 L69 PBY160808T-221Y-N(220,2A) +FCH_VDDCR_11_USB_S TRACE WIDTH >=15mil

C573 0.1U/10V_4 C579 0.1U/10V_4 C888 10U/6.3V_8

SI , AMD SR tool review

M3 chipset need to stuff for support USB3.0

+FCH_VDD_11_SSUSB_S

+1.1VS5 L48 PBY160808T-221Y-N(220,2A) R293 *0_8/S +FCH_VDDAN_11_SSUSB_S_R

VDDAN_11_SSUSB_S : USB3.0 PHY PLL analog power

R289 *0_4 R300 *0_8/S +FCH_VDDCR_11_SSUSB_S

M2 chipset need to connect to GND M3 remove

C605 1U/6.3V_4 C607 0.1U/10V_4 C606 0.1U/10V_4 C604 1U/6.3V_4 C627 10U/6.3V_8 C630 1U/6.3V_4 C629 0.1U/10V_4 C628 0.1U/10V_4

VDDCR_11_SSUSB_S : USB3.0 PHY core power

M3 chipset need to stuff for support USB3.0

if support Modem wake up should be change pull hi to S5 power

+3VS5 +FCH_VDDPL_33_SSUSB_S

L50 PBY160808T-221Y-N(220,2A)

C633 2.2U/6.3V_6 C634 0.1U/10V_4

M3 chipset need to stuff for support USB3.0

+3V +VDDIO_AZ

R477 *0_4/S

VDDIO_AZ_S -- HD Audio Interface I/O power

C563 2.2U/6.3V_4

U34C

HUDSON-M3 Part 3 of 5

Hudson-M2-A13

AB17	VDDIO_33_PCIGP_1	PCI/GPIO I/O	
AB18	VDDIO_33_PCIGP_2		
AE9	VDDIO_33_PCIGP_3		
AD10	VDDIO_33_PCIGP_4		
AG7	VDDIO_33_PCIGP_5		
AC13	VDDIO_33_PCIGP_6		
AB12	VDDIO_33_PCIGP_7		
AB13	VDDIO_33_PCIGP_8		
AB14	VDDIO_33_PCIGP_9		
AB16	VDDIO_33_PCIGP_10		
T14	VDDCR_11_1	CORE S0	
T17	VDDCR_11_2		
T20	VDDCR_11_3		
U16	VDDCR_11_4		
U18	VDDCR_11_5		
V14	VDDCR_11_6		
V17	VDDCR_11_7		
V20	VDDCR_11_8		
Y17	VDDCR_11_9		
H24	VDDPL_33_SYS		47mA
V22	VDDPL_33_DAC		20mA
U22	VDDAN_33_DAC		20mA
T22	VDDPL_33_ML		30mA
L18	VDDPL_33_SSUSB_S		11mA
D7	VDDPL_33_USB_S		14mA
AH29	VDDPL_33_PCIE		11mA
AG28	VDDPL_33_SATA		12mA
H26	VDDAN_11_CLK_1	CLKGEN I/O	
J25	VDDAN_11_CLK_2		
K24	VDDAN_11_CLK_3		
L22	VDDAN_11_CLK_4		
M22	VDDAN_11_CLK_5		
N21	VDDAN_11_CLK_6		
N22	VDDAN_11_CLK_7		
P22	VDDAN_11_CLK_8		
M31	LDO_CAP		
V21	VDDPL_11_DAC		7mA
Y22	VDDAN_11_ML_1	MAIN LINKS EXPRESS	226mA
V23	VDDAN_11_ML_2		
V24	VDDAN_11_ML_3		
V25	VDDAN_11_ML_4		
AB24	VDDAN_11_PCIE_1		
Y21	VDDAN_11_PCIE_2		
AE25	VDDAN_11_PCIE_3		
AD24	VDDAN_11_PCIE_4		
AB23	VDDAN_11_PCIE_5		
AA22	VDDAN_11_PCIE_6		
AE26	VDDAN_11_PCIE_7		
AG27	VDDAN_11_PCIE_8		
AB10	VDDIO_33_GBE_S	GBE LAN SERIAL ATA	
AB11	VDDCR_11_GBE_S_1		
AA11	VDDCR_11_GBE_S_2		
AA9	VDDIO_GBE_S_1		
AA10	VDDIO_GBE_S_2		
AA21	VDDAN_11_SATA_1		
Y20	VDDAN_11_SATA_4		
AB21	VDDAN_11_SATA_2		
AB22	VDDAN_11_SATA_3		
AC22	VDDAN_11_SATA_5		
AC21	VDDAN_11_SATA_6		
AA20	VDDAN_11_SATA_7		
AA18	VDDAN_11_SATA_8		
AB20	VDDAN_11_SATA_9		
AC19	VDDAN_11_SATA_10		
G7	VDDAN_33_USB_S_1	3.3V_S5 I/O USB	470mA
H8	VDDAN_33_USB_S_2		
J8	VDDAN_33_USB_S_3		
K8	VDDAN_33_USB_S_4		
K9	VDDAN_33_USB_S_5		
M9	VDDAN_33_USB_S_6		
M10	VDDAN_33_USB_S_7		
N9	VDDAN_33_USB_S_8		
N10	VDDAN_33_USB_S_9		
M12	VDDAN_33_USB_S_10		
N12	VDDAN_33_USB_S_11		
M11	VDDAN_33_USB_S_12		
U12	VDDAN_11_USB_S_1		140mA
U13	VDDAN_11_USB_S_2		
T12	VDDCR_11_USB_S_1		42mA
T13	VDDCR_11_USB_S_2		
P16	VDDAN_11_SSUSB_S_1	USB SS	282mA
M14	VDDAN_11_SSUSB_S_2		
N14	VDDAN_11_SSUSB_S_3		
P13	VDDAN_11_SSUSB_S_4		
P14	VDDAN_11_SSUSB_S_5		
N16	VDDCR_11_SSUSB_S_1		424mA
N17	VDDCR_11_SSUSB_S_2		
P17	VDDCR_11_SSUSB_S_3		
M17	VDDCR_11_SSUSB_S_4		
N18	VDDIO_33_S_1		59mA
L19	VDDIO_33_S_2		
M18	VDDIO_33_S_3		
V12	VDDIO_33_S_4		
V13	VDDIO_33_S_5		
Y12	VDDIO_33_S_6		
Y13	VDDIO_33_S_7		
W11	VDDIO_33_S_8		
G24	VDDXL_33_S		5mA
N20	VDDCR_11_S_1		187mA
M20	VDDCR_11_S_2		
J24	VDDPL_11_SYS_S		70mA
M8	VDDAN_33_HWM_S		12mA
AA4	VDDIO_AZ_S		26mA

1007mA for M3
902mA for M2

+1.1V_VDDCR

VDDCR-- S/B CORE power

TRACE WIDTH >=100mil

C588 0.1U/10V_4 C597 0.1U/10V_4 C598 1U/6.3V_4 C590 1U/6.3V_4 C591 10U/6.3V_8

+1.1V_CKVDD

VDDAN_11_CLK-- Internal clock Generator I/O power 340mA

TRACE WIDTH >=30mil

C626 1U/6.3V_4 C618 1U/6.3V_4 C622 0.1U/10V_4 C624 0.1U/10V_4 C916 22U/6.3VS_8

Reserve for VDDAN_11_CL leakage current issue

R514 0_8 Q42 *AO3416 L72 BLM18PG181SN1D(180,1.5A)_6 +1.1V

MAINON 33,34,36,40,41

+1.1V_PCIE_VDDR

VDDAN_11_PCIE --PCIE/UMI analog power 1088mA

TRACE WIDTH >=100mil

L56 BLM18PG181SN1D(180,1.5A)_6 +1.1V

C610 0.1U/10V_4 C620 0.1U/10V_4 C621 1U/6.3V_4 C623 1U/6.3V_4 C642 22U/6.3VS_8

+1.1VS5

VDDPL_11_SYS_S : System Clock Gen PLLs analog power

+VDDPL_1.1V L47 PBY160808T-221Y-N(220,2A)

C608 2.2U/6.3V_4 C614 0.1U/10V_4

+1.1V_AVDD_SATA

VDDAN_11_SATA--SATA PHY analog/IO power 1337mA

TRACE WIDTH >=50mil

L45 BLM18PG181SN1D(180,1.5A)_6 +1.1V

C596 1U/6.3V_4 C611 1U/6.3V_4 C599 0.1U/10V_4 C595 0.1U/10V_4 C600 22U/6.3VS_8

if support USB 3.0 wake up should be change pull hi to S5 power

VDDAN_33_HWM_S -- Hardware monitor interface I/O power

+VDDAN_3.3V_HWM

+3VS5 L66 PBY160808T-221Y-N(220,2A)

C878 2.2U/6.3V_4 C566 0.1U/10V_4

+VDDIO_3.3V

VDDIO_33_S-- 3.3v S5 I/O power 59mA

TRACE WIDTH >=20mil

C593 *0.1U/10V_4 C576 2.2U/6.3V_4 C594 1U/6.3V_4 C584 1U/6.3V_4 C603 1U/6.3V_4 C580 1U/6.3V_4

+3VS5

if support USB 3.0 wake up should be change pull hi to S5 power

VDDXL_33_S-- 25MHZ XTAL IO power 5mA

+VDDXL_3.3V

VDDCR_1.1_S-- 1.1V S5 Core power 187mA

+VDDCR_1.1V

TRACE WIDTH >=15mil

+1.1VS5

C625 *0.1U/10V_4 C612 2.2U/6.3V_4

L49 PBY160808T-221Y-N(220,2A) +3VS5

C601 1U/6.3V_4 C616 2.2U/6.3V_4

+VDDPL_1.1V 70mA

+VDDAN_3.3V_HWM 12mA

+VDDIO_AZ 26mA

Trace width >=20 mil

This circuit is for switch DAC and UMI analog power

32 mA Max

+3V Q25 AO3404

+FCH_VDDAN_33_DAC_R

+FCH_VDDAN_33_DAC L71 PBY160808T-221Y-N(220,2A)

C915 2.2U/6.3V_4 C914 0.1U/10V_4

+12VALW R315 330K_6

+FCH_VGA_PWR_EN

Q24 ME2N7002E

VGA will power down when CRT no insert

6 VGA_POWER_DOWN VGA_POWER_DOWN

VGA_PD is generated from FCH

R282 2.2K_4 C569 1U/6.3V_4 C637 0.022U/25V_4

+1.1V Q26 AO3404

+FCH_VDDAN_33_DAC_R +FCH_VDDPL_33_MLDAC

R511 *0_8/S

C901 2.2U/6.3V_4 C893 0.1U/10V_4

233 mA Max

+VDDAN_11_MLDAC L55 PBY160808T-221Y-N(220,2A) +FCH_VDDAN_11_MLDAC

SI2 , remove discharge circuit

SI , reserve for leakage issue

PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Hudson-M3 POWER/GND	1A
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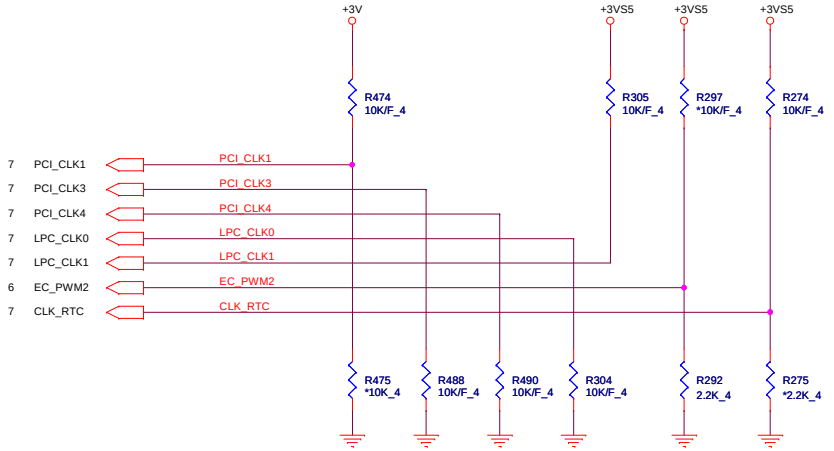
STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



REQUIRED STRAPS

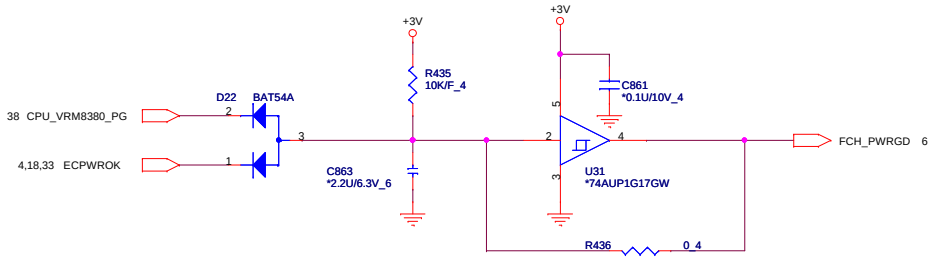
	--------	PCI_CLK1	--------	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	CLK_RTC
PULL HIGH	--------	ALLOW PCIE Gen2 DEFAULT	--------	USE DEBUG STRAP	non_Fusion CLOCK MODE	AMD internal EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM DEFAULT	S5 PLUS MODE ENABLED
PULL LOW	--------	FORCE PCIE Gen1	--------	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM	S5 PLUS MODE DISABLED DEFAULT

DEBUG STRAPS

FCH has 15K Internal Pull Up for PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

FCH PWRGD



PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Hudson-M3 STRAP/PWRGD	1A

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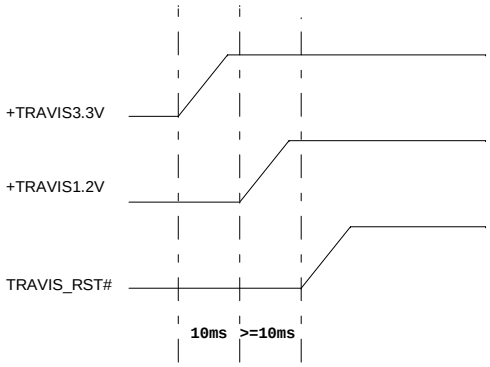
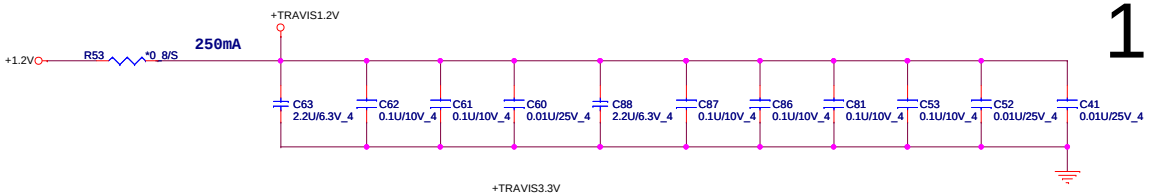
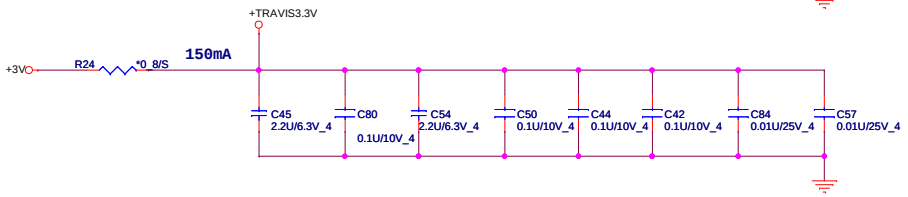
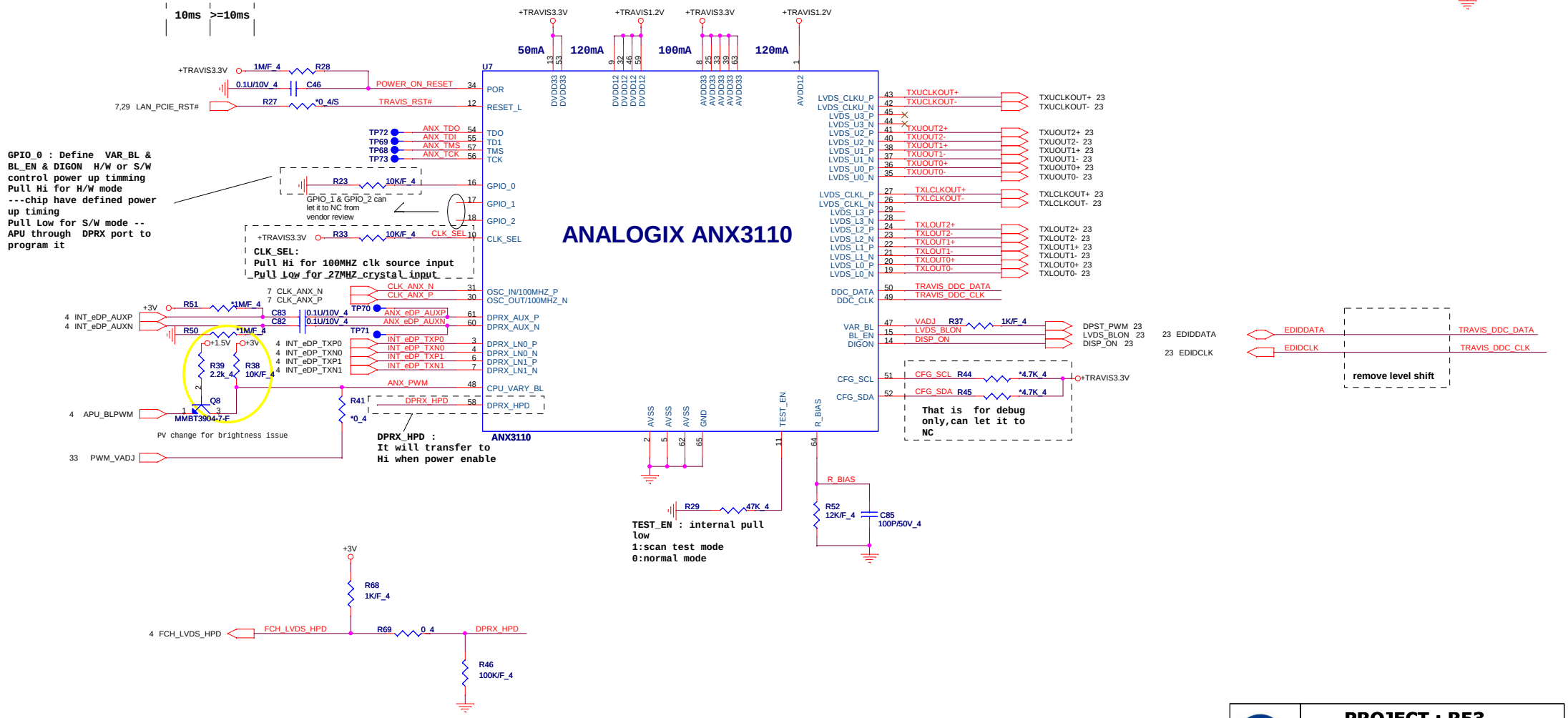
ANX3110 Power Up Sequence









PROJECT : R53 Quanta Computer Inc.		
Size: Custom	Document Number: ANX3110	Rev: 1A
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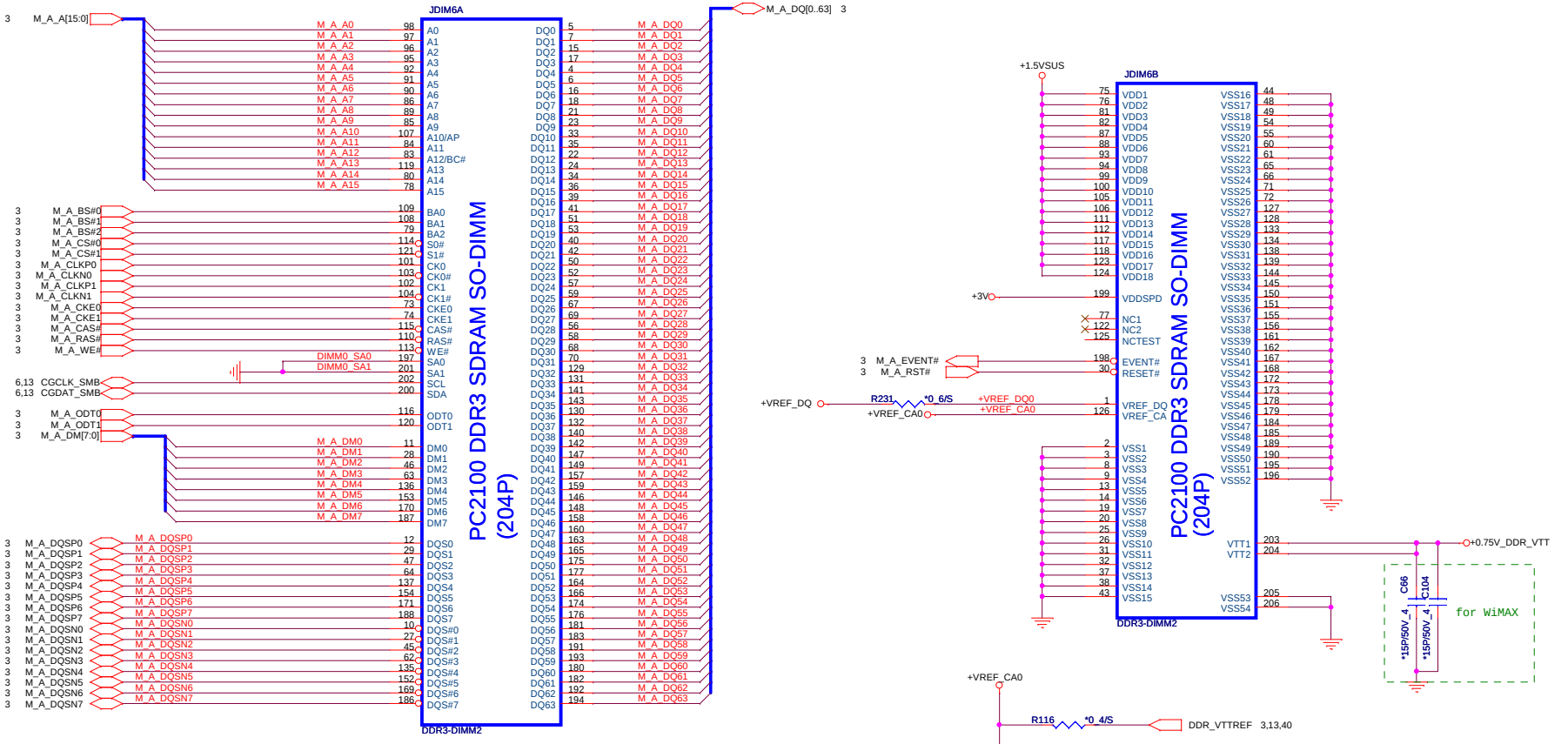
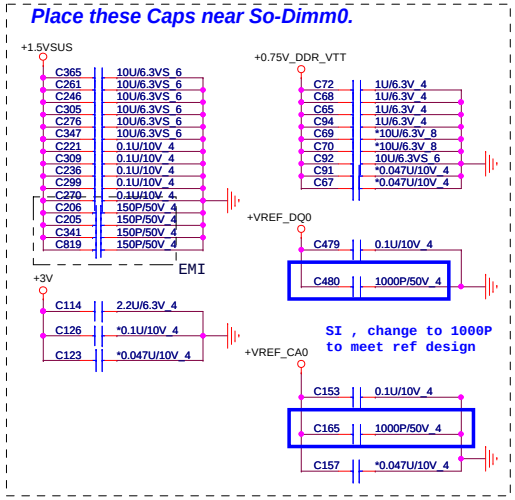
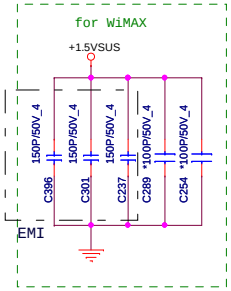
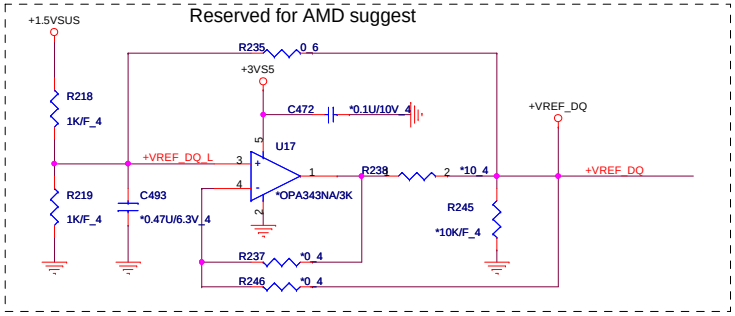


H9．2mm







13,40 +0.75V_DDR_VTT
2,3,4,5,13,40,41,44 +1.5VSUS
2,4,6,8,9,10,11,13,14,18,23,24,25,26,27,28,29,30,31,32,33,41,42,44 +3V

PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM-0	1A

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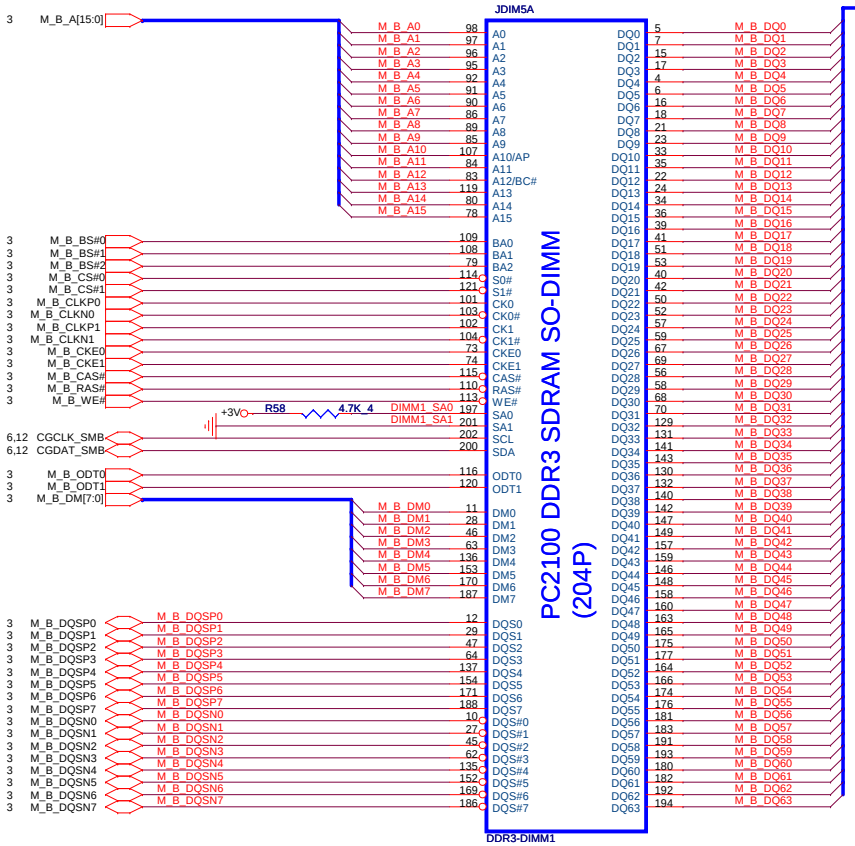
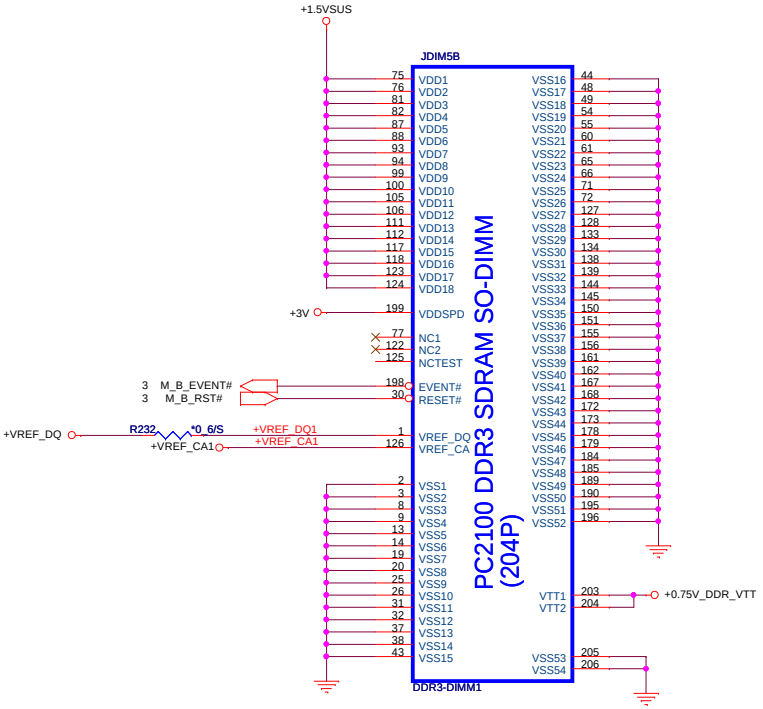
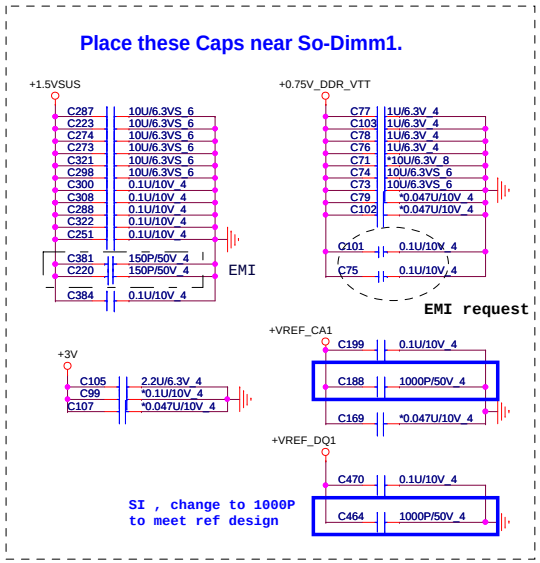




H5.2mm



12,40 +0.75V_DDR_VTT
2,3,4,5,12,40,41,44 +1.5VSUS
2,4,6,8,9,10,11,12,14,18,23,24,25,26,27,28,29,30,31,32,33,41,42,44 +3V

PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM-1	1A

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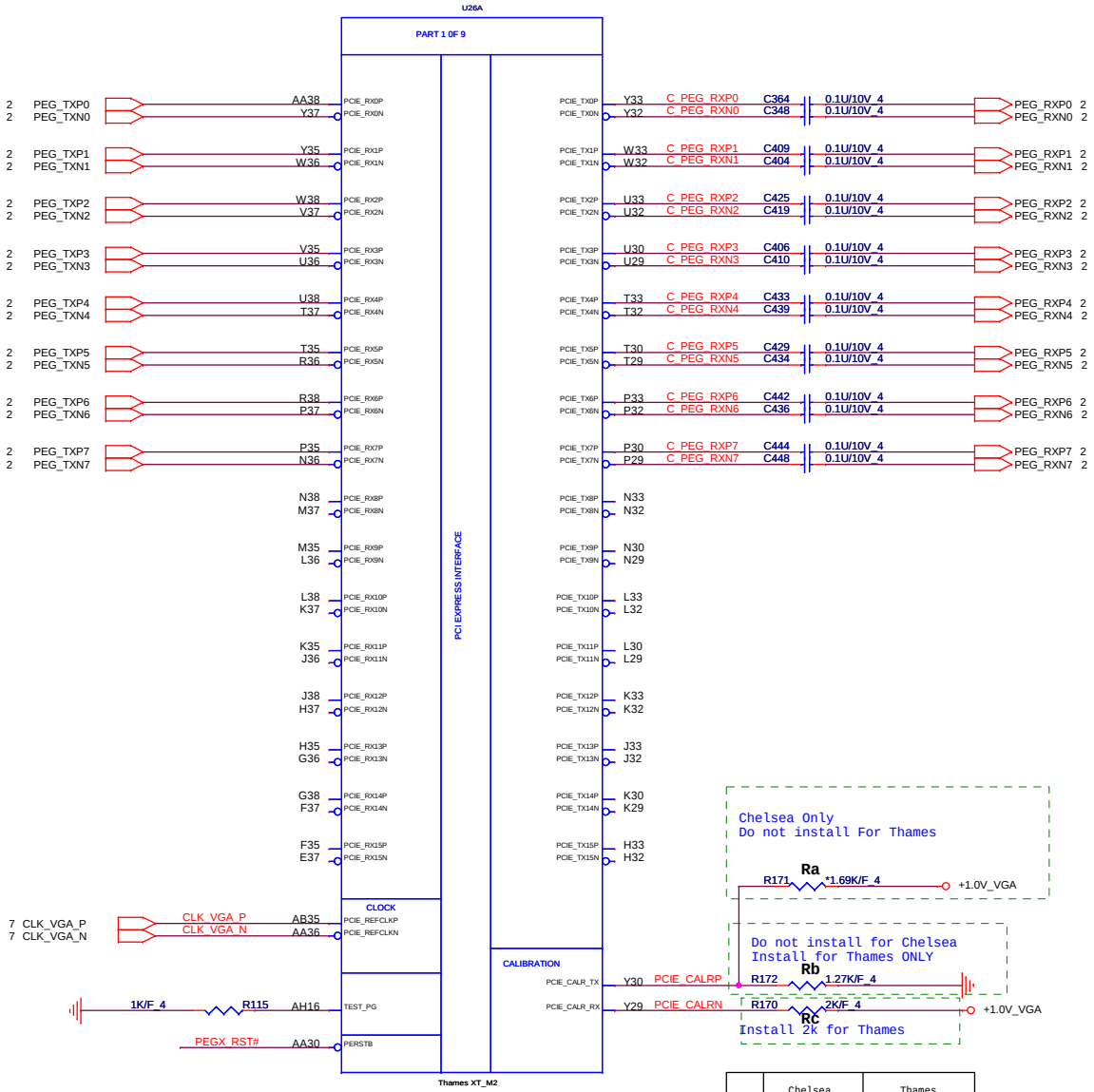

	Chelsea	Thames
Ra	1.69K	n/a
Rb	n/a	1.27K
Rc	1K	2K

16,18,19,44 +1.0V_VGA → +1.0V_VGA
15,16,18,19,43 +1.8V_VGA → +1.8V_VGA

PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Chelsea_PCIE_Interface	1A

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MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Hynix- D die	64Mx16 *8, 900Mhz	H5TQ1G63DFR-11C
0001	Micron- G die	64Mx16 *8, 900Mhz	MT41J64M16JT-107G:G
0010	Samsung- G die	64Mx16 *8, 900Mhz	K4W1G1646G-BC11
0011	Hynix- D die	128Mx16 *8, 900Mhz	H5TQ2G63DFR-11C
0100	Micron- D die	128Mx16 *8, 900Mhz	MT41J128M16HA-107G:D
0101	Samsung- C die	128Mx16 *8, 900Mhz	K4W2G1646C-HC11
0110			
0111			
1000			
1001			
1010			
1011			
1100			
1101			
1110			
1111			

GPIO16 GPIO20 GPIO15

Thames-XT	PWRCNTL 2	PWRCNTL 1	PWRCNTL 0	VGA CORE
L	0	0	0	1.0V
M	0	0	1	0.9V
H	0	1	0	0.875V
	0	1	1	0.85V
	1	0	0	0.8V
	1	0	1	0.75V

Memory ID

Access to SMBBus ans SDA/SCL is mandatory on all designs
Add test points on SMBBus and SDA/SCL for debug

Reserve for AMD debug only

GPIO22(ROMCS#)
3-k external pull up is required
if an external BIOS ROM chip is used.
Must be unconnected if no external
BIOS ROM chip is used

GPIO29, GPIO30 are NC on Thames

Thames INSTALL, do not install for Chelsea
PS_0 should be tied to GND on Thames

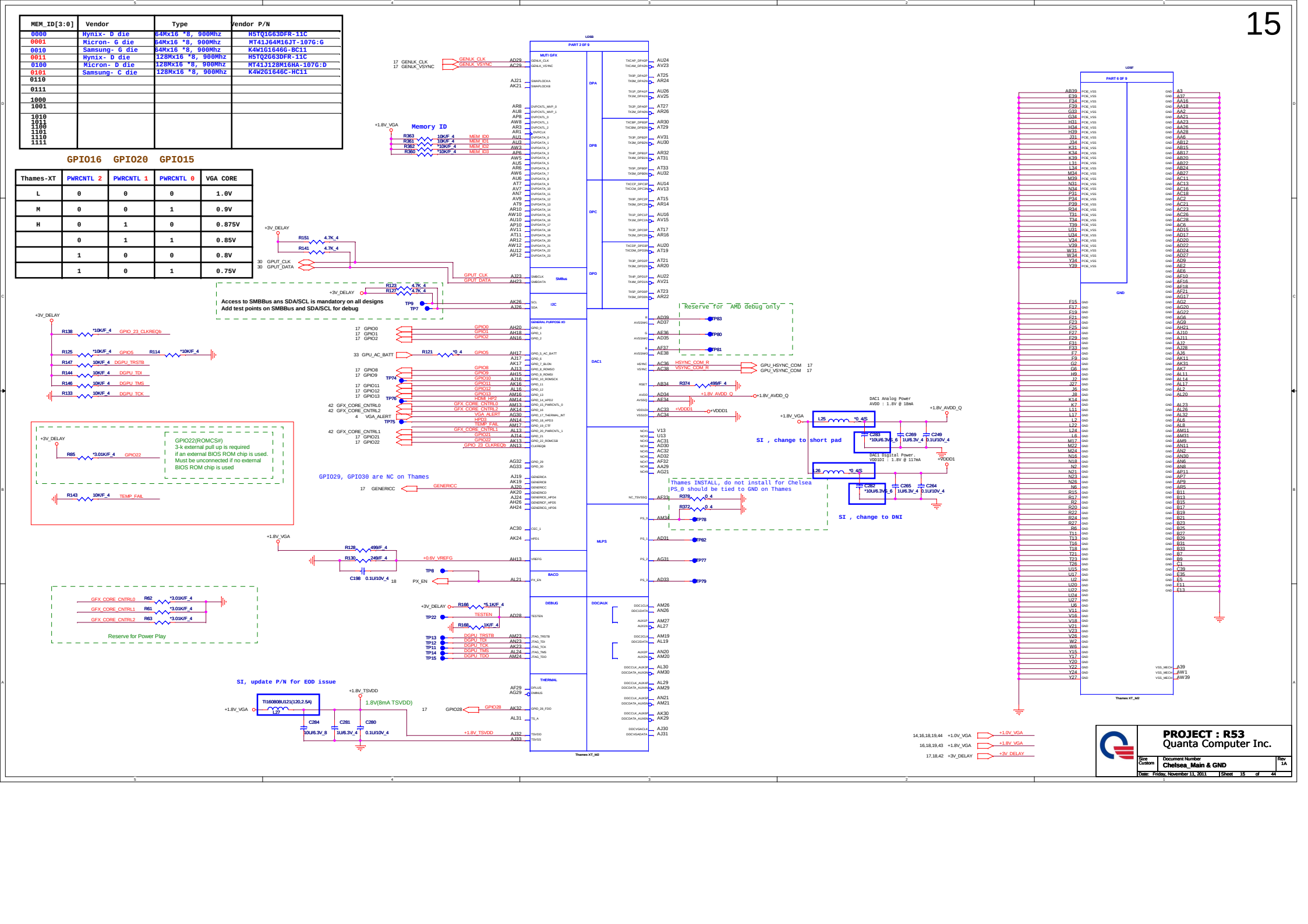
SI , change to short pad

SI , change to DNI

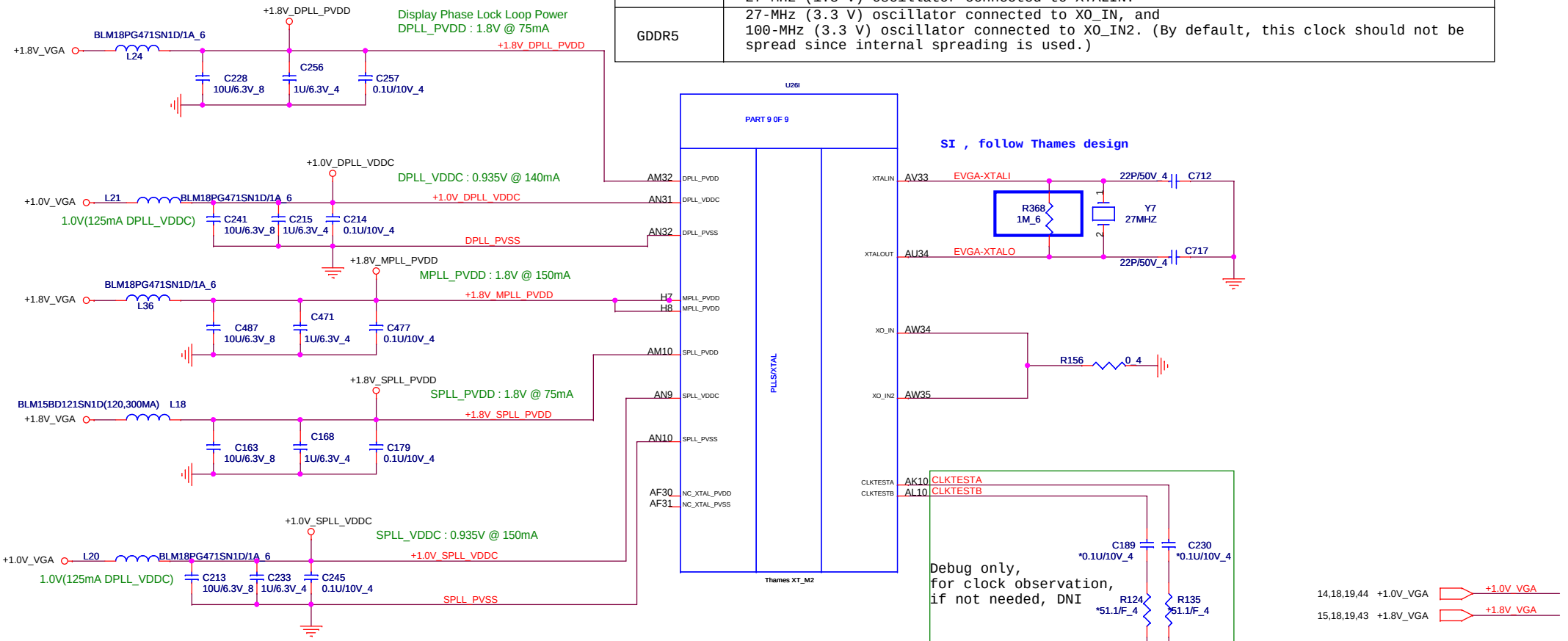
Reserve for Power Play

SI, update P/N for EOD issue

1.8V(8mA TSVDD)



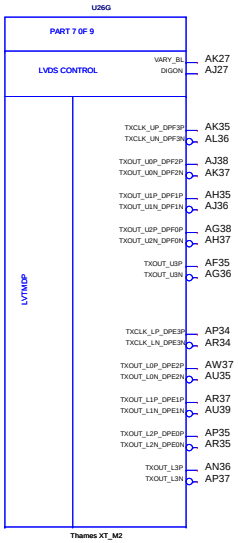
Memory Type	
DDR3	27-MHz (± 30 ppm) crystal connected to XTALIN/XTALOUT, or 27-MHz (1.8 V) oscillator connected to XTALIN.
GDDR5	27-MHz (3.3 V) oscillator connected to XO_IN, and 100-MHz (3.3 V) oscillator connected to XO_IN2. (By default, this clock should not be spread since internal spreading is used.)



PROJECT : R53
Quanta Computer Inc.

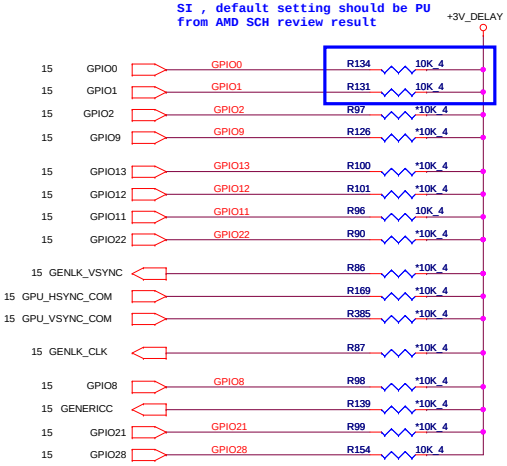
Size	Document Number	Rev
Custom	Chelsea_XTAL	1A

Date: Monday, November 14, 2011 Sheet 16 of 44



CONFIGURATION STRAPS -- SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET				
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	X
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIE Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIE Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1
BIF_VGA DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	XXX
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	X
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled	X
			NOTE: ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOS ARE USEED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET	
RESERVED RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA NA	GENLK_CLK GPIO8 GPIO21 GENERICC	Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only)	0 0 0 0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

SI , default setting should be PU from AMD SCH review result

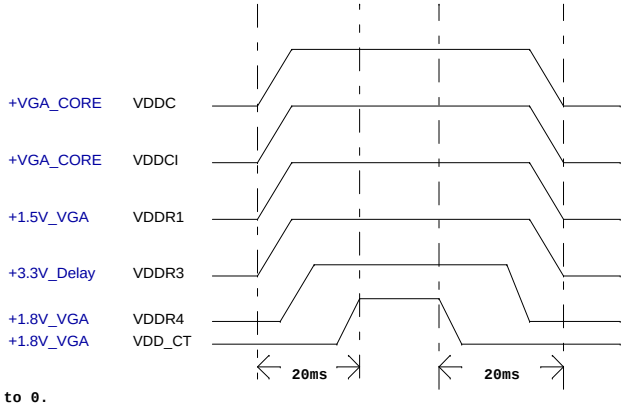


Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

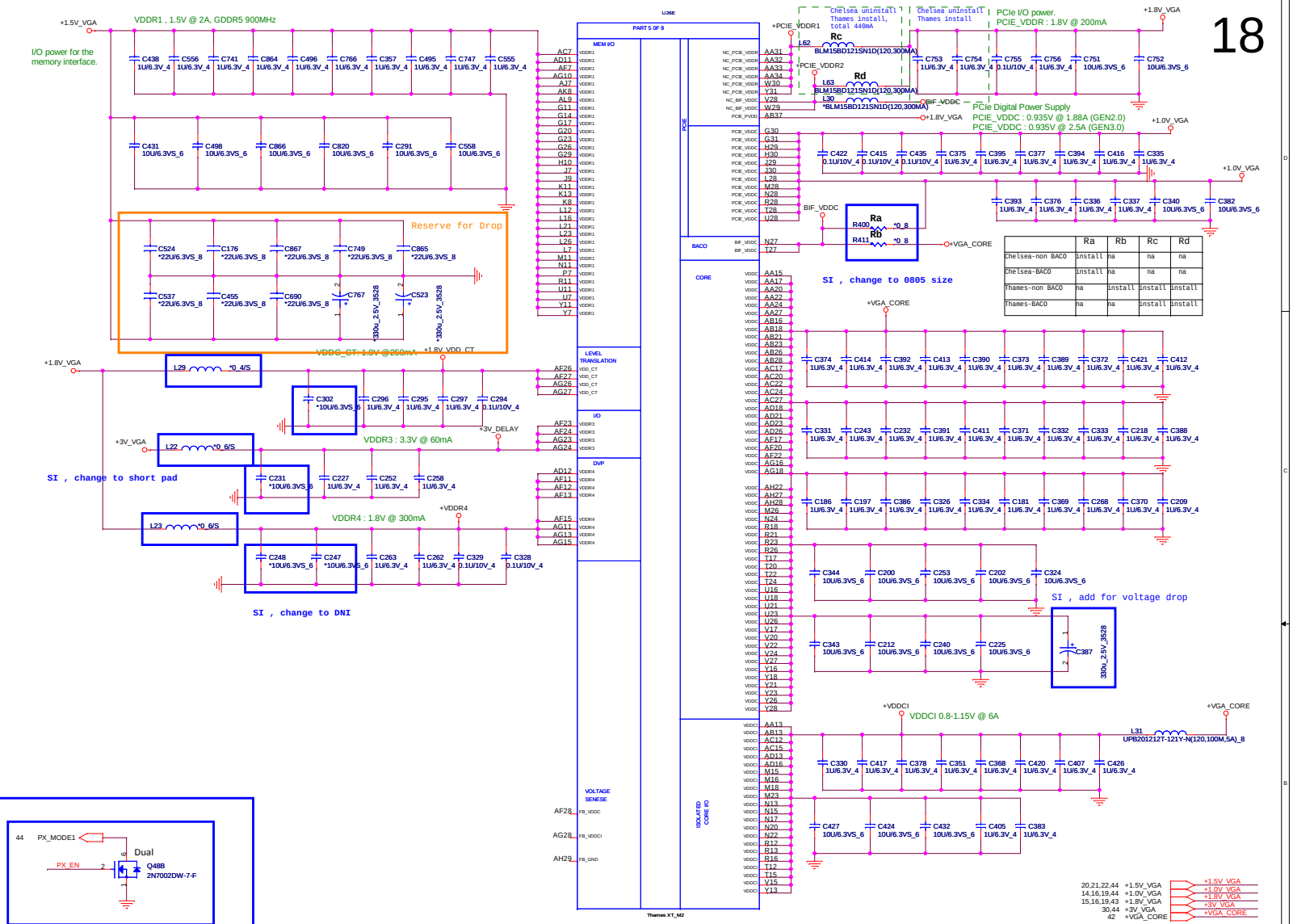
Power Up/Down Sequence



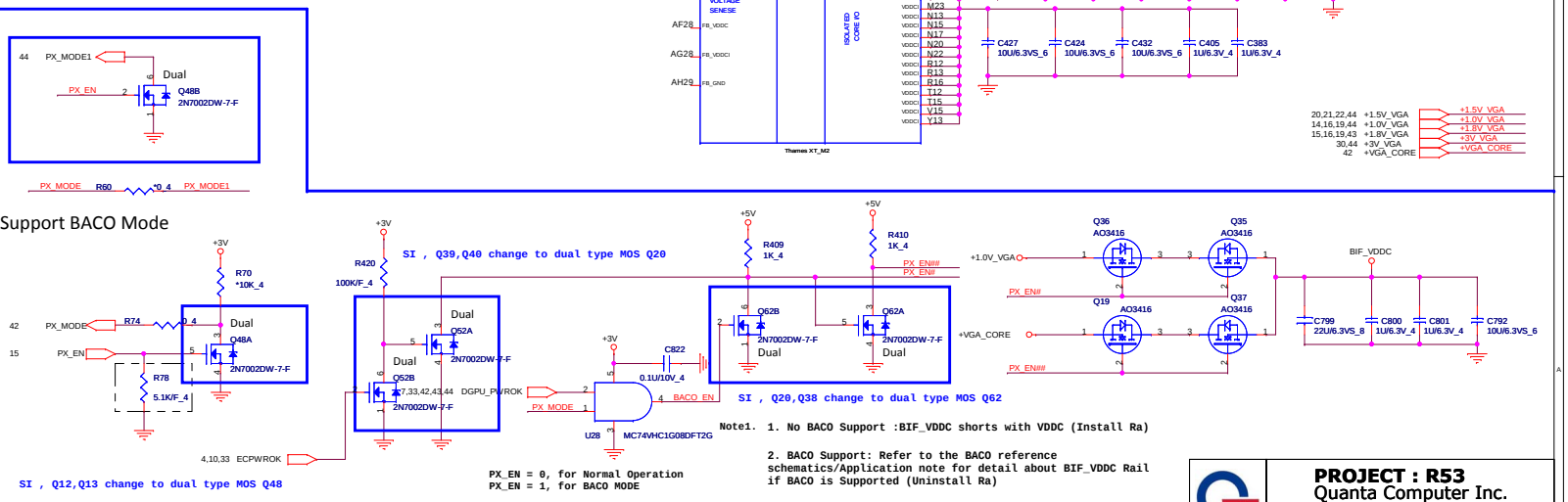
PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Chelsea_LVDS / STRAP	1A

Date: Friday, November 11, 2011 Sheet 17 of 44



	Ra	Rb	Rc	Rd
Chelsea-non BACO	install	na	na	na
Chelsea-BACO	install	na	na	na
Thames-non BACO	na	install	install	install
Thames-BACO	na	na	install	install



Note1. 1. No BACO Support :BIF_VDDC shorts with VDDC (Install Ra)

2. BACO Support: Refer to the BACO reference schematics/Application note for detail about BIF_VDDC Rail if BACO is Supported (Uninstall Ra)

PX_EN = 0, for Normal Operation
PX_EN = 1, for BACO MODE

PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Chelsea_Power & BACO	1A
Date: Monday, November 14, 2011	Sheet 18 of 44	

For Thames a dedicated BEAD is required
for each DPAB_VDD18, DPCD_VDD18, DPEF_VDD18

For Thames a dedicated BEAD is required
for each DPAB_VDD10, DPCD_VDD10, DPEF_VDD10

U26H

PART 8 0F 9

DP_VDDR

DP_VDDC

DP GND

CALIBRATION

Thames XT_M2

DP/TMDS/LVDS Transmitter Power
HDMI mode: 1.8V@237mA per port
DP mode: 1.8V@188mA per port

+1.8V_VGA

DPAB_VDD18

L59 *0_4/S

C709 *10U/6.3VS_6 | C711 1U/6.3V_4 | C714 0.1U/10V_4

AN24 DP_VDDR
AP24 DP_VDDR
AP25 DP_VDDR
AP26 DP_VDDR
AU28 DP_VDDR
AV29 DP_VDDR

DPCD_VDD18

L57 *0_4/S

C699 *10U/6.3VS_6 | C708 1U/6.3V_4 | C702 0.1U/10V_4

AP20 DP_VDDR
AP21 DP_VDDR
AP22 DP_VDDR
AP23 DP_VDDR
AU18 DP_VDDR
AV19 DP_VDDR

DPEF_VDD18

L61 *0_4/S

C732 *10U/6.3VS_6 | C728 1U/6.3V_4 | C733 0.1U/10V_4

AH34 DP_VDDR
AJ34 DP_VDDR
AF34 DP_VDDR
AG34 DP_VDDR
AM37 DP_VDDR
AL38 DP_VDDR

SI , change to short pad

SI , change to DNI

R150 150/F_4 AW28 DPAB_CALR

R365 150/F_4 AW18 DPCD_CALR

R377 150/F_4 AM39 DPEF_CALR

DP_VDDC AP31
DP_VDDC AP32
DP_VDDC AN33
DP_VDDC AP33

DP_VDDC AP13
DP_VDDC AT13
DP_VDDC AP14
DP_VDDC AP15

DP_VDDC AL33
DP_VDDC AM33
DP_VDDC AK33
DP_VDDC AK34

DP_VSSR AN27
DP_VSSR AP27
DP_VSSR AP28
DP_VSSR AW24
DP_VSSR AW26
DP_VSSR AN29
DP_VSSR AP29
DP_VSSR AP30
DP_VSSR AW30
DP_VSSR AW32
DP_VSSR AN17
DP_VSSR AP16
DP_VSSR AP17
DP_VSSR AW14
DP_VSSR AW16
DP_VSSR AN19
DP_VSSR AP18
DP_VSSR AP19
DP_VSSR AW20
DP_VSSR AW22
DP_VSSR AN34
DP_VSSR AP39
DP_VSSR AR39
DP_VSSR AU37
DP_VSSR AF39
DP_VSSR AH39
DP_VSSR AK39
DP_VSSR AL34
DP_VSSR AV27
DP_VSSR AR28
DP_VSSR AV17
DP_VSSR AR18
DP_VSSR AN38
DP_VSSR AM35

DPAB_VDD10

DP/TMDS/LVDS Transmitter Power
0.935V@222mA per port

+1.0V_VGA

*0_4/S L60

C722 0.1U/10V_4 | C721 1U/6.3V_4 | C720 *10U/6.3VS_6

DPCD_VDD10

DP/TMDS/LVDS Transmitter Power
0.935V@222mA per port

+1.0V_VGA

*0_4/S L58

C710 0.1U/10V_4 | C706 1U/6.3V_4 | C700 *10U/6.3VS_6

SI , change to short pad

DPEF_VDD10

DP/TMDS/LVDS Transmitter Power
0.935V@222mA per port

+1.0V_VGA

*0_4/S L28

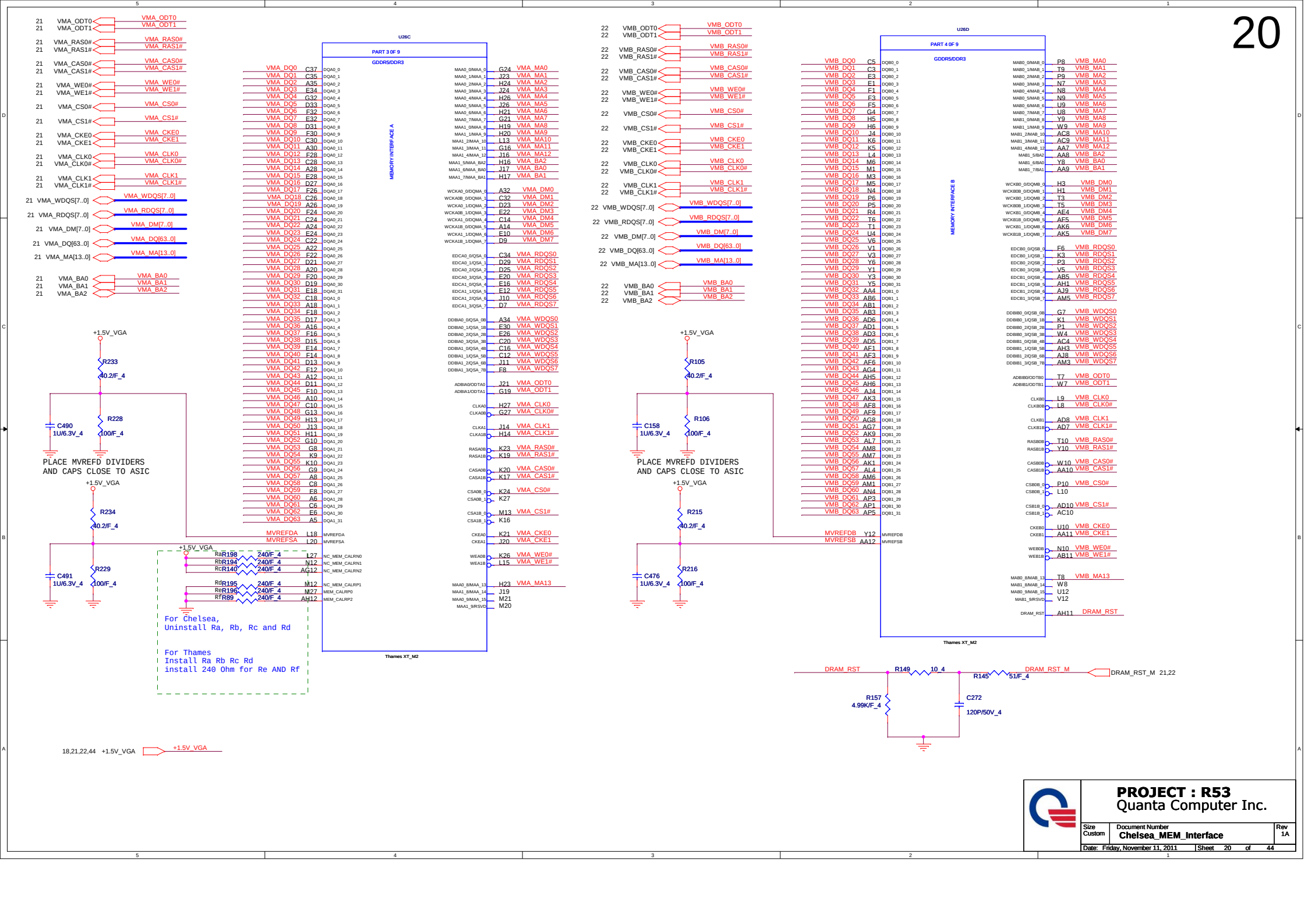
C279 0.1U/10V_4 | C278 1U/6.3V_4 | C277 *10U/6.3VS_6

SI , change to DNI

PROJECT : R53
Quanta Computer Inc.

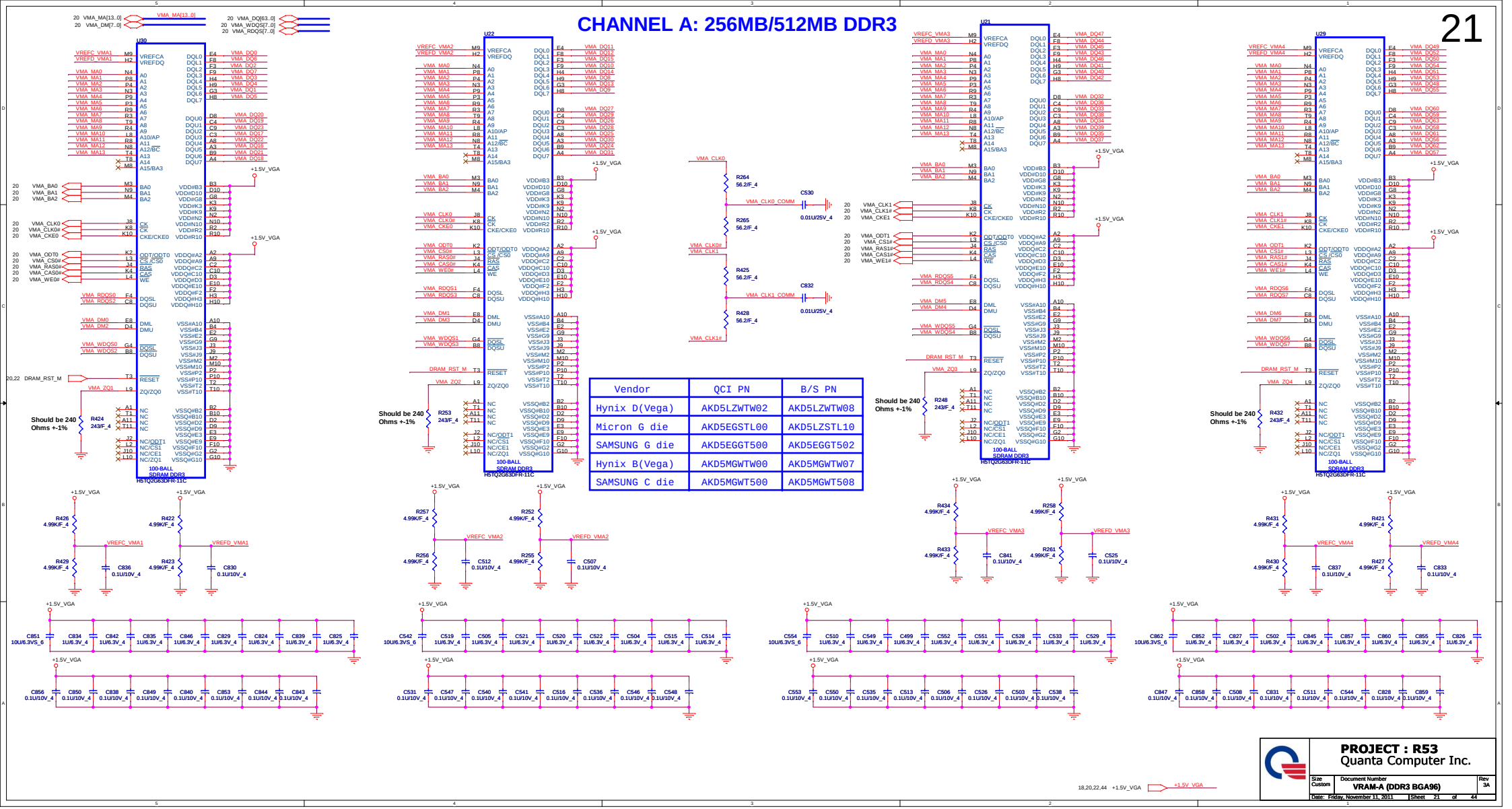
Size	Document Number	Rev
Custom	Chelsea_DP Powers	1A

Date: Monday, November 14, 2011 | Sheet 19 of 44



PROJECT : R53	
Quanta Computer Inc.	
Size: Custom	Document Number: Chelsea_MEM_Interface
Rev: 1A	
Date: Friday, November 11, 2011	Sheet 20 of 44

CHANNEL A: 256MB/512MB DDR3



Vendor	QCI PN	B/S PN
Hynix D(Vega)	AKD5LZWTW02	AKD5LZWTW08
Micron G die	AKD5EGSTL00	AKD5LZSTL10
SAMSUNG G die	AKD5EGGT500	AKD5EGGT502
Hynix B(Vega)	AKD5MGWTW00	AKD5MGWTW07
SAMSUNG C die	AKD5MGWT500	AKD5MGWT508

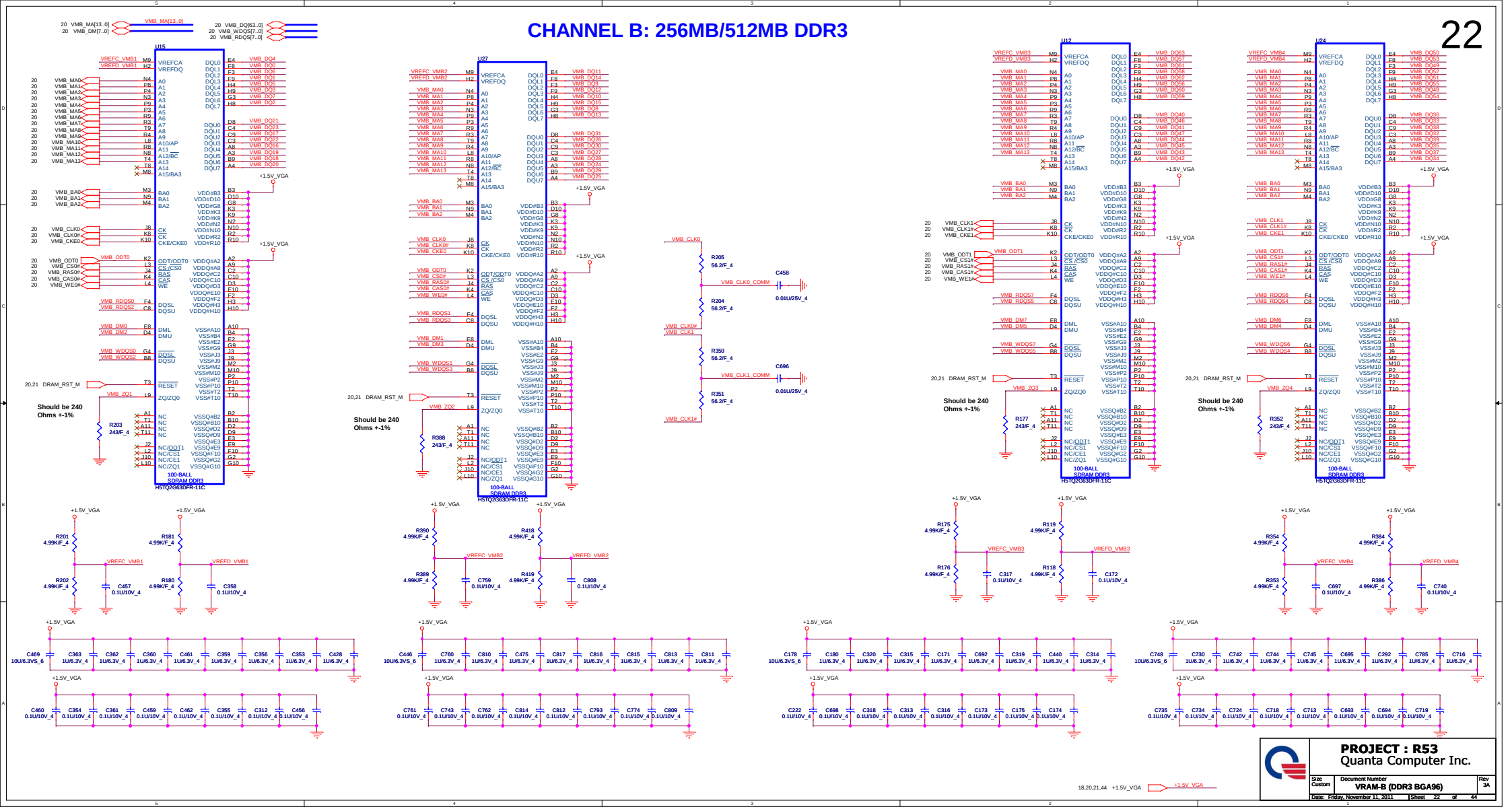
18,20,22,44 +1.5V_VGA +1.5V_VGA

PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	VRAM-A (DDR3 BGA96)	3A

Date: Friday, November 11, 2011 Sheet 21 of 44

CHANNEL B: 256MB/512MB DDR3



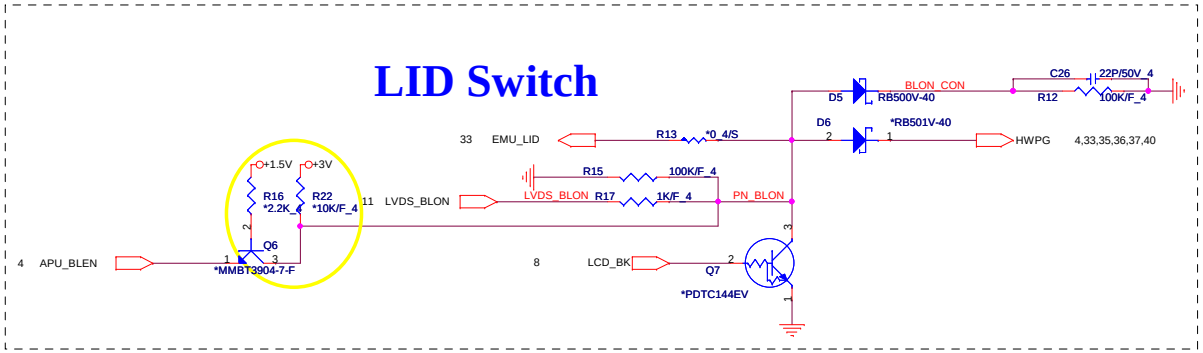
18,20,21,44 +1.5V_VGA +1.5V_VGA

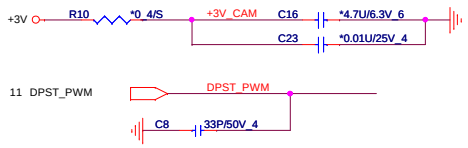
PROJECT : R53
Quanta Computer Inc.

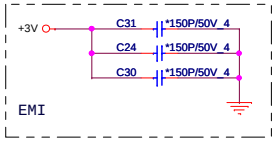
Size	Document Number	Rev
Custom	VRAM-B (DDR3 BGA96)	3A

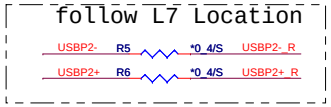
Date: Friday, November 11, 2011 Sheet 22 of 44

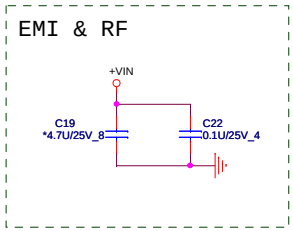
LID Switch

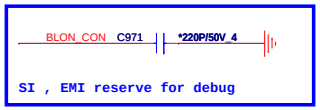


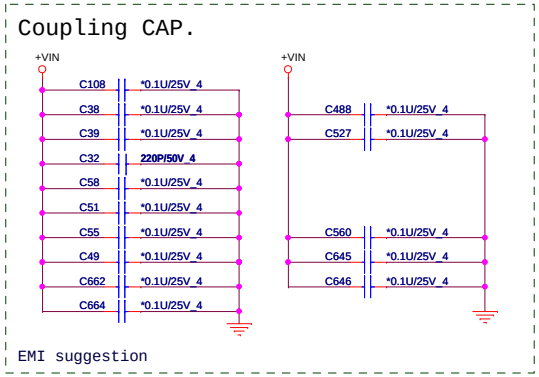


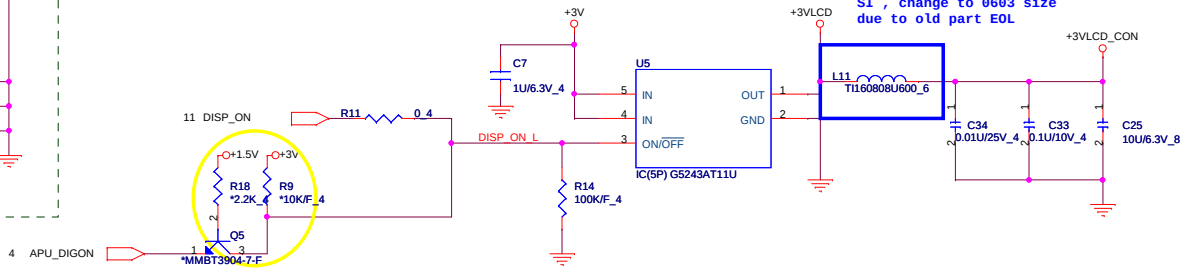


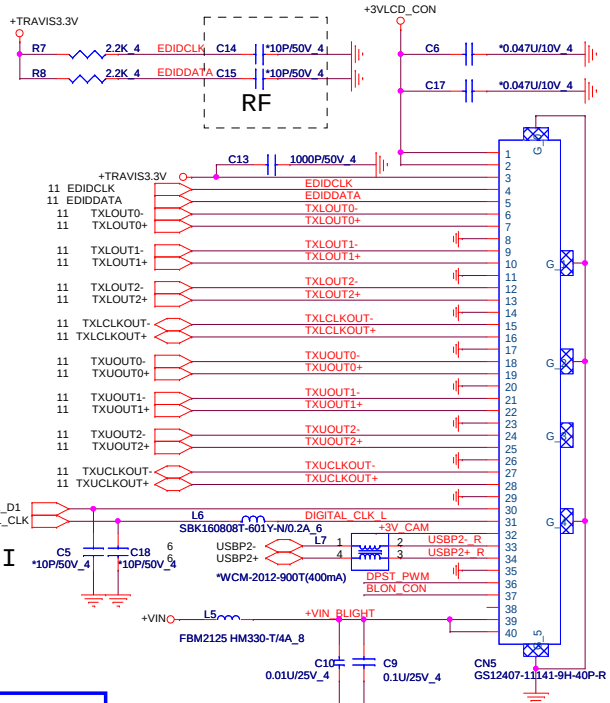










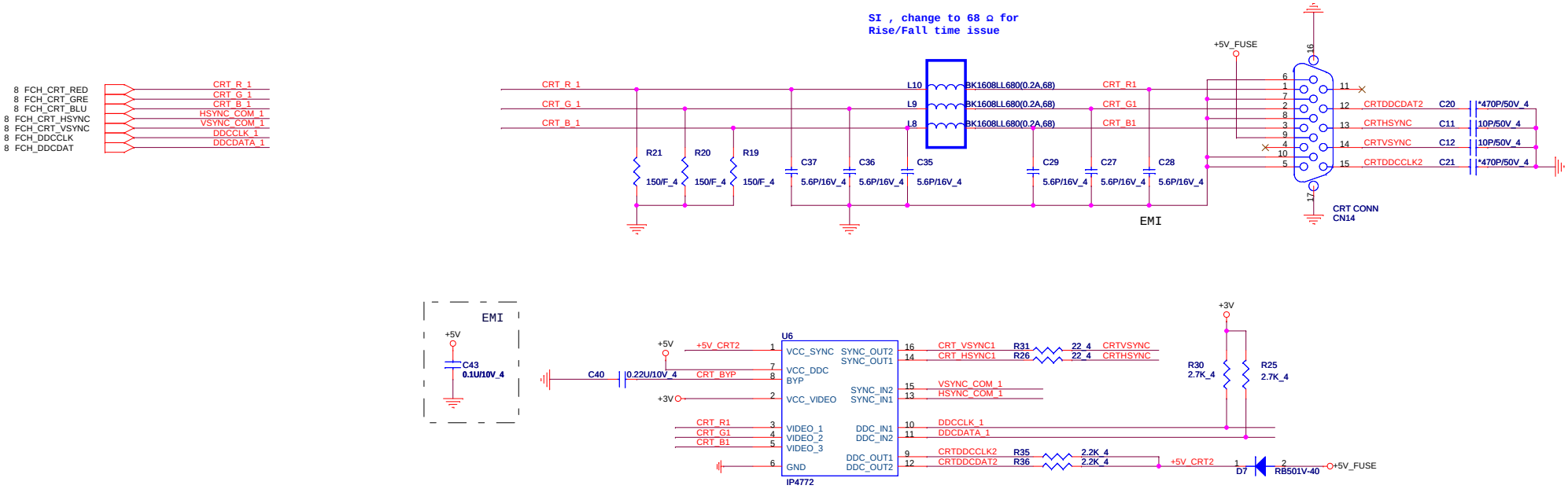


4,7,30,33,34,35 +3VPCU
2,4,6,8,9,10,11,12,13,14,18,24,25,26,27,28,29,30,31,32,33,41,42,44 +3V
9,34,41,44 +12VALW
34,35,36,37,39,40,41,42,44 +VIN

PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN/LID/CAM	1A
Date: Friday, November 11, 2011	Sheet 23 of 44	

CRT PORT



HOLE

SI2 , update footprint

H15 *H-C354I150D110P2
H18 *H-C354I150D110P2
H10 *H-O472X354I272X150D232X110P2
H6 *h-c354i150d110p2
H14 *H-C354I150D110P2
H5 *H-C354I150D110P2
H7 *H-C354I150D110P2
H8 *H-C236I150D110P2
H16 *H-C276I150D110P2
H17 *H-C197D110P2
H22 *SPAD-CXX-1
H19 *h-c354d354n

PAD2
*EMIPAD
SI , add for EMI

FCH NUT

H21 H-TC354BC217I197D157P2
H20 H-TC354BC217I197D157P2

VGA BKT

H13 *H-TC248BC197D150P2
H12 *H-TC248BC197D150P2
H9 *H-TC248BC197D150P2

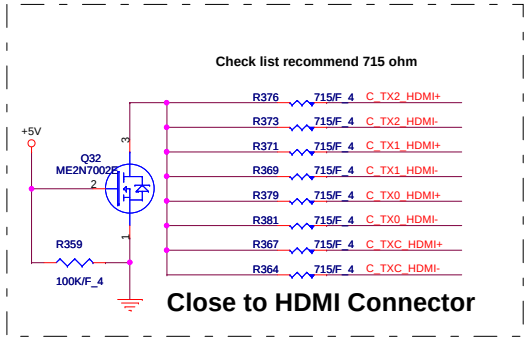
APU BKT

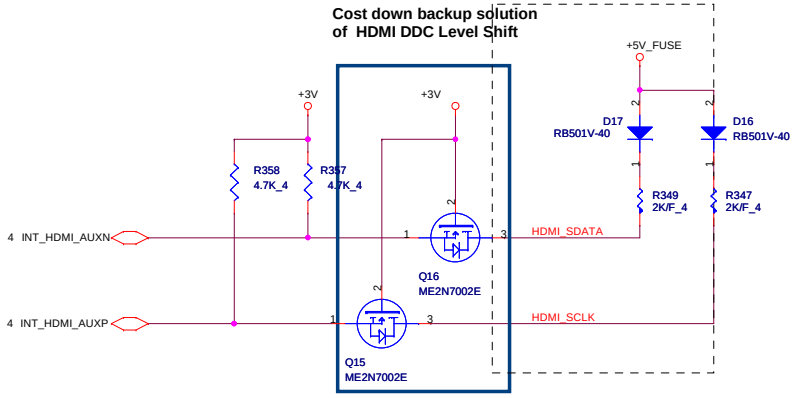
H11 *intel-cpu-bkt2

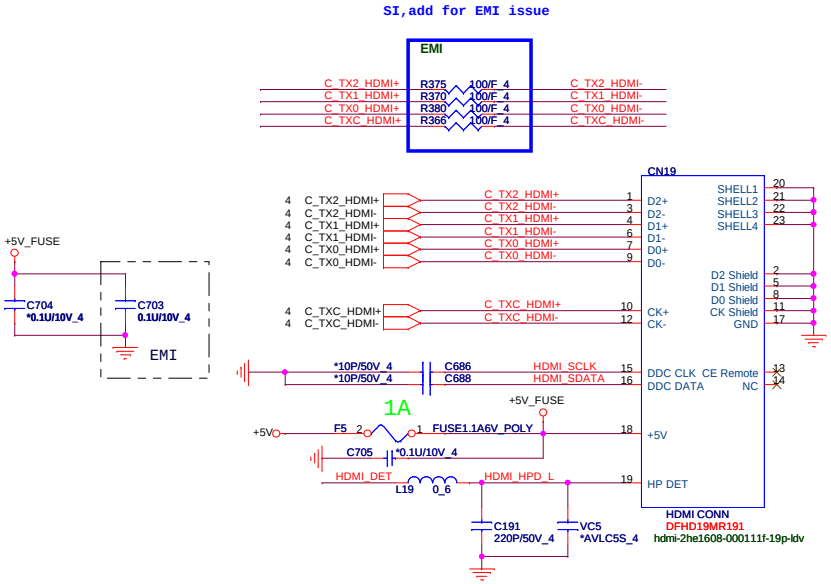
PROJECT : R53
Quanta Computer Inc.

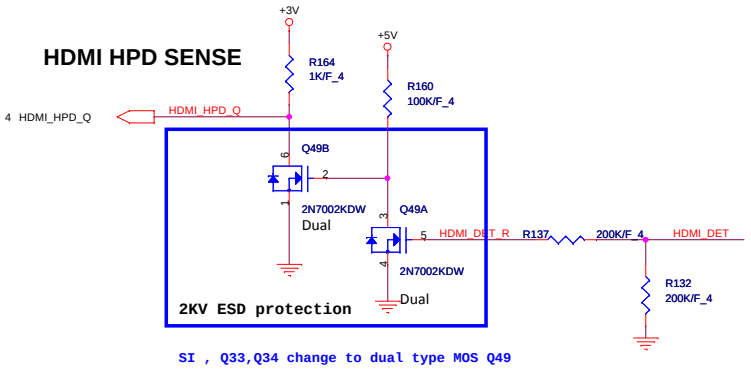
Size	Document Number	Rev
Custom	CRT,Hole	1A
Date: Friday, November 11, 2011	Sheet 24 of 44	

HDMI PORT



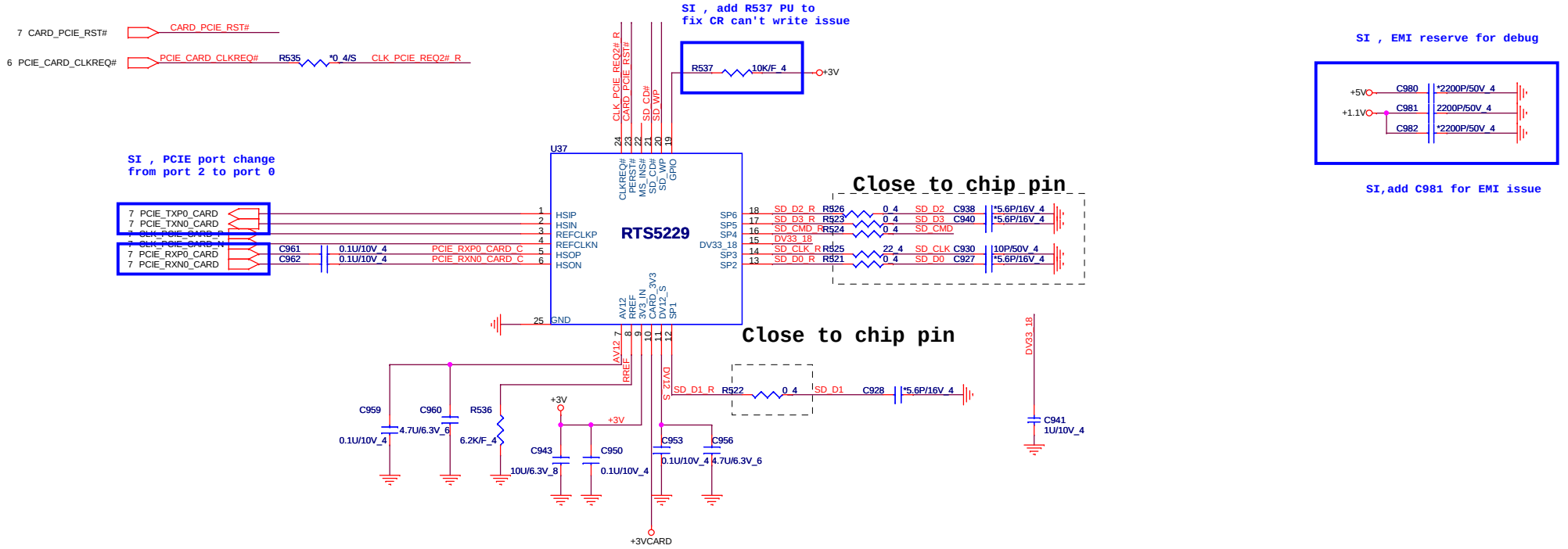




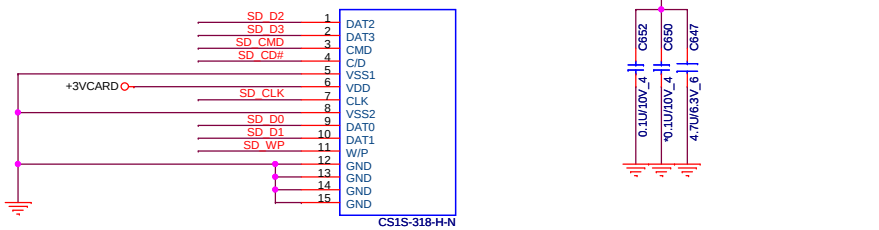


SI , Q33,Q34 change to dual type MOS Q49

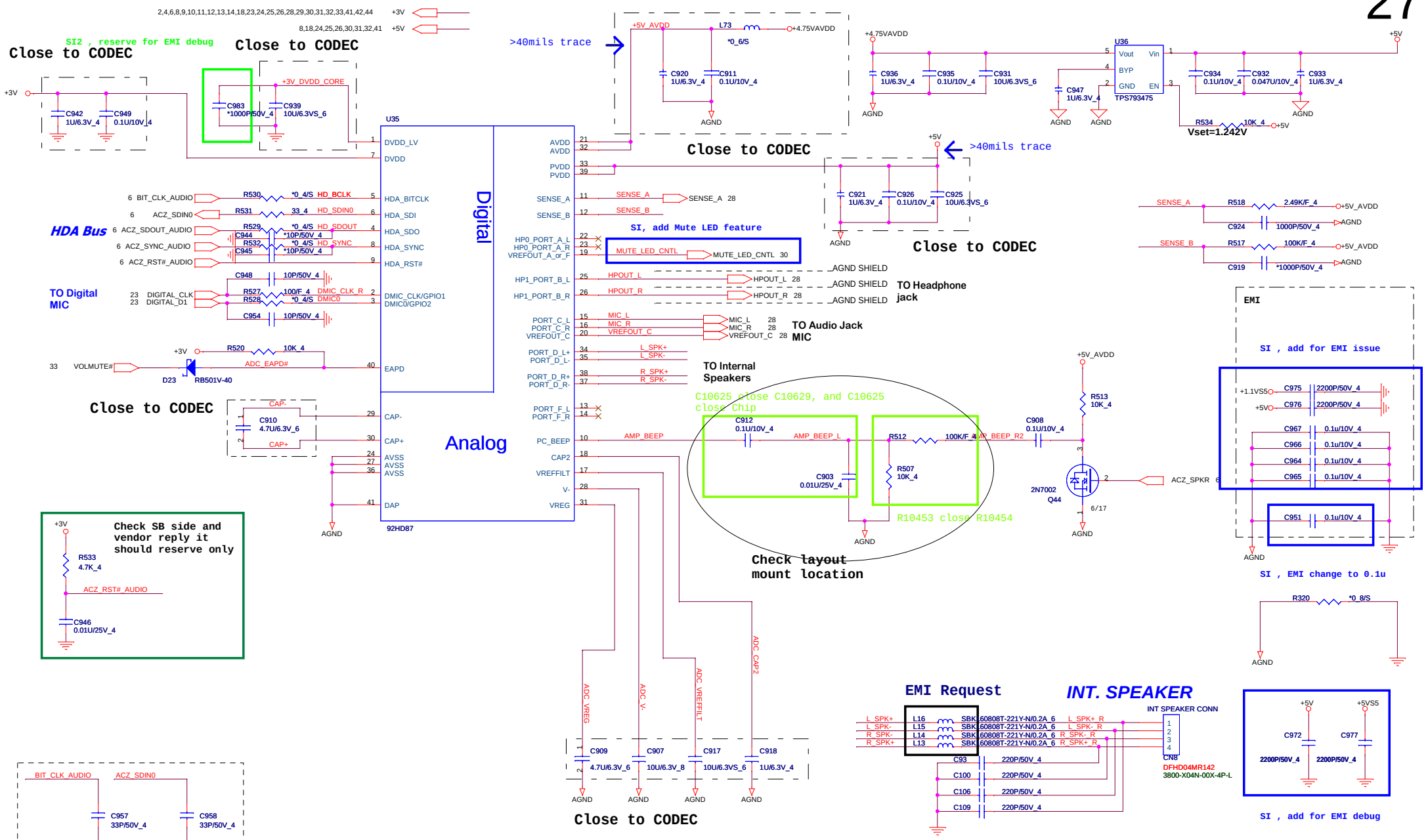
PROJECT : R53 Quanta Computer Inc.		
Size: Custom	Document Number: HDMI CONN	Rev: 1A
Date: Friday, November 11, 2011	Sheet 25 of 44	



SD / MMC CARD READER



CLOSE CONN



PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Azalia 92HD80	1A

Date: Friday, November 11, 2011 Sheet 27 of 44

USB3.0 X 2/USB2.0 COMBO

28

USB 3.0

SI,add choke remove R for EMI issue

EMI 1A

CN21 USB3.0 CONN

USB 3.0

SI,add choke remove R for EMI issue

EMI 1A

CN22 USB3.0 CONN

Right SIDE USBX1

9/14 SI for HW

EMI request

Line out

Normal Open

MIC

Normal Open

COMPONENT CHOICES:
The selection of ferrite beads can have a large effect on THD+N, causing failures versus the WLP requirements.
At this time, IDT has verified three ferrite beads that will meet the WLP performance requirements:
Murata: BLM18BD601SN1
TDK: MMZ1608Y601BTA
Taiyo Yuden: LF BK 1608HM601-T

PROJECT : R53 Quanta Computer Inc.		
Size: Custom	Document Number: USB/BT/Audio JacK	Rev: 1A
Date: Monday, November 14, 2011	Sheet 28 of 44	

For EMI 0 ~ 22 ohm

R72 10_4 LAN_XTAL1 XTAL1
Y5 25MHz XTAL2
C130 33P/50V_4
C129 33P/50V_4

+3VLANVCC
+3V_LAN
C127 0.1U/10V_4
C134 0.1U/10V_4
C131 0.1U/10V_4
C148 0.1U/10V_4

GND VIA x 9 Pcs

+1.05V_LAN
R71 2.49K/F_4 LANRSET
+3V_LAN
LAN_TX#
LAN_GPIOS R73 1K/F_4 +3V_LAN
LAN_GLINK100#

U10 RTL8105E

49	GND	REGOUT	36
48	AVDD33	VDDREG	35
47	AVDD33	VDDREG	34
46	RSET	ENSWREG	33
45	AVDD10	EEDI	32
44	CKXTAL2	LED3/EEDO	31
43	CKXTAL1	EECS	30
42	AVDD33	DVDD10	29
41	DVDD10(NC)	LANWAKEB	28
40	LED1	DVDD33	27
39	DVDD33	ISOLATEB	26
38	GPO/SMBALERT	PERSTB	25
37	LED1/EESK		
1	MDIP0		
2	MDIN0		
3	AVDD10		
4	MDIP1		
5	MDIN1		
6	AVDD10(NC)		
7	MDIP2(NC)		
8	MDIN2(NC)		
9	AVDD10(NC)		
10	MDIP3(NC)		
11	MDIN3(NC)		
12	AVDD33(NC)		
13	DVDD10		
14	SMBCLK(NC)		
15	SMBDATA(NC)		
16	CLKREQB		
17	HSIP		
18	HSIN		
19	REFCLK_P		
20	REFCLK_N		
21	DVDD10		
22	HSOP		
23	HSON		
24	GND		

MDI0+ MDI0-
MDI1+ MDI1-
LAN_GLINK10# R82 10K/F_4
LAN_ECS_SCL R80 10K/F_4
PCIE_WAKE# +1.05V_LAN
+3V_LAN
ISOLATEB
LAN_PCIE_RST# 7,11
PCIE_WAKE# 6,32

+1.05V_LAN
PCIE_LAN_CLKREQ# R107 *0_4/S
LAN_CLKRQ
PCIE_TXP1_LAN
PCIE_TXN1_LAN
CLK_PCIE_LANP
CLK_PCIE_LANN
PCIE_RXN1_LAN_L C161 0.1U/10V_4 PCIE_RXN1_LAN 7
PCIE_RXP1_LAN_L C160 0.1U/10V_4 PCIE_RXP1_LAN 7
+1.05V_LAN

+3V
R104 1K_4
ISOLATEB
R94 15K/F_4

if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

U9 NS681684

LAN_MX0+	1 TD+	TX+ 16	MDI0+
LAN_MX0-	3 TD-	CMT 15	V_DAC2
LAN_MCT1	2 CT	TX- 14	MDI0-
LAN_MX1+	6 RD+	RX- 9	MDI1-
LAN_MX1-	8 RD-	CT 10	V_DAC1
LAN_MCT0	7 CT	RX+ 11	MDI1+

75_4 R47 C89 0.01U/100V_0603
75_4 R48 C90 0.01U/100V_0603
C64 10P/3KV_1808
C95 0.01U/25V_4
6 PCIE_LAN_CLKREQ#
7 PCIE_TXP1_LAN
7 PCIE_TXN1_LAN
7 CLK_PCIE_LANP
7 CLK_PCIE_LANN

IND SMD 4.7UH +-20% 680MA(CBC2518T4R7M)
CV-4707MZ00

Power trace Layout 寬度> 60mil
>60mil

+1.05V_LAN
C112 1U/6.3V_4
C159 0.1U/10V_4
C149 0.1U/10V_4
C132 0.1U/10V_4
C145 0.1U/10V_4

+1.05V_LAN
C146 0.1U/10V_4
C155 0.1U/10V_4
C125 0.1U/10V_4
C115 0.1U/10V_4

LAN_GLINK100# LAN_GLED#
LAN_TX# LAN_YLED#
C764 *1000P/50V_4
C789 *1000P/50V_4
Link

RJ45

+3V_LAN R405 330_4 C791 1000P/50V_4
LAN_YLED
LAN_YLED#
LAN_MX1-
LAN_MX1+
LAN_MX0-
LAN_MX0+
+3V_LAN R391 330_4
LAN_GLED
LAN_GLED#
C779 180P/50V_4
C758 1000P/50V_4

CN20 RJ45_CONN

11	LED_AMBER_P	RX1-	8
12	LED_AMBER_N	RX1+	7
		RX0-	6
		TX1-	5
		TX1+	4
		RX0+	3
		TX0-	2
		TX0+	1
14	GND1	C797	180P/50V_4
13	GND	C757	180P/50V_4
9	LED_WHITE_P		
10	LED_WHITE_N		

PROJECT :	R53
Quanta Computer Inc.	
Size: Custom	Document Number: RTL 8105E/RJ45
Rev: 1A	
Date: Monday, November 14, 2011	Sheet 29 of 44

POWER BOTTON CONNECT

SI , reserve for Lid
+3VPCU noise

100mA

C963 *4.7U/6.3V_6
C122 1U/6.3V_4
C121 0.1U/10V_4

+3VPCU

33 LID_EC#
33 NBSWON1#
33 PWR_LED#

PWR_LED#

CN7
PWR BTN CONN

1. +3VPCU(LIDSWITCH PWR)
2. +3VPCU(LIDSWITCH PWR)
3. LIDSWITCH
4.POWERON#
5. PWRLED#
6. GND

SI , contact to +3VPCU

C117 PWR_LED# 0.1U/10V_4
C119 LID_EC# 0.1U/10V_4

SI , delete C120 for QB button drop

C118 NBSWON1# 0.1U/10V_4

SI , delete G5 for space save

KEYBOARD Con.

MY5 C141 220P/50V_4
MY6 C166 220P/50V_4
MY3 C170 220P/50V_4
MY7 C154 220P/50V_4

MY8 C162 220P/50V_4
MY9 C124 220P/50V_4
MY10 C211 220P/50V_4
MY11 C201 220P/50V_4

MY1 C143 220P/50V_4
MY2 C147 220P/50V_4
MY4 C150 220P/50V_4
MY0 C136 220P/50V_4

MX4 C128 220P/50V_4
MX6 C116 220P/50V_4
MX3 C139 220P/50V_4
MX2 C138 220P/50V_4

MX7 C113 220P/50V_4
MX0 C144 220P/50V_4
MX5 C133 220P/50V_4
MX1 C110 220P/50V_4

MY12 C182 220P/50V_4
MY13 C187 220P/50V_4
MY14 C196 220P/50V_4
MY15 C219 220P/50V_4
MY16 C235 220P/50V_4
MY17 C244 220P/50V_4

33 MY[0..17] MY[0..17]
33 MX[0..7] MX[0..7]

SI , mount for EMI

CN9

MX1 1
MX7 2
MX6 3
MY9 4
MX4 5
MX5 6
MY0 7
MX2 8
MX3 9
MY5 10
MY1 11
MX0 12
MY2 13
MY4 14
MY7 15
MY8 16
MY6 17
MY3 18
MY12 19
MY13 20
MY14 21
MY11 22
MY10 23
MY15 24
MY16 25
MY17 26
27
28
29
30
31
32

KB CONN

SI2 , for mute LED issue

33 CAPSLED#

+3V

R541 10K/F_4

27 MUTE_LED_CNTL

C984 *220P/50V_4

Q47 2N7002

R392 *10K/F_4

SI2 , reserve for EMI

SI, add Mute LED feature

R152 200/F_6 CAPSLED# R
R153 200/F_6 MUTE_LED_CNTL_R
WIRELESS_ON_R
WIRELESS_OFF_R

+5V

R159 1K/F_4

R158 *200/F_6

WIRELESS_ON_R

33 WIRELESS_ON

Q17 PDTC144EU

R161 1K/F_4

R163 *200/F_6

WIRELESS_OFF_R

33 WIRELESS_OFF

Q18 PDTC144EU

KEYBOARD PULL-UP

RP6
+3VPCU
MY13 MY12 MY3 MY6
MY14 MY11 MY10 MY15
*10P8R-8.2K

RP5
+3VPCU
MY1 MY5 MY0 MY9
MY2 MY4 MY7 MY8
*10P8R-8.2K

R142 *8.2K_4 MY16
R148 *8.2K_4 MY17

TOUCH PAD Con.

TP_LED# C970 *220P/50V_4
SMB_ACC_DAT C968 *220P/50V_4
SMB_ACC_CLK C969 *220P/50V_4

+5VS5

C973 *220P/50V_4
C974 *220P/50V_4
C978 *2200P/50V_4

SI , EMI reserve for debug

change to +3VSUS
close conn

+3VSUS R254 4.7K_4 TPCLK
R251 4.7K_4 TPDATA

33 TPLED# TP_LED#

C509 10P/50V_4
L39 BLM18BA470SN1D/0.3A_6
L38 BLM18BA470SN1D/0.3A_6
C501 10P/50V_4

33 TPCLK
33 TPDATA

TPCLK-1
TPDATA-1

25 mils

SMB_ACC_DAT
SMB_ACC_CLK

CN11
8 7 6 5 4 3 2 1

+3VSUS C492 0.1U/10V_4

TOUCH PAD CONN
DFFC08FR026
50503-0080n-001-8p-l

Q51A 2N7002KDW
Dual

15 GPUT_CLK
SMB_ACC_CLK
SMB_ACC_CLK 33

R263 4.7K_4
+3VSUS

+3V_VGA

R262 4.7K_4
SMB_ACC_DAT 33

15 GPUT_DATA
SMB_ACC_DAT

Q51B 2N7002KDW
Dual

2KV ESD protection

SI , Q21,Q22 change to dual type MOS Q51

4,7,33,34,35 +3VPCU
8,18,24,25,26,27,31,32,41 +5V
32,41 +3VSUS
2,4,6,8,9,10,11,12,13,14,18,23,24,25,26,27,28,29,31,32,33,41,42,44 +3V

Q64A *2N7002KDW
Dual
SMB_ACC_CLK
SCL1 6
+3VSUS
SMB_ACC_DAT
SDA1 6
Dual
Q64B *2N7002KDW

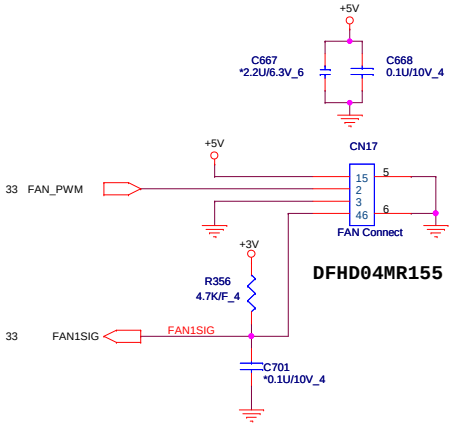
SI2 , HP request Image sensor
SMBUS reserve to FCH

PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KB/SW/TP	1A

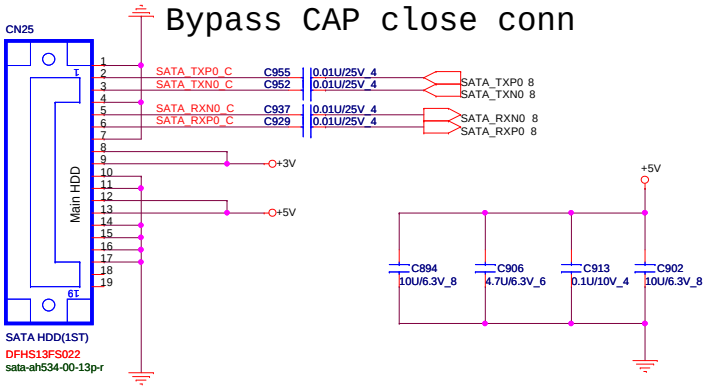
Date: Friday, November 11, 2011 Sheet 30 of 44

CPU FAN



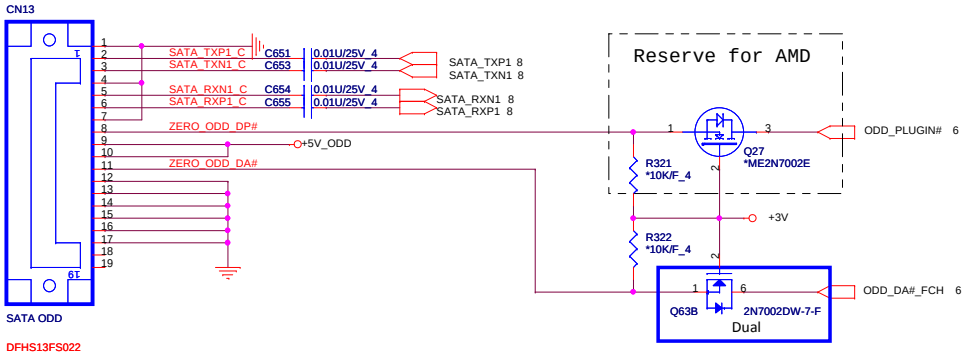
SATA HDD CONNECTOR

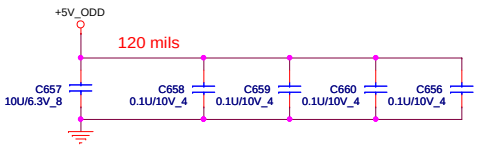
Bypass CAP close conn

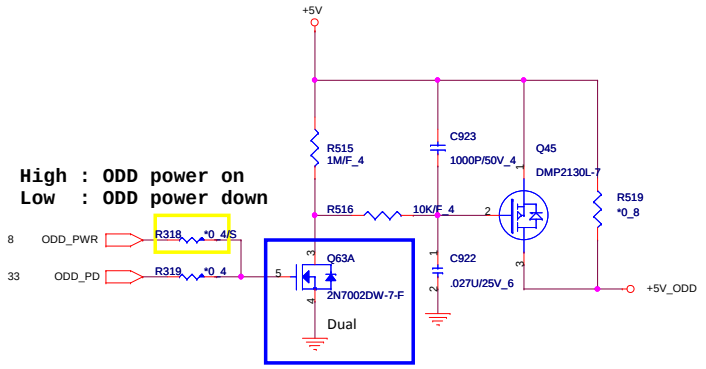


SATA ODD CONNECTOR

SATA ODD







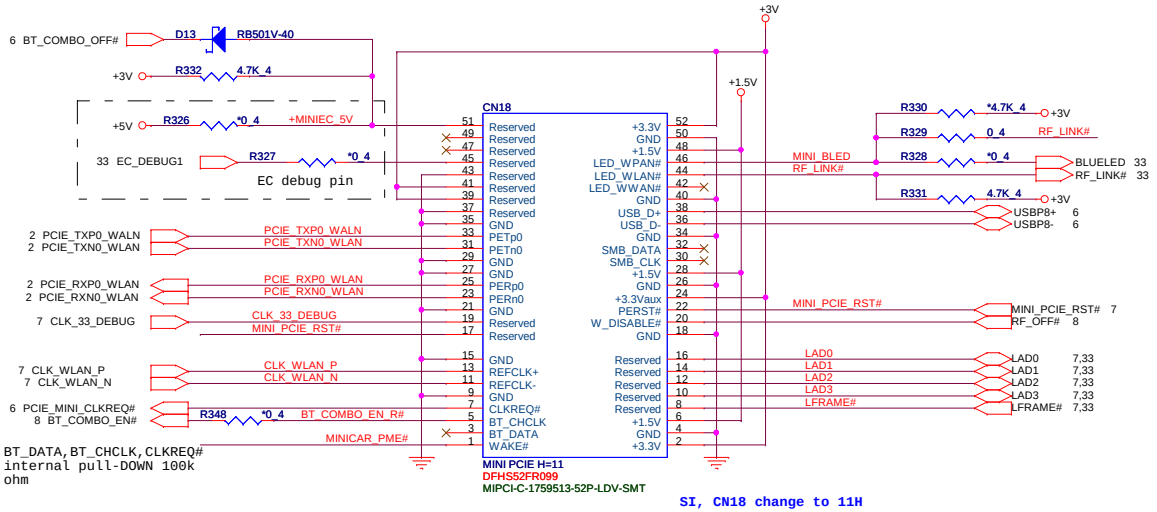
SI , Q28,Q43 change to dual type MOS Q63

PROJECT : R53
Quanta Computer Inc.

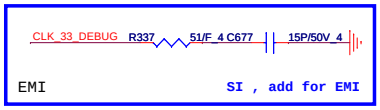
Size	Document Number	Rev
Custom	HDD/ODD/FAN	1A

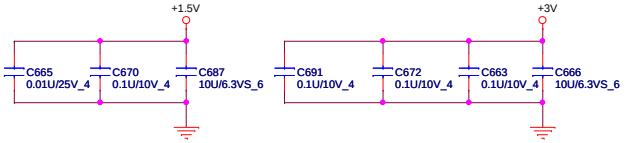
Date: Friday, November 11, 2011 Sheet 31 of 44

Mini PCI-E Card 1 WLAN

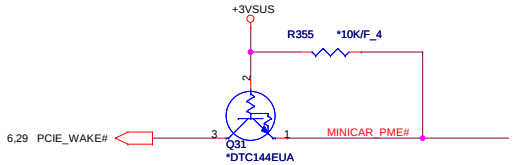


SI, CN18 change to 11H



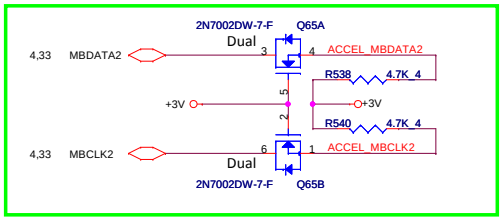


INTEL WLAN CARD PIN 20 W_DISABLE# have internal pull-up 110k ohm

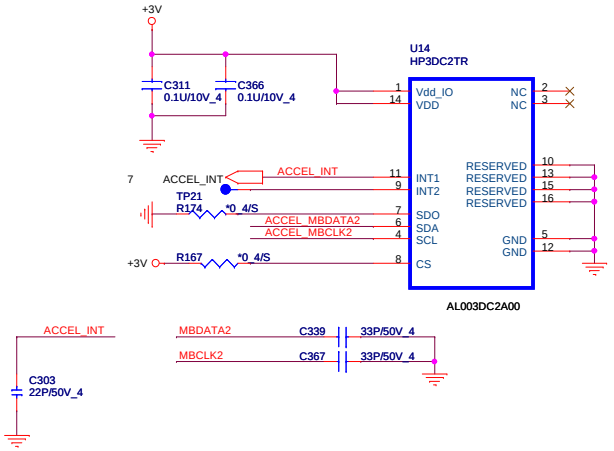


2,4,11,23,38,41 +1.5V
2,4,6,8,9,10,11,12,13,14,18,23,24,25,26,27,28,29,30,31,33,41,42,44 +3V
4,7,30,33,34,35 +3VPCU
8,18,24,25,26,27,30,31,41 +5V

Accelerometer Sensor



SI2 , add for avoid leakage from SUS power



PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MINI PCIE & G-sensor	1A
Date: Friday, November 11, 2011	Sheet 32 of 44	

ITE pin 100 , 104 , 106 default can not pull up to +3VPCU it will cause chip into test mode

+3VPCU CAP close to EC pin

Smart adapter Type check

Change to 1SS355 as Current loss

D18 1SS355

AD_TYPE R387 10K/F_4 R383 100/F_4 AD_ID 34

C739 0.1U/10V_4 R382 12K/F_4 C737 100P/50V_4

+3VPCU_AC L65 SBK160808T-121Y-N

+3VPCU_EC L64 SBK160808T-121Y-N

500mA

Change to RB500 as Current loss

SCI1# D20 RB501V-40 SIO_EXT_SCI# 6

DNBSWON1# D21 RB501V-40 DNBSWON# 6

KBSMI#1 D19 RB501V-40 SIO_EXT_SMI# 6

SI , del QB button PU resistor R392

HWPG C802 *0.1U/10V_4

FAN1SIG C763 *0.1U/10V_4

DGPU_PR_EN C483 *0.1U/10V_4

For +VIN noise

SI2,change to +3VS5 for leakage issue

Vender	Size	P/N
AMIC	4M	AKE39F-0800
EON	4M	AKE39ZN0Q02
Socket		DFHS08FS023

4M SPI EC ROM

U20 EN25Q32B-104HIP AKE39ZN0Q02 SOIC8-8-1_27

BIOS_CS# BIOS_SPI_CLK_I BIOS_WR# BIOS_RD# SPI_3P SPI_7P

SI , add for EMI

128K byte SPI EC ROM

U19 *DFHS08FS023 SOIC8-6-1_27

TP92 TP90 TP91 TP89 TP39 TP37

ICT need TP2675 size test point

R259 33_4 EMI C517 22P/50V_4

R223 10K/F_4 SPI_3P R222 *100K/F_4 SI

TP place on top lay for ICT request

Adapter select

+3VPCU R395 10K/F_4 GPIO42 R396 *10K/F_4

Hi ==> DIS/SG
Low ==>UMA

Platform model	GPIO42	adapter
SG/DIS	High	90W
UMA	Low	65W

IT8518E/HX

AJ085180F04

IT8518E/HX

LPC: LAD0 LAD1 LAD2 LAD3 KBC_RST# CLK_33M_KBC LFRAME# LPCPD#/WUI6/GPE6 EC_A20GATE SERIRQ KBSMI#1 SCI1# 3920_RST# EC_RCIN#

SI, remove NUMLED#

GPIO: GA20/GPB5 SERIRQ ECSMI#/GPD4 ECSCI#/GPD3 WRST# KBRST#/GPB6 PWUREQ#/BBO/GPC7 GPC0 TMA0/GPB2 RSMRST# H_PROCHOT# BLUELED TPDATA TPCLK VR2.5_ON DGPU_PR_EN HWPG EMU_LID EC_DEBUG1 USBPW_ON# BIOS_SPI_CLK BIOS_RD# BIOS_WR# BIOS_CS# GPU_AC_BATT

PS/2: PS2DAT0/TMB1/GPF1 PS2CLK0/TMB0/GPF0 PS2DAT2/WUI21/GPF5 PS2CLK2/WUI20/GPF4

UART: DAC4/DCD0#/GPJ4 DSR0#/GPG6 GINT/CTS0#/GPD5 PS2DAT1/RTS0#/GPF3 DAC5/RIG0#/GPJ5 PS2CLK1/DTR0#/GPF2 RXD/SIN0/GPB0 TXD/SOUT0/GPB1

FLASH: GPG0 FSCK FMISO FMOSI FSCE# SSCE0#/GPG2

KBMX: KSO0/PD0 KSO1/PD1 KSO2/PD2 KSO3/PD3 KSO4/PD4 KSO5/PD5 KSO6/PD6 KSO7/PD7 KSO8/ACK# KSO9/BUSY KSO10/PE KSO11/ERR# KSO12/SLCT KSO13 KSO14 KSO15 KSI0/STB# KSI1/AFD# KSI2/INIT# KSI3/SLIN# KSI4 KSI5 KSI6 KSI7 MY0 MY1 MY2 MY3 MY4 MY5 MY6 MY7 MY8 MY9 MY10 MY11 MY12 MY13 MY14 MY15 MX0 MX1 MX2 MX3 MX4 MX5 MX6 MX7

CLOCK: CK32K CK32KE OSCI OSCIO *32.768KHZ *27P/50V_4 C481 C473 Y6 R217 0_4

SMBUS: SMB_ACC_CLK SMB_ACC_DAT MBCLK MBDATA MBCLK2 MBDATA2

Add TP SMBUS signal

Add G-sensor SMBUS signal

For GPU thermal

for Battery charge/discharge

for CPU themal

PWM: PWM0/GPA0 PWM1/GPA1 PWM2/GPA2 PWM3/GPA3 PWM4/GPA4 PWM5/GPA5 PWM6/SSCK/GPA6 PWM7/GPA7 TACH0/GPD6 TACH1/TMA1/GPD7 TMR0/WUI2/GPC4 TMR1/WUI3/GPC6

WIRELESS_OFF WIRELESS_ON AC_LED_ON# MBATLED0# FAN_PWM LAN_POWER VOLMUTE# PWM_VADJ FAN1SIG S5_ON SUSC# ECPWROK

WAKE UP: PWRSW/GPE4 RI1#/WUI0/GPD0 RI2#/WUI1/GPD1 WUI5/GPE5 RING#/PWRFAIL#/CK32KOUT/LPCRST#/GPB7 NBSWON1# LID_EC# ACIN SUSB# PWR_LED#

from power button

A/D D/A: ADC0/GPI0 ADC1/GPI1 ADC2/GPI2 ADC3/GPI3 ADC4/WUI28/GPI4 ADC5/WUI29/GPI5 ADC6/WUI30/GPI6 ADC7/WUI31/GPI7 R185 0_4 R393 0_4 VGA_ON_SB DGPU_PWROK SYS_I AD_AIR TEMP_MBAT AD_TYPE GPIO42

SI , drop QB button feature

DAC0/GPJ0 DAC1/GPJ1 DAC2/GPJ2 DAC3/GPJ3 BATSHIP PCI_SERR# ODD_PD DNBSWON1#

L32 BK1608HS121-T L34 BLM15AG700SS1_4 C484 *22P/50V_4 C447 0.1U/10V_4 C451 0.1U/10V_4 C775 0.1U/10V_4 R406 0_4 KBC_P+3V R416 0_4

C806 C485 C798 C780 C768 C805 C804 C783 C765 C807 0.1U/10V_4 *10U/6.3V_8

+3V +3VPCU +5VPCU +3VPCU_AC +3VPCU_EC

IT8518_AGND

DC_JACK 90W

Do Not add test pad on BATDIS_G signal

Place this ZVS close to Diode away +VIN

To PWR LED

Place this ZVS close to Far-Far away +VIN

Place this cap close to EC

Place this cap close to EC

Place this cap close to EC

ACDET=13V

MIN. BATV=7.2V

PU8 BQ24728

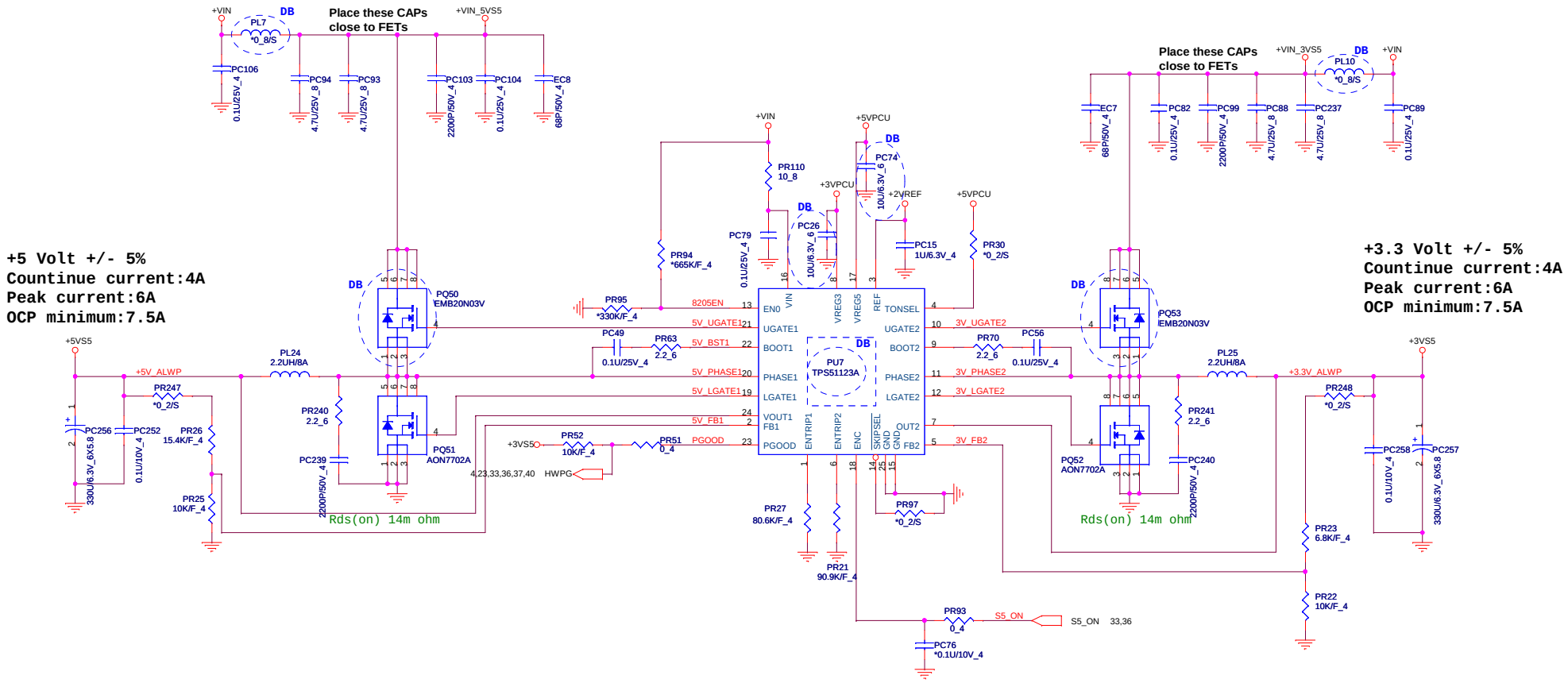
DC-IN CONN

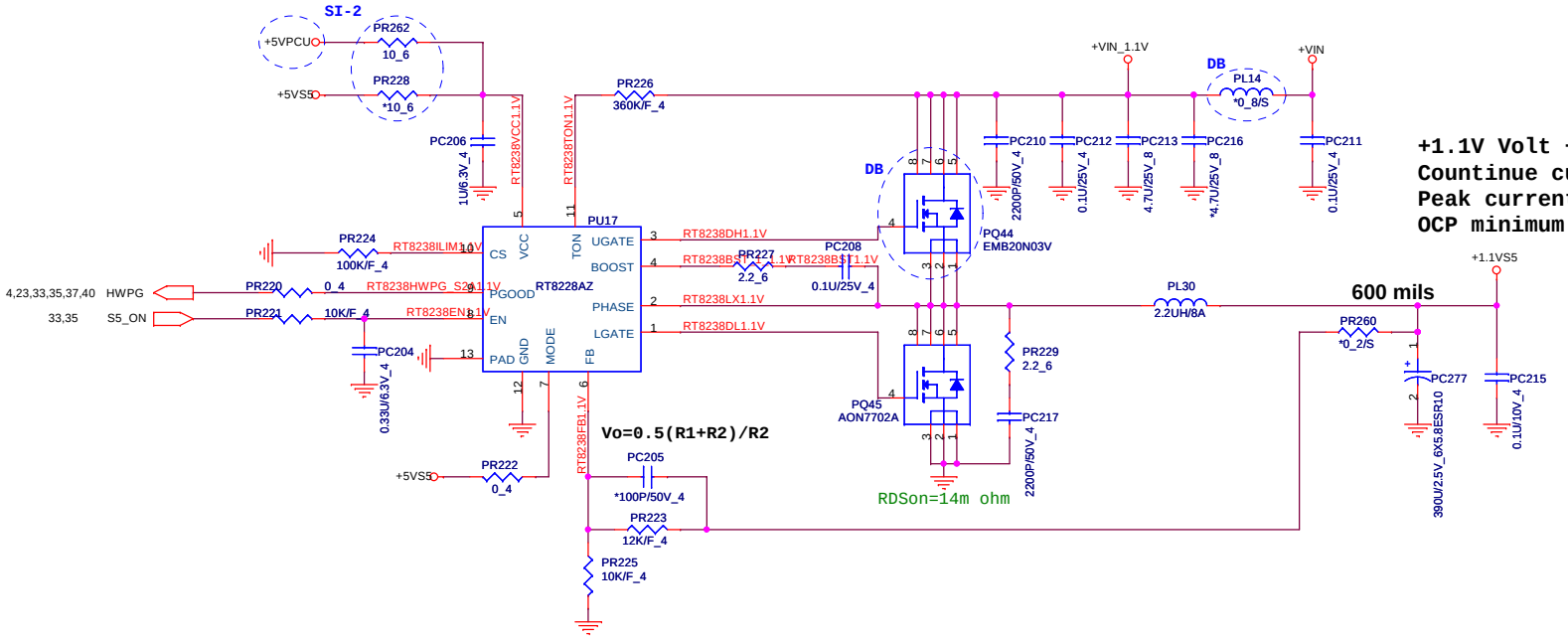
+VA
+VH28 41
+VAD_1 41
+3VPCU 4,7,30,33,35
+5VPCU 4,35,36
+BATCHG

PROJECT : R53
Quanta Computer Inc.

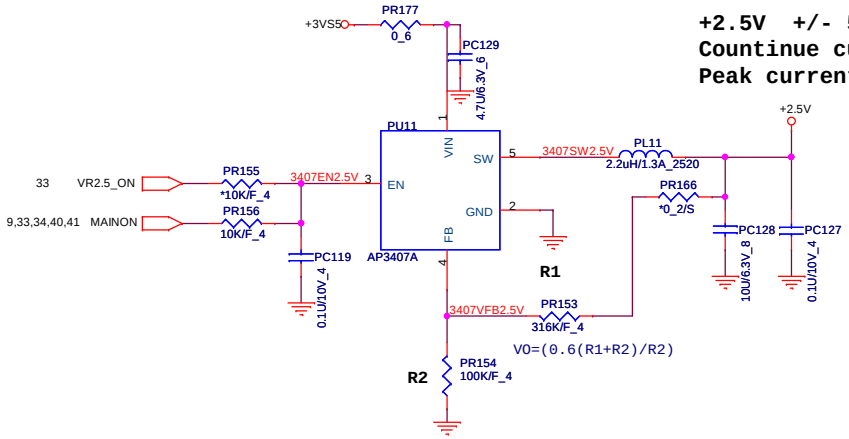
Size	Document Number	Rev
Custom	Charger (BQ24728)	1A

Date: Friday, November 11, 2011 Sheet 34 of 44


+5 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A
+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A
Place these CAPs close to FETs
Place these CAPs close to FETs
DB for prevent interference
PU7 TPS51123A
PQ50 EMB20N03V
PQ51 AON7702A
PQ52 AON7702A
PQ53 EMB20N03V
Rds(on) 14m ohm
Rds(on) 14m ohm
PROJECT : R53
Quanta Computer Inc.
3/5VPCU(TPS51123A)
Friday, November 11, 2011



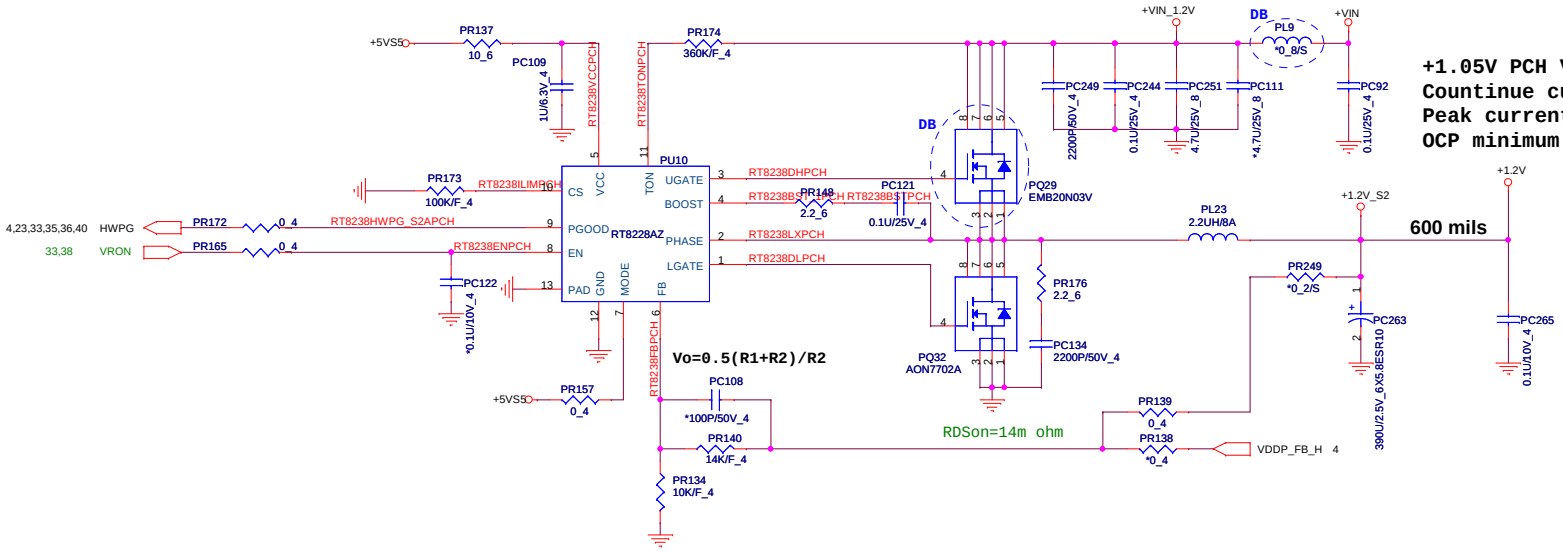
+1.1V Volt +/- 5%
Countinue current:5A
Peak current: 6.5A
OCP minimum:7.5A



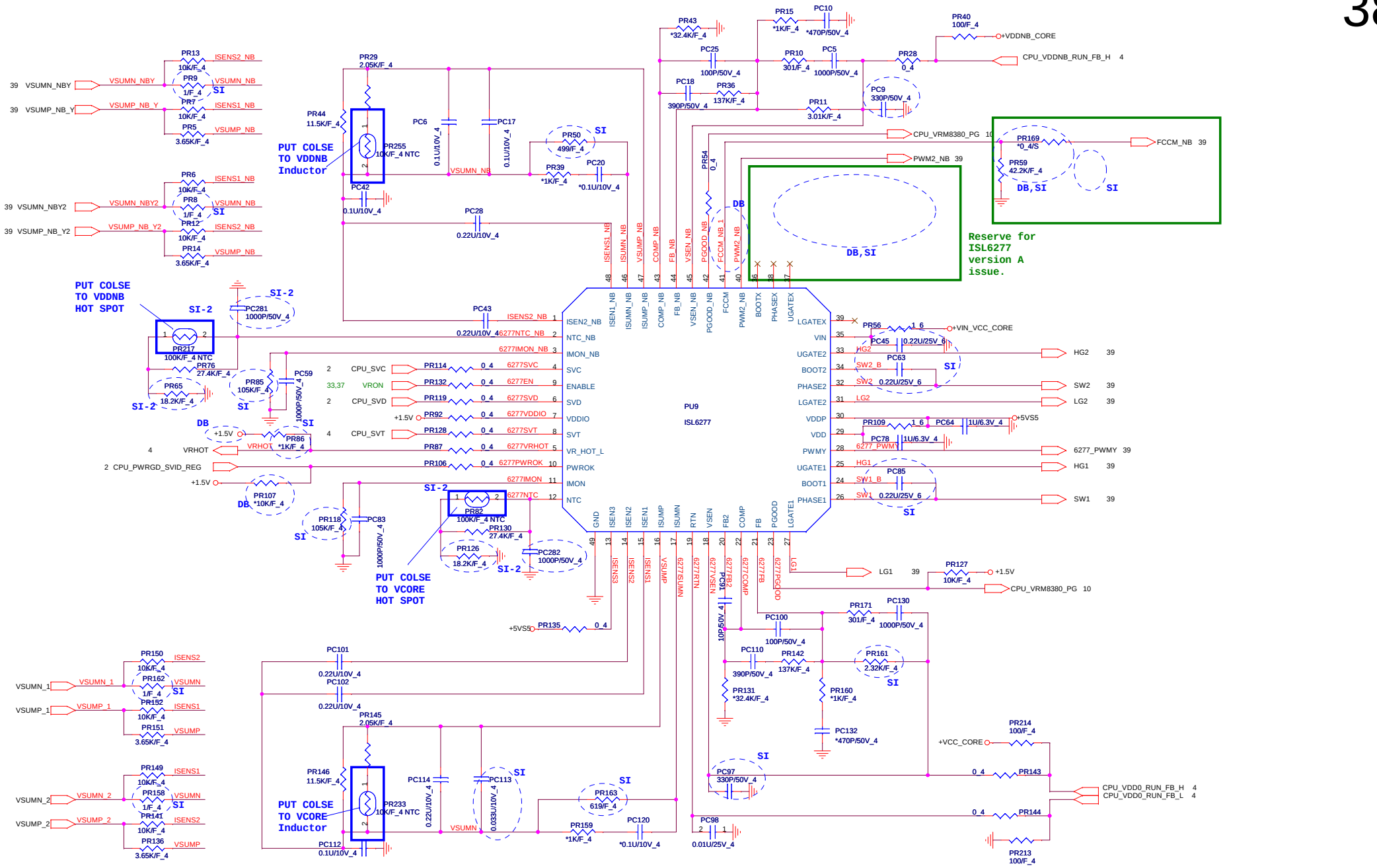
+2.5V +/- 5%
Countinue current:0.3A
Peak current:0.75A

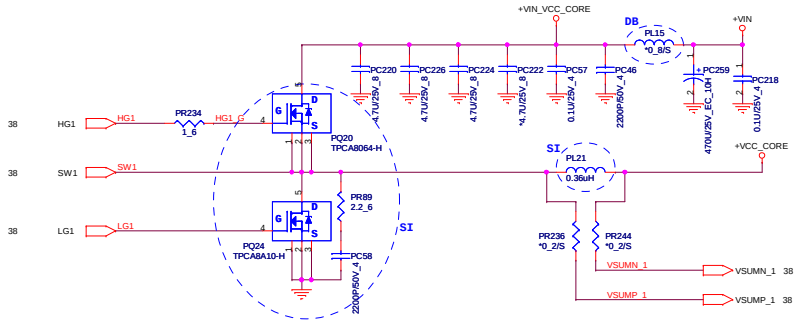
PROJECT : R53
Quanta Computer Inc.

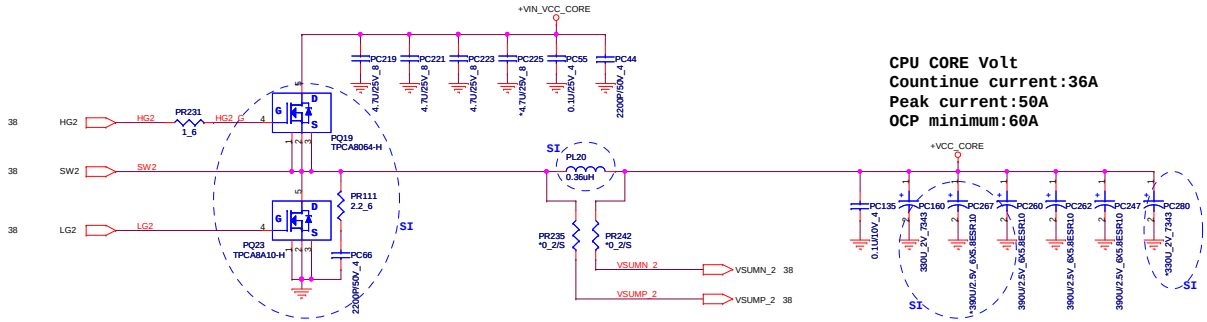
Size	Document Number	Rev
Custom	+1.1VS5 (RT8228)/2.5V	1A
Date: Friday, November 11, 2011	Sheet 36 of 44	



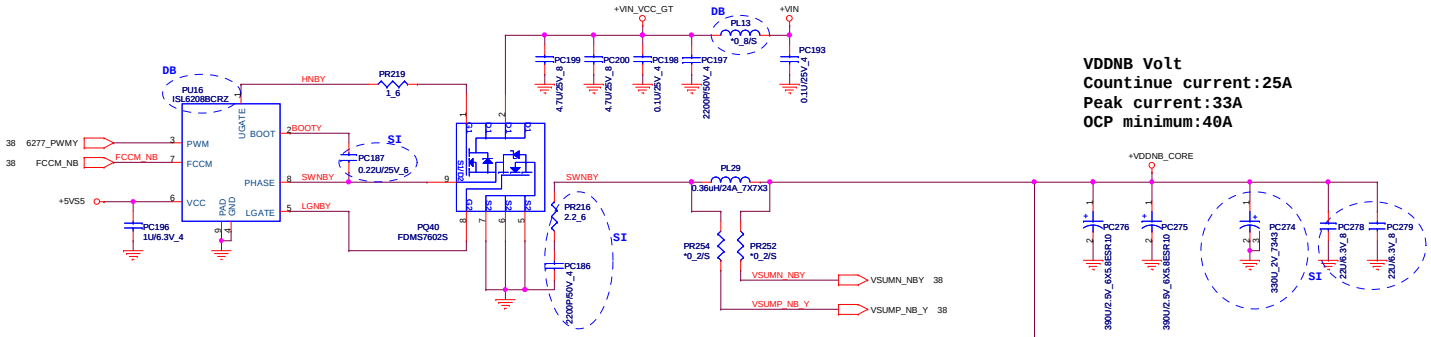
Quanta Computer Inc.	**PROJECT : R53**		
Size: Custom	Document Number: **+1.2V (RT8228)**		Rev: 1A
Date: Friday, November 11, 2011	Sheet 37 of 44		

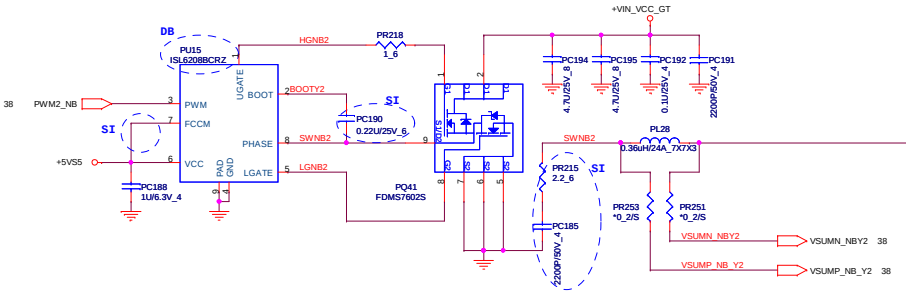

PU9
ISL6277
PUT COLSE TO VDDNB Inductor
PUT COLSE TO VDDNB HOT SPOT
PUT COLSE TO VCORE HOT SPOT
PUT COLSE TO VCORE Inductor
Reserve for ISL6277 version A issue.
DB,SI
SI
SI-2
DB
ISEN2_NB
NTC_NB
IMON_NB
SVC
ENABLE
SVD
VDDIO
SVT
VR_HOT_L
PWROK
IMON
NTC
LGATEX
VIN
UGATE2
BOOT2
PHASE2
LGATE2
VDDP
VDD
PWMY
UGATE1
BOOT1
PHASE1
GND
ISEN3
ISEN2
ISEN1
ISUMP
ISUMN
RTN
VSEN
FB2
COMP
FB
PGOOD
LGATE1
+VDDNB_CORE
+VIN_VCC_CORE
+VCC_CORE
+5VS5
+1.5V
CPU_VDDNB_RUN_FB_H
CPU_VRM8380_PG
CPU_VDD0_RUN_FB_H
CPU_VDD0_RUN_FB_L
PROJECT : R53
Quanta Computer Inc.
ISL6277
Friday, November 11, 2011





CPU CORE Volt
Countinue current:36A
Peak current:50A
OCP minimum:60A





VDDNB Volt
Countinue current:25A
Peak current:33A
OCP minimum:40A

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Size	Document Number	Rev
Custom	ISL6208	1A

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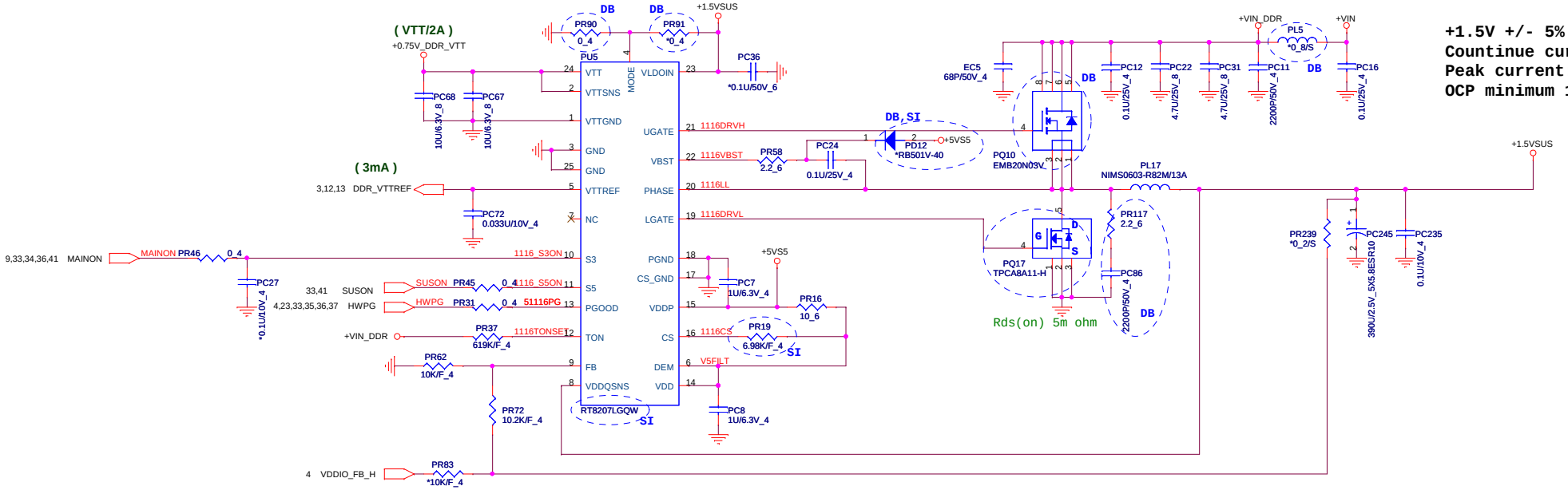

+1.5V +/- 5%
Countinue current:10A
Peak current:12A
OCP minimum 15A

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Size	Document Number	Rev
Custom	DDRIII(G5616)	1A
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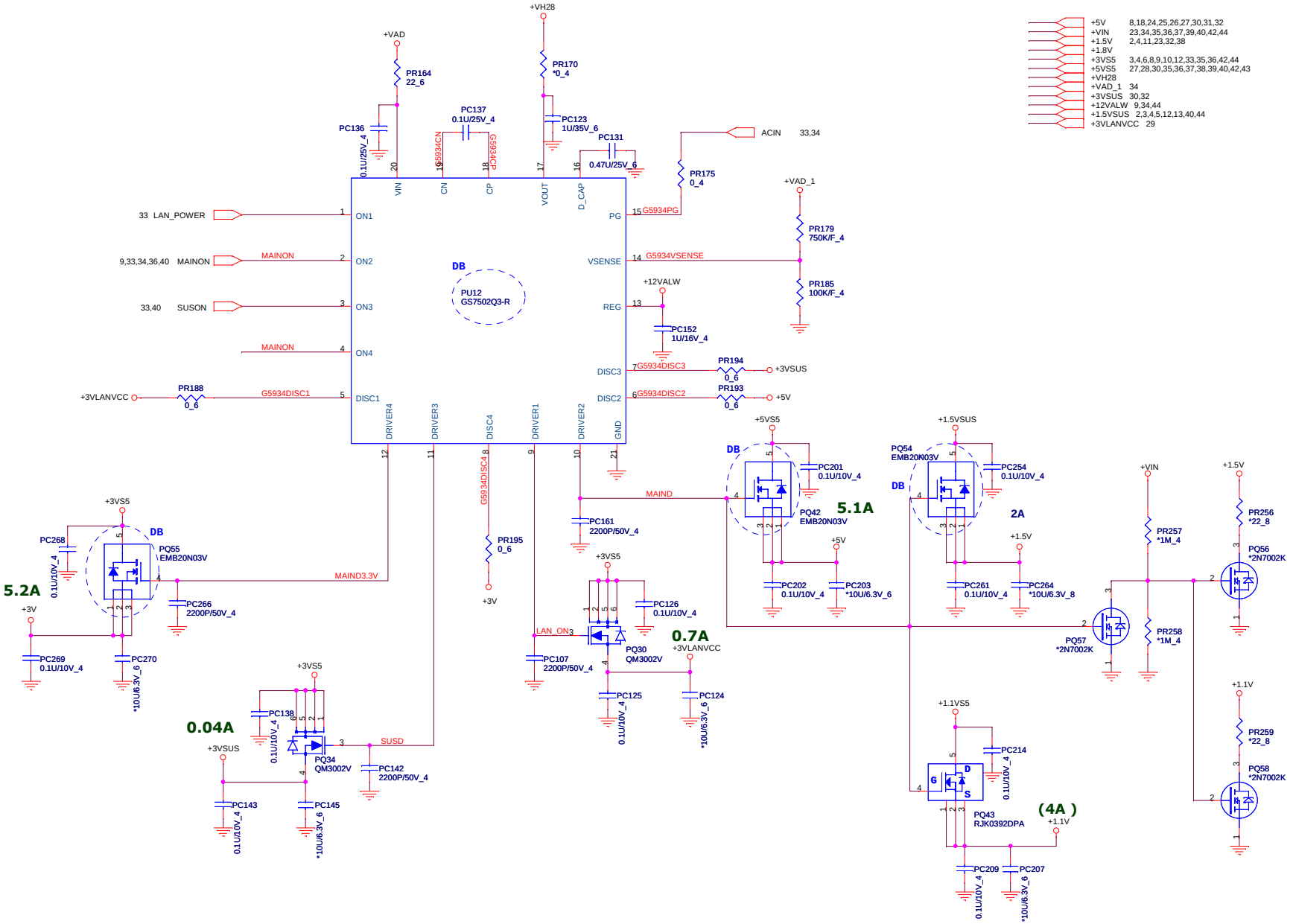

+5V	8,18,24,25,26,27,30,31,32
+VIN	23,34,35,36,37,39,40,42,44
+1.5V	2,4,11,23,32,38
+1.8V	
+3VS5	3,4,6,8,9,10,12,33,35,36,42,44
+5VS5	27,28,30,35,36,37,38,39,40,42,43
+VH28	
+VAD_1	34
+3VSUS	30,32
+12VALW	9,34,44
+1.5VSUS	2,3,4,5,12,13,40,44
+3VLANVCC	29

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Size	Document Number	Rev
Custom	Dis-charge IC (GS7502)	1A

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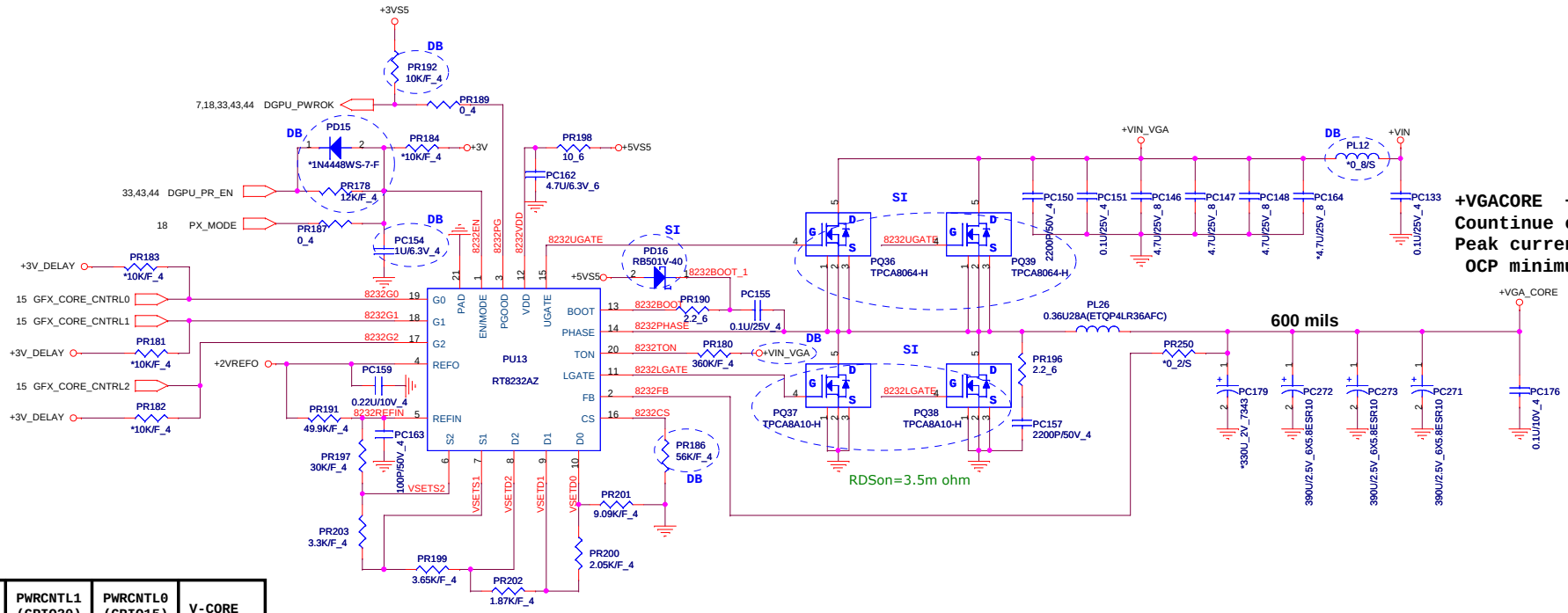
VGA Core



+VGACORE +/- 5%
Countinue current:20A
Peak current:23A
OCP minimum 33A

Symour-XT	PWRCNTL2 (GPIO16)	PWRCNTL1 (GPIO20)	PWRCNTL0 (GPIO15)	V-CORE
L	0	0	0	1.0V
M	0	0	1	0.9V
H	0	1	0	0.875V
	0	1	1	0.85V
	1	0	0	0.8V
	1	0	1	0.75V

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Size	Document Number	Rev
Custom	+VGACORE (RT8232AZ)	1A

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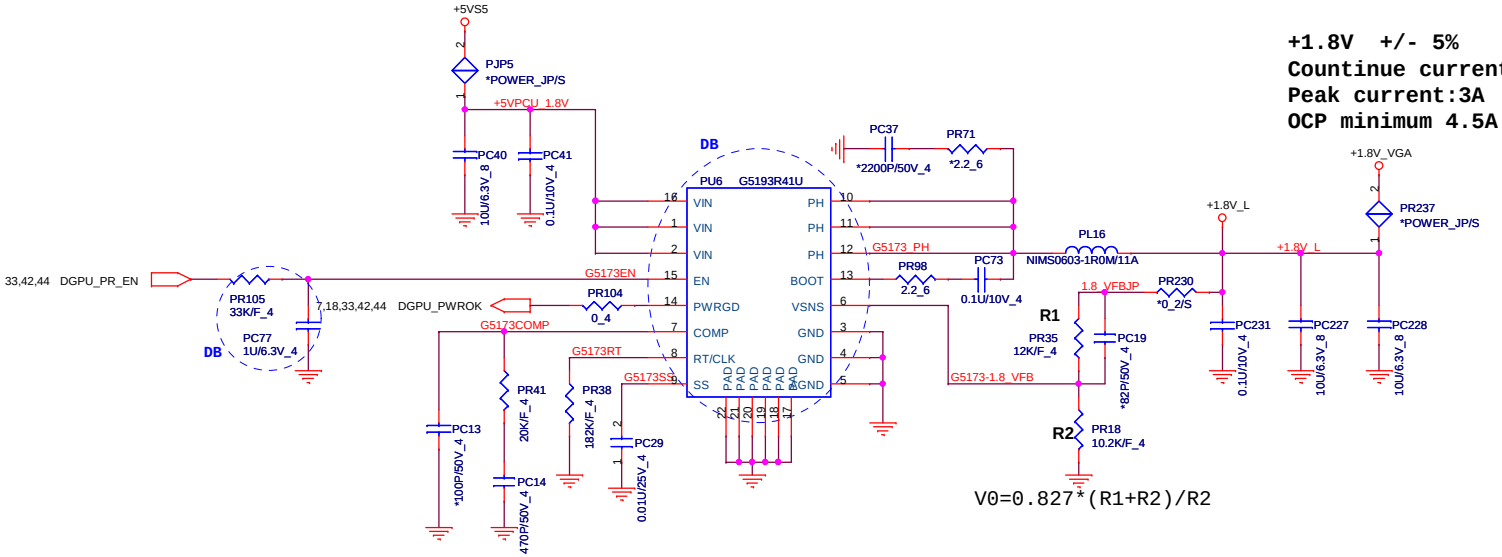
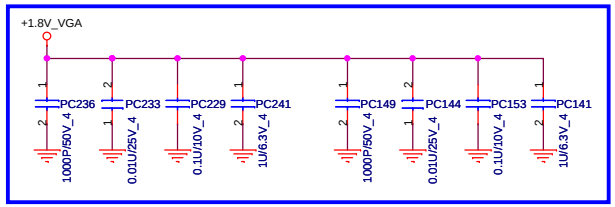


+1.8V +/- 5%
Countinue current:2A
Peak current:3A
OCP minimum 4.5A

$$V0=0.827*(R1+R2)/R2$$

DB for prevent interference



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Size	Document Number	Rev
Custom	+1.8V_VGA (G5193)	1A
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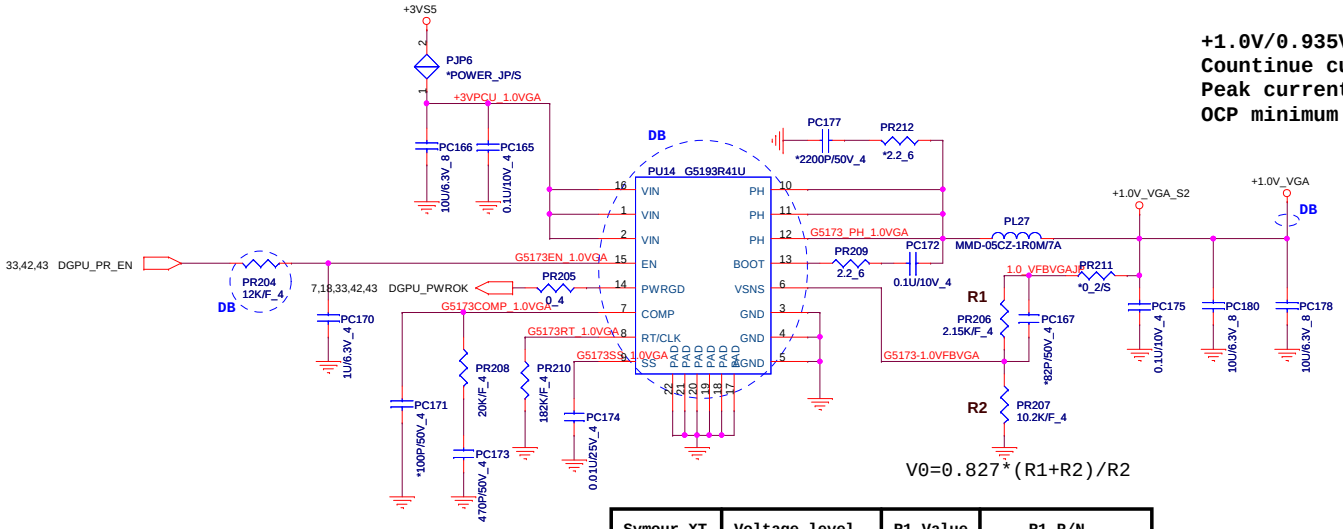
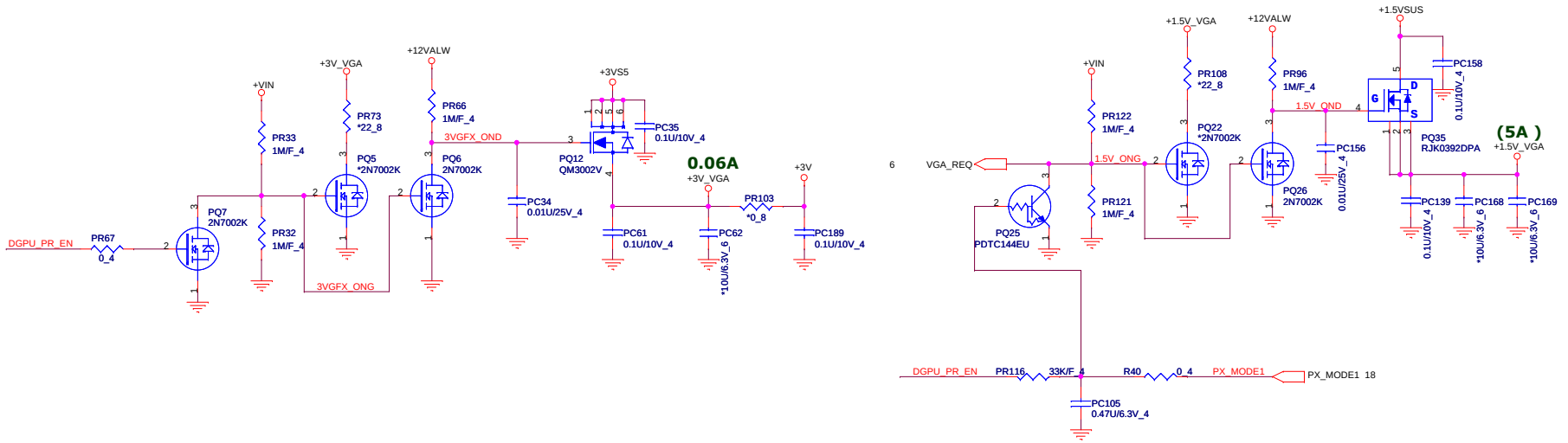


+1.0V/0.935V +/- 5%
Countinue current:2A
Peak current:3A
OCP minimum 4.5A

+3V	2,4,6,8,9,10,11,12,13,14,18,23,24,25,26,27,28,29,30,31,32,33,41,42
+VIN	23,34,35,36,37,39,40,41,42
+3VS5	3,4,6,8,9,10,12,33,35,36,41,42
+5VS5	27,28,30,35,36,37,38,39,40,41,42,43
+3V_VGA	18,30
+12VALW	9,34,41
+1.5VSUS	2,3,4,5,12,13,40,41
+1.5V_VGA	18,20,21,22

V0=0.827*(R1+R2)/R2

Symour-XT	Voltage level	R1 Value	R1 P/N
17W	1.0V	2.15K	CS22152FB07
25W	0.935V	1.37K	CS21372FB19



PROJECT : R53
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.0V_VGA (G5193)	1A

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