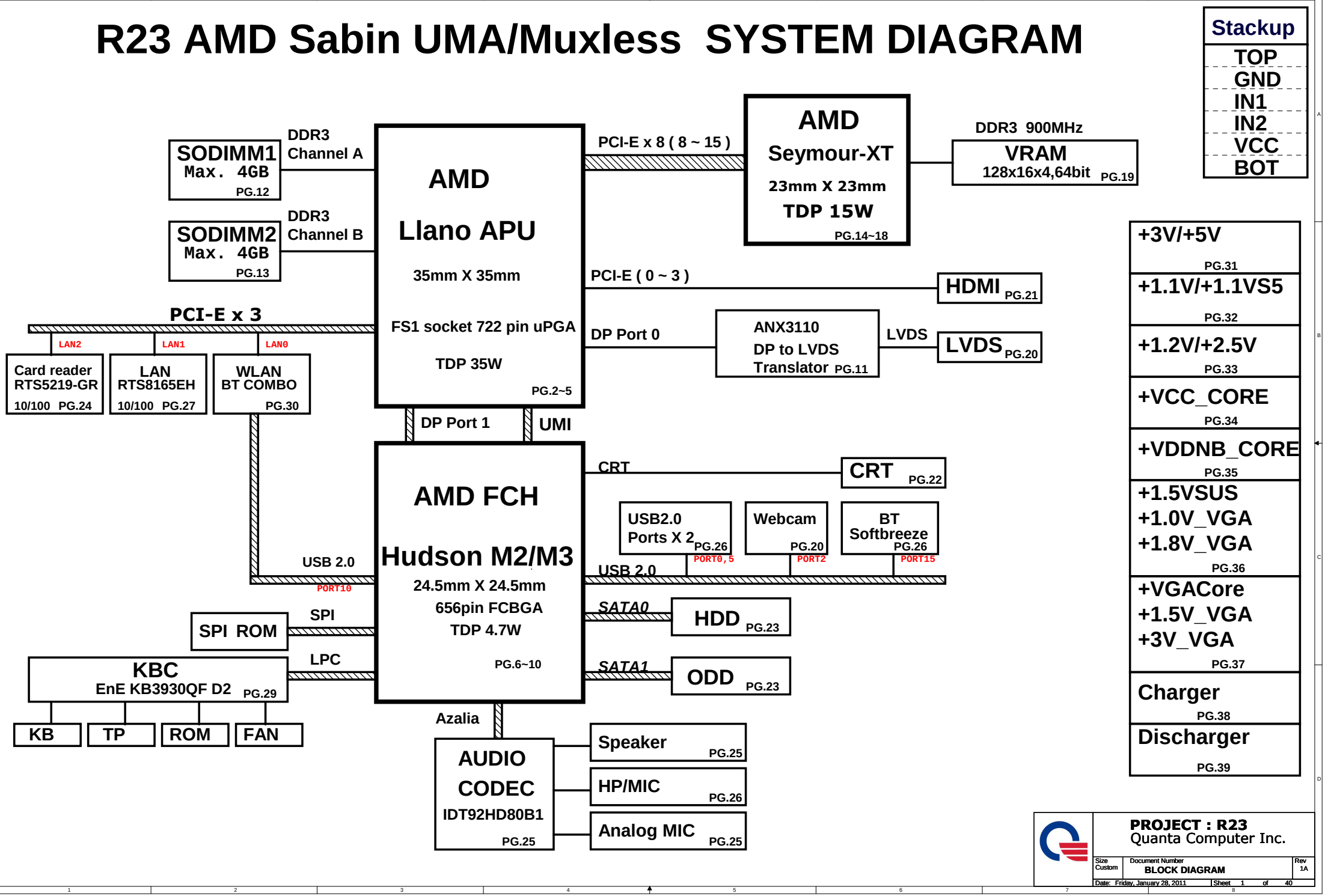
R23 AMD Sabin UMA/Muxless SYSTEM DIAGRAM



PROJECT : R23
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

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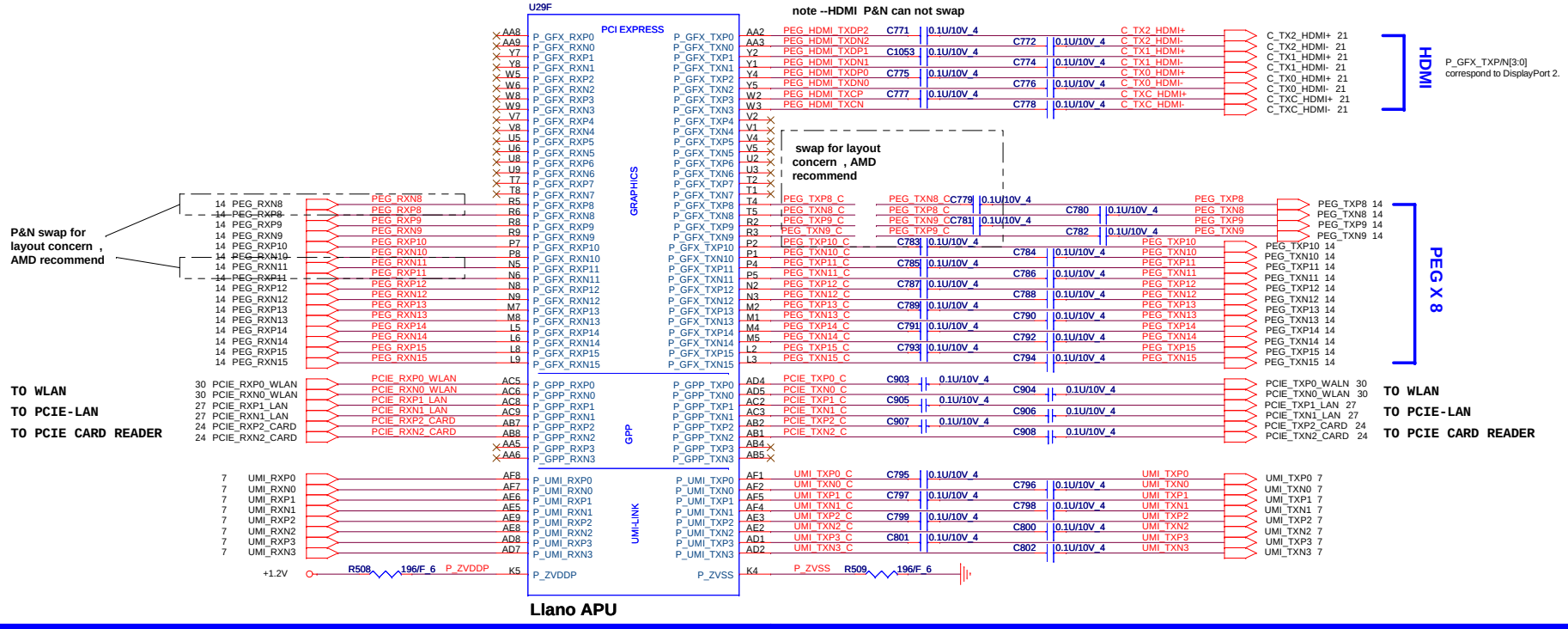
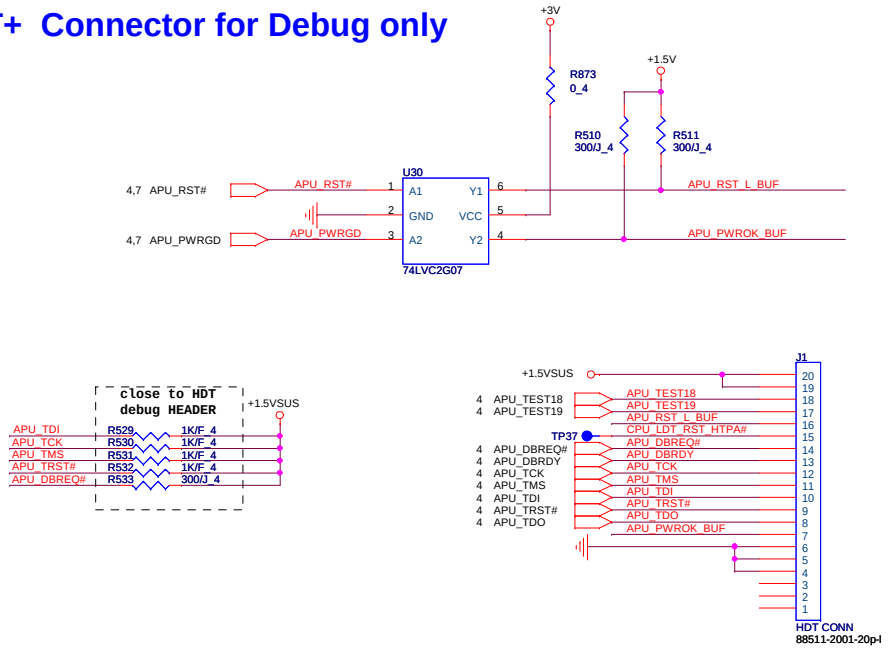


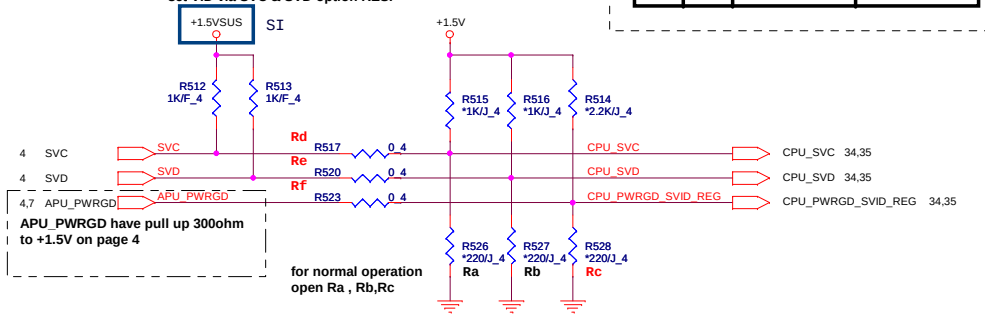
HDT+ Connector for Debug only



VID Override Circuit

	BOOT VOLTAGE	
SVC	SVD	VFIX_+VDD =VCC/GND	VFIX_+VDD =OPEN
0	0	1.1	1.1
0	1	1.0	1.2
1	0	0.9	1.0
1	1	0.8	0.8

Note:
To override VID,Remove Rd, Re, Rf, install Rc
set VID via SVC & SVD option RES.



Quanta Computer Inc.
PROJECT : R23
Size
Document Number
Llano PCIE/UMI/GPP
Rev 1A
Date: Friday, January 28, 2011
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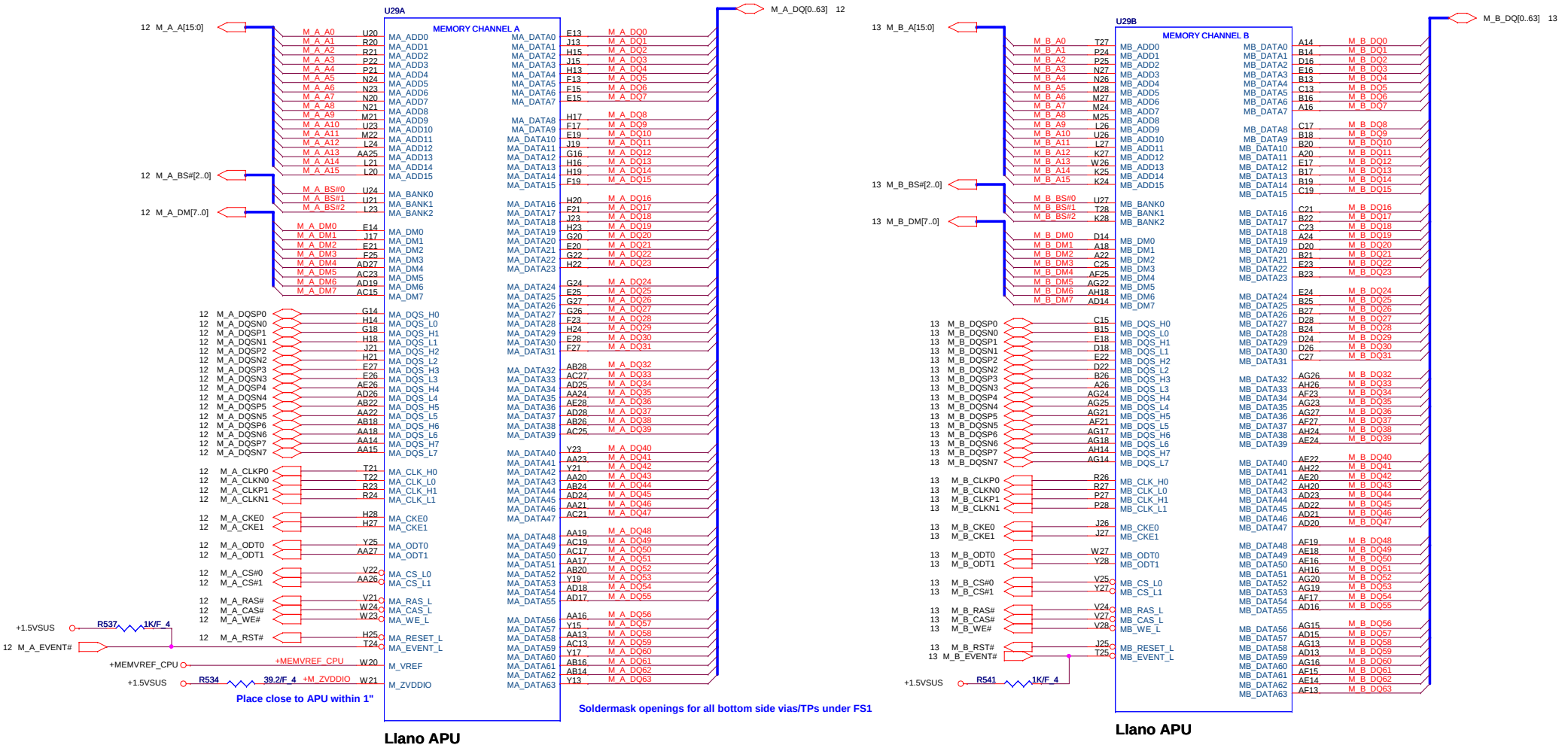

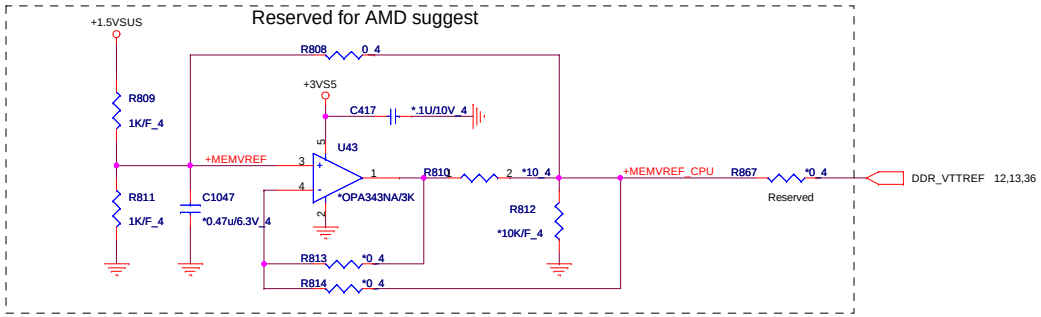

Quanta Computer Inc.			
PROJECT : R23			
Size	Document Number		Rev
	Llano DDR3 MEM I/F		1A
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Place caps with APU < 1 inch
route PCIE as 85ohm +/- 10%

DP0 output to
eDP to LVDS converter

Display port power 1.5V min 1.2v max : 1.65v

DP1 output to Hudson-M2
for VGA translator interface

Note: CLK_APU_HCLKP/N is 100MHZ SSC

Note: CLK_DP_NSSCP/N is 100MHZ non-SSC

U29C

ANALOG/DISPLAY/MISC

DISPLAY PORT 0 | DISPLAY PORT 1 | DISPLAY PORT MISC. | CLK | SER. | CTRL | JTAG | RSVD | SENSE | TEST

LVDS

VGA

HDMI

Display port power 1.5V min 1.2v max : 1.65v

DMAACTIVE_L controls
entry and exit from the
sleep and power states

To AMD HDT

AMD internal test only

FS1R1 signals is for detect CPU TYPE and protect it.
FS1R1 CPU this pin is N.C
FS1R2 CPU this pin is LOW
can remove it at MP

Llano APU

Thermal

THERMTRIP# shutdown temperature 125度C

APU_PROCHOT# 可以當 input or output
當Low 時CPU 會降 P - STATE

to EC reserve only

ADD VGA TEMP_ FAIL function is active Hi

over 120 degree C= Low

When 100K-NTC 100 C=6.164K
Thermal Trip = 120 C

TEST35 PU FOR INTERNAL
TEST35 PD FOR CUSTOMER

M_TEST CONNECTION TBD

SI

Quanta Computer Inc.	
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APU POWER TABLE

PIN NAME	NET NAME	VOLTAGE
VDD	+VCC_CORE	+1.1V
VDDNB	+VDDNB_CORE	??
VDDIO	+1.5VSUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V

SI EMI

+VCC_CORE
C388 *470P/50V_4
C383 *470P/50V_4
C371 *470P/50V_4

U29D — Llano APU

+VCC_CORE
C830 22U/6.3VS_8
C831 22U/6.3VS_8
C832 22U/6.3VS_8
C833 22U/6.3VS_8
C834 0.22U/6.3V_4
C845 0.22U/6.3V_4
C842 0.22U/6.3V_4
C843 180P/50V_4
C844 180P/50V_4

18A
Maximum IDDNBspike 22.5A

+VDDNB_CORE
C851 0.22U/6.3V_4
C852 0.22U/6.3V_4
C853 0.22U/6.3V_4
C854 0.22U/6.3V_4
C855 180P/50V_4
C856 180P/50V_4
4A Up to DDR3-1333 @ 1.50V VDDIO
+1.5VSUS
EMI reserve

VDDP_A + VDDP_B = 3.5A
1.75A
+1.2V
R591 *0_8/S
+1.2V_VDDP_A
C864 10U/6.3V_8
C867 0.22U/6.3V_4
C869 180P/50V_4

1.5A
R592 *0_8/S
+1.2V_VDDR_A
C871 1000P/50V_4
C872 1000P/50V_4
C875 0.22U/6.3V_4
C876 0.22U/6.3V_4
C883 4.7U/6.3V_6
C884 4.7U/6.3V_6
C887 180P/50V_4
C888 180P/50V_4

VDDA= 0.75A
+2.5V
L62 BLM21PG221SN1D(220,100M,2A)_8
+2.5V_VDDA
C879 4.7U/6.3V_6
C880 0.22U/6.3V_4
C881 3300P/50V_4

36A
Maximum IDDspike 50A
C823 22U/6.3VS_8
C824 22U/6.3VS_8
C825 22U/6.3VS_8
C826 22U/6.3VS_8
C827 22U/6.3VS_8
C828 22U/6.3VS_8
C829 22U/6.3VS_8
C835 0.22U/6.3V_4
C836 0.22U/6.3V_4
C837 180P/50V_4
C838 180P/50V_4
C839 0.01U/25V_4
C840 0.01U/25V_4
C841 0.01U/25V_4

DECOUPLING between PROCESSOR and DIMMs
Across VDDIO and VSS split
+1.5VSUS
C846 0.22U/6.3V_4
C847 0.22U/6.3V_4
C848 180P/50V_4
C849 180P/50V_4

+1.5VSUS
C857 22U/6.3VS_8
C858 22U/6.3VS_8
C859 4.7U/6.3V_6
C860 4.7U/6.3V_6
C861 4.7U/6.3V_6
C862 4.7U/6.3V_6
C863 0.22U/6.3V_4

If the VSS plane is cut to create a VDDIO plane,
ceramic capacitors are connected across
the VDDIO and VSS plane split as follows

1.75A
+1.2V_VDDP_B
R824 *0_8/S
+1.2V
C865 10U/6.3V_8
C866 10U/6.3V_8
C868 0.22U/6.3V_4
C870 180P/50V_4

1.5A
+1.2V_VDDR_B
R825 *0_8/S
+1.2V
C873 1000P/50V_4
C874 1000P/50V_4
C877 0.22U/6.3V_4
C878 0.22U/6.3V_4
C885 4.7U/6.3V_6
C886 4.7U/6.3V_6
C889 180P/50V_4
C890 180P/50V_4

VDDR = 3A (Up to DDR3-1333 @ 1.5V)

U29E — Llano APU

Quanta Computer Inc.
PROJECT : R23

Size	Document Number	Rev
	Llano POWER/GND	1A

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NC,no install by default

+3VS5
R594 *2.2K/J_4 FCH_TEST0
R596 *2.2K/J_4 FCH_TEST1
R598 *2.2K/J_4 FCH_TEST2

remove PCIE_RST2# from AMD recommend

+3V
R602 2.2K_4 CGCLK_SMB
R603 2.2K_4 CGDAT_SMB
R604 *1K/J_4
J2 1 2 SYS_RST#
*SOLDERJUMPER-2
to DDR3 SMBUS
SYS_RST# internal 10K pull up

GEVENT0# internal pull Hi 8.2K to +3V
GEVENT1# internal pull Hi 8.2K to +3V
GEVENT23# internal pull Hi 8.2K to +3V
GEVENT5# internal pull Hi 8.2K to +3VS5
PCIE_WAKE# no need to pull Hi resistor from check list

CLK_REQ2# internal pull Hi 8.2K to +3V
CLK_REQ3# internal pull Hi 8.2K to +3V
CLK_REQ4# internal pull Hi 8.2K to +3V

+3VS5
R856 10K/F_4 SCL3
R857 10K/F_4 SDA3
R611 10K/F_4 SCL2
R613 10K/F_4 SDA2
R614 10K/F_4 SCL1
R616 10K/F_4 SDA1
R618 *4.7K/J_4 FCH_THERMTRIP#
C1073 *0.01U/25V_4
R629 10K/F_4 DNBSWON#

This pin is used to power down VGA DAC regulators when CRT no connected

GEVENT16# internal pull Hi 8.2K to +3VS5
GEVENT15# internal pull Hi 8.2K to +3VS5

To Azalia

ACZ_SDOUT_R R635 33/J_4 ACZ_SDOUT_AUDIO 25
ACZ_SYNC_R R636 33/J_4 ACZ_SYNC_AUDIO 25
ACZ_BCLK_R R637 33/J_4 BIT_CLK_AUDIO 25
ACZ_RST#_R R638 33/J_4 ACZ_RST#_AUDIO 25
ACZ_SDIN0 ACZ_SDIN0 25

Pure UMA can remove
CLK_REQ# already internal pull up 8.2K
37 VGA_REQ 1 2 CLKREQ1#
D26 RB501V-40

29 SUSB# SUSB#
29 SUSC# SUSC#
29 DNBSWON# DNBSWON#
10 FCH_PWRGD FCH_PWRGD
TP153 PCIE_RST2#
TP154 RI#
FCH_TEST0 FCH_TEST1 FCH_TEST2
29 EC_A20GATE EC_A20GATE
29 EC_RCIN# EC_RCIN#
TP155 FCH_PME#
29 SIO_EXT_SMI# SIO_EXT_SMI#
29 SIO_EXT_SCI# R829 0_4 GEVENT5#
SYS_RST#
27,30 PCIE_WAKE# PCIE_WAKE#
C1075 *100P/50V_4
4 FCH_THERMTRIP# FCH_THERMTRIP#
+3V R607 10K/F_4 WD_PWRGD
SI
29 RSMRST# RSMRST#
24 PCIE_CARD_CLKREQ# PCIE_CARD_CLKREQ#
27 PCIE_LAN_CLKREQ# PCIE_LAN_CLKREQ#
27,29 LAN_DISABLE# R868 *0/J_4 LAN_DISABLE#_FCH
25 ACZ_SPKR R612 0_4 FCH_GPIO66
12,13 CGCLK_SMB CGCLK_SMB
12,13 CGDAT_SMB CGDAT_SMB
SCL1
SDA1
30 PCIE_MINI_CLKREQ# PCIE_MINI_CLKREQ#
CLKREQ1#
LLB Not Implemented ,left unconnected.
LLB#
9 VGA_POWER_DOWN R619 0_4 SMARTVOLT2
TP160 VGA_PD
TP161 GBE_LED0
24 CARD_EECS R904 0_4
SI
TP163
TP165
TP167 GEVENT17#
23 ODD_DA#_FCH ODD_DA#_FCH
23 ODD_PLUGIN# ODD_PLUGIN#
TP168 FCH_JTAG_TCK
TP169 FCH_JTAG_TDI
TP170 FCH_JTAG_RST#
For Zero ODD

HD audio interface is +3V_S5 voltage
R630 *10K/F_4 ACZ_BCLK_R
ACZ_SDOUT_R
R631 *10K/F_4 ACZ_SDIN0
R632 *10K/F_4 ACZ_SDIN1
R633 *10K/F_4 ACZ_SDIN2_R
R634 *10K/F_4 ACZ_SDIN3_R
ACZ_SYNC_R
ACZ_RST#_R
TP171
TP172

HUDSON-M3
Part 4 of 5

PCIE_RST2#/GEVENT4#
RI#/GEVENT22#
SPI_CS3#/GBE_STAT1/GEVENT21#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
TEST0
TEST1/TMS
TEST2
GA20IN/GEVENT0#
KBRST#/GEVENT1#
PME#/GEVENT3#
LPC_SMI#/GEVENT23#
LPC_PD#/GEVENT5#
SYS_RESET#/GEVENT19#
WAKE#/GEVENT8#
IR_RX1/GEVENT20#
THRMTRIP#/SMBALERT#/GEVENT2#
WD_PWRGD
RSMRST#
ACPI / WAKE UP EVENTS
CLK_REQ4#/SATA_IS0#/GPIO64
CLK_REQ3#/SATA_IS1#/GPIO63
SMARTVOLT1/SATA_IS2#/GPIO50
CLK_REQ0#/SATA_IS3#/GPIO60
SATA_IS4#/FANOUT3/GPIO55
SATA_IS5#/FANIN3/GPIO59
SPKR/GPIO66
SCL0/GPIO43
SDA0/GPIO47
SCL1/GPIO227
SDA1/GPIO228
CLK_REQ2#/FANIN4/GPIO62
CLK_REQ1#/FANOUT4/GPIO61
IR_LED#/LLB#/GPIO184
SMARTVOLT2/SHUTDOWN#/GPIO51
DDR3_RST#/GEVENT7#/VGA_PD
GBE_LED0/GPIO183
SPI_HOLD#/GBE_LED1/GEVENT9#
GBE_LED2/GEVENT10#
GBE_STAT0/GEVENT11#
CLK_REQG#/GPIO65/OSCIN/IDLEEXIT#
GPIO
BLINK/USB_OC7#/GEVENT18#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GEVENT17#
USB_OC4#/IR_RX0/GEVENT16#
USB_OC3#/AC_PRES/TDO/GEVENT15#
USB_OC2#/TCK/GEVENT14#
USB_OC1#/TDI/GEVENT13#
USB_OC0#/SPI_TPM_CS#/TRST#/GEVENT12#
USB OC
AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO167
AZ_SDIN1/GPIO168
AZ_SDIN2/GPIO169
AZ_SDIN3/GPIO170
AZ_SYNC
AZ_RST#
HD AUDIO
PS2_DAT/SDA4/GPIO187
PS2_CLK/CEC/SCL4/GPIO188
SPI_CS2#/GBE_STAT2/GPIO166
PS2KB_DAT/GPIO189
PS2KB_CLK/GPIO190
PS2M_DAT/GPIO191
PS2M_CLK/GPIO192
KSO_0/GPIO209
KSO_1/GPIO210
KSO_2/GPIO211
KSO_3/GPIO212
KSO_4/GPIO213
KSO_5/GPIO214
KSO_6/GPIO215
KSO_7/GPIO216
KSO_8/GPIO217
KSO_9/GPIO218
KSO_10/GPIO219
KSO_11/GPIO220
KSO_12/GPIO221
KSO_13/GPIO222
KSO_14/XDB0/GPIO223
KSO_15/XDB1/GPIO224
KSO_16/XDB2/GPIO225
KSO_17/XDB3/GPIO226
EMBEDDED CTRL
USBCLK/14M_25M_48M_OSC
USB_RCOMP
USB_FSD1P/GPIO186
USB_FSD1N
USB_FSD0P/GPIO185
USB_FSD0N
USB MISC
USB 1.1
USB_HSD13P
USB_HSD13N
USB_HSD12P
USB_HSD12N
USB_HSD11P
USB_HSD11N
USB_HSD10P
USB_HSD10N
USB_HSD9P
USB_HSD9N
USB_HSD8P
USB_HSD8N
USB_HSD7P
USB_HSD7N
USB_HSD6P
USB_HSD6N
USB_HSD5P
USB_HSD5N
USB_HSD4P
USB_HSD4N
USB_HSD3P
USB_HSD3N
USB_HSD2P
USB_HSD2N
USB_HSD1P
USB_HSD1N
USB_HSD0P
USB_HSD0N
USB 2.0
USBSS_CALRP
USBSS_CALRN
USB_SS_TX3P
USB_SS_TX3N
USB_SS_RX3P
USB_SS_RX3N
USB_SS_TX2P
USB_SS_TX2N
USB_SS_RX2P
USB_SS_RX2N
USB_SS_TX1P
USB_SS_TX1N
USB_SS_RX1P
USB_SS_RX1N
USB_SS_TX0P
USB_SS_TX0N
USB_SS_RX0P
USB_SS_RX0N
USB 3.0
SCL2/GPIO193
SDA2/GPIO194
SCL3_LV/GPIO195
SDA3_LV/GPIO196
EC_PWM0/EC_TIMER0/GPIO197
EC_PWM1/EC_TIMER1/GPIO198
EC_PWM2/EC_TIMER2/WOL_EN/GPIO199
EC_PWM3/EC_TIMER3/GPIO200
KSI_0/GPIO201
KSI_1/GPIO202
KSI_2/GPIO203
KSI_3/GPIO204
KSI_4/GPIO205
KSI_5/GPIO206
KSI_6/GPIO207
KSI_7/GPIO208
Hudson-M2

USB_RCOMP_SB R597 11.8K/F_6
USBP15+ 26 USBP15- 26 BLUETOOTH
USBP11+ TP156 USBP11- TP157
USBP10+ 30 USBP10- 30 WLAN Min-Card
USBP7+ TP158 USBP7- TP159
USBP6+ 26 USBP6- 26 USB Connector
USBP5+ 26 USBP5- 26 USB Connector
USBP2+ 20 USBP2- 20 Carama USB
USBP1+ TP164 USBP1- TP166
USBP0+ 26 USBP0- 26 USB Connector
USBSS_CALRP TP151 USBSS_CALRN TP152
USB 3.0 Not Implemented: left unconnected.

SCL2 SDA2 SCL3 SDA3
EC_PWM2 EC_PWM2 10
No need for GPIO200

SCL3 of a TSI-capable APU's thermal bus,Pulled up to APU_VDDIO. Resistor value verified in the relevant APU design guide.

Quanta Computer Inc.
PROJECT : R23
Size | Document Number: Hudson-M3 GPIO/USB/AZ/RGMII | Rev: 1A
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HUDSON-M3

Part 1 of 5

U32E

Place these PICE AC coupling cap close to FCH

Note: CLK_FCH_SRCP/N is 100MHZ SSC

Note: CLK_PCIE_TRAVISP/N is 100MHZ non-SSC

Note: CLK_DP_NSSCP/N is 100MHZ non-SSC

Note: CLK_APU_HCLKP/N is 100MHZ SSC

Note: CLK_PCIE_VGAP/N is 100MHZ SSC

Note: GPP_CLK(0:8)P/N is 100MHZ SSC capable

FCH PROCHOT#--- (input 0.8V threshold) When it isasserted, it can generate SCI or SMI to OS/BIOS

LDT_STP# let is NC from schematic recommend

S5_CORE_EN is necessary to connect enable pin of +3VPCU/+5VPCU regulator for S5+ mode implementation

INTRUDER_ALERT# Left not connected (FCH has 50-kohm internal pull-up to VBAT).

USE GROUND GUARD FOR 32K_X1 AND 32K_X2

Hudson-M2

Quanta Computer Inc. PROJECT : R23			
Size	Document Number: Hudson-M3 ACPI/PCI/CLOCK		Rev: 1A
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U32D

HUDSON-M3

Part 5 of 5

GROUND

VSS_1 VSS_2 VSS_3 VSS_4 VSS_5 VSS_6 VSS_7 VSS_8 VSS_9 VSS_10 VSS_11 VSS_12 VSS_13 VSS_14 VSS_15 VSS_16 VSS_17 VSS_18 VSS_19 VSS_20 VSS_21 VSS_22 VSS_23 VSS_24 VSS_25 VSS_26 VSS_27 VSS_28 VSS_29 VSS_30 VSS_31 VSS_32 VSS_33 VSS_34 VSS_35 VSS_36 VSS_37 VSS_38 VSS_39 VSS_40 VSS_41 VSS_42 VSS_43 VSS_44 VSS_45 VSS_46 VSS_47 VSS_48 VSS_49 VSS_50 VSS_51 VSS_52 VSS_53 VSS_54 VSS_55 VSS_56 VSS_57 VSS_58 VSS_59 VSS_60 VSS_61 VSS_62 VSS_63 VSS_64

VSSAN_HWM

VSSXL

VSSPL_SYS

VSS_65 VSS_66 VSS_67 VSS_68 VSS_69 VSS_70 VSS_71 VSS_72 VSS_73 VSS_74 VSS_75 VSS_76 VSS_77 VSS_78 VSS_79 VSS_80 VSS_81 VSS_82 VSS_83 VSS_84 VSS_85 VSS_86 VSS_87 VSS_88 VSS_89 VSS_90 VSS_91 VSS_92 VSS_93 VSS_94 VSS_95 VSS_96 VSS_97 VSS_98 VSS_99 VSS_100 VSS_101 VSS_102 VSS_103 VSS_104 VSS_105 VSS_106 VSS_107 VSS_108 VSS_109 VSS_110 VSS_111 VSS_112 VSS_113 VSS_114 VSS_115 VSS_116 VSS_117 VSS_118 VSS_119 VSS_120 VSS_121 VSS_122 VSS_123 VSS_124 VSS_125 VSS_126 VSS_127 VSS_128

VSSPL_DAC VSSAN_DAC VSSANQ_DAC VSSIO_DAC

EFUSE

Hudson-M2

PLACE SATA AC COUPLING
CAPS CLOSE TO HUDSON-M2/M3

SATA HDD

SATA ODD

SATA_TXP0 SATA_TXN0 SATA_RXP0 SATA_RXN0 SATA_TXP1 SATA_TXN1 SATA_RXP1 SATA_RXN1

SATA_TX0P SATA_TX0N SATA_RX0N SATA_RX0P SATA_TX1P SATA_TX1N SATA_RX1N SATA_RX1P SATA_TX2P SATA_TX2N SATA_RX2N SATA_RX2P SATA_TX3P SATA_TX3N SATA_RX3N SATA_RX3P SATA_TX4P SATA_TX4N SATA_RX4N SATA_RX4P SATA_TX5P SATA_TX5N SATA_RX5N SATA_RX5P

U36 TC7SH08FU

+3V C921 0.1U/10V_4

SATA_LED# SB_SATA_LED#

PLACE SATA_CAL RES VERY CLOSE TO BALL OF HUDSON-M2/M3

+1.1V_AVDD_SATA R682 1K/F_4 R683 1K/F_4 SATA_CALRP SATA_CALRN

+3V R685 10K/F_4 SB_SATA_LED# SATA_ACT#/GPIO67

SATA_X1 SATA_X2

Integrated Clock Mode:
Leave unconnected.

NC6 NC7 NC8 NC9 NC10 NC11 NC12 NC13

GPIO52 internal pull Hi 8.2K to +3V
GPIO53 internal pull Hi 8.2K to +3V
GPIO54 internal pull Hi 8.2K to +3V
GPIO56 internal pull Hi 8.2K to +3V
GPIO57 internal pull Hi 8.2K to +3V
GPIO58 internal pull Hi 8.2K to +3V

RF_OFF# BT_OFF# BT_COMBO_EN# ODD_PWR BT_COMBO_OFF# LCD_BK

FANOUT0/GPIO52 FANOUT1/GPIO53 FANOUT2/GPIO54 FANIN0/GPIO56 FANIN1/GPIO57 FANIN2/GPIO58

TEMPIN0 TEMPIN1 TEMPIN2 TEMPIN3

TEMPIN0/GPIO171 TEMPIN1/GPIO172 TEMPIN2/GPIO173 TEMPIN3/TALERT#/GPIO174

R693 10K/F_4 R694 10K/F_4 R695 10K/F_4 R696 10K/F_4

TEMP(0 - 3)
Temp Monitor Not Implemented
10-KΩ 5% pull-up to +3VS5
or 10-KΩ 5% pull-down

U32B

HUDSON-M3

Part 2 of 5

SERIAL ATA

SD CARD

SD_CLK/SCLK_2/GPIO73 SD_CMD/SLOAD_2/GPIO74 SD_CD#/GPIO75 SD_WP/GPIO76 SD_DATA0/SDATI_2/GPIO77 SD_DATA1/SDATO_2/GPIO78 SD_DATA2/GPIO79 SD_DATA3/GPIO80

GBE LAN

GBE_COL GBE_CRS GBE_MDCK GBE_MDIO GBE_RXCLK GBE_RXD3 GBE_RXD2 GBE_RXD1 GBE_RXD0 GBE_RXCTL/RXDV GBE_RXERR GBE_TXCLK GBE_TXD3 GBE_TXD2 GBE_TXD1 GBE_TXD0 GBE_TXCTL/TXEN GBE_PHY_PD GBE_PHY_RST# GBE_PHY_INTR

GBE_COL R668 10K/F_4 GBE_CRS R670 10K/F_4 GBE_MDIO R672 10K/F_4 +3VS5

follow AMD check list to pull UP / LOW

GBE_RXERR R674 10K/F_4

GBE_PHY_INTR R675 10K/F_4 +3VS5

SPI ROM

SPI_DI/GPIO164 SPI_DO/GPIO163 SPI_CLK/GPIO162 SPI_CS1#/GPIO165 ROM_RST#/SPI_WP#/GPIO161

FCH_SPI_SI FCH_SPI_SO FCH_SPI_CLK FCH_SPI_CS0# FCH_SPI_WP

TP188 TP189 TP190 TP191 TP192

FCH_SPI_CS0# R878 *0_4 SPI_CS0# FCH_SPI_CLK R879 *0_4 SPI_CLK FCH_SPI_SO R880 *0_4 SPI_SO FCH_SPI_SI R881 *0_4 SPI_SI

SPI_WP 7,29 SPI_WP

*MX25L1605DM2I-12G

VGA DAC

VGA_RED L30 FCH_CRT_R R676 *0_4/S FCH_CRT_RED 22

VGA_GREEN L32 FCH_CRT_G R678 *0_4/S FCH_CRT_GRE 22

VGA_BLUE M29 FCH_CRT_B R680 *0_4/S FCH_CRT_BLU 22

VGA_HSYNC/GPO68 FCH_CRT_HSYNC 22
VGA_VSYNC/GPO69 FCH_CRT_VSYNC 22

VGA_DDC_SDA/GPO70 FCH_DDCDAT 22
VGA_DDC_SCL/GPO71 FCH_DDCCLK 22

VGA_DAC_RSET K31 VGA_DAC_REST R684 715/F_4

R place close to PCH

FCH_CRT_R R677 150/F_4
FCH_CRT_G R679 150/F_4
FCH_CRT_B R681 150/F_4

VGA MAINLINK

AUX_VGA_CH_P V28 APU_DP_AUXP 4
AUX_VGA_CH_N V29 APU_DP_AUXN 4

AUXCAL U28 AUXCAL R686 100/F_4 +FCH_VDDAN_11_MLDAC

ML_VGA_L0P T31 APU_DP_TXP0 4
ML_VGA_L0N T33 APU_DP_TXN0 4
ML_VGA_L1P T29 APU_DP_TXP1 4
ML_VGA_L1N T28 APU_DP_TXN1 4
ML_VGA_L2P R32 APU_DP_TXP2 4
ML_VGA_L2N R30 APU_DP_TXN2 4
ML_VGA_L3P P29 APU_DP_TXP3 4
ML_VGA_L3N P28 APU_DP_TXN3 4

ML_VGA_HPD/GPO229 C29 VGA_HPD R687 10K/F_4 +3V

HW MONITOR

VIN0/GPIO175 VIN1/GPIO176 VIN2/SDATI_1/GPIO177 VIN3/SDATO_1/GPIO178 VIN4/SLOAD_1/GPIO179 VIN5/SCLK_1/GPIO180 VIN6/GBE_STAT3/GPIO181 VIN7/GBE_LED3/GPIO182

SIDE_PORT_ID0 SIDE_PORT_ID1 SIDE_PORT_ID2 BOARD_ID0 BOARD_ID1 BOARD_ID2 BOARD_ID3 BOARD_ID4

NC1 NC2 NC3 NC4 NC5

VIN(0 - 7)
Voltage Monitor Not Implemented
10-KΩ 5% pull-up to +3VS5
or 10-KΩ 5% pull-down

Hudson-M2

Vender	Size	P/N
AMIC	2M	AKE38ZN0801
WINBOND	2M	AKE38FP0N01
Socket		DFHS08FS023

SPI_CLK C1064 *22P/50V_4 EMI

FCH SPI ROM

SI

R876 *10K/F_4 C1063 *0.1U/10V_4 R877 *10K/F_4

U44 CE# SCK SI SO WP# VDD VSS HOLD#

VGA Hot-plug

+1.5V R692 10K/F_4 FCH_VGA_HPD

+5V R697 100K/F_4

Q53 DMN601K-7 Q54 DMN601K-7

VGA_HPD R700 *100K/F_4

ID4	ID3	ID2	ID1	ID0	CONFIG	31- Level BOM	Item
0	0	0	0	0	UMA		1
0	0	0	1	0			2
0	0	1	0	0			3
0	0	1	1	0			4
0	1	0	1	0			5
0	1	1	1	0			6
1	0	0	1	0			7
1	0	1	1	0			8
0	0	0	0	1	SG / Muxless		9
0	0	1	0	1			10
1	0	0	1	1			11
1	0	1	1	1			12

SIDE_PORT_ID2	SIDE_PORT_ID1	SIDE_PORT_ID0	
0	0	0	Samsung
0	0	1	Hynix
0	1	0	NC
0	1	1	no supprot side port

+3VS5 R836 10K/F_4 BOARD_ID0 R837 *10K/F_4
R838 *10K/F_4 BOARD_ID1 R839 10K/F_4
R840 *10K/F_4 BOARD_ID2 R841 10K/F_4
R842 *10K/F_4 BOARD_ID3 R843 10K/F_4
R844 *10K/F_4 BOARD_ID4 R845 10K/F_4
R846 10K/F_4 SIDE_PORT_ID0 R688 *10K/F_4
R847 10K/F_4 SIDE_PORT_ID1 R689 *10K/F_4
R848 *10K/F_4 SIDE_PORT_ID2 R690 10K/F_4

Quanta Computer Inc.
PROJECT : R23

Size	Document Number	Rev
	Hudson-M3 SATA/HWM/SPI	1A

Date: Friday, January 28, 2011 Sheet 8 of 40

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

U32C

HUDSON-M3 Part 3 of 5

Hudson-M2

POWER

VDDQ--3.3V I/O power 102mA

M2 chipset need to connect to GND

1007mA for M3
902mA for M2

VDDCR-- S/B CORE power

VDDAN_11_CLK-- Internal clock Generator I/O power 340mA

VDDAN_11_PCIE --PCIE/UMI analog power 1088mA

VDDAN_11_SATA--SATA PHY analog/IO power 1337mA

VDDPL_11_SYS_S : System Clock Gen PLLs analog power

VDDPL_33_USB_S : USB PHY PLL analog power

VDDAN_33_HWM_S -- Hardware monitor interface I/O power

VDDAN_33_USB_S : USB PHY I/O analog power 470mA

VDDIO_33_S-- 3.3v S5 I/O power 59mA

VDDAN_11_USB_S : USB PHY PLL analog power 140mA

VDDXL_33_S-- 25MHZ XTAL IO power 5mA

VDDCR_1.1_S-- 1.1V S5 Core power 187mA

VDDCR_11_USB_S : USB PHY core power 42mA

VDDAN_11_SSUSB_S : USB3.0 PHY PLL analog power 282mA

VDDCR_11_SSUSB_S : USB3.0 PHY core power 424mA

M2 chipset can let it to GND

VDDPL_1.1V 70mA

VDDAN_3.3V_HWM 12mA

VDDIO_AZ 26mA

next stage should be change to +1.2VS5 from AMD Errta 1.2

This circuit is for switch DAC and UMI analog power 32 mA Max

VGA will power down when CRT no insert

VGA_PD is generated from FCH

233 mA Max

if support Modem wake up should be change pull hi to S5 power

VDDIO_AZ_S -- HD Audio Interface I/O power

if support USB 3.0 wake up should be change pull hi to S5 power

NOTE : LDO_CAP
A11 stepping : C will install 1nf cap
A12 stepping : C will let it to NC

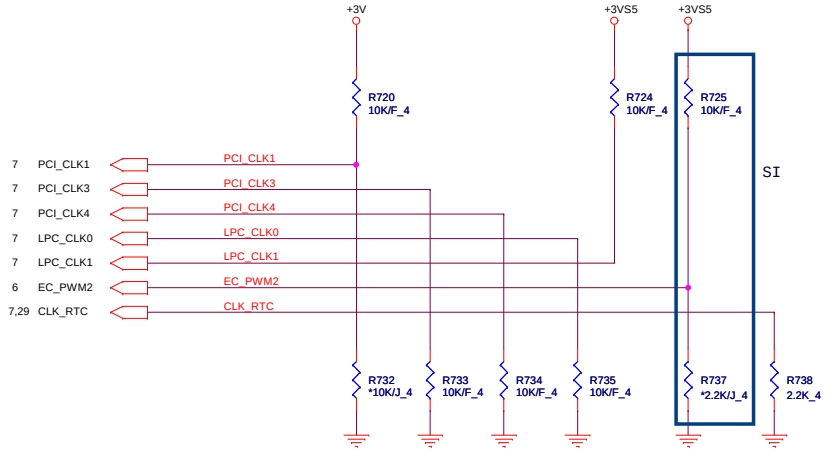
Quanta Computer Inc.
PROJECT : R23

Size	Document Number	Rev
	Hudson-M3 POWER/GND	1A

Date: Friday, January 28, 2011 Sheet 9 of 40

STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



REQUIRED STRAPS

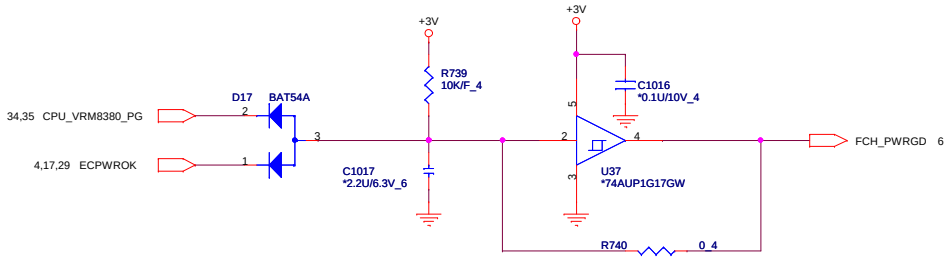
	--------	PCI_CLK1	--------	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	CLK_RTC
PULL HIGH	--------	ALLOW PCIE Gen2 DEFAULT	--------	USE DEBUG STRAP	non_Fusion CLOCK MODE	AMD internal EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM DEFAULT	S5 PLUS MODE ENABLED
PULL LOW	--------	FORCE PCIE Gen1	--------	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM	S5 PLUS MODE DISABLED DEFAULT

DEBUG STRAPS

FCH has 15K Internal Pull Up for PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

FCH PWRGD



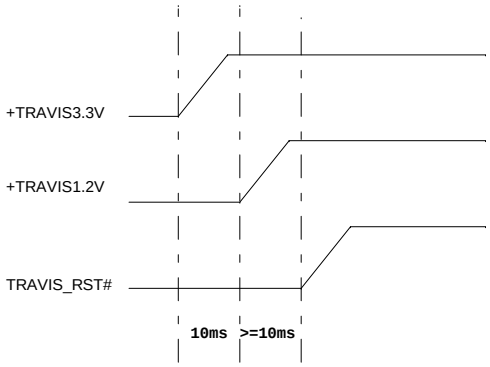
Quanta Computer Inc.

PROJECT : R23

Size	Document Number	Rev
	Hudson-M3 STRAP/PWRGD	1A

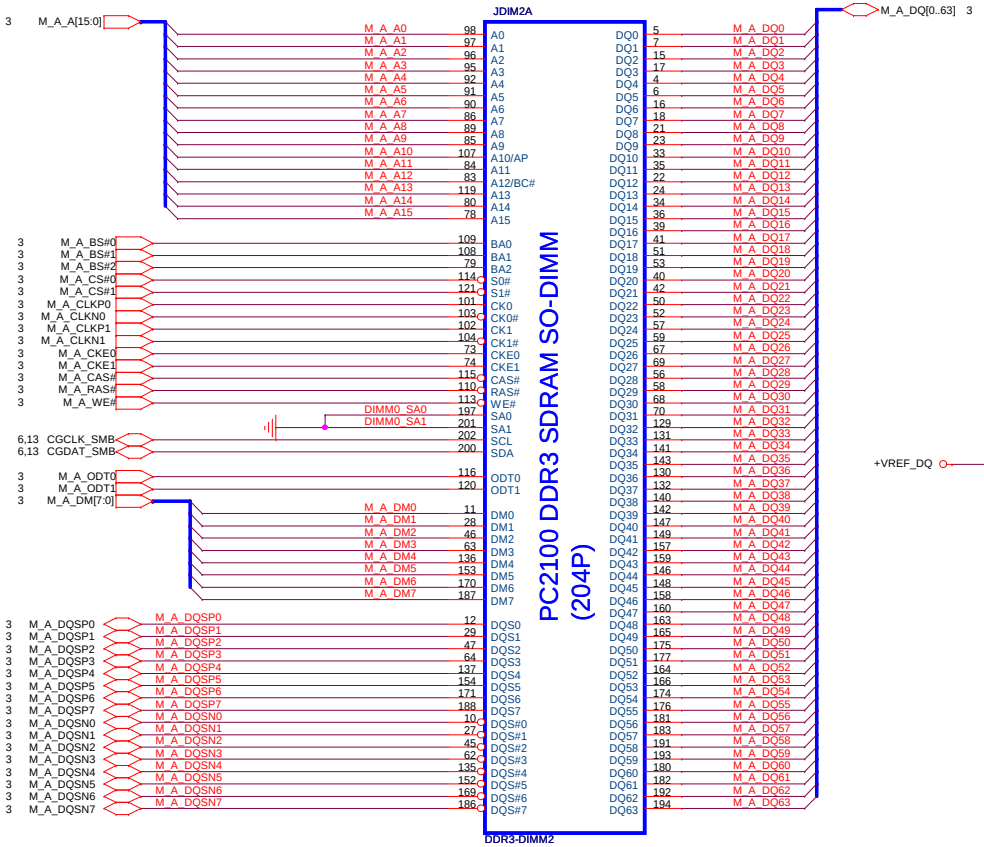
Date: Friday, January 28, 2011 Sheet 10 of 40

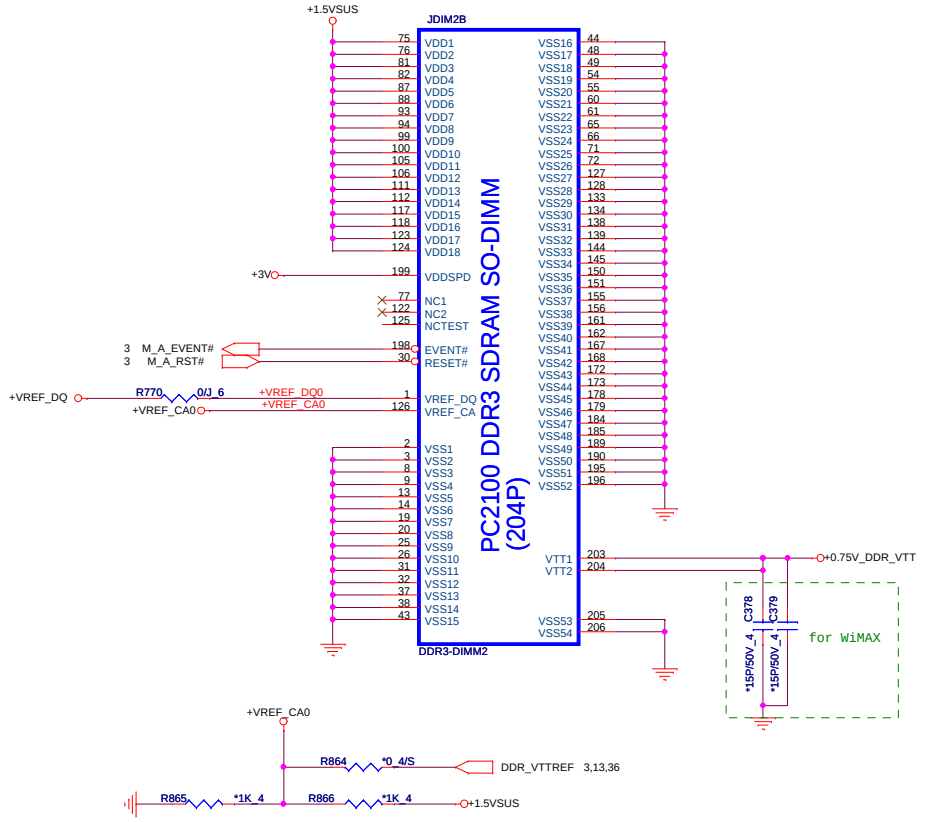
ANX3110 Power Up Sequence



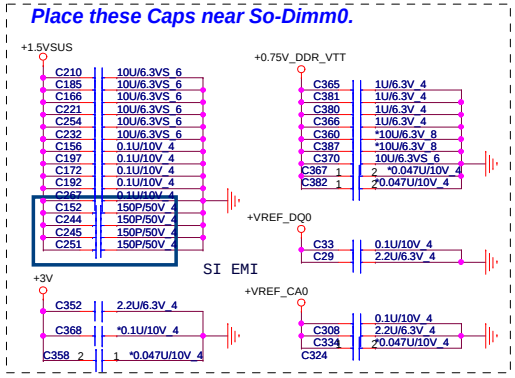
PROJECT : R23
Quanta Computer Inc.

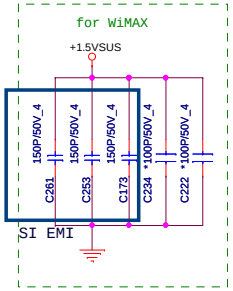
Size	Document Number	Rev
Custom	ANX3110	1A
Date: Friday, January 28, 2011	Sheet 11 of 40	

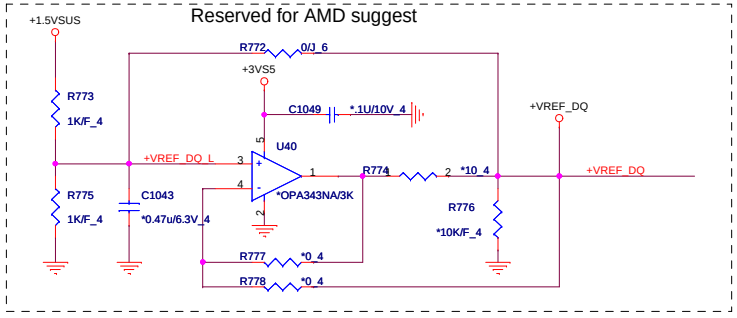




H9.2mm



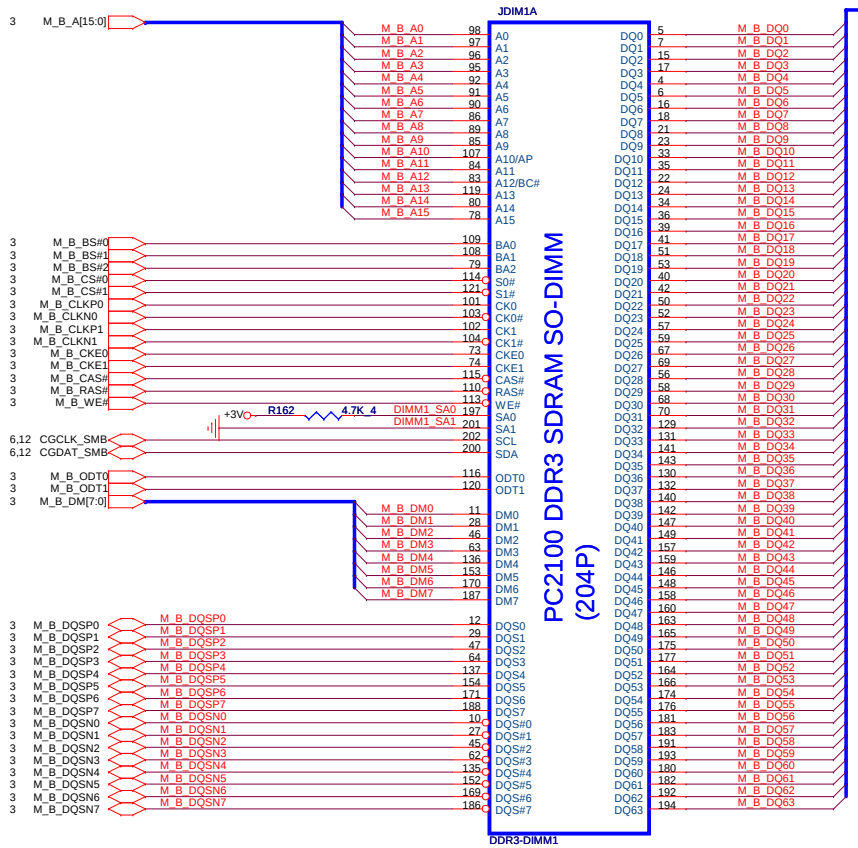


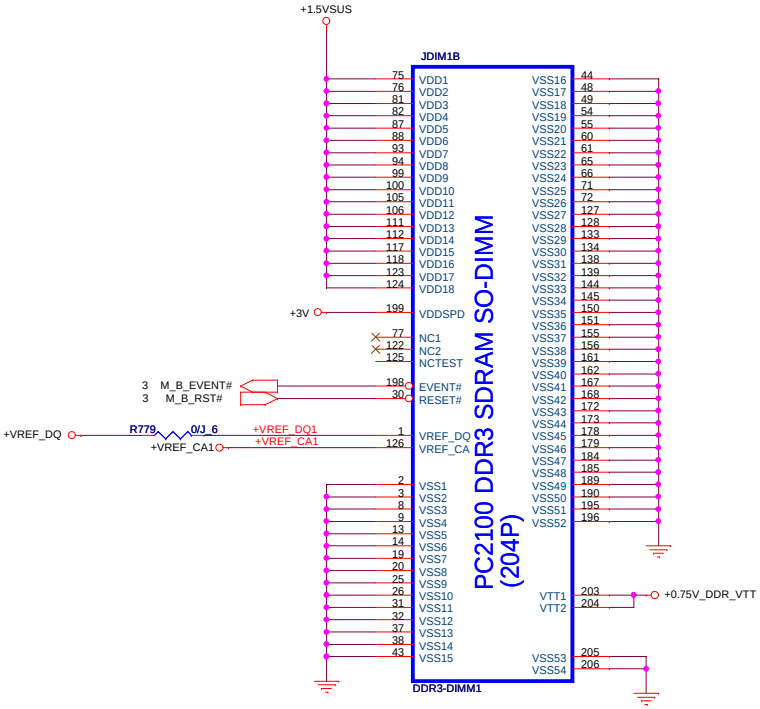


13,36 +0.75V_DDR_VTT
2,3,4,5,13,36,37,39 +1.5VSUS
2,4,6,8,9,10,11,13,14,17,20,22,23,24,25,27,28,29,30,34,37,39 +3V

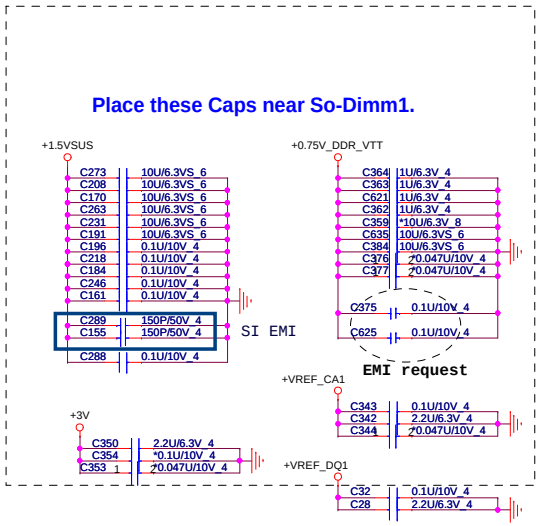
PROJECT : R23
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM-0	1A
Date: Friday, January 28, 2011	Sheet 12 of 40	





H5.2mm



12,36 +0.75V_DDR_VTT
2,3,4,5,12,36,37,39 +1.5VSUS
2,4,6,8,9,10,11,12,14,17,20,22,23,24,25,27,28,29,30,34,37,39 +3V

PROJECT : R23
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM-1	1A

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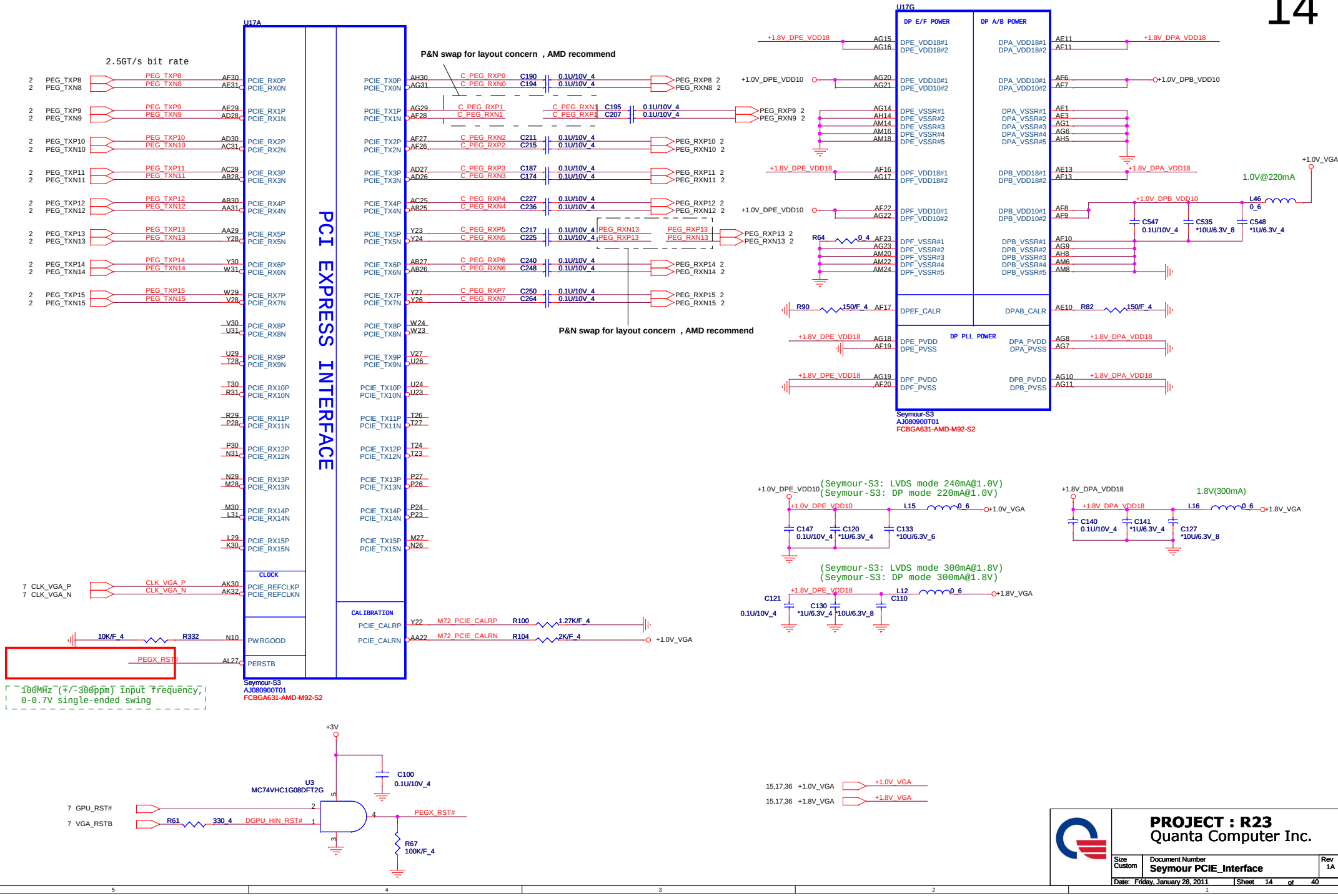
U17A
PCI EXPRESS INTERFACE
2.5GT/s bit rate
P&N swap for layout concern , AMD recommend
P&N swap for layout concern , AMD recommend
CLOCK
CALIBRATION
Seymour-S3
AJ080900T01
FCBGA631-AMD-M92-S2
100MHz (+/-300ppm) input frequency,
0-0.7V single-ended swing
U17G
DP E/F POWER
DP A/B POWER
DP PLL POWER
Seymour-S3
AJ080900T01
FCBGA631-AMD-M92-S2
(Seymour-S3: LVDS mode 240mA@1.0V)
(Seymour-S3: DP mode 220mA@1.0V)
(Seymour-S3: LVDS mode 300mA@1.8V)
(Seymour-S3: DP mode 300mA@1.8V)
1.0V@220mA
1.8V(300mA)
U3
MC74VHC1G08DFT2G
PROJECT : R23
Quanta Computer Inc.
Seymour PCIE_Interface
Date: Friday, January 28, 2011
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MEM_ID[3:0]	Vendor	Type	Vendor P/N	QUANTA P/N
0000	Samsung- E die	64*16-800MHZ	K4W1G1646E-HC12	Reserved
0001	Hynix- Vega die	64*16-800MHZ	H5TQ1G63DFR-12C	Reserved
0010	Hynix- Vega die	128*16-800MHZ	H5TQ2G63BFR-12C	Reserved
0011	Samsung- C die	128*16-800MHZ	K4W2G1646C-HC12	Reserved
0100	Micron	128*16-800MHZ	MT41J128M16HA-125:D	Reserved
0101	Reserved	Reserved	Reserved	Reserved
0110	Hynix- Vega die	64*16-900MHZ	H5TQ1G63DFR-11C	AKD5LZWTW02
0111	Samsung- E die	64*16-900MHZ	K4W1G1646E-HC11	Reserved
1000	Samsung- G die	64*16-900MHZ	K4W1G1646G-BC11	AKD5EGG1500
1001	Reserved	Reserved	Reserved	Reserved
1010	Hynix- Vega die	128*16-900MHZ	H5TQ2G63BFR-11C	AKD5MGWTW00
1011	Samsung- C die	128*16-900MHZ	K4W2G1646C-HC11	AKD5MGWT500
1100			Reserved	Reserved
1101			Reserved	Reserved
1110			Reserved	Reserved
1111			Reserved	Reserved

AMD request to use Hi voltage enter O.S

GPIO15 GPIO20

Seymour-XT	PWRCNTL0	PWRCNTL1	V-CORE
L	0	0	0.9V
M	0	1	1V
H	1	0	1.1V (Default)
TBD	1	1	NA

Access to SCL and SDA is mandatory on BACO designs for debug purposes

GPIO22(ROMCS#) PD without external VBIOS ROM

If no contact this pin to LVDS need pull low

Seymour uninstall Ra to meet AF24 N/C

DAC2 is NC on Seymour

Reserve for AMD debug only

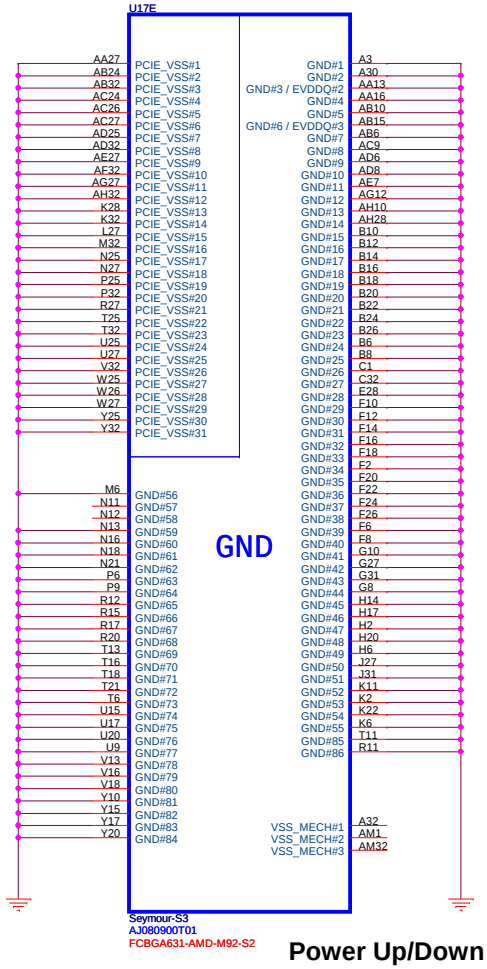
Reserve for DB debug only

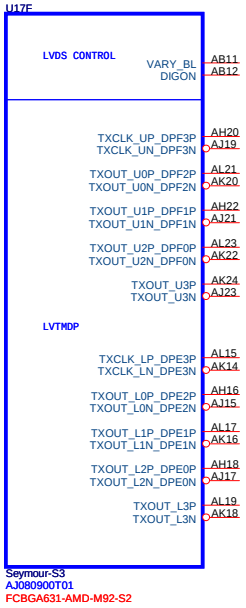
Seymour-S3--NC ROBSON--install

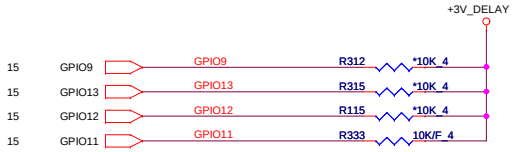
Robson-- Install Seymour- NC BACO mode -- install

follow AMD checklist change from 10M to 1Mohm

For Int Clk 27Mhz







CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	**Transmitter Power Savings Enable** 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	**PCI Express Transmitter De-emphasis Enable** 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

AMD RESERVED CONFIGURATION STRAPS

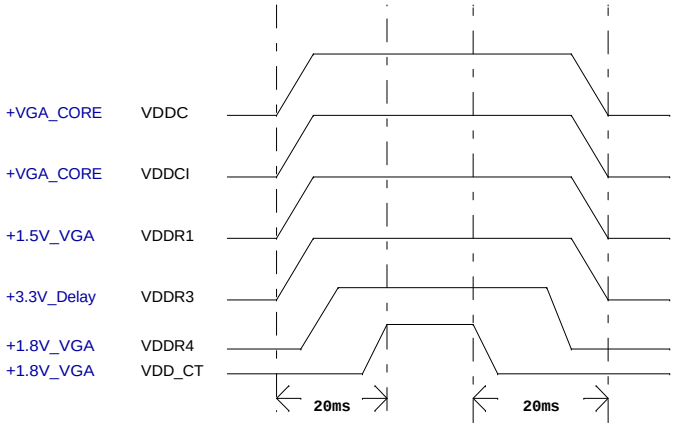
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO21_BB_EN

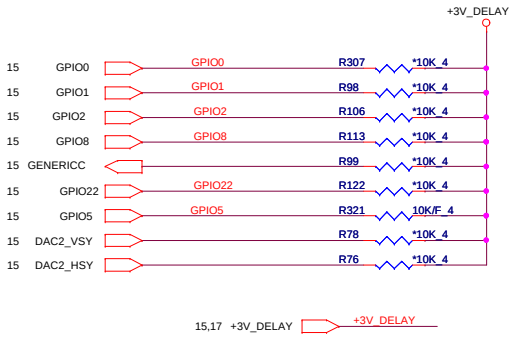
Power Up/Down Sequence



Memory Aperture size

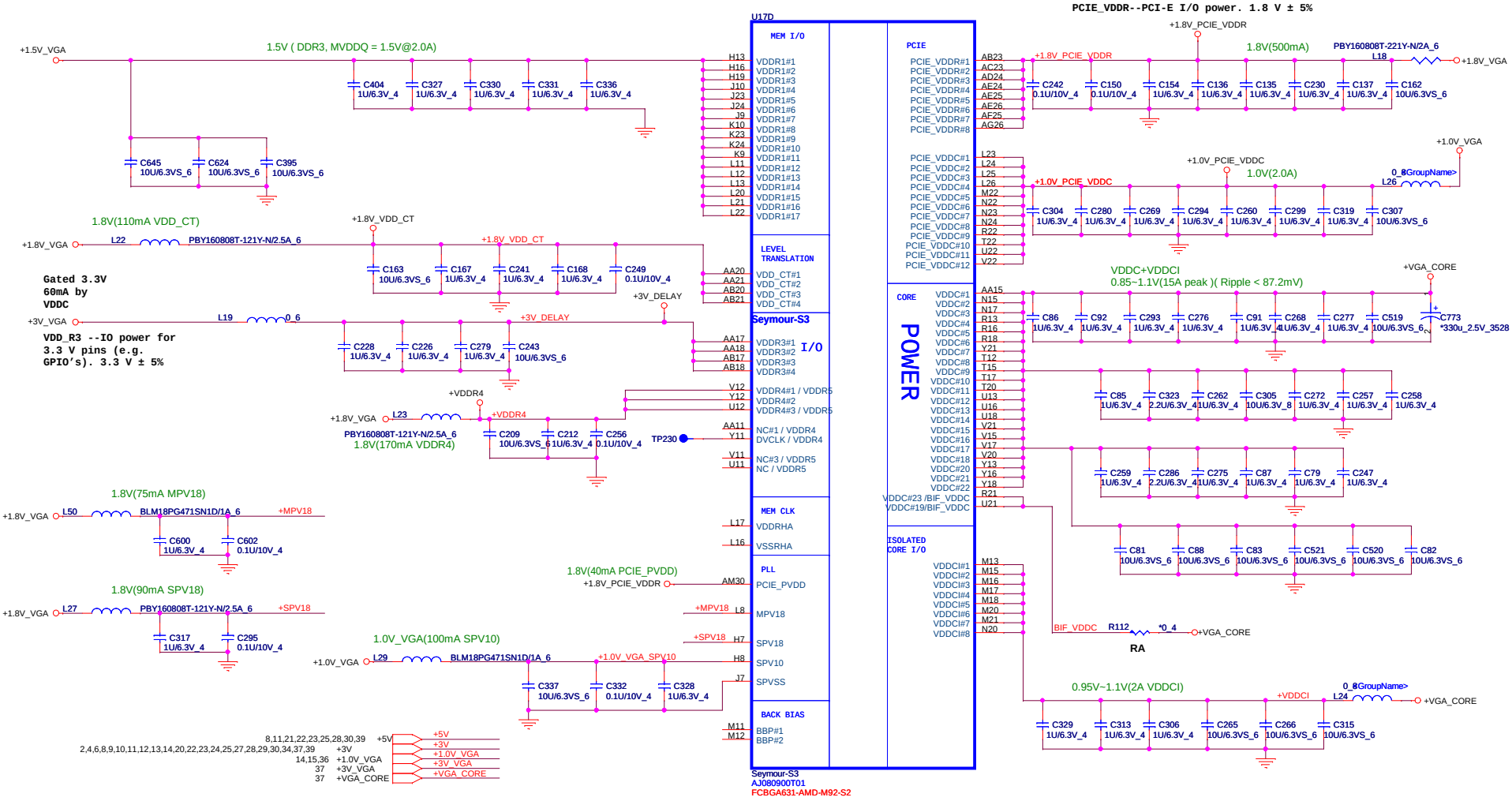
GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

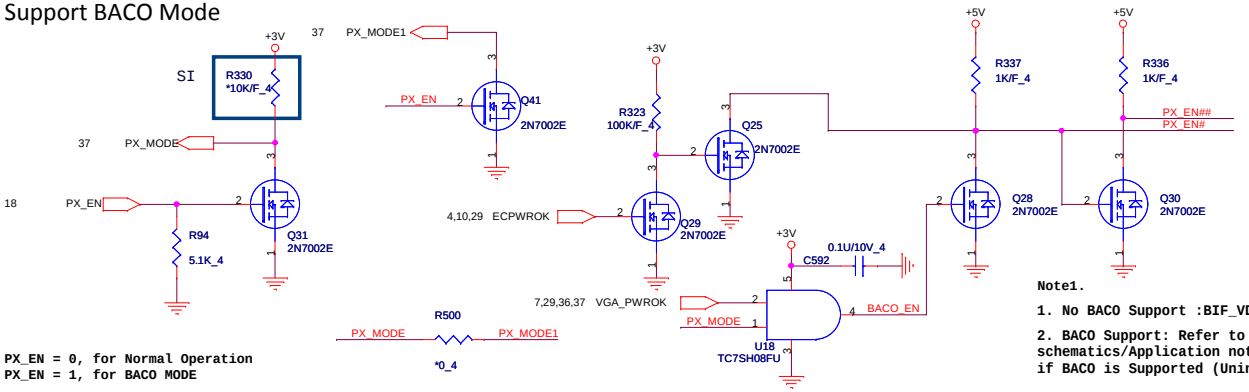


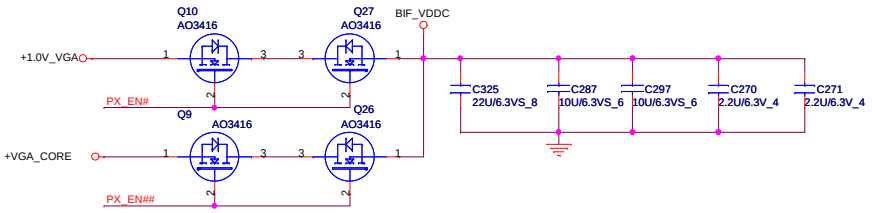
PROJECT : R23
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Seymour GND / LVDS/ Straps	1A
Date: Friday, January 28, 2011	Sheet 16 of 40	



Support BACO Mode





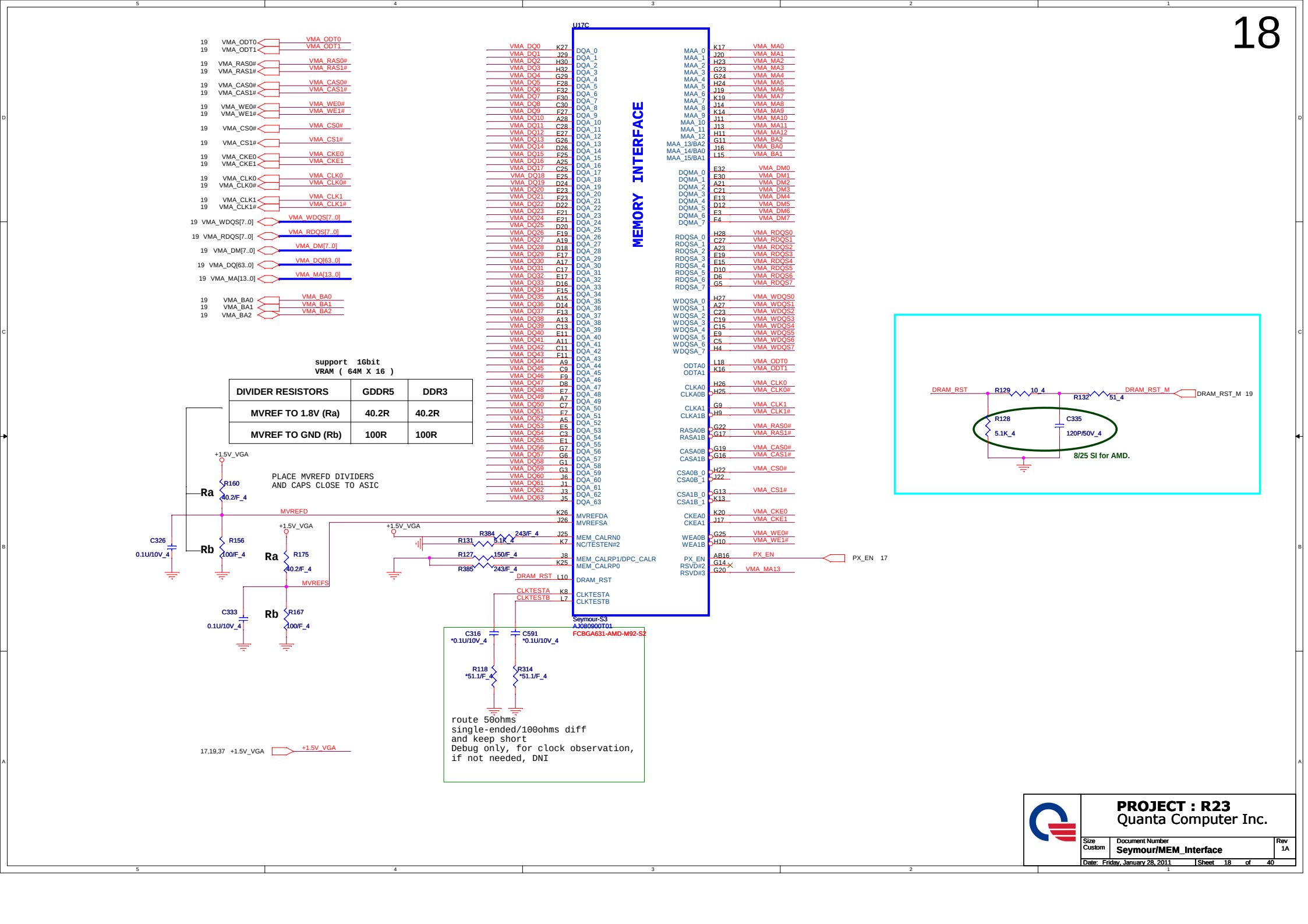
PX_EN = 0, for Normal Operation
PX_EN = 1, for BACO MODE

Note1.

1. No BACO Support :BIF_VDDC shorts with VDDC (Install Ra)
2. BACO Support: Refer to the BACO reference schematics/Application note for detail about BIF_VDDC Rail if BACO is Supported (Uninstall Ra)

PROJECT : R23
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Seymour_Power_and_NC	1A
Date: Friday, January 28, 2011	Sheet 17 of 40	


U17C
MEMORY INTERFACE
Seymour-S3
AJ080900T01
FCBGA631-AMD-M92-S2
support 1Gbit
VRAM (64M X 16)
DIVIDER RESISTORS | GDDR5 | DDR3
MVREF TO 1.8V (Ra) | 40.2R | 40.2R
MVREF TO GND (Rb) | 100R | 100R
PLACE MVREFD DIVIDERS
AND CAPS CLOSE TO ASIC
route 50ohms
single-ended/100ohms diff
and keep short
Debug only, for clock observation,
if not needed, DNI
8/25 SI for AMD.
PROJECT : R23
Quanta Computer Inc.
Size Custom
Document Number
Seymour/MEM_Interface
Rev 1A
Date: Friday, January 28, 2011
Sheet 18 of 40

1GB DDR3

18 VMA_MA[13..0]
18 VMA_DM[7..0]
VMA_MA[13..0]
18 VMA_DQ[63..0]
18 VMA_WDQS[7..0]
18 VMA_RDQS[7..0]

U7 / U19 / U6 / U20 — 100-BALL SDRAM DDR3 — K4W2G1646C-HC11

Should be 243 Ohms +-1%: R174 243/F_4 (U7), R389 243/F_4 (U19), R159 243/F_4 (U6), R379 243/F_4 (U20)

+1.5V_VGA

R401 4.99K/F_4 / R400 4.99K/F_4 / C644 0.1U/10V_4 — VREFC_VMA1
R148 4.99K/F_4 / R151 4.99K/F_4 / C372 0.1U/10V_4 — VREFD_VMA1
R392 4.99K/F_4 / R405 4.99K/F_4 / C650 0.1U/10V_4 — VREFC_VMA2
R146 4.99K/F_4 / R153 4.99K/F_4 / C369 0.1U/10V_4 — VREFD_VMA2
R185 4.99K/F_4 / R183 4.99K/F_4 / C402 0.1U/10V_4 — VREFC_VMA3
R165 4.99K/F_4 / R181 4.99K/F_4 / C396 0.1U/10V_4 — VREFD_VMA3
R383 4.99K/F_4 / R388 4.99K/F_4 / C626 0.1U/10V_4 — VREFC_VMA4
R378 4.99K/F_4 / R386 4.99K/F_4 / C623 0.1U/10V_4 — VREFD_VMA4

VMA_CLK0 — R161 56.2/F_4 — VMA_CLK0_COMM — C374 0.01U/25V_4 — R169 56.2/F_4 — VMA_CLK0#
VMA_CLK1 — R154 56.2/F_4 — VMA_CLK1_COMM — C385 0.01U/25V_4 — R158 56.2/F_4 — VMA_CLK1#
17,18,37 +1.5V_VGA

+1.5V_VGA: C355 C357 C406 C397 C393 C349 C347 C655 1U/6.3V_4
+1.5V_VGA: C653 C648 C637 C403 C408 C345 C641 C643 1U/6.3V_4
+1.5V_VGA: C656 C633 C410 C409 10U/6.3VS_6
+1.5V_VGA: C620 C618 C651 C346 C654 C636 C614 C611 0.1U/10V_4
+1.5V_VGA: C627 C622 C628 C632 C639 C642 C400 C405 0.1U/10V_4

	QCI PN
SAM 1G	AKD5MGWT500
HYU 1G	AKD5MGWTW00
SAMSUNG	AKD5EGGT500
HYNIX	AKD5LZWTW02

PROJECT : R23
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Seymour VRAM(DDR3 BGA96)	3A

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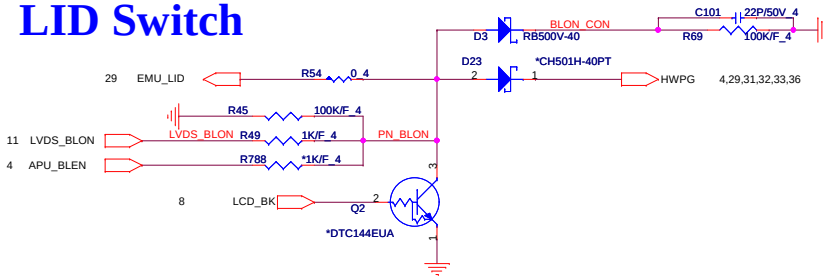
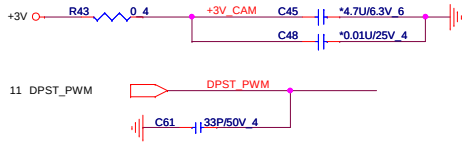
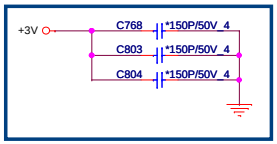
LID Switch

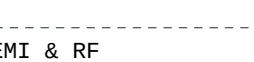




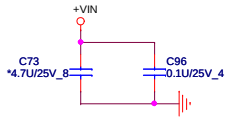
SI EMI



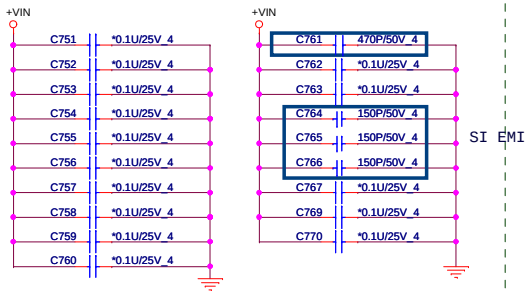
follow L7 Location

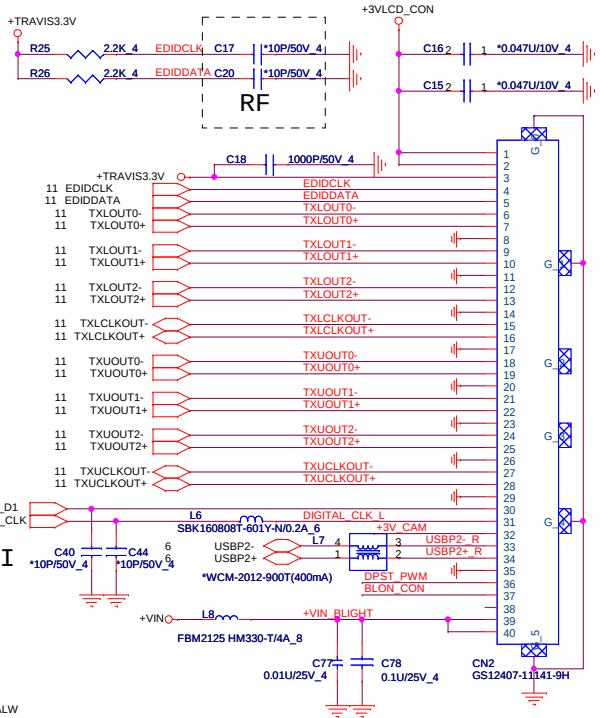


EMI & RF



Coupling CAP.



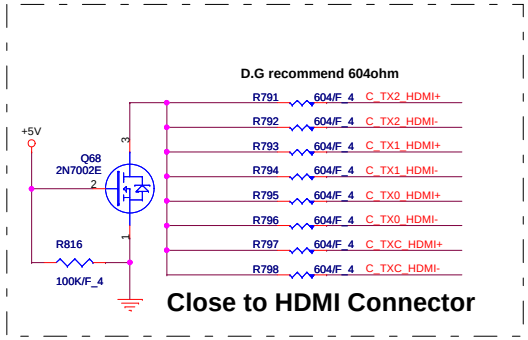


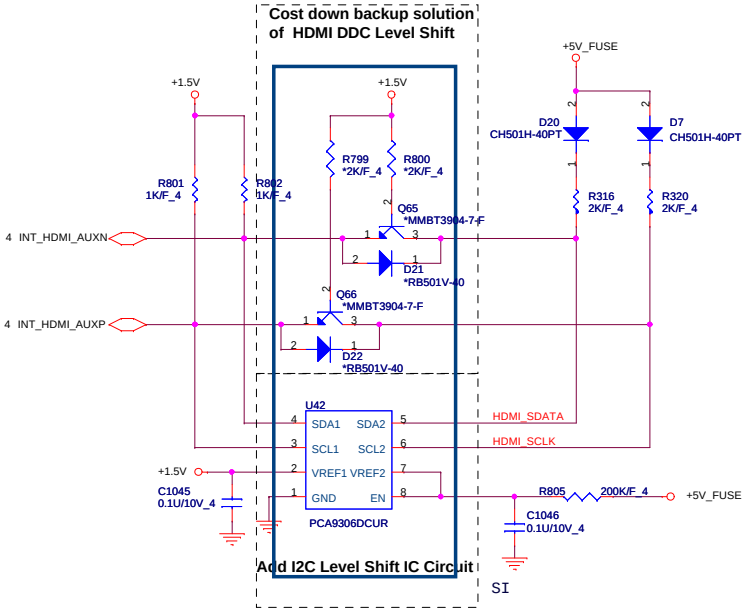
4,7,26,28,29,31,38 +3VPCU
2,4,6,8,9,10,11,12,13,14,17,22,23,24,25,27,28,29,30,34,37,39 +3V
9,37,38,39 +12VALW
31,32,33,34,35,36,37,38,39 +VIN

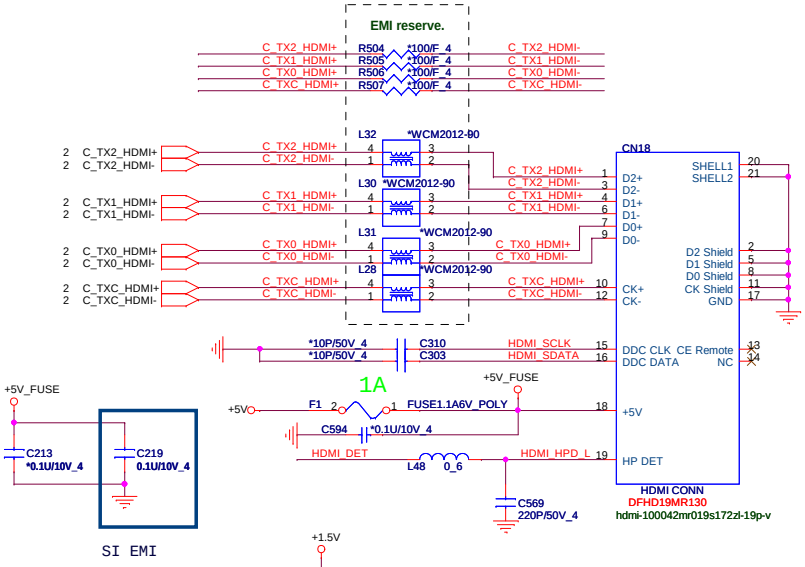
PROJECT : R23
Quanta Computer Inc.

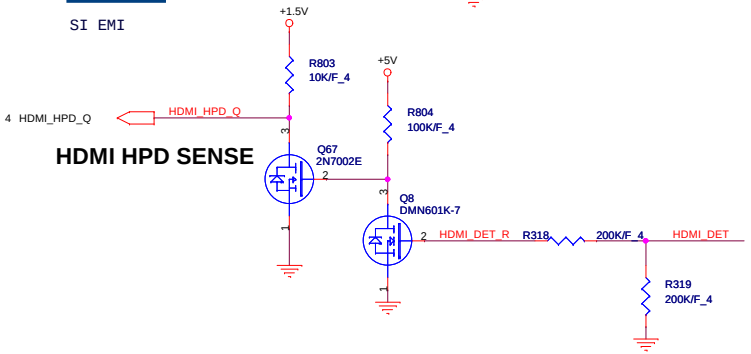
Size	Document Number	Rev
Custom	LCD CONN/LID/CAM	1A
Date: Friday, January 28, 2011	Sheet 20 of 40	

HDMI PORT







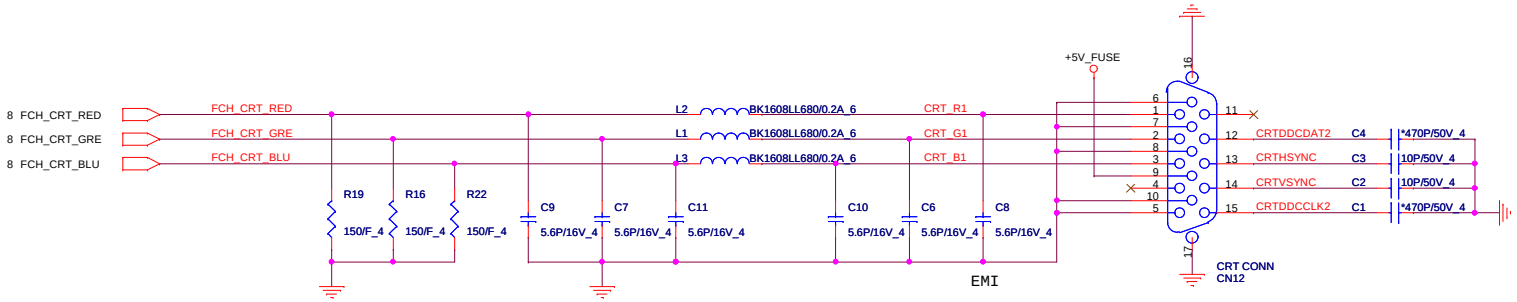


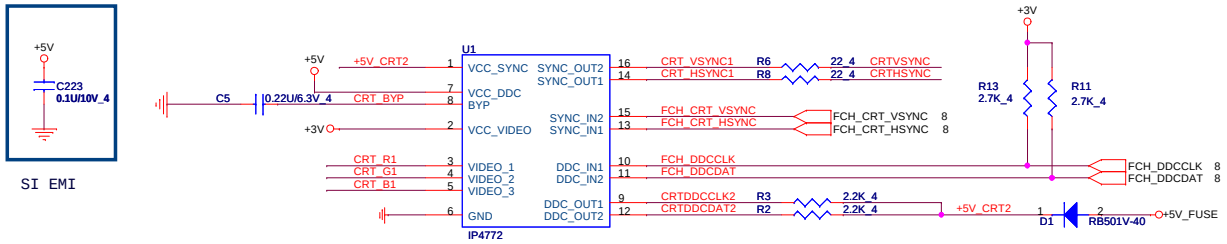
PROJECT : R23
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDMI CONN	1A

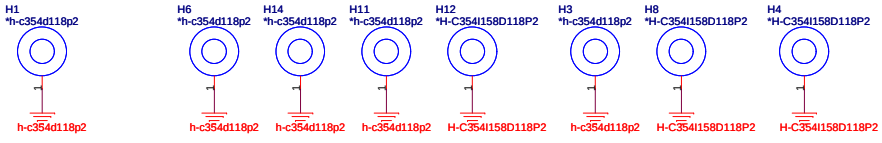
Date: Friday, January 28, 2011 Sheet 21 of 40

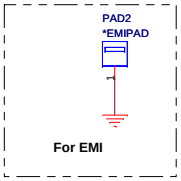
CRT PORT



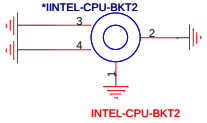


HOLE

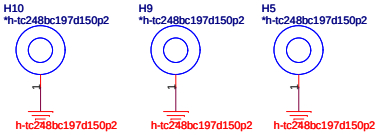




CPU



VGA



PROJECT : R23
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT,Hole	1A

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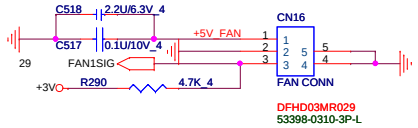
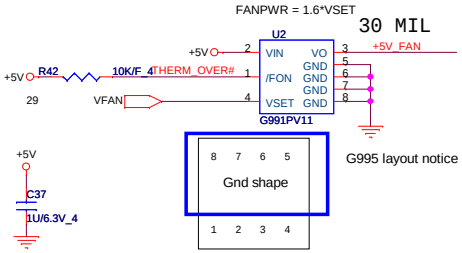
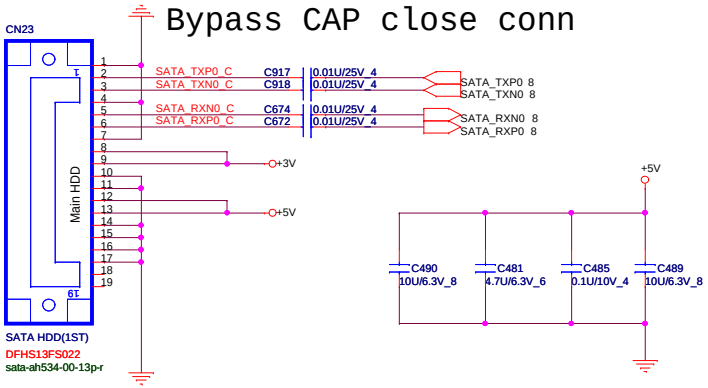
CPU FAN





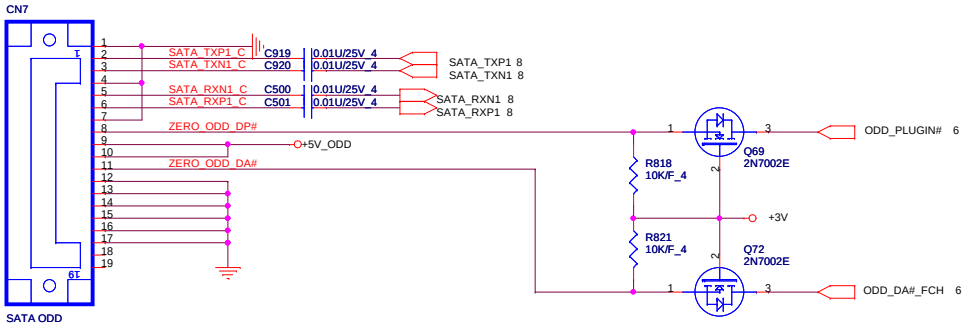
SATA HDD CONNECTOR

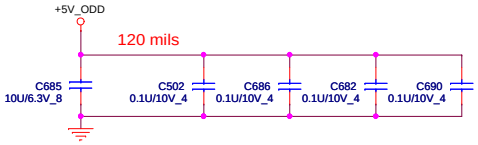
Bypass CAP close conn

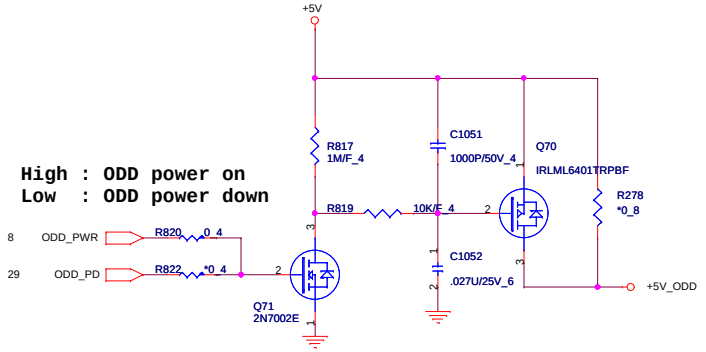


SATA ODD CONNECTOR

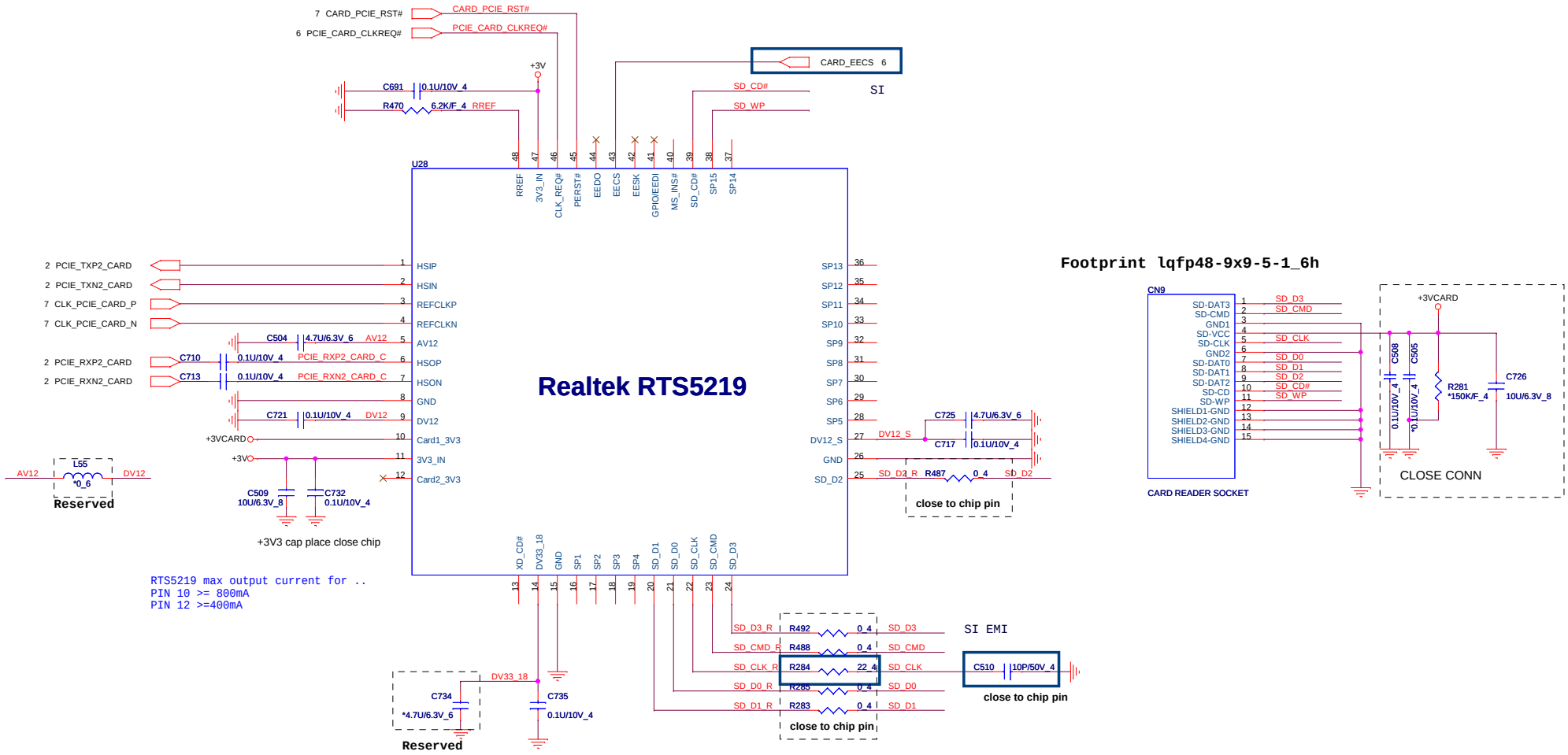
SATA ODD





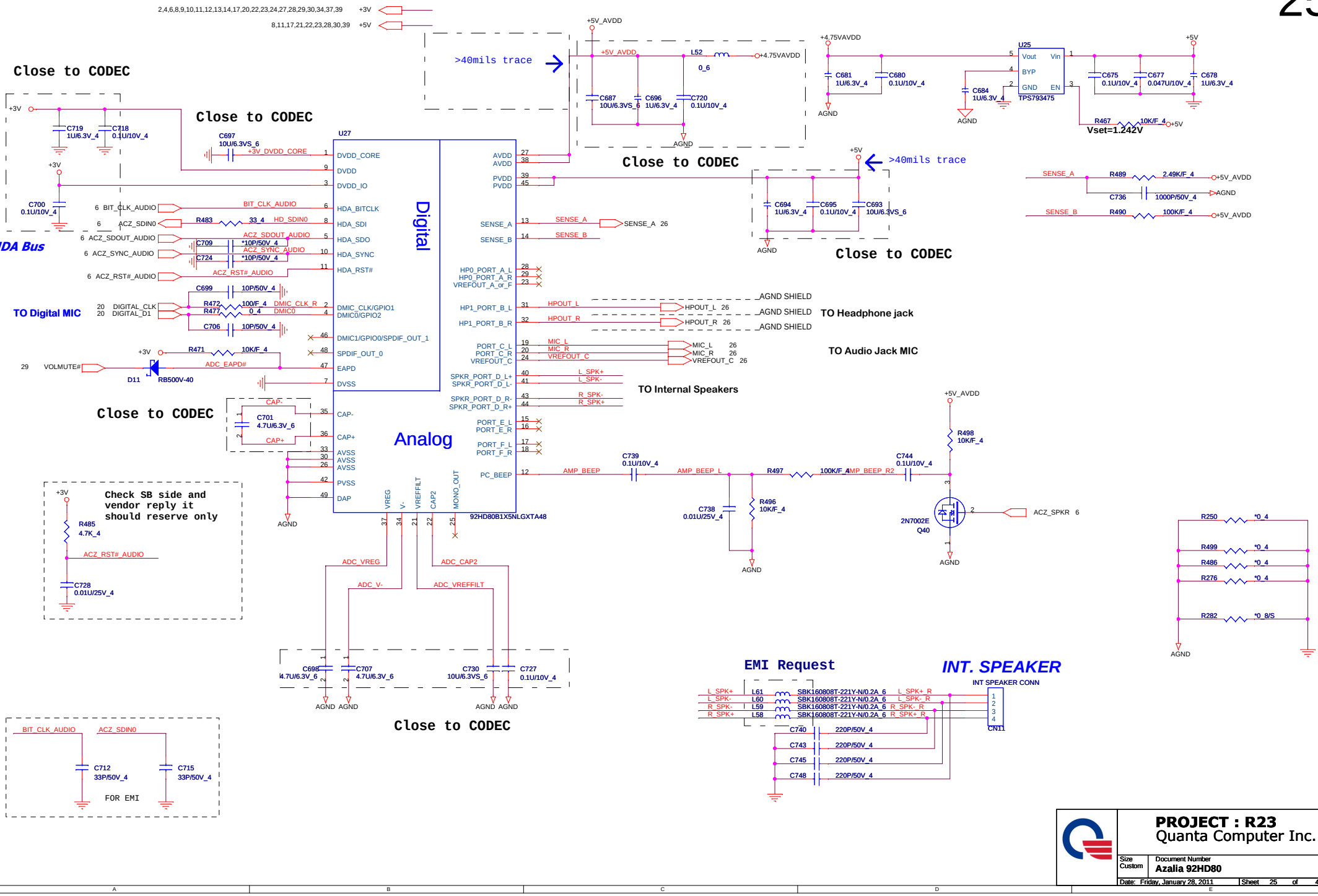


PROJECT : R23 Quanta Computer Inc.		
Size: Custom	Document Number: HDD/ODD/FAN	Rev: 1A
Date: Friday, January 28, 2011	Sheet 23 of 40	

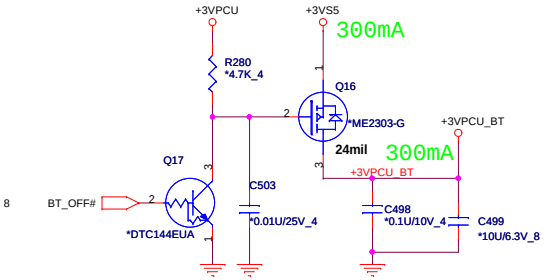


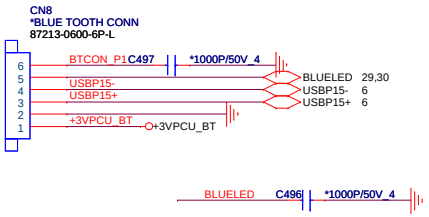
Footprint lqfp48-9x9-5-1_6h

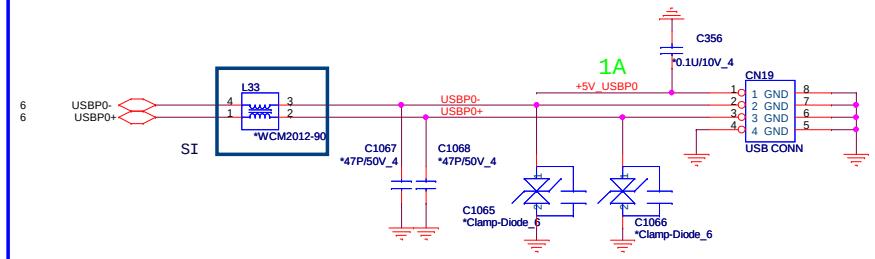
PROJECT : R23 Quanta Computer Inc.		
Size: Custom	Document Number: RTS5219 & CR SOCKET &HOLE	Rev: 1A
Date: Friday, January 28, 2011	Sheet 24 of 40	

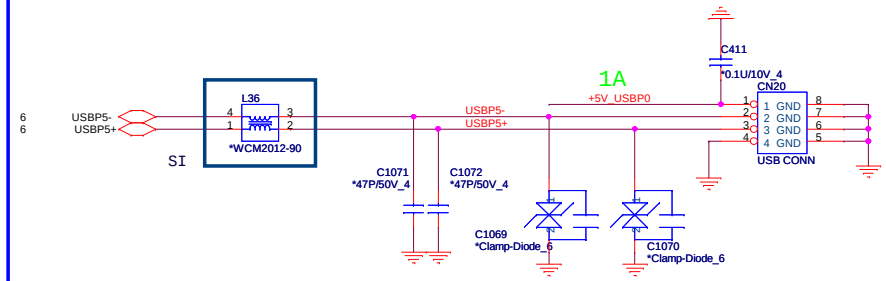

Close to CODEC
Close to CODEC
Close to CODEC
Close to CODEC
Close to CODEC
Close to CODEC
>40mils trace
>40mils trace
HDA Bus
TO Digital MIC
TO Headphone jack
TO Audio Jack MIC
TO Internal Speakers
Digital
Analog
U27
92HD80B1X5NLGXTA48
U25
TPS793475
Vset=1.242V
Check SB side and vendor reply it should reserve only
EMI Request
INT. SPEAKER
INT SPEAKER CONN
CN11
FOR EMI
AGND SHIELD
+5V_AVDD
+4.75VAVDD
+3V_DVDD_CORE
ACZ_RST#_AUDIO
ADC_VREG
ADC_V-
ADC_CAP2
ADC_VREFFILT
AMP_BEEP
ACZ_SPKR 6
2N7002E
Q40

BLUETOOTH

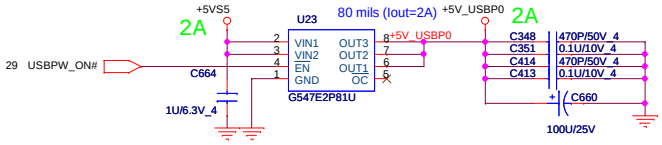




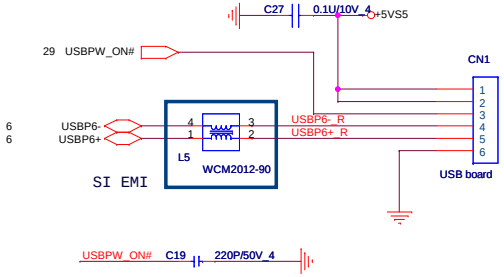




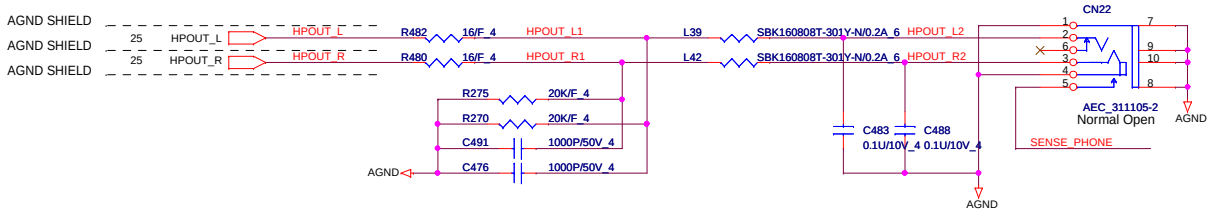
LEFT SIDE USBX2



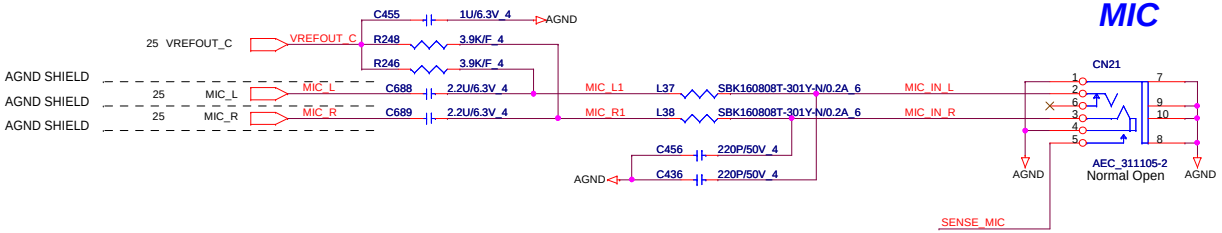
Right SIDE USBX1



Line out

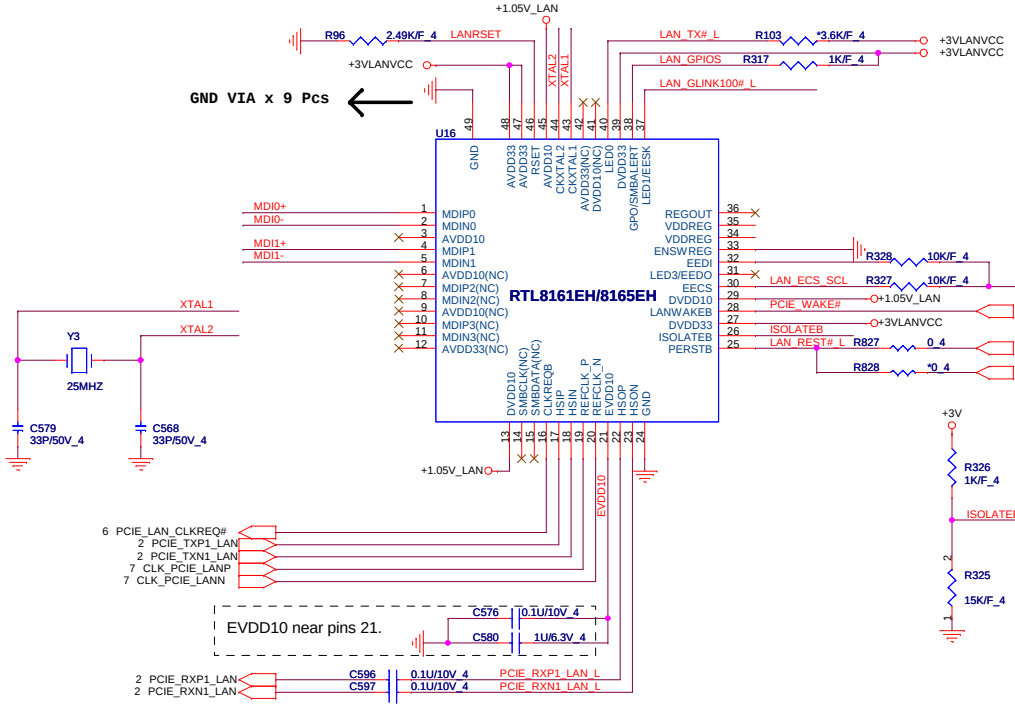


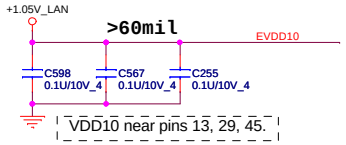
MIC

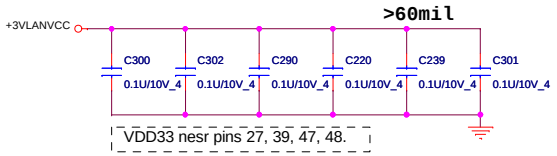


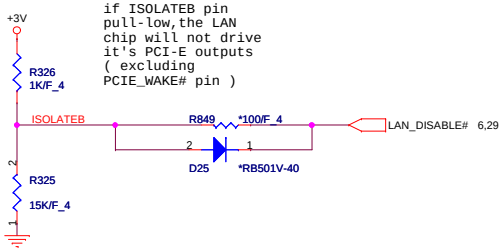
PROJECT : R23
Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB/BT/Audio JacK	1A
Date: Friday, January 28, 2011	Sheet 26 of 40	

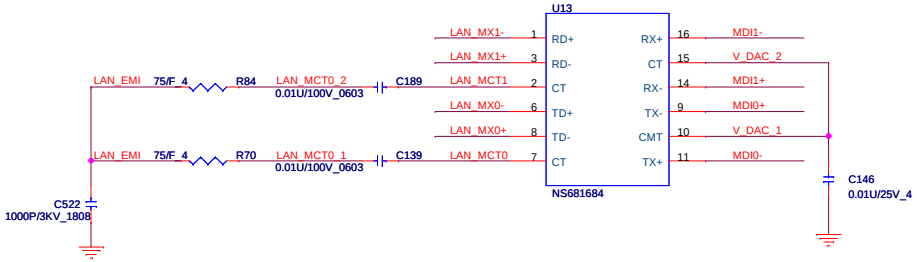




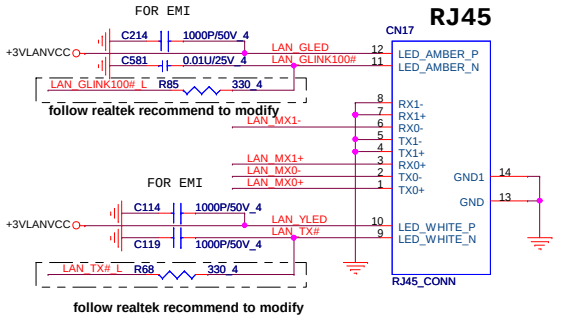




Transformer for 10/100



Lan Con.



39 +3VLANVCC
2,4,6,8,9,10,11,12,13,14,17,20,22,23,24,25,28,29,30,34,37,39 +3V

PROJECT : R23
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTL8165EH	1A

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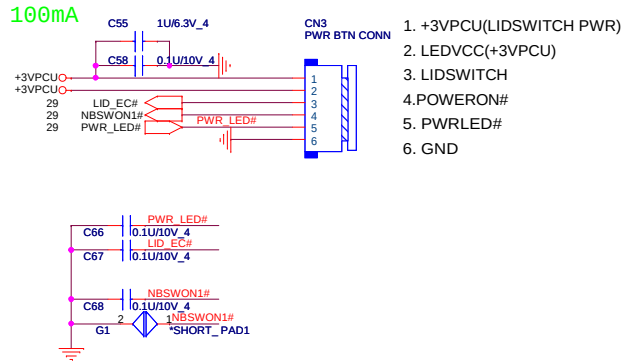
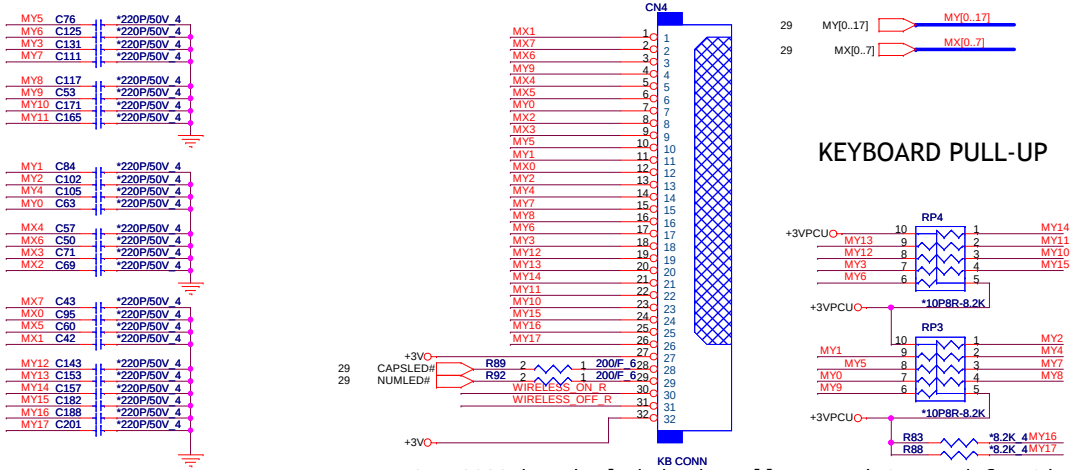
POWER BOTTON CONNECT



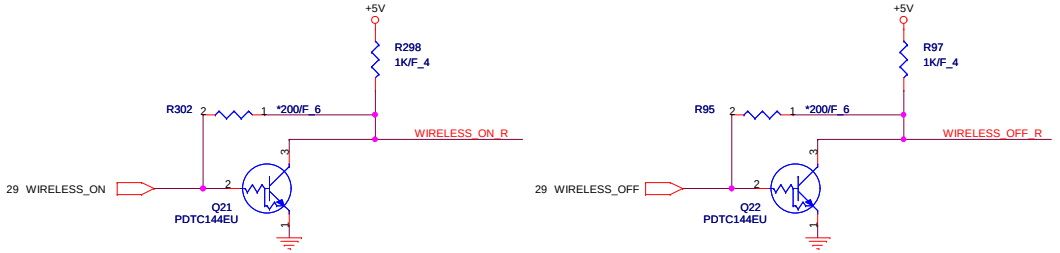
1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4.POWERON#
5. PWRLED#
6. GND

KEYBOARD Con.

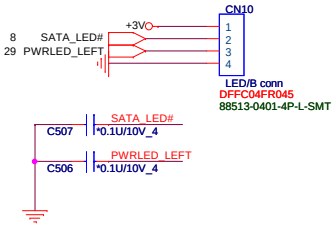


KEYBOARD PULL-UP

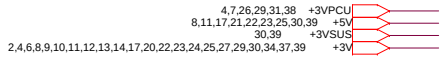
EC KB3930 has included K/B pull-up resistor and function



LED Con.

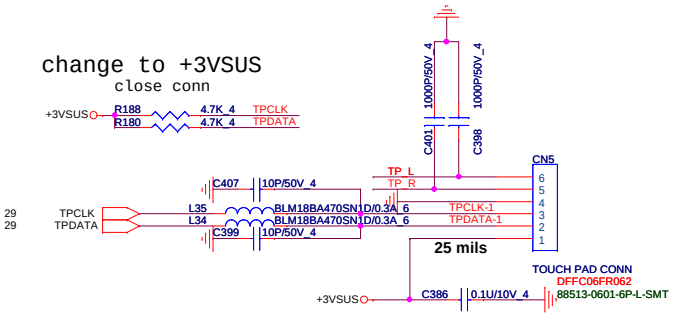


1. +3V
2. SATA_LED#
3. PWR_LED#
4.GND

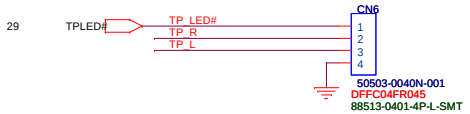


TOUCH PAD Con.

change to +3VSUS
close conn



To TOUCH PAD SW board



PROJECT : R23
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LED/KB/SW/TP	1A

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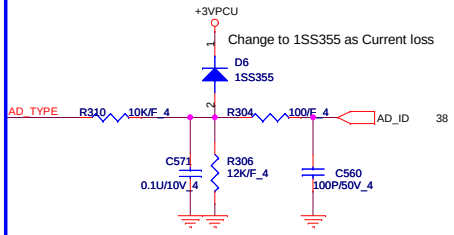
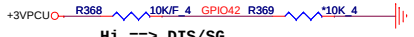
Smart adapter Type check

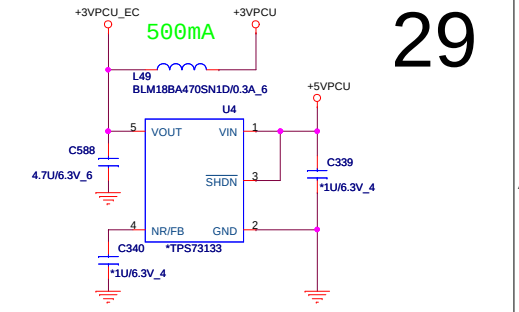


Adapter select

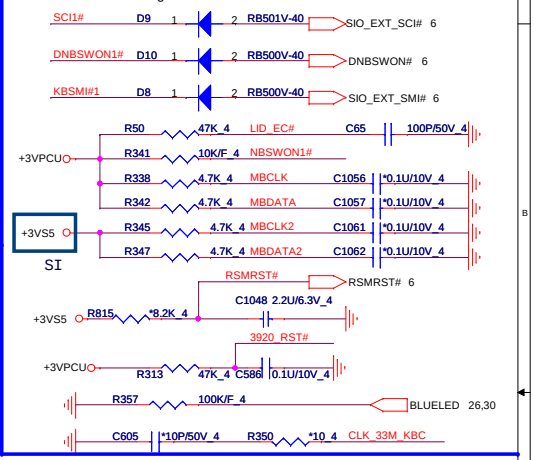


Hi ==> DIS/SG
Low ==>UMA

Platform model	GPIO42	adapter
SG/DIS	High	90W
UMA	Low	65W

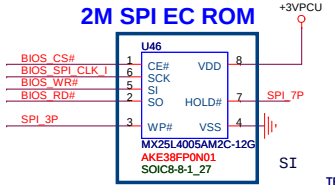


Change to RB500 as Current loss

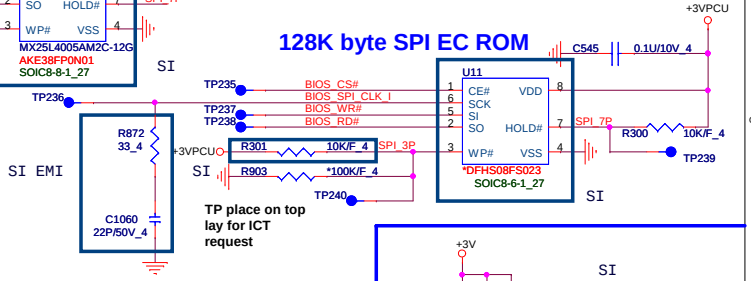


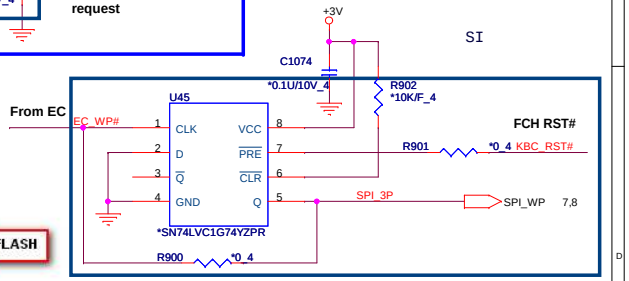
Vender	Size	P/N
AMIC	128K	AKE35ZN0801
EON	128K	AKE35FN0Q00
Socket		DFHS08FS023

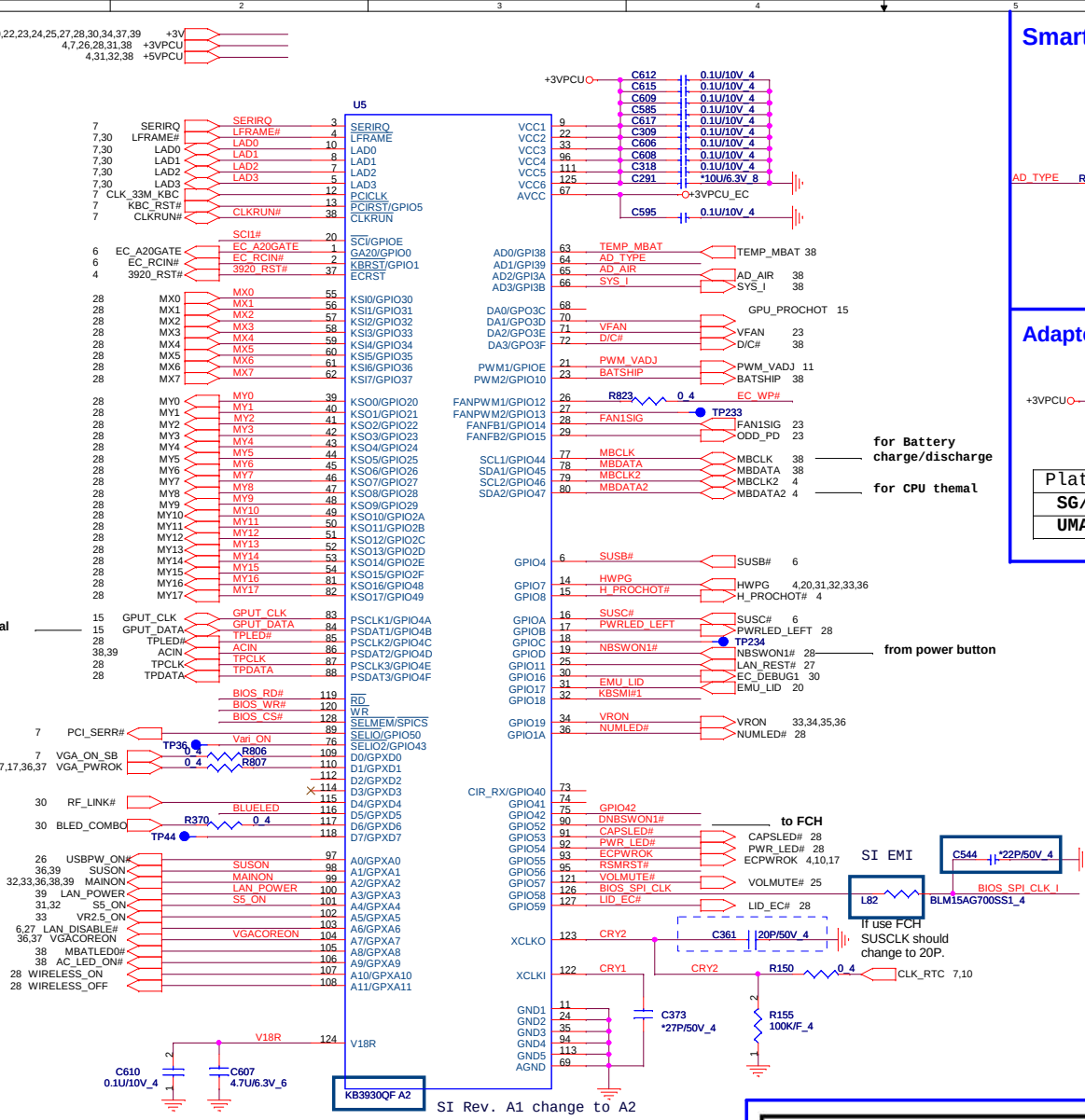
2M SPI EC ROM



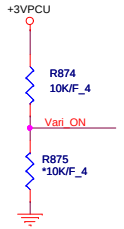
128K byte SPI EC ROM



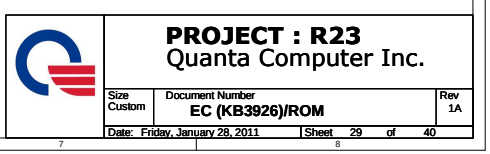




CPU Thermal SMBUS select	Vari_ON	project
SCL1/SDA1	Low	R22
SCL2/SDA2	High	R23,R24

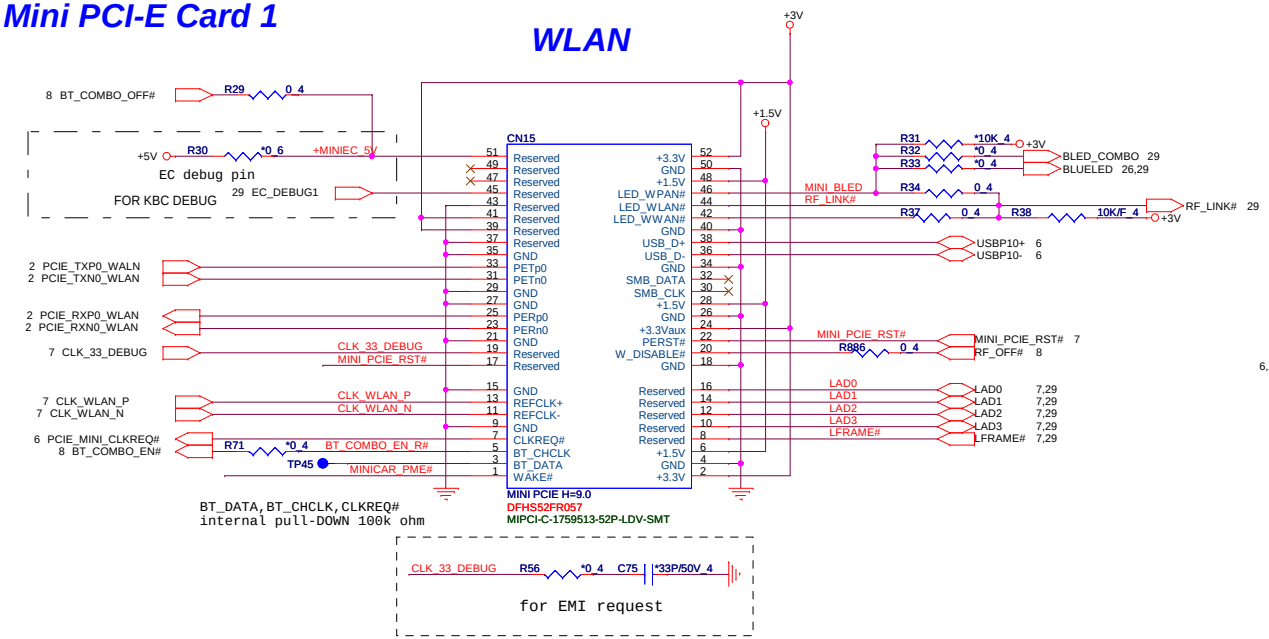


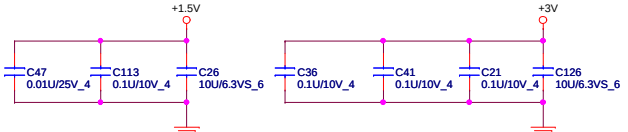
INPUTS				OUTPUTS		
PRE	CLR	CLK	D	Q	Q	
L	H	X	X	H	L	FLASH
H	L	X	X	L	H	
L	L	X	X	H (1)	H (1)	
H	H	↑	H	H	L	
H	H	↑	L	L	H	LOCK
H	H	L	X	Q_0	$\overline{Q_0}$	

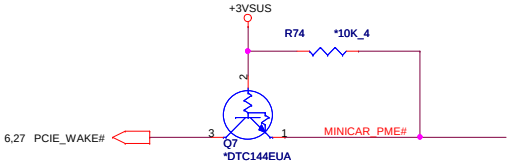


Mini PCI-E Card 1

WLAN





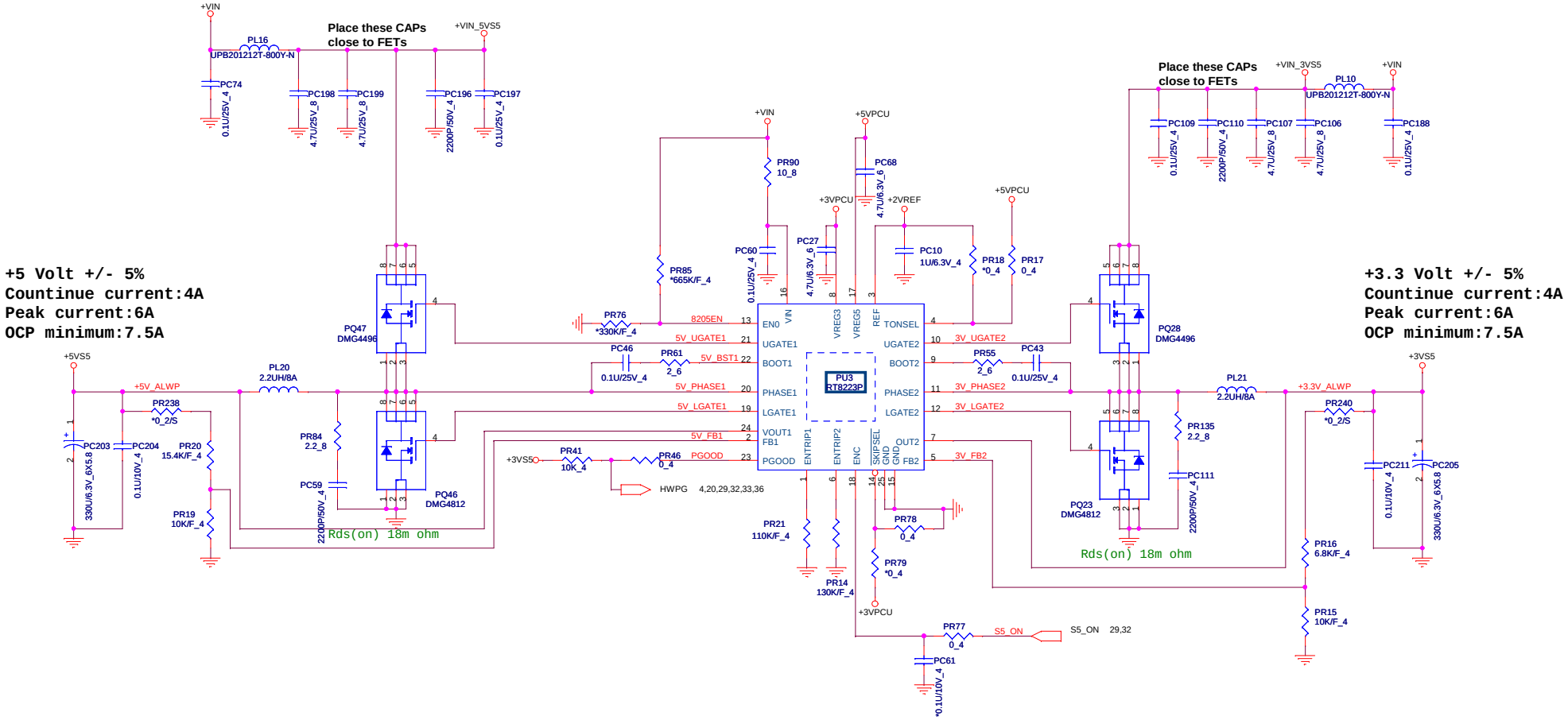


2,4,8,11,21,34,35,39 +1.5V
2,4,6,8,9,10,11,12,13,14,17,20,22,23,24,25,27,28,29,34,37,39 +3V
4,7,26,28,29,31,38 +3VPCU
8,11,17,21,22,23,25,28,39 +5V

PROJECT : R23
Quanta Computer Inc.

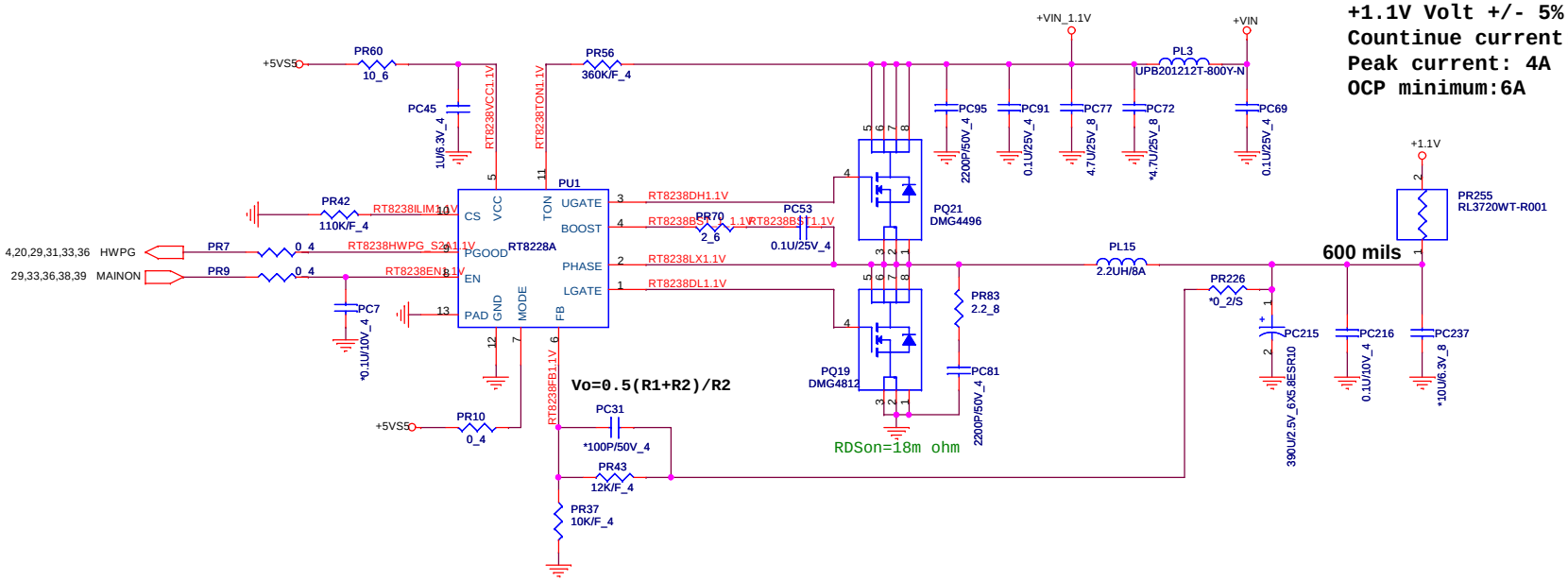
Size	Document Number	Rev
Custom	MINI PCIE CONN X1	1A

Date: Friday, January 28, 2011 Sheet 30 of 40

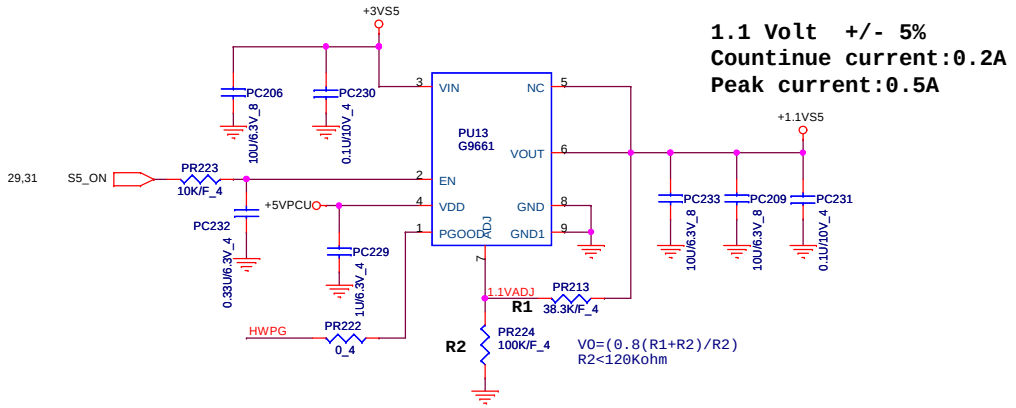


PROJECT : R23 Quanta Computer Inc.		
Size: Custom	Document Number: +5V/+3V (RT8206B)	Rev: 1A
Date: Friday, January 28, 2011	Sheet 31 of 40	

+1.1V Volt +/- 5%
Countinue current:3A
Peak current: 4A
OCP minimum:6A



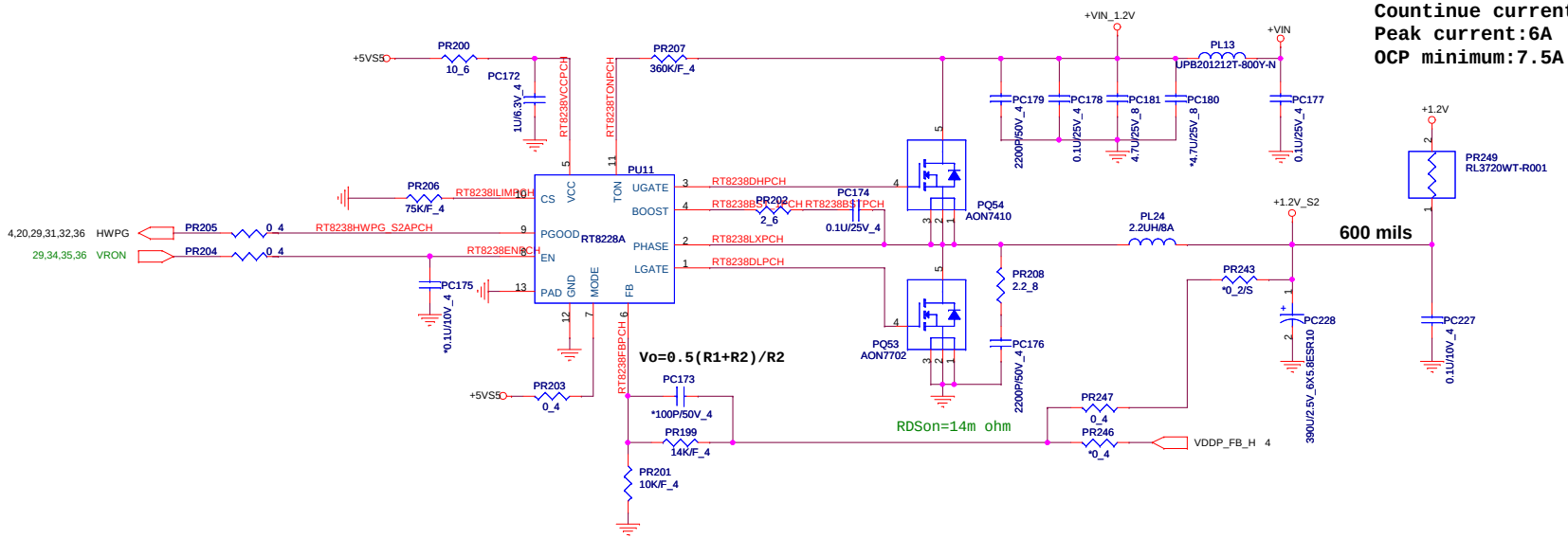
1.1 Volt +/- 5%
Countinue current:0.2A
Peak current:0.5A



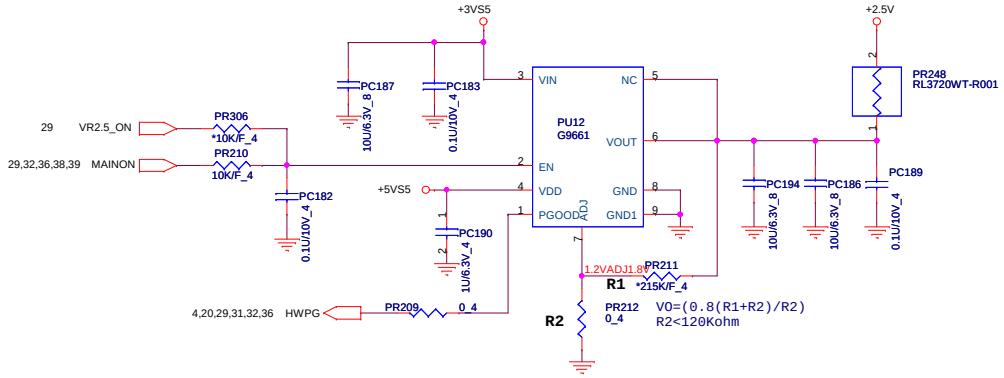
PROJECT : R23
Quanta Computer Inc.

Size	Document Number	Rev
Custom	VGA Core/+1.8VGFX/1.0VGFX	1A
NB5/RD2	Date: Friday, January 28, 2011	Sheet 32 of 40

+1.05V PCH Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

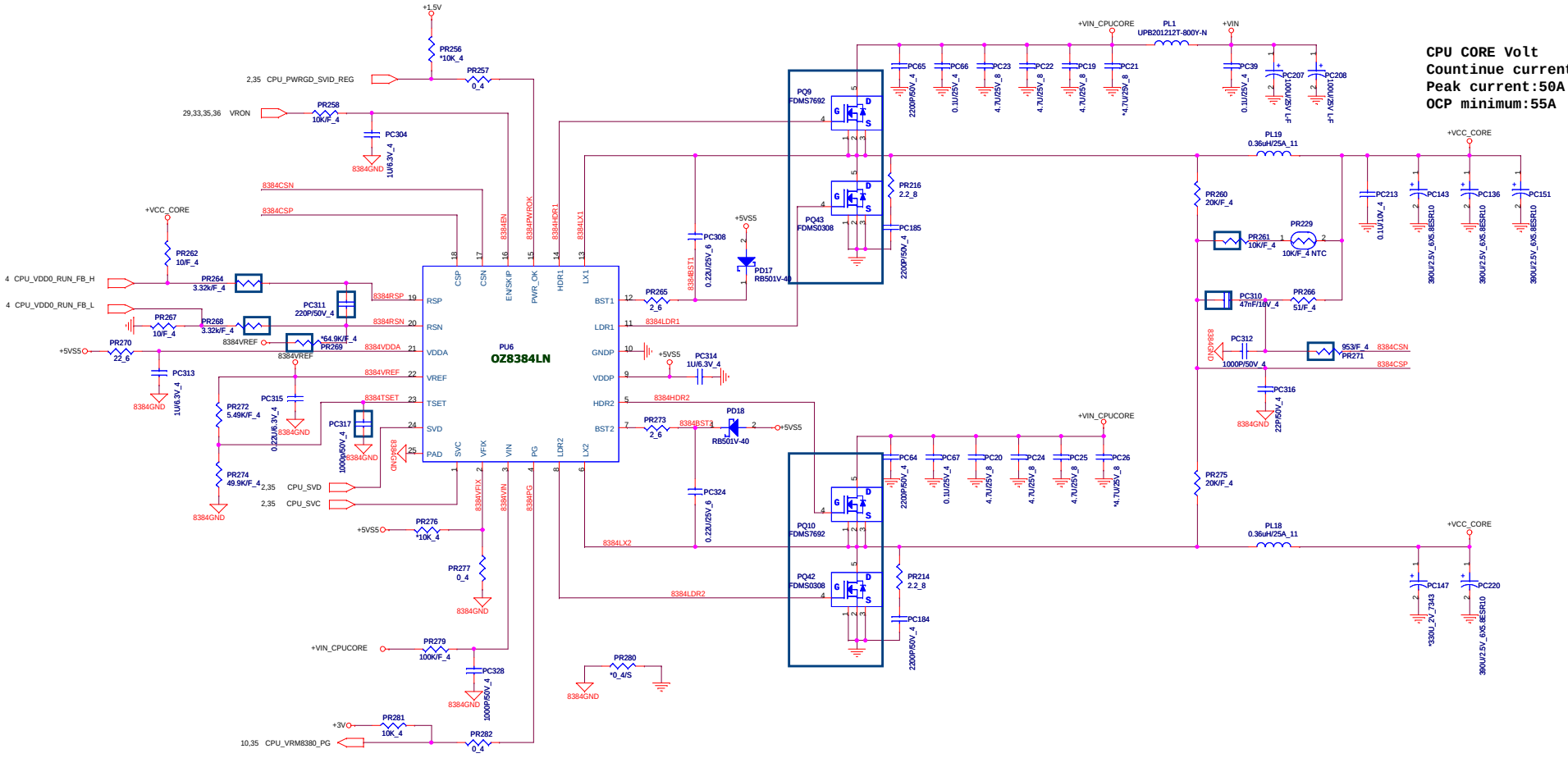


+2.5V +/- 5%
Countinue current:0.3A
Peak current:0.75A

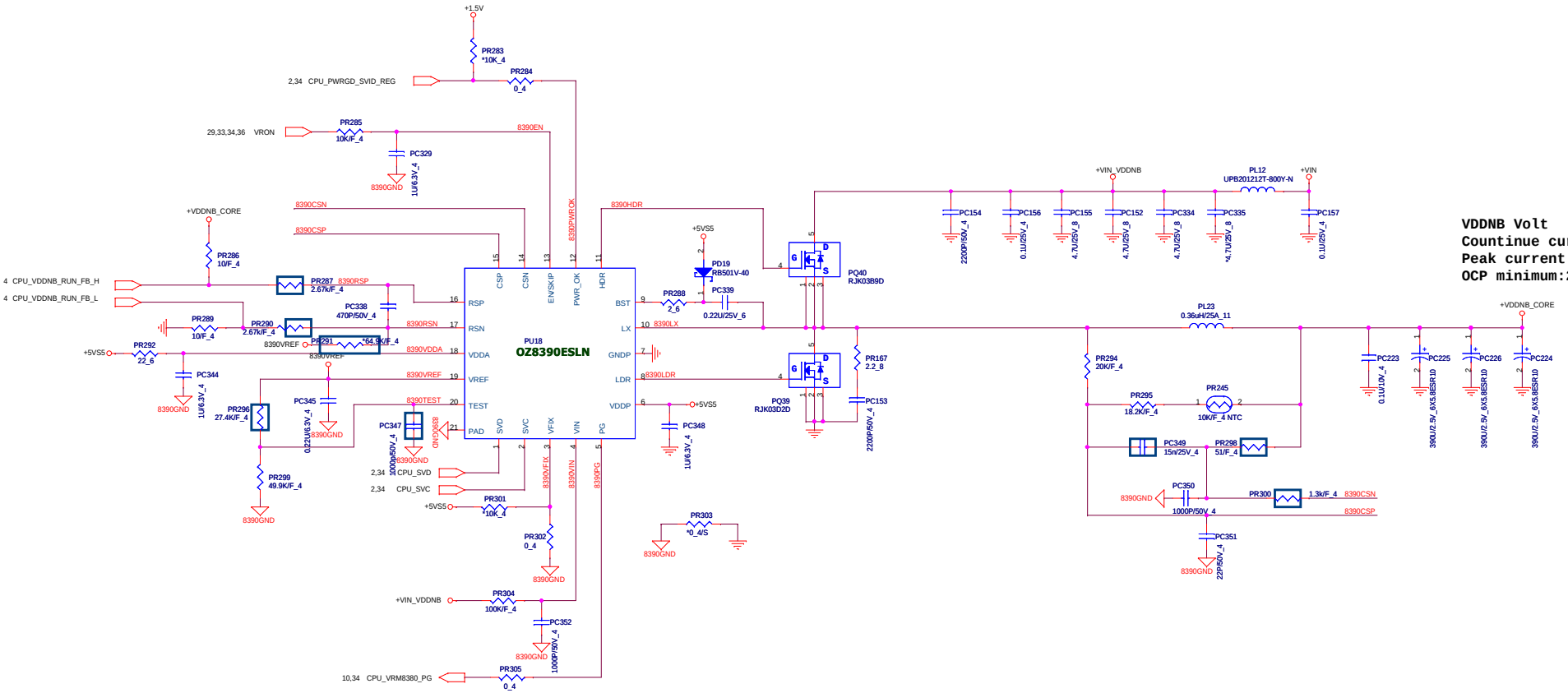


PROJECT : R23
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.05V (RT8238A)	1A
Date: Friday, January 28, 2011	Sheet 33 of 40	



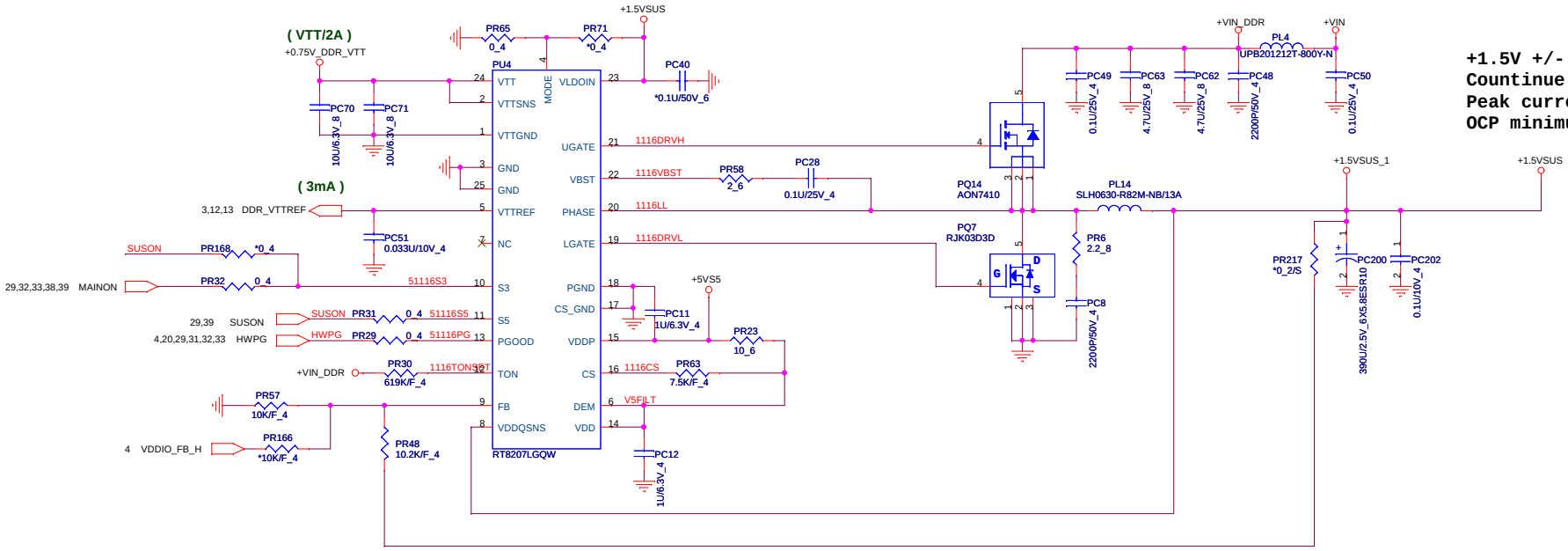
NB5/RD2	PROJECT : R23 Quanta Computer Inc.		
Size C	Document Number +1.1V VTT / PCH		Rev 1A
Date: Friday, January 28, 2011		Sheet 34 of 40	



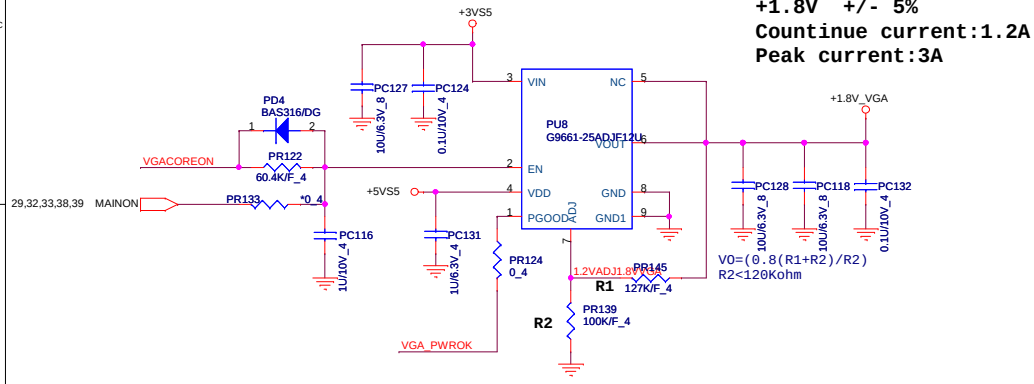
VDDNB Volt
Countinue current:18A
Peak current:22.5A
OCP minimum:27A

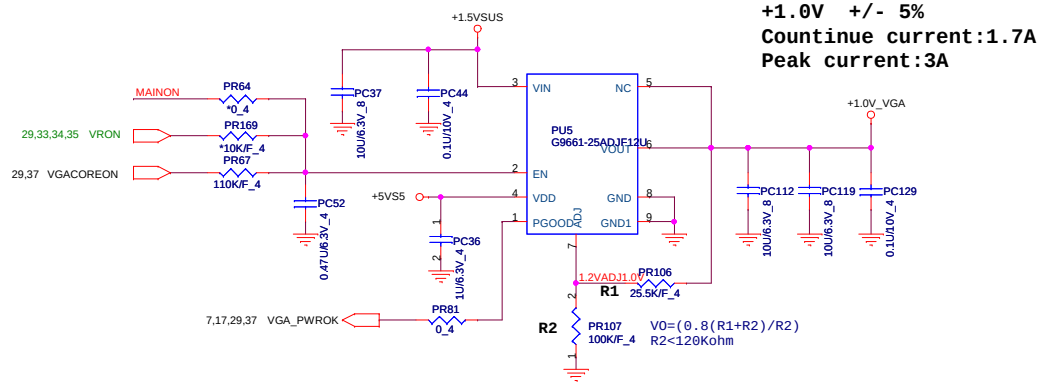
PROJECT : R23
Quanta Computer Inc.

Size	Document Number	Rev
C	+1.1V VTT / PCH	1A
NB5/RD2	Date: Friday, January 28, 2011	Sheet 35 of 40



SG & Discrete Only





PROJECT : R23
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 (RT8207)	1A

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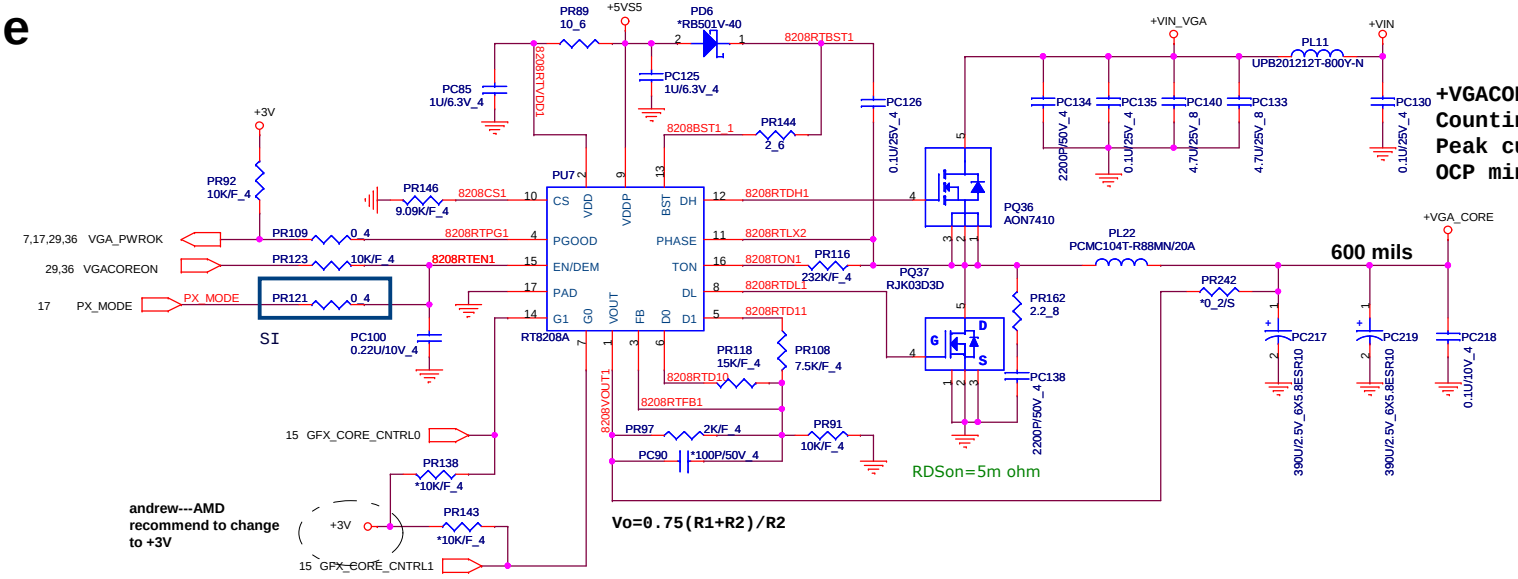
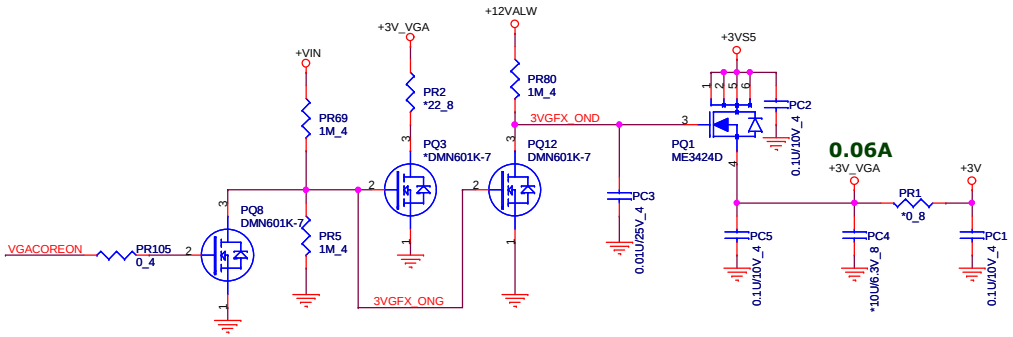
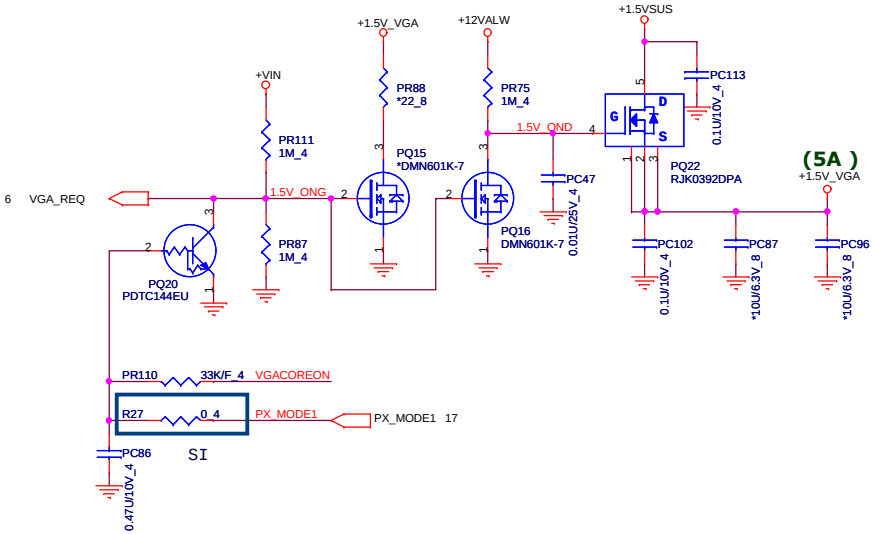
VGA Core



Seymour-XT	PWRCNTL0	PWRCNTL1	V-CORE
L	0	0	0.9V
M	0	1	1V
H	1	0	1.1V (Default)
TBD	1	1	NA





PROJECT : R23
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VGACORE (RT8208/1.8V)	1A

Date: Friday, January 28, 2011 Sheet 37 of 40

Do Not add test pad on BATDIS_G signal

To PWR LED

Place this ZVS close to Diode away +VIN

Place this ZVS close to Far-Far away +VIN

Place this cap close to EC

Place this cap close to EC

Place this cap close to EC

Place this cap close to EC

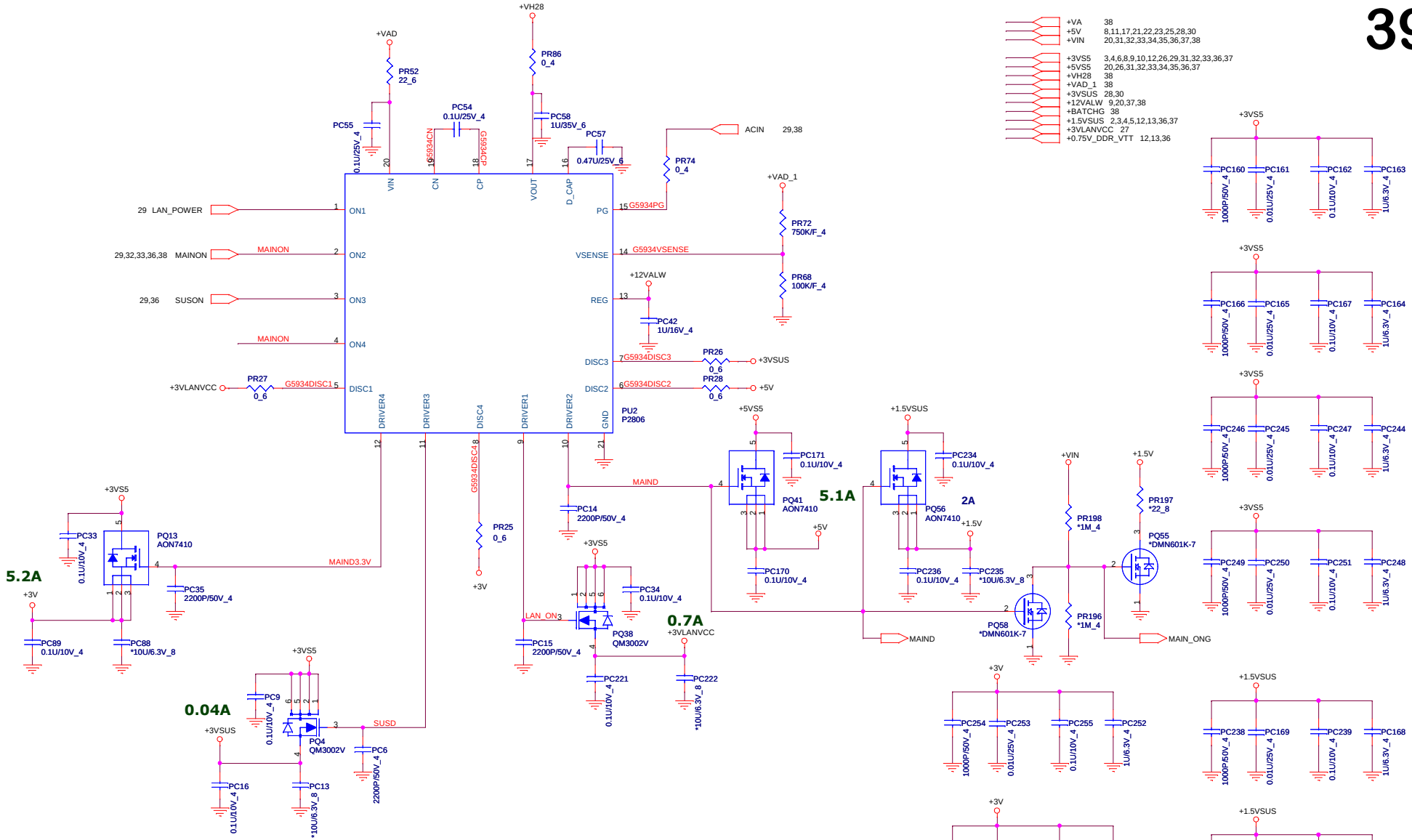
PU9
OZ8681

+VA
+VH28 39
+VAD_1 39
+3VPCU 4,7,26,28,29,31
+5VPCU 4,29,31,32
+BATCHG

PROJECT : R23
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Charger (OZ8681)	1A

Date: Friday, January 28, 2011 Sheet 38 of 40



PROJECT : R23
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Dis-charge IC (G5934)	1A

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