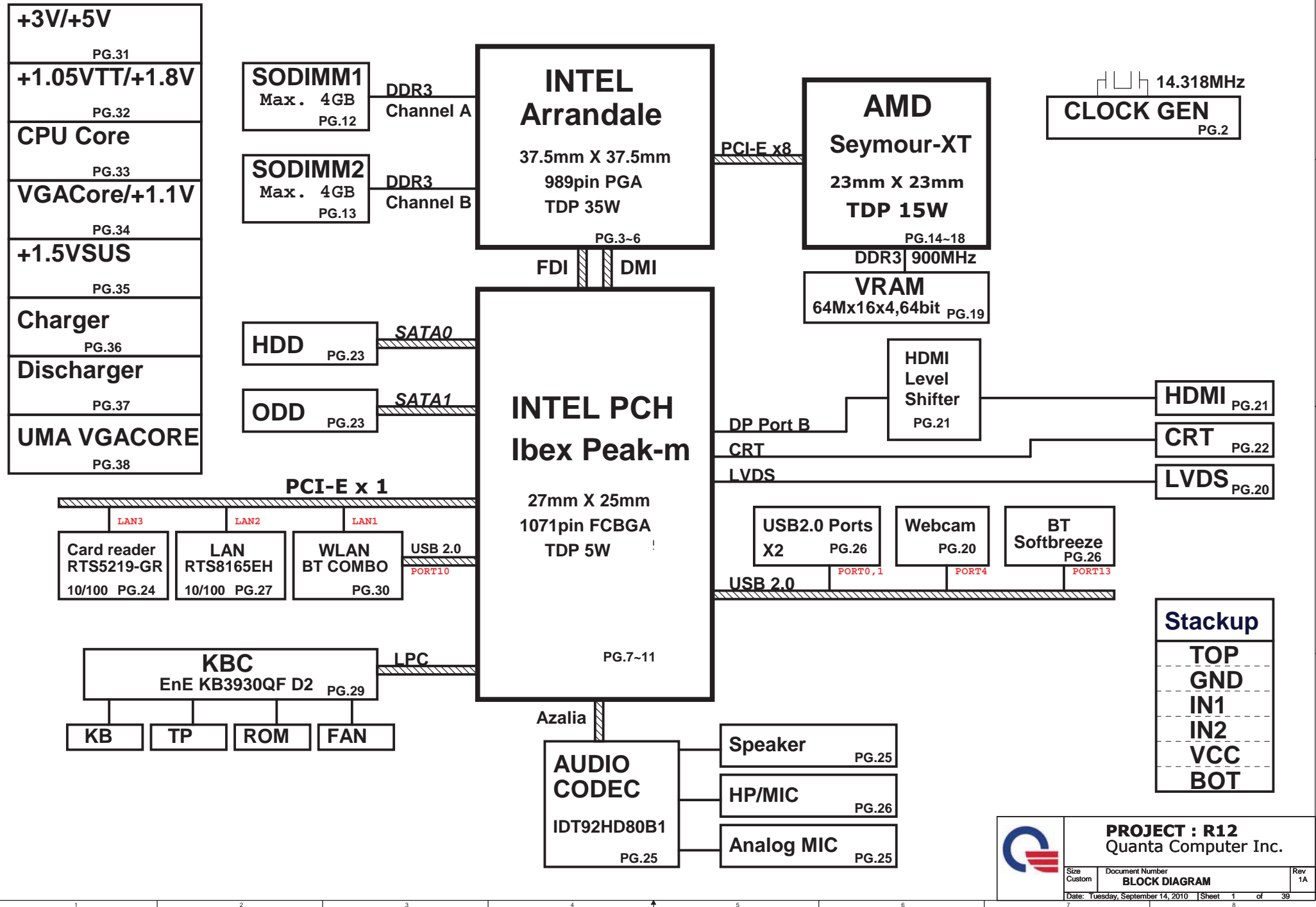
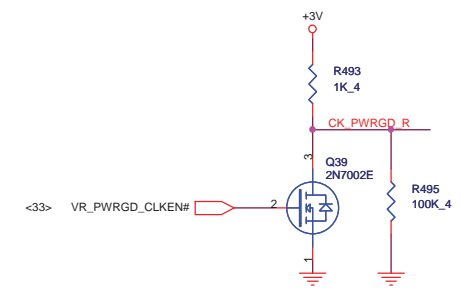
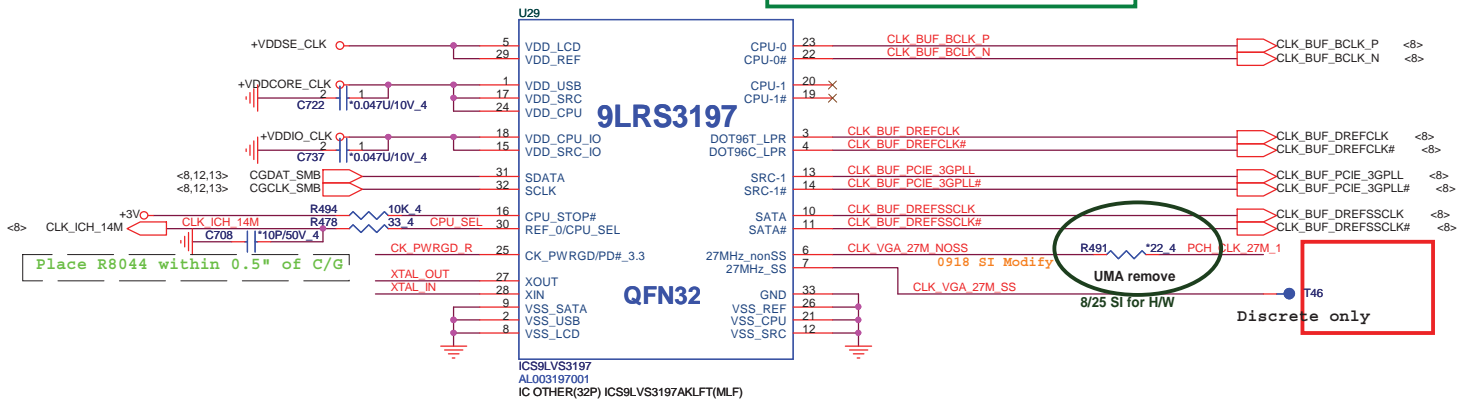
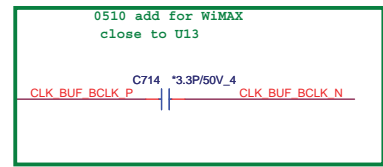
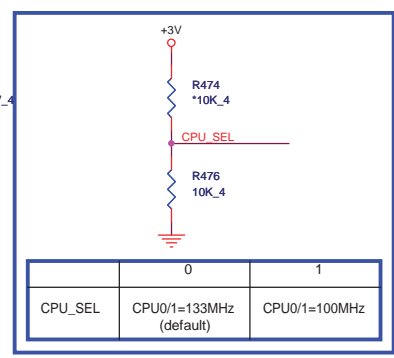
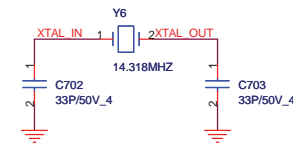
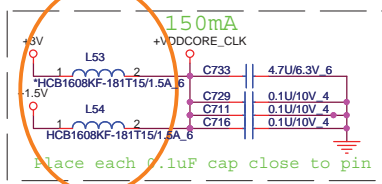
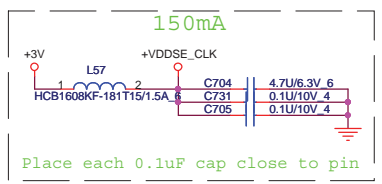
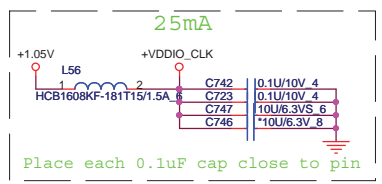


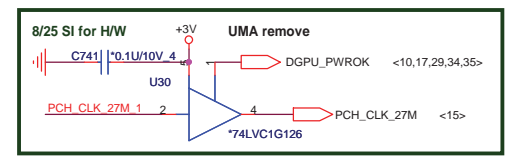
R12 INTEL UMA/DISCRETE SYSTEM DIAGRAM



PROJECT : R12
Quanta Computer Inc.

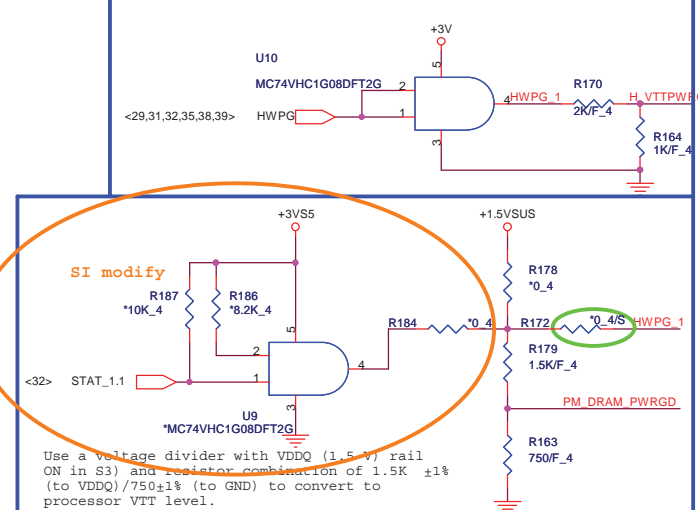
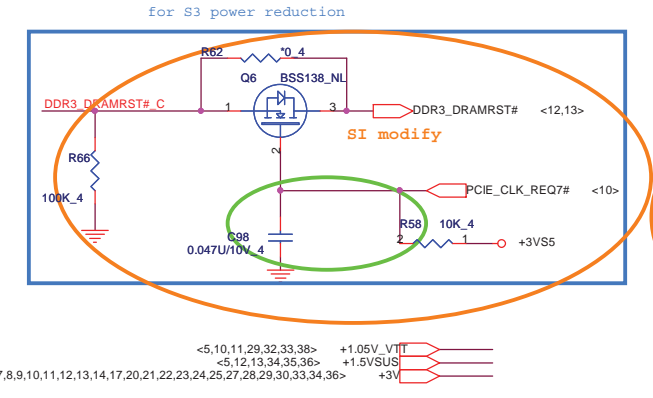
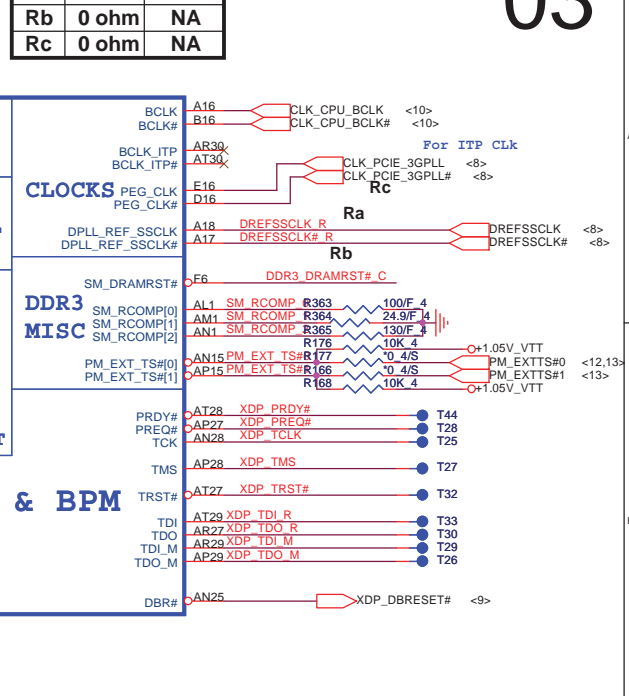
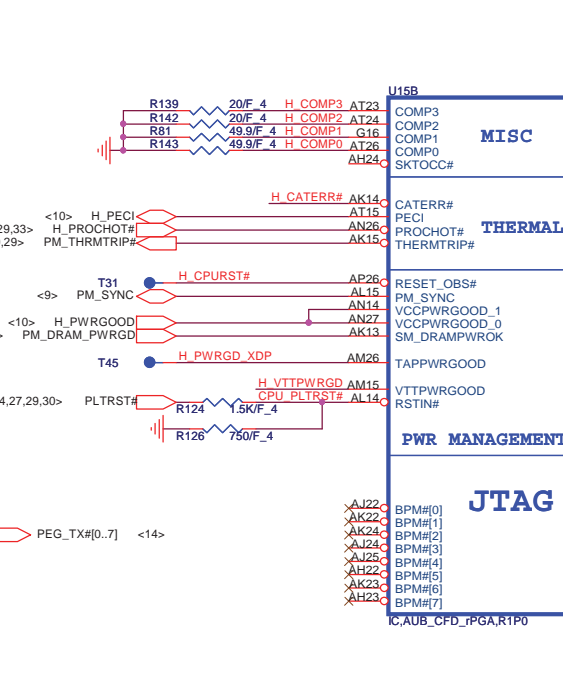
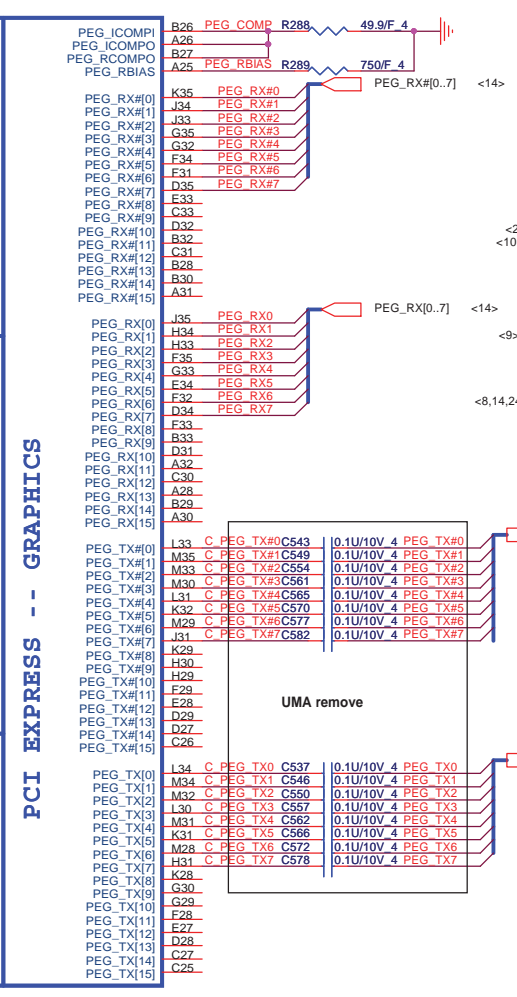
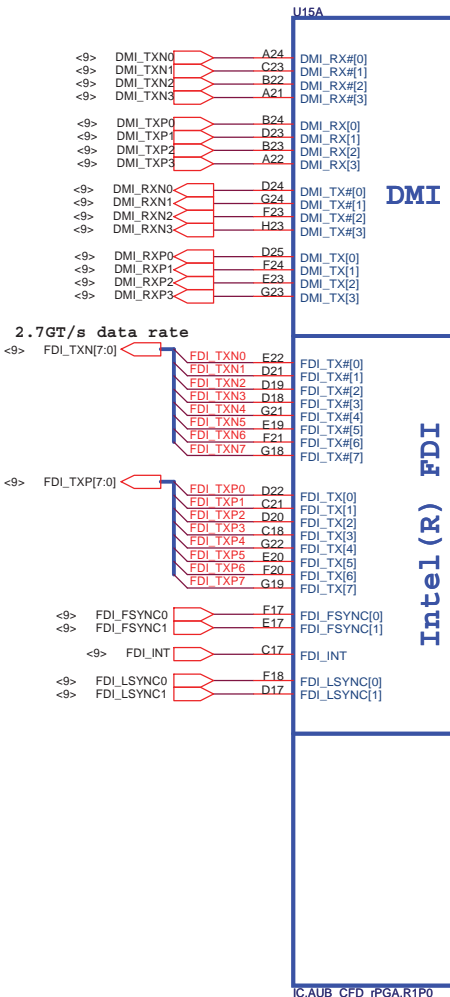


Vender	Part	Part Number	Part Description
ICS	ICS9LVS3197	AL003197000	IC OTHER(32P) ICS9LVS3197AKLFT(MLF)
Realtek	RTM890N-632	AL000890000	IC OTHER(32P) RTM890N-632-GRT(QFN)
Silego	SLG8LV595VTR	AL000595000	IC OTHER(32P)SLG8LV595VTR(QFN)



+1.05V <7,8,9,11,39>
 +1.5V <5,30>
 +3V <3,7,8,9,10,11,12,13,14,17,20,21,22,23,24,25,27,28,29,30,33,34,36>

	DIS	UMA
Ra	NA	0 ohm
Rb	0 ohm	NA
Rc	0 ohm	NA

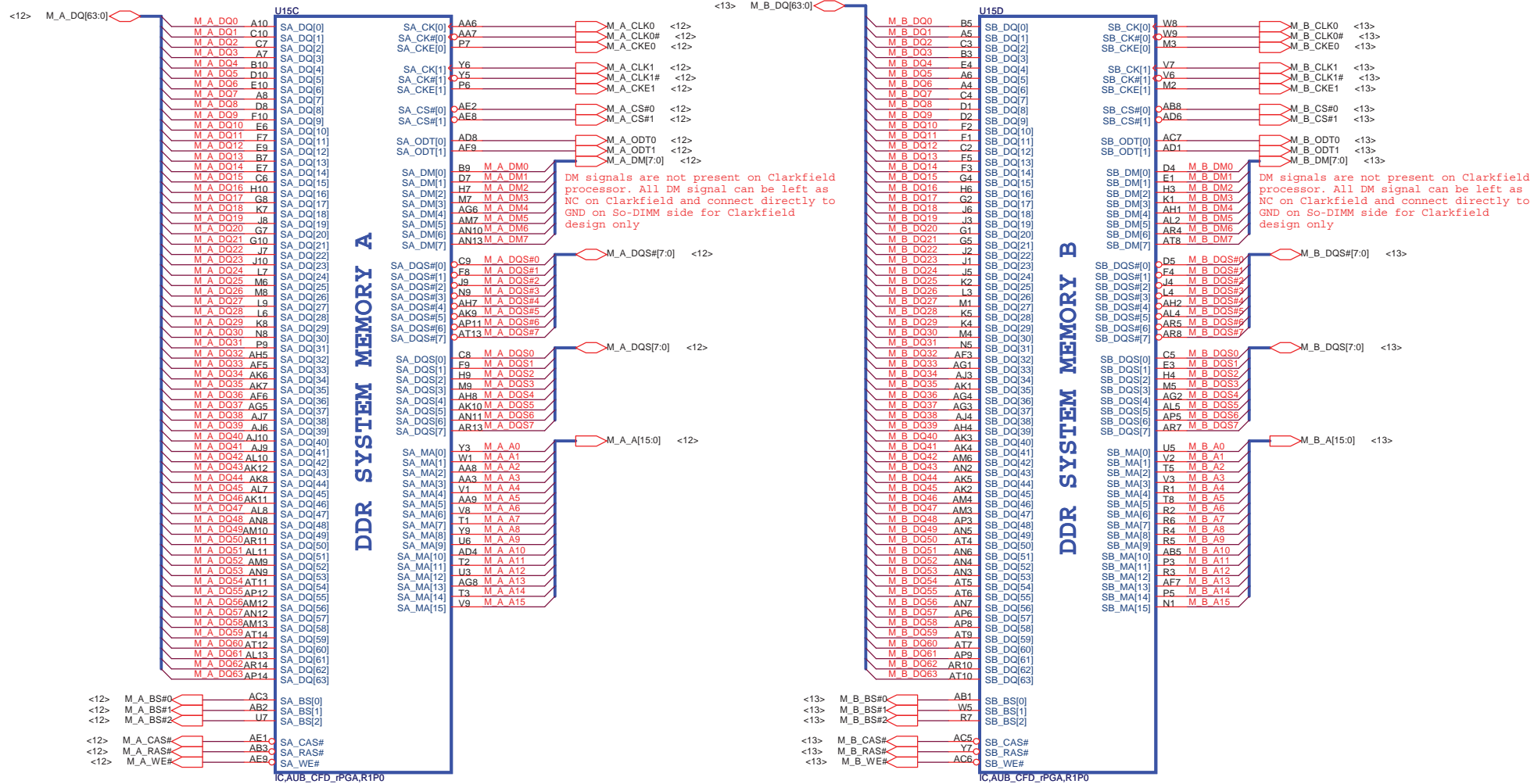


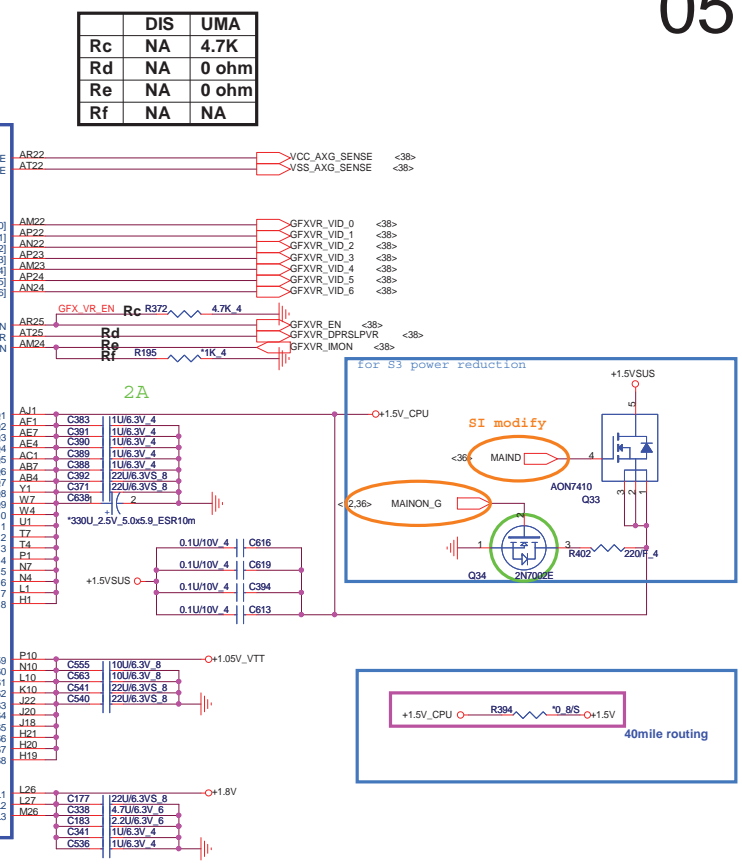
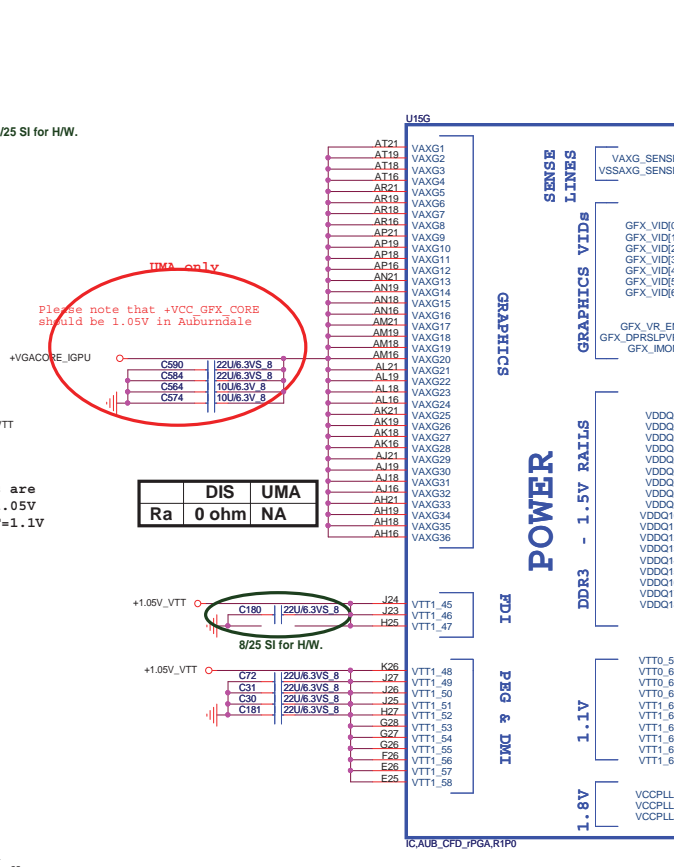
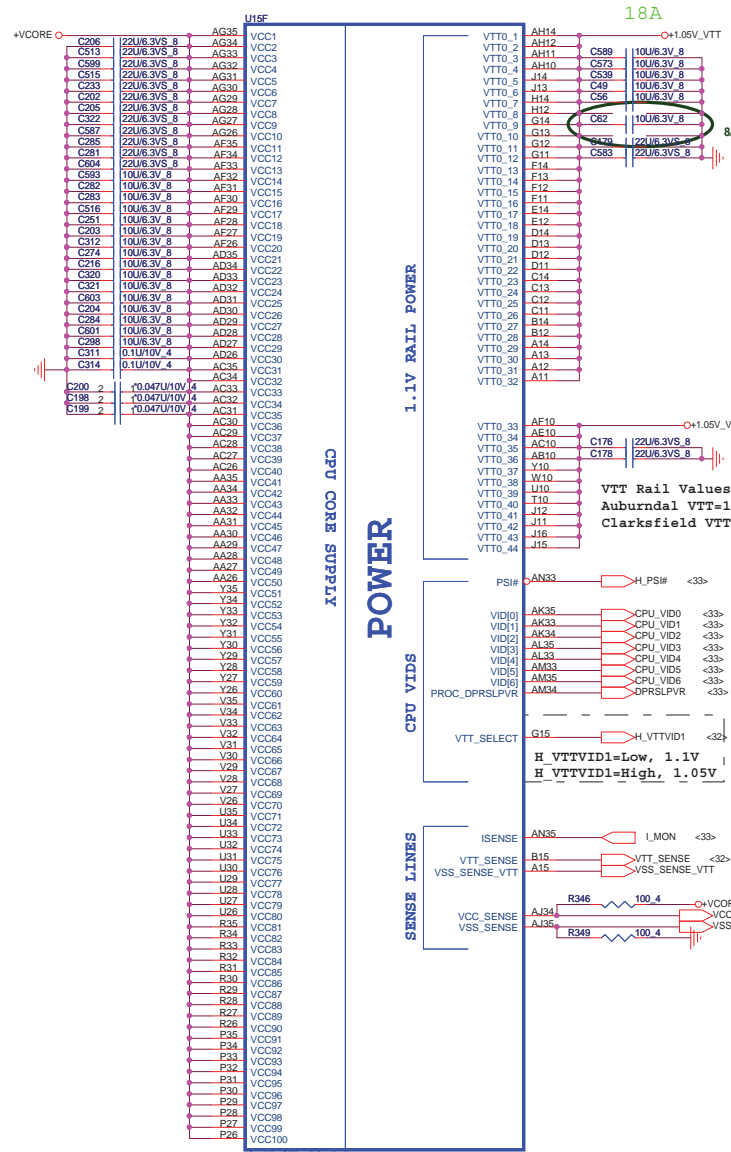
Scan Chain (Default)	STUFF -> Ra, Rc, Re NO STUFF -> Rb, Rd
CPU Only	STUFF -> Ra, Rb NO STUFF -> Rc, Rd, Re
GMCH Only	STUFF -> Rd, Re NO STUFF -> Ra, Rb, Rc

PROJECT : R12
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
	PROCESSOR 1/4(HOST&PEX)	
Date: Sunday, September 19, 2010	Sheet 3 of 39	

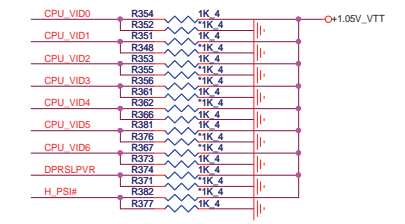
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)





	DIS	UMA
Rc	NA	4.7K
Rd	NA	0 ohm
Re	NA	0 ohm
Rf	NA	NA

DIS	UMA
0 ohm	NA

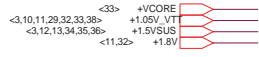


HFM_VID : Max 1.4V
LFM_VID : Min 0.65V



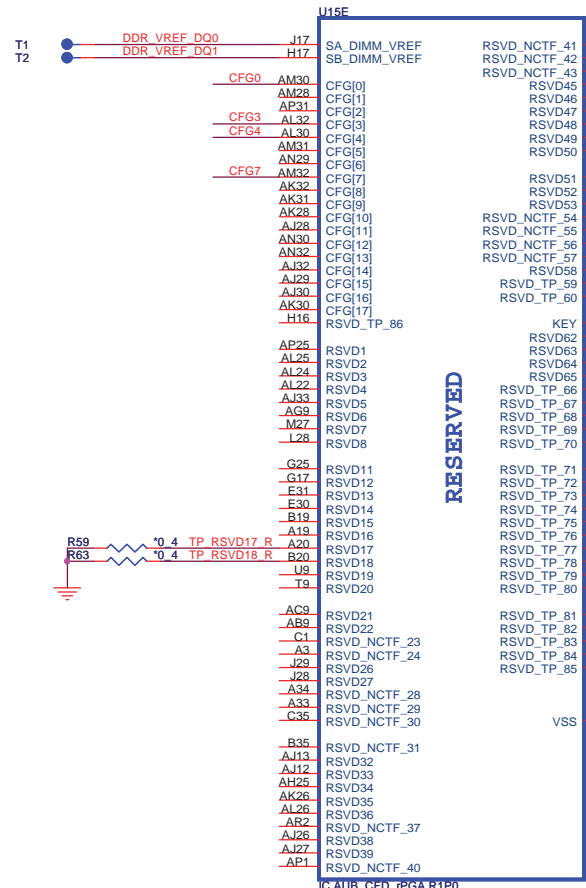
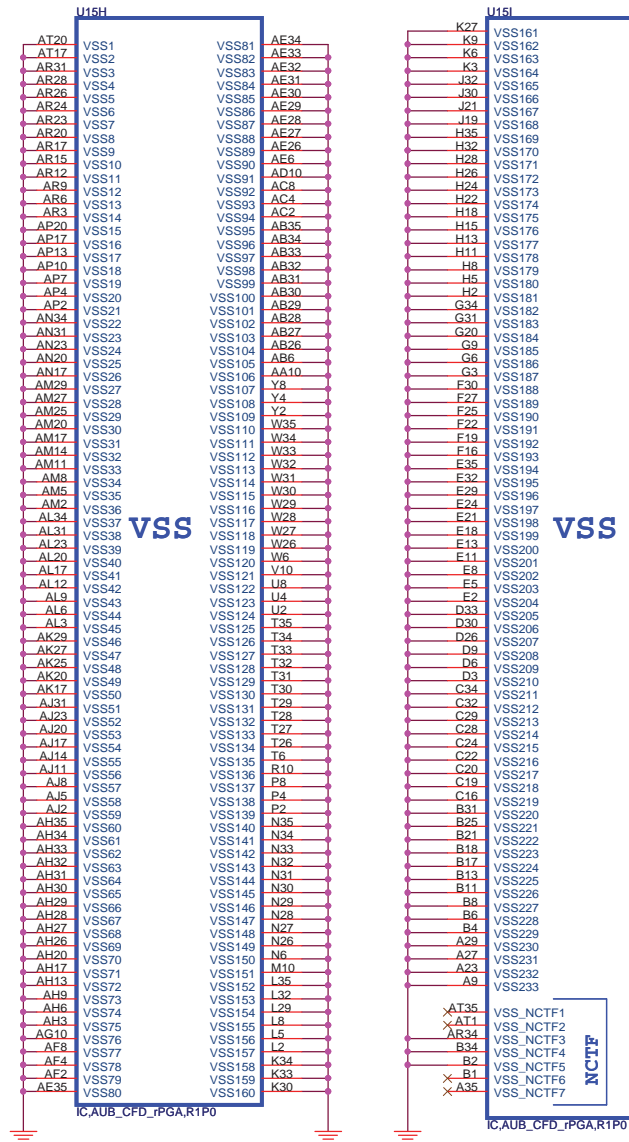
PROJECT : R12
Quanta Computer Inc.

Size Custom	Document Number PROCESSOR 3/4(POWER)	Rev 1A
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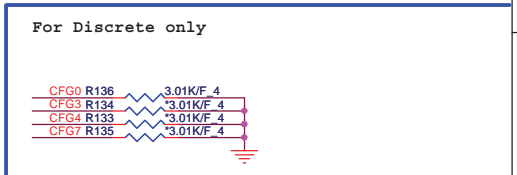
AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0, 14 -> 1



For Discrete only

CFG[1:0] - PCI_Epress Configuration Select
 * 11= 1 x 16 PEG
 * 10= 2 x 8 PEG

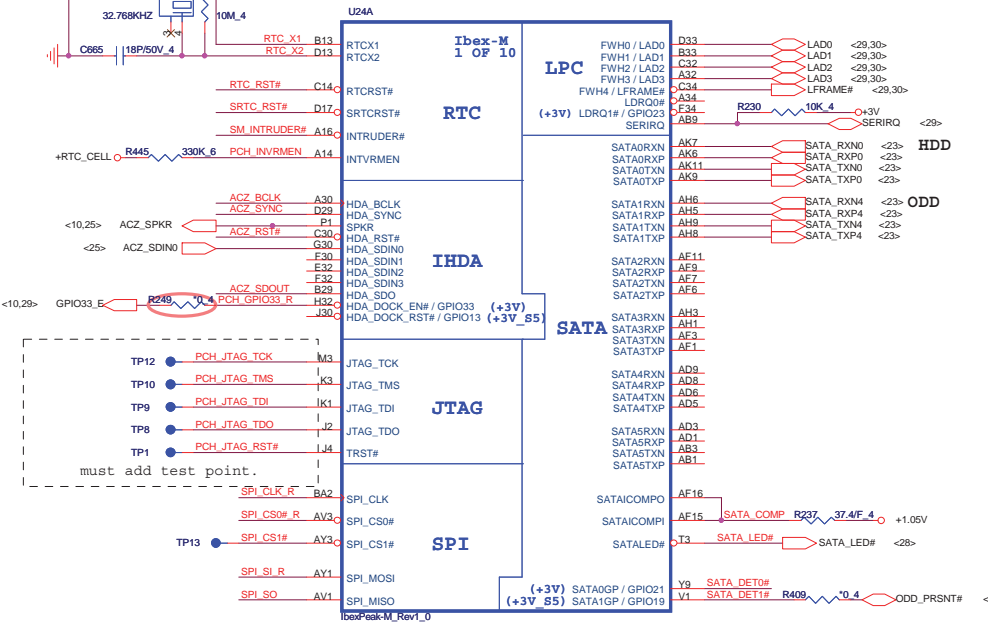
PROJECT : R12
Quanta Computer Inc.

Size Custom Document Number
PROCESSOR 4/4 (GND)

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INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

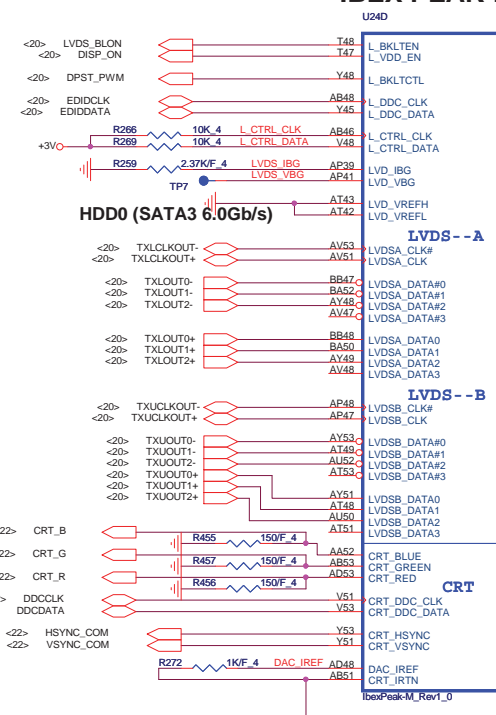
IBEX PEAK-M (HDA,JTAG,SATA)



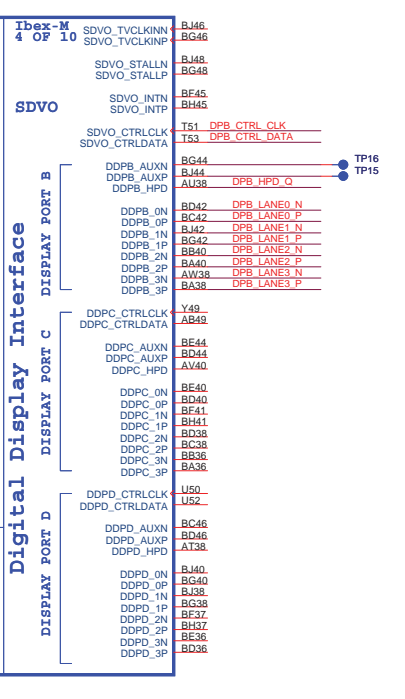
1205 The SATALED# signal is open-collector and requires a weak external pull-up (8.2 k to 10 k) to +V3.3.



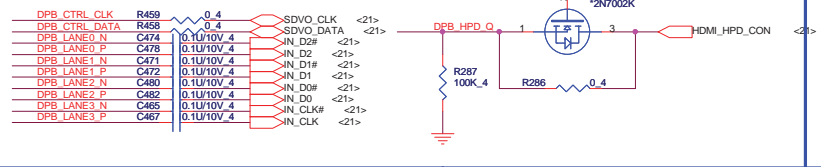
UMA CRT, LVDS&HDMI signals



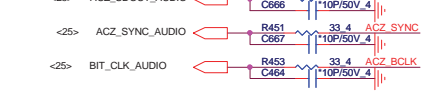
IBEX PEAK-M (LVDS,DDI)



UMA HDMI signals

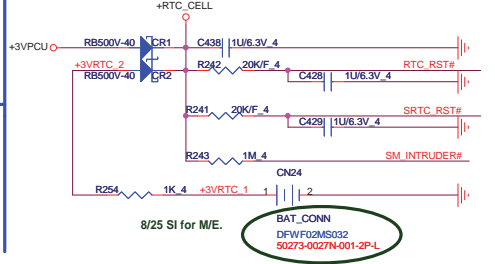


For AUDIO

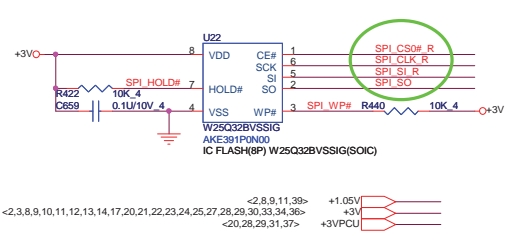


For MDC

RTC



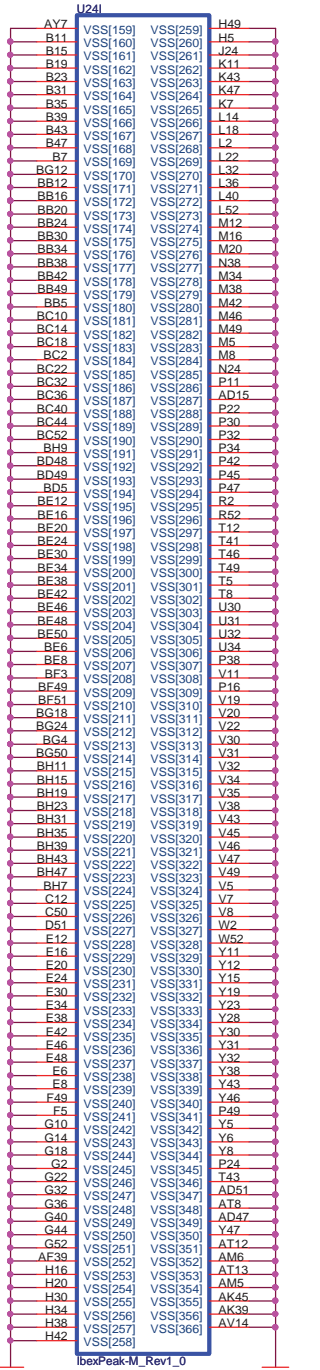
4M byte SPI ROM



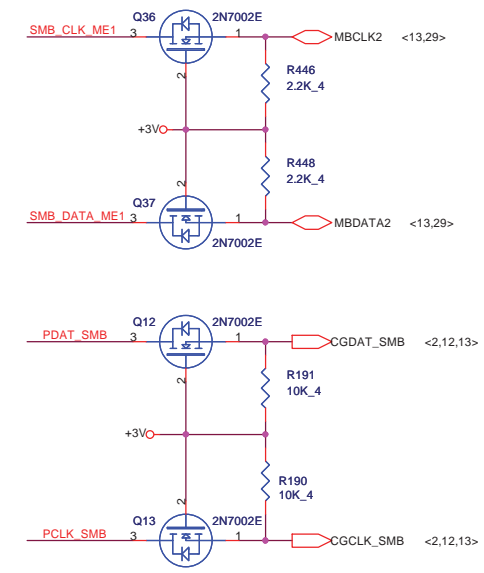
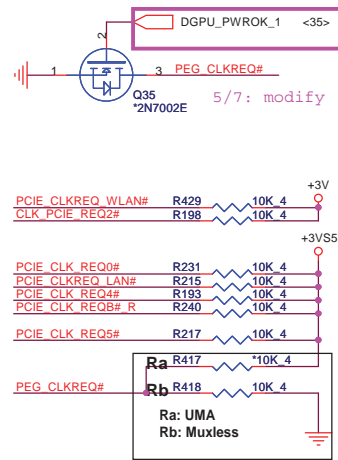
Vender
 Socket DG008000031
 EON - EN25F32-100HIP
 AKE39FN0Q00 IC FLASH(8P) EN25F32-100HIP (SOIC)
 WINBOND - W25Q32BVSSIG
 AKE391P0N00 IC FLASH(8P) W25Q32BVSSIG(SOIC)

PROJECT : R12
Quanta Computer Inc.

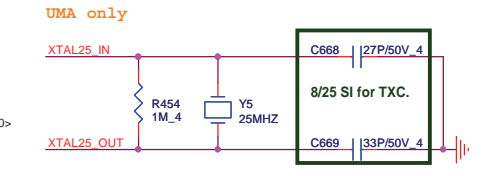
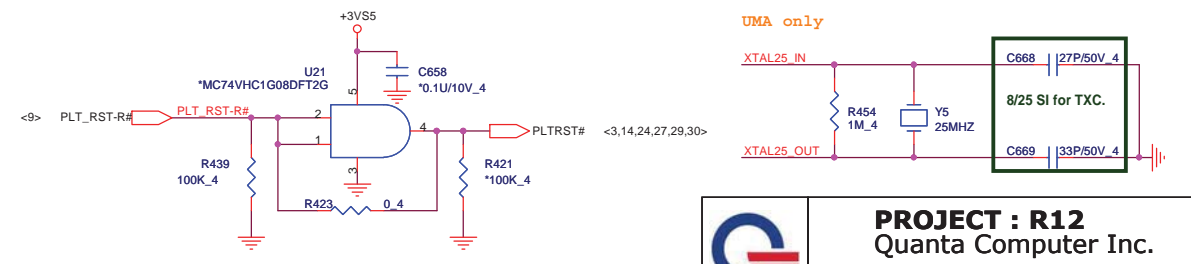
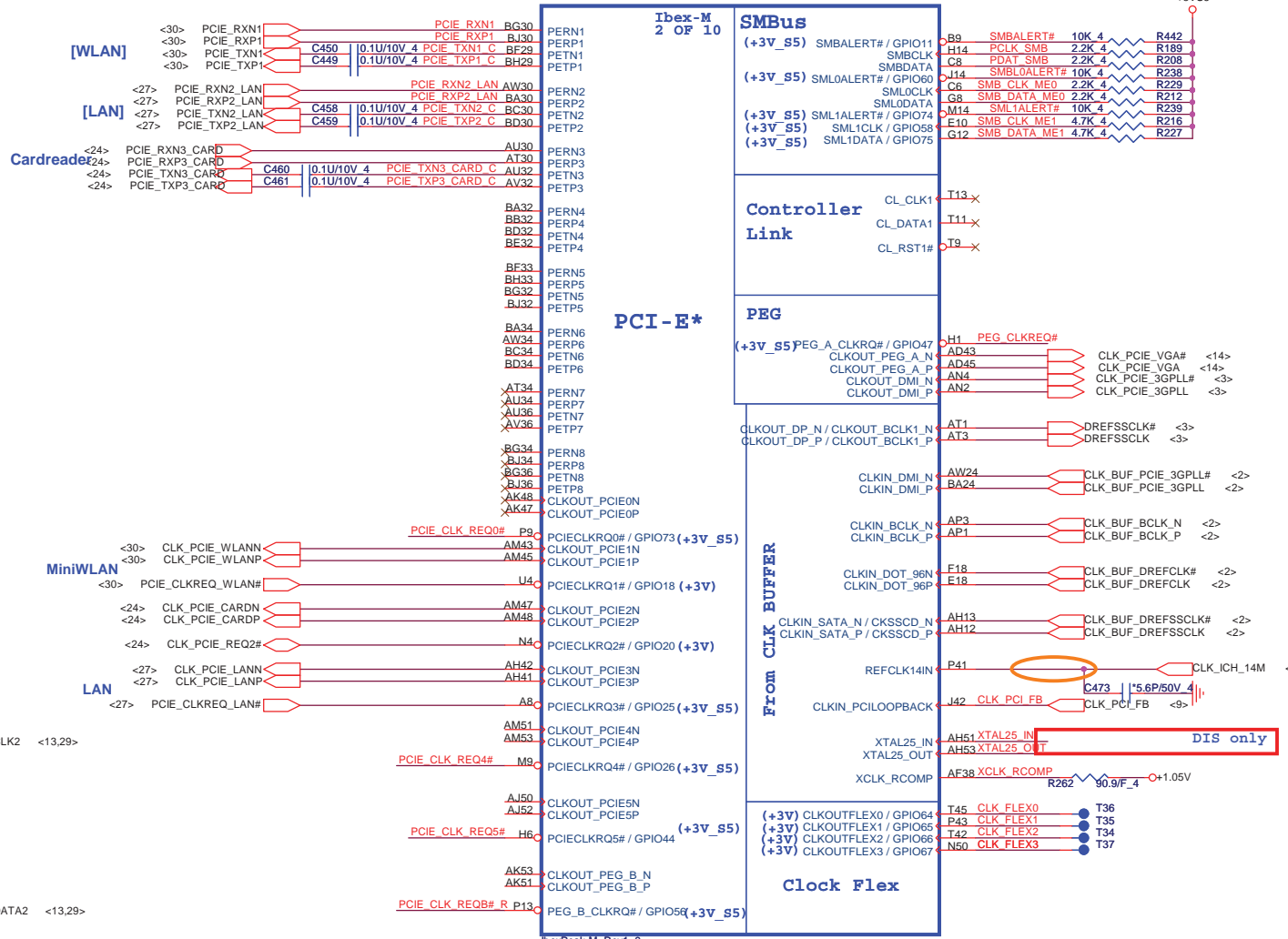
Size Custom Document Number **PCH 1/5 (SATA,HDA,LPC)** Rev 1A
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PEG Clock detect (SG only)



IBEX PEAK-M (PCI-E,SMBUS,CLK)

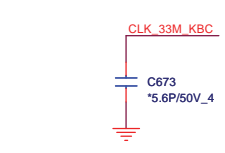
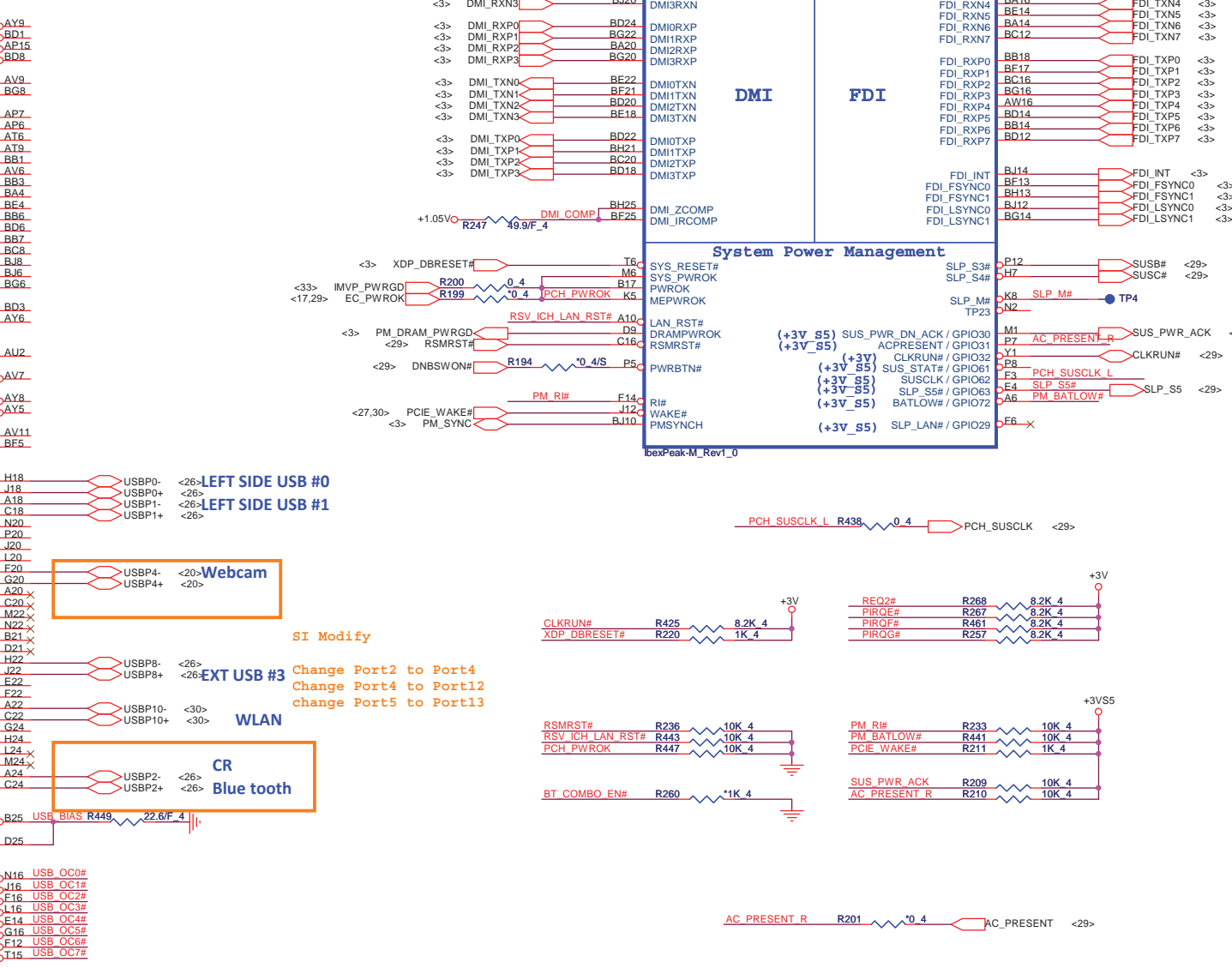
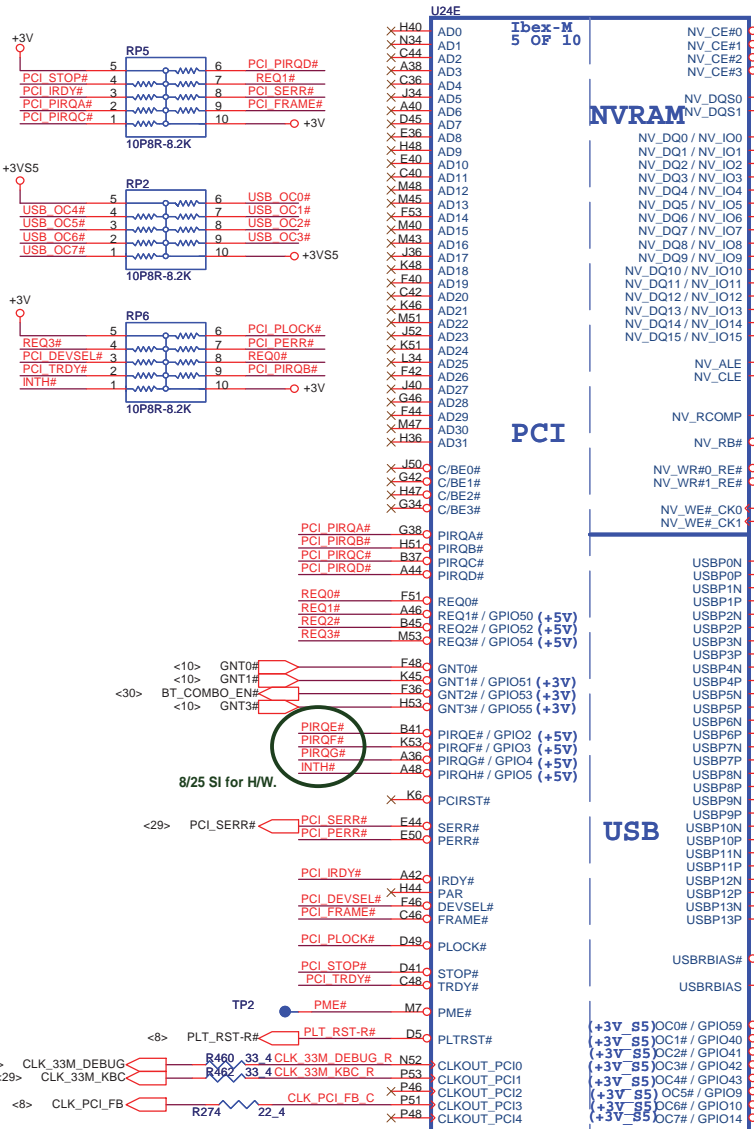


PROJECT : R12
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Size Custom	Document Number PCH 2/5 (PCI-E, SMBUS, CK)	Rev 1A
Date: Sunday, September 19, 2010 Sheet 8 of 39		

IBEX PEAK-M (DMI,FDI,GPIO)

IBEX PEAK-M (PCI,USB,NVRAM)



PROJECT : R12
Quanta Computer Inc.

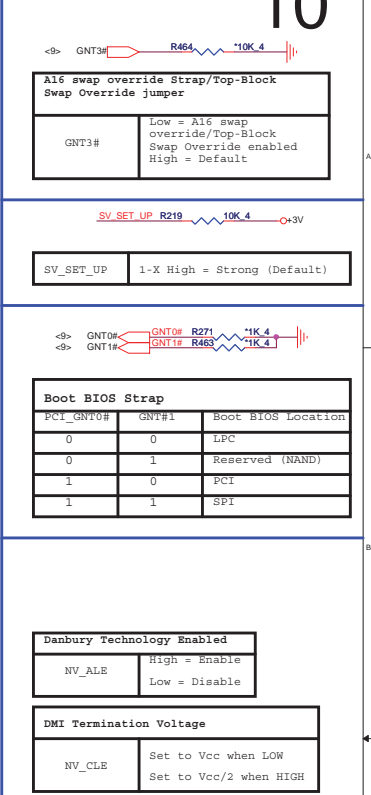
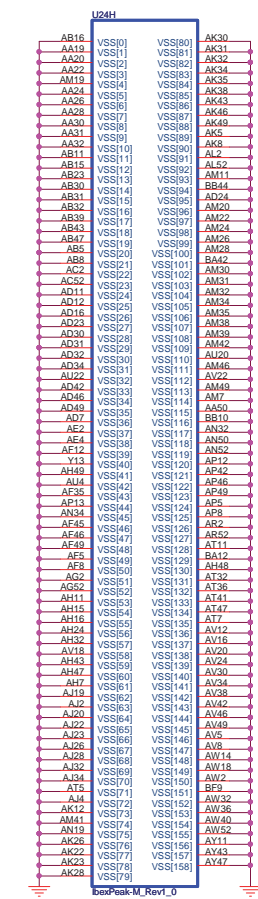
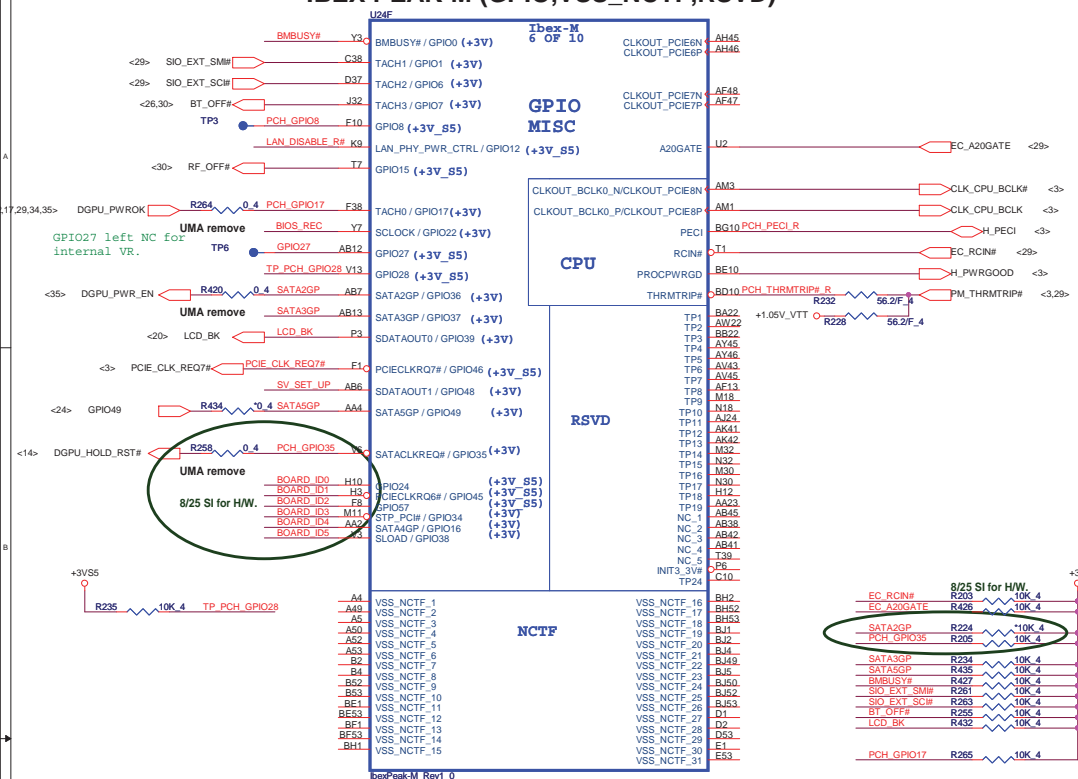
Size Custom	Document Number PCH 3/5 (PCI,ONFI,USB,DMI)	Rev 1A
Date: Sunday, September 19, 2010 Sheet 9 of 39		



IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

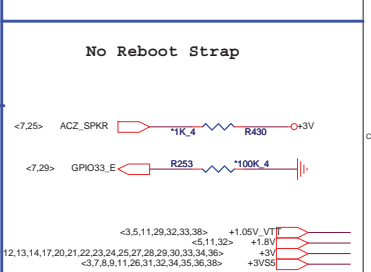
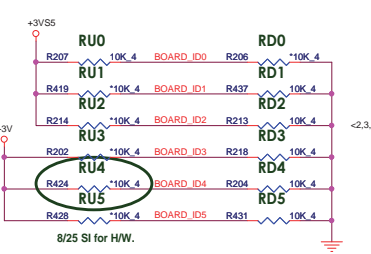
IBEX PEAK-M (GND)

10



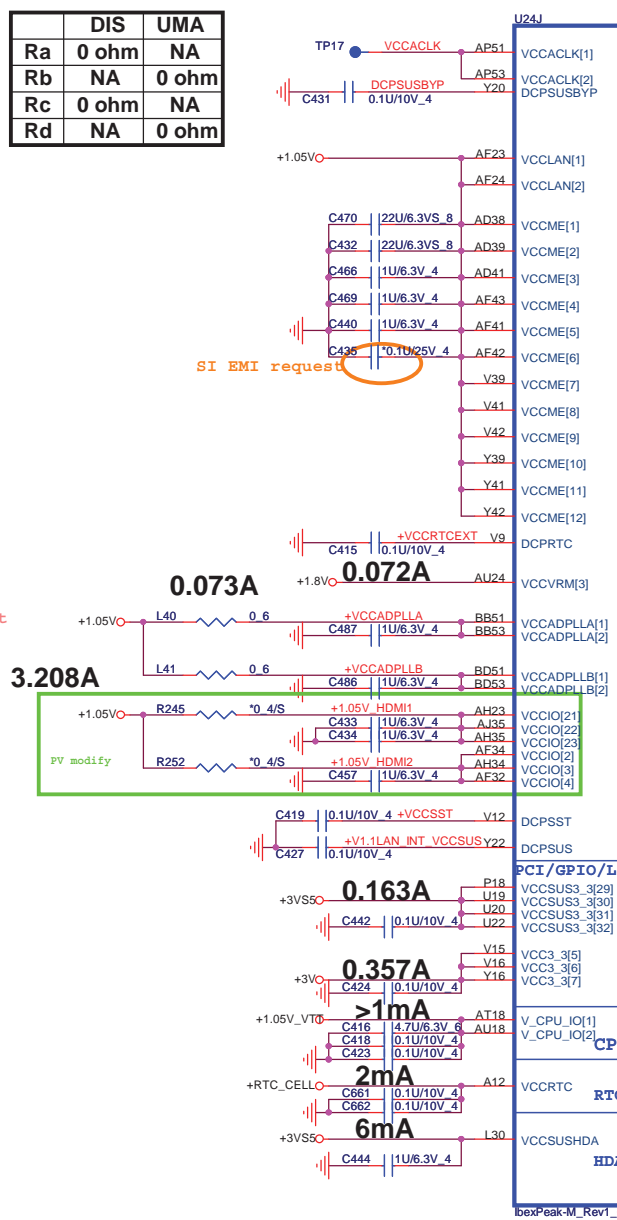
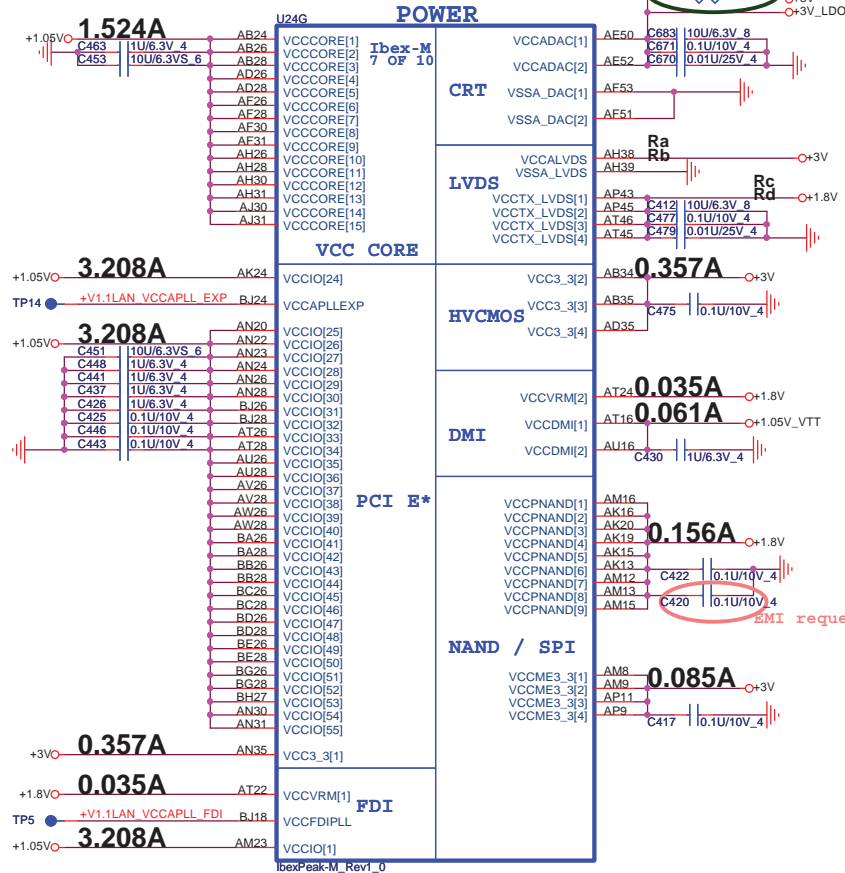
R12.MB P/N	ID0	ID1	ID2	ID3	ID4	ID5
UMA						
31R12MB0000 (PIM)	0	0	0	0	0	0
31R12MB0010 (PDT)	0	0	0	0	0	0
Seymour XT						
Hynix 512						
31R12MB0020 (PIM)	1	0	0	0	0	0
31R12MB0030 (PDT)	1	0	0	0	0	0
Samsung 512						
31R12MB0040 (PIM)	1	0	0	0	0	0
31R12MB0050 (PDT)	1	0	0	0	0	0
Hynix 1G						
31R12MB0060 (PIM)	1	0	0	0	0	0
31R12MB0070 (PDT)	1	0	0	0	0	0
Samsung 1G						
31R12MB0080 (PIM)	1	0	0	0	0	0
31R12MB0090 (PDT)	1	0	0	0	0	0

Board ID	ID0	ID1	ID2	ID3	ID4	ID5
UMA						
UMA/DIS	0=UMA 1=Dis.					
Reserve						
Reserve		0=No 1=Yes				
Reserve			0=No 1=Yes			
Reserve				0=No 1=Yes		
Reserve					0=No 1=Yes	
Reserve						0=No 1=Yes

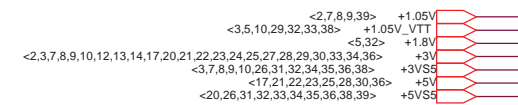
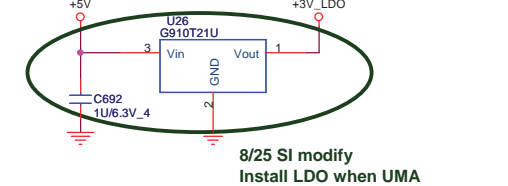


8/25 SI modify
Uninstall on UMA
Install on DIS

	DIS	UMA
Ra	0 ohm	NA
Rb	NA	0 ohm
Rc	0 ohm	NA
Rd	NA	0 ohm



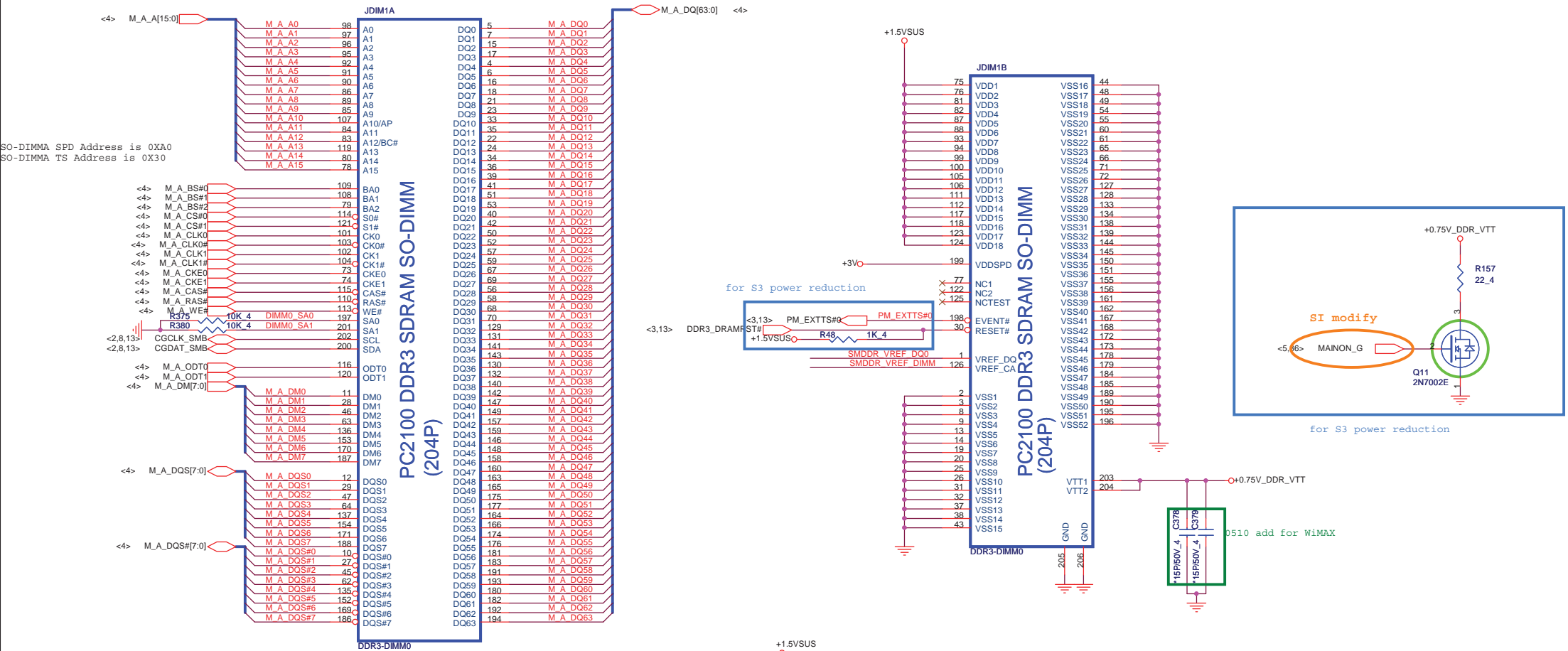
UMA Only, If have power noise issue then stuff it.



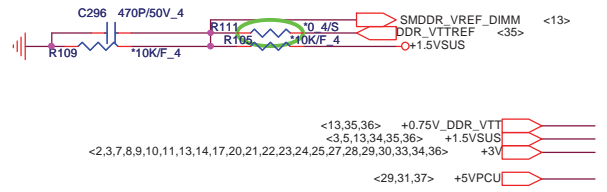
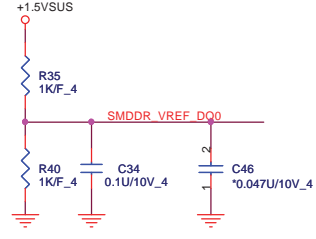
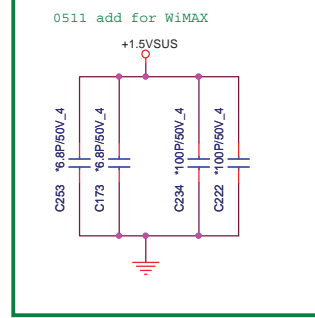
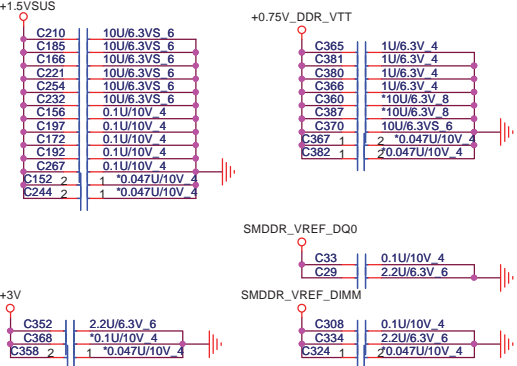
PROJECT : R12
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Size Custom Document Number **PCH 5/5 (POWER)** Rev 1A

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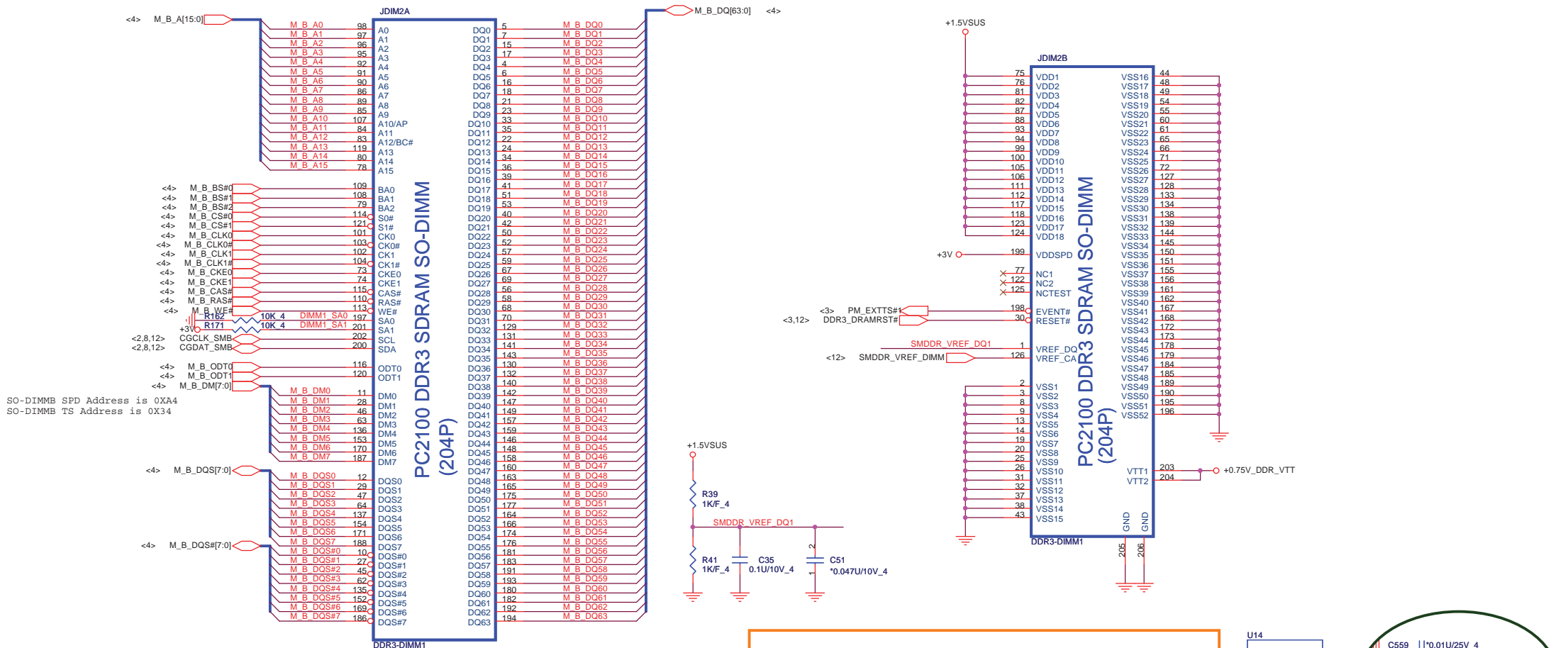


Place these Caps near So-Dimm0.
 Some Projects replace 10UF 0805 by 4.7UF 0603
 It can cost down 30%

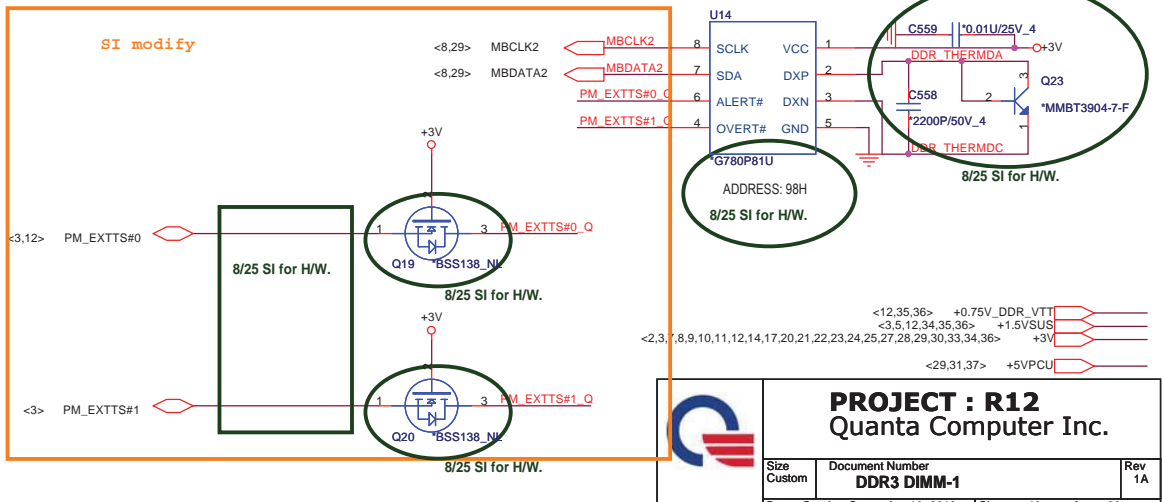
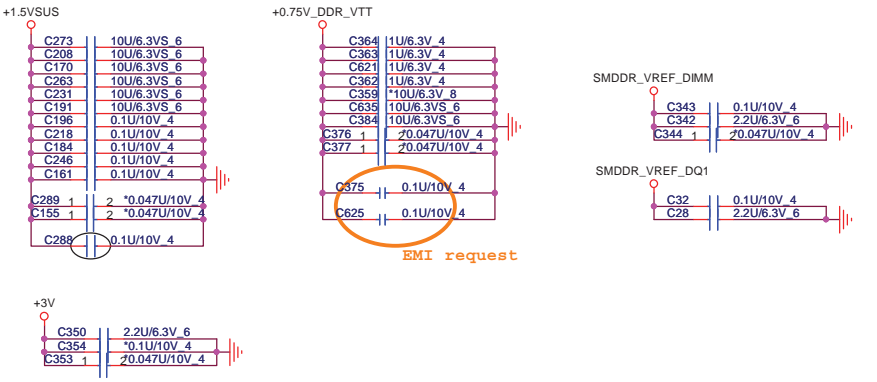


PROJECT : R12
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Size Custom	Document Number DDR3 DIMM-0	Rev 1A
Date: Sunday, September 19, 2010 Sheet 12 of 39		

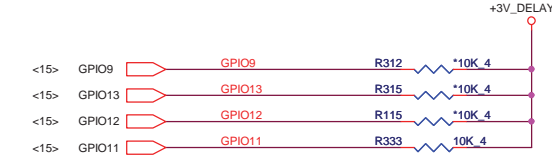
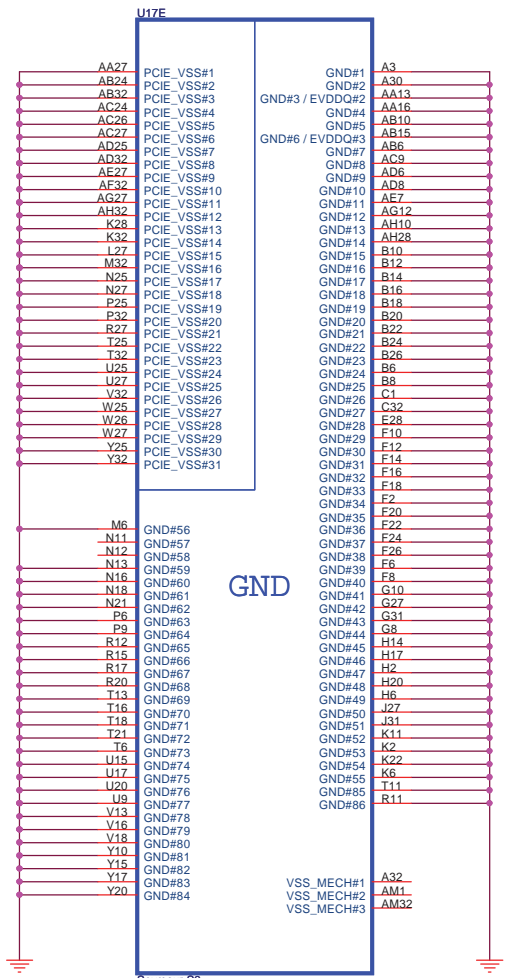


Place these Caps near So-Dimm1.
 Some Projects replace 10UF 0805 by 4.7UF 0603
 It can cost down 30%



PROJECT : R12
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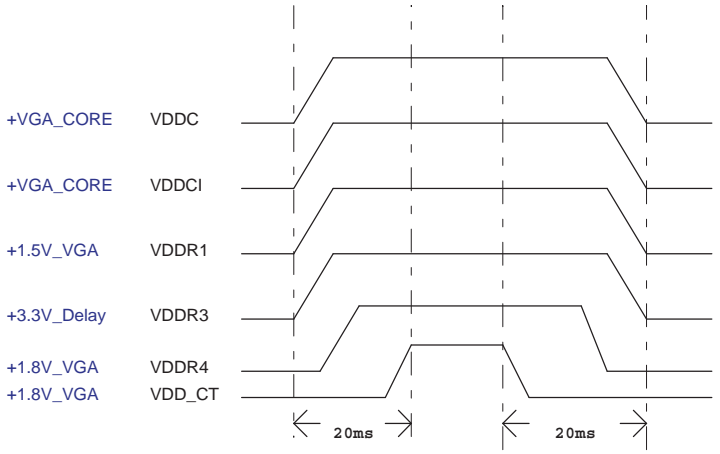
Size Custom	Document Number DDR3 DIMM-1	Rev 1A
Date: Sunday, September 19, 2010 Sheet 13 of 39		



CONFIGURATION STRAPS			RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

AMD RESERVED CONFIGURATION STRAPS		
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET		
H2SYNC	GENERICC	
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET		
GPIO21_BB_EN		

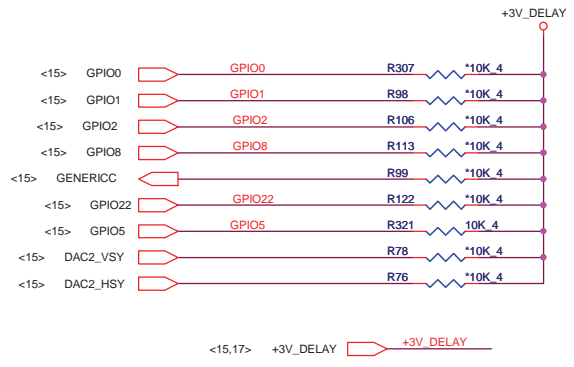
Power Up/Down Sequence



Memory Aperture size

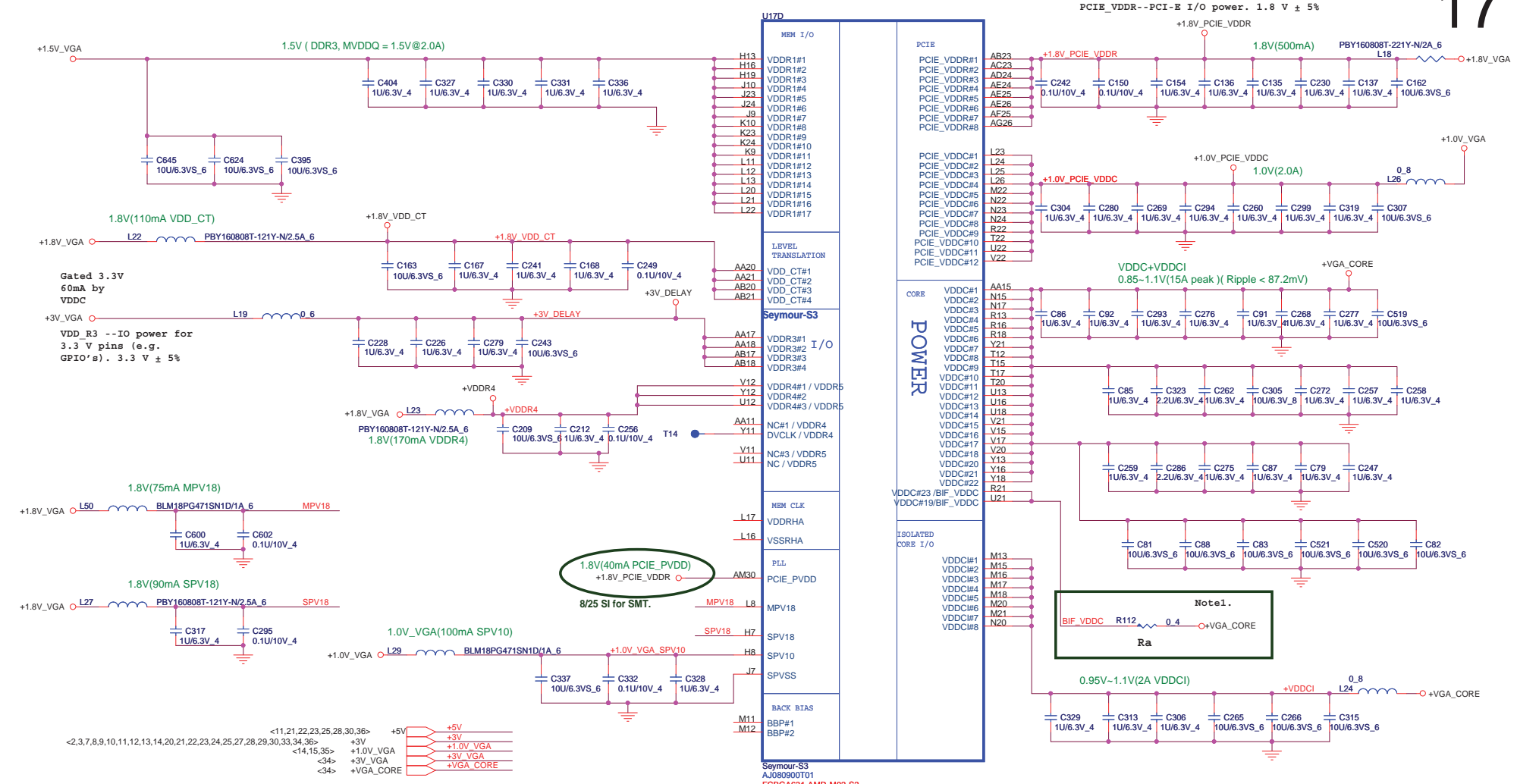
GPIO9 BIOSROM	GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0
0	256M	0	1
0	64M	0	1
0	32M	0	1
0	512M	1	0
0	1G	1	0
0	2G	1	1
0	4G	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

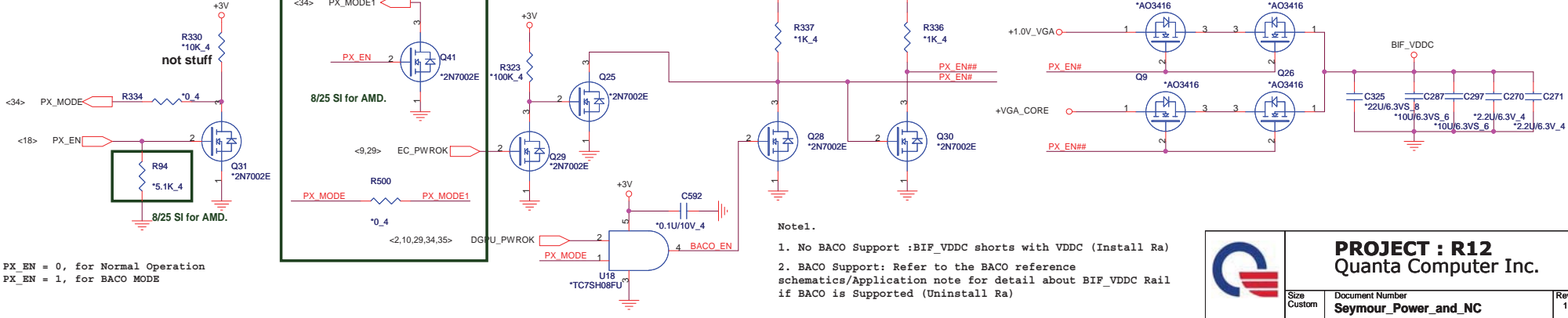


PROJECT : R12
 Quanta Computer Inc.

Size Custom	Document Number Seymour GND / LVDS / Straps	Rev 1A
Date: Sunday, September 19, 2010 Sheet 16 of 39		

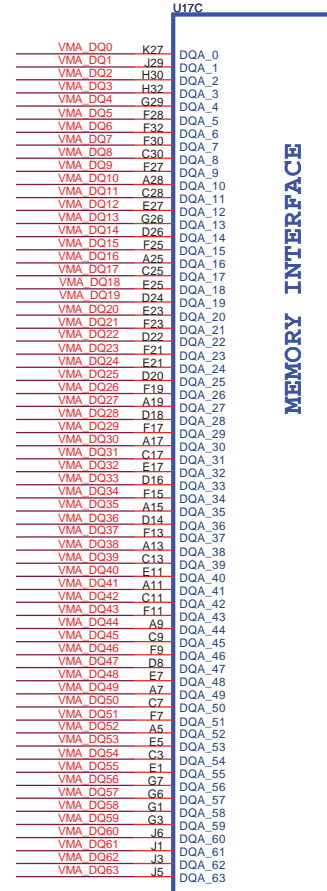
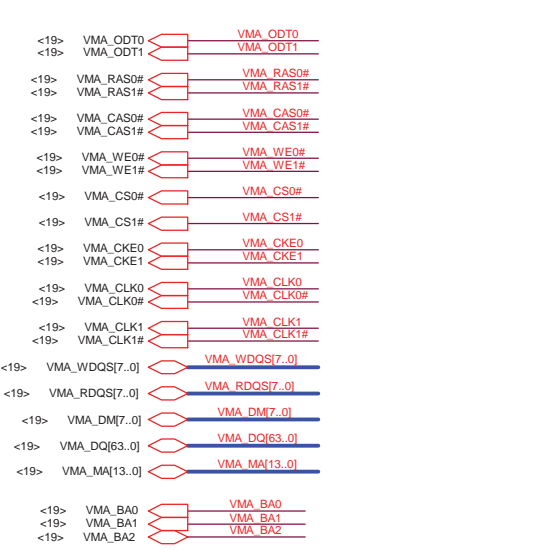


Support BACO Mode

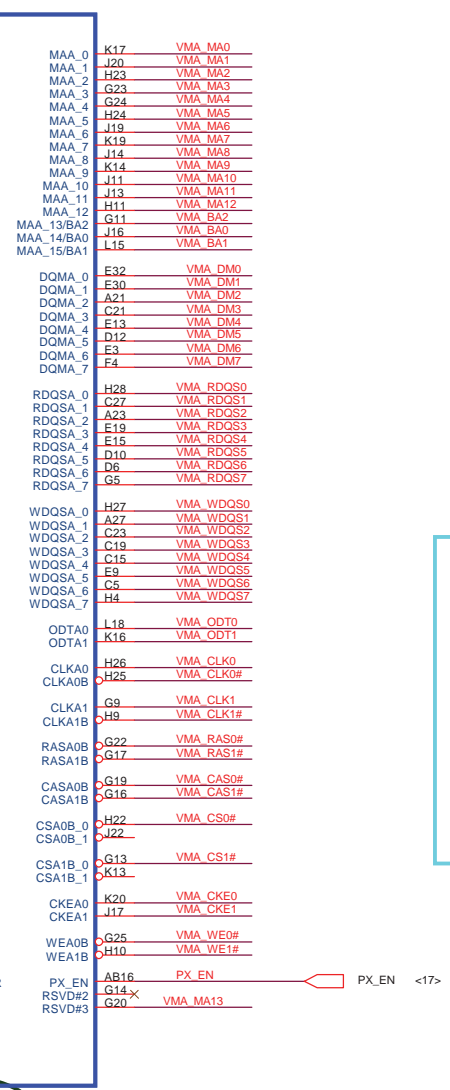


PROJECT : R12
Quanta Computer Inc.

Size Custom	Document Number Seymour_Power_and_NC	Rev 1A
Date: Sunday, September 19, 2010 Sheet 17 of 39		

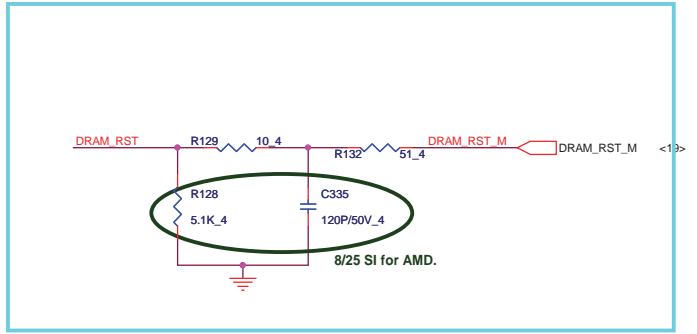
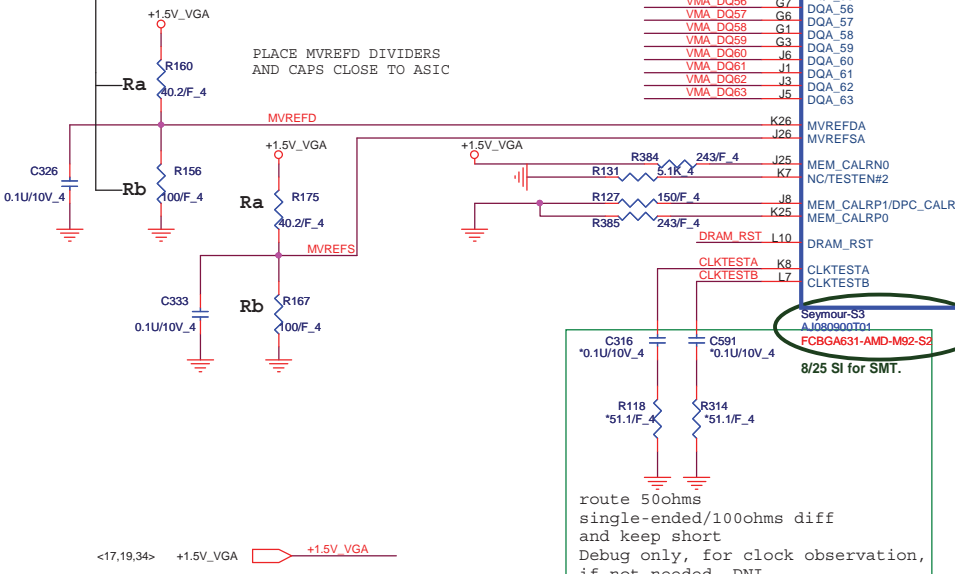


MEMORY INTERFACE



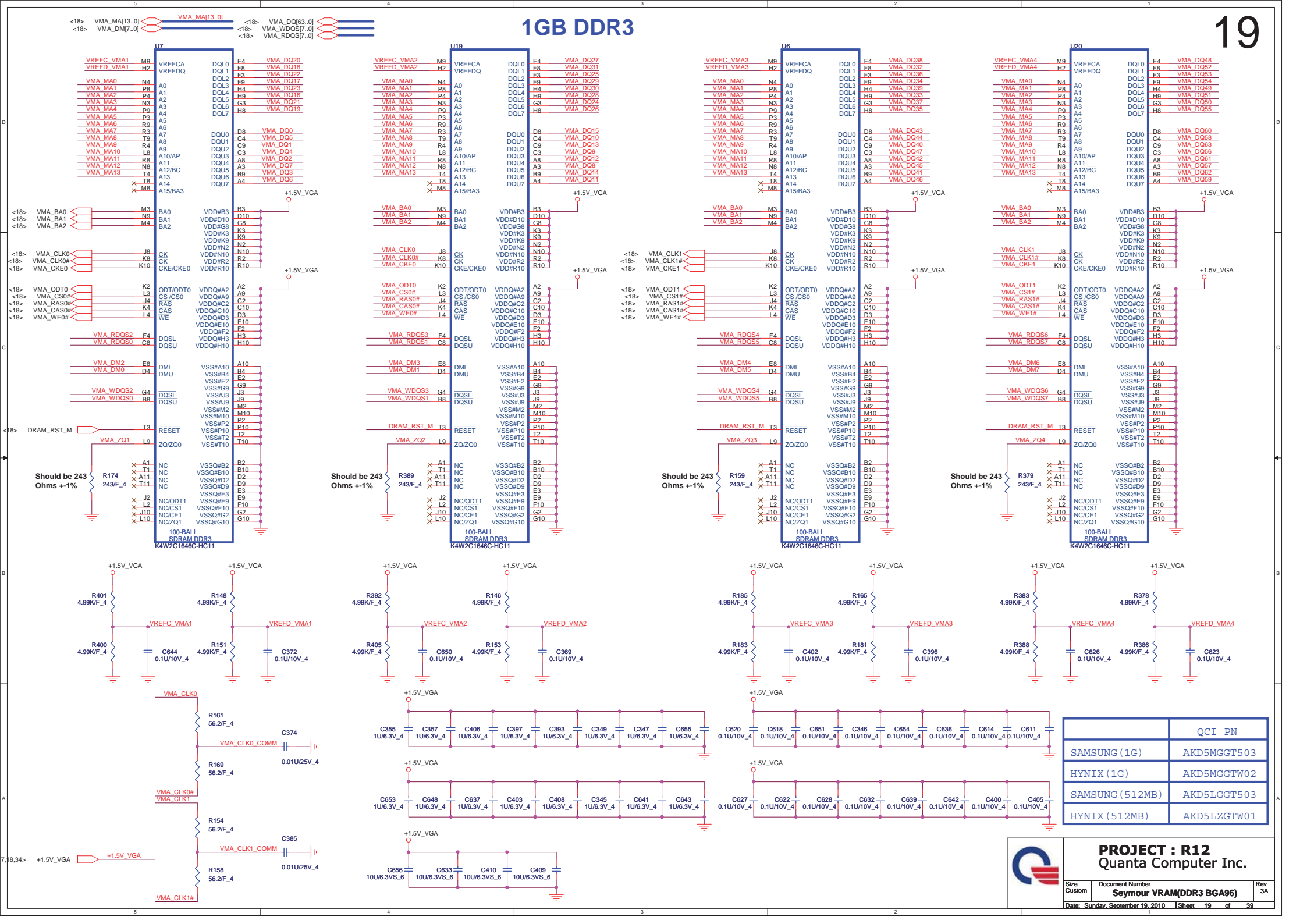
support 1Gbit
VRAM (64M X 16)

DIVIDER RESISTORS	GDDR5	DDR3
MVREF TO 1.8V (Ra)	40.2R	40.2R
MVREF TO GND (Rb)	100R	100R

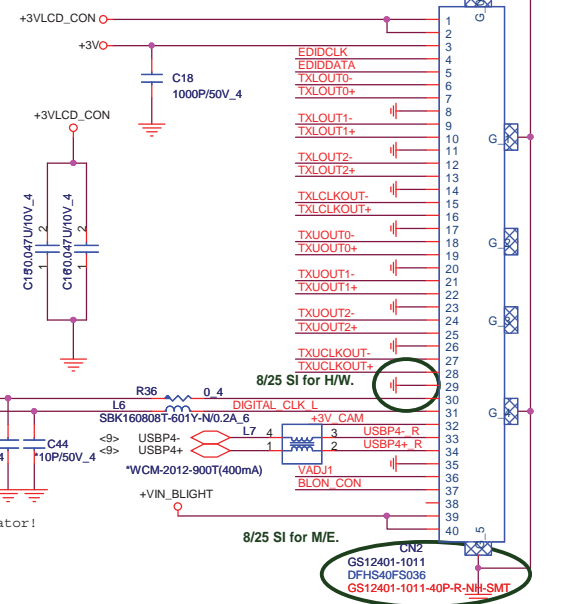
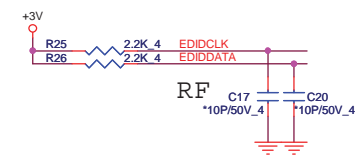
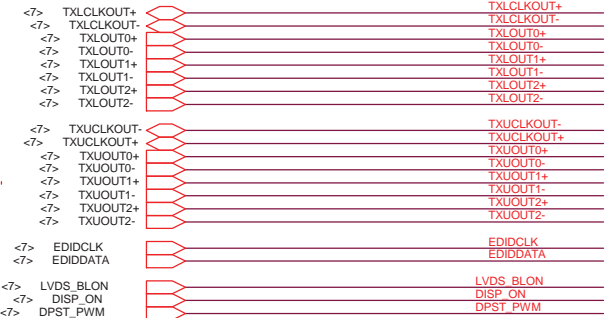
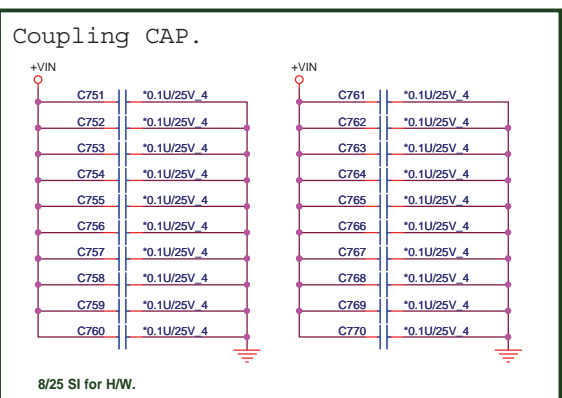
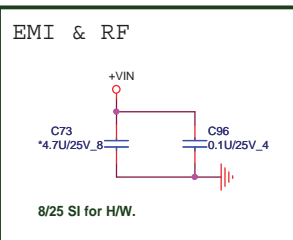
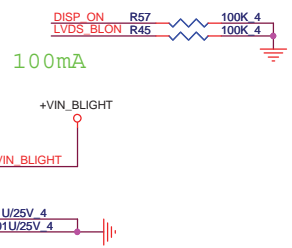
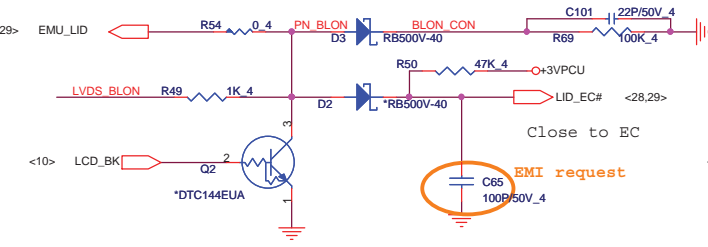


PROJECT : R12
Quanta Computer Inc.

1GB DDR3



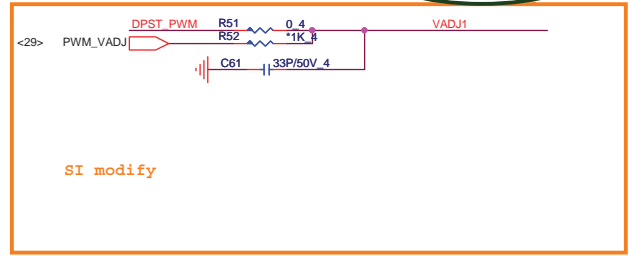
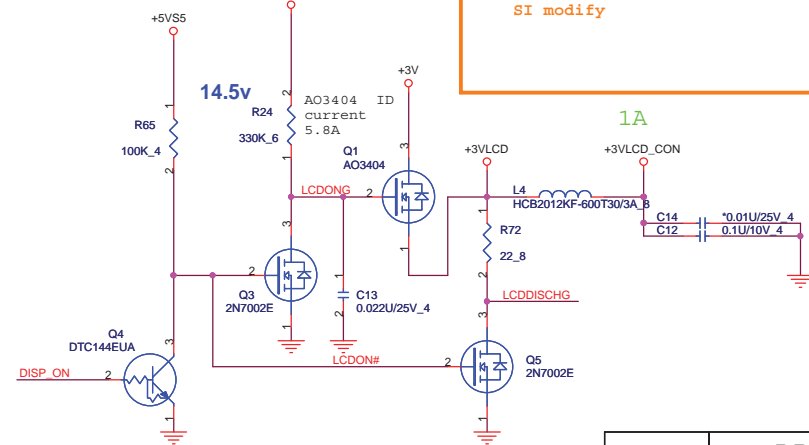
LID Switch



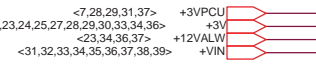
follow L4 location
 USBP4- R44 0.4 USBP4- R
 USBP4+ R46 0.4 USBP4+ R

Please note that 2011 camera is +3V as we do not need to use 5V -> 3.95V regulator!

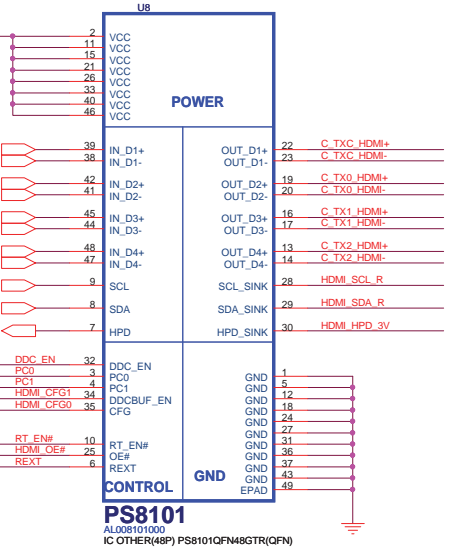
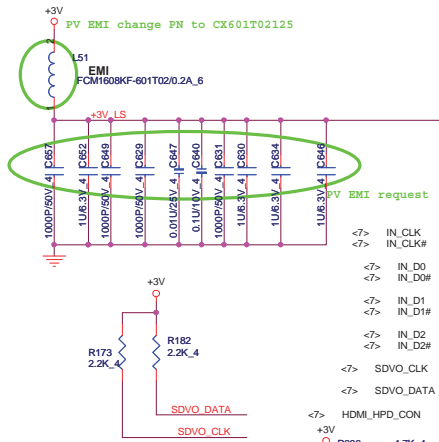
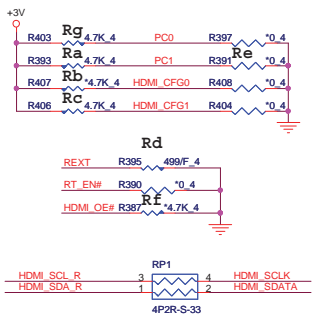
change to +5VS5



PROJECT : R12
 Quanta Computer Inc.



Signals		PDT	PIM	CHR
PC1	Ra	4.7K	4.7K	NC
HDMI_CFG0	Rb	NC	NC	NC
HDMI_CFG1	Rc	4.7K	NC	NC
REXT	Rd	499	4.7K	1.2K
PC1	Re	NC	NC	4.7K
HDMI_OE#	Rf	NC	NC	4.7K
PC0	Rg	4.7K	4.7K	4.7K

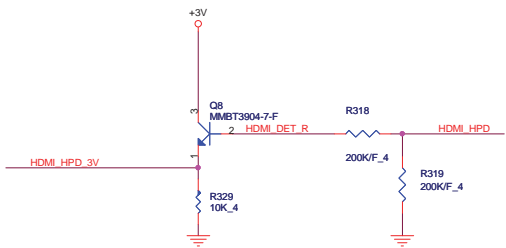
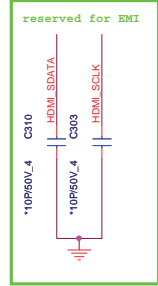
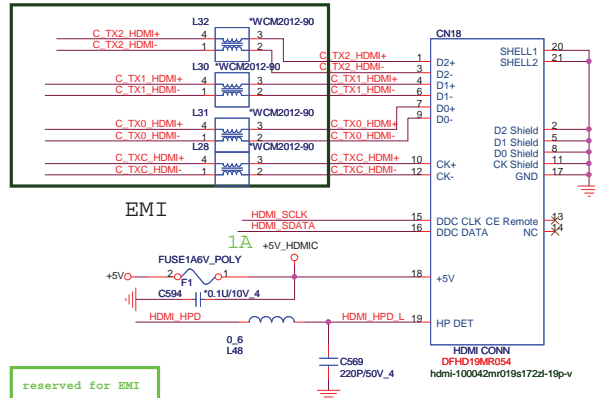
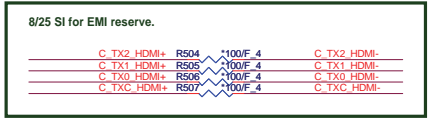
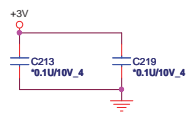


EQUALIZATION SETTING
 PC1:PC0=0:0 8dB
 PC1:PC0=0:1 4dB Recommended
 PC1:PC0=1:0 12dB
 PC1:PC0=1:1 0dB

SCLZ/SDAZ Low-level input/output Voltage
 CFG1:CFG0=0:0 VIL:-0.4V VOL:0.6V (Default)
 CFG1:CFG0=0:1 VIL:-0.36V VOL:0.55V
 CFG1:CFG0=1:0 VIL:-0.44V VOL:0.65V
 CFG1:CFG0=1:1 VIL:-0.36V VOL:0.6V

Vender	Part	Part Number	Part Description
PDT	PS8101	AL008101000	IC OTHER(48P) PS8101QFN48GTR(QFN)
PIM	PI3VDP411LSRZBE	ALP411LS004	IC OTHER(48P) PI3VDP411LSRZBE(TQFN)
CHR	CH7318C	AL007318002	IC OTHER(48P) CH7318C-BF-TR(QFN)

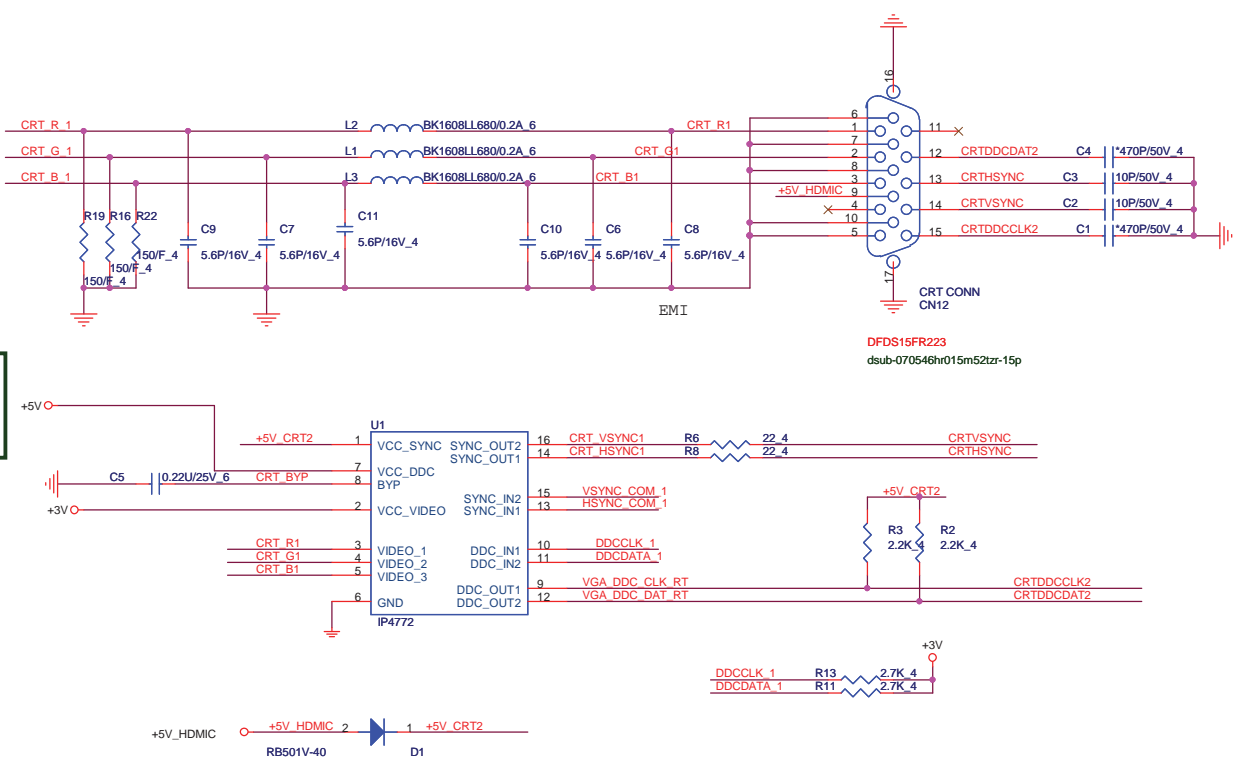
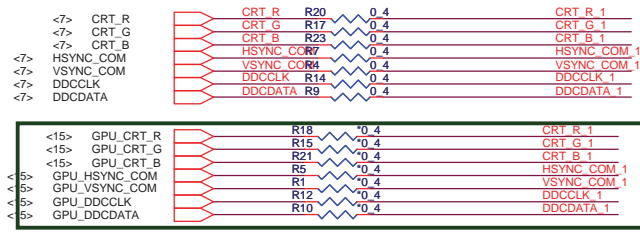
9/16 : PIM: need use ALP411LS000 or ALP411LS004 for capella
 CHR : need Na R1182, add R1027 for capella



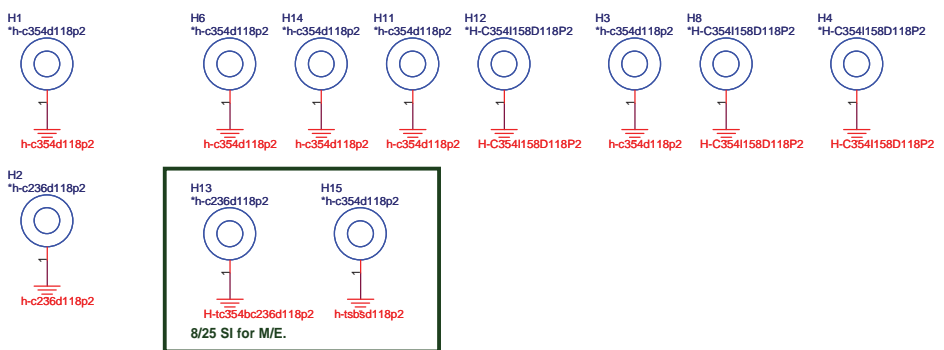
PROJECT : R12
 Quanta Computer Inc.

Size Custom	Document Number HDMI CONN	Rev 1A
Date: Sunday, September 19, 2010		Sheet 21 of 38

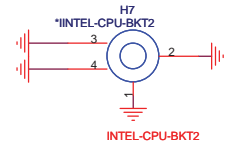
CRT PORT



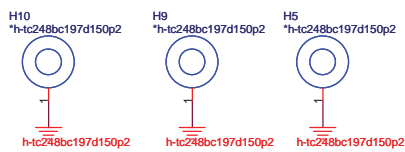
HOLE



CPU



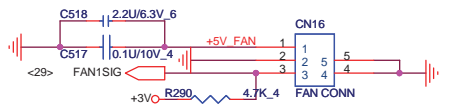
VGA



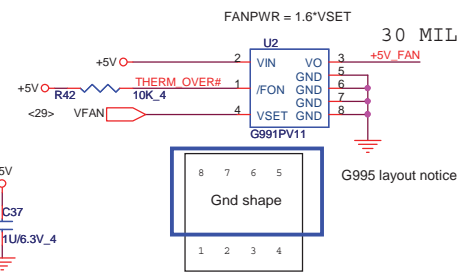
PROJECT : R12
Quanta Computer Inc.

Size Custom Document Number CRT,Hole Rev 1A
Date: Sunday, September 19, 2010 Sheet 22 of 39

CPU FAN



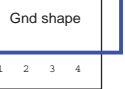
DFHD03MR029
53398-0310-3P-L



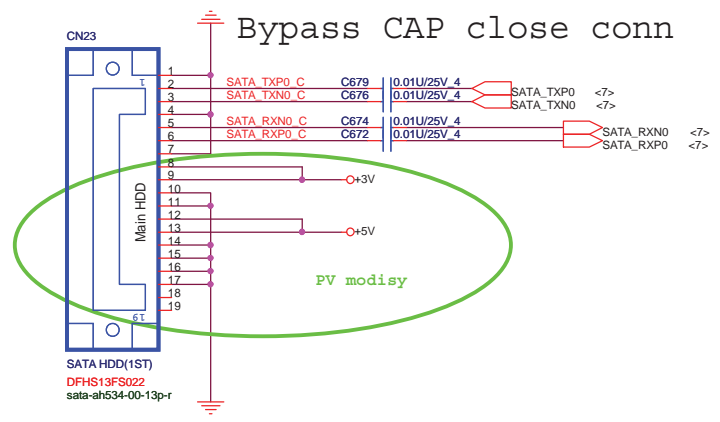
FANPWR = 1.6"VSET

30 MIL

G995 layout notice



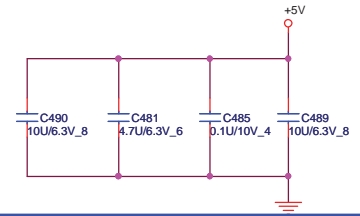
SATA HDD CONNECTOR



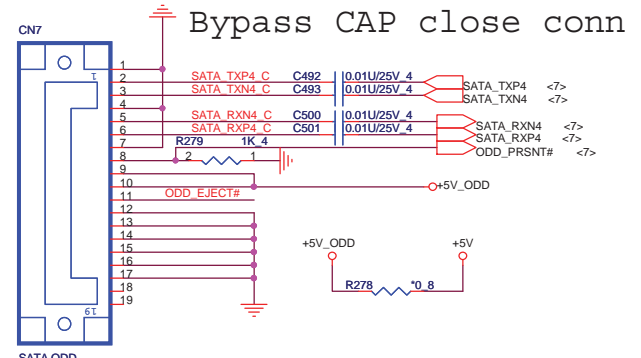
Bypass CAP close conn

PV modisy

SATA HDD(1ST)
DFHS13FS022
sata-ah534-00-13p-r

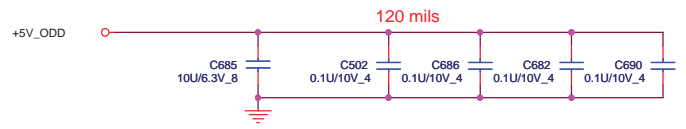


SATA ODD CONNECTOR



Bypass CAP close conn

SATA ODD
DFHS13FS022
sata-ah534-00-13p-r



120 mils

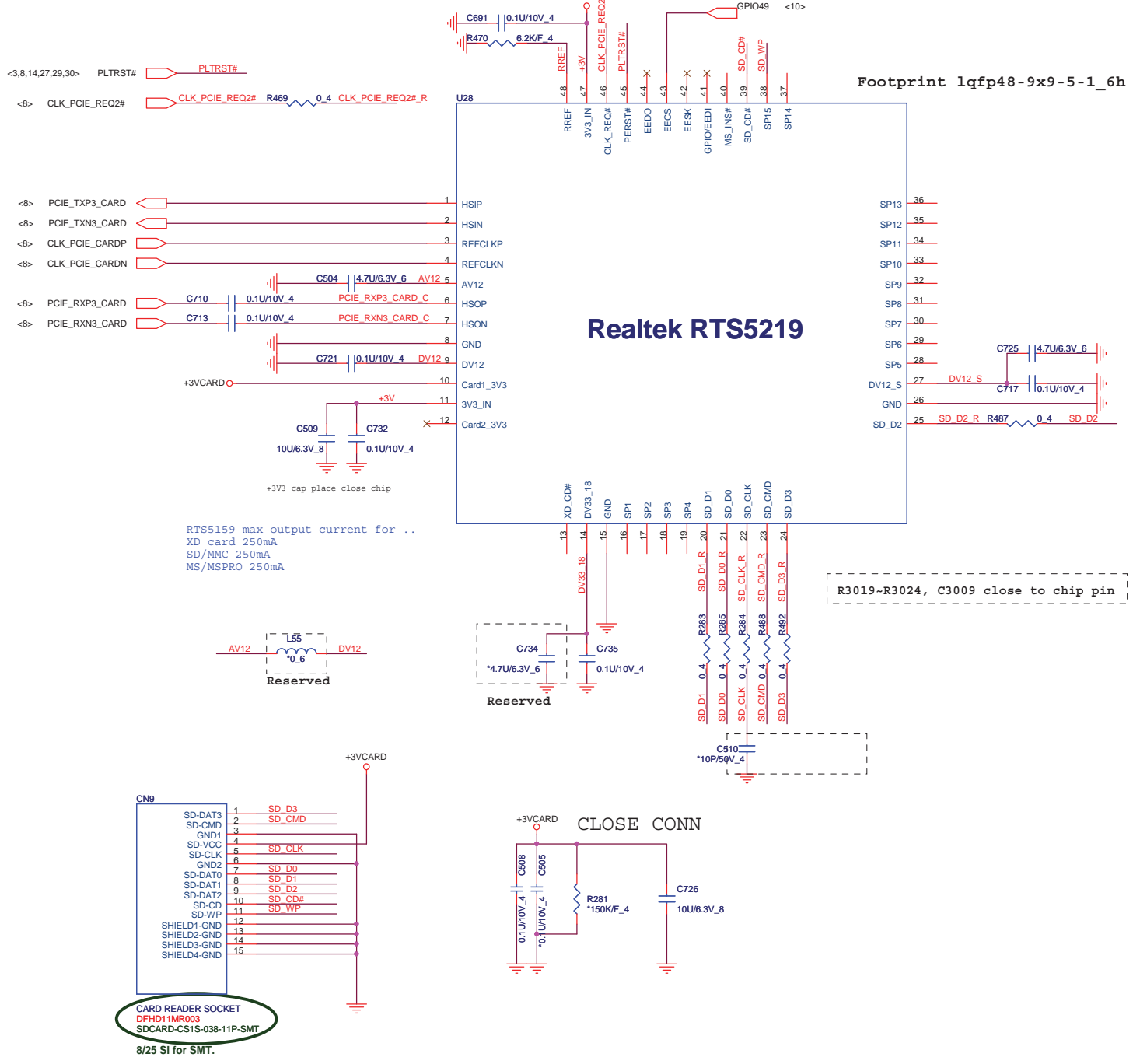
follow INTEL DG change eject PU to +3V.

High : ODD power down
Low : ODD power on



PROJECT : R12
Quanta Computer Inc.

Size Custom	Document Number HDD/ODD/FAN	Rev 1A
Date: Sunday, September 19, 2010 Sheet 23 of 39		



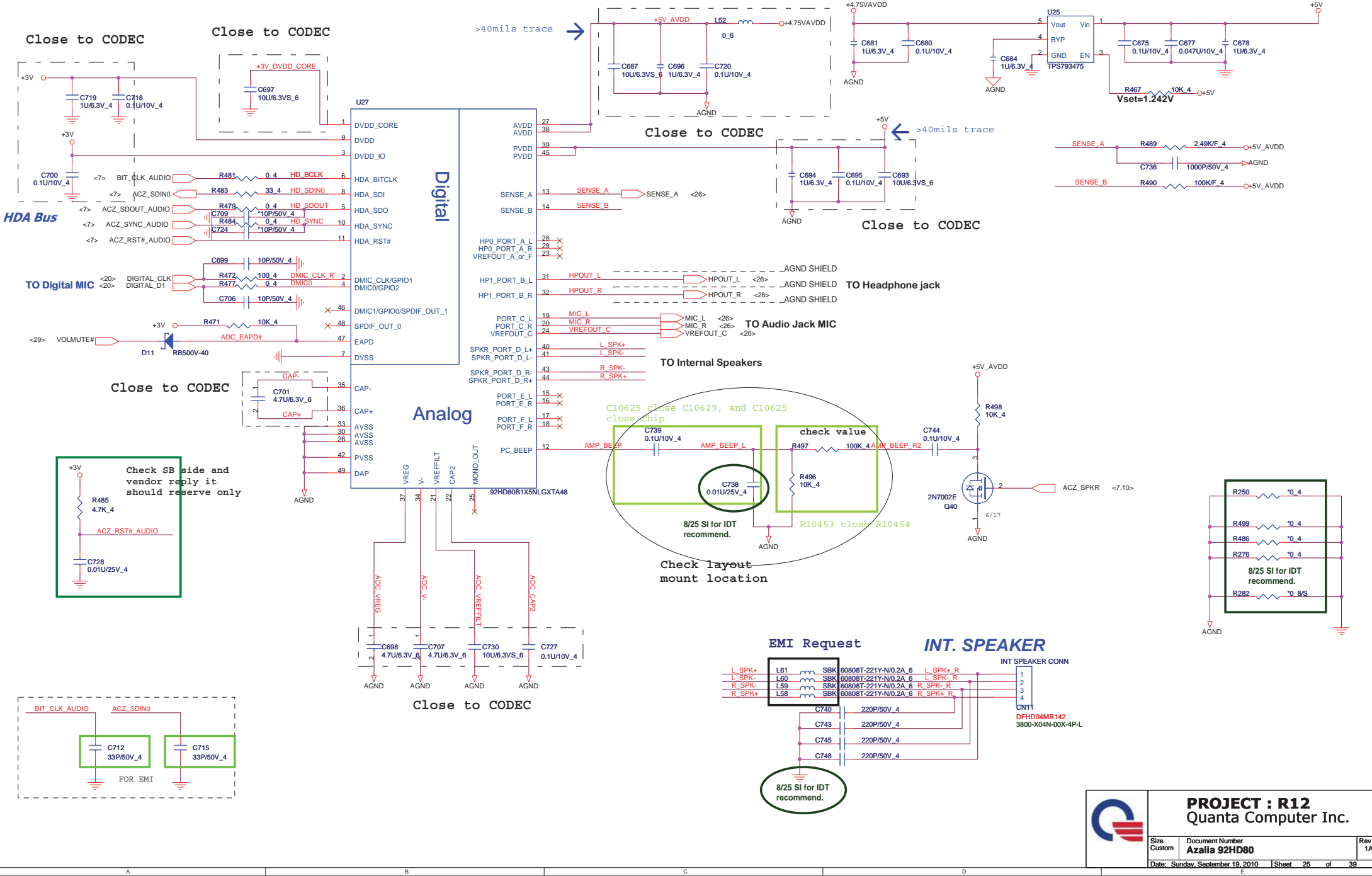
R3019-R3024, C3009 close to chip pin



PROJECT : R12
Quanta Computer Inc.

Size Custom	Document Number RTS5219 & CR SOCKET & HOLE	Rev 1A
Date: Sunday, September 19, 2010 Sheet 24 of 39		

<2,3,7,8,9,10,11,12,13,14,17,20,21,22,23,24,27,28,29,30,33,34,36> +3V
 <11,17,21,22,23,28,30,36> +5V



Check SB side and vendor reply it should reserve only


C10625 close C10629, and C10625 close chip

check value

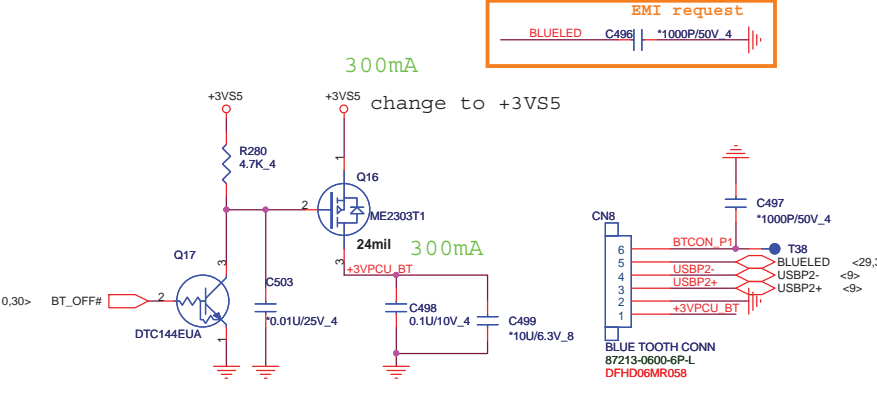
8/25 SI for IDT recommend.

Check layout mount location

8/25 SI for IDT recommend.

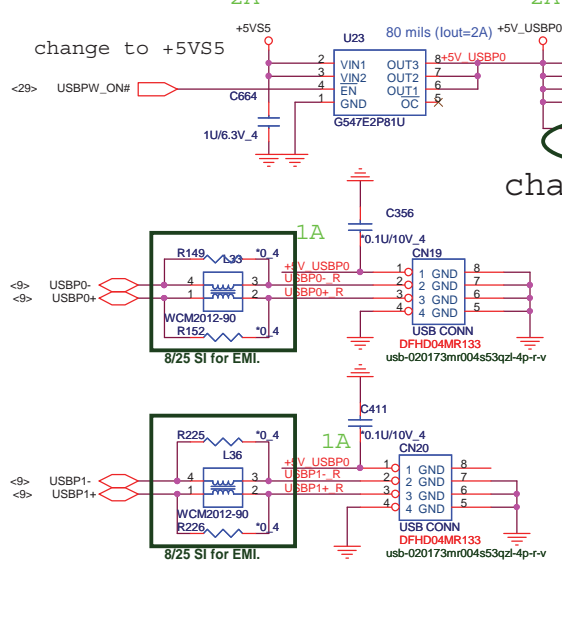
		
PROJECT : R12 Quanta Computer Inc.		
Size Custom	Document Number Azalia 92HD80	Rev 1A
Date: Sunday, September 19, 2010	Sheet 25 of 39	

BLUETOOTH

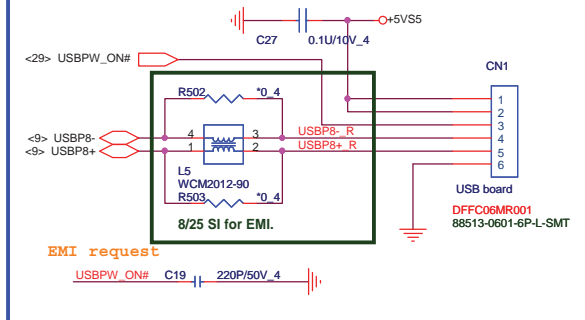


LEFT SIDE USB2

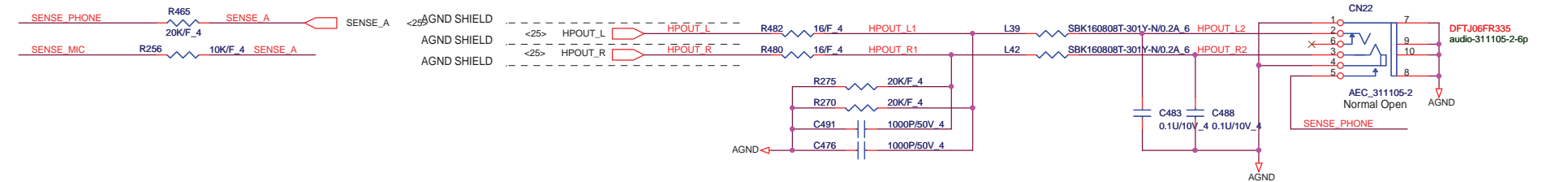
change to AL000547005



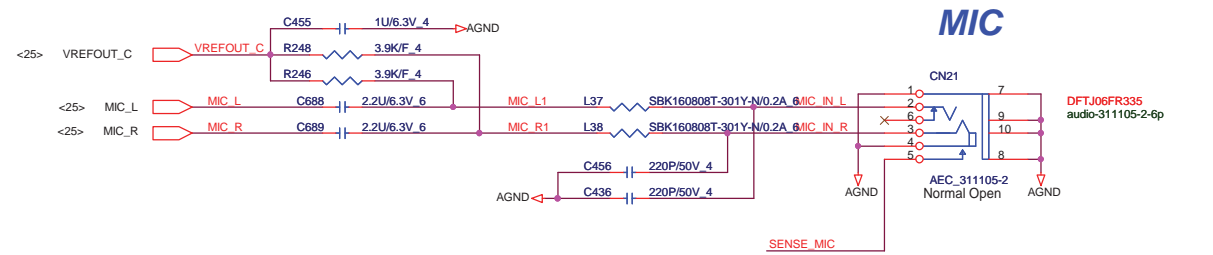
Right SIDE USBX1



Line out

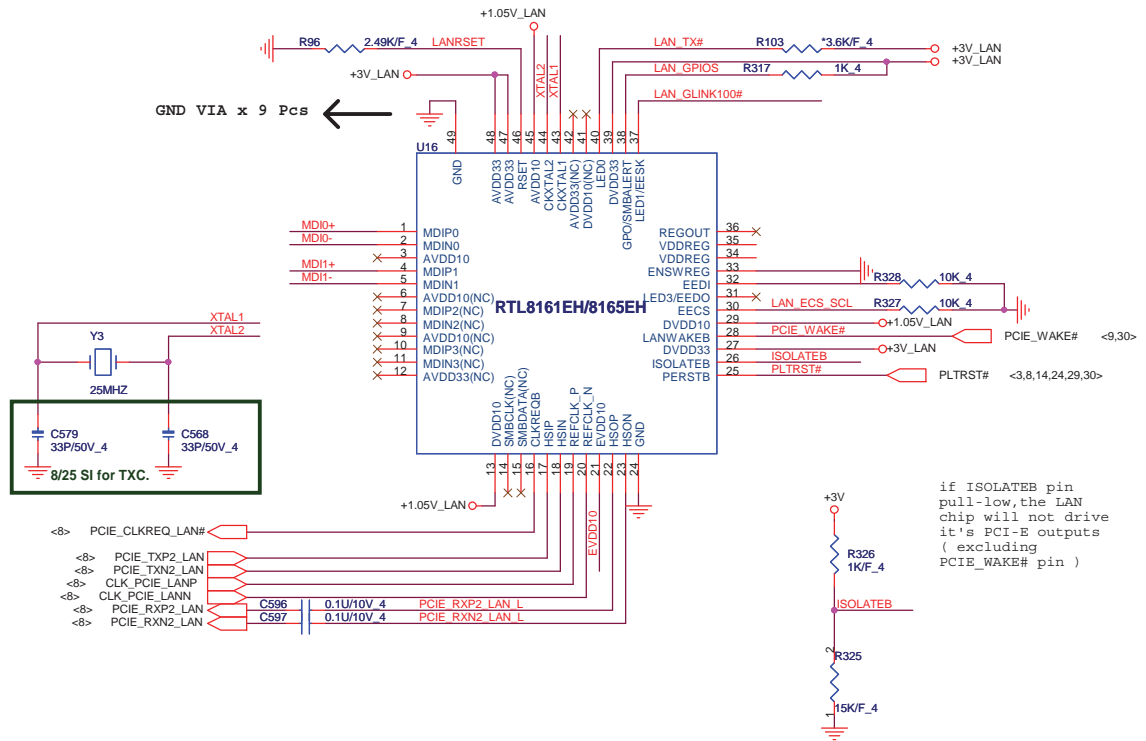


MIC



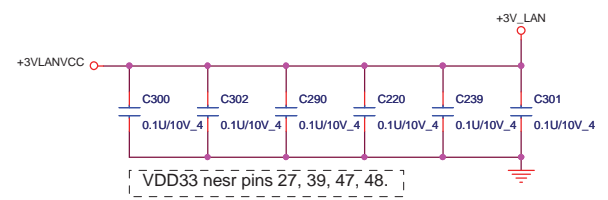
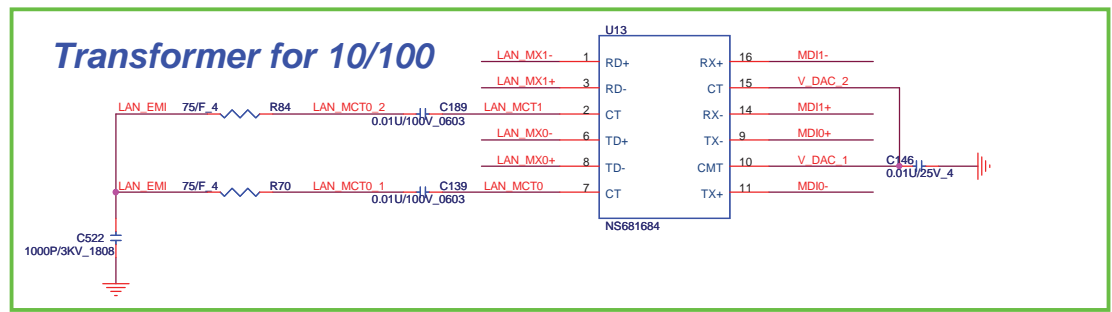
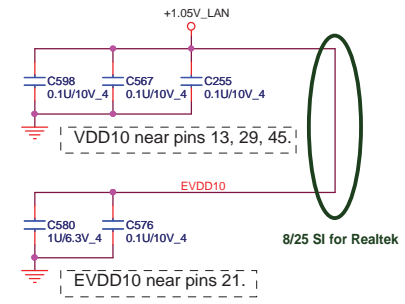
PROJECT : R12
Quanta Computer Inc.

Size Custom	Document Number USB/BT/Audio Jack	Rev 1A
Date: Sunday, September 19, 2010 Sheet 26 of 39		

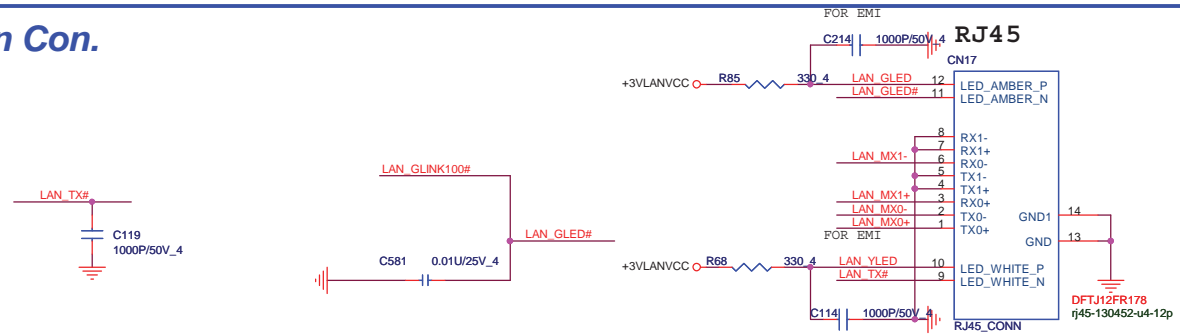


IND SMD 4.7UH +/-20% 680MA (CBC2518T4R7M)
CV-4707MZ00

Power trace Layout 寬度 > 60mil
>60mil



Lan Con.



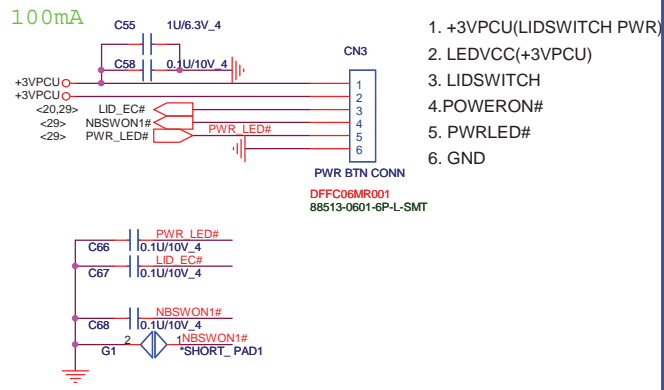
<2,3,7,8,9,10,11,12,13,14,17,20,21,22,23,24,25,28,29,30,33,34,36> <36> +3V_LANVCC +3V



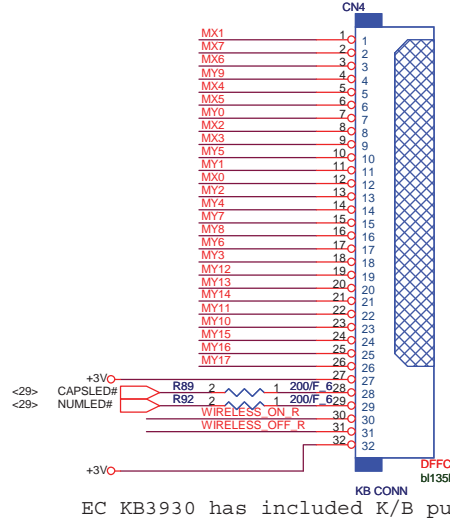
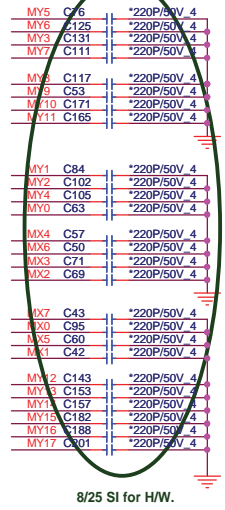
PROJECT : R12
Quanta Computer Inc.

Size Custom	Document Number RTL8165EH	Rev 1A
Date: Sunday, September 19, 2010		Sheet 27 of 39

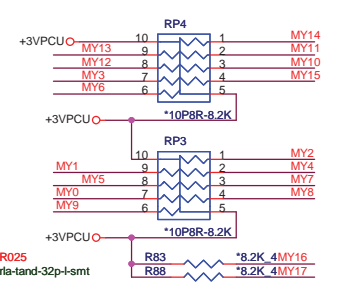
POWER BOTTON CONNECT



KEYBOARD Con.



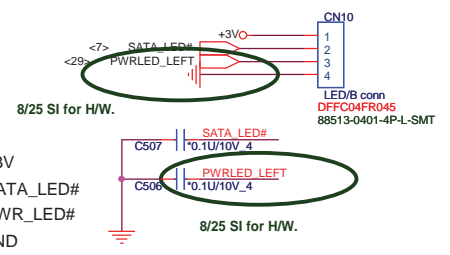
KEYBOARD PULL-UP



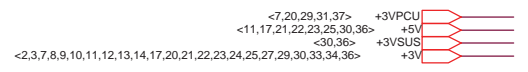
SI Modify



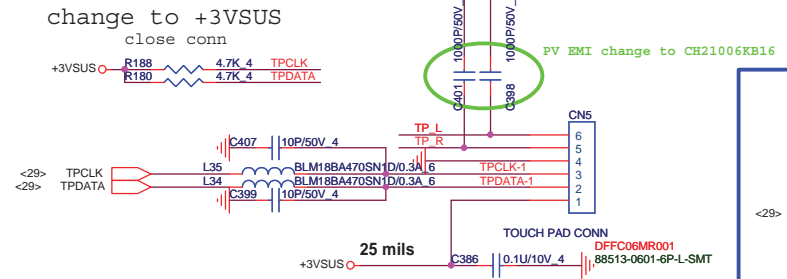
LED Con.



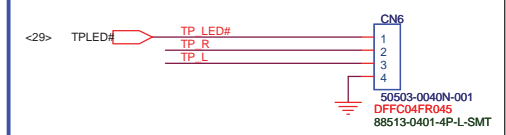
1. +3V
2. SATA_LED#
3. PWR_LED#
4. GND



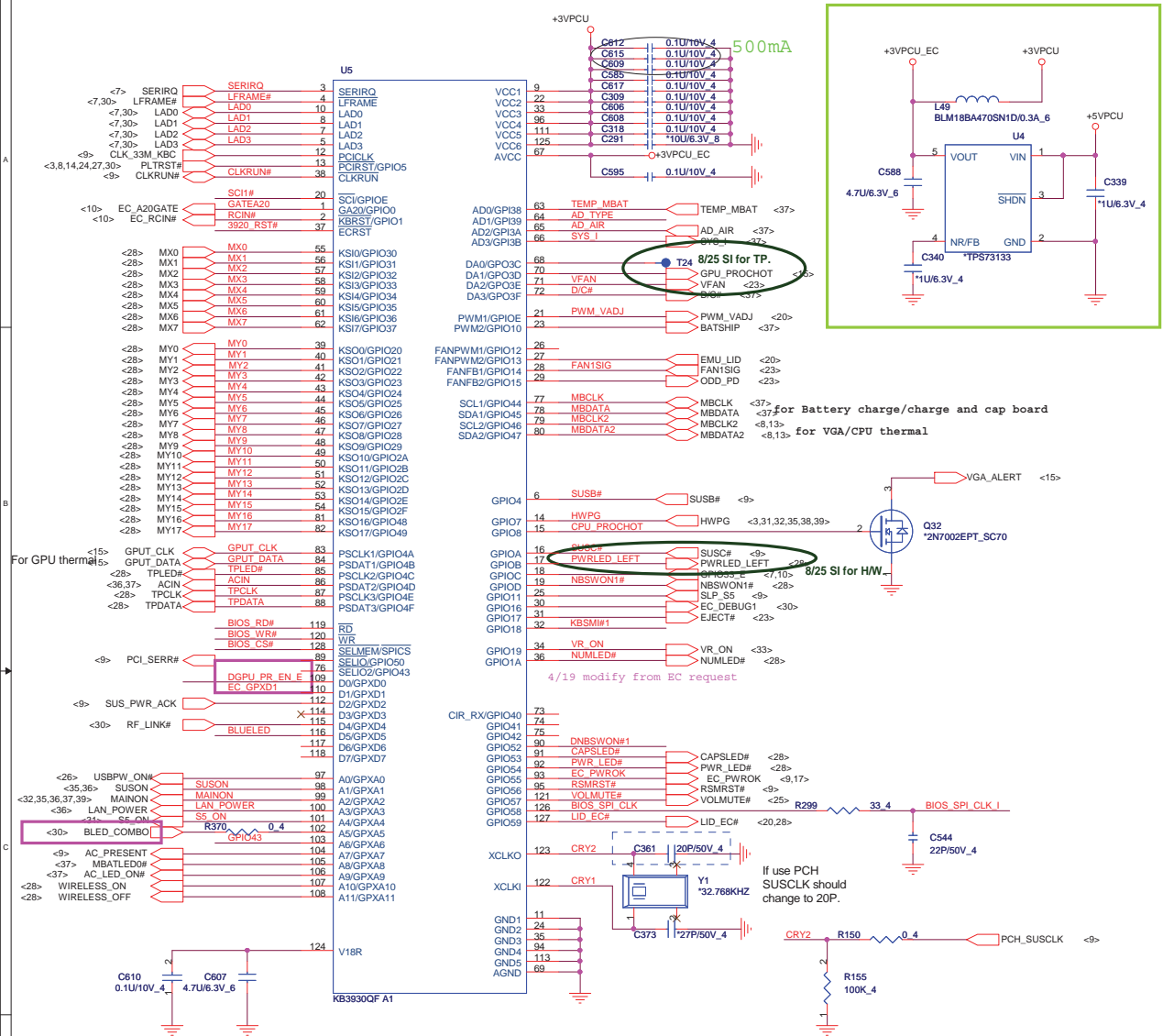
TOUCH PAD Con.



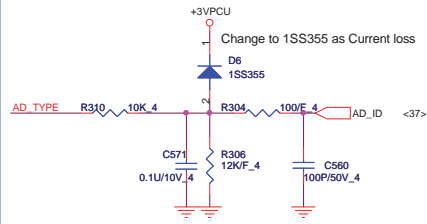
To TOUCH PAD SW board



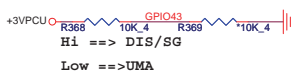
PROJECT : R12
Quanta Computer Inc.



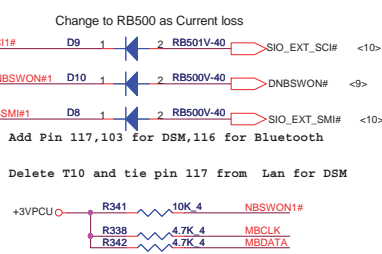
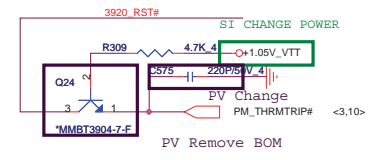
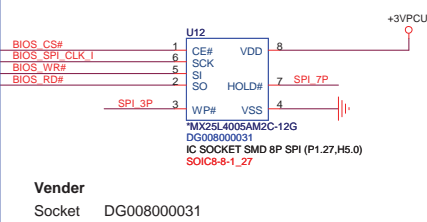
adapter Type check



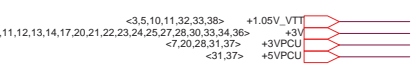
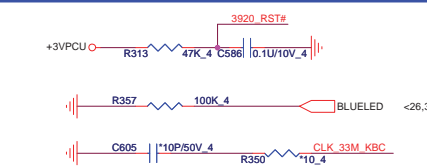
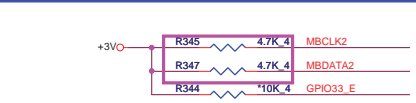
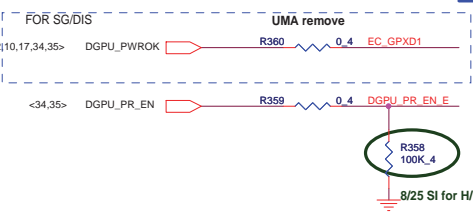
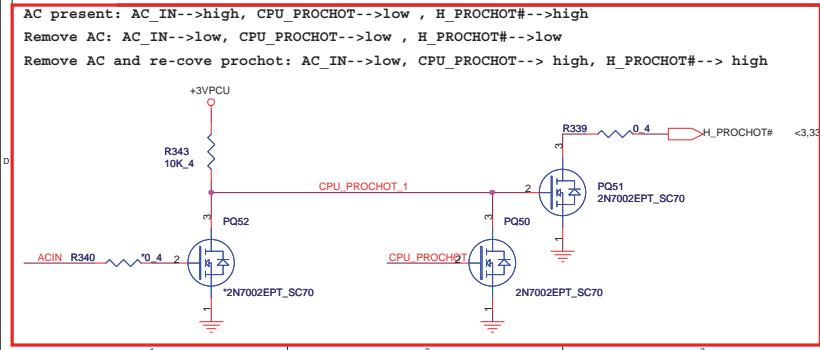
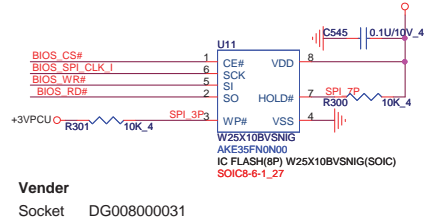
adapter select for EC



512K byte SPI EC ROM



128K byte SPI EC ROM

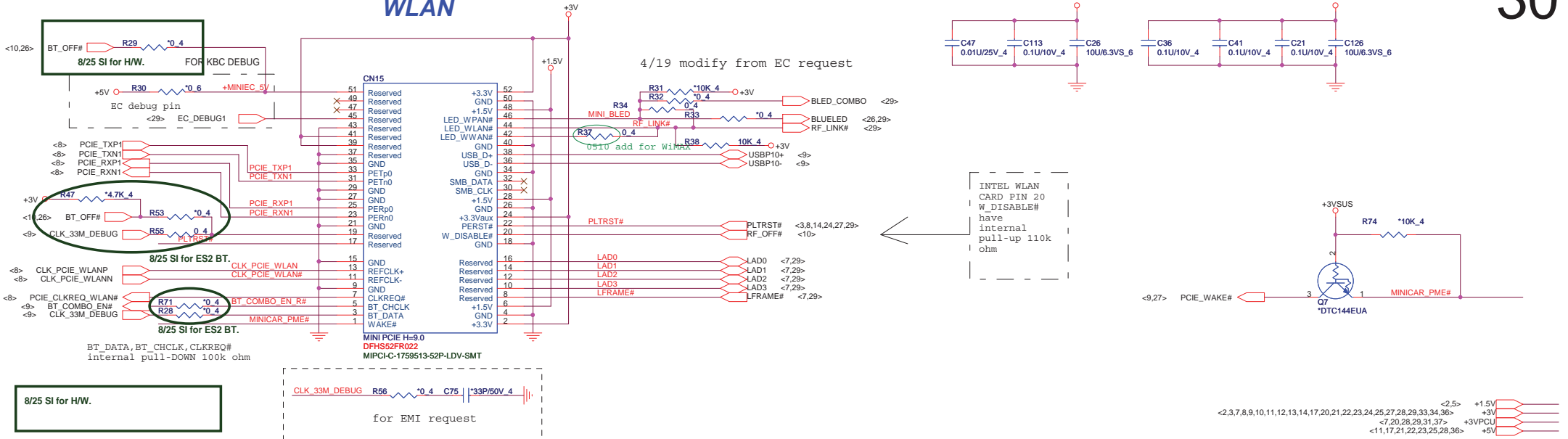


PROJECT : R12
Quanta Computer Inc.

Size	Custom	Document Number	EC (KB3926)ROM	Rev	1A
Date:	Sunday, September 19, 2010	Sheet	29	of	39

Mini PCI-E Card 1

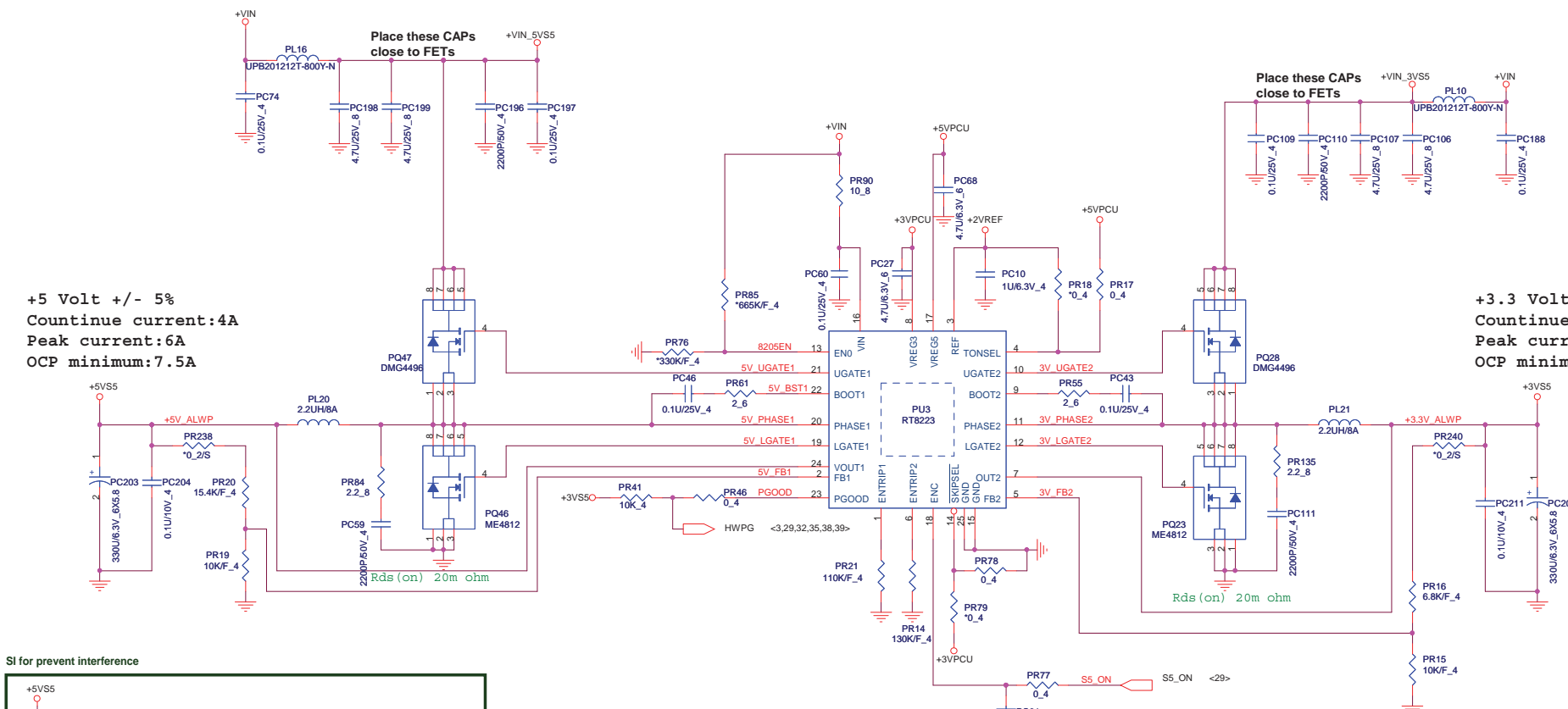
WLAN



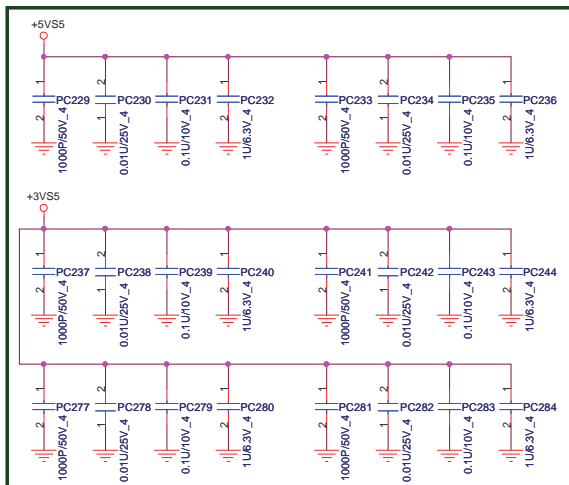
	PROJECT : R12 Quanta Computer Inc.		
	Size Custom	Document Number MINI PCI-E CONN X1	Rev 1A
	Date: Sunday, September 19, 2010 Sheet 30 of 39		


+5 Volt +/- 5%
 Countinue current:4A
 Peak current:6A
 OCP minimum:7.5A

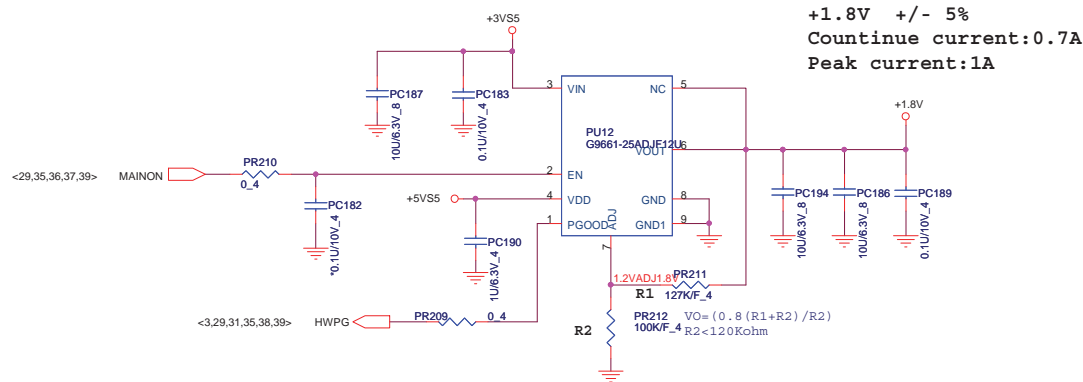
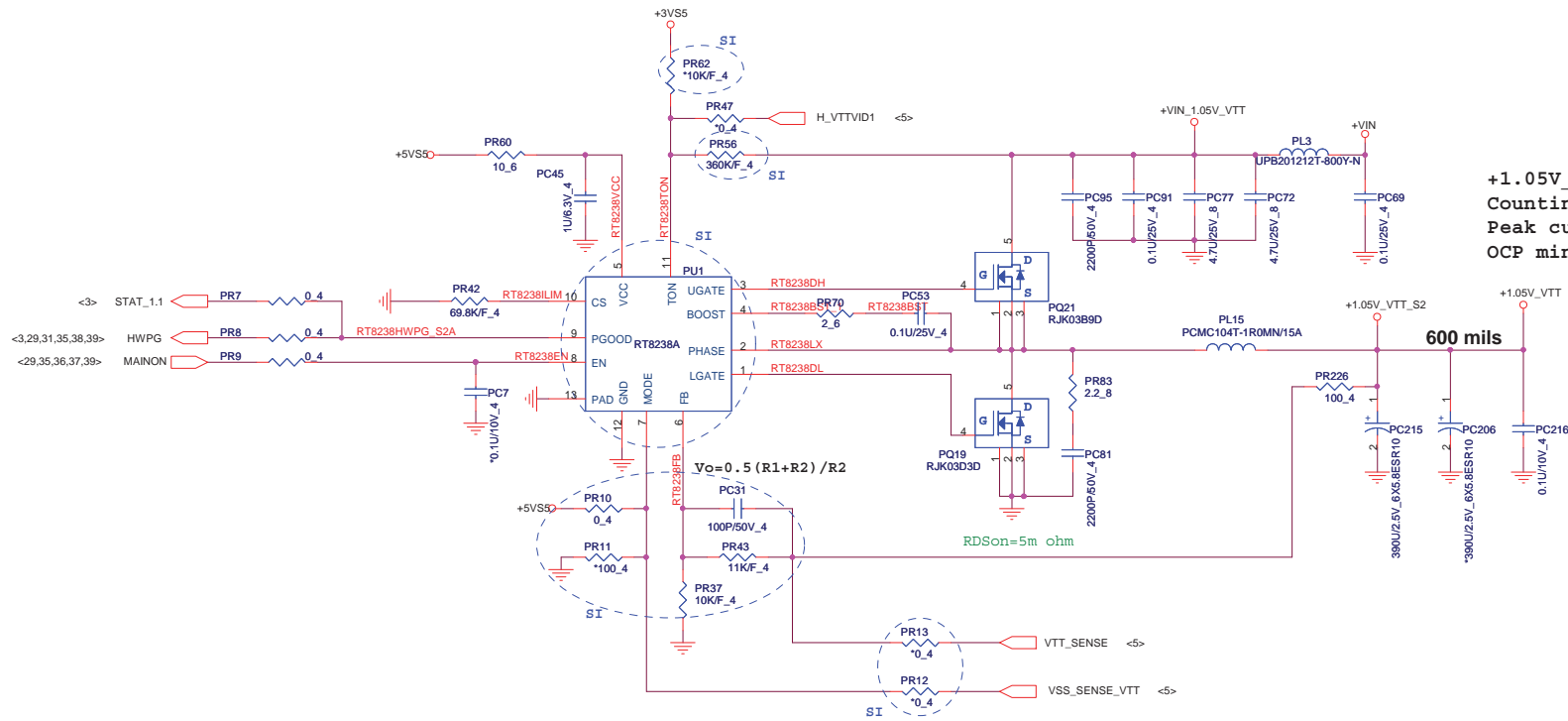
+3.3 Volt +/- 5%
 Countinue current:4A
 Peak current:6A
 OCP minimum:7.5A

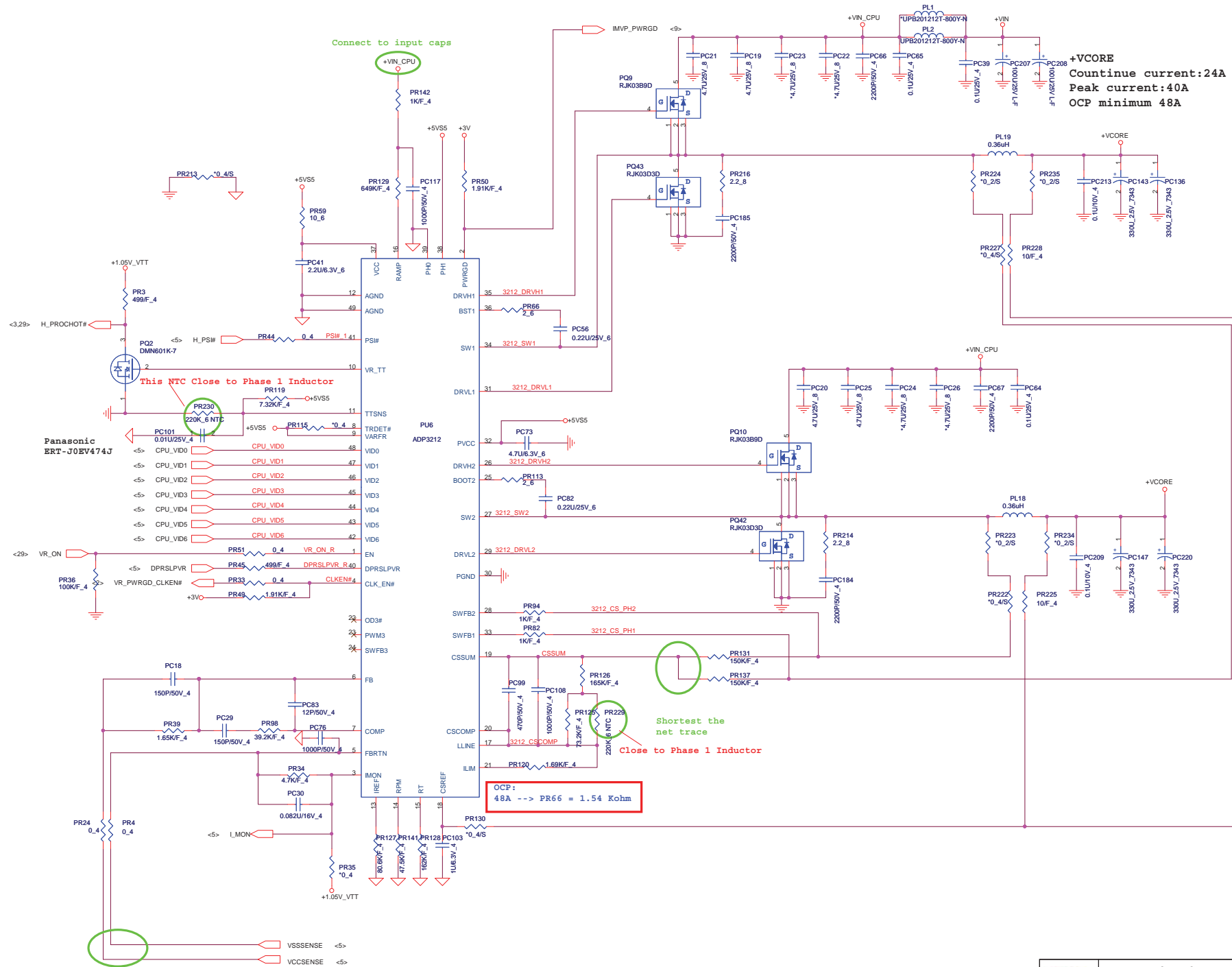


SI for prevent interference

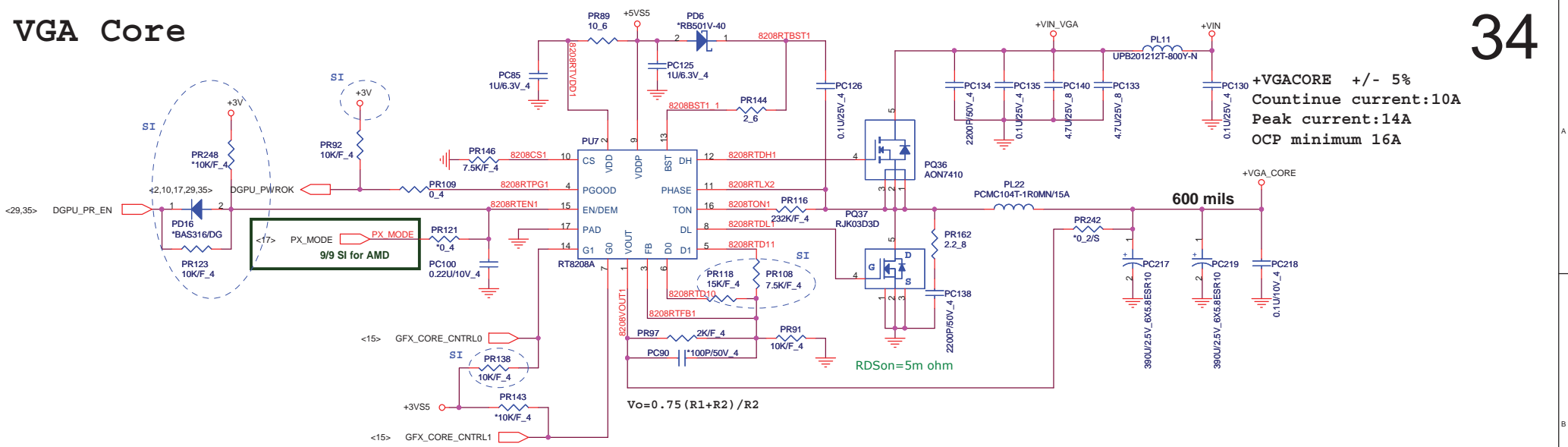


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			Quanta Computer Inc.	
Size Custom	Document Number	+5V/+3V (RT8206B)		Rev 1A
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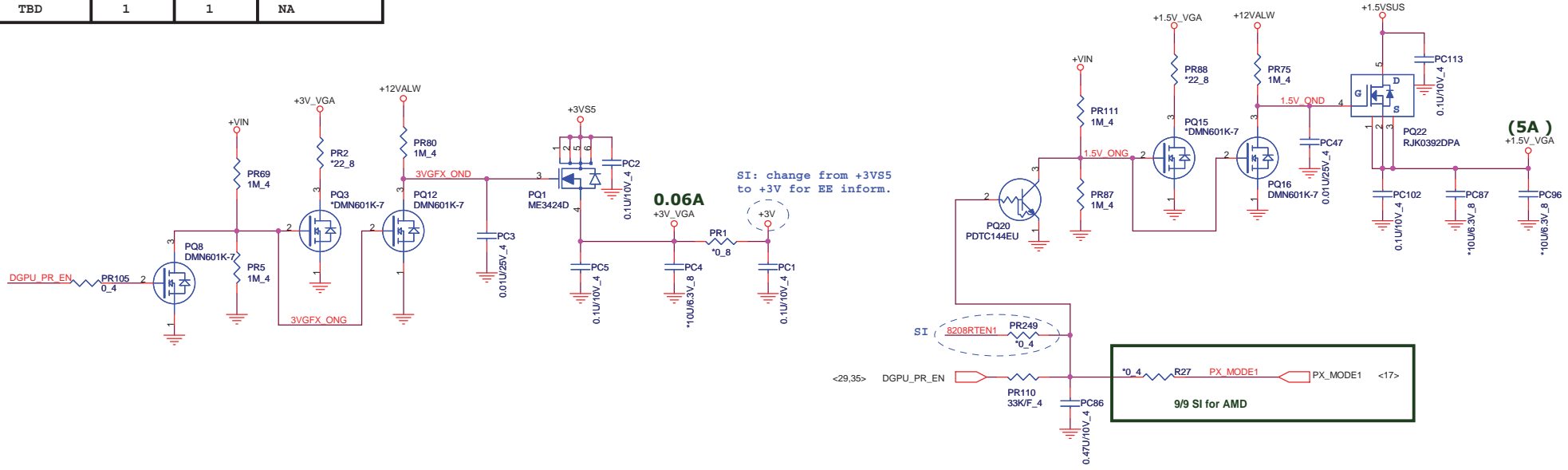




VGA Core



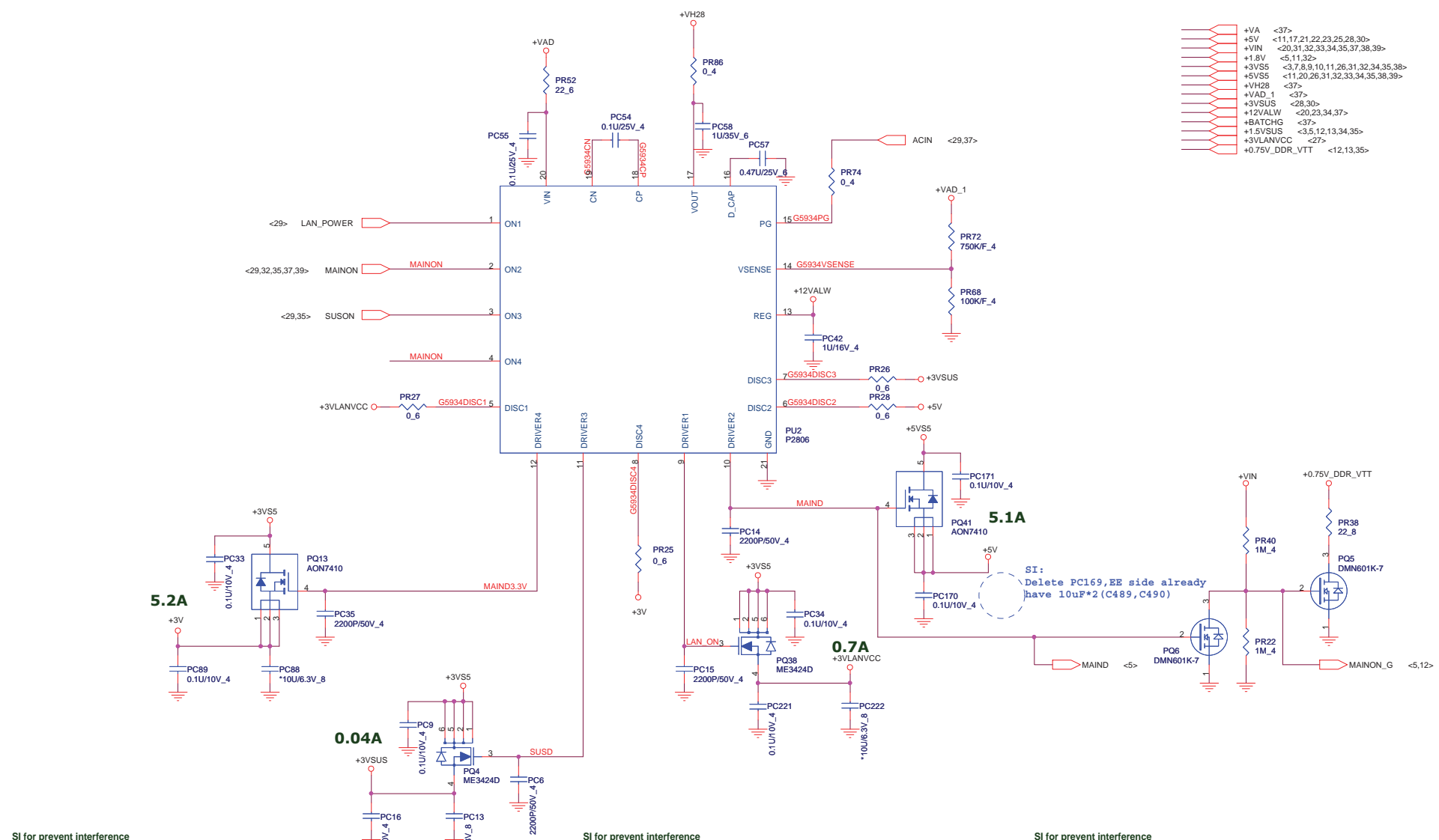
Seymour-XT	PWRCNTL0	PWRCNTL1	V-CORE
L	0	0	0.9V
M	0	1	1V
H	1	0	1.1V (Default)
TBD	1	1	NA



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Quanta Computer Inc.

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- +VA <37>
- +5V <11,17,21,22,23,25,28,30>
- +VIN <20,31,32,33,34,35,37,38,39>
- +1.8V <5,11,32>
- +3VS5 <3,7,8,9,10,11,26,31,32,34,35,38>
- +5VS5 <11,20,26,31,32,33,34,35,38,39>
- +VH28 <37>
- +VAD_1 <37>
- +3VSUS <28,30>
- +12VALW <20,23,34,37>
- +BATCHG <37>
- +1.5VSUS <3,5,12,13,34,35>
- +3VLNVCC <27>
- +0.75V_DDR_VTT <12,13,35>



5.2A

5.1A

0.04A

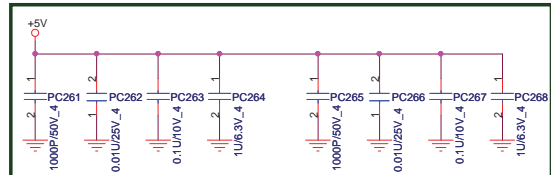
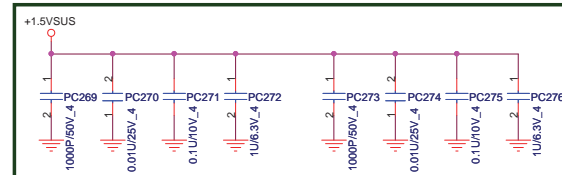
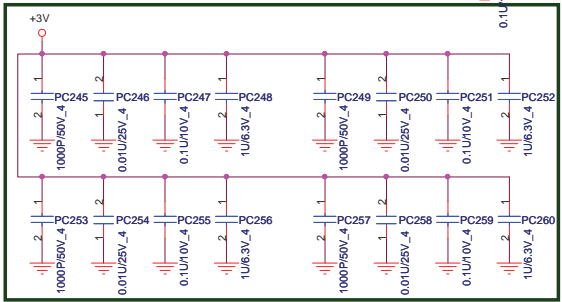
0.7A

SI: Delete PC169, EE side already have 10uF*2 (C489, C490)

SI for prevent interference

SI for prevent interference

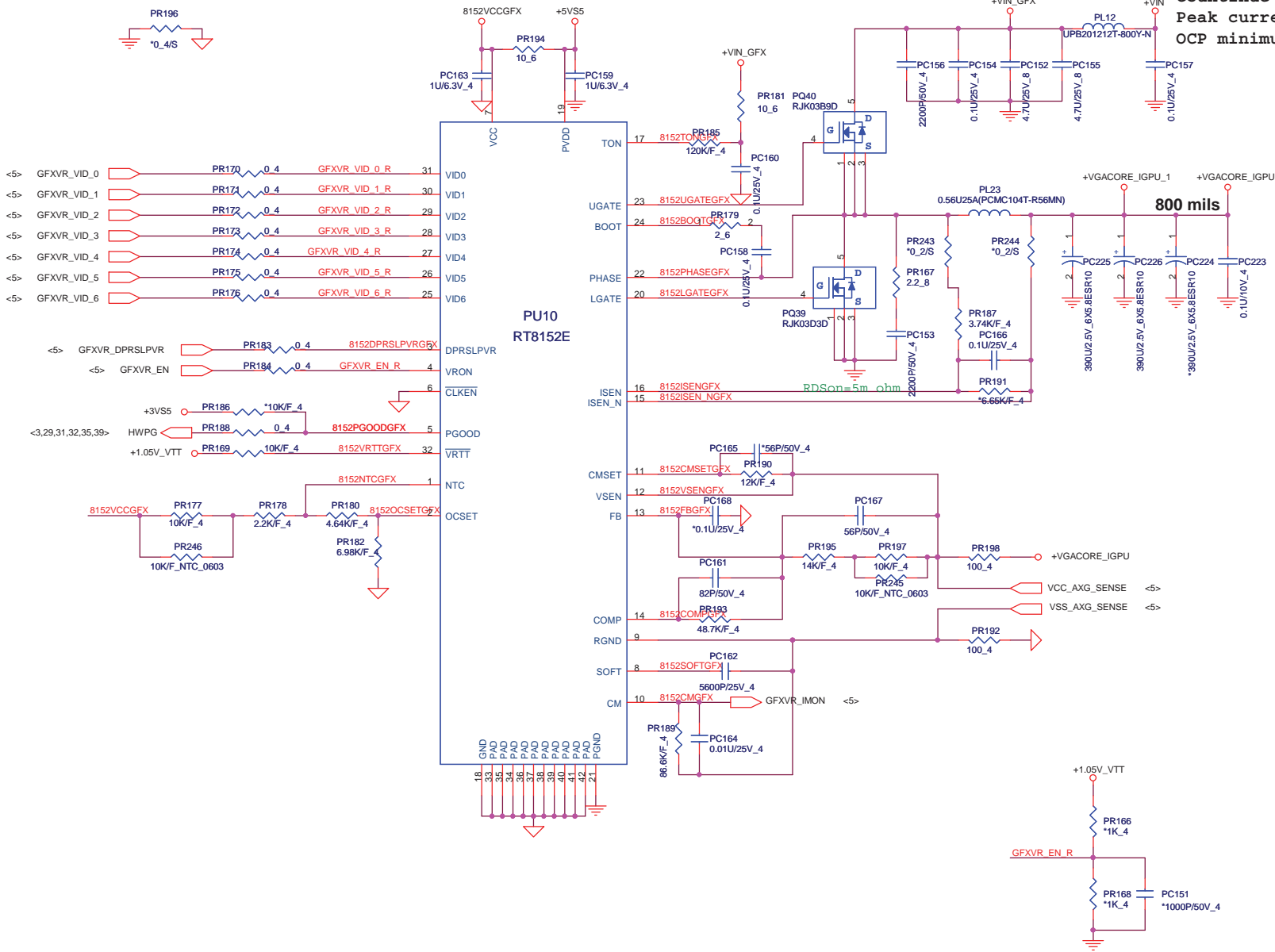
SI for prevent interference

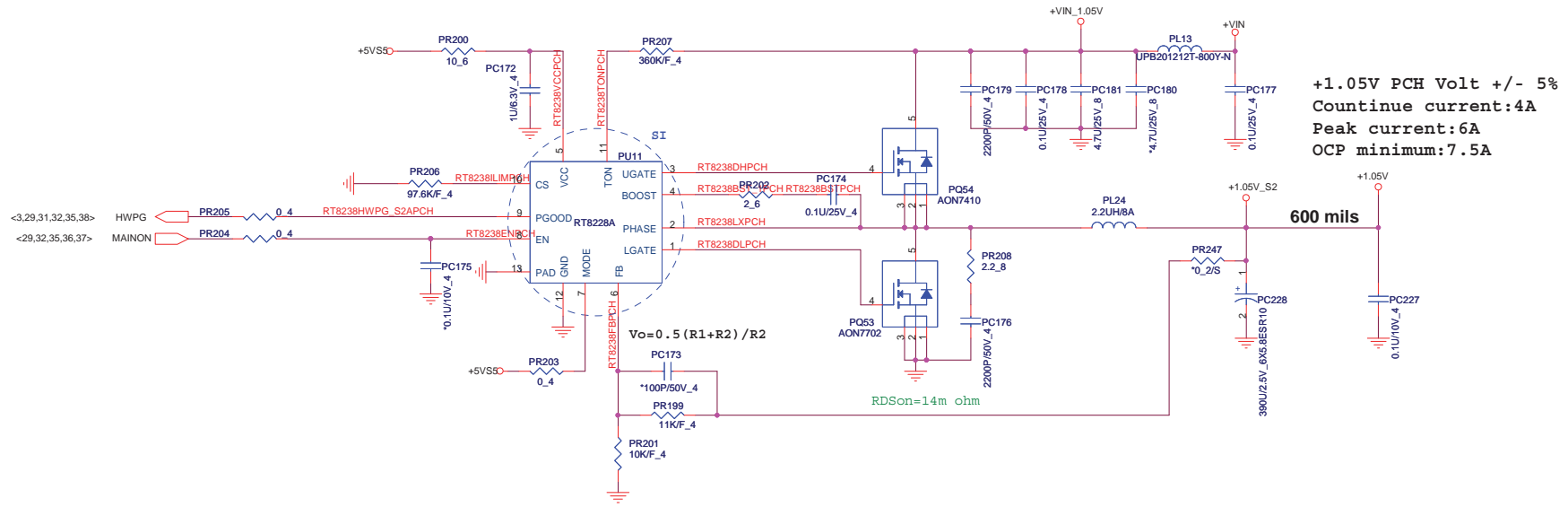


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+VGA_UMA +/- 5%
 Continue current:12A
 Peak current:18A
 OCP minimum 22A





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