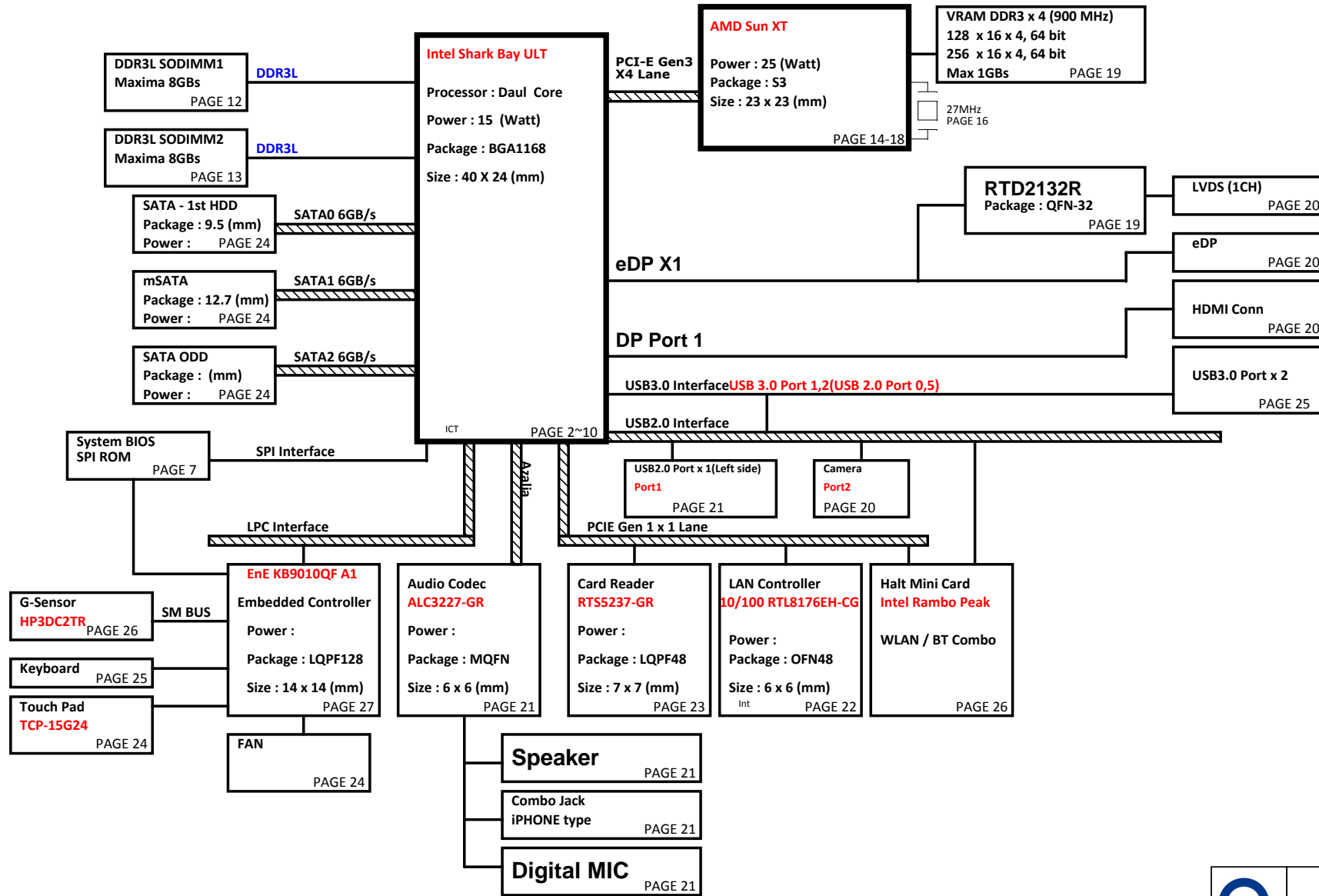
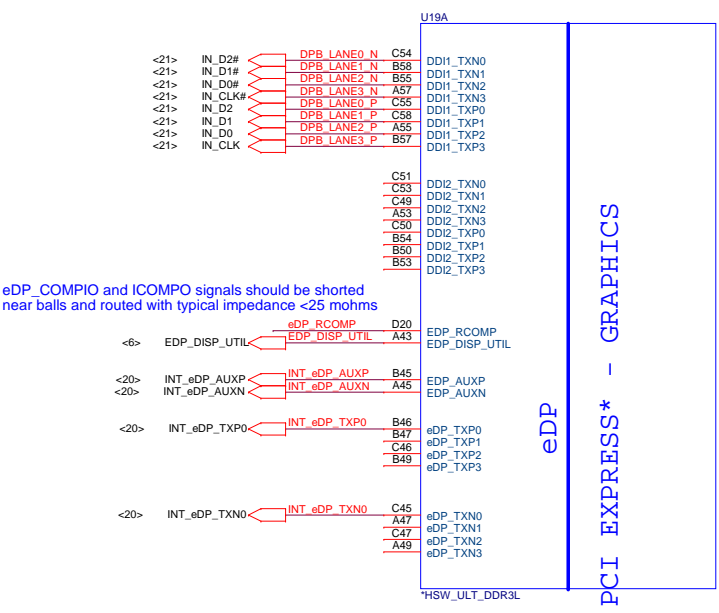


U83 DIS (14"/15.6") Ultra/Slim Intel Shark Bay ULT Platform Block Diagram

PCB 6L STACK UP

LAYER 1 : TOP
 LAYER 2 : SGND
 LAYER 3 : IN1(High)
 LAYER 4 : IN2(Low)
 LAYER 5 : SVCC
 LAYER 6 : BOT

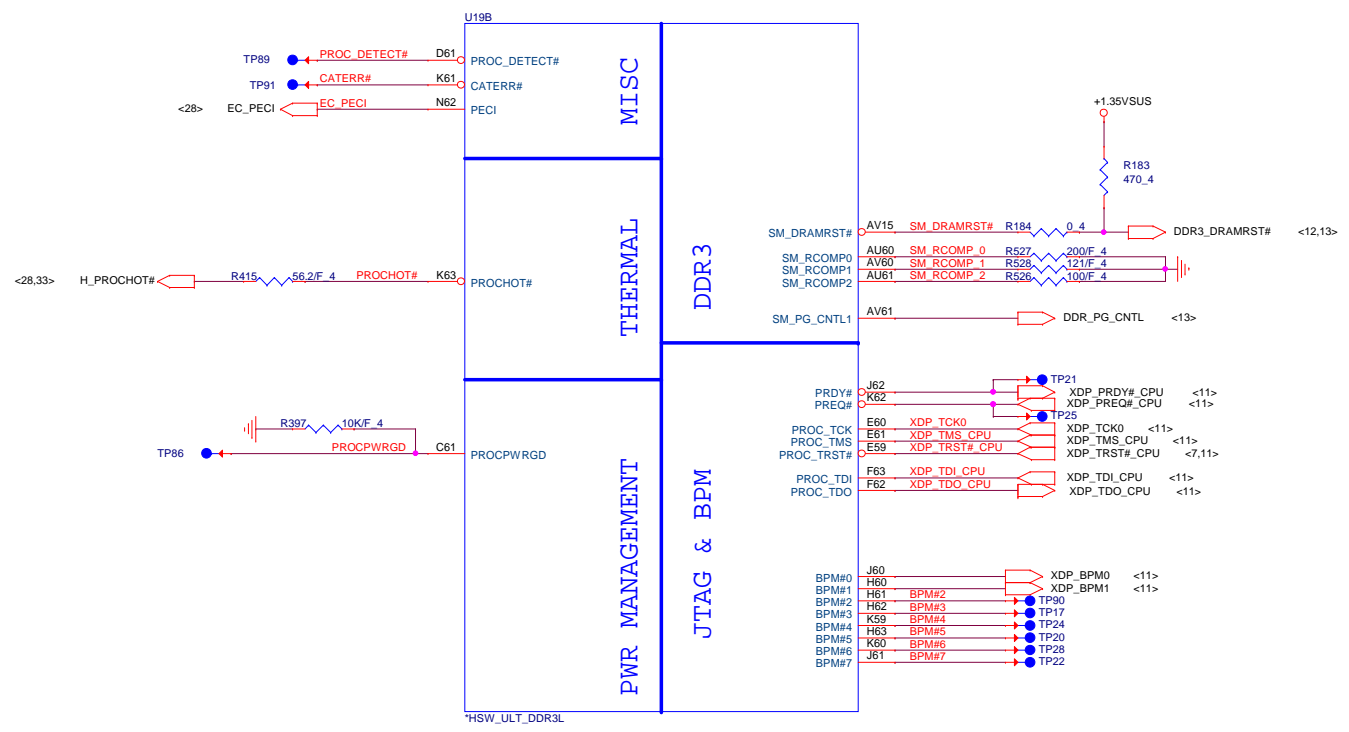




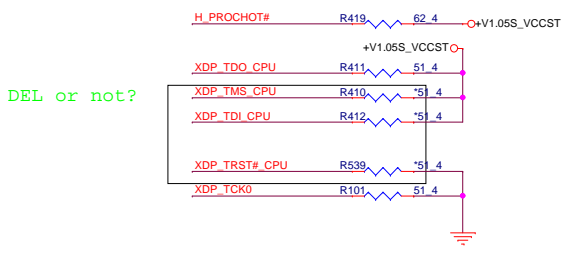
eDP_COMPIO and ICOMP0 signals should be shorted near balls and routed with typical impedance <25 mohms

+VCCIOA_OUT R109 24.9F 4 eDP_RCOMP

eDP_COMPIO and ICOMP0 signals should be shorted near balls and routed with typical impedance <25 mohms



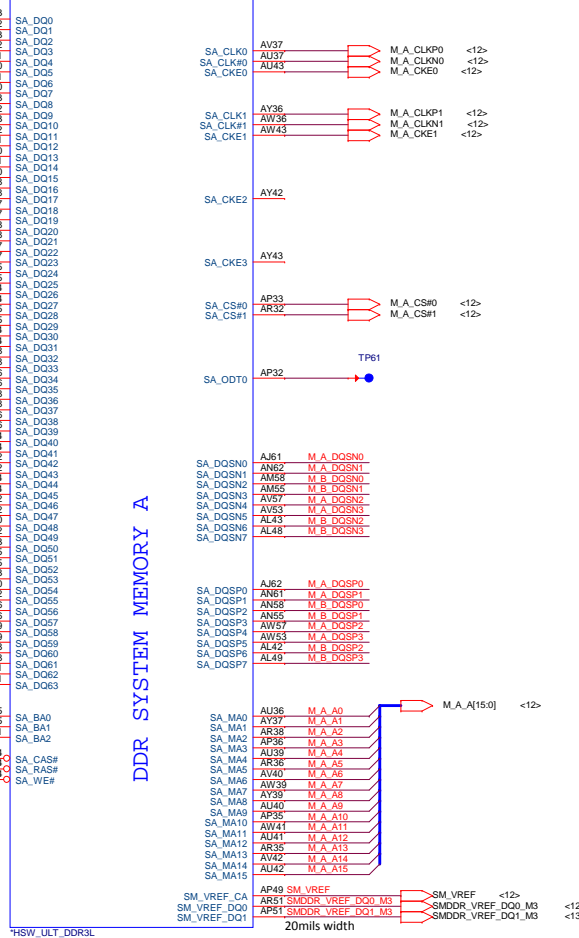
Processor pull-up (CPU)



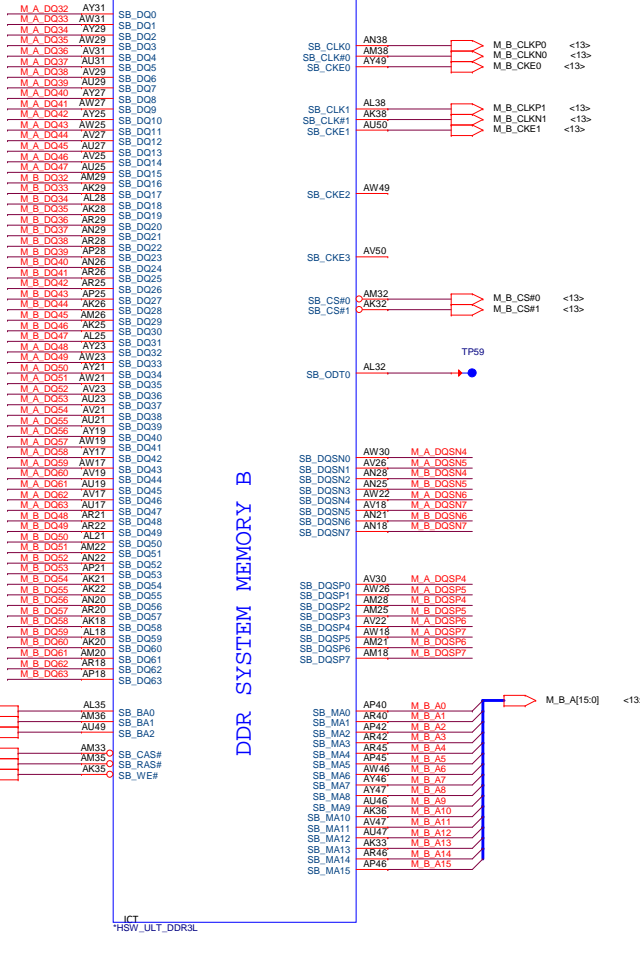
Haswell ULT Processor (DDR3L)

- <12> M_A_DQ[63:0]
- <13> M_B_DQ[63:0]
- <12> M_A_DQSN[7:0]
- <12> M_A_DQSP[7:0]
- <13> M_B_DQSN[7:0]
- <13> M_B_DQSP[7:0]

U19C



U19D

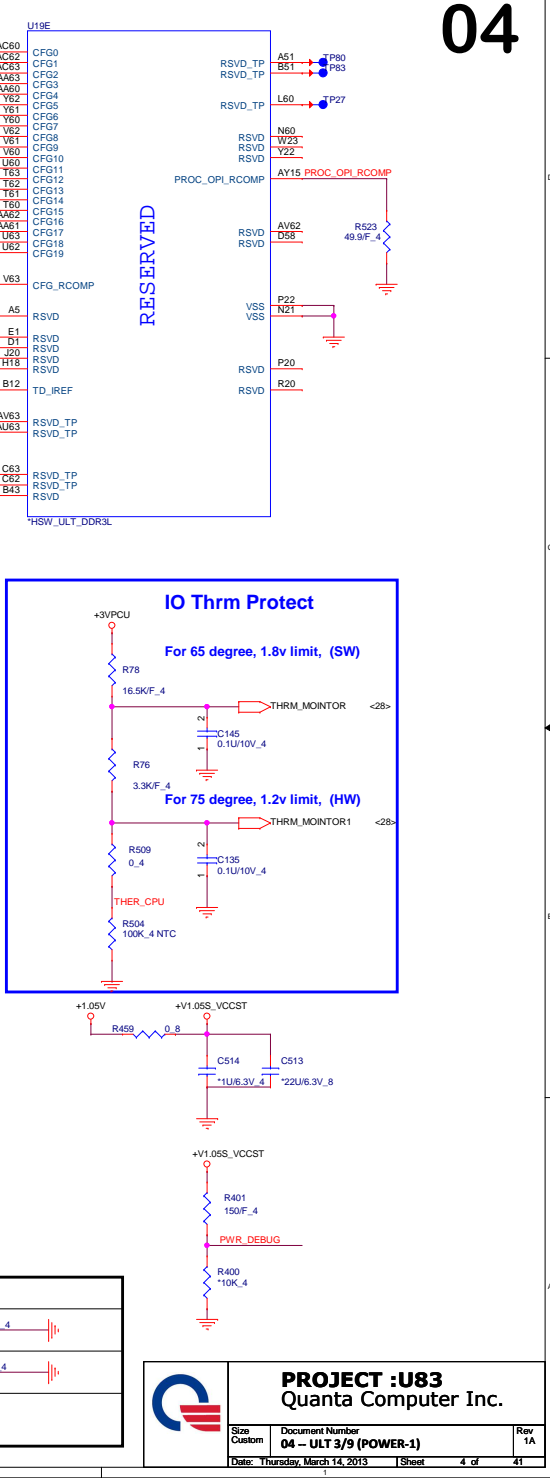
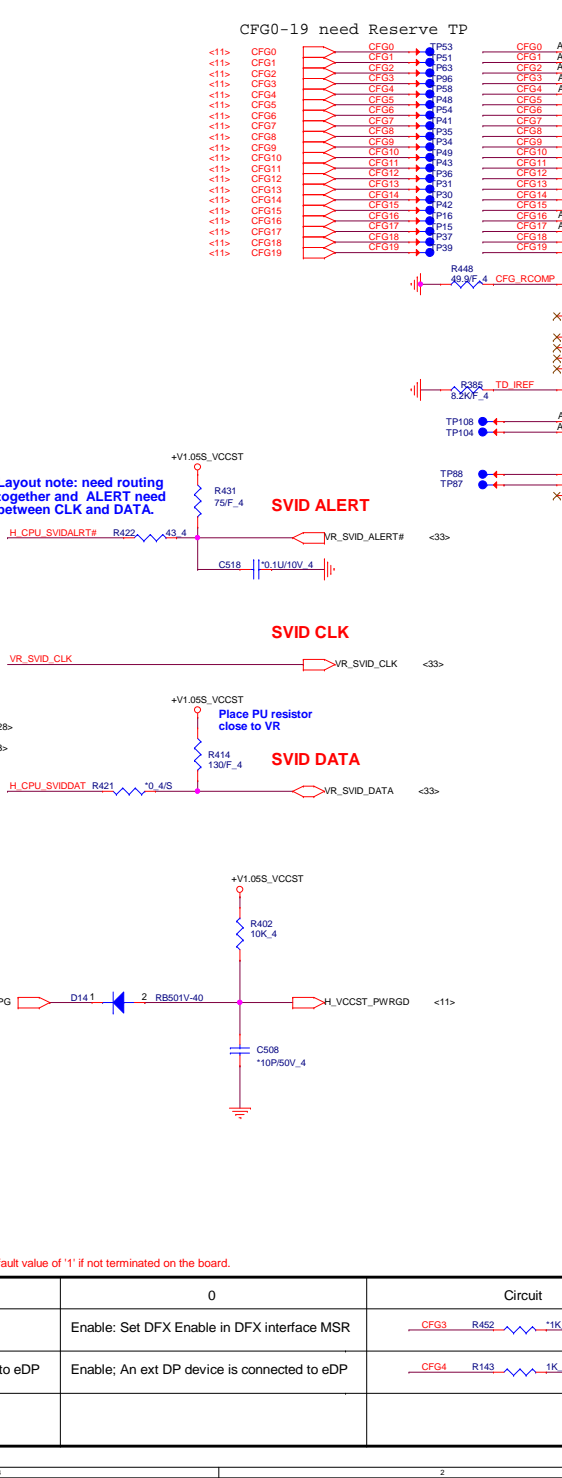
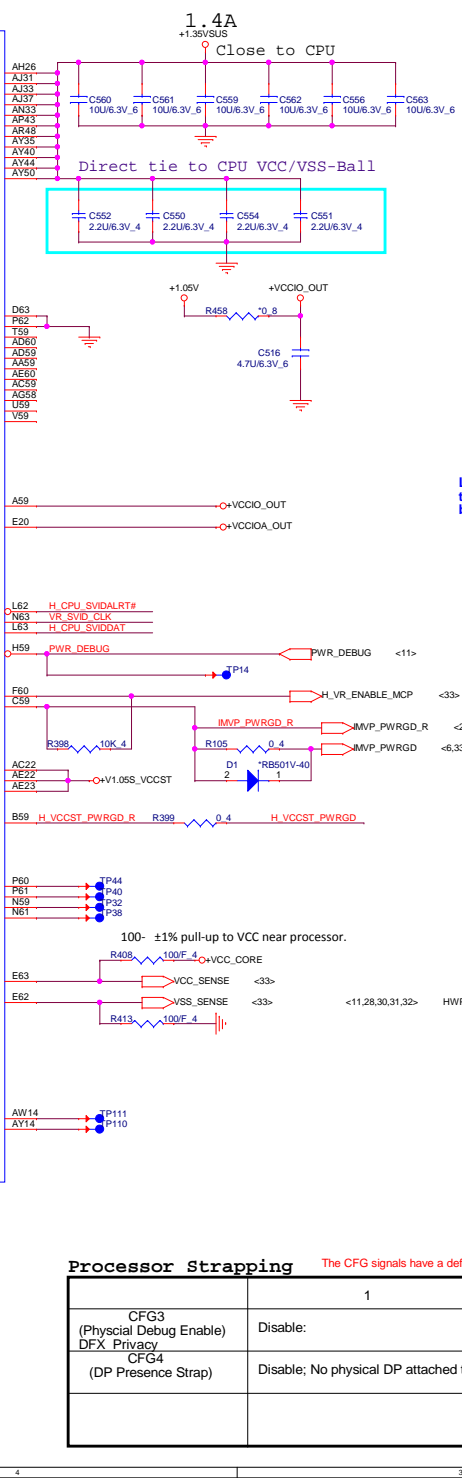
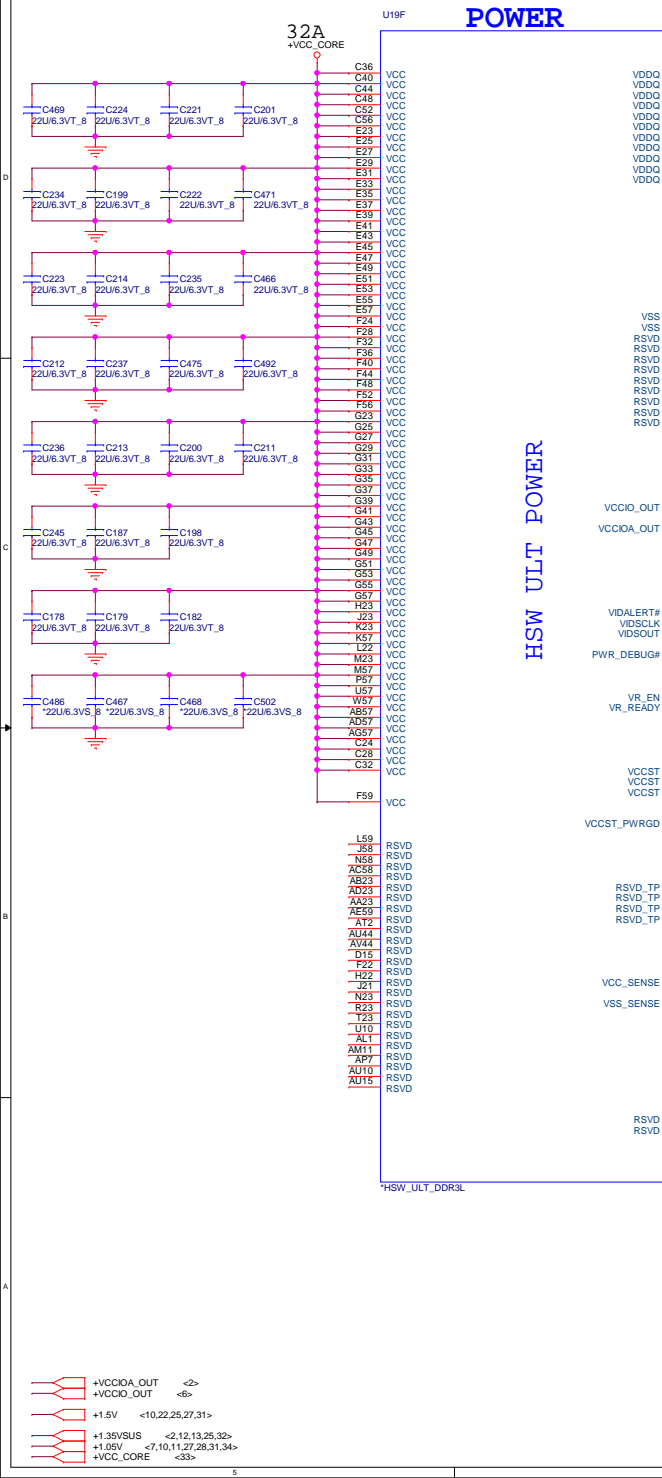


*HSW_ULT_DDR3L

HSW_ULT_DDR3L

PROJECT :U83
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ULT 2/9 (DDR3 I/F)	1A
Date: Monday, March 18, 2013	Sheet	3 of 41

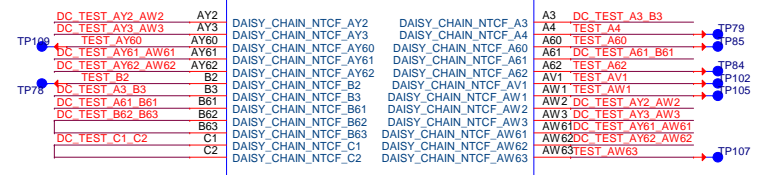
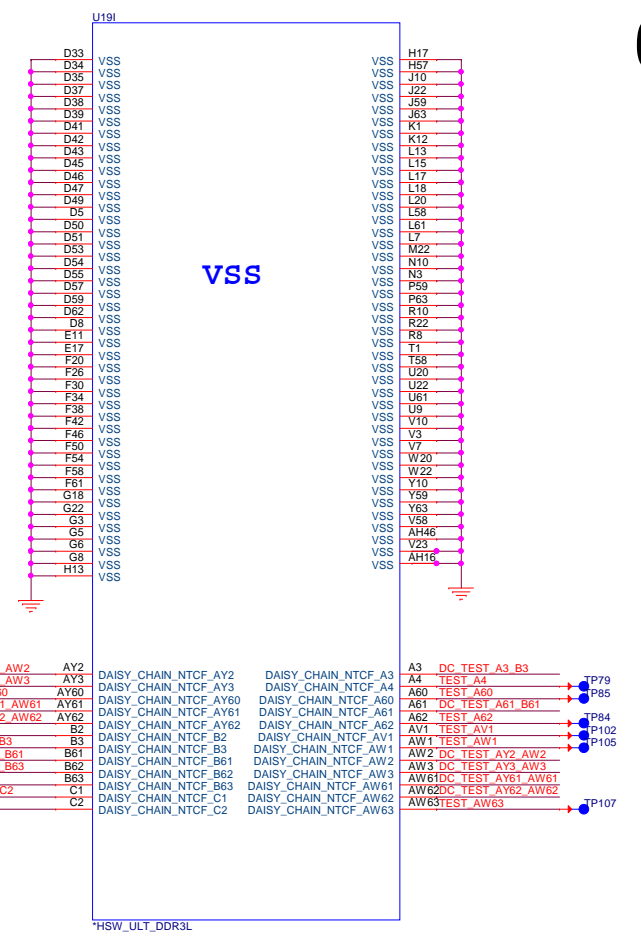
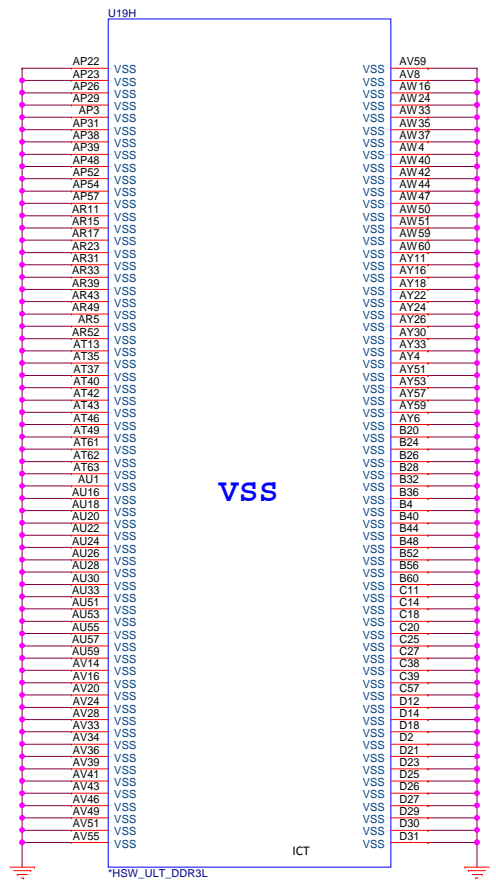
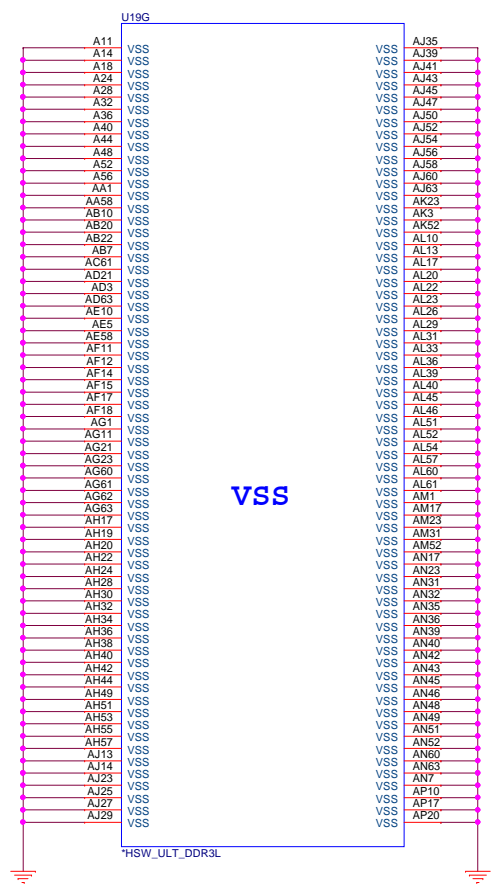


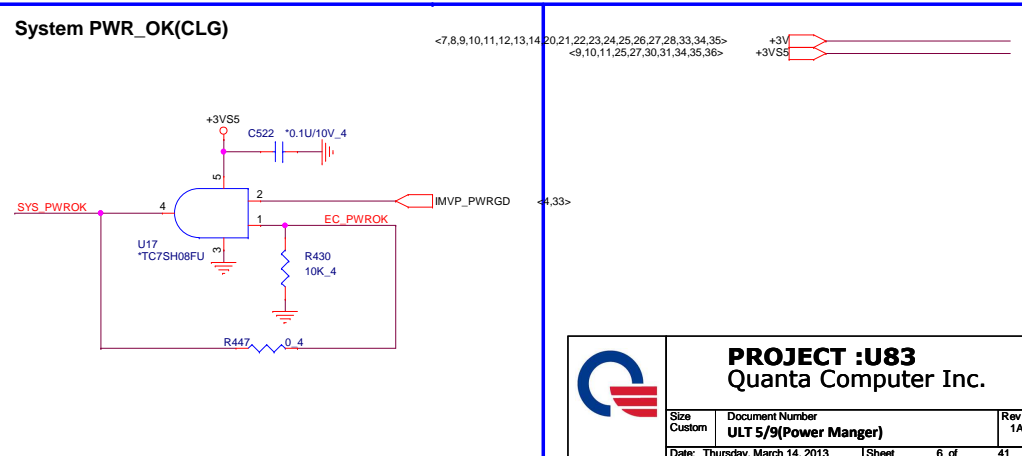
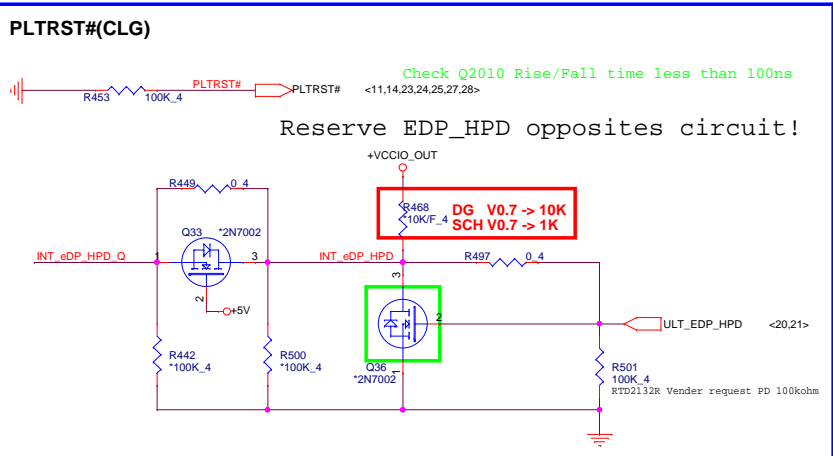
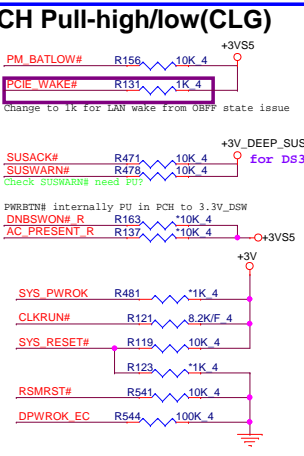
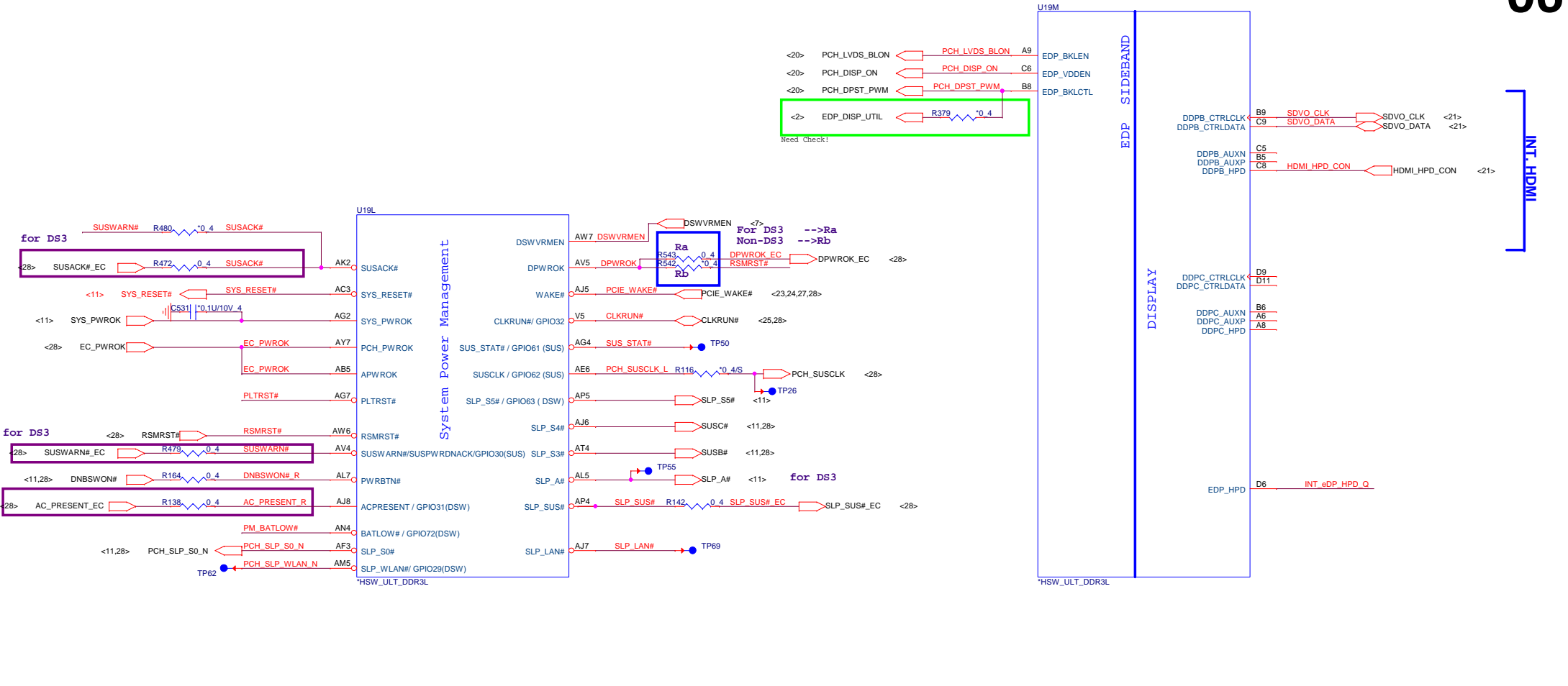
Processor Strapping The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physical Debug Enable) DFX_Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	
CFG4 (DP Presence Strap)	Disable: No physical DP attached to eDP	Enable: An ext DP device is connected to eDP	

PROJECT :U83
Quanta Computer Inc.

Size Custom Document Number 04 - ULT 3/9 (POWER-1) Rev 1A
Date: Thursday, March 14, 2013 Sheet 4 of 41

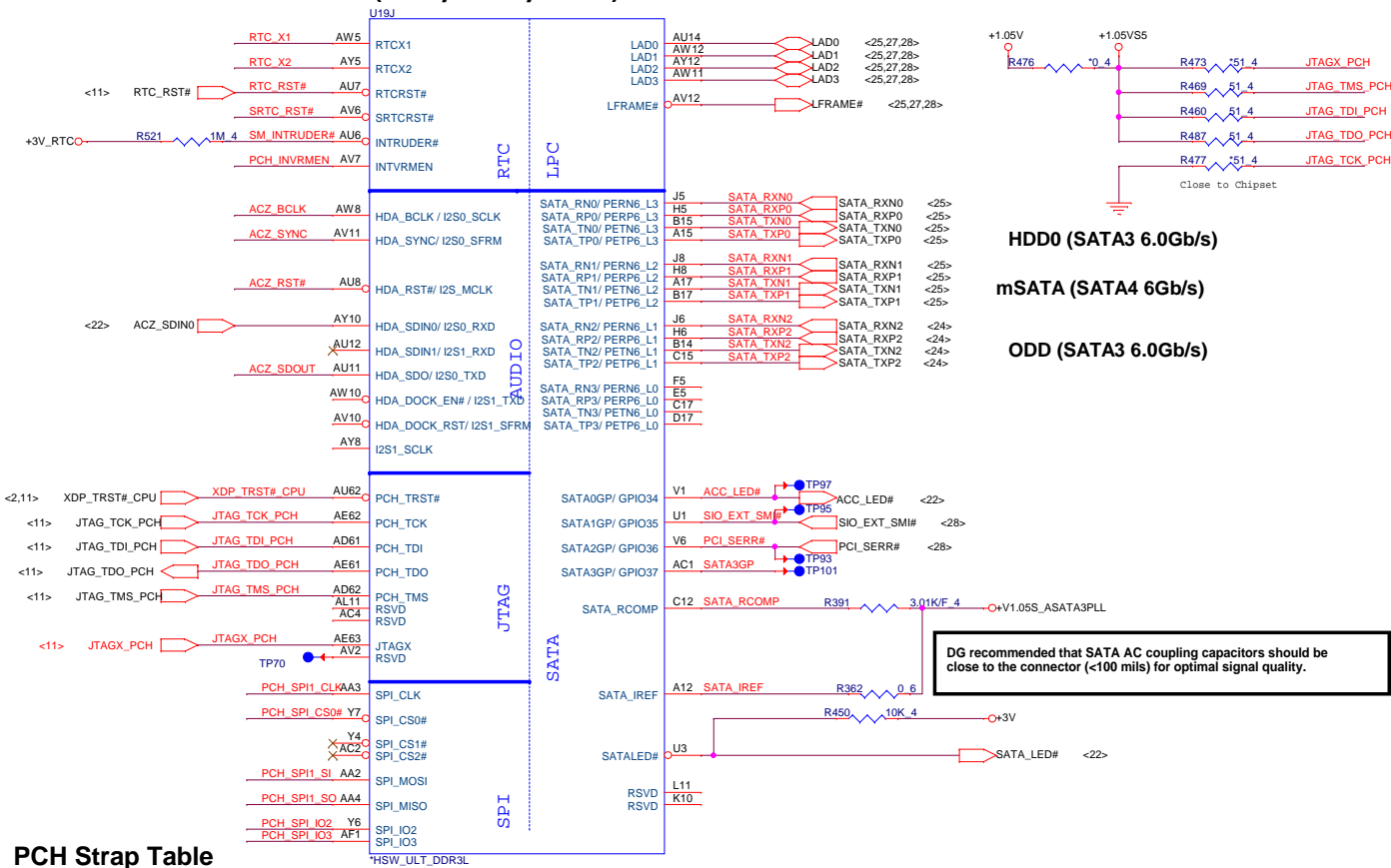




PROJECT :U83
Quanta Computer Inc.

Size Custom	Document Number ULT 5/9(Power Manger)	Rev 1A
Date: Thursday, March 14, 2013	Sheet 6 of 41	

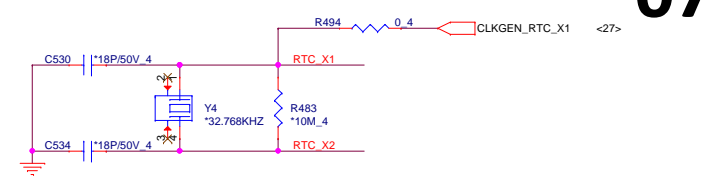
Lynx Point-LP Platform Controller Hub (HDA, JTAG, SATA)



PCH Strap Table

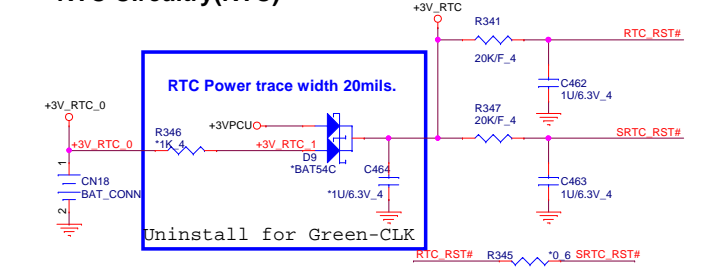
Pin Name	Strap description	Sampled	Configuration	Circuit																
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V → R455 (*1K 4) → SPKR <9>																
SDIO_D0 / GPIO66	Top-Block Swap	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	GPIO66_UL0 <9>																
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC → R519 (330K 4) → PCH_INVRMEN																
HDA_SDO / I2S0_TXD	Flash Descriptor Security Only for Interposer	PWROK	0 = Default (weak pull-down 20K) 1 = Can be Overridden	<28> GPIO33_EC → R182 (1K 4) → ACZ_SDOU0																
GSPI0_MOSI / GPIO86	Boot BIOS Selection	PWROK	<table border="1"> <thead> <tr> <th>GNT0#</th> <th>Boot Location</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>LPC</td> </tr> <tr> <td>0</td> <td>SPI(Default)</td> </tr> </tbody> </table>	GNT0#	Boot Location	1	LPC	0	SPI(Default)											
GNT0#	Boot Location																			
1	LPC																			
0	SPI(Default)																			
GPIO15	TLS Confidentiality	PWROK	0 = ME Crypto Transport Layer Security cipher suite with no confidentiality(Default) 1 = Intel ME Crypto TLS cipher suite with confidentiality	+3V_DEEP_SUS → R125 (*1K 4) → GPIO15_UL0 <9>																
DSWVRMEN	Deep Sx Well On-Die Voltage Regulator Enable	ALWAYS	Should be always pull-up	+3V_RTC → R520 (330K 4) → DSWVRMEN <6>																
				<table border="0"> <tr> <td><28></td> <td>PCH_SPI_CS0# R</td> <td>→</td> <td>PCH_SPI_CS0# R</td> </tr> <tr> <td><28></td> <td>PCH_SPI_CLK R</td> <td>→</td> <td>PCH_SPI_CLK R</td> </tr> <tr> <td><28></td> <td>PCH_SPI_SI R</td> <td>→</td> <td>PCH_SPI_SI R</td> </tr> <tr> <td><28></td> <td>PCH_SPI_SO R</td> <td>→</td> <td>PCH_SPI_SO R</td> </tr> </table>	<28>	PCH_SPI_CS0# R	→	PCH_SPI_CS0# R	<28>	PCH_SPI_CLK R	→	PCH_SPI_CLK R	<28>	PCH_SPI_SI R	→	PCH_SPI_SI R	<28>	PCH_SPI_SO R	→	PCH_SPI_SO R
<28>	PCH_SPI_CS0# R	→	PCH_SPI_CS0# R																	
<28>	PCH_SPI_CLK R	→	PCH_SPI_CLK R																	
<28>	PCH_SPI_SI R	→	PCH_SPI_SI R																	
<28>	PCH_SPI_SO R	→	PCH_SPI_SO R																	

RTC Clock 32.768KHz

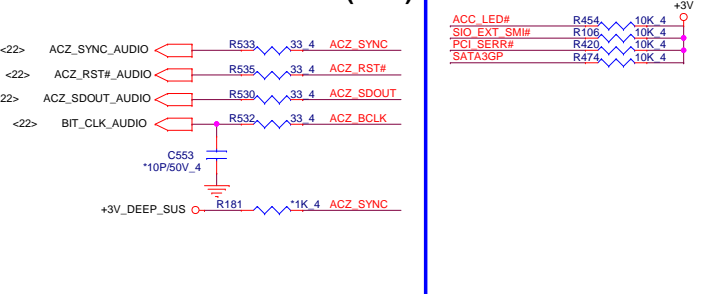


no stuff if use green Clock

RTC Circuitry(RTC)



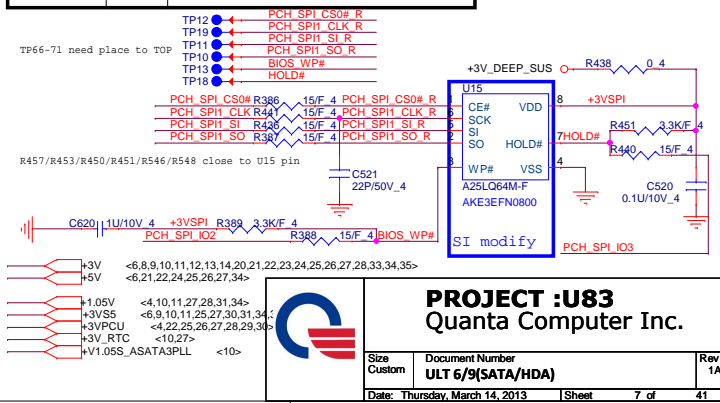
HDA Bus(CLG)



GPIO Pull UP



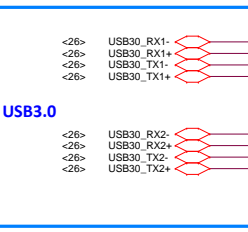
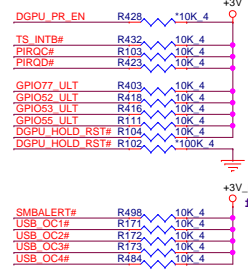
Vender	Size	P/N	PCH SPI ROM(CLG)
AMIC	8MB	AKE3EFN0800 (A25LQ64M-F)	
Winbond	8MB	AKE3EPF0N07 (W25Q64FVSSIQ)	
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)	
Socket		DFHS08FS023	



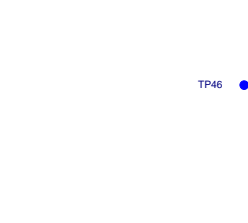
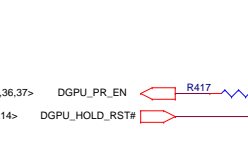
PROJECT :U83
Quanta Computer Inc.

Lynx Point-LP Platform Controller Hub (HDA, JTAG, SATA)

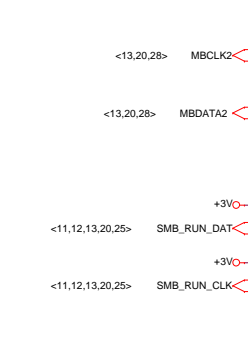
PCI/USBOC# Pull-up(CLG)



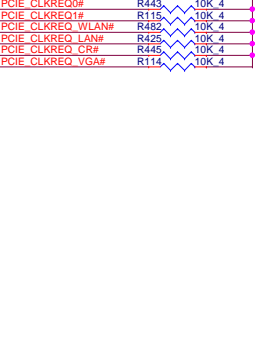
20111130 Modify USB3.0 for HM70



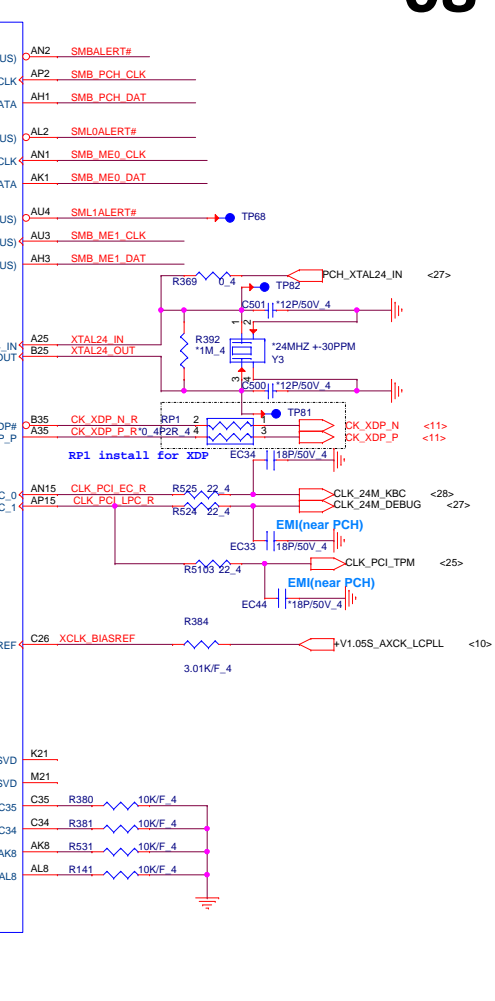
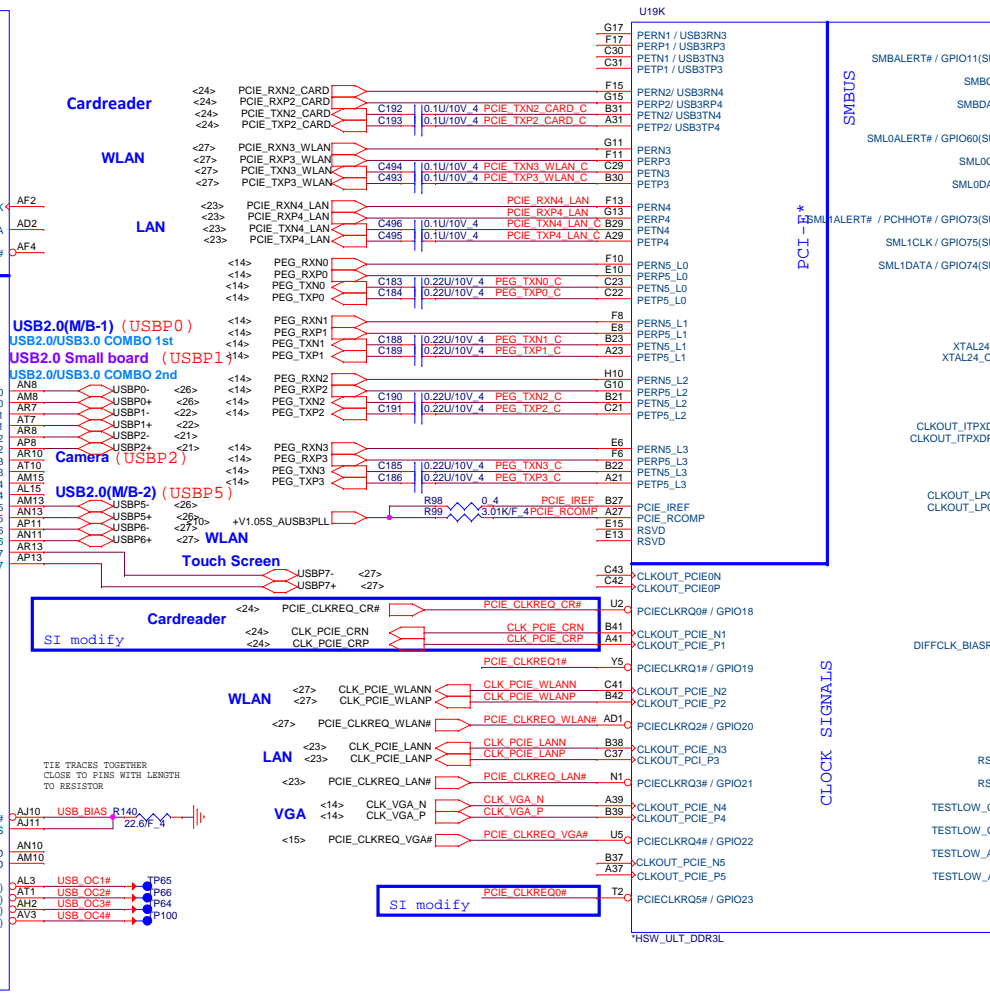
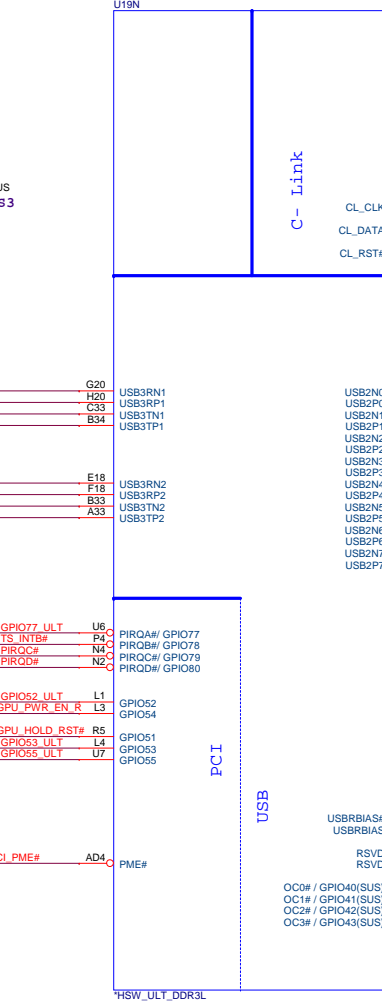
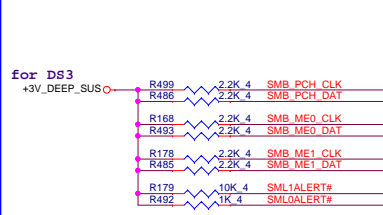
SMBus/Pull-up(CLG)



CLK_REQ/Strap Pin(CLG)



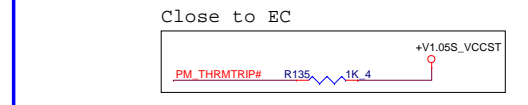
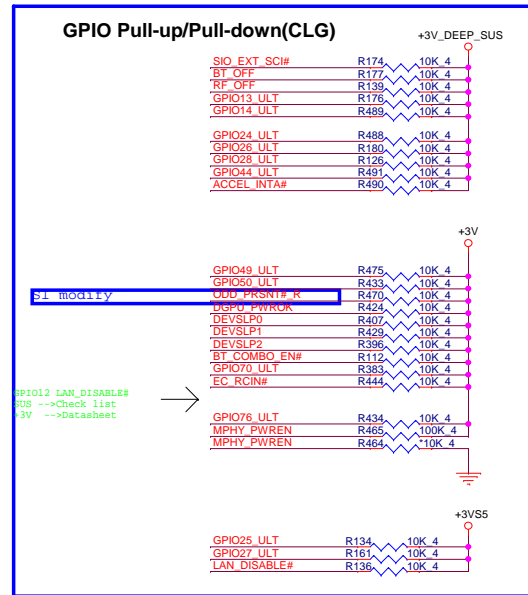
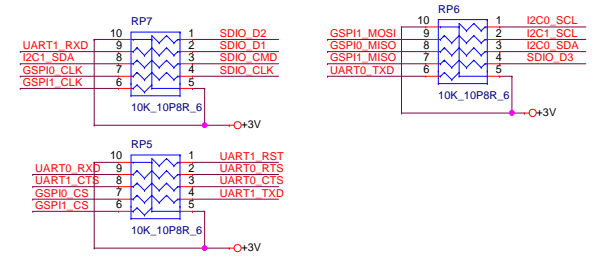
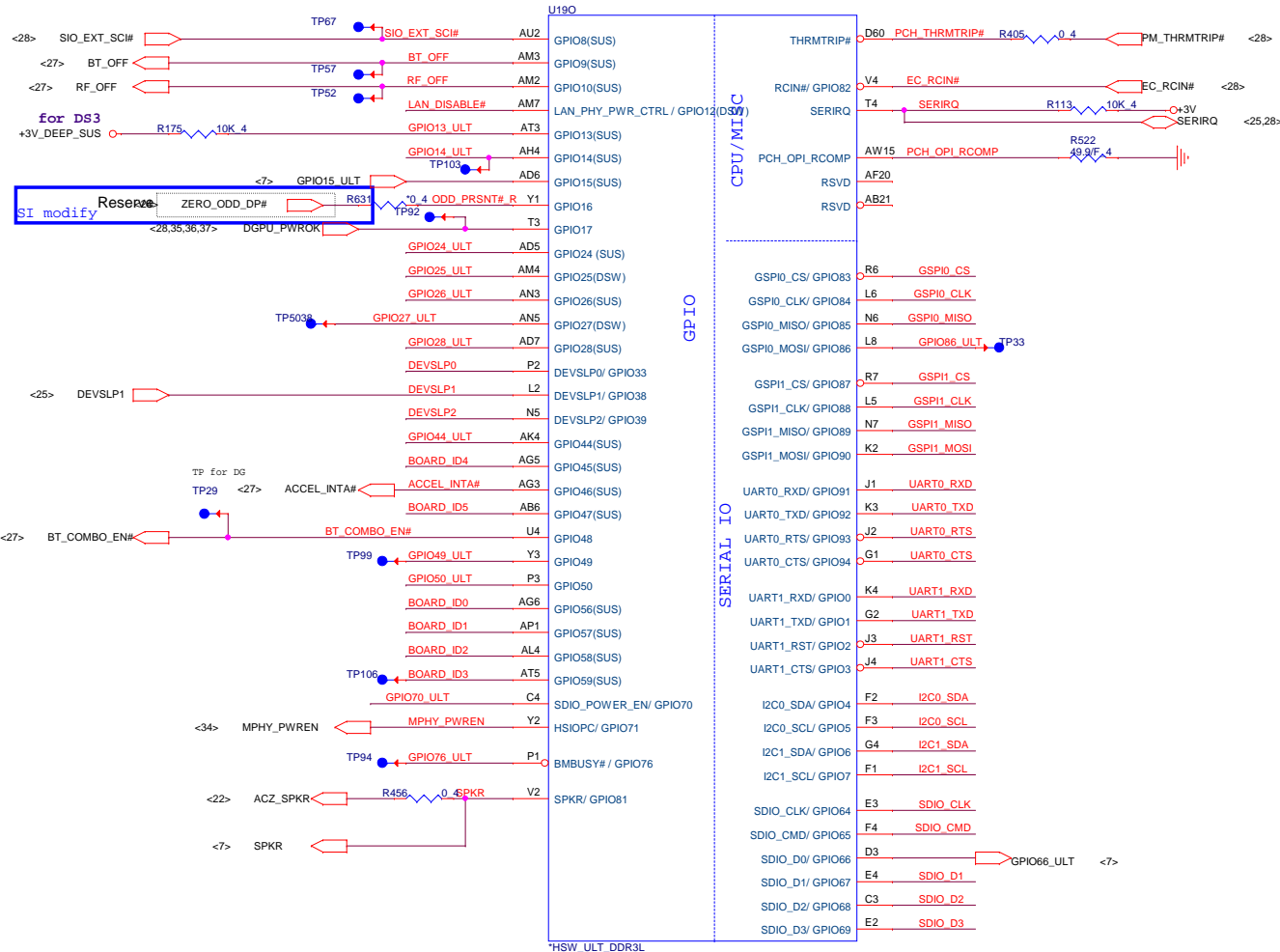
SMBus/Pull-up(CLG)



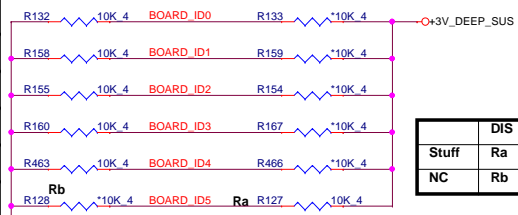
PROJECT :U83
Quanta Computer Inc.
 Size Custom
 Document Number **ULT 7/9 (PCIe/USB/CLK)**
 Date: Thursday, March 14, 2013
 Sheet 8 of 41

Lynx Point-LP Controller Hub (HDA,JTAG,SATA) Haswell (GPIO)

09



Model	BOARD_ID5 UMA:0 DIS:1	BOARD_ID4 14:0 15:1	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
U83 DIS-14	1	0	0	0	0	0
U83 UMA-15	0	1	0	0	0	0
	0	0	0	0	0	0
	0	0	0	0	0	0
	0	0	0	0	0	0
	0	0	0	0	0	0



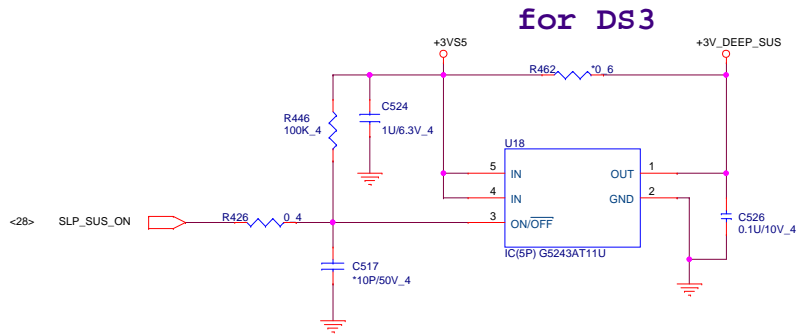
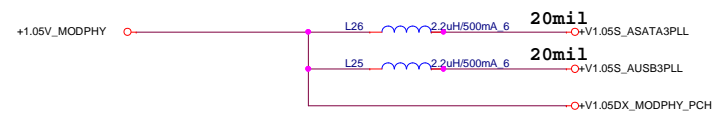
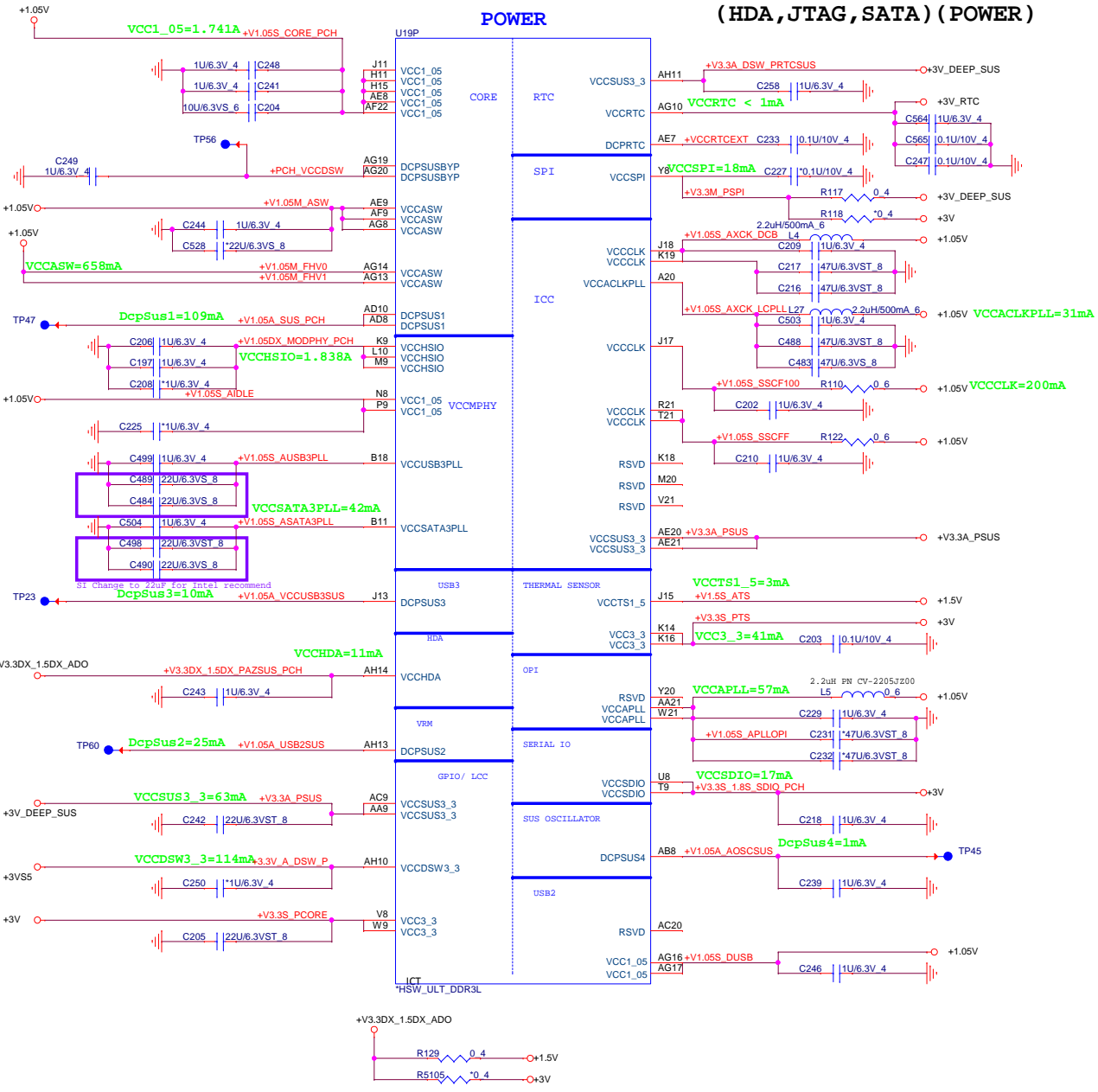
	DIS	UMA
Stuff	Ra	Rb
NC	Rb	Ra

<6,7,8,10,11,12,13,14,20,21,22,23,24,25,26,27,28,33,34,35> +3V
 <6,10,11,25,27,30,31,34,35,36> +3VSS

PROJECT :U83
Quanta Computer Inc.

Size Custom	Document Number ULT 8/9 (GPIO/MISC)	Rev 1A
Date: Thursday, March 14, 2013	Sheet 9 of	41

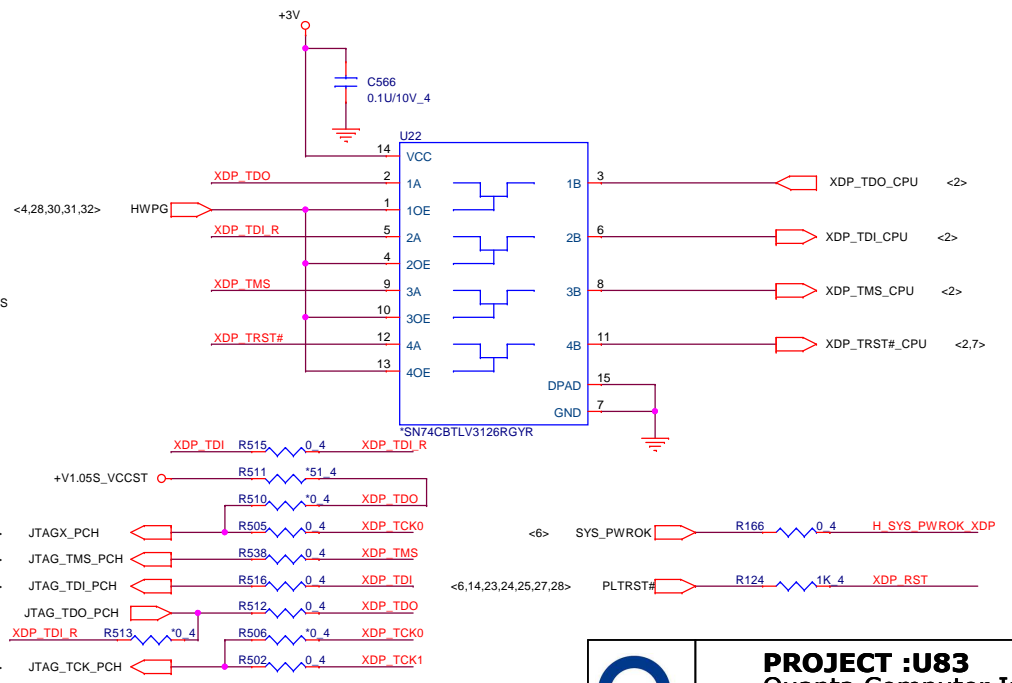
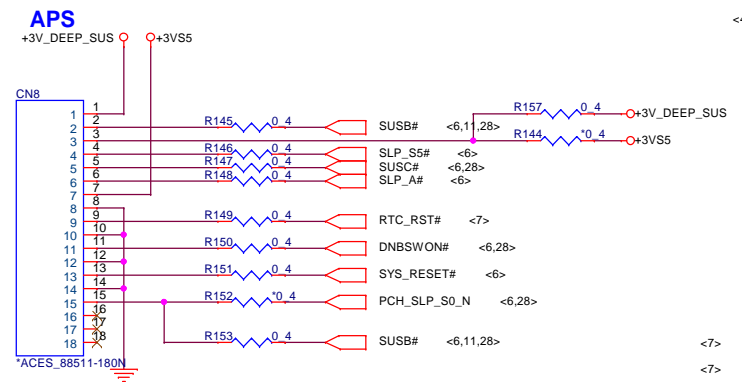
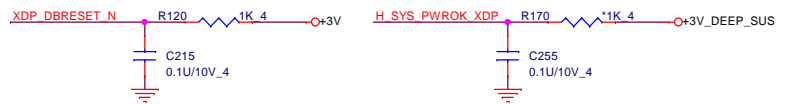
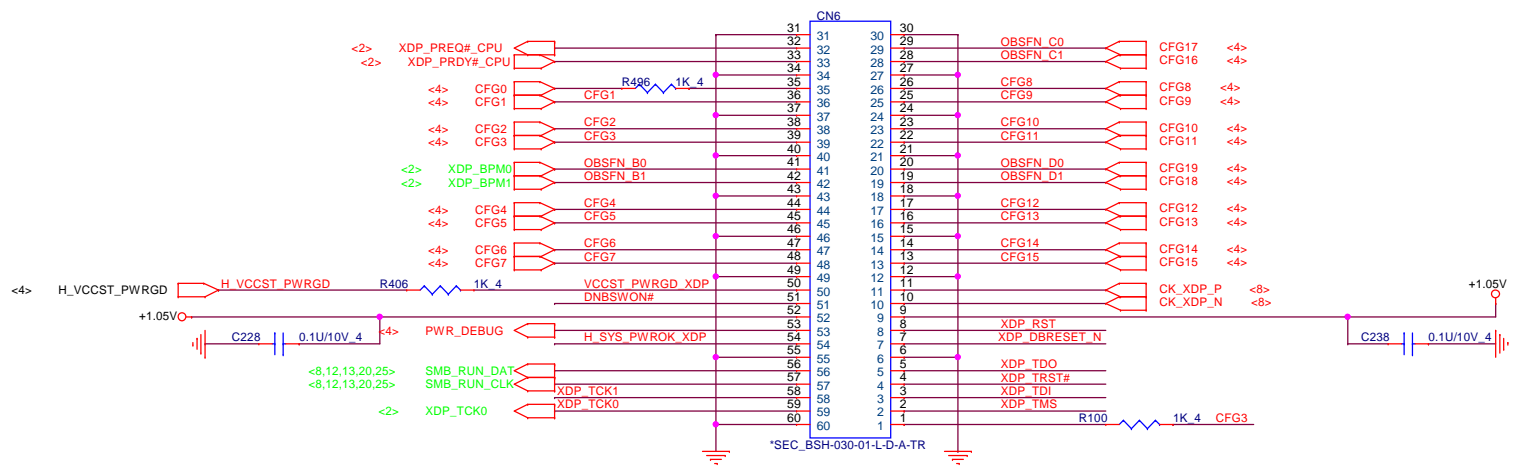
Lynx Point-LP Platform Controller Hub (HDA, JTAG, SATA) (POWER)




<6,7,8,9,11,12,13,14,20,21,22,23,24,25,26,27,28,33,34,35>	+3V	<8>	+V1.05S_AUSB3PLL
<6,7,11,22,24,25,26,27,34>	+5V	<7>	+V1.05S_ASATA3PLL
<4,7,11,27,28,31,34>	+1.05V	<7,27>	+3V_RTC
<6,9,11,25,27,30,31,34,35,36>	+3VS5	<2,4,12,13,25,32>	+1.35VSUS
<13,22,25,26,30,32,33,34,35,36,37>	+5VS5		

PROJECT :U83
Quanta Computer Inc.

Size Custom	Document Number ULT 9/9(Power-2)	Rev 1A
Date: Monday, March 18, 2013	Sheet 10 of	41

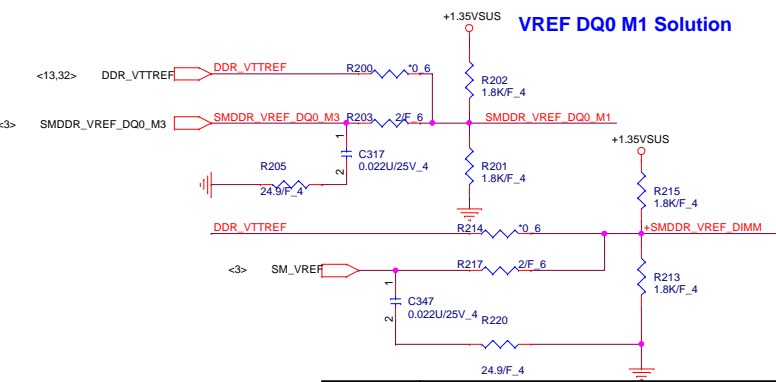
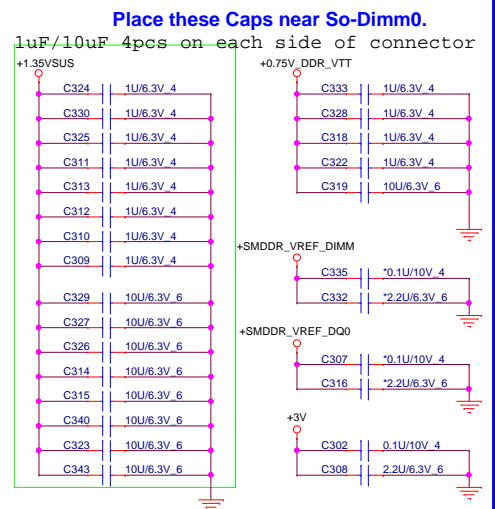
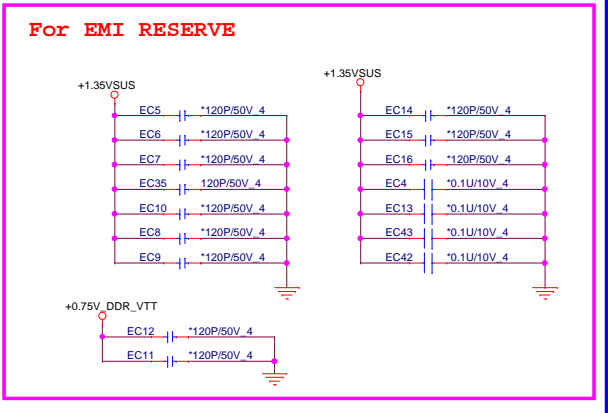
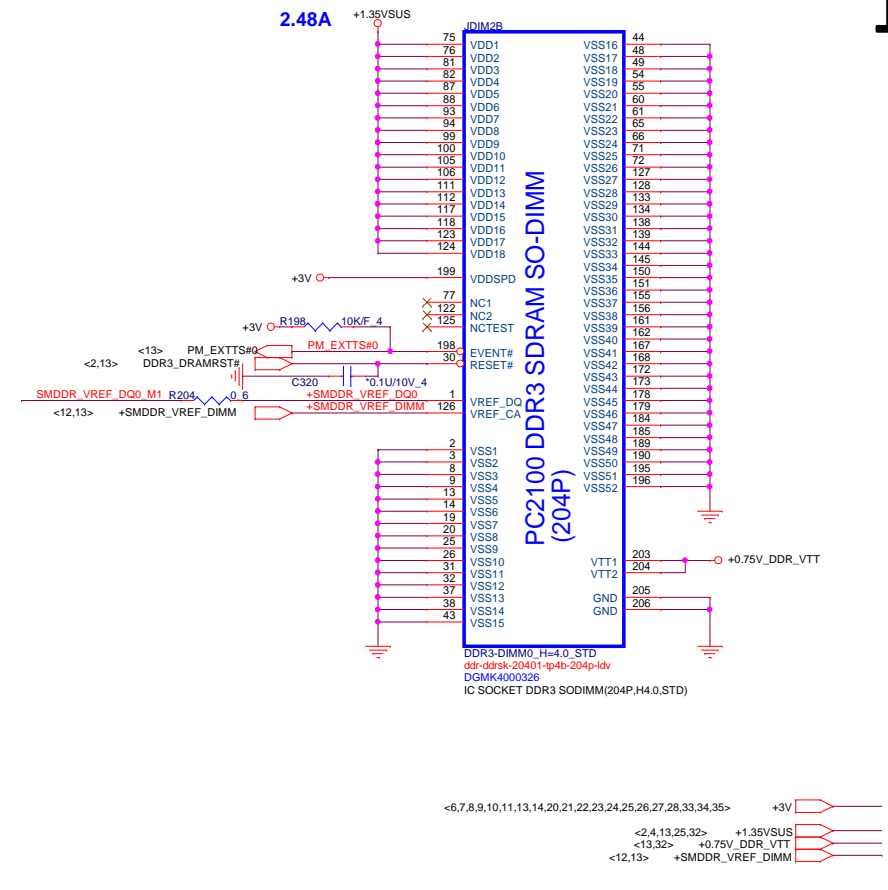
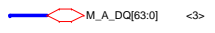
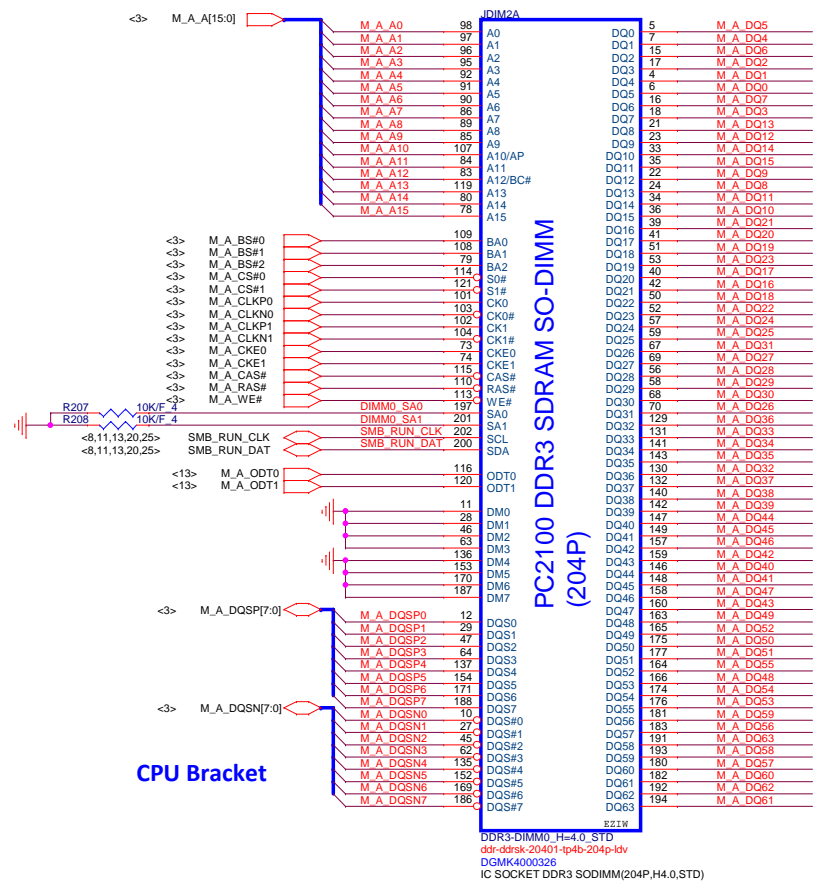




PROJECT :U83
Quanta Computer Inc.
ULT

Size	Document Number	Rev
	HSW XDP & APS	1A

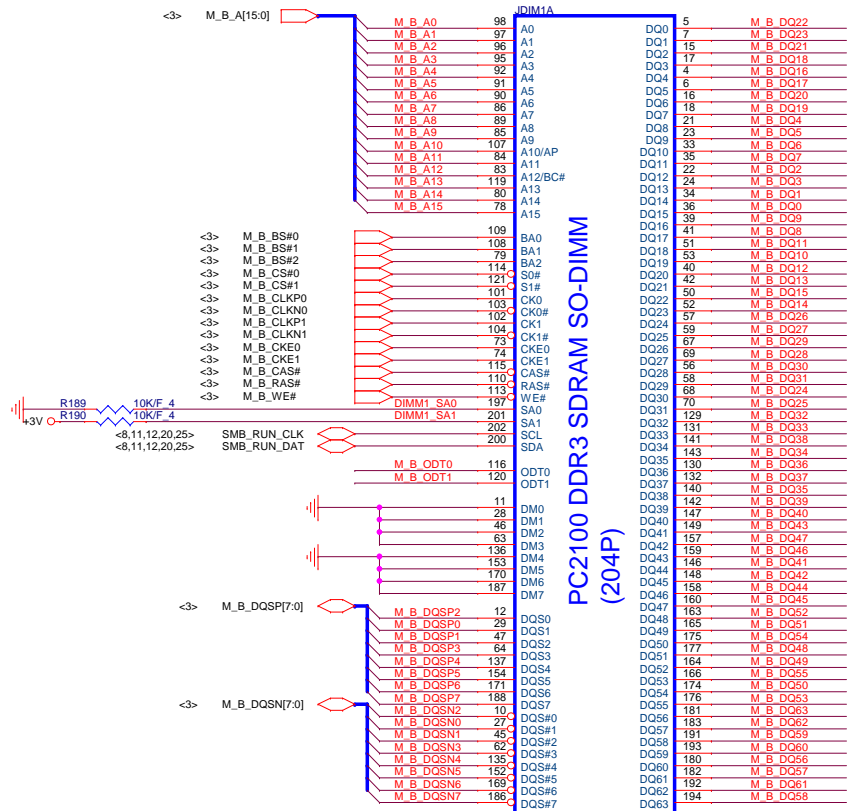
Thursday, March 14, 2013 11:51 AM



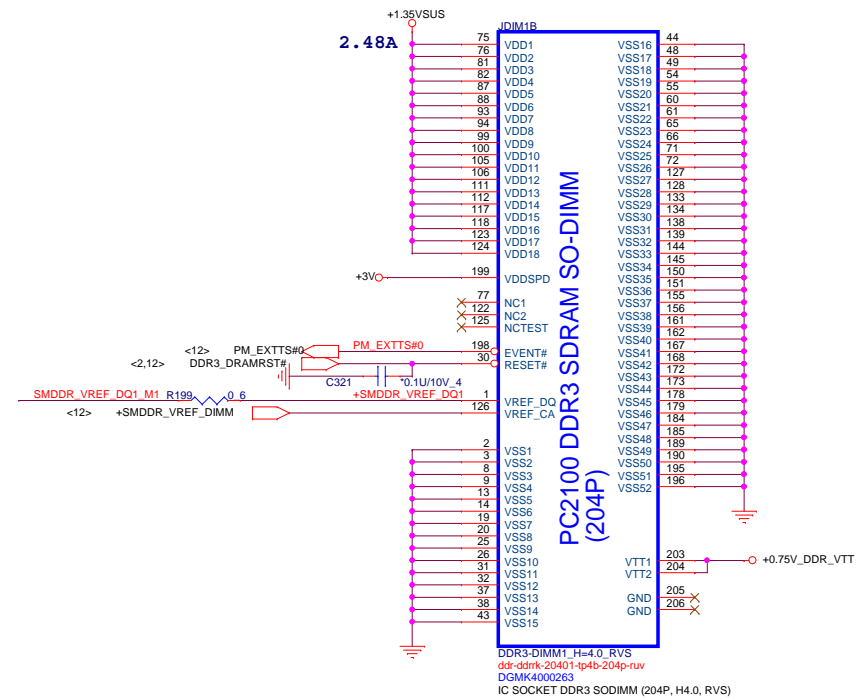
PROJECT :U83
 Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM0-STD(4.0H)	1A
Date: Thursday, March 14, 2013	Sheet	12 of 41

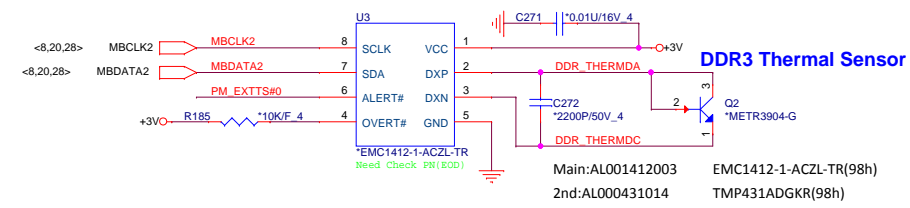
M_B_DQ[63:0] <->



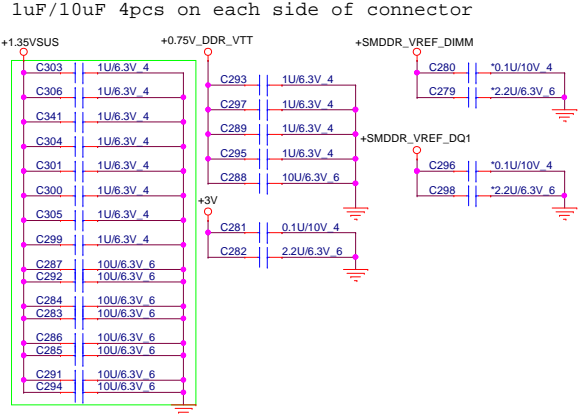
DDR3-DIMM1_H=4.0_RVS
 ddr-ddr3k-20401-tp4b-204p-ruv
 DGMK4000263
 IC SOCKET DDR3 SODIMM (204P, H4.0, RVS)



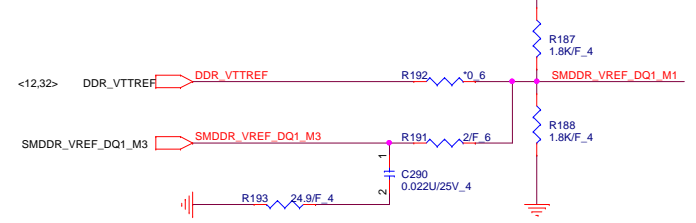
Local Thermal Sensor



Place these Caps near So-Dimm1.

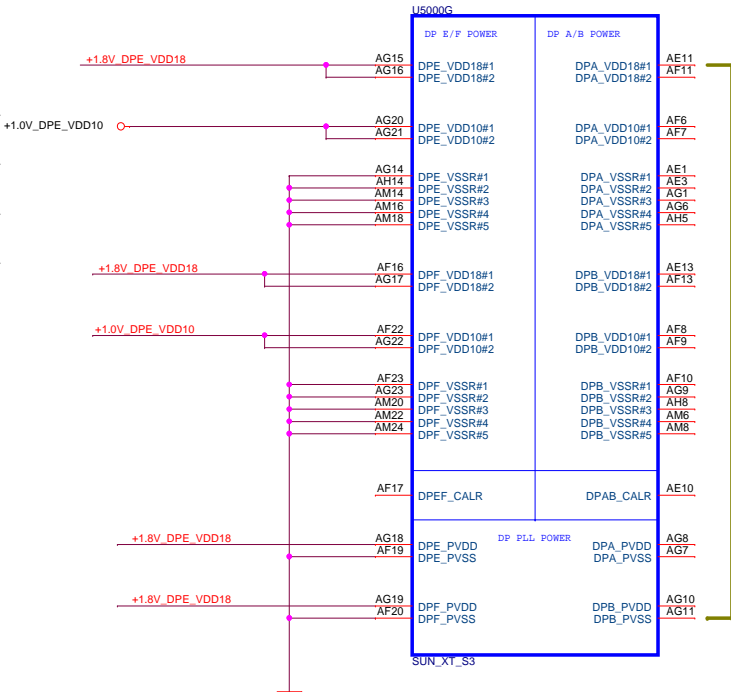
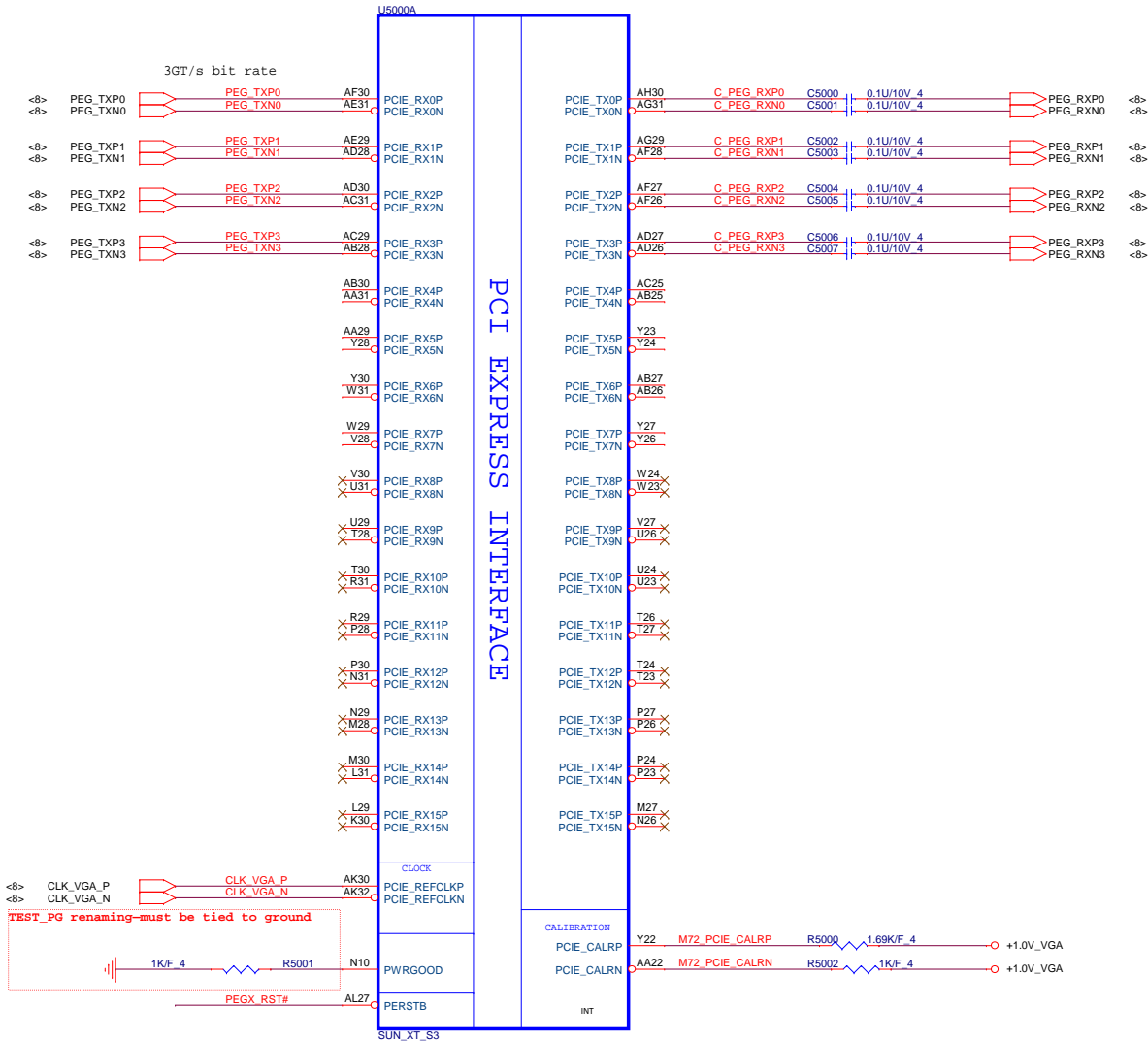


VREF DQ1 M1 Solution

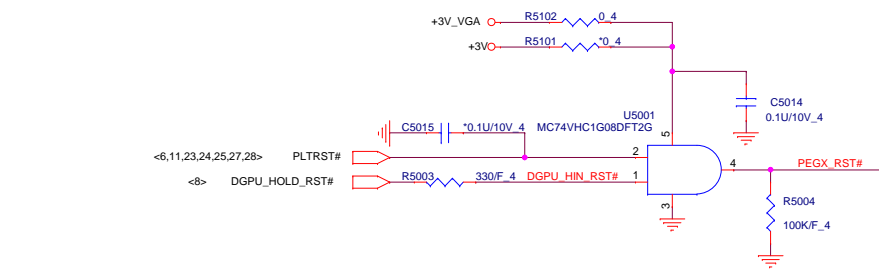
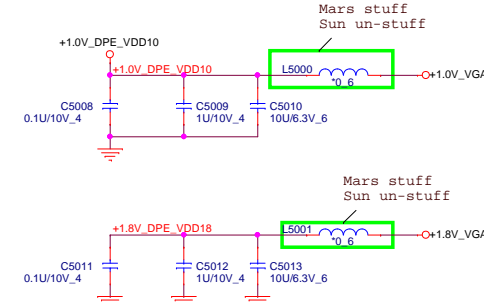


PROJECT :U83
 Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM1-RV5(4.0H)	1A
Date:	Thursday, March 14, 2013	Sheet 13 of 41



NC for Mars & Sun

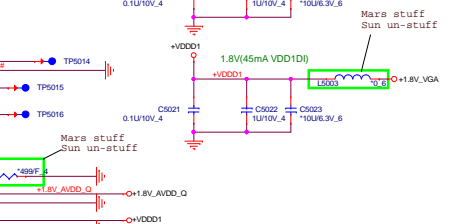
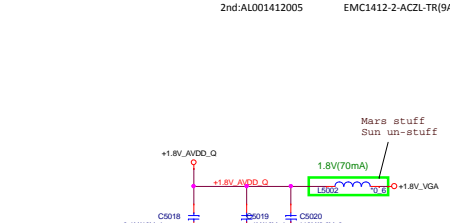
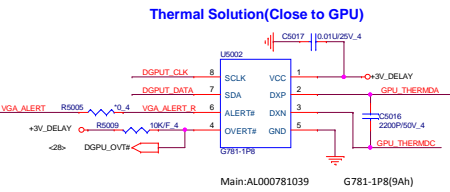
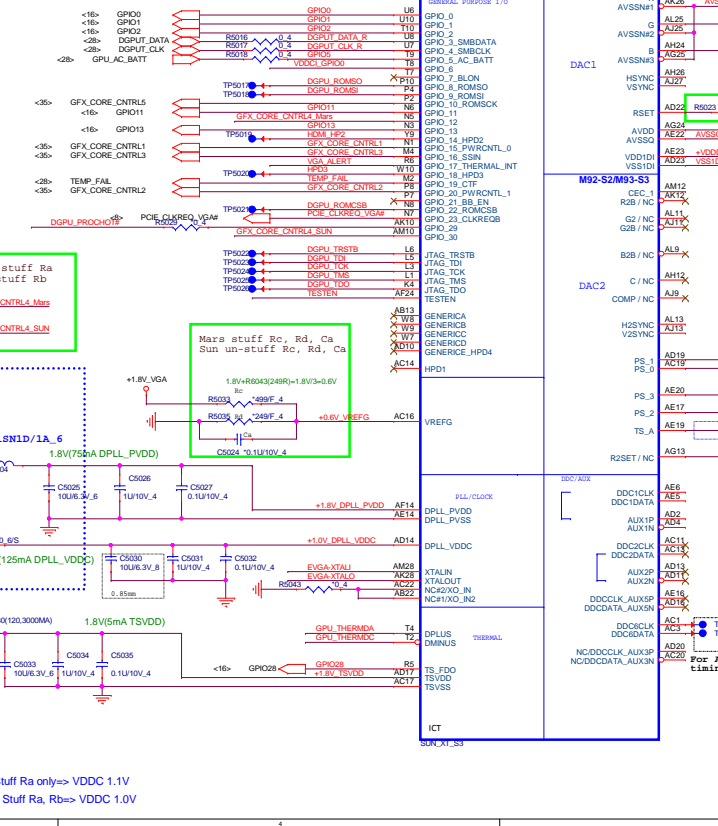
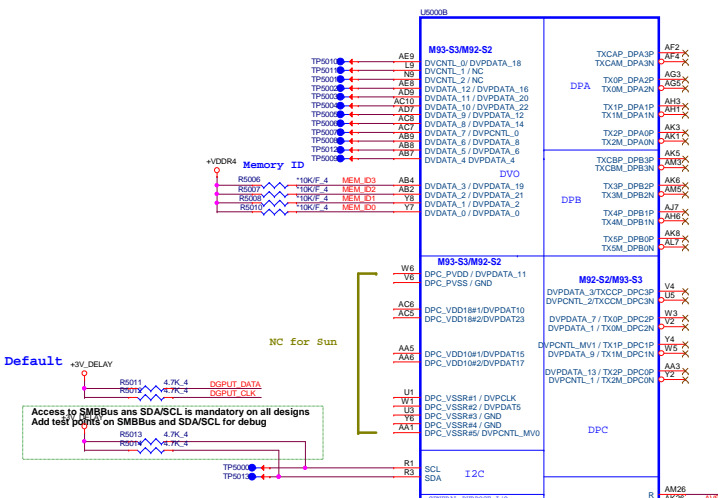


Legend: \Rightarrow +1.0V_VGA, \Rightarrow +1.8V_VGA, \Rightarrow <15,17,36>, \Rightarrow <15,17,27,36>

PROJECT :U83
Quanta Computer Inc.

Size Custom	Document Number Sun S3 PCIe Interface	Rev 1A
Date: Thursday, March 14, 2013 Sheet 14 of 41		

GPIO10	GPIO30	GPIO16	GPIO20	GPIO15	Sun XT
PWRCTRL5	PWRCTRL4	PWRCTRL3	PWRCTRL2	PWRCTRL1	1.175V
0	1	1	0	1	1.150V
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	1	0.800V
1	1	1	0	0	0.775V

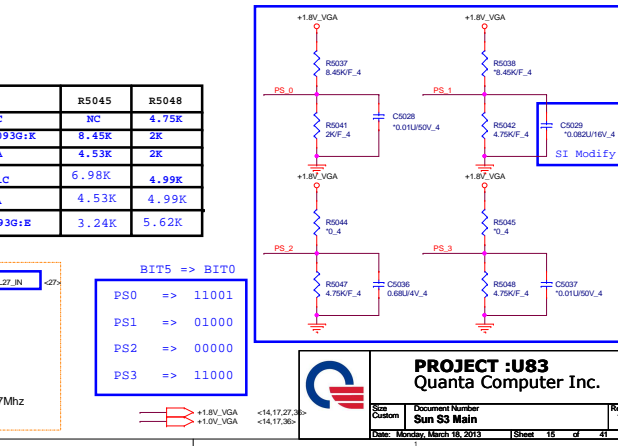
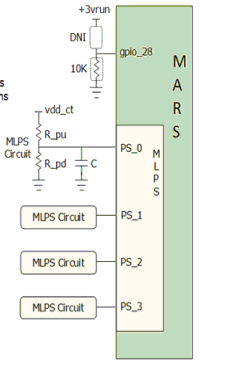


PS_3[3:1]	Vendor	Type	Vendor P/N	R5045	R5048
000	Hynix- F(Ruma)	128Mx16 *4, 900Mhz	H5TC2663FPR-11C	NC	4.75K
001	Micron- V89C/K	128Mx16 *4, 900Mhz	MT41J128M16JT-093G:K	8.45K	2K
010	Samsung- E die	128Mx16 *4, 900Mhz	K4W2G1646E-BC1A	4.53K	2K
011	Hynix- Huma die	256Mx16 *4, 900Mhz	H5TC463FAPR-11C	6.98K	4.99K
100	Samsung- E die	256Mx16 *4, 900Mhz	K4W4G1646B-HCL1A	4.53K	4.99K
101	Micron- E	256Mx16 *4, 900Mhz	MT41J256M16HA-093G:E	3.24K	5.62K

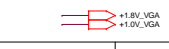
- ### MLPS Implementation
- Connect GPIO_28 to 10K pulldown to enable MLPS
 - If any of PS_0,1,2 is not used, leave "no connect"
 - R_pu, R_pnd and C must be properly populated per tables below
 - Place MLPS circuit components as close to the ASIC as possible
 - Total DC resistance of trace between PS pin and C should be less than 2 ohms
 - Total DC resistance of trace between C and ground should be less than 2 ohms
 - Trace capacitance should be less than 100pF. Resistors should be +/- 1% tolerance

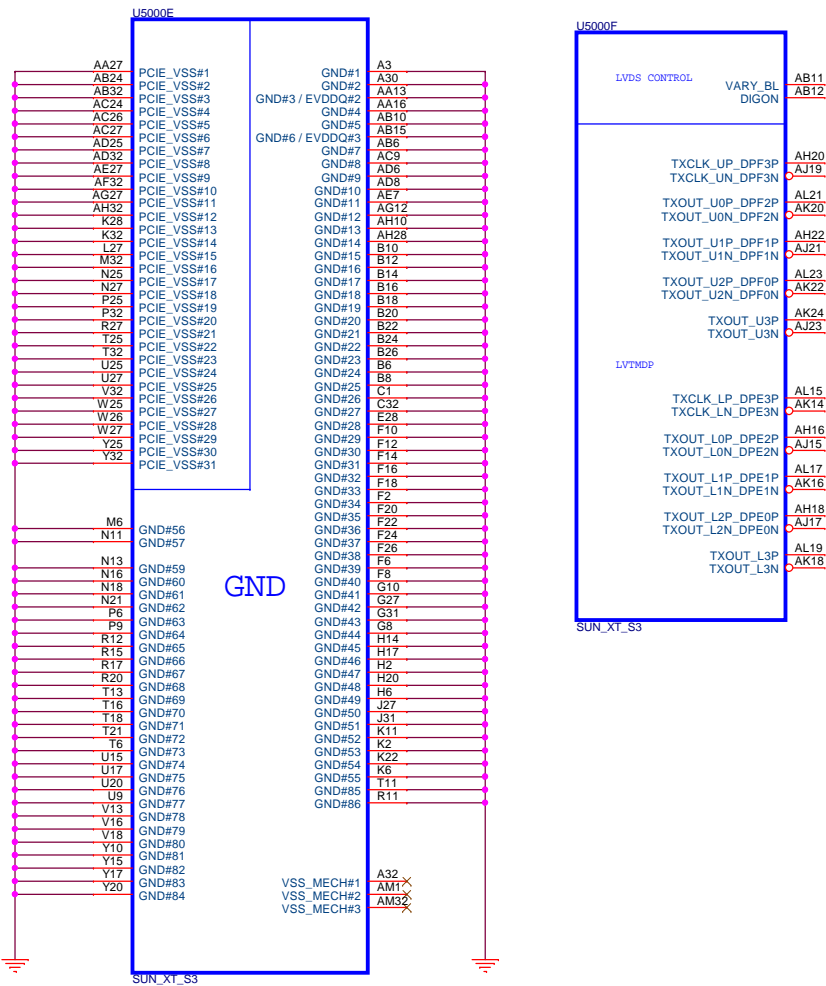
Capacitor Lookup Table		Resistor Divider Lookup Table		
C (nF)	Bits(5,4)	R_pu (Ohm)	R_pnd (Ohm)	Bits(3,2,1)
680	00	NC	4750	000
82	01	8450	2000	001
10	10	4530	2000	010
NC	11	6980	4990	011
		4530	4990	100
		3240	5620	101
		3400	10000	110
		4750	NC	111

Pin/Bit	Name	Description	Default	Legacy
PS_0[3:1]	romidfg[2:0]	Memory aperture size or ROM type select: If bios_rom_en = 0, romidfg[2:0] define memory aperture size. If bios_rom_en = 1, romidfg[2:0] define ROM type	xxx	gpio_13 gpio_12 gpio_11
PS_0[4]	n/a	Reserved		1
PS_1[1]	bif_gen3_en_a	PCIe Gen3 capability: 1=Gen3 supported, 0=Gen3 not supported	x	gpio_2
PS_1[2]	bif_clk_pm_en	PCIe CLK PM capability: 1 = CLKREQB supported	x	gpio_8
PS_1[3]	n/a	Reserved		genclk_vsync
PS_1[4]	tx_pwrs_enb	PCIe Tx power savings: 0=50% swing, 1=full swing	x	gpio_0
PS_1[5]	tx_deemph_en	PCIe Tx de-emphasis: 1=Tx de-emphasis enabled	x	gpio_1
PS_2[1]	n/a	Reserved		n/a
PS_2[2]	n/a	Reserved		n/a
PS_2[3]	bios_rom_en	Enable external BIOS ROM: 1=External ROM connected	x	gpio_22
PS_2[4]	vga_dis	VGA disable: 1=Disable this GPU as the system's VGA controller	0	gpio_9
PS_2[5]	n/a	Reserved		n/a
PS_3[1]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[2]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[3]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[5] PS_3[4] PS_0[5]	aud_port_cp[2] aud_port_cp[1] aud_port_cp[0]	3-bit field indicating number of audio-capable display outputs	xxx	n/a



BIT5 => BIT0	
PS0 => 11001	
PS1 => 01000	
PS2 => 00000	
PS3 => 11000	





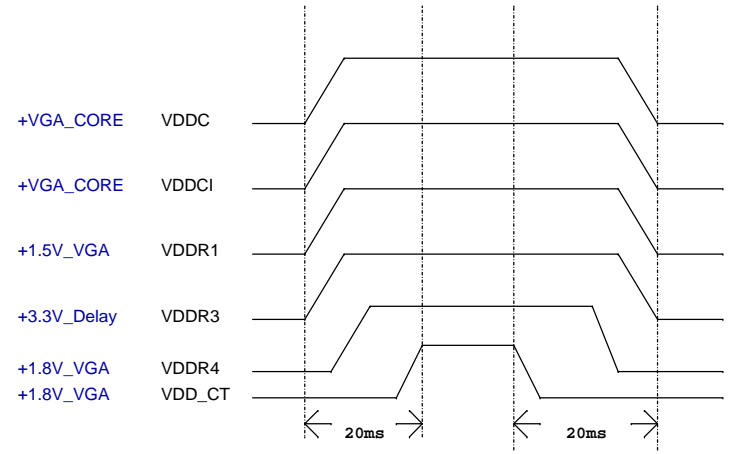
CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRs_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	0
RSVD	GPIO2	RESERVED	X
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIOQ[13:1]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSNC	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS
ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21 H2SYNC GENERICC GPIO8 GPIO2

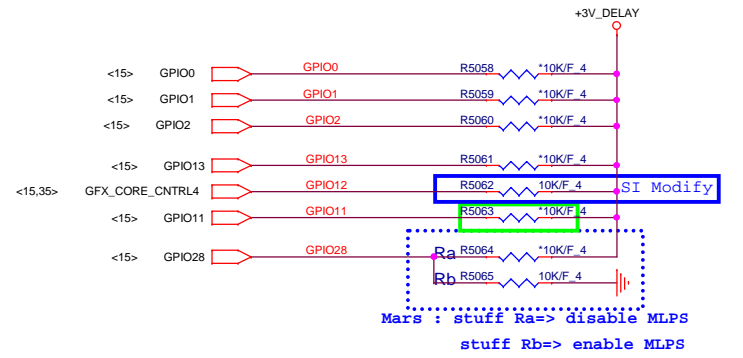
Power Up/Down Sequence



Memory Aperture size(Seymour)

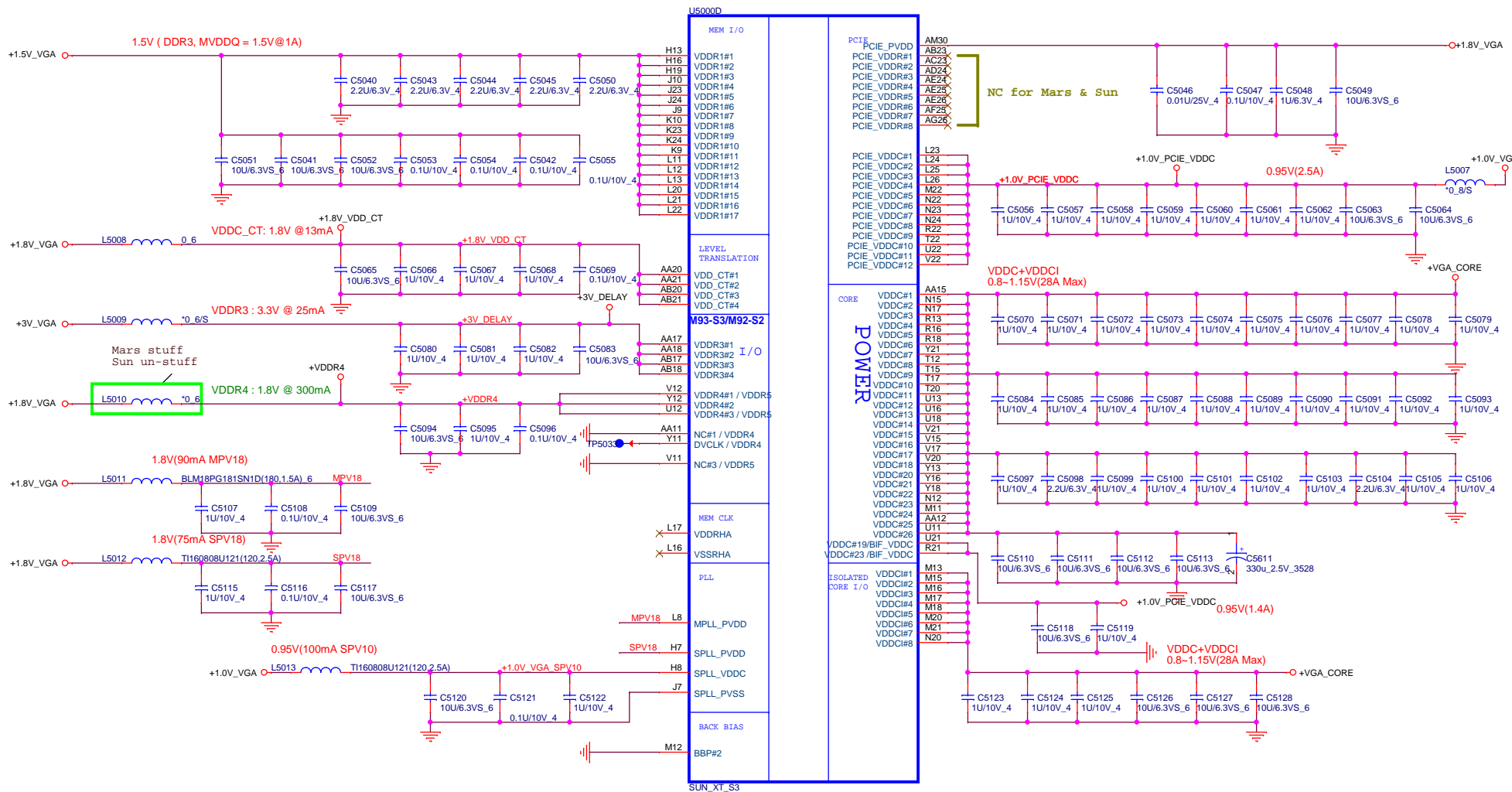
GPIO9 BIOSROM	GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0
0	256M	0	1
0	64M	0	0
0	32M	0	1
0	512M	1	0
0	1G	1	0
0	2G	1	1
0	4G	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.



PROJECT :U83
Quanta Computer Inc.

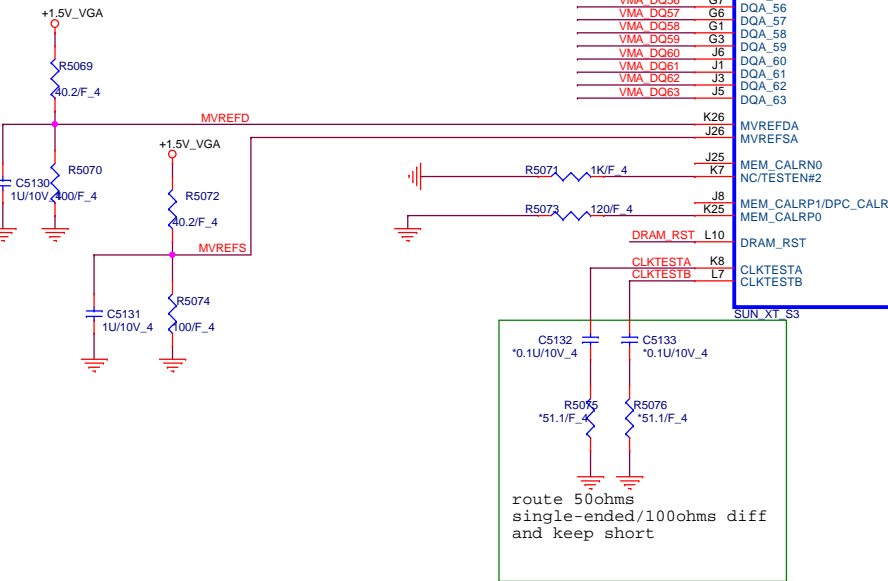
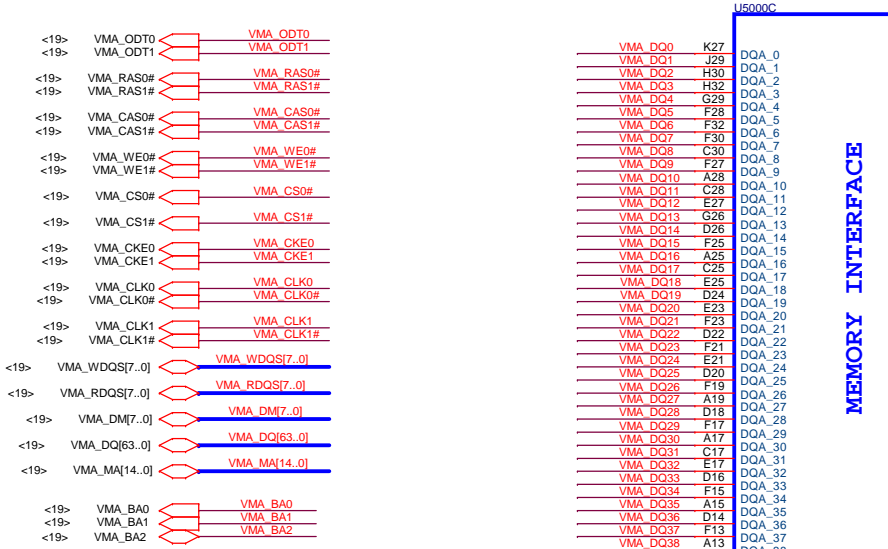
Size Custom Document Number Sun S3 GND / LVDS/ Straps Rev 1A
 Date: Thursday, March 14, 2013 Sheet 16 of 41



- +1.5V_VGA <18,19,37>
- +1.8V_VGA <14,15,27,36>
- +1.0V_VGA <14,15,36>
- +VGA_CORE <35,36>
- +3V <6,7,8,9,10,11,12,13,14,20,21,22,23,24,25,26,27,28,33,34,35>
- +5V <6,21,22,24,25,26,27,34>

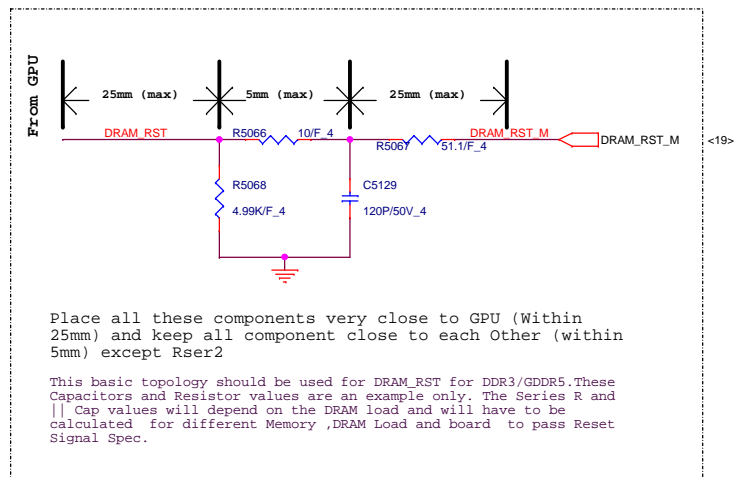
PROJECT :U83
Quanta Computer Inc.

Size Custom	Document Number Sun S3 Power_and_NC	Rev 1A
Date: Thursday, March 14, 2013 Sheet 17 of 41		



MEMORY INTERFACE

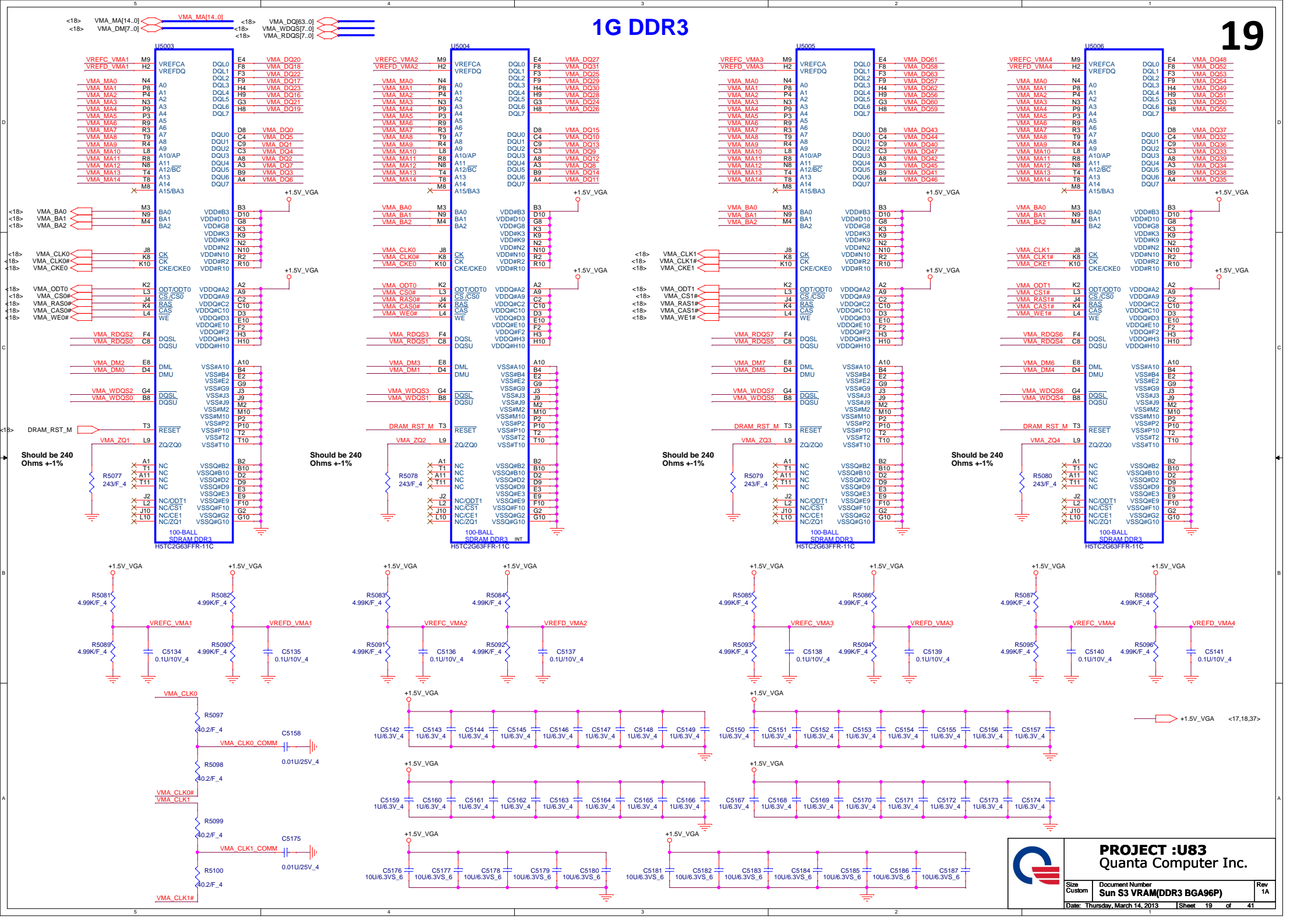
MAA_0	K17	VMA_MA0
MAA_1	J20	VMA_MA1
MAA_2	H23	VMA_MA2
MAA_3	G23	VMA_MA3
MAA_4	G24	VMA_MA4
MAA_5	H24	VMA_MA5
MAA_6	J19	VMA_MA6
MAA_7	K19	VMA_MA7
MAA_8	J14	VMA_MA8
MAA_9	K14	VMA_MA9
MAA_10	J11	VMA_MA10
MAA_11	J13	VMA_MA11
MAA_12	H11	VMA_MA12
MAA_13/BA2	G11	VMA_BA2
MAA_14/BA0	J16	VMA_BA0
MAA_15/BA1	L15	VMA_BA1
DQMA_0	E32	VMA_DM0
DQMA_1	E30	VMA_DM1
DQMA_2	A21	VMA_DM2
DQMA_3	C21	VMA_DM3
DQMA_4	E13	VMA_DM4
DQMA_5	D12	VMA_DM5
DQMA_6	E3	VMA_DM6
DQMA_7	F4	VMA_DM7
RDQSA_0	H28	VMA_RDQS0
RDQSA_1	C27	VMA_RDQS1
RDQSA_2	A23	VMA_RDQS2
RDQSA_3	E19	VMA_RDQS3
RDQSA_4	E15	VMA_RDQS4
RDQSA_5	D10	VMA_RDQS5
RDQSA_6	D6	VMA_RDQS6
RDQSA_7	G5	VMA_RDQS7
WDQSA_0	H27	VMA_WDQS0
WDQSA_1	A27	VMA_WDQS1
WDQSA_2	C23	VMA_WDQS2
WDQSA_3	C19	VMA_WDQS3
WDQSA_4	C15	VMA_WDQS4
WDQSA_5	E9	VMA_WDQS5
WDQSA_6	C5	VMA_WDQS6
WDQSA_7	H4	VMA_WDQS7
ODTA0	L18	VMA_ODT0
ODTA1	K16	VMA_ODT1
CLKA0	H26	VMA_CLK0
CLKA0B	H25	VMA_CLK0#
CLKA1	G9	VMA_CLK1
CLKA1B	H9	VMA_CLK1#
RASA0B	G22	VMA_RAS0#
RASA1B	G17	VMA_RAS1#
CASA0B	G19	VMA_CAS0#
CASA1B	G16	VMA_CAS1#
CSA0B_0	H22	VMA_CS0#
CSA0B_1	J22	VMA_CS1#
CSA1B_0	G13	VMA_CS1#
CSA1B_1	K13	VMA_CS1#
CKEA0	K20	VMA_CKE0
CKEA1	J17	VMA_CKE1
WEA0B	G25	VMA_WE0#
WEA1B	H10	VMA_WE1#
PX_EN	AB16	PX_EN
RSVD#2	G14	TP5034
RSVD#3	G20	VMA_MA14



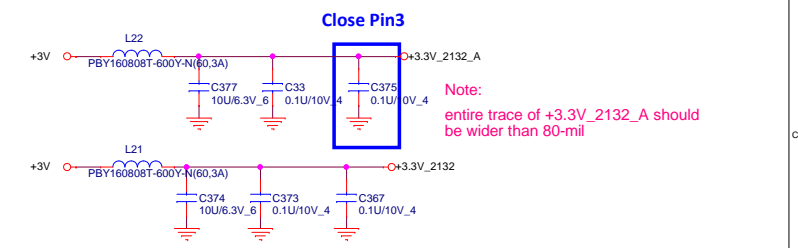
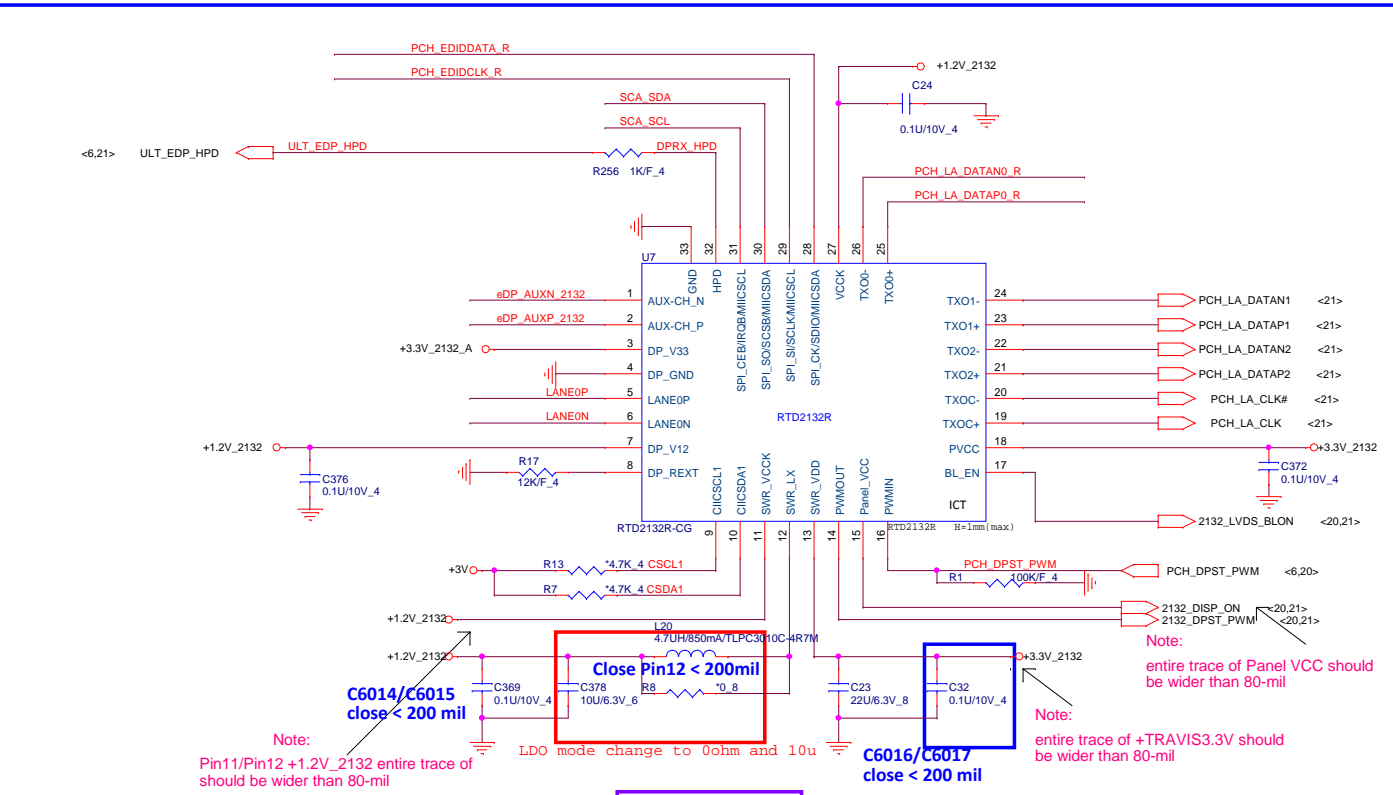
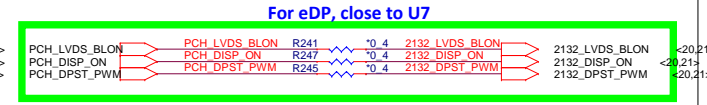
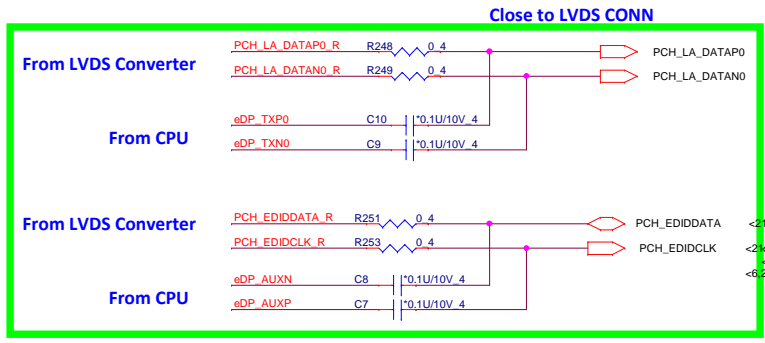
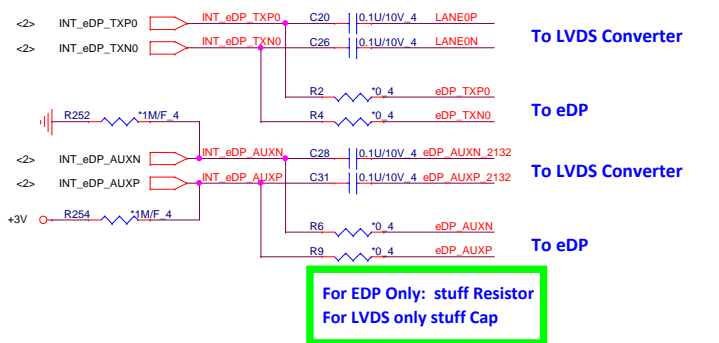
PROJECT :U83
Quanta Computer Inc.

Size Custom	Document Number Sun S3 MEM_Interface	Rev 1A
Date: Thursday, March 14, 2013	Sheet 18 of 41	

1G DDR3

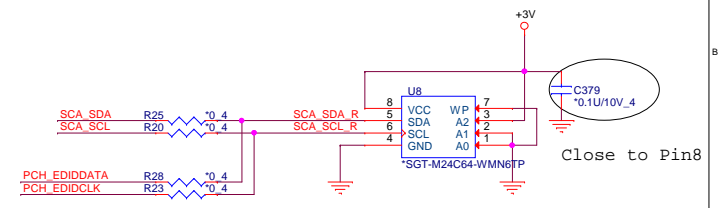


	PROJECT :U83	
	Quanta Computer Inc.	
Size Custom	Document Number	Rev 1A
Sun S3 VRAM(DDR3 BGA96P)		
Date: Thursday, March 14, 2013	Sheet 19 of 41	

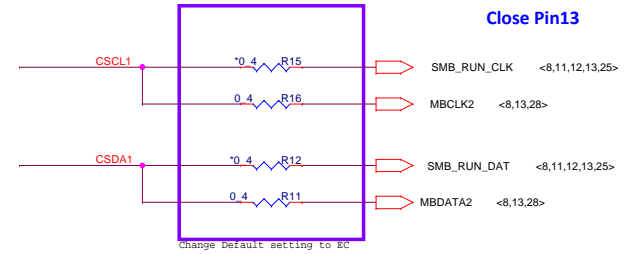


SCA_SCL pull high => EEPROM mode
SCA_SDA pull low => EEPROM Free mode

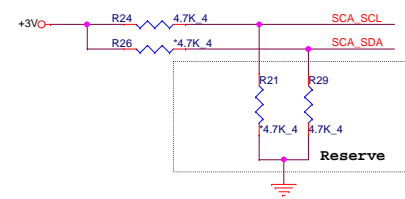
Address=0xA8



RTD2132S => R25, R20
RTD2132R => R28, R23



EE PROM R15,R12
EC OPTION R16,R11

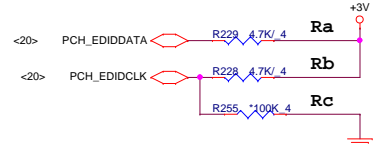
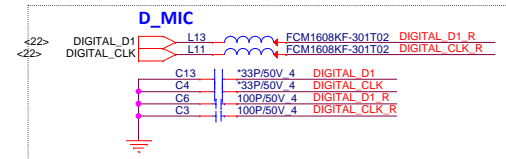
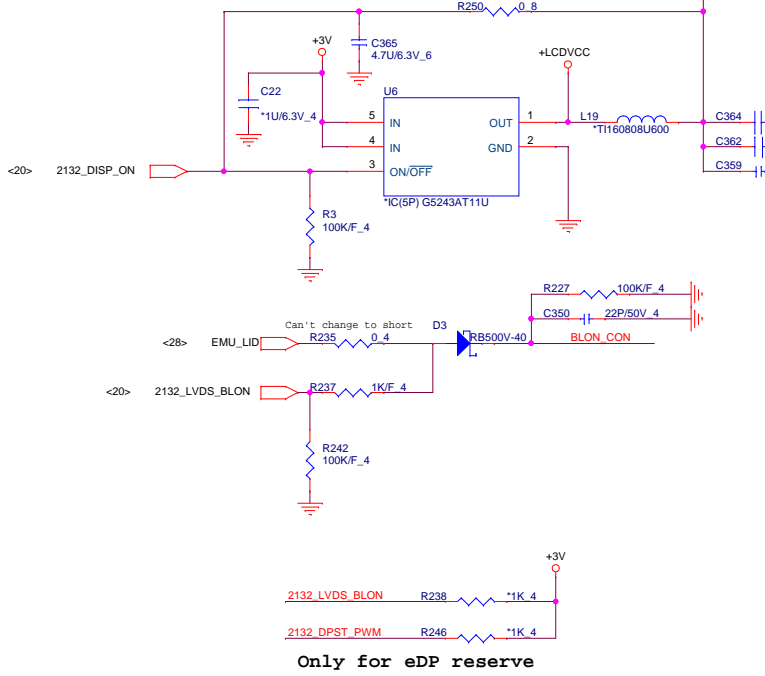


		MODE_CFG0(PIN30)	
		0	1
MODE_CFG1(PIN31)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

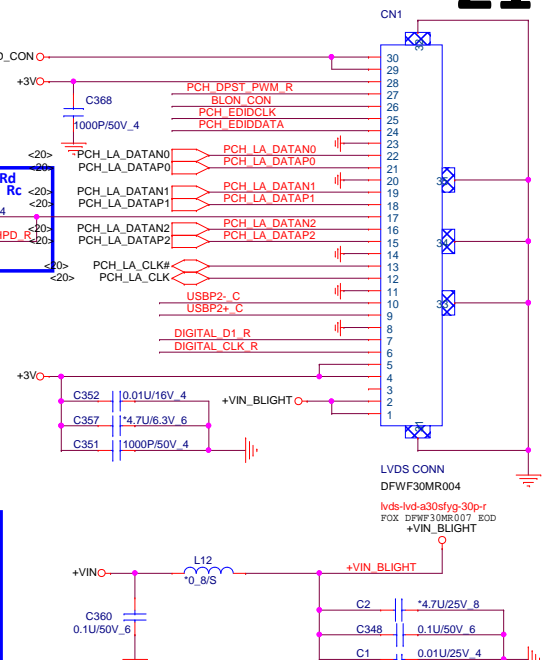
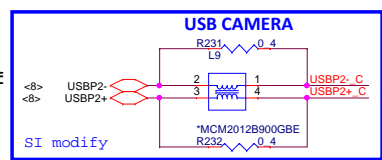
PROJECT :U83
Quanta Computer Inc.

Size Custom	Document Number LVDS converter RTD2132R	Rev 1A
Date: Monday, March 18, 2013	Sheet 20 of 41	

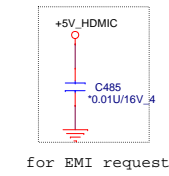
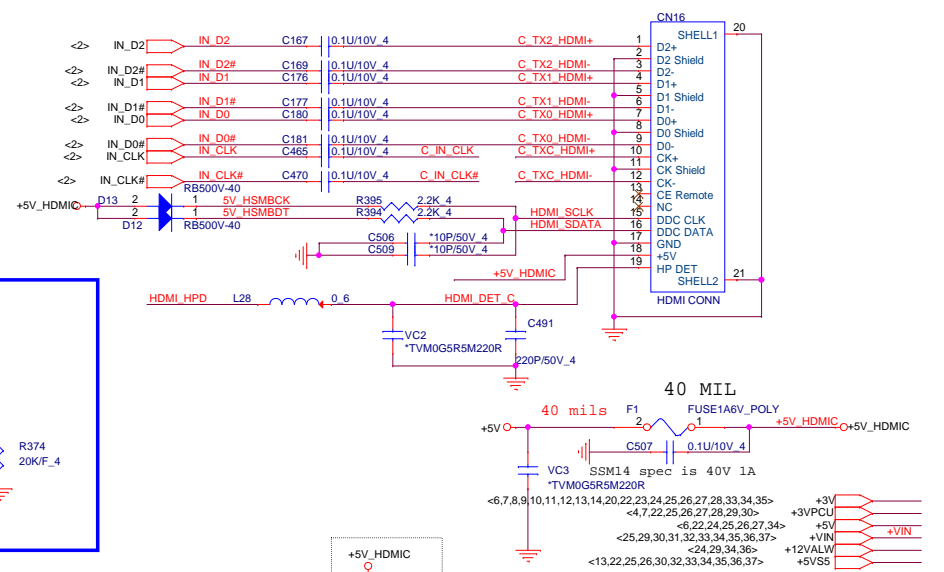
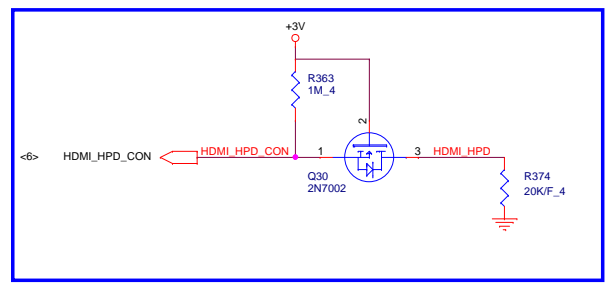
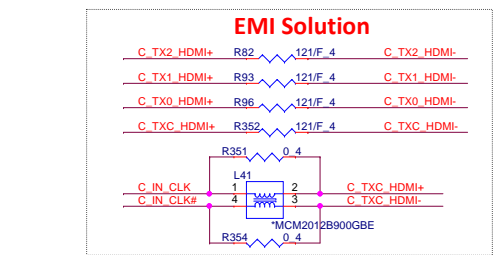
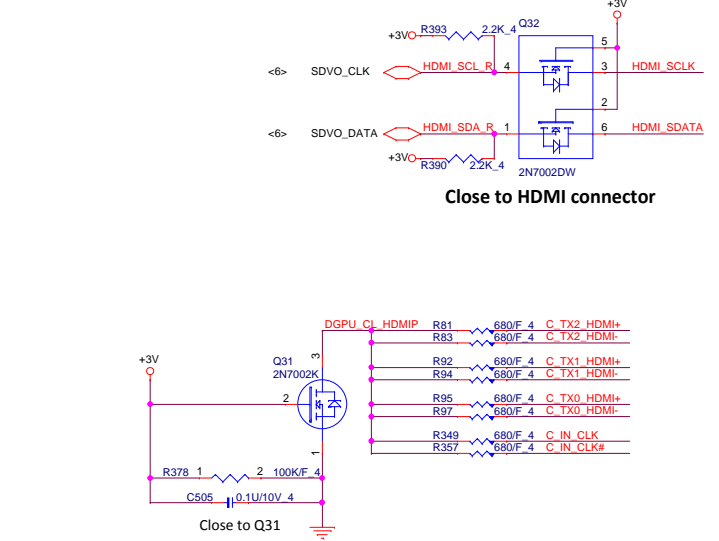
LVDS Conn.



For LVDS stuff Ra=4.7k,Rb=4.7k,Rc un-stuff
 For eDP reserve Ra=100k,Rc=100k,Rb un-stuff

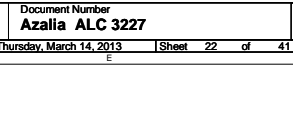
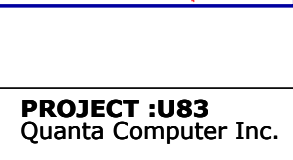
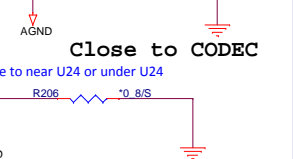
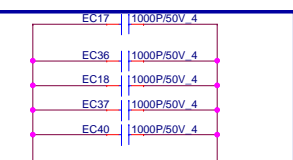
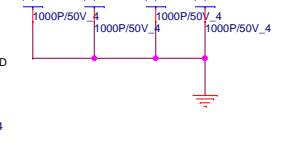
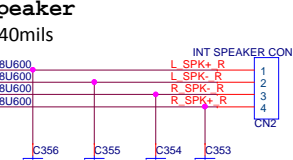
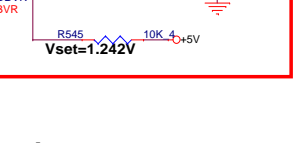
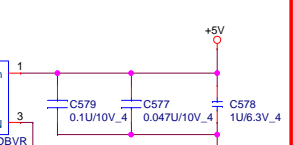
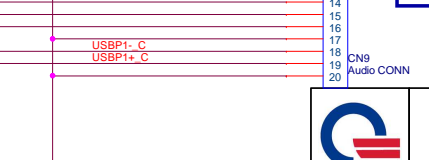
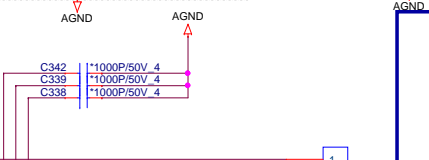
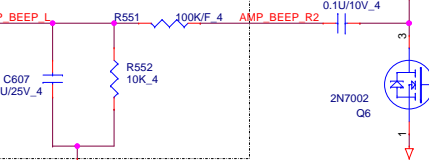
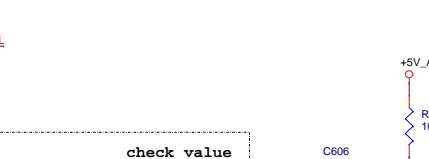
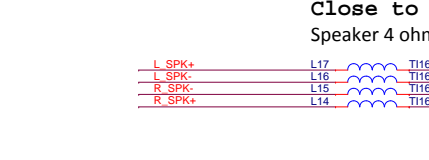
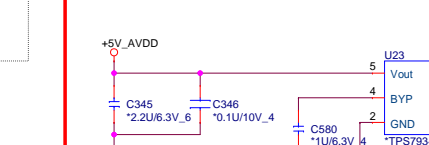
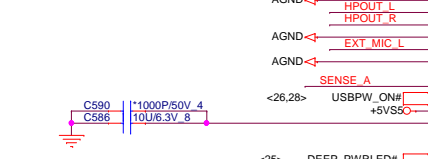
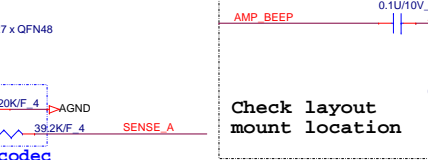
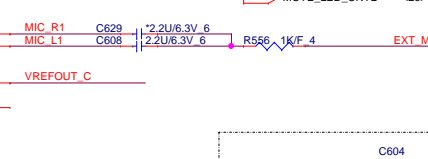
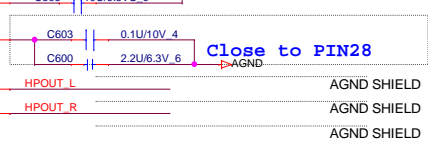
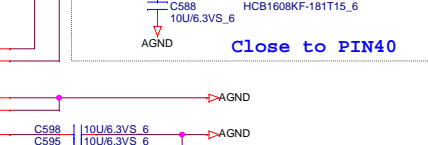
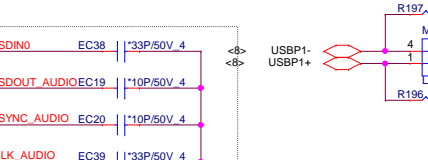
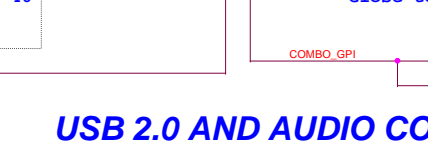
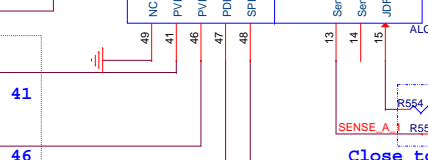
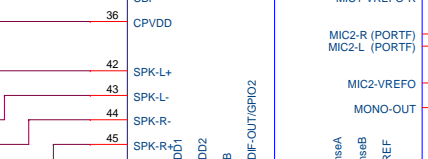
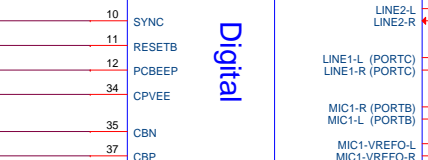
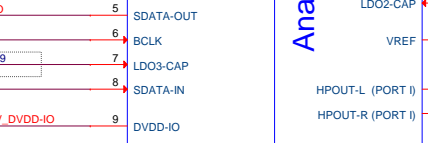
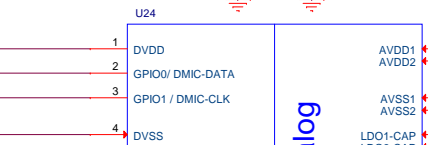
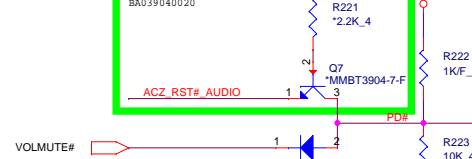
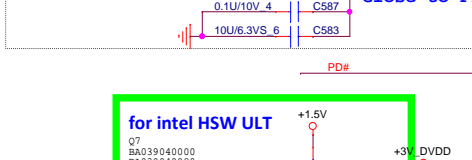
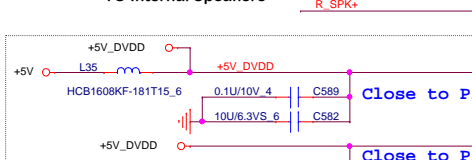
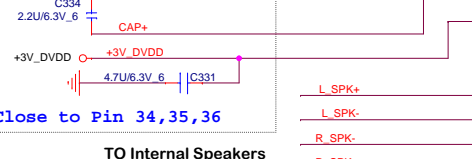
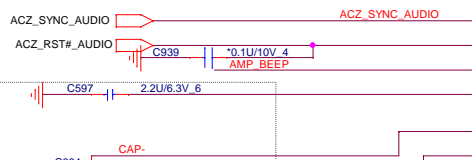
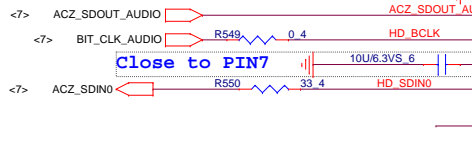
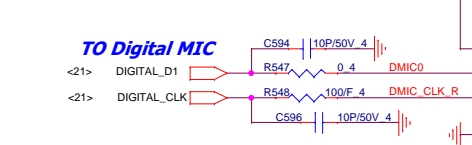
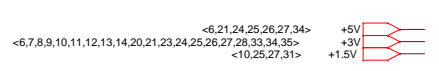
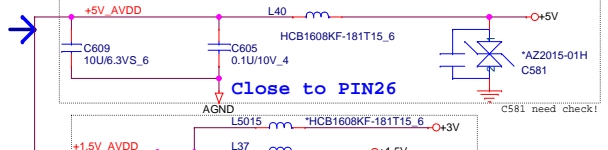
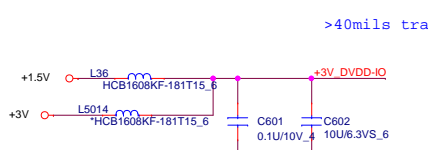
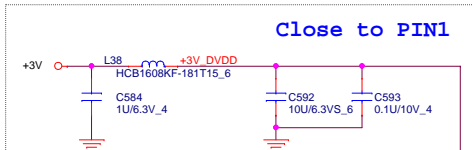


HDMI Conn.

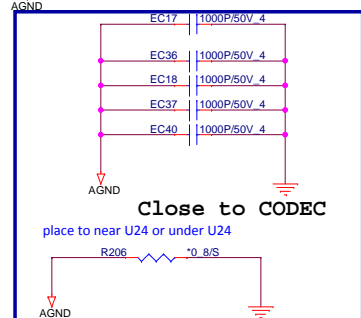
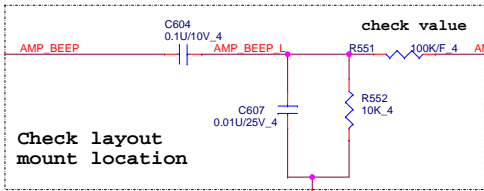


PROJECT :U83
 Quanta Computer Inc.

Size Custom	Document Number LCD/HDMI/Camera/D-MIC	Rev 1A
Date: Thursday, March 14, 2013	Sheet 21 of 41	



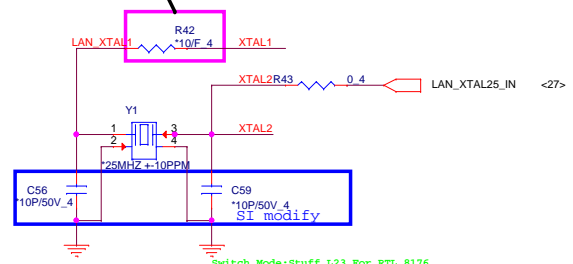
USB 2.0 AND AUDIO COMBO JACK



PROJECT :U83
Quanta Computer Inc.

Size Custom	Document Number Azalia ALC 3227	Rev 1A
Date: Thursday, March 14, 2013		Sheet 22 of 41

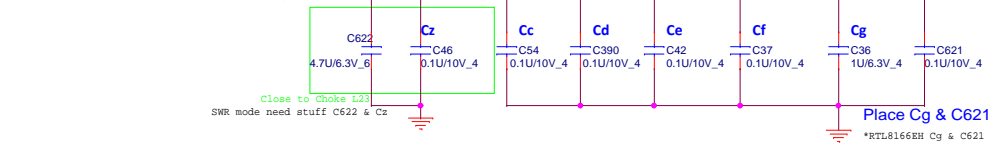
For EMI 0 ~ 22 ohm



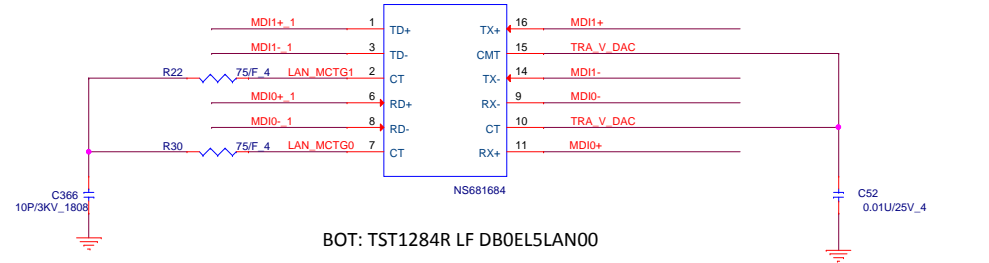
Trace < 30 mil
Width > 60 mil
Power trace Layout 宽度 > 60mil

Switch Mode: Stuff L23 For RTL 8176
LDO Mode: Stuff R259 For RTL8166

Place Cc, Cd, Ce, Cf close to each VDD10 pin-- 3, 8, 22, 30



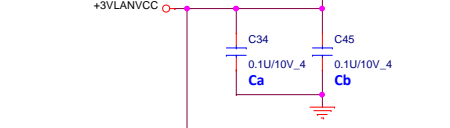
Place Cg & C621 close to each VDD10 pin22
*RTL8166EH Cg & C621 close pin30



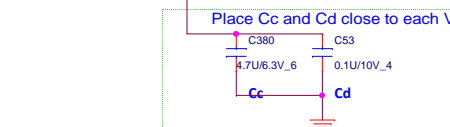
Stuff Ca and Cb only, close to each VDD33 pin-- 11, 32

Place Cc and Cd close to each VDD33 pin-- 23

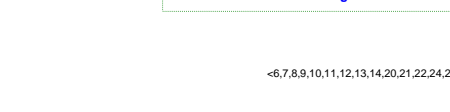
Remove For Not Using SWR mode



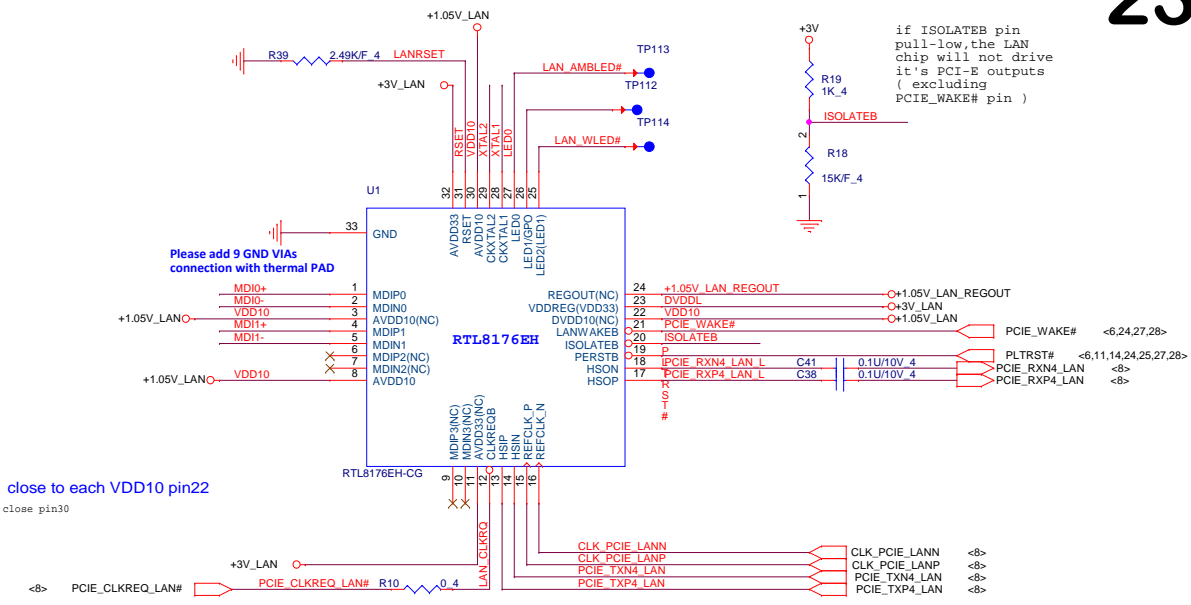
Remove For Not Using SWR mode



Remove For Not Using SWR mode



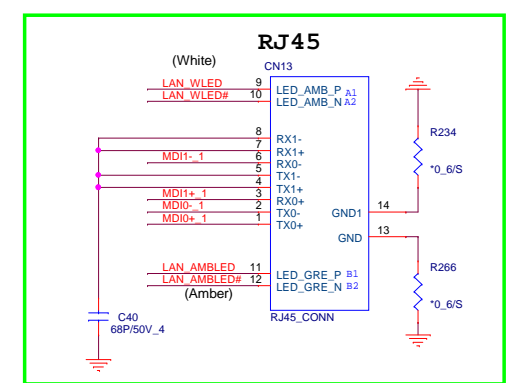
Remove For Not Using SWR mode



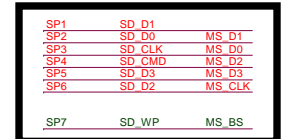
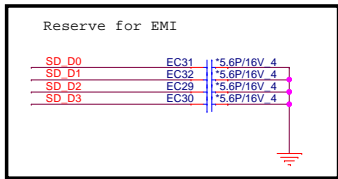
Please add 9 GND VIAS connection with thermal PAD

if ISOLATEB pin pull-low, the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

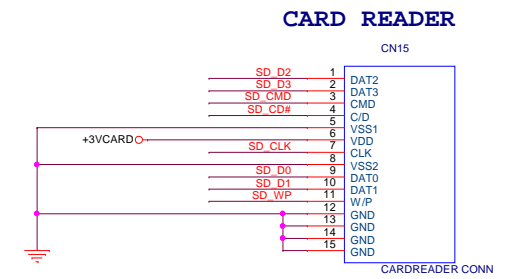
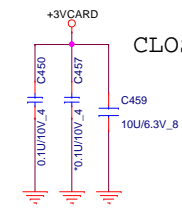
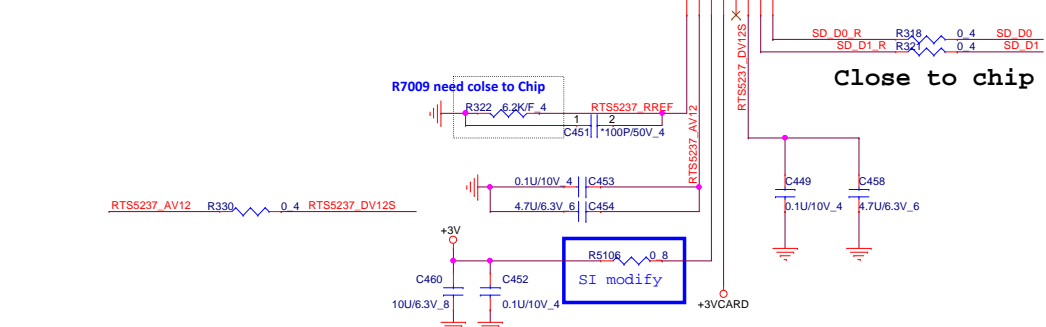
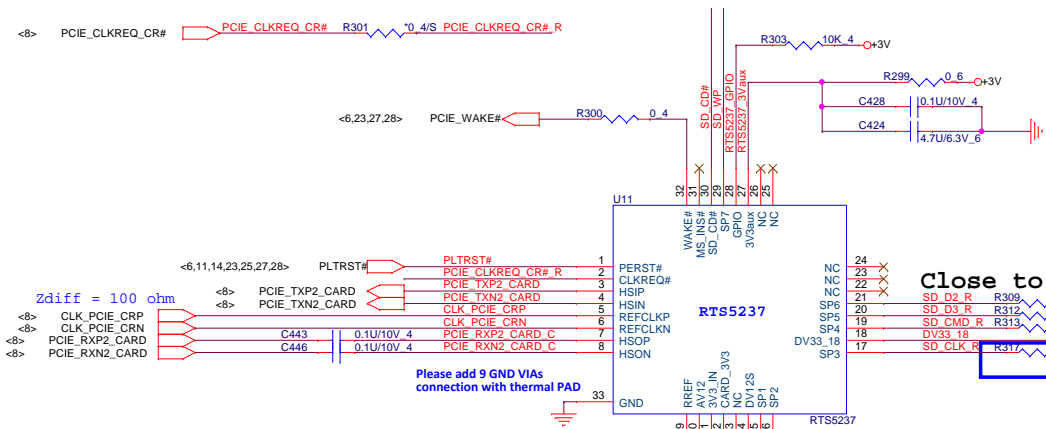
LAN conn TWD Type



	PROJECT :U83	
	Quanta Computer Inc.	
Size Custom	Document Number LAN RTL8176EH/RJ45	Rev 1A
Date: Friday, March 15, 2013	Sheet 23 of 41	



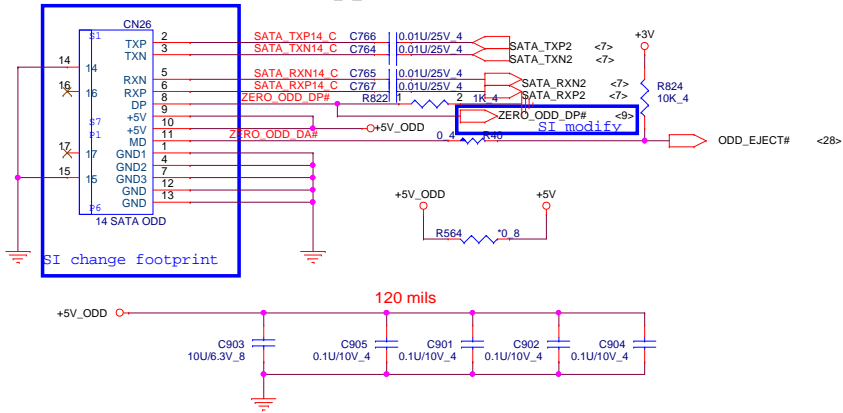
Share Pin
SD / MMC



SATA ODD CONNECTOR

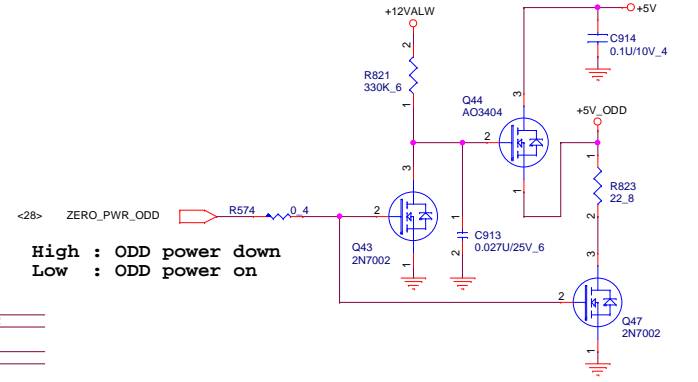
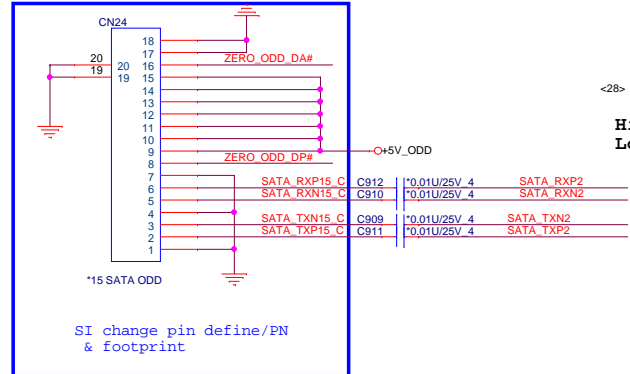
14" SATA ODD

Bypass CAP close conn



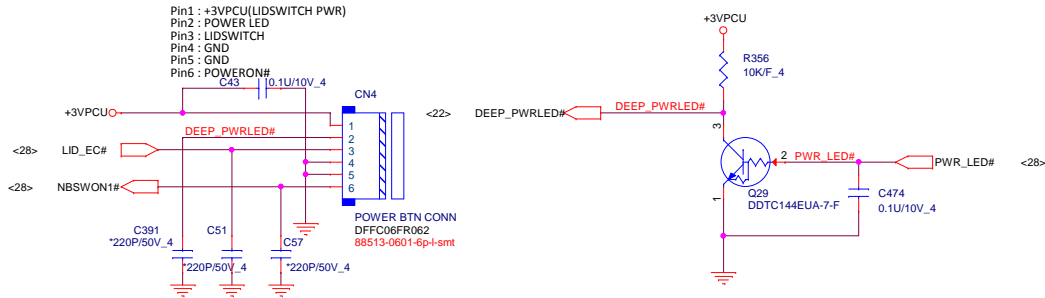
15" SATA ODD

New Type

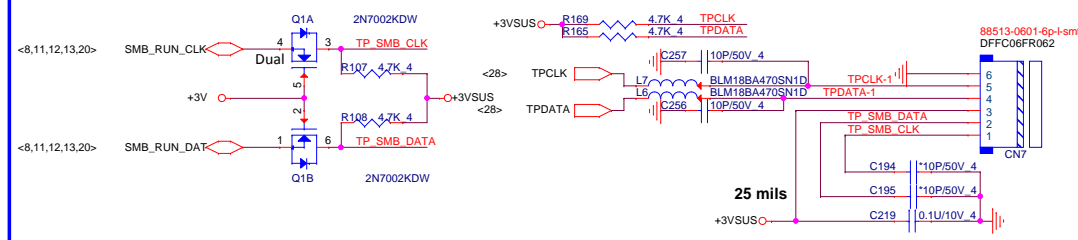


<p>PROJECT :U83 Quanta Computer Inc.</p>		
Size Custom	Document Number CR RTS5237 & CR SOCKET	Rev 1A
Date: Thursday, March 14, 2013	Sheet 24	of 41

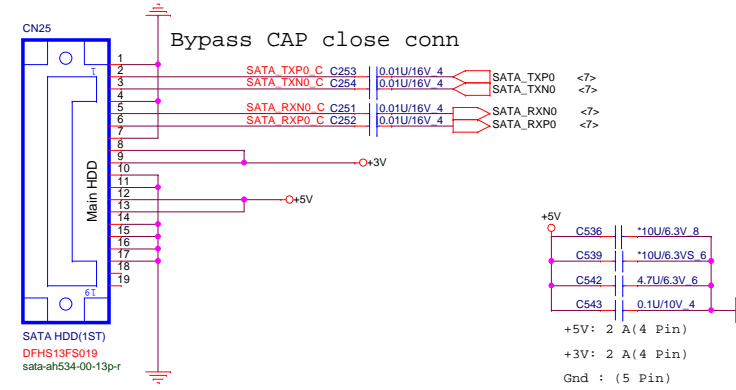
Power Button Connector



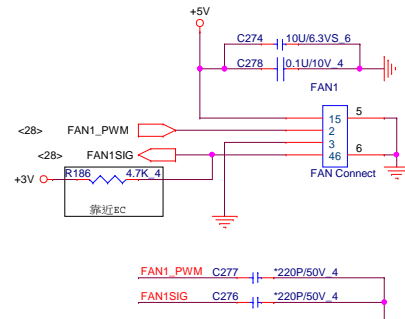
Touch Pad Connector



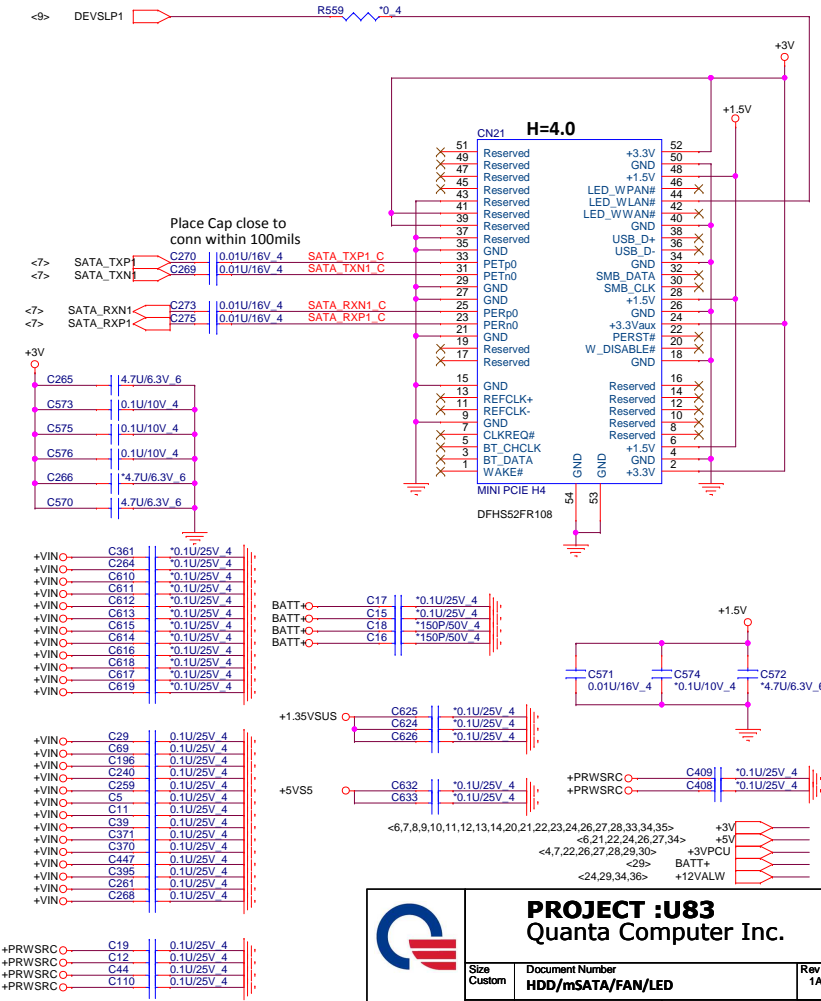
SATA HDD Connector(Cable type)



FAN

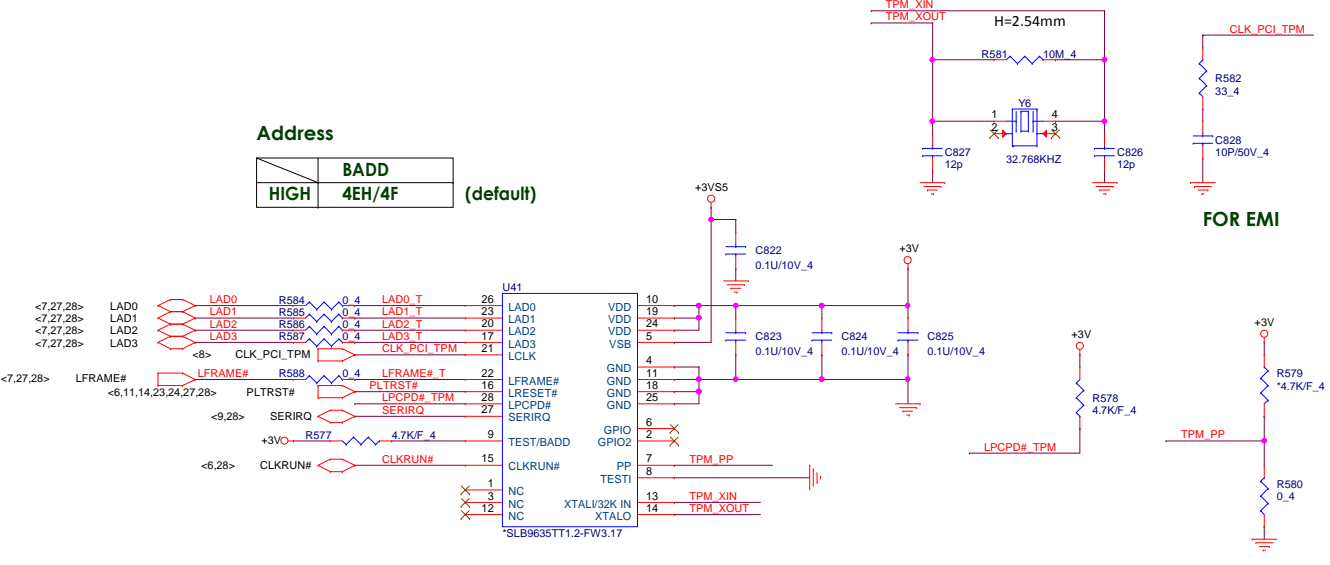


Mini PCI-E Card 2- Full size mSATA



TPM (1.2)

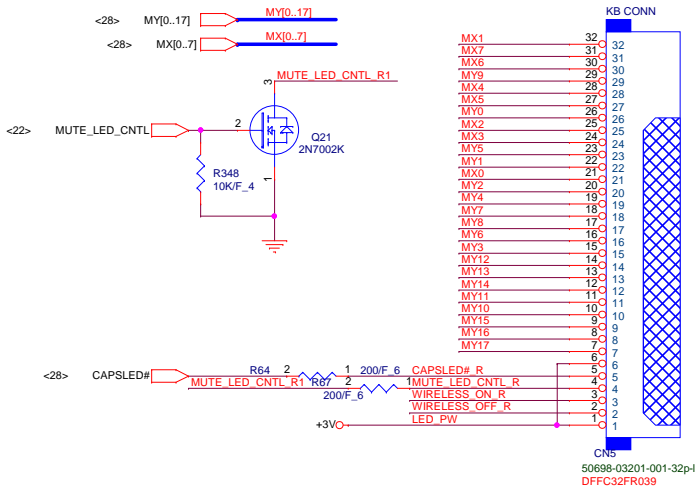
Address	BADD
HIGH	4EH/4F (default)



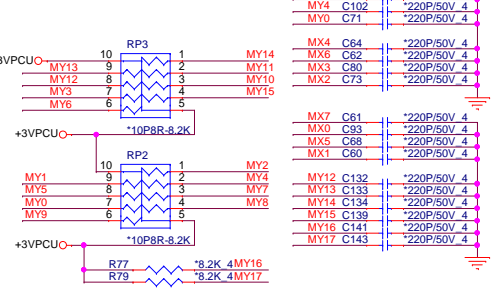
PROJECT :U83
 Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDD/mSATA/FAN/LED	1A
Date: Thursday, March 14, 2013	Sheet	25 of 41

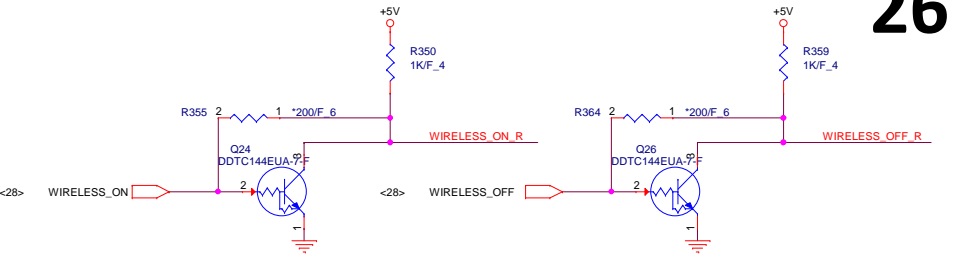
KEYBOARD Con.



KEYBOARD PULL-UP

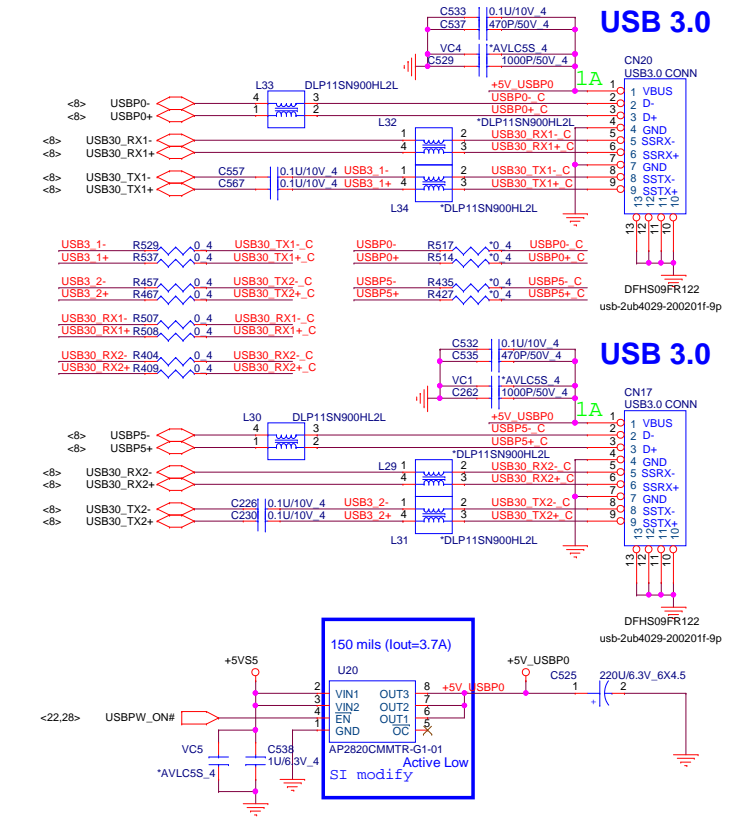
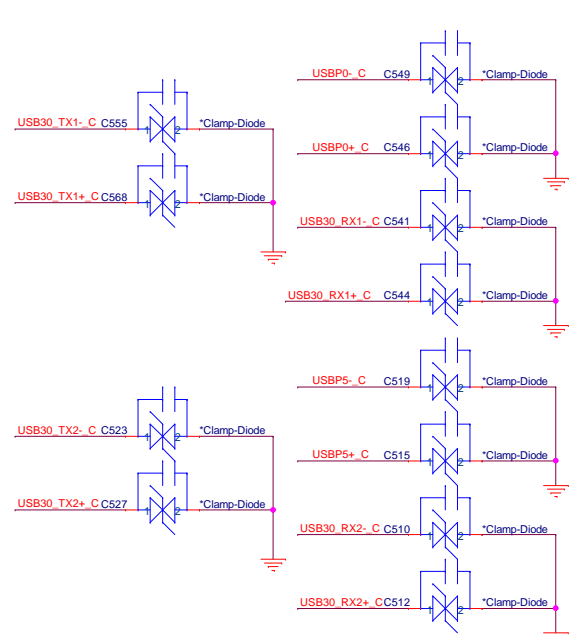


MY5	C83	*220P/50V_4
MY6	C124	*220P/50V_4
MY3	C128	*220P/50V_4
MY7	C106	*220P/50V_4
MY8	C114	*220P/50V_4
MY9	C63	*220P/50V_4
MY10	C137	*220P/50V_4
MY11	C136	*220P/50V_4
MY1	C89	*220P/50V_4
MY2	C103	*220P/50V_4
MY4	C102	*220P/50V_4
MY0	C71	*220P/50V_4
MX4	C64	*220P/50V_4
MX6	C62	*220P/50V_4
MX3	C80	*220P/50V_4
MX2	C73	*220P/50V_4
MX7	C61	*220P/50V_4
MX0	C93	*220P/50V_4
MX5	C68	*220P/50V_4
MX1	C60	*220P/50V_4
MY12	C132	*220P/50V_4
MY13	C133	*220P/50V_4
MY14	C134	*220P/50V_4
MY15	C139	*220P/50V_4
MY16	C141	*220P/50V_4
MY17	C143	*220P/50V_4

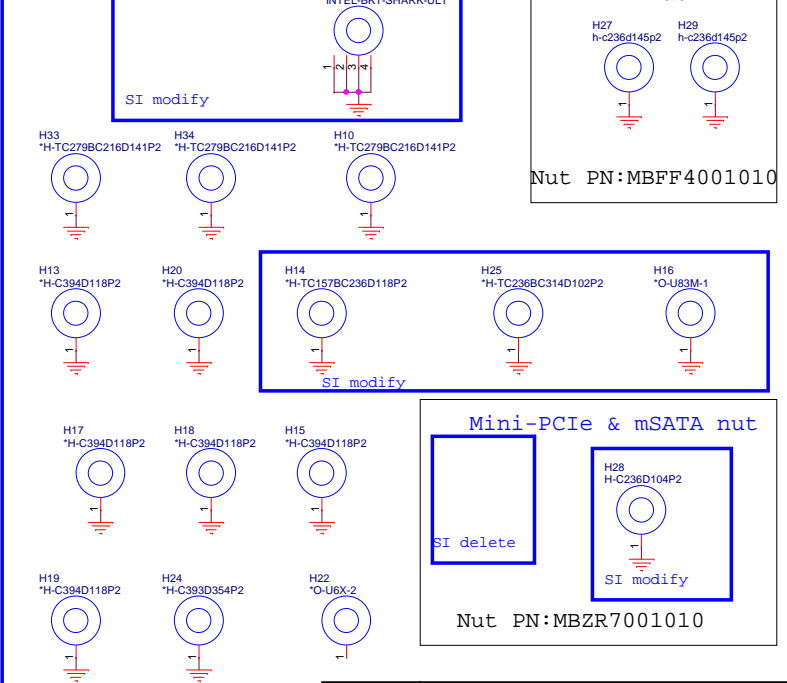


R6X Type

USB 2.0/3.0 Combo

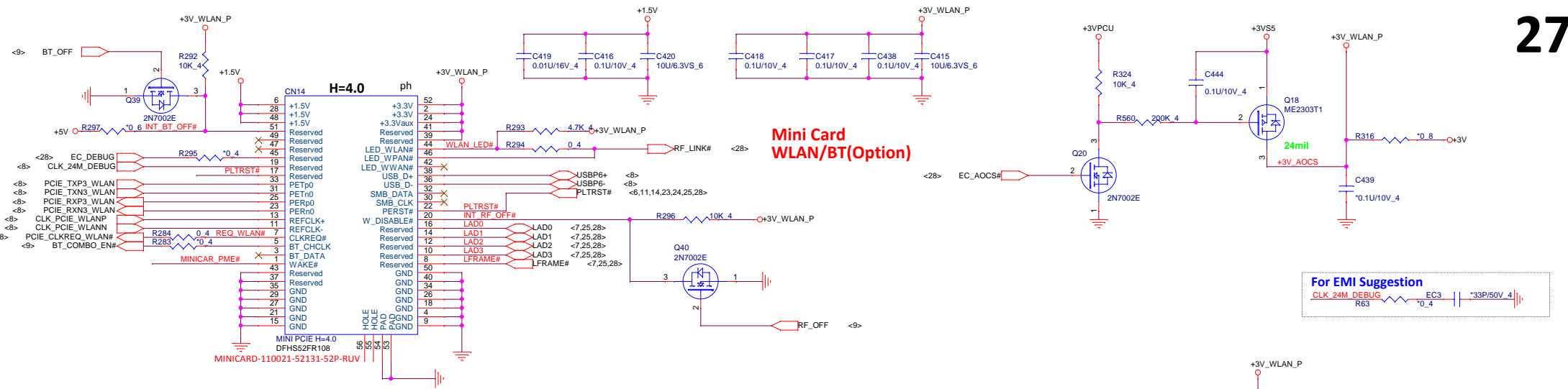


Hole

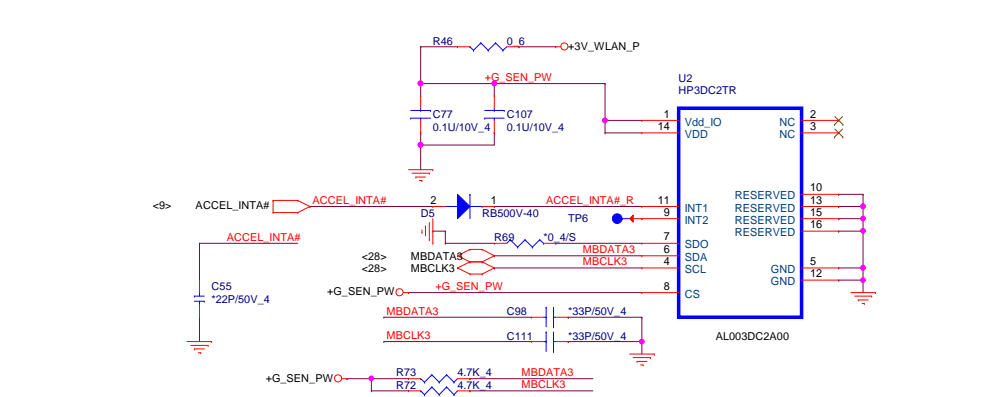


PROJECT :U83
Quanta Computer Inc.

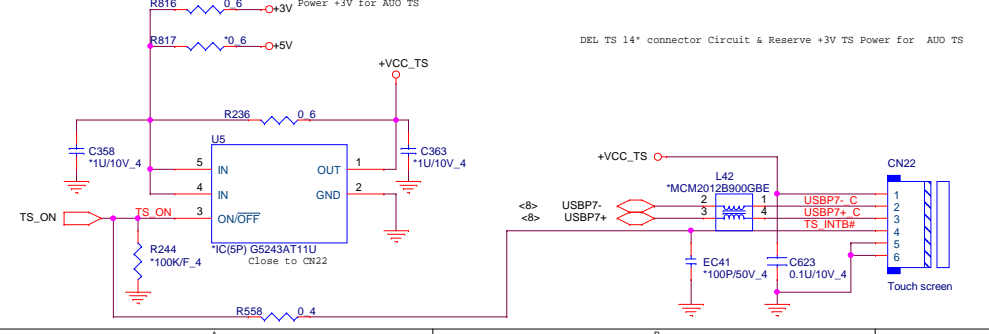
Size Custom	Document Number USB3.0/KB	Rev 1A
Date: Friday, March 15, 2013	Sheet 26of	41



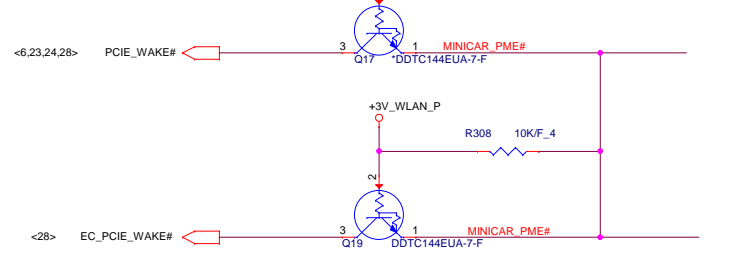
Accelerometer Sensor



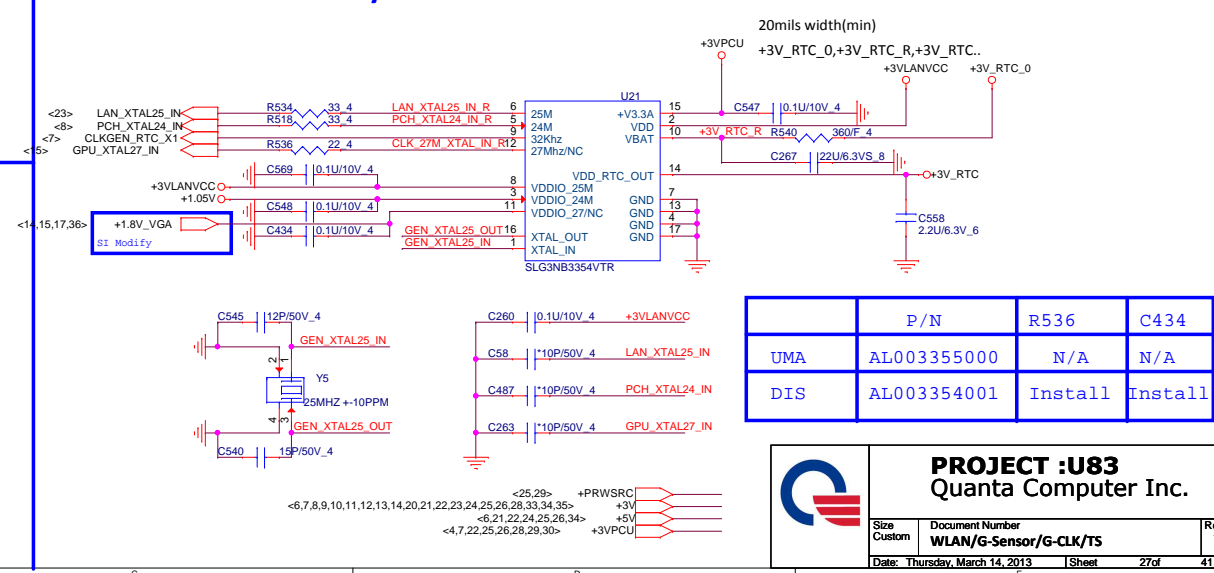
Touch screen



Support Wake Function(Reserve)

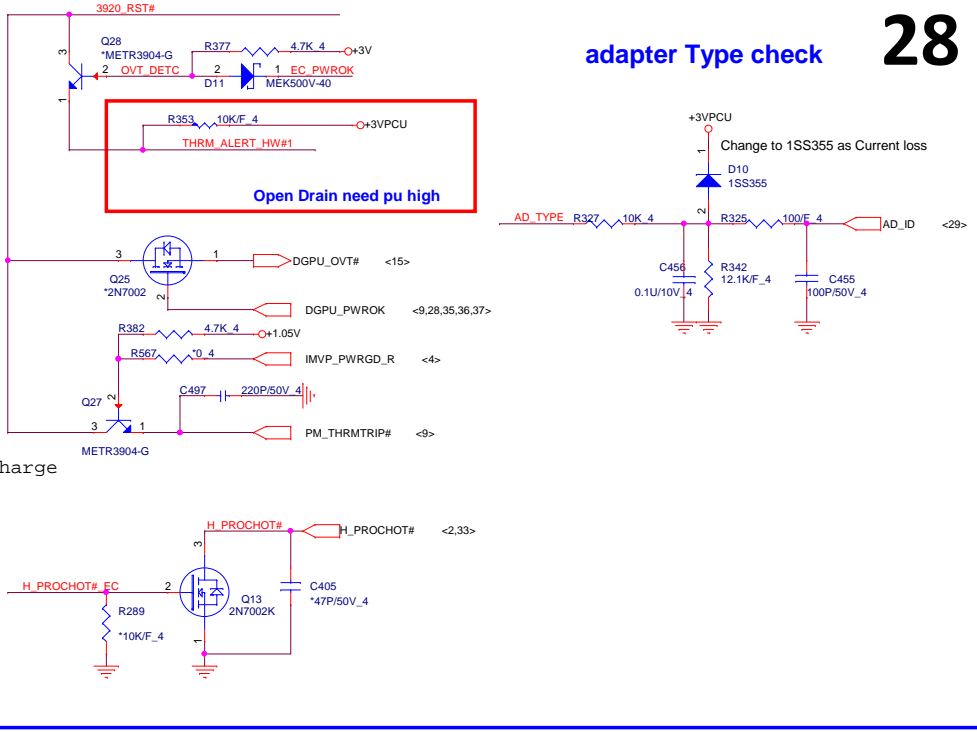
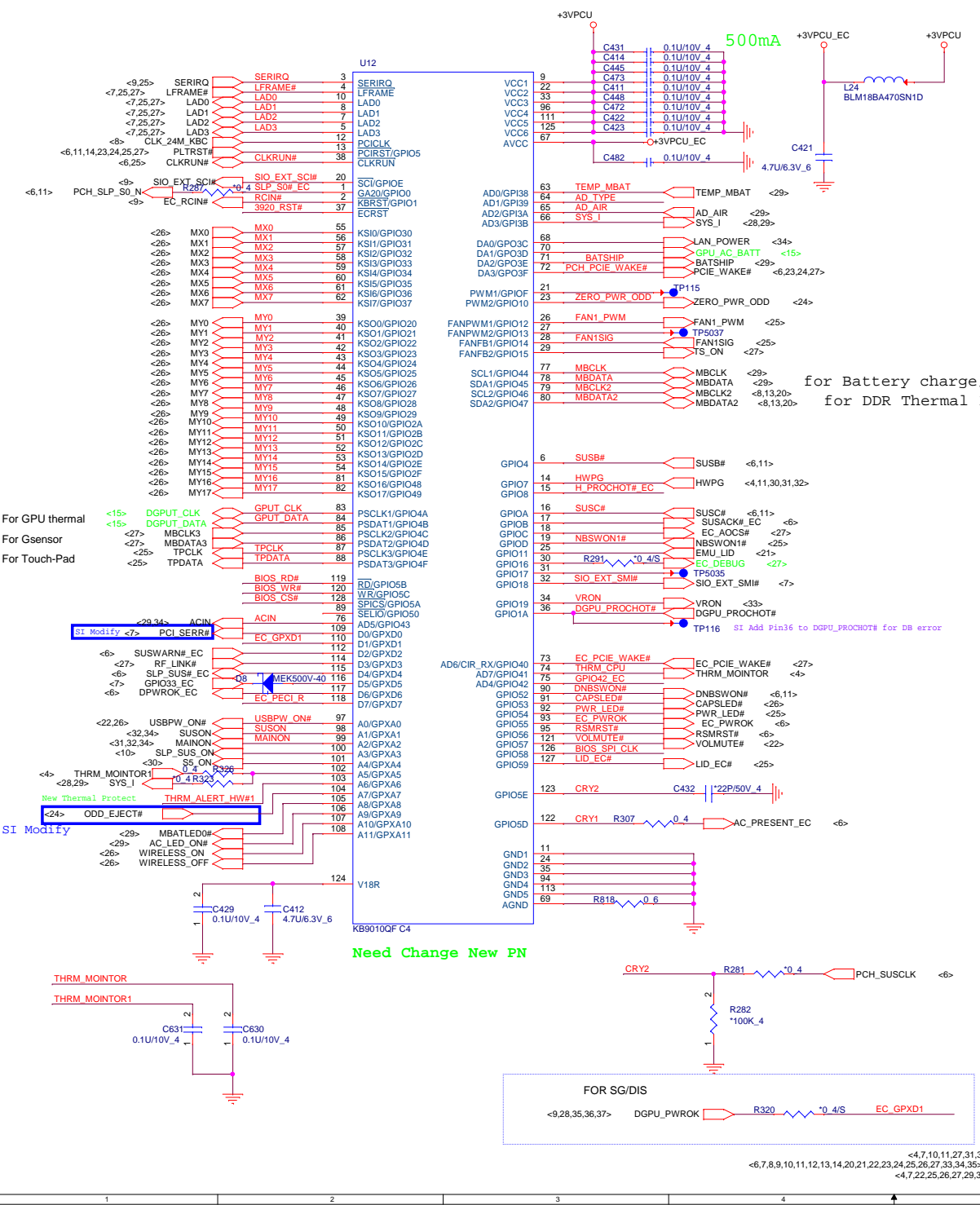


Green CLK Circuitry



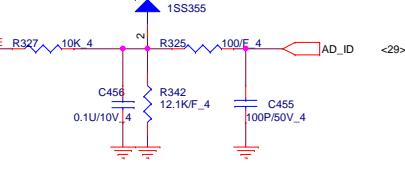
PROJECT :U83
 Quanta Computer Inc.

Size Custom	Document Number WLAN/G-Sensor/G-CLK/TS	Rev 1A
Date: Thursday, March 14, 2013	Sheet 27 of 41	

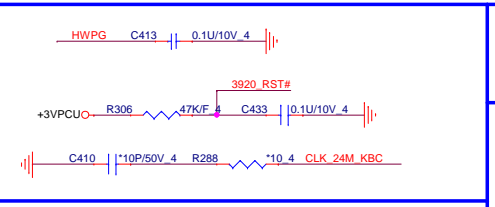
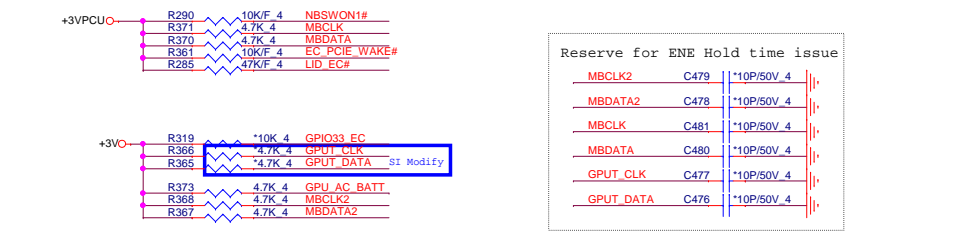


adapter Type check

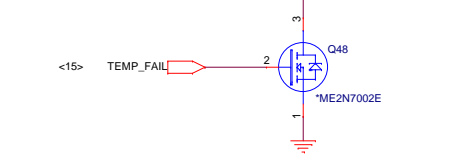
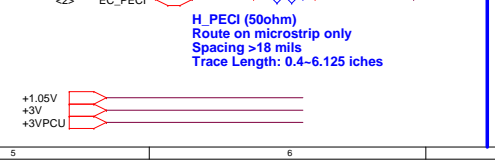
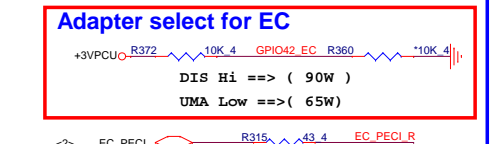
Change to 1SS355 as Current loss



for Battery charge/charge for DDR Thermal IC



DGPU Thermal protect

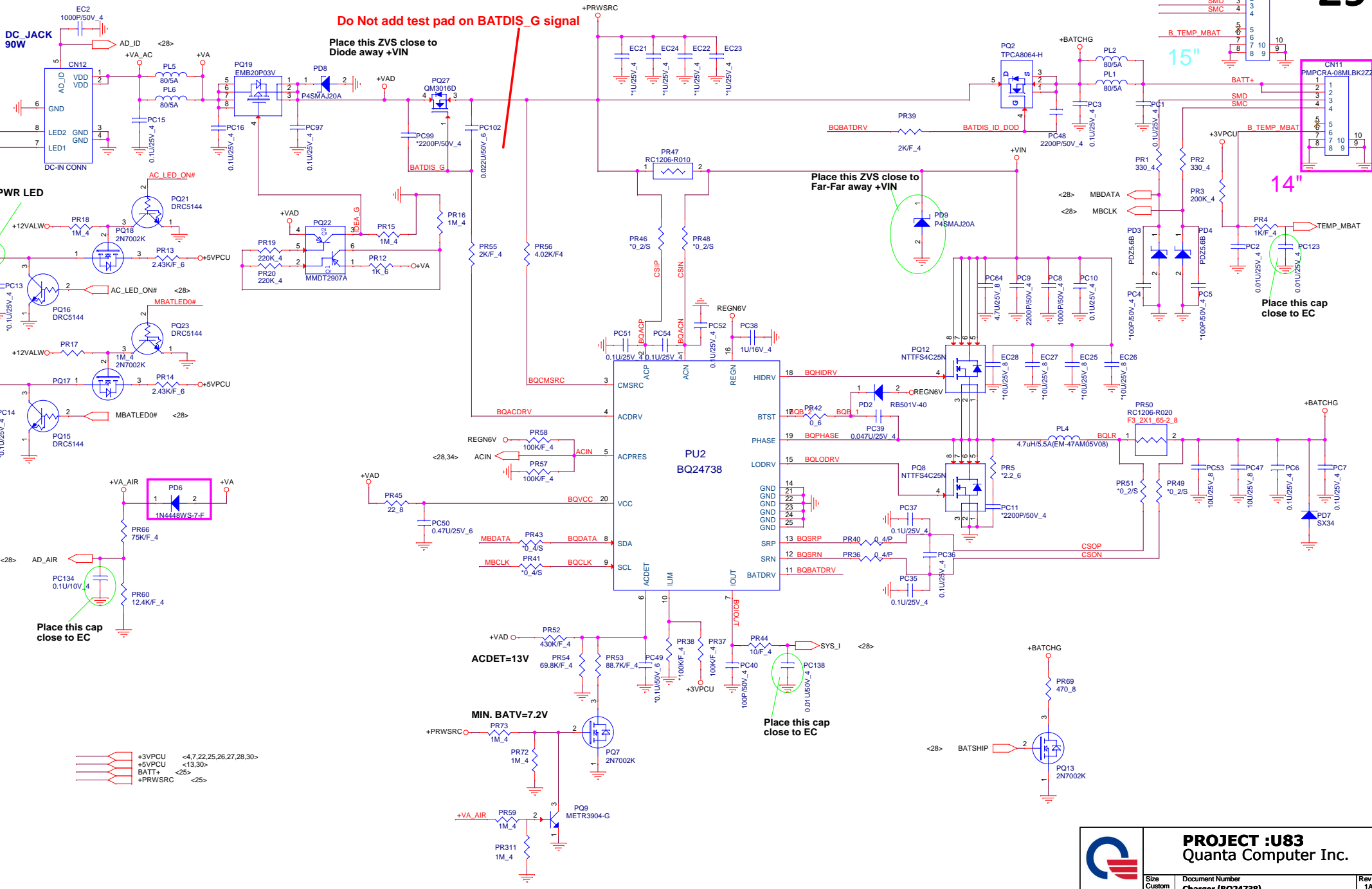


Need Change New PN



PROJECT :U83
Quanta Computer Inc.

Size Custom	Document Number EC (KB9010QF C4)	Rev 1A
Date: Thursday, March 14, 2013	Sheet 28 of 41	



Do Not add test pad on BATDIS_G signal

Place this ZVS close to Diode away +VIN


Place this ZVS close to Far-Far away +VIN

Place this cap close to EC

Place this cap close to EC

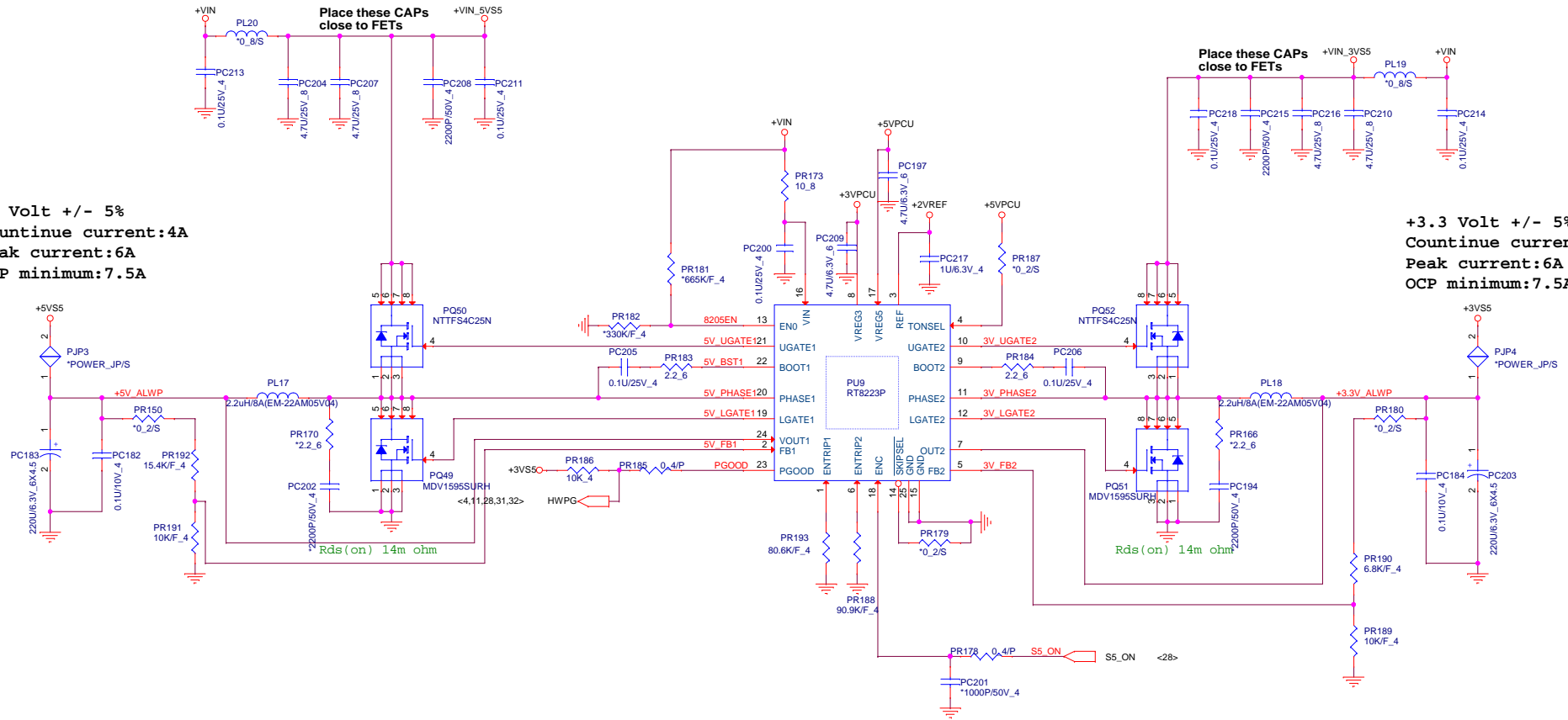
Place this cap close to EC

- +3VPCU <4,7,22,25,26,27,28,30>
- +5VPCU <13,30>
- BATT+ <25>
- +PRWSRC <25>

 <p>PROJECT :U83 Quanta Computer Inc.</p>			
			<p>Size Custom</p>
<p>Date: Thursday, March 14, 2013</p>			<p>Sheet 29 of 41</p>


+5 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

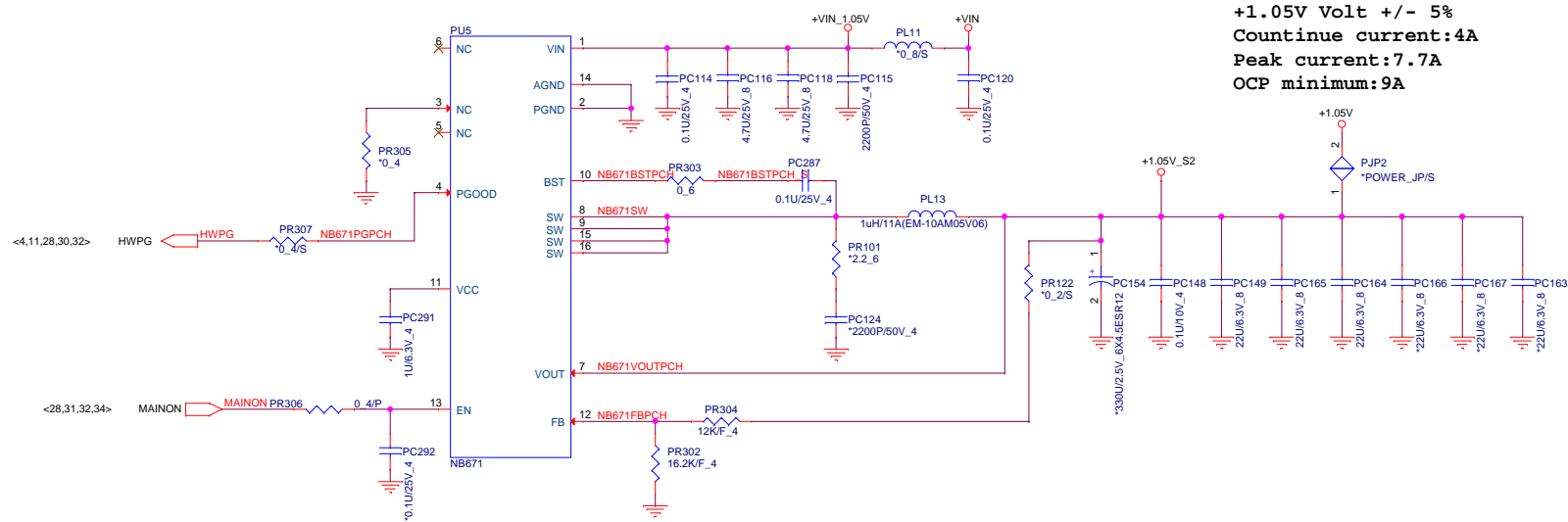
+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A



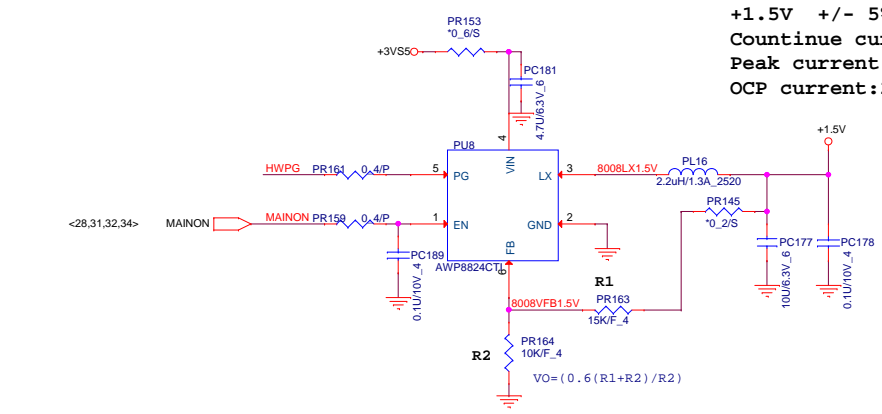
Place these CAPS close to FETs

Place these CAPS close to FETs

	PROJECT :U83 Quanta Computer Inc.		
	Size Custom	Document Number 3/5VPCU(RT8223P)	Rev 1A
	Date: Thursday, March 14, 2013	Sheet 30	of 41



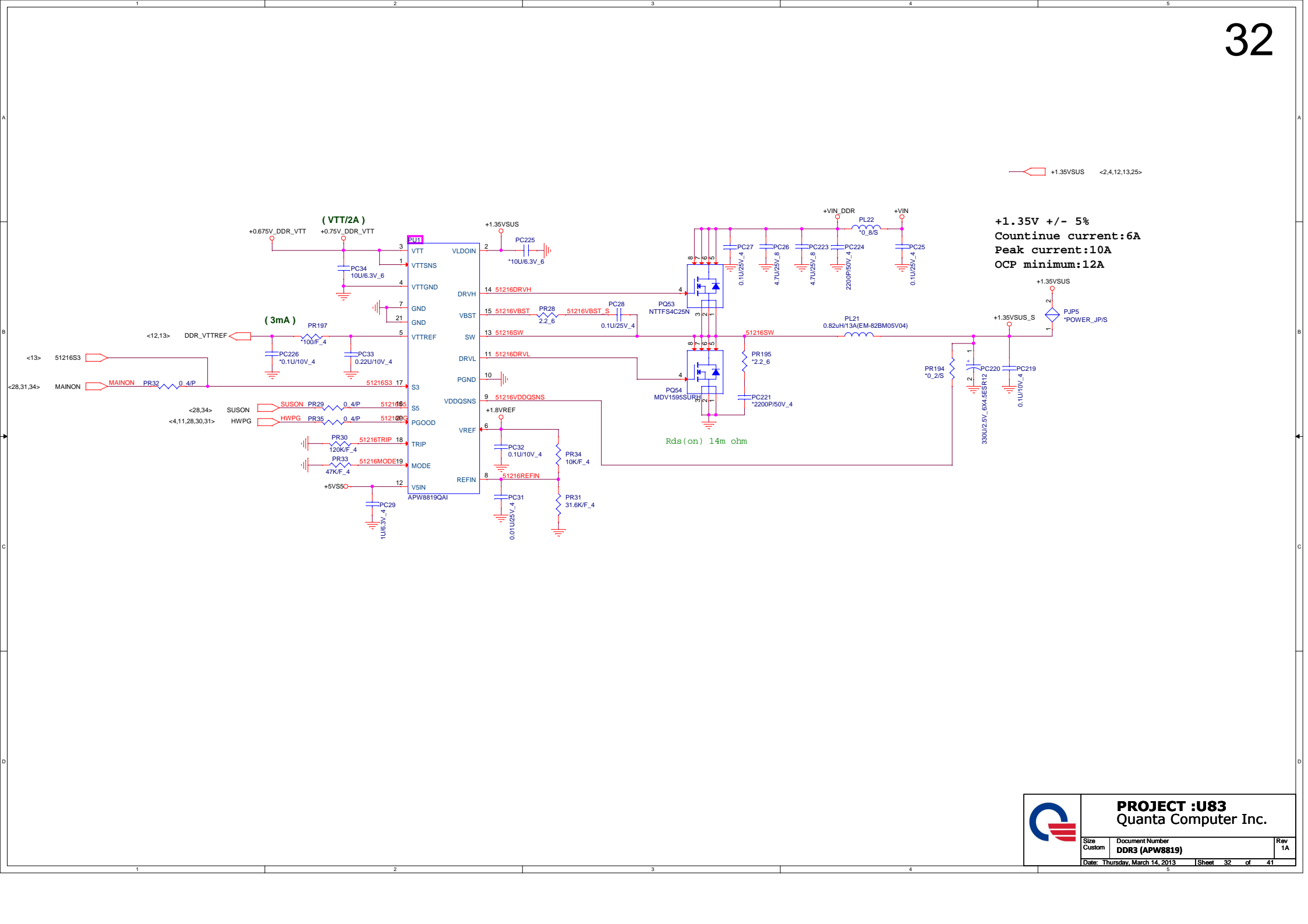
+1.05V Volt +/- 5%
Countinue current:4A
Peak current:7.7A
OCP minimum:9A



+1.5V +/- 5%
Countinue current:1.3A
Peak current:1.5A
OCP current:2A

- +VIN <21,25,29,30,32,33,34,35,36,37>
- +3VSS <6,9,10,11,25,27,30,34,35,36>
- +5VSS <13,22,25,26,30,32,33,34,35,36,37>
- +5VPCU <13,29,30>

	PROJECT :U83	
	Quanta Computer Inc.	
Size Custom	Document Number	Rev
	+1.05V (NB671)1.5V	1A
Date: Thursday, March 14, 2013 Sheet 31 of 41		

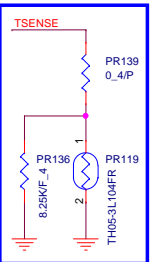


+1.35VSUS <2.4,12,13,25>

+1.35V +/- 5%
 Countinue current: 6A
 Peak current: 10A
 OCP minimum: 1.2A

Rds(on) 14m ohm

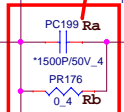
Place close to inductor



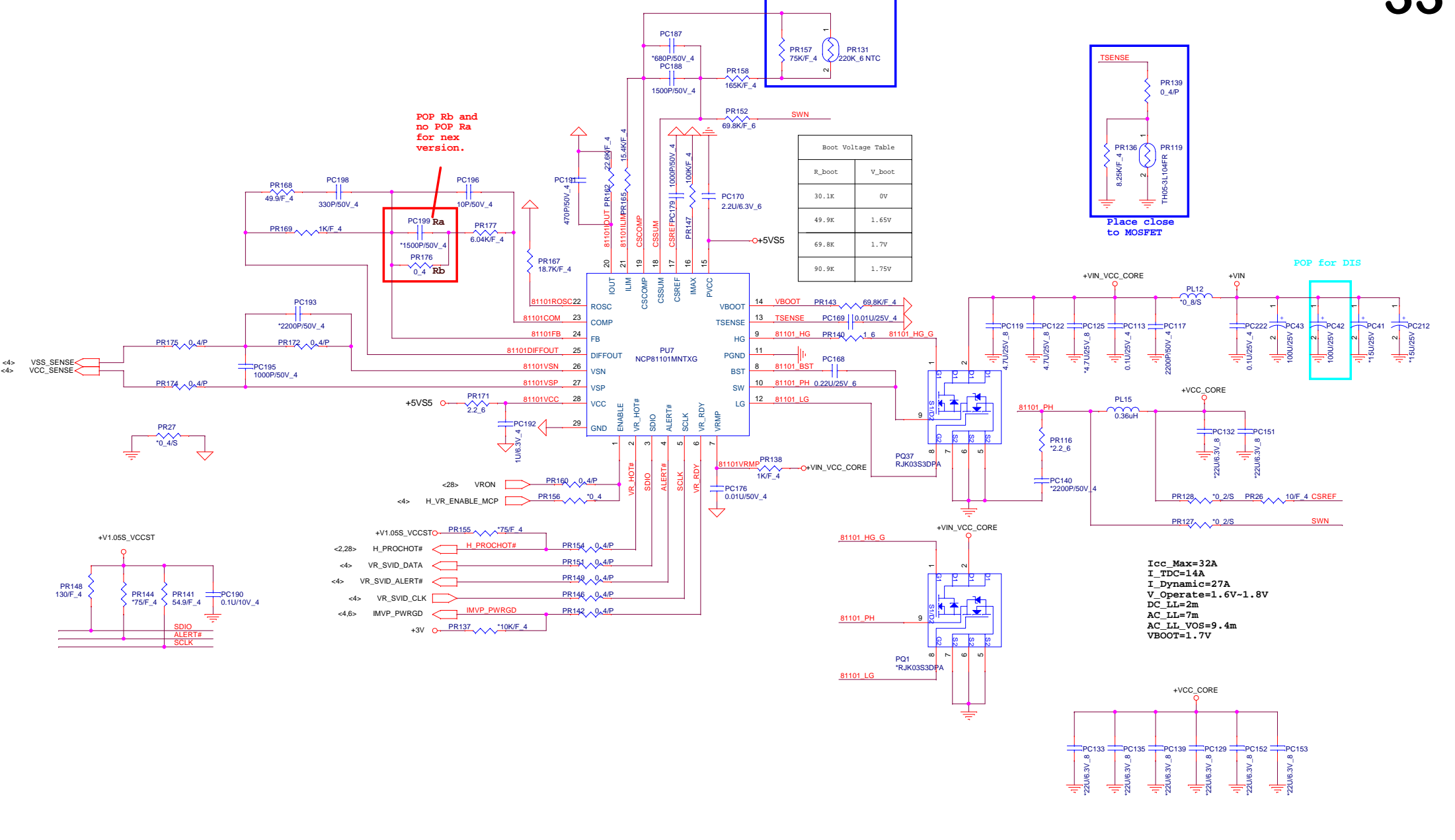
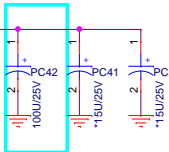
Place close to MOSFET

R_boot	V_boot
30.1K	0V
49.9K	1.65V
69.8K	1.7V
90.9K	1.75V

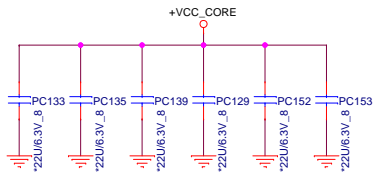
POP Rb and no POP Ra for nex version.



POP for DIS



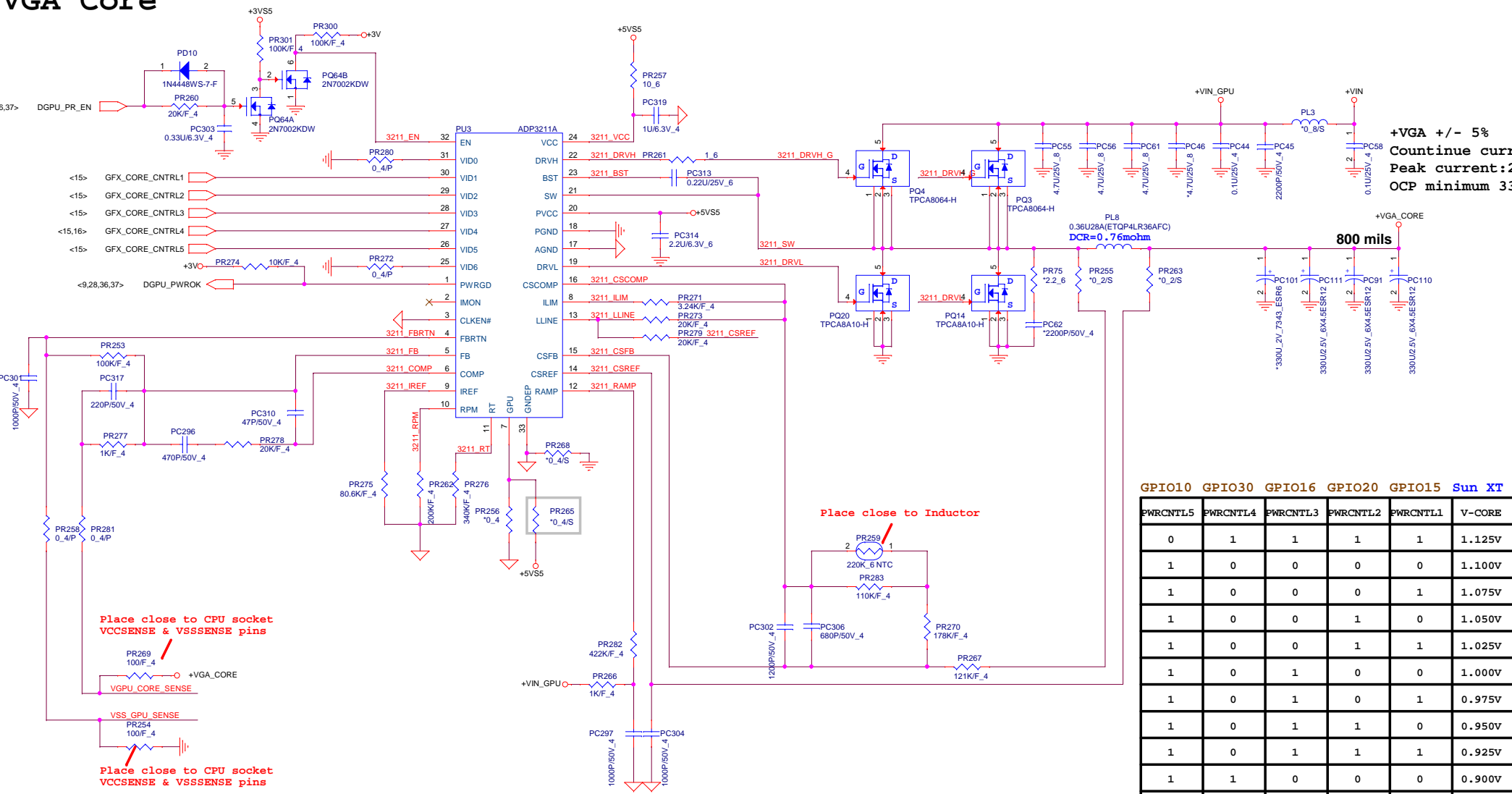
I_{cc_Max}=32A
I_{TDC}=14A
I_{Dynamic}=27A
V_{Operate}=1.6V-1.8V
DC_{LL}=2m
AC_{LL}=7m
AC_{LL_VOS}=9.4m
VBOOT=1.7V



PROJECT :U83
Quanta Computer Inc.

Size Custom	Document Number CPU Core (NCP81101)ULT	Rev 1A
Date: Thursday, March 14, 2013	Sheet 33	of 41

VGA Core



+VGA +/- 5%
Countinue current:21A
Peak current:27A
OCP minimum 33A

PL8
 0.36U28A(ETQP4LR36AFC)
DCR=0.76mohm

800 mils

GPIO10 GPIO30 GPIO16 GPIO20 GPIO15 Sun XT

PWRCNTL5	PWRCNTL4	PWRCNTL3	PWRCNTL2	PWRCNTL1	V-CORE
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	1	1	1	0.825V
1	1	1	0	0	0.800V
1	1	1	0	1	0.775V

Default

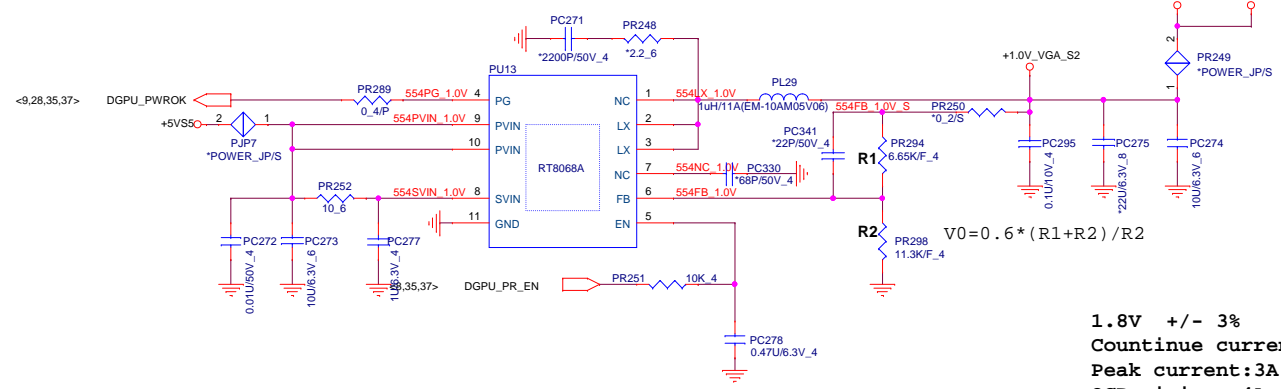


PROJECT :U83
Quanta Computer Inc.

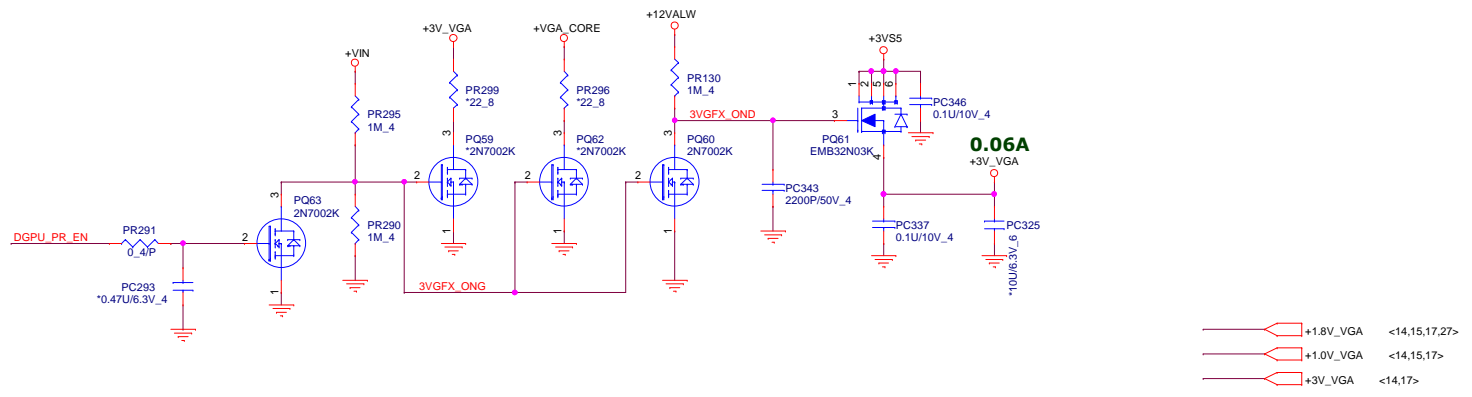
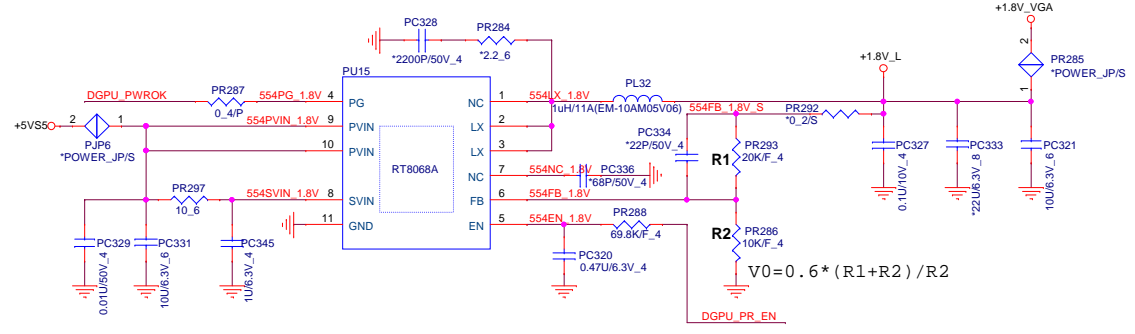
Size Custom	Document Number +VGCORE (ADP3211)	Rev 1A
Date: Thursday, March 14, 2013	Sheet 35 of 41	

VGA TYPE	R2 Value	P/N	1.0V_VGA
Thems	10K	CS31002FB26	1.0V
MARS	11.3K	CS31132FB07	0.95V

+0.95V +/- 3%
Countinue current:2A
Peak current:3A
OCP minimum:4A

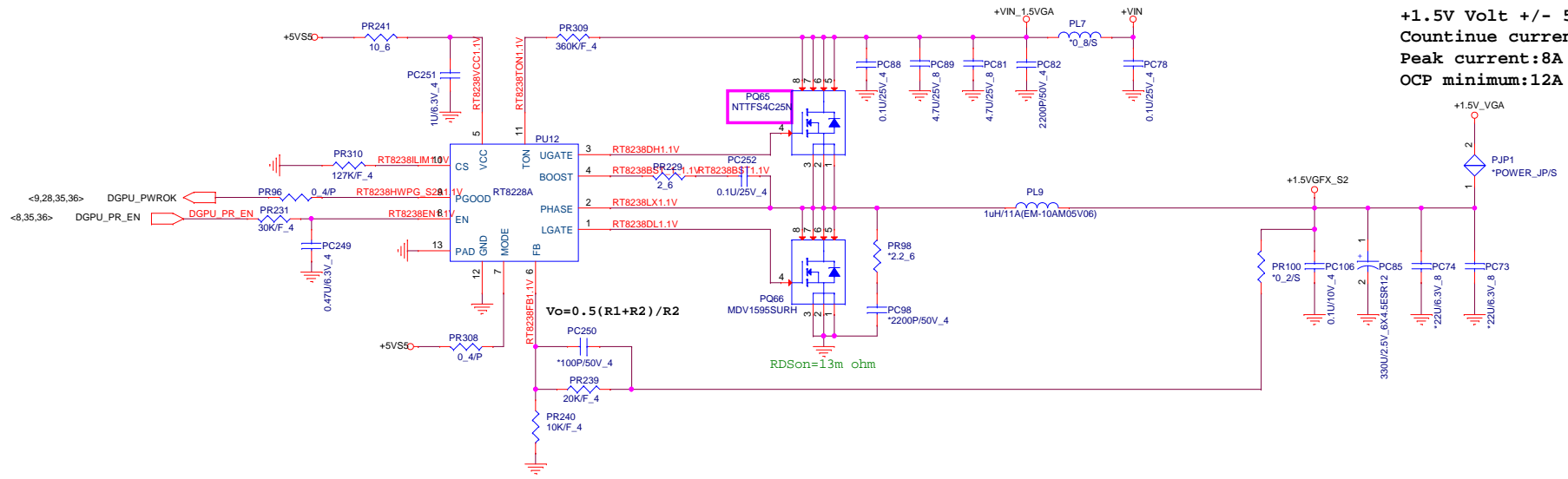


1.8V +/- 3%
Countinue current:2A
Peak current:3A
OCP minimum:4A



- +1.8V_VGA <14,15,17,27>
- +1.0V_VGA <14,15,17>
- +3V_VGA <14,17>

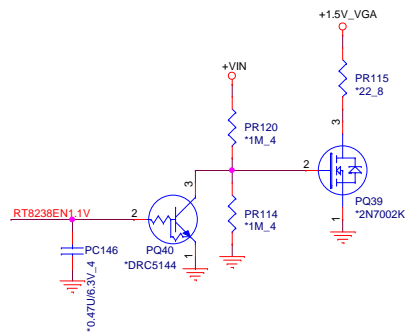
	PROJECT :U83 Quanta Computer Inc.	
	Size Custom	Document Number +1.0V_VGA/1.8V_VGA/3V_VGA
Date Thursday, March 14, 2013	Sheet 36 of 41	Rev 1A



+1.5V Volt +/- 5%
Countinue current:6A
Peak current:8A
OCP minimum:12A

$$V_o = 0.5 (R1 + R2) / R2$$

RDson=1.3m ohm



	PROJECT :U83	
	Quanta Computer Inc.	
	Size Custom	Document Number +1.5V_VGA(RT8228)
Date: Thursday, March 14, 2013 Sheet 37 of 41		

USB3.0	Port Assignment	Power control pin
PORT1	USB2.0/USB3.0 COMBO 1st	USBPW_ON#(from EC)
PORT2	USB2.0/USB3.0 COMBO 2nd	USBPW_ON#(from EC)
PORT3	NC	N/A
PORT4	NC	N/A

USB2.0	Port Assignment	Power control pin
PORT0	USB2.0/USB3.0 COMBO 1st	USBPW_ON#(from EC)
PORT1	USB2.0/USB3.0 COMBO 2nd	USBPW_ON#(from EC)
PORT2	Camera	N/A
PORT3	NC	N/A
PORT4	NC	N/A
PORT5	Left side USB daughter B	USBPW_ON#(from EC)
PORT6	WLAN	N/A
PORT7	Touch Screen 15" used	TS_ON(from EC)

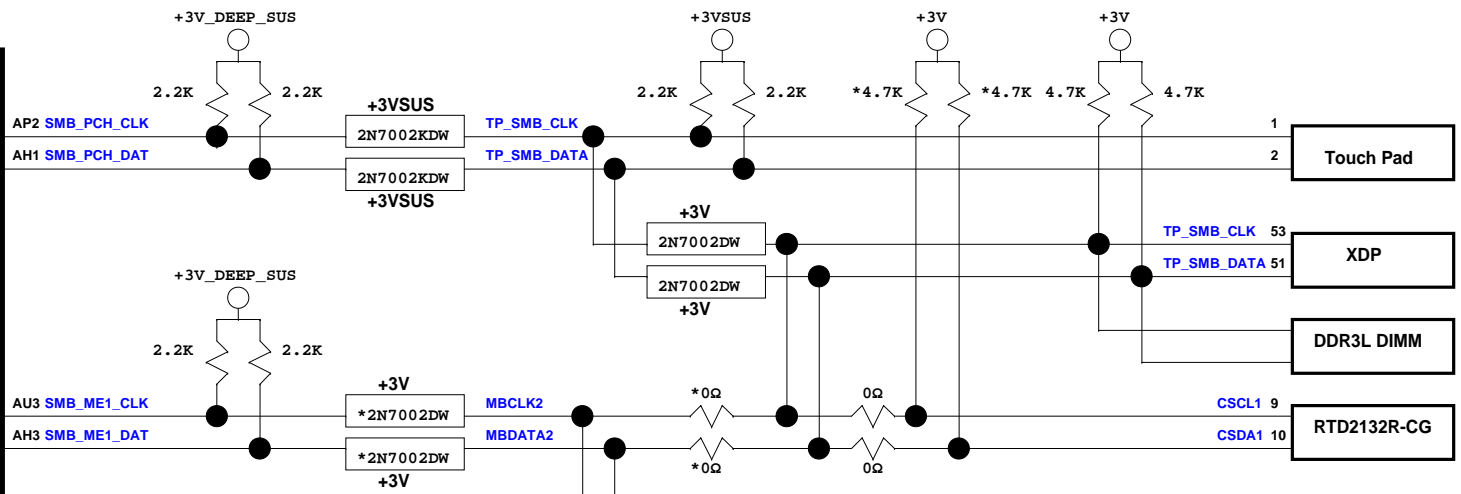
SATA Master	Port Assignment	Power control pin
SATA0	HDD	N/A
SATA1	mSATA	N/A
SATA2	NC	N/A
SATA3/PCIE	Card reader	N/A

PCIE	Port Assignment	Control pin
PCIE 5_L0	PEG0	
PCIE 5_L1	PEG1	
PCIE 5_L2	PEG2	
PCIE 5_L3	PEG3	
PCIE 1	NC	
PCIE 2	NC	
PCIE 3	WLAN	
PCIE 4	LAN	

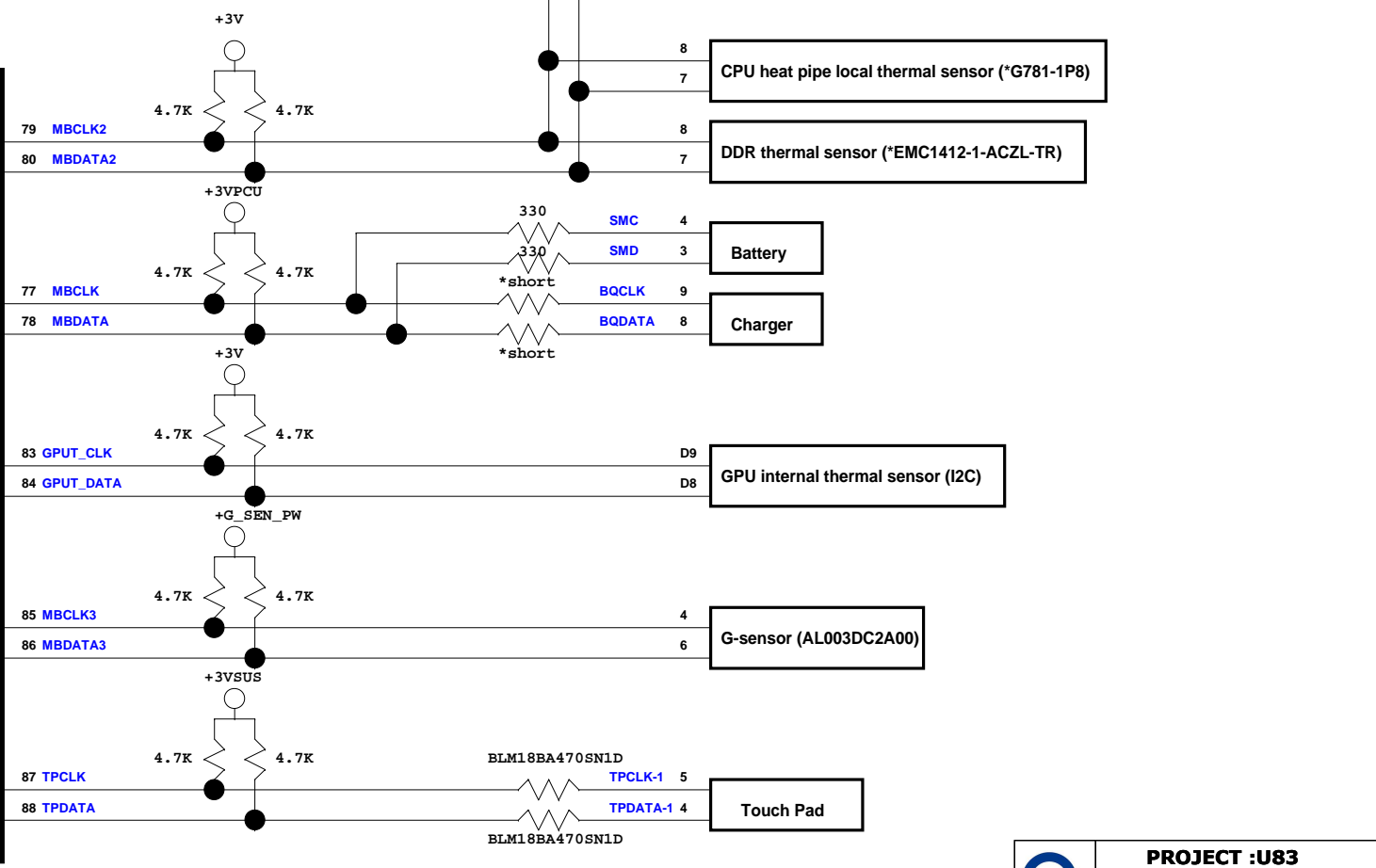


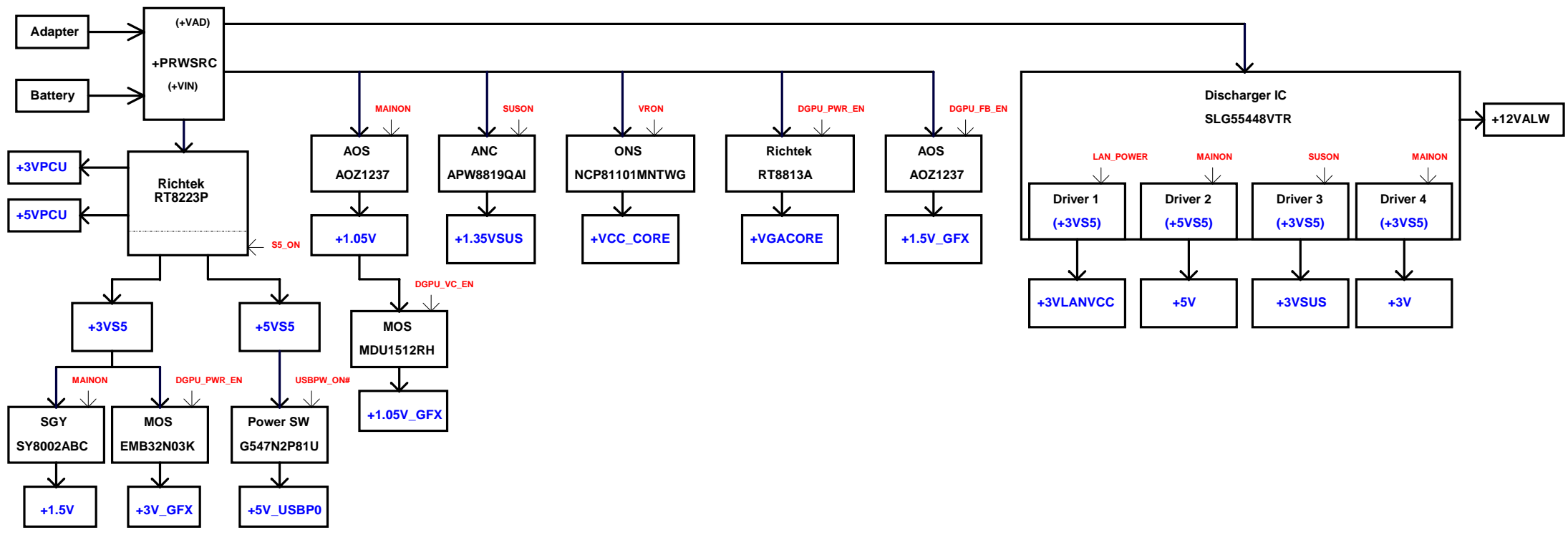
PROJECT :U83
Quanta Computer Inc.

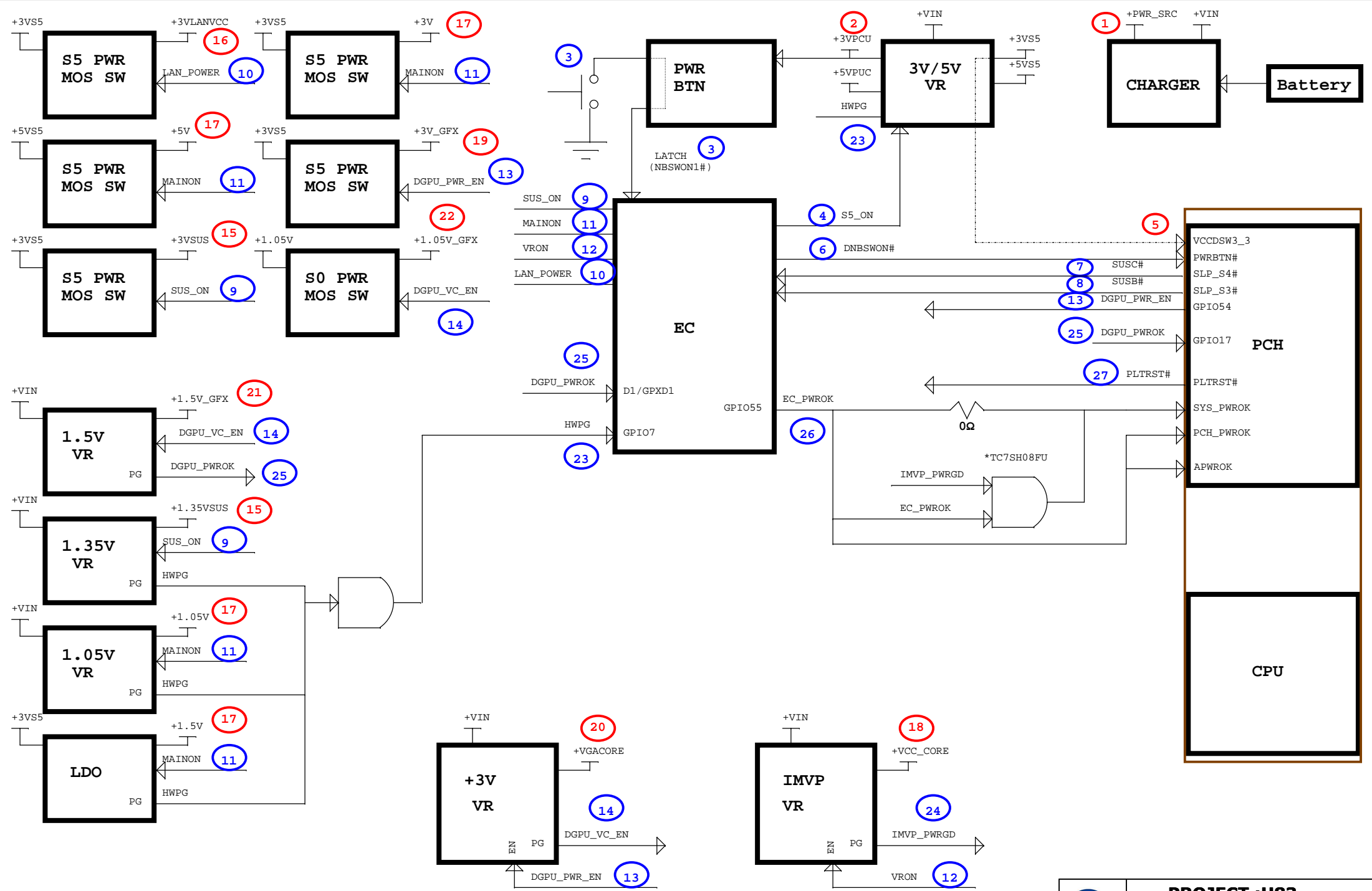
Haswell ULT



EC KB9010QF







www.s-manuals.com