Compal confidential

Schematics Document
Mobile Yonah uFCPGA with Intel
Calistoga_P/GM+ ICH7-M core logic

2005-10-26

REV:0.3

Security Classification	Compal Secret Data		
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Title: *Cover Sheet*		
Size: Custom	Document Number: *LA-2952P*	Rev: 0.3
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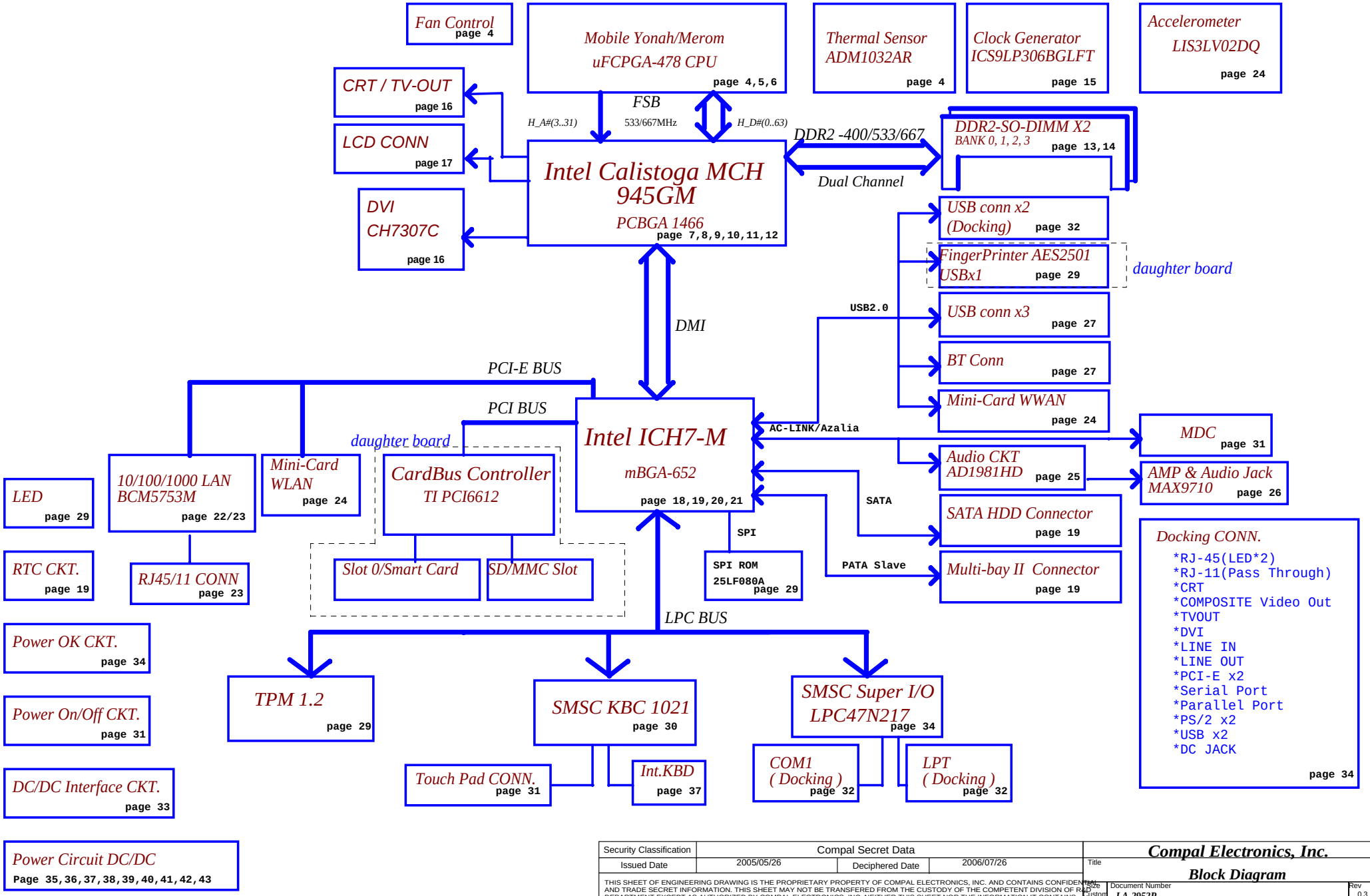
File Name : LA-2952P

Caymus



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Title: Block Diagram		
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Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (18.5V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VCCP	1.05V power rail for Processor I/O and MCH/ICH core power	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDRII Vtt	ON	OFF	OFF
+1.5VS	1.5V switched power rail for PCI-E interface	ON	OFF	OFF
+1.8V	1.8V power rail for DDRII	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail for MCH video PLL	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+RTC_VCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

Internal PCI Devices

DEVICE	Bus	PCI Device ID	IDSEL #
LAN	1	D8	AD24
Azalia	0	D27	AD11
PCI-E	0	D28	AD12
USB1.1/2.0	0	D29	AD13
PCI to PCI (DMI to PCI)	0	D30	AD14
AC97 MODEM	0	D30	AD14
AC97 Audio	0	D30	AD14
PATA/SATA	0	D31	AD15
LPC I/F	0	D31	AD15
SMBUS	0	D31	AD15
CPU I/F	0	D31	AD15
DMA	0	D31	AD15
PMU	0	D31	AD15

External PCI Devices

DEVICE	PCI Device ID	IDSEL #	REQ/GNT #	PIRQ
CARD BUS	D6	AD22	2	C D E G

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

Symbol Note :

: means Digital Ground

: means Analog Ground

@ : means just reserve , no build
M52@ : means build discrete sku with ATI VGA M52 .
UMA@ : means build UMA sku with Intel 945GM .

SPI@ : means just build when SPI I/F BIOS function reserve.
FWH@ : means just build when FWH I/F BIOS function reserve.
NOXDP@ : means just build when XDP function disable.
XDP@ : means just build when XDP function enable. When this time, docking PCI express will not work.

1021@ : means just build when SMsC KBC1021 chip selected.
LP@ : means just build when Low power clock gen. install
NOLP@ : means just build when Low power clock gen. NO install

45@ : means need be mounted when 45 level assy or rework stage.

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Title	Notes List	
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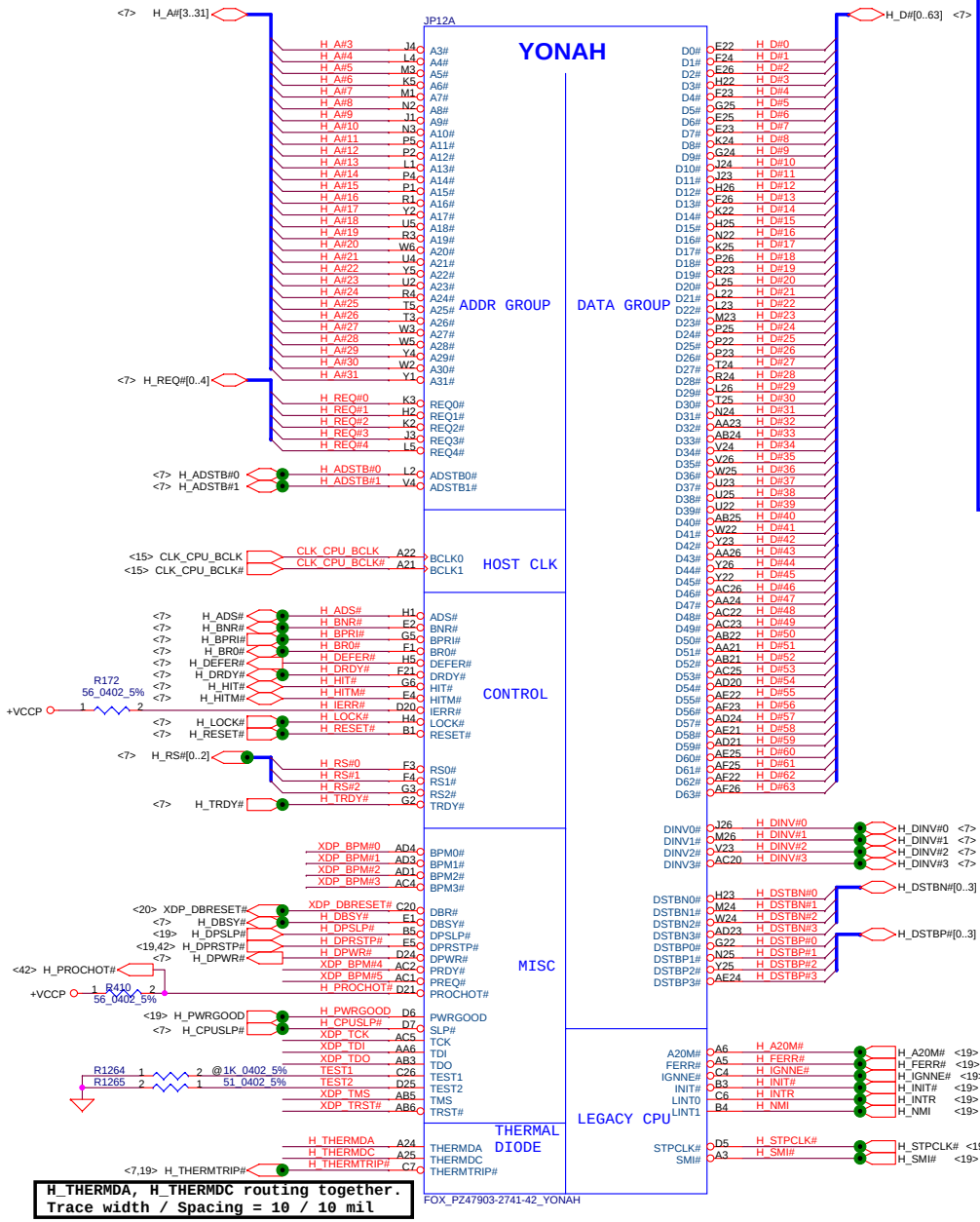

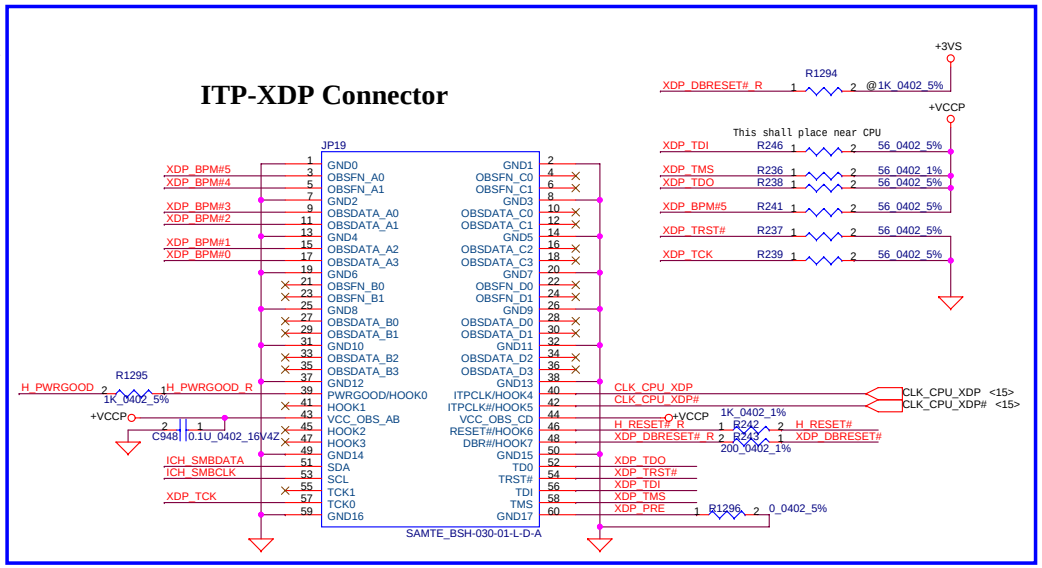

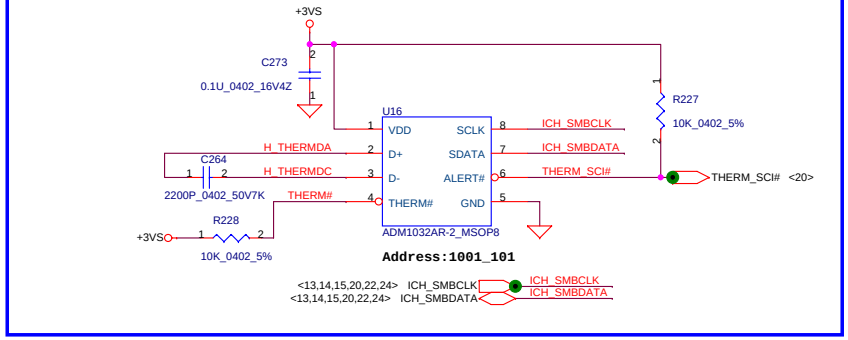

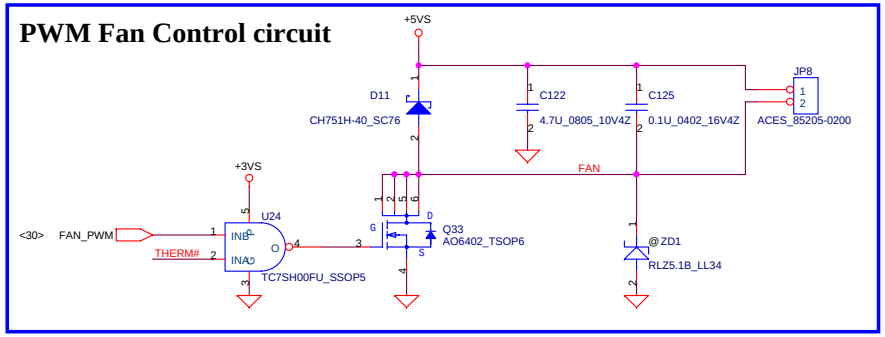

Security Classification	Compal Secret Data		
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Title: **Yonah CPU in mFCPGA479**

Size	Document Number	Rev
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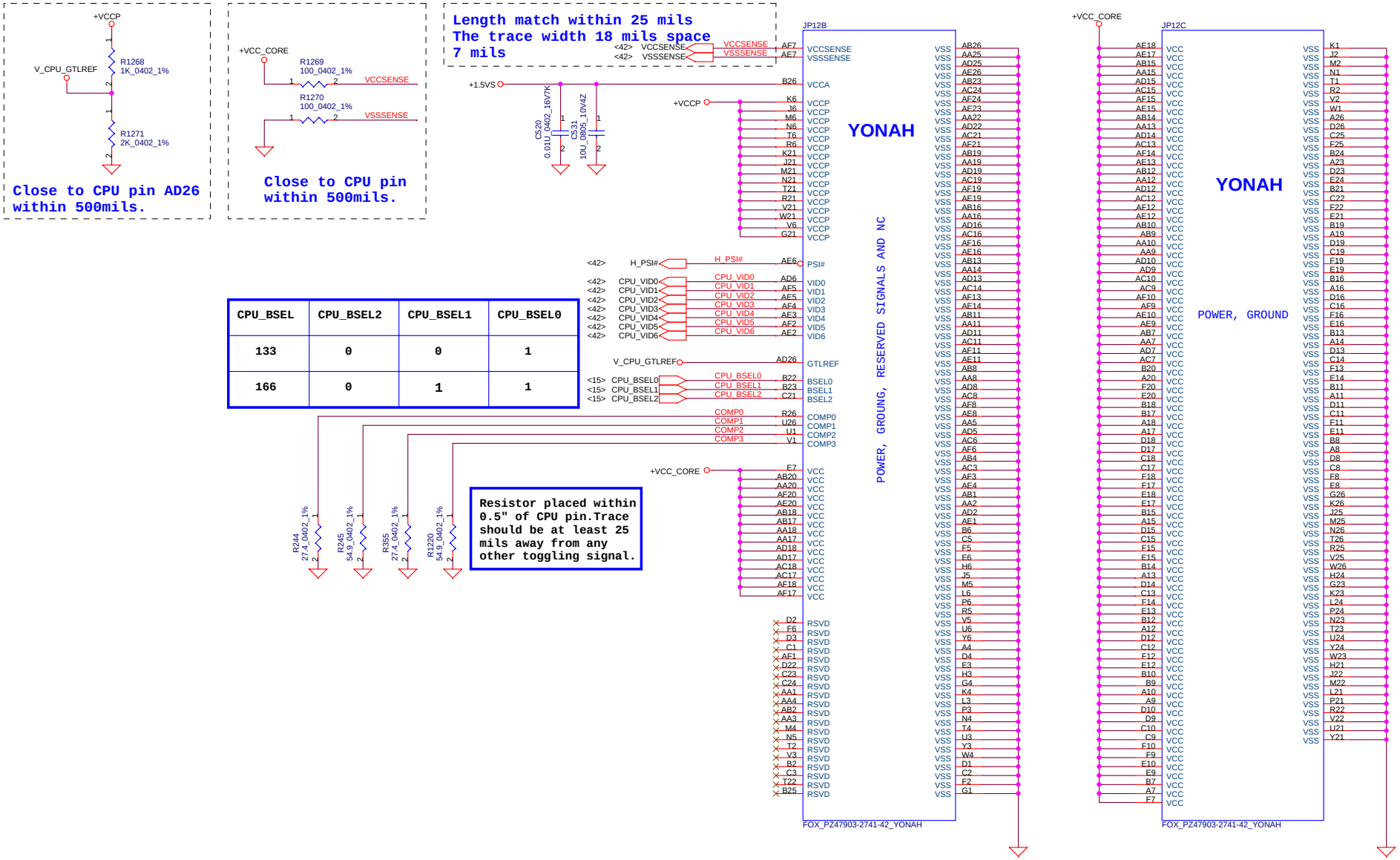

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1

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Title: Yonah CPU in mFCPGA479

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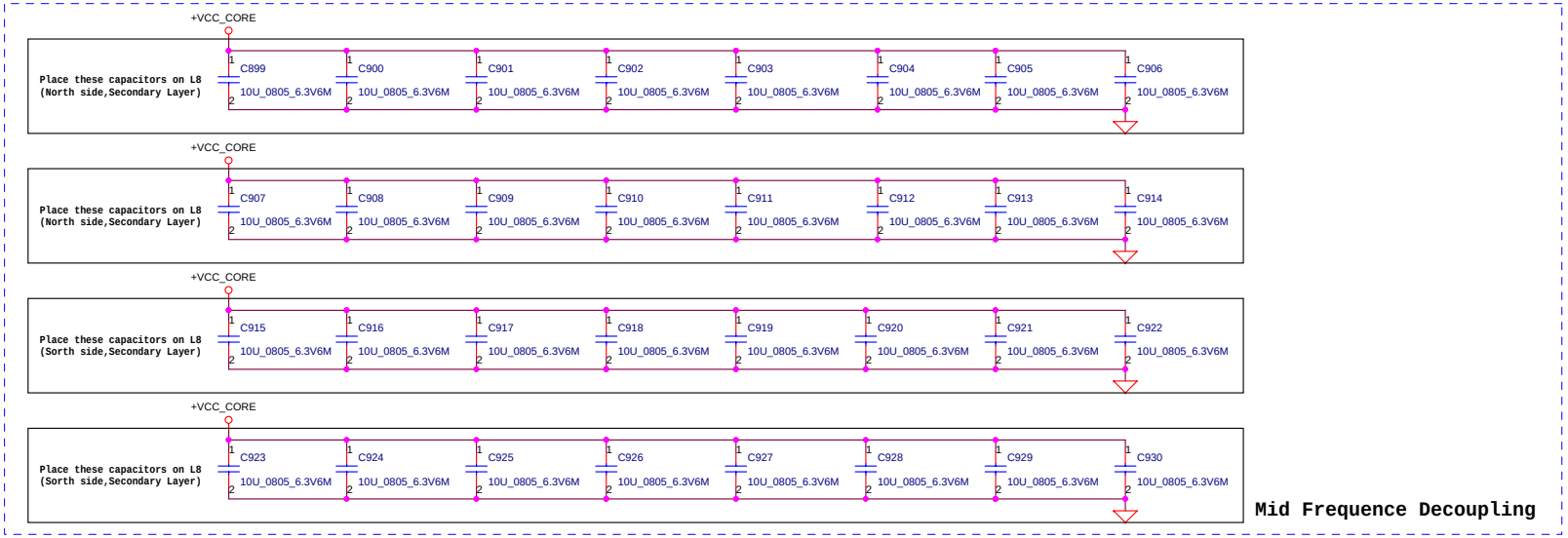
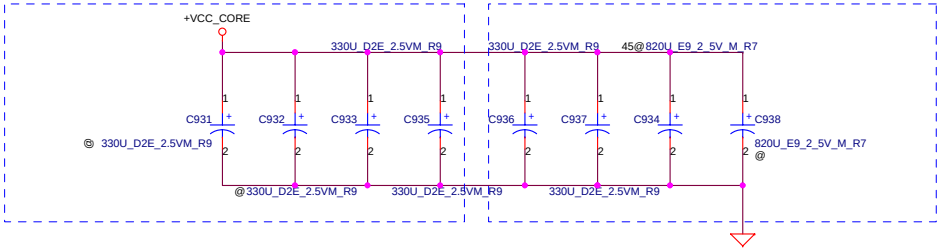
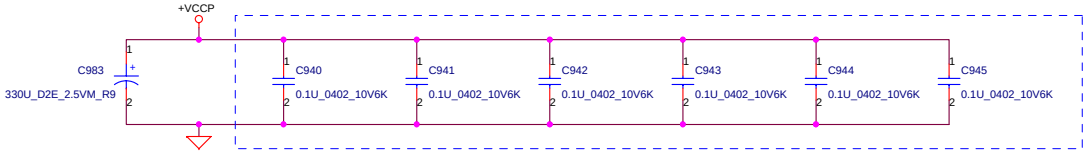


Mid Frequence Decoupling



ESR <= 1.5m ohm
Capacitor > 1980uF



Security Classification	Compal Secret Data		
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Title: **CPU Bypass capacitors**

Size	Document Number	Rev
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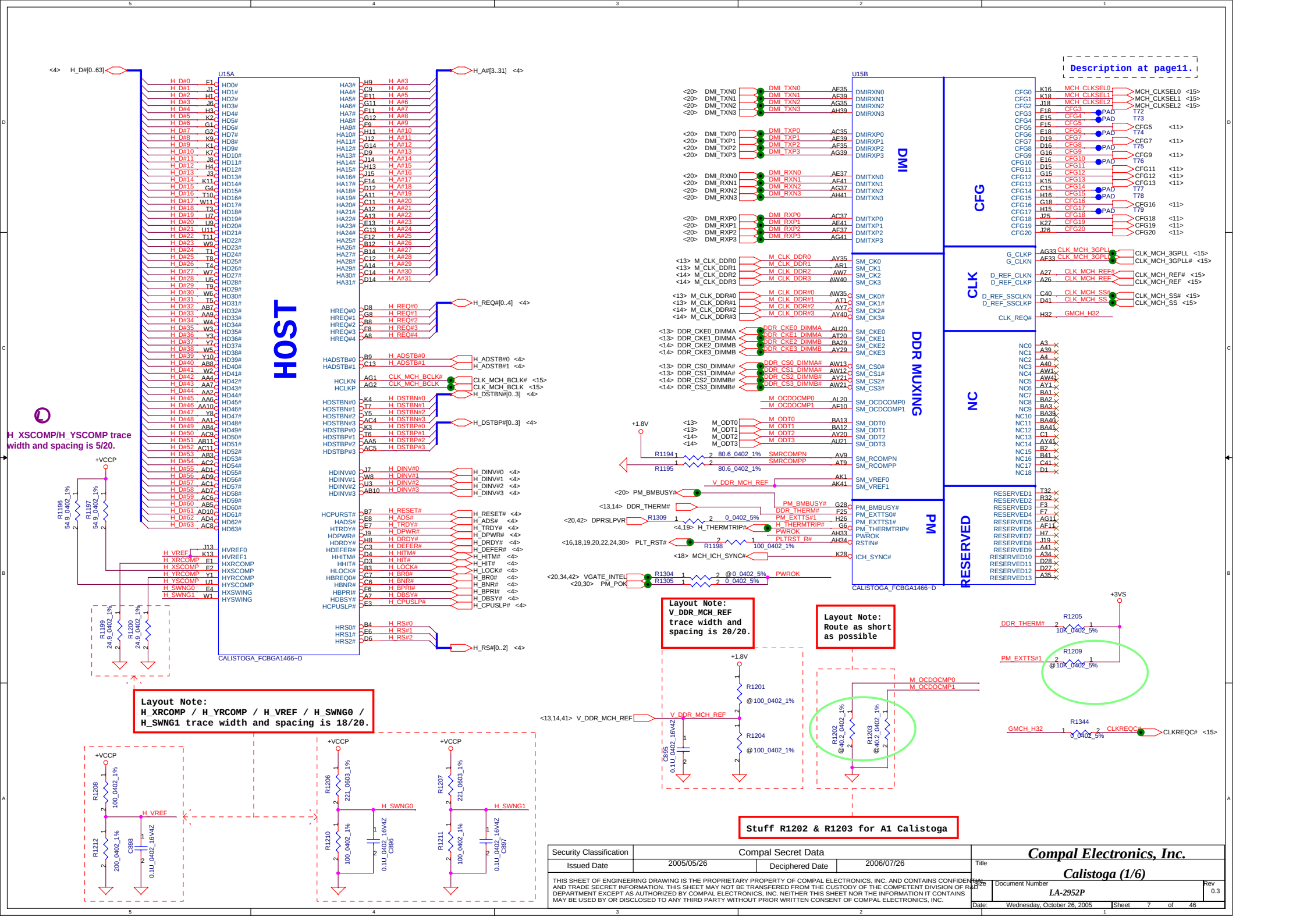
Description at page11.
U15A
HOST
CALISTOGA_FCBGA1466-D
U15B
DMI
DDR MUXING
CFG
CLK
NC
PM
RESERVED
CALISTOGA_FCBGA1466-D
H_XSCOMP/H_YSCOMP trace width and spacing is 5/20.
Layout Note: H_XRCOMP / H_YRCOMP / H_VREF / H_SWNG0 / H_SWNG1 trace width and spacing is 18/20.
Layout Note: V_DDR_MCH_REF trace width and spacing is 20/20.
Layout Note: Route as short as possible
Stuff R1202 & R1203 for A1 Calistoga
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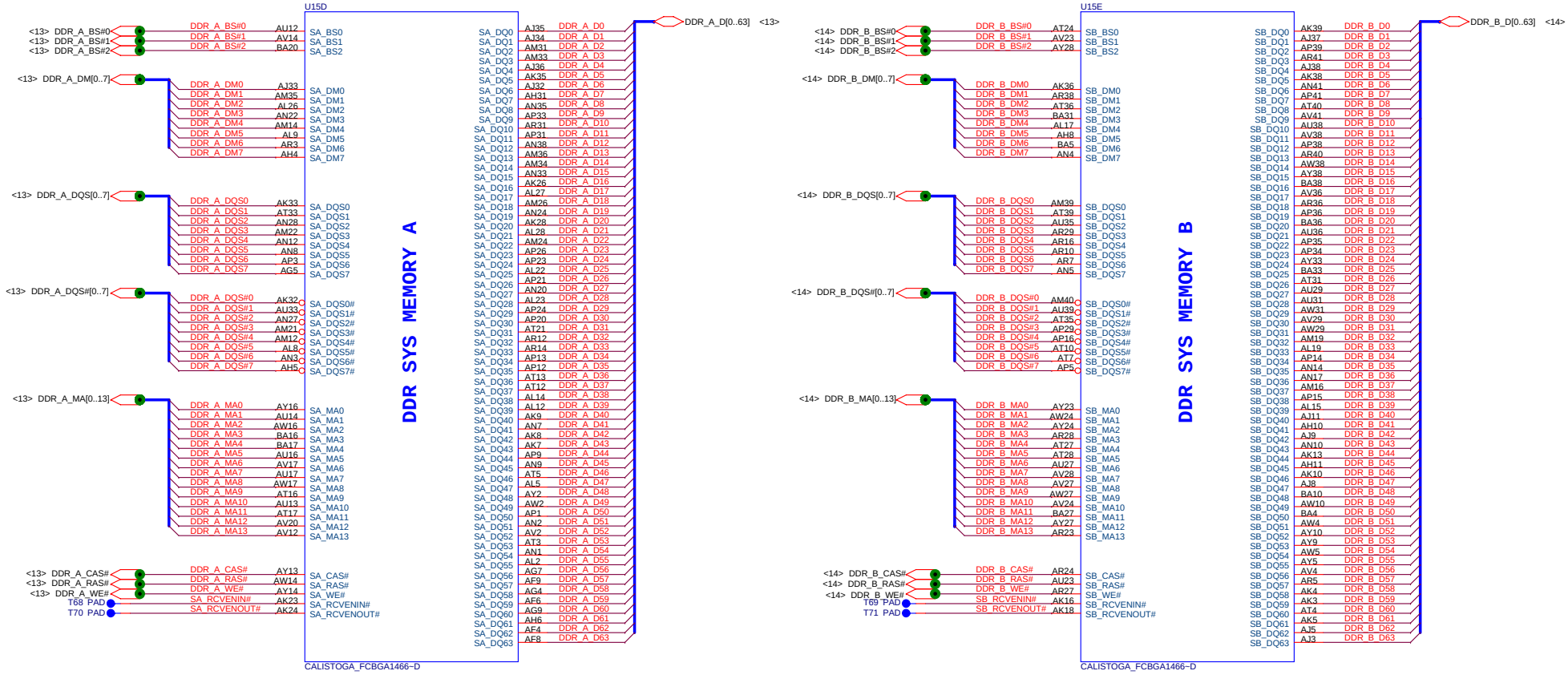

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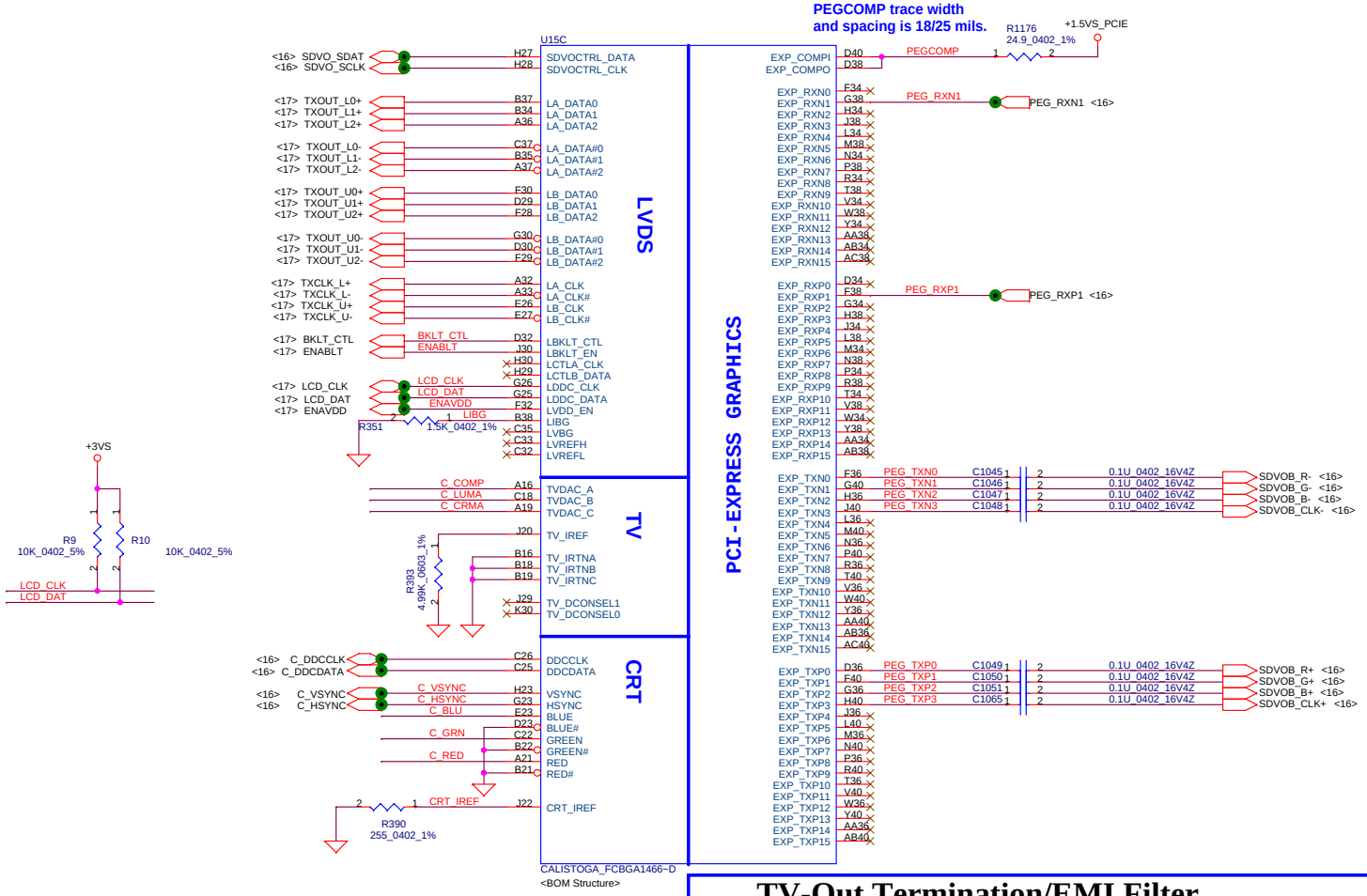
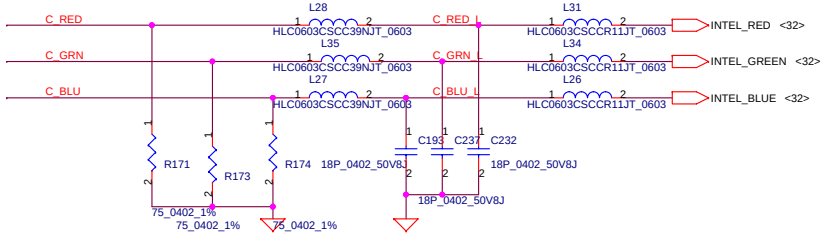
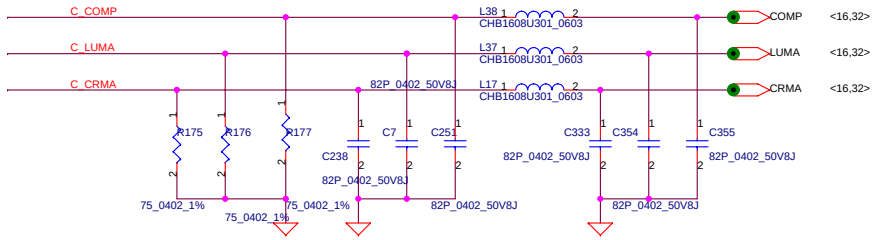


CRT Termination/EMI Filter



TV-Out Termination/EMI Filter



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Title: **Calistoga (3/6)**

Size	Document Number	Rev
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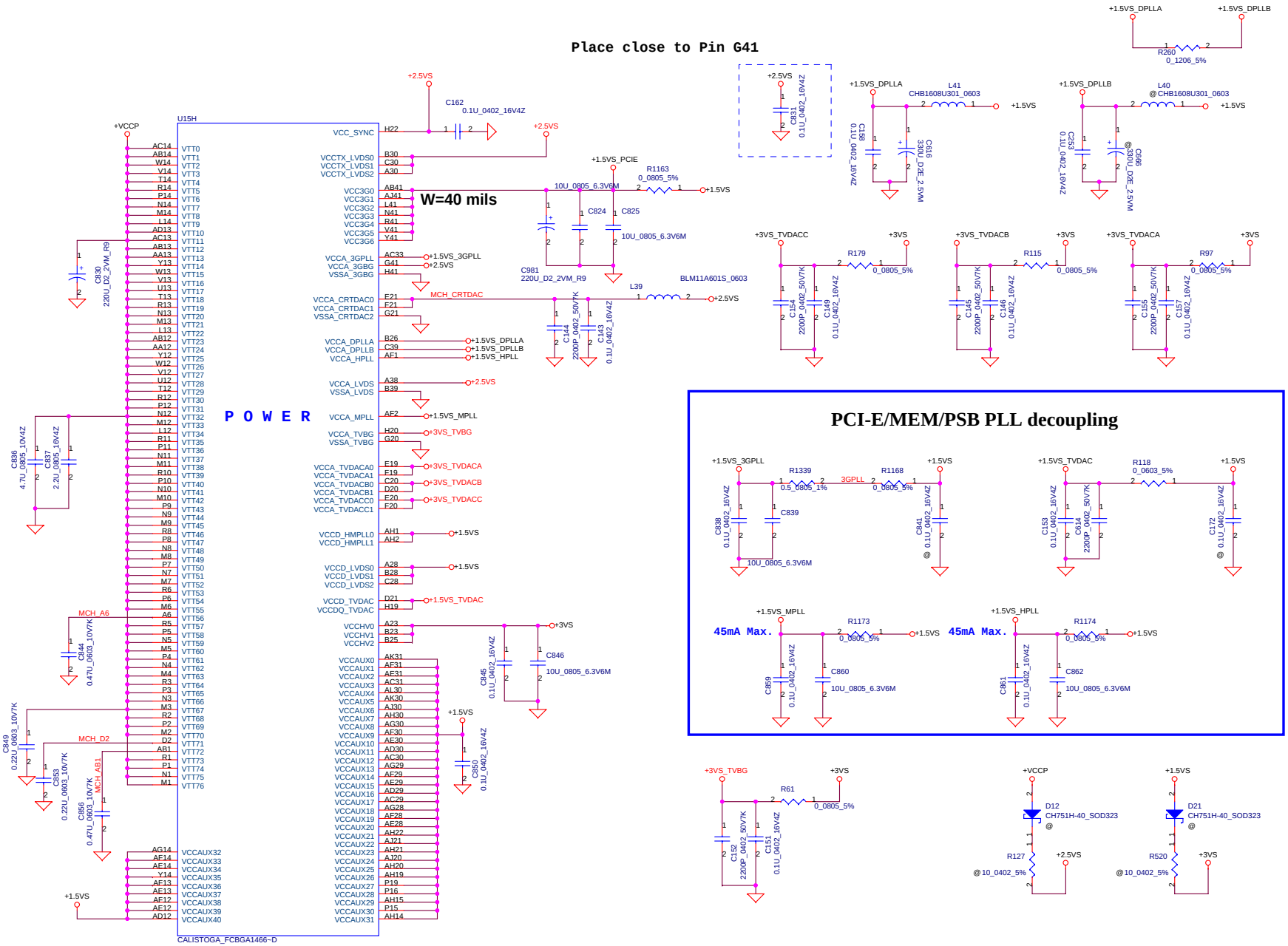

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Title: Calistoga (4/6)			
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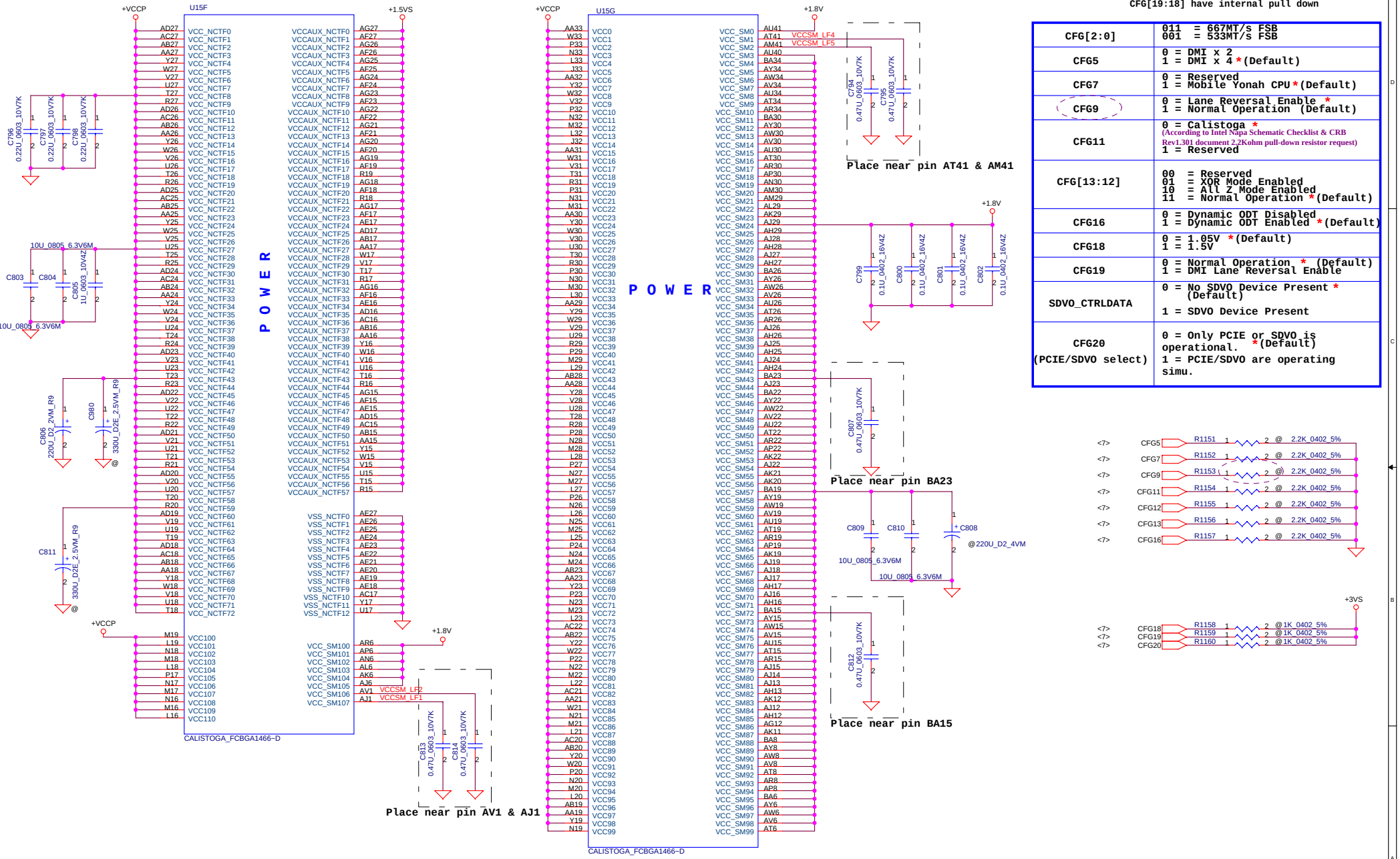
Strap Pin Table

CFG[3:17] have internal pull up

CFG[19:18] have internal pull down

CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU *(Default)
CFG9	0 = Lane Reversal Enable * 1 = Normal Operation (Default)
CFG11	0 = Calistoga * (According to Intel Napa Schematic Checklist & CRB Rev1.301 document 2.2Kohm pull-down resistor request) 1 = Reserved
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation *(Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG18	0 = 1.05V *(Default) 1 = 1.5V
CFG19	0 = Normal Operation * (Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present * (Default) 1 = SDVO Device Present
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. *(Default) 1 = PCIE/SDVO are operating simu.



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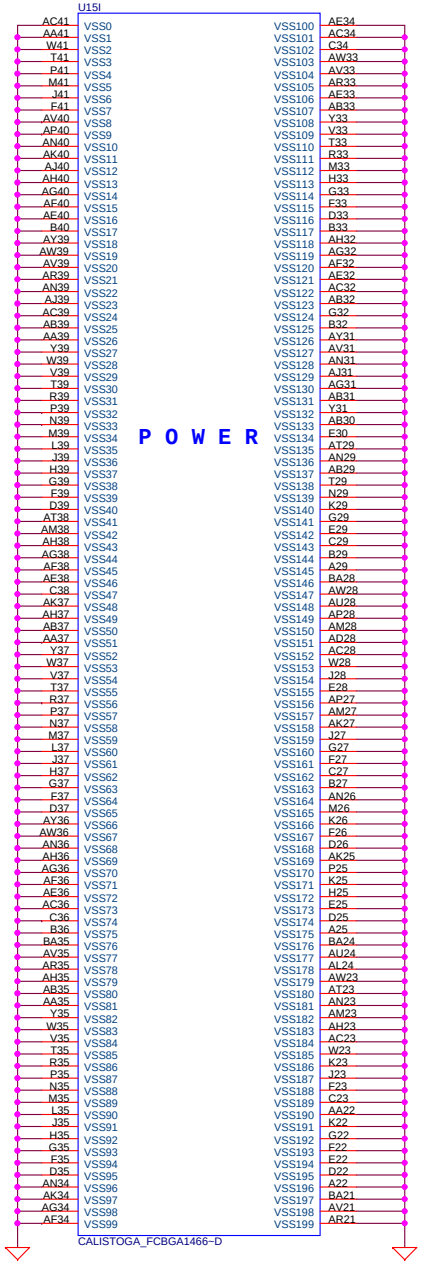

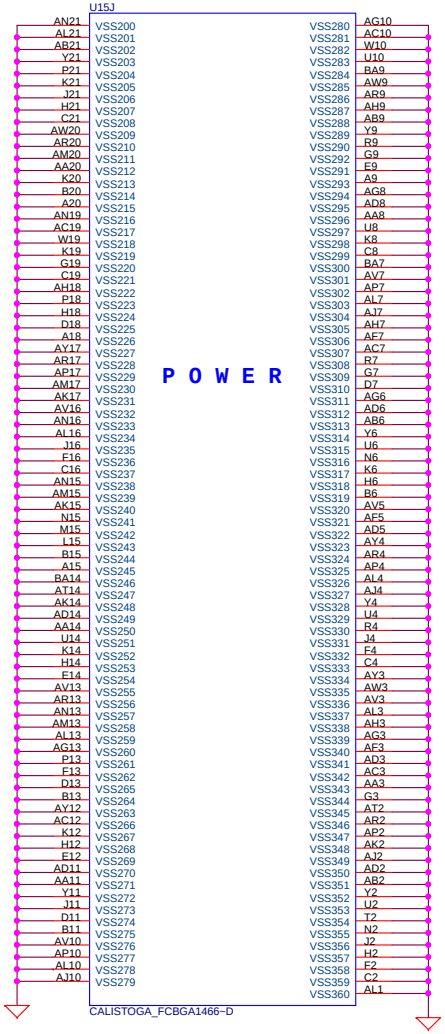

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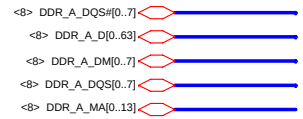
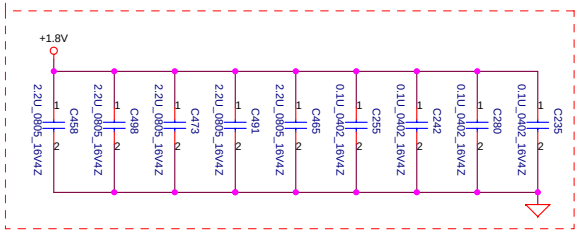
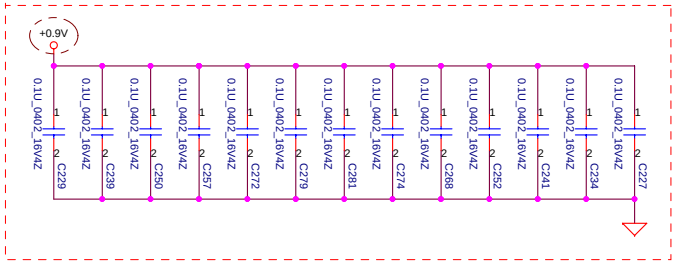
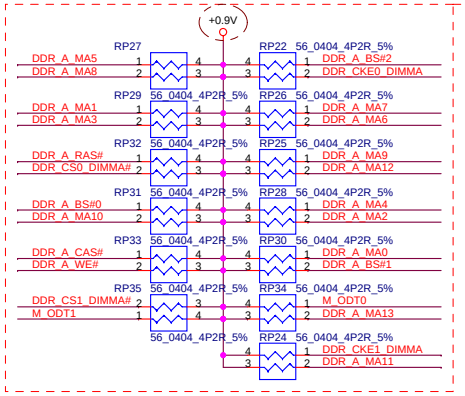


Layout Note:
Place near JP34

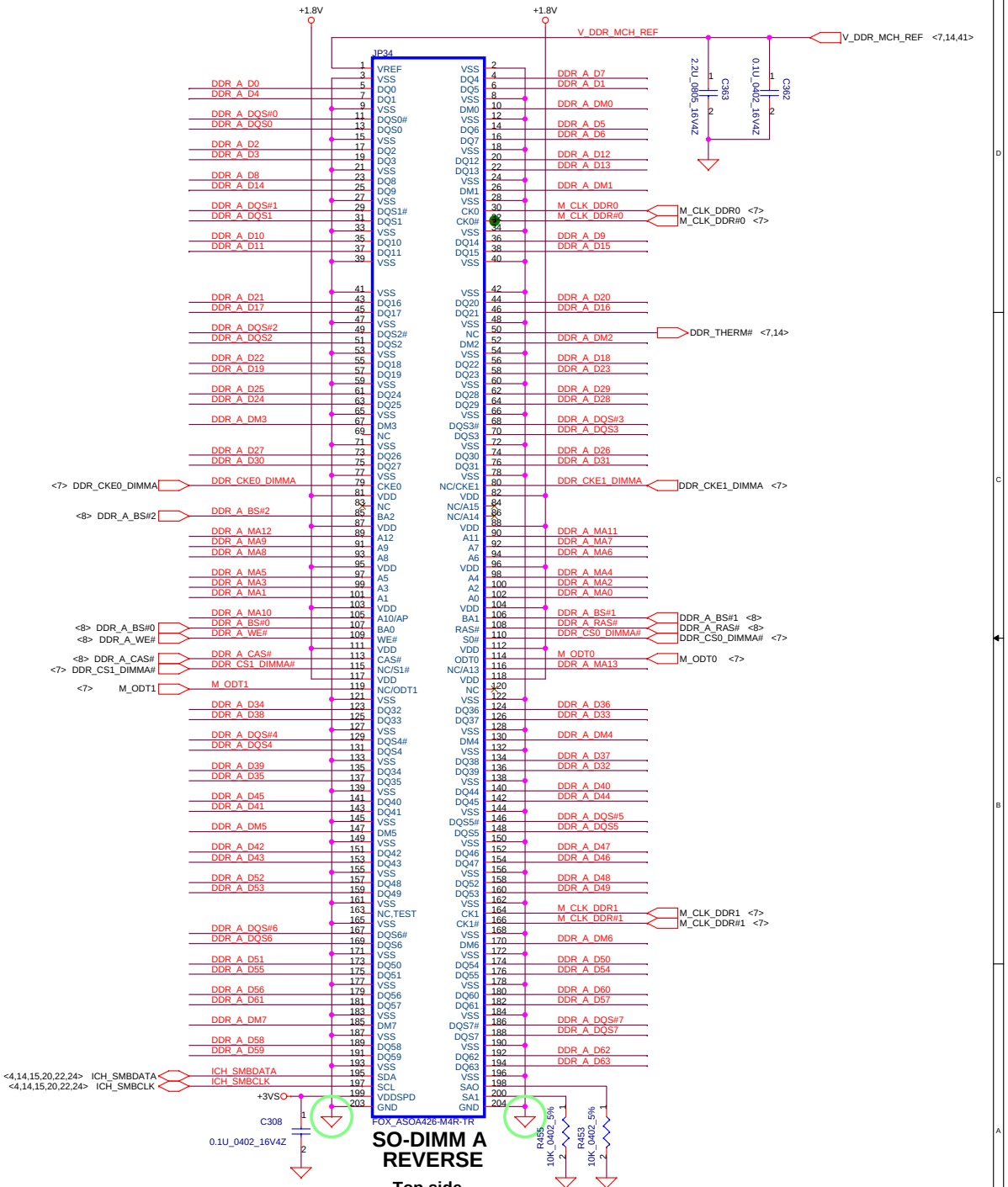


Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V





Layout Note:
Place these resistor closely JP34,all trace length Max=1.5"



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Title	*Compal Electronics, Inc.*
	DDRII-SODIMM SLOT1
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<8> DDR_B_DQS#[0..7]
<8> DDR_B_D[0..63]
<8> DDR_B_DM[0..7]
<8> DDR_B_DQS[0..7]
<8> DDR_B_MA[0..13]

Layout Note:
Place near JP34

+1.8V

2.2U_0805_16V4Z: C236, C265, C247, C159, C164
0.1U_0402_16V4Z: C166, C219, C188, C161

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V

+0.9V

0.1U_0402_16V4Z: C176, C179, C186, C197, C213, C220, C183, C210, C199, C173, C218, C163, C177

Layout Note:
Place these resistor closely JP10,all trace length Max=1.5"

+0.9V

RP14: DDR_B_MA1, DDR_B_MA3 / RP10_56_0404_4P2R_5%: DDR_B_MA9, DDR_B_MA12
RP17: DDR_B_BS#0, DDR_B_MA10 / RP11_56_0404_4P2R_5%: DDR_CKE3_DIMMB, DDR_B_MA11
RP16: DDR_B_MA0, DDR_B_BS#1 / RP12_56_0404_4P2R_5%: DDR_B_MA5, DDR_B_MA8
RP18: DDR_B_RAS#, DDR_CS2_DIMMB# / RP13_56_0404_4P2R_5%: DDR_B_MA7, DDR_B_MA6
RP19: DDR_B_CAS#, DDR_B_WE# / RP15_56_0404_4P2R_5%: DDR_B_MA4, DDR_B_MA2
RP23: DDR_CS3_DIMMB#, M_ODT3 / RP21_56_0404_4P2R_5%: M_ODT2, DDR_B_MA13
RP9: DDR_B_BS#2, DDR_CKE2_DIMMB
56_0404_4P2R_5%

+1.8V

V_DDR_MCH_REF → V_DDR_MCH_REF <7,13,41>

C89 2.2U_0805_16V4Z, C90 0.1U_0402_16V4Z

JP10 — FOX_ASOA426-M2RN-7F

1 VREF	2 VSS		
3 VSS	4 DQ4	DDR_B_D0	DDR_B_D4
5 DQ0	6 DQ5	DDR_B_D5	DDR_B_D1
7 DQ1	8 VSS		
9 VSS	10 DM0		DDR_B_DM0
11 DQS0#	12 VSS	DDR_B_DQS#0	
13 DQS0	14 DQ6	DDR_B_DQS0	DDR_B_D6
15 VSS	16 DQ7		DDR_B_D2
17 DQ2	18 VSS	DDR_B_D7	
19 DQ3	20 DQ12	DDR_B_D3	DDR_B_D12
21 VSS	22 DQ13		DDR_B_D13
23 DQ8	24 VSS	DDR_B_D8	
25 DQ9	26 DM1	DDR_B_D9	DDR_B_DM1
27 VSS	28 VSS		
29 DQS1#	30 CK0	DDR_B_DQS#1	M_CLK_DDR3 <7>
31 DQS1	32 CK0#	DDR_B_DQS1	M_CLK_DDR#3 <7>
33 VSS	34 VSS		
35 DQ10	36 DQ14	DDR_B_D10	DDR_B_D14
37 DQ11	38 DQ15	DDR_B_D11	DDR_B_D15
39 VSS	40 VSS		
41 VSS	42 VSS		
43 DQ16	44 DQ20	DDR_B_D21	DDR_B_D16
45 DQ17	46 DQ21	DDR_B_D20	DDR_B_D18
47 VSS	48 VSS		
49 DQS2#	50 NC	DDR_B_DQS#2	DDR_THERM# <7,13>
51 DQS2	52 DM2	DDR_B_DQS2	DDR_B_DM2
53 VSS	54 VSS		
55 DQ18	56 DQ22	DDR_B_D22	DDR_B_D17
57 DQ19	58 DQ23	DDR_B_D23	DDR_B_D19
59 VSS	60 VSS		
61 DQ24	62 DQ28	DDR_B_D24	DDR_B_D26
63 DQ25	64 DQ29	DDR_B_D25	DDR_B_D28
65 VSS	66 VSS		
67 DM3	68 DQS3#	DDR_B_DM3	DDR_B_DQS#3
69 NC	70 DQS3		DDR_B_DQS3
71 VSS	72 VSS		
73 DQ26	74 DQ30	DDR_B_D30	DDR_B_D29
75 DQ27	76 DQ31	DDR_B_D31	DDR_B_D27
77 VSS	78 VSS		
79 CKE0	80 NC/CKE1	<7> DDR_CKE2_DIMMB	DDR_CKE3_DIMMB <7>
81 VDD	82 VDD		
83 NC	84 NC/A15		
85 BA2	86 NC/A14	<8> DDR_B_BS#2	
87 VDD	88 VDD		
89 A12	90 A11	DDR_B_MA12	DDR_B_MA11
91 A9	92 A7	DDR_B_MA9	DDR_B_MA7
93 A8	94 A6	DDR_B_MA8	DDR_B_MA6
95 VDD	96 VDD		
97 A5	98 A4	DDR_B_MA5	DDR_B_MA4
99 A3	100 A2	DDR_B_MA3	DDR_B_MA2
101 A1	102 A0	DDR_B_MA1	DDR_B_MA0
103 VDD	104 VDD		
105 A10/AP	106 BA1	DDR_B_MA10	DDR_B_BS#1 <8>
107 BA0	108 RAS#	<8> DDR_B_BS#0	DDR_B_RAS# <8>
109 WE#	110 S0#	<8> DDR_B_WE#	DDR_CS2_DIMMB# <7>
111 VDD	112 VDD		
113 CAS#	114 ODT0	<8> DDR_B_CAS#	M_ODT2
115 NC/S1#	116 NC/A13	<7> DDR_CS3_DIMMB#	DDR_B_MA13 <7>
117 VDD	118 VDD		
119 NC/ODT1	120 NC	<7> M_ODT3	M_ODT2 <7>
121 VSS	122 VSS		
123 DQ32	124 DQ36	DDR_B_D37	DDR_B_D33
125 DQ33	126 DQ37	DDR_B_D36	DDR_B_D32
127 VSS	128 VSS		
129 DQS4#	130 DM4	DDR_B_DQS#4	DDR_B_DM4
131 DQS4	132 VSS	DDR_B_DQS4	
133 VSS	134 DQ38		DDR_B_D38
135 DQ34	136 DQ39	DDR_B_D35	DDR_B_D39
137 DQ35	138 VSS	DDR_B_D34	
139 VSS	140 DQ44		DDR_B_D44
141 DQ40	142 DQ45	DDR_B_D40	DDR_B_D45
143 DQ41	144 VSS	DDR_B_D41	
145 VSS	146 DQS5#		DDR_B_DQS#5
147 DM5	148 DQS5	DDR_B_DM5	DDR_B_DQS5
149 VSS	150 VSS		
151 DQ42	152 DQ46	DDR_B_D42	DDR_B_D43
153 DQ43	154 DQ47	DDR_B_D47	DDR_B_D46
155 VSS	156 VSS		
157 DQ48	158 DQ52	DDR_B_D48	DDR_B_D49
159 DQ49	160 DQ53	DDR_B_D53	DDR_B_D52
161 VSS	162 VSS		
163 NC,TEST	164 CK1		M_CLK_DDR2 <7>
165 VSS	166 CK1#		M_CLK_DDR#2 <7>
167 DQS6#	168 VSS	DDR_B_DQS#6	
169 DQS6	170 DM6	DDR_B_DQS6	DDR_B_DM6
171 VSS	172 VSS		
173 DQ50	174 DQ54	DDR_B_D51	DDR_B_D54
175 DQ51	176 DQ55	DDR_B_D50	DDR_B_D55
177 VSS	178 VSS		
179 DQ56	180 DQ60	DDR_B_D60	DDR_B_D56
181 DQ57	182 DQ61	DDR_B_D61	DDR_B_D57
183 VSS	184 VSS		
185 DM7	186 DQS7#	DDR_B_DM7	DDR_B_DQS#7
187 VSS	188 DQS7		DDR_B_DQS7
189 DQ58	190 VSS	DDR_B_D58	
191 DQ59	192 DQ62	DDR_B_D59	DDR_B_D62
193 VSS	194 DQ63		DDR_B_D63
195 SDA	196 VSS	<4,13,15,20,22,24> ICH_SMBDATA	
197 SCL	198 SA0	<4,13,15,20,22,24> ICH_SMBCLK	
199 VDDSPD	200 SA1	+3VS	
203 GND	204 GND		

ICH_SMBDATA, ICH_SMBCLK

C301 0.1U_0402_16V4Z

R257 10K_0402_5% → +3VS

R254 10K_0402_5%

SO-DIMM B
STANDARD
Bottom side

Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

Compal Electronics, Inc.

Title: DDRII-SODIMM SLOT2

Size: Document Number: LA-2952P Rev: 0.3

Date: Wednesday, October 26, 2005 Sheet 14 of 46

FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	1	133	100	33.3
0	1	1	166	100	33.3

Table : ICS954306

FSB Frequency Selet:

CPU Driven *(Default)	Stuff	CLK_Ra CLK_Rb CLK_Rc
	No Stuff	CLK_Rd CLK_Re CLK_Rf
533MHz	Stuff	CLK_Rd CLK_Re CLK_Rf
	No Stuff	CLK_Ra CLK_Rb CLK_Rc
667MHz	Stuff	CLK_Rd CLK_Rf
	No Stuff	CLK_Ra CLK_Rb CLK_Rc CLK_Re

Place close to U25

Place crystal within 500 mils of CK410

Routing the trace at least 10mil

NOXDP@ : means just build when XDP function disable.

XDP@ : means just build when XDP function enable. When this time, docking PCI express will not work.

LCD(Low)/SRC(High) clock select

*High:Pin18/19 = 100MHz
Low:Pin18/19 = 96MHz

Pin44/45 function select

High:Pin44/45 = CLKREQ
*Low:Pin44/45 = CPUCLK2_ITP

ICS9LP306_TSSOP64

* Internal Pull-Up Resistor
** Internal Pull-Down Resistor

Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

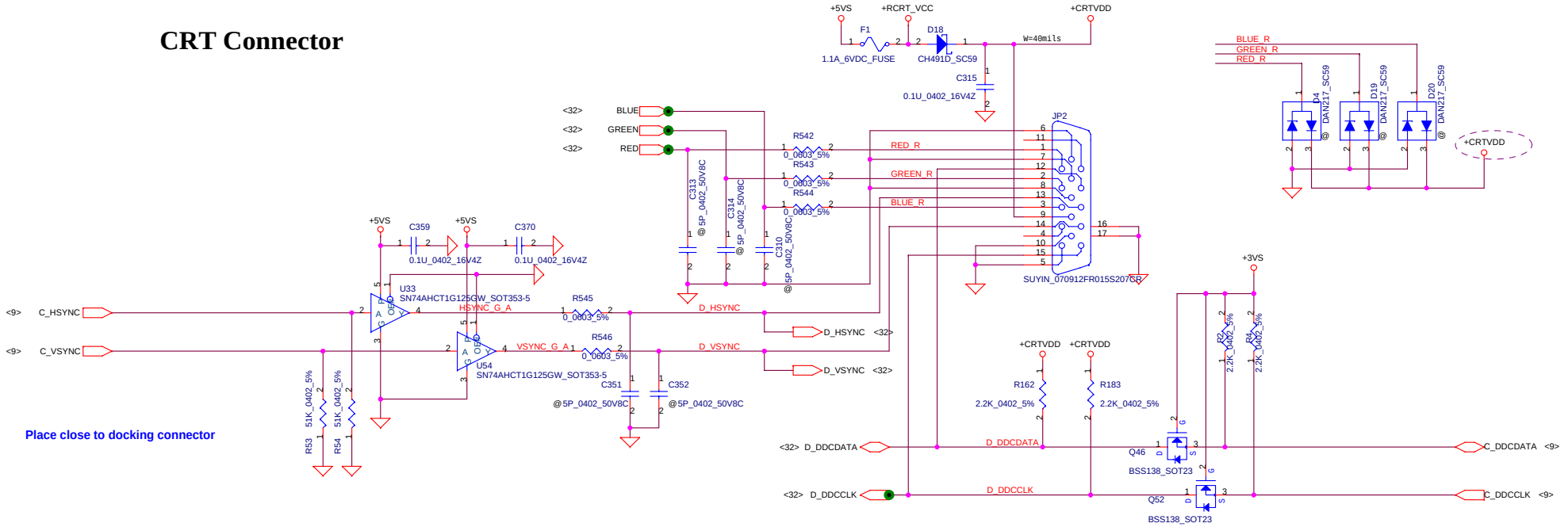
Compal Electronics, Inc.

Title: Clock generator

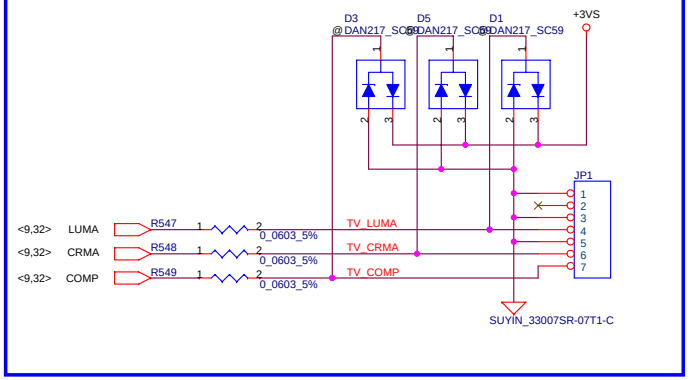
Size: Document Number: LA-2952P Rev: 0.3

Date: Wednesday, October 26, 2005 Sheet 15 of 46

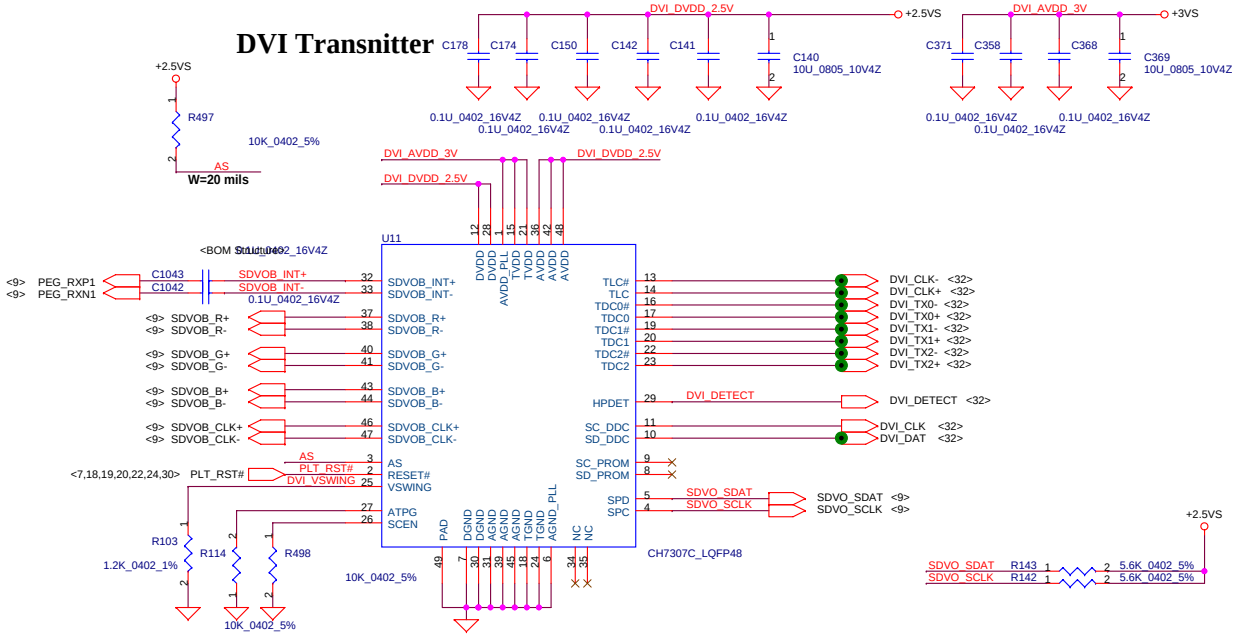
CRT Connector



TV-Out Connector



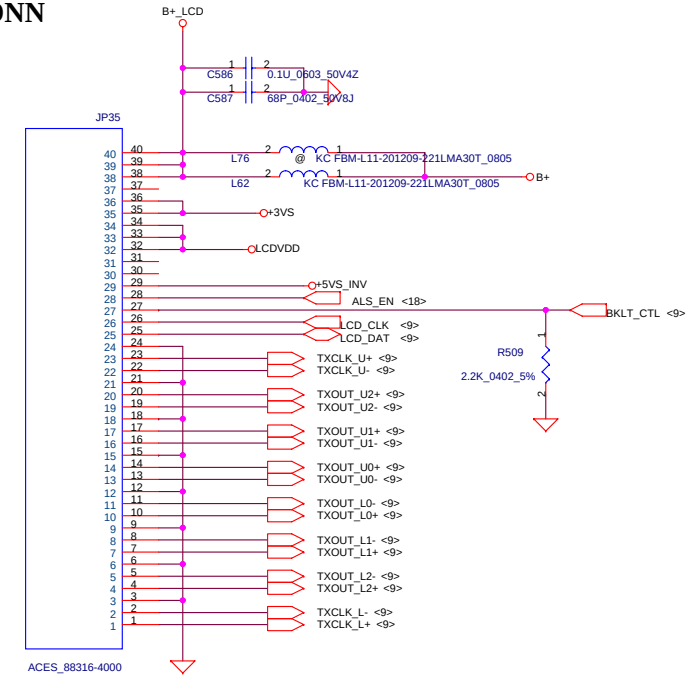
DVI Transnitter



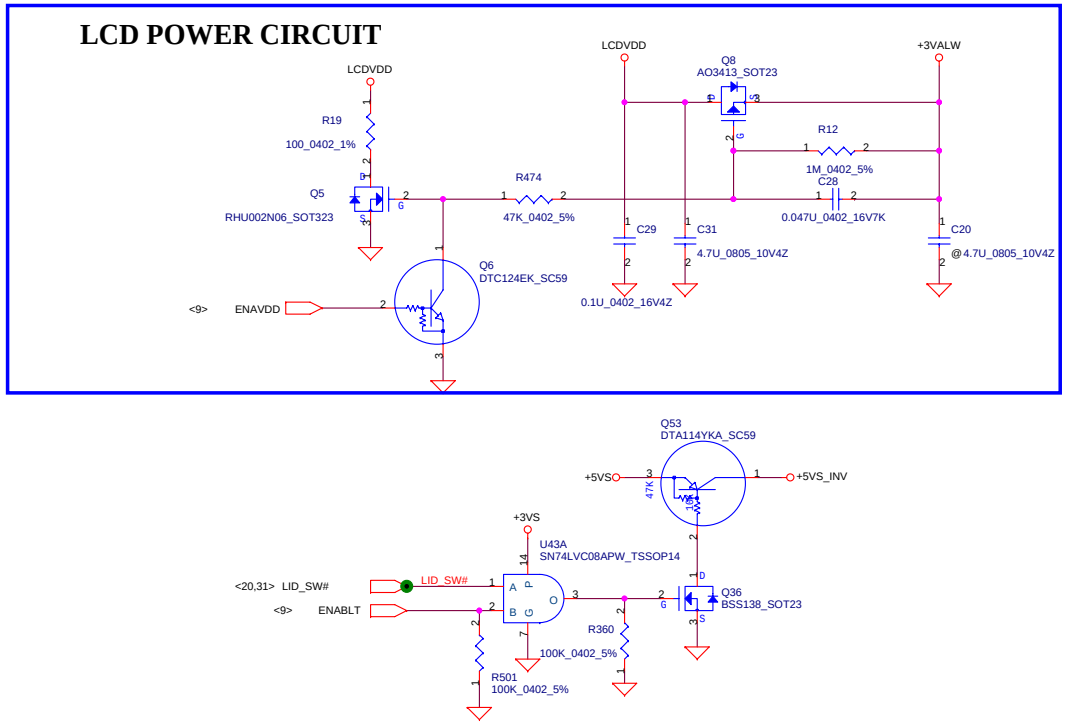
Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

Compal Electronics, Inc.			
Title: CRT & TVout Connector			
Size	Document Number: LA-2952P		Rev: 0.3
Date: Wednesday, October 26, 2005	Sheet 16 of 46		

LVDS CONN

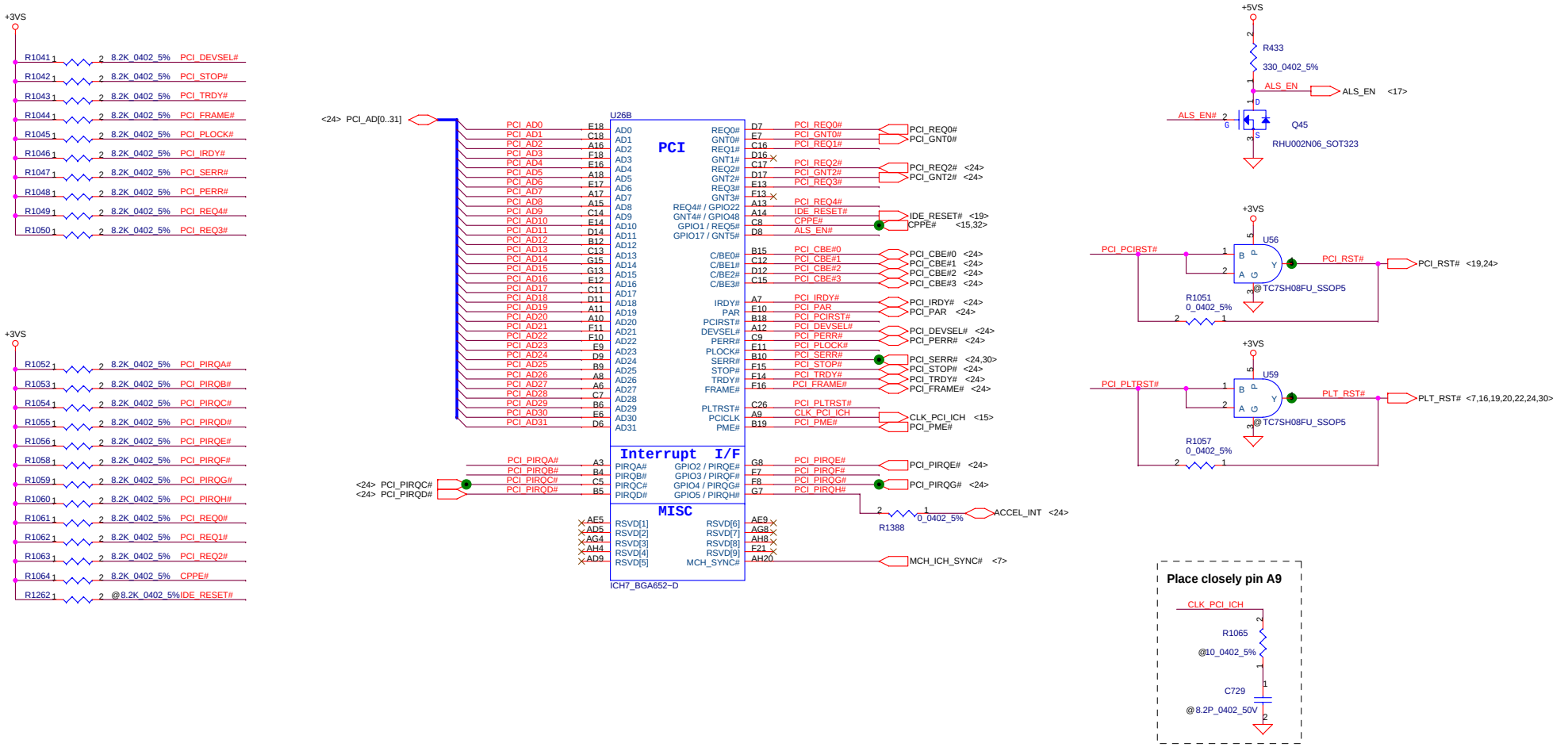


LCD POWER CIRCUIT



Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

Compal Electronics, Inc.			
Title: LCD CONN.			
Size	Document Number: LA-2952P		Rev: 0.3
Date: Wednesday, October 26, 2005	Sheet 17 of 46		



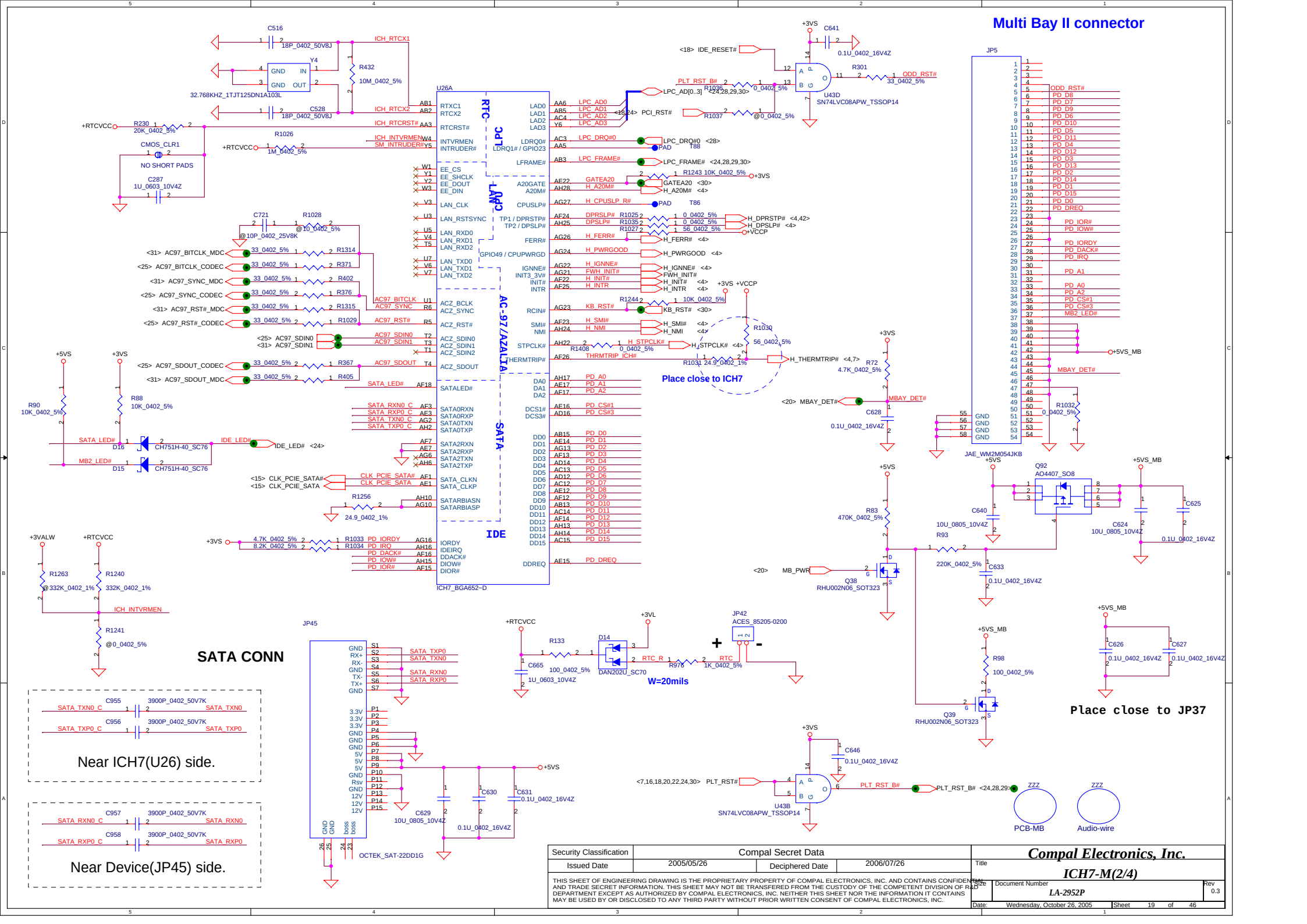
Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

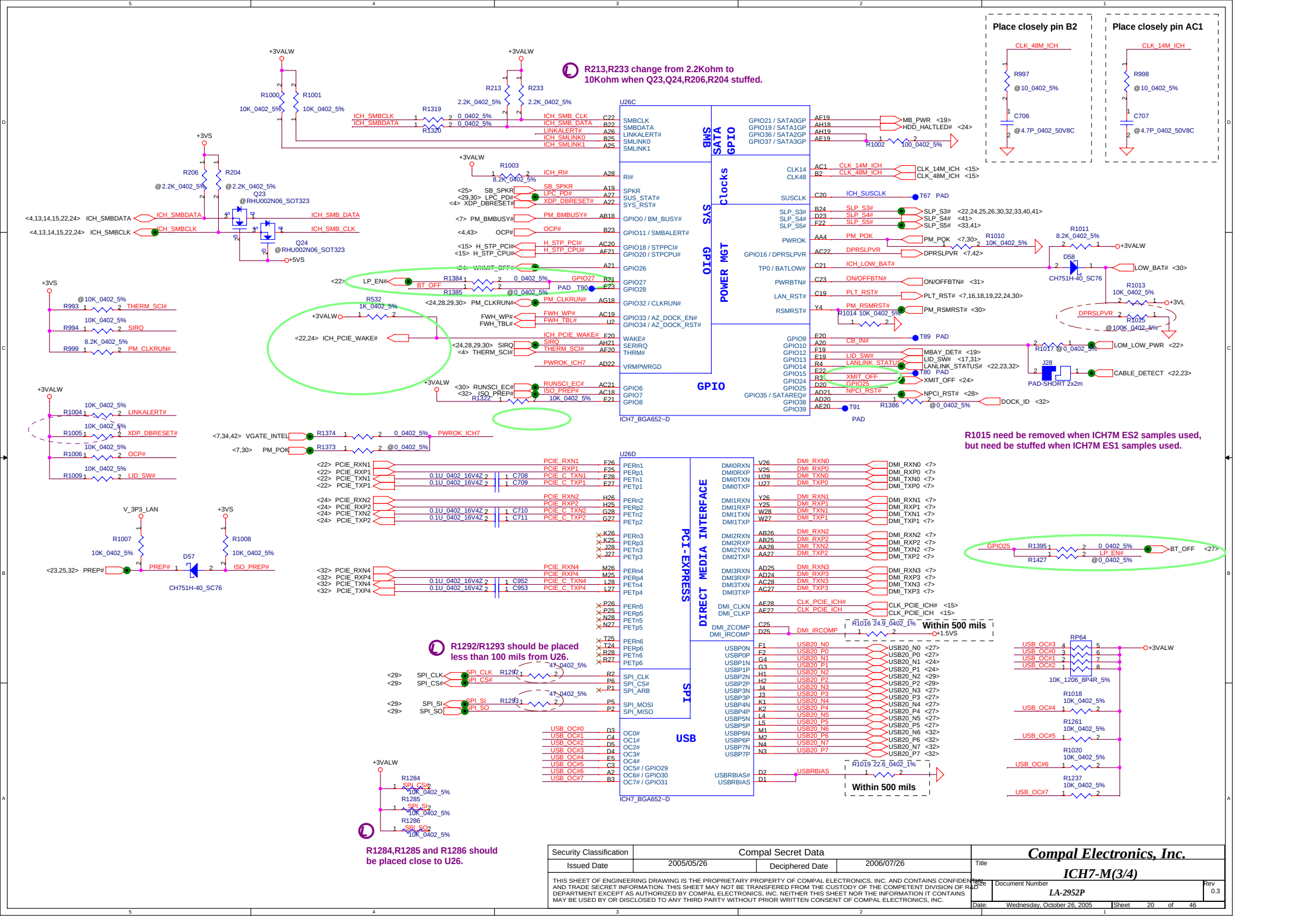
Compal Electronics, Inc.

Title: ICH7-M(1/4)

Size | Document Number: LA-2952P | Rev: 0.3

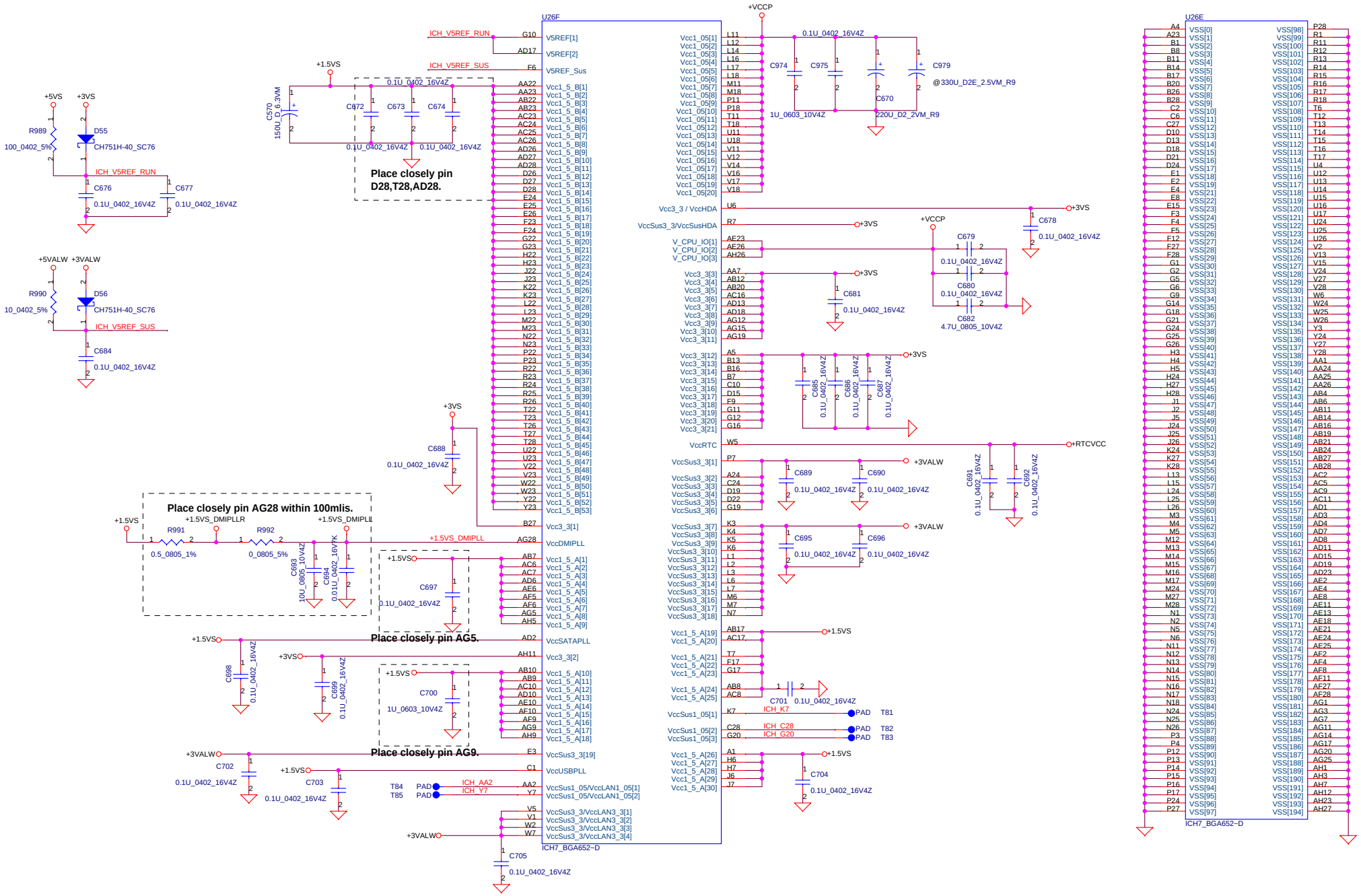
Date: Wednesday, October 26, 2005 | Sheet 18 of 46


Multi Bay II connector
U26A
RTC
LPC
LAN
AC-97/AZALIA
SATA
IDE
ICH7_BGA652-D
Place close to ICH7
Place close to JP37
SATA CONN
Near ICH7(U26) side.
Near Device(JP45) side.
W=20mils
JP5
JAE_WM2M054JKB
JP45
OCTEK_SAT-22DD1G
JP42
ACES_85205-0200
U43D
SN74LVC08APW_TSSOP14
U43B
SN74LVC08APW_TSSOP14
Q92
AO4407_SO8
Q38
RHU002N06_SOT323
Q39
RHU002N06_SOT323
D16
CH751H-40_SC76
D15
CH751H-40_SC76
D14
DAN202U_SC70
32.768KHZ_1TJT125DN1A103L
PCB-MB
Audio-wire
Security Classification
Compal Secret Data
Issued Date
2005/05/26
Deciphered Date
2006/07/26
Compal Electronics, Inc.
ICH7-M(2/4)
LA-2952P
Rev 0.3
Wednesday, October 26, 2005
Sheet 19 of 46



Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

Compal Electronics, Inc.			
Title: ICH7-M(3/4)			
Size	Document Number: LA-2952P		Rev: 0.3
Date: Wednesday, October 26, 2005	Sheet 20 of 46		



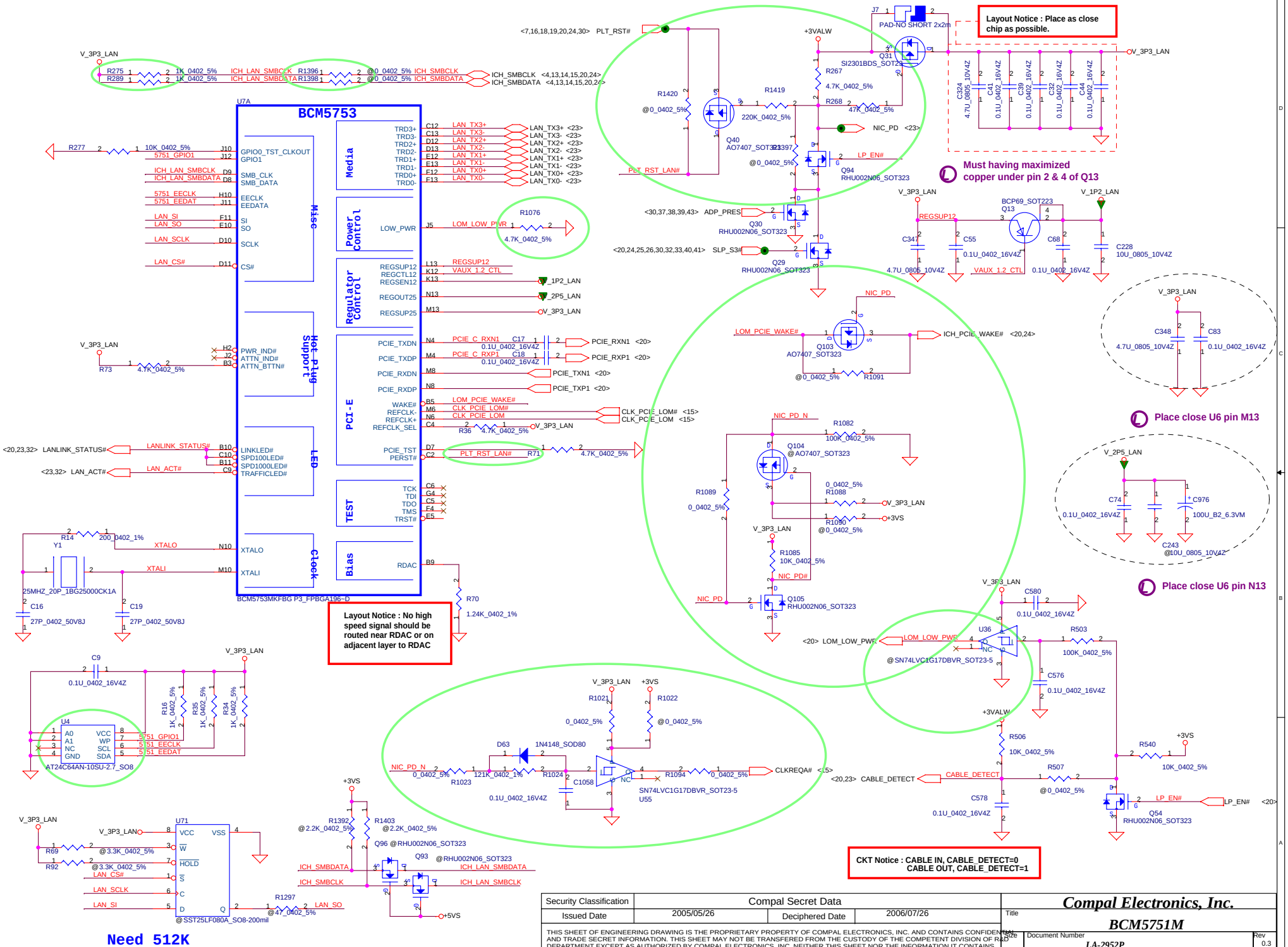
Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

Compal Electronics, Inc.

Title: **ICH7-M(4/4)**

Size	Document Number	Rev
	LA-2952P	0.3

Date: Wednesday, October 26, 2005 | Sheet 21 of 46



Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

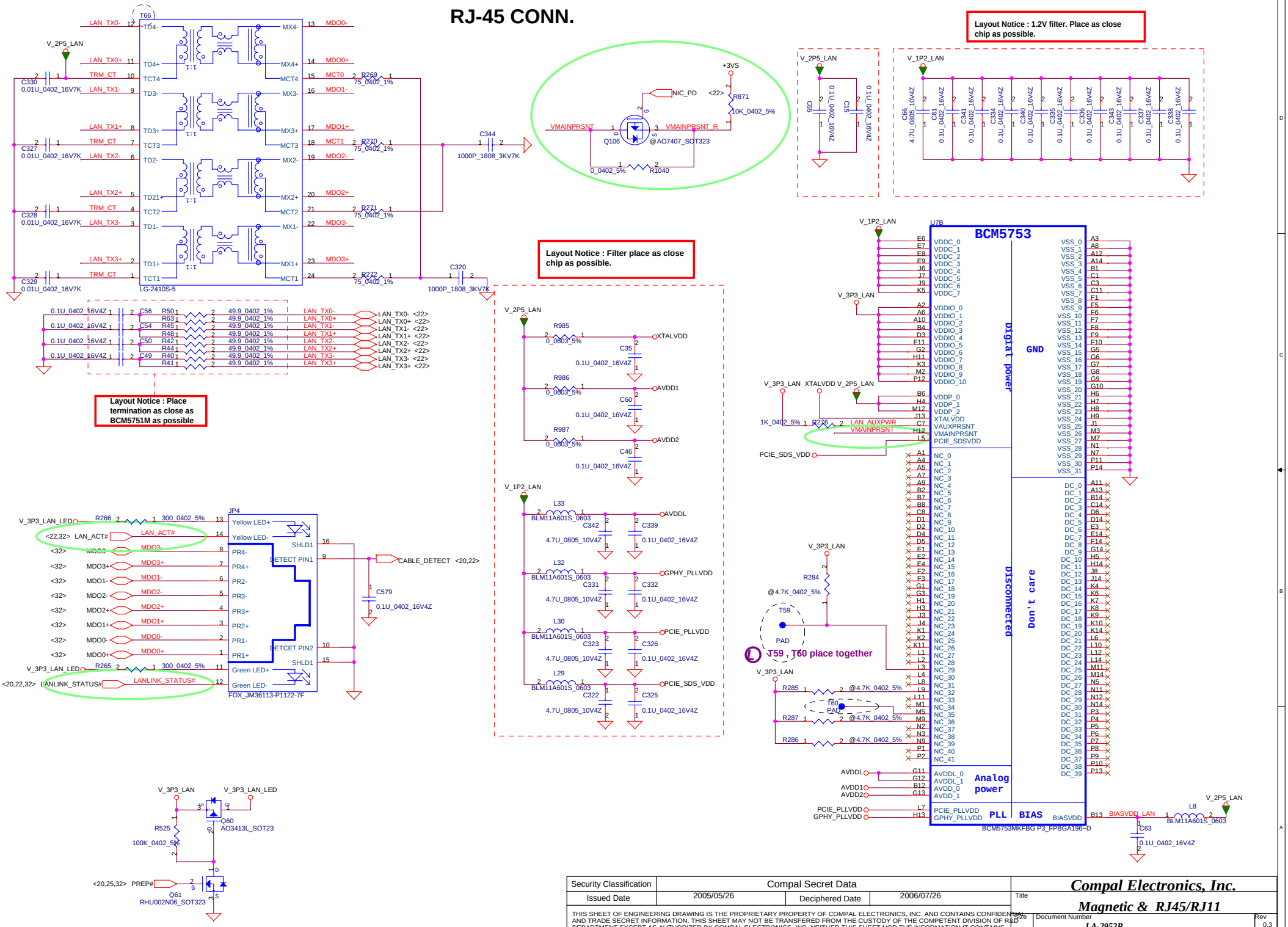
Compal Electronics, Inc.

Title: **BCM5751M**

Size: | Document Number: **LA-2952P** | Rev: 0.3

Date: Wednesday, October 26, 2005 | Sheet 22 of 46

RJ-45 CONN.



Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

Compal Electronics, Inc.

Title: **Magnetic & RJ45/RJ11**

Size	Document Number	Rev
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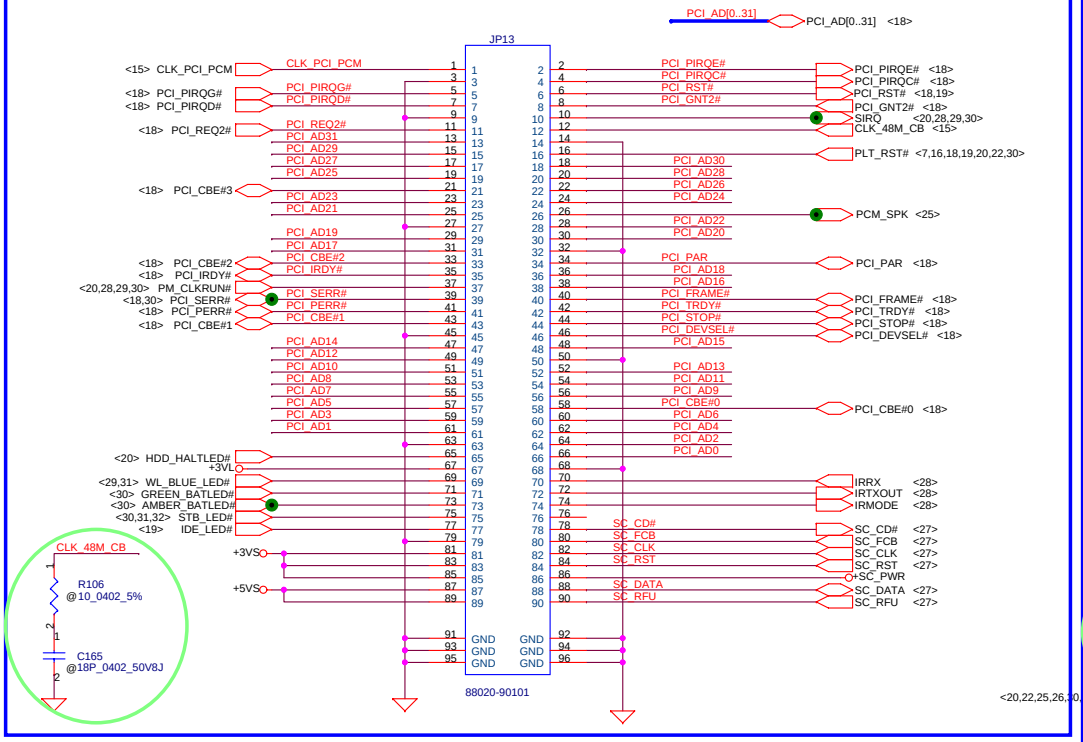
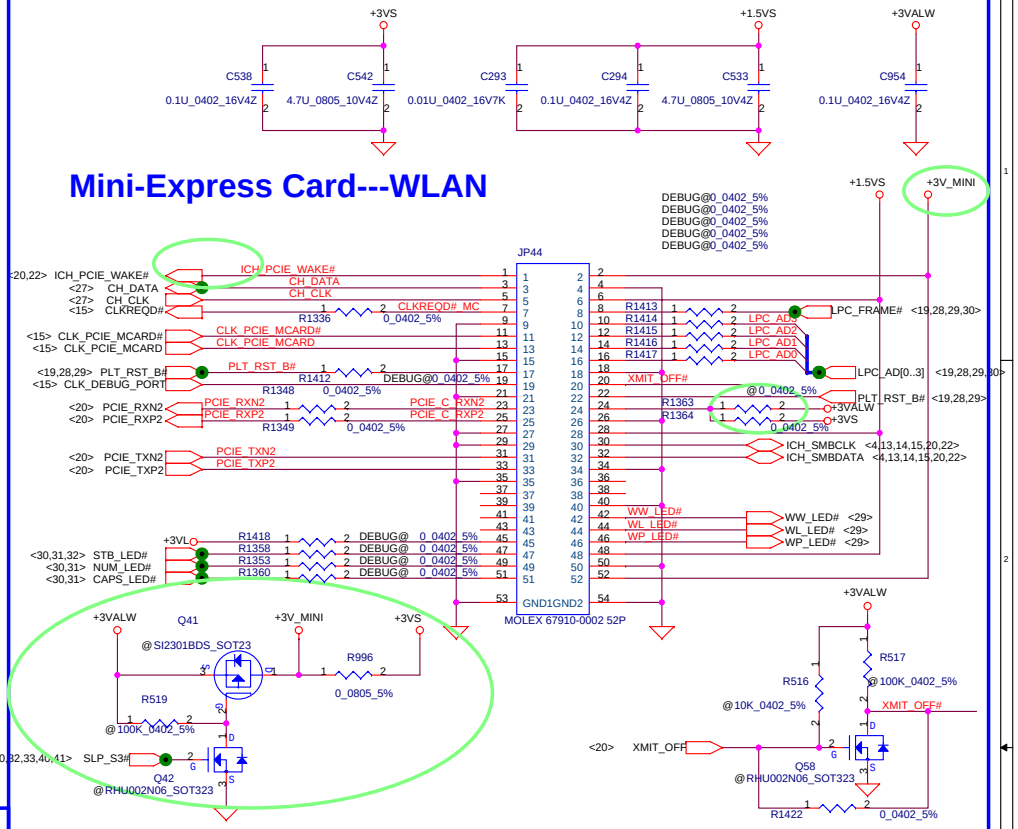
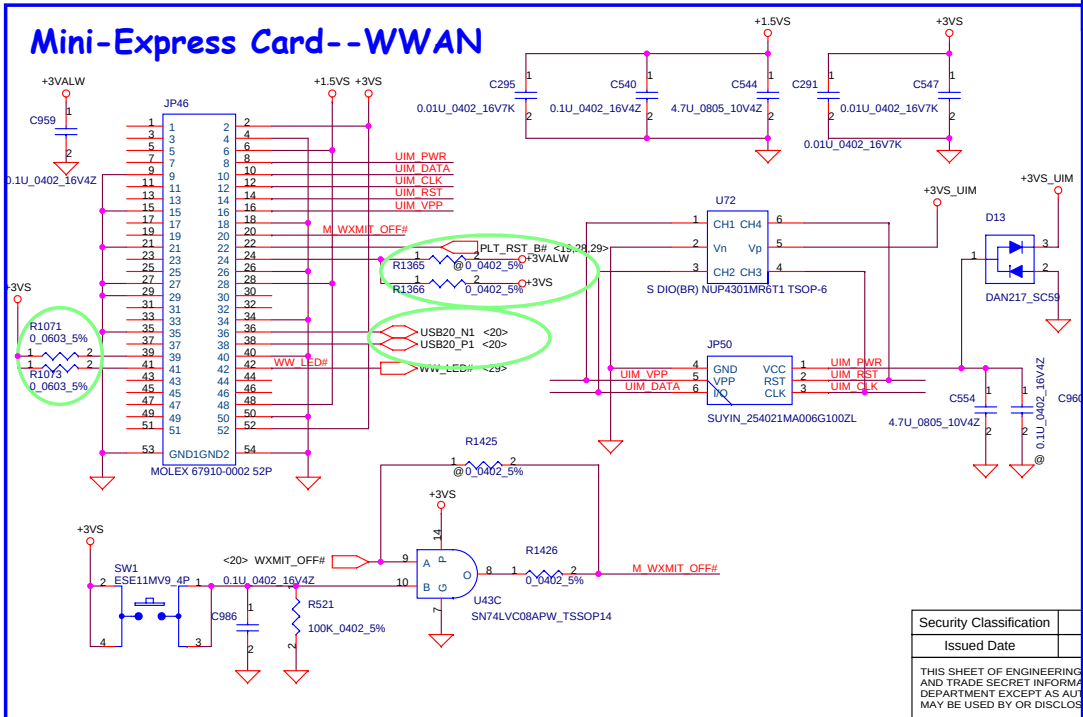
B/B connector with PCI / LED / FIR / SC interface



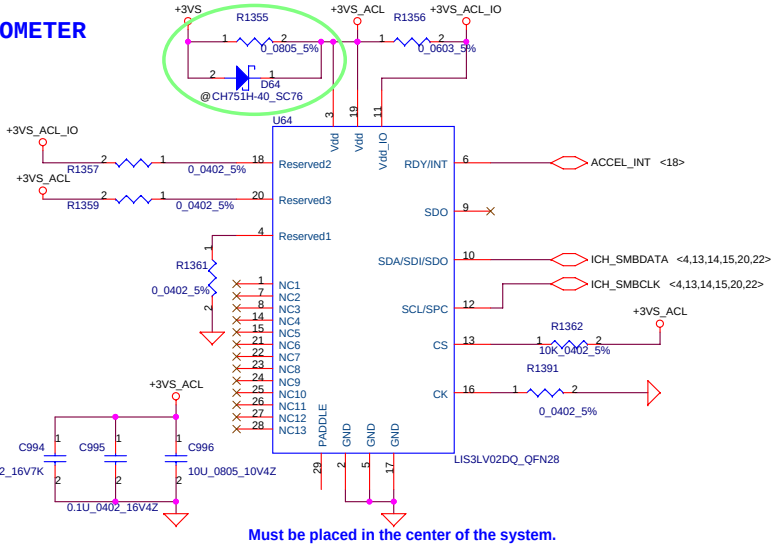
Mini-Express Card---WLAN



Mini-Express Card--WWAN



ACCELEROMETER



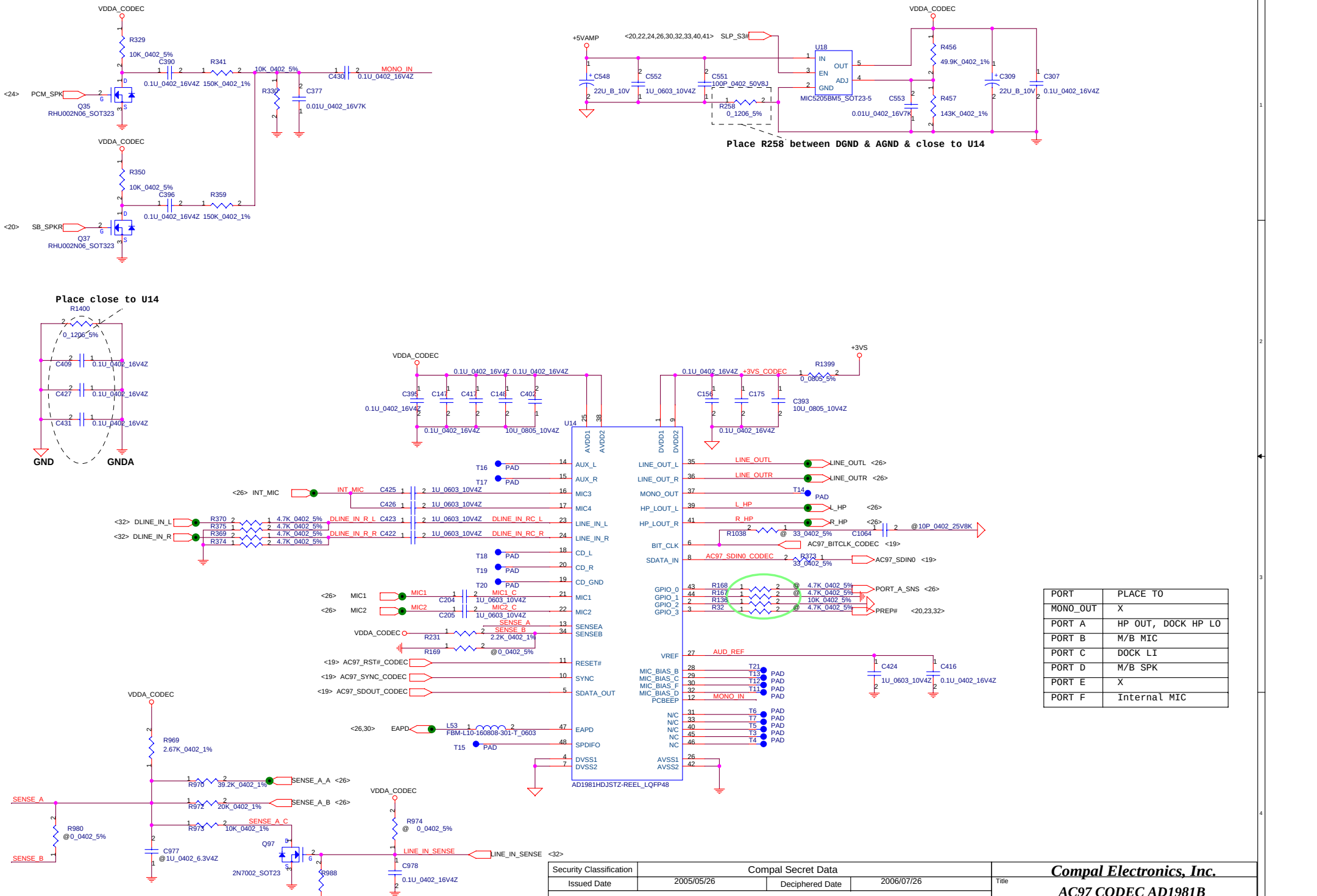
Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

Compal Electronics, Inc.

Title: **Mini-Card/Mini-PCI/Accelerometer**

Size	Document Number	Rev
	LA-2952P	0.3

Date: Wednesday, October 26, 2005 | Sheet 24 of 46



Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

Compal Electronics, Inc.

Title: **AC97 CODEC AD1981B**

Size: | Document Number: **LA-2952P** | Rev: 0.3

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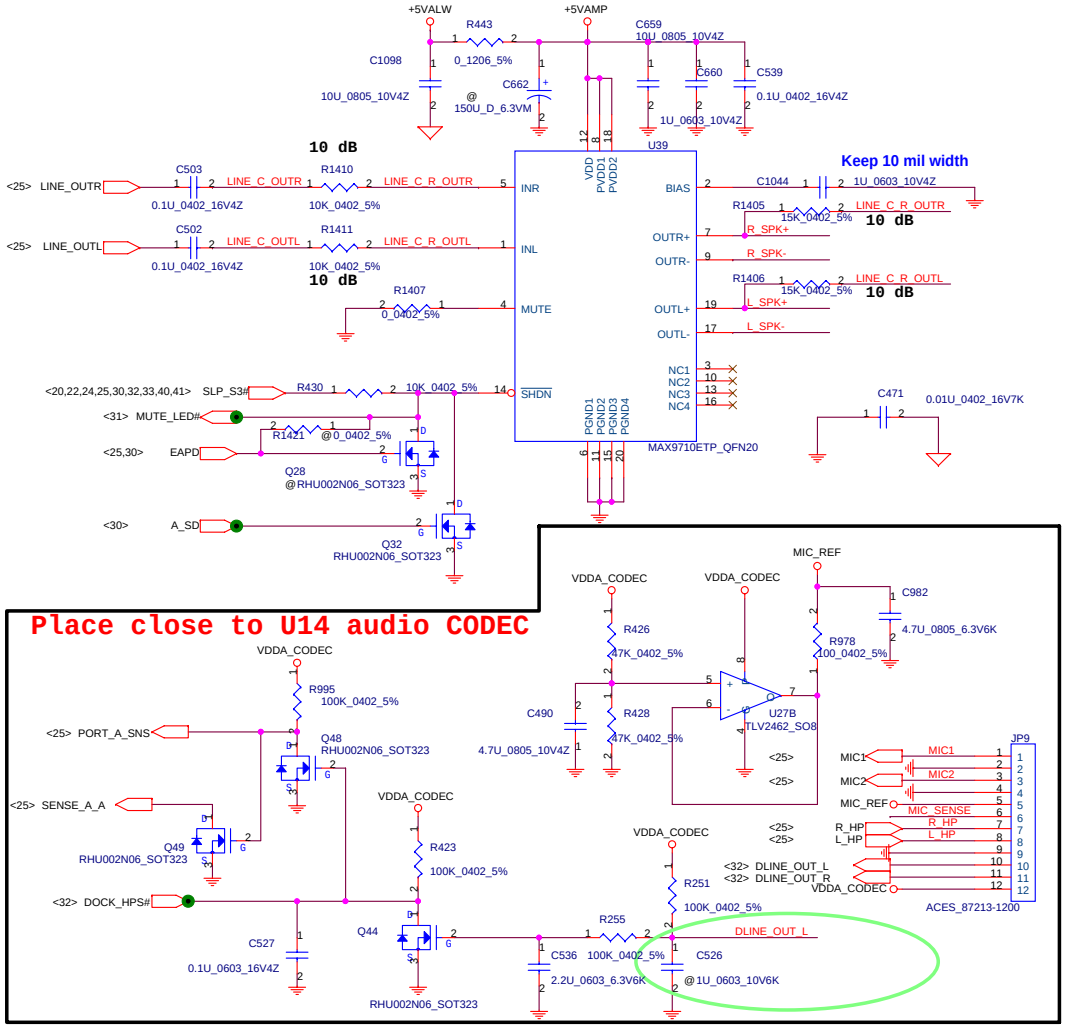
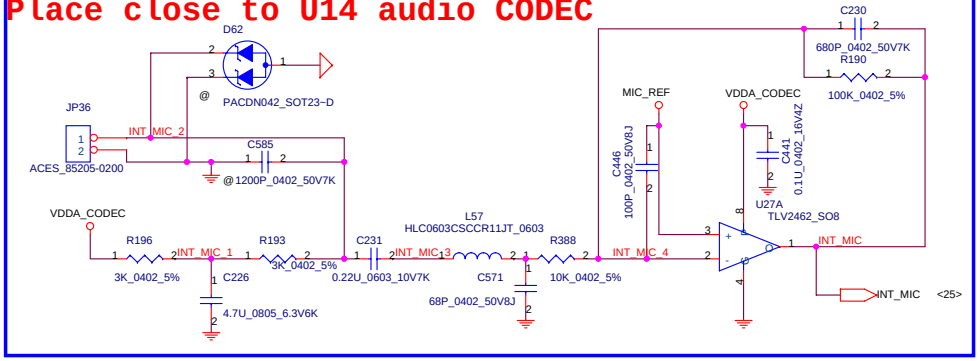
AMP. FOR INTERNAL SPEAKER



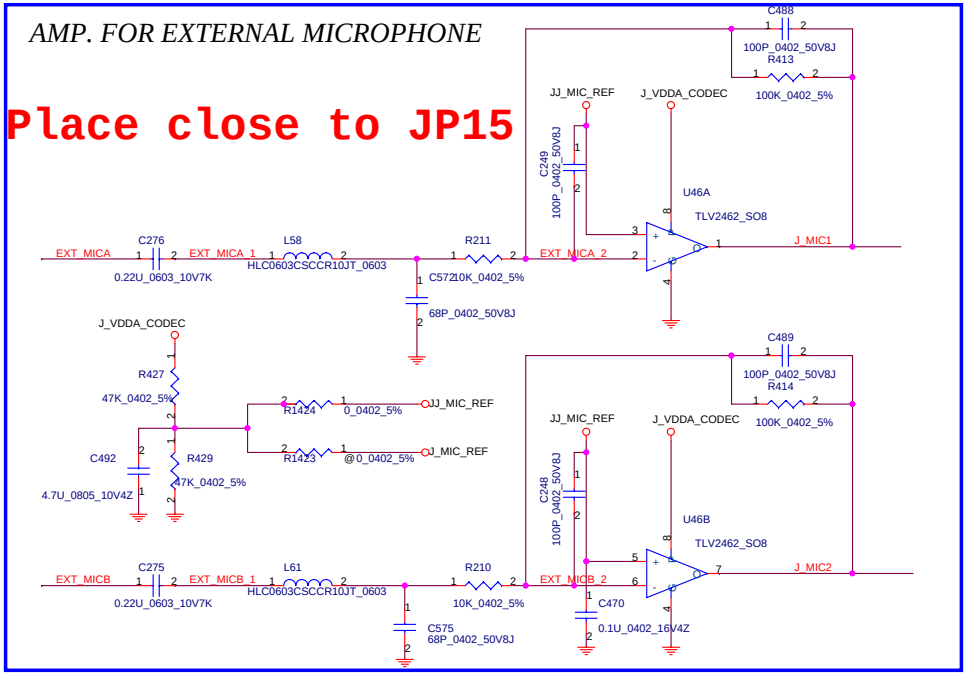
AMP. FOR INTERNAL MICROPHONE

Place close to U14 audio CODEC

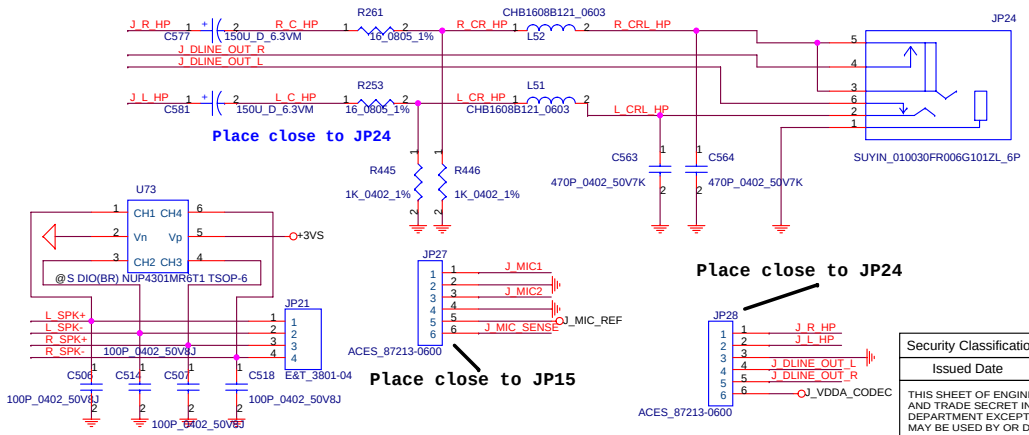


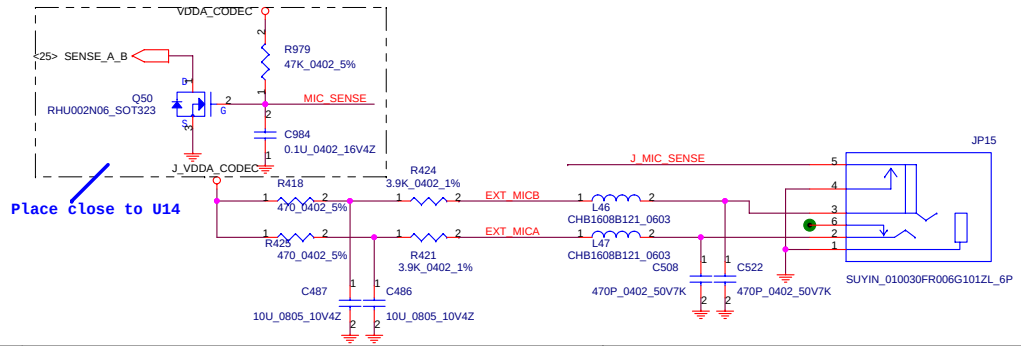
AMP. FOR EXTERNAL MICROPHONE

Place close to JP15



Place close to U14 audio CODEC





Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

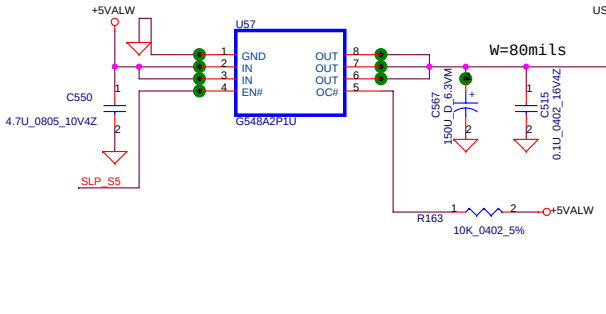
Compal Electronics, Inc.

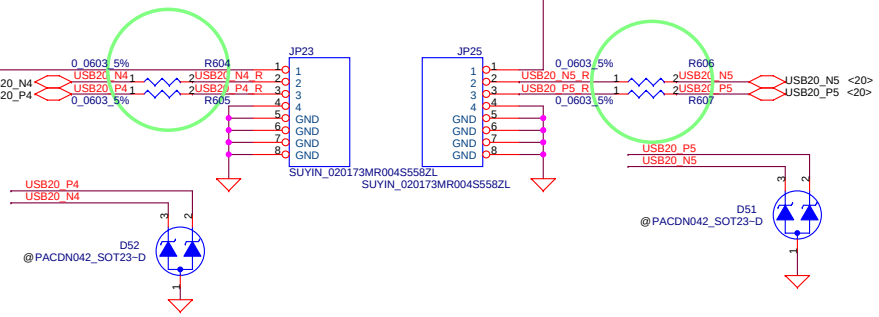
Title: **AMP & Audio Jack**

Size	Document Number	Rev
	LA-2952P	0.3

Date: Wednesday, October 26, 2005 Sheet 26 of 46

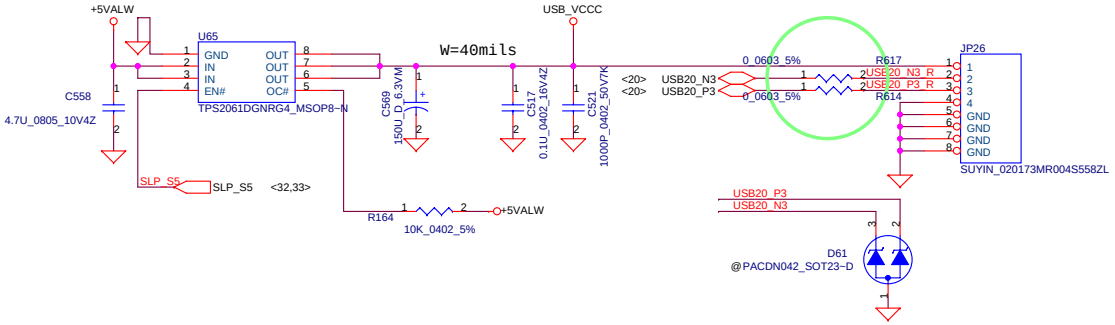
Left side USB CONNECTOR 0



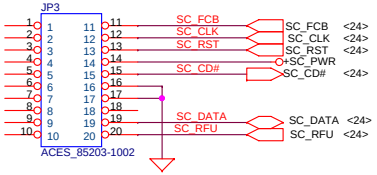


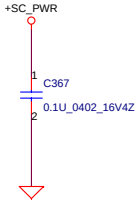
Left side USB CONNECTOR 1

Right side USB CONNECTOR 0

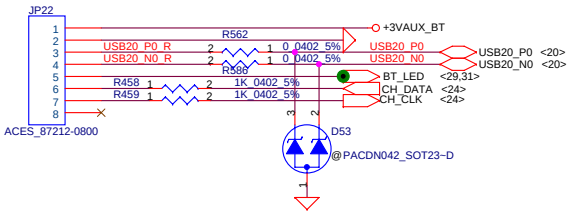


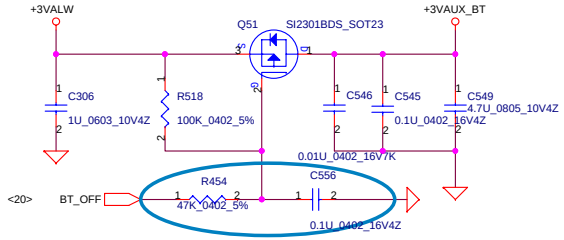
SMART Card connector





BT Connector





Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

Compal Electronics, Inc.	
Title	USB & BT Connector
Size	Document Number: LA-2952P
Rev	0.3
Date:	Wednesday, October 26, 2005
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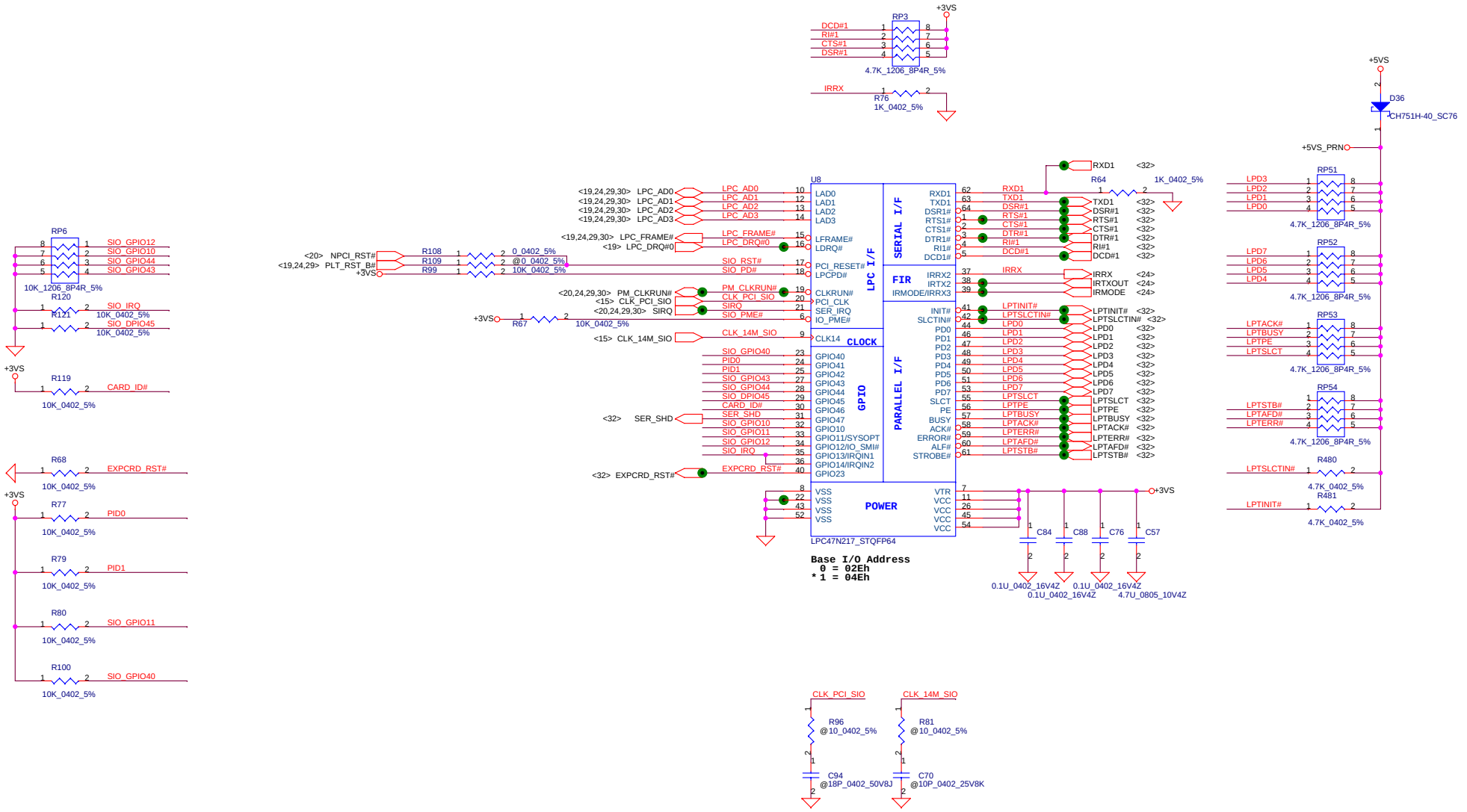


Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

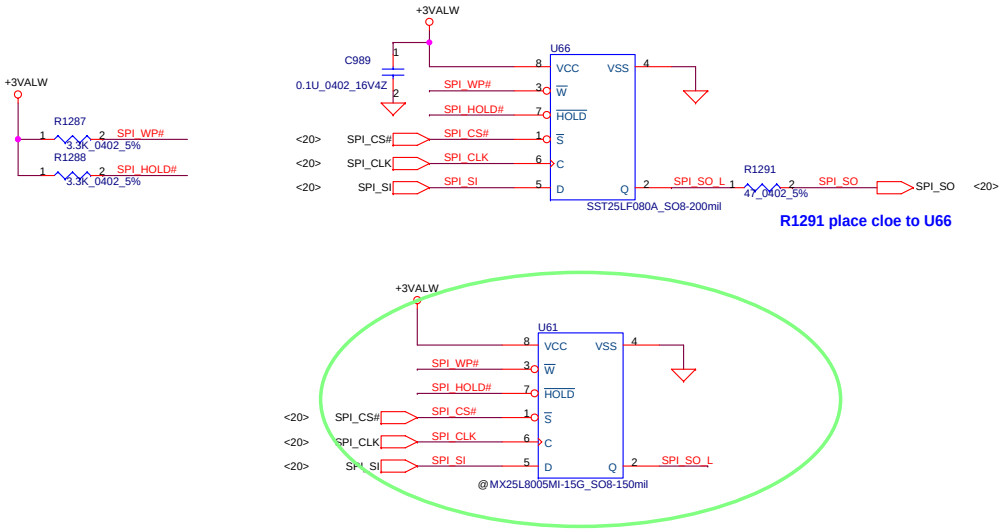
Compal Electronics, Inc.

Title: **SUPER I/O LPC47N217**

Size: | Document Number: **LA-2952P** | Rev: 0.3

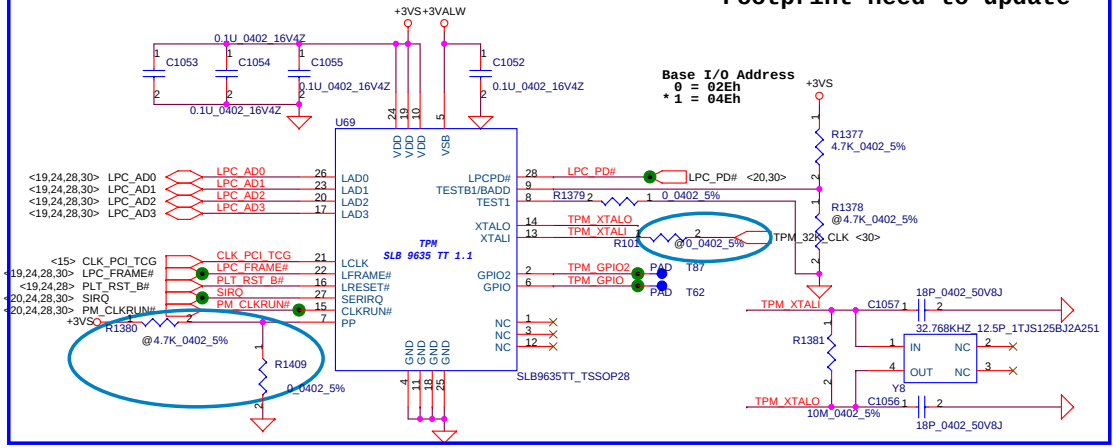
Date: Wednesday, October 26, 2005 | Sheet 28 of 46

BIOS ROM

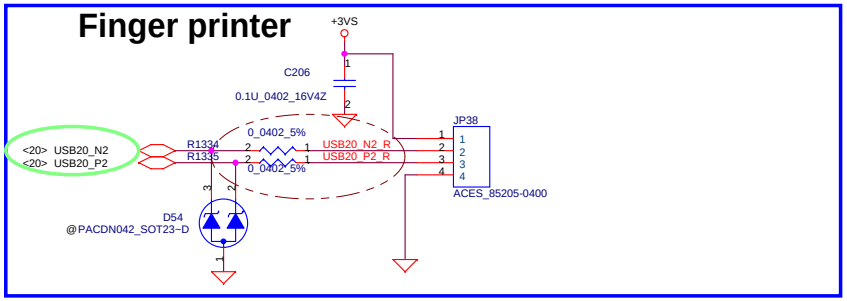


TPM1.2

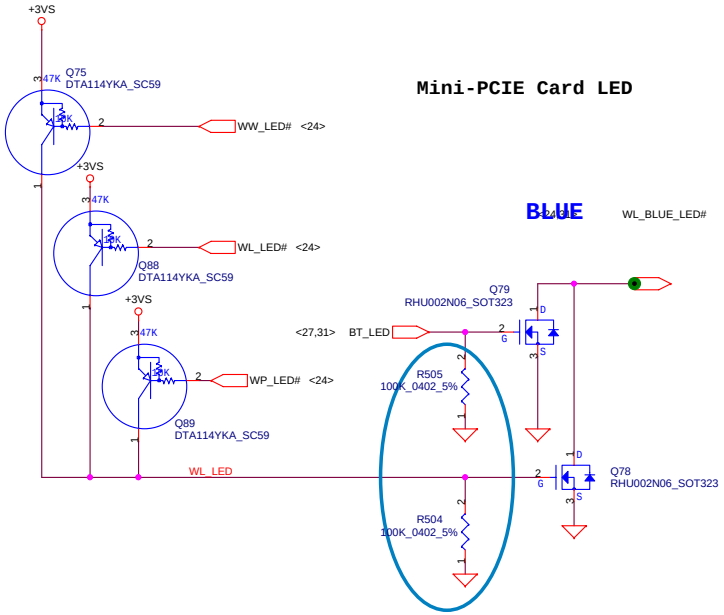
Footprint need to update



Finger printer



Mini-PCIE Card LED



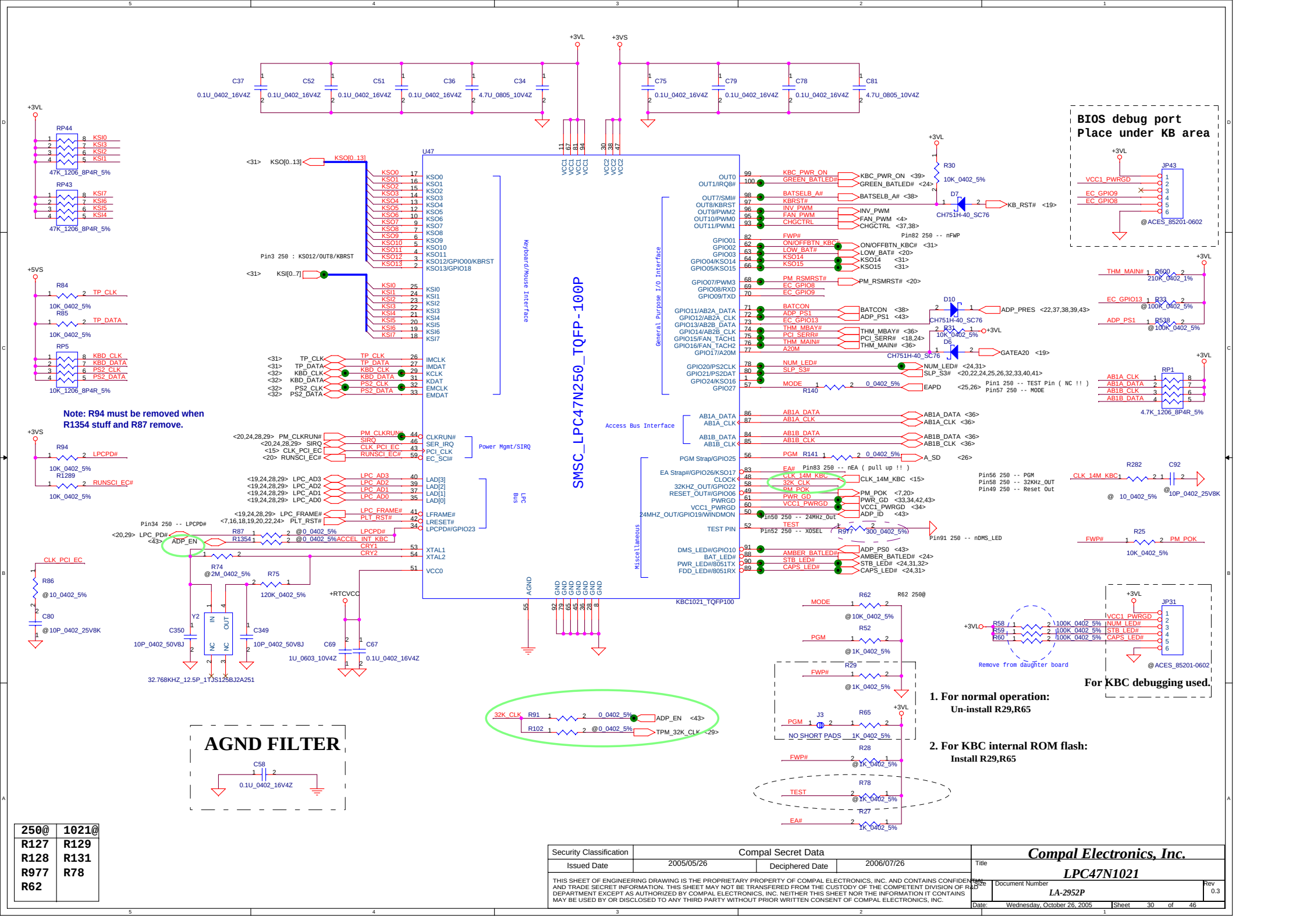
Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

Compal Electronics, Inc.

Title: **TCG/BIOS ROM/PS2/LED/SW**

Size	Document Number	Rev
	LA-2952P	0.3

Date: Wednesday, October 26, 2005 Sheet 29 of 46



Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

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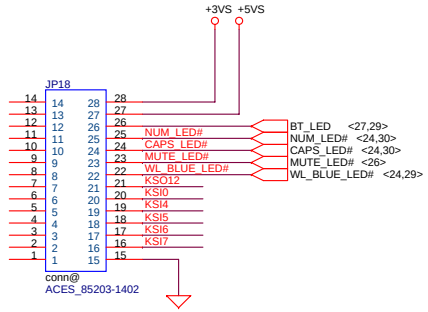
Compal Electronics, Inc.

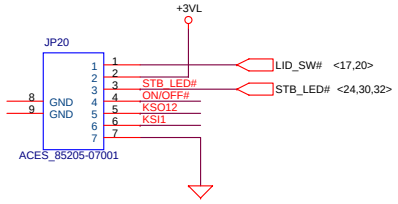
Title: **LPC47N1021**

Size: Document Number: **LA-2952P** Rev: 0.3

Date: Wednesday, October 26, 2005 Sheet 30 of 46

SWITCH BOARD.

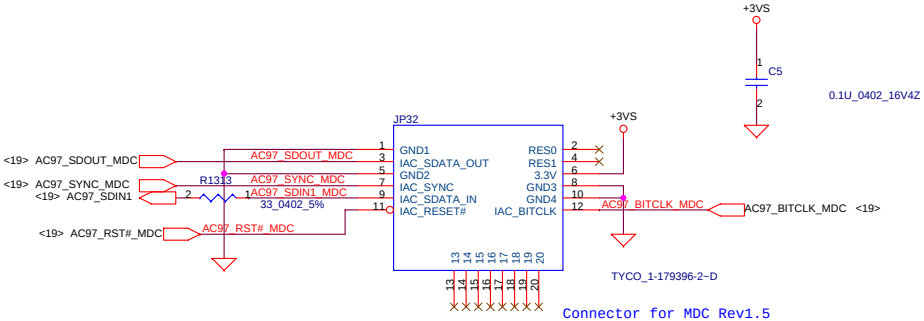




On/off ,information button

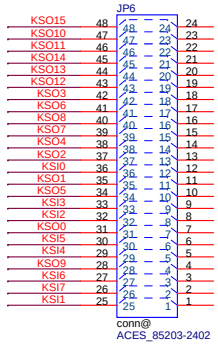
WL,Vol up,Vol down,Mute,Present button

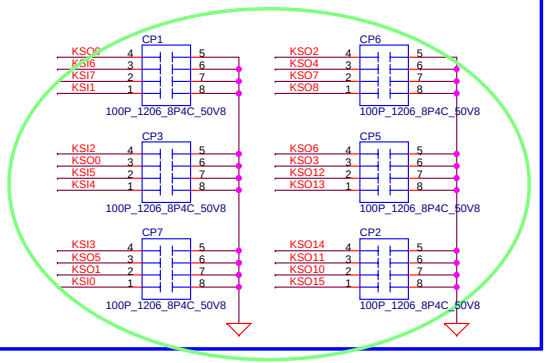
MDC 1.5 Conn.



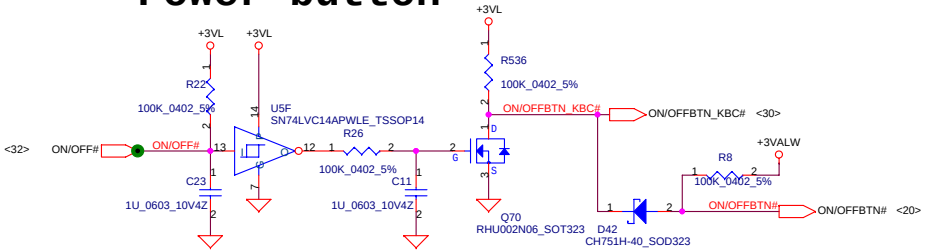
Connector for MDC Rev1.5

INT_KBD CONN.

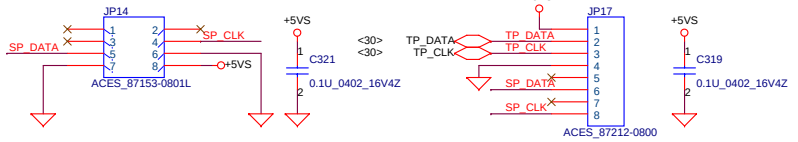




Power button



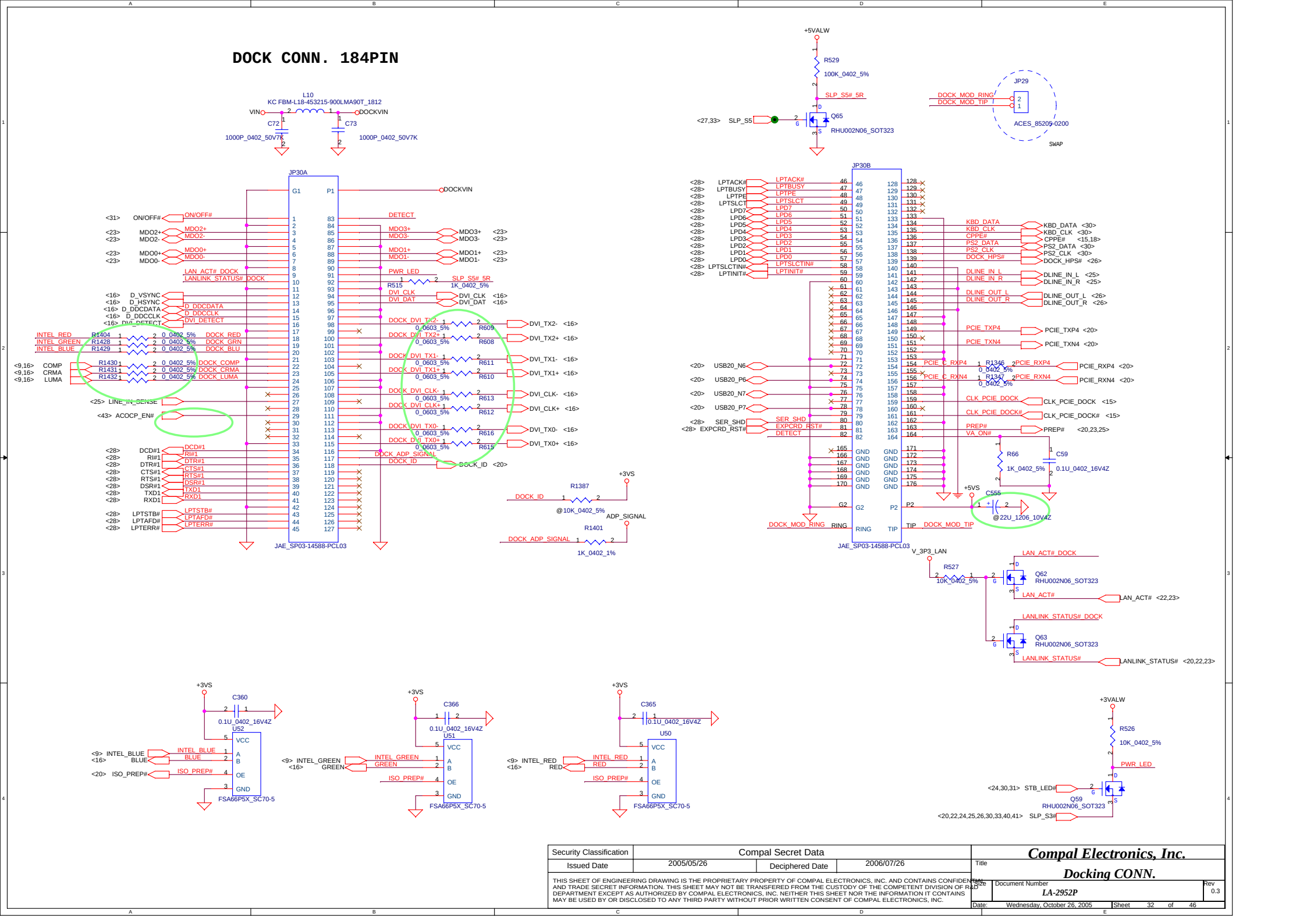
TrackPoint CONN. T/P BOARD.



Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

Compal Electronics, Inc.			
Title: MDC/KBD/ON_OFF/LID			
Size	Document Number: LA-2952P		Rev: 0.3
Date: Wednesday, October 26, 2005		Sheet 31 of 46	

DOCK CONN. 184PIN



Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

Compal Electronics, Inc.

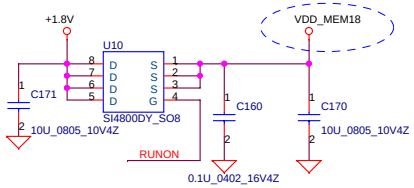
Title: **Docking CONN.**

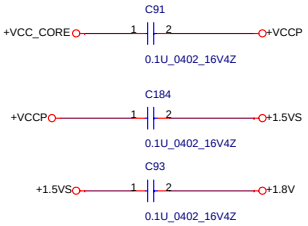
Size: Document Number: **LA-2952P** Rev: 0.3

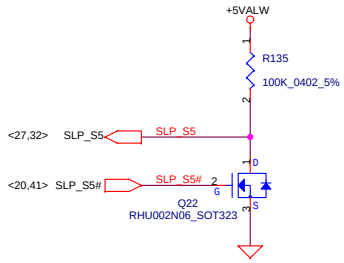
Date: Wednesday, October 26, 2005 Sheet 32 of 46

+1.8V to +1.8VS Transfer

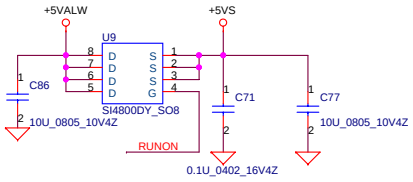
VRAM



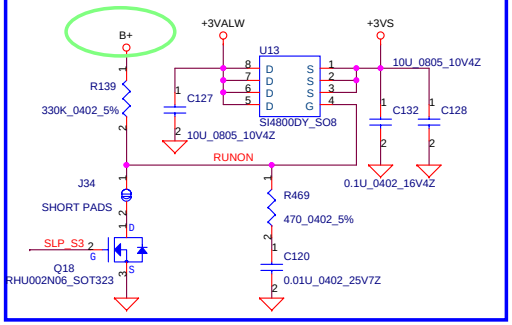


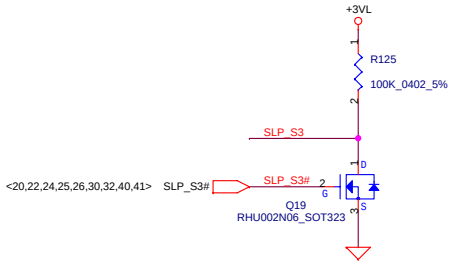


+5VALW to +5VS Transfer

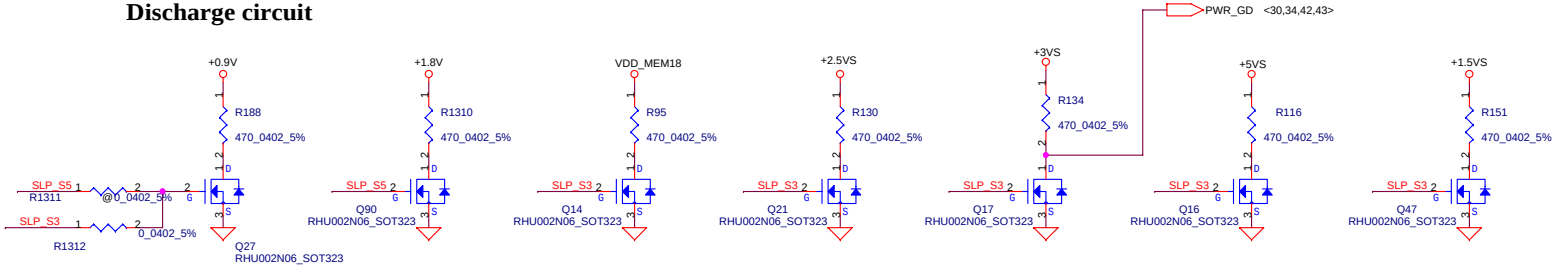


+3VALW to +3VS Transfer





Discharge circuit



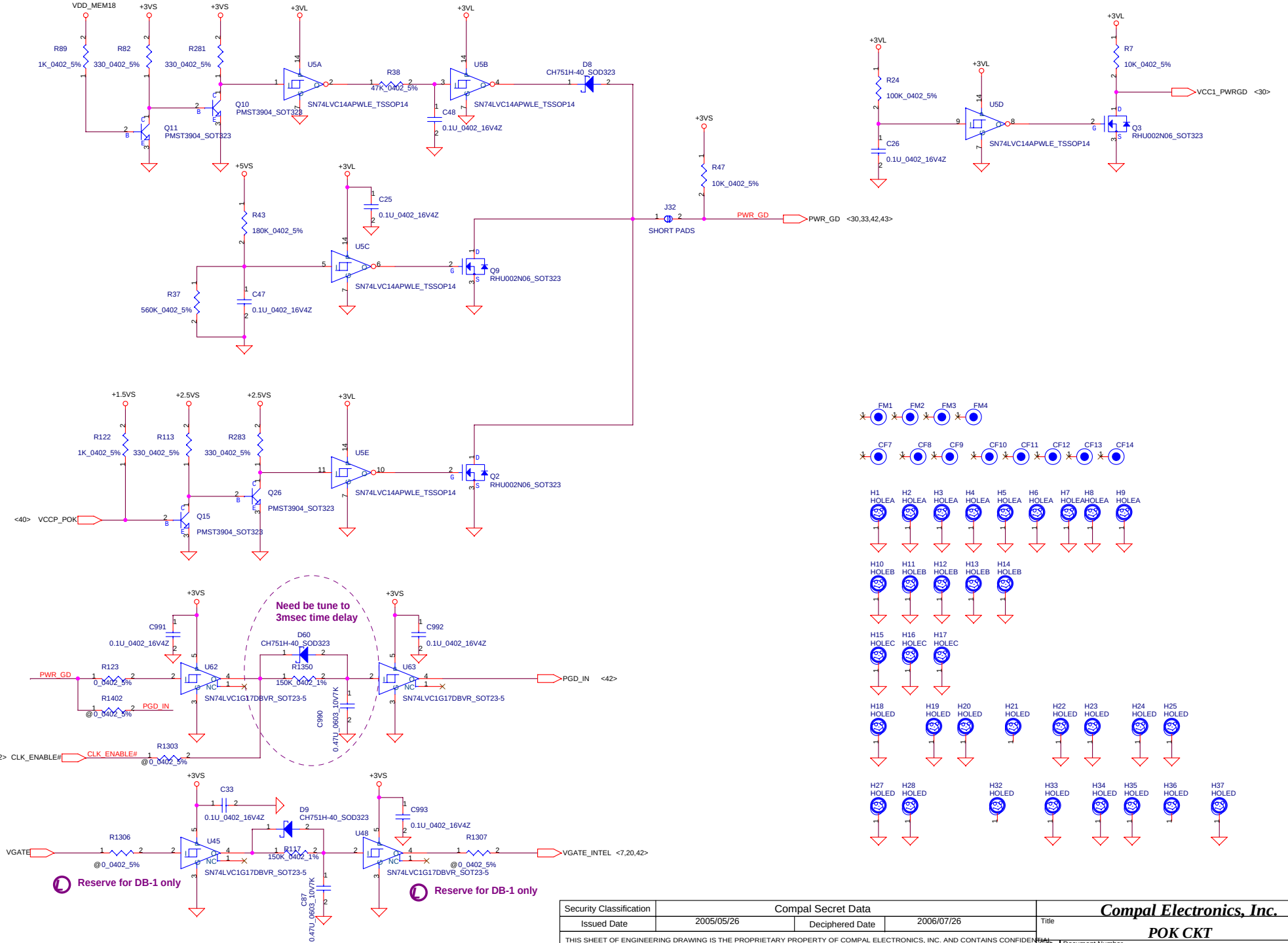
Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

Compal Electronics, Inc.

Title: **DC/DC Circuits**

Size: | Document Number: **LA-2952P** | Rev: 0.3

Date: Wednesday, October 26, 2005 | Sheet 33 of 46



Security Classification	Compal Secret Data		
Issued Date	2005/05/26	Deciphered Date	2006/07/26

Compal Electronics, Inc.

Title: **POK CKT**

Size: D | Document Number: **LA-2952P** | Rev: 0.3

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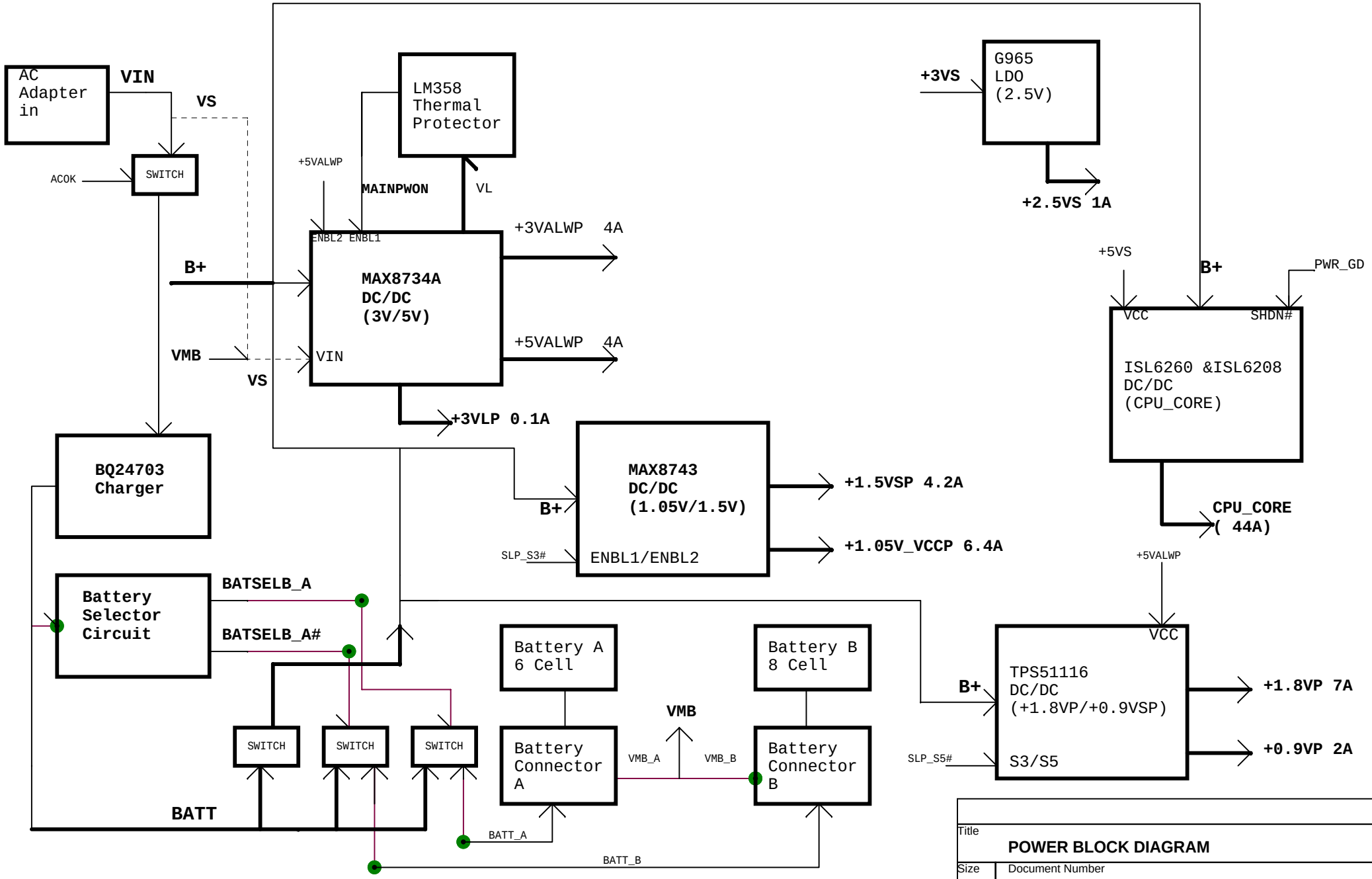
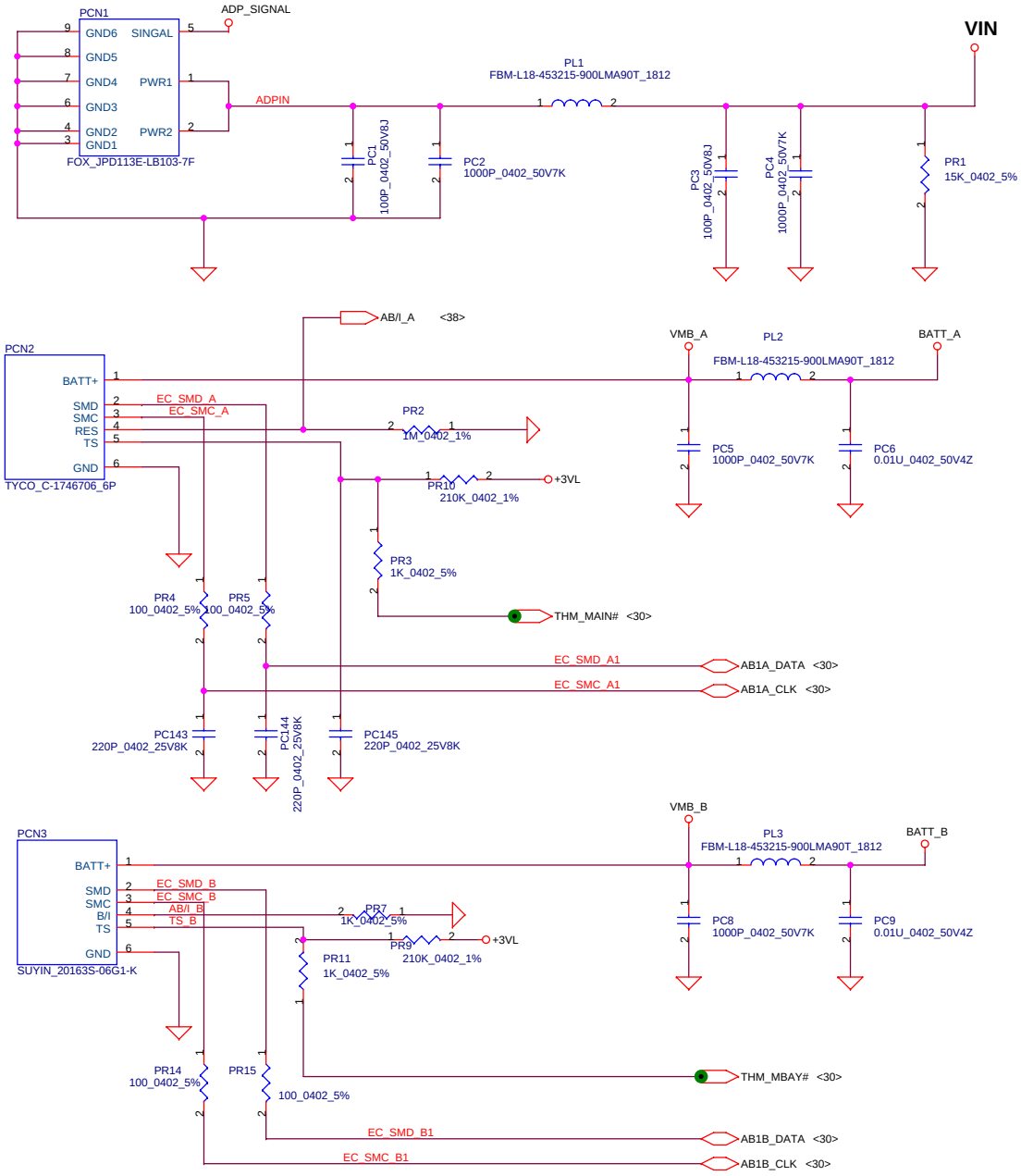


Title	POWER BLOCK DIAGRAM	
Size	Document Number	Rev
Date: Wednesday, October 26, 2005	Sheet 35 of 46	



Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **BATTERY CONN**

Size	Document Number	Rev
Custom	LA-2821	

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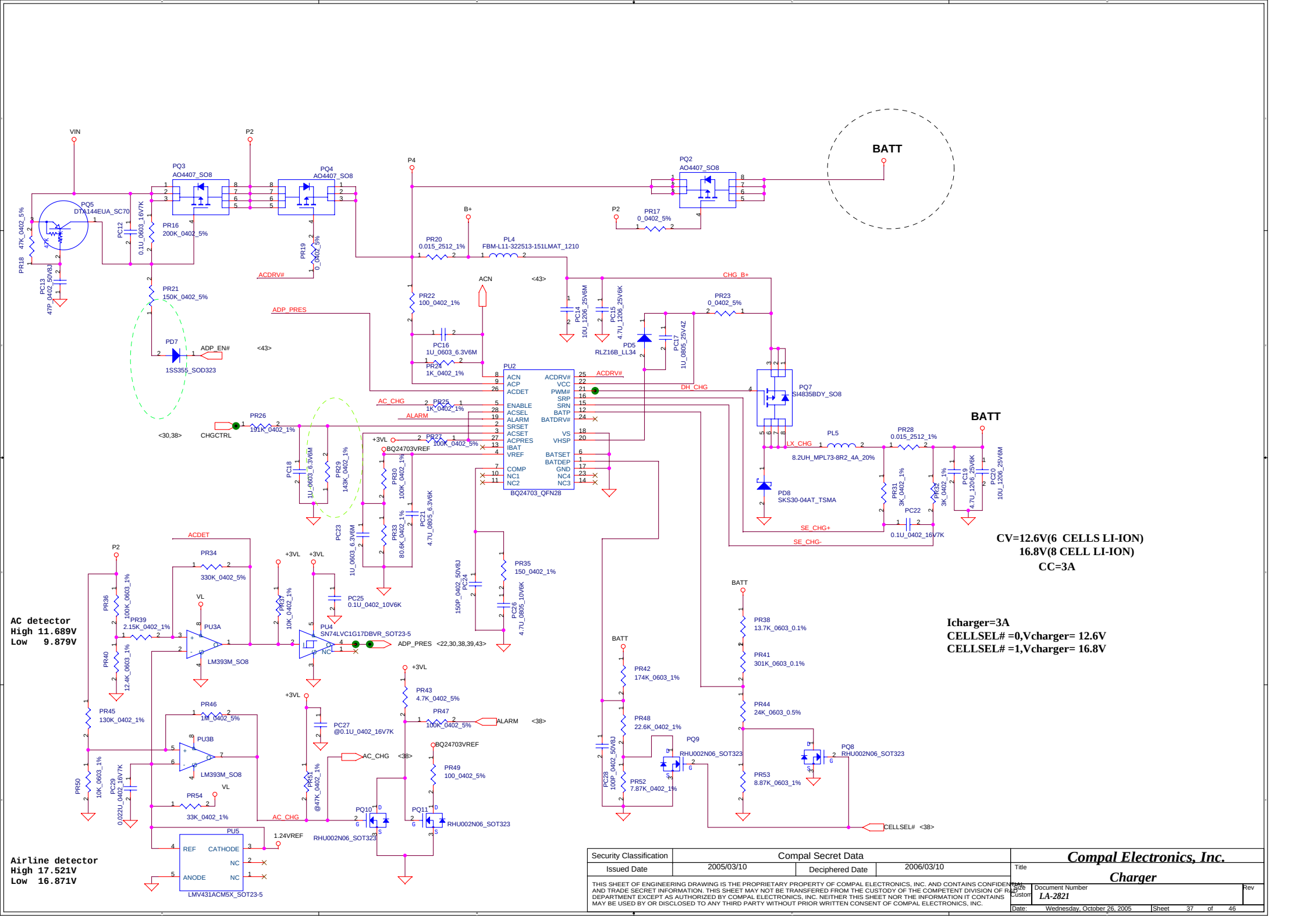


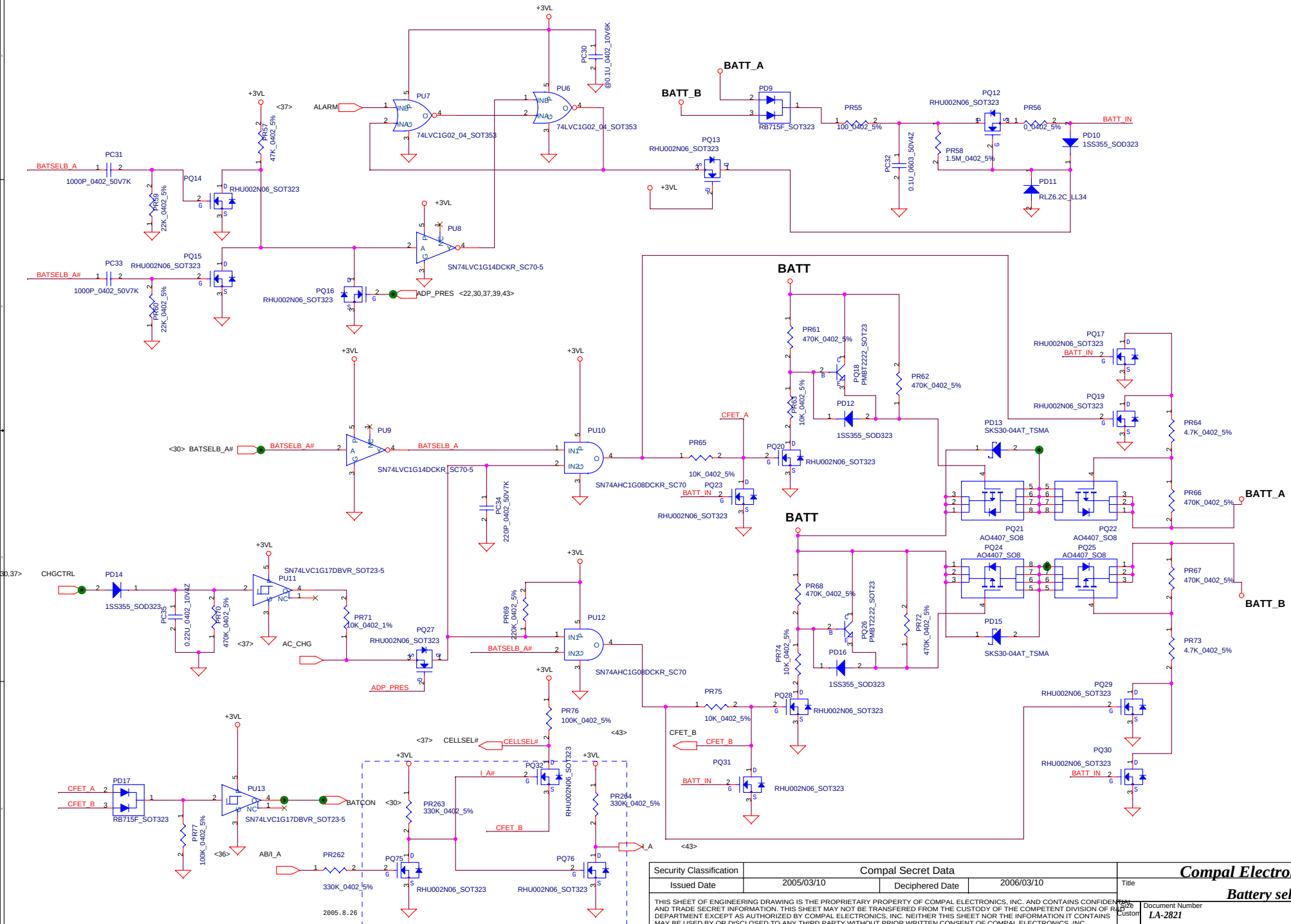
Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **Charger**

Size	Document Number	Rev
Custom	LA-2821	

Date: Wednesday, October 26, 2005 Sheet 37 of 46



Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **Battery selector**

Size	Document Number	Rev
Custom	LA-2821	

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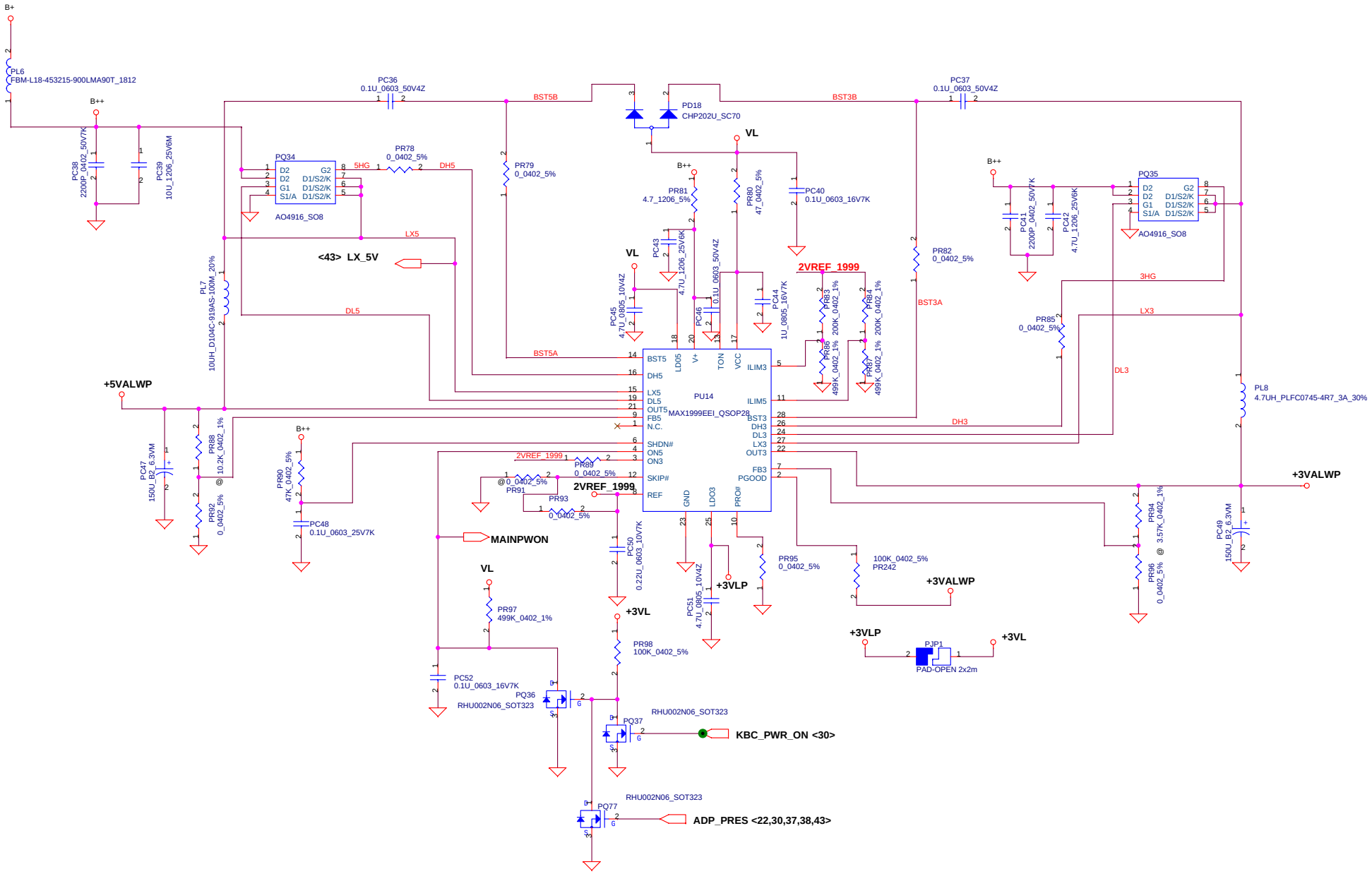
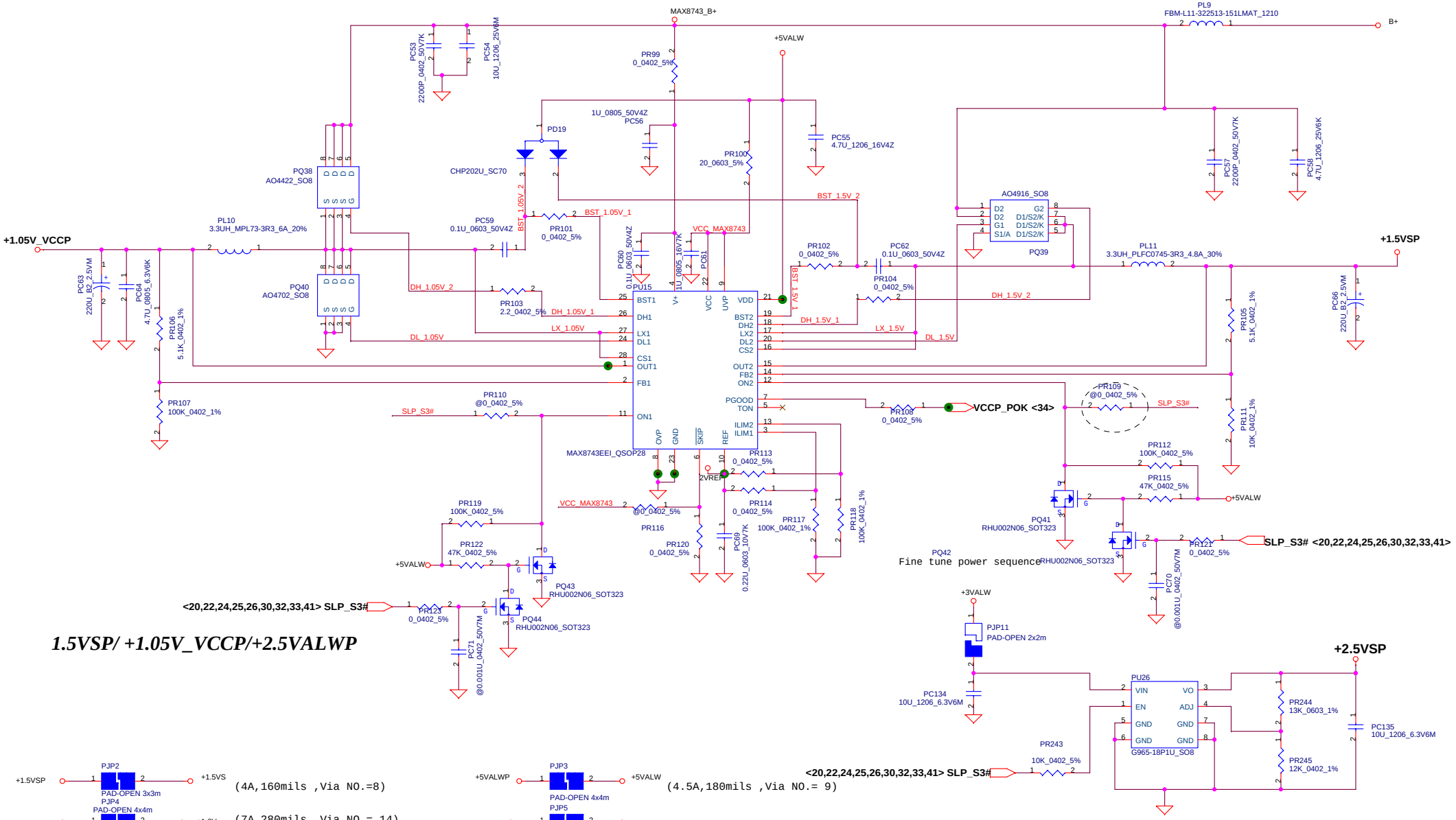
+3.3V/+5V



Security Classification	Compal Secret Data		
Issued Date	2005/03/01	Deciphered Date	2006/03/01

Title	3.3V / 5V	
Size: B	Document Number: LA-2541	Rev: 0.3
Date: Wednesday, October 26, 2005	Sheet 39 of 46	



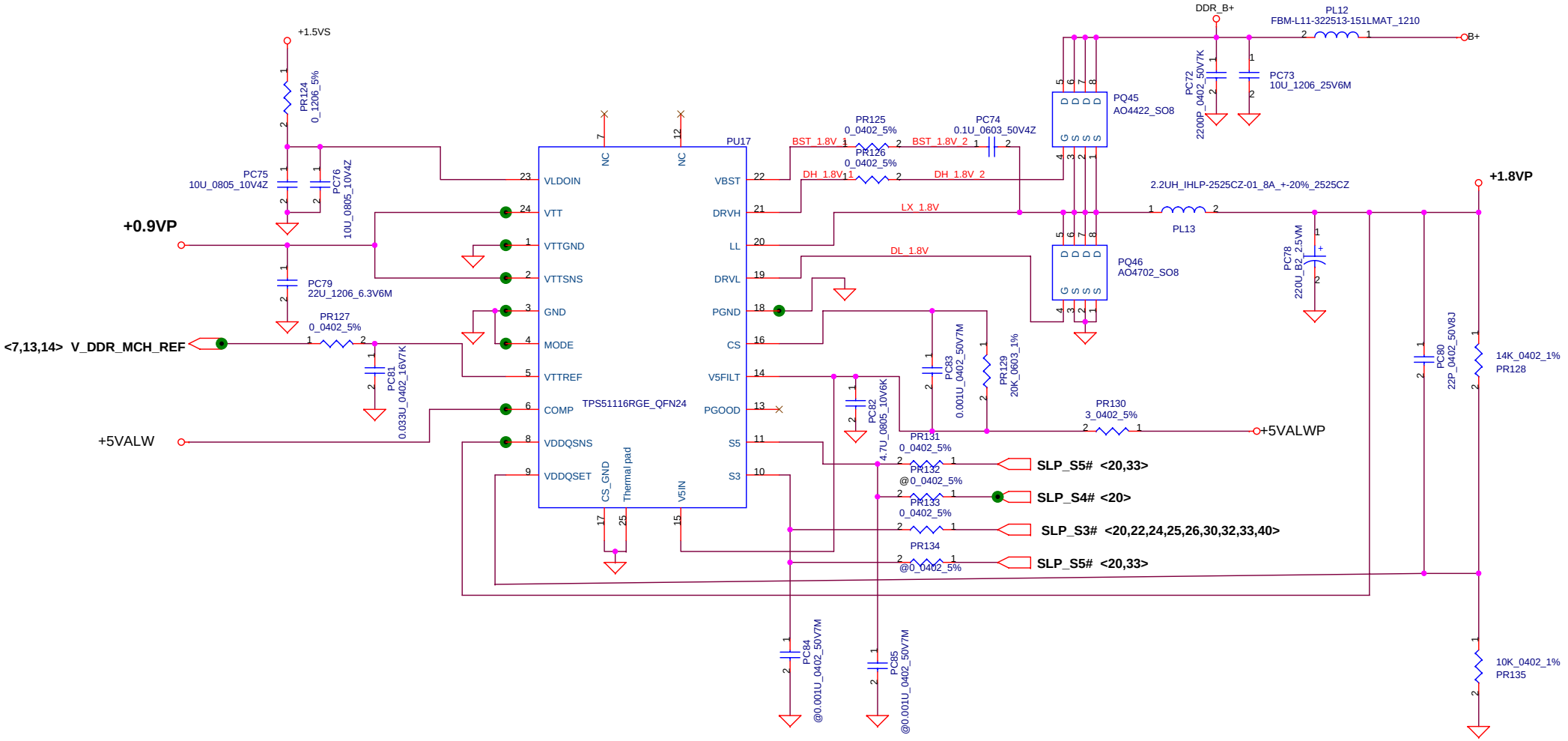
Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: 2.5VALW/1.5VS/1.05VCCP

Size	Document Number	Rev
Custom	LA-2821	

Date: Wednesday, October 26, 2005 Sheet 40 of 46



Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **1.8V/0.9VS**

Size	Document Number	Rev
B	LA-2821	

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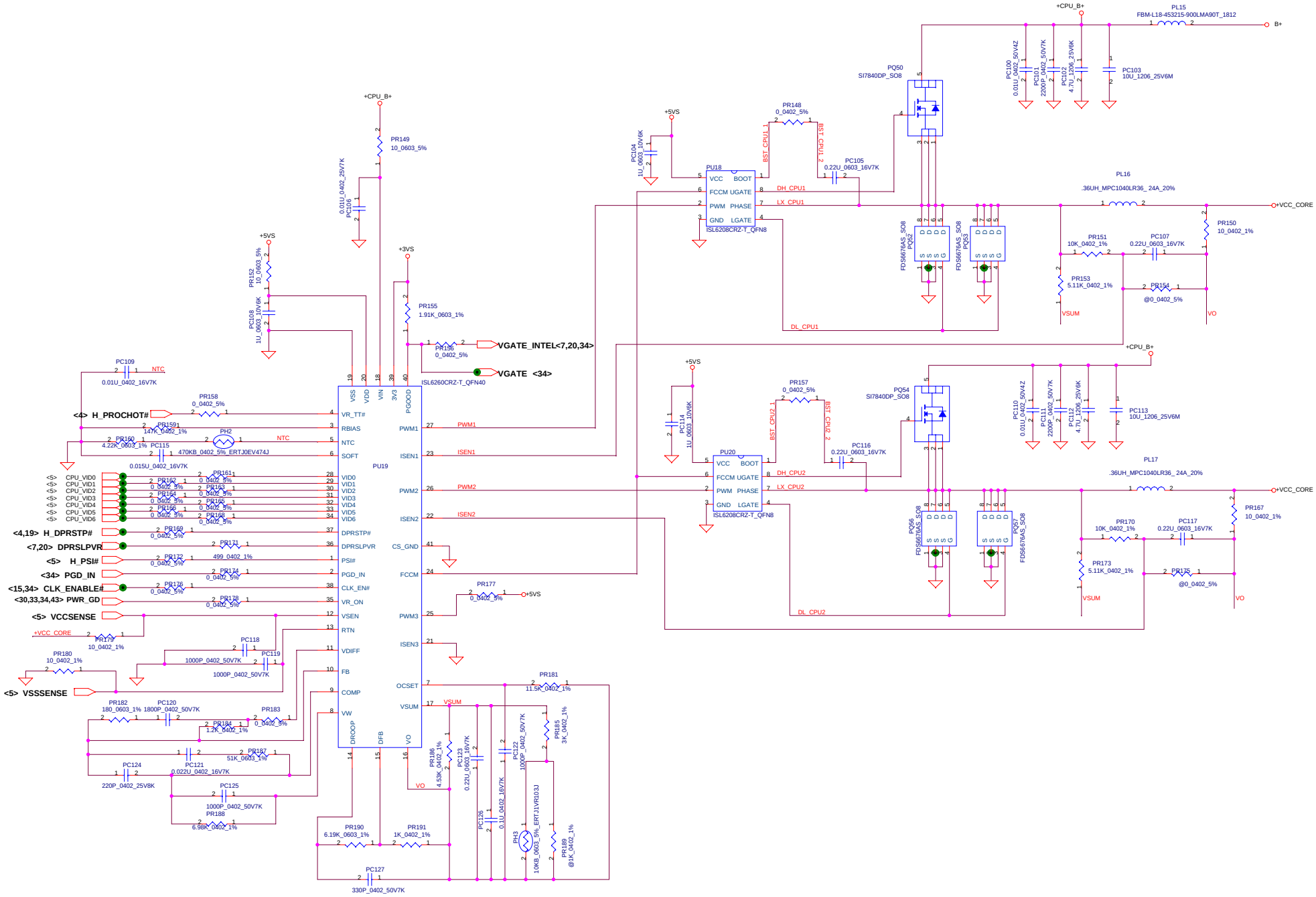

Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **CPU_CORE**

Size	Document Number	Rev
C	LA-2821	

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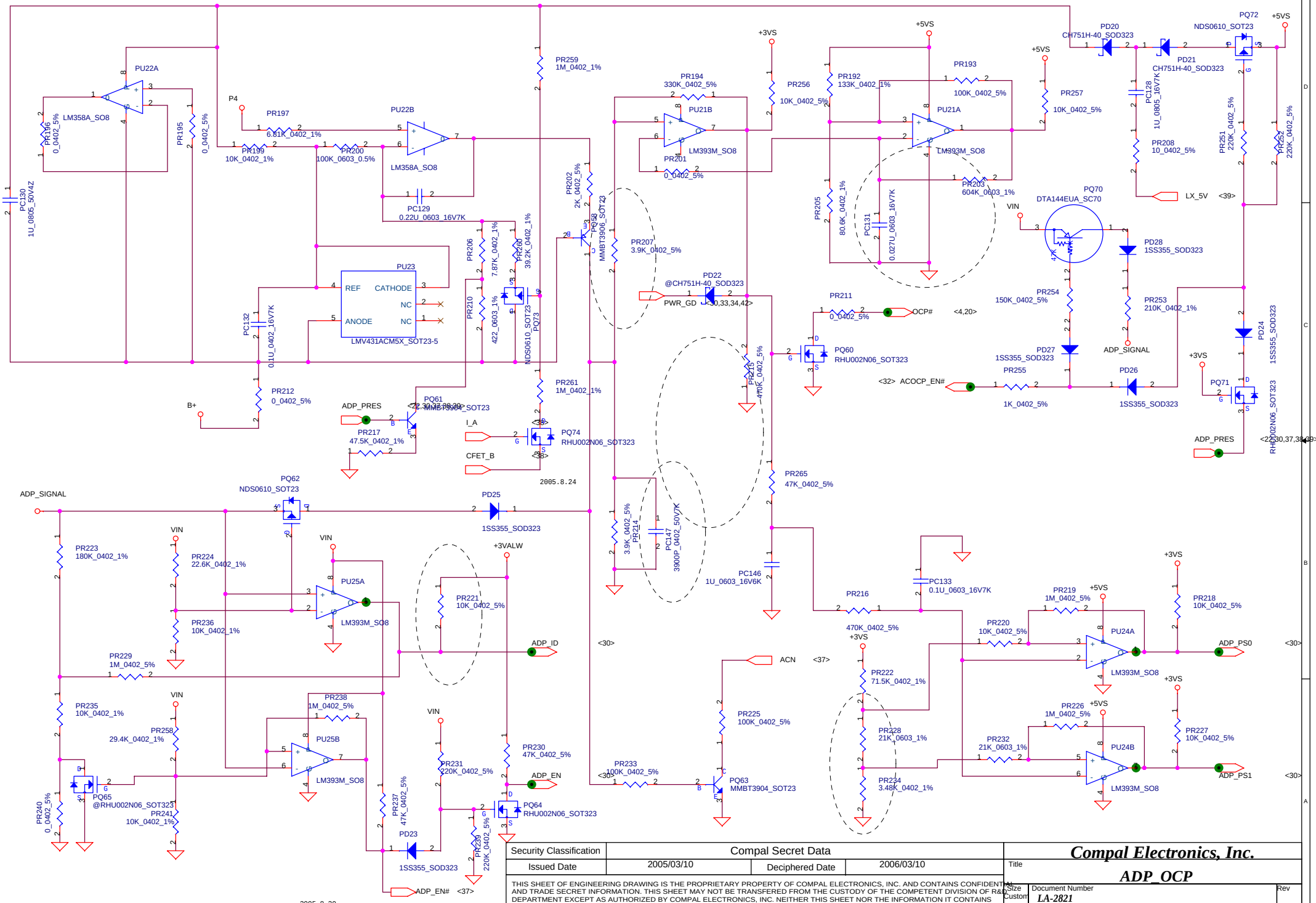

Security Classification	Compal Secret Data		
Issued Date	2005/03/10	Deciphered Date	2006/03/10

Compal Electronics, Inc.

Title: **ADP_OCP**

Size	Document Number	Rev
Custom	LA-2821	

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EE PIR list

06/01/2005 schematics review start :

06/02/2005

Page38 : Add R58,R59,R60 ,those are removed from daughter board

Page39 : JP18 pin3 change from ground to BT_LED

Page37 : Remove JP16 & change debug port interface to JP44

Page27 : ICH7M pin R7 change to +3VS

Page32 : JP44 PLT_RST# change to PLT_RST_B# to reduce the loading

Page33 : Update audio amp to MAX9710

06/03/2005

Page10 : Add R260 to reduce one 330U cap C666

Page25 : 1. R27 change to +3VS
2..Add R1035 for H_DPSLP#

Page26 : 1.Add T80 for GPIO25
2. GPIO21 change net name to VGARST#
3. Add T88 for GPIO23
4. Add T89 for GPIO26
5. GPIO30 change net name to USB_OC#6
6. GPIO31 change net name to USB_OC#7
7. Add R1036/7 for RESET option
8. Remove the connection of USB_OC#3/4/5

Page24 : Add ALS_EN on JP35 pin24 for light sensor

Page32 : 1.JP13 change to 90 pins connector
2.Add U72 for ESD protection

06/04/2005

Page10 : A. U71 change to U43D (the fourth gate in U43)
B. Add +3VS_TVBG R/C filters & voltage follower D12,D21,R127,R520

Page34 : audio change-- add R1419 ,R431,R434,R435 for BIASA/B/C

Page35 : Add JP3 for Smart card FFC connector

Page18 : 1.R1365 CHANGE TO 2K_0402_1%
2. R1366 change to 562_0402_1%
3. R1367 change to 1.47K_0402_1%

Page31 : JP4 update to RJ45 connector

Page15 :Add the connection for UMA VGA clock , & SRC0/2 SWAP
1.Add R1148/R1149 , R1129/R1132 , R1118/R1121
2.Add R1242/R1248,R1253/R1272

Page09 : Change 0 ohm resistors before filters ,
and delete the other group of filtes at page 19

Page16 : add R671~R678 ,R530,R531 for DVI

Page19 : Swap I2C bus for LVDS/Thermal sensor

06/07/2005

Page47 : PQ34 pin5/6/7 change netname to LX_5V

Page38 : Pin96: INVPWM rename to OUT9 & add T90

Page36 : Delete R500 & rename to EXPCRD_RST#

Page35 : Add JP3 for Smart card FFC connector

06/08/2005

Page7 : Delete PD resistor R1340~R1343.

Page17 : Update JP35 LVDS connector

Page26 : A. GPIO28 ==Delete R1321 & A_SD , change to VGA_RST#
B. GPIO21 ==Change to MB_PWR
C. GPIO19 ==Change to PD

06/09/2005

Page17 : Delete Q56 ,R510 ,Caymus support 3V PWM

Page25 : Update Q92 to AOS4407

Page26 : Delete R252

Page37 : Add PD RP42,R273

Delete Cardbus 6612 circuit & move to daughter board LS-2953

06/10/2005

Page17 : Add R458,R459 for ch_data,ch_clk

Page33 : Add C367 0.1U for +SC_PWR

06/11/2005

Page28: 1.Delete R15 ,due to Internal PD
2.Delete R69 ,due to Internal PD
3. Add U70,U71,R69,R92 R1297 for serial falsh support.

Page19 : Add T8/T9 for GPIO10/14

Page23 : Change L1,L2,L63,L6,L7,L9,L11-16,L65,L66 to FB

Page30 : Disconnect the I2C bus / WL_LED#/WP_LED# on JP46

Page10 : 1. Add R504/R505 for VCC_SYNC
2. Add R490/R491 for VCCTX_LVDS
3. Add R494 for VCCA_CRTDAC
4. Add R492/R493 for VCCA_LVDS
5. Add R495 for +3VS_TVBG
6. Add R500 for +3VS_TVDACA
7. Add R502 for +1,5VS_TVDAC
7. Add R499 for +3VS_TVDACB
8. Add R496 for +3VS_TVDACC

Page09 : 1.Add R460,R461, R550,R552,R553 for CRT discrete/uma option
2. Add R462,R463,R464 for TV discrete/uma option

06/13/2005

Page23 : Add R6 R15,R106,R128,R129 GPIO PD

06/14/2005

Page21 : Change L1,L2,L63 to FB

Page16 : 1. Add C174,C150,C142,C371,C358 for DVI
2. R103 change to 1%

Page35 : U69 pin7 change to PD

06/15/2005

Page04 : R1265 change to 51_0402_5% & install

Page07 : Install R1344

Page28 : Delete U70 ,reserve U71 for 200 mil

Page35 : Delete U61 , resevre U66 for 200 mil

Page29 : Update U7 symbol pinB7/B8/C8

06/16/2005

Page36 : Delete R32 ,double PU

Page41 : Delete R180,Q49 ,the same function for +1.8VS

Page10 : Delete C982 for Lead-free

Page20 : Add C570 for Lead free

Page32 : 1,Delete Q28 .
2. D49,D50 change to U73
3. Add C577,C581 for Lead free

Page33 : Add R163,R164,R165 for USB power switch PU

Page26 : Separate PCIE_WAKE# to NIC/Mini-card PCIE_WAKE# to avoid battery mode can't enter S3 issue

Page23 : Delete L65,C270,C269,C271 for M52-T

Page18~23 : ATI VGA controller change to M52T

06/22/2005

Page09 : Add R554 , R555 for CRT disable

Page10 : 1. Add R508,R510 for VCCD_LVDS1/1/2
2. R504,R505 chnage for +2.5VS_GMCH,&delete R490,R491,R492,R493

Page30 : Delete JP48,49 & change screw holes

06/23/2005

Page16 : Change SDVOB_INT+/- net name to PEG_RXP1/N1

Page10 : 1.R505 / R510 for M52 , R504 / R508 for UMA
2. R499,R500,R496 connect to +1.5VS for diable CRT

Page36: Delete R49 & CB_CLK

Page25: JP42 change to wire to board connector

Page19: 1.Add CRT,TV filters for M52T
2. Add DVI BOM option 0 ohm

Page16 : Move 0 ohm to TV-out connector for TV

Page38 : Move 0 ohm to docking connector for CRT

06/24/2005

Page19 : Add LVDS L-shape BOM option resistors

Page10 : Enable TV/ CRT when using 945PM

Page9 : Enable TV/ CRT when using 945PM

06/25/2005

Page33 : Delete U58, R165,C568,C1,C312,C311 FOR LAYOUT SPACE

06/27/2005

Change All 2N7002_SOT23 to RHU002N06_SOT323 to save layout space

06/28/2005

Page40 : Change Q10,Q11,Q15,Q26 from SOT23 to SOT323
to save layout space

Page37 : 1 . Update JP20 to 6 pin connector
2. Update JP20 & JP18 pin assignments to follow Taos

06/30/2005

Page28 : Y1 update to smaller package 6x3.5

Page25 : Y4 update to smaller package 14M-J

Page15 : Y3 update to smaller package 6x3.5

07/01/2005

Page23 : Add HW strpping pin on DVPDATA20,21,22,23 for VRAM ID0,1,2,3

Page33 : U57 change to 2A current limit power switch G548

07/04/2005

Page17 : Add R131 for inverter PWM when ATI PWM issue

Page19 : 1. Add R49 , R189 for 1.2V voltage divider
2. Add Q12 for M52_therm# & change to GPIO14

Page32 : The limitation for 5 pin audio jack can't switch
headphone/docking line-out ,so add R1420,R1421,C526,R252
Delete R256,R255,C536.

Page39 : Delete C984~C988

Page33 : Delete C527

Page10 : Delete C823 reserved pad

Page25 : Add JP5 slim type ODD connector

07/12/2005

Page25 : Add C629,C630,C631 for SATA connector

Page33 : Swap JP3 samrt card pin assignment for FFC

07/14/2005

Page25 : Add R133 100 ohm to avoid RTC short

Page15 : 1. clock gen. pin 5 change to connect to +ck_vdd_dp
2. C731,C732,C733 change from 0.1u to 0.01u
3. C361,C364 change from 33p to 27p

07/19/2005

Page39 : Add C91,C93,C181 for low speed signal

07/20/2005

Page30 : Add R1422 pad for XMIT_OFF

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Size	Document Number: LA-2952P	Rev: 0.3
Date: Wednesday, October 26, 2005	Sheet 44 of 46	

For DB2 Modification

08/11/2005

Page31/32 : Update Audio portion for jack sensing
Page35 : Delete LED circuit & connect to LS-2953 directly
Page11 : Change R1154 to NI
Page30 : Add C554 for UIM power
Page25 : Delete JP37 MB2 conector
Page19 : Change C611 to NI ,R662 to 0 ohm for clcok spectrum
Page15 : Add R1136 PD for clk_pcie_m52 ,R1084 change to NI
Page24 : R1388 change to Install
Page26 : R1364 change to NI
Page36 : R1354 change to NI

08/15/2005

Page30 : R1418 , R1360 change to NI

08/19/2005

Page35 : Delete FWH , SPI change to +3VALW
Page36 :Delete R538
Page10 : Delete L39
Page25 : Add D15, D16 , R90 , R88 for HDD LED

08/20/2005

Page30 : Change +3VL / Caps_LED# to Pin45/51
Page38 : Delete R551 ,R548,R549,R541
Page25 : Add D15,D16,R88,R90 for HDD_LED
Page30 : Add SW1 C986, R521 , D65,D66 for SIM power off

08/24/2005

Page15 : Add C353~C372 for clk cap

08/25/2005

Page31/32 : Add JP16 for audio cable
Page30 : Internal MIC signal change to JP13

08/26/2005

Page32 : Add R427,R429,C492 for J_MIC_REF

08/29/2005

Page32 : Add 1423,R1424 for MIC_REF , & MIC_SENSE connection
Page23 : R154 change to NI
Page29 : Add C333 for NIC

08/30/2005

Page15 : Add C373 for clk_debug_port
Page23 : Add R173 for Therm_SCI#
Page36 : R538 change to NI
Page21 : Add C140, C172 , C141 , L17 for VDDPLL

08/31/2005

Page32 : Delete R1419, R1420
Page19 : R189 change to 56_0402_1%

10/04/2005

Page26 : R251.2/C526.1 connect to DLINE_OUT_L
Page32 : PR255.1 connect to pin 29 of the docking connector.
(ACOCP_EN#)
Page29 : Add discharge circuit for BT_LED and WL_LED(R504,R505)
(this issue occurs when there is no WLAN card)
Page20 : Delete R1323 (EAPD to ICH7)
Page22 : Add Q40,R1419, reserve R1420
Page24 : Add R996,reserve R519,Q41,Q42
Page29 : Install R1409, Make R1380 NI；reserve R101
Page30 : Reserve R91,R102
Page27 : Change R454 to 47K , add C556
Page25 : Install R136
Page15 :Delete R1071,R1073,R1076,R1082,R1094,R1096,R1258,R1260
R1112,R1116,R1250,R1252,R1124,R1127,R1134,R1137,R1238
R1239,R1242,R1248,R1253,R1272(NOLP@)

10/04/2005

Page32 : Reserve C555

10/06/2005

Page24: NI D64 ,install R1355
Page07: NI R1202,R1203
Page22: NI R1397,U36；Install Q94；Add R1076
Page29:Reserve U61
Page24:Add R1364；Reserve R1363
Page30:Install R91
Page24:Add R1366；Reserve R1365

10/07/2005

Page24: Add R1071,R1073
Page07: NI R1209
Page22: Install R275,R289；NI R1396,R1398
Page20: Install R1384,R1395；Reserve R1385,R1427
Del Q71,R1345
Page20: Add R1040,R871；Reserve Q106；Del R1404
Page22 : Add R1091,R1082,R1088,R1085,Q105,R1023,
R1024,D63,C1042,U55,R1021,R1076；
Reserve Q103,Q104,R1090,
Del R601.
Page15 : Del R1084,R1136

10/08/2005

Page28 :Install Q103；NI R1091

10/13/2005

Page33 :Delete J33
Page18 :Delete BIOS_SEL jump

10/26/2005

Page26 :NI C526
Page32 :Add R1404,R1428,R1429,R1430,R1431,R1432,
R609,R608,R611,R610,R613,R612,R616,R615
Page31 :Install CP1~CP6

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Version Change List (P. I. R. List) for Power Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	42,44,50		8/26/2005 (DB)	HP	To implement 4 cell main battery	Add PR2,PR259,PR261(1M ohm), Add PQ73,PQ74,PQ75,PQ76(RHU002N06_SOT323) Add PR260(39.2k)	DB
2	48		8/30/2005 (DB)	HP	To fix VDD_CORE in 1V(Only for Discrete).	Remove PQ49,PQ66	DB
3	50		10/18/2005 (SI)	HP	Changes for OCP circuit	Add PC147 3900pF capacitor across PR214 Change PR207 from 0 Ohm to 3.9K_5% Change PC131 from 0.22uF to 0.027uF Change PR203 from 649K to 604K_1% Change PR221 from 47K to 10K_5% Add a newPR265 47K_5% resistor in series with PR216-2 Add a new PC146 1uF X7R capacitor from PR216-2 to GND Change PC133 from 10uF to 0.1uF X7R Change PR228 from 10K to 21K_1% Change PR234 from 11.5K to 3.48K_1% Change PR232 from 3.3K to 21K_1%	SI
4	43		10/18/2005 (SI)	HP	sets Max charge current to 3.75A	Change PR29 from 100K to 143K_1%	SI

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