

Compal confidential

Schematics Document

Mobile Merom uFCPGA with Satna Rosa Platform

2007-07-30

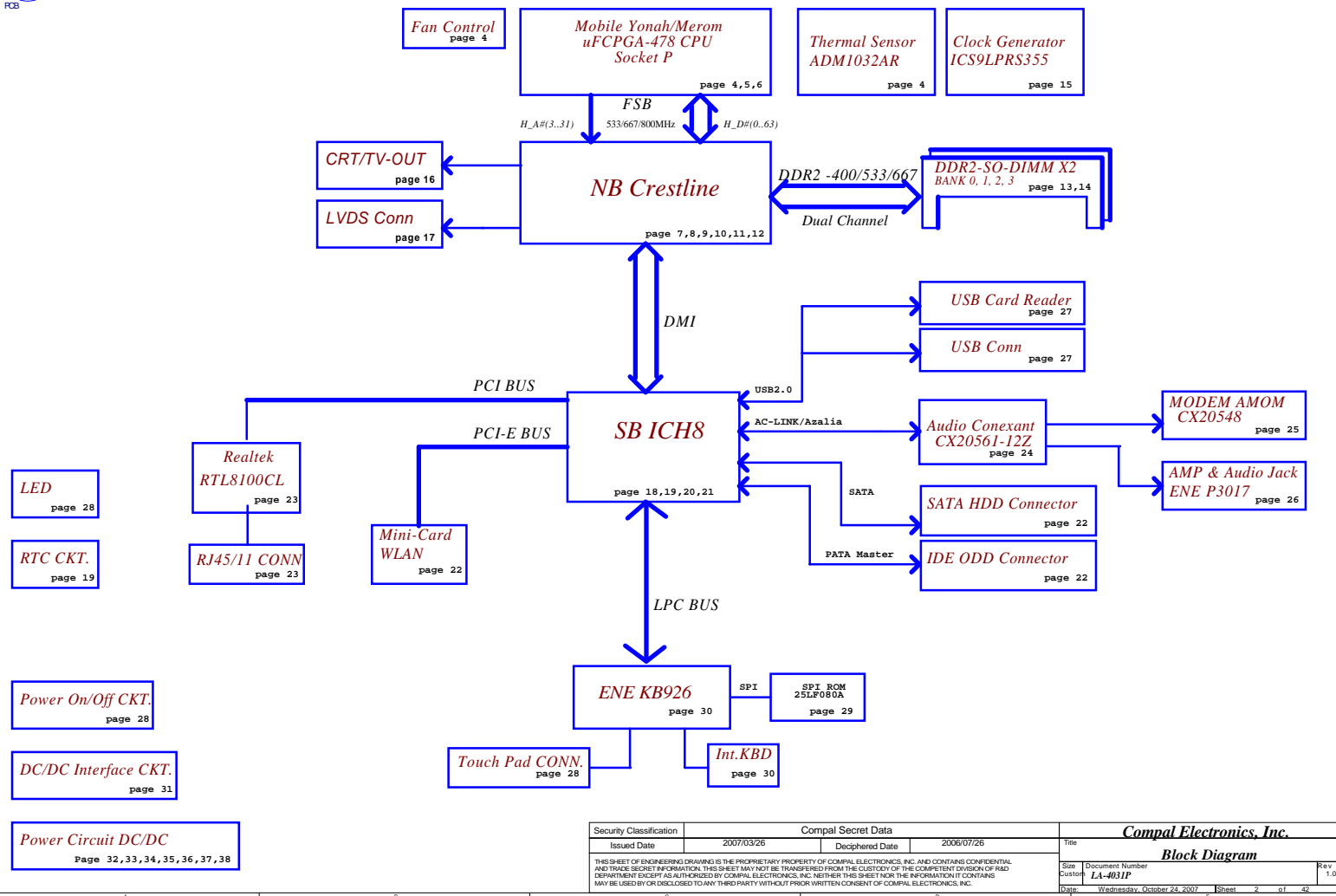
REV: 0.2

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Spartan 1.1 (Merom +Crestline+ICH8)



PCB



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Compal Electronics, Inc.				Block Diagram
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Voltage Rails

power plane State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +1.25VS +0.9V +VCCP +CPU_CORE
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :



: means Digital Ground



: means Analog Ground

@ : means just reserve , no build

DEBUG@ : means just reserve for debug.

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
LAN	AD17	0	A

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010

SMBUS Control Table

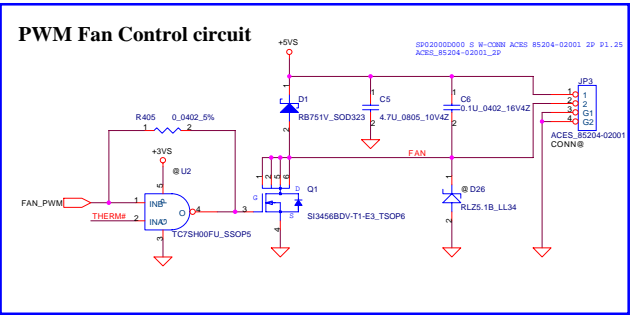
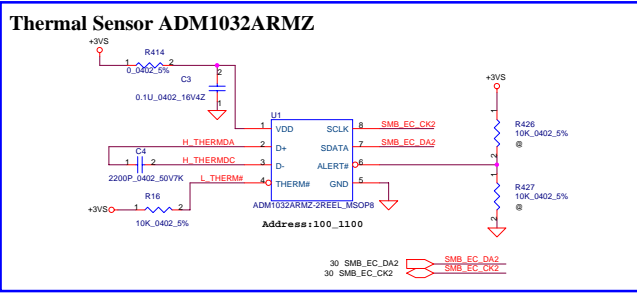
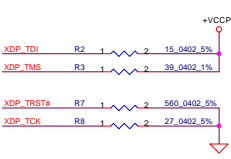
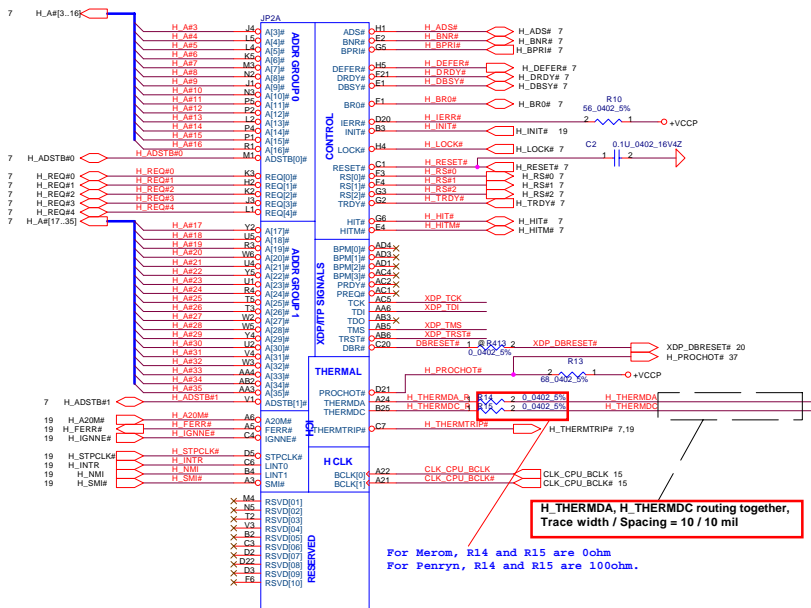
	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU) ADM1032	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB925	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB925	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CR_DAT1	ICH8	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Crestline	X	X	X	X	X	X	X	V

BOM: 43152432L03(965GM) & 43152432L04(960GML) with card reader

BOM: 43152432L01(965GM) & 43152432L02(960GML) without card reader

Jump-Short: PJP?

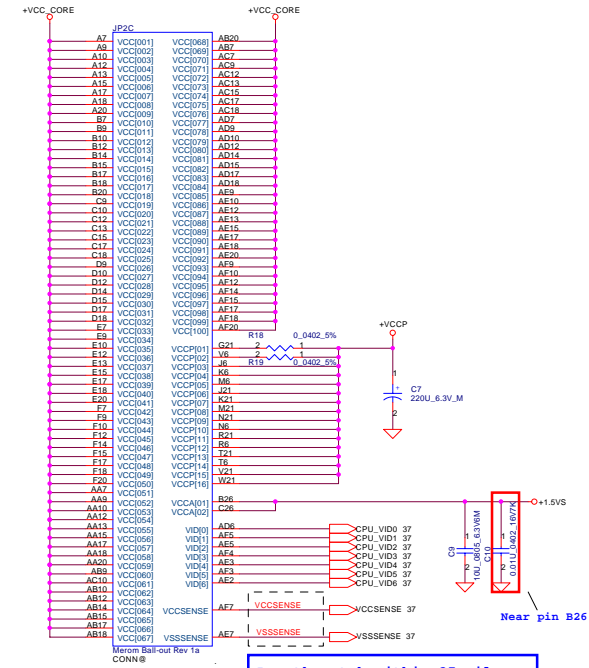
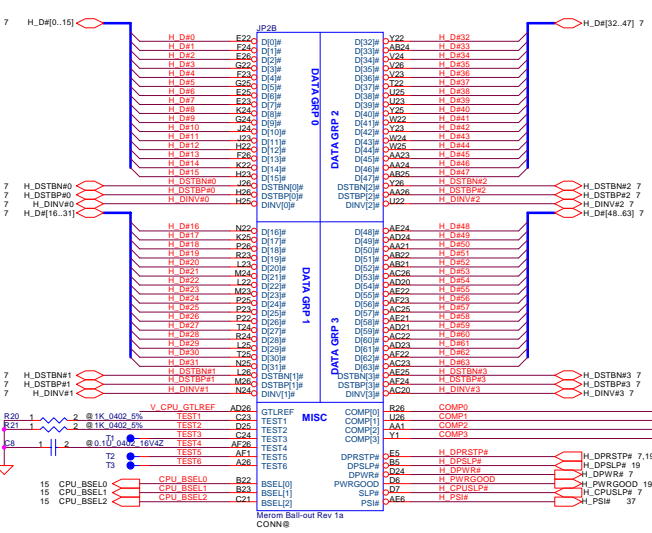
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**H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil**

For Merom, R14 and R15 are 0ohm
For Penryn, R14 and R15 are 100ohm.

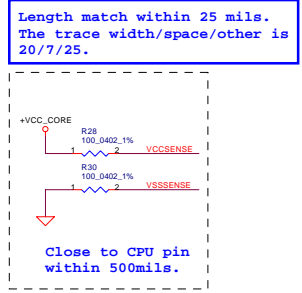
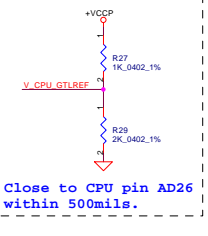
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layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

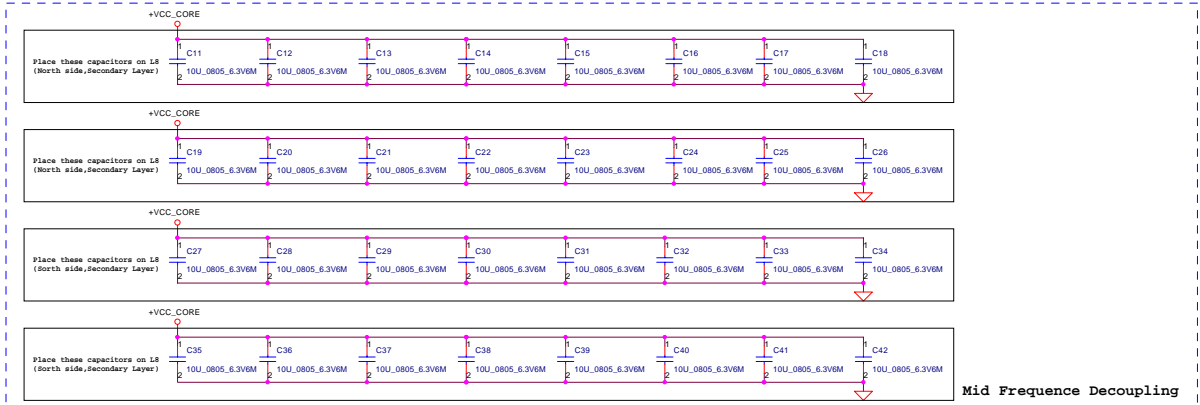
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



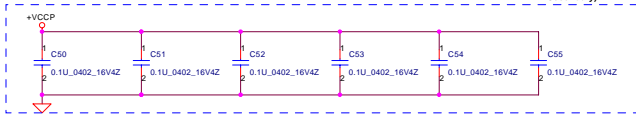
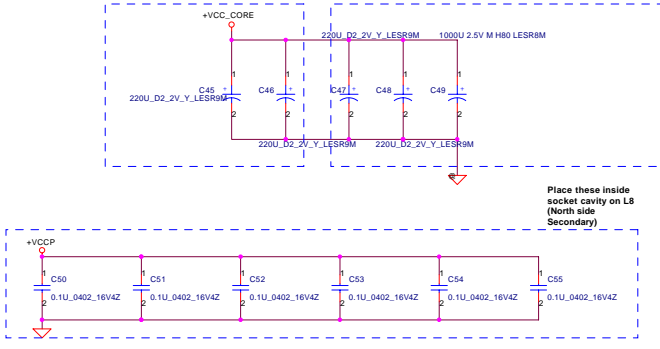
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JP2D			
A4	VSS1001	VSS1080	P6
A5	VSS1002	VSS1083	P21
A6	VSS1003	VSS1084	P22
A14	VSS1004	VSS1085	R2
A16	VSS1006	VSS1087	R22
A19	VSS1009	VSS1090	R22
A22	VSS1012	VSS1093	T1
AF2	VSS1077	VSS1088	T1
BB	VSS1008	VSS1089	T4
BB	VSS1009	VSS1090	T4
B11	VSS1011	VSS1092	T26
B13	VSS1012	VSS1093	T27
B18	VSS1013	VSS1094	U6
B19	VSS1014	VSS1095	U2
B21	VSS1016	VSS1097	U24
C2	VSS1017	VSS1098	U2
C4	VSS1018	VSS1099	U22
C8	VSS1021	VSS1102	U4
C11	VSS1022	VSS1103	U22
C14	VSS1023	VSS1104	U2
C16	VSS1024	VSS1105	U2
C19	VSS1027	VSS1108	U2
C2	VSS1028	VSS1109	U2
C22	VSS1030	VSS1111	U2
C25	VSS1031	VSS1112	U2
D1	VSS1032	VSS1113	U2
D11	VSS1033	VSS1114	U2
D18	VSS1034	VSS1115	U2
D19	VSS1035	VSS1116	U2
D23	VSS1036	VSS1117	U2
D28	VSS1037	VSS1118	U2
E3	VSS1038	VSS1119	U2
E8	VSS1039	VSS1120	U2
E11	VSS1040	VSS1121	U2
E16	VSS1041	VSS1122	U2
E21	VSS1042	VSS1123	U2
F4	VSS1043	VSS1124	U2
F8	VSS1044	VSS1125	U2
F11	VSS1045	VSS1126	U2
F13	VSS1046	VSS1127	U2
F16	VSS1047	VSS1128	U2
F19	VSS1048	VSS1129	U2
F21	VSS1049	VSS1130	U2
F2	VSS1050	VSS1131	U2
F22	VSS1051	VSS1132	U2
F25	VSS1052	VSS1133	U2
G4	VSS1053	VSS1134	U2
G11	VSS1054	VSS1135	U2
G28	VSS1055	VSS1136	U2
H8	VSS1056	VSS1137	U2
H8	VSS1057	VSS1138	U2
H21	VSS1058	VSS1139	U2
H24	VSS1059	VSS1140	U2
J2	VSS1060	VSS1141	U2
J2	VSS1061	VSS1142	U2
J22	VSS1062	VSS1143	U2
K5	VSS1063	VSS1144	U2
K1	VSS1064	VSS1145	U2
K4	VSS1065	VSS1146	U2
K4	VSS1066	VSS1147	U2
K29	VSS1067	VSS1148	U2
K28	VSS1068	VSS1149	U2
L3	VSS1069	VSS1150	U2
L6	VSS1070	VSS1151	U2
L21	VSS1071	VSS1152	U2
L24	VSS1072	VSS1153	U2
M2	VSS1073	VSS1154	U2
M2	VSS1074	VSS1155	U2
M22	VSS1075	VSS1156	U2
M28	VSS1076	VSS1157	U2
N1	VSS1077	VSS1158	U2
N4	VSS1078	VSS1159	U2
N23	VSS1079	VSS1160	U2
N21	VSS1080	VSS1161	U2
P1	VSS1081	VSS1162	U2
	VSS1082	VSS1163	U2

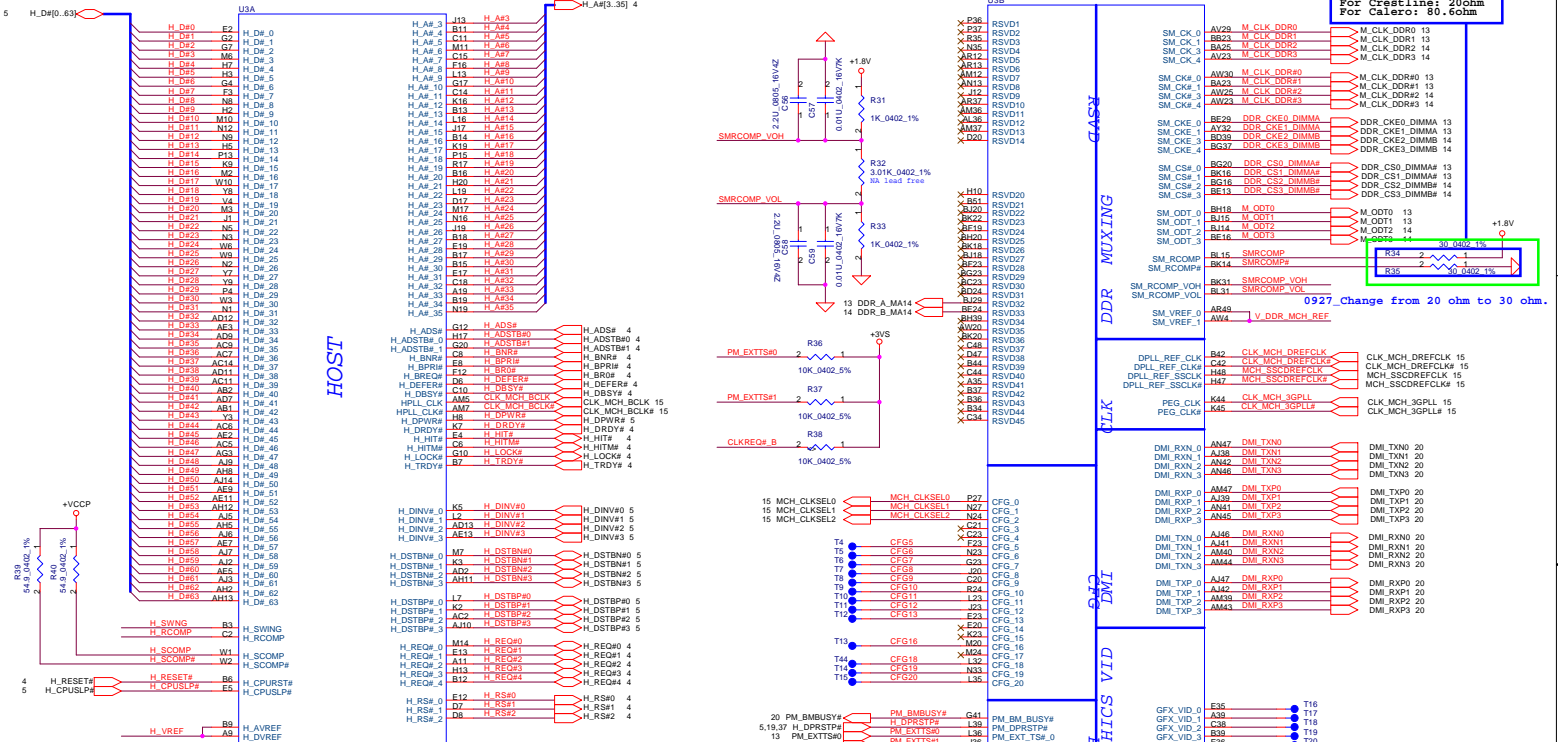


Mid Frequency Decoupling

Near CPU CORE regulator ESR <= 1.5m ohm Capacitor > 1980uF



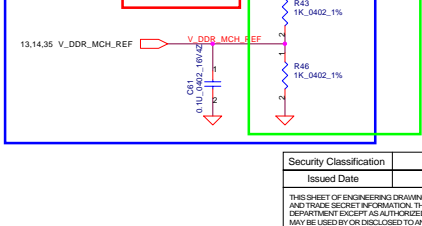
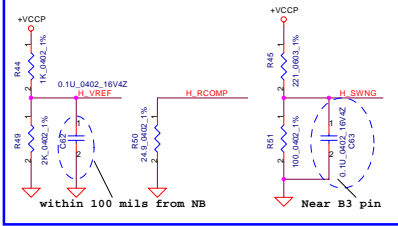
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layout note:
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as F8B data traces

Layout Note:
H_RCMP / H_VREF / H_SWNG trace width and spacing is 10/20

Layout Note:
V_DDR_MCH_REF trace width and spacing is 20/20.

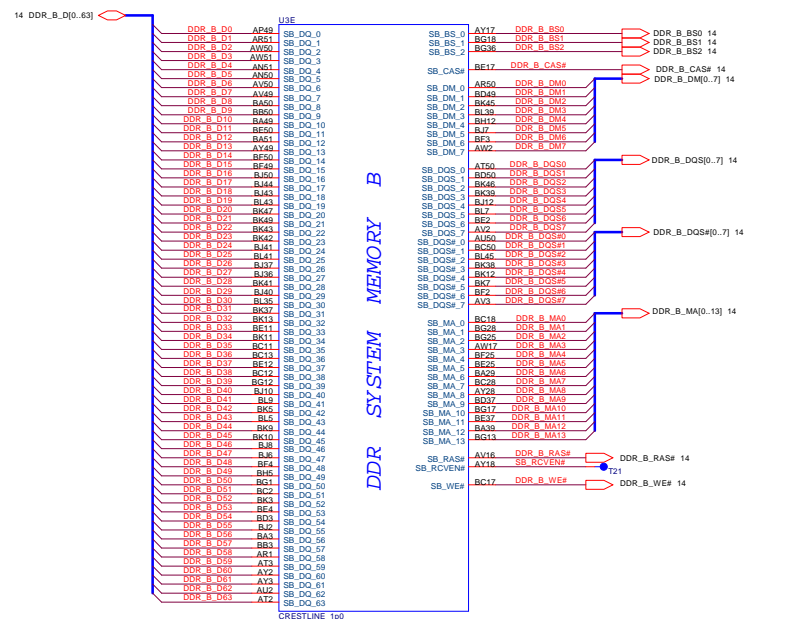
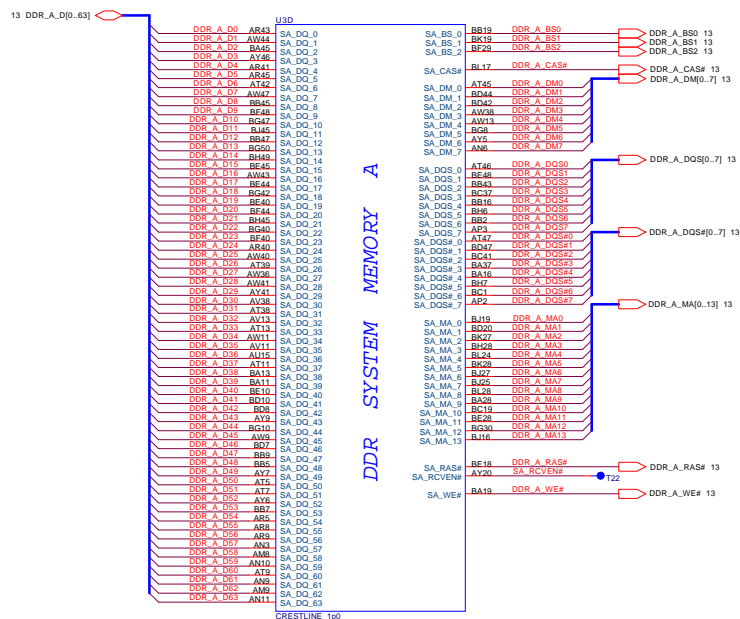


0925_Stuff R43 and R46.

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Title		CRESTLINE(1/6)-AGTL+DMI/DDR2	
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CRESTLINE_1p0

CRESTLINE_1p0

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Strap Pin Table

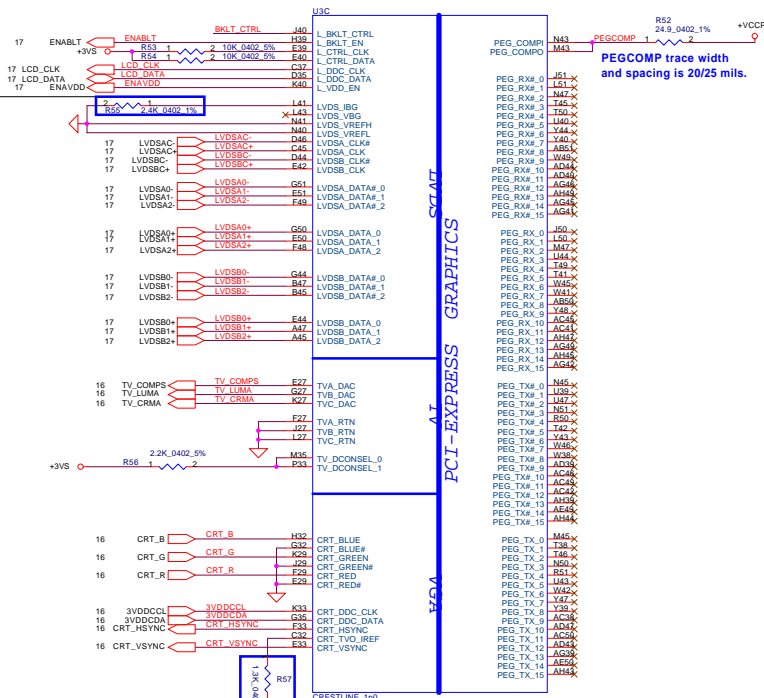
CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIe)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.

CFG[17:3] have internal pull up
CFG[19:18] have internal pull down

For Crestline: 2.4kohm
For Calero: 1.5kohm

PEGCOMP trace width and spacing is 20/25 mils.

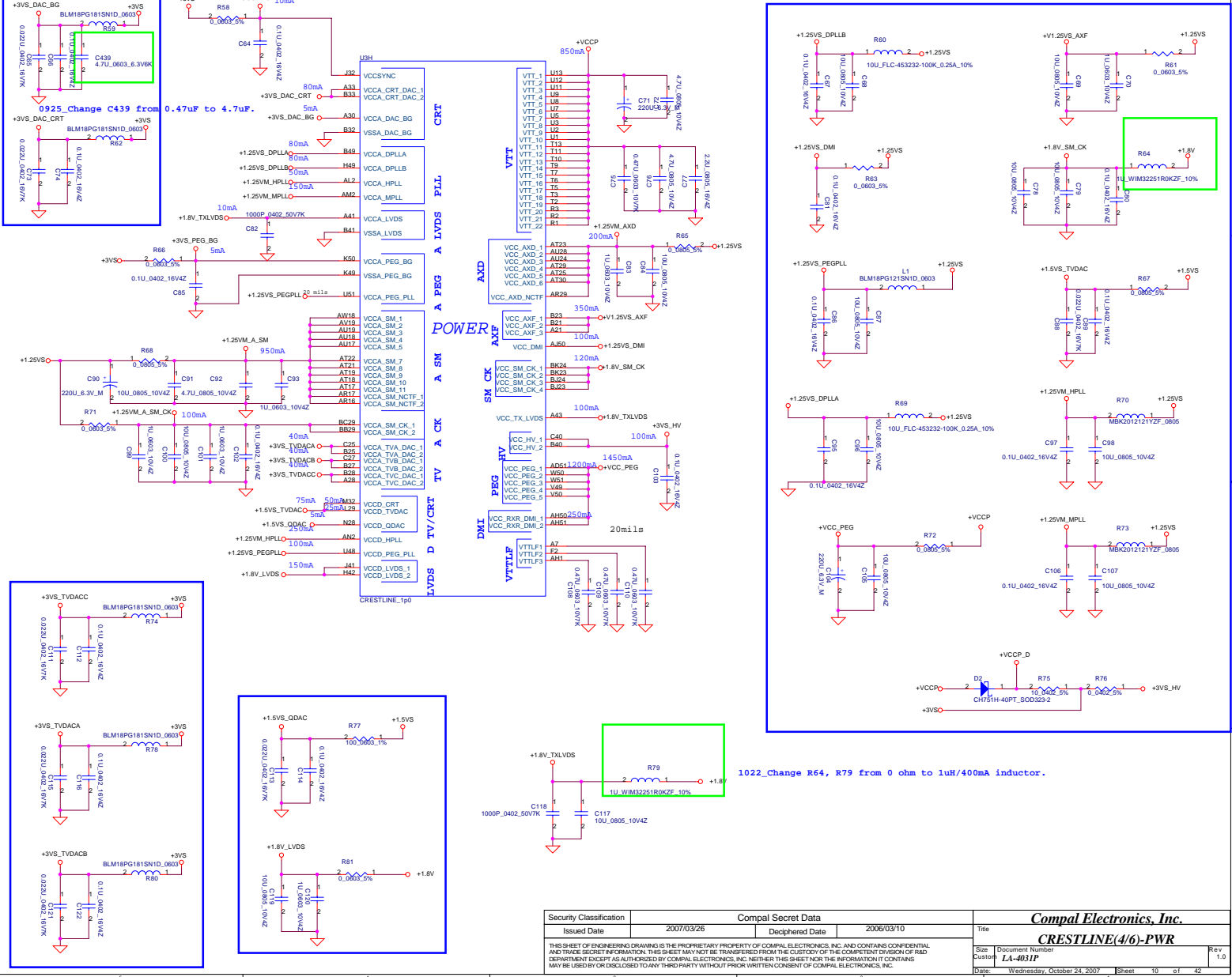
For Crestline: 1.3kohm
For Calero: 255ohm



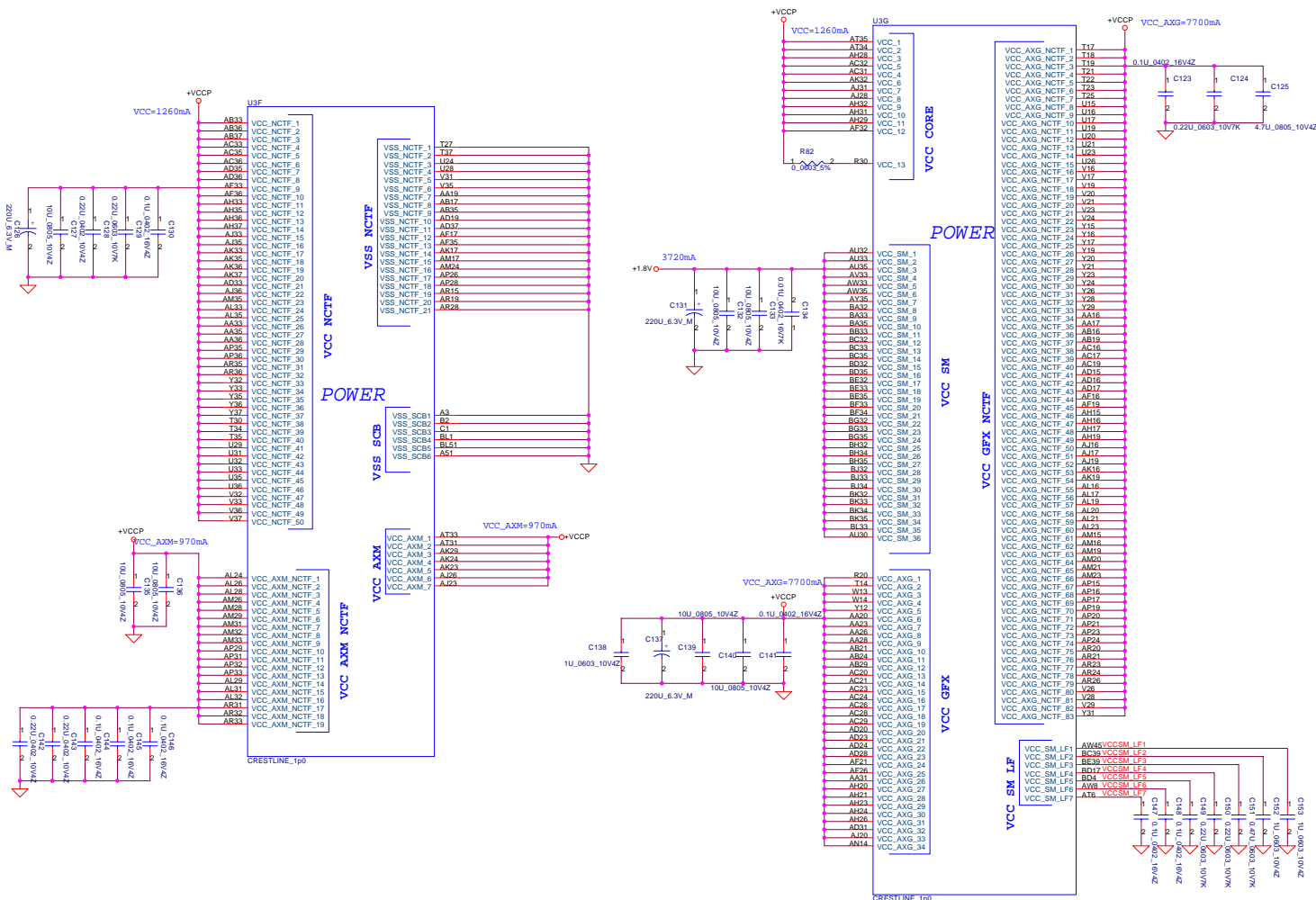
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CRESTLINE(3/6)-VGA/LVDS/TV

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CRESTLINE((5/6)-PWR/GND

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U31

A13	VSS_1	AW24
A15	VSS_2	AW23
A17	VSS_3	AW22
A2	VSS_4	AW21
AA21	VSS_5	AW20
AA24	VSS_6	AW19
AA25	VSS_7	AW18
AB20	VSS_8	AW17
AB23	VSS_9	AW16
AB26	VSS_10	AW15
AB28	VSS_11	AW14
AB31	VSS_12	AW13
AC10	VSS_13	AW12
AC13	VSS_14	AW11
AC1	VSS_15	AW10
AC2	VSS_16	AW9
AC43	VSS_17	AW8
AD1	VSS_18	AW7
AD21	VSS_19	AW6
AD26	VSS_20	AW5
AD29	VSS_21	AW4
AD3	VSS_22	AW3
AD41	VSS_23	AW2
AD49	VSS_24	AW1
AD5	VSS_25	AW0
AD5	VSS_26	AW0
AD50	VSS_27	AW0
AE10	VSS_28	AW0
AE14	VSS_29	AW0
AE1	VSS_30	AW0
AE1	VSS_31	AW0
AE1	VSS_32	AW0
AF23	VSS_33	AW0
AF24	VSS_34	AW0
AF24	VSS_35	AW0
AF31	VSS_36	AW0
AG2	VSS_37	AW0
AG38	VSS_38	AW0
AG43	VSS_39	AW0
AG47	VSS_40	AW0
AH3	VSS_41	AW0
AH9	VSS_42	AW0
AH41	VSS_43	AW0
AH7	VSS_44	AW0
AH9	VSS_45	AW0
AH9	VSS_46	AW0
AJ11	VSS_47	AW0
AJ3	VSS_48	AW0
AJ21	VSS_49	AW0
AJ24	VSS_50	AW0
AJ29	VSS_51	AW0
AJ32	VSS_52	AW0
AJ43	VSS_53	AW0
AJ45	VSS_54	AW0
AJ45	VSS_55	AW0
AK20	VSS_56	AW0
AK21	VSS_57	AW0
AK28	VSS_58	AW0
AK28	VSS_59	AW0
AK31	VSS_60	AW0
AK51	VSS_61	AW0
AL1	VSS_62	AW0
AM11	VSS_63	AW0
AM3	VSS_64	AW0
AM4	VSS_65	AW0
AM41	VSS_66	AW0
AN1	VSS_67	AW0
AN45	VSS_68	AW0
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AN7	VSS_73	AW0
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AP48	VSS_75	AW0
AP48	VSS_76	AW0
AP50	VSS_77	AW0
AR1	VSS_78	AW0
AR2	VSS_79	AW0
AR2	VSS_80	AW0
AR44	VSS_81	AW0
AR7	VSS_82	AW0
AT10	VSS_84	AW0
AT14	VSS_85	AW0
AT41	VSS_86	AW0
AT6	VSS_87	AW0
AU1	VSS_88	AW0
AU23	VSS_89	AW0
AU2	VSS_90	AW0
AU36	VSS_91	AW0
AU36	VSS_92	AW0
AU49	VSS_93	AW0
AU4	VSS_94	AW0
AV38	VSS_95	AW0
AV48	VSS_96	AW0
AW1	VSS_97	AW0
AW12	VSS_98	AW0
AW16	VSS_99	AW0

VSS

U31

C46	VSS_199	W11
C50	VSS_200	W39
C7	VSS_201	W43
D13	VSS_202	W47
D24	VSS_203	W5
D3	VSS_204	W7
D32	VSS_205	Y13
D39	VSS_206	Y2
D45	VSS_207	Y41
D49	VSS_208	Y46
E10	VSS_209	Y49
E14	VSS_210	Y50
E24	VSS_211	Y50
E28	VSS_212	Y50
E47	VSS_214	T29
F19	VSS_215	T31
F36	VSS_216	T33
F4	VSS_217	T35
F40	VSS_218	R28
F50	VSS_219	
G1	VSS_220	
G13	VSS_221	VSS_306
G16	VSS_222	AA32
G19	VSS_223	AD32
G24	VSS_224	VSS_308
G28	VSS_225	VSS_309
G28	VSS_226	AF29
G34	VSS_227	VSS_310
G42	VSS_228	AV27
G46	VSS_229	VSS_311
G48	VSS_230	AV25
G48	VSS_231	H50
H24	VSS_232	
H28	VSS_233	
H4	VSS_234	
H45	VSS_235	
J11	VSS_236	
J16	VSS_237	
J2	VSS_238	
J24	VSS_239	
J33	VSS_240	
J35	VSS_241	
J35	VSS_242	
J35	VSS_243	
K12	VSS_245	
K47	VSS_246	
L1	VSS_247	
L17	VSS_248	
L20	VSS_249	
L24	VSS_250	
L24	VSS_251	
L28	VSS_252	
L3	VSS_253	
L33	VSS_254	
L48	VSS_255	
M28	VSS_256	
M42	VSS_257	
M48	VSS_258	
M49	VSS_259	
M5	VSS_260	
M50	VSS_261	
M9	VSS_262	
N14	VSS_263	
N17	VSS_264	
N29	VSS_265	
N32	VSS_266	
N32	VSS_267	
N39	VSS_268	
N44	VSS_269	
N49	VSS_270	
N7	VSS_271	
P19	VSS_272	
P2	VSS_273	
P23	VSS_274	
P23	VSS_275	
P3	VSS_276	
P39	VSS_277	
P49	VSS_278	
P59	VSS_279	
T43	VSS_280	
T47	VSS_281	
T47	VSS_282	
U41	VSS_283	
U50	VSS_284	
V2	VSS_285	
V3	VSS_286	

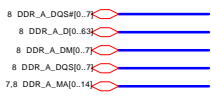
VSS

Security Classification	Compal Secret Data		Title	
Issued Date	2007/03/26	Deciphered Date	2006/03/10	Customer
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Date: Wednesday, October 24, 2007				Sheet 12 of 42

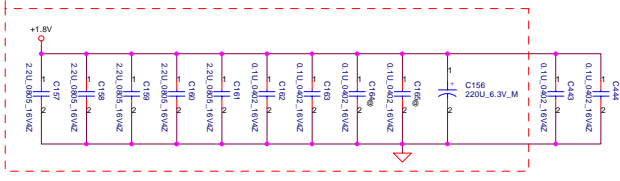
Compal Electronics, Inc.
CRESTLINE((6/6)-PWR/GND

Customer: LA-403P Rev 1.0

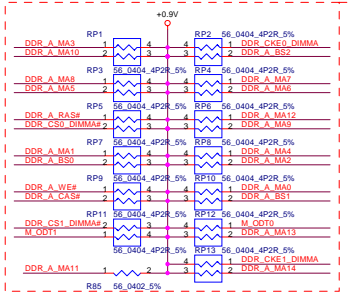
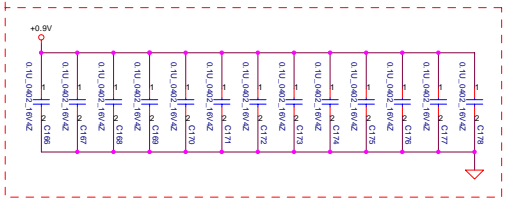
Date: Wednesday, October 24, 2007 Sheet 12 of 42



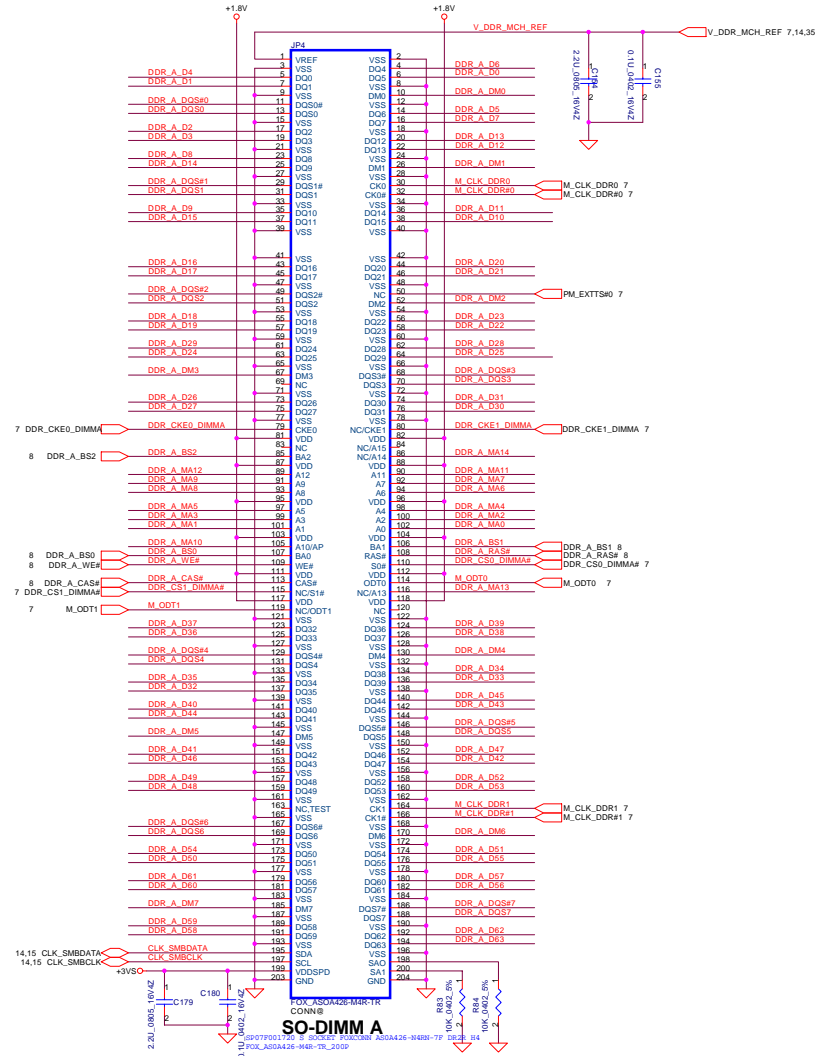
Layout Note:
Place near JP34



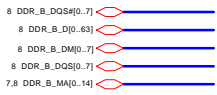
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



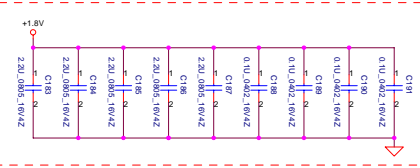
Layout Note:
Place these resistor closely JP34, all trace length Max=1.5"



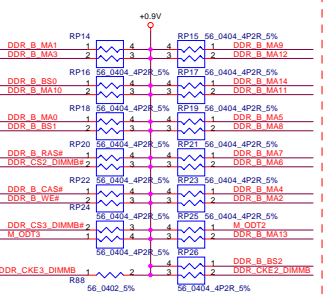
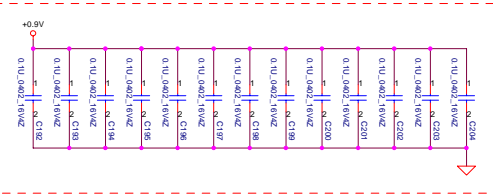
Compal Security Data				Title	
Security Classification	Deciphered Date	Deciphered Date	Deciphered Date	2006/03/10	DDR2-SODIMM SLOT
Issued Date	2007/03/26	Deciphered Date	2006/03/10		
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Size	Document Number	Rev			
Customer	LA-4031P	1.0			
Date	Wednesday, October 24, 2007	Sheet	13	of	42



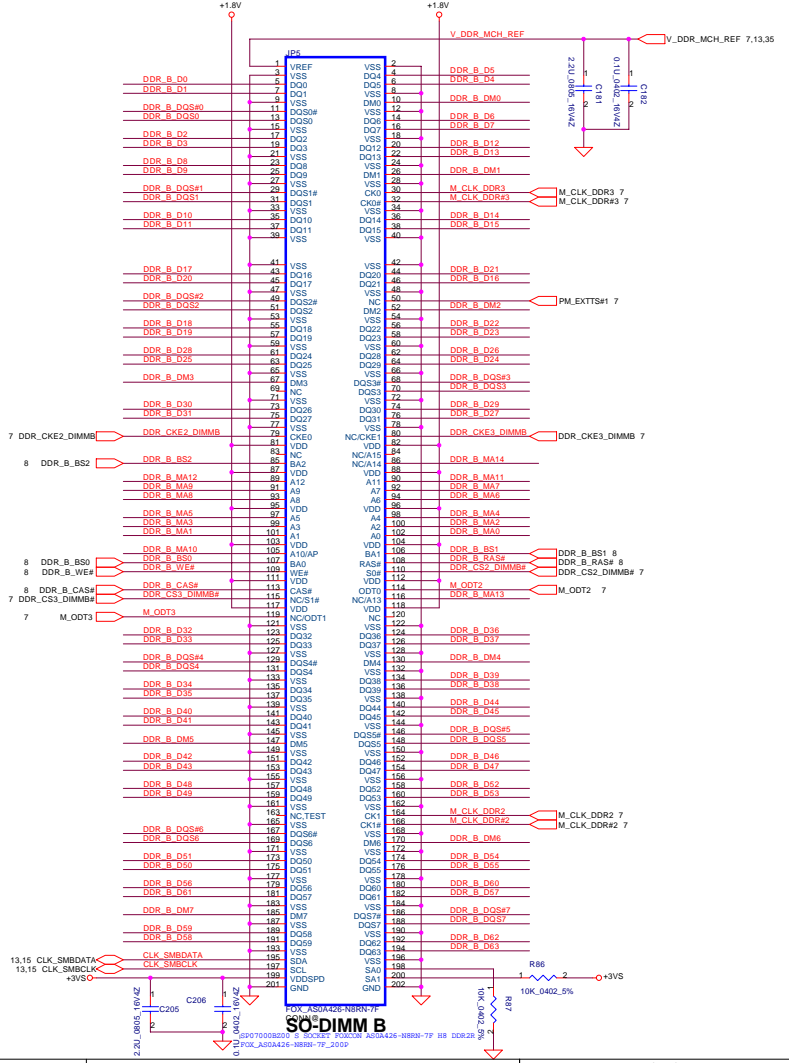
Layout Note:
Place near JP10



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V



Layout Note:
Place these resistor closely JP10, all trace length Max=1.5"



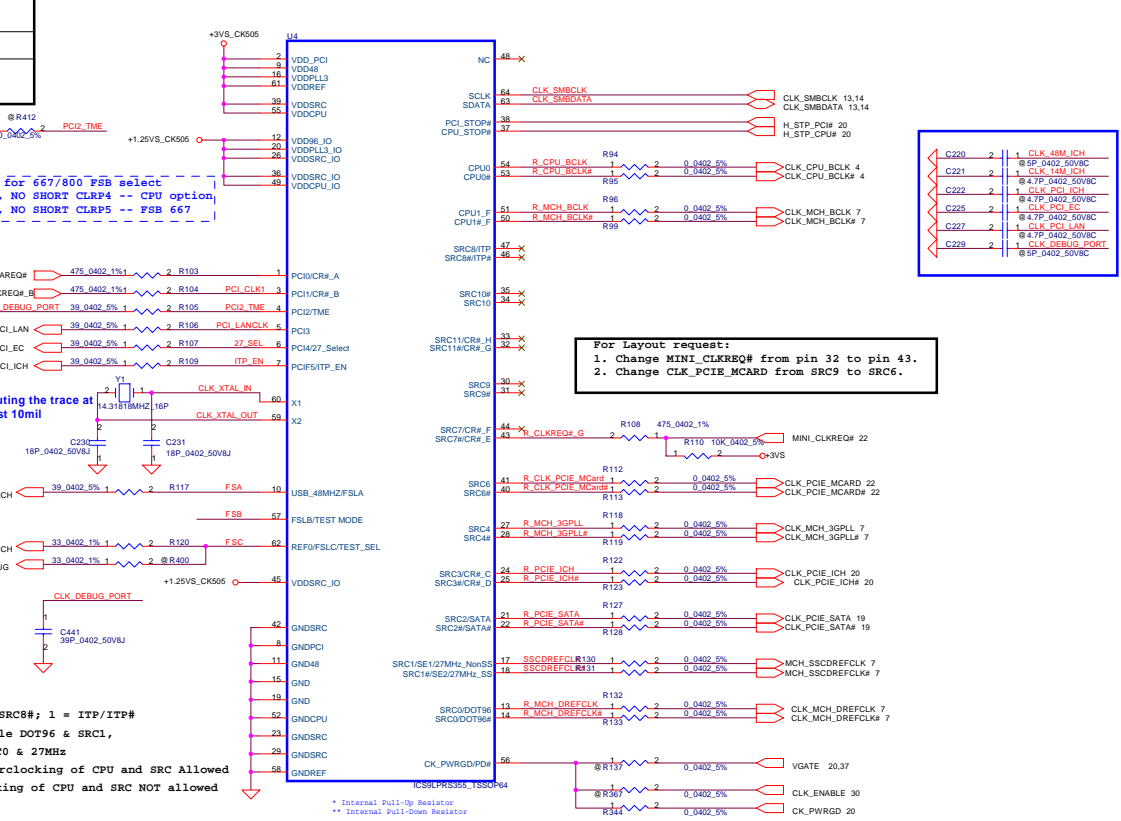
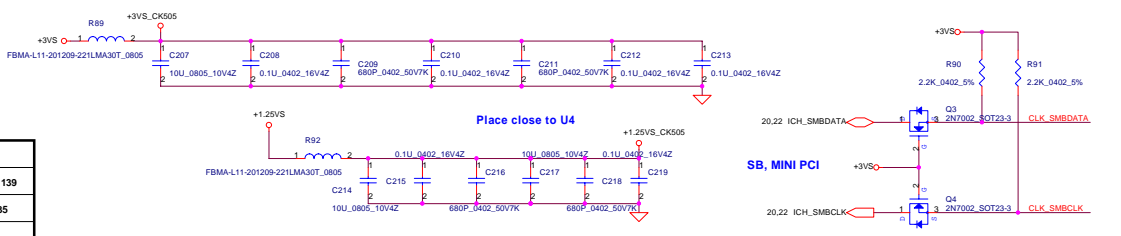
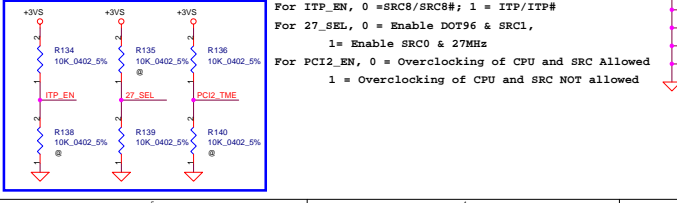
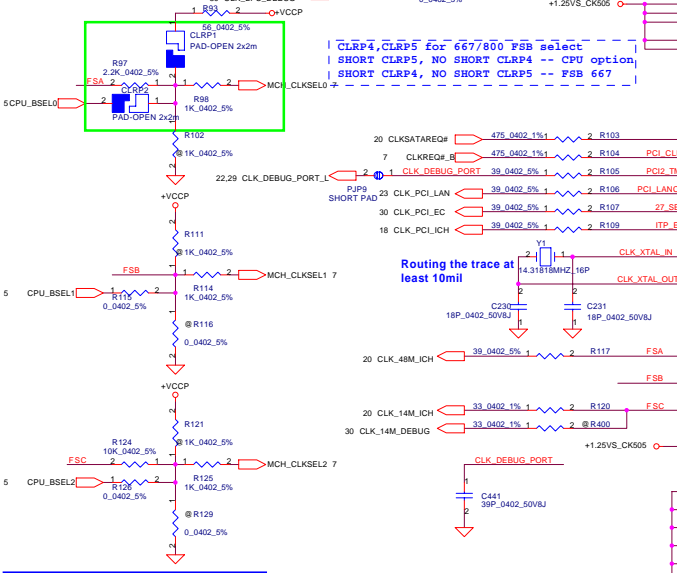
Compal Security Data				Title	
Security Classification	Issued Date	Deciphered Date	2006/03/10	DDR1-SODIMM SLOT2	
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				Date: Wednesday, October 24, 2007	Sheet 14 of 42

FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	1	133	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3

FSB Frequency Set:

CPU Driven	Stuff	R107	R1135	R1083
*(Default)	No Stuff	R1074	R1086	R1098 R1113 R1128 R1139
	Stuff	R1086	R1139	R1135 R1074 R1139 R1135
667MHz	No Stuff	R1083	R1107	R1128 R1113 R1098
	Stuff	R1135	R1139	
800MHz	No Stuff	R1083	R1086	R1098 R1128 R1074 R1107 R1113

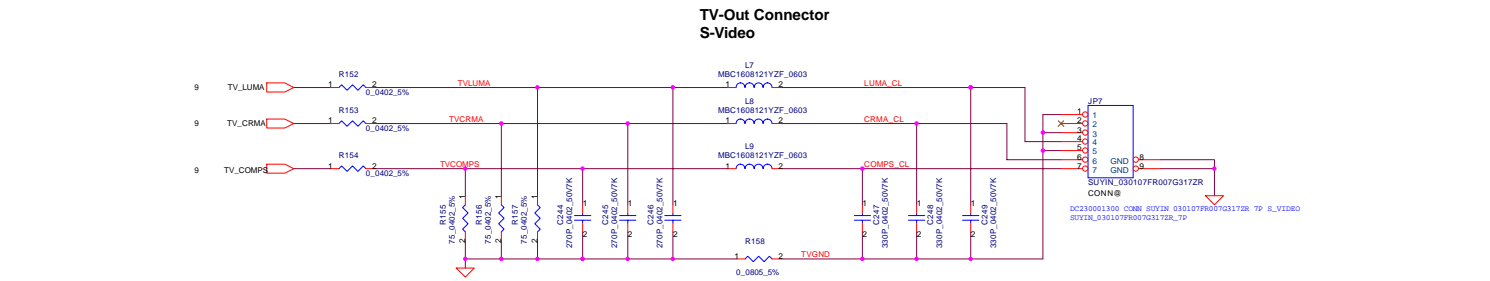
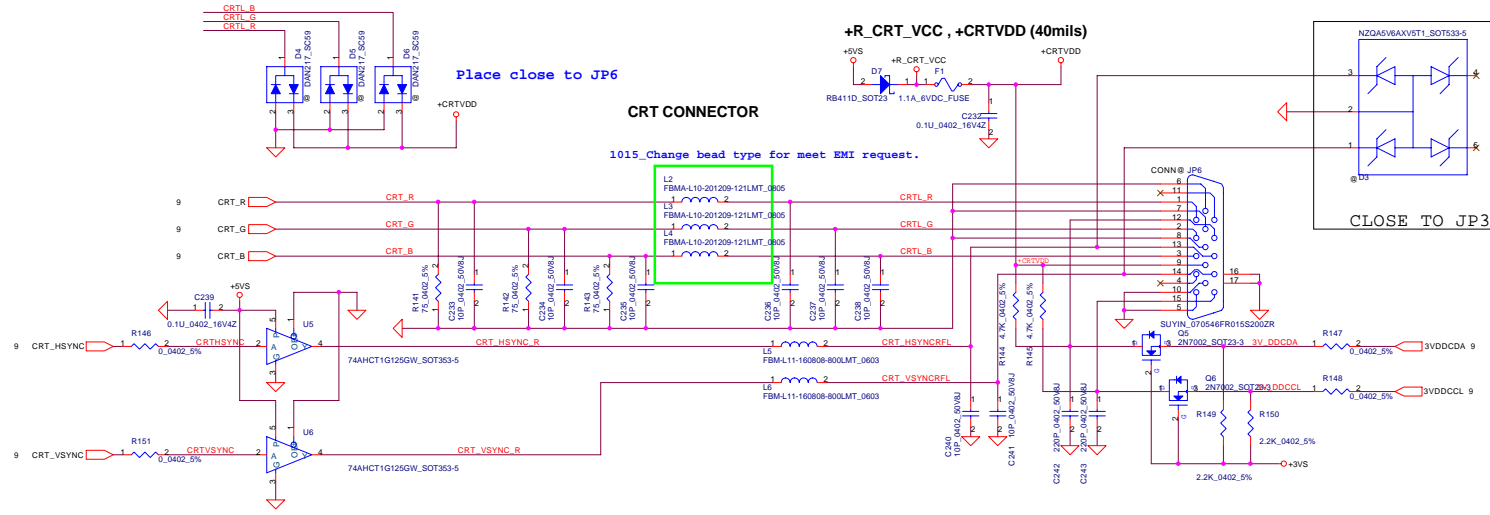
1015_Change CLR1P and CLR2 type like the same as RJP4.



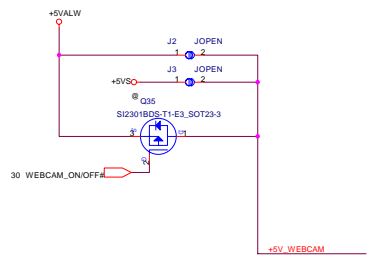
C220	2	1	CLK_48M_ICH
C221	2	1	5P_0402_50VBC
C222	2	1	CLK_14M_ICH
C223	2	1	4.7P_0402_50VBC
C224	2	1	CLK_PCIE_ICH
C225	2	1	4.7P_0402_50VBC
C226	2	1	4.7P_0402_50VBC
C227	2	1	CLK_PCL_LAN
C228	2	1	4.7P_0402_50VBC
C229	2	1	CLK_DEBUG_PORT
			5P_0402_50VBC

For Layout request:
 1. Change MINI_CLKREQ# from pin 32 to pin 43.
 2. Change CLK_PCIE_MCARD from SRC9 to SRC6.

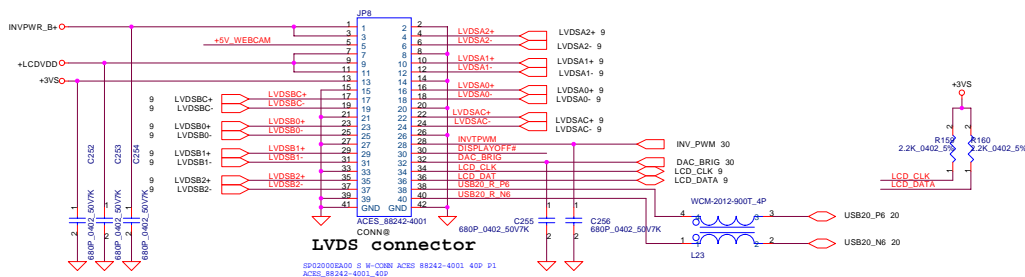
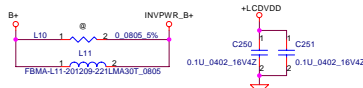
Security Classification	Compal Secret Data	Deciphered Date	2006/03/10	Title	Compal Electronics, Inc.
Issued Date	2007/03/26	Deciphered Date	2006/03/10		
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Size	Document Number	LA-4031P	Rev	1.0	
Date	Wednesday, October 24, 2007	Sheet	16	of	42



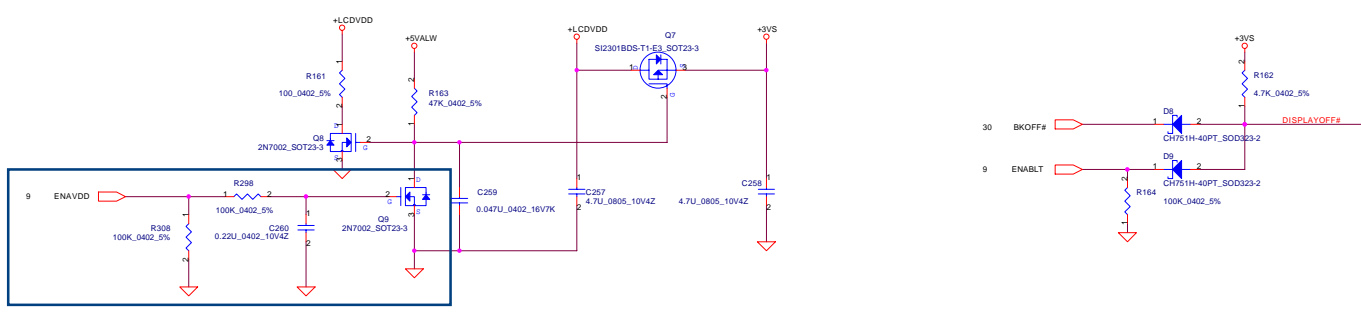
Security Classification	Compal Secret Data		
Issued Date	2007/03/26	Deciphered Date	2006/07/26
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Title			Compal Electronics, Inc.
Size			CRT & TVout Connector
Document Number			LA-4031P
Date	Wednesday, October 24, 2007	Sheet	16 of 42



LVDS CONN

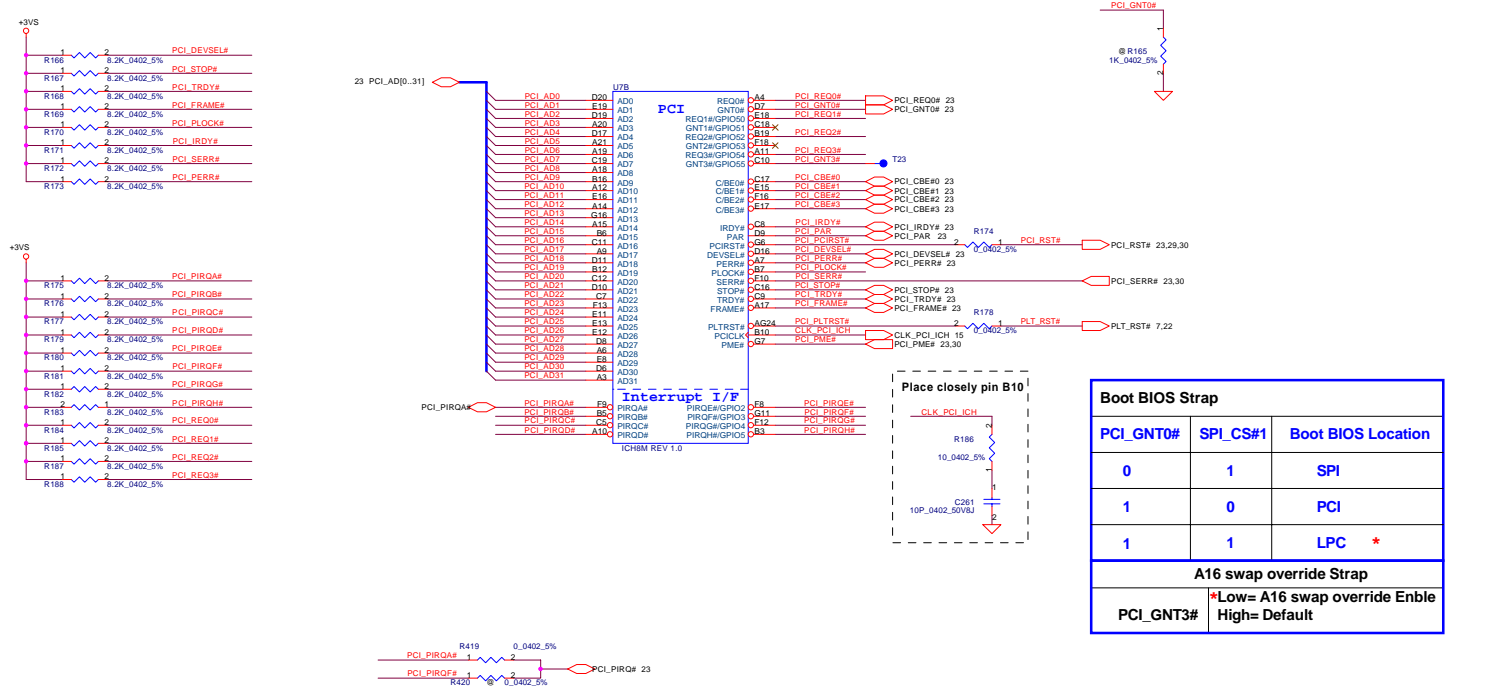


LVDS connector
 ACES_86242-4001
 CONNR
 880P_0402_50V7K
 680P_0402_50V7K
 C255
 680P_0402_50V7K
 C256
 680P_0402_50V7K
 WCM-2012-900T_4P
 L23
 USB20_P6 20
 USB20_N6 20
 ACES_86242-4001 40P P1
 ACES_86242-4001_40P

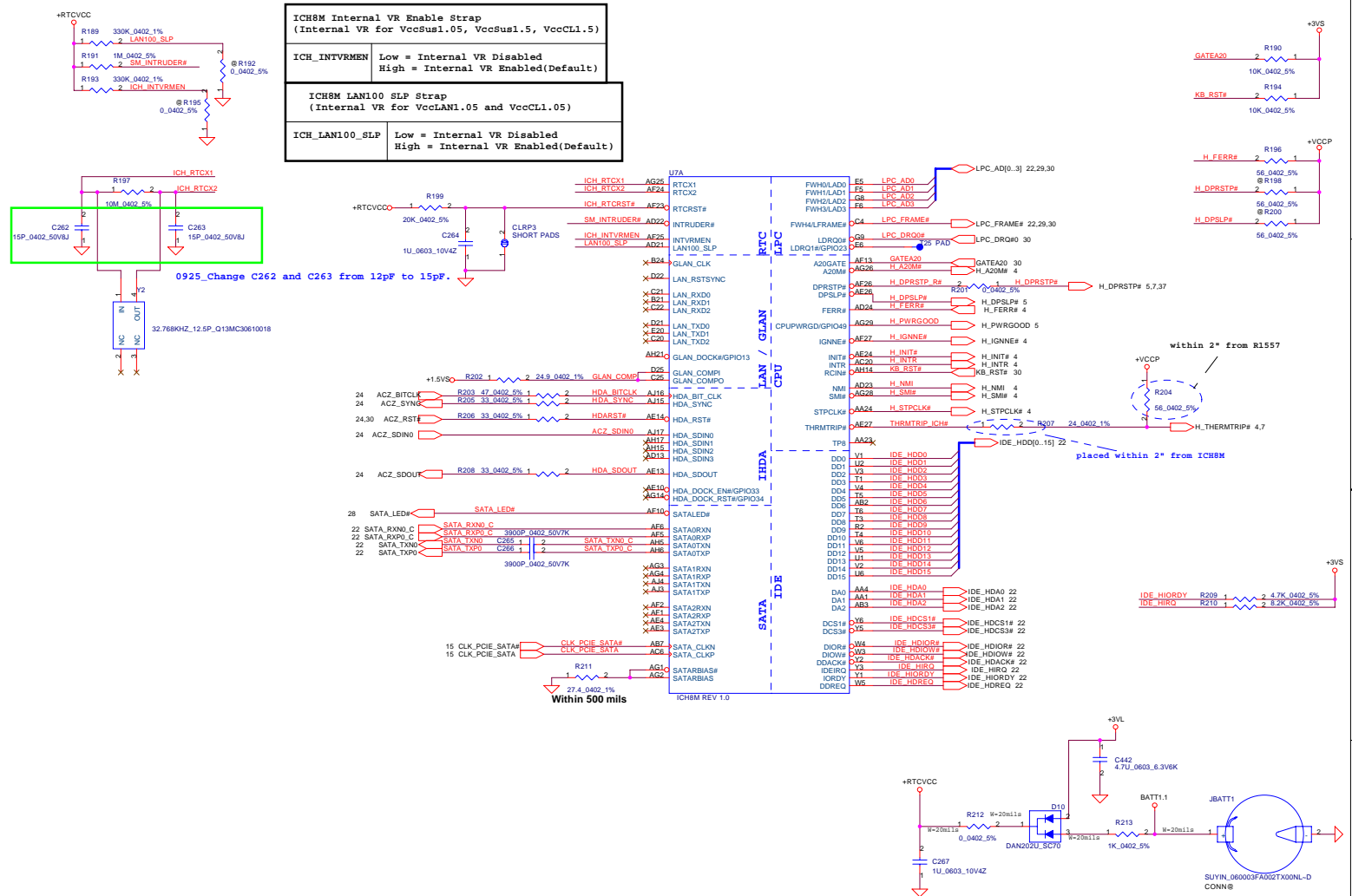


Avoid Panel display garbage after power on.

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Issued Date	2007/03/26	Deciphered Date	2006/07/26	LCD CONN.	
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Size	Document Number	Rev		Date	
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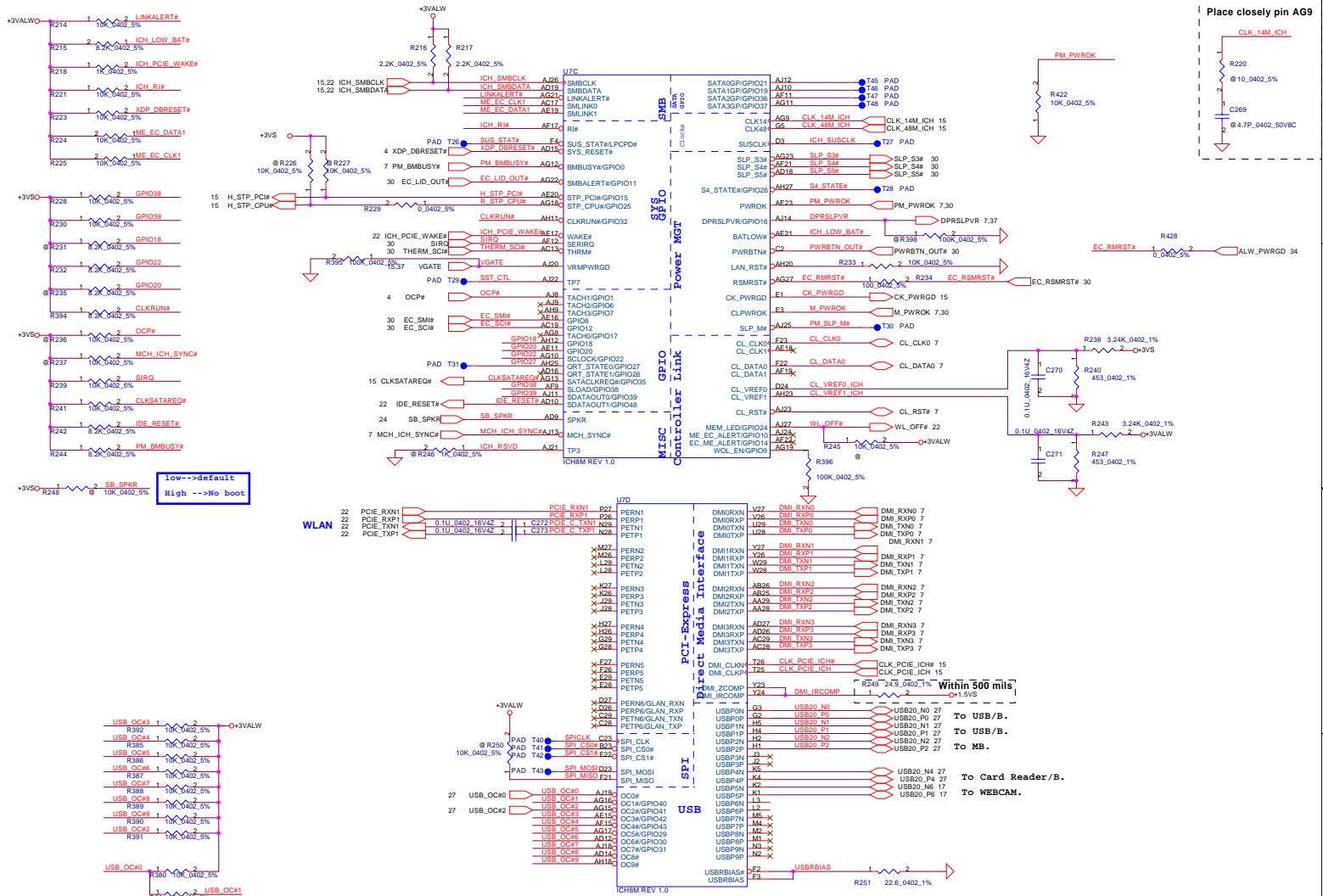


Security Classification		Compal Secret Data		Title	
Issued Date	2007/03/26	Deciphered Date	2006/03/10	Compal Electronics, Inc.	
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					LA-4031P
Date: Wednesday, October 24, 2007				Sheet	18 of 42

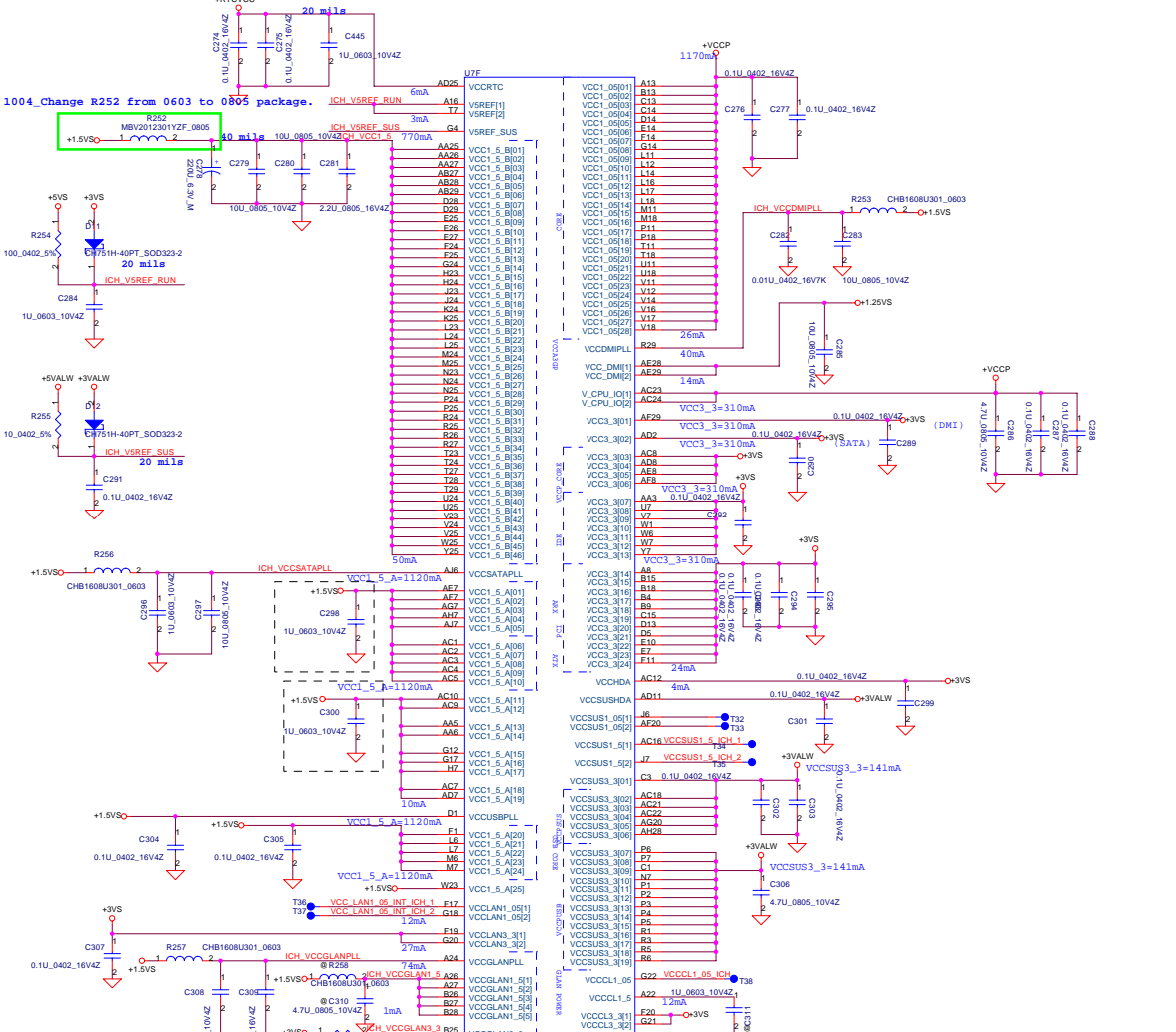


ICH8M Internal VR Enable Strap (Internal VR for VccSua1.05, VccSua1.5, VccCLL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)
ICH8M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCLL1.05)	
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)

Security Classification		Compal Secret Data		Title	
Issued Date	2007/03/26	Deciphered Date	2006/03/10	ICH8(2/4) LAN,HD,IDE,LPC	
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Size	Document Number	Customer	Rev	Date	
18	LA-4031P		1.0	Wednesday, October 24, 2007 11:42 AM	



Security Classification	Compal Secret Data		Title
Issued Date	2007/03/26	Deciphered Date	2006/03/10
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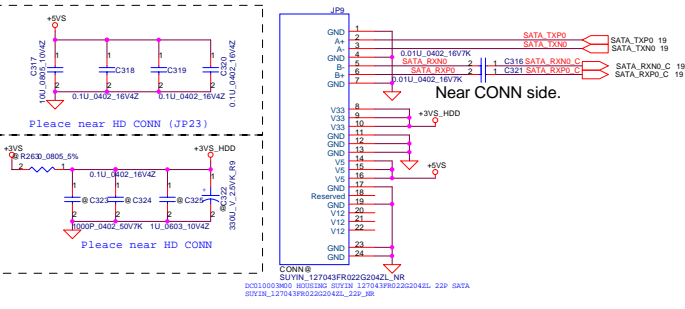


UTE		K7
AC	VSS(001)	VSS(001)
AA2	VSS(003)	VSS(003)
AA7	VSS(006)	VSS(006)
AA5	VSS(005)	VSS(005)
AB1	VSS(008)	VSS(008)
AB24	VSS(009)	VSS(009)
AC11	VSS(010)	VSS(010)
AC14	VSS(011)	VSS(011)
AC5	VSS(012)	VSS(012)
AC6	VSS(013)	VSS(013)
AC27	VSS(014)	VSS(014)
AD17	VSS(015)	VSS(015)
AD20	VSS(016)	VSS(016)
AD3	VSS(017)	VSS(017)
AD4	VSS(018)	VSS(018)
AD6	VSS(019)	VSS(019)
AE1	VSS(020)	VSS(020)
AE12	VSS(021)	VSS(021)
AE22	VSS(022)	VSS(022)
AE1	VSS(023)	VSS(023)
AE25	VSS(024)	VSS(024)
AE3	VSS(025)	VSS(025)
AE9	VSS(026)	VSS(026)
AE10	VSS(027)	VSS(027)
AF4	VSS(028)	VSS(028)
AF18	VSS(029)	VSS(029)
AF3	VSS(030)	VSS(030)
AF3	VSS(031)	VSS(031)
AF4	VSS(032)	VSS(032)
AG5	VSS(033)	VSS(033)
AG6	VSS(034)	VSS(034)
AH10	VSS(035)	VSS(035)
AH13	VSS(036)	VSS(036)
AH8	VSS(037)	VSS(037)
AH9	VSS(038)	VSS(038)
AH11	VSS(039)	VSS(039)
AH12	VSS(040)	VSS(040)
AH2	VSS(041)	VSS(041)
AH22	VSS(042)	VSS(042)
AH24	VSS(043)	VSS(043)
AH28	VSS(044)	VSS(044)
AH4	VSS(045)	VSS(045)
AH6	VSS(046)	VSS(046)
AH7	VSS(047)	VSS(047)
AH3	VSS(048)	VSS(048)
B14	VSS(049)	VSS(049)
B17	VSS(050)	VSS(050)
AEB	VSS(051)	VSS(051)
B22	VSS(052)	VSS(052)
B20	VSS(053)	VSS(053)
B2	VSS(054)	VSS(054)
BB	VSS(055)	VSS(055)
C2	VSS(056)	VSS(056)
C26	VSS(057)	VSS(057)
C27	VSS(058)	VSS(058)
CD	VSS(059)	VSS(059)
D12	VSS(060)	VSS(060)
D15	VSS(061)	VSS(061)
D18	VSS(062)	VSS(062)
DL	VSS(063)	VSS(063)
EA	VSS(064)	VSS(064)
E24	VSS(065)	VSS(065)
E4	VSS(066)	VSS(066)
E3	VSS(067)	VSS(067)
F15	VSS(068)	VSS(068)
F28	VSS(069)	VSS(069)
F3	VSS(070)	VSS(070)
F7	VSS(071)	VSS(071)
G1	VSS(072)	VSS(072)
G2	VSS(073)	VSS(073)
G10	VSS(074)	VSS(074)
G13	VSS(075)	VSS(075)
G19	VSS(076)	VSS(076)
G23	VSS(077)	VSS(077)
G25	VSS(078)	VSS(078)
G28	VSS(079)	VSS(079)
G38	VSS(080)	VSS(080)
G37	VSS(081)	VSS(081)
H25	VSS(082)	VSS(082)
H29	VSS(083)	VSS(083)
H2	VSS(084)	VSS(084)
H5	VSS(085)	VSS(085)
H8	VSS(086)	VSS(086)
J25	VSS(087)	VSS(087)
J27	VSS(088)	VSS(088)
J4	VSS(089)	VSS(089)
K23	VSS(090)	VSS(090)
K28	VSS(091)	VSS(091)
K29	VSS(092)	VSS(092)
K3	VSS(093)	VSS(093)
K6	VSS(094)	VSS(094)
KA	VSS(095)	VSS(095)
KB	VSS(096)	VSS(096)
LC	VSS(097)	VSS(097)
LC	VSS(098)	VSS(098)
LA	VSS(099)	VSS(099)
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LA	VSS(122)	VSS(122)
LA	VSS(123)	VSS(123)
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LA	VSS(128)	VSS(128)
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LA	VSS(130)	VSS(130)
LA	VSS(131)	VSS(131)
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LA	VSS(133)	VSS(133)
LA	VSS(134)	VSS(134)
LA	VSS(135)	VSS(135)
LA	VSS(136)	VSS(136)
LA	VSS(137)	VSS(137)
LA	VSS(138)	VSS(138)
LA	VSS(139)	VSS(139)
LA	VSS(140)	VSS(140)
LA	VSS(141)	VSS(141)
LA	VSS(142)	VSS(142)
LA	VSS(143)	VSS(143)
LA	VSS(144)	VSS(144)
LA	VSS(145)	VSS(145)
LA	VSS(146)	VSS(146)
LA	VSS(147)	VSS(147)
LA	VSS(148)	VSS(148)
LA	VSS(149)	VSS(149)
LA	VSS(150)	VSS(150)
LA	VSS(151)	VSS(151)
LA	VSS(152)	VSS(152)
LA	VSS(153)	VSS(153)
LA	VSS(154)	VSS(154)
LA	VSS(155)	VSS(155)
LA	VSS(156)	VSS(156)
LA	VSS(157)	VSS(157)
LA	VSS(158)	VSS(158)
LA	VSS(159)	VSS(159)
LA	VSS(160)	VSS(160)
LA	VSS(161)	VSS(161)
LA	VSS(162)	VSS(162)
LA	VSS(163)	VSS(163)
LA	VSS(164)	VSS(164)
LA	VSS(165)	VSS(165)
LA	VSS(166)	VSS(166)
LA	VSS(167)	VSS(167)
LA	VSS(168)	VSS(168)
LA	VSS(169)	VSS(169)
LA	VSS(170)	VSS(170)
LA	VSS(171)	VSS(171)
LA	VSS(172)	VSS(172)
LA	VSS(173)	VSS(173)
LA	VSS(174)	VSS(174)
LA	VSS(175)	VSS(175)
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LA	VSS(200)	VSS(200)

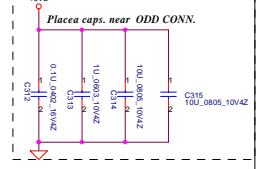
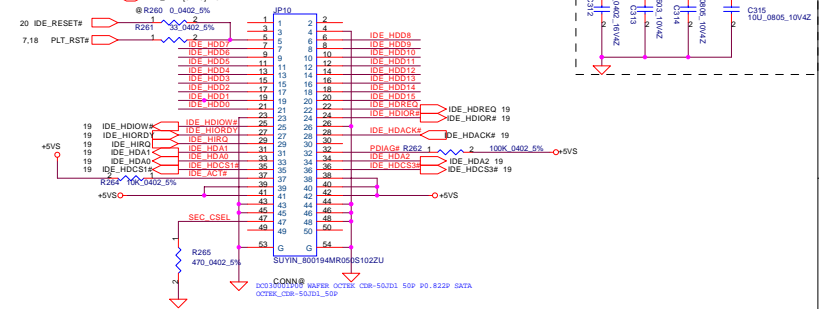
ICH8M REV 1.0

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Compal Secret Data	2007/03/26	2006/03/10	ICH8(4) POWER&GND
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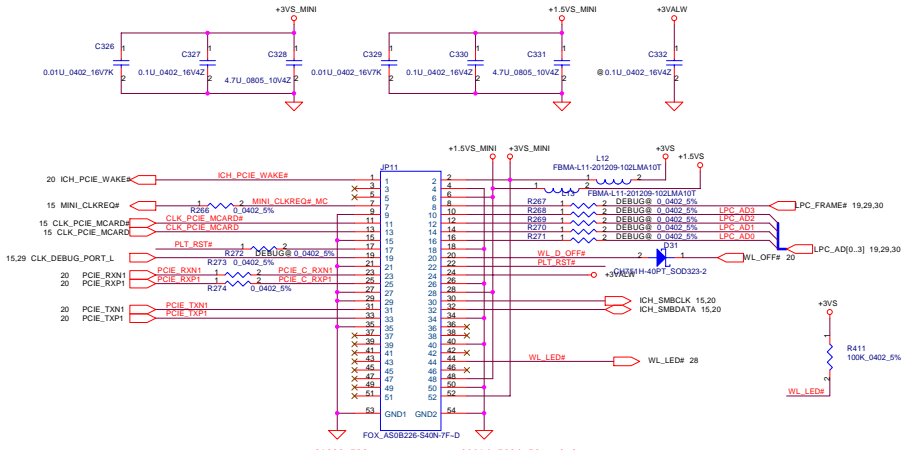
HDD Connector



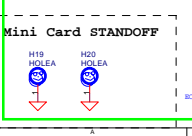
CD-ROM Connector



Mini-Express Card---WLAN

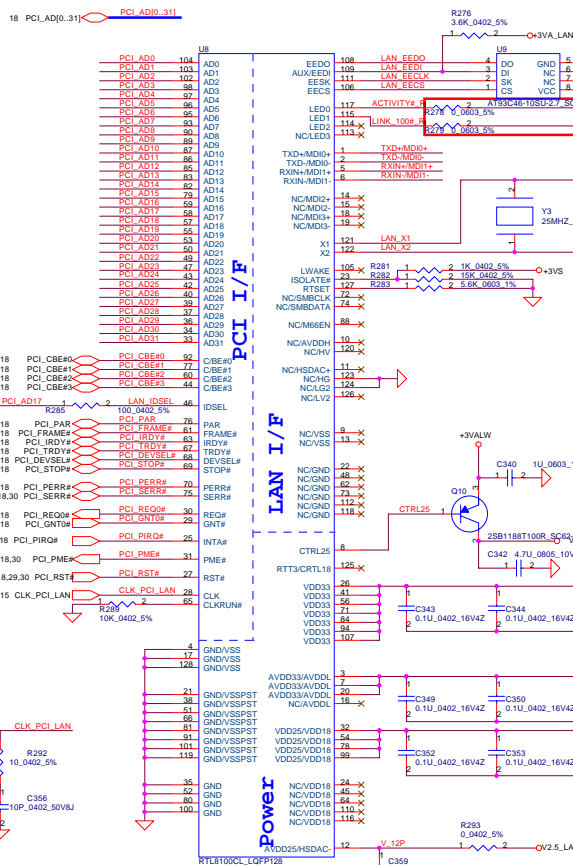
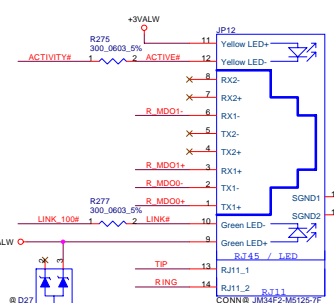
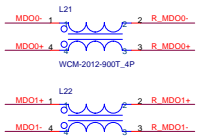


7/13 Update HX footprint



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				LA-4031P	
				Date	Wednesday, October 24, 2007
				Sheet	22 of 42

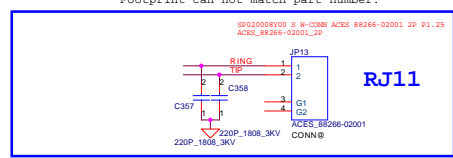
Close to JP12.



For RMI, locate close to LAN chip

close to chip

close to magnetic



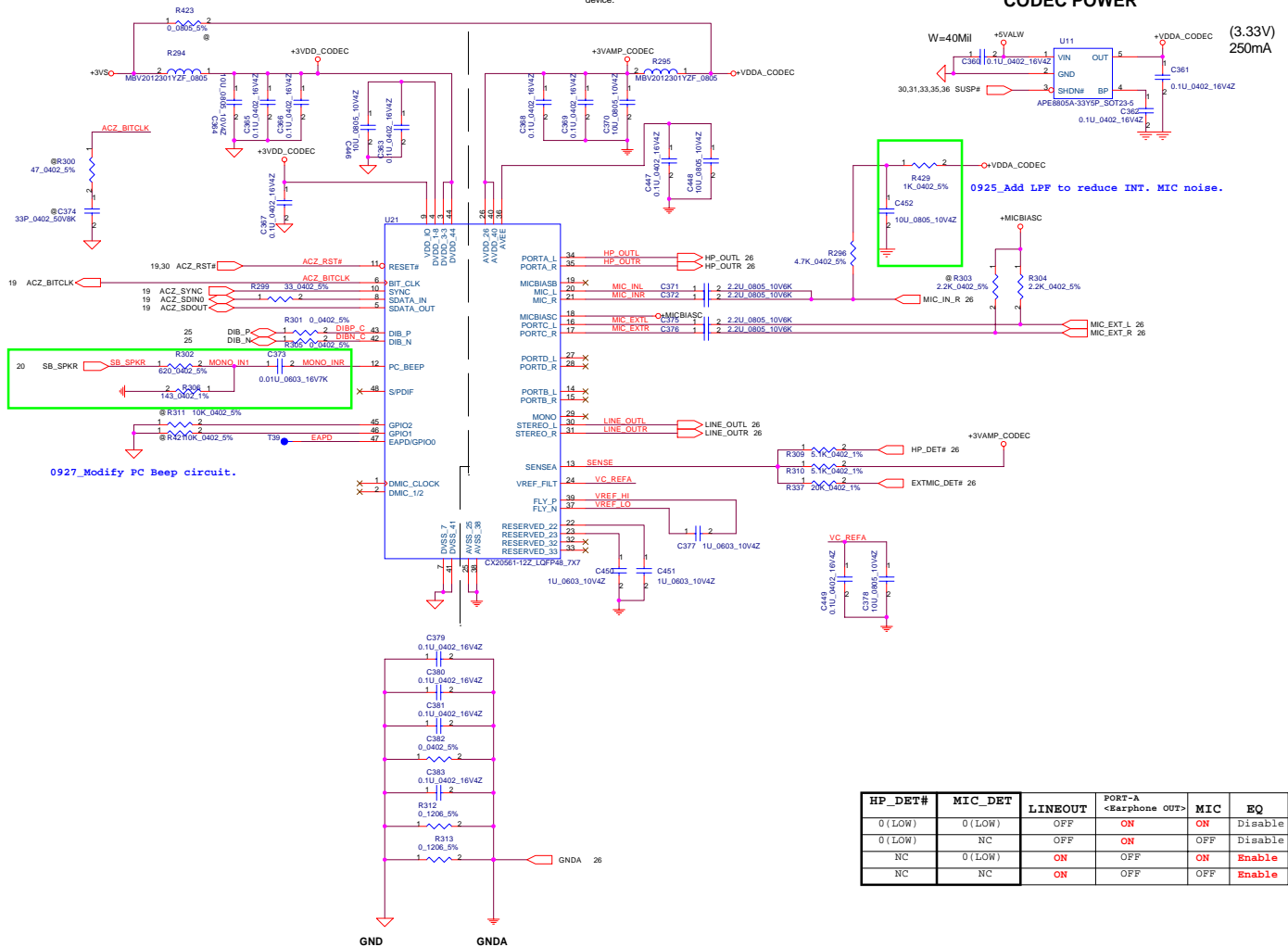
Security Classification		Compal Secret Data		Title	
Issued Date	2007/03/26	Deciphered Date	2007/08/29	LAN-8100CL	
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In order for the modem wake on ring feature to function, the CODEC must be powered by a rail that is not removed when the system is in standby.

AUDIO CODEC

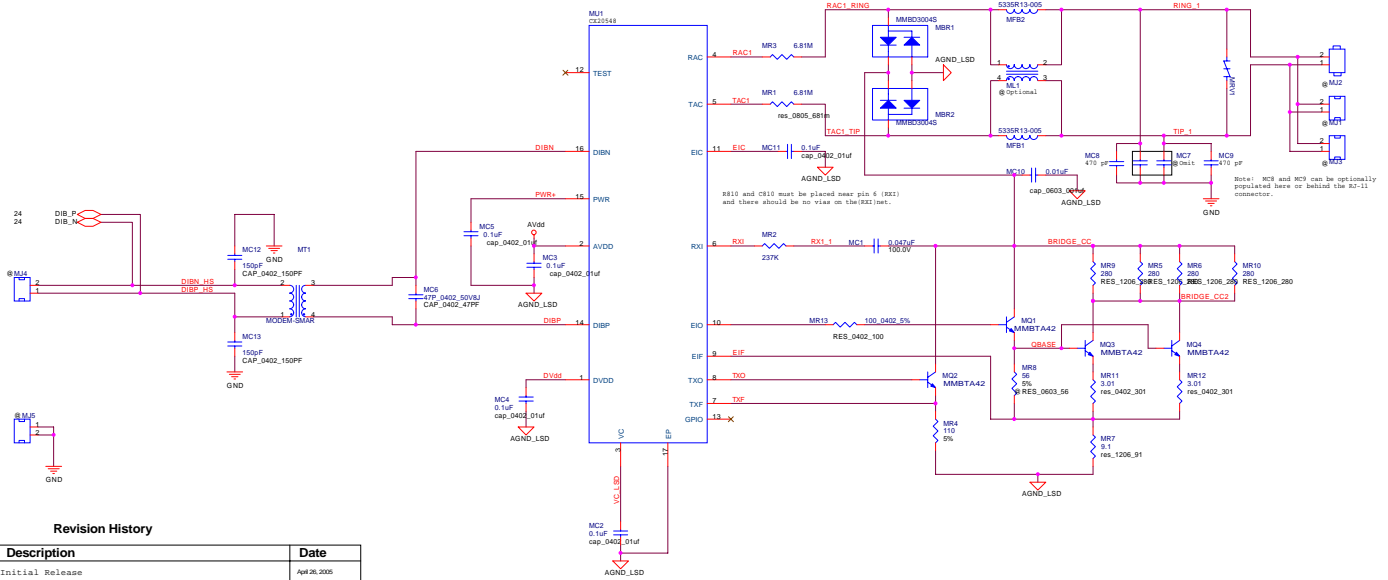
For Layout:
Place decoupling caps near the power pins of SmartAMC device.

CODEC POWER



HP_DET#	MIC_DET	LINEOUT	PORT-A <Earphone OUT>	MIC	EQ
0 (LOW)	0 (LOW)	OFF	ON	ON	Disable
0 (LOW)	NC	OFF	ON	OFF	Disable
NC	0 (LOW)	ON	OFF	ON	Enable
NC	NC	ON	OFF	OFF	Enable

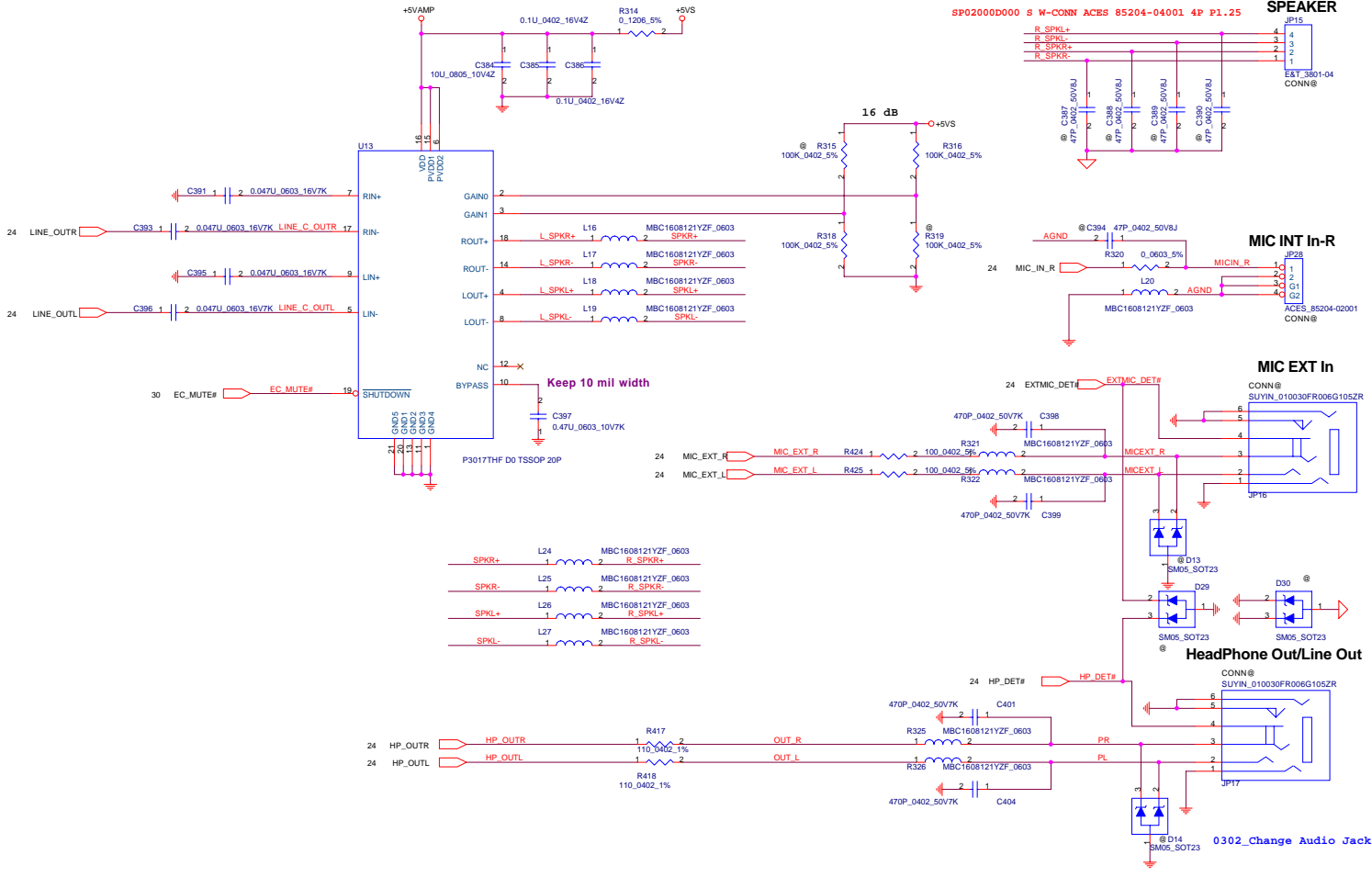
Security Classification		Compal Secret Data		Title		Compal Electronics, Inc.	
Issued Date	2007/03/26	Deciphered Date	2006/03/10	Size	Document Number		Rev
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				Date	Wednesday, October 24, 2007	Sheet	24 of 42



Revision History

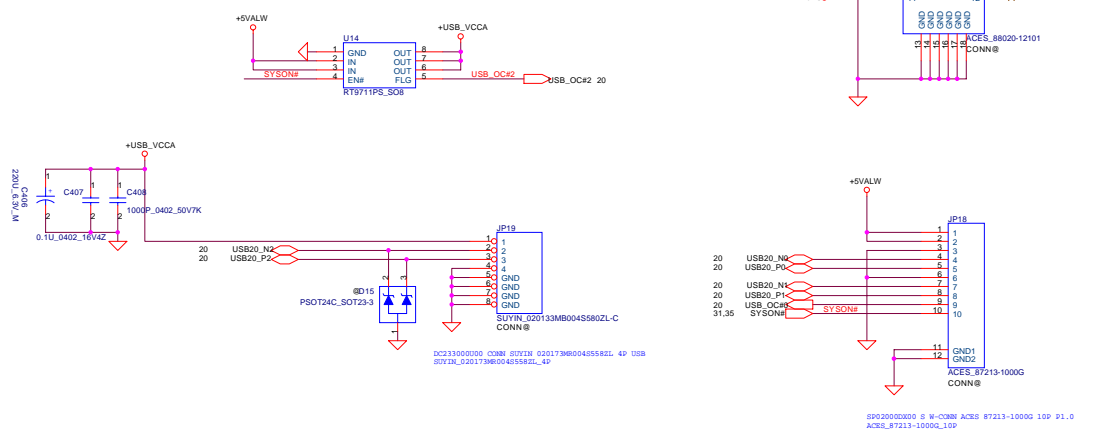
REV	Description	Date
0	Initial Release	April 26, 2005
1	No changes to schematic. PCB updated to -003. Updated footprints and corrected via spacing errors.	April 18, 2005
2	Changed MC8 and MC9 pads. No schematic changes. PCB updated to -005.	November 3, 2005
3	Added MR11 and MR12. PCB updated to -007.	November 18, 2005
4	Added MR13. PCB updated to -009.	January 3, 2006
4.01	AVL update only.	April 20, 2006

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<p>AMOM-CX20548</p>			Rev 1.0
<p>LA-401P</p>			Date: Wednesday, October 24, 2007 Sheet 25 of 42



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Date	Wednesday, October 24, 2007	Sheet	26	of 42

USB Port

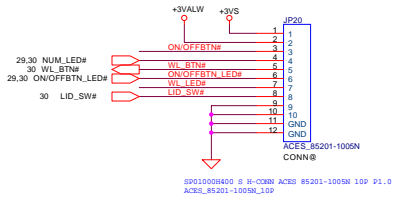


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				Document Number
				LA-403P
				Rev
				1.0
				Date
				Wednesday, October 24, 2007
				Sheet
				27 of 42

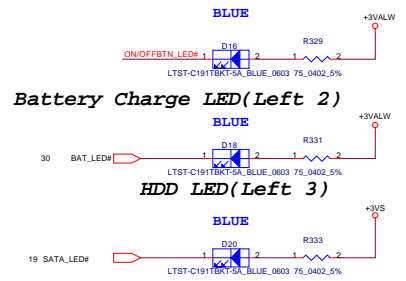
1015_Remove U22 and U23.



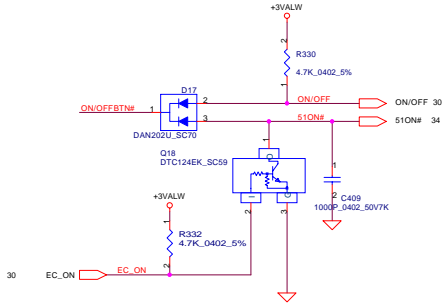
M/BtoS/B



POWER LED(Left 1)

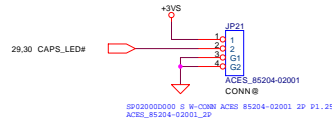


Power ON/OFF

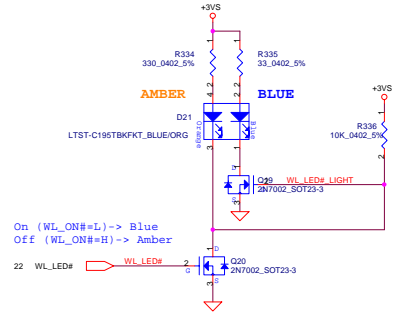


0426_Change all LED power source from 5V to 3V.

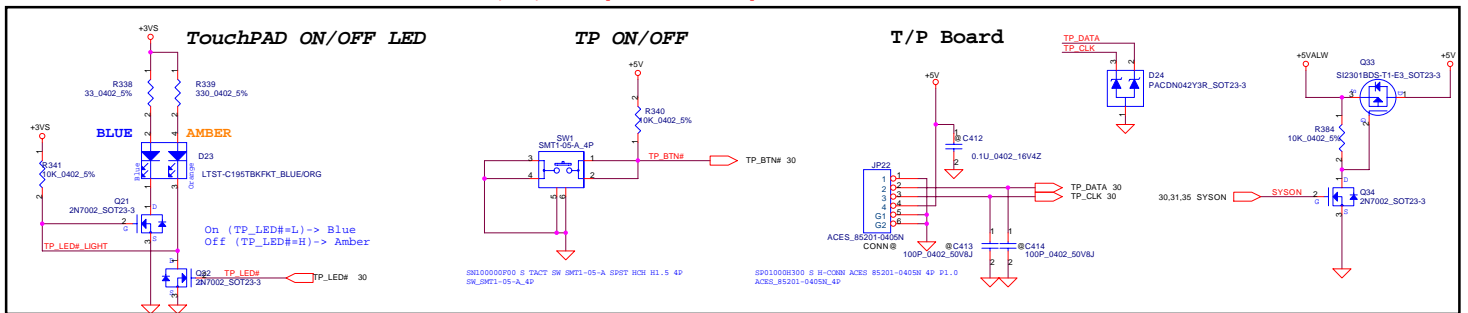
M/B to SB(Caps Lock LED)



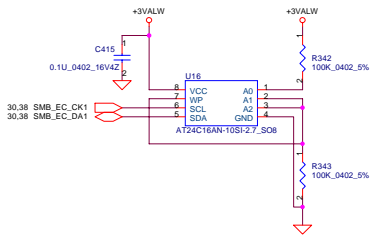
Wireless ON/OFF LED(Left 4)



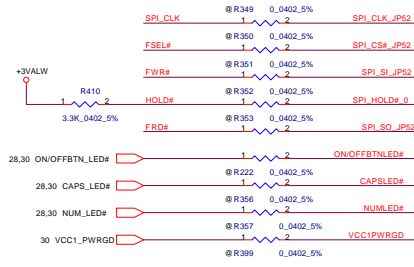
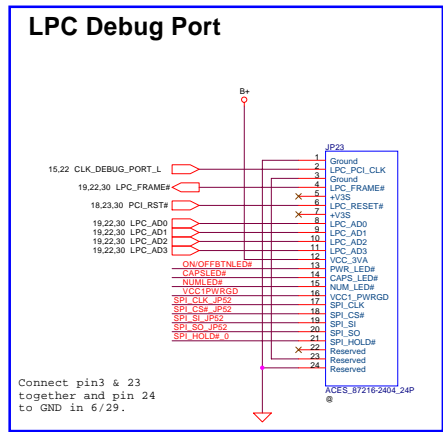
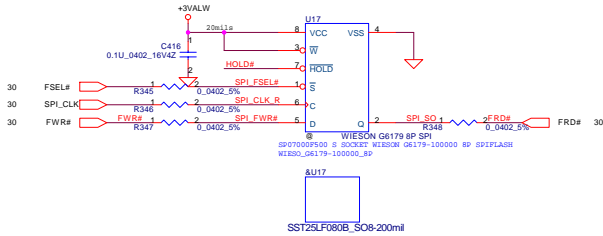
D21, D25, D23 Footprint can not match part number.



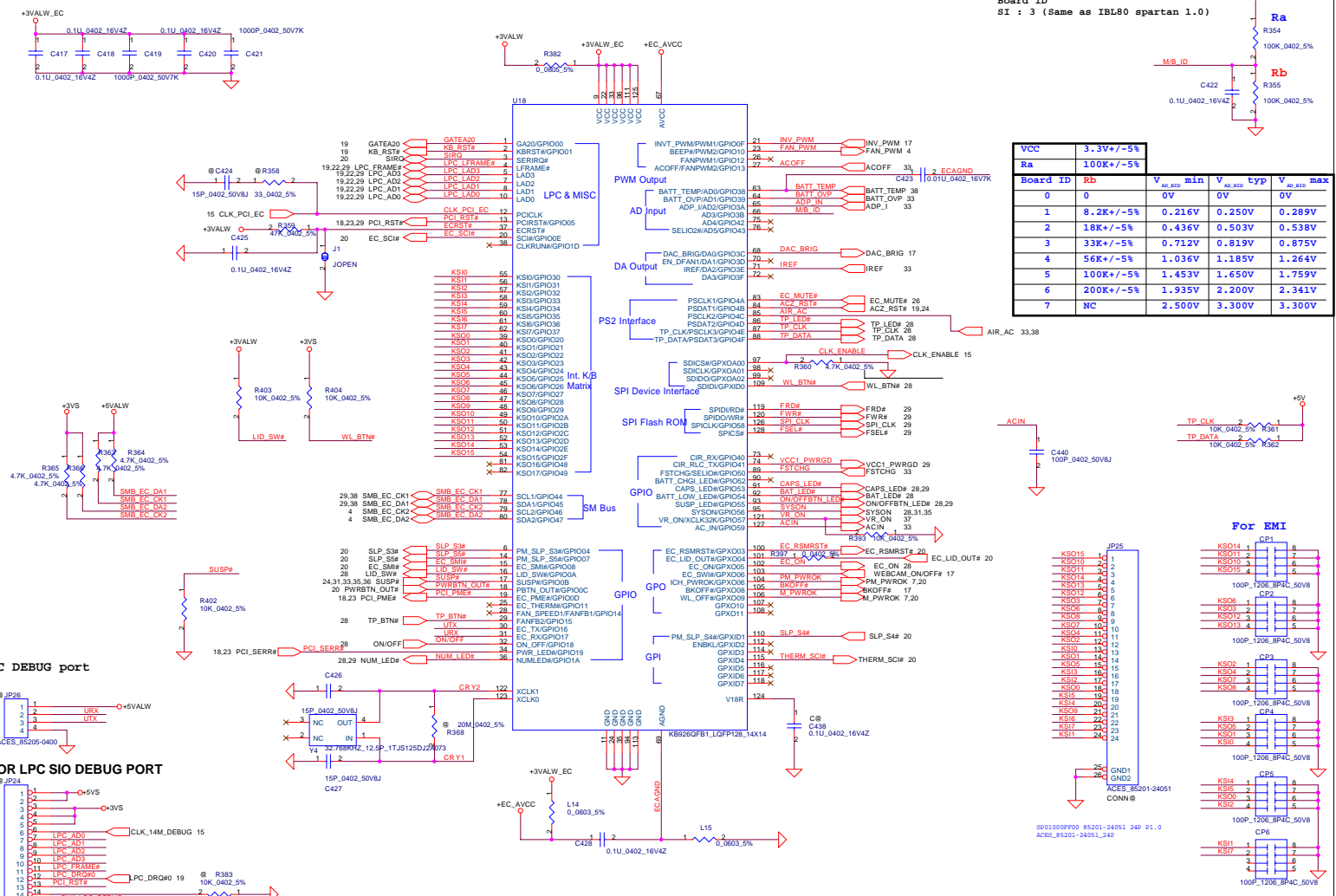
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/03/26	Deciphered Date	2006/07/26	Title
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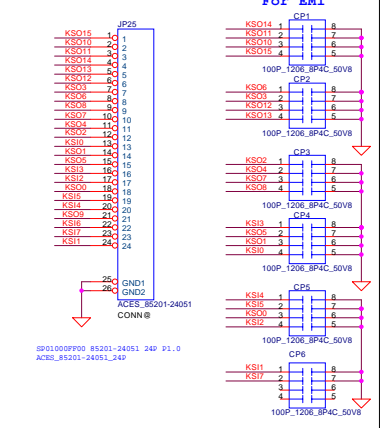
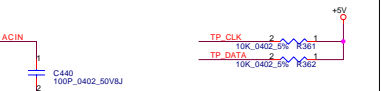
SPI ROM



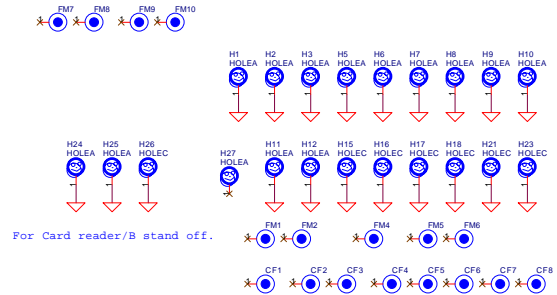
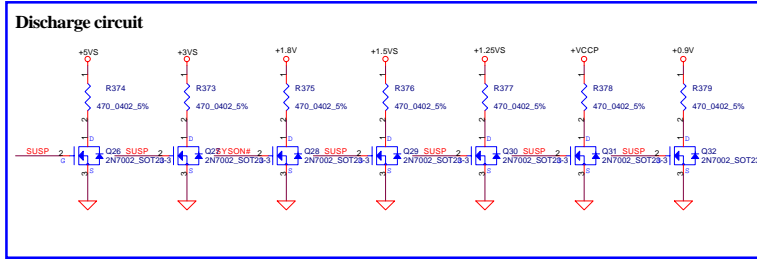
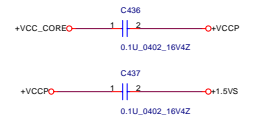
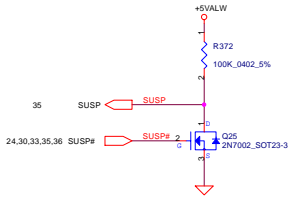
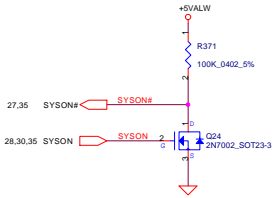
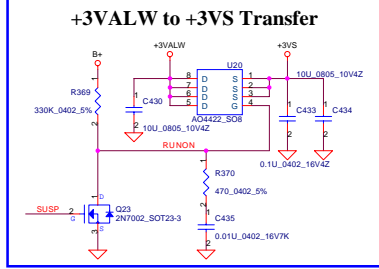
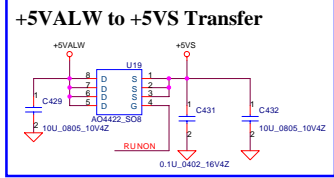
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Date	Wednesday, October 24, 2007	Sheet	29	of 42



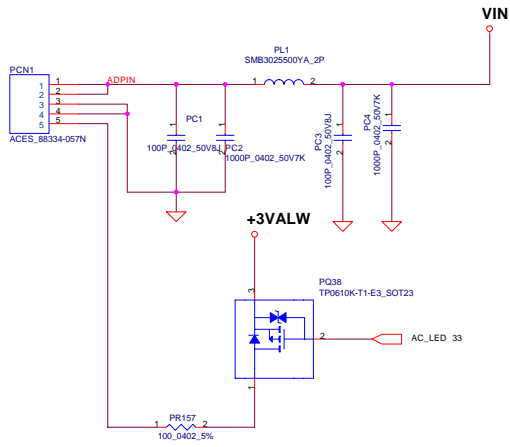
VCC	3.3V+/-5%			
Ra	100K+/-5%			
Board ID	Rb	V _{AD_MIN}	V _{AD_TYP}	V _{AD_MAX}
0	0	0V	0V	0V
1	8.2K+/-5%	0.216V	0.250V	0.289V
2	1.8K+/-5%	0.436V	0.503V	0.538V
3	33K+/-5%	0.712V	0.819V	0.875V
4	56K+/-5%	1.036V	1.185V	1.264V
5	100K+/-5%	1.453V	1.650V	1.759V
6	200K+/-5%	1.935V	2.200V	2.341V
7	NC	2.500V	3.300V	3.300V



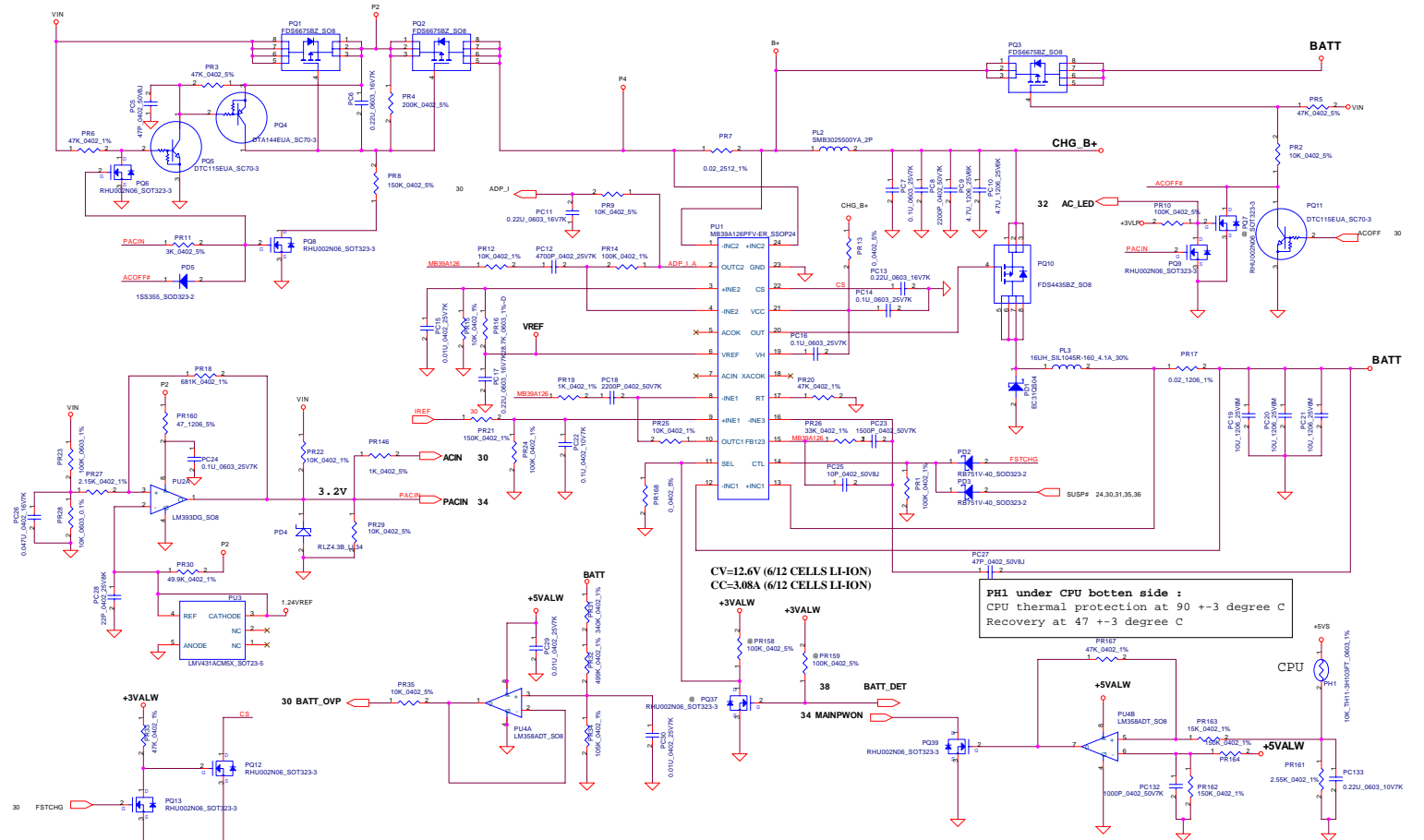
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Size	Document Number	LA-4031P		Rev	1.0
Date	Wednesday, October 24, 2007	Sheet	31	of	42



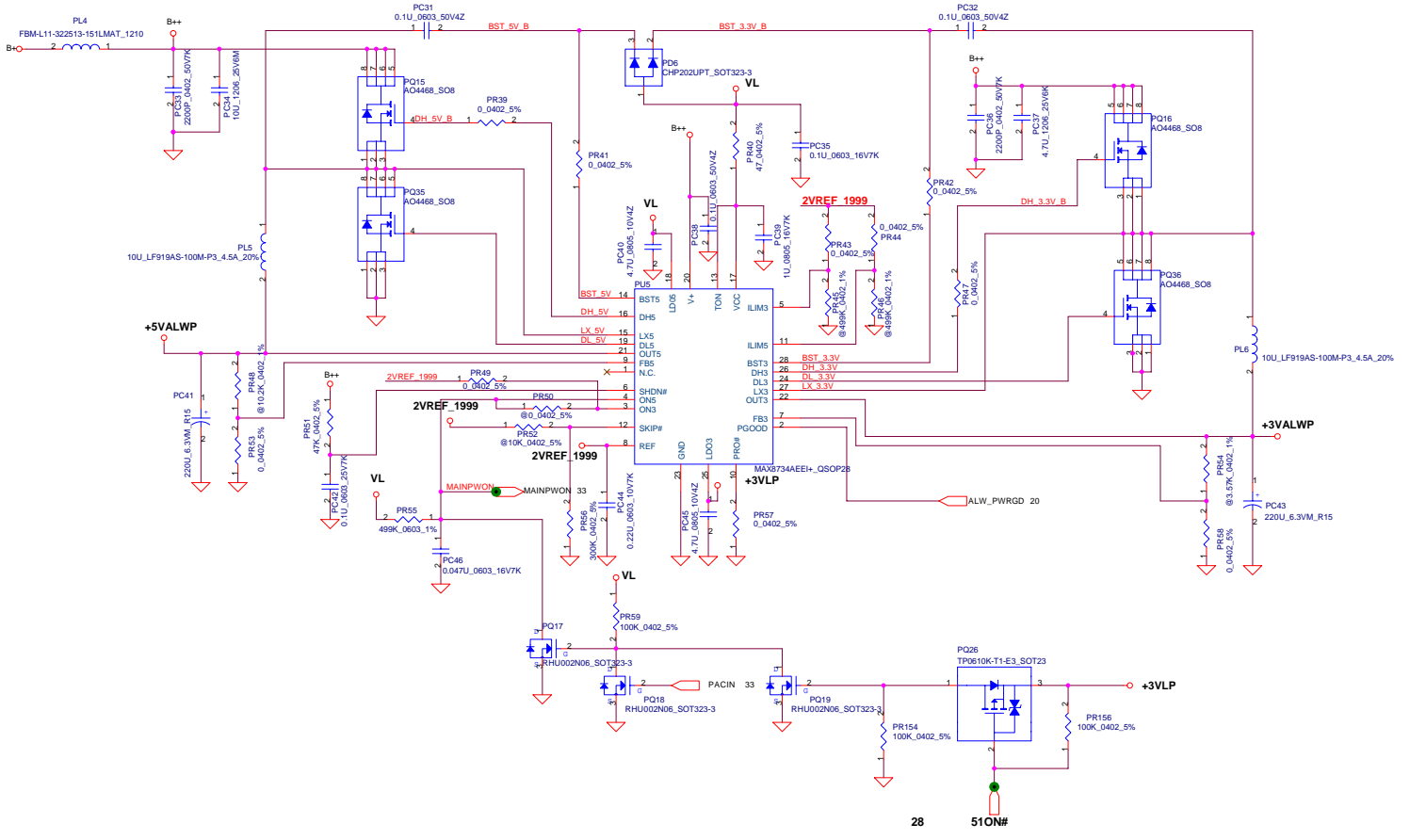
Security Classification	Compal Secret Data			Title
Issued Date	<Issued_Date>	Deciphered Date	<Deciphered_Date>	DC CONN
<small>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</small>				Document Number LA-4031P
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PH1 under CPU bottom side :
 CPU thermal protection at 90 +/-3 degree C
 Recovery at 47 +/-3 degree C

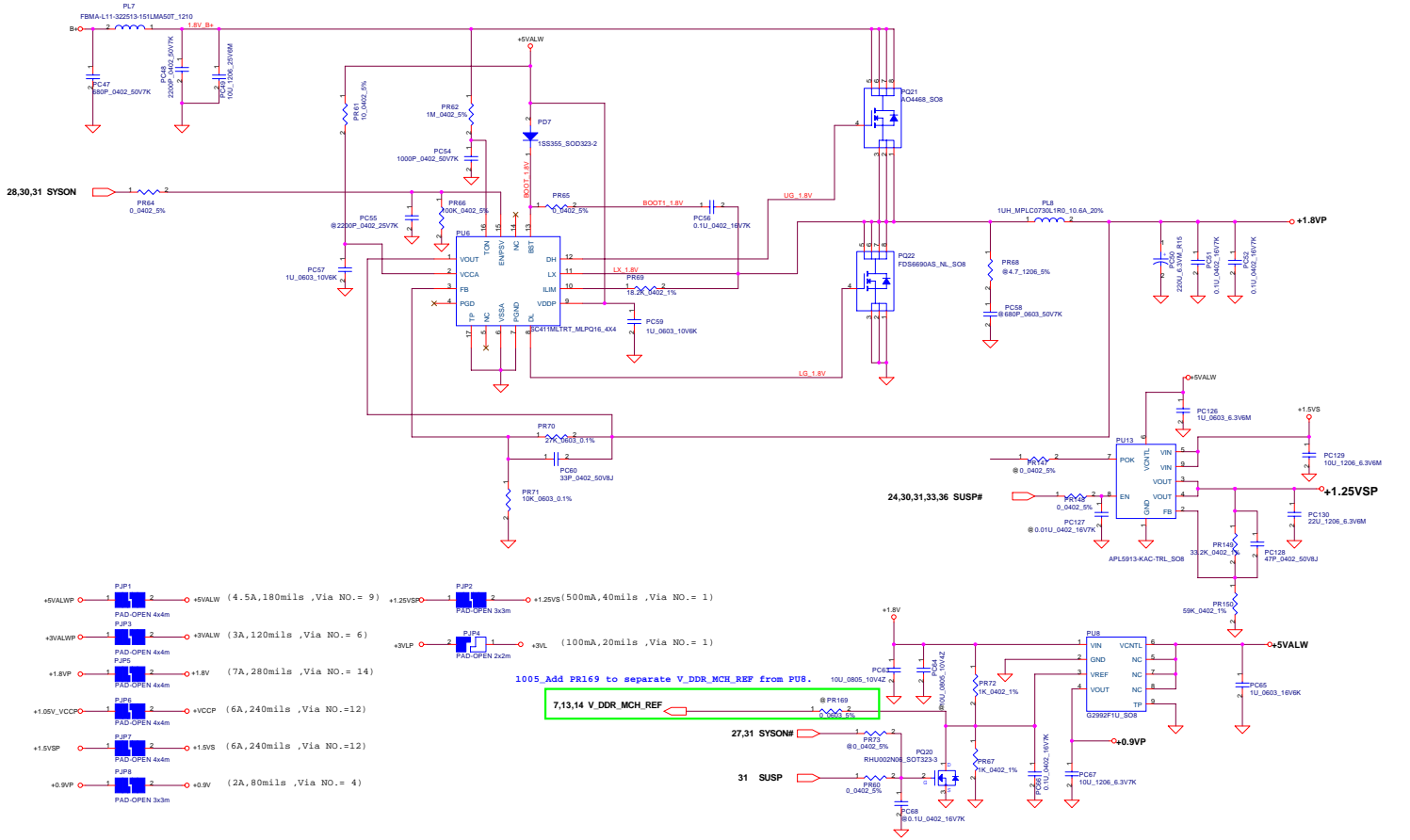
CV=12.6V (6/12 CELLS LI-ION)
 CC=3.08A (6/12 CELLS LI-ION)

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DATE	WSP20150714	DESIGNER	CS



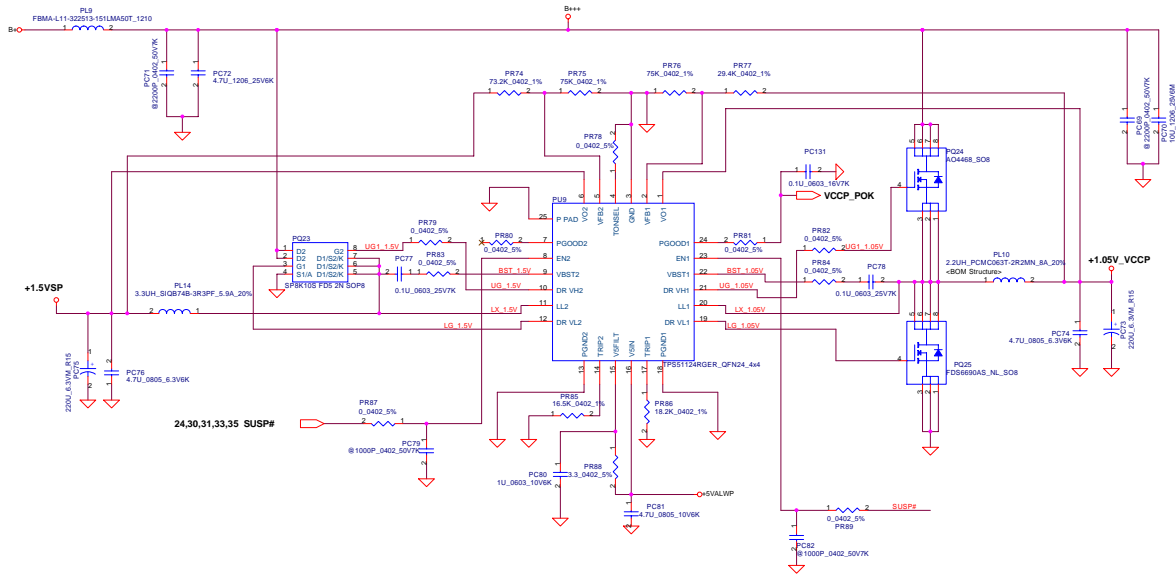
28 510N#

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Date	Wednesday, October 24, 2007	Sheet	34	of 42

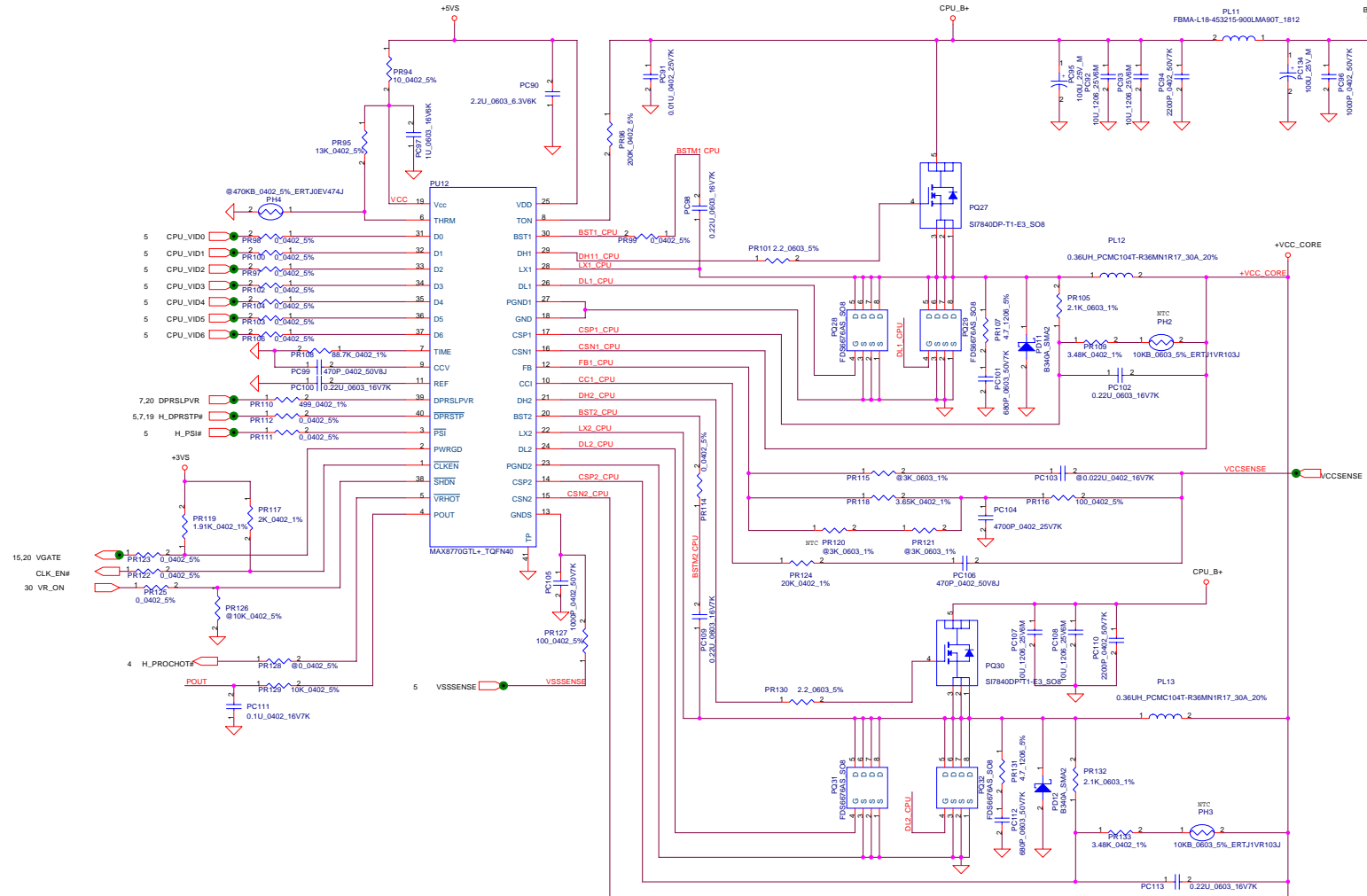


- +SVALW PUS1 2 +SVALW (4.5A,180mils ,Via NO.= 9)
- +SVALW PUS2 2 +SVALW (3A,120mils ,Via NO.= 6)
- +1.8VP PUS3 2 +1.8V (7A,280mils ,Via NO.= 14)
- +1.05V_VCCP PUS4 2 +VCCP (6A,240mils ,Via NO.=12)
- +1.5VSP PUS5 2 +1.5VS (6A,240mils ,Via NO.=12)
- +0.9VP PUS6 2 +0.9V (2A,80mils ,Via NO.= 4)
- +1.25VSP PUS7 2 +1.25VS (500mA,40mils ,Via NO.= 1)
- +3VLP PUS8 1 +3VL (100mA,20mils ,Via NO.= 1)

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Date	Wednesday, October 28, 2009	Issue	35	of	49

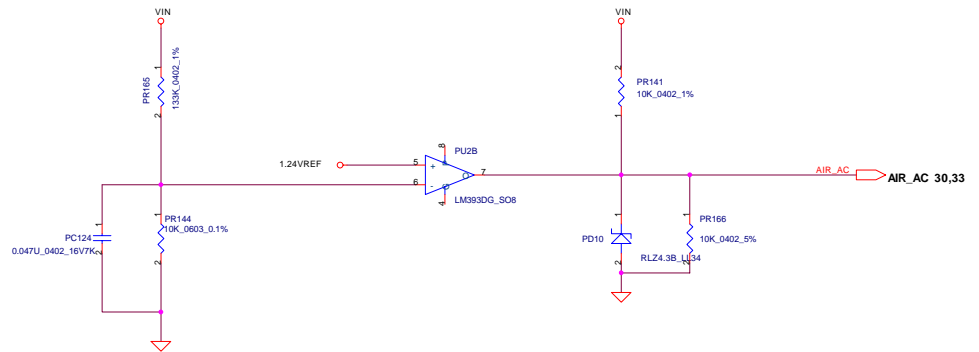
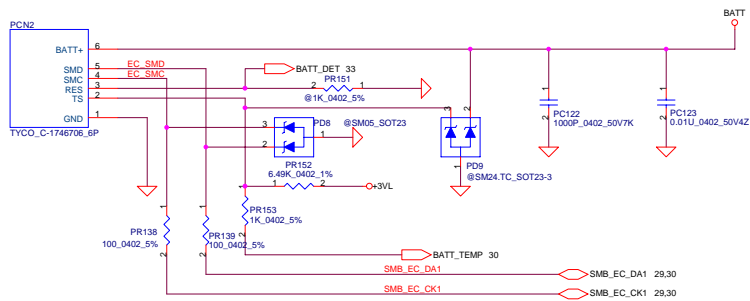


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Item	Reason for change	PG#	Modify List	Date	Phase
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14					

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				Date: Wednesday, October 24, 2007

Version Change List (P. I. R. List) for HW Circuit

Item	Change item	Page	Date	Phase
1	Change R296 2.2K to 4.7K and Reserved R303	24	8/6	SI-->PV
2	Add R424 R425 100ohm on MIC_EXT_R and MIC_EXT_L	26	8/6	SI-->PV
3	Fine tune R298 C260 value	17	8/6	SI-->PV
4	Change PIRQ from F to A	18	8/14	SI-->PV
5	Connect PCI_SERR# to EC GPIO pin.	18	8/31	SI-->PV
6	Modify PC BEEP circuit.	20	8/31	SI-->PV
7	For support Intel Penryn CPU.	04	9/3	SI-->PV
8	For ESD request.	28	9/3	SI-->PV
9	For EMI request.	26	9/5	SI-->PV
10	Change C391, C393, C395, C396 from 0.47uF to 0.047uF.	26	9/7	SI-->PV
11	Add R417 and R418 to fine-tune Vp-p.	26	9/7	SI-->PV
12	For ESD request.	20	9/7	SI-->PV
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Version Change List (P. I. R. List) for HW Circuit

Item	Change item	Page	Date	Phase
1	Solve Vref miss when entry S3 mode.	7	9/25	PV-->MV
2	Solve wave ripple on CRT and TV.	10	9/25	PV-->MV
3	Solve RTC timing too exceed.	18	9/25	PV-->MV
4	Reduce INT_MIC noise.	24	9/25	PV-->MV
5	Solve S3 resume fail when use Micron DDR module.	35	10/05	PV-->MV
6	Solve pop noise when entry or resume from S3.	24	9/27	PV-->MV
7	Solve EMI fail for Memory module.	7	9/27	PV-->MV
8	ICH 1.5V power rail 700mA current requirement.	21	10/04	PV-->MV
9	Remove U22 and U23.	28	10/15	PV-->MV
10	For EMI request.	16	10/15	PV-->MV
11	To avoid too easy to open solder for CLRP2.	15	10/15	PV-->MV
12	Solve acoustic noise issue.	10	10/22	PV-->MV
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