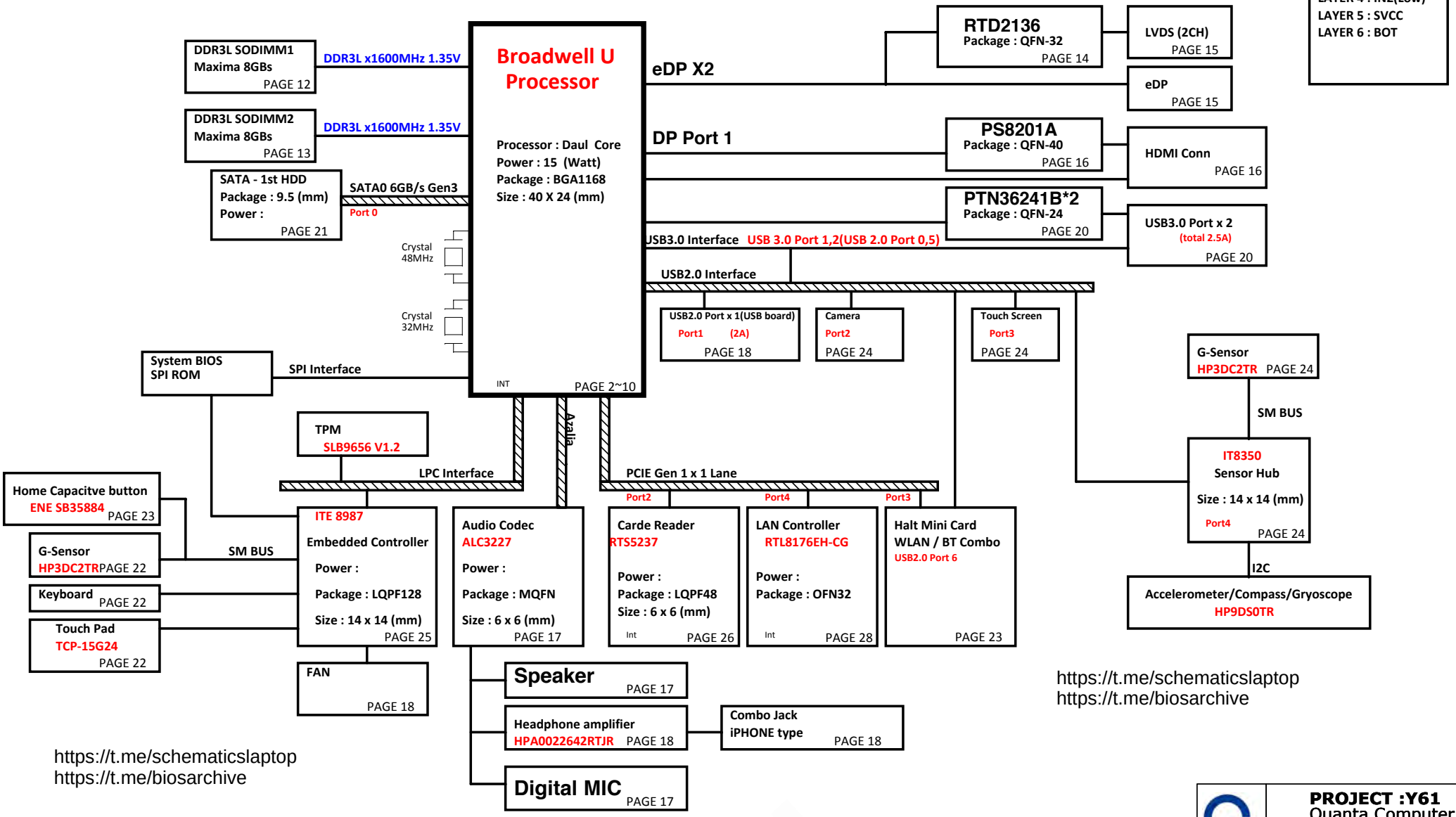
13"/15"
Y61 Intel Cresent Bay ULT Platform Block Diagram

PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT

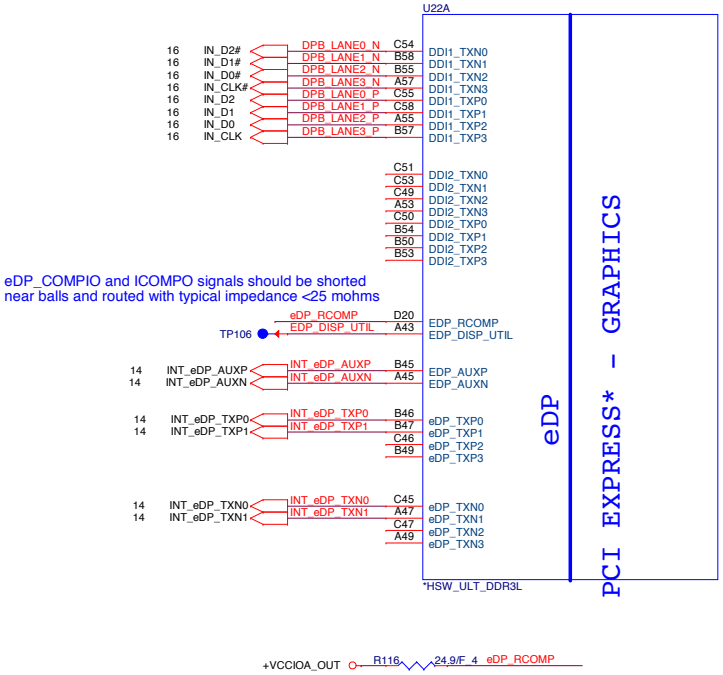


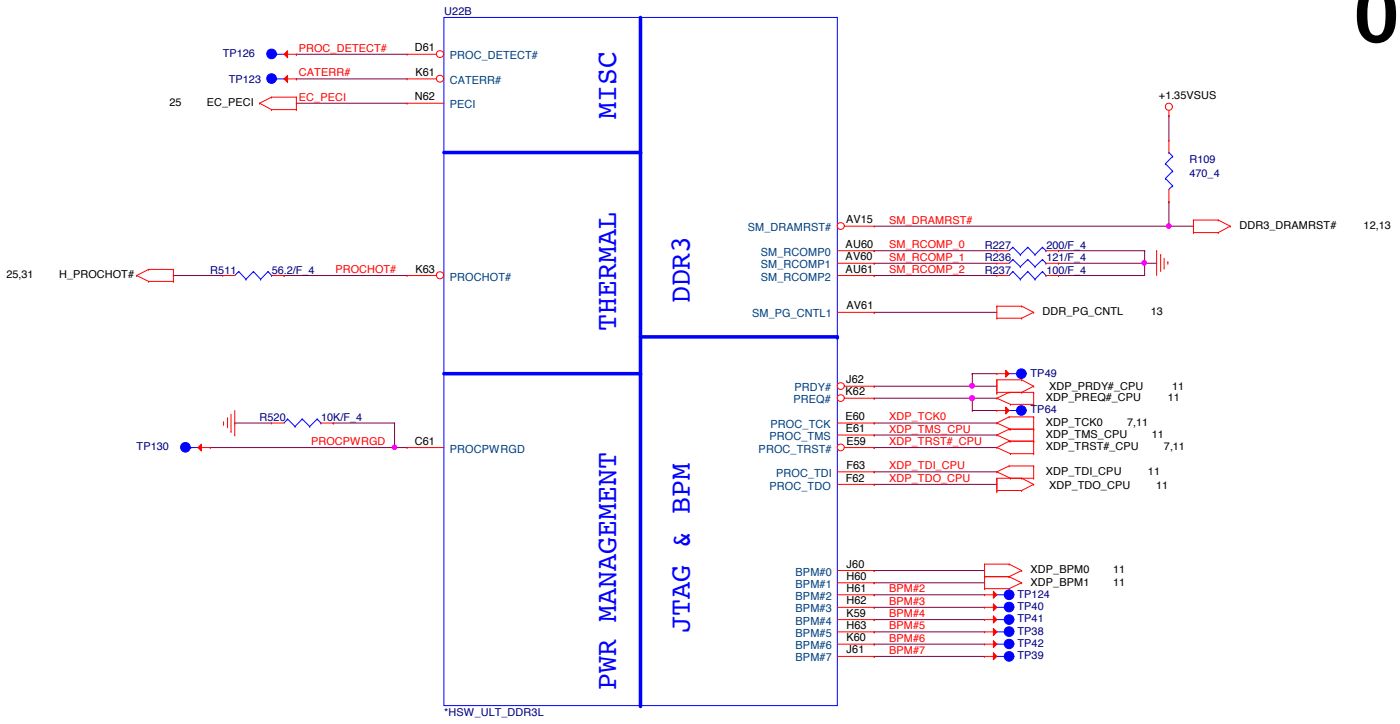
https://t.me/schematicslaptop
https://t.me/biosarchive

PROJECT :Y61
Quanta Computer Inc.

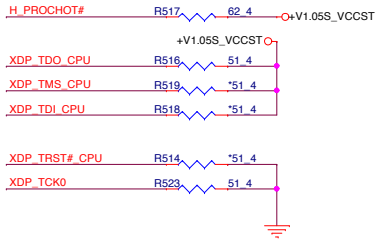
Size	Document Number	Rev
Custom	Block Diagram	1A

Date: Monday, April 21, 2014 Sheet 1 of 32





Processor pull-up (CPU)

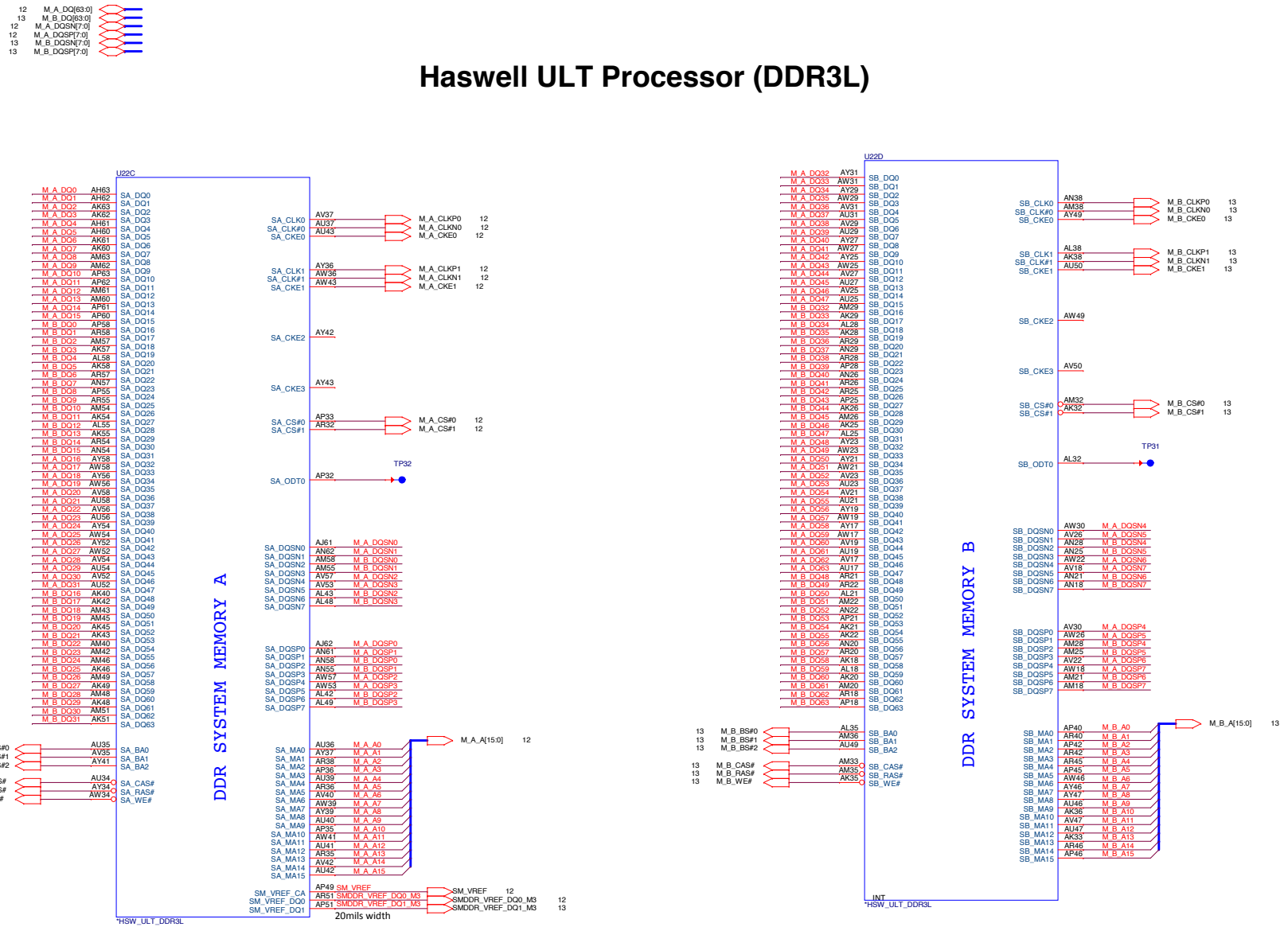


PROJECT :Y61
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ULT 1/9(eDP/DDI)	1A

Date: Monday, April 21, 2014 | Sheet 2 of 32

Haswell ULT Processor (DDR3L)



https://t.me/schematicslaptop
https://t.me/biosarchive

PROJECT :Y61
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ULT 2/9 (DDR3 I/F)	1A
Date: Monday, April 21, 2014	Sheet 3 of 32	

POWER

HSW ULT POWER

U22F

32A
+VCC_CORE

1.4A
+1.35VSUS

Close to CPU

Direct tie to CPU VCC/VSS-Ball

*HSW_ULT_DDR3L

PV reserve for RF request

CFG0-19 need Reserve TP

U22E

RESERVED

*HSW_ULT_DDR3L

Layout note: need routing together and ALERT need between CLK and DATA.

SVID ALERT

SVID CLK

SVID DATA

IO Thrm Protect

For 65 degree, 1.8v limit, (SW)

For 75 degree, 1.2v limit, (HW)

PV change to shortpad

100- ±1% pull-up to VCC near processor.

https://t.me/schematicslaptop
https://t.me/biosarchive

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physcial Debug Enable) DFX Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	CFG3 R508 *1K_4
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	CFG4 R272 1K_4

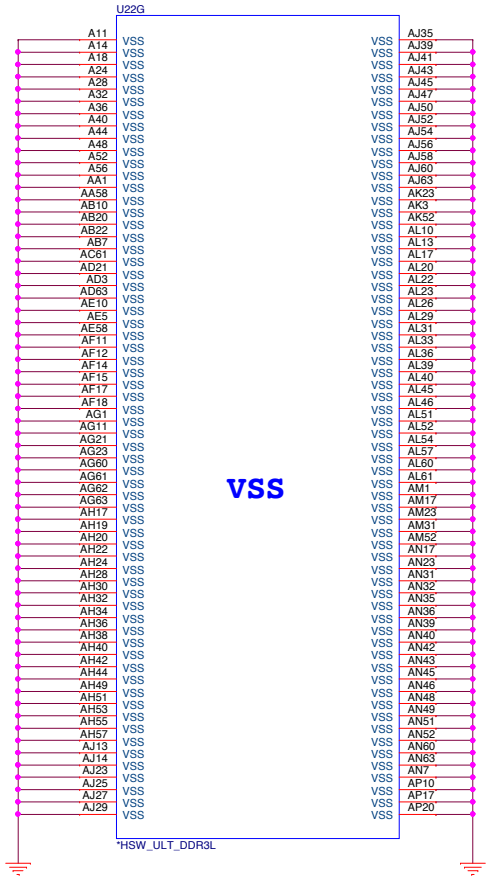
+VCCIOA_OUT 2
+VCCIO_OUT 6

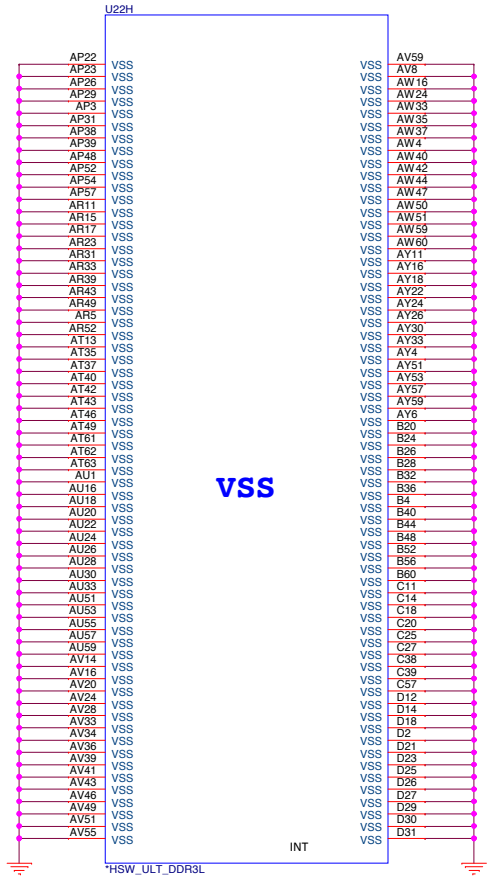
+1.35VSUS 2,12,13,29
+1.05V 7,10,11,25,30,32
+VCC_CORE 31

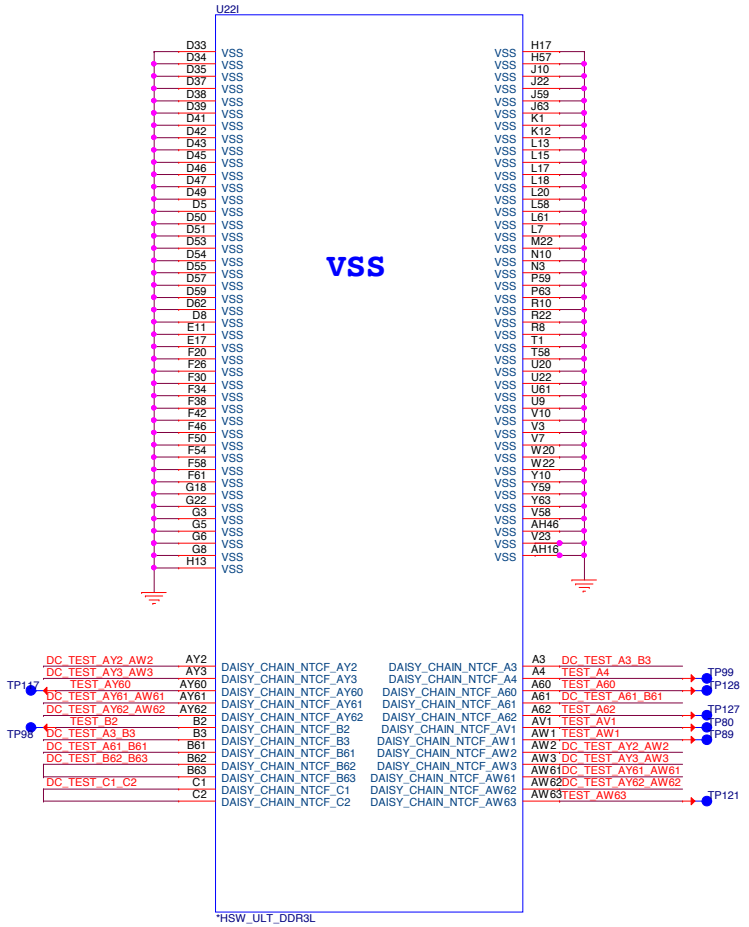
PROJECT :Y61
Quanta Computer Inc.

Size	Document Number	Rev
Custom	04 – ULT 3/9 (POWER-1)	1A

Date: Monday, April 21, 2014 | Sheet 4 of 32





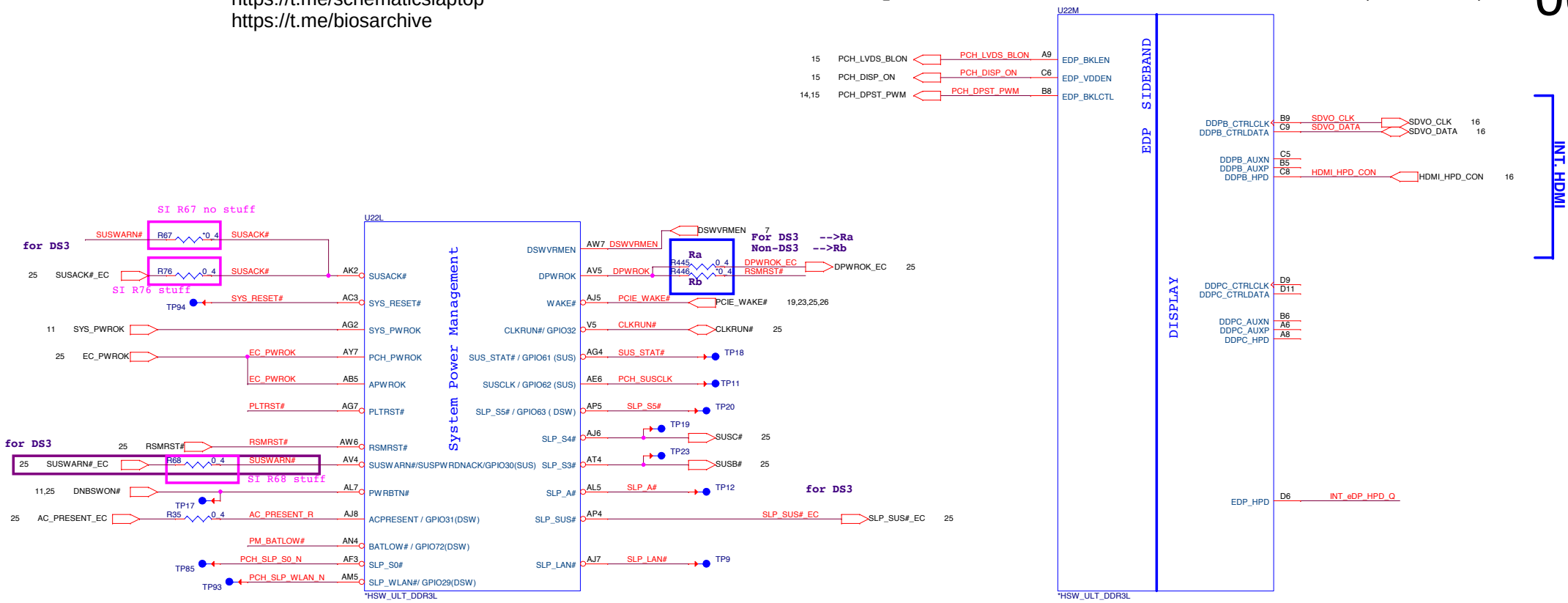


PROJECT :Y61
Quanta Computer Inc.

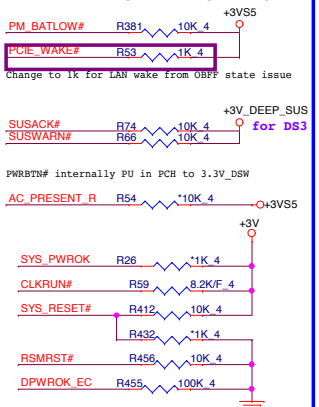
Size	Document Number	Rev
Custom	ULT 4/9 (RSV,GND)	1A

Date: Monday, April 21, 2014 Sheet 5 of 32

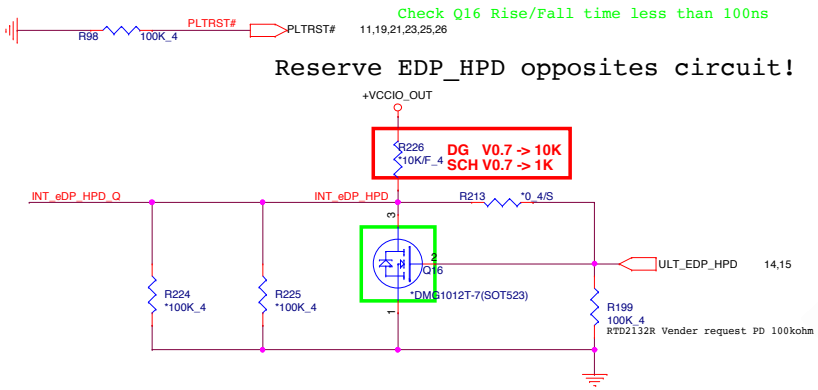
Lynx Point-LP Platform Controller Hub (LVDS,DDI)



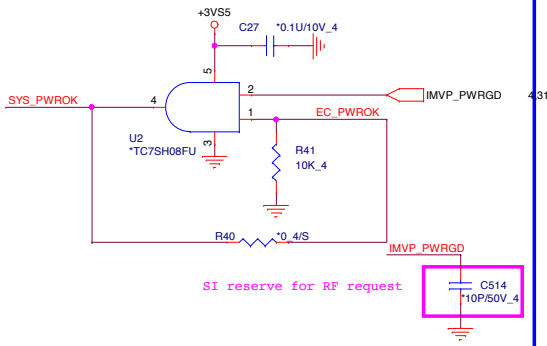
PCH Pull-high/low(CLG)



PLTRST#(CLG)



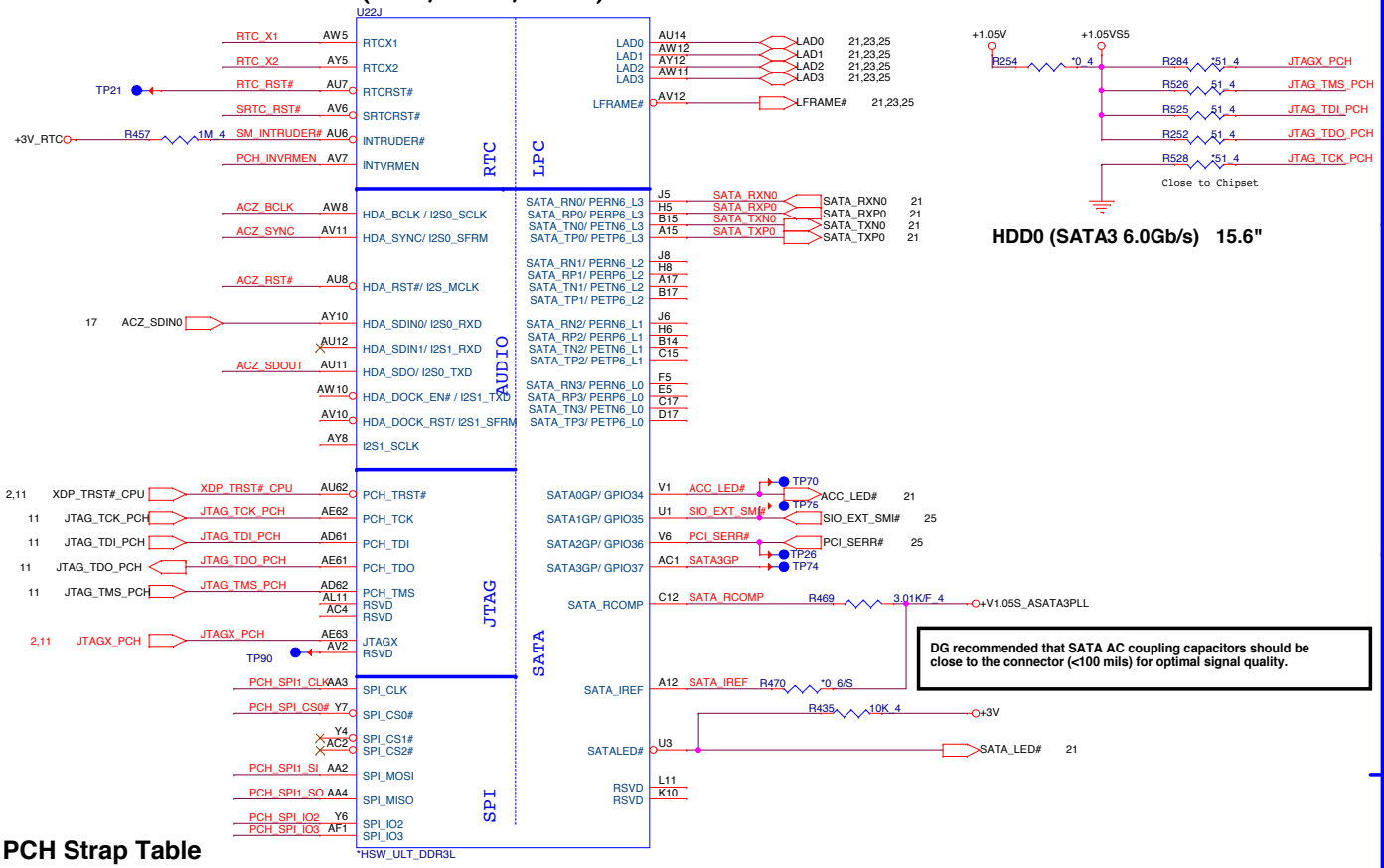
System PWR_OK(CLG)



PROJECT :Y61 Quanta Computer Inc.			
Size: Custom	Document Number: ULT 5/9(Power Manger)		Rev: 1A
Date: Monday, April 21, 2014		Sheet: 6 of	32

Lynx Point-LP Platform Controller Hub (HDA,JTAG,SATA)

07

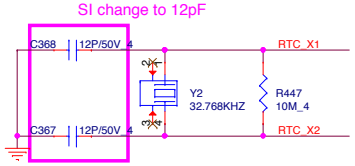


HDD0 (SATA3 6.0Gb/s) 15.6"

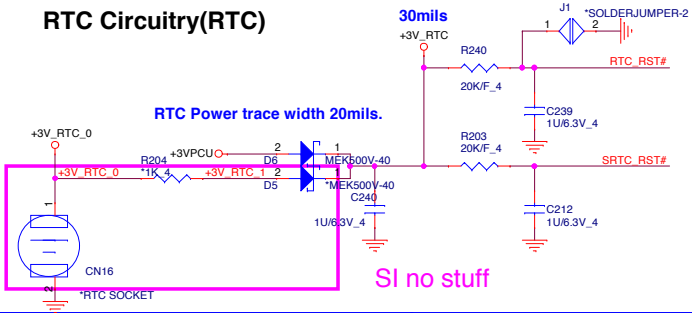
DG recommended that SATA AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

RTC Clock 32.768KHz

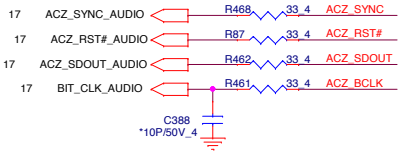
SI change to 12pF



RTC Circuitry(RTC)



HDA Bus(CLG)



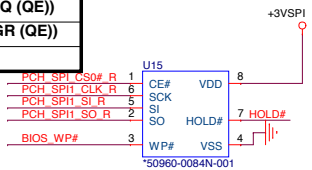
GPIO Pull UP

PCH Strap Table

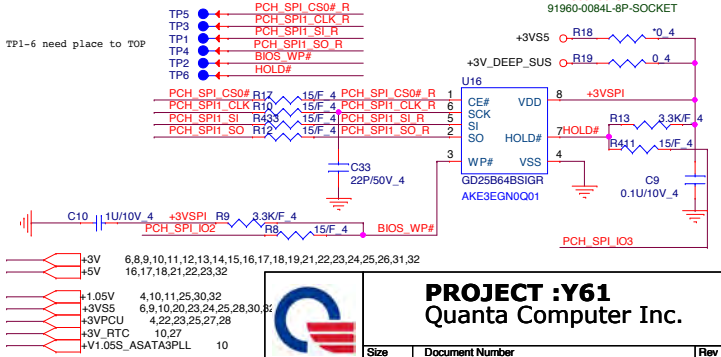
Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V R414 *1K_4 SPKR SPKR 9
SDIO_D0 /GPIO66	Top-Block Swap	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R459 *1K_4 R458 *1K_4 GPIO66_ULT 9
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC R460 330K_4 PCH_INVRMEN
HDA_SDO /I2S0_TXD	Flash Descriptor Security Only for Interposer	PWROK	0 = Default (weak pull-down 20K) 1 = Can be Overridden	25 GPIO33_EC R467 1K_4 ACZ_SDOUT
GSPI0_MOSI /GPIO86	Boot BIOS Selection	PWROK	GNT0# 1 = LPC; 0 = SPI(Default)	
GPIO15	TLS Confidentiality	PWROK	0 = ME Crypto Transport Layer Security cipher suite with no confidentiality(Default) 1 = Intel ME Crypto TLS cipher suite with confidentiality	+3V_DEEP_SUS R33 *1K_4 GPIO15_ULT 9
DSWVRMEN	Deep Sx Well On-Die Voltage Regulator Enable	ALWAYS	Should be always pull-up	+3V_RTC R463 330K_4 DSWVRMEN 6
				25 PCH_SPI_CS0#_R → PCH_SPI_CS0#_R 25 PCH_SPI1_CLK_R → PCH_SPI1_CLK_R 25 PCH_SPI1_SI_R → PCH_SPI1_SI_R 25 PCH_SPI1_SO_R → PCH_SPI1_SO_R

Vender	Size	P/N
EON	8MB	AKE3EZN0Q01 (EN25QH64-104HIP (QE))
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ (QE))
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR (QE))
Socket		DFHS08FS023

4M SPI ROM Socket



PCH SPI ROM(CLG)



+3V 6,8,9,10,11,12,13,14,15,16,17,18,19,21,22,23,24,25,26,31,32
+5V 16,17,18,21,22,23,32
+1.05V 4,10,11,25,30,32
+3VS5 6,9,10,20,23,24,25,28,30,3
+3VPCU 4,22,23,25,27,28
+3V_RTC 10,27
+V1.05S_ASATA3PLL 10

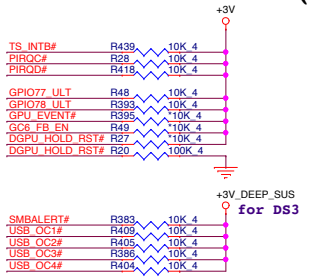
PROJECT :Y61
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ULT 6/9(SATA/HDA)	1A
Date: Monday, April 21, 2014	Sheet 7 of 32	

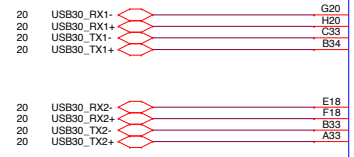
Lynx Point-LP Platform Controller Hub (HDA,JTAG,SATA)

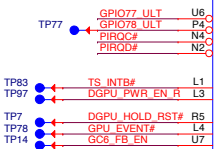
08

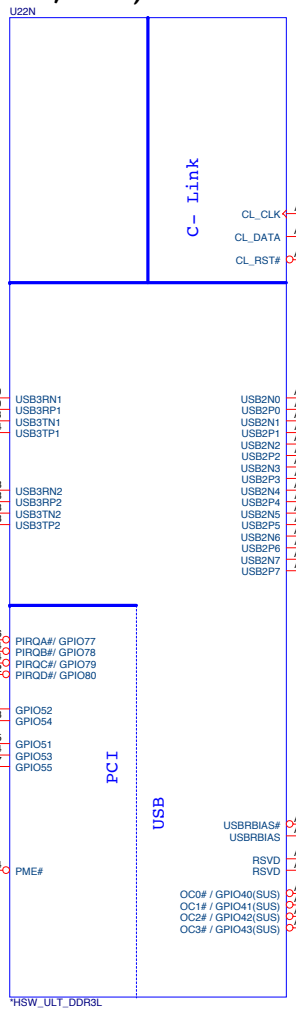
PCI/USBOC# Pull-up(CLG)

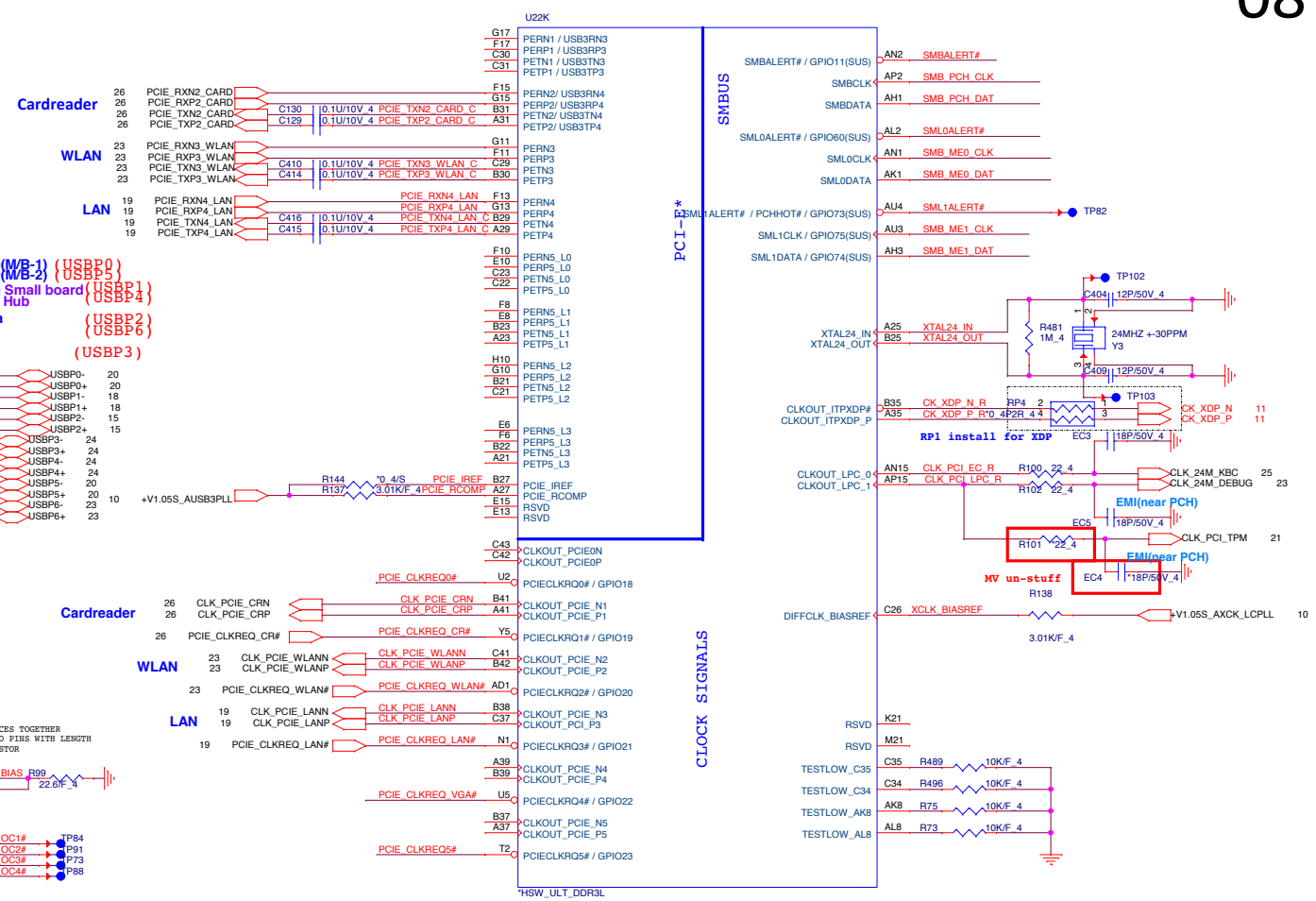


USB3.0



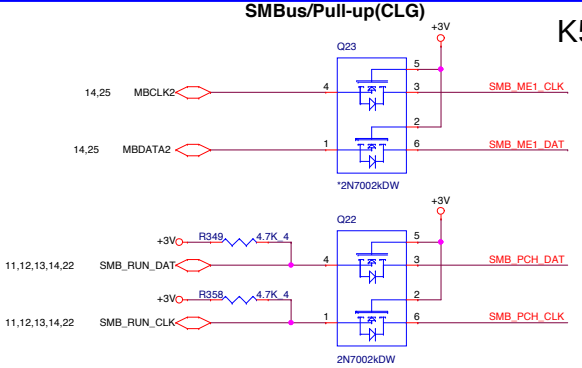




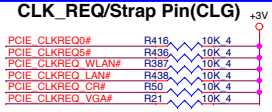


SMBus/Pull-up(CLG)

K501UB



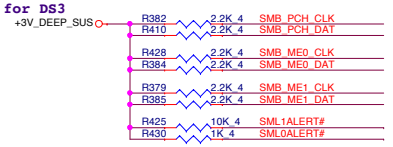
CLK_REQ/Strap Pin(CLG)



https://t.me/schematicslaptop
https://t.me/biosarchive

6,7,9,10,11,12,13,14,15,16,17,18,19,21,22,23,24,25,26,31,32 +3V
6,7,9,10,11 +3V_DEEP_SUS

SMBus/Pull-up(CLG)



PROJECT :Y61
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ULT 7/9 (PCIE/USB/CLK)	1A
Date: Monday, April 21, 2014	Sheet 8 of 32	

Lynx Point-LP Platform Controller Hub (HDA,JTAG,SATA) Haswell (GPIO)

09

PV change to shortpad

U22O

GPIO8(SUS) AU2 — SIO_EXT_SCI# (TP81) — 25 SIO_EXT_SCI#
GPIO9(SUS) AM3 — BT_OFF (TP72) — 23 BT_OFF
GPIO10(SUS) AM2 — RF_OFF (TP92) — 23 RF_OFF
LAN_PHY_PWR_CTRL / GPIO12(DSW) AM7 — LAN_DISABLE#
GPIO13(SUS) AT3 — GPIO13_ULT
GPIO14(SUS) AH4 — GPIO14_ULT
GPIO15(SUS) AD6 — (TP16) — 7 GPIO15_ULT
GPIO16 Y1 — ODD_PRSNT#_R (TP95)
GPIO17 T3 — (TP15)
GPIO24 (SUS) AD5 — GPIO24_ULT
GPIO25(DSW) AM4 — GPIO25_ULT
GPIO26(SUS) AN3 — GPIO26_ULT
GPIO27(DSW) AN5 — DSW_WAKE# (TP13)
GPIO28(SUS) AD7 — GPIO28_ULT
DEVSLP0/ GPIO33 P2 — DEVSLP0
DEVSLP1/ GPIO38 L2 — DEVSLP1 (TP87)
DEVSLP2/ GPIO39 N5 — DEVSLP2
GPIO44(SUS) AK4 — GPIO44_ULT
GPIO45(SUS) AG5 — BOARD_ID4
GPIO46(SUS) AG3 — ACCEL_INTA# — 22 ACCEL_INTA# (TP for DG)
GPIO47(SUS) AB6 — BOARD_ID5 (TP86)
GPIO48 U4 — BT_COMBO_EN# — 23 BT_COMBO_EN#
GPIO49 Y3 — ACCEL_INTH# — 24 ACCEL_INTH#
GPIO50 P3 — XRESB_R (TP76)
GPIO56(SUS) AG6 — BOARD_ID0
GPIO57(SUS) AP1 — BOARD_ID1
GPIO58(SUS) AL4 — BOARD_ID2
GPIO59(SUS) AT5 — BOARD_ID3 (TP10)
SDIO_POWER_EN/ GPIO70 C4 — GPIO70_ULT
HSIOPC/ GPIO71 Y2 — MPHY_PWREN — 32 MPHY_PWREN
BMBUSY# / GPIO76 P1 — GPIO76_ULT (TP96)
SPKR/ GPIO81 V2 — SPKR — R390 *0_4/S — 17 ACZ_SPKR; 7 SPKR

GPIO

CPU/MISC

THRMTRIP# D60 — PCH_THRMTRIP# — R521 *0_4/S — PM_THRMTRIP# 25
RCIN#/ GPIO82 V4 — EC_RCIN# — EC_RCIN# 25
SERIRQ T4 — SERIRQ — R29 10K_4 — +3V; SERIRQ 21,25
PCH_OPI_RCOMP AW15 — PCH_OPI_RCOMP — R475 49.9/F_4
RSVD AF20
RSVD AB21

SERIAL IO

GSPI0_CS/ GPIO83 R6 — GSPI0_CS
GSPI0_CLK/ GPIO84 L6 — GSPI0_CLK
GSPI0_MISO/ GPIO85 N6 — GSPI0_MISO
GSPI0_MOSI/ GPIO86 L8 — GPIO86_ULT — TP24
GSPI1_CS/ GPIO87 R7 — GSPI1_CS
GSPI1_CLK/ GPIO88 L5 — GSPI1_CLK
GSPI1_MISO/ GPIO89 N7 — GSPI1_MISO
GSPI1_MOSI/ GPIO90 K2 — GSPI1_MOSI
UART0_RXD/ GPIO91 J1 — UART0_RXD
UART0_TXD/ GPIO92 K3 — UART0_TXD
UART0_RTS/ GPIO93 J2 — UART0_RTS
UART0_CTS/ GPIO94 G1 — UART0_CTS
UART1_RXD/ GPIO0 K4 — UART1_RXD
UART1_TXD/ GPIO1 G2 — UART1_TXD
UART1_RST/ GPIO2 J3 — UART1_RST
UART1_CTS/ GPIO3 J4 — UART1_CTS
I2C0_SDA/ GPIO4 F2 — I2C0_SDA
I2C0_SCL/ GPIO5 F3 — I2C0_SCL
I2C1_SDA/ GPIO6 G4 — I2C1_SDA
I2C1_SCL/ GPIO7 F1 — I2C1_SCL
SDIO_CLK/ GPIO64 E3 — SDIO_CLK
SDIO_CMD/ GPIO65 F4 — SDIO_CMD
SDIO_D0/ GPIO66 D3
SDIO_D1/ GPIO67 E4 — SDIO_D1
SDIO_D2/ GPIO68 C3 — SDIO_D2
SDIO_D3/ GPIO69 E2 — SDIO_D3

*HSW_ULT_DDR3L

RP1: 10 UART1_RXD; 9 I2C1_SDA; 8 GSPI0_CLK; 7 GSPI1_CLK; 6 — 1 SDIO_D2; 2 SDIO_D1; 3 SDIO_CMD; 4 SDIO_CLK; 5 — 10K_10P8R_6 — +3V
RP3: 10 GSPI1_MOSI; 9 GSPI0_MISO; 8 GSPI1_MISO; 7 UART0_TXD; 6 — 1 I2C1_SCL; 2 SDIO_D3; 3; 4; 5 — 10K_10P8R_6 — +3V
RP2: 10 UART0_RXD; 9 UART1_CTS; 8 GSPI0_CS; 7 GSPI1_CS; 6 — 1 UART1_RST; 2 UART0_RTS; 3 UART0_CTS; 4 UART1_TXD; 5 — 10K_10P8R_6 — +3V

GPIO Pull-up/Pull-down(CLG)

+3V_DEEP_SUS
SIO_EXT_SCI# R380 10K_4
BT_OFF R408 10K_4
RF_OFF R429 10K_4
GPIO13_ULT R426 10K_4
GPIO14_ULT R64 10K_4
GPIO24_ULT R431 10K_4
GPIO25_ULT R407 10K_4
GPIO28_ULT R62 10K_4
GPIO44_ULT R65 10K_4
ACCEL_INTA# R23 10K_4

+3V
I2C0_SCL R396 10K_4
I2C0_SDA R448 10K_4
ACCEL_INTH# R369 10K_4
XRESB_R R417 10K_4
ODD_PRSNT#_R R389 10K_4
DEVSLP0 R394 10K_4
DEVSLP2 R47 10K_4
BT_COMBO_EN# R415 *10K_4
GPIO70_ULT R464 10K_4
EC_RCIN# R60 10K_4
GPIO76_ULT R437 10K_4
MPHY_PWREN R413 100K_4
MPHY_PWREN R434 *10K_4

+3VS5
GPIO25_ULT R36 10K_4
LAN_DISABLE# R55 10K_4
DSW_WAKE# R37 10K_4

Close to EC

+V1.05S_VCCST
PM_THRMTRIP# R180 1K_4

Model	BOARD_ID5	BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
13" clamshell wo/TS	0	0	0	0	0	1
13" convertible w/TS	0	0	0	0	1	0
15" convertible w/TS+ Giga NIC	0	0	0	0	1	1
13" clamshell w/TS (Reserve)	0	0	0	0	0	0
13" convertible wo/TS (Reserve)	0	0	0	0	0	0
15" convertible w/TS (Reserve)	0	0	0	0	0	0

R63 *10K_4 BOARD_ID0 R51 10K_4 +3V_DEEP_SUS
R427 *10K_4 BOARD_ID1 R406 10K_4
R24 10K_4 BOARD_ID2 R25 *10K_4
R39 10K_4 BOARD_ID3 R38 *10K_4
R34 10K_4 BOARD_ID4 R52 *10K_4
R61 10K_4 BOARD_ID5 R32 *10K_4

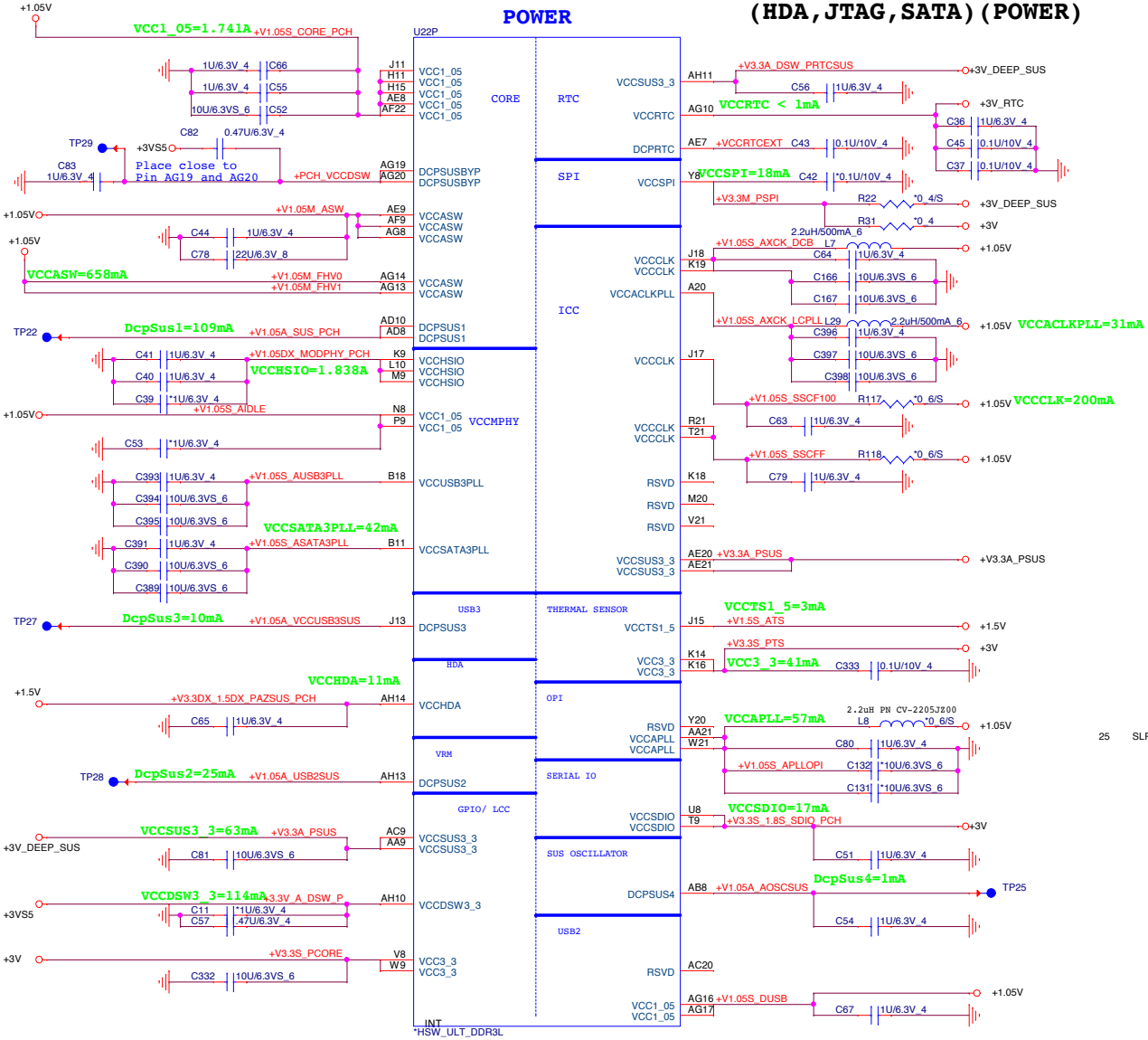
6,7,8,10,11,12,13,14,15,16,17,18,19,21,22,23,24,25,26,31,32 +3V
6,7,10,20,23,24,25,28,30,32 +3VS5

PROJECT :Y61
Quanta Computer Inc.

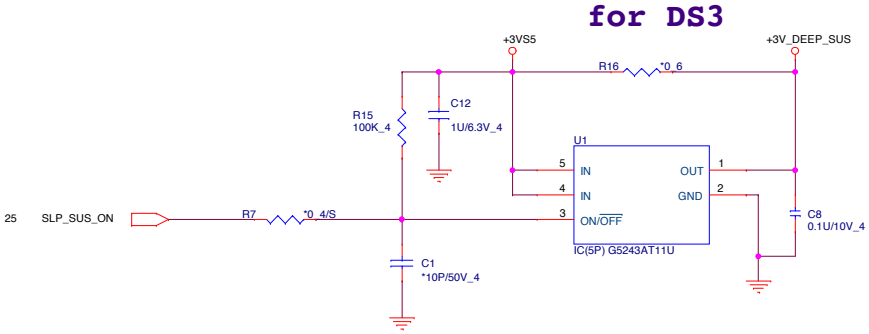
Size	Document Number	Rev
Custom	ULT 8/9 (GPIO/MISC)	1A
Date: Monday, April 21, 2014	Sheet 9 of 32	

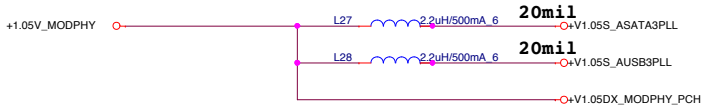
Lynx Point-LP Platform Controller Hub (HDA,JTAG,SATA)(POWER)

POWER



for DS3





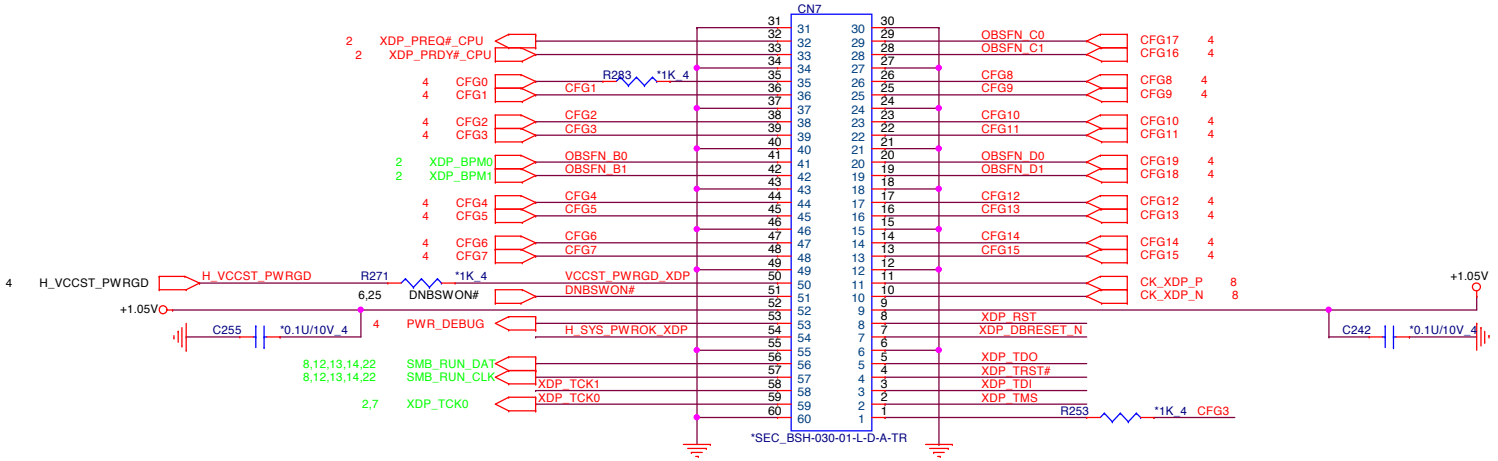
https://t.me/schematicslaptop
https://t.me/biosarchive

6,7,8,9,11,12,13,14,15,16,17,18,19,21,22,23,24,25,26,31,32 +3V
16,17,18,21,22,23,32 +5V
4,7,11,25,30,32 +1.05V
6,7,9,20,23,24,25,28,30,32 +3VS5
13,18,20,28,29,30,31,32 +5VS5
8 +V1.05S_AUSB3PLL
7 +V1.05S_ASATA3PLL
8 +V1.05S_AXCK_LCPLL
7,27 +3V_RTC
2,4,12,13,29 +1.35VSUS

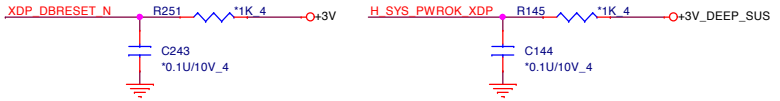
PROJECT :Y61
Quanta Computer Inc.

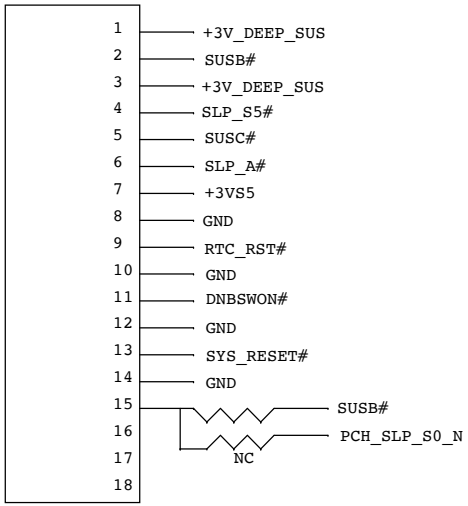
Size	Document Number	Rev
Custom	ULT 9/9(POWER-2)	1A

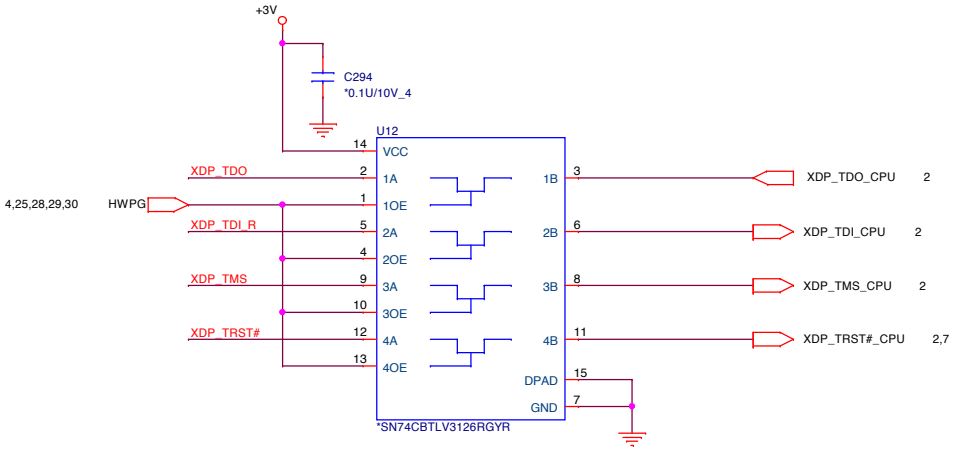
Date: Monday, April 21, 2014 Sheet 10of 32

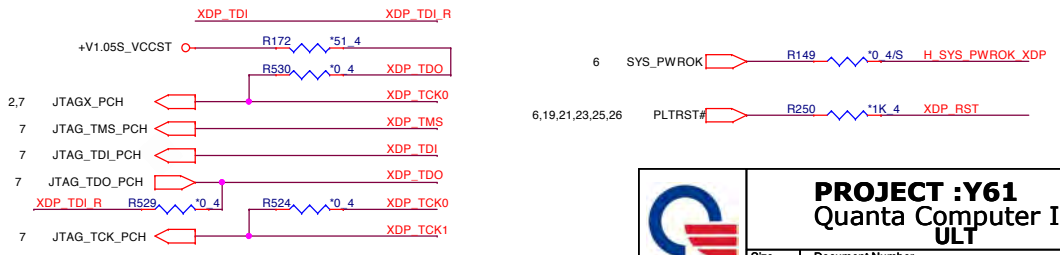


https://t.me/schematicslaptop
https://t.me/biosarchive





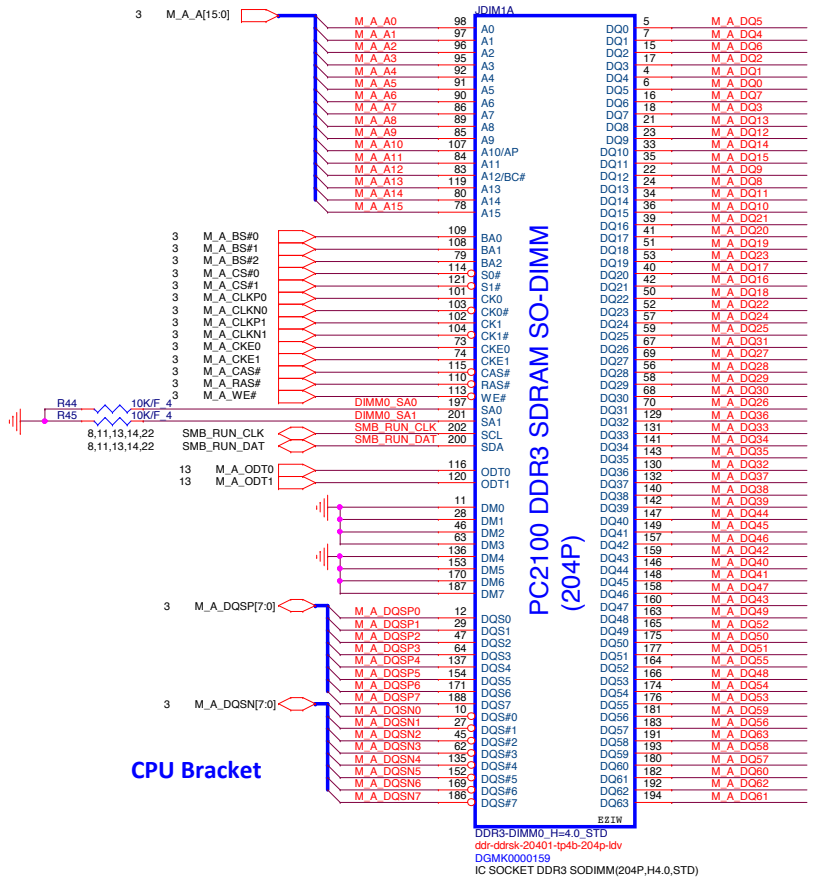


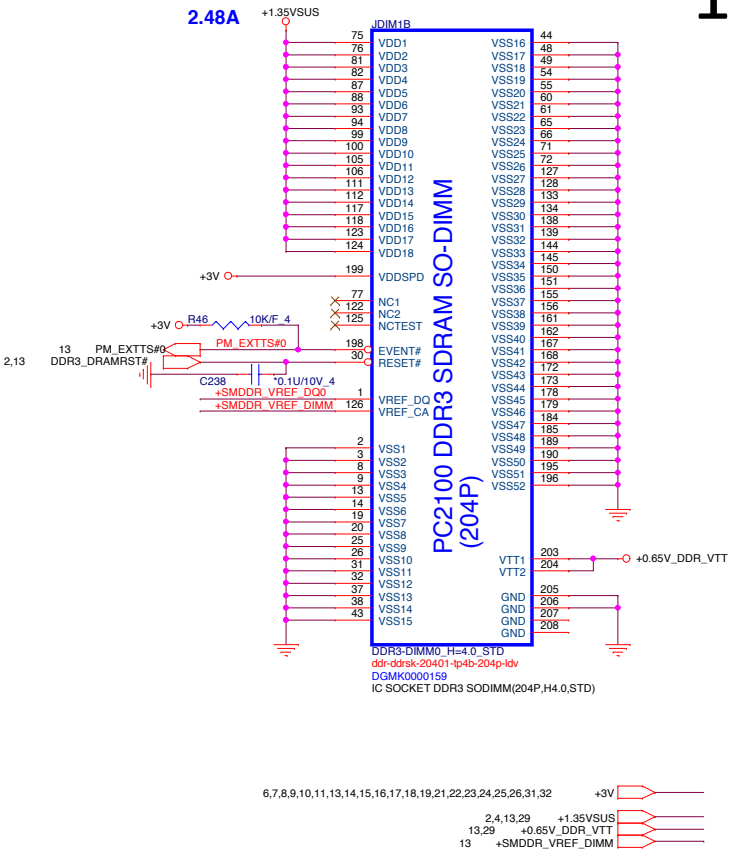


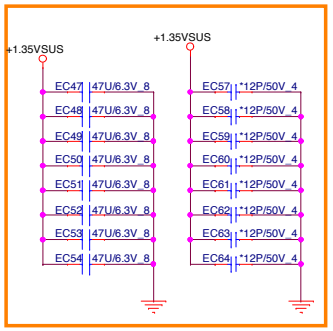
PROJECT :Y61
Quanta Computer Inc.
ULT

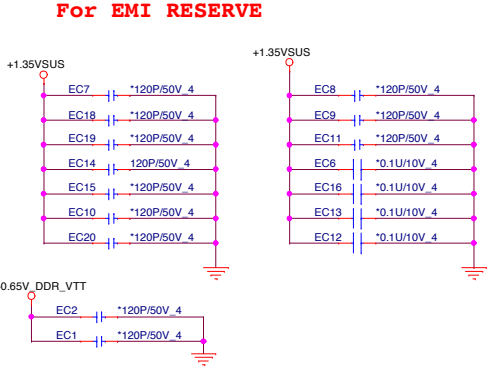
Size	Document Number	Rev
	HSW XDP & APS	1A

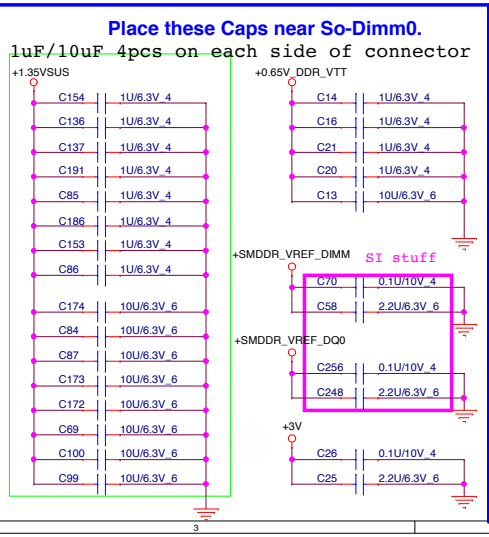
Date: Monday, April 21, 2014 | Sheet 11 of 32

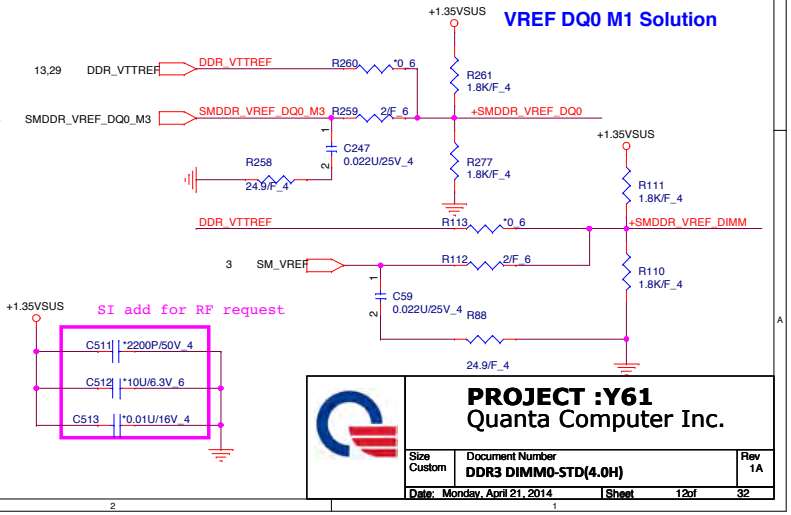






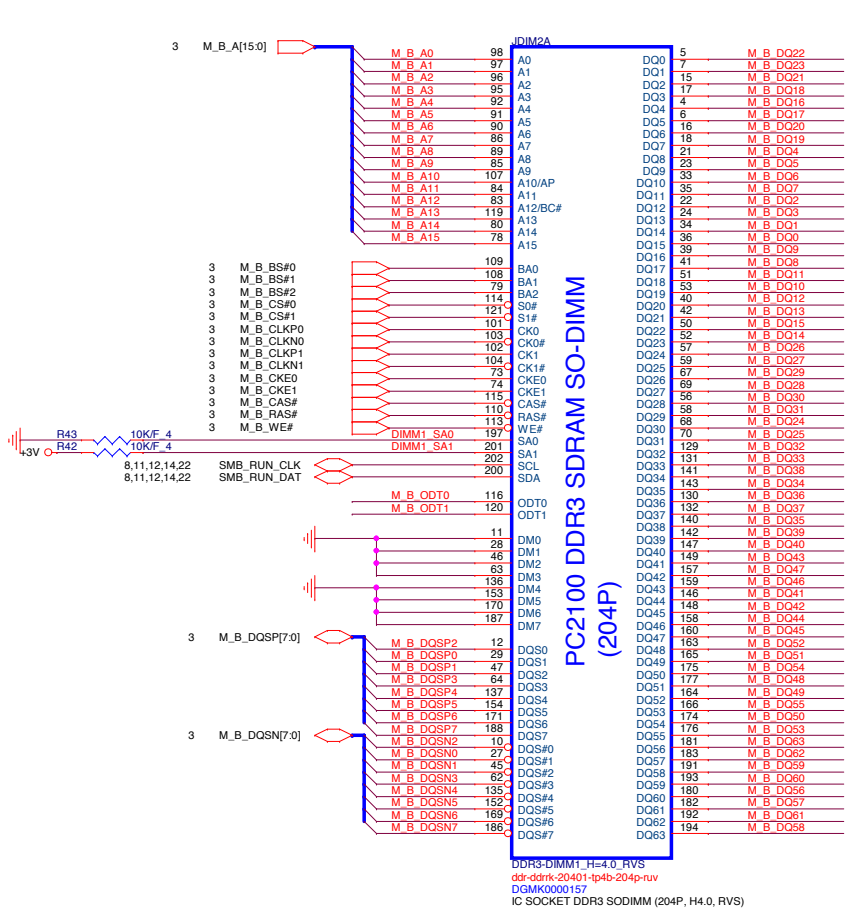


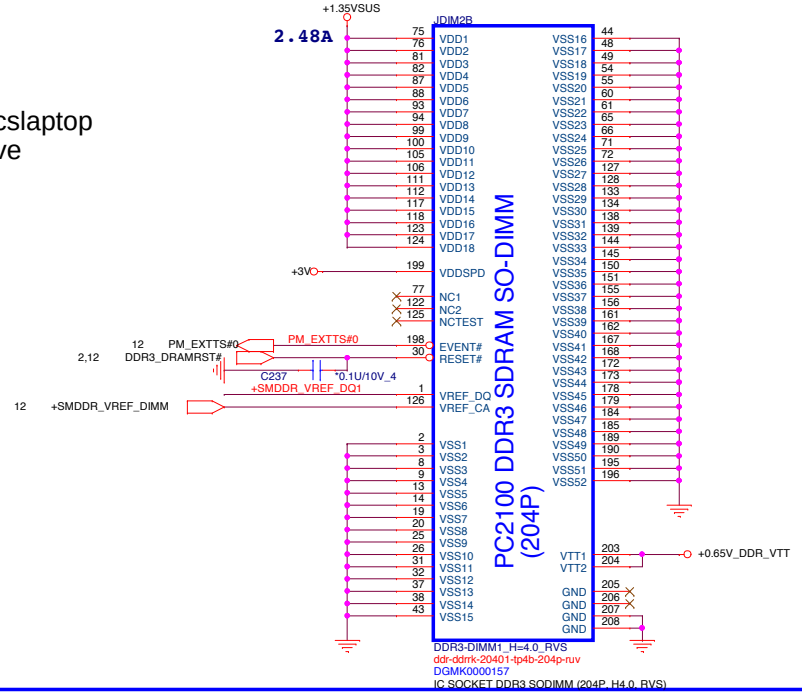


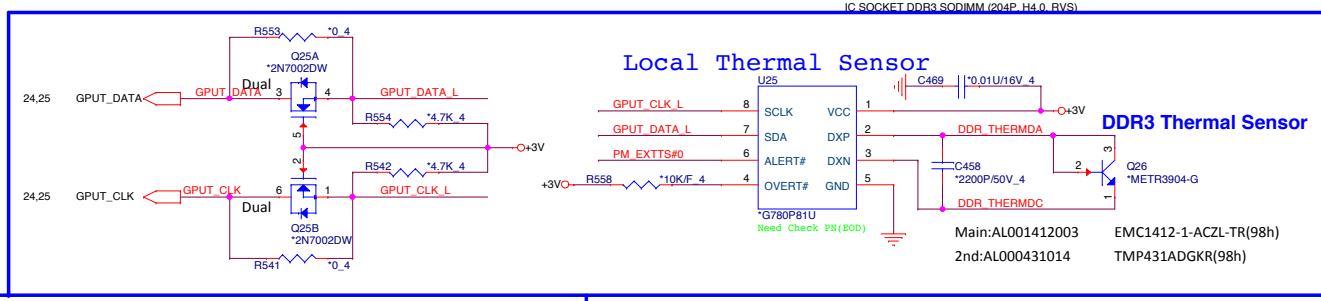


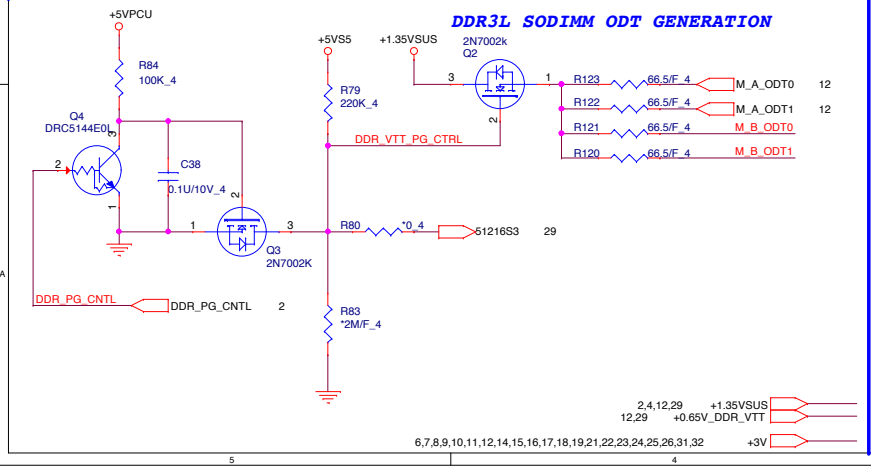
PROJECT :Y61
Quanta Computer Inc.

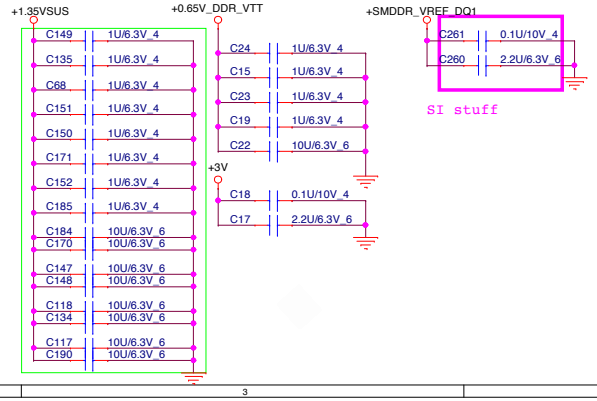
Size	Document Number	Rev
Custom	DDR3 DIMM0-STD(4.0H)	1A
Date: Monday, April 21, 2014	Sheet 12of 32	

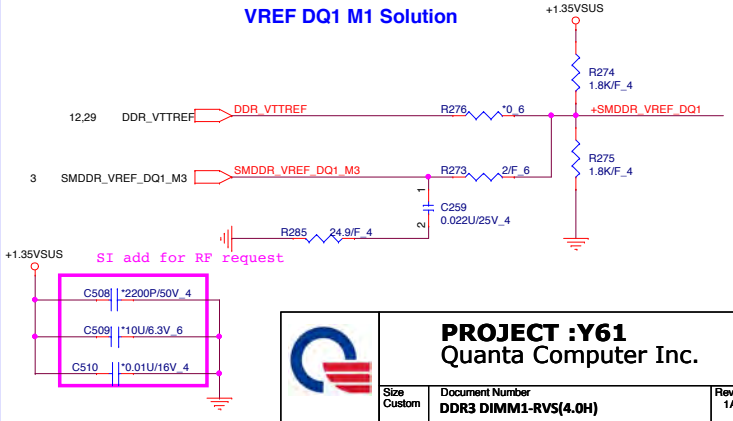










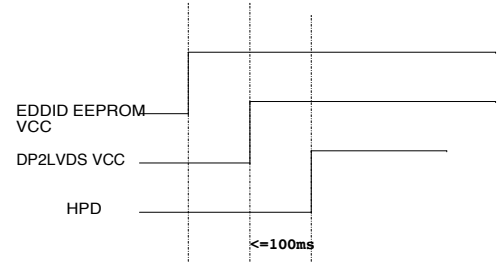


PROJECT :Y61
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM1-RVS(4.0H)	1A
Date: Monday, April 21, 2014	Sheet 13of 32	

RTD2136 Dual Channel only

RTD2136S Power Up Sequence 14



Reserve for co layout EDP CON, EDP only please stuff

Pine 18: keep 80 Mile Trace

PV remove EEPROM

https://t.me/schematicslaptop
https://t.me/biosarchive

Reserve

PV Add TP

Default PV change to shortpad

For EDP: unstuff Ra

Ra

RTD2136R
R376;R365: NA
R375;R374: Stuff

keep 80 Mile Trace

L10: need use CV-4709MN00 for Vendor suggestion

Close to Pin18

Close to Pin5

Close to Pin17

Close to Pin43

Close to Pin11

CLOSE TO Pin22

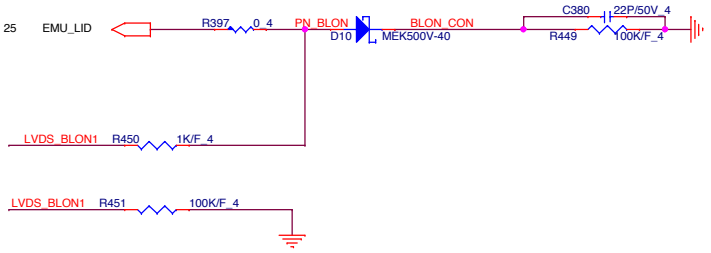
SWR MODE	LDO MODE
Stuff L22	Stuff R372

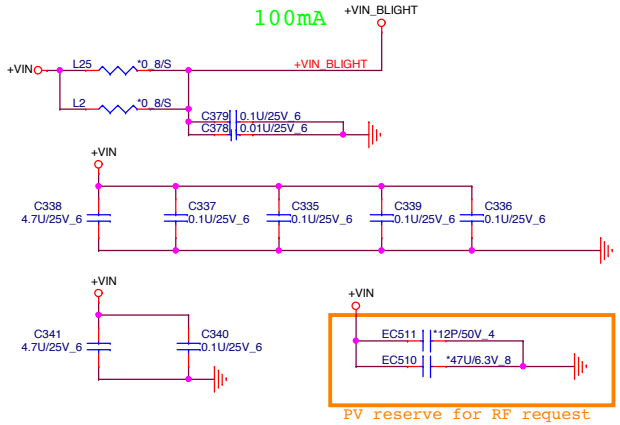
PROJECT :Y61
Quanta Computer Inc.

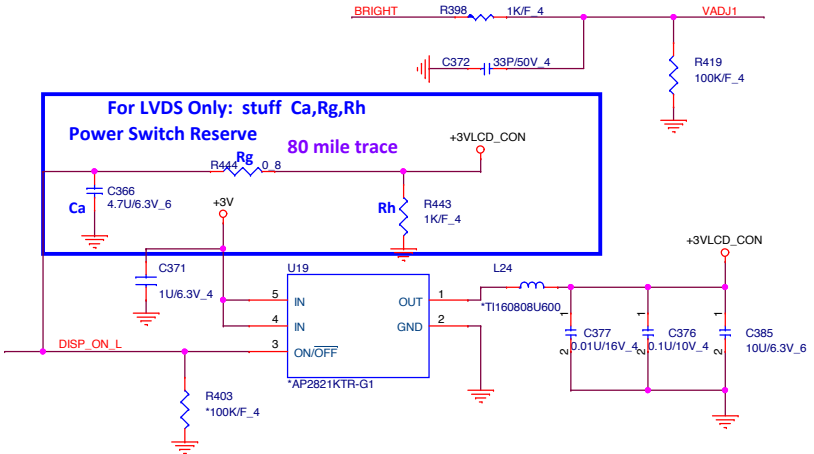
Size	Document Number	Rev
Custom	RTD2136	1A

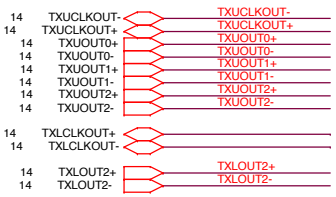
Date: Monday, April 21, 2014 Sheet 14 of 32

LID Switch

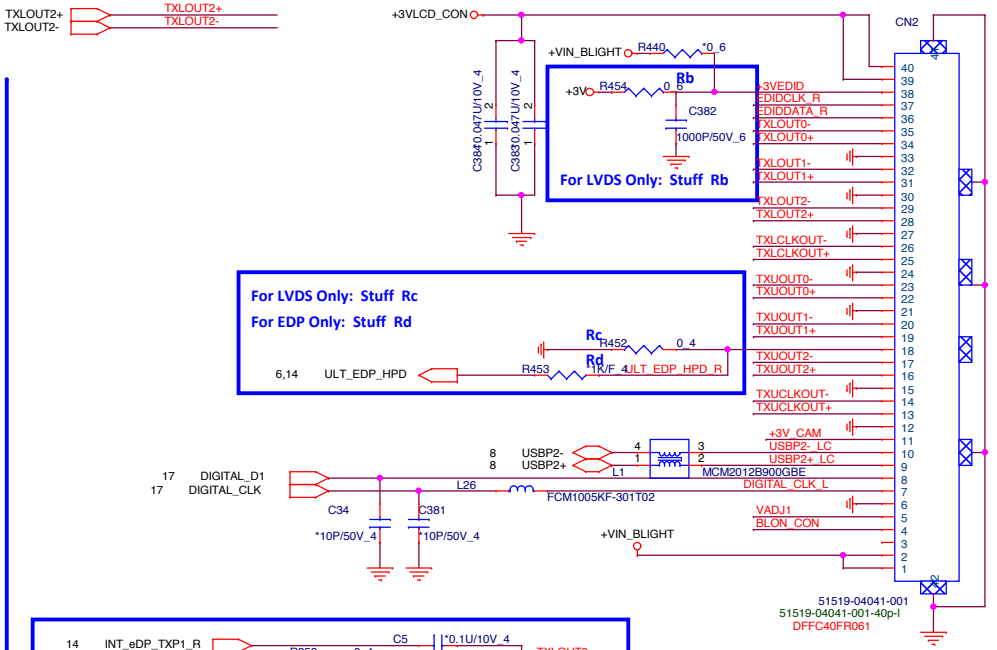


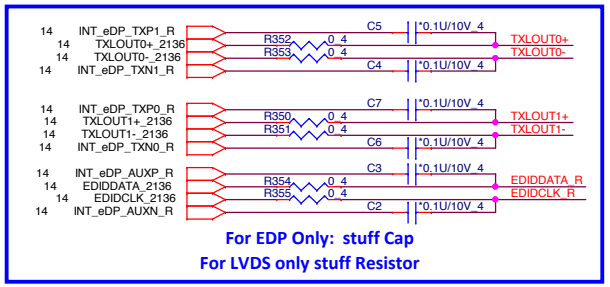


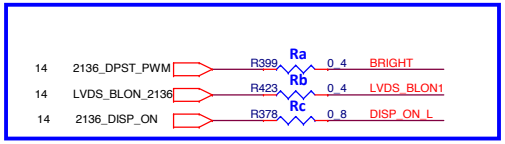


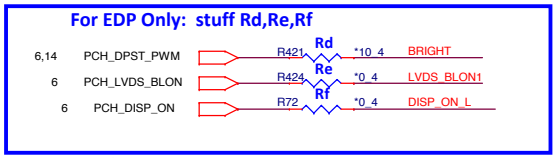


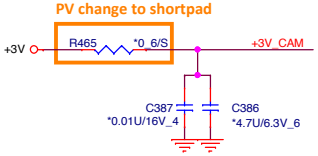
LVDS Conn.

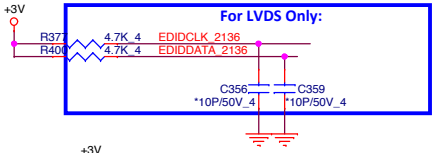


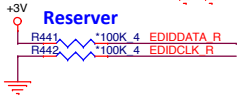








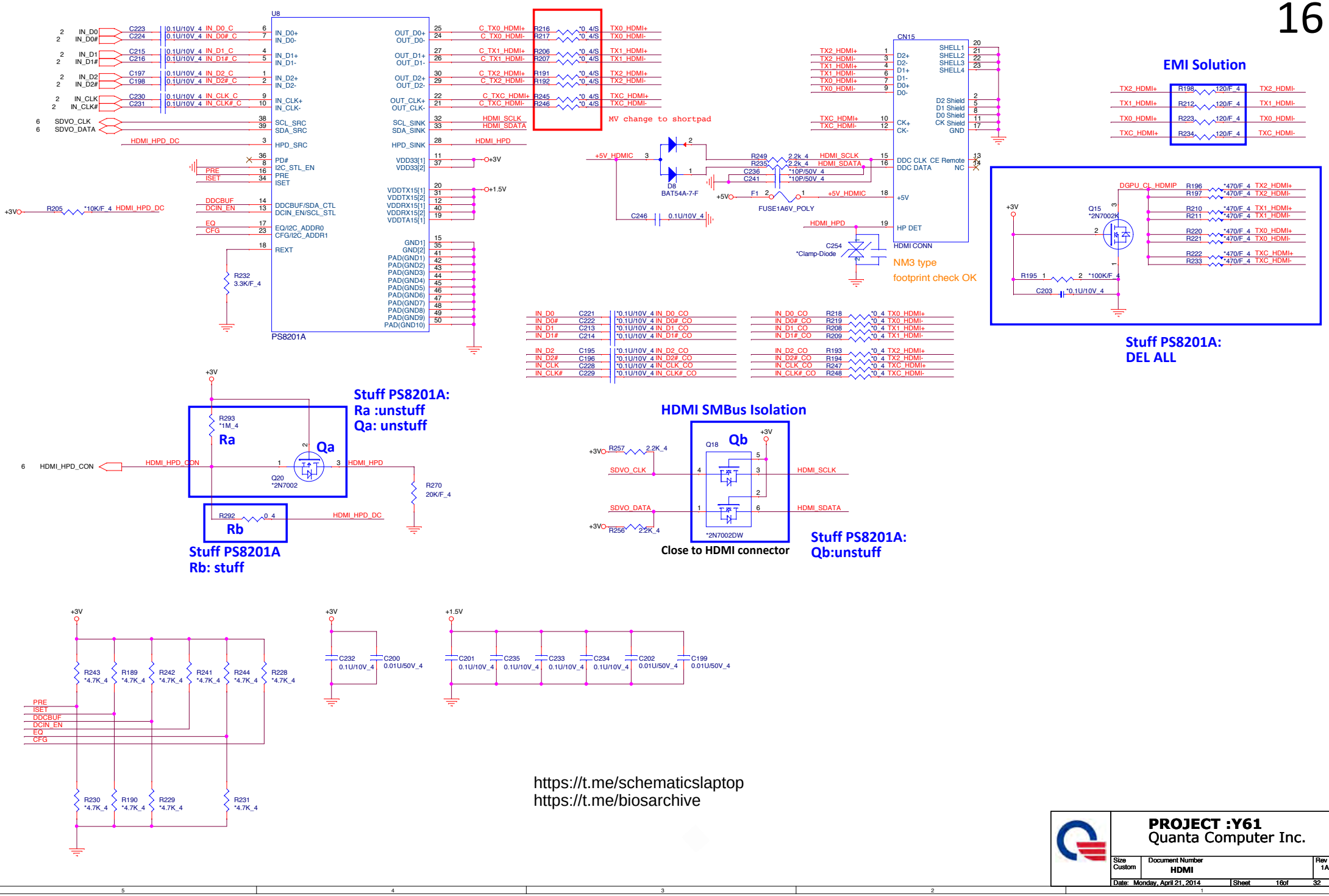




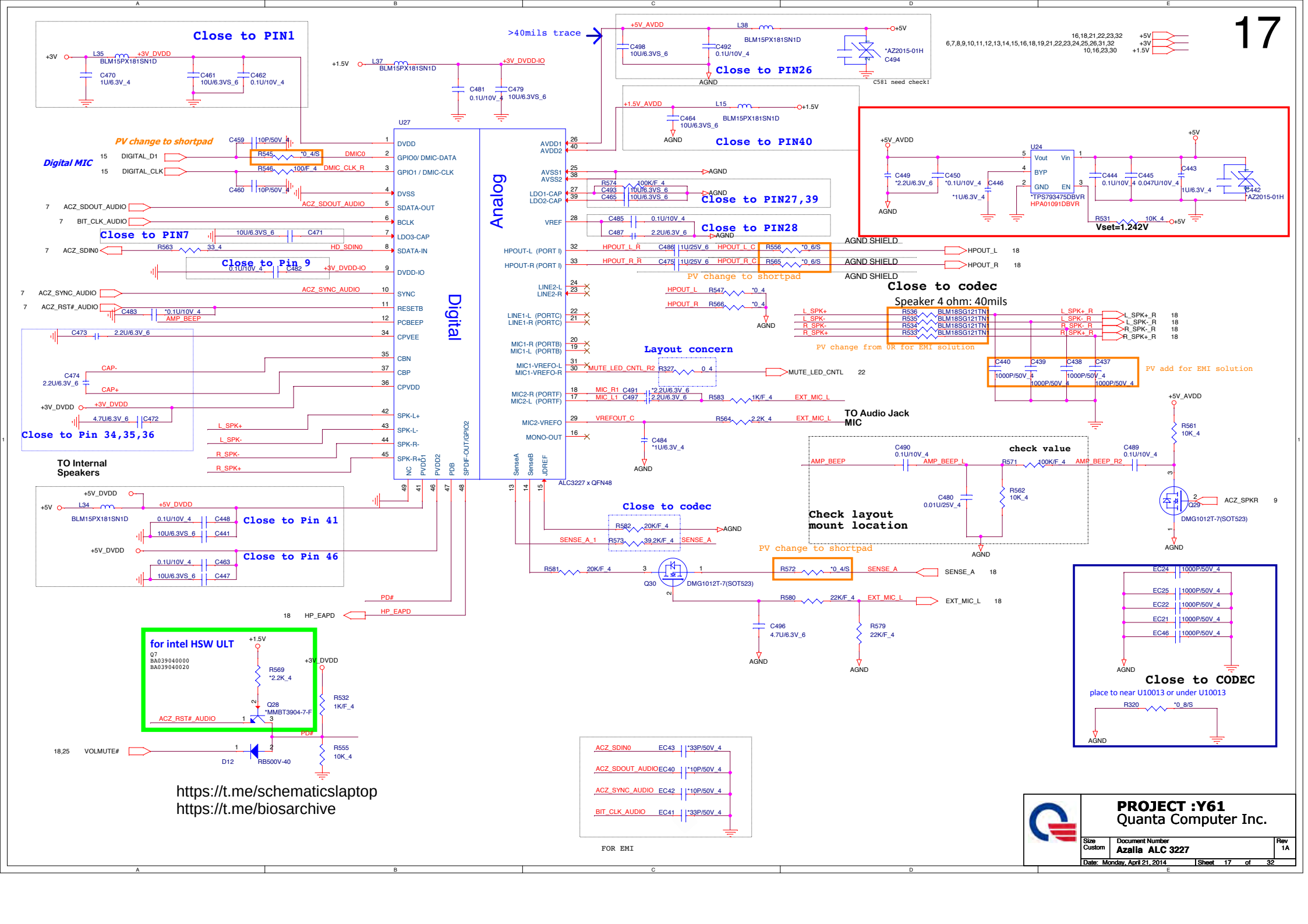
6,7,8,9,10,11,12,13,14,16,17,18,19,21,22,23,24,25,26,31,32 +3V
4,7,22,23,25,27,28 +3VPCU
16,17,18,21,22,23,32 +5V
22,27,28,29,30,31,32 +VIN

PROJECT :Y61
Quanta Computer Inc.

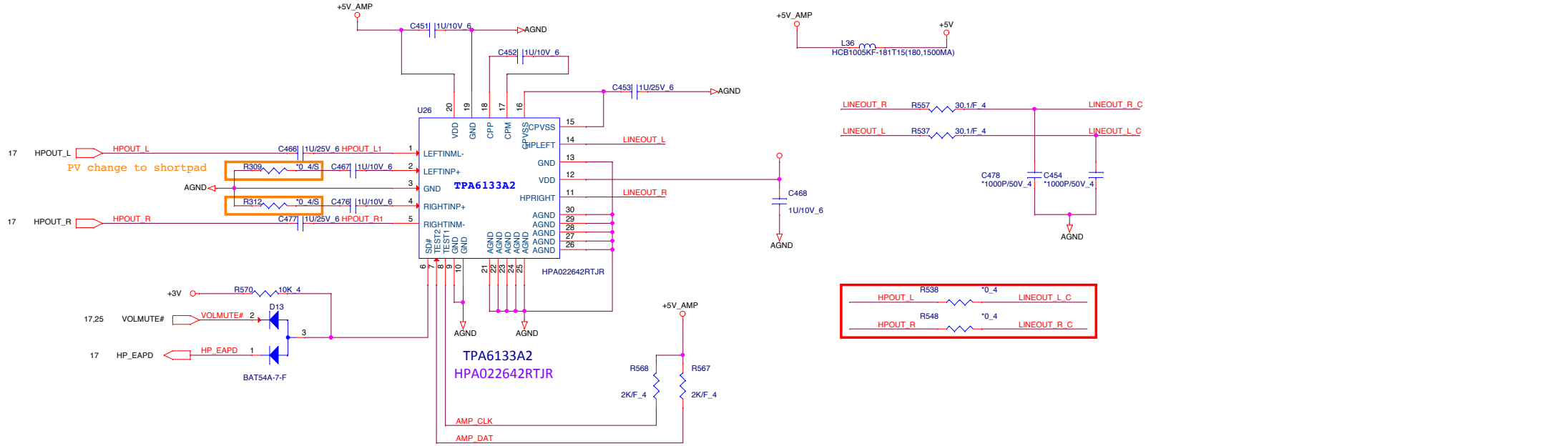
Size	Document Number	Rev
Custom	LCD CONN/LID/CAM	1A
Date: Monday, April 21, 2014	Sheet 15 of 32	



PROJECT	:Y61
Quanta Computer Inc.	
Size	Custom
Document Number	HDMI
Rev	1A
Date:	Monday, April 21, 2014
Sheet	16of 32

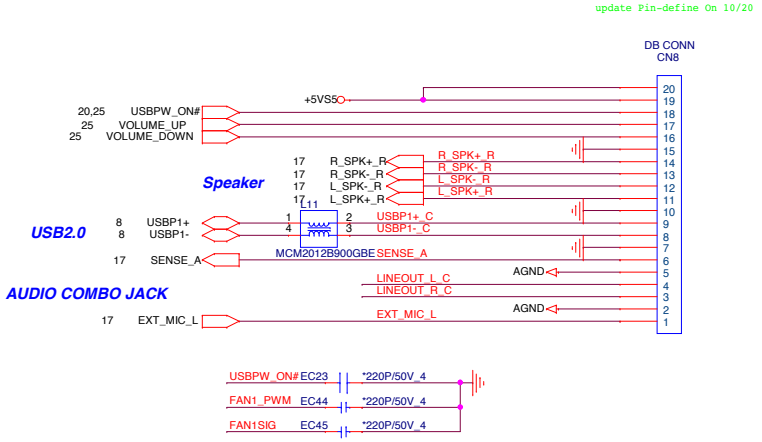

17
Close to PIN1
>40mils trace
Close to PIN26
Close to PIN40
Close to PIN27,39
Close to PIN28
Close to PIN7
Close to Pin 9
Close to Pin 34,35,36
Close to Pin 41
Close to Pin 46
Close to codec
Speaker 4 ohm: 40mils
Layout concern
TO Audio Jack MIC
TO Internal Speakers
check value
Check layout mount location
Close to CODEC
place to near U10013 or under U10013
PV change to shortpad
PV change from 0R for EMI solution
PV add for EMI solution
Digital MIC
for intel HSW ULT
Vset=1.242V
Analog
Digital
U27
ALC3227 x QFN48
U24
*TPS793475DBVR
HPA01091DBVR
*AZ2015-01H
DMG1012T-7(SOT523)
FOR EMI
https://t.me/schematicslaptop
https://t.me/biosarchive
PROJECT :Y61
Quanta Computer Inc.
Azalia ALC 3227
Size Custom
Document Number
Rev 1A
Date: Monday, April 21, 2014
Sheet 17 of 32

Head Phone out

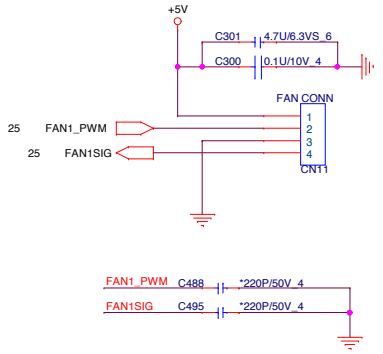


TPA6133A2
HPA022642RTJR

Audio Board



FAN



https://t.me/schematicslaptop
https://t.me/biosarchive

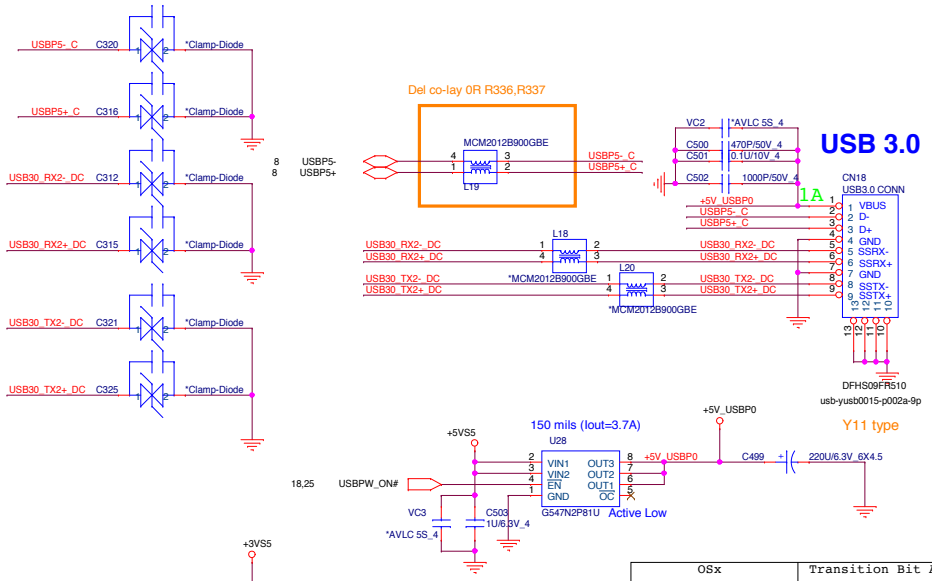
6,7,8,9,10,11,12,13,14,15,16,17,19,21,22,23,24,25,26,31,32 +3V
16,17,21,22,23,32 +5V
13,20,28,29,30,31,32 +5VS5

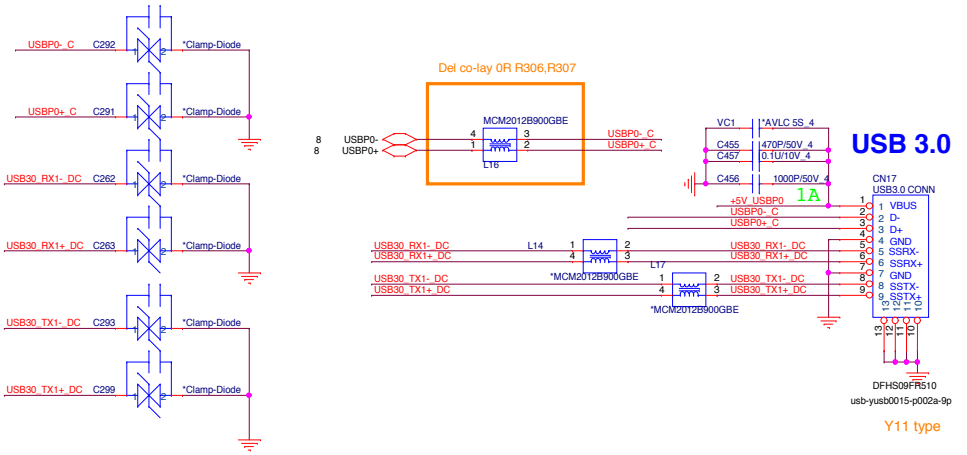
PROJECT :Y61
Quanta Computer Inc.

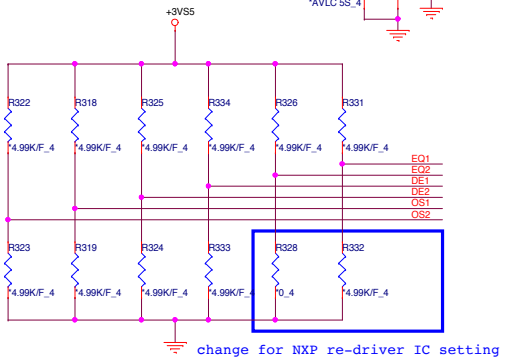
Size	Document Number	Rev
Custom	Audio/AMP HPA022642RTJR	1A

Date: Monday, April 21, 2014 Sheet 18 of 32

USB 2.0/3.0 Combo







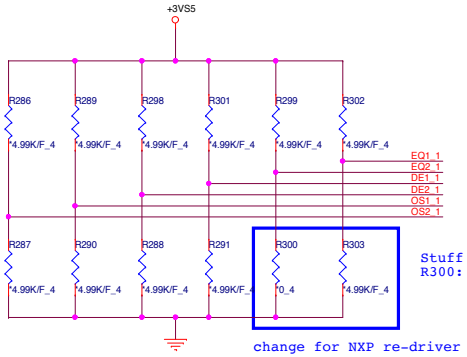
OSx	Transition Bit Amplitude
NC(default)	1000
0	870
1	1085

EQx	Equalization dB
NC(default)	0
0	7
1	15

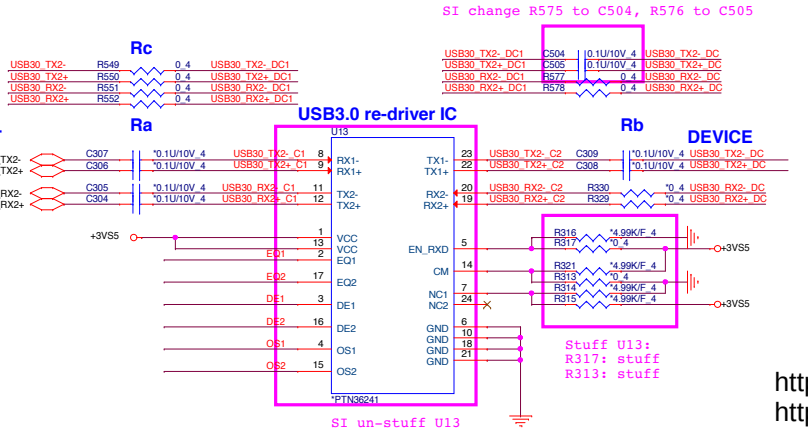
DEx	OSx=NC	OSx=0	OSx=1
NC	-3.5dB	-2.2dB	-4.4dB
0	-6.0dB	-5.2dB	-6.0dB
1	-8.5dB	-8.9dB	-7.6dB

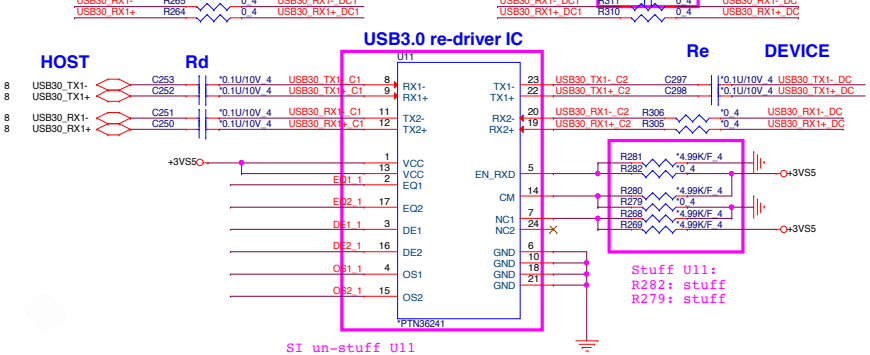
EN_RXD	DEVICE FUNCTION
1(default)	Normal operating mode
0	Sleep mode

CM	DEVICE FUNCTION
0(default)	Normal operating mode
1	Compliance mode



SI change R575 to C504, R576 to C505





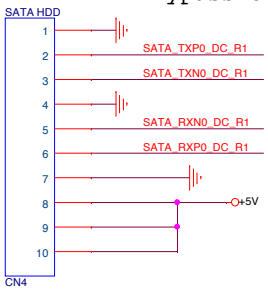
6,7,9,10,23,24,25,26,30,32 +3VS5
13,18,28,29,30,31,32 +5VS5
4,7,22,23,25,27,28 +3VPCU

PROJECT :Y61
Quanta Computer Inc.

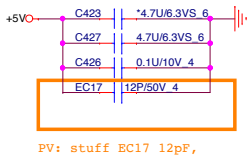
Size	Document Number	Rev
Custom	USB 3.0	1A
Date: Monday, April 21, 2014	Sheet 20 of 32	

SATA HDD Connector(Cable type)

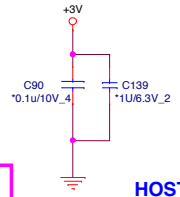
Bypass CAP close conn



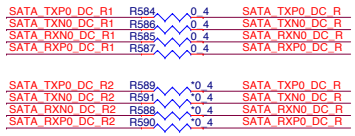
footprint check OK



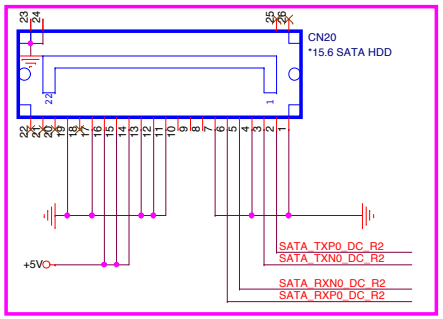
PV: stuff EC17 12pF,



SI add for co-lay use

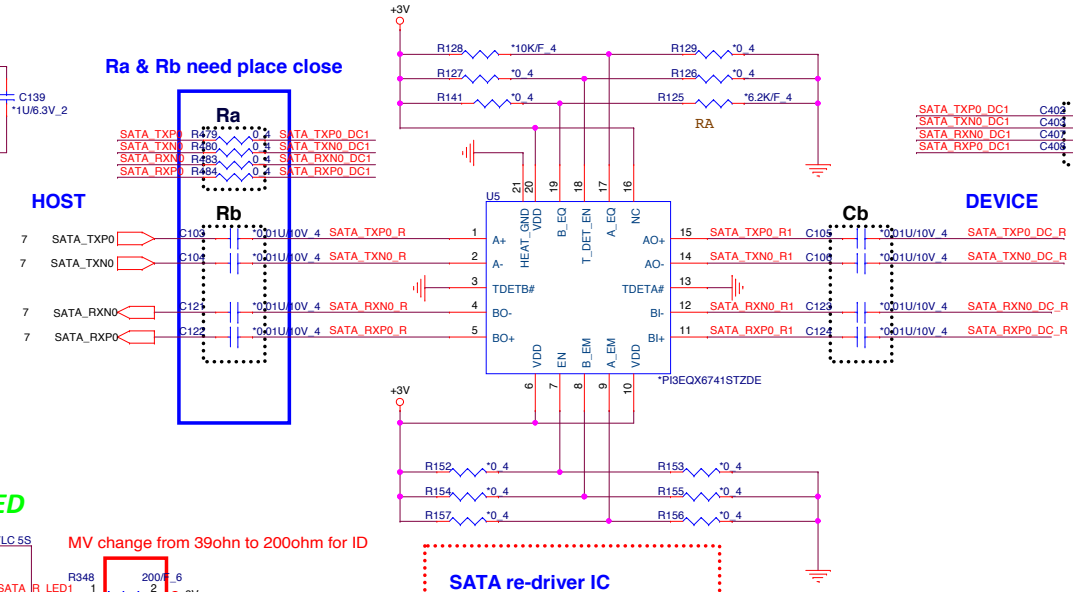


SI-co-lay SATA HDD Connector



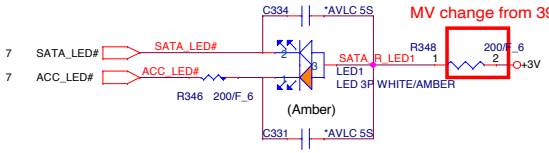
SATA Re-driver

Ra & Rb need place close



SATA LED

MV change from 39ohn to 200ohm for ID



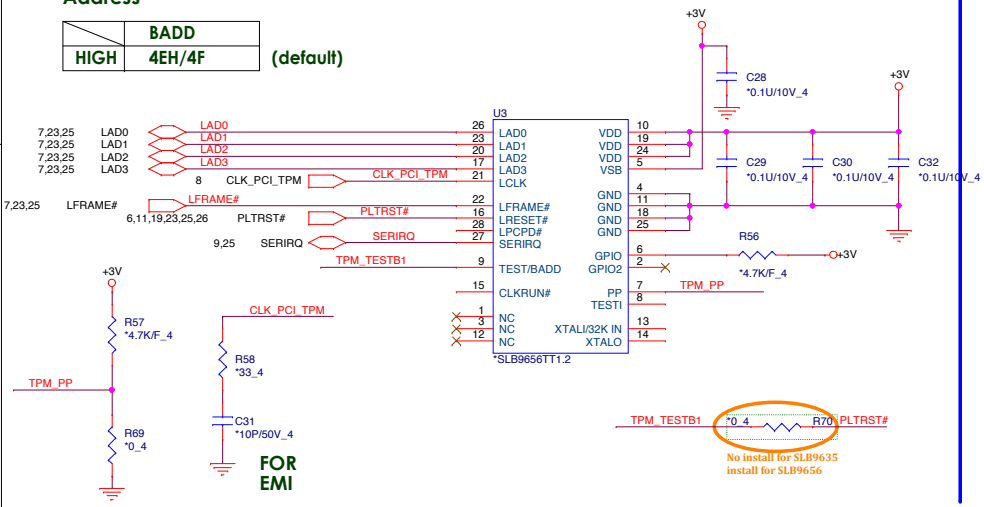
SATA re-driver IC
stuff Rb,Cb , unstuff Ra,Ca

unstuff SATA re-driver IC
stuff Ra,Ca , unstuff Rb,Cb

TPM (1.2)

Address

	BADD
HIGH	4EH/4F (default)



https://t.me/schematicslaptop
https://t.me/biosarchive

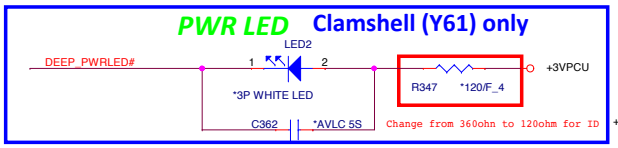
6,7,8,9,10,11,12,13,14,15,16,17,18,19,22,23,24,25,26,31,32 +3V
16,17,18,22,23,32 +5V
4,7,22,23,25,27,28 +3VPCU
27 BATT+

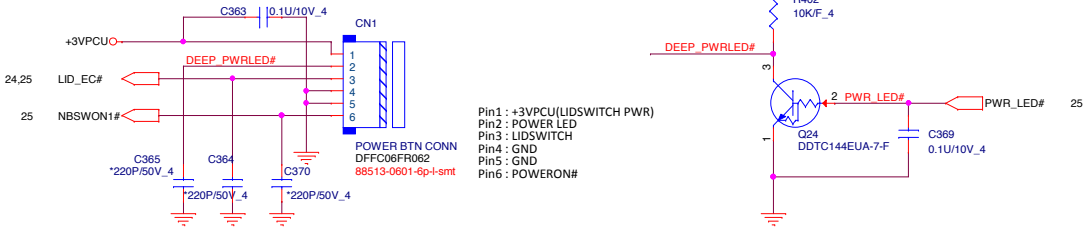
PROJECT :Y61
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDD/mSATA/FAN/LED	1A
Date: Monday, April 21, 2014	Sheet 21of 32	

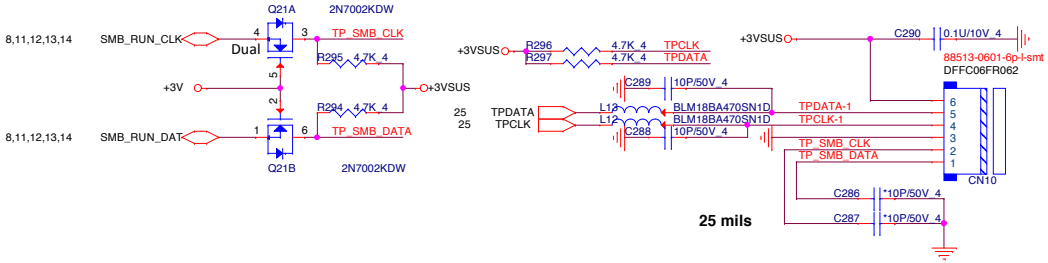
Power Botton Connector

PWR LED Clamshell (Y61) only

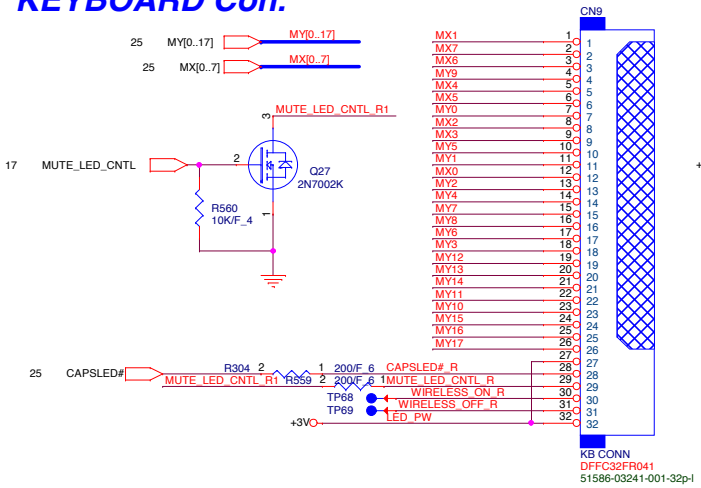




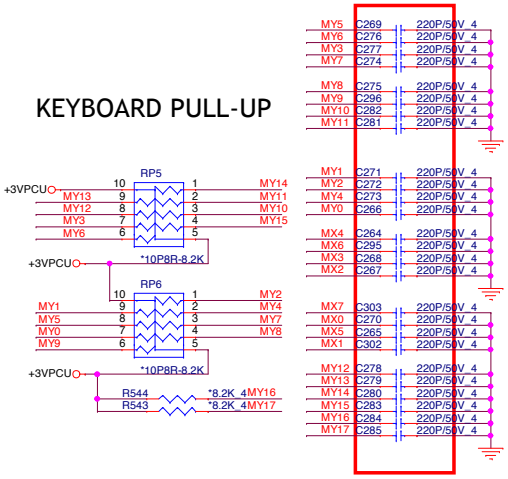
Touch Pad Connector



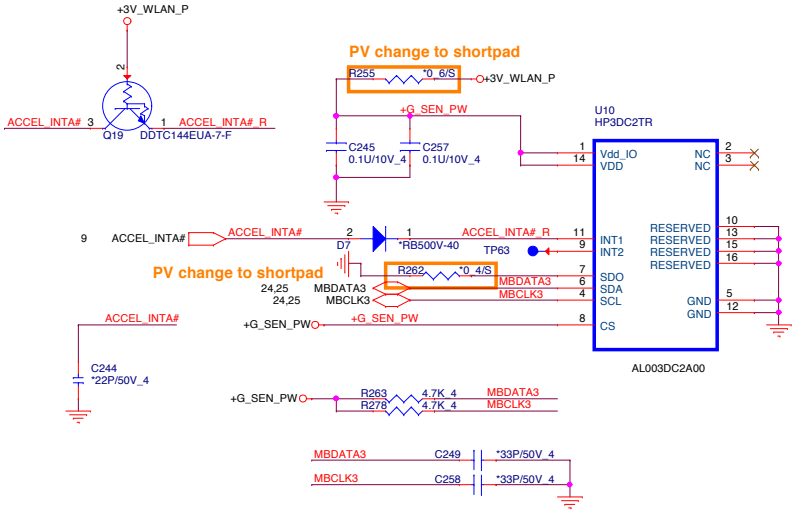
KEYBOARD Con.



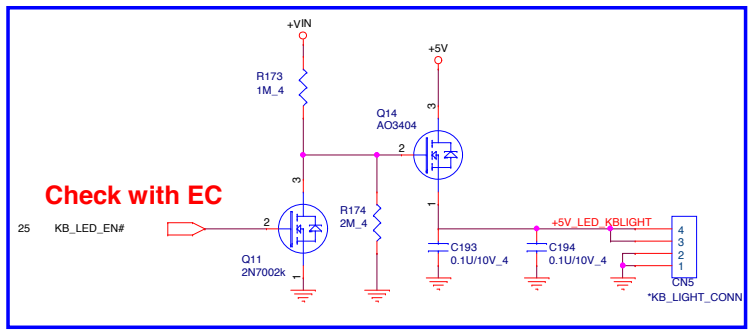
KEYBOARD PULL-UP



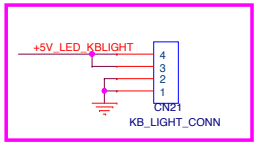
Accelerometer Sensor



15" KB backlight only



Co-lay



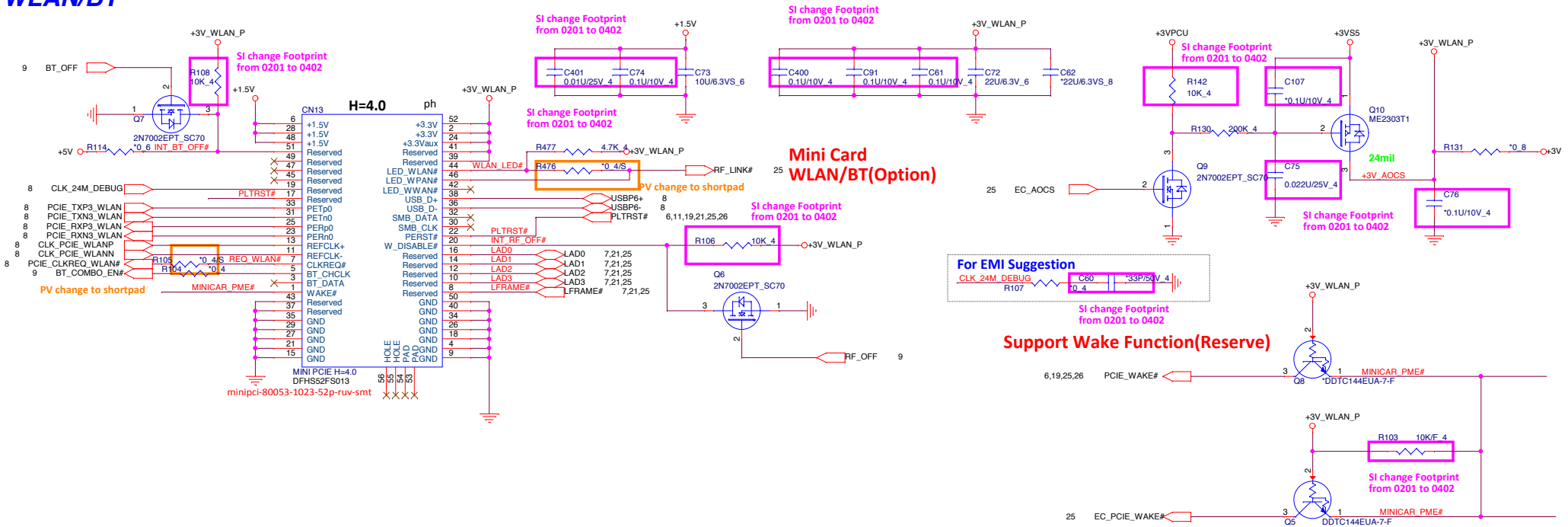
https://t.me/schematicslaptop
https://t.me/biosarchive

6,7,8,9,10,11,12,13,14,15,16,17,18,19,21,23,24,25,26,31,32 +3V
16,17,18,21,23,32 +5V
4,7,23,25,27,28 +3VPCU

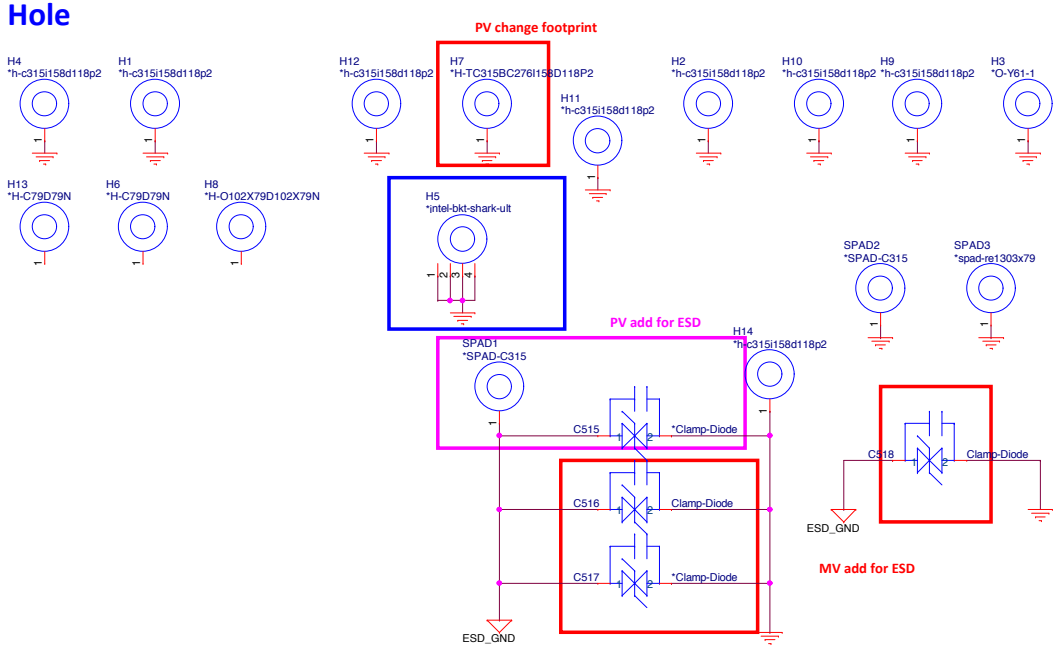
PROJECT :Y61
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PB/TP/KB/FAN/EMI Cap	1A
Date: Monday, April 21, 2014	Sheet 22 of 32	

WLAN/BT



Hole



https://t.me/schematicslaptop
https://t.me/biosarchive

27	+PRWSRC
6,7,8,9,10,11,12,13,14,15,16,17,18,19,21,22,24,25,26,31,32	+3V
16,17,18,21,22,32	+5V
4,7,22,25,27,28	+3VPCU

PROJECT :Y61
Quanta Computer Inc.

Size	Document Number	Rev
Custom	WLAN/G-Sensor/G-CLK/TS	1A
Date: Monday, April 21, 2014	Sheet 23of 32	

Accelerometer Sensor

Put it on MB side

Close to U9

Note: Place all capacitors close to IT8350.

20MIL

20MIL

20MIL 10MIL (For PLL Power)

U23
IT8350E_LQFP-48

IT8350E
LQFP-48

SM BUS
FSPI
PWM
UART
USB
A/D
SSPI
GPIO
CLOCK

Reserved SMBus channel 0 for debugging & updating FW
Reserved
SMbus channel 4 for connecting the Sensor (G-sensor)

To APU

To EC SMBUS

To Sensor Hub SMBUS

USB for Host

SI short L33

Reserved TX/RX for debugging

if no use ADC function,
please pull down to GND
SMINTx for sensor interrupt

PV change to shortpad

GPG2 can't floating

GPG2 Pull High Enable mirror function.
GPG2 Pull Low Disable mirror function.

3 IN 1-Sensor
connector to HOME IC

Touch screen

For Home button IC update fw

SI co-lay 6 pin TS CON

SI short L4

External crystal is must be item
when USB func. is used !

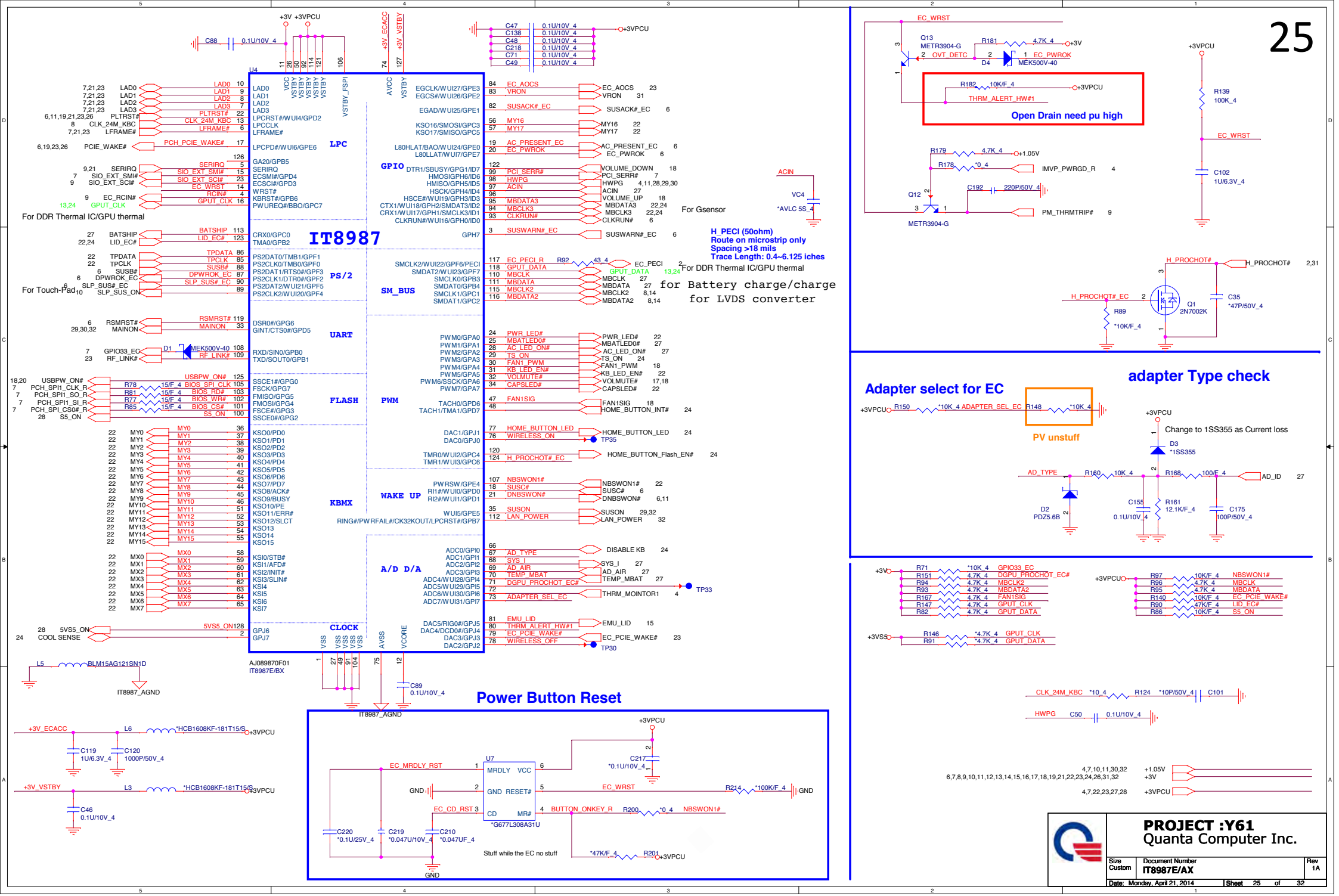
32.768kHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.

https://t.me/schematicslaptop
https://t.me/biosarchive

PROJECT :Y61
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ITE8350/HP9DS0/HP3DC2	1A

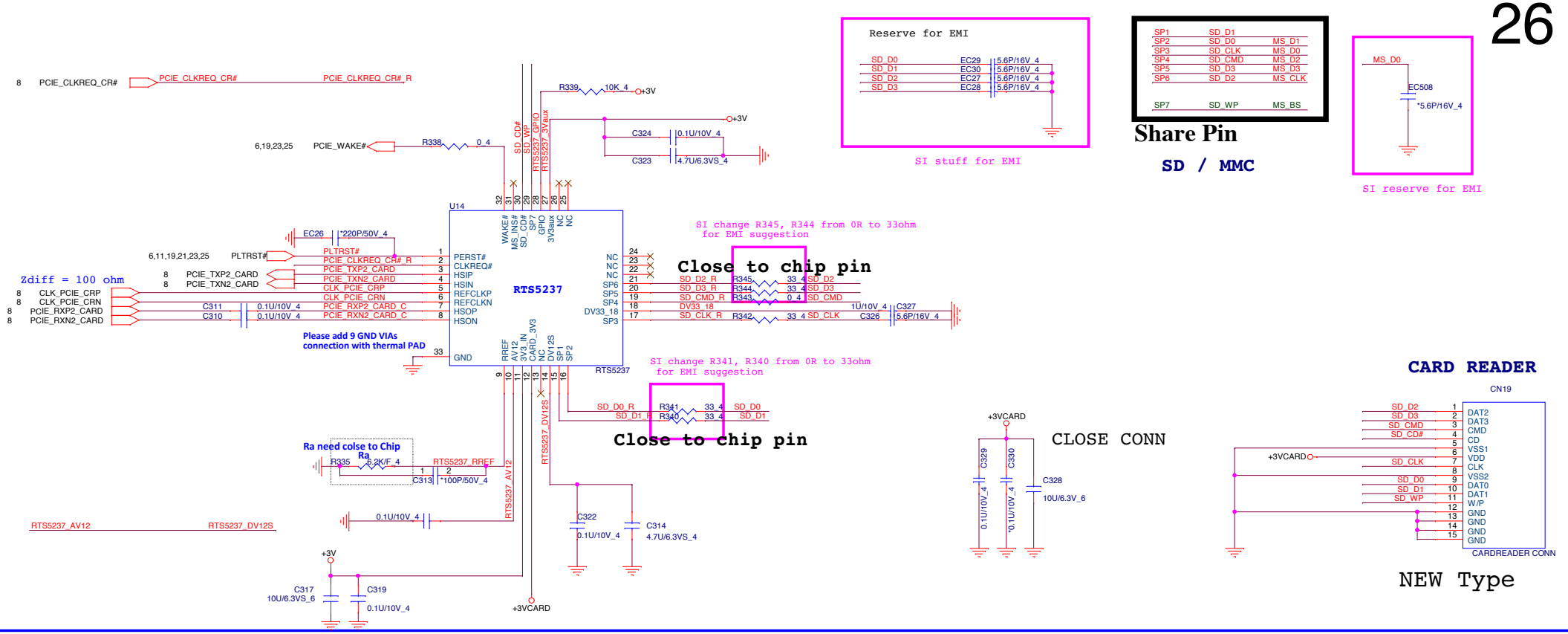
Date: Monday, April 21, 2014 Sheet 24 of 32



PROJECT :Y61
Quanta Computer Inc.

Size	Document Number	Rev
Custom	IT8987E/AX	1A

Date: Monday, April 21, 2014 Sheet 25 of 32



https://t.me/schematicslaptop
https://t.me/biosarchive

PROJECT :Y61 Quanta Computer Inc.		
Size: Custom	Document Number: CR RTS5237 & HOLE	Rev: 1A
Date: Monday, April 21, 2014	Sheet 26 of 32	

DC_JACK/65W

Place this ZVS close to Diode away +VIN

Do Not add test pad on BATDIS_G signal

EMI request for ISN

Place this cap close to EC

15.6"

Place this ZVS close to Far-Far away +VIN

EMI request for ISN

ACDET=13V

MIN. BATV=7.2V

Setting MAX Icharge to 5A

Place this cap close to EC

Place this cap close to EC

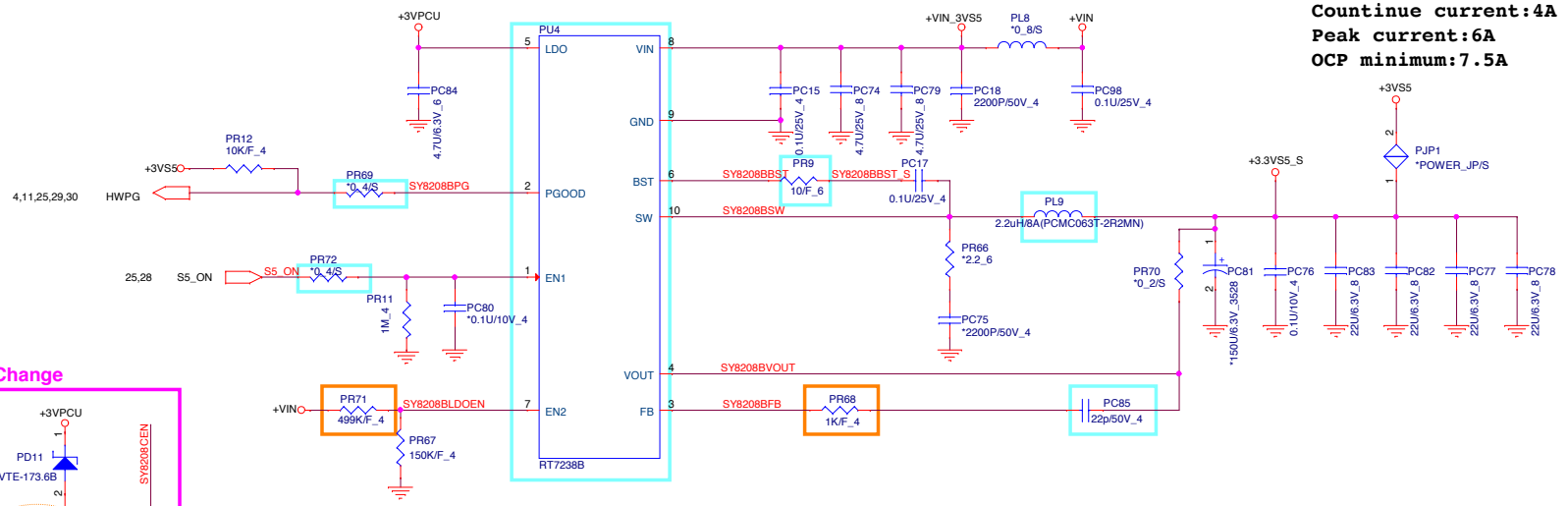
PU8 BQ24738H

+3VPCU 4,7,22,23,25,28
+5VPCU 13,28
BATT+
+PRWSRC

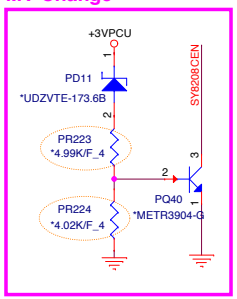
PROJECT :NAPA	
Quanta Computer Inc.	
Size: Custom	Document Number: Charger (BQ24738H)
Rev: 1A	
Date: Monday, April 21, 2014	Sheet 27 of 32

+3VS5 6,7,9,10,20,23,24,25,30,32
+5VS5 13,18,20,29,30,31,32

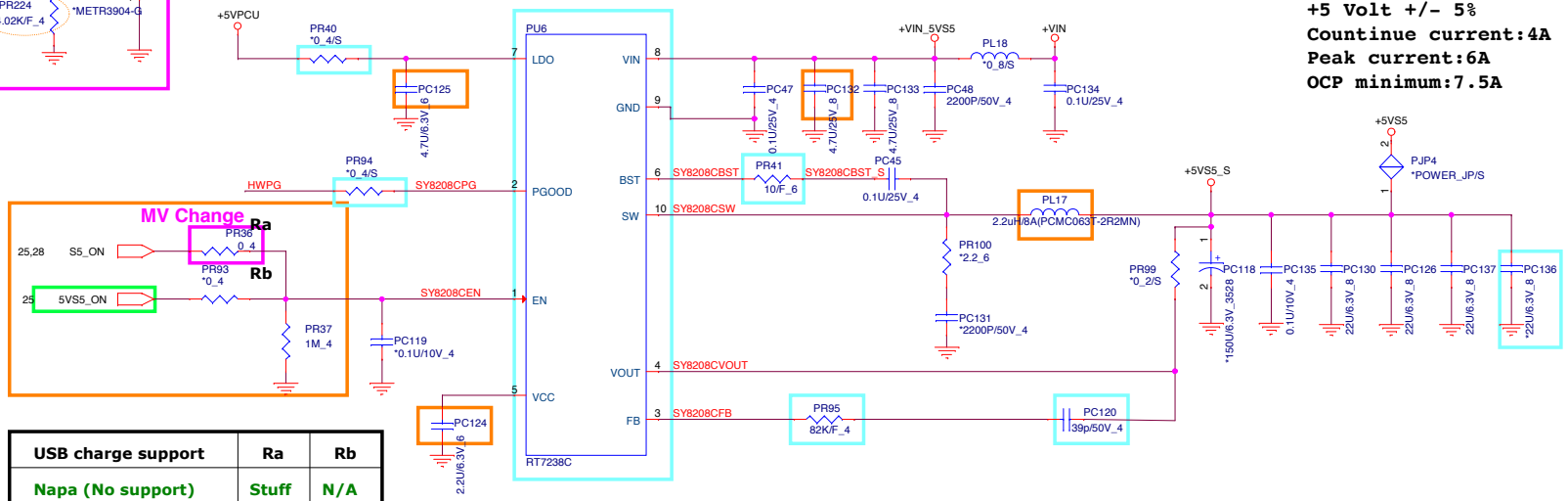
+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A



MV Change



+5 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

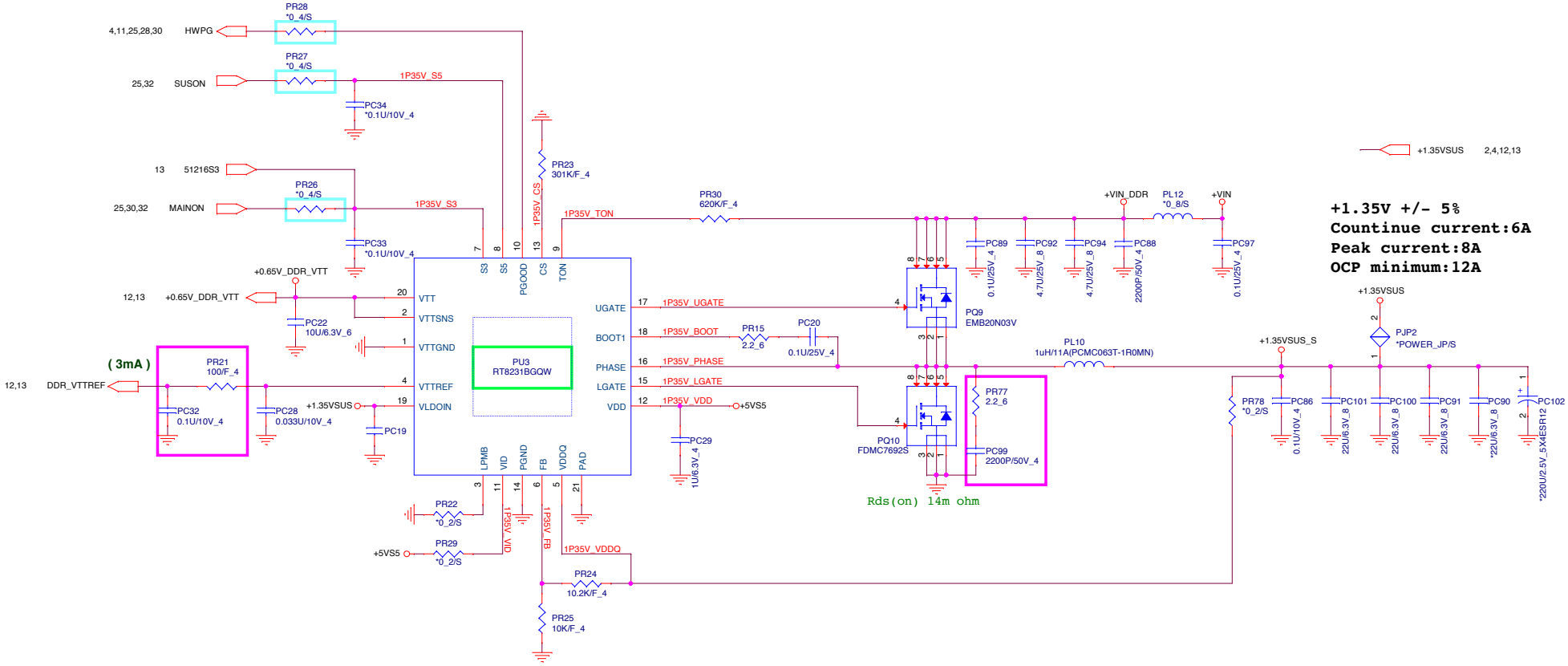


USB charge support	Ra	Rb
Napa (No support)	Stuff	N/A
Whisky (Support)	N/A	Stuff

https://t.me/schematicslaptop
https://t.me/biosarchive

PROJECT :NAPA
Quanta Computer Inc.

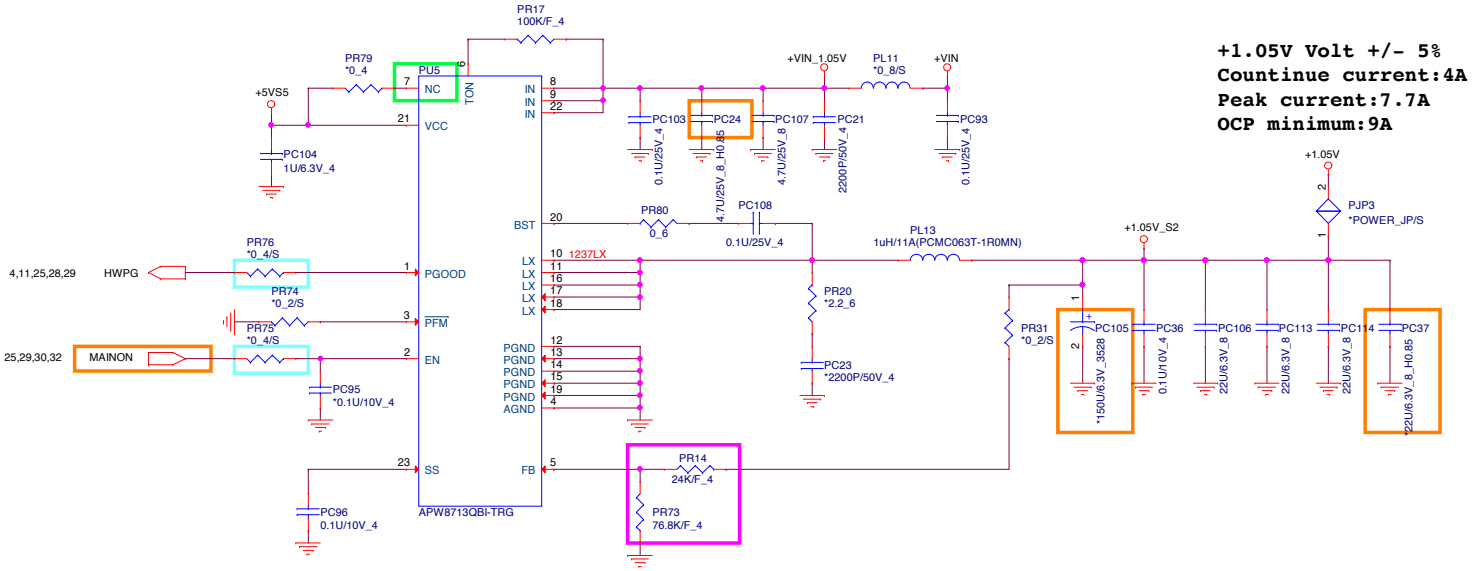
Size	Document Number	Rev
Custom	3/5VS5 (SY8208B/SY8208C)	1A
Date: Monday, April 21, 2014	Sheet 28 of 32	



PROJECT :NAPA
Quanta Computer Inc.

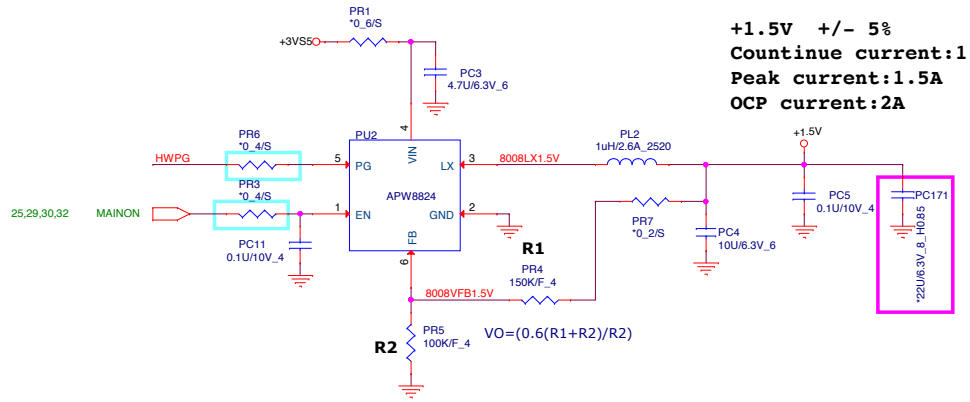
Size	Document Number	Rev
Custom	DDR3 (RT8231B)	1A

Date: Monday, April 21, 2014 Sheet 29 of 32

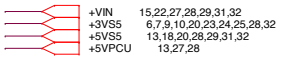


+1.05V Volt +/- 5%
Countinue current:4A
Peak current:7.7A
OCP minimum:9A

https://t.me/schematicslaptop
https://t.me/biosarchive



+1.5V +/- 5%
Countinue current:1.3A
Peak current:1.5A
OCP current:2A



PROJECT :NAPA
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.05V (APW8713)/1.5V	1A
Date: Monday, April 21, 2014	Sheet 30 of 32	

ULV 15W	ULV 28W
Vboot :1.7V	Vboot :1.7V
Icc TDC PL2: 14A	Icc TDC PL2: 19A
Icc Max= 32A	Icc Max= 40A
O.C.P.=38A	O.C.P.=48A
R_DC_LL : -2.0 mV/A	R_DC_LL : -2.0 mV/A
R_AC_LL : -7.0 mV/A	R_AC_LL : -7.0 mV/A

CPU	Re	P/N
15W	90.9K	CS39092FB11
28W	113K	CS41132FB17

CPU	Re	P/N
15W	88.7K	CS38872FB18
28W	95.3K	CS39532FB03

CPU	Re	P/N
15W	270	CS12702FB12
28W	324	CS13242FB07

CPU	Re	P/N
15W	1.21K	CS21212FB18
28W	1.62K	CS21622FB17

slew rate=53A/us, Vboot=1.7V

DCR = 0.6 m-ohm +/- 7%

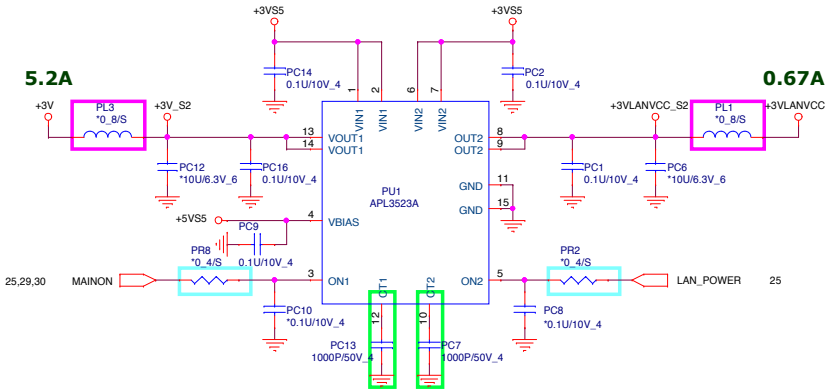
Ra PLACE NEAR Hi side MOSFET

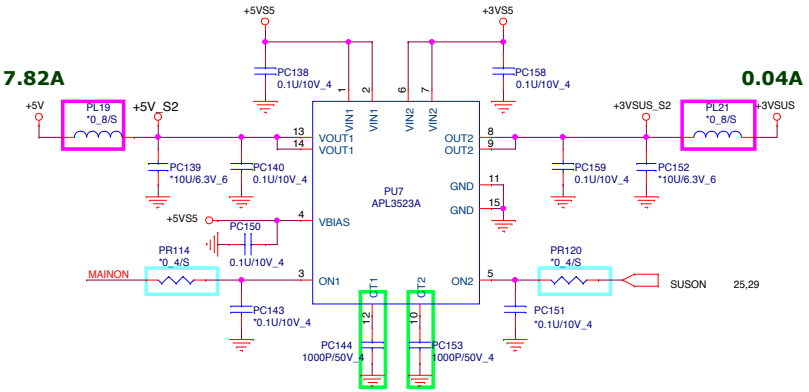
https://t.me/schematicslaptop
https://t.me/biosarchive

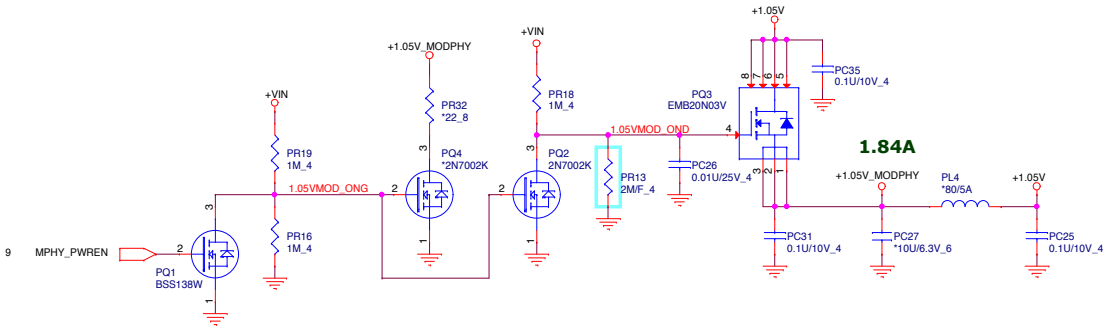
PROJECT :NAPA
Quanta Computer Inc.

Size	Document Number	Rev
	CPU_CORE(ISL95813) 15W	1A

Date: Monday, April 21, 2014 Sheet 31 of 32







6,7,8,9,10,11,12,13,14,15,16,17,18,19,21,22,23,24,25,26,31 +3V
16,17,18,21,22,23 +5V
15,22,27,28,29,30,31 +VIN
6,7,9,10,20,23,24,25,28,30 +3VS5
13,18,20,28,29,30,31 +5VS5
19 +3VLANVCC

PROJECT :NAPA
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Load switch IC (APL3523A)	1A
Date: Monday, April 21, 2014	Sheet 32 of 32	