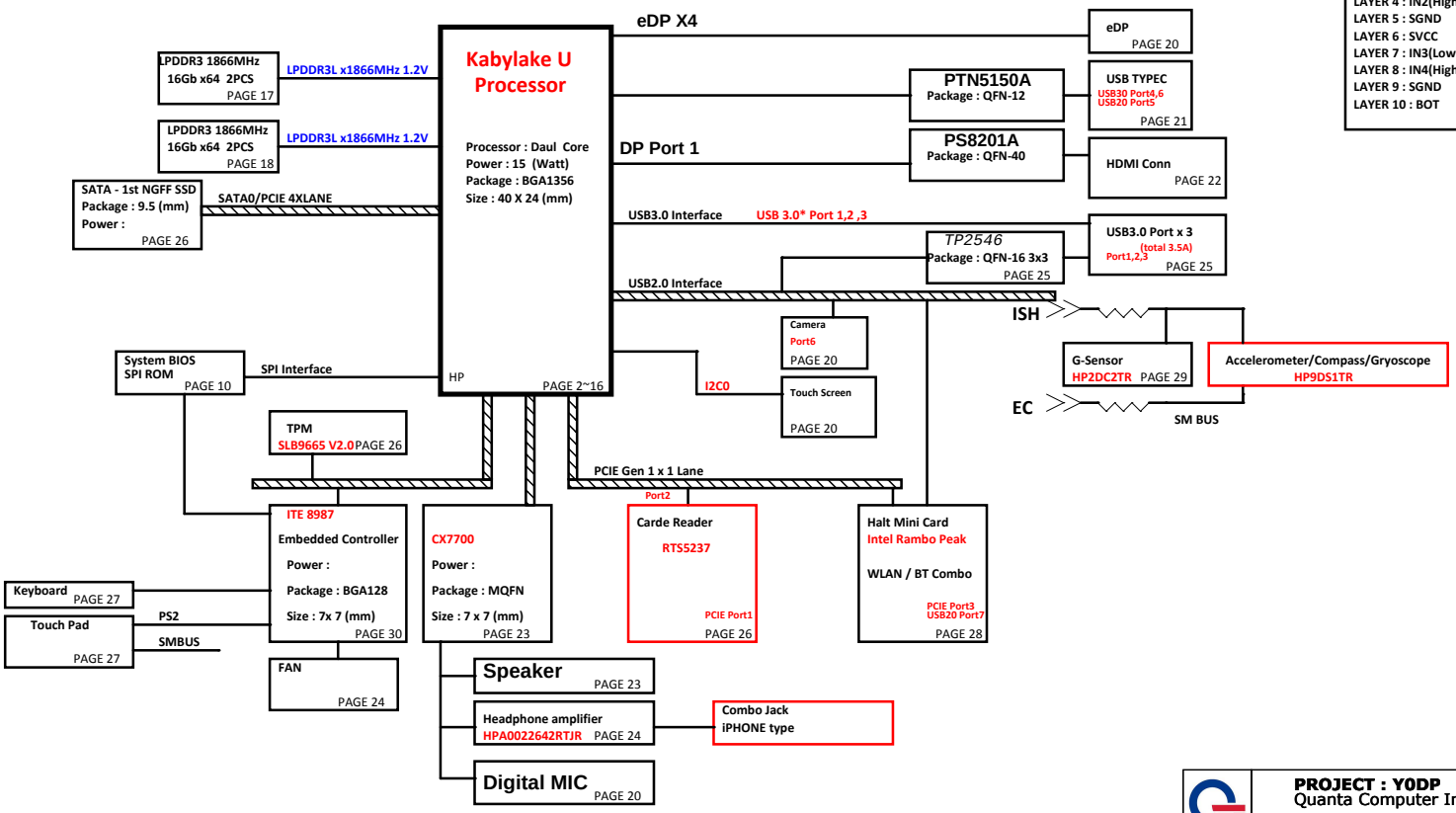
Pavlova Intel KABYLAKE ULT Platform Block Diagram

PCB 10L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(High)
LAYER 5 : SGND
LAYER 6 : SVCC
LAYER 7 : IN3(Low)
LAYER 8 : IN4(High)
LAYER 9 : SGND
LAYER 10 : BOT



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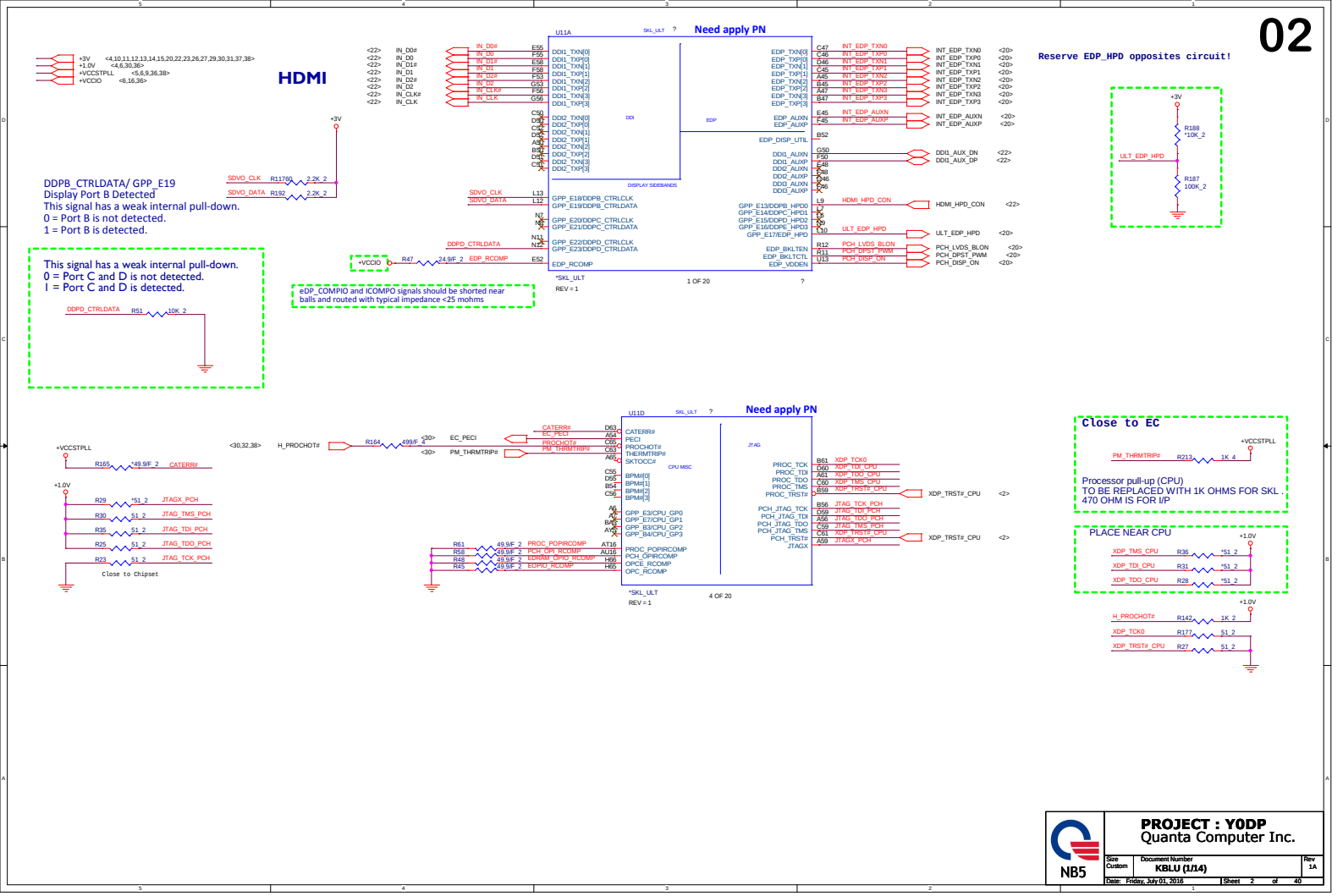

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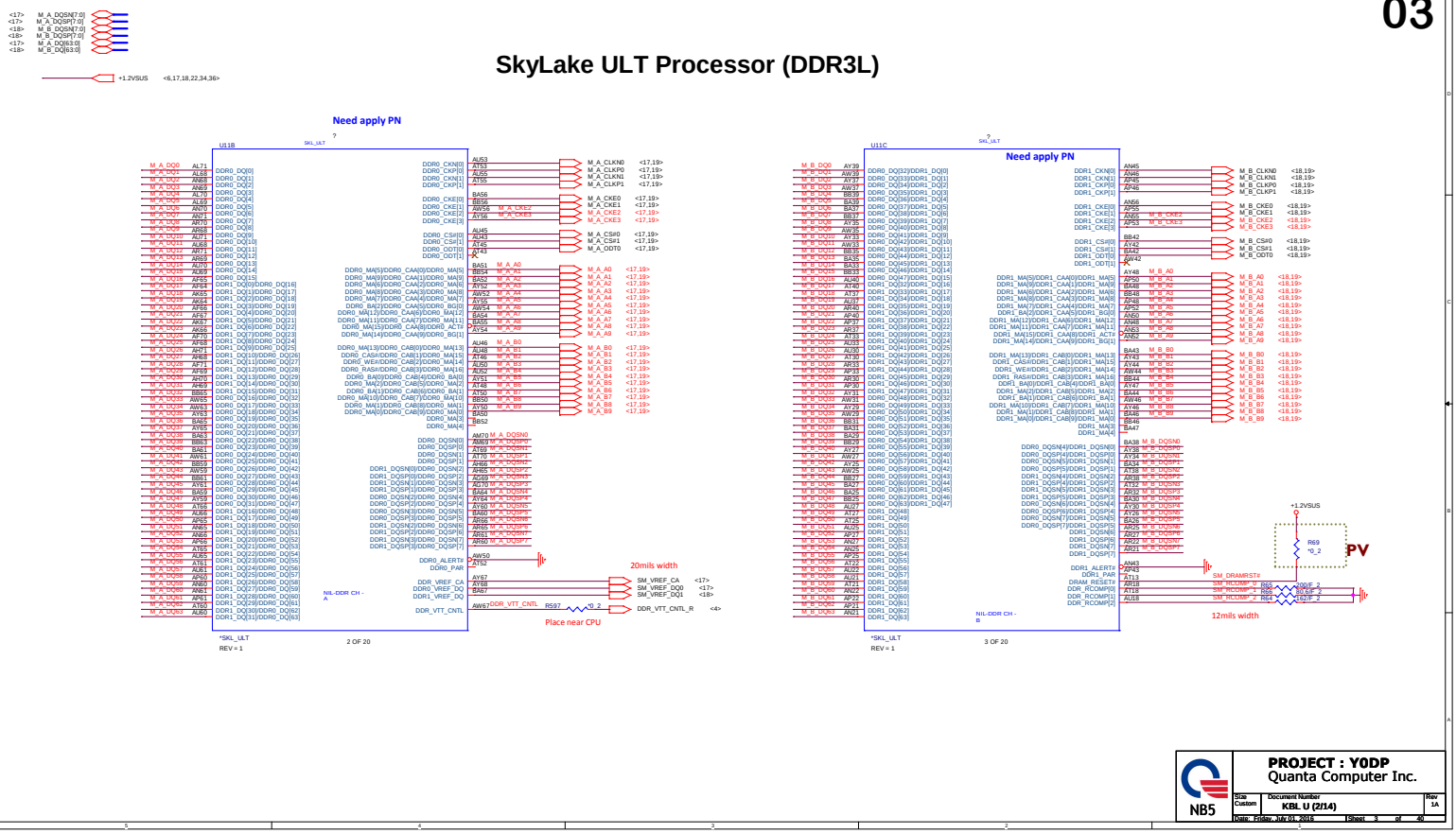
SkyLake ULT Processor (DDR3L)



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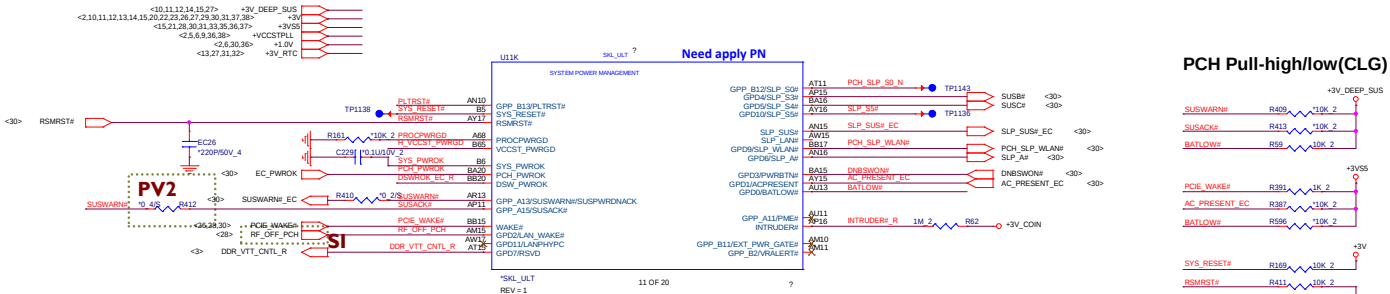
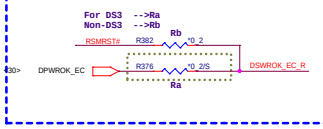


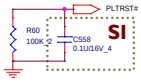
PCH Pull-high/low(CLG)

For DS3 Sequence



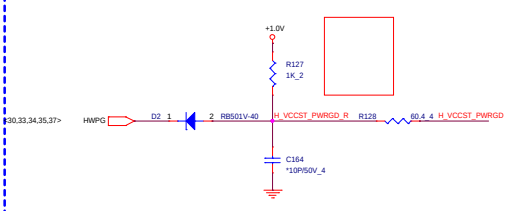
PLTRST#(CLG)

Check Q2010 Rise/Fall time less than 100ns

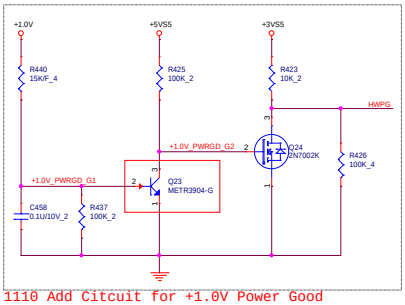


System PWR_OK(CLG)

1211 Del
+VCCSTPLL and R134



R10479 close to CPU side
H_VCCST_PWRGD trace 0.3" - 1.5"



1110 Add Citcuit for +1.0V Power Good

1118 Change Change Q7062 P/N from BA051440000 to BA039040020, Del D7002,D7003, R10526, R10527

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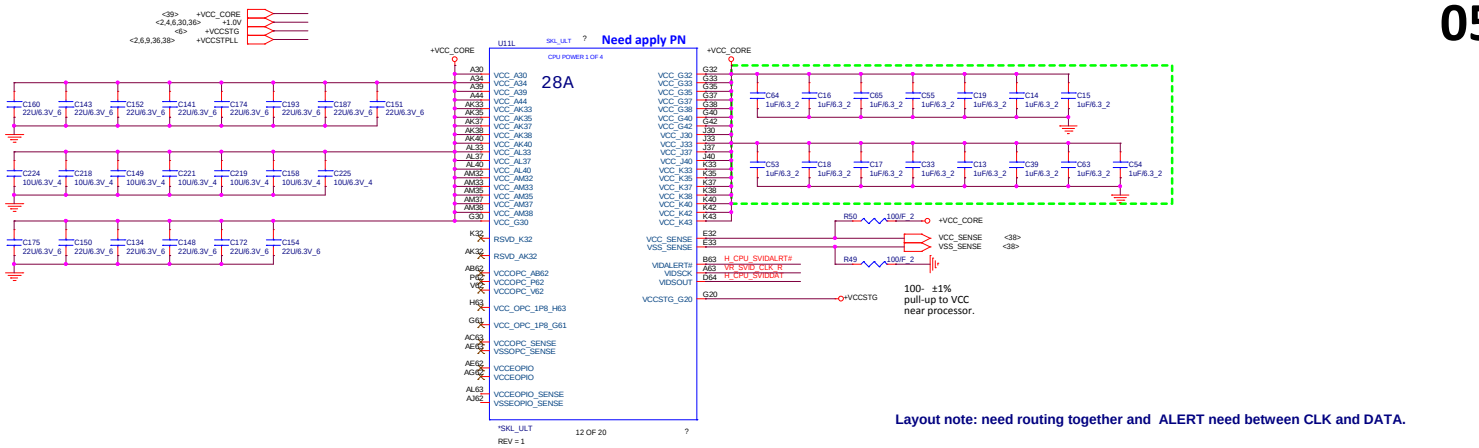
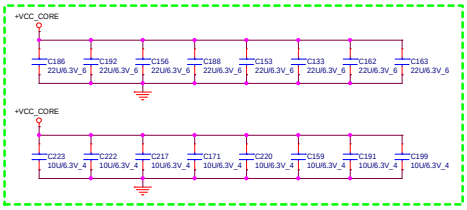
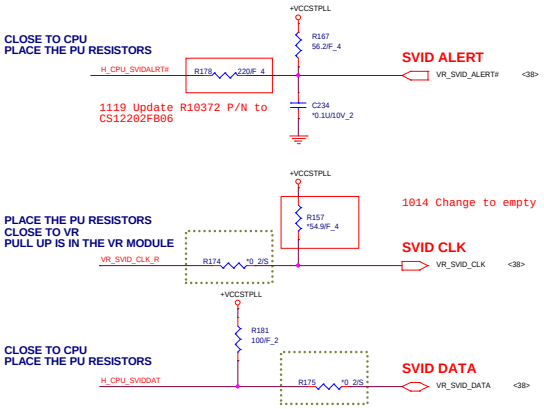


Close U11



Layout note: need routing together and ALERT need between CLK and DATA.



Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

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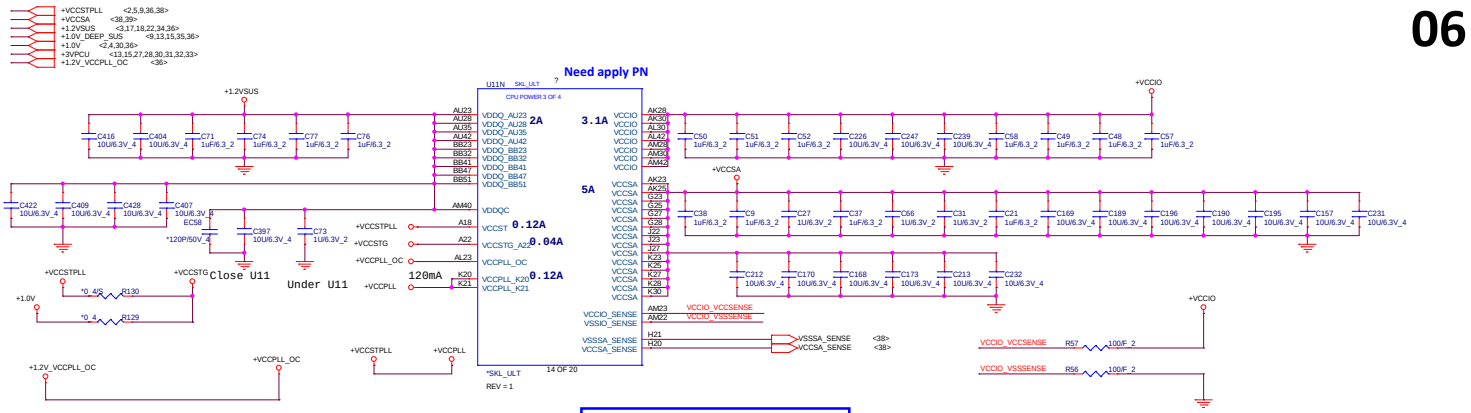

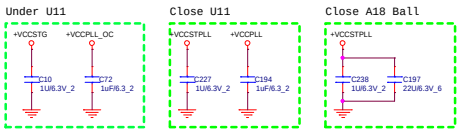

IO Thrm Protect

For 65 degree, 1.8v limit, (SW)

PV

For 75 degree, 1.2v limit, (HW)

Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
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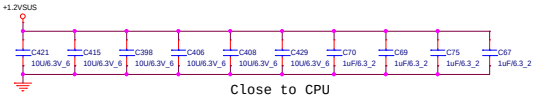

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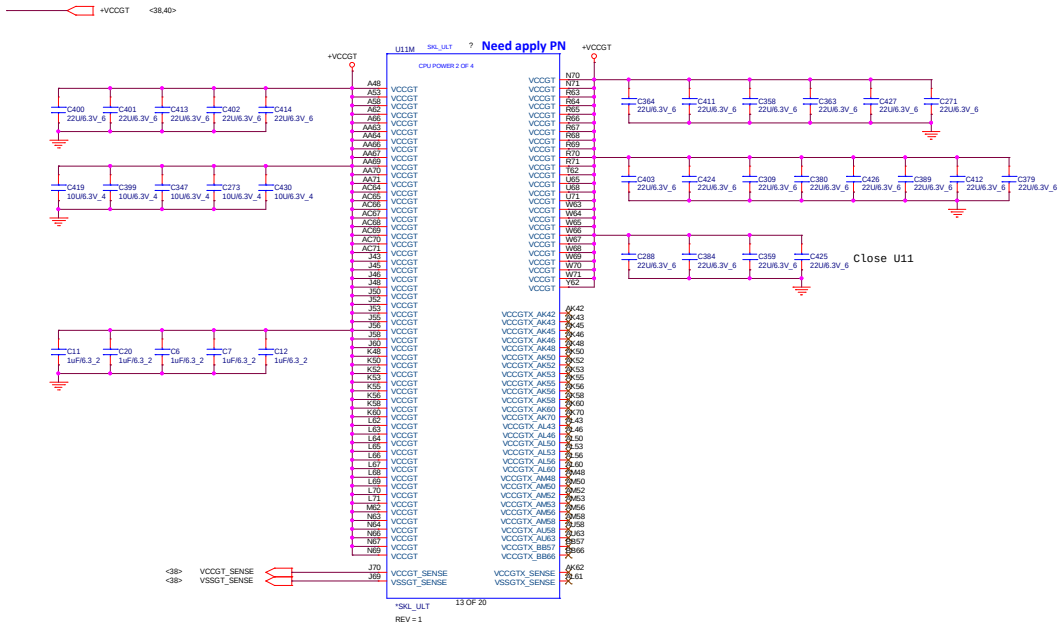

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Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

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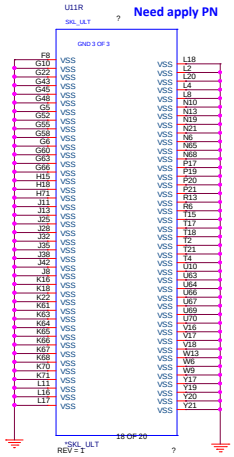

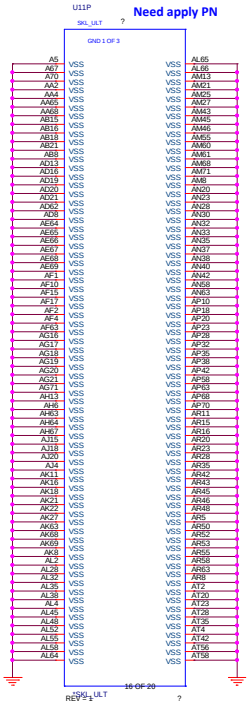

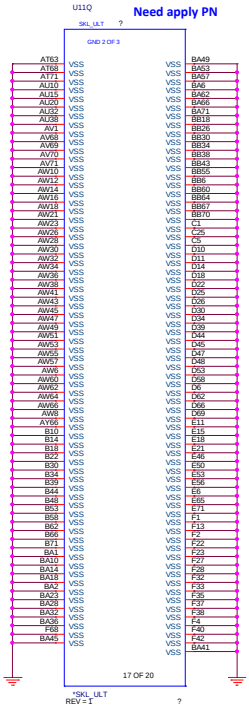

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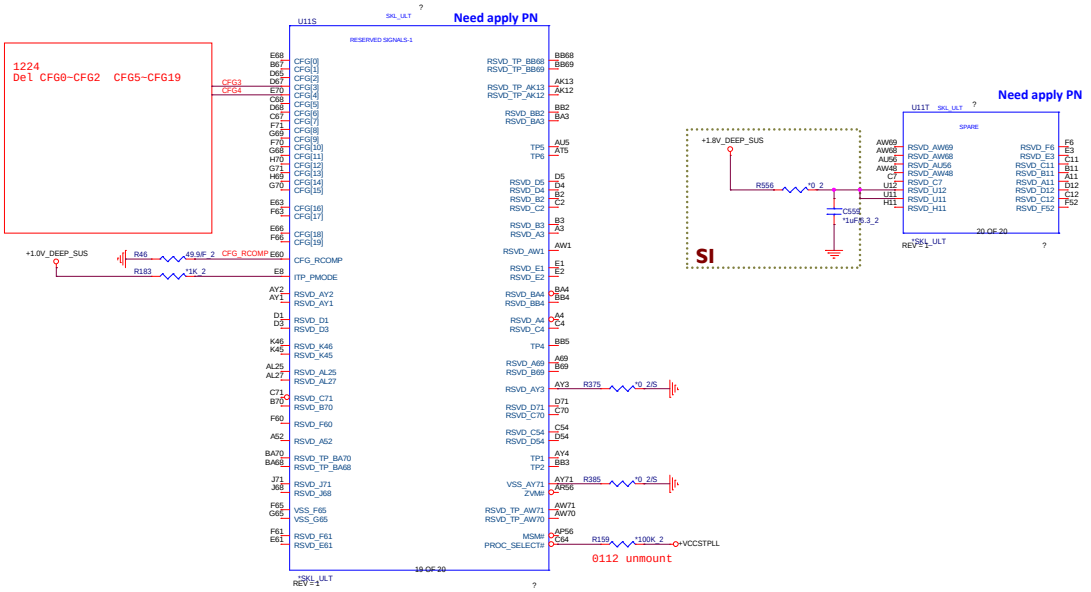

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physcial Debug Enable) DFX_Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	CFG3 R143 *1K_2
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	CFG4 R42 1K_2

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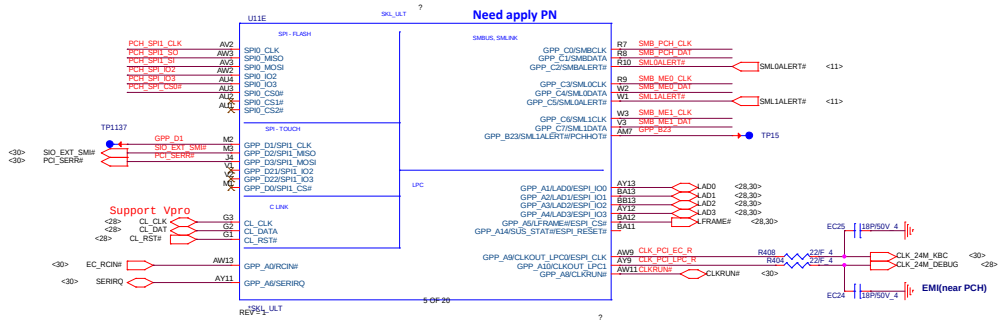
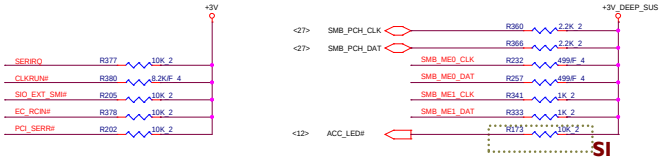
+3V_DEEP_SUS <4,11,12,14,15,27>
+3V <2,4,11,12,13,14,15,20,22,23,26,27,29,30,31,37,38>
+5V <22,23,24,27,37>
+1.0V <2,4,6,30,36>
+3VS5 <4,15,21,28,30,31,33,35,36,37>



GPIO Pull UP



SMBus/Pull-up(CLG)

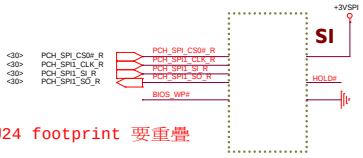
1230
Change net name from SMB_RUN_CLK to SMB_PCH_CLK
Change net name from SMB_RUN_DAT to SMB_PCH_DAT

Touch Pad
XDP

PCH SPI ROM(CLG)

Vender	Size	P/N
EON	8MB	AKE3EZN0Q01 (EN25QH64-104HIP)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)
Socket		DFHS08FS023

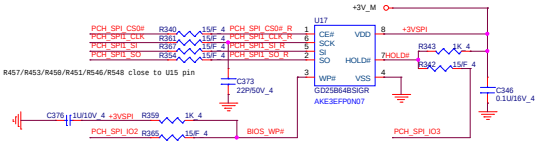
4M SPI ROM Socket



U23&U24 footprint 要重疊

PCH SPI ROM(CLG)

<15> +3V_M



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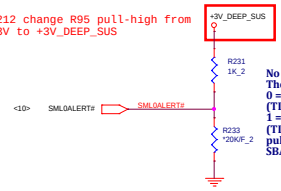
Functional Strap Definitions

DESIGN NOTE:
WEAK PULL UP RESISTOR PRESENT ON THIS NET

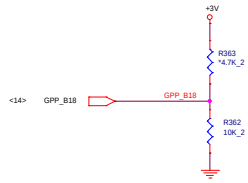
TOP SWAP OVERRIDE
HIGH - TOP SWAP ENABLE
LOW-DISABLED
HIGH: LPC SELECTED FOR SYSTEM FLASH
WEAK INTERNAL PD

No Boot:
The signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.

1212 change R95 pull-high from +3V to +3V_DEEP_SUS



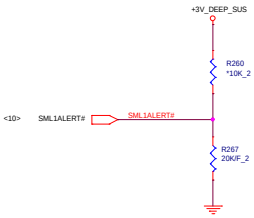
No Boot:
The signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.



No Boot:
The signal has a weak internal pull-down.
0 = Disable No Reboot mode.
1 = Enable No Reboot mode
(PCH will disable the TCO Timer system reboot feature).
This function is useful when running ITP/XDP.

No Boot:
The signal has a weak internal pull-down.
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.

Bit 10	Boot BIOS Destination
0	SPI
1	LPC



No Boot:
The signal has a weak internal pull-down.
0 = LPC Is selected for EC.
1 = eSPI Is selected for EC.

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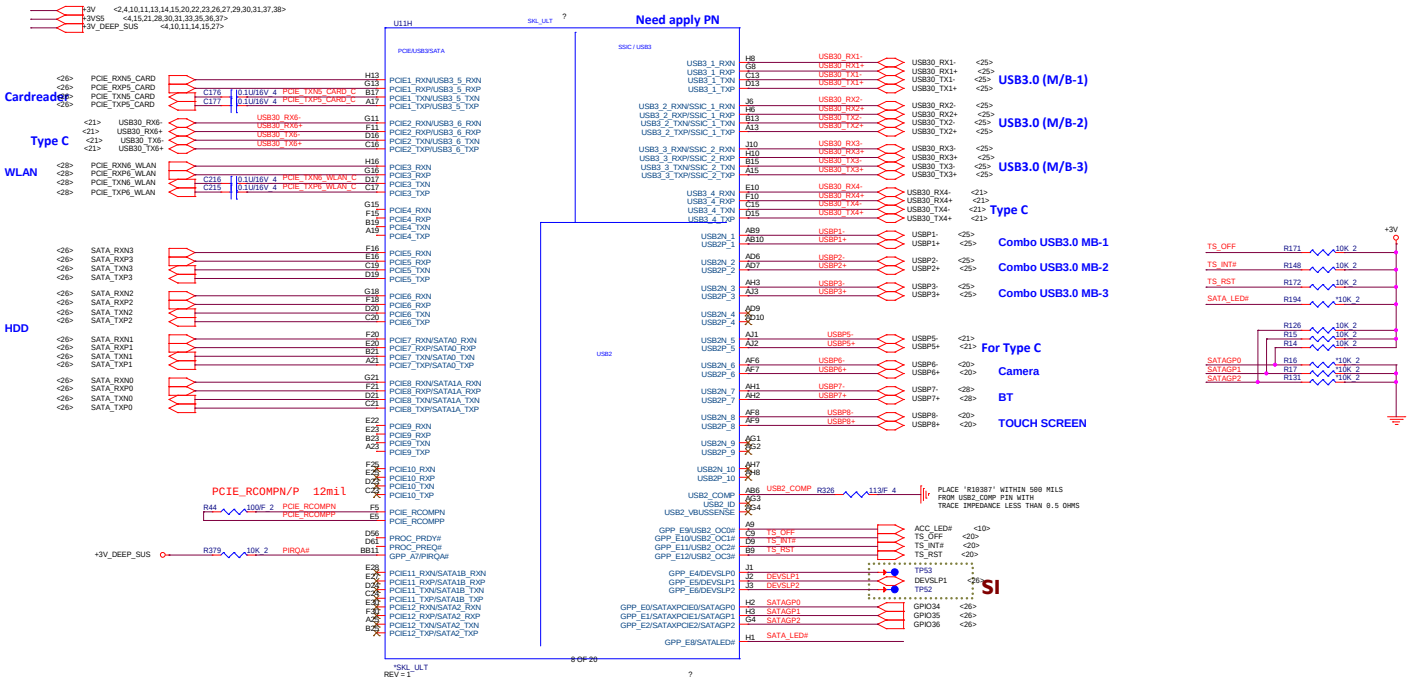

PCI-E Port Mapping Table

PCI-E Port	Function	CLK RQ Port	Function
Port1	CardReader	Port0	Un-used
Port2	Un-used	Port1	CardReader
Port3	WLAN	Port2	WLAN
Port4	Un-used	Port3	Un-used
Port5	SSD	Port4	Un-used
Port6	SSD	Port5	SSD
Port7	SSD		
Port8	SSD		
Port9	Un-used		
Port10	Un-used		

USB3.0 Port Mapping Table

USB3.0	Function
PORT-1	USB3.0 MB-2
PORT-2	USB3.0 MB-3
PORT-3	USB3.0 MB-4
PORT-4,6	TYPEC

USB2.0 Port Mapping Table

USB2.0	Function
PORT-1	USB3.0 MB-1
PORT-2	USB3.0 MB-2
PORT-3	USB3.0 MB-3
PORT-4	NC
PORT-5	TYPEC
PORT-6	Camera
PORT-7	WLAN
PORT-8	Touch Screen
PORT-9	NC
PORT-10	NC

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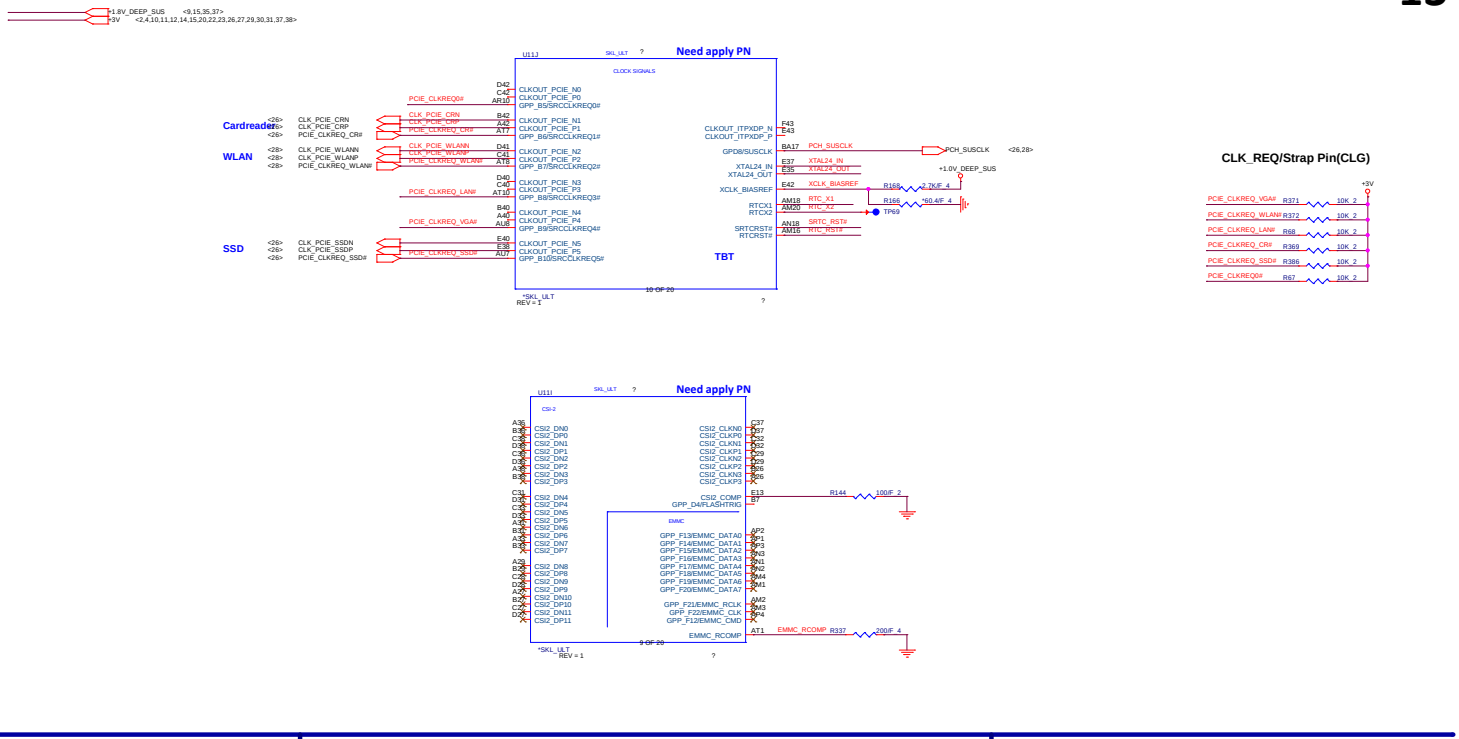
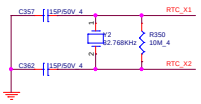
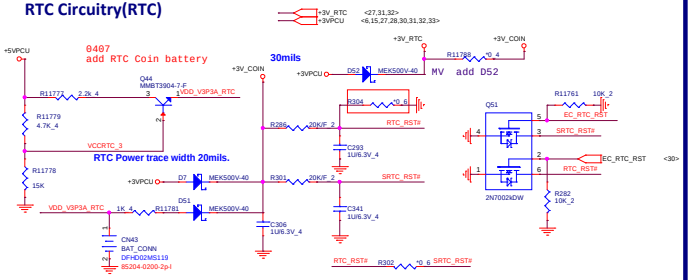


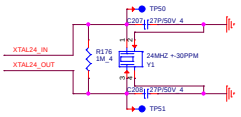
RTC Clock 32.768KHz



RTC Circuitry(RTC)



External Crystal



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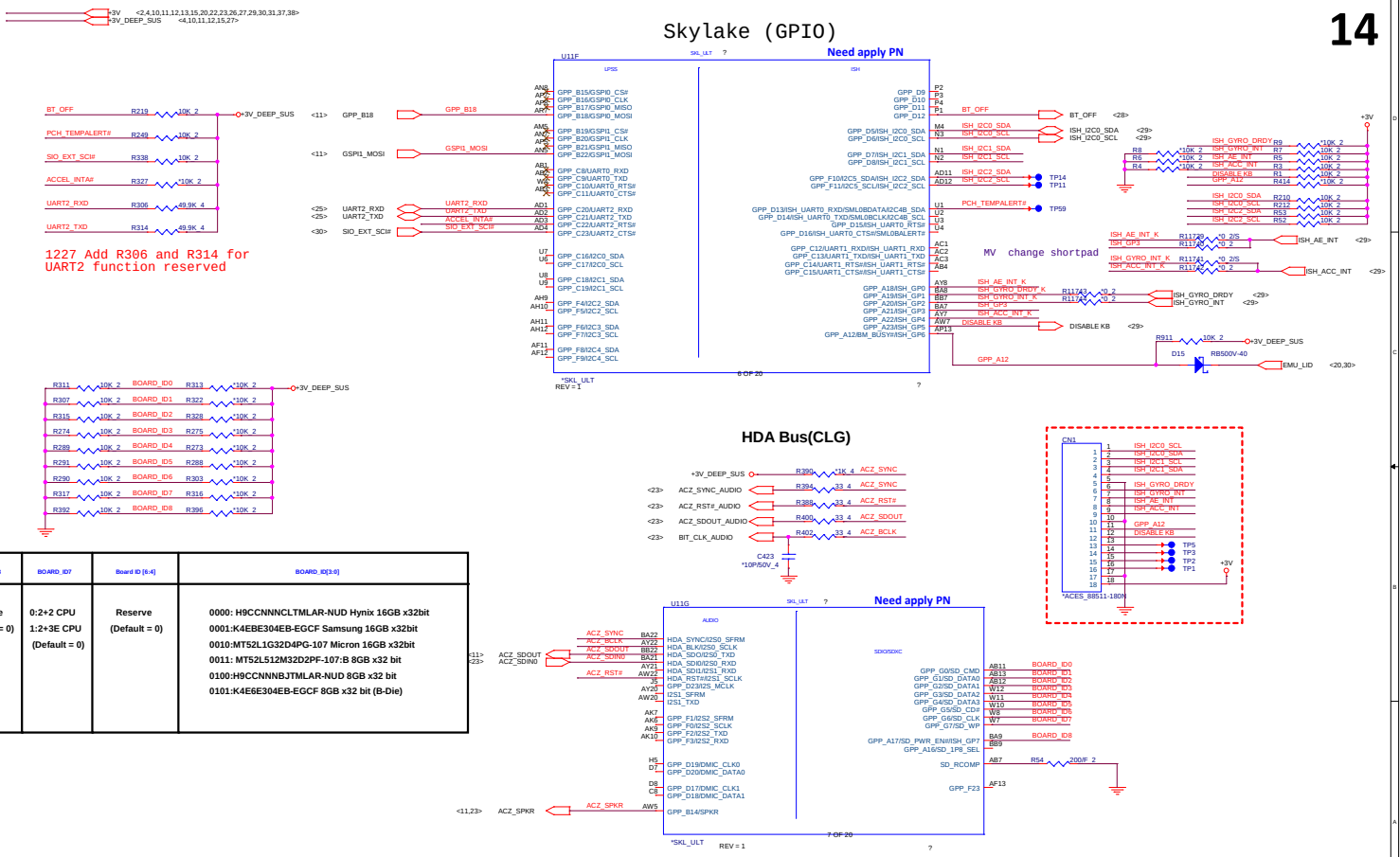
Skylake (GPIO)



Model	BOARD_ID8	BOARD_ID7	Board ID [6:4]	BOARD_ID[3:0]
Y0DP	Reserve (Default = 0)	0:2+2 CPU 1:2+3E CPU (Default = 0)	Reserve (Default = 0)	0000: H9CCNNNCLTMLAR-NUD Hynix 16GB x32bit 0001:K4EBE304EB-EGCF Samsung 16GB x32bit 0010:MT52L1G32D4PG-107 Micron 16GB x32bit 0011: MT52L512M32D2PF-107:B 8GB x32 bit 0100:H9CCNNNBJTMLAR-NUD 8GB x32 bit 0101:K4E6E304EB-EGCF 8GB x32 bit (B-Die)

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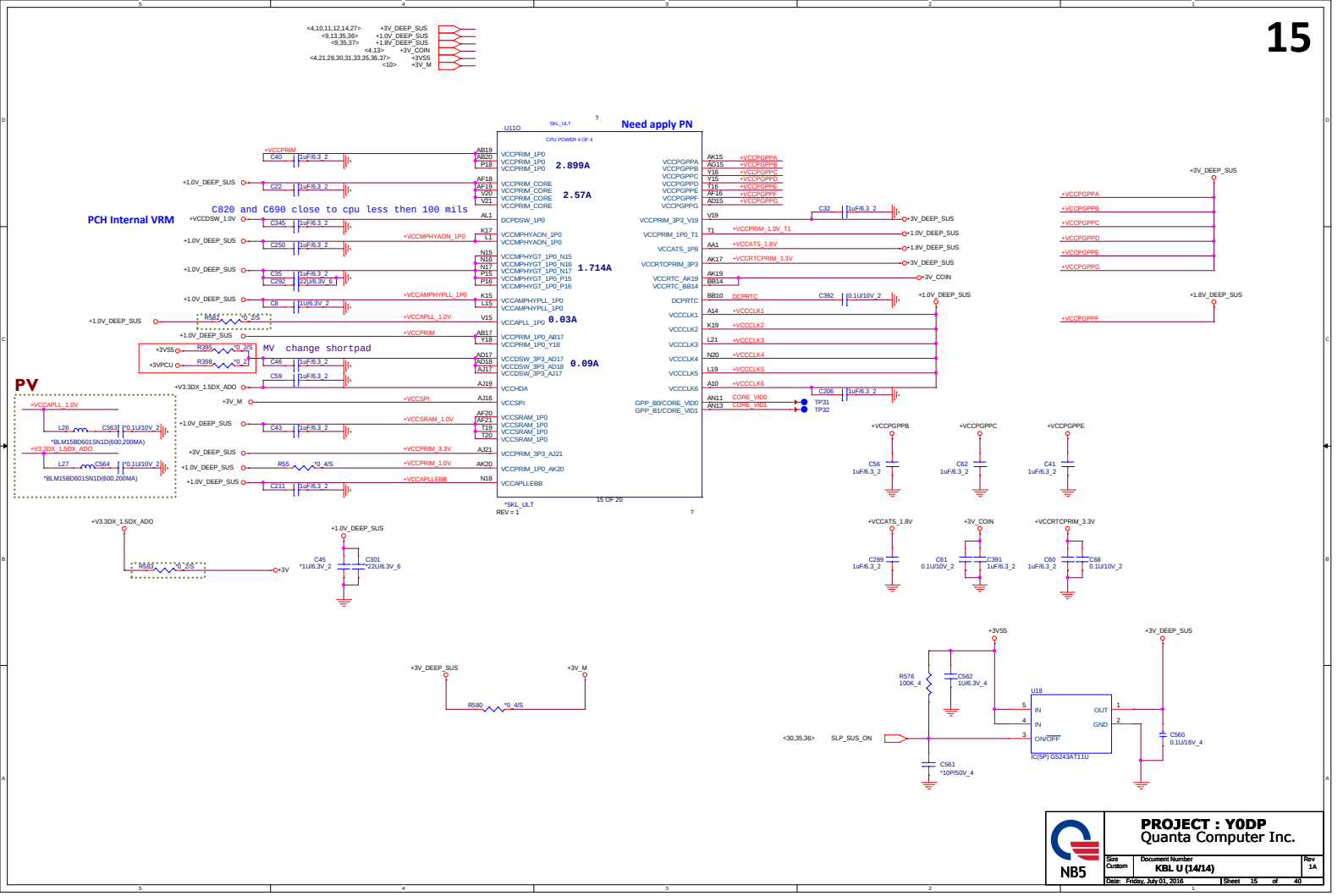

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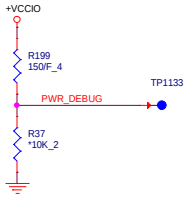

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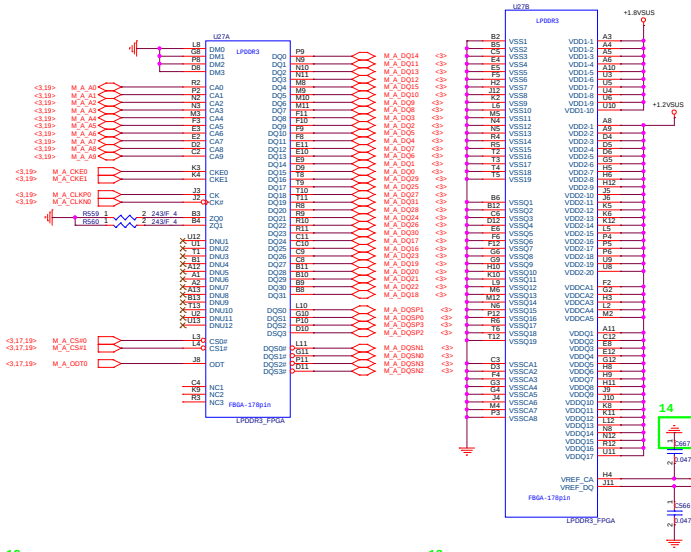
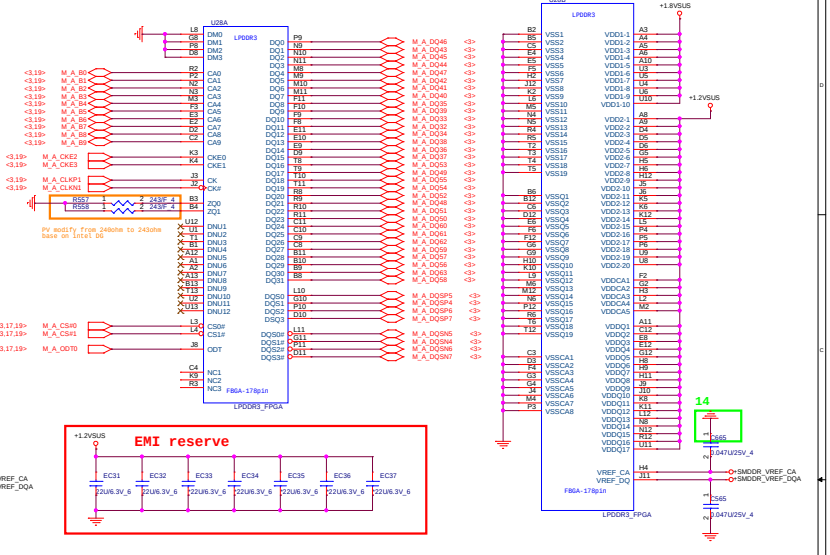
CHANNEL A:8Gb*2 LPDDR3

bit:0-31



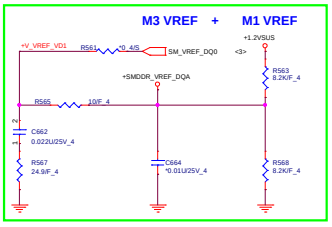
bit:32-63



EMI reserve

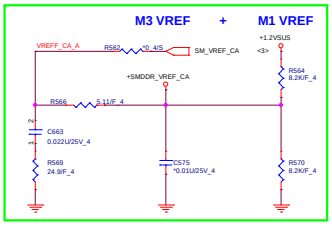
12

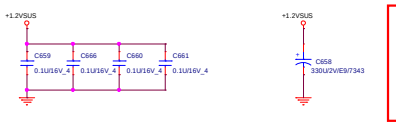
M3 VREF + M1 VREF

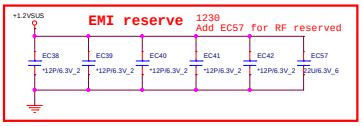


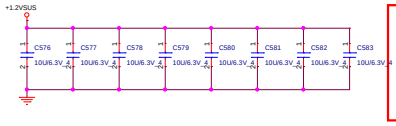
12

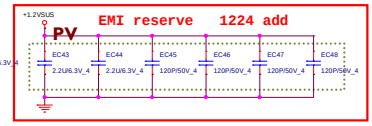
M3 VREF + M1 VREF

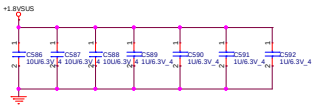


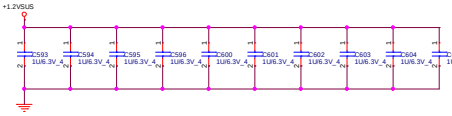


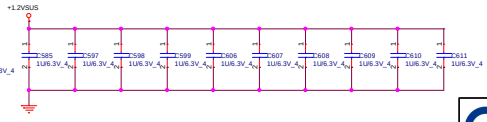












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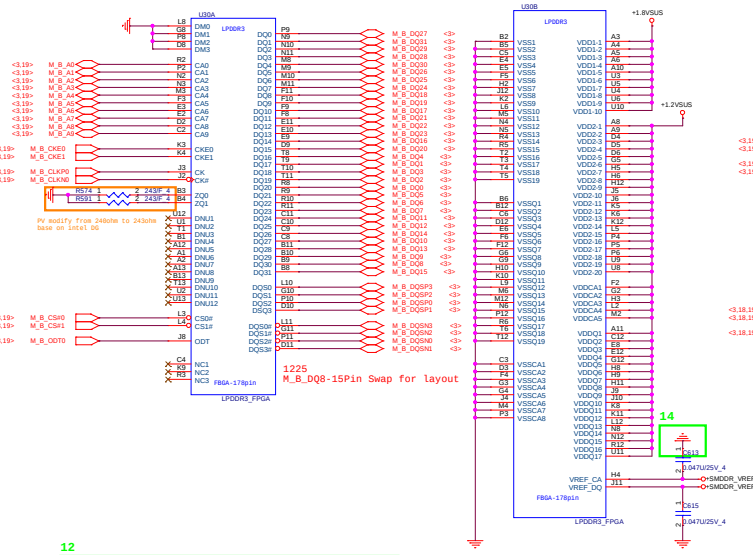
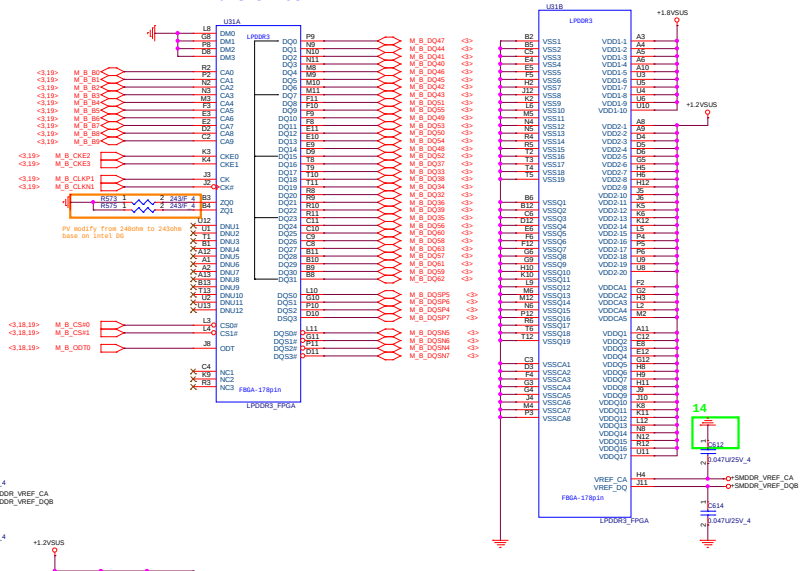
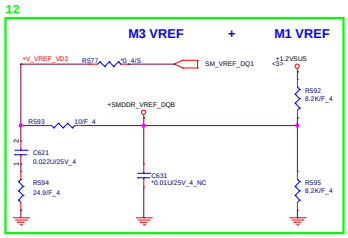
CHANNEL B:8Gb*2 LPDDR3

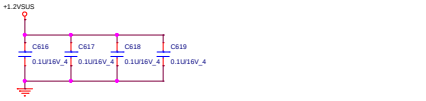
bit:0-31

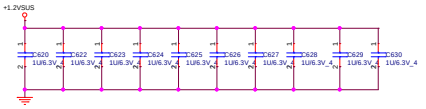


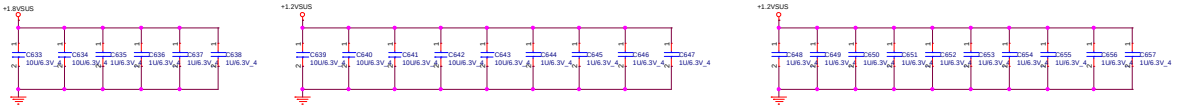
bit:32-63











PROJECT : Y0DP	
Quanta Computer Inc.	
NB5	Size: Document Number: LPDDR3 B; Rev: 1A
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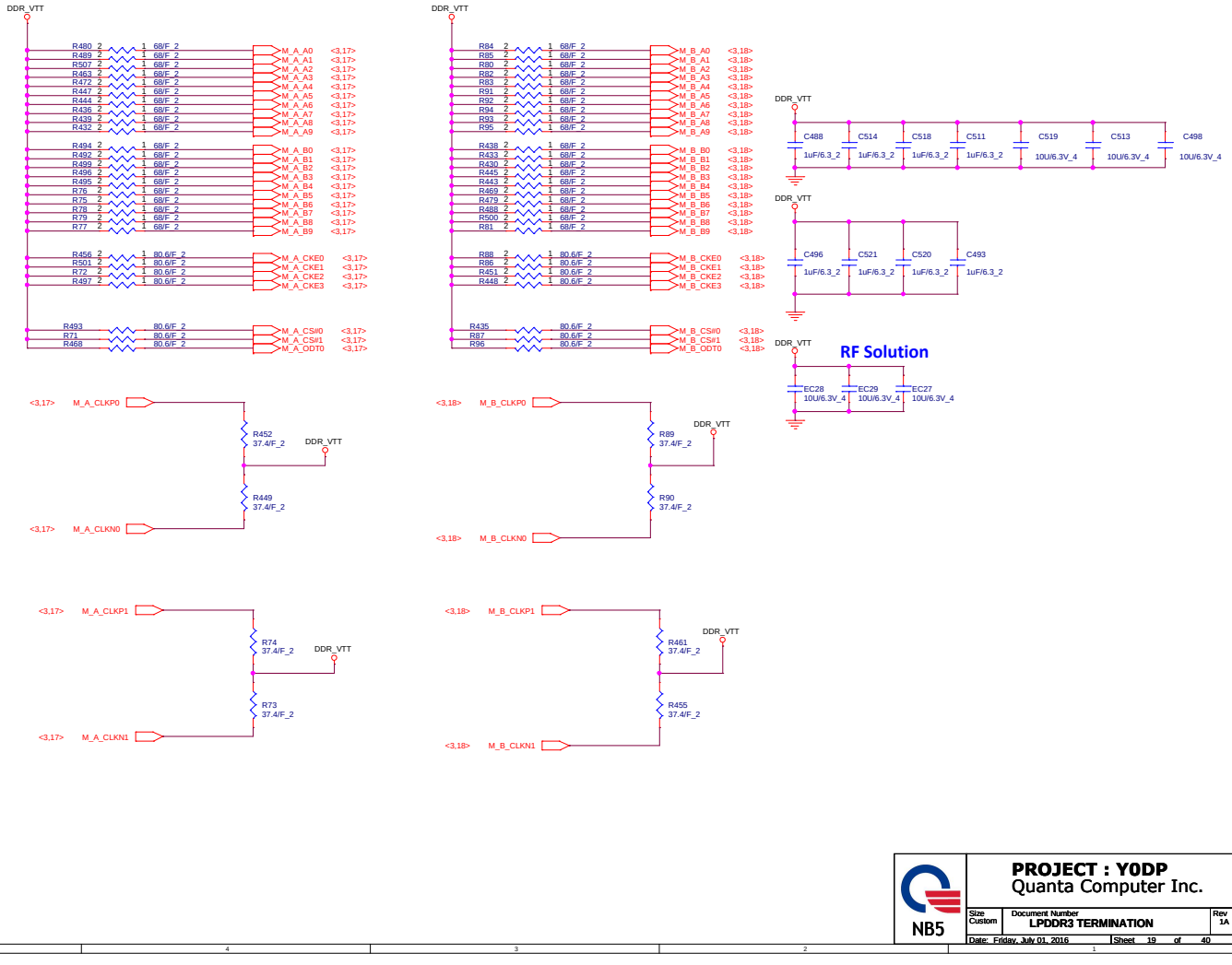

NB5	PROJECT : Y0DP Quanta Computer Inc.	
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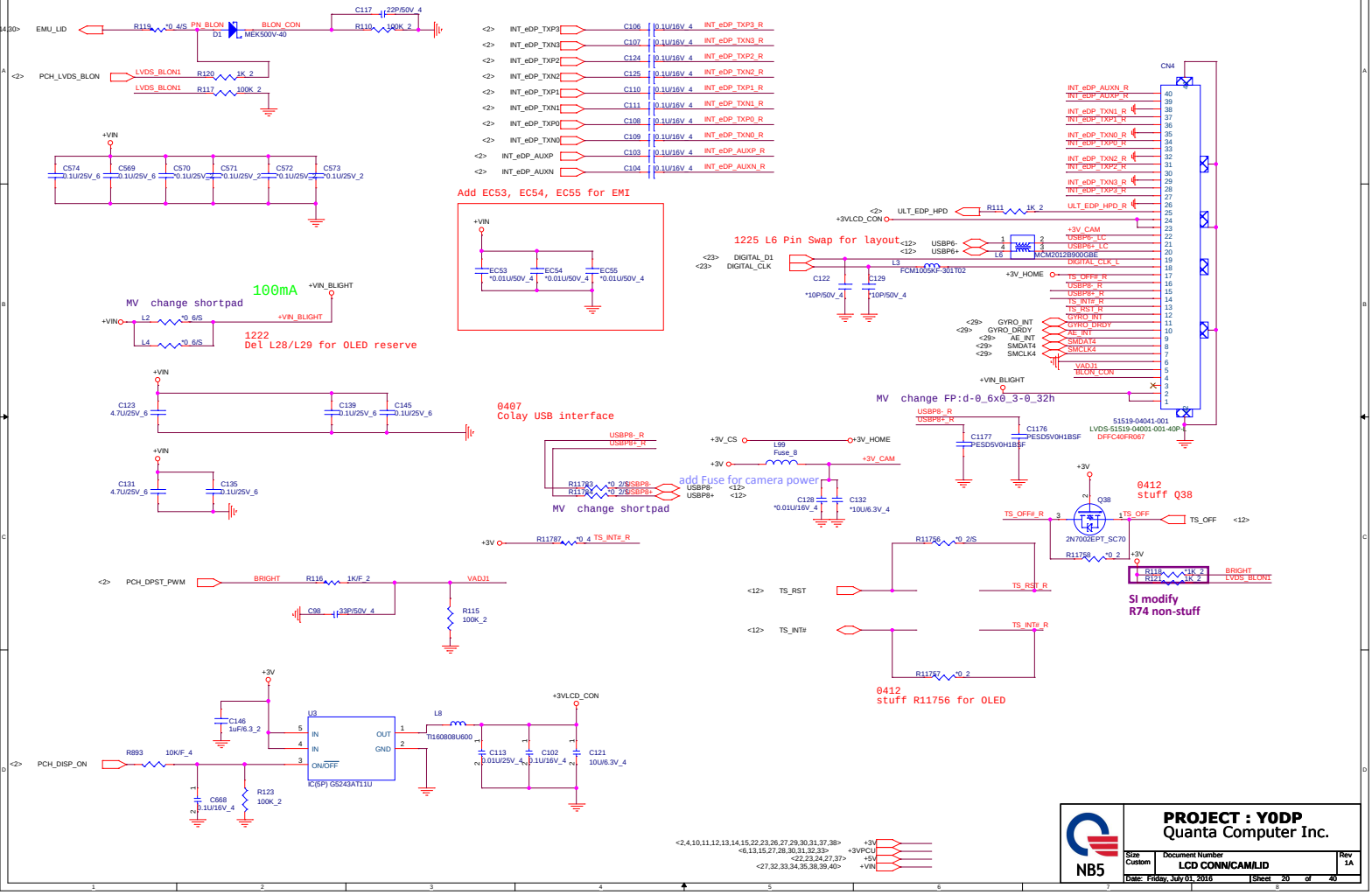
LID Switch

LVDS Conn.

20



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NB5	Size Custom	Document Number LCD CONN/CAM/LID	Rev 1A
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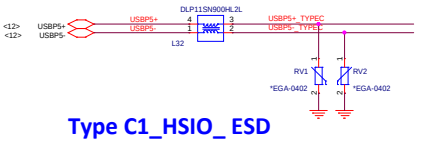
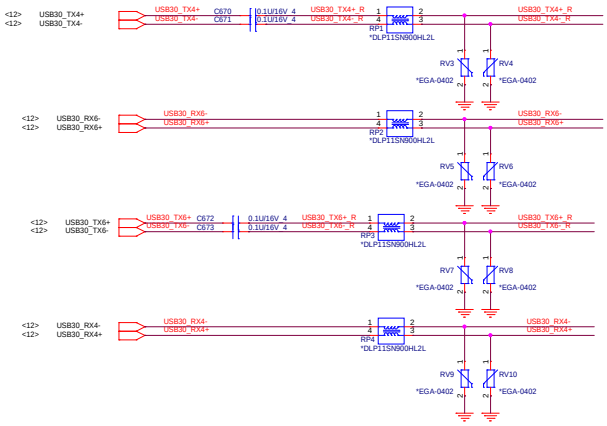
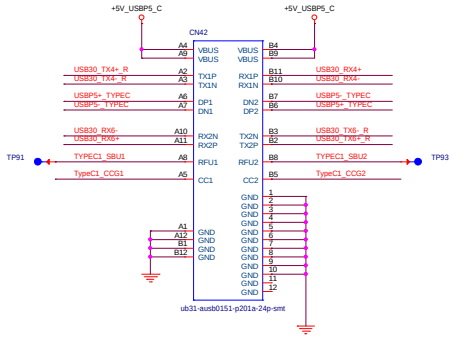
USB2.0 ESD



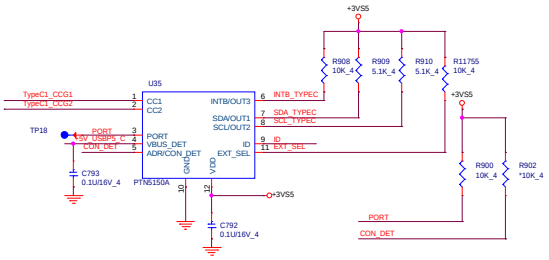
Type C1_HSIO_ ESD

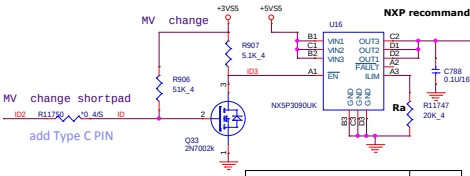




MV change FP:ub31-ausb0151-p201a-24p-smt

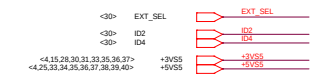
MV del





NXP recommand:MAX current:1.2A

ILIM to current limit values	Ra
1.0A/900mA	56K
1.65A	33K
2.5A	20K
3.5A	14K



NB5

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Quanta Computer Inc.

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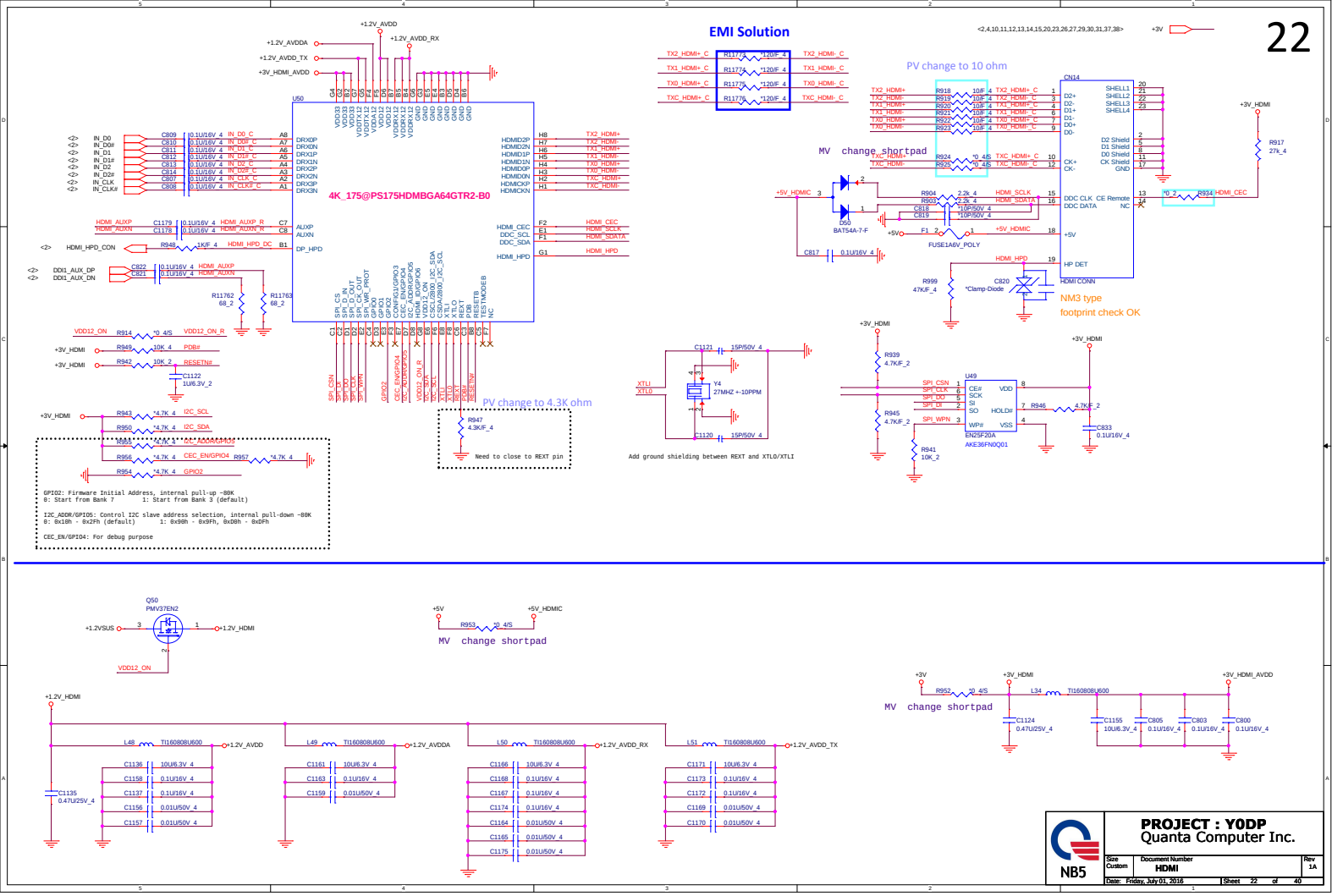

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Size: Custom	Document Number: HDMI
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NB5

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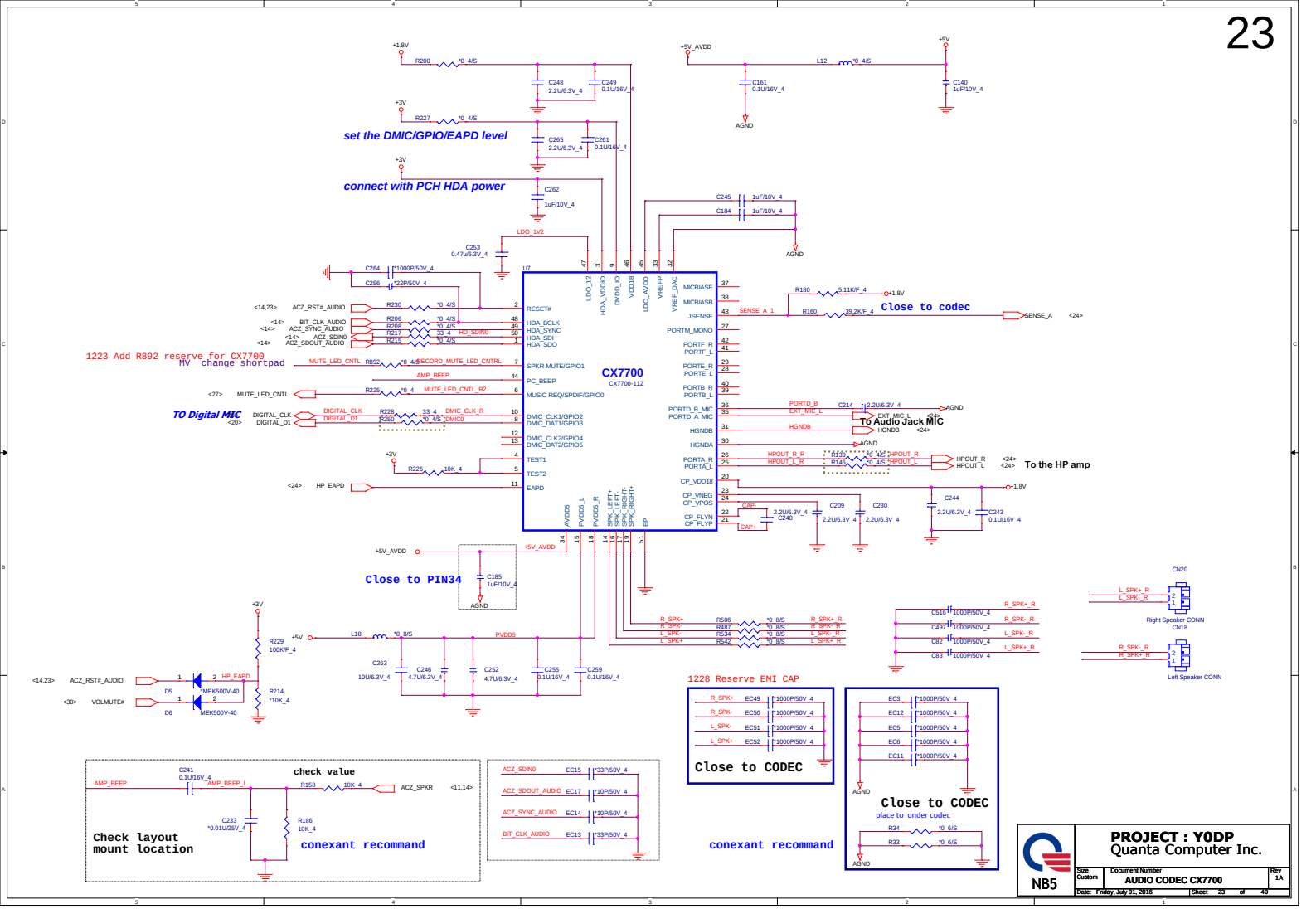

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	Quanta Computer Inc.
NB5	
Size: Custom	Document Number: AUDIO CODEC CX7700
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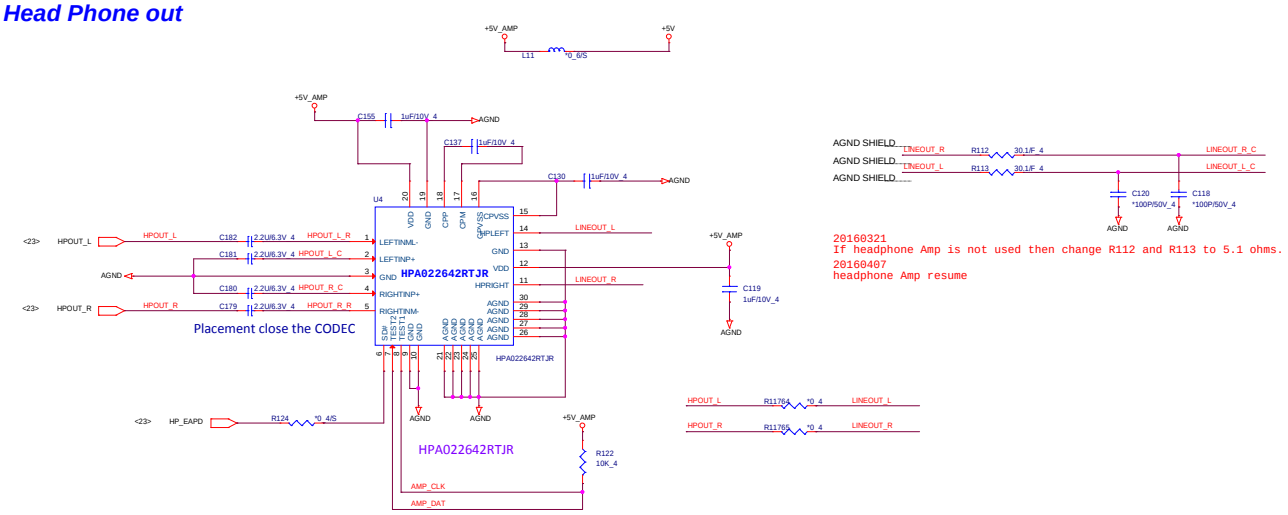
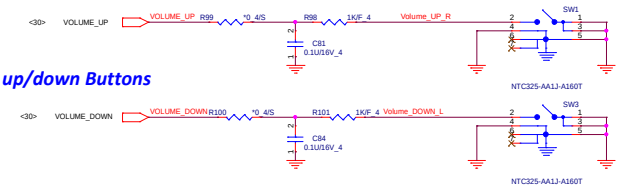
Head Phone out



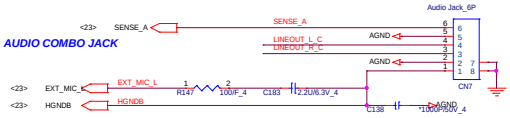
20160321
If headphone Amp is not used then change R112 and R113 to 5.1 ohms.
20160407
headphone Amp resume

Audio combo JACK & Volume up/down Button

Volume up/down Buttons

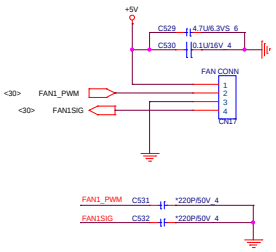


AUDIO COMBO JACK



FAN

1203
Update footprint from 88266-0400-4p-l to 88266-04xl-4p-l-smt



<2,4,10,11,12,13,14,15,20,22,23,26,27,29,30,31,37,38> +3V
<22,23,27,37> +5V
<4,21,25,33,34,35,36,37,38,39,40> +5VS

NB5

PROJECT : Y0DP
Quanta Computer Inc.

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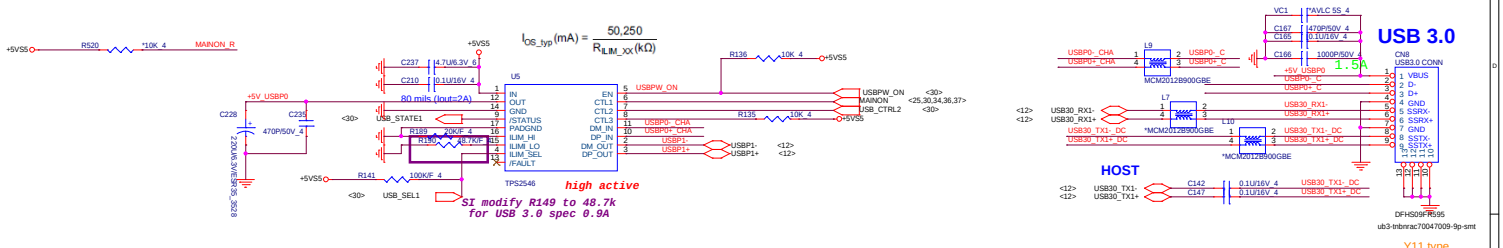
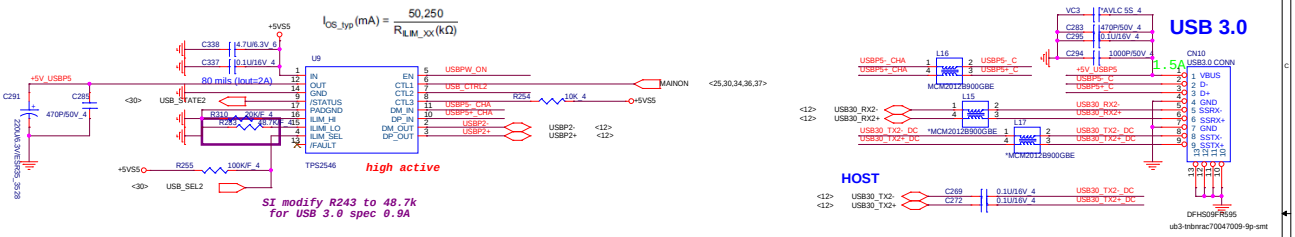
Right side USB 2.0/3.0 Combo

PV ADD R554/R555/R556 10k for USB 3.0 PU



1203
Update footprint from ub3-tnbnrac70047009-9p to ub3-tnbnrac70047009-9p-smt



Intel UART

Left side USB 2.0/3.0 Combo

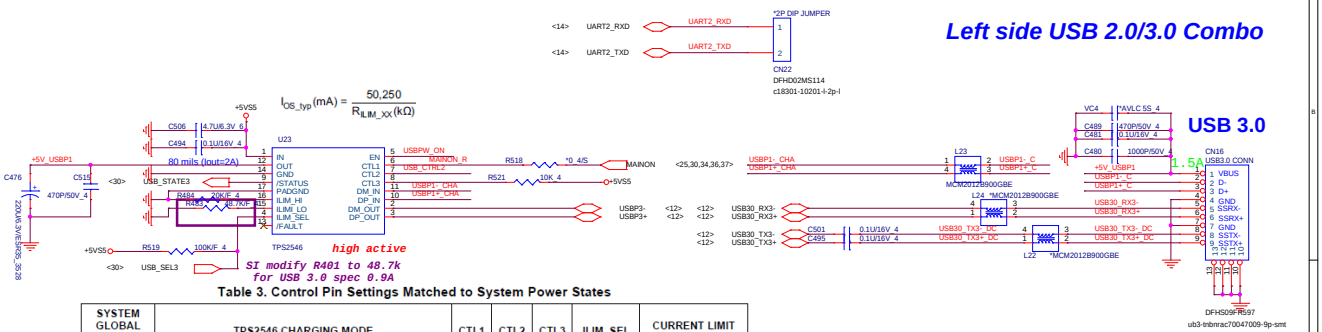


Table 3. Control Pin Settings Matched to System Power States

SYSTEM GLOBAL POWER STATE	TPS2546 CHARGING MODE	CTL1	CTL2	CTL3	ILIM_SEL	CURRENT LIMIT SETTING
S0	SDP1	1	1	0	1 or 0	ILIM_HI / ILIM_LO
S0	SDP2, no discharge to / from CDP	1	1	1	0	ILIM_LO
S0	CDP, load detection with ILIM_LO + 60mA thresholds or if a BC1.2 primary detection occurs	1	1	1	1	ILIM_HI
S4/S5	Auto mode, load detection with power wake thresholds	0	0	1	1	ILIM_HI
S3/S4/S5	Auto mode, no load detection	0	0	1	0	ILIM_HI
S3	Auto mode, keyboard/mouse wake up, load detection with ILIM_LO + 60 mA thresholds	0	1	1	1	ILIM_HI
S3	Auto mode, keyboard/mouse wake-up, no load detection	0	1	1	0	ILIM_HI
S3	SDP1, keyboard/mouse wake-up	0	1	0	1 or 0	ILIM_HI / ILIM_LO

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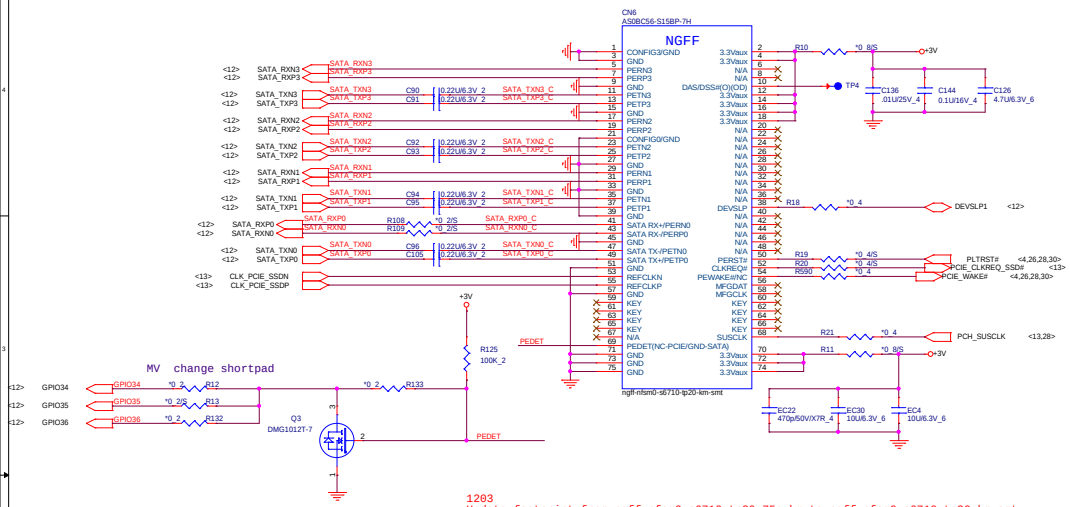
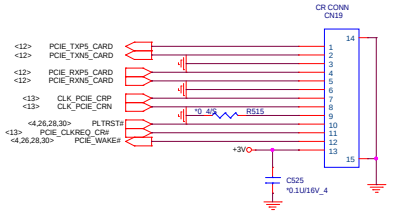


1203
Update footprint from ngff-nfsm0-s6710-tp20-75p-km to ngff-nfsm0-s6710-tp20-km-smt

TPM (2.0)

Card Reader CON



<2,4,10,11,12,13,14,15,20,22,23,27,29,30,31,37,38> +3V
<22,23,24,27,37> +5V
<6,13,15,27,28,30,31,32,33> +3VPCU

NB5

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Power Botton

PWR LED

1203
Update footprint from ledl-s110kgct-3p-smt toledltw-110uc5-3p

1230
Change net name from SMB_RUN_CLK to SMB_PCH_CLK
Change net name from SMB_RUN_DAT to SMB_PCH_DAT

SI Add for solve leakage

PV modify

KEYBOARD Con.

KEYBOARD PULL-UP

SI

1230
Add EC56 for EMI reserved

1203
Update footprint from 51586-03241-001-32p-l to 51586-03201-001-32p-l

KB backlight

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Quanta Computer Inc.
NB5
Size: Custom
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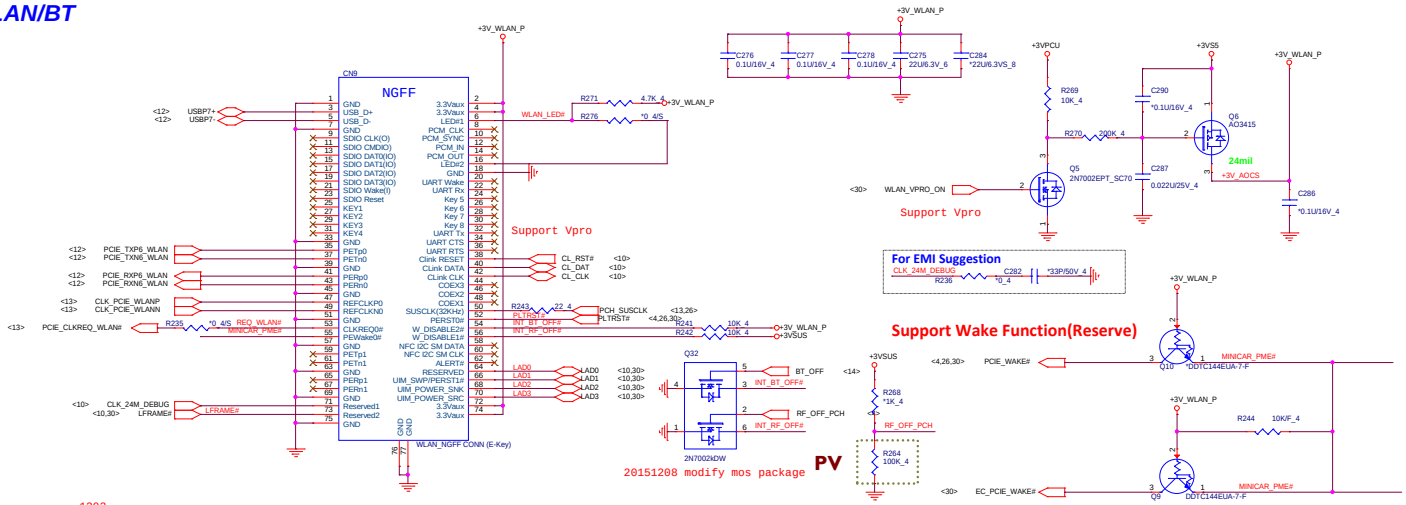
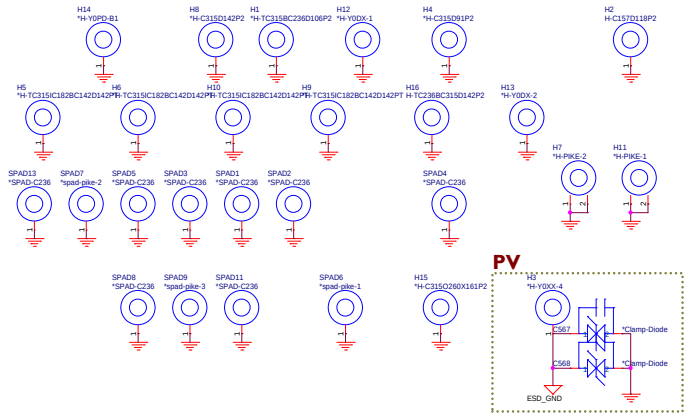
WLAN/BT



1203
Update footprint from ngff-nfse0-s6710-tp20-75p-ke to ngff-nfse0-s6710-tp20-ke-smt

Hole

1229
Update H8 footprint from H-C315I142D142P2

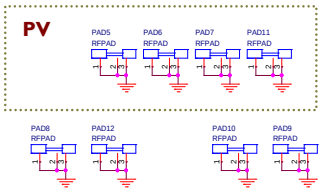


GND GUARD

1229
Add PAD13 for EMI

1230
Add PAD14 for EMI

1231
Shielding for Y0XX



0106
stuff Pad6, unstuff Pad5

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Quanta Computer Inc.
NB5
WLAN/HOLE
Rev 1A
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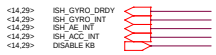

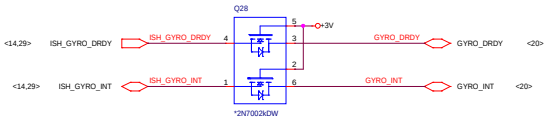

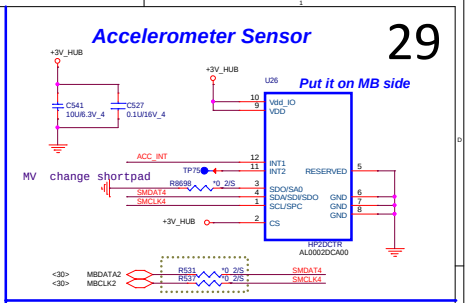

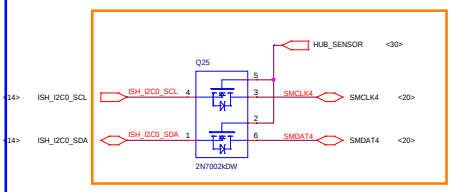

1222
Del Q26/ R587/ R588 for OLED reserve

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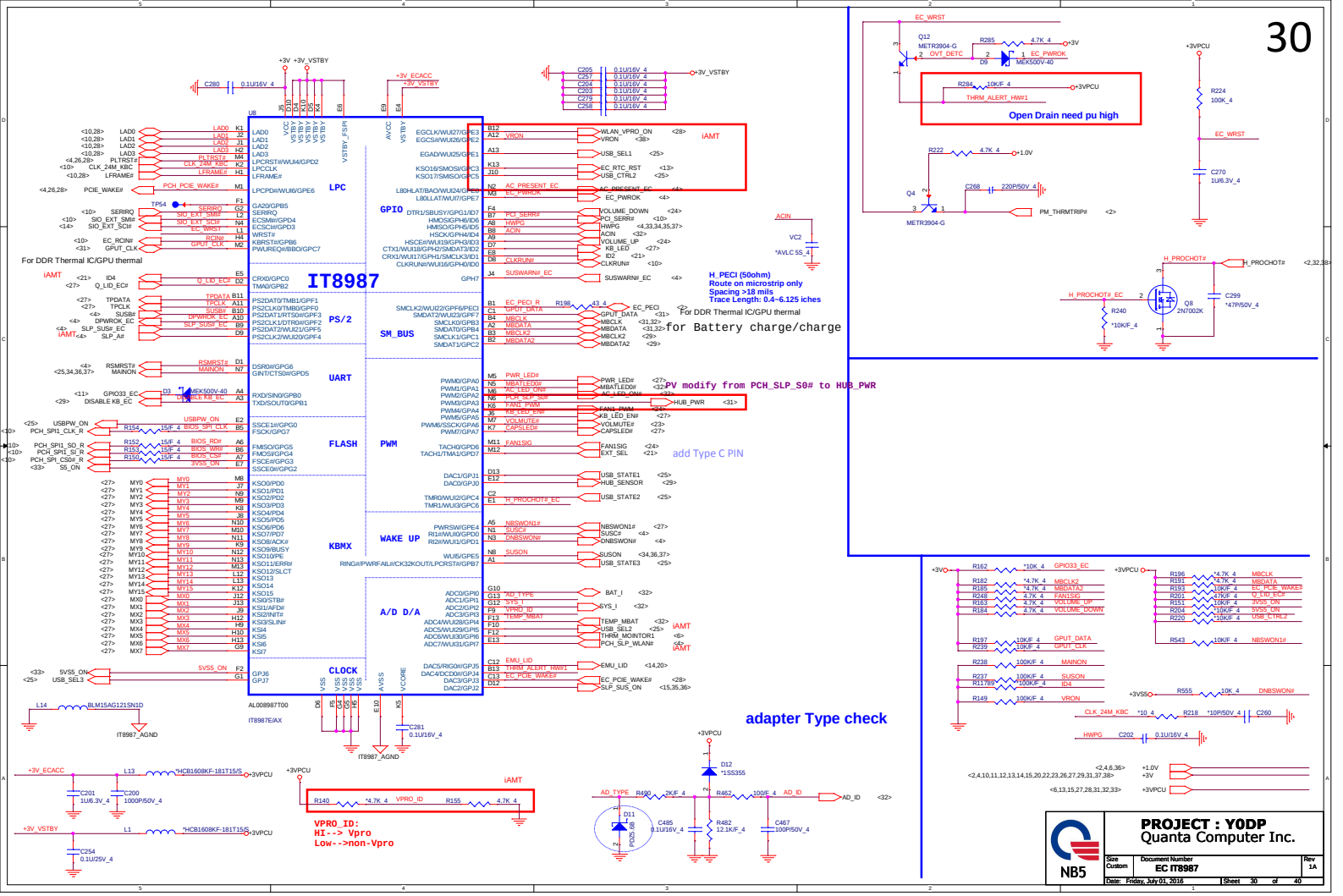

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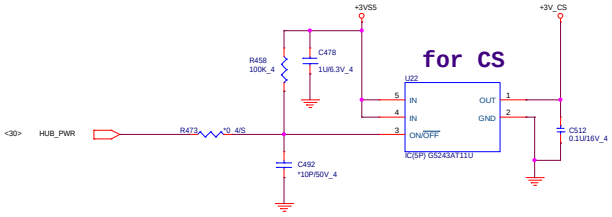

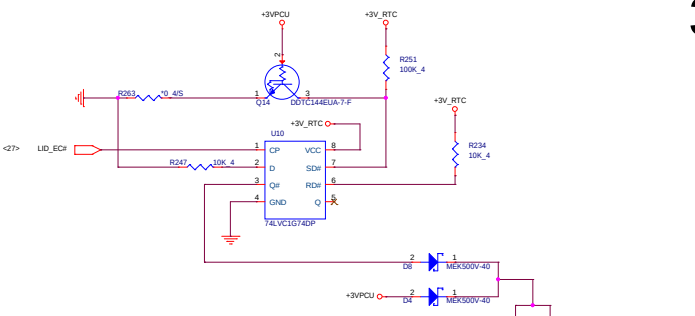

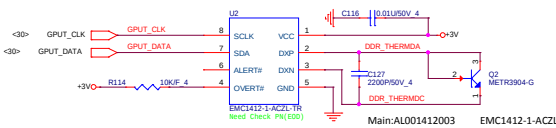

Main:AL001412003 EMC1412-1-ACZL-TR(98h)
2nd:AL000431014 TMP431ADGKR(98h)
2nd:AL000781039

Input				Output	
$\overline{SD}$	$\overline{RD}$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care.

Input				Output	
$\overline{SD}$	$\overline{RD}$	CP	D	Q_{n+1}	$\overline{Q}_{n+1}$
H	H	↑	L	L	H
H	H	↑	H	H	L

[1] H = HIGH voltage level;
L = LOW voltage level;
↑ = LOW-to-HIGH CP transition;
Q_{n+1} = state after the next LOW-to-HIGH CP transition.

NB5

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Custom	CS	1A
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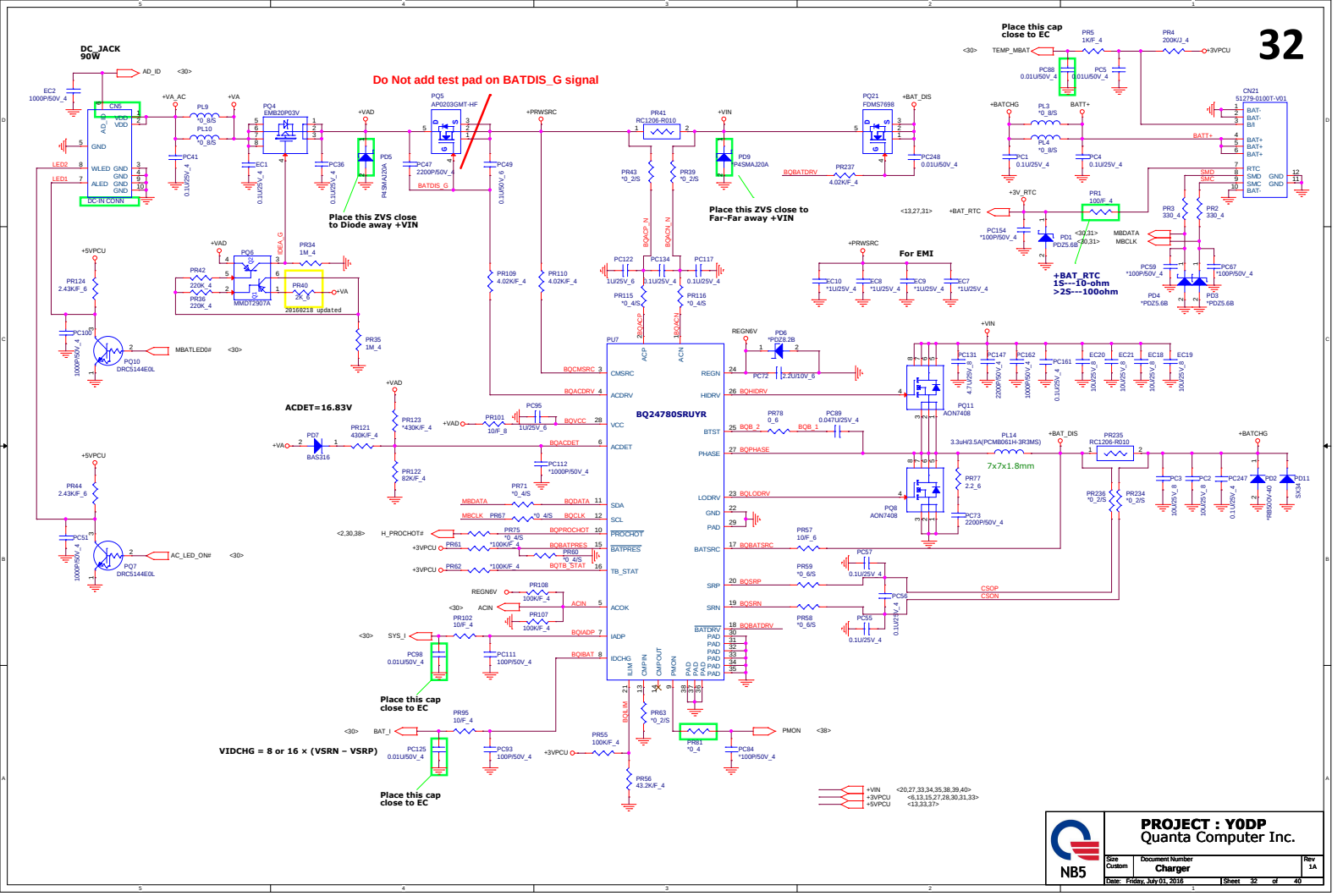

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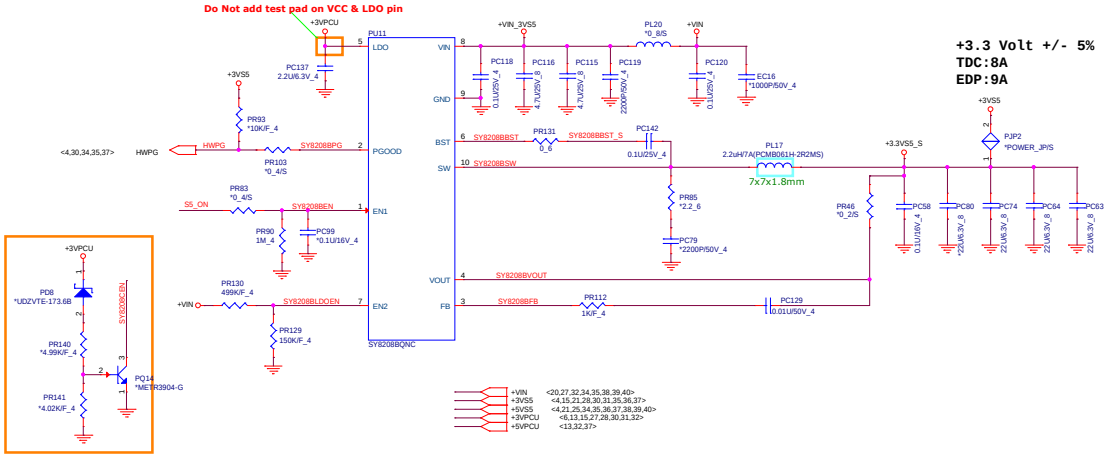

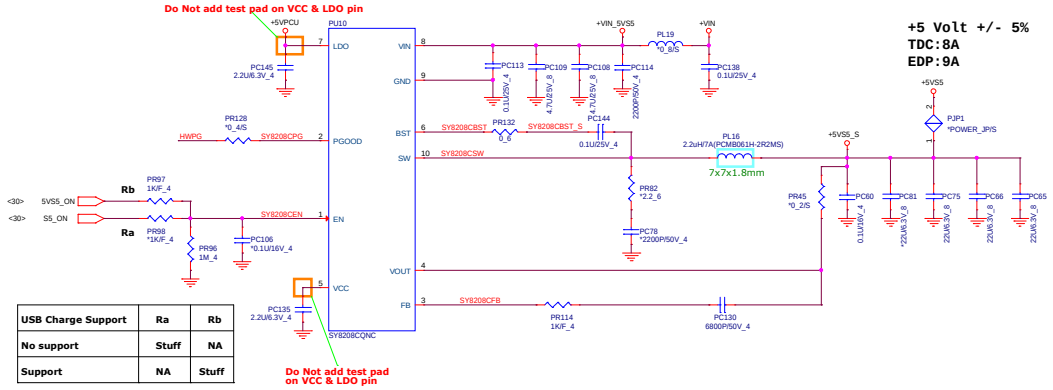

USB Charge Support	Ra	Rb
No support	Stuff	NA
Support	NA	Stuff

Do Not add test pad on VCC & LDO pin

NB5

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Size	Document Number	Rev
Custom	3/5S5	1A

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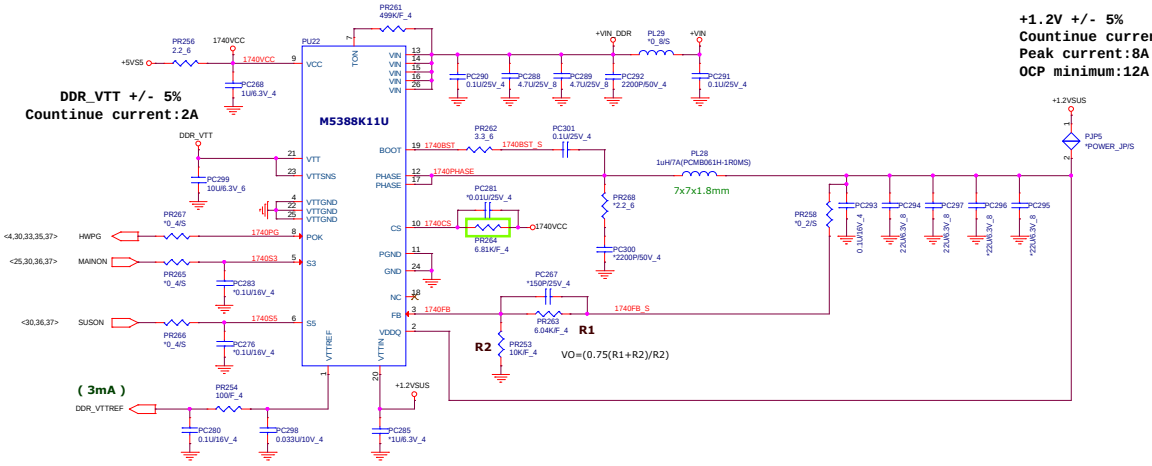

	S3	S5	+1.2VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

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NB5

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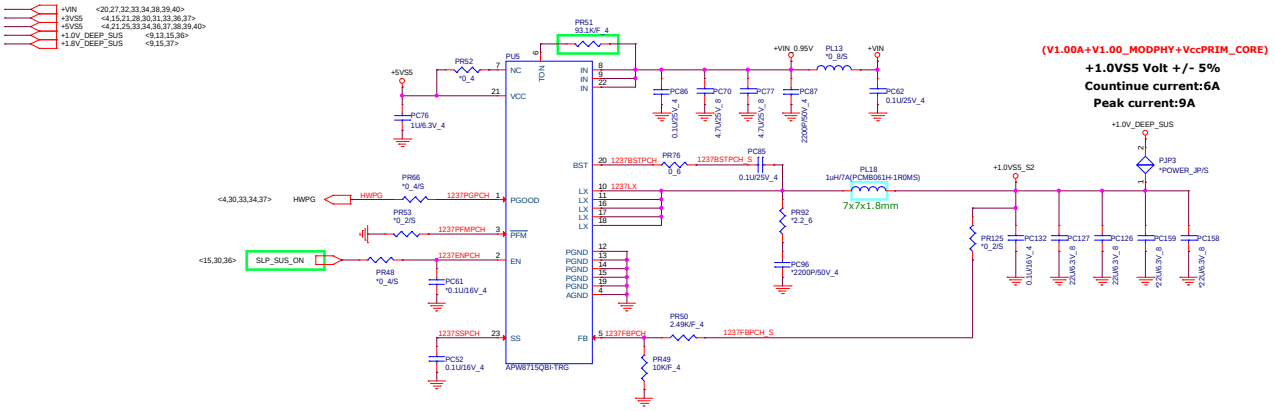

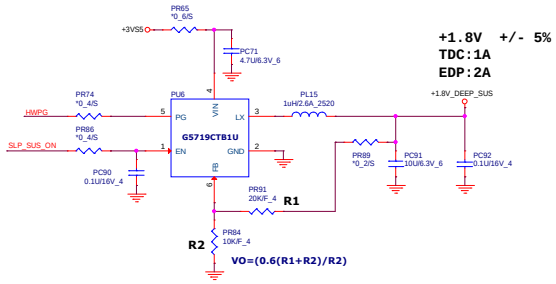

NB5	PROJECT : Y0DP Quanta Computer Inc.	
Size: Custom	Document Number: +1.0/+1.5V/+1.8V_DEEP_SUS	Rev: 1A
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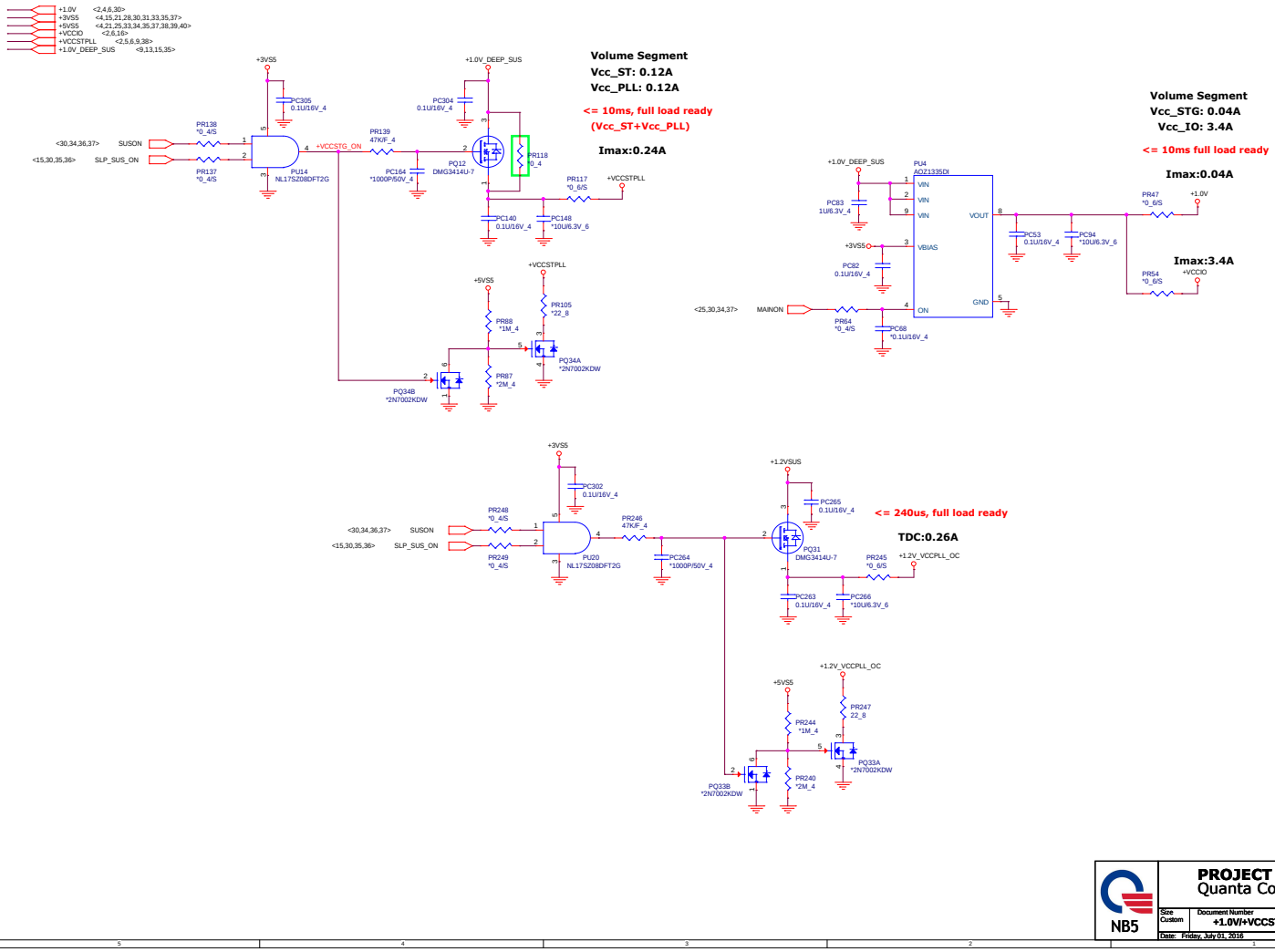

NB5	**PROJECT : Y0DP** Quanta Computer Inc.
Size: Custom	Document Number: +1.0V/+VCCSTPLL — Rev: 1A
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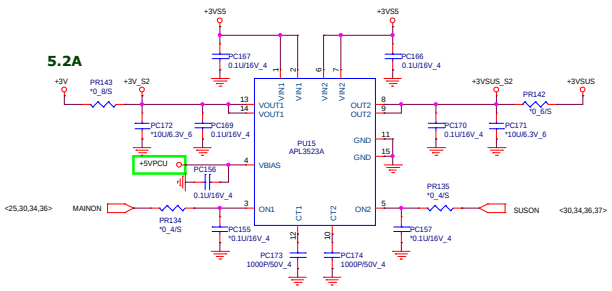
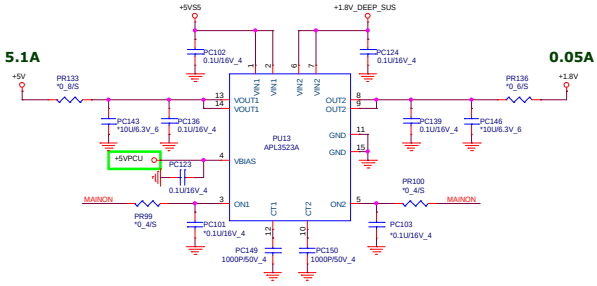
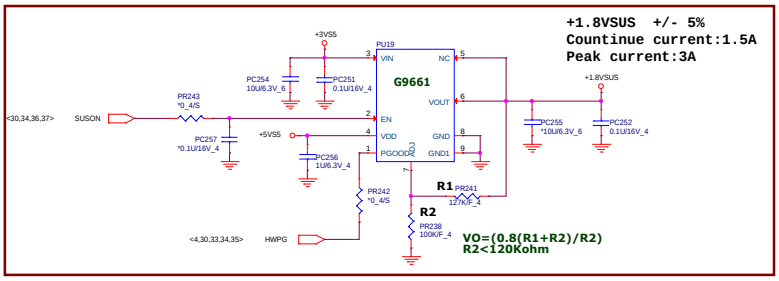
+3V <2,4,10,11,12,13,14,15,20,22,23,26,27,29,30,31,38>
+5V <22,23,24,27,37>
+3VS5 <4,15,21,28,30,31,33,35,36>
+5VS5 <4,21,25,33,34,35,36,38,39,40>
+3VSUS <27,28>
+1.8V_DEEP_SUS <9,15,35>
+1.8V <23>
+5V <22,23,24,27,37>
+VIN <20,27,32,33,34,35,38,39,40>
+1.8VSUS <17,18>







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Quanta Computer Inc.
NB5
Size: Custom
Document Number: Load switch IC
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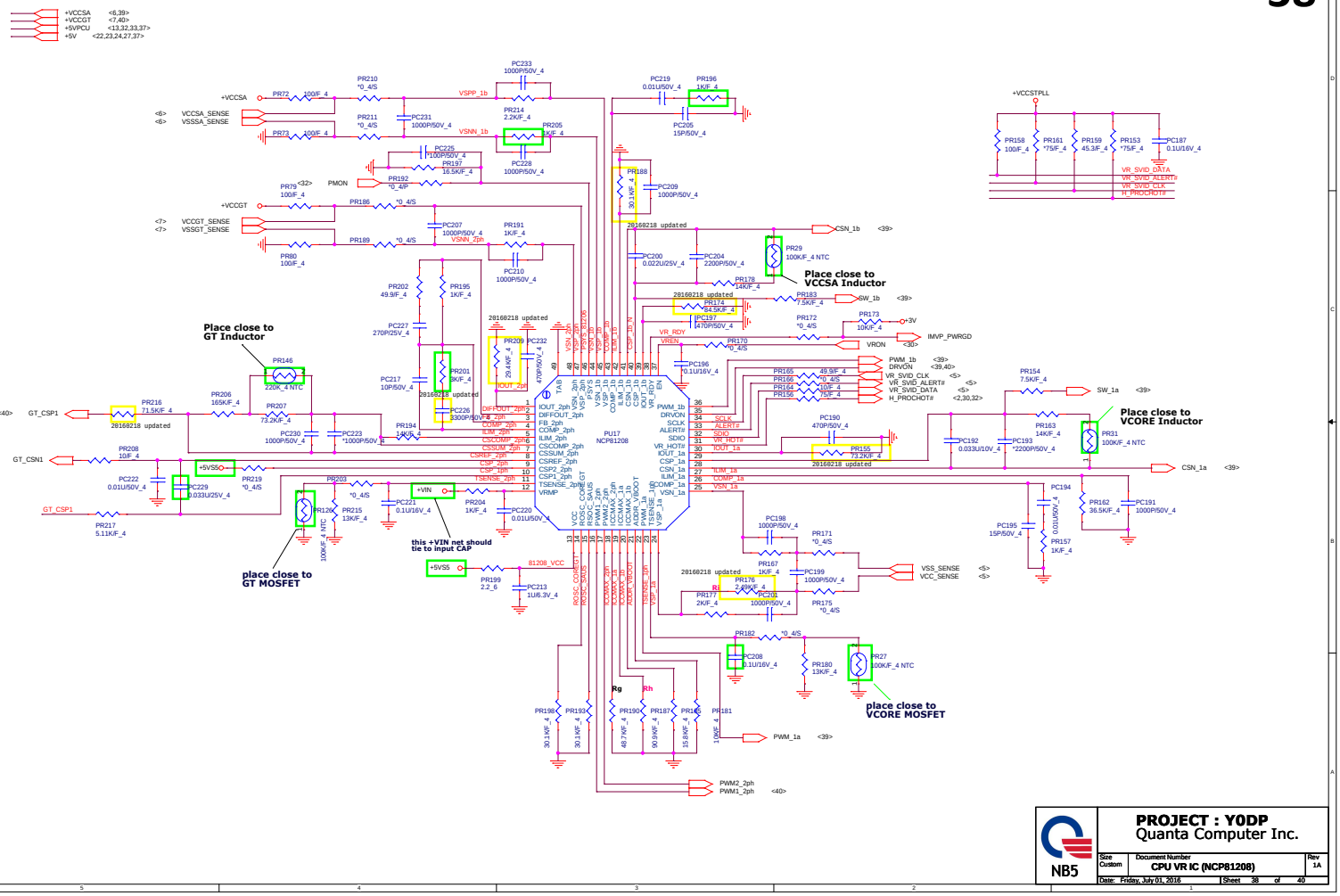

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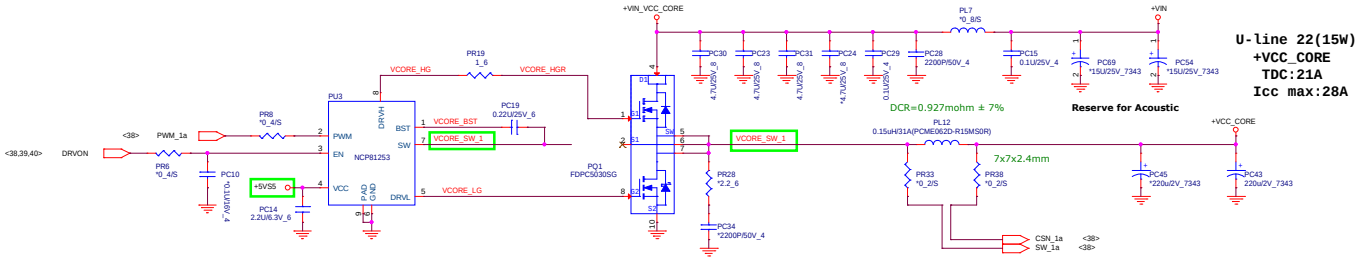
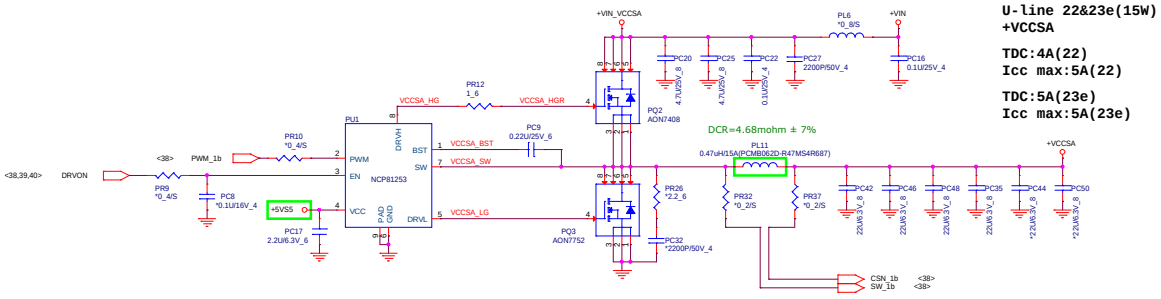
CPU CORE



VCCSA



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Size	Document Number	Rev
Custom	+VCORE/VCCSA (NCP81253)	1A

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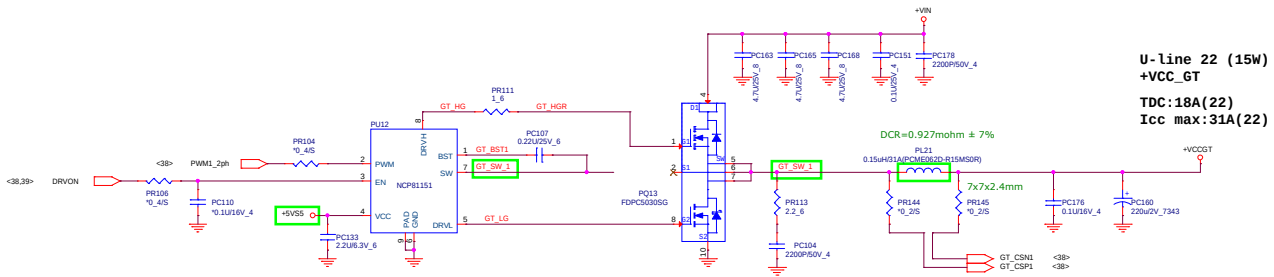
+VIN <20,27,32,33,34,35,38,39>
+VCCGT <7,38>
+VIN_VCC_CORE
+5VPCU <13,32,33,37>
+5V <22,23,24,27,37>



U-line 22 (15W)
+VCC_GT

TDC:18A(22)
Icc max:31A(22)

NB5

PROJECT : Y0DP
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VCCGT (NCP81151)	1A

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