

Compal Confidential

Schematics Document

AUBURNDALE/CLARKSFIELD with
Intel IBEX PEAK-M core logic

Versace

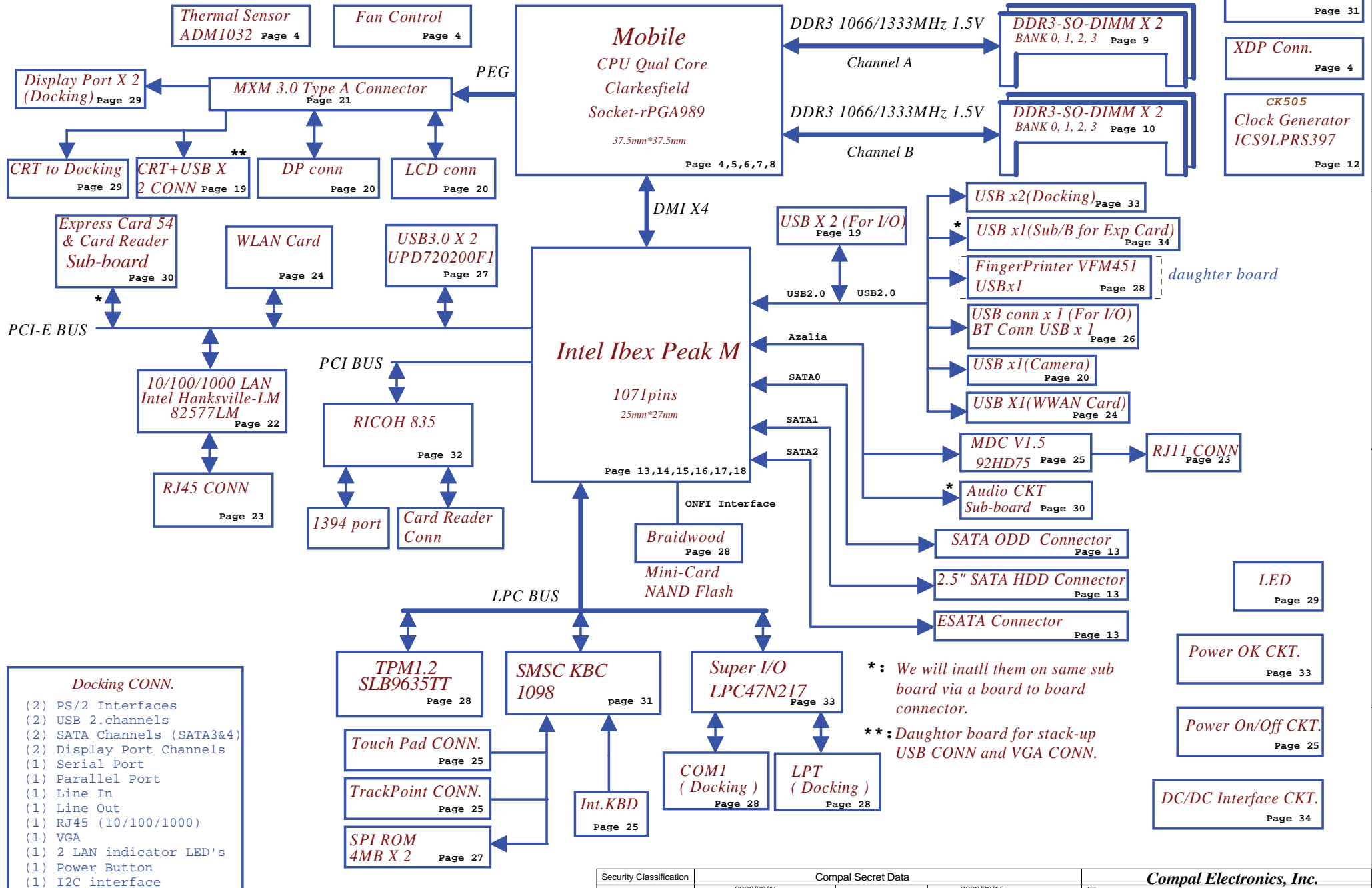
2009-07-24

REV:0.4



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Versace



- Docking CONN.**
- (2) PS/2 Interfaces
 - (2) USB 2.channels
 - (2) SATA Channels (SATA3&4)
 - (2) Display Port Channels
 - (1) Serial Port
 - (1) Parallel Port
 - (1) Line In
 - (1) Line Out
 - (1) RJ45 (10/100/1000)
 - (1) VGA
 - (1) 2 LAN indicator LED's
 - (1) Power Button
 - (1) I2C interface

* : We will inatll them on same sub board via a board to board connector.

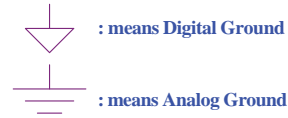
** : Daughter board for stack-up USB CONN and VGA CONN.

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Voltage Rails (O MEANS ON X MEANS OFF)

power plane State	+RTCVCC	+B +3VL	+5VALW +3VALW	+1.5V +0.75V	+5VS +3VS +1.5VS +NVVDD +VCCP +CPU_CORE +1.05VS +1.8VS
S0	O	O	O	O	O
S1	O	O	O	O	O
S3	O	O	O	O	X
S5 S4/AC	O	O	O	X	X
S5 S4/ Battery only	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X

Symbol Note :



Install below 43 level BOM structure for ver. 0.1

DEBUG@ : means just build when PCIE port 80 CARD function enable. *Remove before MP*

M92@ : Install for M92 Graphic controller

8072@ : Install for 8072 NIC controller

1098@ : Install for 1098 KBC controller

CK32@ : Install for 32 pin CLOCK GEN

Install below 45 level BOM structure for ver. 0.1

45@ : means just put it in the BOM of 45 level.

Reserve below BOM structure for ver. 0.1

@ : means just reserve , no build

CONN@ : means ME part.

M93@ : Install for M93 Graphic controller

8075@ : Install for 8075 NIC controller

1091@ : Install for 1091 KBC controller

CK72@ : Install for 72 pin CLOCK GEN

SMBUS Control Table

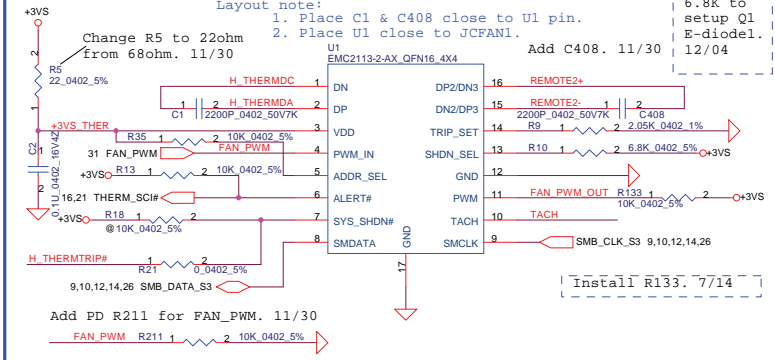
	SOURCE	BATT	XDP	SODIMM	CLK CHIP	MINI CARD	DOCK	NIC	THERMAL SENSOR	G-SENSOR
SMB_EC_CK1 SMB_EC_DA1	SMSC1098	V	X	X	X	X	X	X	X	X
SMBCLK SMBDATA	Calpella	X	V	V	V	V	V	X	X	X
SML0CLK SML0DATA	Calpella	X	X	X	X	X	X	V	X	X
SML1CLK SML1DATA	Calpella	X	X	X	X	X	X	X	V	V

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Thermal Sensor EMC2113 with CPU PWM FAN

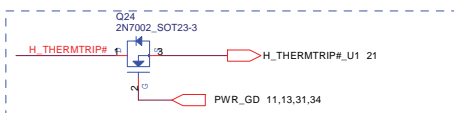
Layout note:

- Place C1 & C408 close to U1 pin.
- Place U1 close to JCFAN1.



Change R10 to 6.8K to setup Q1 E-diode. 12/04

Install R133. 7/14



Change Q24.2 connect from +3VS to PWR_GD. 12/11

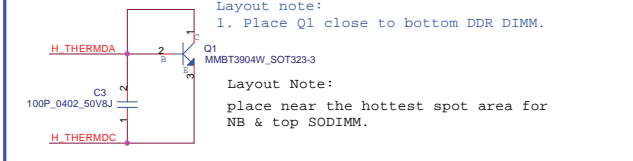
REMOTE thermal sensor

Layout note:

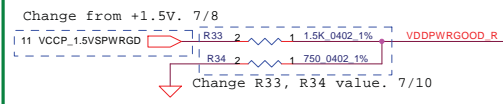
- Place Q1 close to bottom DDR DIMM.

Layout Note:

place near the hottest spot area for NB & top SODIMM.

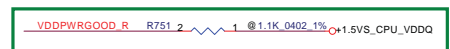


Intel S3



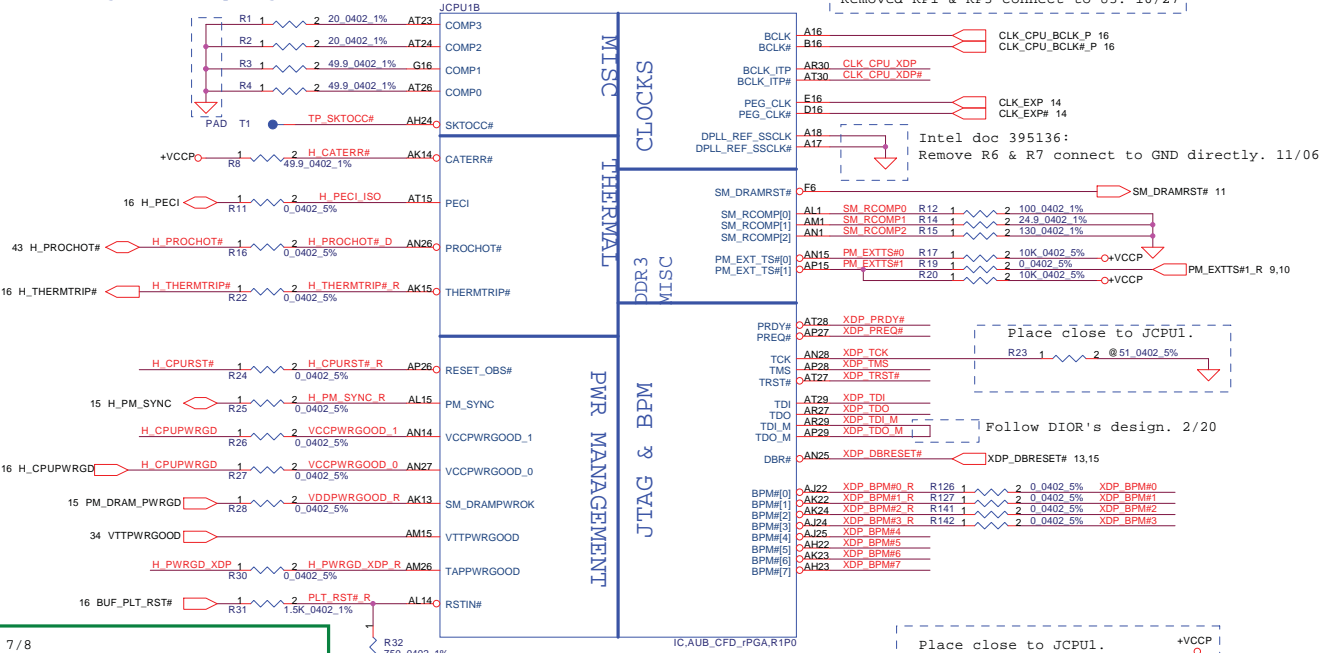
Change R33, R34 value. 7/10

Intel S3



Place close to JCPU1.

Layout rule: 10mil width trace length < 0.5", spacing 20mil



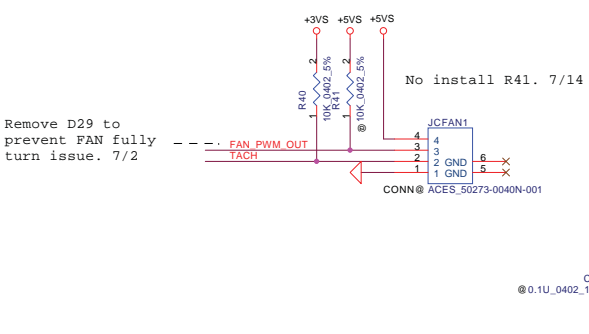
Removed RP1 & RP3 connect to U3. 10/27

Intel doc 395136: Remove R6 & R7 connect to GND directly. 11/06

Place close to JCPU1.

Follow DIOR's design. 2/20

FAN Connector

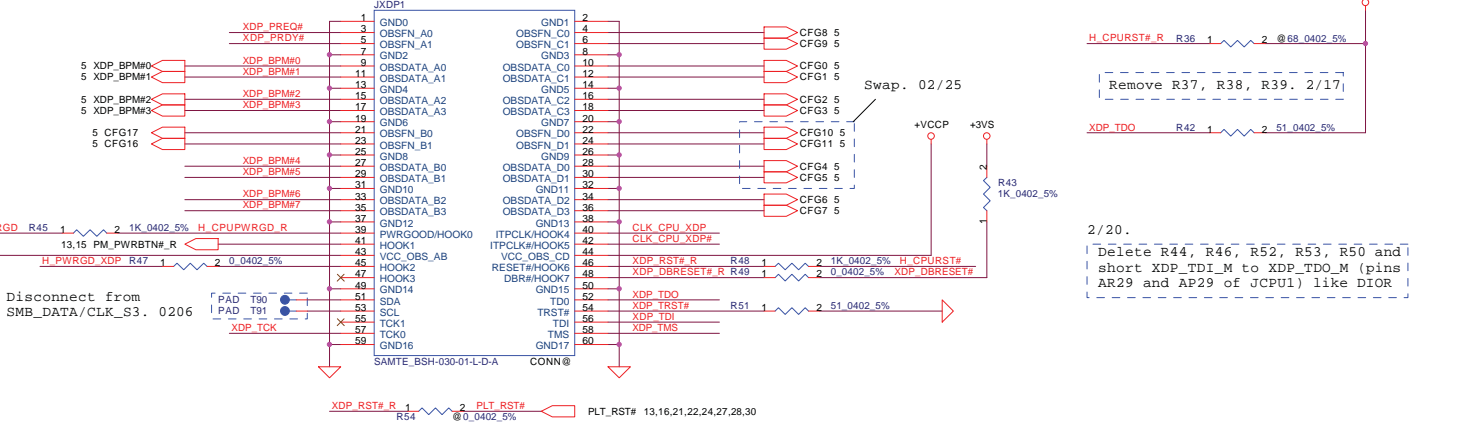


Remove D29 to prevent FAN fully turn issue. 7/2

No install R41. 7/14

Disconnect from SMB_DATA/CLK_S3. 0206

XDP Connector

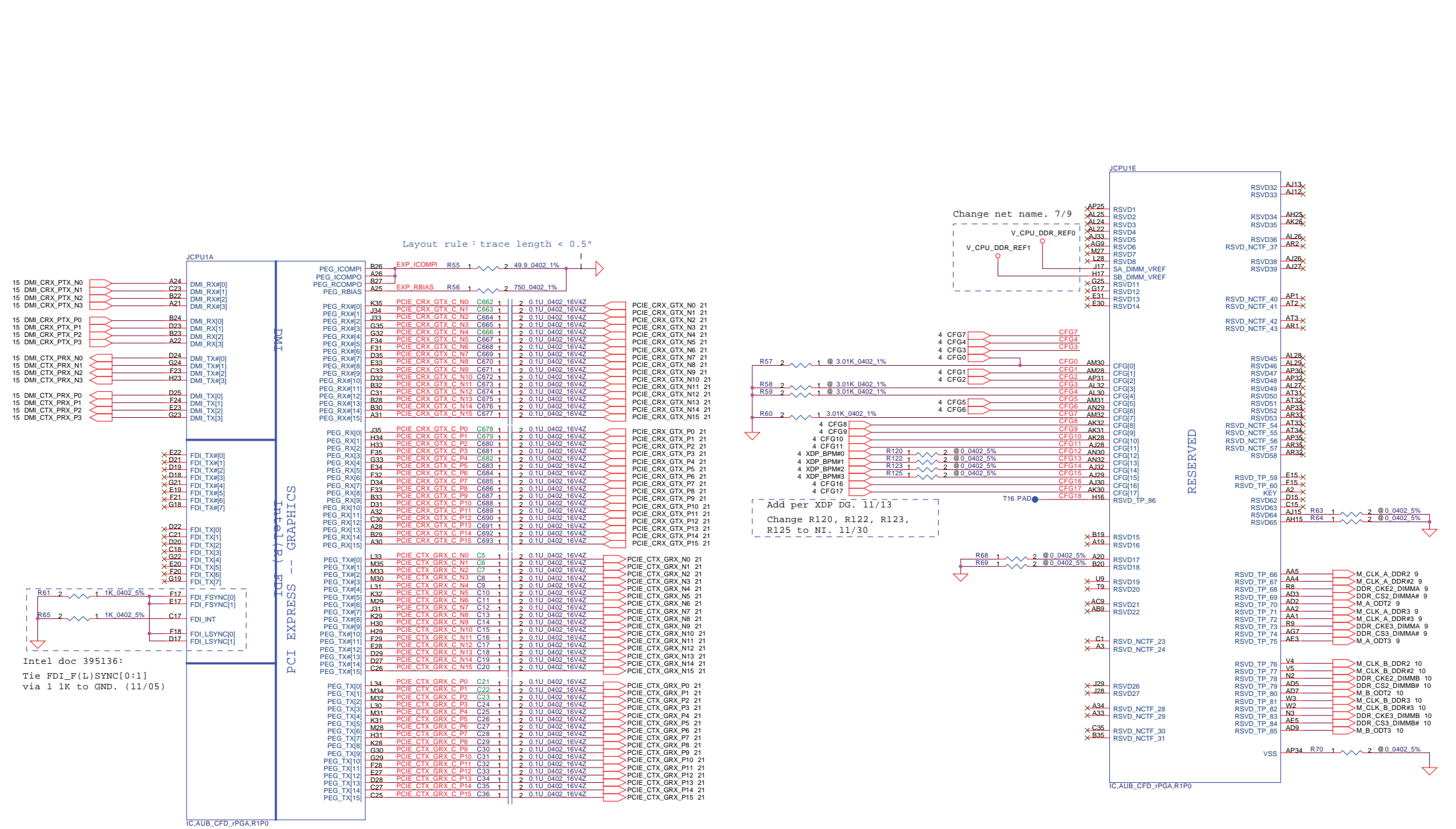


Swap. 02/25

Remove R37, R38, R39. 2/17

Delete R44, R46, R52, R53, R50 and short XDP_TDI_M to XDP_TDO_M (pins AR29 and AP29 of JCPU1) like DIOR

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9 DDR_A_D[0..63] \leftrightarrow DDR_A_D[0..63]

10 DDR_B_D[0..63] \leftrightarrow DDR_B_D[0..63]

JCPU1C

JCPU1D

- DDR A D0 A10 SA_DQ[0]
- DDR A D1 C10 SA_DQ[1]
- DDR A D2 C7 SA_DQ[2]
- DDR A D3 A7 SA_DQ[3]
- DDR A D4 B10 SA_DQ[4]
- DDR A D5 D10 SA_DQ[5]
- DDR A D6 E10 SA_DQ[6]
- DDR A D7 D8 SA_DQ[7]
- DDR A D8 A8 SA_DQ[8]
- DDR A D9 F10 SA_DQ[9]
- DDR A D10 E6 SA_DQ[10]
- DDR A D11 F7 SA_DQ[11]
- DDR A D12 E9 SA_DQ[12]
- DDR A D13 B7 SA_DQ[13]
- DDR A D14 E7 SA_DQ[14]
- DDR A D15 H10 SA_DQ[15]
- DDR A D16 H10 SA_DQ[16]
- DDR A D17 G8 SA_DQ[17]
- DDR A D18 K8 SA_DQ[18]
- DDR A D19 J8 SA_DQ[19]
- DDR A D20 G7 SA_DQ[20]
- DDR A D21 G10 SA_DQ[21]
- DDR A D22 J7 SA_DQ[22]
- DDR A D23 J10 SA_DQ[23]
- DDR A D24 L7 SA_DQ[24]
- DDR A D25 L7 SA_DQ[25]
- DDR A D26 M8 SA_DQ[26]
- DDR A D27 L9 SA_DQ[27]
- DDR A D28 L6 SA_DQ[28]
- DDR A D29 L6 SA_DQ[29]
- DDR A D30 N8 SA_DQ[30]
- DDR A D31 P9 SA_DQ[31]
- DDR A D32 A8 SA_DQ[32]
- DDR A D33 A5 SA_DQ[33]
- DDR A D34 A6 SA_DQ[34]
- DDR A D35 A7 SA_DQ[35]
- DDR A D36 A8 SA_DQ[36]
- DDR A D37 A9 SA_DQ[37]
- DDR A D38 A8 SA_DQ[38]
- DDR A D39 A7 SA_DQ[39]
- DDR A D40 A10 SA_DQ[40]
- DDR A D41 A9 SA_DQ[41]
- DDR A D42 A10 SA_DQ[42]
- DDR A D43 A12 SA_DQ[43]
- DDR A D44 A8 SA_DQ[44]
- DDR A D45 A7 SA_DQ[45]
- DDR A D46 A11 SA_DQ[46]
- DDR A D47 A8 SA_DQ[47]
- DDR A D48 A8 SA_DQ[48]
- DDR A D49 A10 SA_DQ[49]
- DDR A D50 A11 SA_DQ[50]
- DDR A D51 A11 SA_DQ[51]
- DDR A D52 A9 SA_DQ[52]
- DDR A D53 A9 SA_DQ[53]
- DDR A D54 A11 SA_DQ[54]
- DDR A D55 A12 SA_DQ[55]
- DDR A D56 A12 SA_DQ[56]
- DDR A D57 A12 SA_DQ[57]
- DDR A D58 A13 SA_DQ[58]
- DDR A D59 A14 SA_DQ[59]
- DDR A D60 A12 SA_DQ[60]
- DDR A D61 A13 SA_DQ[61]
- DDR A D62 A14 SA_DQ[62]
- DDR A D63 A14 SA_DQ[63]

DDR SYSTEM MEMORY - A

- SA_CK[0] AA6 M_CLK_A_DDR0 9
- SA_CK#0 AA7 M_CLK_A_DDR#0 9
- SA_CKE[0] F7 DDR_CKE0_DIMMA 9
- SA_CK[1] Y6 M_CLK_A_DDR1 9
- SA_CK#1 Y5 M_CLK_A_DDR#1 9
- SA_CKE[1] F6 DDR_CKE1_DIMMA 9
- SA_CS#0 AE2 DDR_CS0_DIMMA# 9
- SA_CS#1 AE8 DDR_CS1_DIMMA# 9
- SA_ODT[0] AD8 M_A_ODT0 9
- SA_ODT[1] AF9 M_A_ODT1 9
- SA_DM[0] B9 DDR A DM0
- SA_DM[1] D7 DDR A DM1
- SA_DM[2] H7 DDR A DM2
- SA_DM[3] M7 DDR A DM3
- SA_DM[4] AG6 DDR A DM4
- SA_DM[5] AM7 DDR A DM5
- SA_DM[6] AN10 DDR A DM6
- SA_DM[7] AN13 DDR A DM7
- SA_DQS#0 C9 DDR A DQS#0
- SA_DQS#1 F8 DDR A DQS#1
- SA_DQS#2 J9 DDR A DQS#2
- SA_DQS#3 N9 DDR A DQS#3
- SA_DQS#4 AH7 DDR A DQS#4
- SA_DQS#5 AK9 DDR A DQS#5
- SA_DQS#6 AP11 DDR A DQS#6
- SA_DQS#7 AT13 DDR A DQS#7
- SA_DQS[0] C8 DDR A DQS0
- SA_DQS[1] F9 DDR A DQS1
- SA_DQS[2] H9 DDR A DQS2
- SA_DQS[3] M9 DDR A DQS3
- SA_DQS[4] AH8 DDR A DQS4
- SA_DQS[5] AK10 DDR A DQS5
- SA_DQS[6] AN11 DDR A DQS6
- SA_DQS[7] AR13 DDR A DQS7
- SA_MA[0] Y3 DDR A MA0
- SA_MA[1] W1 DDR A MA1
- SA_MA[2] AA8 DDR A MA2
- SA_MA[3] AA3 DDR A MA3
- SA_MA[4] V1 DDR A MA4
- SA_MA[5] AA9 DDR A MA5
- SA_MA[6] V8 DDR A MA6
- SA_MA[7] T1 DDR A MA7
- SA_MA[8] Y9 DDR A MA8
- SA_MA[9] U6 DDR A MA9
- SA_MA[10] AD4 DDR A MA10
- SA_MA[11] T2 DDR A MA11
- SA_MA[12] U3 DDR A MA12
- SA_MA[13] AG8 DDR A MA13
- SA_MA[14] T3 DDR A MA14
- SA_MA[15] V9 DDR A MA15

- 9 DDR_A_BS0 AC3 SA_BS[0]
- 9 DDR_A_BS1 AB2 SA_BS[1]
- 9 DDR_A_BS2 U7 SA_BS[2]
- 9 DDR_A_CAS# AE1 SA_CAS#
- 9 DDR_A_RAS# AB3 SA_RAS#
- 9 DDR_A_WE# AE9 SA_WE#

IC_AUB_CFD_rPGA_R1P0

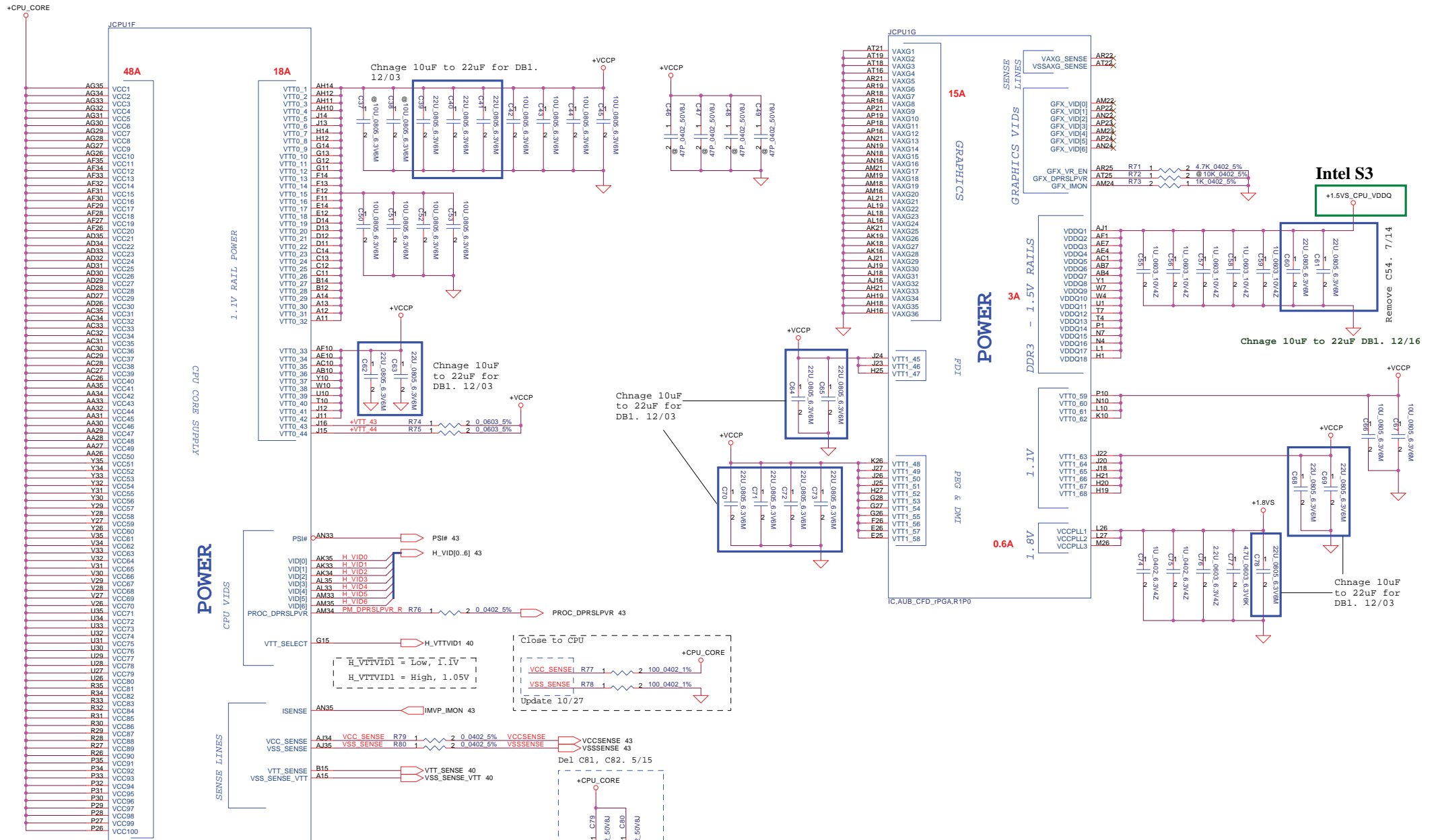
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- DDR B D1 A5 SB_DQ[1]
- DDR B D2 C3 SB_DQ[2]
- DDR B D3 B3 SB_DQ[3]
- DDR B D4 E4 SB_DQ[4]
- DDR B D5 A6 SB_DQ[5]
- DDR B D6 A4 SB_DQ[6]
- DDR B D7 D1 SB_DQ[7]
- DDR B D8 D1 SB_DQ[8]
- DDR B D9 D2 SB_DQ[9]
- DDR B D10 F1 SB_DQ[10]
- DDR B D11 F2 SB_DQ[11]
- DDR B D12 C2 SB_DQ[12]
- DDR B D13 F5 SB_DQ[13]
- DDR B D14 F3 SB_DQ[14]
- DDR B D15 G4 SB_DQ[15]
- DDR B D16 H6 SB_DQ[16]
- DDR B D17 G2 SB_DQ[17]
- DDR B D18 J6 SB_DQ[18]
- DDR B D19 J3 SB_DQ[19]
- DDR B D20 G5 SB_DQ[20]
- DDR B D21 G1 SB_DQ[21]
- DDR B D22 J2 SB_DQ[22]
- DDR B D23 J1 SB_DQ[23]
- DDR B D24 J5 SB_DQ[24]
- DDR B D25 K2 SB_DQ[25]
- DDR B D26 L3 SB_DQ[26]
- DDR B D27 M1 SB_DQ[27]
- DDR B D28 K5 SB_DQ[28]
- DDR B D29 K4 SB_DQ[29]
- DDR B D30 M4 SB_DQ[30]
- DDR B D31 K8 SB_DQ[31]
- DDR B D32 AE3 SB_DQ[32]
- DDR B D33 AG1 SB_DQ[33]
- DDR B D34 AJ3 SB_DQ[34]
- DDR B D35 AK1 SB_DQ[35]
- DDR B D36 AG4 SB_DQ[36]
- DDR B D37 AG3 SB_DQ[37]
- DDR B D38 AJ4 SB_DQ[38]
- DDR B D39 AH4 SB_DQ[39]
- DDR B D40 AK3 SB_DQ[40]
- DDR B D41 AK4 SB_DQ[41]
- DDR B D42 AM6 SB_DQ[42]
- DDR B D43 AN2 SB_DQ[43]
- DDR B D44 AK5 SB_DQ[44]
- DDR B D45 AK2 SB_DQ[45]
- DDR B D46 AM4 SB_DQ[46]
- DDR B D47 AM3 SB_DQ[47]
- DDR B D48 AP3 SB_DQ[48]
- DDR B D49 AN5 SB_DQ[49]
- DDR B D50 AT4 SB_DQ[50]
- DDR B D51 AM6 SB_DQ[51]
- DDR B D52 AN4 SB_DQ[52]
- DDR B D53 AN3 SB_DQ[53]
- DDR B D54 AT5 SB_DQ[54]
- DDR B D55 AT6 SB_DQ[55]
- DDR B D56 AN7 SB_DQ[56]
- DDR B D57 AP8 SB_DQ[57]
- DDR B D58 AP8 SB_DQ[58]
- DDR B D59 AT9 SB_DQ[59]
- DDR B D60 AT7 SB_DQ[60]
- DDR B D61 AP9 SB_DQ[61]
- DDR B D62 AR10 SB_DQ[62]
- DDR B D63 AT10 SB_DQ[63]
- 10 DDR_B_BS0 AB1 SB_BS[0]
- 10 DDR_B_BS1 W5 SB_BS[1]
- 10 DDR_B_BS2 R7 SB_BS[2]
- 10 DDR_B_CAS# AC5 SB_CAS#
- 10 DDR_B_RAS# V7 SB_RAS#
- 10 DDR_B_WE# AC6 SB_WE#

DDR SYSTEM MEMORY - B

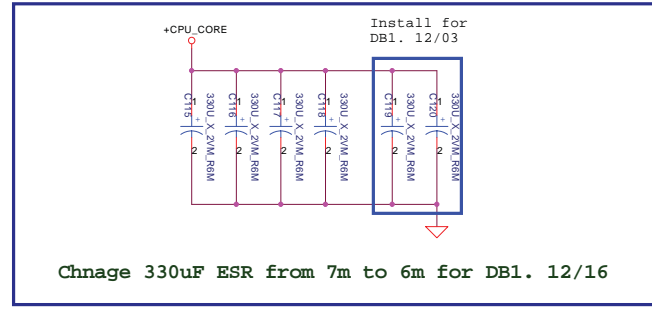
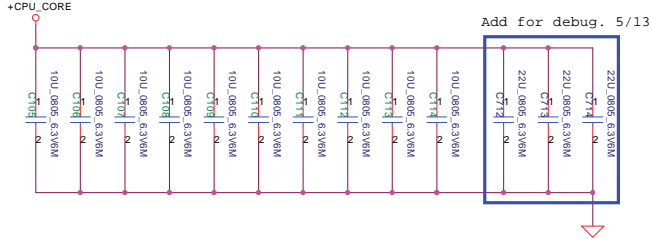
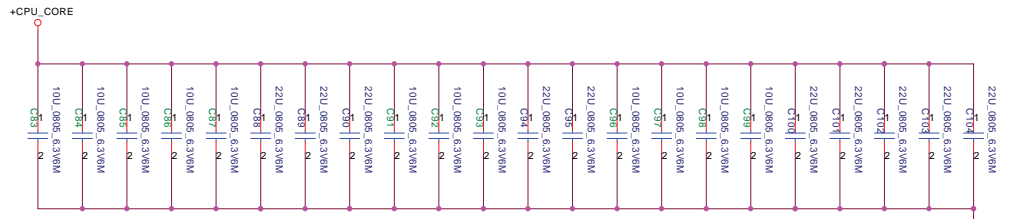
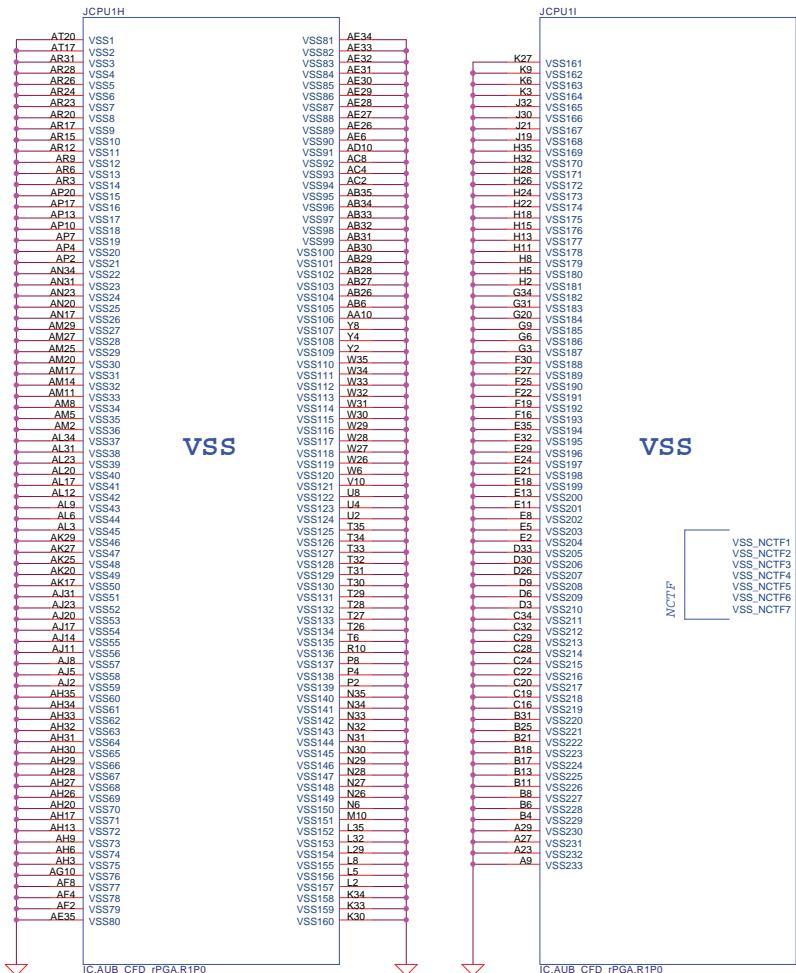
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- SB_CK#0 W9 M_CLK_B_DDR#0 10
- SB_CKE[0] M3 DDR_CKE0_DIMMB 10
- SB_CK[1] V8 M_CLK_B_DDR1 10
- SB_CK#1 V7 M_CLK_B_DDR#1 10
- SB_CKE[1] M2 DDR_CKE1_DIMMB 10
- SB_CS#0 AB8 DDR_CS0_DIMMB# 10
- SB_CS#1 AD6 DDR_CS1_DIMMB# 10
- SB_ODT[0] AC7 M_B_ODT0 10
- SB_ODT[1] AD1 M_B_ODT1 10
- SB_DM[0] D4 DDR B DM0
- SB_DM[1] E1 DDR B DM1
- SB_DM[2] H1 DDR B DM2
- SB_DM[3] K1 DDR B DM3
- SB_DM[4] AH1 DDR B DM4
- SB_DM[5] AL2 DDR B DM5
- SB_DM[6] AR4 DDR B DM6
- SB_DM[7] AR8 DDR B DM7
- SB_DQS#0 D5 DDR B DQS#0
- SB_DQS#1 E4 DDR B DQS#1
- SB_DQS#2 J4 DDR B DQS#2
- SB_DQS#3 J4 DDR B DQS#3
- SB_DQS#4 AH2 DDR B DQS#4
- SB_DQS#5 AL4 DDR B DQS#5
- SB_DQS#6 AR5 DDR B DQS#6
- SB_DQS#7 AR8 DDR B DQS#7
- SB_DQS[0] C5 DDR B DQS0
- SB_DQS[1] E3 DDR B DQS1
- SB_DQS[2] H4 DDR B DQS2
- SB_DQS[3] M5 DDR B DQS3
- SB_DQS[4] AG2 DDR B DQS4
- SB_DQS[5] AL5 DDR B DQS5
- SB_DQS[6] AP5 DDR B DQS6
- SB_DQS[7] AR7 DDR B DQS7
- SB_MA[0] U5 DDR B MA0
- SB_MA[1] V2 DDR B MA1
- SB_MA[2] T6 DDR B MA2
- SB_MA[3] V3 DDR B MA3
- SB_MA[4] T8 DDR B MA4
- SB_MA[5] R1 DDR B MA5
- SB_MA[6] R2 DDR B MA6
- SB_MA[7] R6 DDR B MA7
- SB_MA[8] R4 DDR B MA8
- SB_MA[9] R5 DDR B MA9
- SB_MA[10] AB5 DDR B MA10
- SB_MA[11] F3 DDR B MA11
- SB_MA[12] R3 DDR B MA12
- SB_MA[13] AF7 DDR B MA13
- SB_MA[14] P5 DDR B MA14
- SB_MA[15] N1 DDR B MA15

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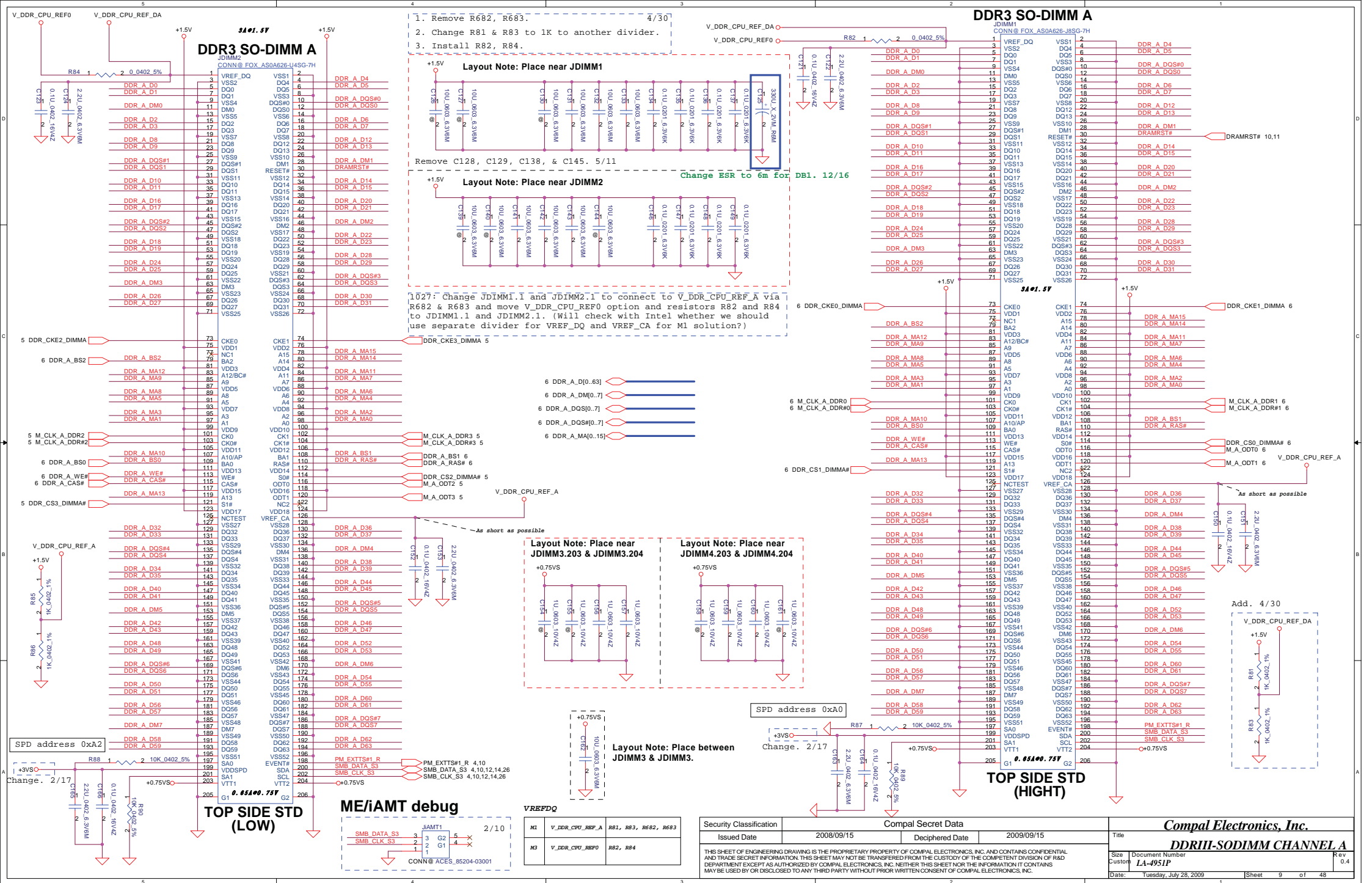
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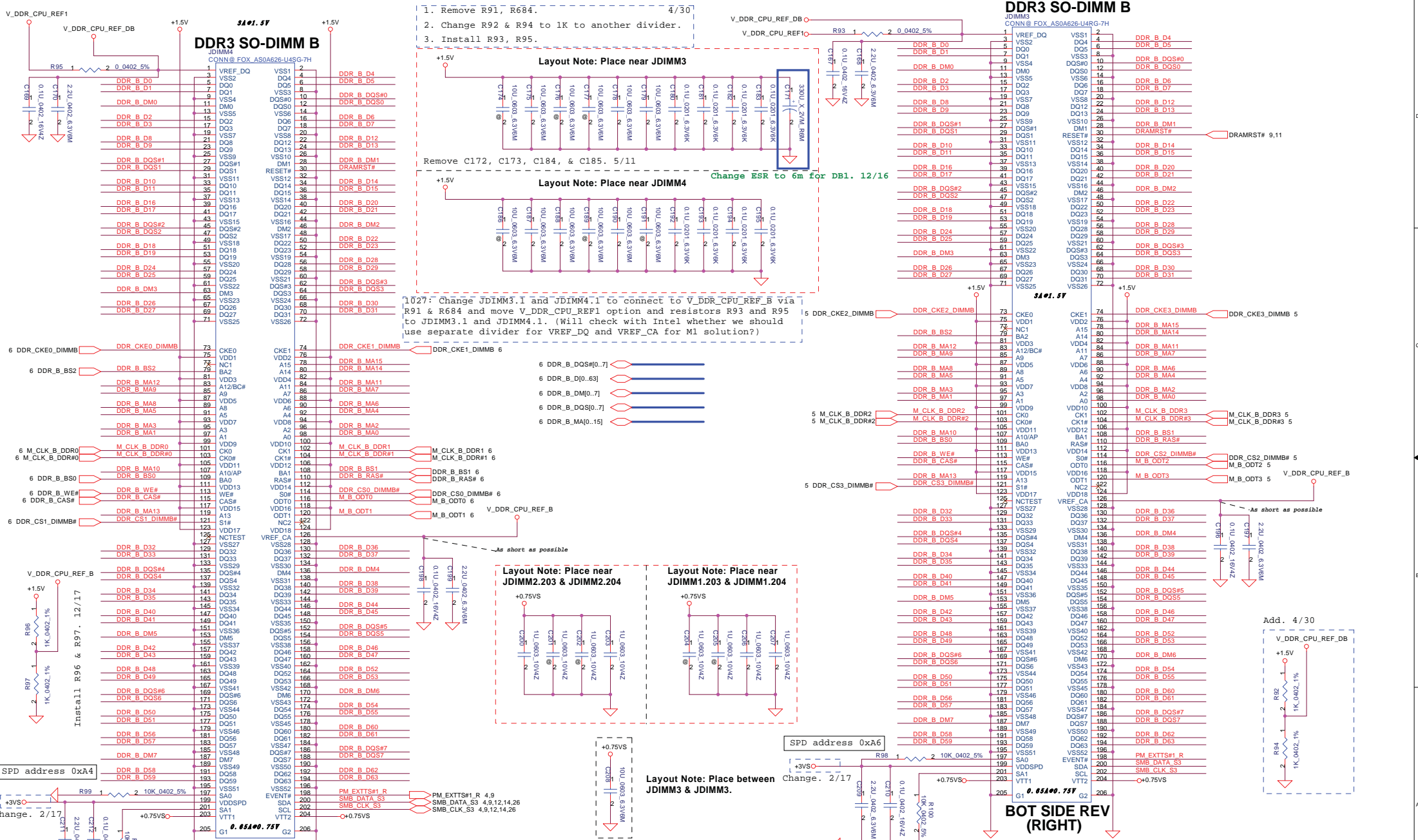


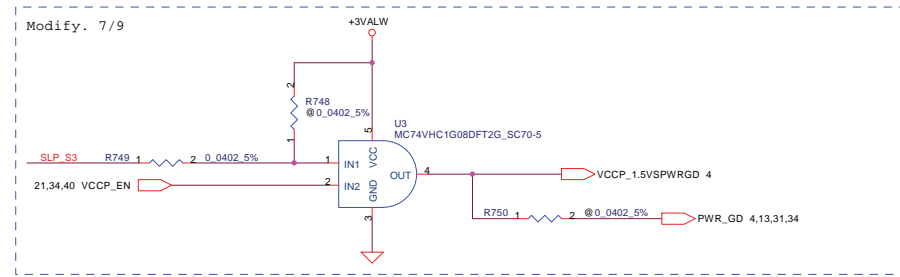
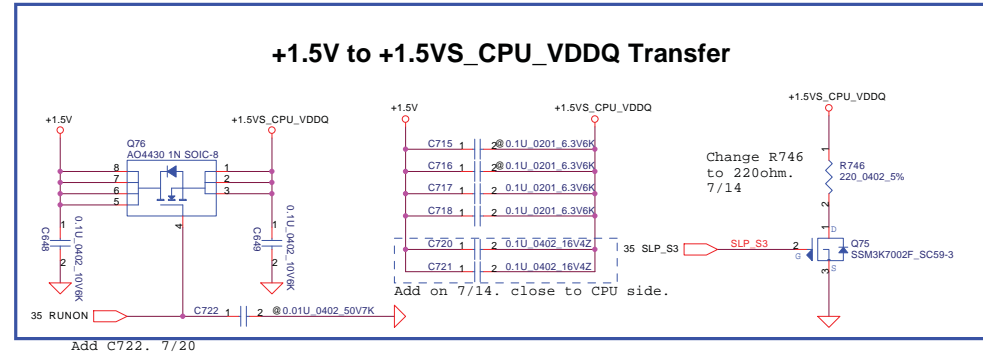
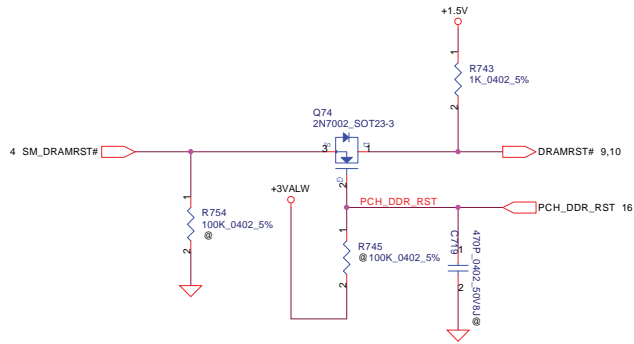
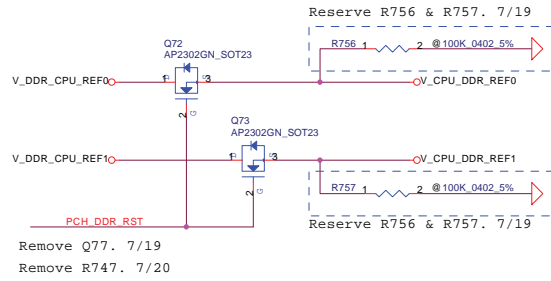
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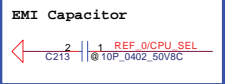
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				Document Number
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				0.4
				Date: Tuesday, July 28, 2009
				Sheet 8 of 48



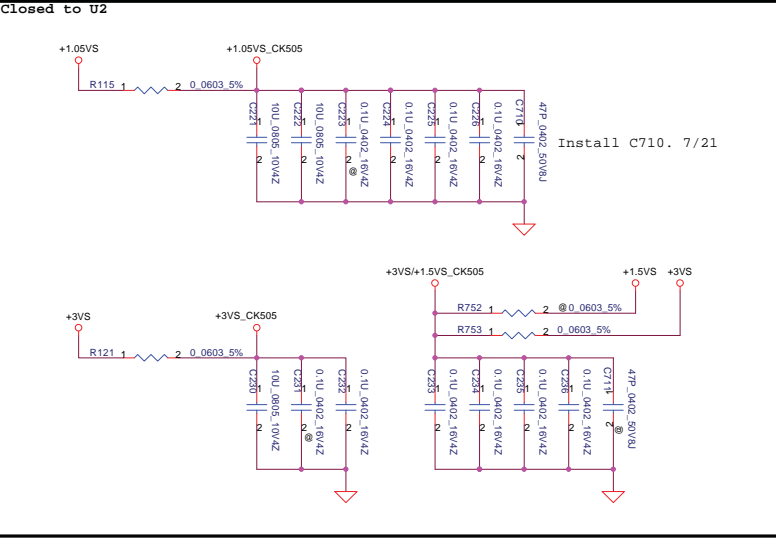
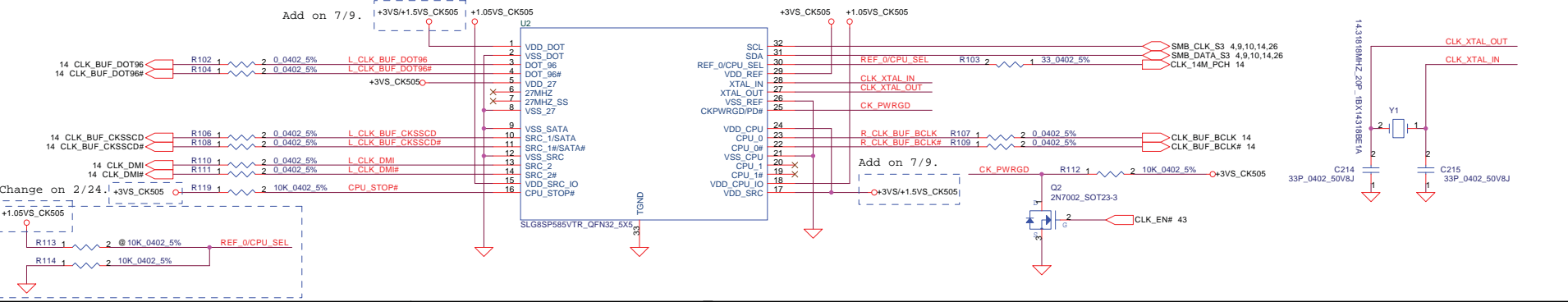




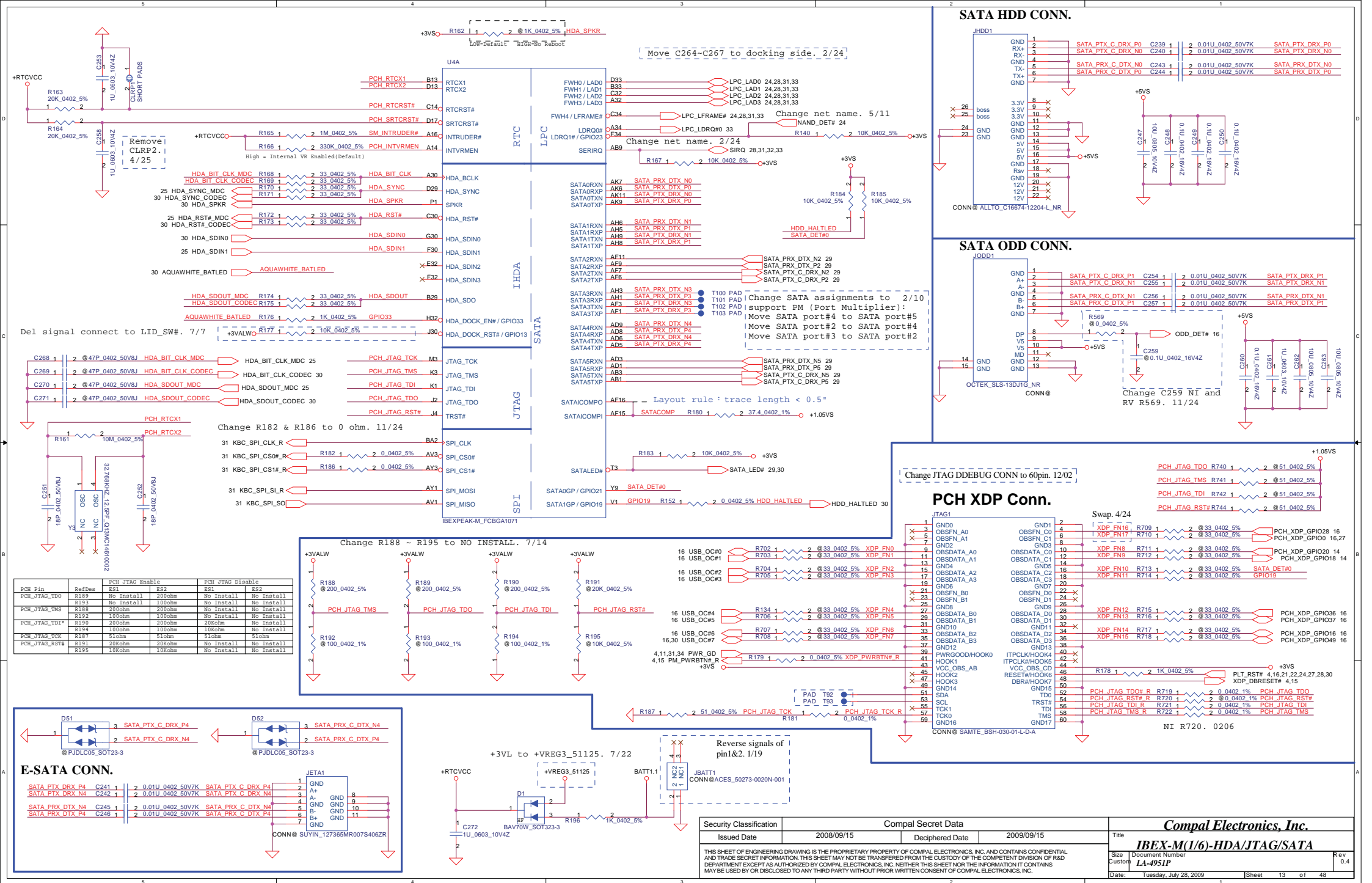
Security Classification	Compal Secret Data		Title	
Issued Date	2008/09/15	Deciphered Date	2009/09/15	Intel S3 power saving
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				Document Number LA-4951P
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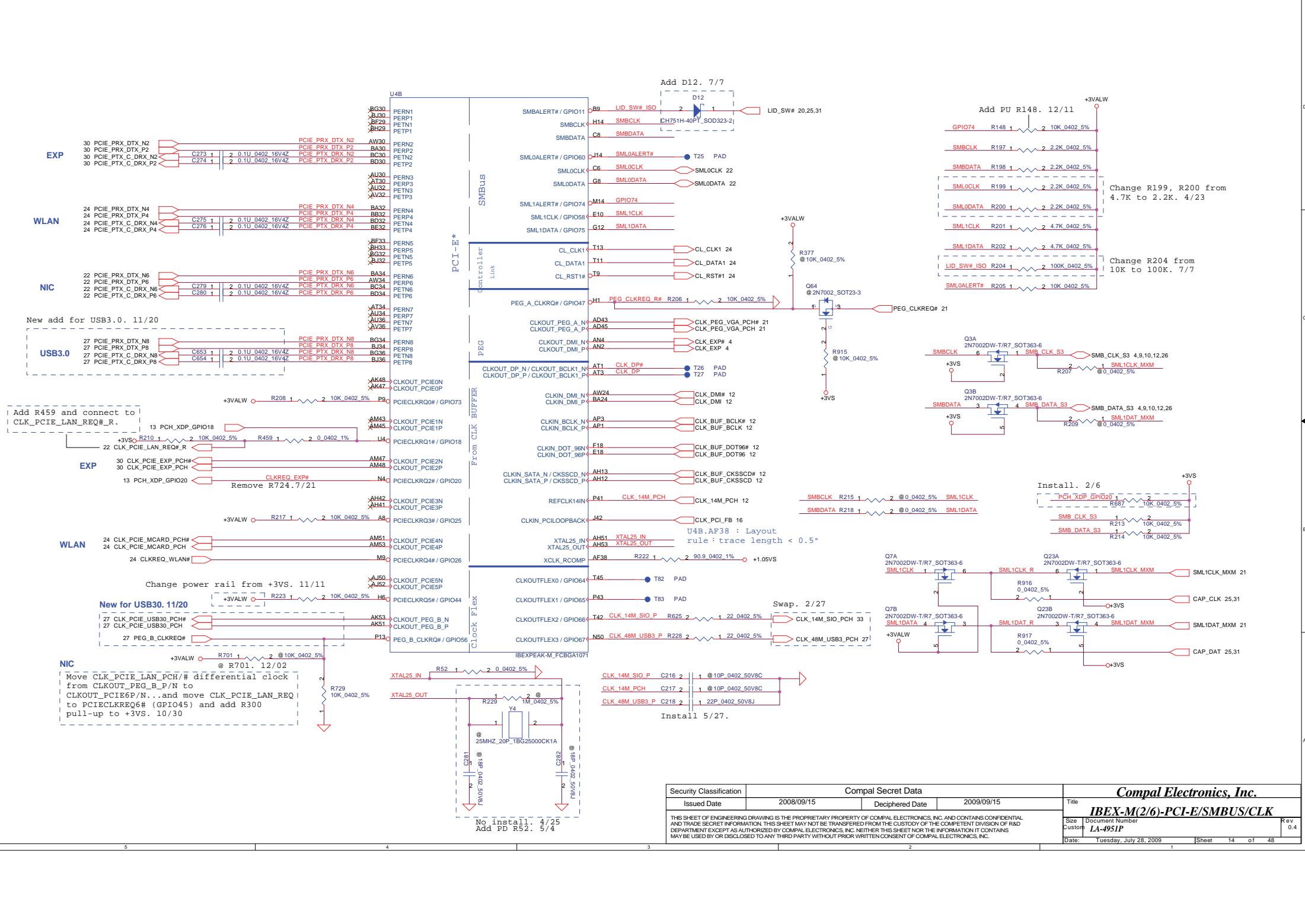


PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

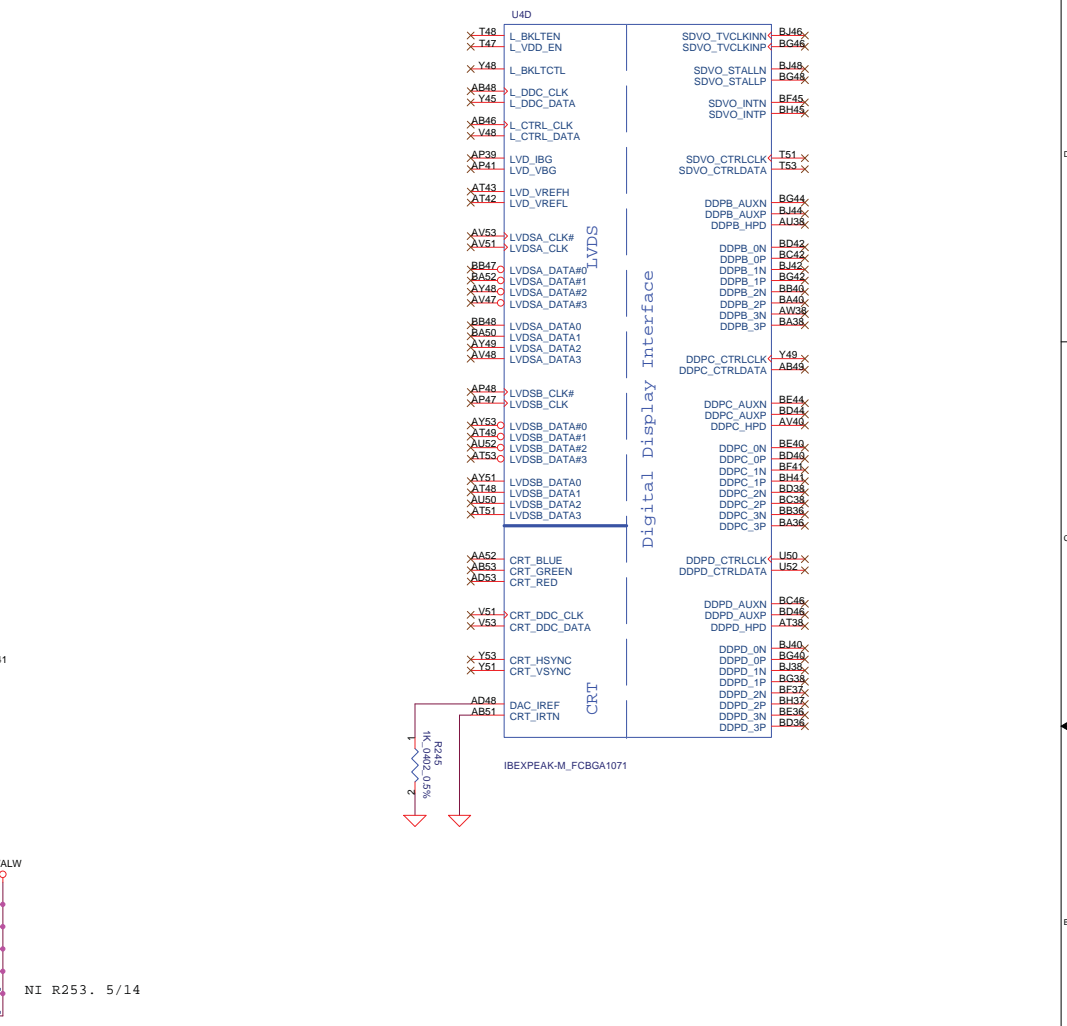
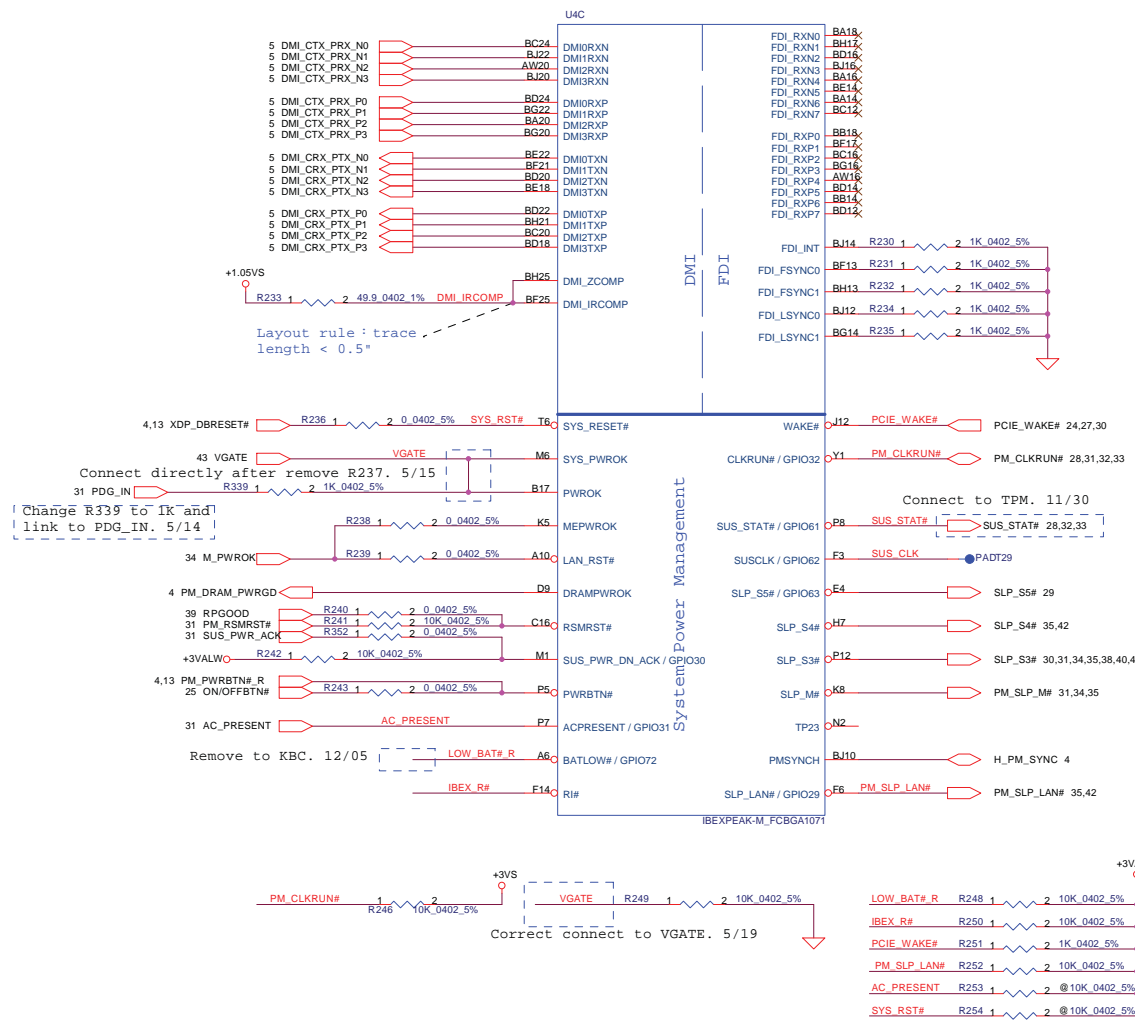


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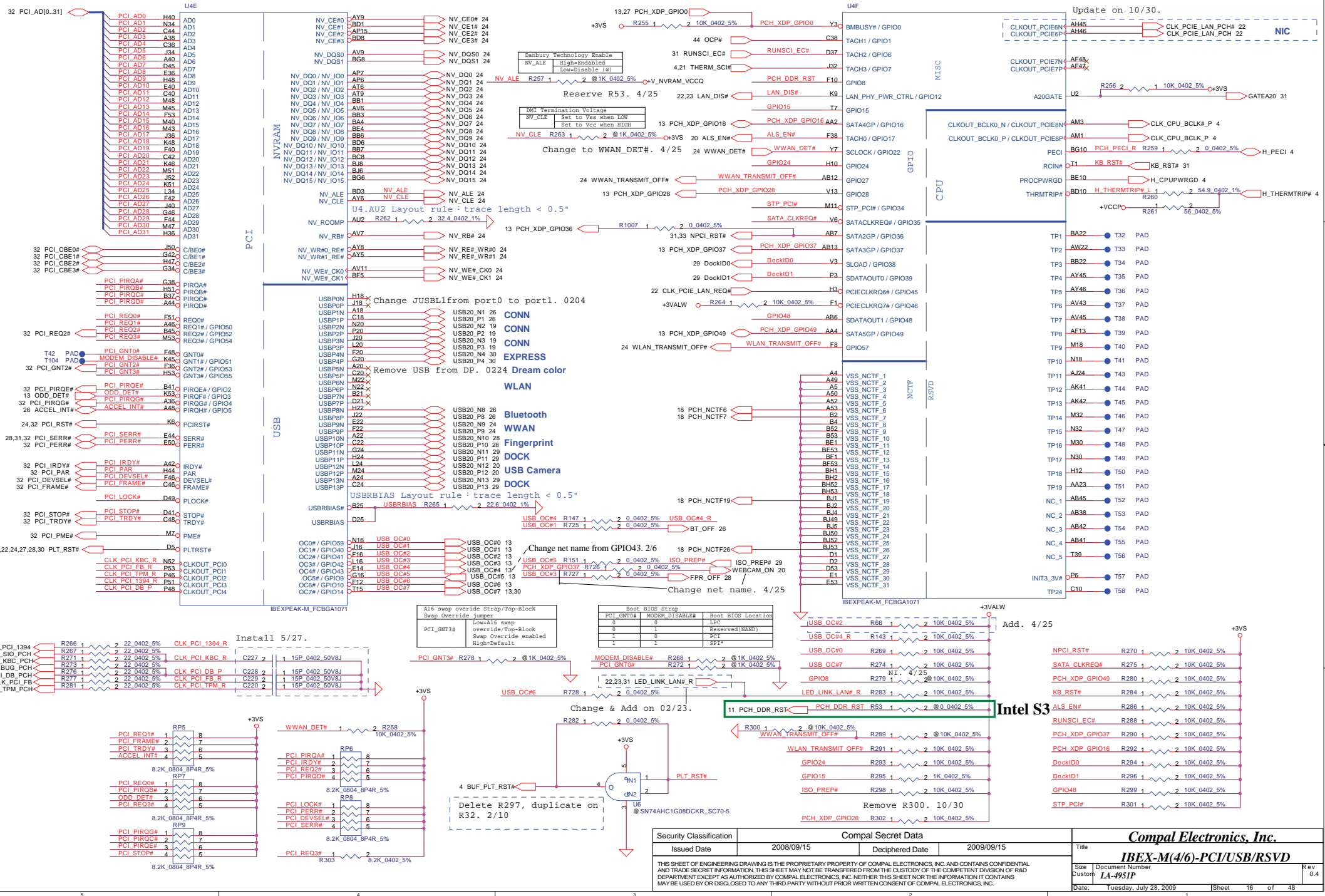


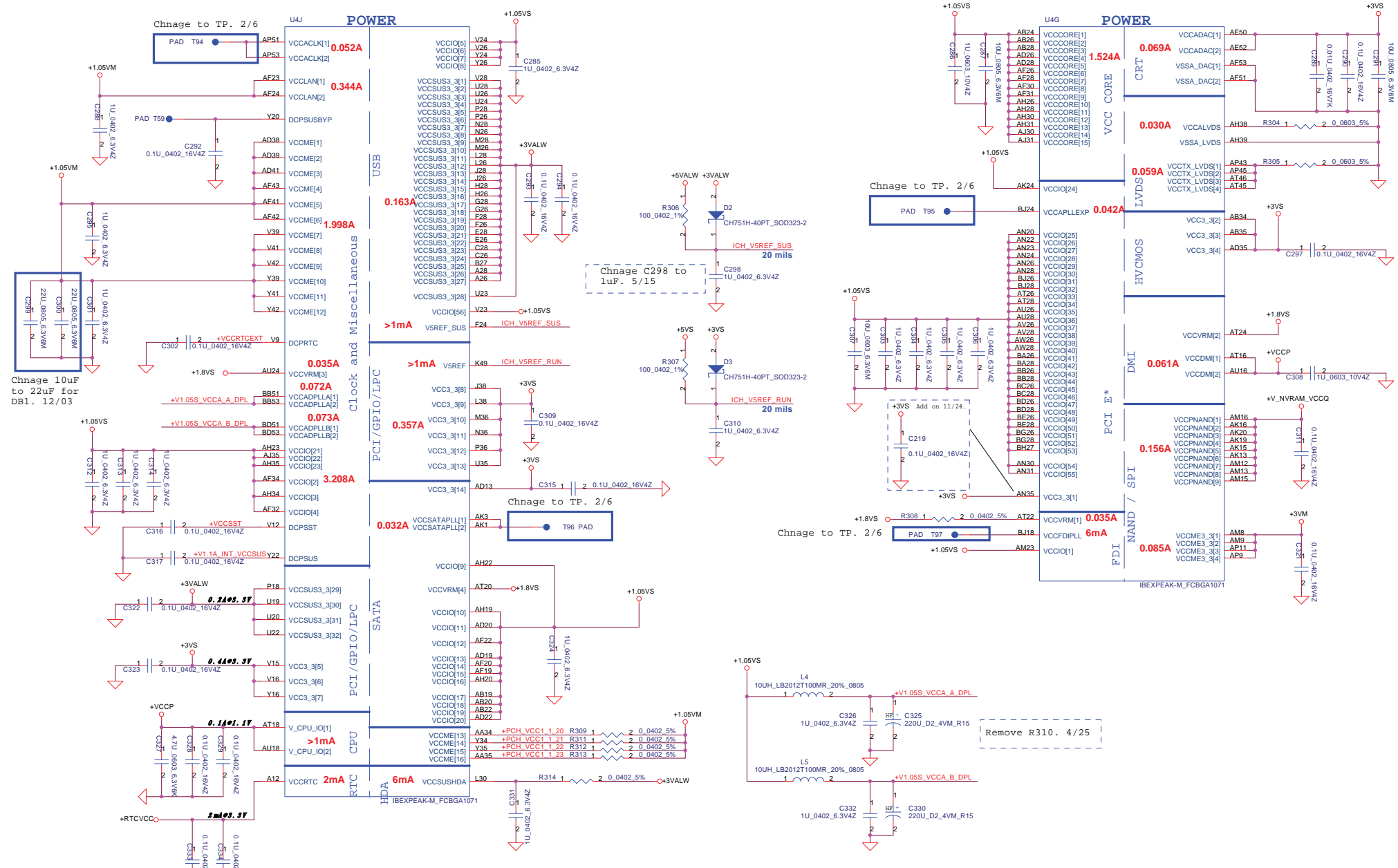


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Chnage 10uF to 22uF for DB1. 12/03

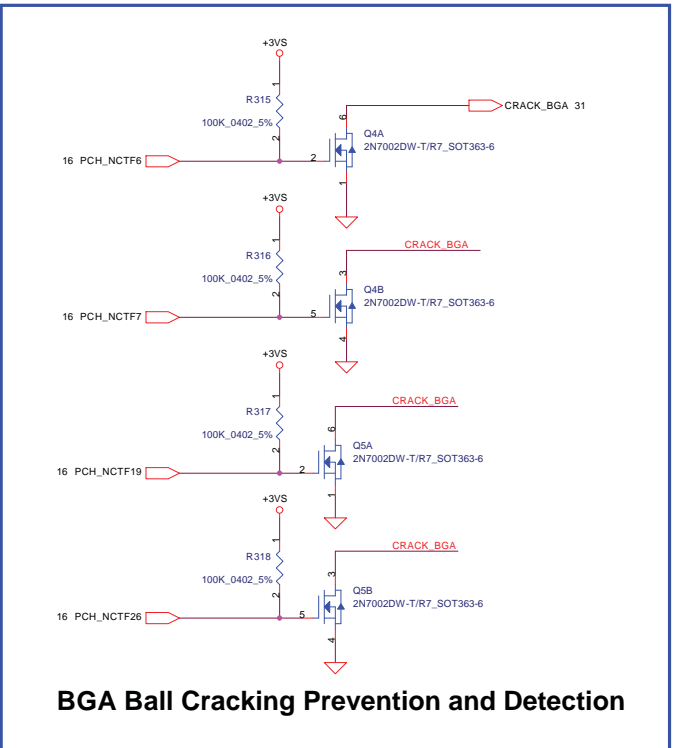
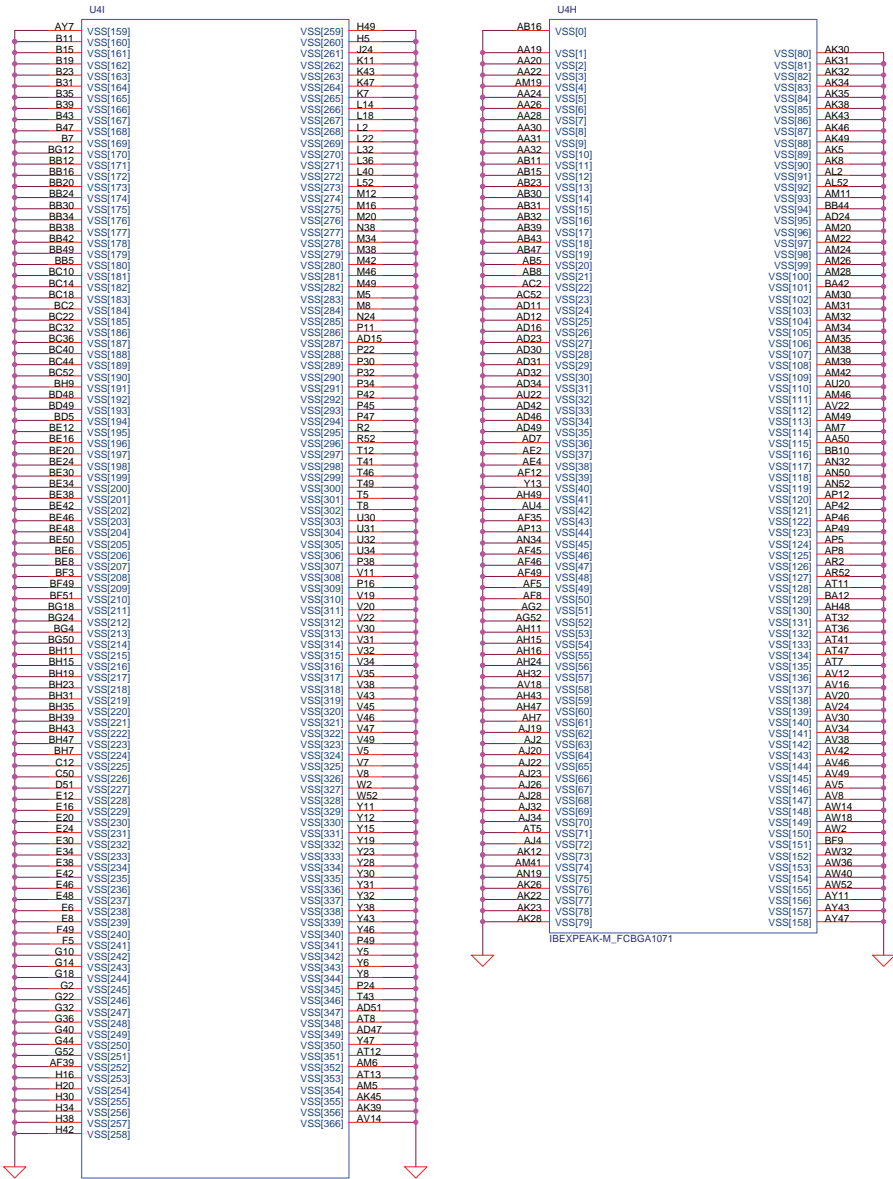
Chnage C298 to 1uF. 5/15

Chnage to TP. 2/6

Chnage to TP. 2/6

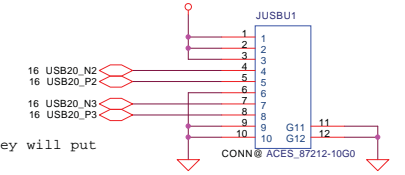
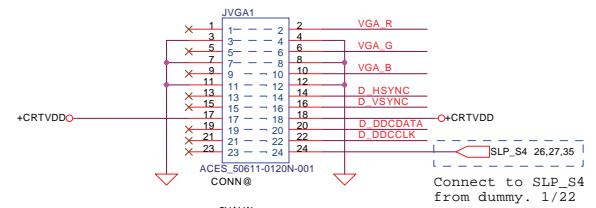
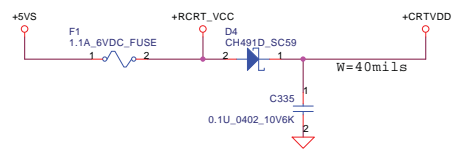
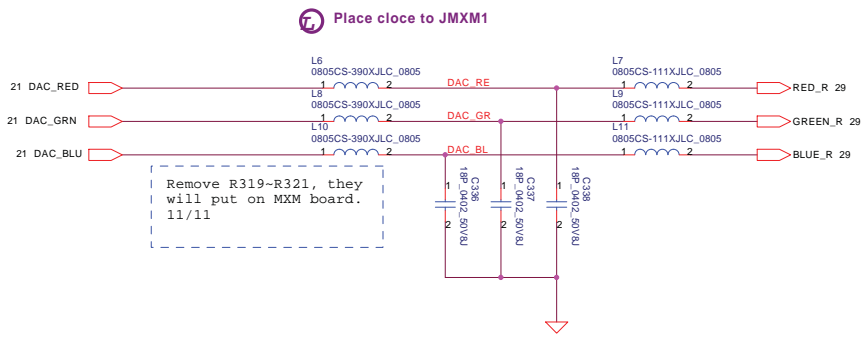
Remove R310. 4/25

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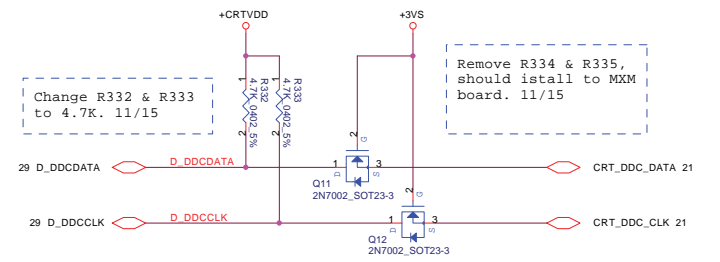
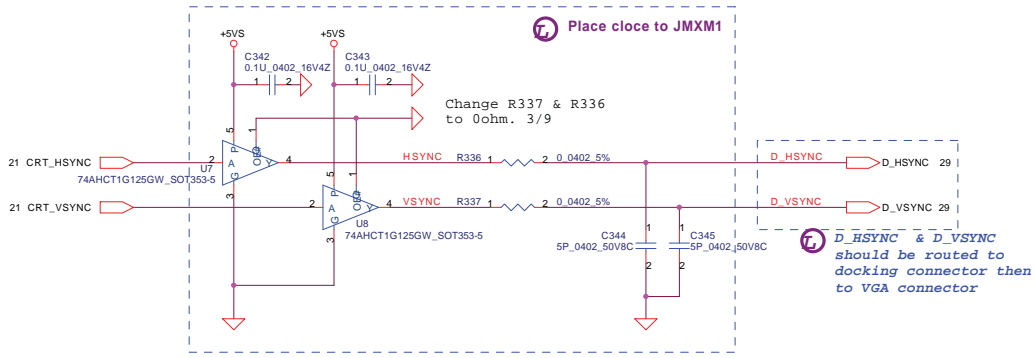
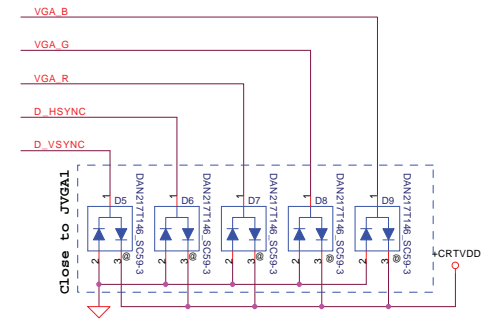
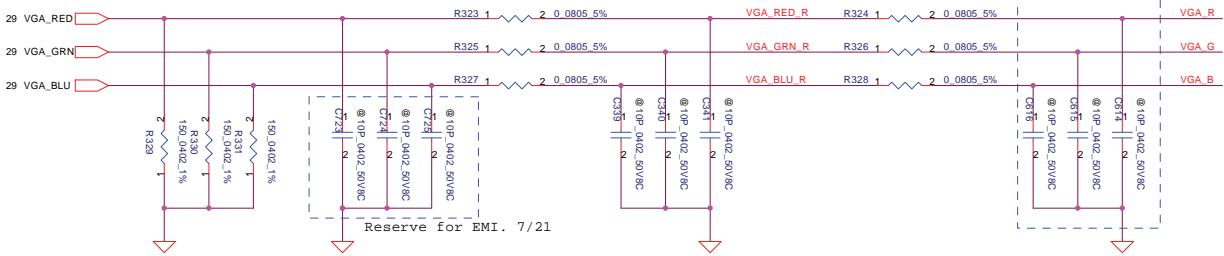
BGA Ball Cracking Prevention and Detection

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1		18		48



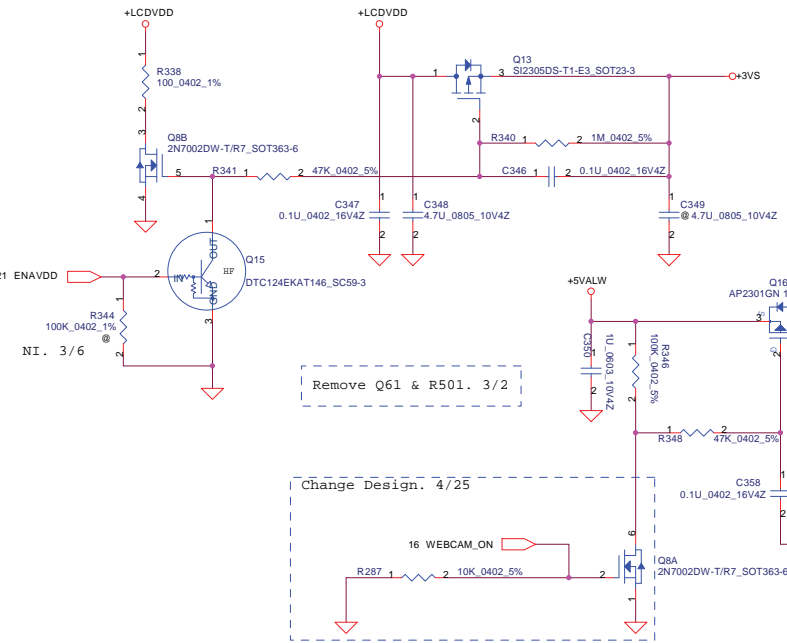
Remove R319-R321, they will put on MXM board. 11/11

Add C614-C616 for Nvidia request. 11/15



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LCD POWER CIRCUIT

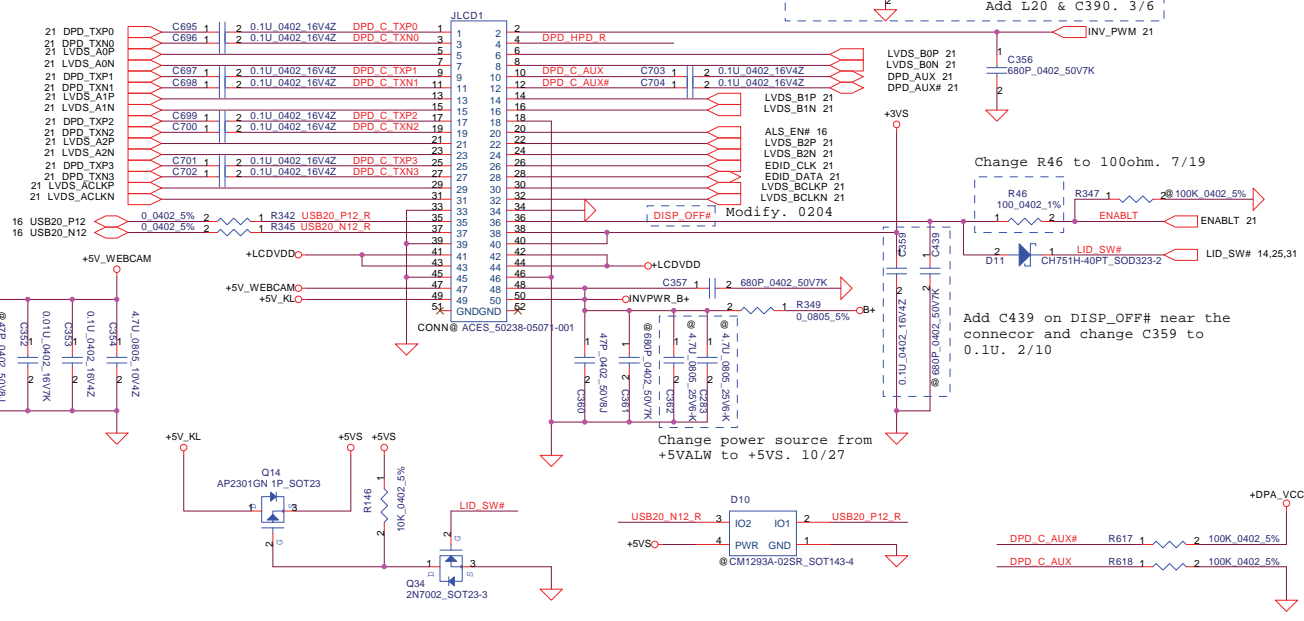


Remove Q61 & R501. 3/2

Change Design. 4/25

LCD/PANEL BD. CONN.

Modify pin assignment. 2/23

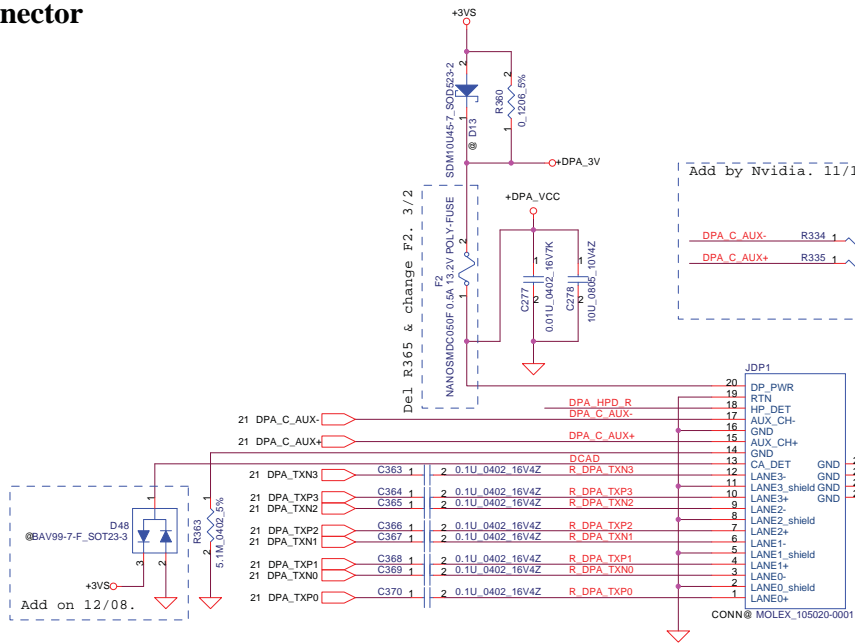


Change R46 to 100ohm. 7/19

Add C439 on DISP_OFF# near the connector and change C359 to 0.1U. 2/10

Change power source from +5VALW to +5VS. 10/27

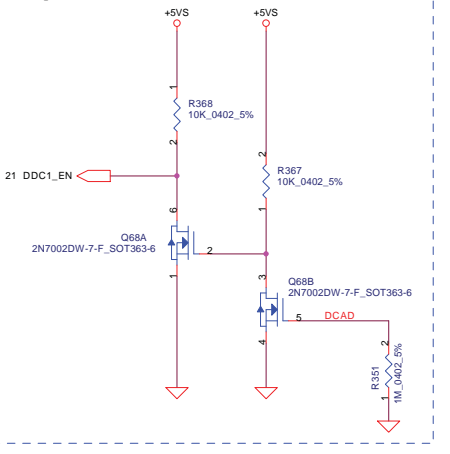
Display port Connector



Add by Nvidia. 11/15

Remove R367 pulldown on DPA_HP. There is a 100k pulldown on the module. 11/15

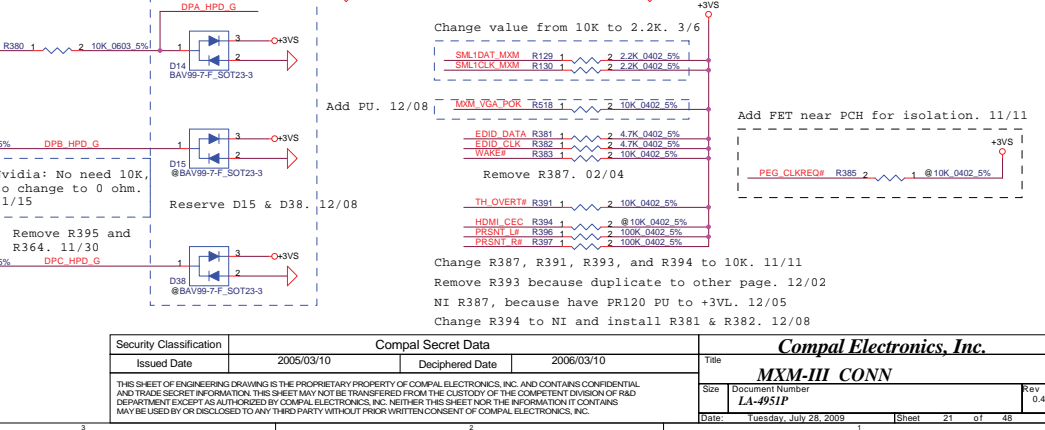
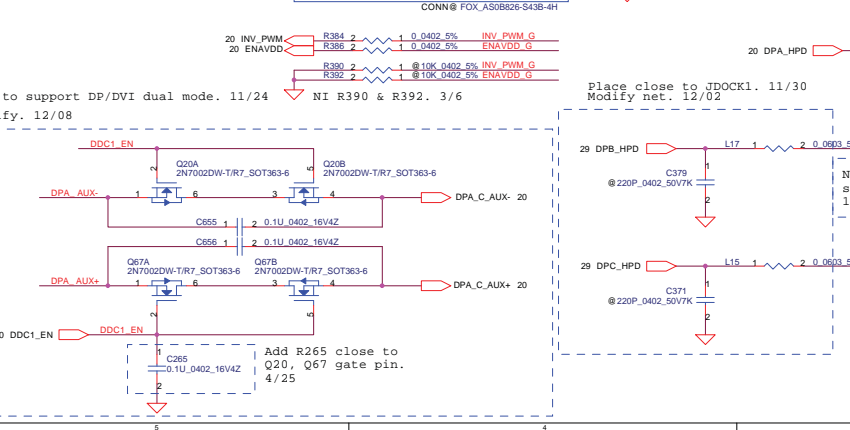
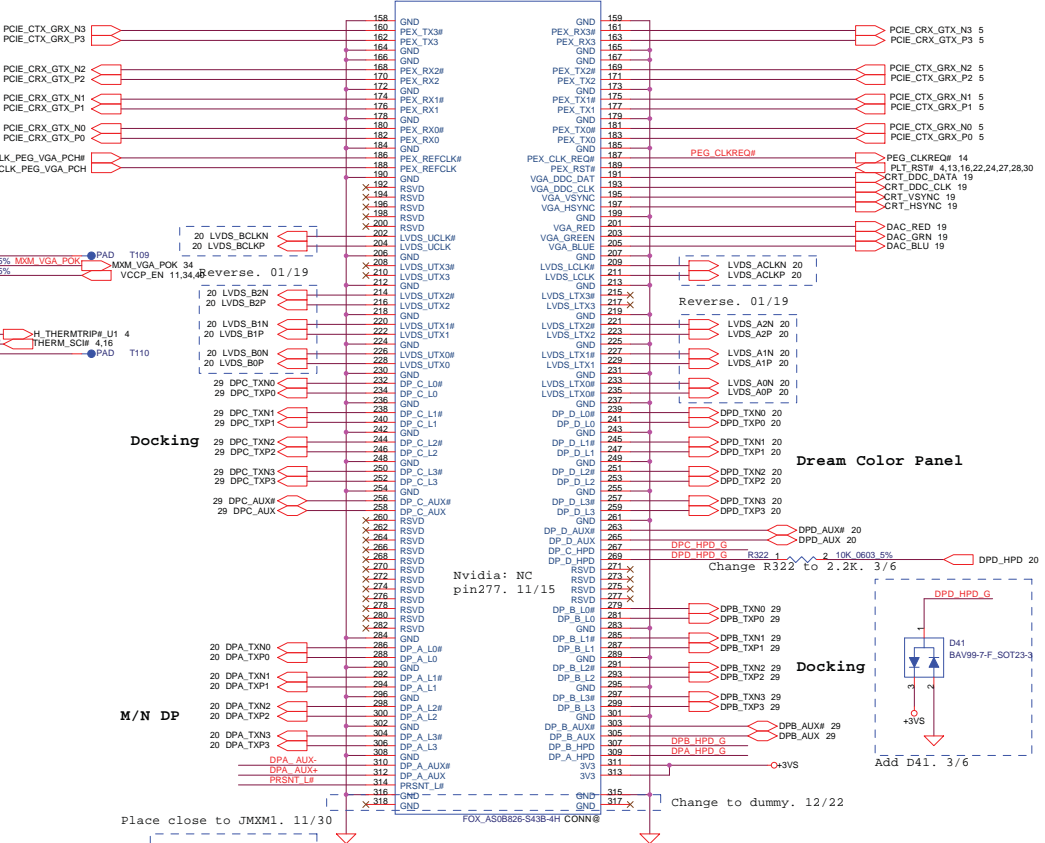
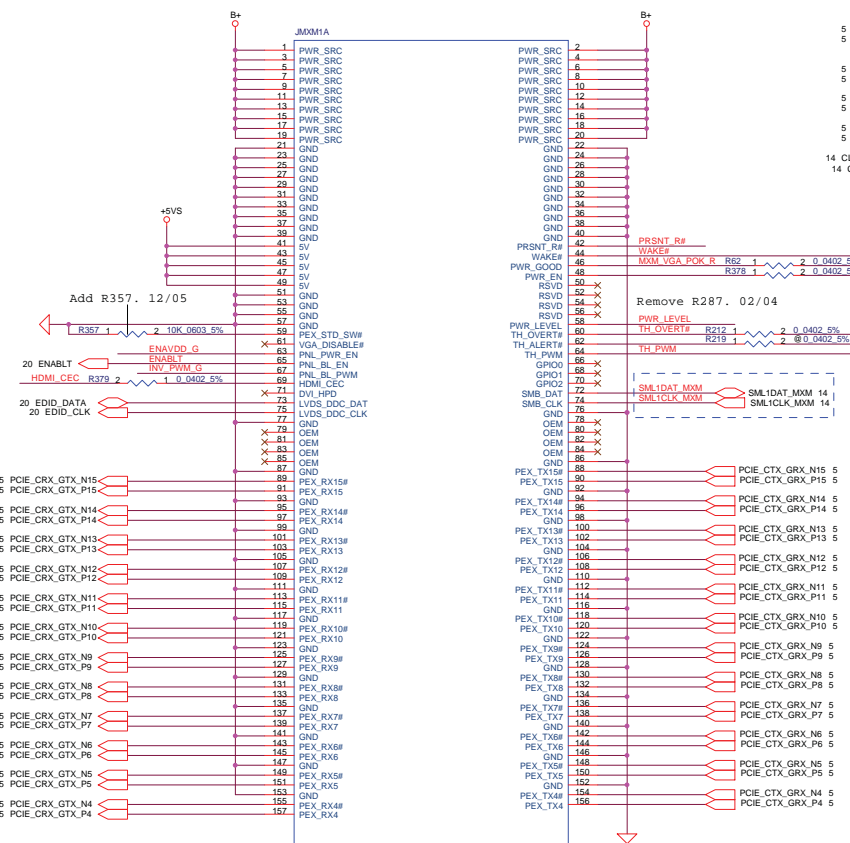
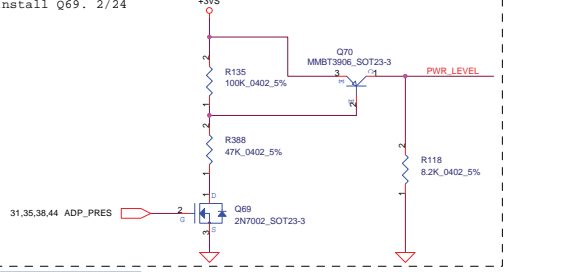
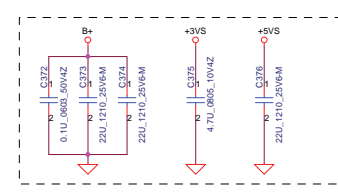
Add by Nvidia. 12/08



Layout Note: DPB_HPD and DPC_HPD must not routed close to high speed signals.

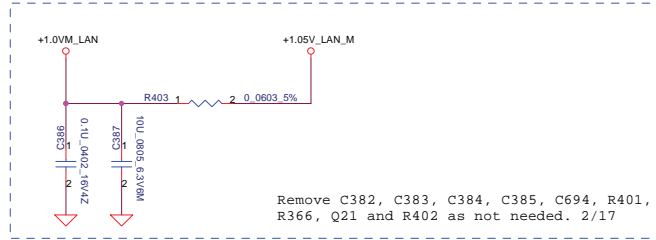
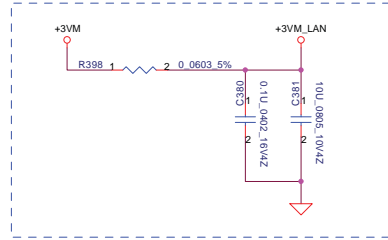
Remove Q19 & R376. 2/24
Remove C377. 7/10

Layout Note:
Place as close as to MXM connector



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Update on 10/27.

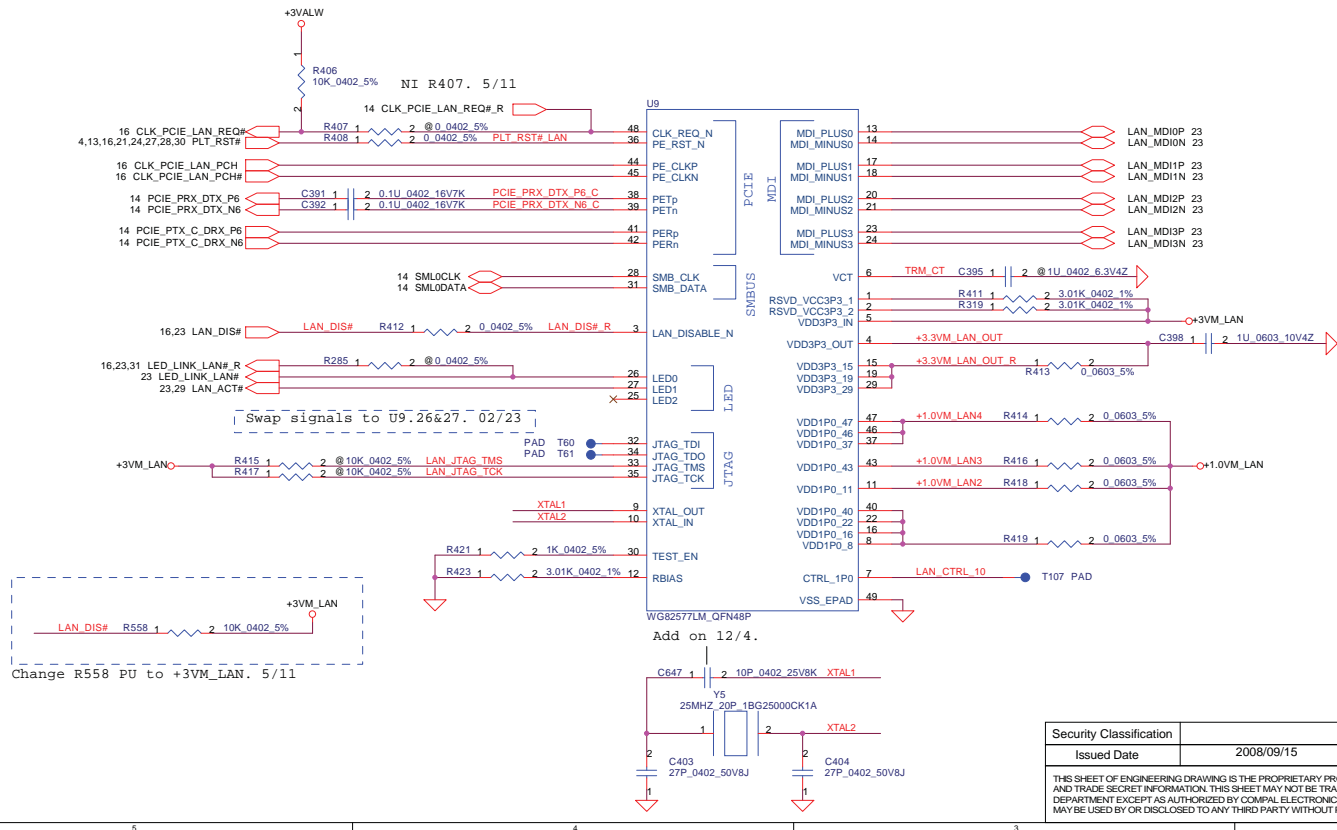


Remove C382, C383, C384, C385, C694, R401, R366, Q21 and R402 as not needed. 2/17

Remove note. 0205
 Remove C388, C389, C390, & C393 on +1.0VM_LAN; Remove C394, C396 & C397 on +3.3VM_LAN_OUT_R; Remove C399 & C400 on +1.0VM_LAN4; Remove C401 on +1.0VM_LAN3; and Remove C402 on +1.0VM_LAN2 as done in Intel's RedFort CRB

Remove Q17, R124, and R405 (Intel confirmed isolation not required for Hanksville)
 2/23

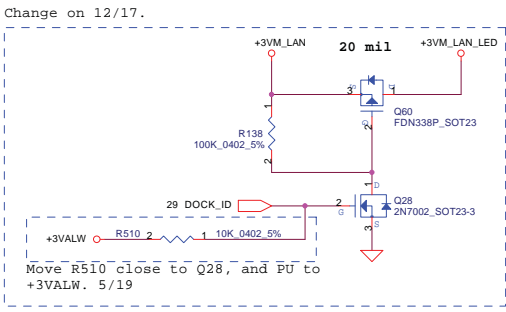
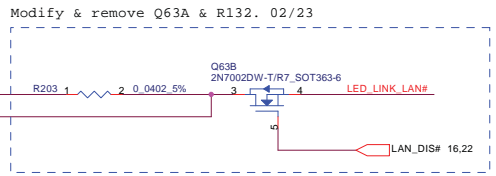
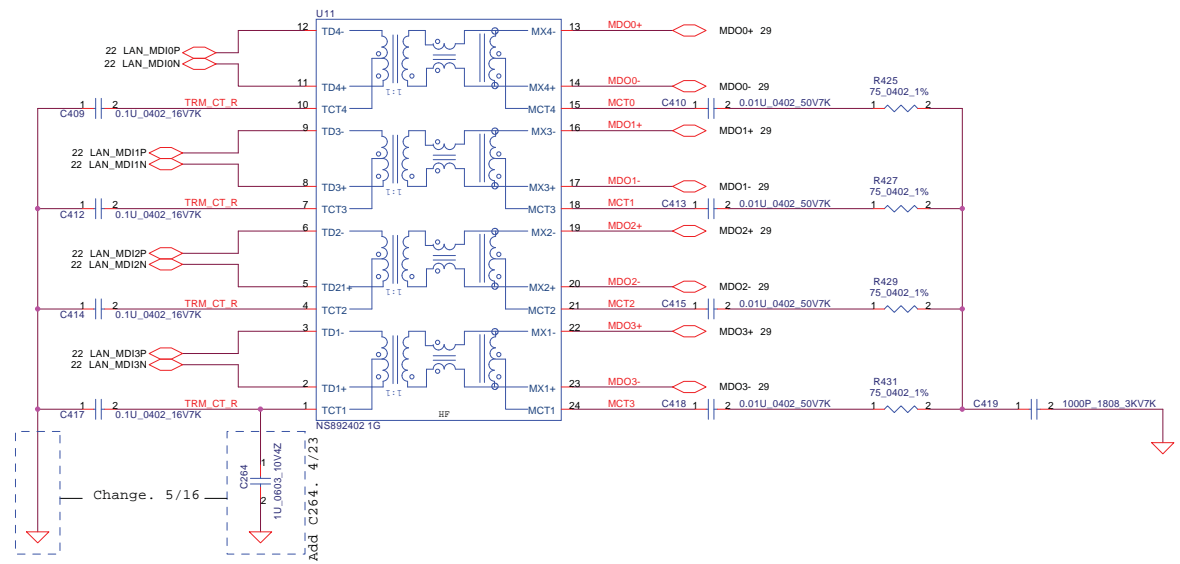
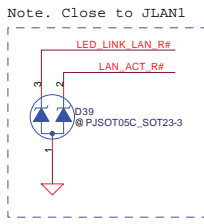
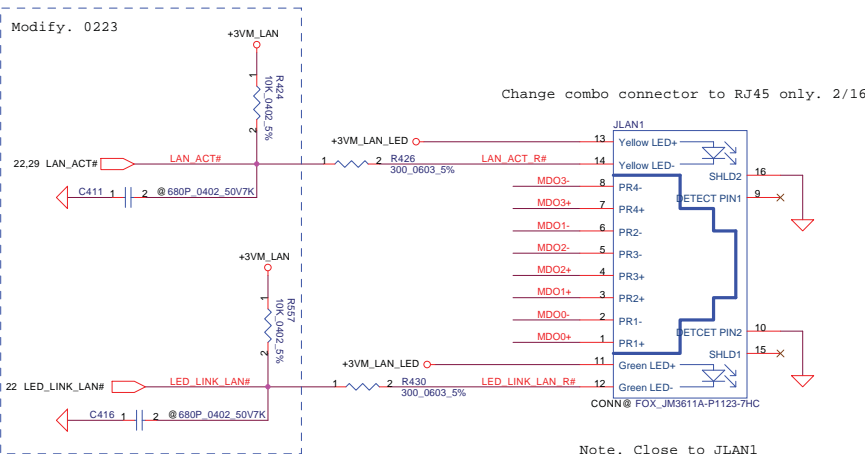
Remove R354, R355, Q22A, Q22B; and connect SML0CLK and SML0DATA directly to LAN_SM_CLK and LAN_SM_DAT. 2/23



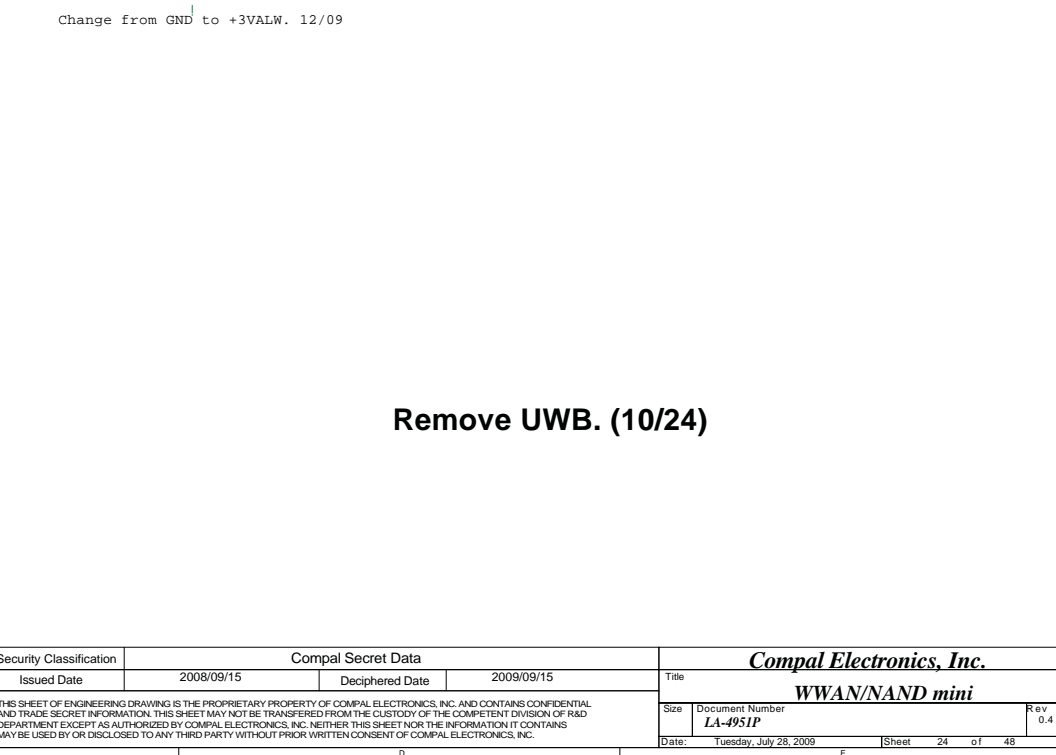
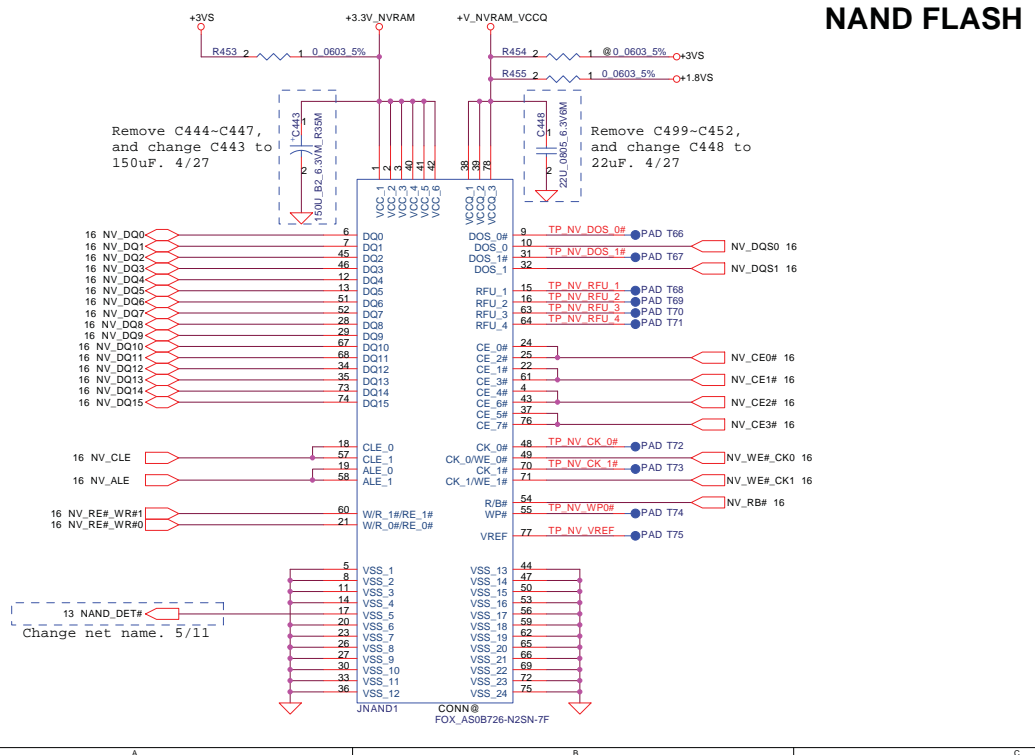
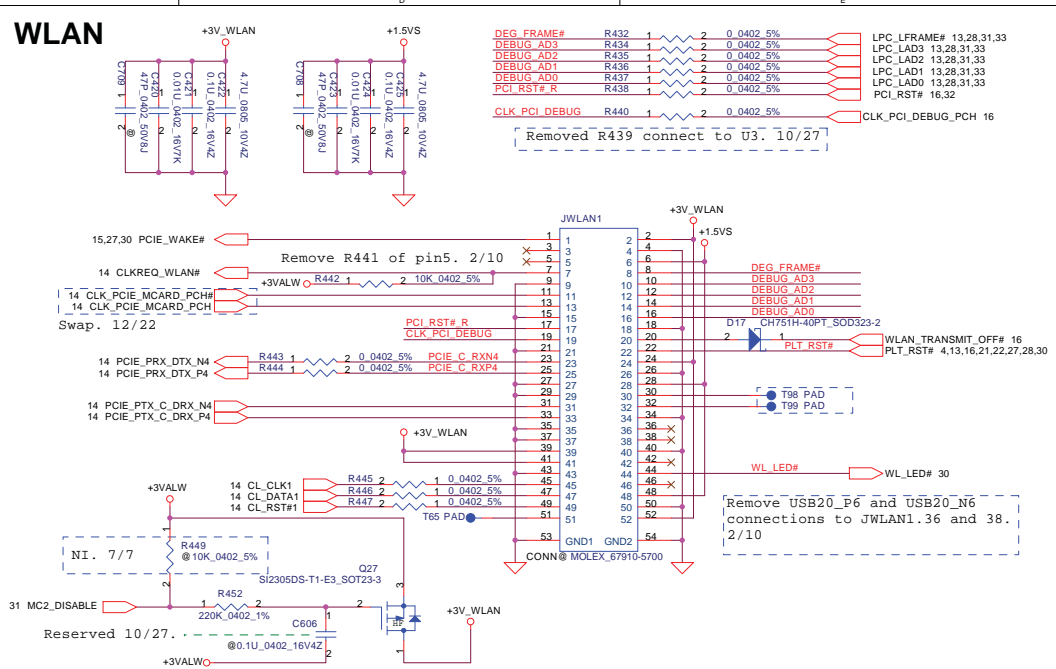
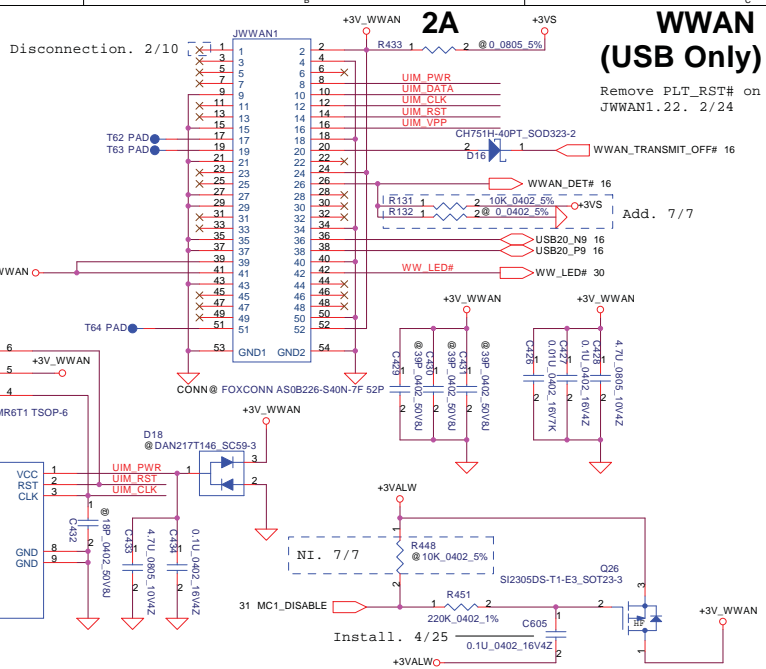
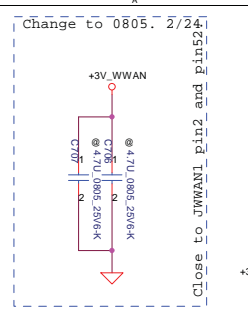
Add on 12/4.

Change R558 PU to +3VM_LAN. 5/11

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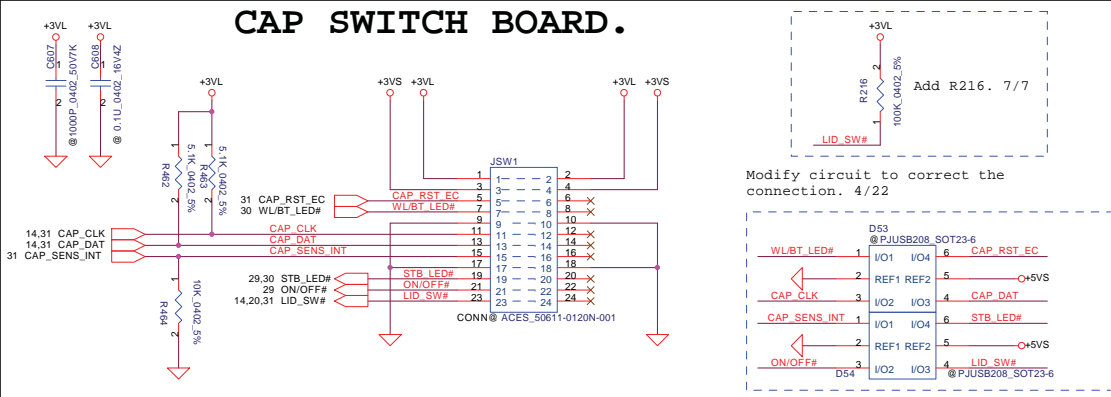


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Size	Document Number	Rev	Date	Sheet
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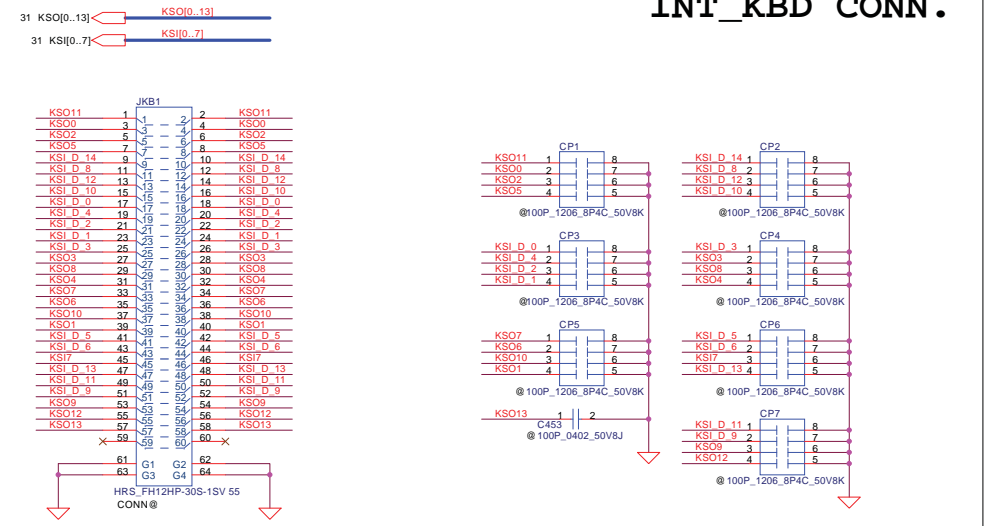


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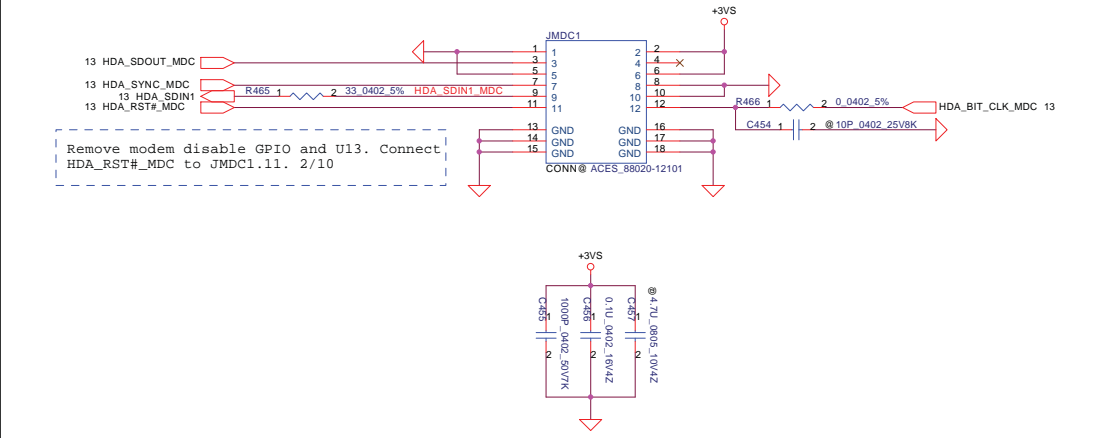
CAP SWITCH BOARD.



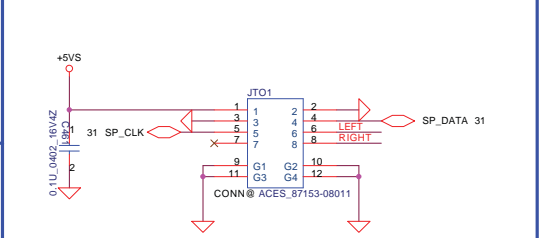
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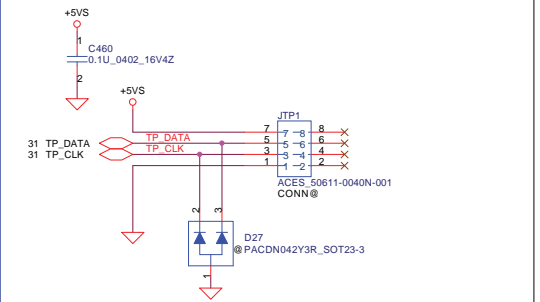
MDC 1.5 Conn.



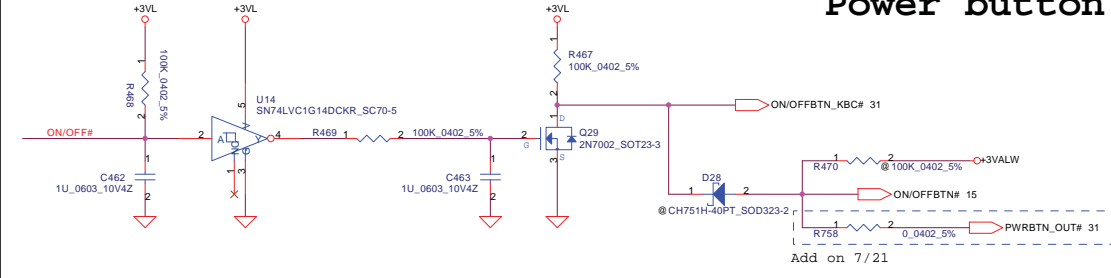
Track Point CONN.



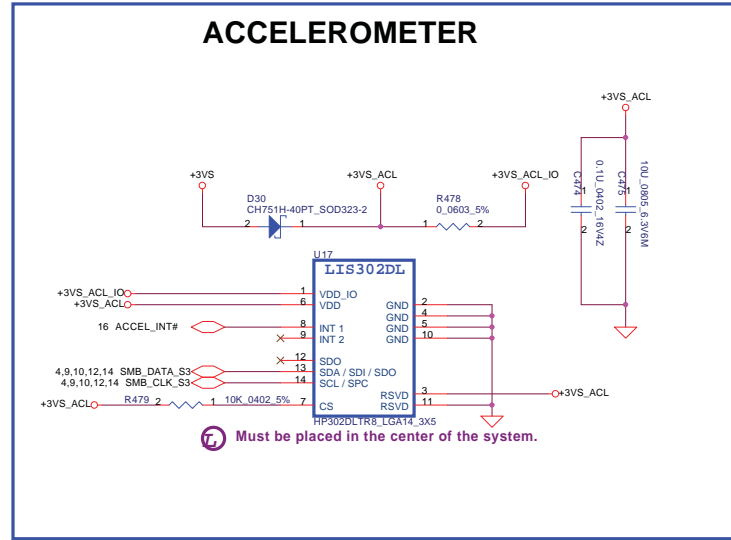
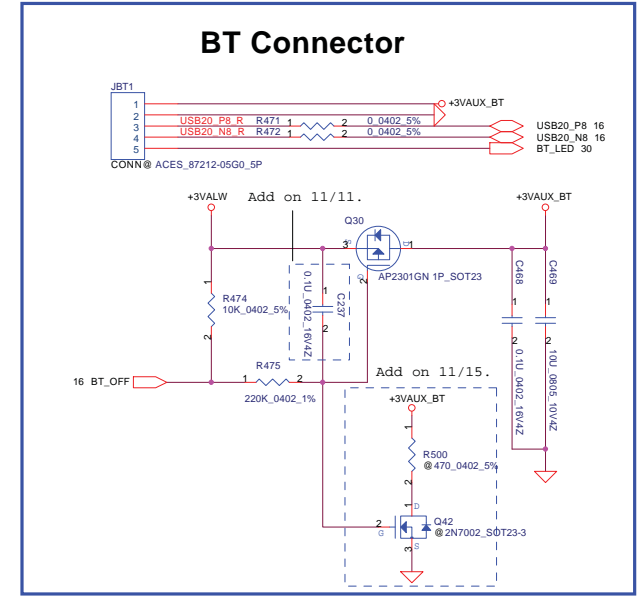
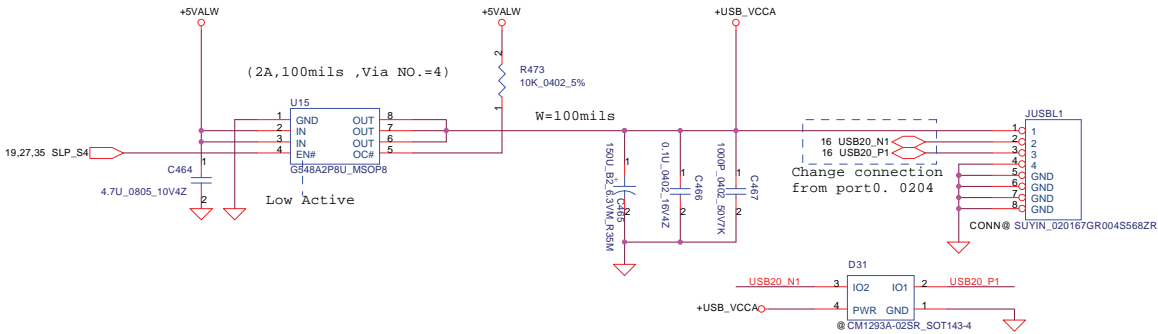
Touch Pad CONN.



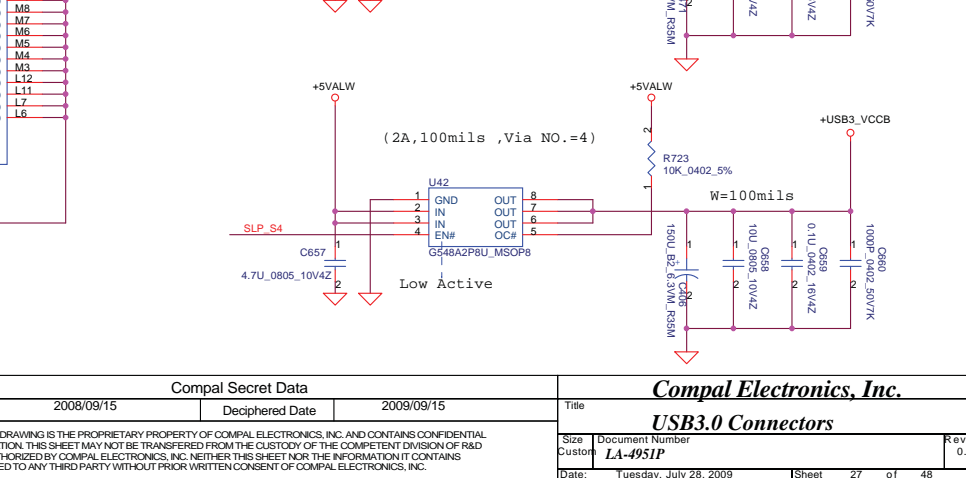
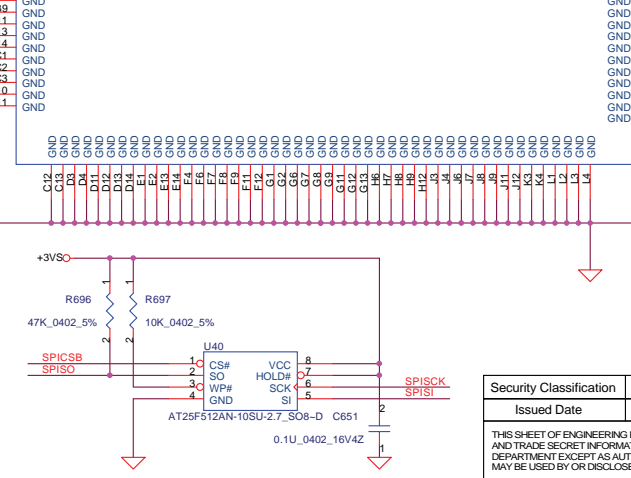
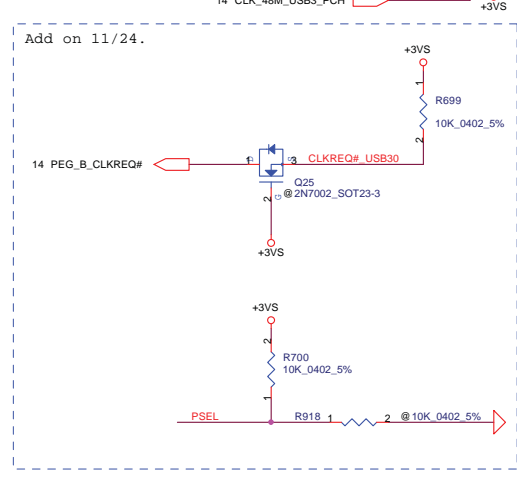
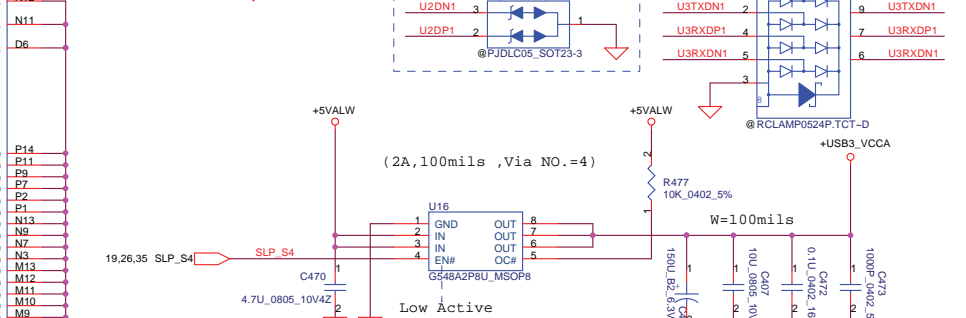
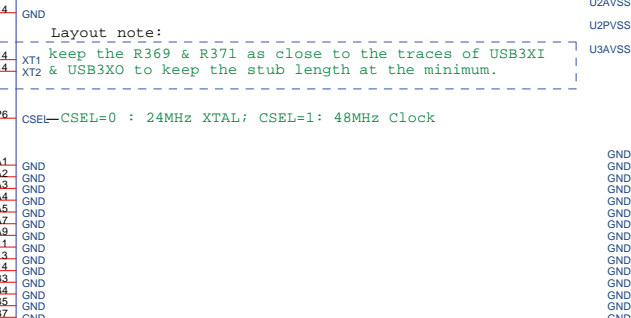
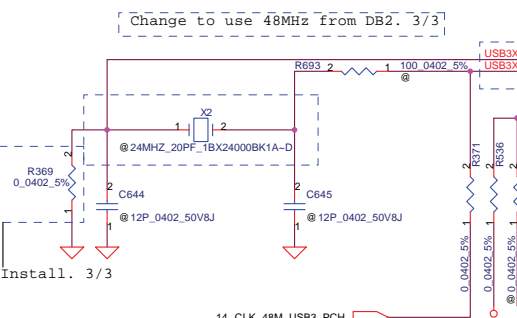
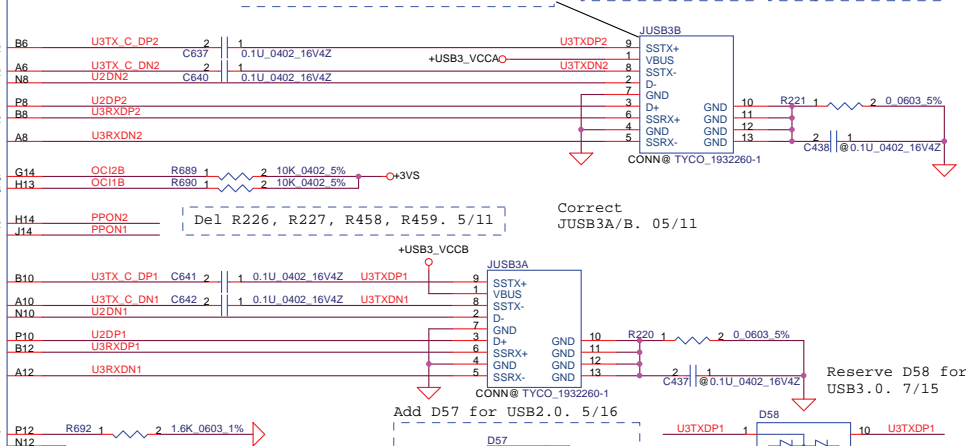
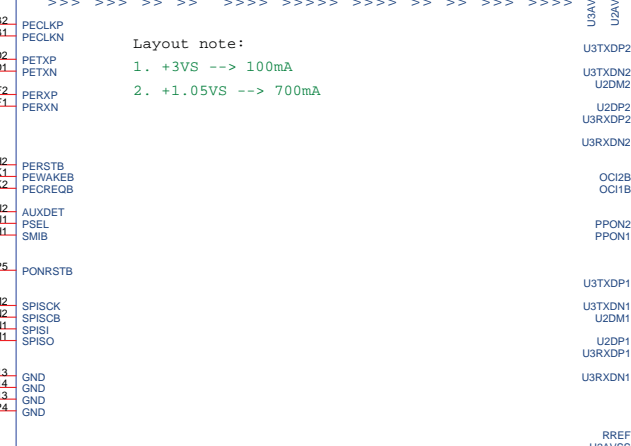
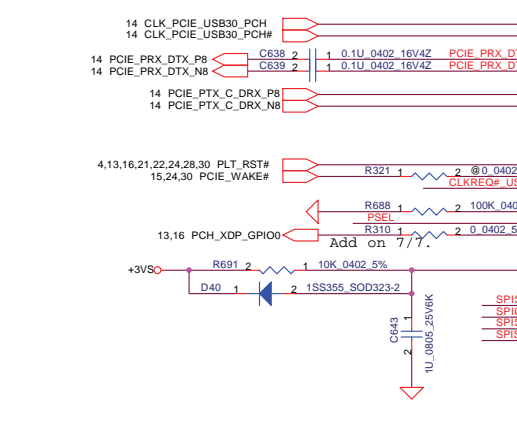
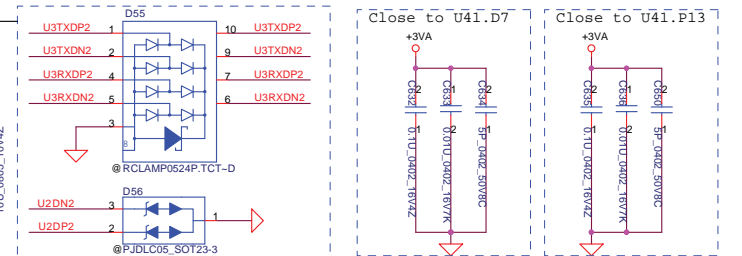
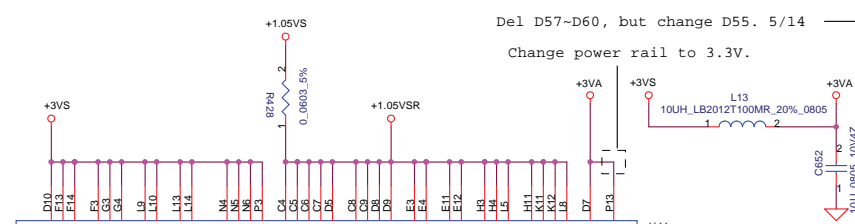
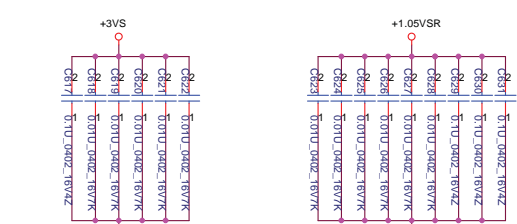
Power button



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Layout note:
 1. +3VS --> 100mA
 2. +1.05VS --> 700mA

Layout note:
 Keep the R369 & R371 as close to the traces of USB3XI
 XT2 & USB3X0 to keep the stub length at the minimum.

Del R226, R227, R458, R459. 5/11

Correct JUSB3A/B. 05/11

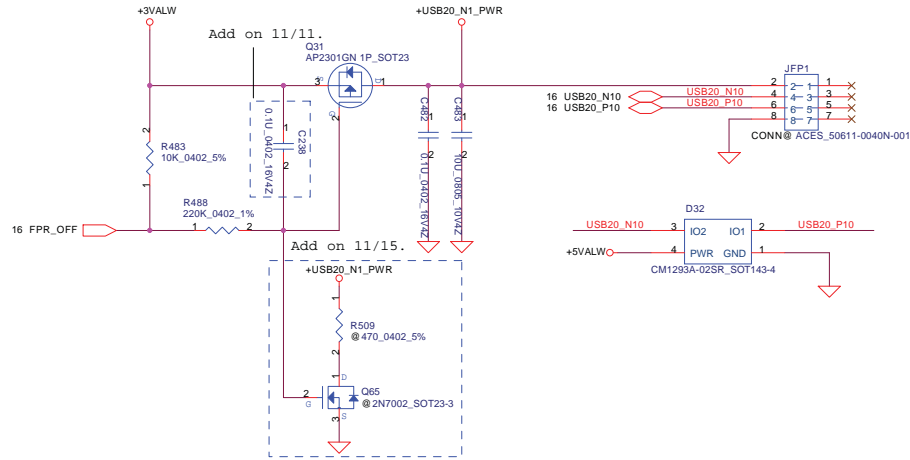
Add D57 for USB2.0. 5/16

Reserve D58 for USB3.0. 7/15

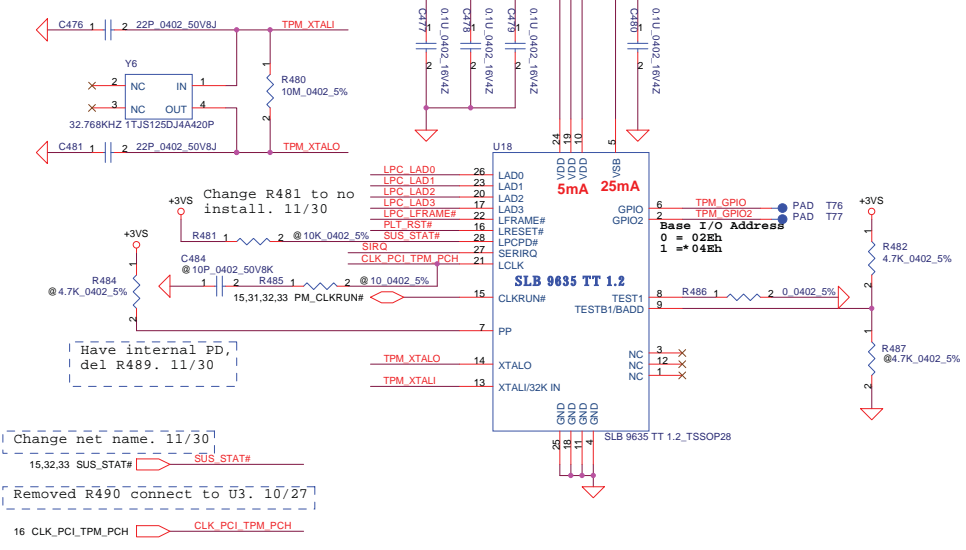
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Issued Date	2008/09/15	Deciphered Date	2009/09/15
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Compal Electronics, Inc.	
USB3.0 Connectors	
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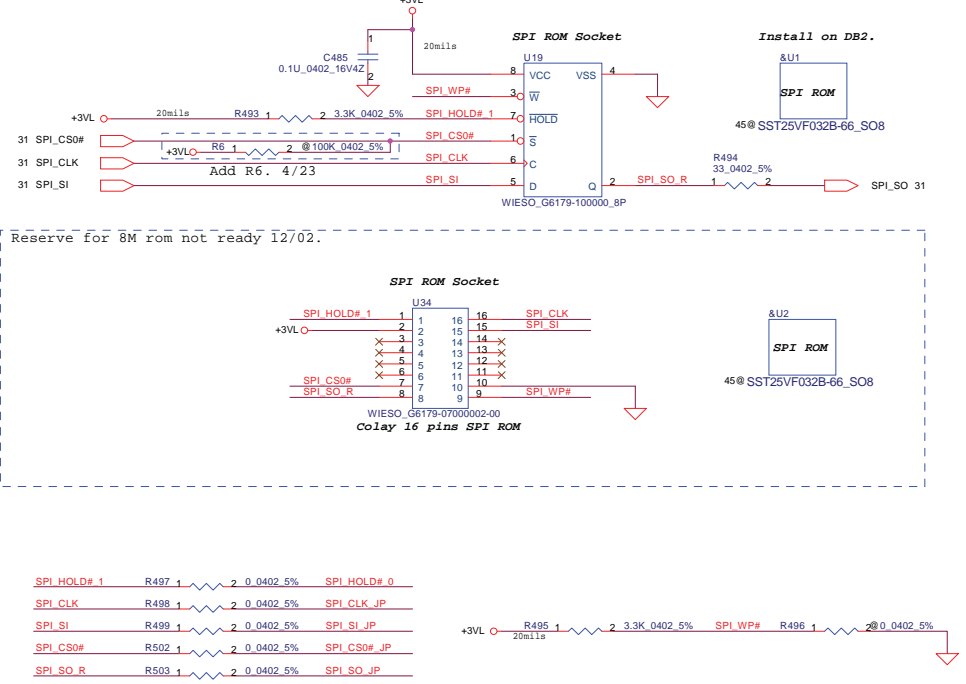
Finger printer



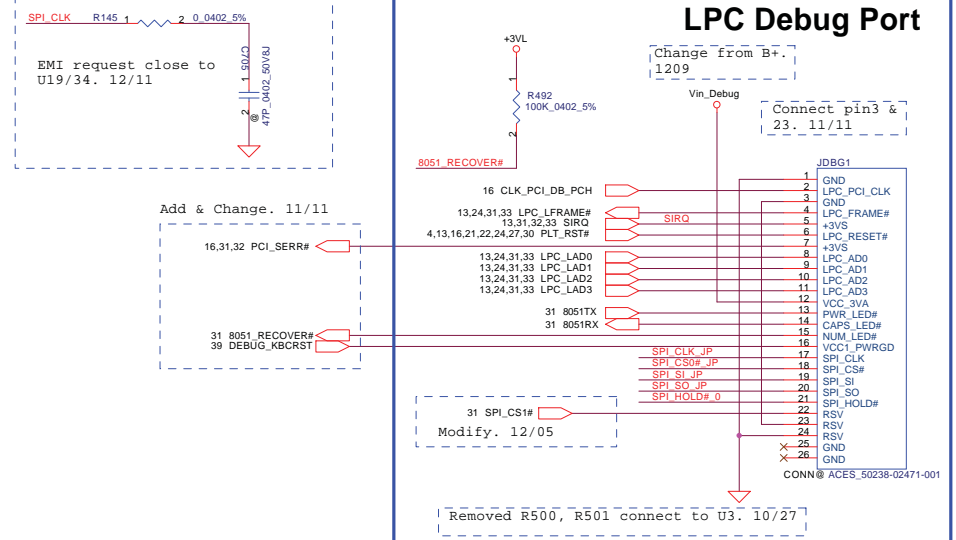
TPM1.2 on board



BIOS ROM(8MB)



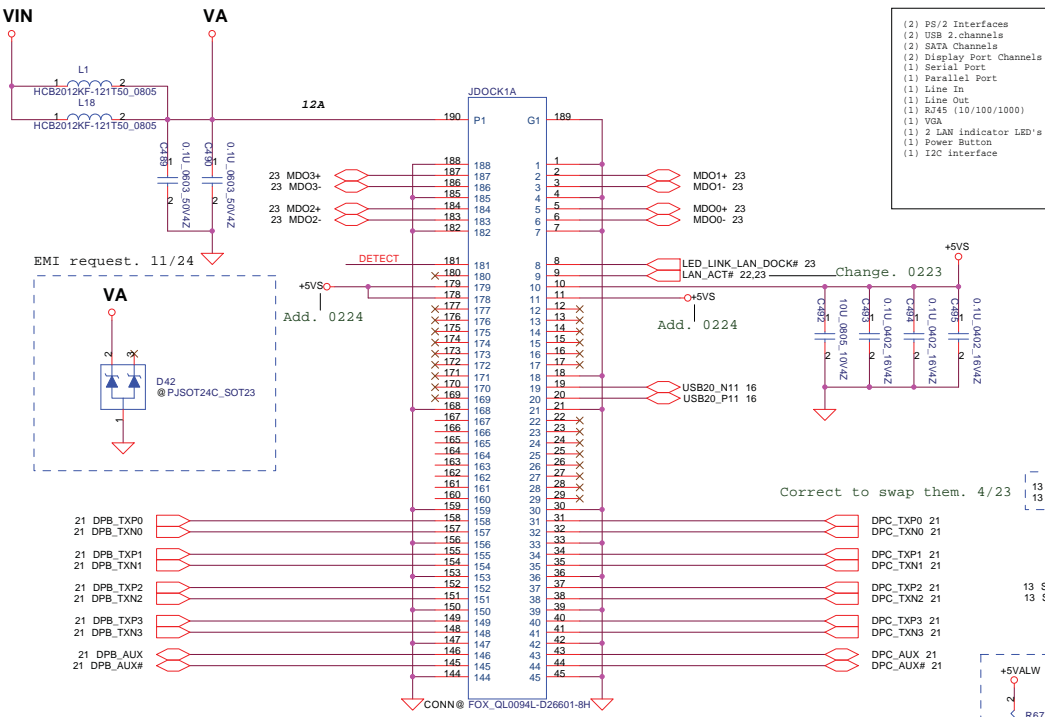
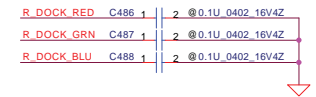
LPC Debug Port



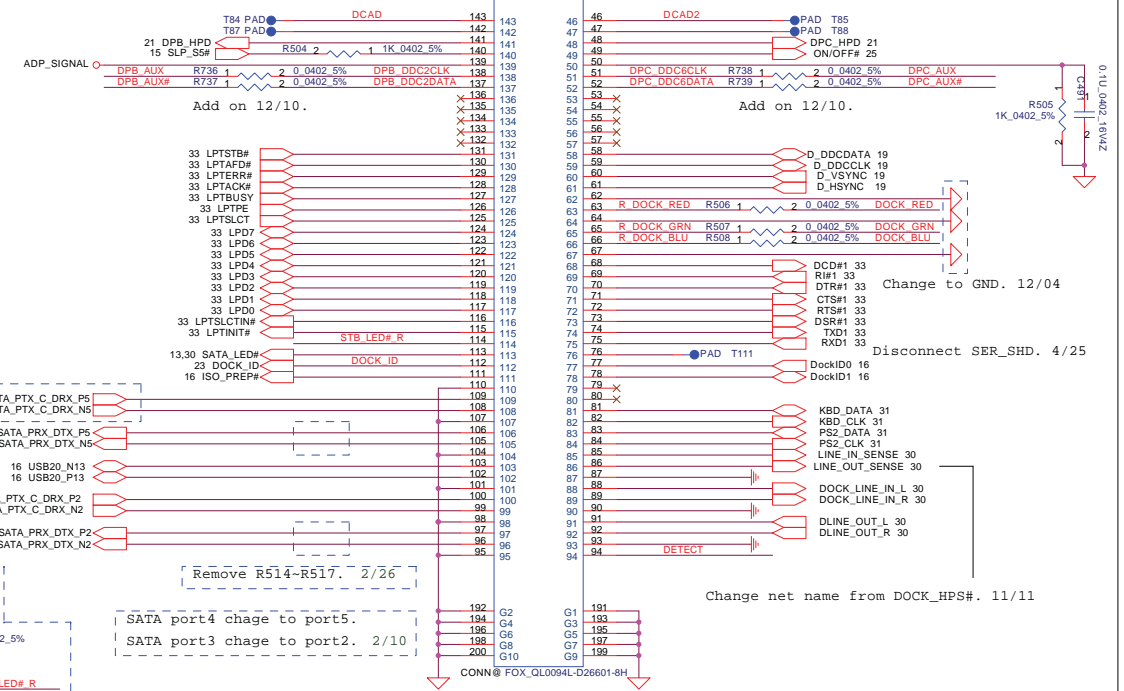
Security Classification	Compal Secret Data		Title TCG/BIOS ROM/PS2/SW LPC DEBUG
Issued Date	2008/09/15	Deciphered Date	
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DOCKING CONNECTOR (190 pins)

Place close to R506 ~ R508. 11/11



- (2) PS/2 Interfaces
- (2) USB 2.channels
- (2) SATA Channels
- (2) Display Port Channels
- (1) Serial Port
- (1) Parallel Port
- (1) Line in
- (1) Line out
- (1) r345 (10/100/1000)
- (1) VGA
- (1) 2 LAN indicator LED's
- (1) Power Button
- (1) I2C interface



Remove C512, C513, C514, C515, R117 & R118, they will place at dock side. 11/30

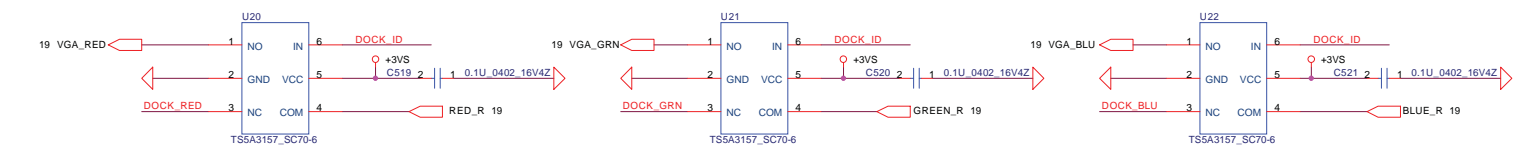
Remove C496 ~ C511, because put them to docking side. 2/17

SATA port4 chage to port5.
SATA port3 chage to port2. 2/10

Change net name from DOCK_HPS#. 11/11

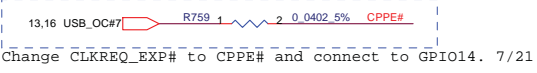
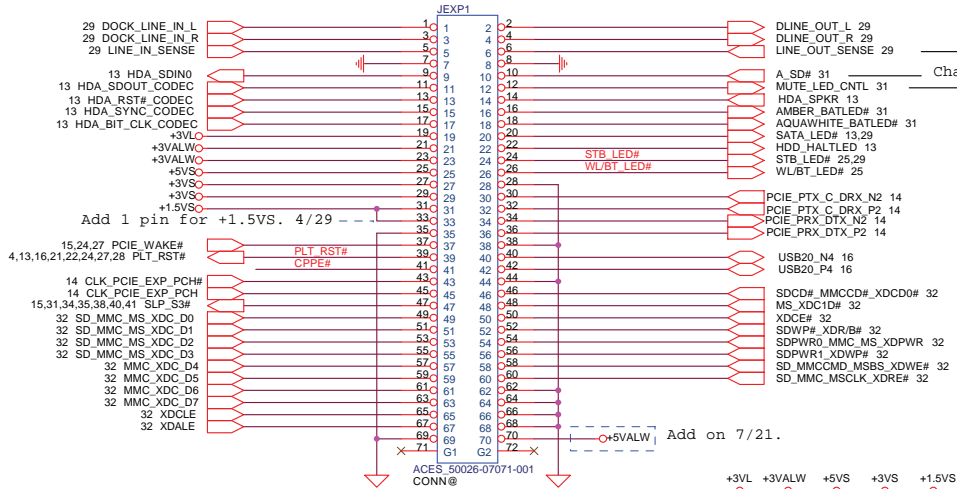
RGB Q-Switch

IN	NC<-->COM	NO<-->COM
L	ON	OFF
H	OFF	ON

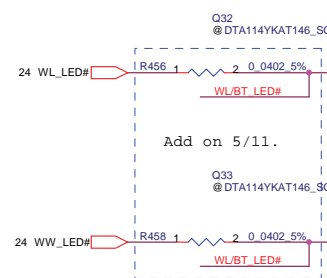
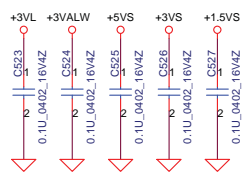
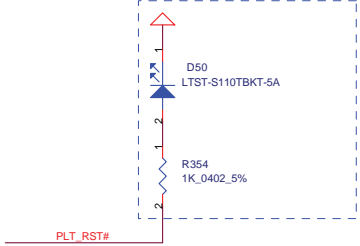


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Audio/Express/LEDs/Card Read Connector



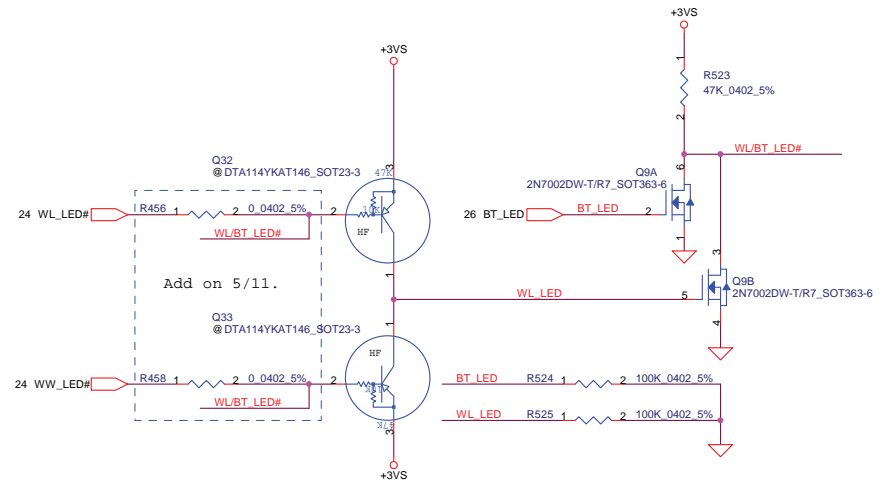
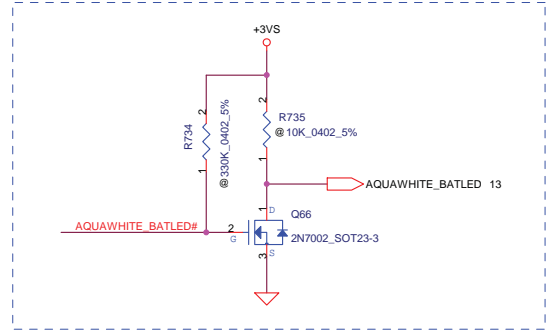
Add for debugging. 3/3



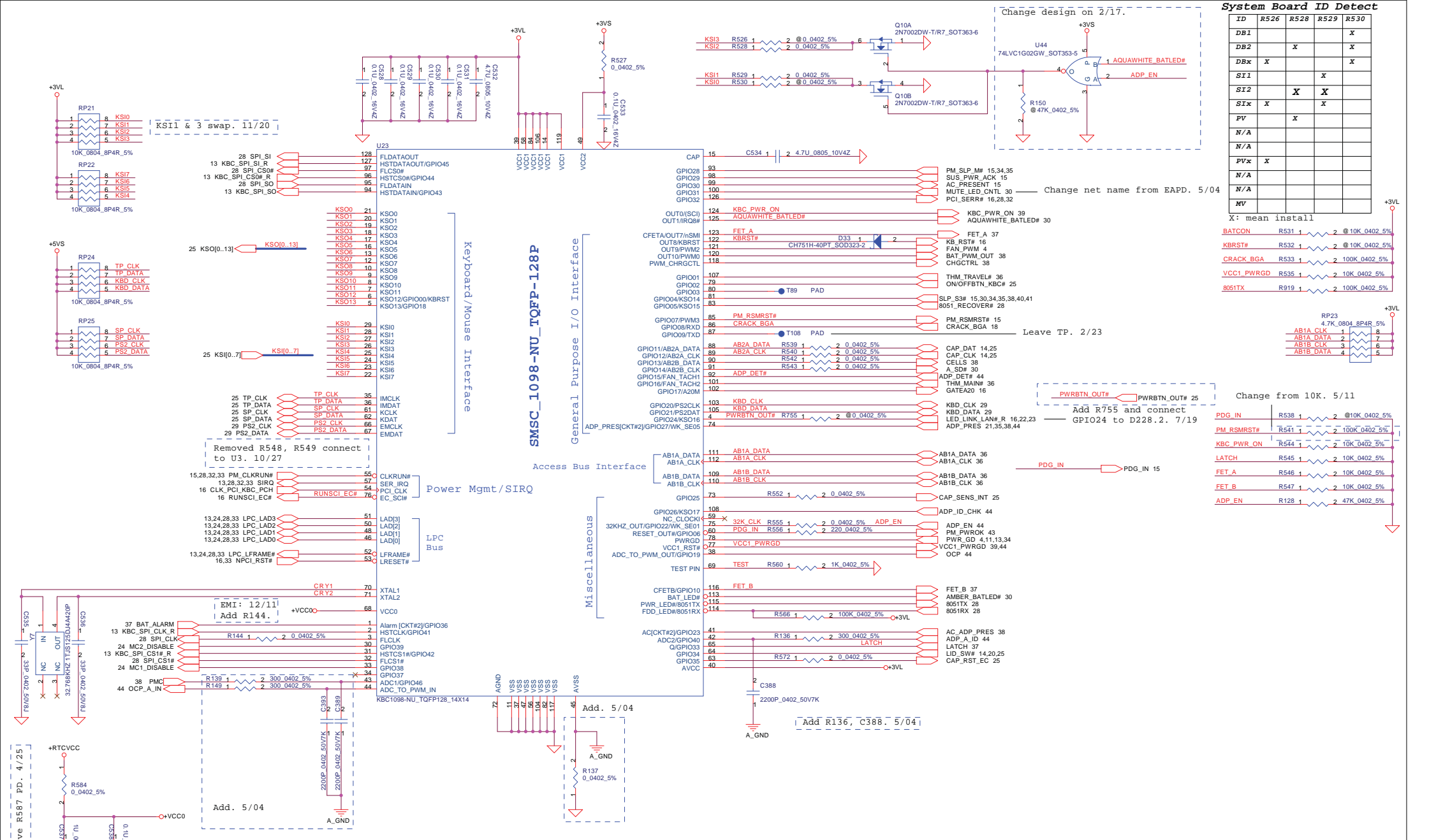
Power Button Connector

Removed Power button JPb1 & C522, combin with JSWITCH1. 11/10

Change R734 & R735 to NI. 02/06



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System Board ID Detect

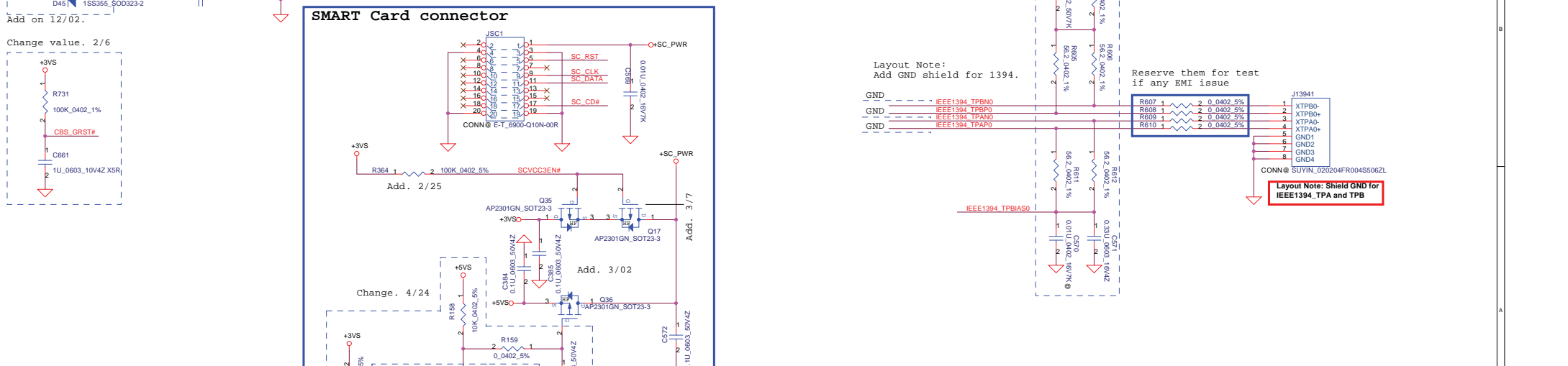
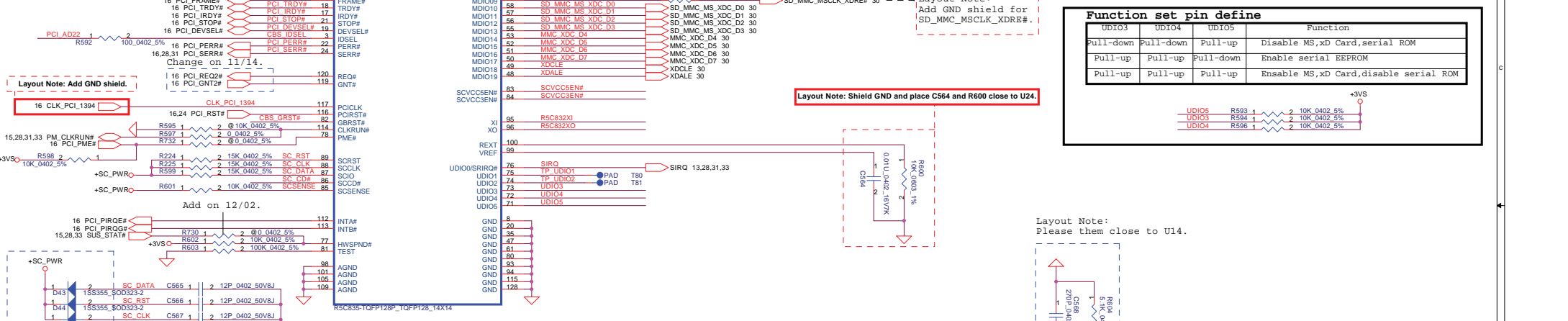
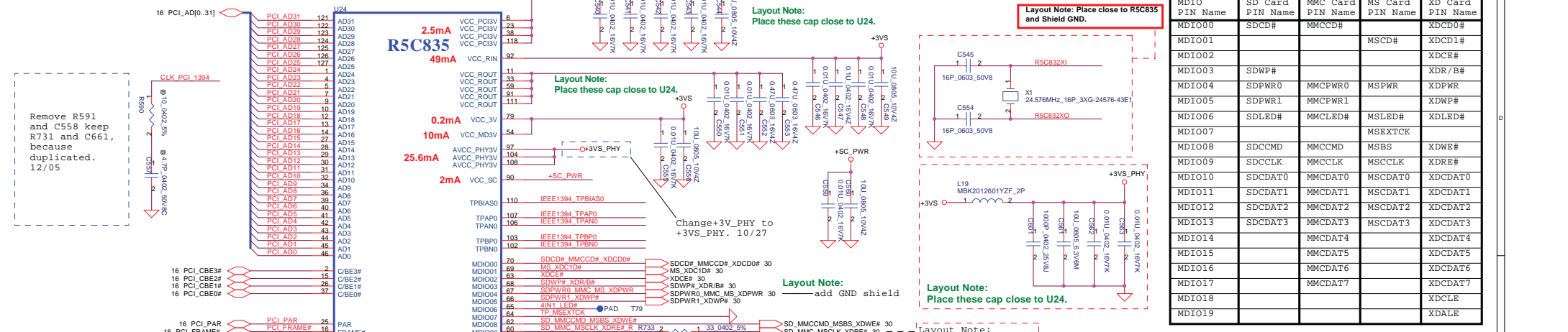
ID	R526	R528	R529	R530
DB1				X
DB2		X		X
DBx	X			X
SI1			X	
SI2		X	X	
Six	X		X	
PV		X		
N/A				
PVx	X			
N/A				
N/A				
MV				

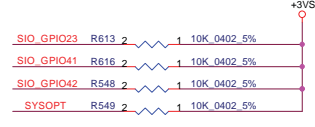
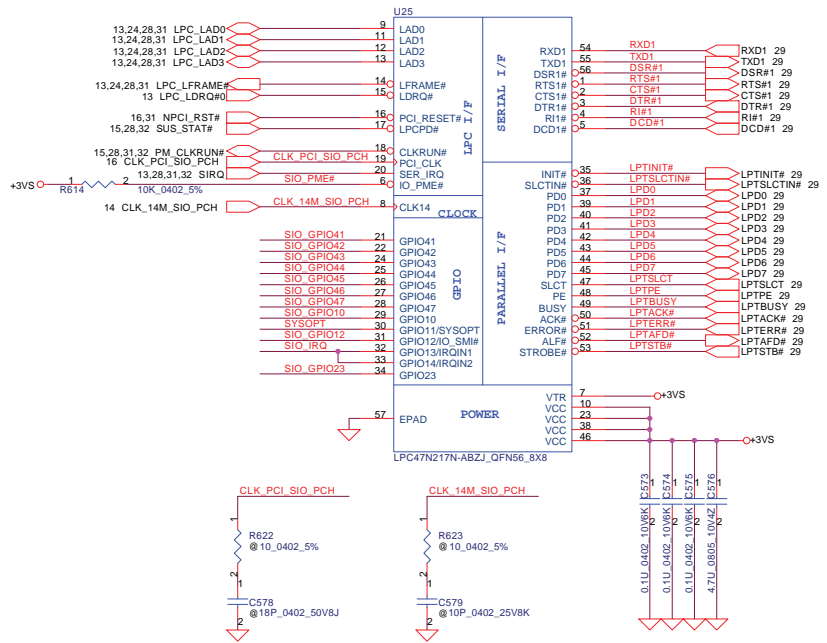
X: mean install

- BATCON R531 1 2 @10K 0.402 5%
- KBRST# R532 1 2 @10K 0.402 5%
- CRACK_BGA R533 1 2 100K 0.402 5%
- VCC1_PWRGD R535 1 2 10K 0.402 5%
- 8051TX R919 1 2 100K 0.402 5%

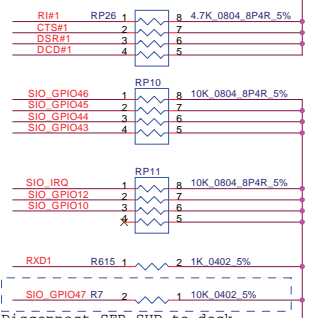
- AB1A_CLK 1 8
 - AB1B_CLK 3 7
 - AB1B_DATA 4 6
 - AB1B_DATA 4 6
- Change from 10K. 5/11
- PDG_IN R538 1 2 @10K 0.402 5%
 - PM_RSMRST# R541 1 2 100K 0.402 5%
 - KBC_PWR_ON R544 1 2 10K 0.402 5%
 - LATCH R545 1 2 10K 0.402 5%
 - FET_A R546 1 2 10K 0.402 5%
 - FET_B R547 1 2 10K 0.402 5%
 - ADP_EN R128 1 2 47K 0.402 5%

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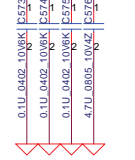
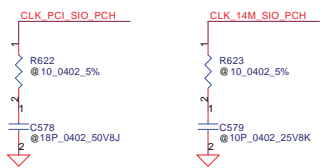
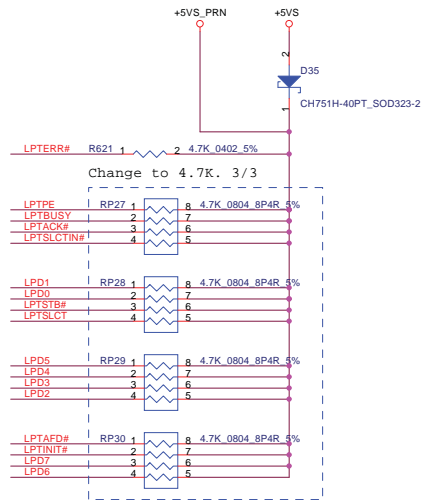




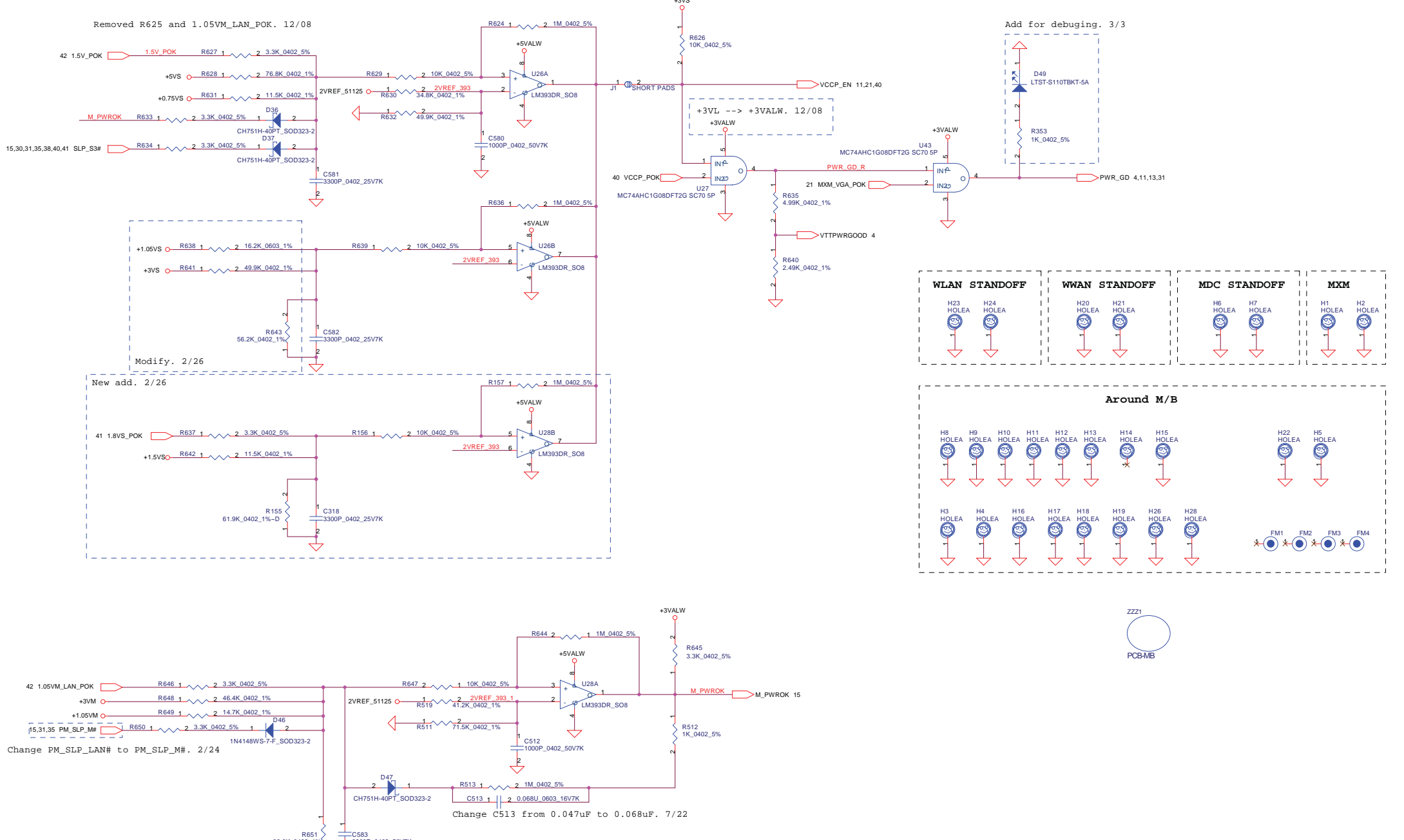
Base I/O Address
 0 = 02Eh
 * 1 = 04Eh



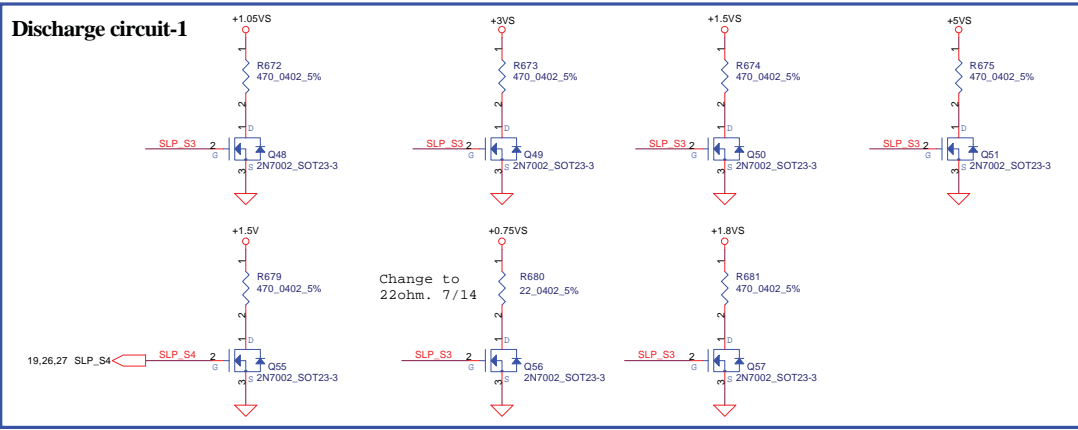
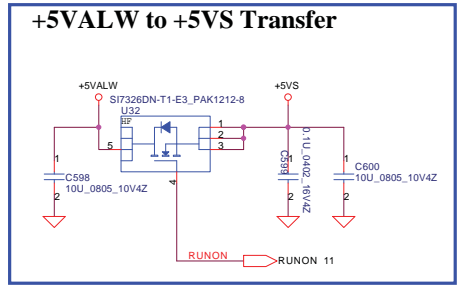
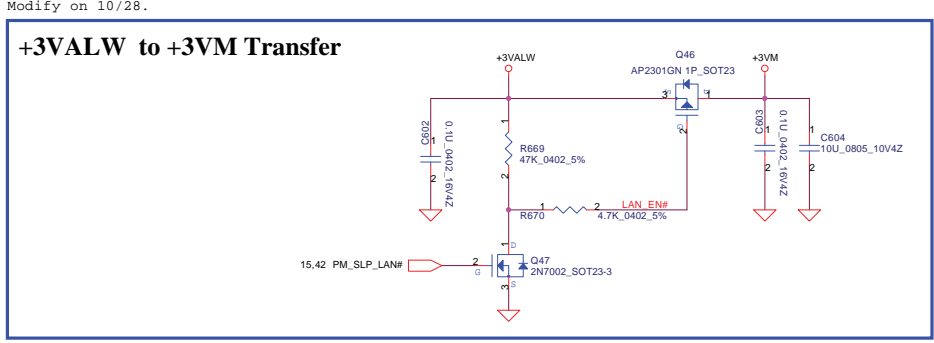
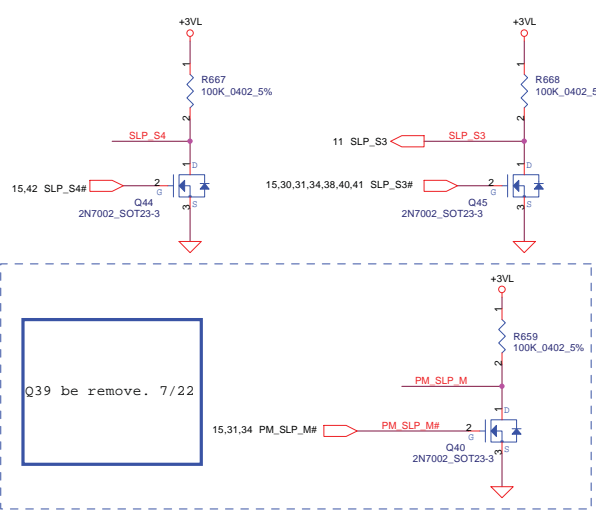
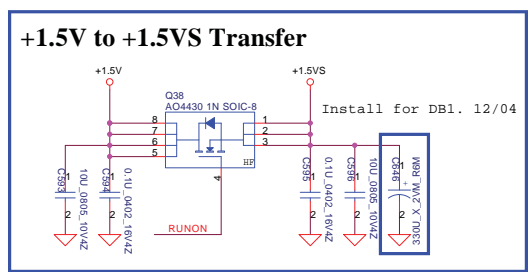
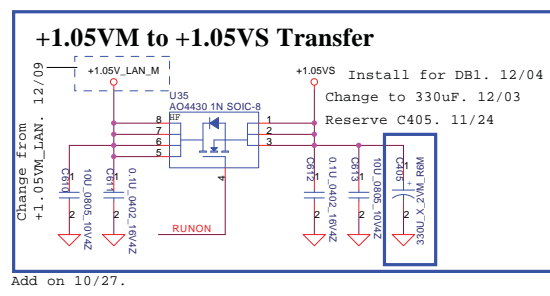
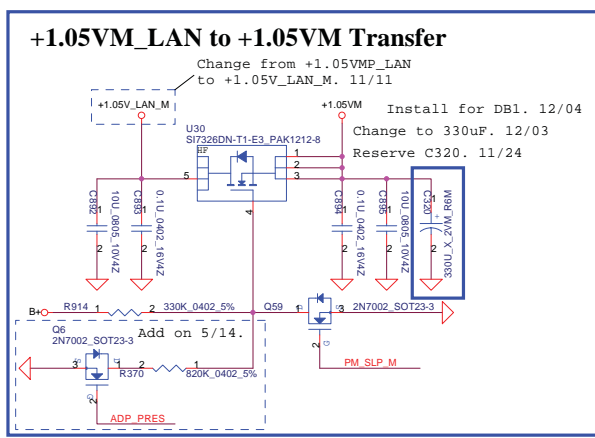
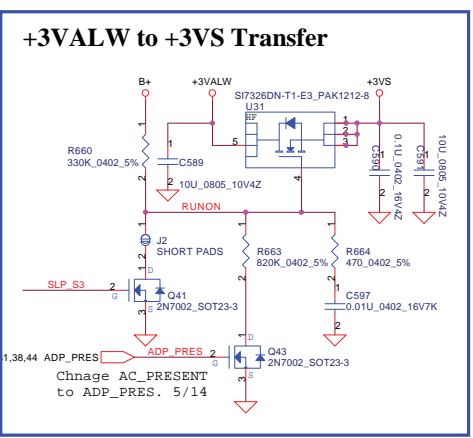
Disconnect SER_SHD to dock,
 but add PD here. 4/25
 Change SER_SHD to SIO_GPIO47. 5/04



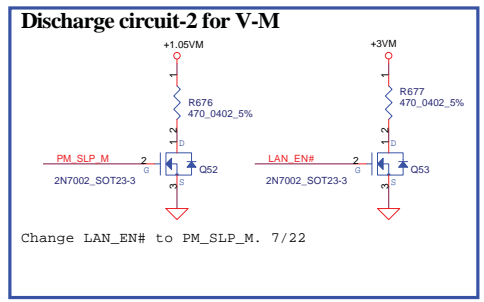
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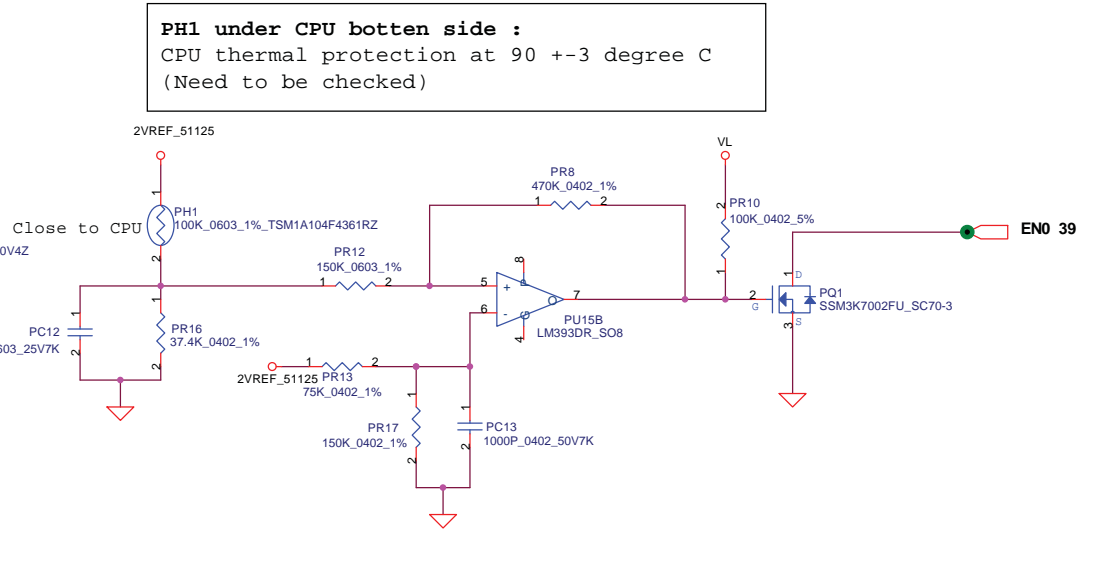
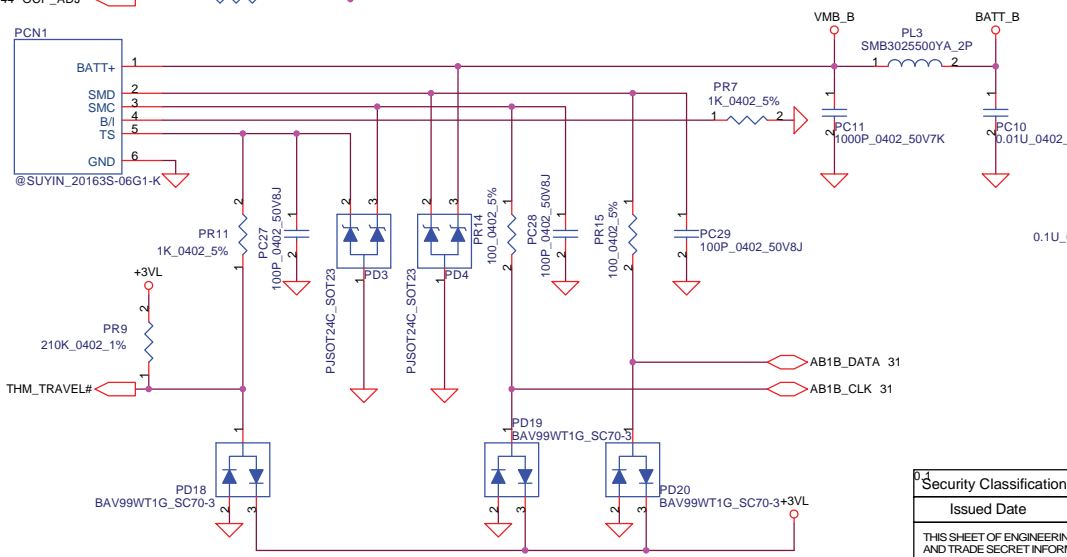
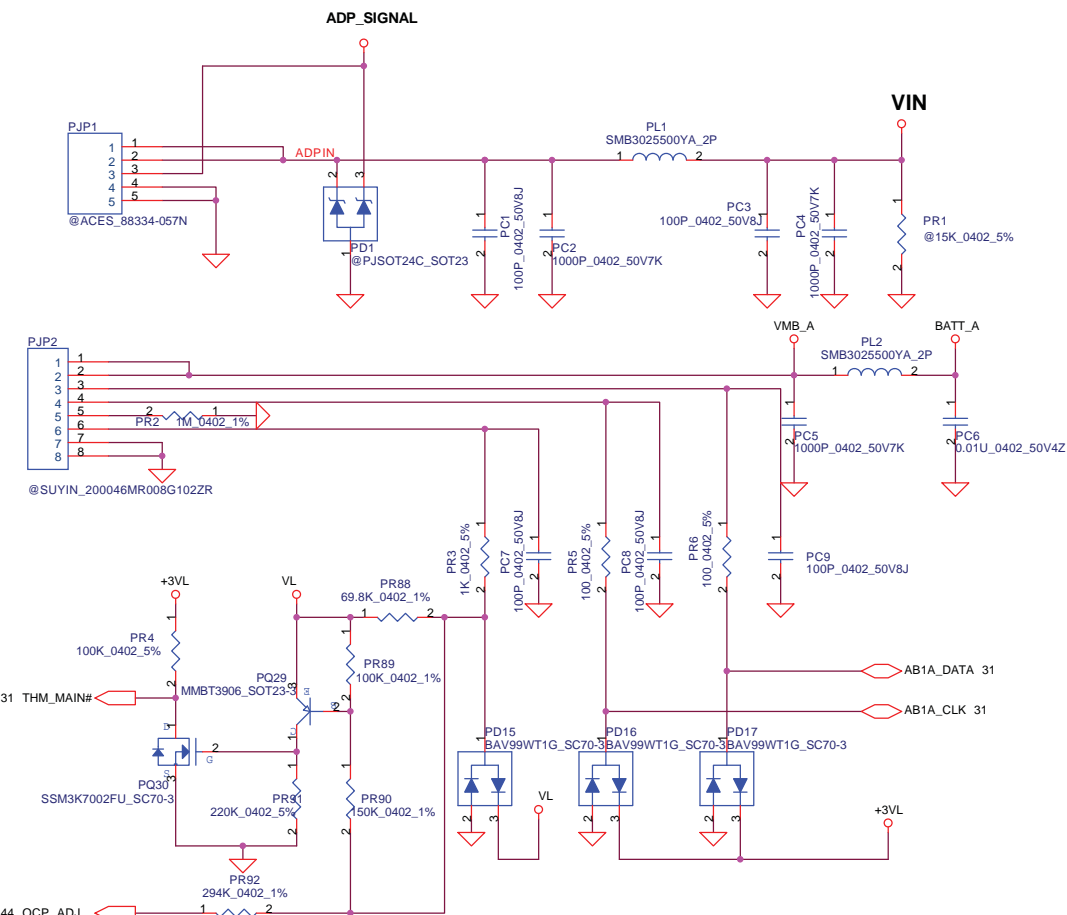


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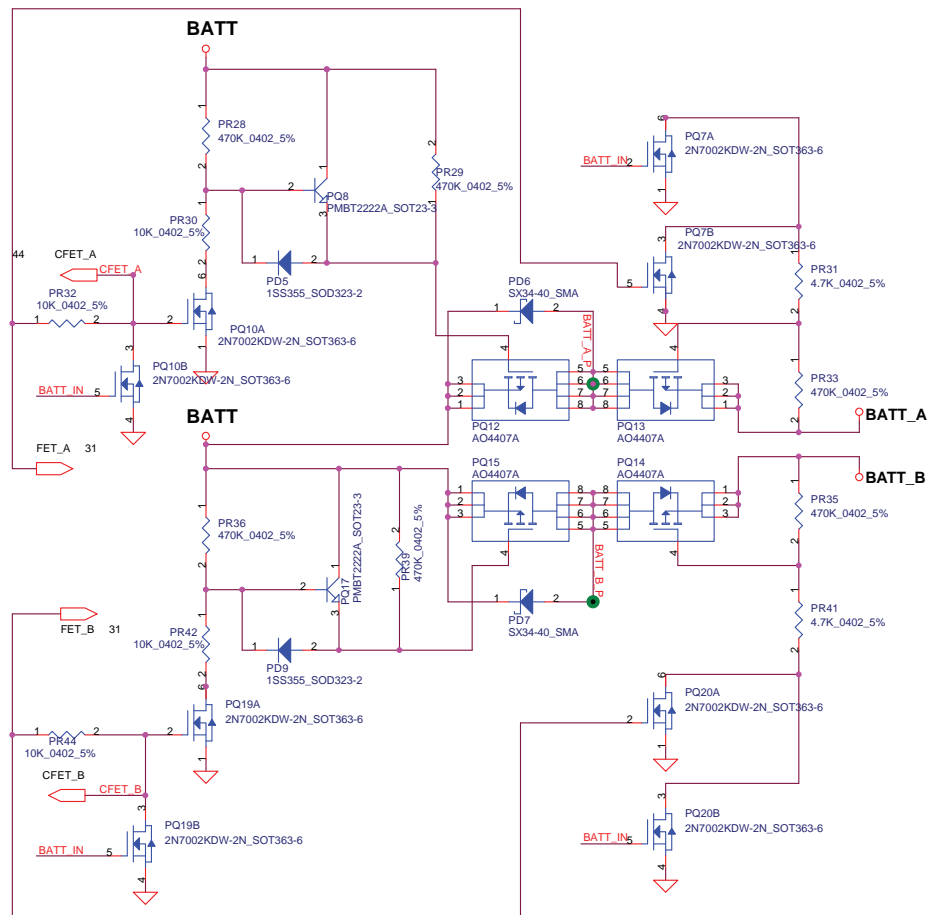
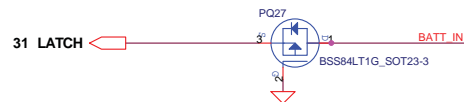
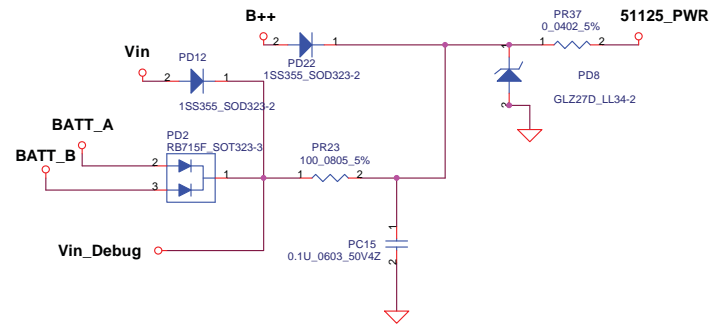
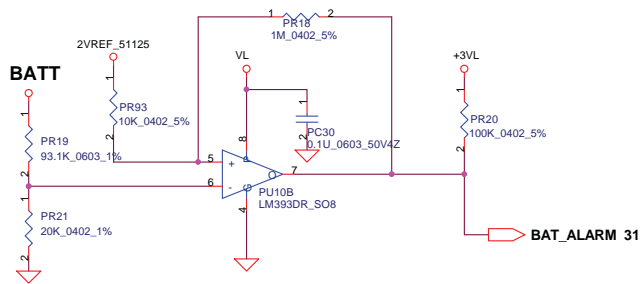


SYS. STATE	PM_SLP_M#	LAN_WOL_EN	+3VM_WOL	+3VM
M-off / No WOL	0	0	0V	0V
M-off / WOL	0	1	3.3V	0V
M1 (ME on)	1	0	3.3V	3.3V
M1 (ME on)	1	1	3.3V	3.3V

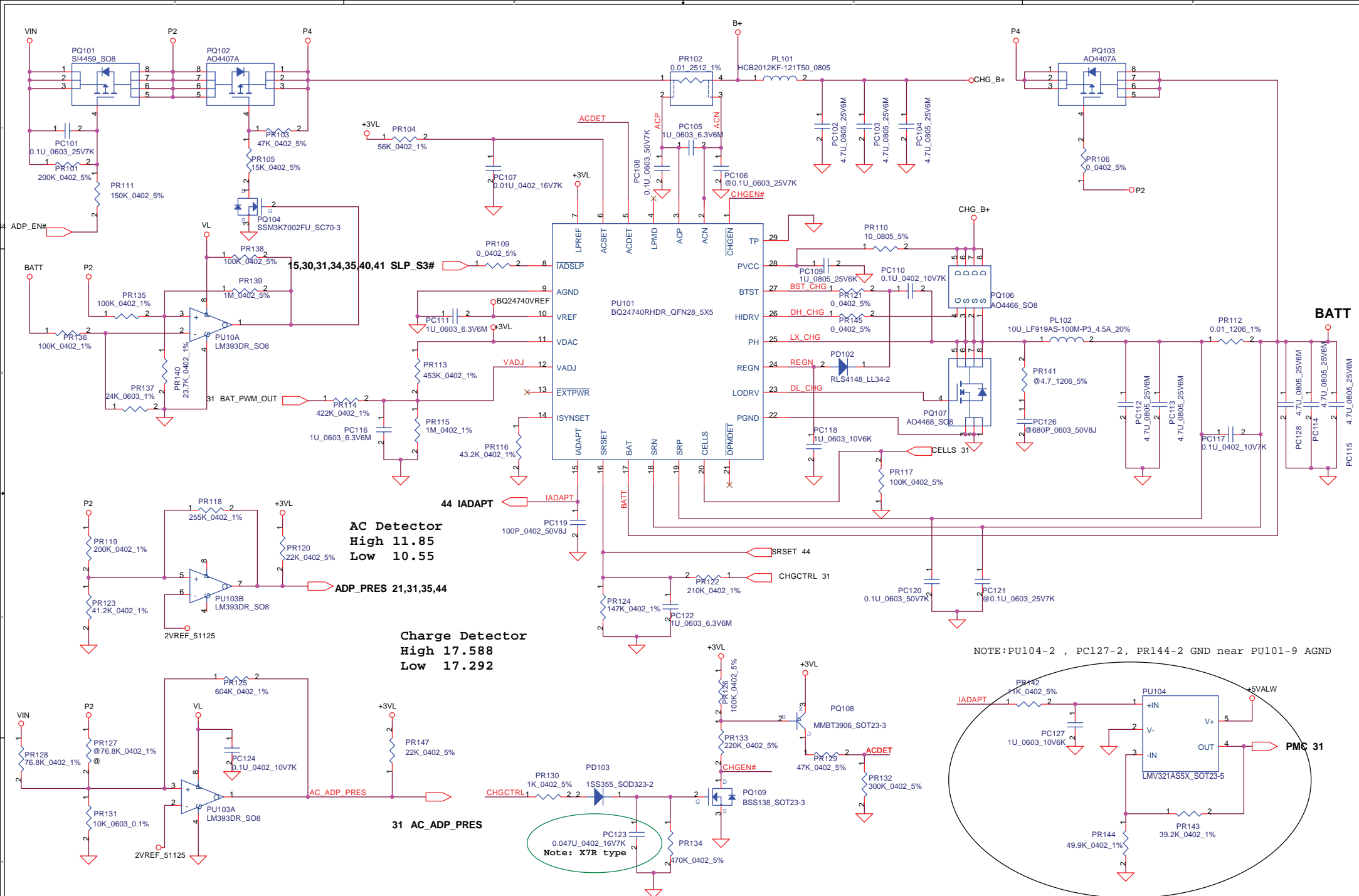




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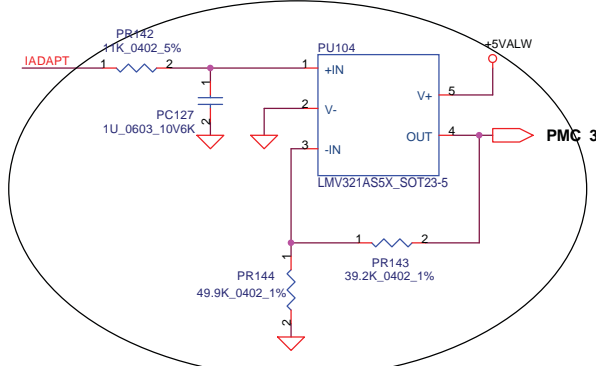


AC Detector
 High 11.85
 Low 10.55

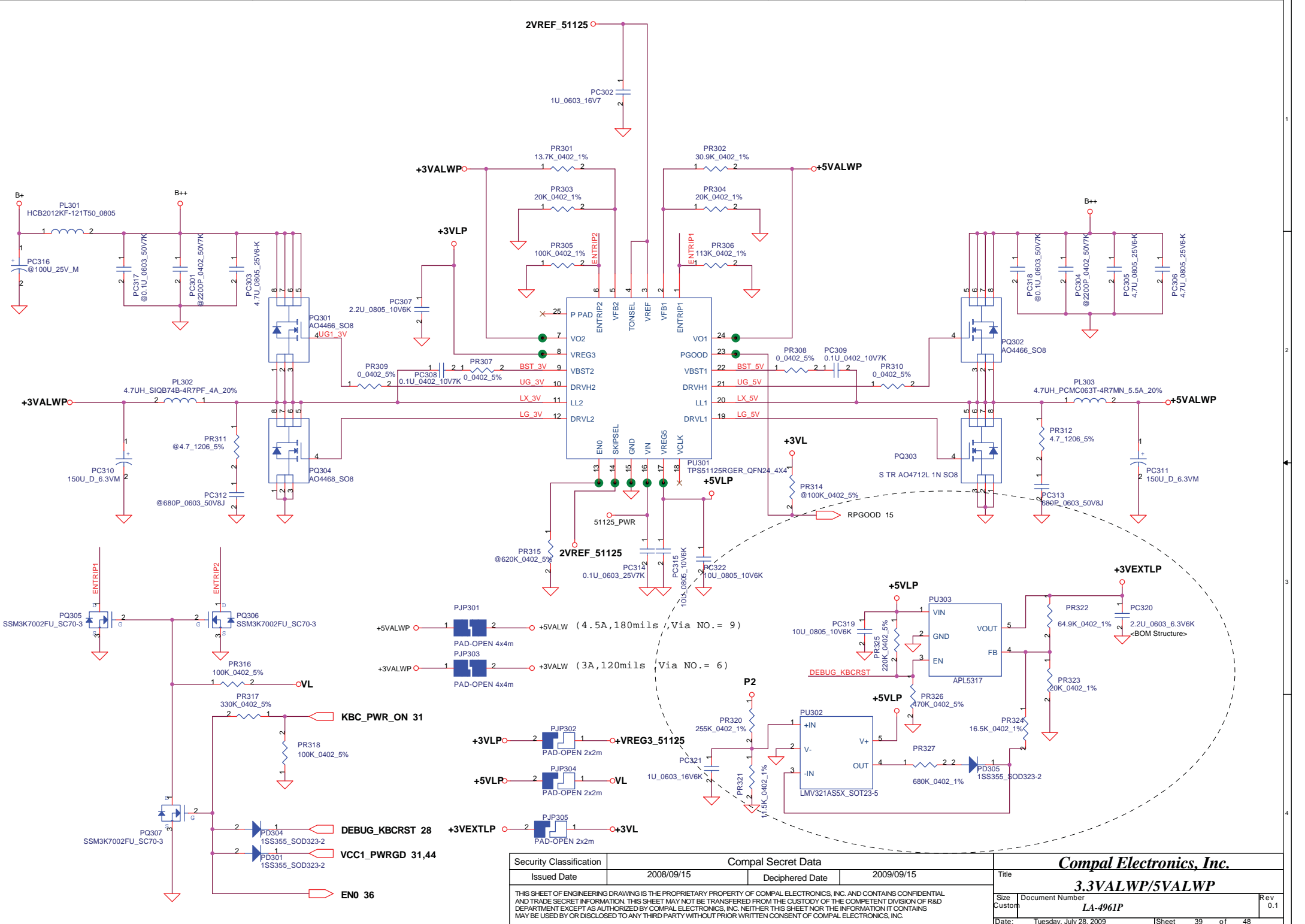
Charge Detector
 High 17.588
 Low 17.292

Note: X7R type

NOTE: PU104-2, PC127-2, PR144-2 GND near PU101-9 AGND

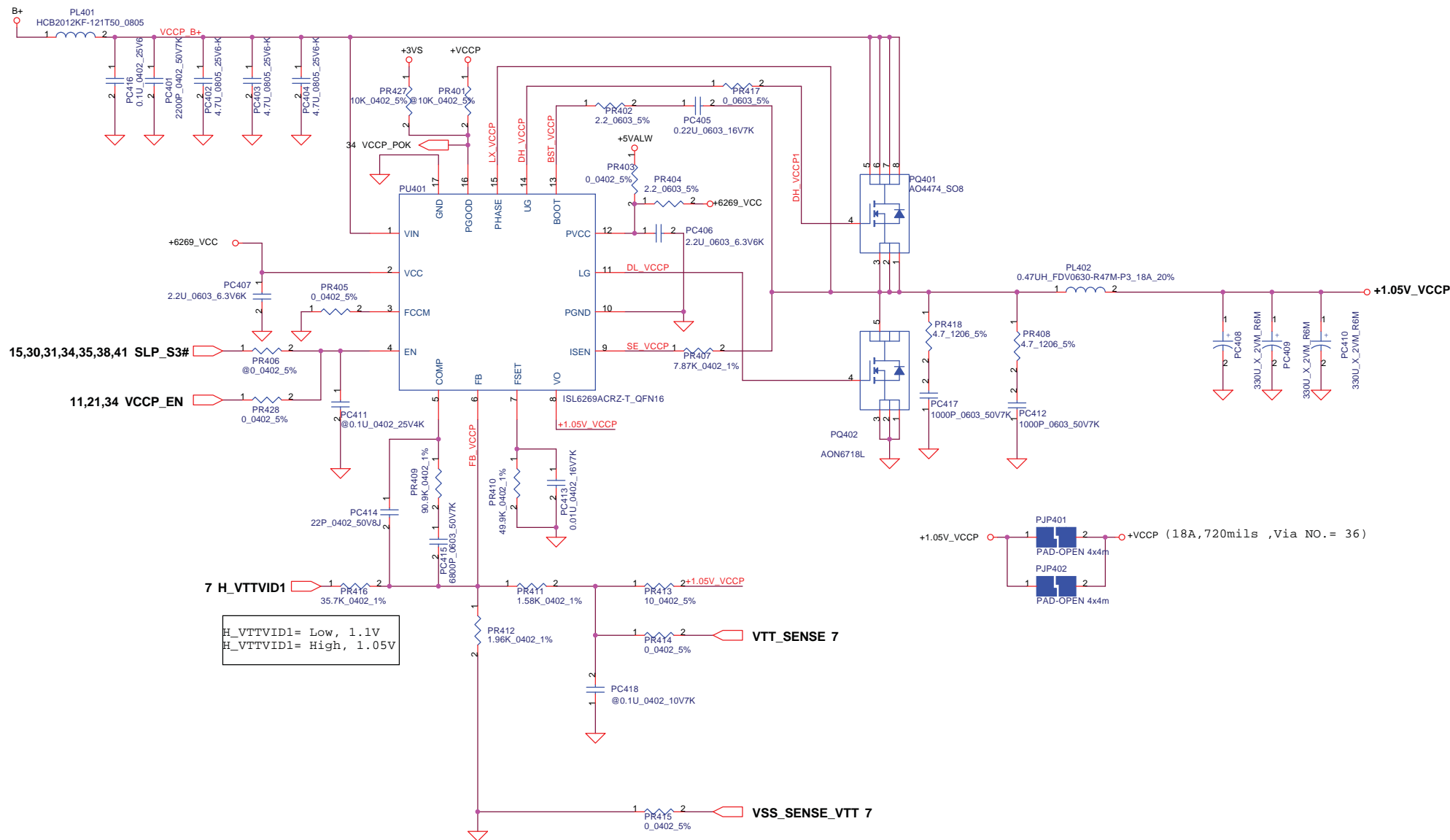


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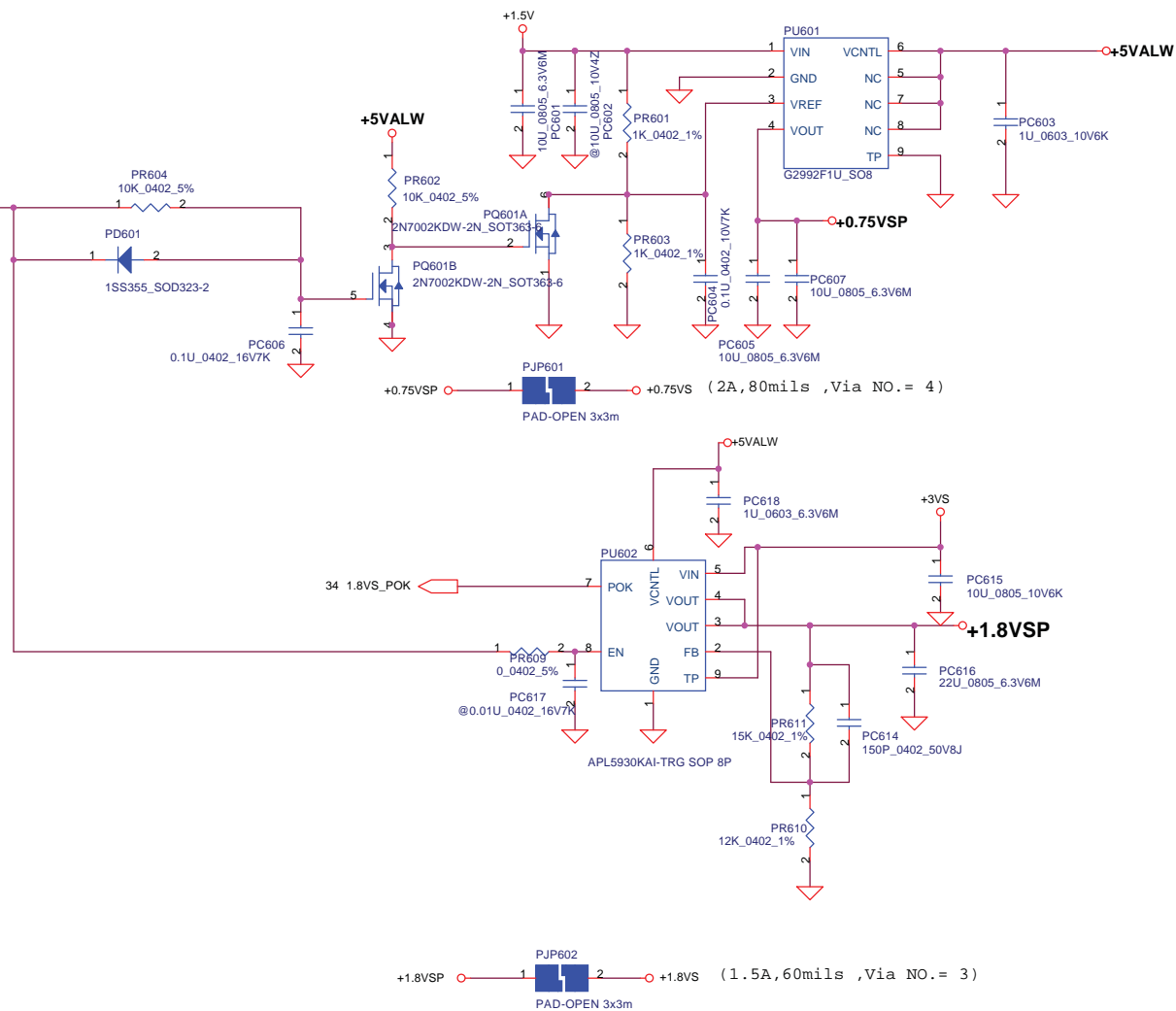
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3.3VALWP/5VALWP			
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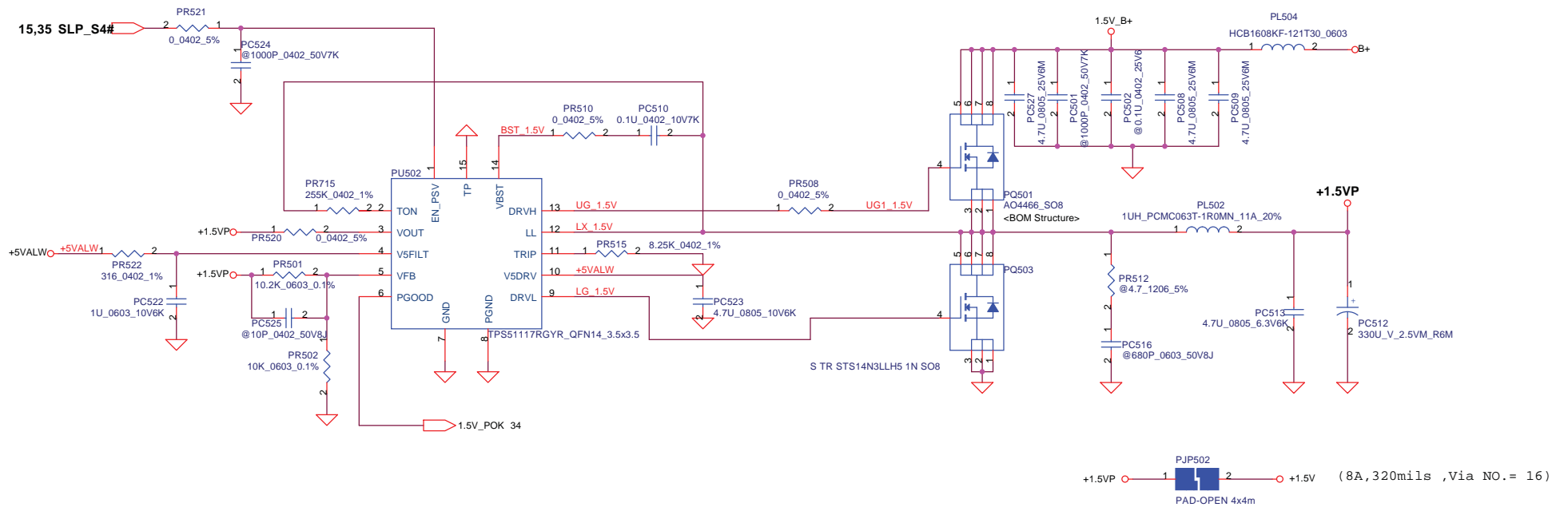
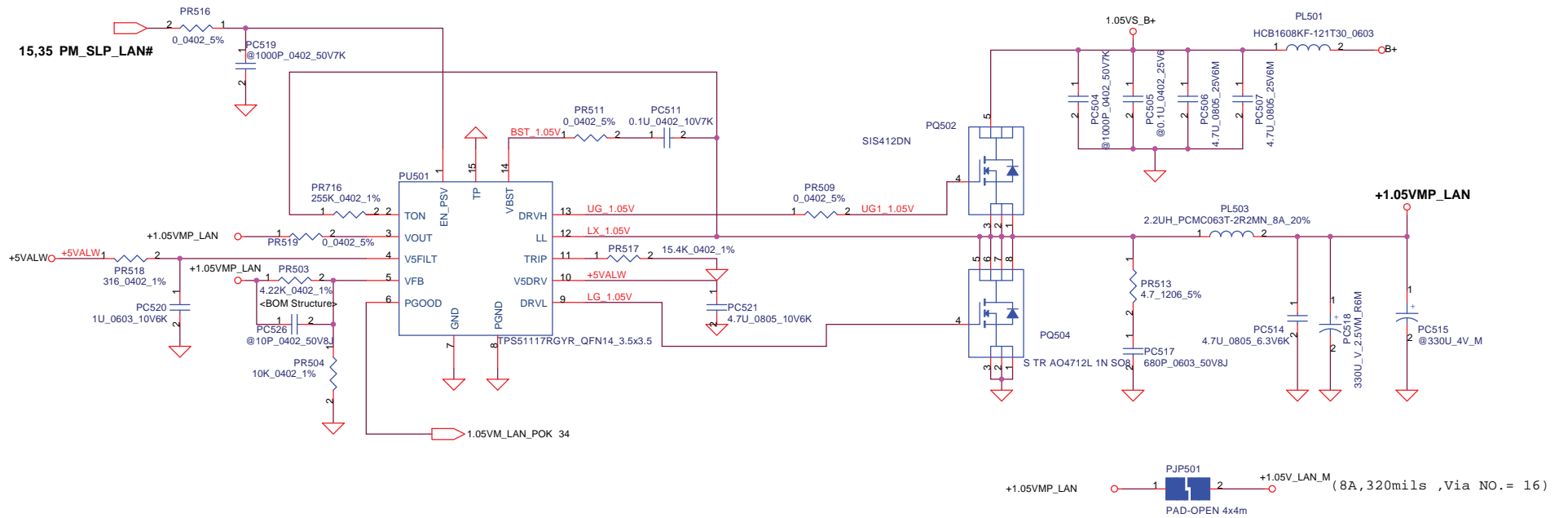


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				LA-4891	
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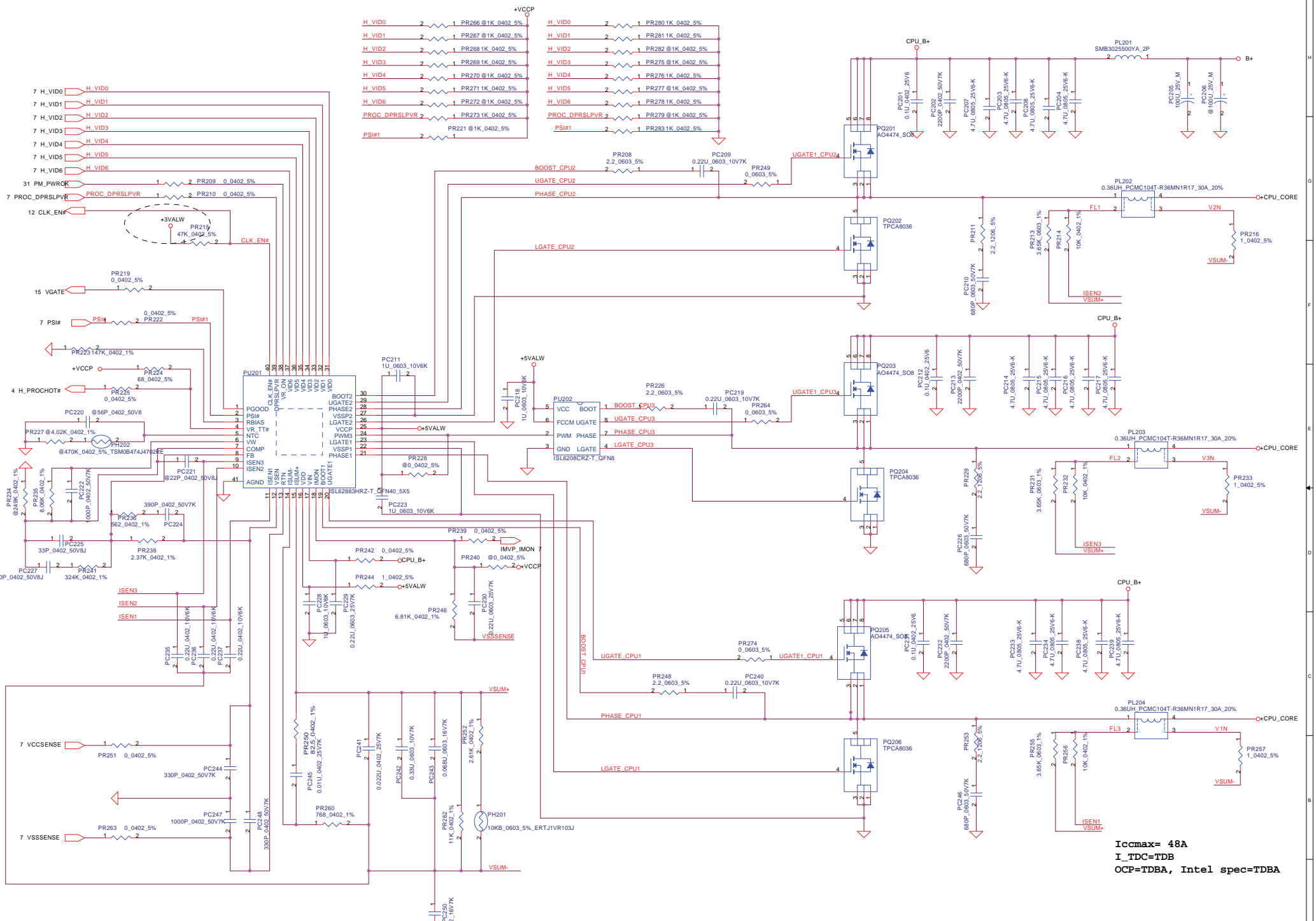
35,38,40 SLP_S3#



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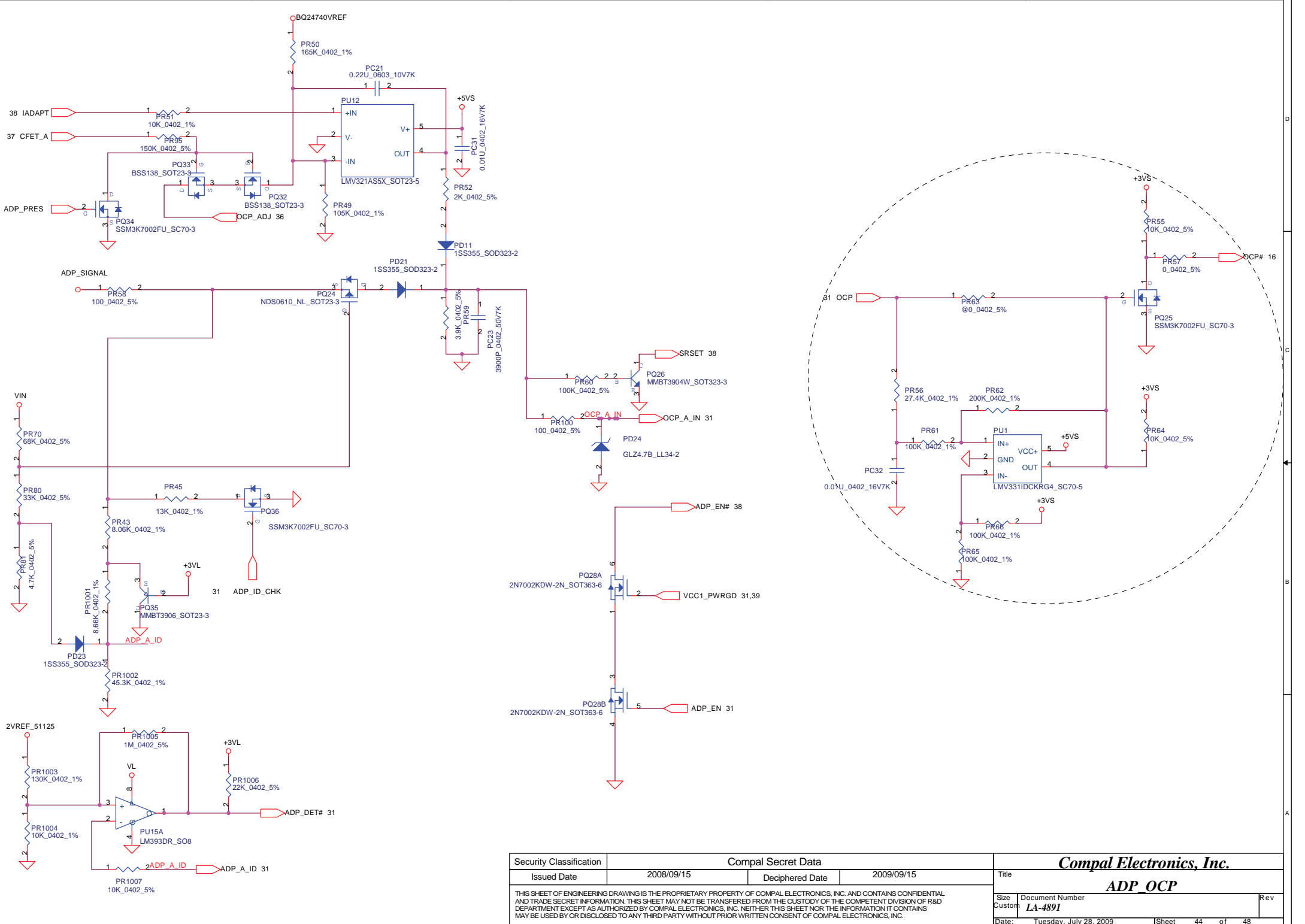


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Iccmax= 48A
I_TDC=TDB
OCF=TDBA, Intel spec=TDBA

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Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					

Version Change List (P. I. R. List) for HW Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	21	MXM PEG Bus	01/19	Compal	Can't detect GPU of MXM board	Need reverse TX & RX bus of PEG.	0.2
2	21	MXM LVDS Bus	01/19	Compal	No display of LVDS panel	Need reverse LVDS low&high bit BUS.	0.2
3	13	RTC	01/19	Compal	RTC no function	Reverse signals of RTC connector.	0.2
4	29	JVGAFFC1	01/20	Compal	JVGAFFC1 pin23&24 was dummy, USB cacn't work	Connect JVGAFFC1 pin23&24 to SLP_S4.	0.2
5	20	DISP_OFF#	02/02	Compal	Use wrong power rail for this signal.	Currently panel spec is +3VS.	0.2
6	20	Left USB port	02/02	Compal	It's wrong port for debug	Change connection from port0 to port1 for debug.	0.2
7	21	PWR_LEVEL	02/04	Compal	Need isolation circit per HP request.	Add Q69, Q70, R397, R388, R118.	0.2
8	4	CPU FAN CONN	02/06	Compal	No GND pin of FAN connector.	Change Connector to 4 pin with GND pin.	0.2
9	4,13,24	SM BUS	02/06	HP	HP request to remove SM bus to XDP, JTAG & WLAN	Leave TP and remove signals.	0.2
10	22	Intel LAN	02/06	HP	Intel change design to remove some caps.	Remove these caps as Intel CRB design.	0.2
11	11	DDR M2 support	02/08	Compal	Data & CLK signals are reverse of U36.	Reverse CLK & DATA.	0.2
12	30	LED CTL circuit	02/06	HP	HP request to update LED control circuit.	No install R734 & R735.	0.2
13	15	Duplicate	02/06	HP	Remove R247 because of R541existing.	Remove R247.	0.2
14	13	PCH_JTAG_RST#	02/06	HP	Change R720 to NO INSTALL.	No install R720.	0.2
15	13	GPIO	02/06	HP	Change GPIO43_R to USB_OC#4 & reserve 33 ohm serial.	Add R134 but no install.	0.2
16	13	LED control	02/06	HP	Remove GND & change connection of R176.	Change R176 to 1K with install it.	0.2
17	14	CLKREQ_EXP#	02/06	HP	Change R687 PU for CLKREQ_EXP# to INSTALL.	Install R687.	0.2
18	17	PCH Power Rail	02/06	HP	Some power rail of PCH are no use.	Remove these power and add TP.	0.2
19	32	Card Reader	02/06	HP	It will need find tune value of R731 & C661.	Change R731 to 100K & C661 to 1uF X5R as Cartier first.	0.2
20	9	Debug port	02/10	HP	HP request to add debug port for IAMT.	Add JIAMT1.	0.2
21	16	WWAN CONN	02/10	HP	WOW# to WWAN connector is no longer supported.	Remove R117 and signal.	0.2
22	13	SATA port	02/10	HP	Change SATA assignments to support PM.	Port 4 --> 5, Port2 --> 4, Port3 -->2.	0.2
23	31	KBC1091	02/10	HP	Remove ADP_DET# on U23 GPIO9.	Add R320 PD on GPIO9.	0.2
24	24	WLAN	02/10	HP	Remove R441 and connection to JWLAN1.5	Remove R441.	0.2
25	24	USB port6	02/10	HP	Remove USB signals to JWLAN1.36 and 38.	Remove them.	0.2
26	20	WLAN	02/10	HP	Add 680P on DISP_OFF# close JLCD1 and change C359.	Change C359 to 0.1uF and add C439.	0.2
27	22	Intel 82578	02/10	HP	Can remove Q17, R405 & R124 if no leakage.	Reserve Q17, R405 and R124 in DB2.	0.2
28	4, 16	Intel Change	02/10	HP	414044 DG update 1.11	Change R31/R32 to 1.5K/750ohm and R297 to 100K.	0.2
29	31	System ID control	02/17	HP	Common Design with other project.	Del D49, R149 and Q154 and Add U44.	0.2
30	20	Webcam	02/17	HP	WEBCAM_OFF is active high, so need change design.	Add R287 to turn on Gate.	0.2
31	15	PWR_GD	02/17	HP	HP request to change design.	Add R399 and install R237.	0.2
32	15	NAND Flash	02/17	HP	HP request to change design.	Add NAND_DETECT# form U4.Y7 to JNAND1.17.	0.2
33	4	XDP PU	02/17	HP	HP request to change design.	Del R37, R38, R39.	0.2
34	22	LAN Power	02/17	HP	Remove power switch from 3V to 1V and related parts.	Remove C382, C383, C384, C385, C694, R401, R366, Q21 and R402.	0.2
35	29	Docking	02/17	HP	HP agree to remove caps for DP from MB to DOCKING.	Remove C496 ~ C511 from MB.	0.2
36	33	Super I/O	02/17	Compal	Common design change to SMS		0.2

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Version Change List (P. I. R. List) for HW Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	25	ESD DIODE	04/23	Compal	Wrong connection of D53 & D54, system can't boot.	Swap +5VS & GND of D53 & D54 pin 2 & 5.	0.3
2	29	SATA Port 5	04/23	Compal	It have wrong connection of JDOCK1 pin108 & pin109.	Swap SATA_PTX_C_DRX_P5/N5 of connector side.	0.3
3	28	SPI_CS0#	04/23	HP	HP request to add pull up resistor close to SPI ROM.	Reserve R6 close to U19.	0.3
4	14	SM BUS	04/23	HP	Intel request to change PU to 2.2K.	Change R199, R200 from 4.7K to 2.2K	0.3
5	23	LAN Transfermer	04/23	HP	Intel request to add 1uF cap between TRM caps to GND	Add C264 to GND.	0.3
6	13	JTAG Port	04/24	HP	HP review need swap JTAG1 pin4 & pin6.	Swap XDP_FN16 & XDP_FN17 at JTAG1 side.	0.3
7	17	PCH +1.05VS	04/25	HP	HP review will no need connect resistor between them.	Remove R310.	0.3
8	14	PCH 25MHz Crystall	04/25	HP	No need 25MHz for PCH as common design.	No install R229, C281, C282, Y4 but add R52.	0.3
9	31	KBC1098 VCC0	04/25	HP	The VCC0 will never connect to GND.	Remove R587 from schematic.	0.3
10	16	LAN_DIS#	04/25	HP	GPIO12 of PCH have internal PU.	No install R279 and reserve R53 PD.	0.3
11	21	DPA AUX	04/25	HP	Need 0.1uF cap for Q20, Q67 gate pin.	Add C265.	0.3
12	30	WWAN_DET#	04/25	HP	Design Change PCH GPIO22 to WWAN_DET#.	Change GPIO of PCH to WWAN_DET#.	0.3
13	16	Webcam control	04/25	HP	Chnage the control pin from GPIO47 to GPIO22 of PCH	Modify WEBCAM_OFF to WEBCAM_ON, add R66 PU for GPIO47.	0.3
14	20	Webcam control	04/25	HP	Chnage the control pin from GPIO47 to GPIO22 of PCH	Del R350.	0.3
15	13	DOCK LED	04/25	HP	Need inverter for docking power LED signal.	Add Q71 & R67.	0.3
16	33	SER_SHD	04/25	HP	HP request to remove SER_SHD from SIO to docking.	Disconnect SER_SHD at docking side, add R7 PU to +3VS.	0.3
17	9, 10	DDR3 M1 & M3	04/30	HP	Need implement M1, M3 but reserve M2 for S11.	Remove R91, R682~R684 and add divider for V_DDR_CPU_REF0/1.	0.3
18	17	PCH Power Rail		HP	Some power rail of PCH are no use.	Remove these power and add TP.	0.3
19	32	Card Reader		HP	It will need find tune value of R731 & C661.	Change R731 to 100K & C661 to 1uF X5R as Cartier first.	0.3
20	9	Debug port		HP	HP request to add debug port for IAMT.	Add JIAMT1.	0.3
21	16	WWAN CONN		HP	WOW# to WWAN connector is no longer supported.	Remove R117 and signal.	0.3
22	13	SATA port		HP	Change SATA assignments to support PM.	Port 4 --> 5, Port2 --> 4, Port3 -->2.	0.3
23	31	KBC1091		HP	Remove ADP_DET# on U23 GPIO9.	Add R320 PD on GPIO9.	0.3
24	24	WLAN		HP	Remove R441 and connection to JWLAN1.5	Remove R441.	0.3
25	24	USB port6		HP	Remove USB signals to JWLAN1.36 and 38.	Remove them.	0.3
26	20	WLAN		HP	Add 680P on DISP_OFF# close JLCD1 and change C359.	Change C359 to 0.1uF and add C439.	0.3
27	22	Intel 82578		HP	Can remove Q17, R405 & R124 if no leakage.	Reserve Q17, R405 and R124 in DB2.	0.3
28	4, 16	Intel Change		HP	414044 DG update 1.11	Change R31/R32 to 1.5K/750ohm and R297 to 100K.	0.3
29	31	System ID control		HP	Common Design with other project.	Del D49, R149 and Q154 and Add U44.	0.3
30	20	Webcam		HP	WEBCAM_OFF is active high, so need change design.	Add R287 to turn on Gate.	0.3
31	15	PWR_GD		HP	HP request to change design.	Add R399 and install R237.	0.3
32	15	NAND Flash		HP	HP request to change design.	Add NAND_DETECT# form U4.Y7 to JNAND1.17.	0.3
33	4	XDP PU		HP	HP request to change design.	Del R37, R38, R39.	0.3
34	22	LAN Power		HP	Remove power switch from 3V to 1V and related parts.	Remove C382, C383, C384, C385, C694, R401, R366, Q21 and R402.	0.3
35	29	Docking		HP	HP agree to remove caps for DP from MB to DOCKING.	Remove C496 ~ C511 from MB.	0.3
36	33	Super I/O		Compal	Common design change to SMS		0.3

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Version Change List (P. I. R. List) for HW Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	4	FAN CTRL Circuit	07/2	HP	FAN always 100% turn after power on	Del D29 & NI R133 to prevent this issue.	0.4
2	29	SATA Port 5	04/23	Compal	It have wrong connection of JDock1 pin108 & pin109.	Swap SATA_PTX_C_DRX_P5/N5 of connector side.	0.3
3	28	SPI_CS0#	04/23	HP	HP request to add pull up resistor close to SPI ROM.	Reserve R6 close to U19.	0.3
4	14	SM BUS	04/23	HP	Intel request to change PU to 2.2K.	Change R199, R200 from 4.7K to 2.2K	0.3
5	23	LAN Transfermer	04/23	HP	Intel request to add 1uF cap between TRM caps to GND	Add C264 to GND.	0.3
6	13	JTAG Port	04/24	HP	HP review need swap JTAG1 pin4 & pin6.	Swap XDP_FN16 & XDP_FN17 at JTAG1 side.	0.3
7	17	PCH +1.05VS	04/25	HP	HP review will no need connect resistor between them.	Remove R310.	0.3
8	14	PCH 25MHz Crystall	04/25	HP	No need 25MHz for PCH as common design.	No install R229, C281, C282, Y4 but add R52.	0.3
9	31	KBC1098 VCC0	04/25	HP	The VCC0 will never connect to GND.	Remove R587 from schematic.	0.3
10	16	LAN_DIS#	04/25	HP	GPIO12 of PCH have internal PU.	No install R279 and reserve R53 PD.	0.3
11	21	DPA AUX	04/25	HP	Need 0.1uF cap for Q20, Q67 gate pin.	Add C265.	0.3
12	30	WWAN_DET#	04/25	HP	Design Change PCH GPIO22 to WWAN_DET#.	Change GPIO of PCH to WWAN_DET#.	0.3
13	16	Webcam control	04/25	HP	Chnage the control pin from GPIO47 to GPIO22 of PCH	Modify WEBCAM_OFF to WEBCAM_ON, add R66 PU for GPIO47.	0.3
14	20	Webcam control	04/25	HP	Chnage the control pin from GPIO47 to GPIO22 of PCH	Del R350.	0.3
15	13	DOCK LED	04/25	HP	Need inverter for docking power LED signal.	Add Q71 & R67.	0.3
16	33	SER_SHD	04/25	HP	HP request to remove SER_SHD from SIO to docking.	Disconnect SER_SHD at docking side, add R7 PU to +3VS.	0.3
17	9, 10	DDR3 M1 & M3	04/30	HP	Need implement M1, M3 but reserve M2 for S11.	Remove R91, R682~R684 and add divider for V_DDR_CPU_REF0/1.	0.3
18	17	PCH Power Rail		HP	Some power rail of PCH are no use.	Remove these power and add TP.	0.3
19	32	Card Reader		HP	It will need find tune value of R731 & C661.	Change R731 to 100K & C661 to 1uF X5R as Cartier first.	0.3
20	9	Debug port		HP	HP request to add debug port for IAMT.	Add JIAMT1.	0.3
21	16	WWAN CONN		HP	WOW# to WWAN connector is no longer supported.	Remove R117 and signal.	0.3
22	13	SATA port		HP	Change SATA assignments to support PM.	Port 4 --> 5, Port2 --> 4, Port3 -->2.	0.3
23	31	KBC1091		HP	Remove ADP_DET# on U23 GPIO9.	Add R320 PD on GPIO9.	0.3
24	24	WLAN		HP	Remove R441 and connection to JWLAN1.5	Remove R441.	0.3
25	24	USB port6		HP	Remove USB signals to JWLAN1.36 and 38.	Remove them.	0.3
26	20	WLAN		HP	Add 680P on DISP_OFF# close JLCD1 and change C359.	Change C359 to 0.1uF and add C439.	0.3
27	22	Intel 82578		HP	Can remove Q17, R405 & R124 if no leakage.	Reserve Q17, R405 and R124 in DB2.	0.3
28	4, 16	Intel Change		HP	414044 DG update 1.11	Change R31/R32 to 1.5K/750ohm and R297 to 100K.	0.3
29	31	System ID control		HP	Common Design with other project.	Del D49, R149 and Q154 and Add U44.	0.3
30	20	Webcam		HP	WEBCAM_OFF is active high, so need change design.	Add R287 to turn on Gate.	0.3
31	15	PWR_GD		HP	HP request to change design.	Add R399 and install R237.	0.3
32	15	NAND Flash		HP	HP request to change design.	Add NAND_DETECT# form U4.Y7 to JNAND1.17.	0.3
33	4	XDP PU		HP	HP request to change design.	Del R37, R38, R39.	0.3
34	22	LAN Power		HP	Remove power switch from 3V to 1V and related parts.	Remove C382, C383, C384, C385, C694, R401, R366, Q21 and R402.	
35	29	Docking		HP	HP agree to remove caps for DP from MB to DOCKING.	Remove C496 ~ C511 from MB.	
36	33	Super I/O		Compal	Common design change to SMS		

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