# Compal Confidential

## QCL51 Schematics Document

### AMD Comal Platform

### AMD Trinity APU / Hudson FCH / ATI Chelsea Pro M2

### Muxless/UMA / PX 4.0 / PX 5.0

2011-10-26

LA-8712P REV: 0.1

| | | | | |
|---|---|---|---|---|
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| | | | | Date: Monday, November 28, 2011; Sheet 1 of 56 |

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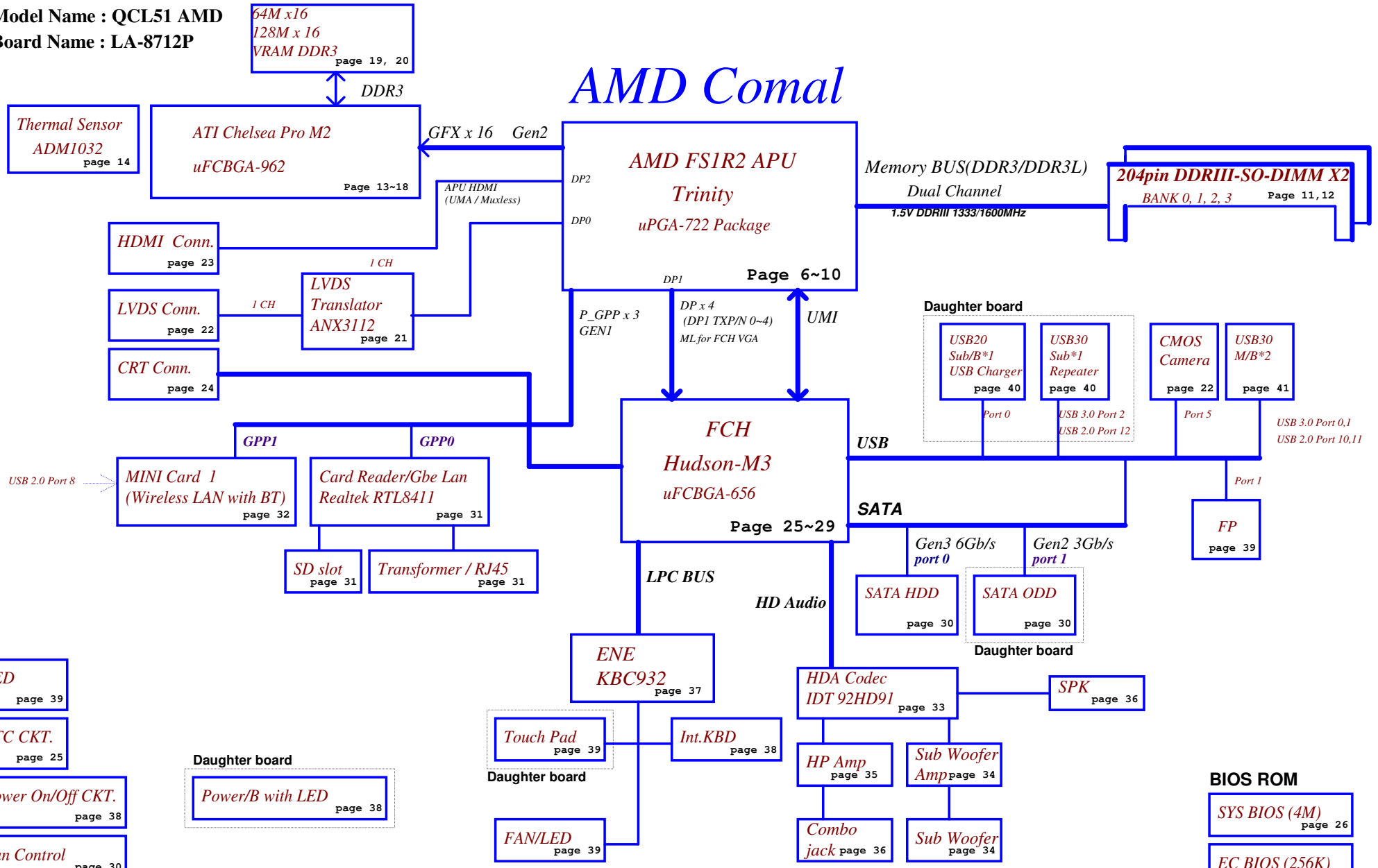
**Model Name : QCL51 AMD**
**Board Name : LA-8712P**

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Title: Block Diagrams

Size: B | Document Number: QCL51 LA-8712P | Rev: 0.1

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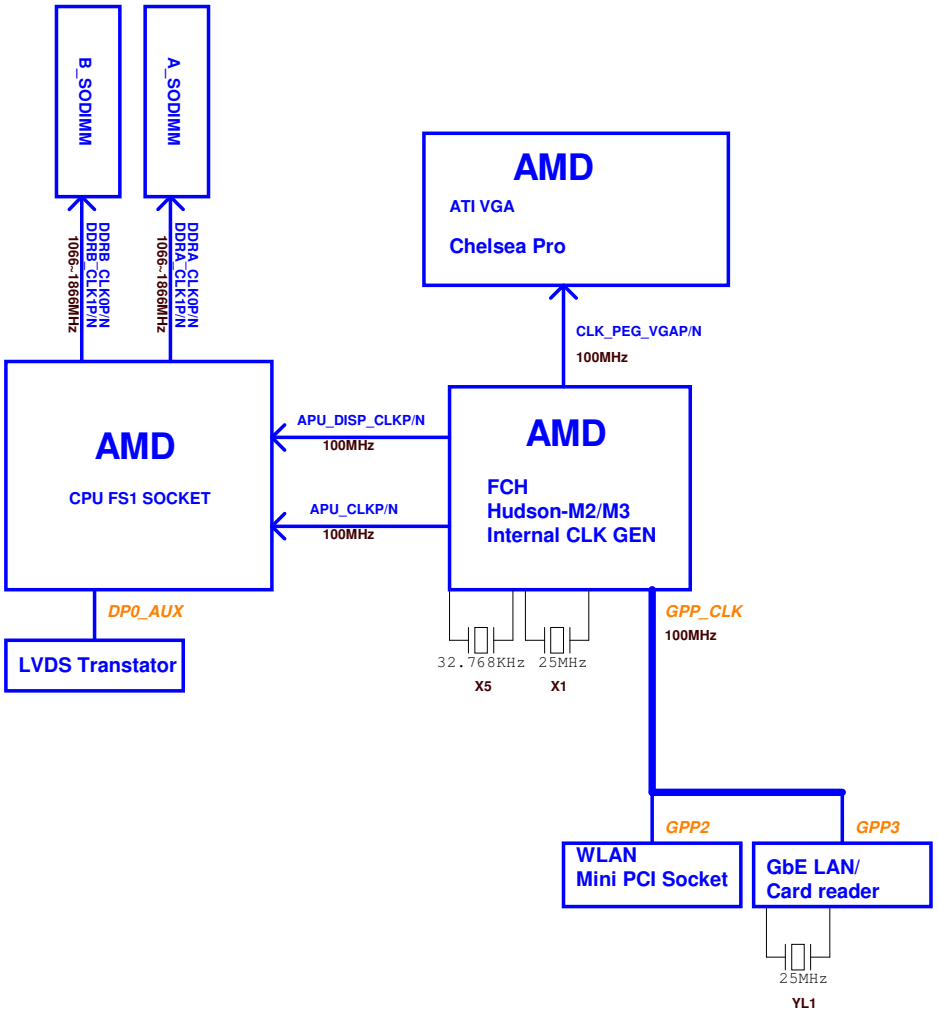
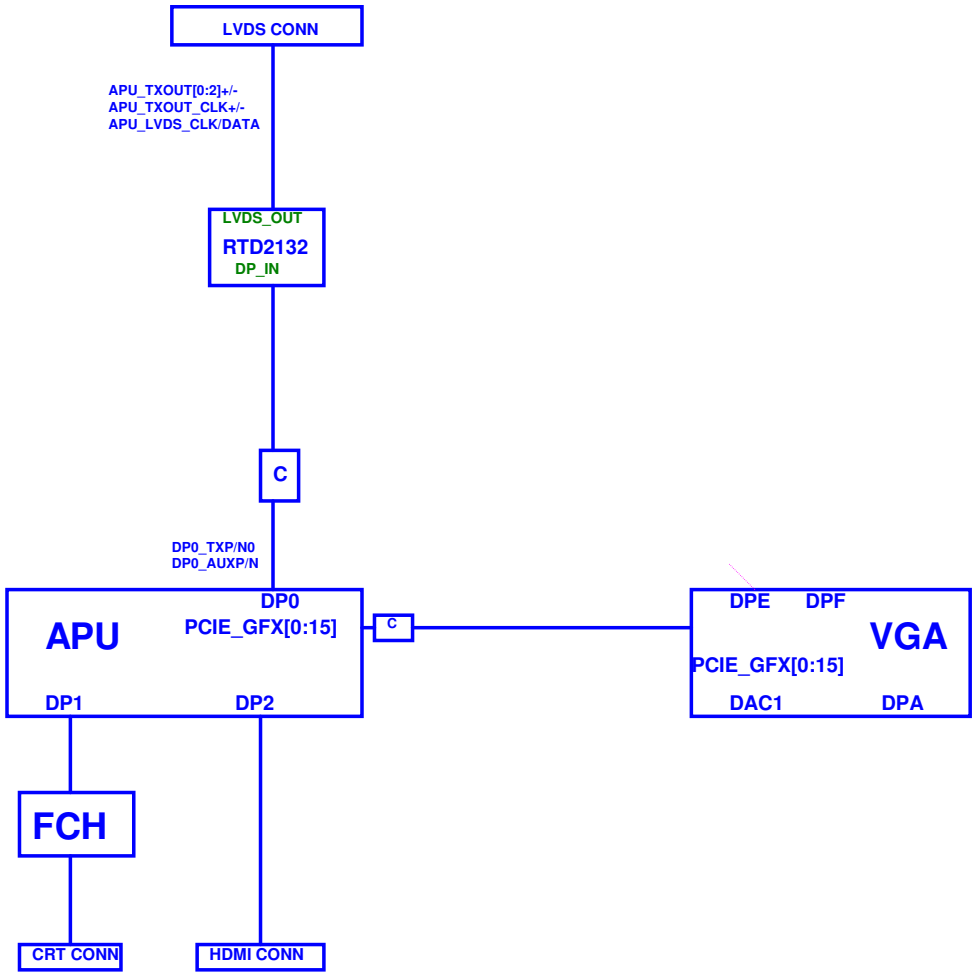
# CLOCK DISTRIBUTION




# DISPLAY OUTPUT

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Title: CLOCK / DISPLAY DISTRIBUTION

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## Voltage Rails

| Power Plane | Description | S1 | S3 | S5 |
|---|---|---|---|---|
| VIN | Adapter power supply (19V) | N/A | N/A | N/A |
| B+ | AC or battery power rail for power circuit. | N/A | N/A | N/A |
| +APU_CORE | Core voltage for CPU | ON | OFF | OFF |
| +APU_CORE_NB | Voltage for On-die VGA of APU | ON | OFF | OFF |
| +VGA_CORE | 0.95-1.2V switched power rail | ON | OFF | OFF |
| +VDDCI | 0.95-1.2V switched power rail | ON | OFF | OFF |
| +0.75VS | 0.75V switched power rail for DDR terminator | ON | ON | OFF |
| +0.935VGS | 0.935V switched power rail for VGA | ON | OFF | OFF |
| +1.1ALW | 1.1V switched power rail for FCH | ON | ON | ON* |
| +1.1VS | 1.1V switched power rail for FCH | ON | OFF | OFF |
| +1.2VS | 1.2V switched power rail for APU | ON | OFF | OFF |
| +1.5V | 1.5V power rail for CPU VDDIO and DDR | ON | ON | OFF |
| +1.5V_PCIE | 1.5V switched power rail | ON | OFF | OFF |
| +1.8VGS | 1.8V switched power rail | ON | OFF | OFF |
| +2.5VS | 2.5V for CPU_VDDA | ON | OFF | OFF |
| +3VALW | 3.3V always on power rail | ON | ON | ON* |
| +LAN_VDD_3V3 | 3.3V power rail for LAN | ON | ON | ON |
| +3VS | 3.3V switched power rail | ON | OFF | OFF |
| +5VALW | 5V always on power rail | ON | ON | ON* |
| +5VS | 5V switched power rail | ON | OFF | OFF |
| +VSB | VSB always on power rail | ON | ON | ON* |
| +RTCVCC | RTC power | ON | ON | ON |

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

| STATE \ SIGNAL | SLP_S1# | SLP_S3# | SLP_S4# | SLP_S5# | +VALW | +V | +VS | Clock |
|---|---|---|---|---|---|---|---|---|
| Full ON | HIGH | HIGH | HIGH | HIGH | ON | ON | ON | ON |
| S1(Power On Suspend) | LOW | HIGH | HIGH | HIGH | ON | ON | ON | LOW |
| S3 (Suspend to RAM) | LOW | LOW | HIGH | HIGH | ON | ON | OFF | OFF |
| S4 (Suspend to Disk) | LOW | LOW | LOW | HIGH | ON | OFF | OFF | OFF |
| S5 (Soft OFF) | LOW | LOW | LOW | LOW | ON | OFF | OFF | OFF |

ZZZ1

PCB
Part Number = DA80000SH00
PCB 0OH LA-8712P REV0 M/B

## Board ID / SKU ID Table for AD channel

| | |
|---|---|
| Vcc | 3.3V +/- 5% |
| Ra/Rb | 100K +/- 5% |

| Board ID | Ra / Rb | $V_{AD\_BID}$ min | $V_{AD\_BID}$ typ | $V_{AD\_BID}$ max |
|---|---|---|---|---|
| 0 | 0 | 0 V | 0 V | 0 V |
| 1 | 8.2K +/- 5% | 0.216 V | 0.250 V | 0.289 V |
| 2 | 18K +/- 5% | 0.436 V | 0.503 V | 0.538 V |
| 3 | 33K +/- 5% | 0.712 V | 0.819 V | 0.875 V |
| 4 | 56K +/- 5% | 1.036 V | 1.185 V | 1.264 V |
| 5 | 100K +/- 5% | 1.453 V | 1.650 V | 1.759 V |
| 6 | 200K +/- 5% | 1.935 V | 2.200 V | 2.341 V |
| 7 | NC | 2.500 V | 3.300 V | 3.300 V |

## BOARD ID Table

| Board ID | PCB Revision |
|---|---|
| 0 | DB |
| 1 | |
| 2 | |
| 3 | |
| 4 | |
| 5 | |
| 6 | |
| 7 | |

## BOM Option Table

| BOM Structure | Description |
|---|---|
| PX@ | PX function |

## BOM Config

| | |
|---|---|
| UMA | PX |
| | V |

x = 1 is read cmd, x= 0 is writee cmd.

## External PCI Devices

| Device | IDSEL# | REQ#/GNT# | Interrupts |
|---|---|---|---|
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |

## EC SM Bus1 address

| Device | Address | HEX |
|---|---|---|
| Smart Battery | 0001 011X b | 16H |
| | | |
| | | |
| | | |
| | | |

## EC SM Bus2 address

| Device | Address | HEX |
|---|---|---|
| ADI ADM1032 (GPU) | 1001 101X b | 9AH |
| SB-TSI (APU) | 1001 100X b | 98H |
| LVDS TR | 1010 100X b | A8H |
| VGA Internal Thermal | 1000 001X b | 82H |
| | | |

## FCH (S0) SM Bus 0 address

| Device | Address | HEX |
|---|---|---|
| DDR DIMM1 | 1010 000X b | A0 |
| DDR DIMM2 | 1010 001X b | A2 |
| Amplifier | | |
| | | |
| | | |

## FCH (S0~S5) SM Bus 1 address

| Device | Address | HEX |
|---|---|---|
| Touch pad | | |
| | | |
| | | |
| | | |
| | | |

| | | | |
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Title: Notes List

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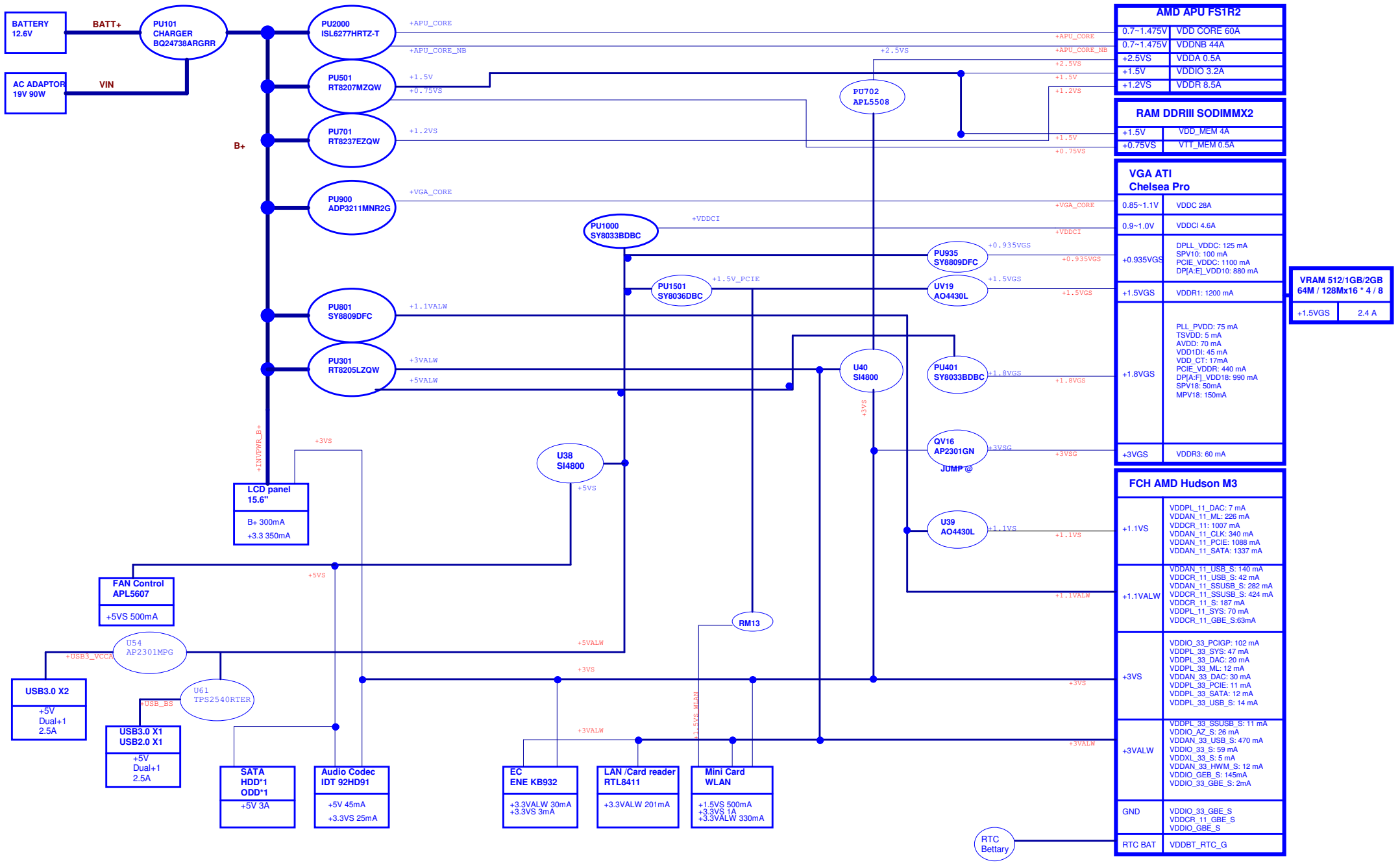


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Title: POWER DELIVERY CHART

| Size | Document Number | Rev |
|---|---|---|
| Custom | QCL51 LA-8712P | 0.1 |

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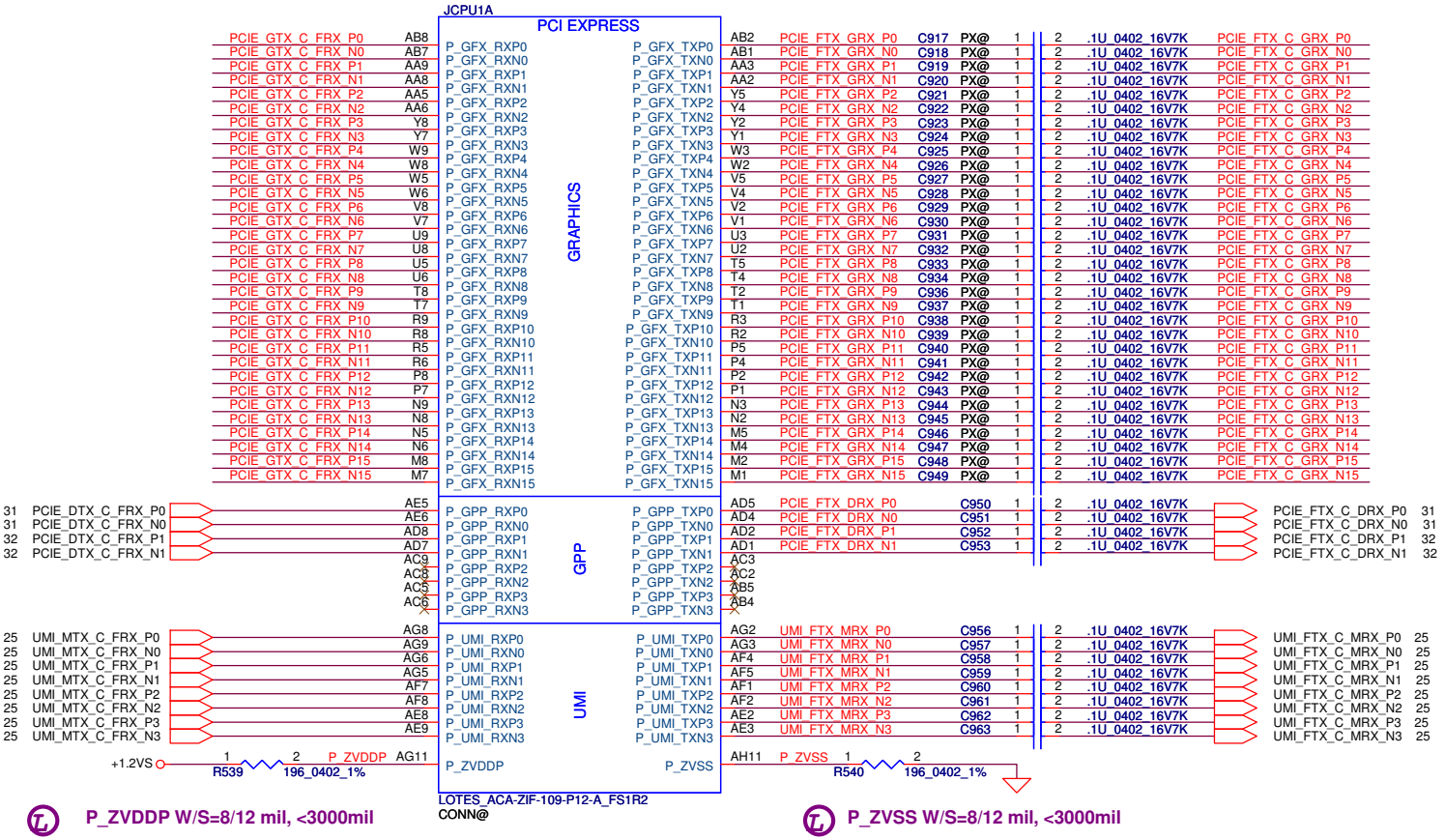
13 PCIE_GTX_C_FRX_P[0..15]
13 PCIE_GTX_C_FRX_N[0..15]

PCIE_FTX_C_GRX_P[0..15] 13
PCIE_FTX_C_GRX_N[0..15] 13

GPU

GLAN/Card reader
WLAN

UMI




P_ZVDDP W/S=8/12 mil, <3000mil

P_ZVSS W/S=8/12 mil, <3000mil

GPU

GLAN/Card reader
WLAN

UMI

| | | | |
|---|---|---|---|
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| | | | |
|---|---|---|---|
| Title | AMD FS1R2 PCIE / GFX / UMI | | |
| Size B | Document Number QCL51 LA-8712P | | Rev 0.1 |
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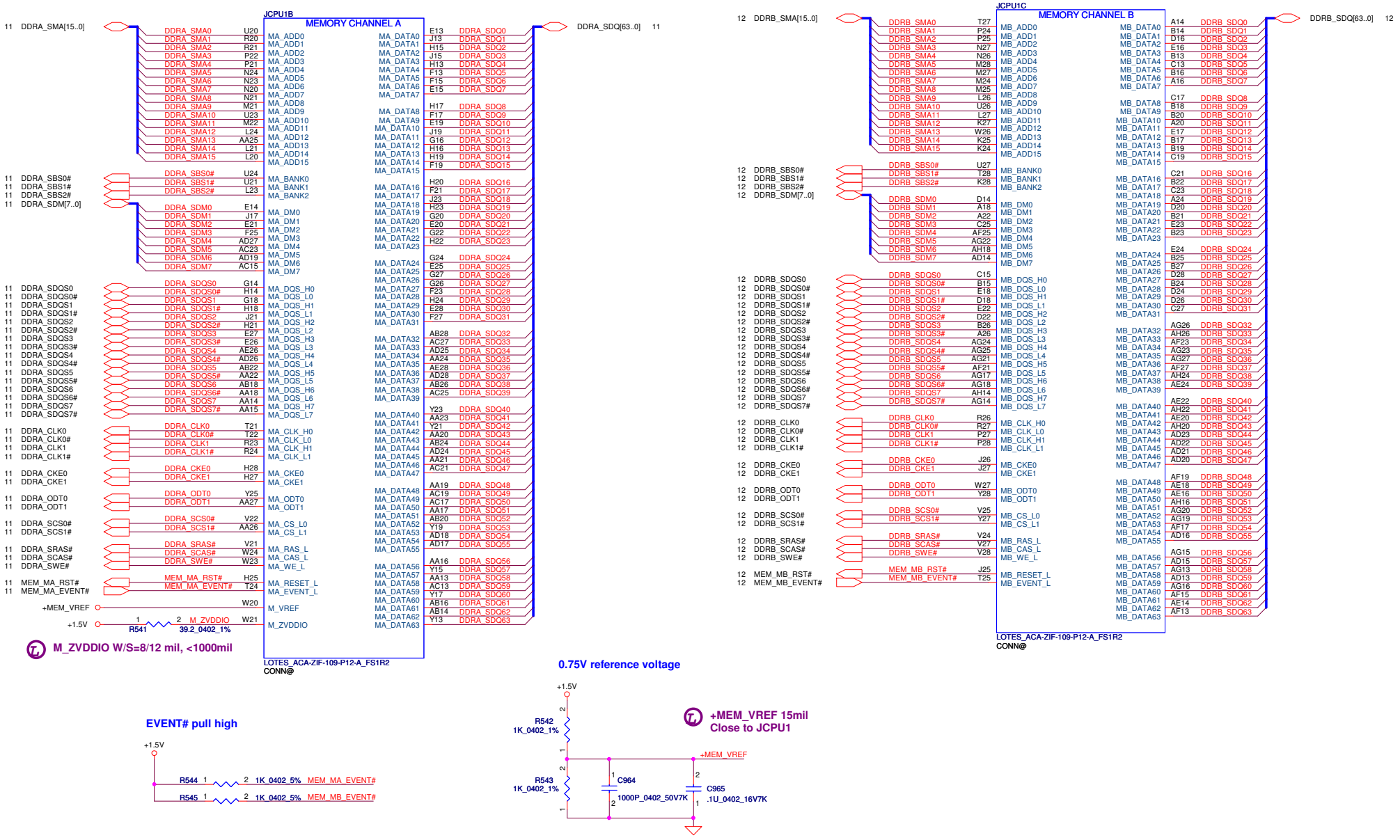


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|---|---|---|---|
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Title: AMD FS1 DDRIII I/F

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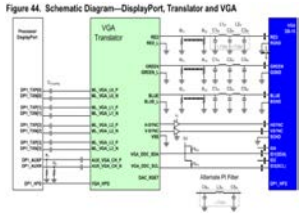


Close to APU (JCPU1)

Place near APU

JCPU1D

ANALOG/DISPLAY/MISC

To LVDS Translator

Del DP0_TXP1/N1

To FCH VGA ML

To HDMI

To LVDS Translator

To FCH

To HDMI

LA-8124 no use this DP_ENBKL.

Del DP_ENVDD

VDDIO level
Need Level shift

LVDS/eDP
CRT
HDMI

DP_AUX_ZVSS W/S=8/12 mil, <3000mil

11/14 Reserve

Allow_STOP leakage issue

For ESD request close APU side

100MHz

100MHz NSS

SVI 2.0 (0 ohm at Power Side)

SB-TSI (S5 Domain)

Internal PU when no use HDT

11/15 RF

TEST35 change to PU for HDMI can not output 20110126

11/14 Change net name

Close to Header

10/27 300 ohm??

Route as differential with APU_VDD_RUN_FB_L

## CPU TSI interface level shift

BSH111, the Vgs is:
min = 0.4V
Max = 1.3V

When APU High -> MOS OFF (Vgs < 0.4V )
APU Low -> MOS ON (Vgs > 1.3V)

Vg = 1.607 V

Asserted as an input to force processor into HTC-active state

THERMTRIP shutdown temperature: 115 degree

Indicates to the FCH that a thermal trip has occurred. Its assertion will cause the FCH to transition the system to S5 immediately

## HDT Debug conn

11/10 del debug connector

| | | | |
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Title: AMD FS1 Display / MISC / HDT

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| Power Name | Consumption |
|---|---|
| VDD<br>+CPU_CORE | 60A |
| VDDNB<br>+CPU_CORE_NB | 37A |
| VDDIO<br>+1.5V | 3.2A |
| VDDP / VDDR<br>+1.2VS | 5A / 3.5A |
| VDDA<br>+2.5VS | 0.75A |

+CPU_CORE-->+APU_CORE

On power team page

On power team page

+CPU_CORE Decoupling

330uF x 4 @ x1
22uF x 10
0.22uF x2
0.01uF x3
180pF x2 @ x1

+CPU_CORE_NB Decoupling

330uF x2
22uF x2 @ x2
10uF x1
0.22uF x2
180pF x3

+1.5V / VDDIO Decoupling

330uF x1
22uF x4
4.7uF x4
0.22uF x6
180pF x1 @x1

Decoupling between CPU and DIMMs across VDDIO and VSS split

VDDR Decoupling
Close JCPU1.AG10,AH8,AH9,AH10

10uF x3
0.22uF x2
1000pF x1
180pF x2

VDDP Decoupling
Close JCPU1.AH3~7

22uF x1
10uF x3
0.22uF x2
1000pF @x1
180pF x2
220uF x1

VDDA Decoupling

47uF x1
0.22uF x1
3300pF x1
180pF x1

+CPU_CORE_NB-->+APU_CORE_NB

Northbridge Power Pins for Remote Decoupling

VDDIO: 3200mA

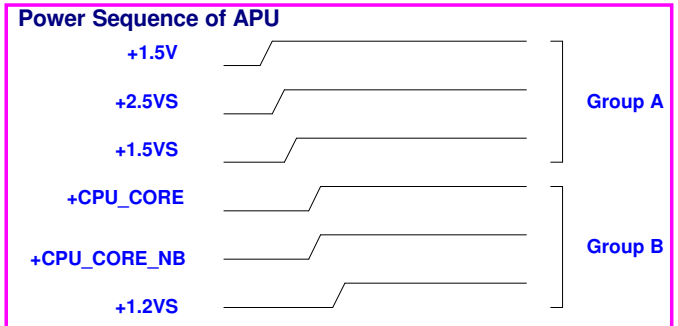
VDDR: 3500mA

VDDP: 5000mA

VDDA: 750mA

FBMA-L11-201209-221LMA30T_0805

## Power Sequence of APU




## Decoupling Caps.

| Pop / @ | 330uF | 220uF | 47uF | 22uF | 10uF | 4.7uF | 0.22uF | 0.01uF | 3300pF | 1nF | 180pF |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pumori 2.0 | | | 0 | 19/11 | 7 | 5 | 17 | 3 | 1 | 1 / 1 | 13/3 |
| Comal | 7 / 2 | 1 | 1 | 19/11 | 7 | 4 | 17 | 3 | 1 | 1 / 1 | 14/2 |
| P5WS5 | 7 / 2 | 1 | 1 | 13 | 3 | 8 | 19 | 3 | 1 | 4 | 16 |



| | | | |
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Title: AMD FS1R2 PWR / GND

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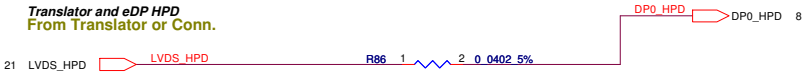
## HPD

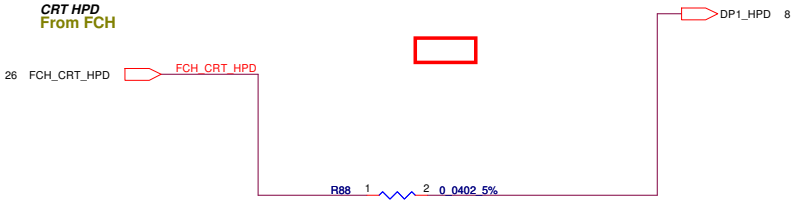
Del reserved NMOS

*Translator and eDP HPD*
From Translator or Conn.



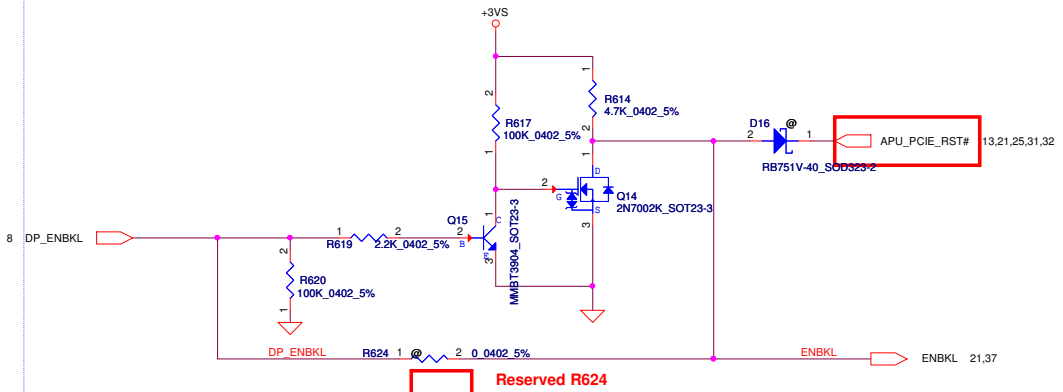

Del reserved NMOS

*CRT HPD*
From FCH




## Panel ENBKL

LA-8124 no use this DP_ENBKL.



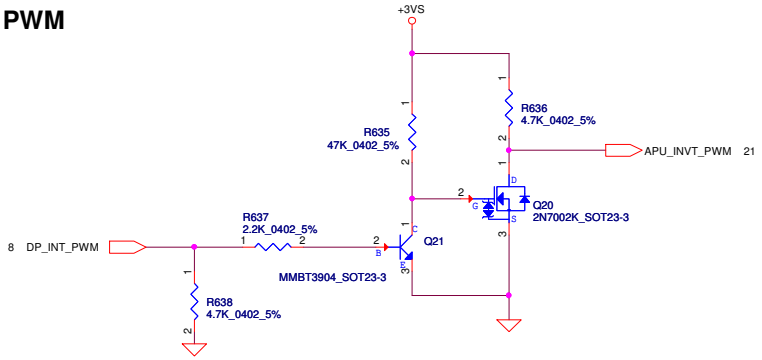

Reserved R624

Del VGA_ENBKL

## eDP Panel ENVDD

Del eDP panel control

## Panel PWM

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Title: AMD FS1R2 Singal Level Shifter

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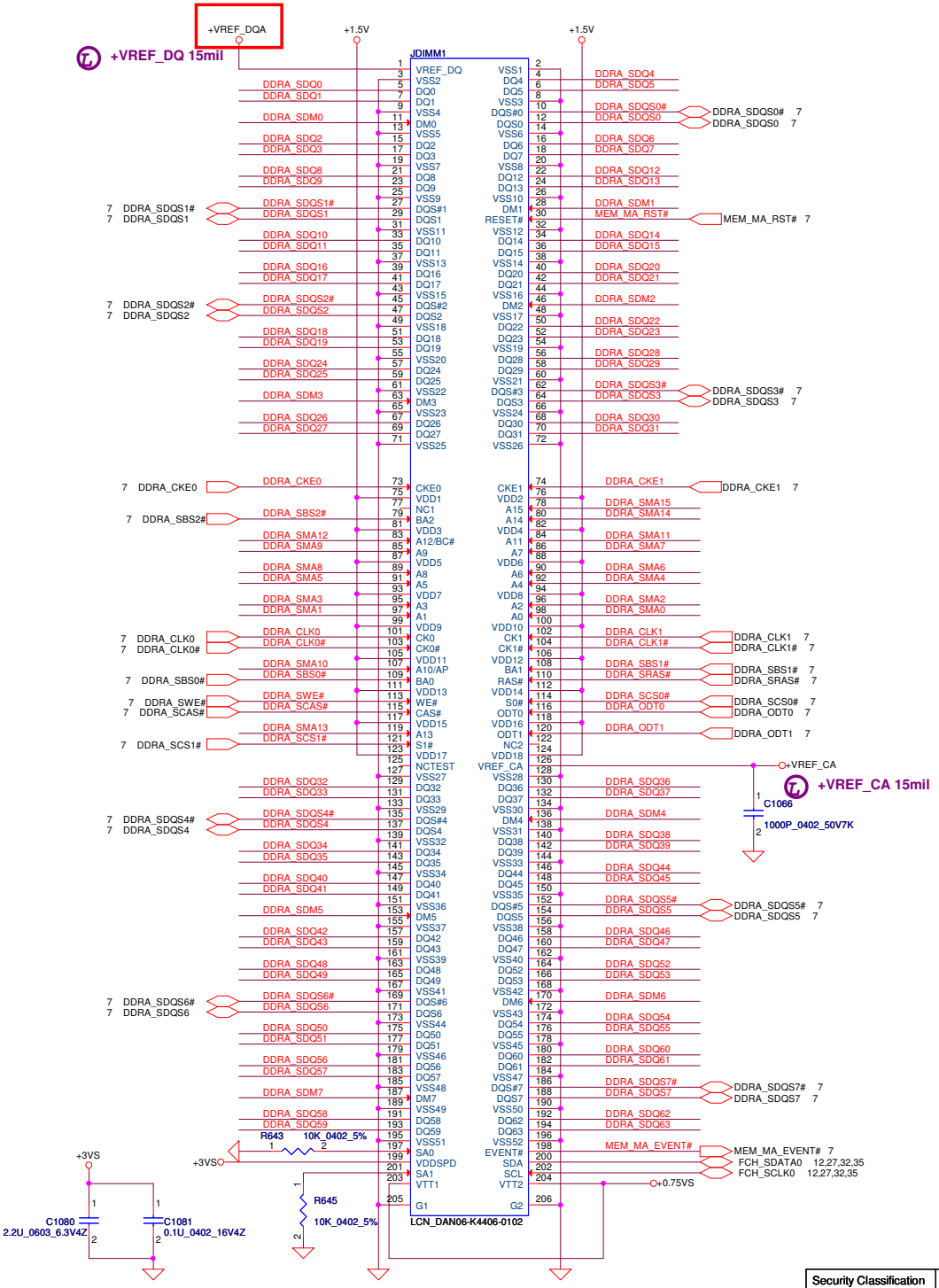


# DIMM_A REV H:4mm

**<Address: 00>**

| | | | |
|---|---|---|---|
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Title: DDRIII SO-DIMM 1

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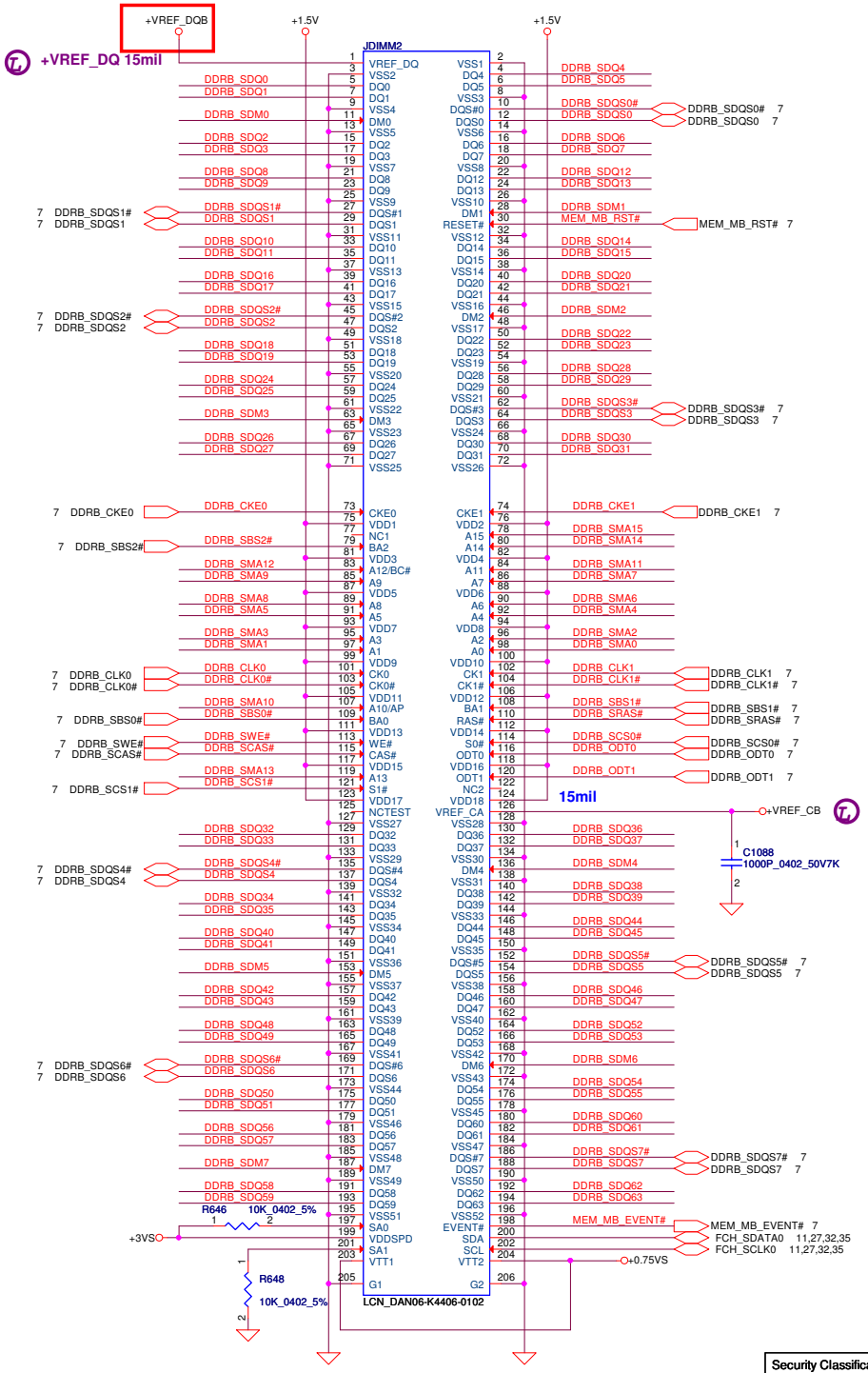
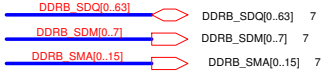
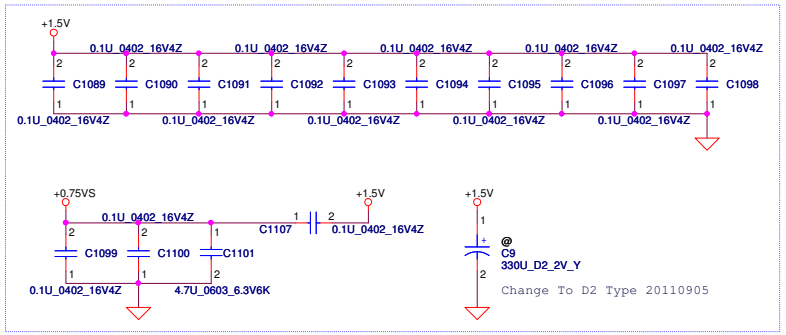
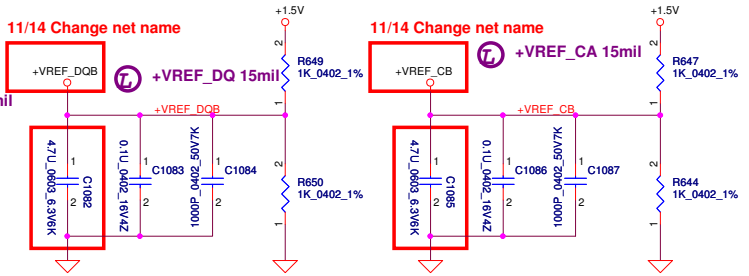



**Place near DIMM2**




**DIMM_B REV H:8mm**

**<Address: 01>**

| | | | |
|---|---|---|---|
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Title: DDRIII SO-DIMM 2

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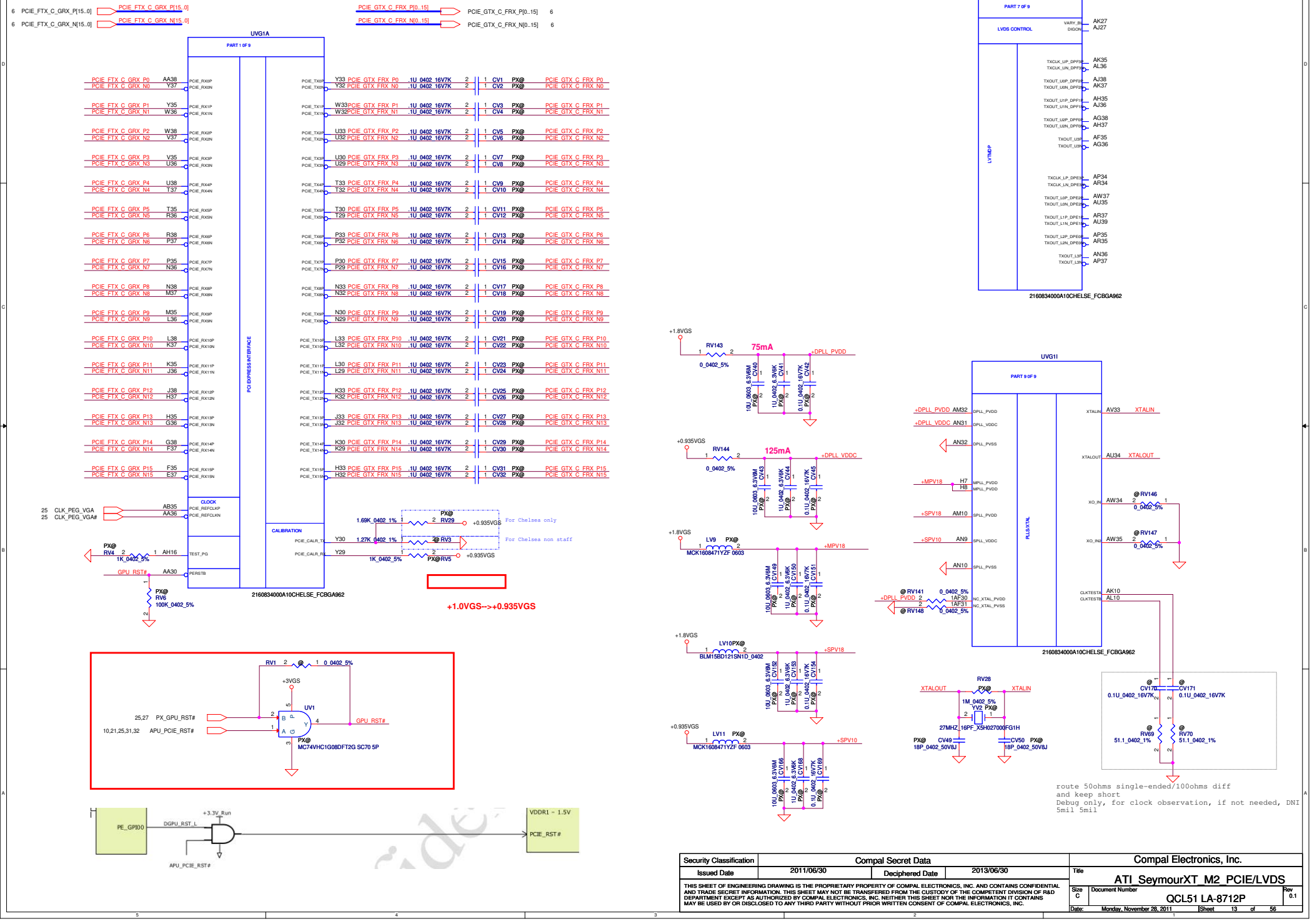
# LVDS Interface

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| Security Classification | Compal Secret Data | | Compal Electronics, Inc. |
| Issued Date | 2011/06/30 | Deciphered Date | 2013/06/30 |
| Title | ATI_SeymourXT_M2_PCIE/LVDS | | |
| Size C | Document Number QCL51 LA-8712P | | Rev 0.1 |
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## CONFIGURATION STRAPS

**ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET**

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

| STRAPS | PIN | DESCRIPTION OF DEFAULT SETTINGS <all internal PD> | RECOMMENDED SETTINGS |
|---|---|---|---|
| TX_PWRS_ENB | GPIO0 | PCIE TRANSMITTER Power Saving Enable<br>0: 50% swing<br>1: Full swing | X |
| TX_DEEMPH_EN | GPIO1 | PCIE TRANSMITTER DE-EMPHASIS<br>0: disable<br>1: enable | X |
| RSVD | GPIO2 | Advertises PCIE speed when compliance test<br>0: 2.5GT/s<br>1: 5GT/s | 0 |
| RSVD | GPIO8 | Internal use only.This Pad has an internal PD and Must be 0V at reset. The pad may be left unconnected. | 0 |
| RSVD | H2SYNC | | 0 |
| RSVD | GPIO21 | | 0 |
| BIOS_ROM_EN | GPIO_22_ROMCSB | ENABLE EXTERNAL BIOS ROM<br>0: disable<br>1: enable | X |
| ROMIDCFG(2:0) | GPIO[13:11] | SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT<br>GPIO13,12,11(config 2,1,0): internal PD.<br>a)If BIOS_ROM_EN=1,the config[2:0] defines the ROM type.<br>b)If BIOS_ROM_EN=0,the config[2:0] defines the primary aperture size. | XXX<br>Memory apertures<br>config[3:0]<br>128MB 000<br>256MB 001<br>64MB 010 |
| VIP_DEVICE_STRAP_ENA | V2SYNC | IGNORE VIP DEVICE STRAPS | 0 |
| BIF_VGA DIS | GPIO9 | VGA ENABLED | 0 |
| RSVD | GENERICC | | 0 |
| AUD[1]<br>AUD[0] | HSYNC<br>VSYNC | AUD[1] AUD[0]<br>0 0 No audio function<br>0 1 Audio for DisplayPort and HDMI if dongle is detected<br>1 0 Audio for DisplayPort only<br>1 1 Audio for both DisplayPort and HDMI | 11 |

## AMD RESERVED CONFIGURATION STRAPS

**ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET**

| GPIO21 | H2SYNC | GENERICC | GPIO2 | GPIO8 |
|---|---|---|---|---|

| | | |
|---|---|---|
| TX_PWRS_ENB | GPIO0 | Transmitter Power Saving Enable<br>0: 50% Tx output swing for mobile mode<br>1: full Tx output swing (Default setting for Desktop) |
| TX_DEEMPH_EN | GPIO1 | PCI Express Transmitter De-emphasis Enable<br>0: Tx de-emphasis diabled for mobile mode<br>1: Tx de-emphasis enabled (Defalit setting for desktop) |

## STRAPS

RV9 SMT-->@

Update net name

## VRAM ID

## Internal VGA Thermal Sensor

Use Internal Thermal Sensor

External VGA Thermal Sensor: No stuff

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/30 | Deciphered Date | 2013/06/30 |



Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_Main_MSIC

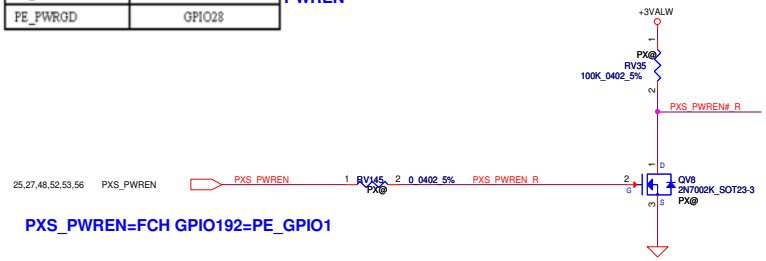
Size: C | Document Number: QCL51 LA-8712P | Rev: 0.1

Date: Monday, November 28, 2011 | Sheet 14 of 56

| Name | FCH Pin Assignments |
|---|---|
| | Hudson-2 / Hudson-3 |
| PE_GPIO0 | GPIO191 |
| PE_GPIO1 | GPIO192 |
| PE_PWRGD | GPIO28 |

GPU_Reset

PWREN

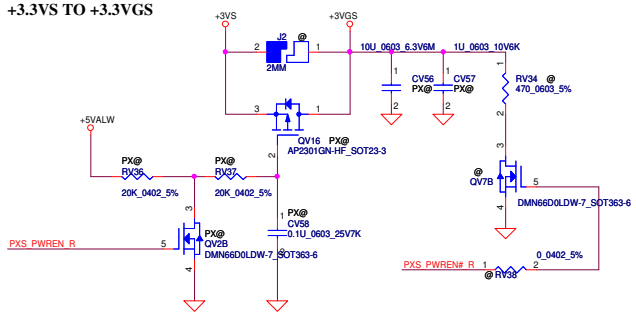



PXS_PWREN=FCH GPIO192=PE_GPIO1

Del +1.8VGS DC DC

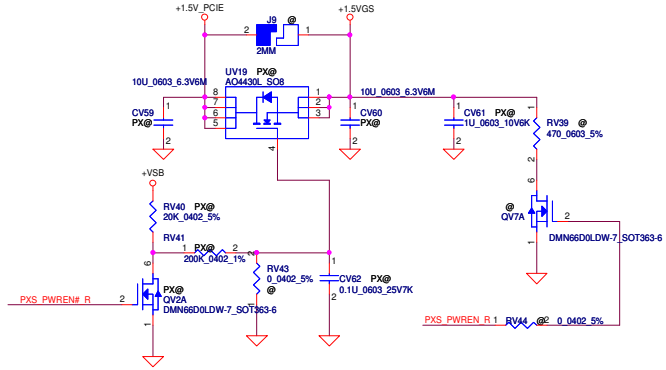
11/10 follow Lotus

+3.3VS TO +3.3VGS




+1.5V_PCIE TO +1.5VGS

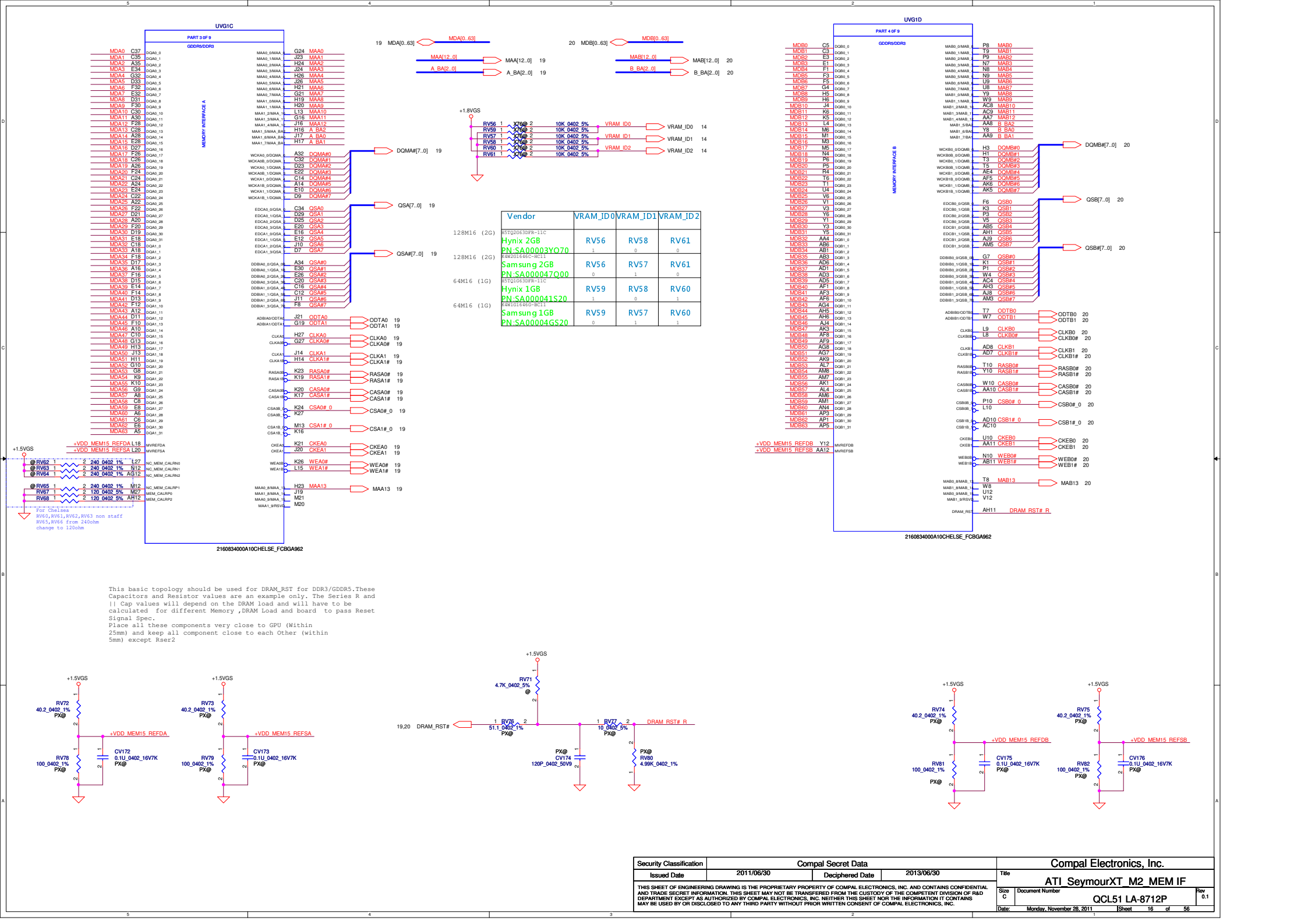
Add +1.5VGS DC DC




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | Compal Electronics, Inc. |
| Issued Date | 2011/06/30 | Deciphered Date | 2013/06/30 |



| | | | |
|---|---|---|---|
| Title | ATI_SeymourXT_M2_BACO POWER | | |
| Size C | Document Number QCL51 LA-8712P | | Rev 0.1 |
| Date: Monday, November 28, 2011 | Sheet 15 of 56 | | |




This basic topology should be used for DRAM_RST for DDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.
Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/30 | Deciphered Date | 2013/06/30 |

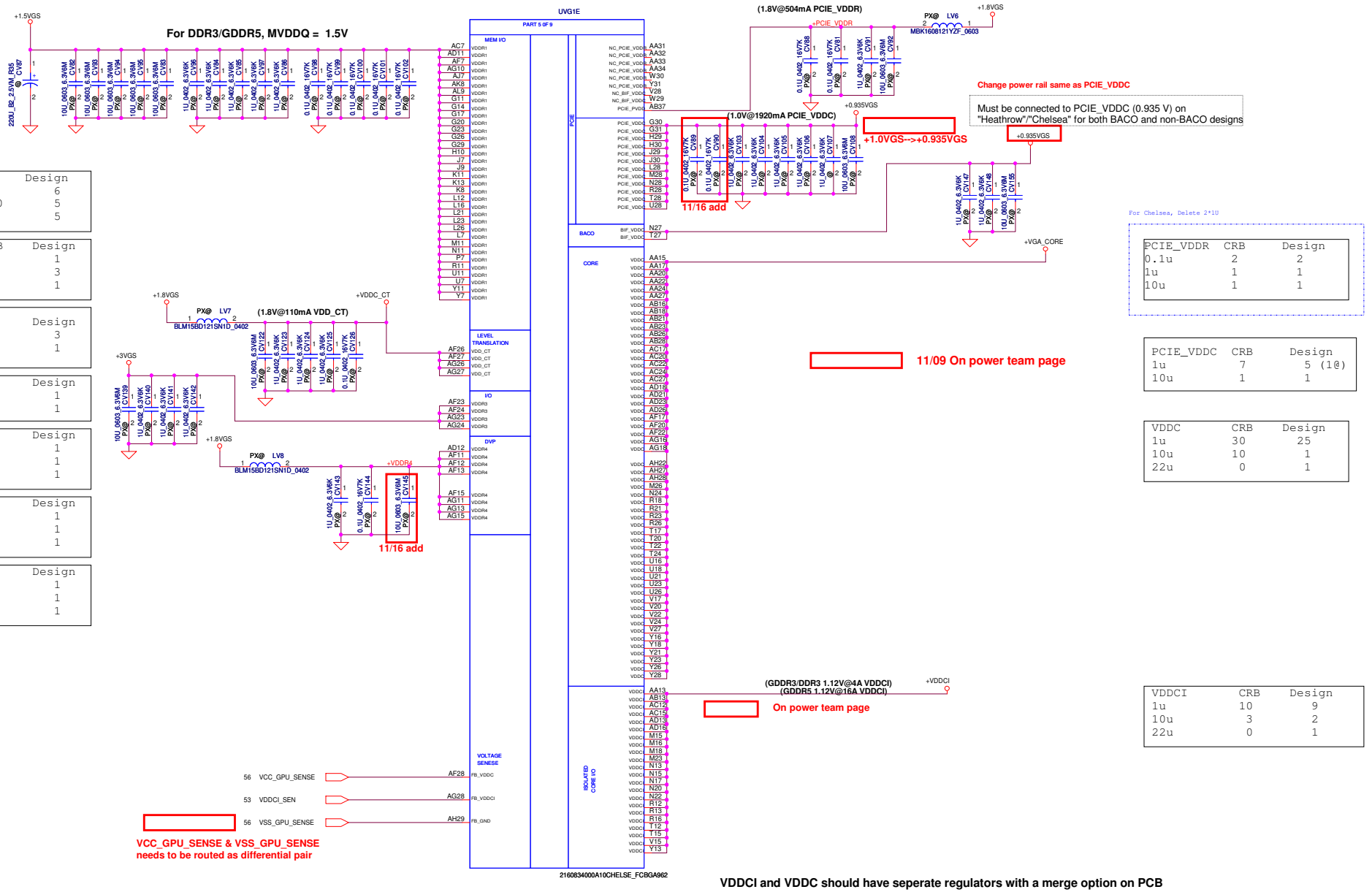


Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_MEM IF

| Size | Document Number | Rev |
|---|---|---|
| C | QCL51 LA-8712P | 0.1 |

Date: Monday, November 28, 2011 Sheet 16 of 56




| VDDR1 | CRB | Design |
|---|---|---|
| 0.1u | 6 | 6 |
| 1u | 10 | 5 |
| 10u | 6 | 5 |

| VDD_CT | CRB | Design |
|---|---|---|
| 0.1u | 1 | 1 |
| 1u | 3 | 3 |
| 10u | 1 | 1 |

| VDDR3 | CRB | Design |
|---|---|---|
| 1u | 3 | 3 |
| 10u | 1 | 1 |

| VDDR4 | CRB | Design |
|---|---|---|
| 0.1u | 1 | 1 |
| 1u | 1 | 1 |

| MPV18 | CRB | Design |
|---|---|---|
| 0.1u | 2 | 1 |
| 1u | 2 | 1 |
| 10u | 1 | 1 |

| SPV18 | CRB | Design |
|---|---|---|
| 0.1u | 1 | 1 |
| 1u | 1 | 1 |
| 10u | 1 | 1 |

| SPV10 | CRB | Design |
|---|---|---|
| 0.1u | 1 | 1 |
| 1u | 1 | 1 |
| 10u | 1 | 1 |

For Chelsea, Delete 2*1U

| PCIE_VDDR | CRB | Design |
|---|---|---|
| 0.1u | 2 | 2 |
| 1u | 1 | 1 |
| 10u | 1 | 1 |

| PCIE_VDDC | CRB | Design |
|---|---|---|
| 1u | 7 | 5 (1@) |
| 10u | 1 | 1 |

| VDDC | CRB | Design |
|---|---|---|
| 1u | 30 | 25 |
| 10u | 10 | 1 |
| 22u | 0 | 1 |

| VDDCI | CRB | Design |
|---|---|---|
| 1u | 10 | 9 |
| 10u | 3 | 2 |
| 22u | 0 | 1 |

**VDDCI and VDDC should have seperate regulators with a merge option on PCB**
**For Madison, Park, Capilano, Robson, Seymour and Whistler, VDDCI and VDDC can share one common regulator**



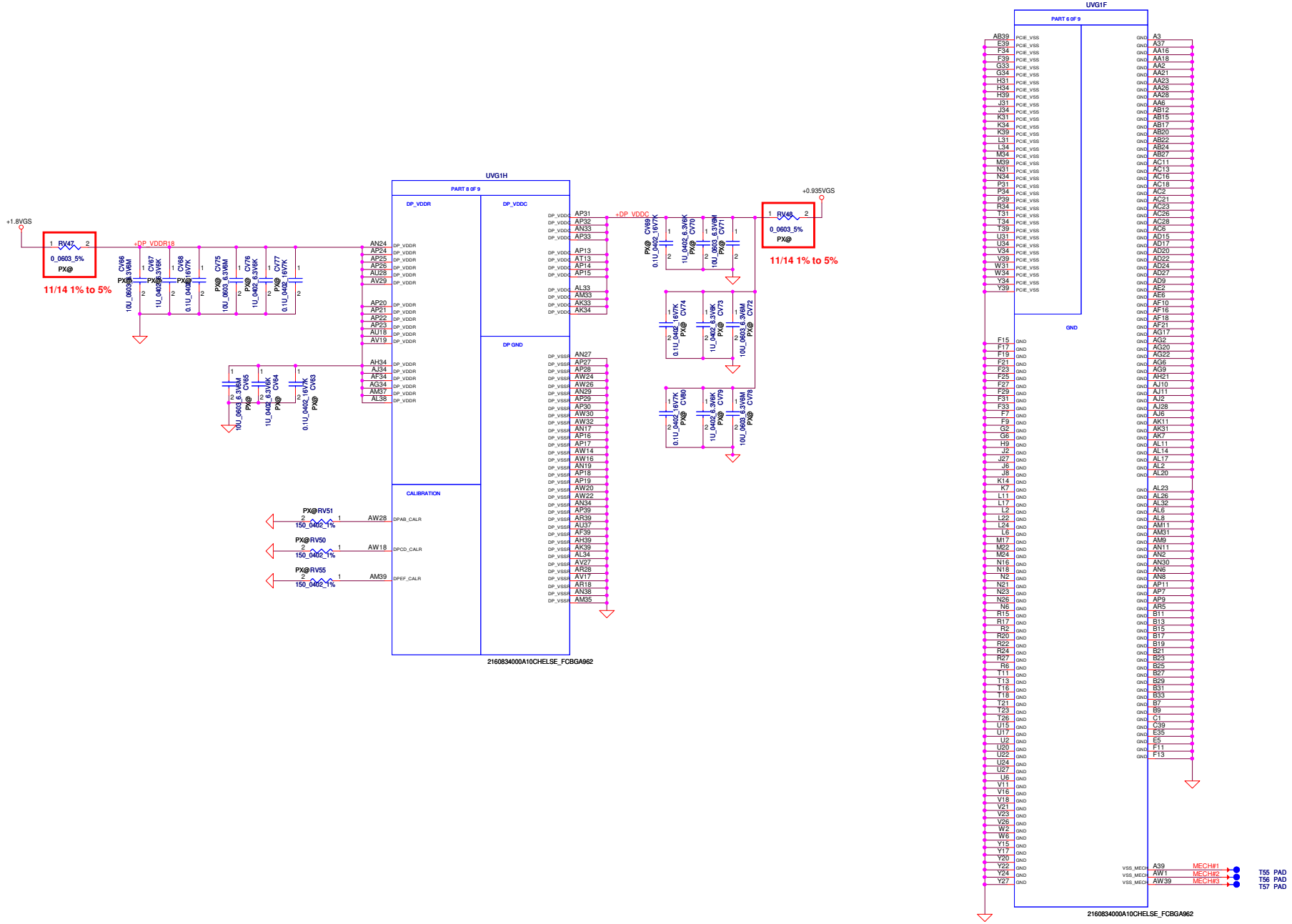
| Security Classification | Compal Secret Data | | |
|---|---|---|---|
| Issued Date | 2011/06/30 | Deciphered Date | 2013/06/30 |

Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_Power

Size: C | Document Number: QCL51 LA-8712P | Rev: 0.1

Date: Monday, November 28, 2011 | Sheet 17 of 56




| | | | |
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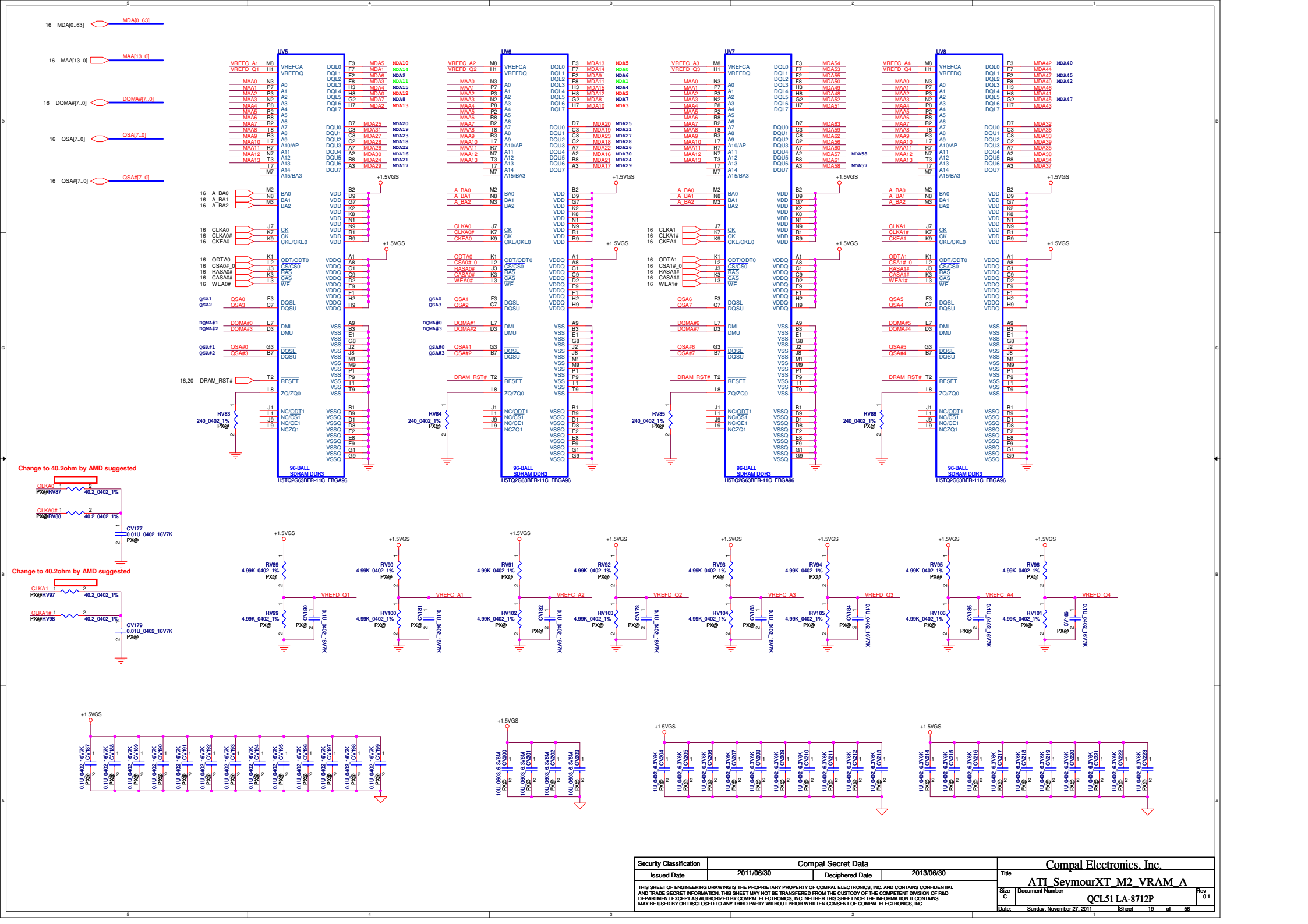
| | | | |
|---|---|---|---|
| Title | ATI_SetmourXT_M2_PWR_GND | | |
| Size C | Document Number QCL51 LA-8712P | | Rev 0.1 |
| Date: Monday, November 28, 2011 | Sheet 18 of 56 | | |




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/30 | Deciphered Date | 2013/06/30 |

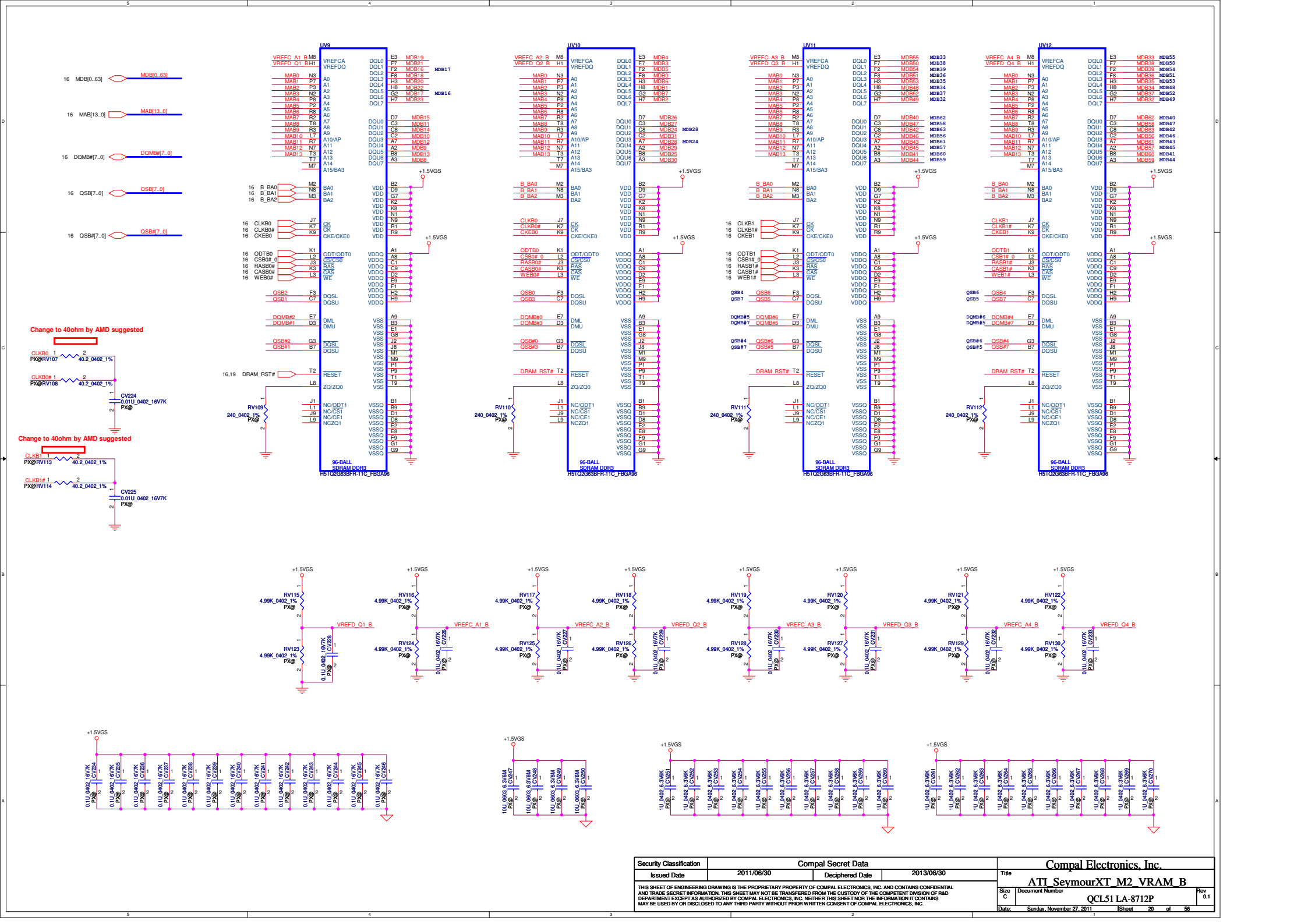


Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_VRAM_A

| Size | Document Number | Rev |
|---|---|---|
| C | QCL51 LA-8712P | 0.1 |

Date: Sunday, November 27, 2011 | Sheet 19 of 56




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/30 | Deciphered Date | 2013/06/30 |

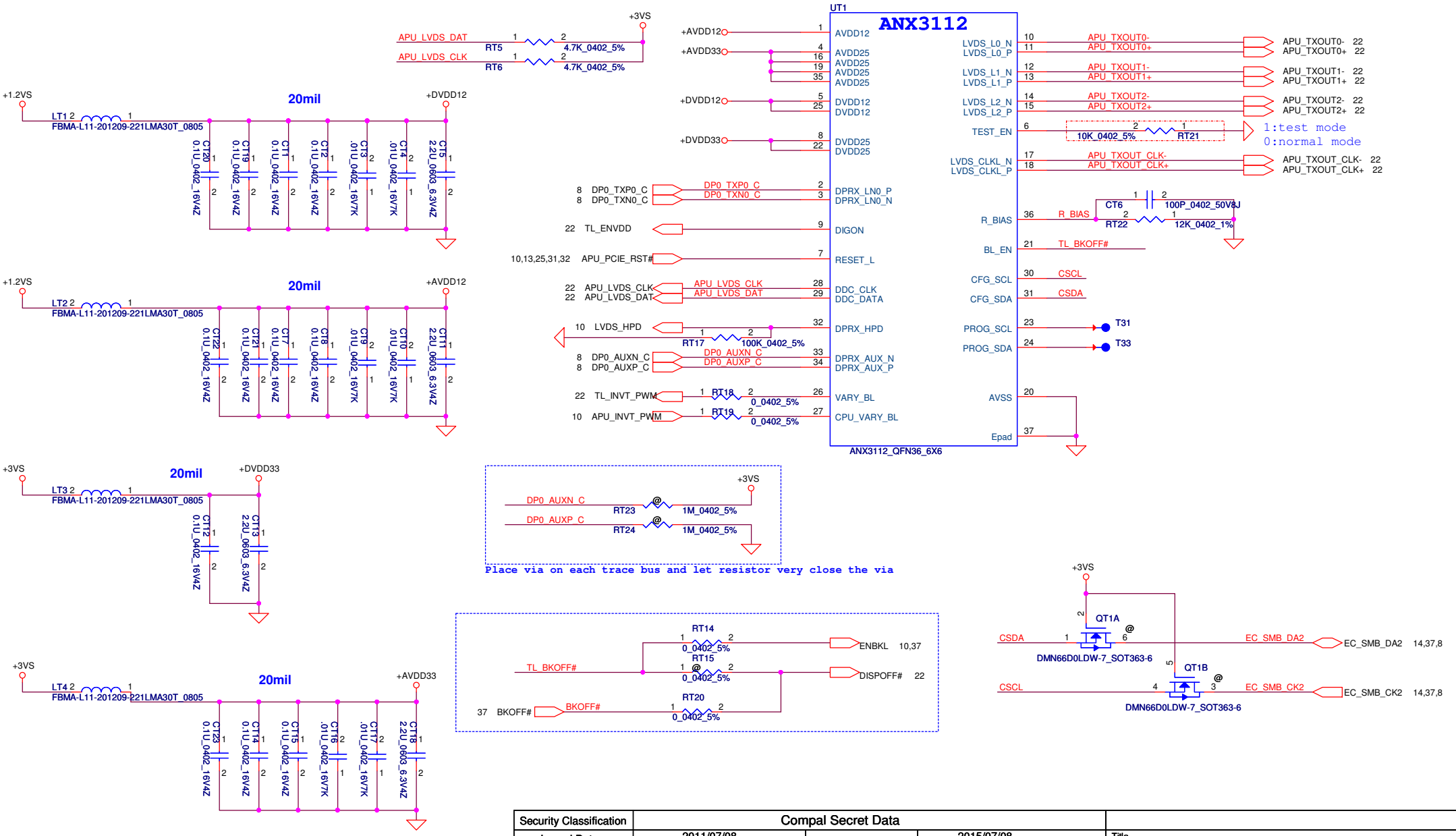


Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_VRAM_B

| Size | Document Number | Rev |
|---|---|---|
| C | QCL51 LA-8712P | 0.1 |

Date: Sunday, November 27, 2011 | Sheet 20 of 56




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/07/08 | Deciphered Date | 2015/07/08 |

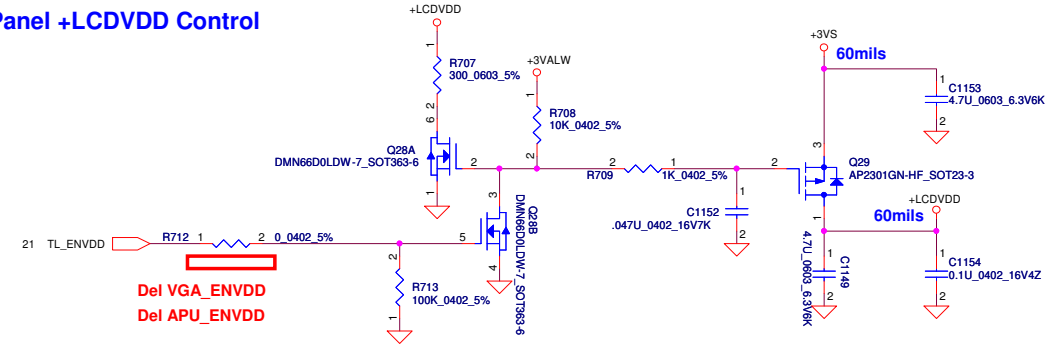


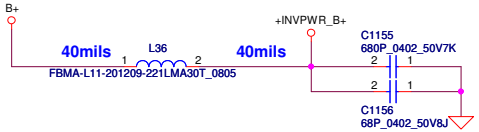
Title: *LVDS Translator - ANX3112X*

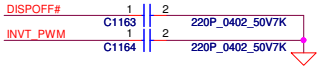
Size: B | Document Number: *QCL51 LA-8712P* | Rev: 0.1

Date: Monday, November 28, 2011 | Sheet 21 of 56

## Panel +LCDVDD Control



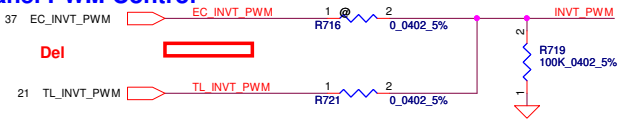



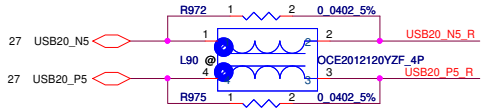



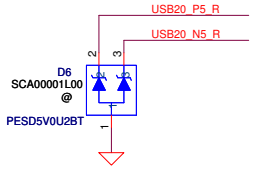

## Panel Backlight Control

Modify and change to page 21

## Panel PWM Control



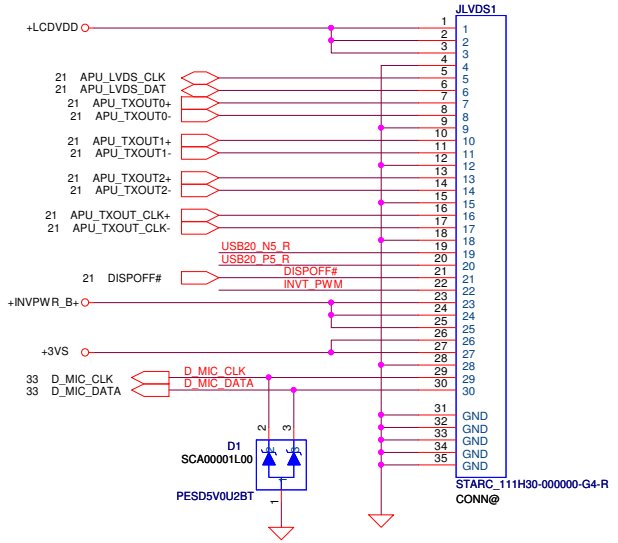





<Translator LVDS Output>


## LVDS Connector




no updated.

11/10 follow QCL50

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/07/08 | Deciphered Date | 2015/07/08 |



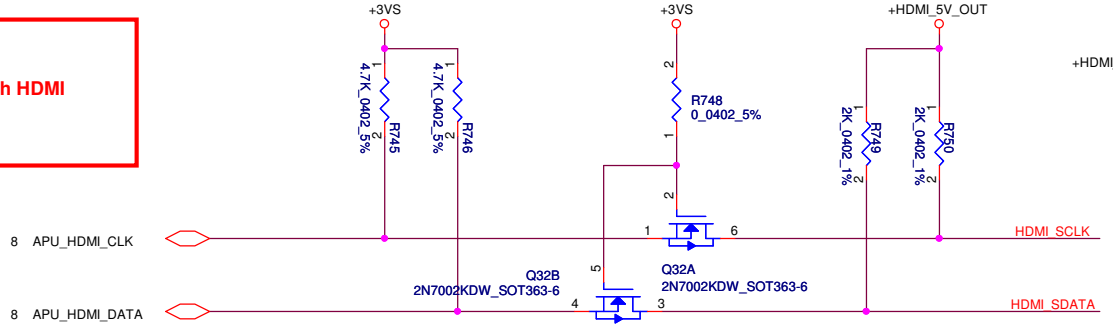
Compal Electronics, Inc.

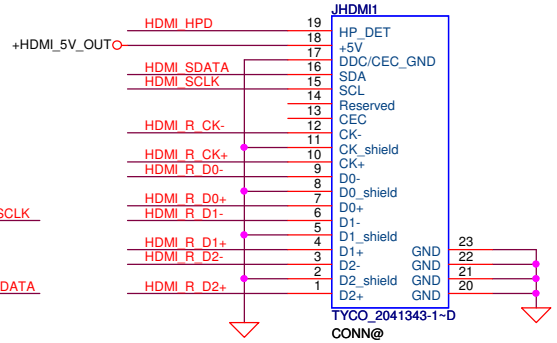
Title: LVDS/eDP Connector

| Size | Document Number | Rev |
|---|---|---|
| Custom | QCL51 LA-8712P | 0.1 |

Date: Monday, November 28, 2011 Sheet 22 of 56

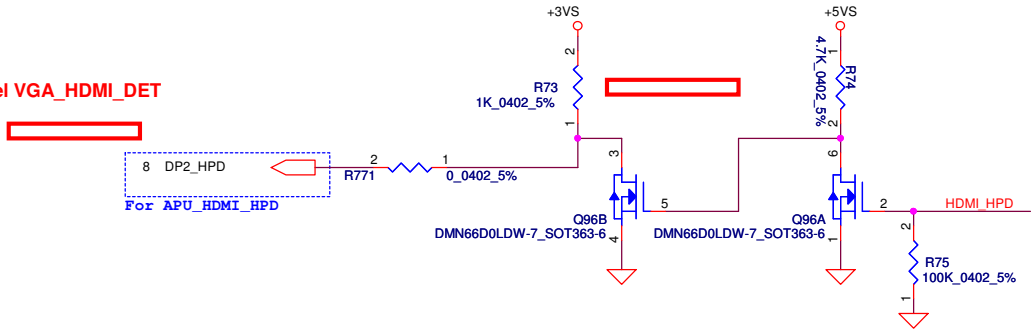
Combine with HDMI




11/05 update footprint.

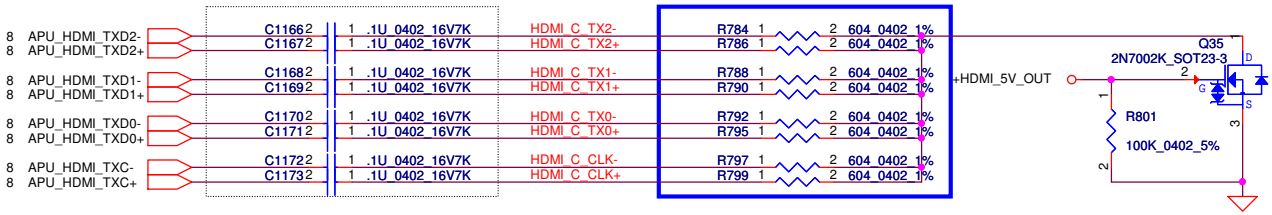
Del VGA_HDMI_DET

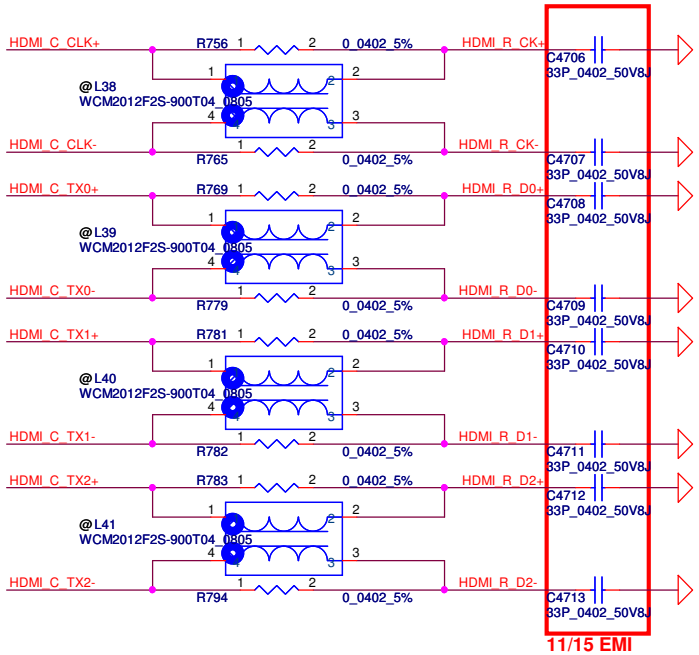



Close to HDMI conn

10/27 change to 604 ohm.

From APU




11/15 EMI
Near connector

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/07/08 | Deciphered Date | 2015/07/08 |

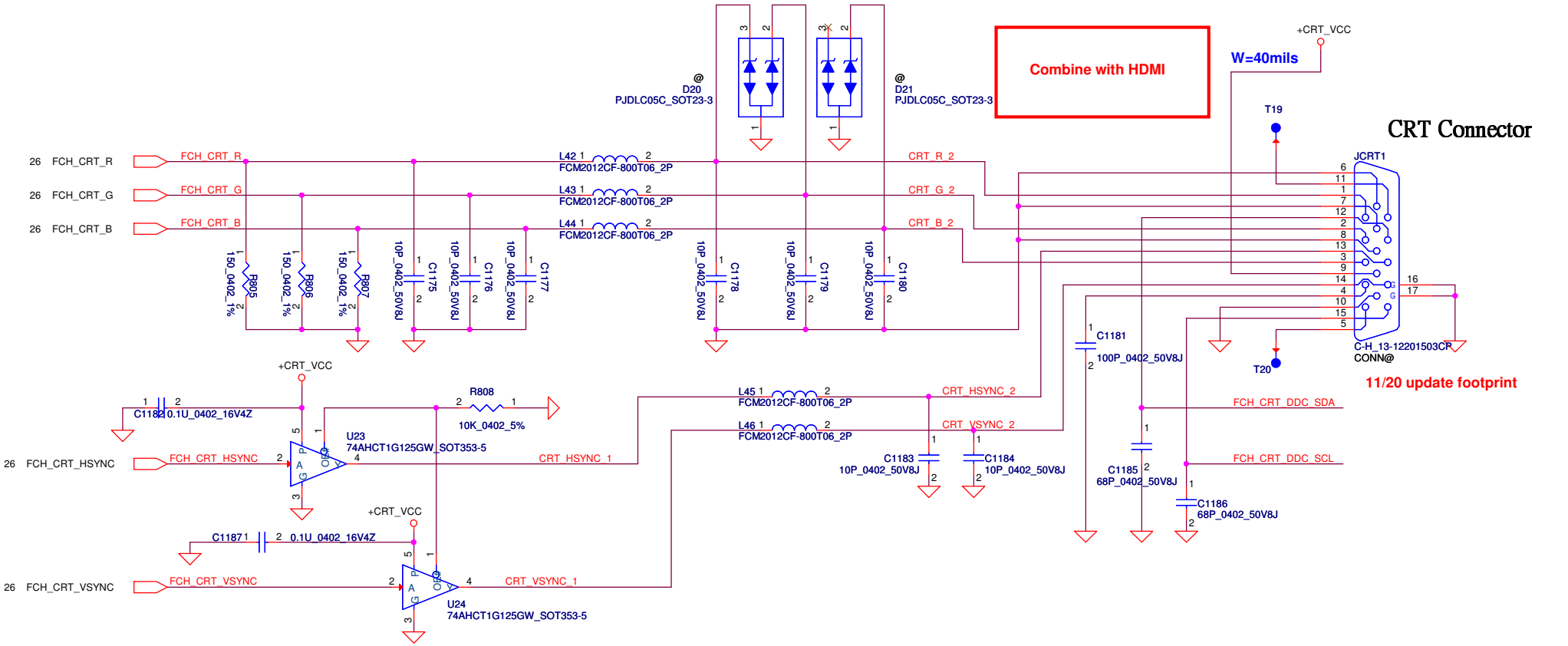


Compal Electronics, Inc.

Title: HDMI Connector

Size: B | Document Number: QCL51 LA-8712P | Rev: 0.1

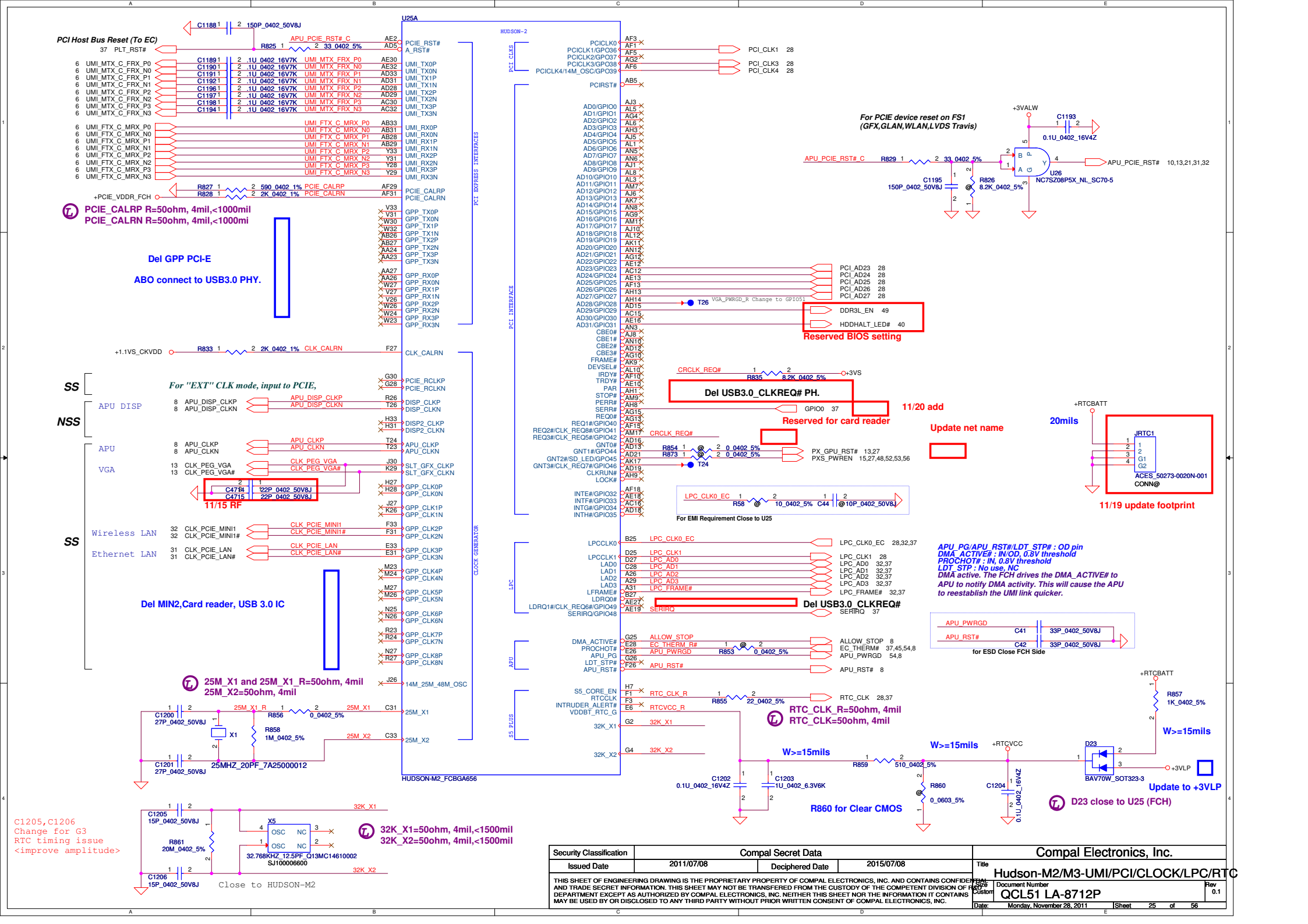
Date: Monday, November 28, 2011 | Sheet 23 of 56




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/07/08 | Deciphered Date | 2015/07/08 |



| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title: CRT Connector | | | |
| Size: B | Document Number: QCL51 LA-8712P | | Rev: 0.1 |
| Date: Monday, November 28, 2011 | Sheet 24 of 56 | | |




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/07/08 | Deciphered Date | 2015/07/08 |

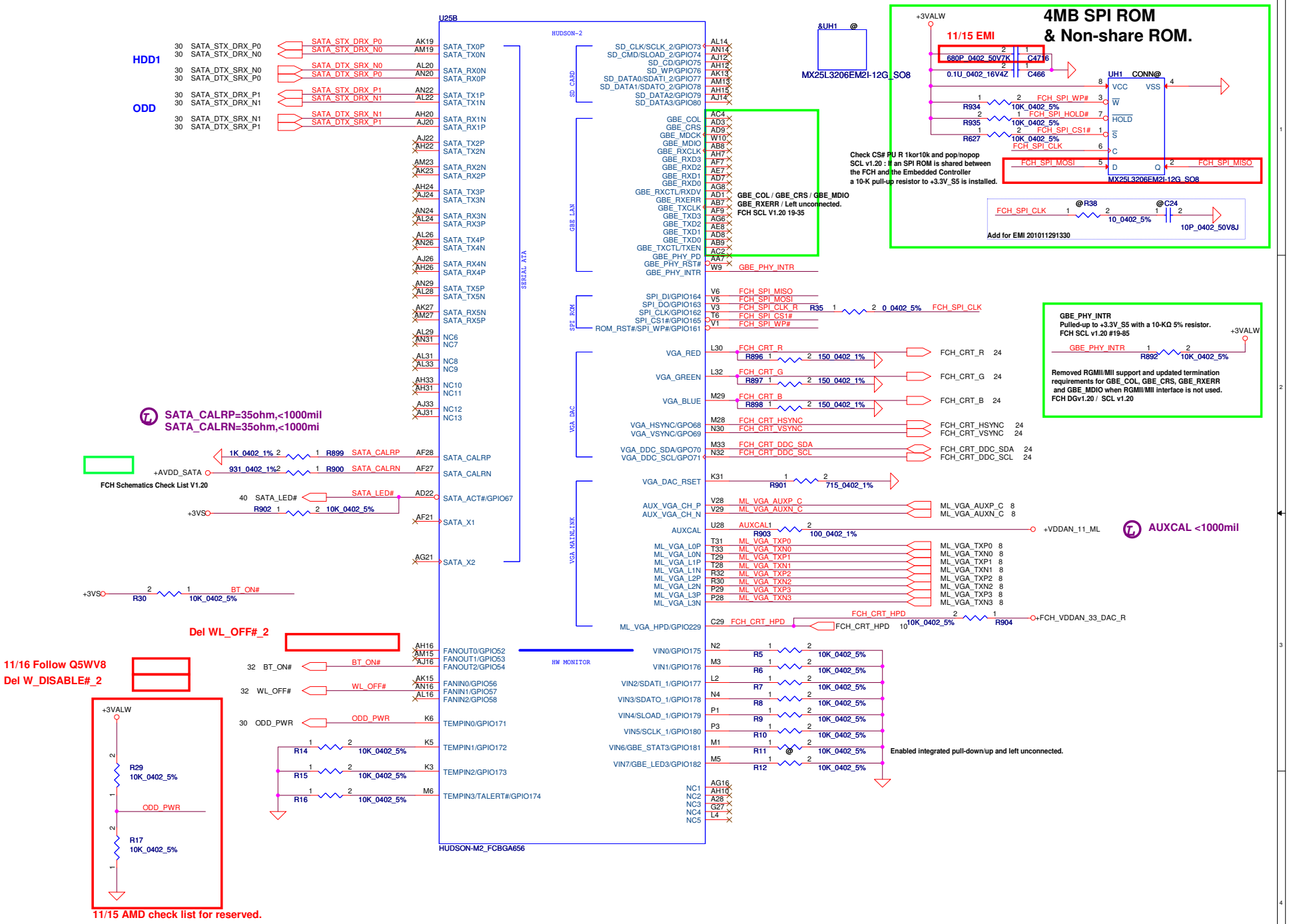


Compal Electronics, Inc.

Title: Hudson-M2/M3-UMI/PCI/CLOCK/LPC/RTC

| Size | Document Number | Rev |
|---|---|---|
| B25 Custom | QCL51 LA-8712P | 0.1 |

Date: Monday, November 28, 2011 | Sheet 25 of 56




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/07/08 | Deciphered Date | 2015/07/08 |



Compal Electronics, Inc.

Title: Hudson-M2/M3-SATA/GBE/HWM

| Size | Document Number | Rev |
|---|---|---|
| Custom | QCL51 LA-8712P | 0.1 |

Date: Monday, November 28, 2011 | Sheet 26 of 56

FCH_PCIE_RST# IS FOR PCIE DEVICES ON Hudson-M2/M3

Del FCH_PCIE_RST#

THERMTRIP:
Need level shift from +3VALW to +1.5V
Note: Ensure FCH internal pull-up resistor to +3.3V S5 is disabled to prevent leakage when APU is powered down.

SM bus 0-->S0 PWR domain
SM bus 1-->S5 PWR domain

FCH GEVENT (S5 domain) with isolation circuit to avoid leakage

Del Card det

Del MINI2_CLKREQ#

PC_BEEP use.

11/08 Reserved BIOS setting

11/15 ESD

Del SIMB output

33ohm termination resistor at CODEC side

Add USB_OC0#

Change GPIO fellow Pumori

Del FCH_GPIO187

Update net name

For FCH internal debug use

Del MINI2_CLKREQ# PH.

11/15 RF

Del FCH_GPIO187 R57 R55

DIS is High

DIS is High

| Project SKU ID | | |
|---|---|---|
| GPIO189 (use VGA) | L(NO) R44 | H(YES) R43 |
| GPIO190 (use PX) | L(NO) R46 | H(YES) R45 |
| GPIO188 | TBD | TBD |
| GPIO187 (Reserved) | | |

U25D

HUDSON-2

HUDSON-M2_FCBGA656

USB 2.0 port(Right-1)

USB 2.0 port(Left-2)

USB 2.0 port(Left-1)

Del USB port 9

Mini1-WLAN

Del USB port 7

Camera

USB port3-->USB port0

FP

USB 2.0 port(Right-2)

USBSS_CALRP=35ohm,<1000mil
USBSS_CALRN=35ohm,<1000mi

USB 3.0 port(Right-1)

USB 3.0 port(Left-2)

USB 3.0 port(Left-1)

For PCIE device reset on FS1
(GFX,GLAN,WLAN,LVDS Travis)

| Security Classification | Compal Secret Data | | |
|---|---|---|---|
| Issued Date | 2011/07/08 | Deciphered Date | 2015/07/08 |



Compal Electronics, Inc.

Title: Hudson-M2/M3-ACPI/USB/EC

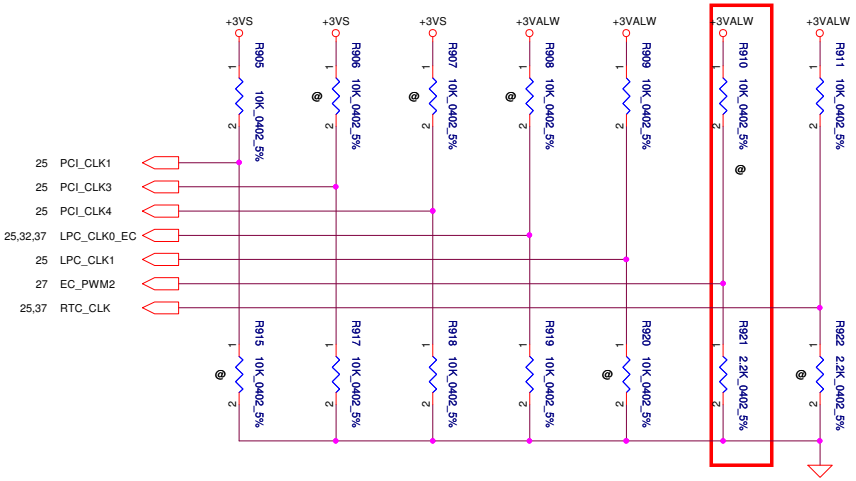
| Size | Document Number | Rev |
|---|---|---|
| C | QCL51 LA-8712P | 0.1 |

Date: Monday, November 28, 2011 Sheet 27 of 56

Change to SPI

## STRAP PINS

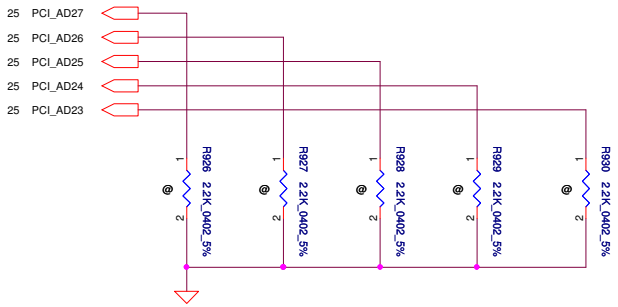
| | PCI_CLK1 | PCI_CLK3 | PCI_CLK4 | LPC_CLK0 | LPC_CLK1 | EC_PWM2 | RTC_CLK |
|---|---|---|---|---|---|---|---|
| PULL HIGH | ALLOW PCIE GEN2 DEFAULT | USE DEBUG STRAPS | NON_FUSION CLOCK MODE | EC ENABLED | CLKGEN ENABLED DEFAULT | LPC ROM DEFAULT | S5 PLUS MODE DISABLED DEFAULT |
| PULL LOW | FORCE PCIE GEN1 | IGNORE DEBUG STRAP DEFAULT | FUSION CLOCK MODE DEFAULT | EC DISABLED DEFAULT | CLKGEN DISABLE | SPI ROM | S5 PLUS MODE ENABLED |

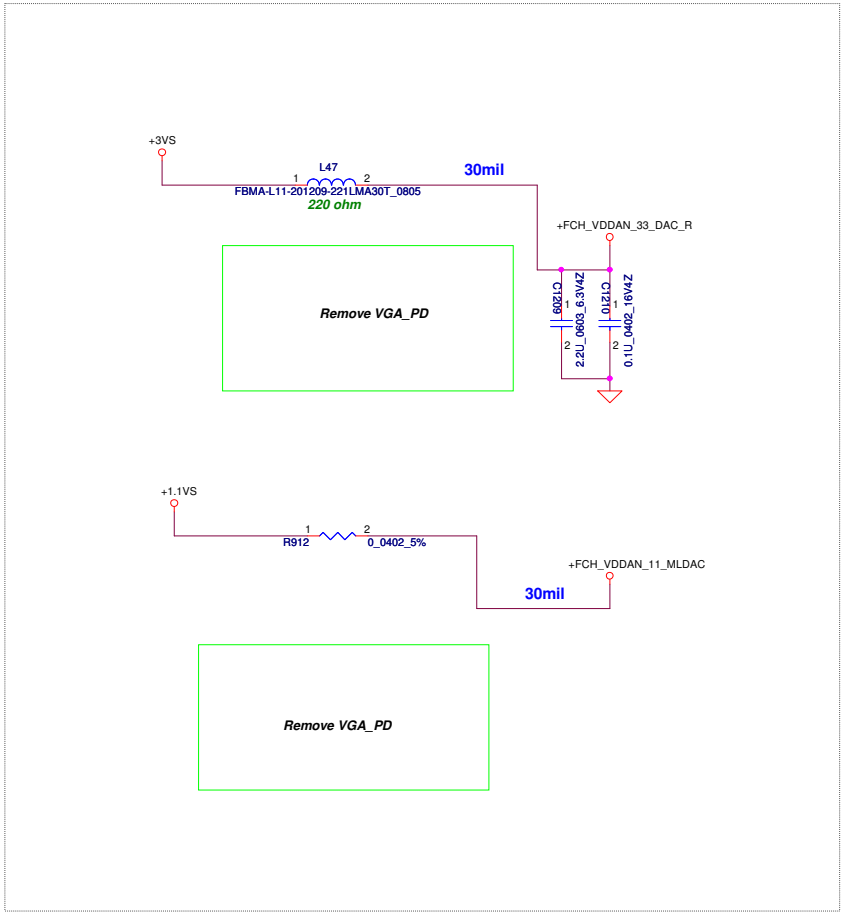



## DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

| | PCI_AD27 | PCI_AD25 | PCI_AD24 | PCI_AD23 |
|---|---|---|---|---|
| No external R | USE PCI PLL DEFAULT | Normal REFCLK termination DEFAULT | USE DEFAULT PCIE STRAPS DEFAULT | DISABLE PCI MEM BOOT DEFAULT |
| PULL LOW | BYPASS PCI PLL | Inverted REFCLK termination | USE EEPROM PCIE STRAPS | ENABLE PCI MEM BOOT |




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/07/08 | Deciphered Date | 2015/07/08 |

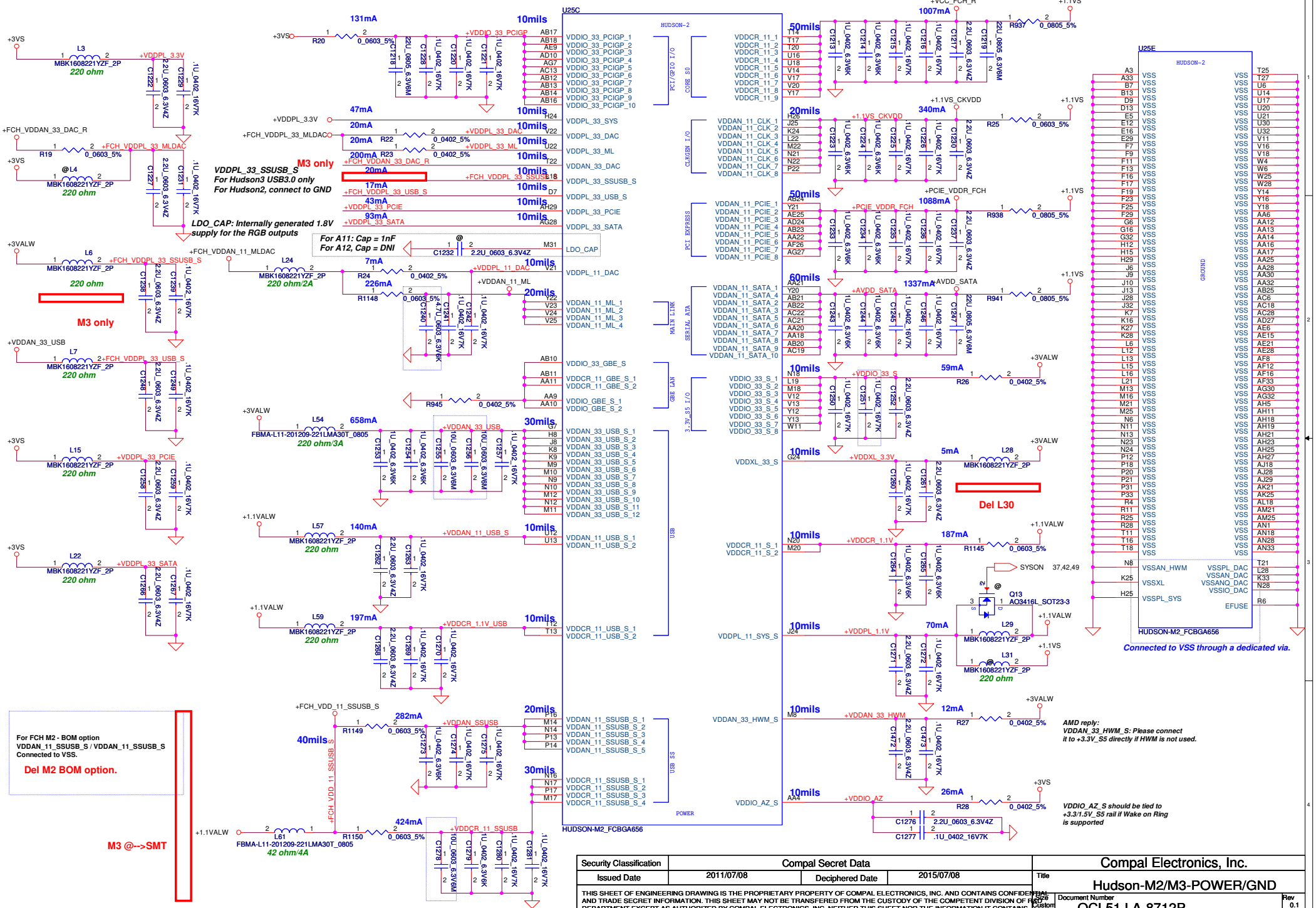


Compal Electronics, Inc.

Title: Hudson-M2/M3-STRAP

Size: B (5/25 Custom) | Document Number: QCL51 LA-8712P | Rev: 0.1

Date: Monday, November 28, 2011 | Sheet 28 of 56




| | | | |
|---|---|---|---|
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| Issued Date | 2011/07/08 | Deciphered Date | 2015/07/08 |

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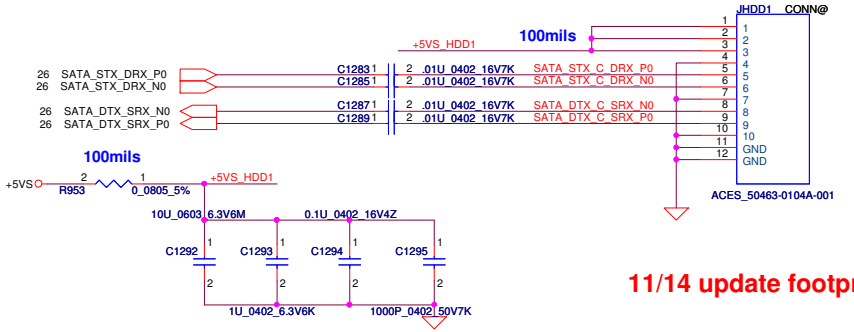
Compal Electronics, Inc.

Title: Hudson-M2/M3-POWER/GND

Size: Custom | Document Number: QCL51 LA-8712P | Rev: 0.1

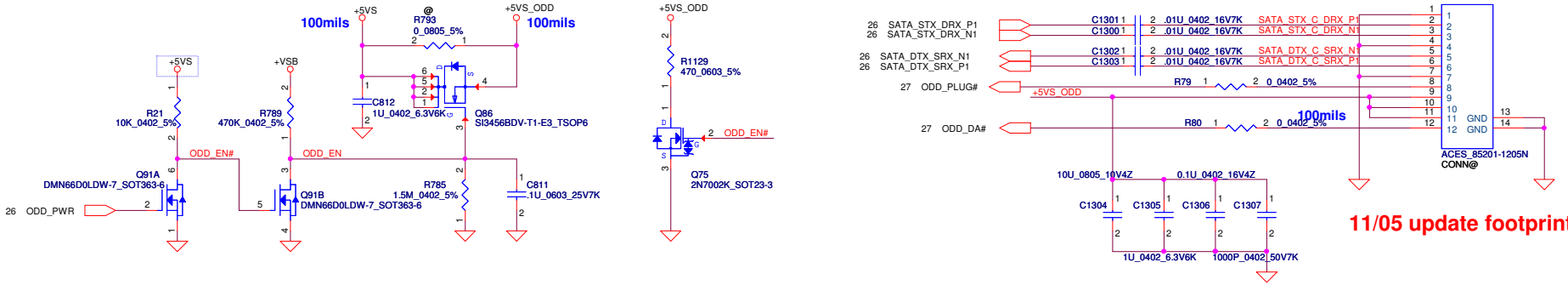
Date: Monday, November 28, 2011 | Sheet 29 of 56

# SATA HDD1 Conn.



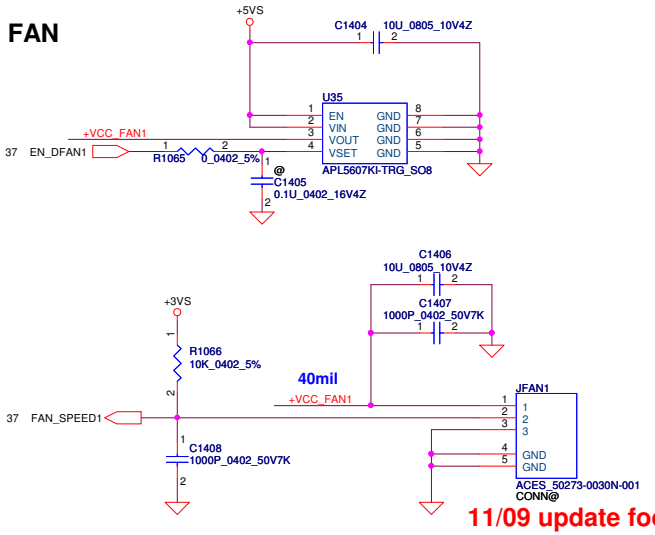

11/14 update footprint

# ODD conn



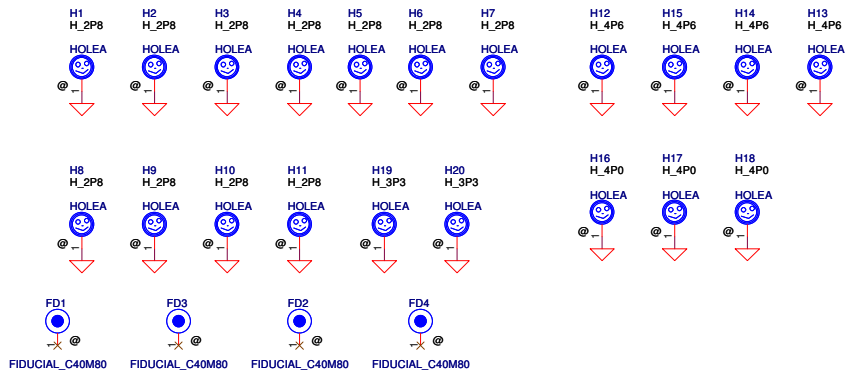

11/05 update footprint

# FAN




11/09 update footprint to VT.

# Screw Hole




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | Compal Electronics, Inc. |
| Issued Date | 2011/07/08 | Deciphered Date | 2015/07/08 |
| Title | HDD/ODD/FAN/SCREW | | |
| Size B | Document Number QCL51 LA-8712P | | Rev 0.1 |
| Date: Monday, November 28, 2011 | Sheet 30 of 56 | | |

W=60mils

W=60mils

+3VALW

RL3 0_1206_5%

QL1 AO3413L_SOT23-3

CL1 1U_0402_6.3V6K

+VSB

RL4 470K_0402_5%

EN_WOL

37 WOL_EN

QL2 SSM3K7002FU_SC70-3

RL5 1.5M_0402_5%

CL9 0.1U_0603_25V7K

+LAN_VDD_3V3

1.5A

These caps close to U1: Pin 11,12,39,58,63,64

CL2 CL3 CL4 CL5 CL6 CL7 CL8 0.1U_0402_16V7K

CL8 10U_0603_6.3V6M

Note:
1.The rise time of +LAN_VDD_3V3 must >1ms and <100ms for the internal LDO.

## Modify by Project

JREAD1

+CR_VDD_3V3

SD_CMD_R SD_CLK_R SD_D0_R SD_D1_R SD_D2_R SD_D3_R SD_WP SD_CD#

CMD VSS VDD CLK VSS DAT0 DAT1 DAT2 CD/DAT3 WP SW CD SW GND SW GND SW GND GND

T-SOL_156-1000302601_NR

CONN@

11/22 NPTH

CL37 0.1U_0402_16V7K CL38 4.7U_0603_6.3V6K

CL37, CL38 close to CR socket

11/05 update footprint

Need to check RL6,RL7,RL8 Option

Close to Chip

+LAN_VDD_3V3

RL6 10K_0402_5%

37 EC_PME#

RL7 0_0402_5%

27,32 FCH_PCIE_WAKE#

RL8 0_0402_5%

ISOLATEB LANWAKEB

Change net name from PLT_RST# to APU_PCIE_RST#

25 CLK_PCIE_LAN CLK_PCIE_LAN

25 CLK_PCIE_LAN# CLK_PCIE_LAN#

10,13,21,25,32 APU_PCIE_RST# LAN_CLKREQ# R

6 PCIE_DTX_C_FRX_P0 CL11 0.1U_0402_16V7K PCIE_DTX_FRX_P0

6 PCIE_DTX_C_FRX_N0 CL12 0.1U_0402_16V7K PCIE_DTX_FRX_N0

6 PCIE_FTX_C_DRX_P0 PCIE_FTX_C_DRX_P0

6 PCIE_FTX_C_DRX_N0 PCIE_FTX_C_DRX_N0

UL1

Power Management/Isolation

ISOLATEB LANWAKEB

PCI-Express

REFCLK_P REFCLK_N PERSTB CLKREQB HSOP HSON HSIP HSIN

EEPROM(TWSI)

SDA SCL/LED_CR

Transceiver Interface

MDIP0 MDIN0 MDIP1 MDIN1 MDIP2 MDIN2 MDIP3 MDIN3

Clock

XTLI XTLO CKXTAL1 CKXTAL2

Regulator and Reference

REGOUT ENSWREG_H VDDREG VDDREG RSET

LEDs

LED0 LED1 LED3

Card Reader

SD_D0/MS_D7/xD_D5 SD_D1/MS_CLK/xD_D6 SD_D2/xD_D7 SD_D3/MS_D2/xD_D2 SD_D4/xD_WE# SD_D5/xD_CE# SD_D6/MS_INS#/xD_RE# SD_D7/xD_RDY SD_CLK/MS_D3/xD_D4 SD_CMD/MS_D6/xD_D3 SD_WP/MS_D1/xD_WP# SD_CD#/MS_D5/xD_ALE MS_BS/xD_CLE MS_D4/xD_D0 MS_D0/xD_D1 XD_CD#

SD_D0 SD_D1 SD_D2 SD_D3 SD_CLK SD_CMD SD_WP_R SD_CD# R

GPIO

DVDD33 AVDD33 DVDD10 AVDD10 EVDD10 Card_3V3 VDD33/18

GND GND GND9(Exposed Pad)

PN : SA00005B400

RTL8411-CG_QFN64_9X9

+LAN_VDD_3V3 +LAN_VDD_1V0 +CR_VDD_3V3 +LAN_EVDD10 +VDD33_18

RL18 2.49K_0402_1%

LAN_LED0 LAN_LED1

+CR_VDD_3V3

RL31 100K_0402_5%

RL32 100K_0402_5%

SD_WP_R

QL3B 2N7002KDWH_SOT363-6

SD_WP

Follow QCL50

RL11 RL12 RL13 RL14 RL15 RL16 0_0402_5%

SD_D0 SD_D1 SD_D2 SD_D3 SD_CMD SD_CLK

SD_D0_R SD_D1_R SD_D2_R SD_D3_R SD_CMD_R SD_CLK_R

CL10 @ 5P_0402_50V8C

## EMI-ESD

LAN_ACTIVITY# CL13 470P_0402_50V8J

LINK_100_1000# CL14 470P_0402_50V8J

DL2 @ PESD5V0U2BT

LAN_ACTIVITY# LINK_100_1000#

+LAN_VDD_3V3

RL33 100K_0402_5%

RL30 100K_0402_5%

SD_CD# R

QL3A 2N7002KDWH_SOT363-6

SD_CD#

## Modify by Project

Amber

LEDL2 HT-110UD_1204

LAN_LED0 RL1 510_0402_5% LAN_ACTIVITY#

White

LEDL1 LTW-110DC5-C_WHITE

Close to Chip

LAN_LED1 RL2 510_0402_5% LINK_100_1000#

Check power rail

JLAN1 @ SANTA_130460-1

RJ45_TX3- RJ45_TX3+ RJ45_RX1- RJ45_TX2- RJ45_TX2+ RJ45_RX1+ RJ45_TX0- RJ45_TX0+

PR4- PR4+ PR2- PR3- PR3+ PR2+ PR1- PR1+ GND GND GND GND GND GND

11/15 Update footprint

11/16 Update footprint for DB

+3VS RL19 1K_0402_5% ISOLATEB

RL20 15K_0402_5%

27P_0402_50V8J CL20 CL21

RL21 0_0402_5% XTLI XTLO

YL1 25MHZ_12PF_X5H025000FC1H-H

27P_0402_50V8J

+LAN_VDD_1V0

RL25 0_0603_5%

+LAN_EVDD10

CL22 0.1U_0402_16V7K CL23 1U_0402_6.3V6K

Close to Pin29

+LAN_VDD_1V0

CL24 CL25 CL26 CL27 CL28 0.1U_0402_16V7K

Place each cap. close Pin 3, 8 , 41 , 52 ,61

VDD33/18 for SD UHS Mode Power

+VDD33_18

CL16 0.1U_0402_10V7K

CL17 4.7U_0603_6.3V6K

CL18 0.1U_0402_10V7K

CL19 4.7U_0603_6.3V6K

CL16,CL17 Close to Pin33

CL18,CL19 close to Pin53

CL15 0.1U_0402_10V7K

RL22 0_0402_5% ENSWREG

RL23 0_0402_5%

+LAN_VDD_3V3

3.3V : Enable Switching Regulator
(Default,For Power Efficiency)
0V : Enable LDO Regulator

## Switching Regulator Circuit

SHI0000AA00

LL1 2.2UH +-5% NLC252018T-2R2J-N DELTA_1008HC-472EJFS-A_2P

W=60mils

+LAN_SROUT1.0V +LAN_VDD_1V0

CL29 4.7U_0603_6.3V6K CL30 0.1U_0402_16V7K

The trace length from LL1 to Pin 48 (REGOUT) and from CL29, CL30 to Lx must be within 200 mils.

+LAN_VDD_3V3

RL24 0_0603_5% +LAN_VDDREG

CL35 4.7U_0603_6.3V6K CL36 0.1U_0402_16V7K

Close to Pin46,47

TS1

TD1+ TD1- TDCT1 TDCT2 TD2+ TD2- TD3+ TD3- TDCT3 TDCT4 TD4+ TD4-

TX1+ TX1- TXCT1 TXCT2 TX2+ TX2- TX3+ TX3- TXCT3 TXCT4 TX4+ TX4-

LAN_MDIP0 LAN_MDIN0 +V_DAC +V_DAC LAN_MDIP1 LAN_MDIN1 LAN_MDIP2 LAN_MDIN2 +V_DAC +V_DAC LAN_MDIP3 LAN_MDIN3

RJ45_TX0+ RJ45_TX0- RJ45_RX1+ RJ45_RX1- RJ45_TX2+ RJ45_TX2- RJ45_TX3+ RJ45_TX3-

350UH_NA0069RLF

SP050006Y00

CL31 0.01U_0402_16V7K

CL39 0.1U_0402_16V7K

11/15 EMI

RL26 RL27 RL28 RL29 75_0402_5%

CL32 SE167100J80 10P_1808_3KV

CL33 0.1U_0402_16V4Z

CL34 4.7U_0603_6.3V6K

DL1 SCA00001L00 @ PESD5V0U2BT

LL2 100UH_SSC0301101MCF_0.18A_20%

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/29 | Deciphered Date | 2011/06/29 |



Compal Electronics, Inc.

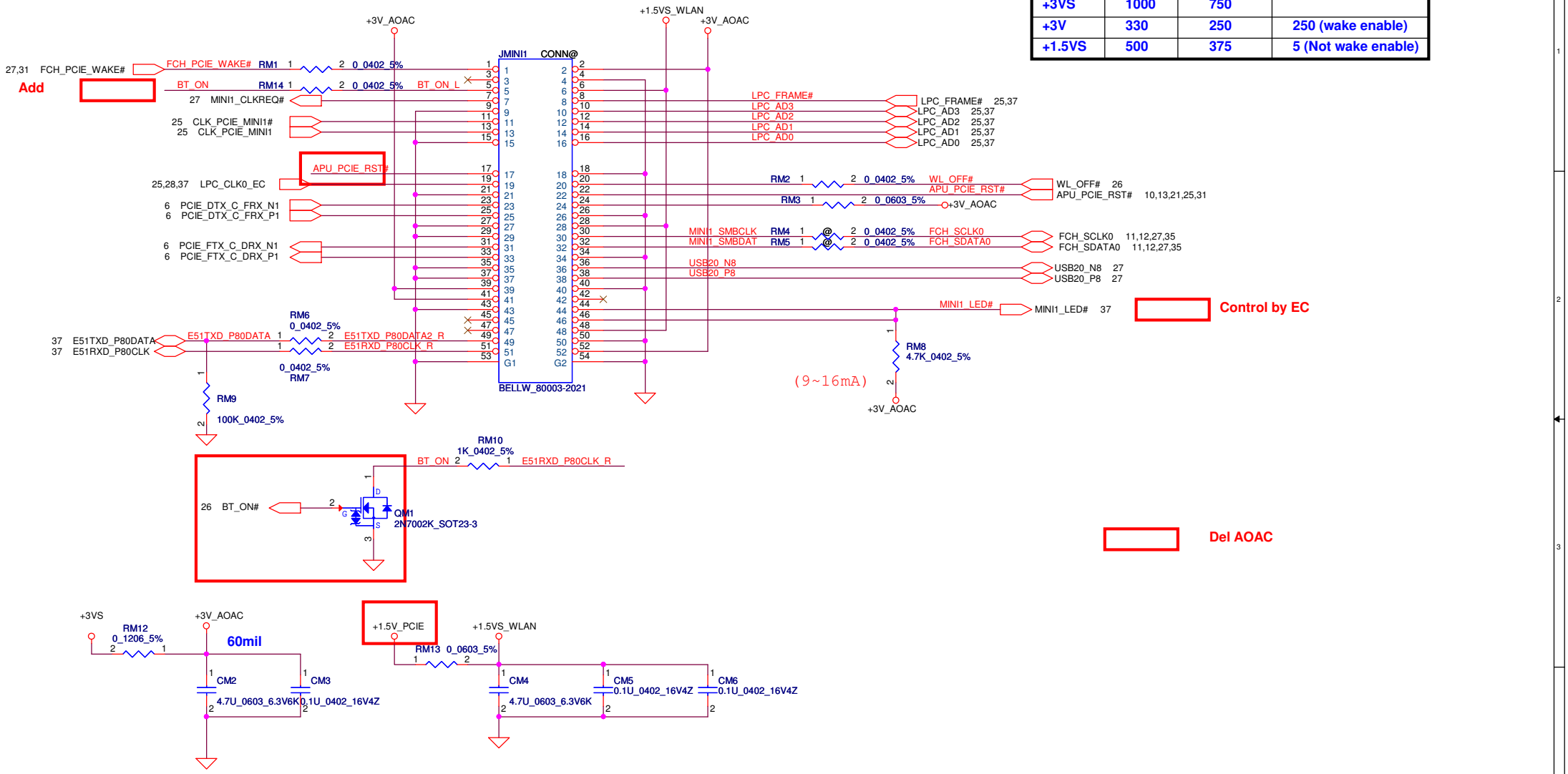
Title: LAN&CardReader Realtek RTL8411

Size: Document Number: QCL51 LA-8712P Rev: 0.1

Date: Monday, November 28, 2011 Sheet 31 of 56

# WLAN

| Mini Card Power Rating | | | |
|---|---|---|---|
| Power | Primary Power (mA) | | Auxiliary Power (mA) |
| | Peak | Normal | Normal |
| +3VS | 1000 | 750 | |
| +3V | 330 | 250 | 250 (wake enable) |
| +1.5VS | 500 | 375 | 5 (Not wake enable) |




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/07/08 | Deciphered Date | 2015/07/08 |



Compal Electronics, Inc.

Title: MINI1 CARD (WLAN) / MINI2 CARD (Option)

| Size | Document Number | Rev |
|---|---|---|
| B | QCL51 LA-8712P | 0.1 |

Date: Monday, November 28, 2011 Sheet 32 of 56

Notes:
Keep PVDD supply and speaker traces routed on the DGND plane.
Keep away from AGND and other analog signals

RA2 0805-->0603

Place AVDD ,PVDD,and DVDD cap close to Codec (UA5)

11/15 EMI near UA5

11/16 vendor review

Place C208 close to Codec

CA8,CA10 near UA5 PIN45
CA9,CA21 near UA5 PIN39

External MIC
Combo jack
Headphone

SPK

C209,C210,CA87,CA89 close to Codec (UA5)

PLACE CLOSE TO UA5 PIN 13

If Sense_A total length is greater than 6 inches, chagne C12 to 0.1uF

If Sense_B is un-used, then pull high Sense_B to AVDD by 10Kohm resistor

PLACE CLOSE TO UA5 PIN 14

11/15 modified

Del AOAC

Close to Audio Codec (UA5)

Need confirmed.

11/15 EMI

RA53 need under or near UA5

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/29 | Deciphered Date | 2011/06/29 |

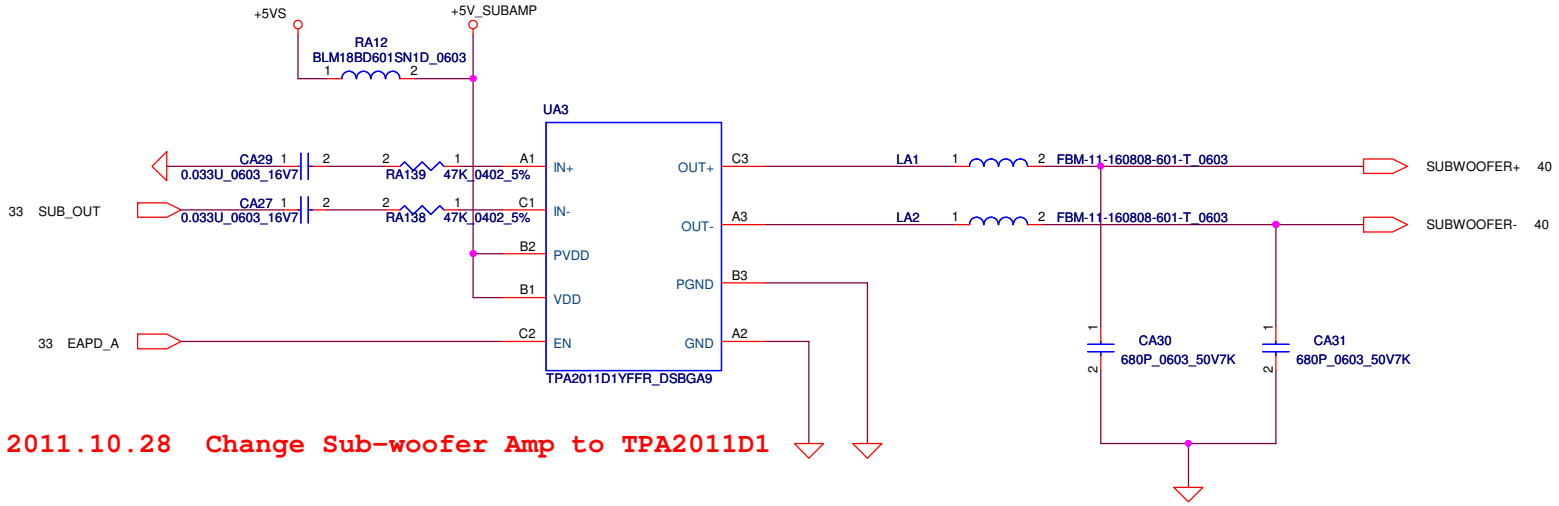


Compal Electronics, Inc.

Title: Audio IDT 92HD91

Size: Custom | Document Number: LA-8551P | Rev: 0.1

Date: Monday, November 28, 2011 | Sheet 33 of 56




2011.10.28 Change Sub-woofer Amp to TPA2011D1

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/29 | Deciphered Date | 2011/06/29 |



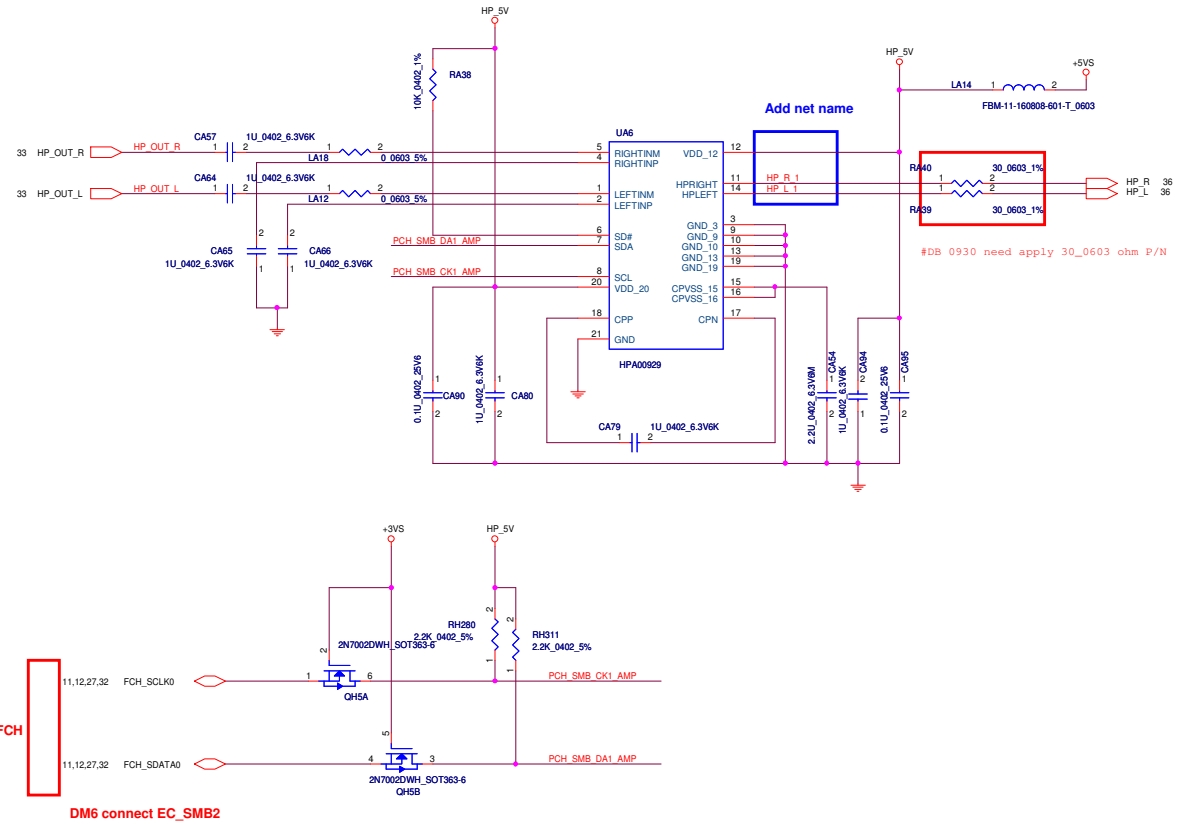
Compal Electronics, Inc.

Title: Audio Woofer Amplifier

Size: B | Document Number: LA-8551P | Rev: 0.1

Date: Monday, November 28, 2011 | Sheet 34 of 56

# Headphone amplifier

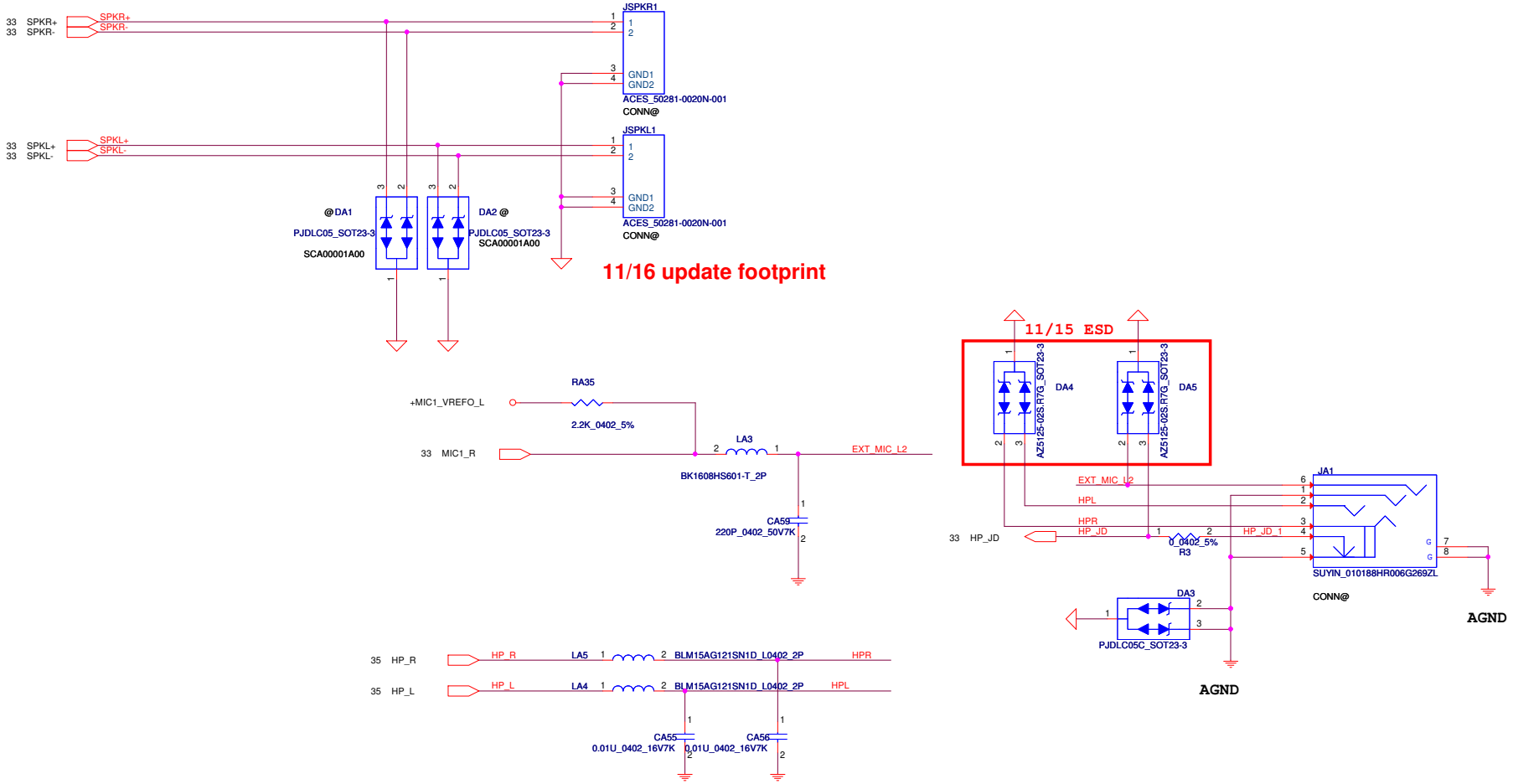



| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/29 | Deciphered Date | 2011/06/29 |



| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title: Audio SPK/HP Amplifier | | | |
| Size: Custom | Document Number: LA-8551P | | Rev: 0.1 |
| Date: Monday, November 28, 2011 | Sheet 35 of 56 | | |

# SPK conn




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2009/04/07 | Deciphered Date | 2012/10/21 |

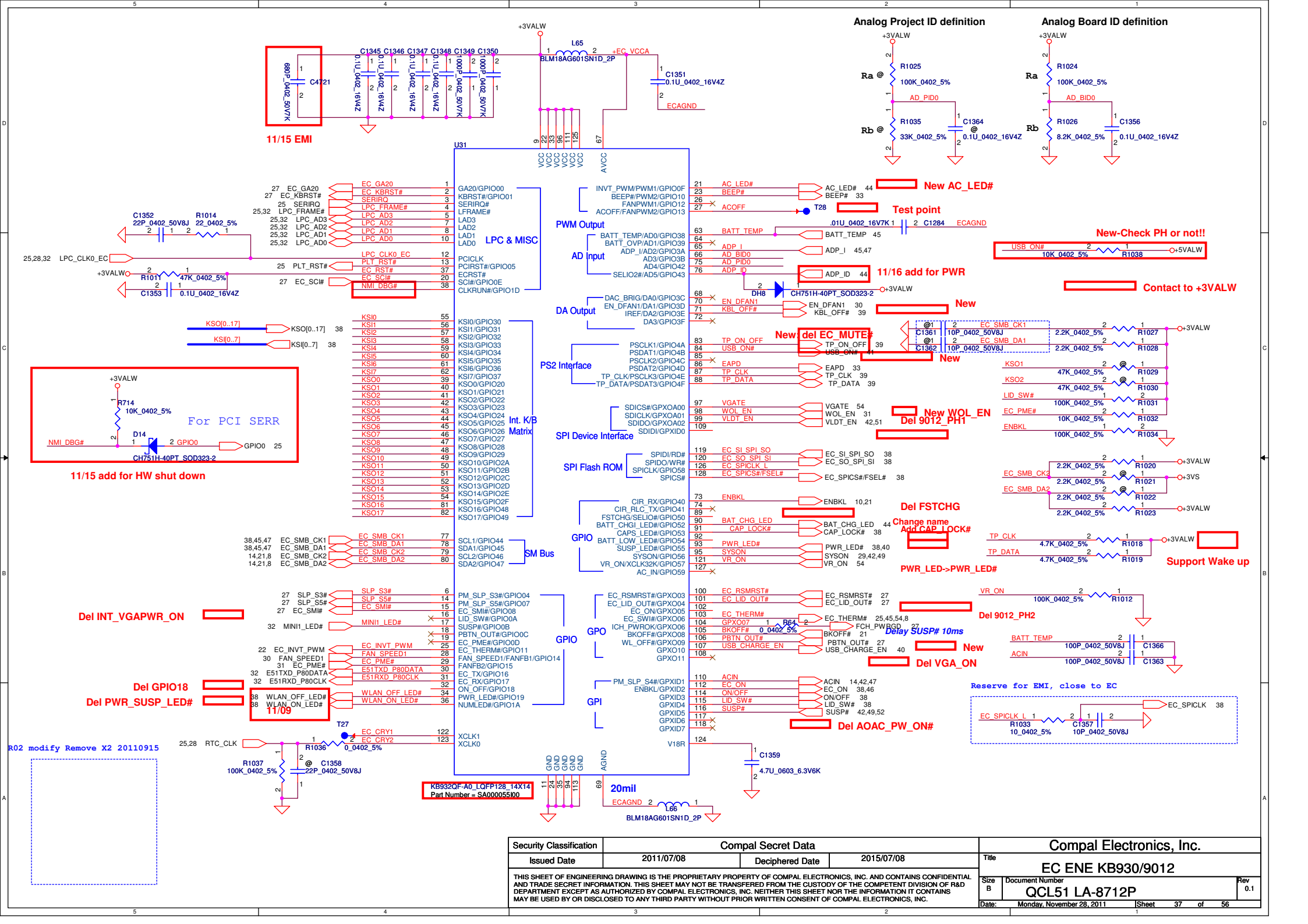


**Compal Electronics, Inc.**

Title: Audio SPK Conn/Jack/MIC

| Size | Document Number | Rev |
|---|---|---|
| Custom | QCL51 LA-8712P | 0.1 |

Date: Monday, November 28, 2011 Sheet 36 of 56




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/07/08 | Deciphered Date | 2015/07/08 |



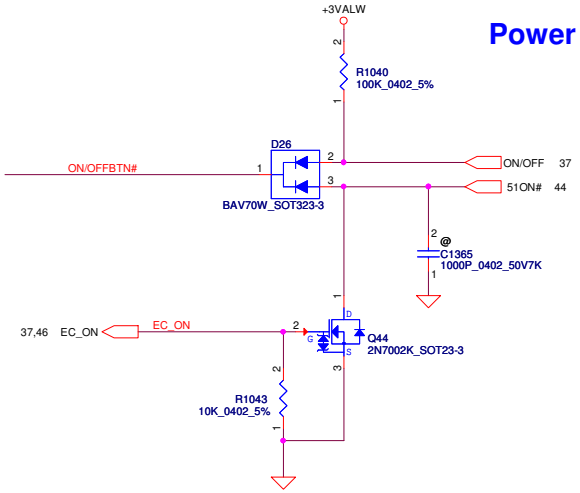
Compal Electronics, Inc.

Title: EC ENE KB930/9012

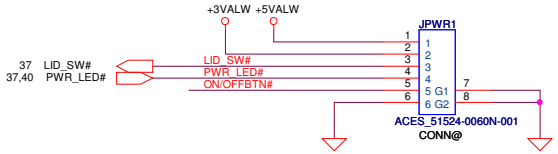
Size: B | Document Number: QCL51 LA-8712P | Rev: 0.1

Date: Monday, November 28, 2011 | Sheet 37 of 56

## Power Button



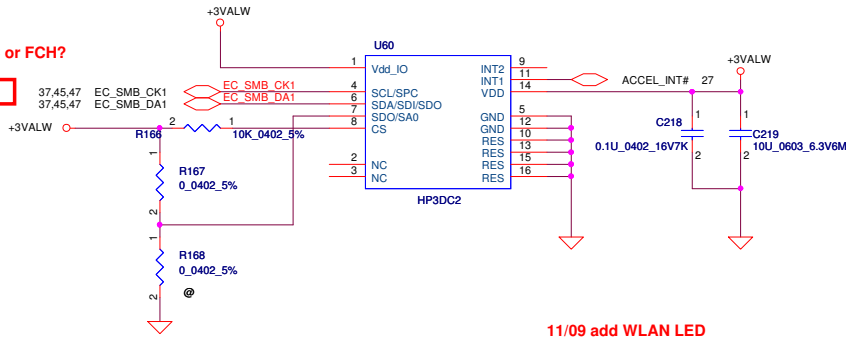

## POWER/B



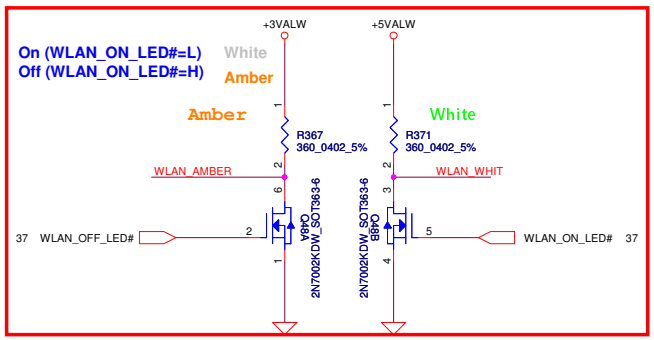

**11/05 update footprint**

## ACCELEROMETER

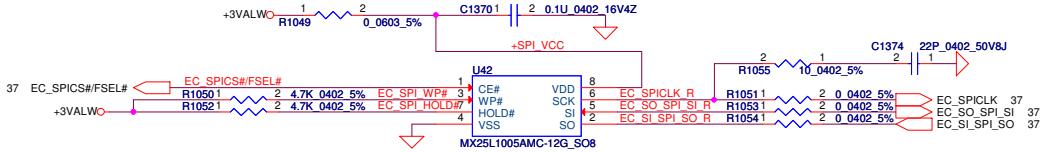
EC or FCH?



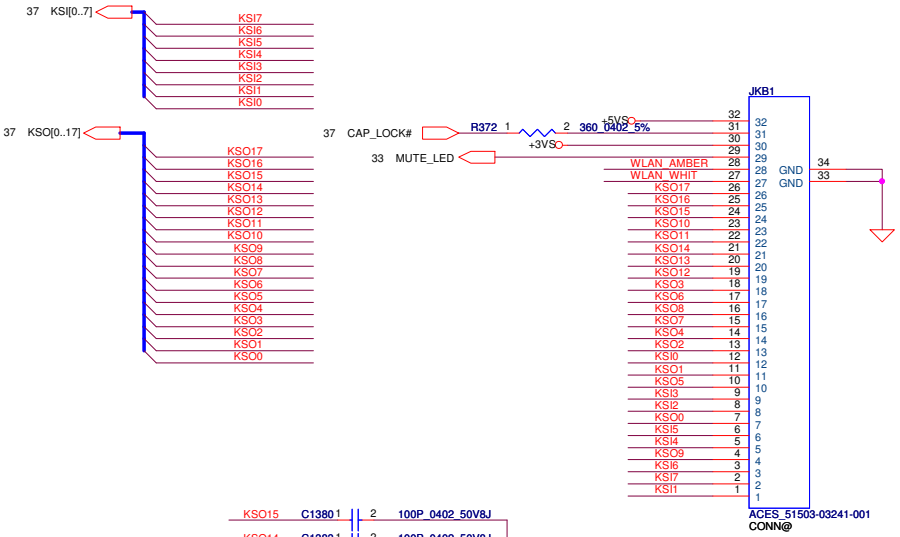

**11/09 add WLAN LED**

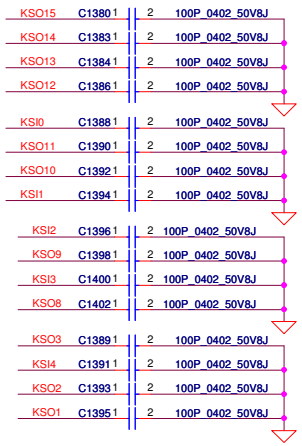



## EC BIOS ROM



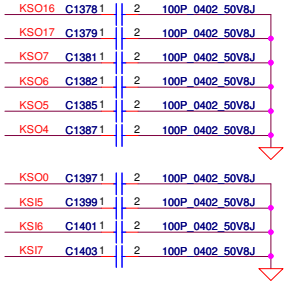

## KB conn




**11/05 update footprint**

**KSO16 and KSO17**

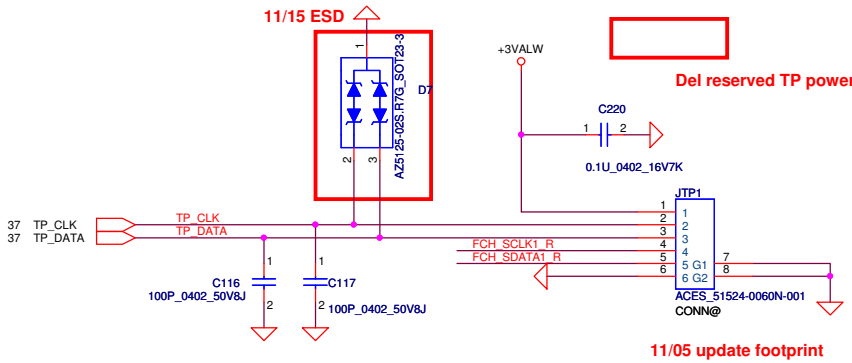



| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | Compal Electronics, Inc. |
| Issued Date | 2011/07/08 | Deciphered Date | 2015/07/08 |



| | | | |
|---|---|---|---|
| Title | BIOS, I/O Port & K/B CONN/TP CONN/PBTN | | |
| Size B | Document Number QCL51 LA-8712P | | Rev 0.1 |
| Date: Monday, November 28, 2011 | Sheet 38 of 56 | | |

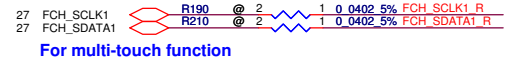
## TP Conn




Del reserved TP power control

11/05 update footprint

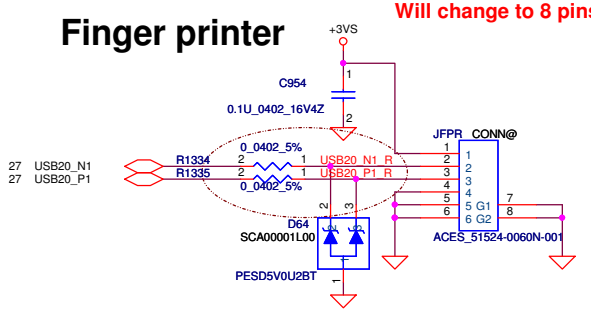
FCH use SMBus 1??




For multi-touch function

## Finger printer

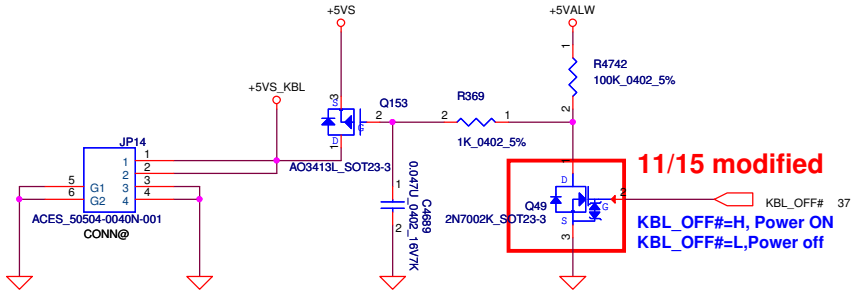
Will change to 8 pins




## WLAN ON/OFF LED

11/09 Change to KB connector

## Keyboard backlight Conn




11/15 modified

KBL_OFF#=H, Power ON

KBL_OFF#=L,Power off

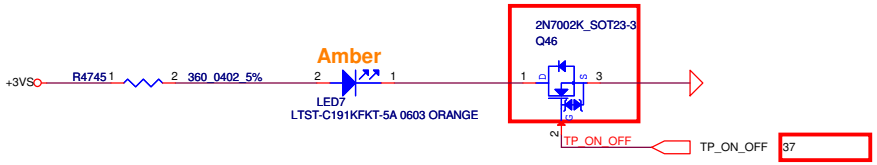
11/05 update footprint

## AOAC power control

Del AOAC

## T/P On/Off LED

11/15 modified




Amber

EC pin

## Mute On/Off LED

11/09 Change to KB connector

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/07/08 | Deciphered Date | 2015/07/08 |



Compal Electronics, Inc.

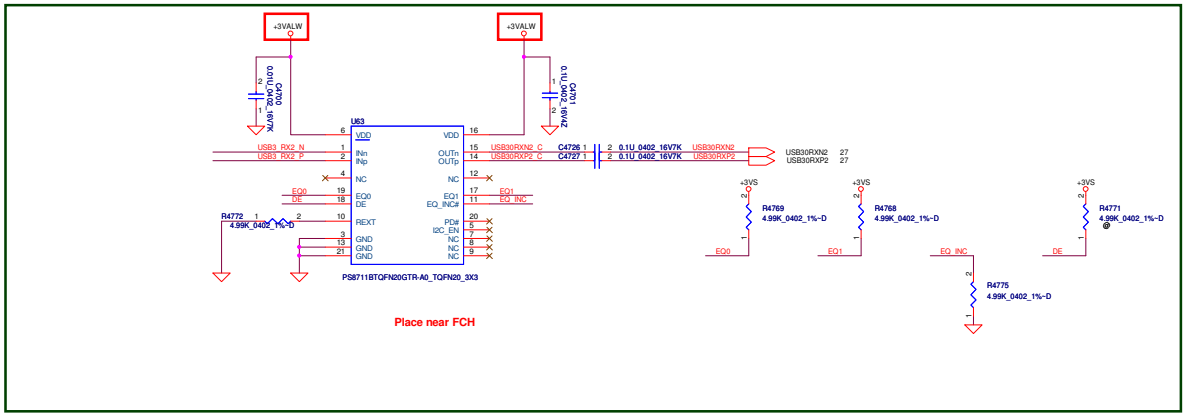
Title: LAN Magnetic & RJ45

Size: Custom | Document Number: QCL51 LA-8712P | Rev: 0.1

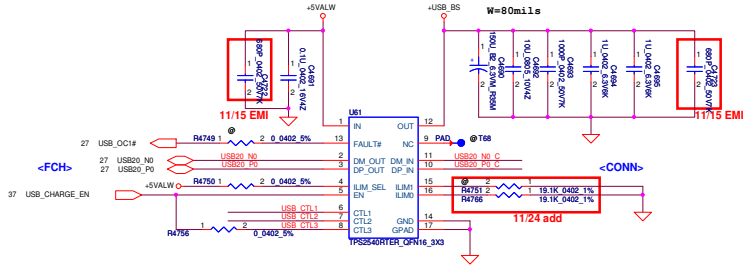
Date: Monday, November 28, 2011 | Sheet 39 of 56

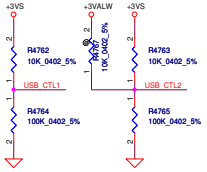
11/24 move to sub board

## USB3.0 Repeater



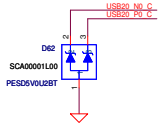

## USB Charger

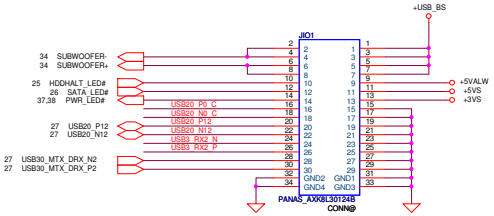



| State | S0 | | | | S3, S4, S5 | | | |
|---|---|---|---|---|---|---|---|---|
| Mode | CDP | | | | DCP | | | |
| Control pin | CTL1 | CTL2 | CTL3 | ILIM_SEL | CTL1 | CTL2 | CTL3 | ILIM_SEL |
| | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |

11/10 del chock




11/16 update footprint

11/24 change pin definition

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/07/08 | Deciphered Date | 2015/07/08 |

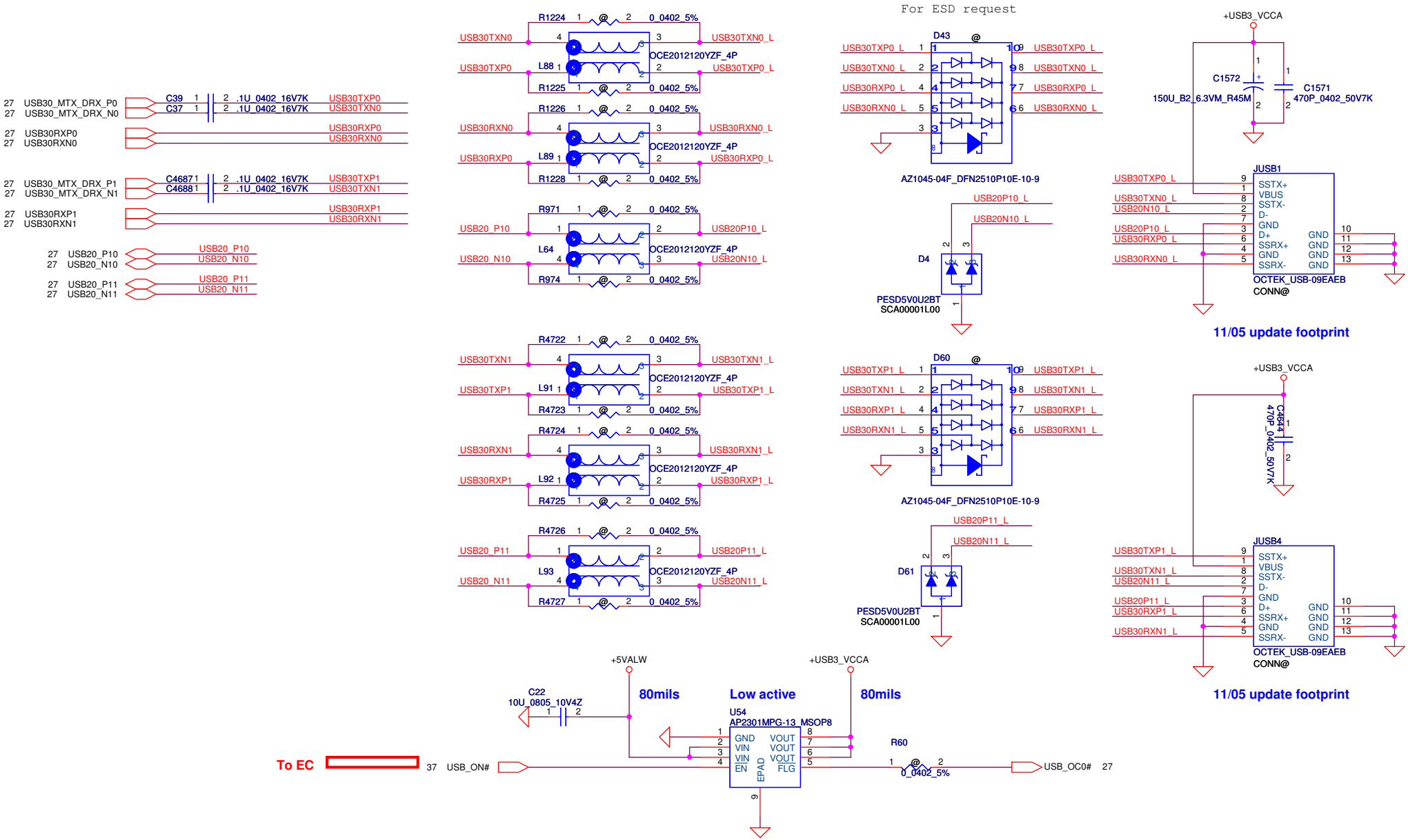


**Compal Electronics, Inc.**

Title: Gsensor/ Sub USB

Size: Custom | Document Number: QCL51 LA-8712P | Rev: 0.1

Date: Monday, November 28, 2011 | Sheet 40 of 56




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/07/08 | Deciphered Date | 2015/07/08 |



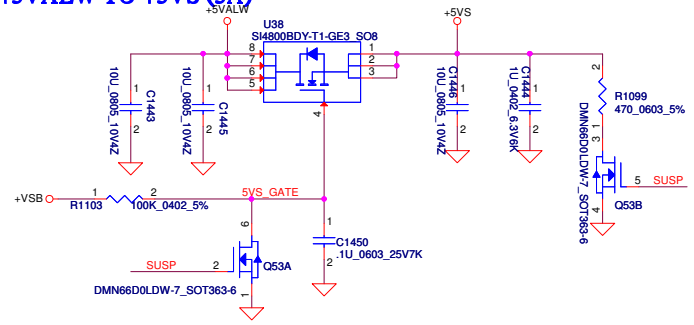
**Compal Electronics, Inc.**

Title: USB2.0 / USB3.0 / BT

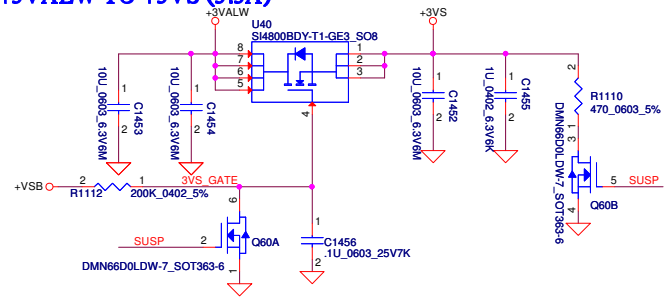
| Size | Document Number | Rev |
|---|---|---|
| B | QCL51 LA-8712P | 0.1 |

Date: Monday, November 28, 2011 Sheet 41 of 56

## +5VALW TO +5VS (5A)



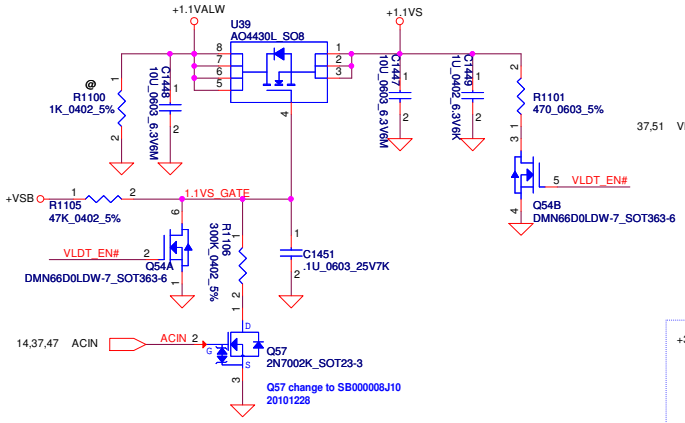

## +3VALW TO +3VS (3.3A)

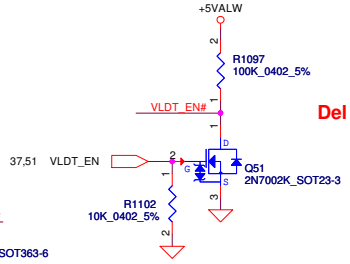



## +1.5V TO +1.5VS (1.5A)

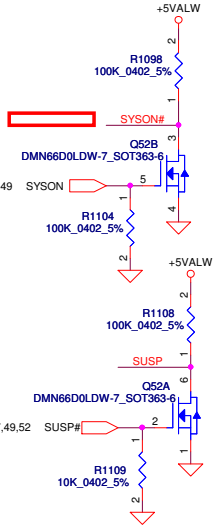
Del +1.5V to +1.5VS

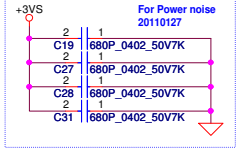
## +1.1VALW TO +1.1VS (1.1A)




Del arrow

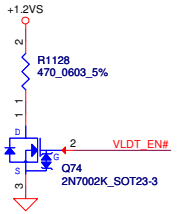


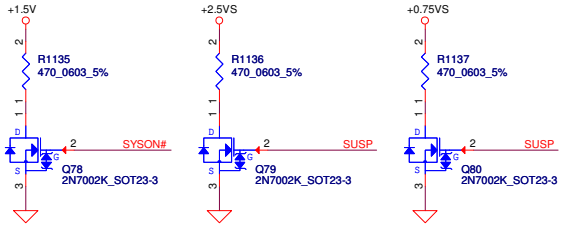




## VGA Power +1.5V to +1.5VSG (1.5A)

Del +1.5VSG and reserved on GPU

Del +3VSG and reserved on GPU




| | | | |
|---|---|---|---|
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| Issued Date | 2011/07/08 | Deciphered Date | 2015/07/08 |

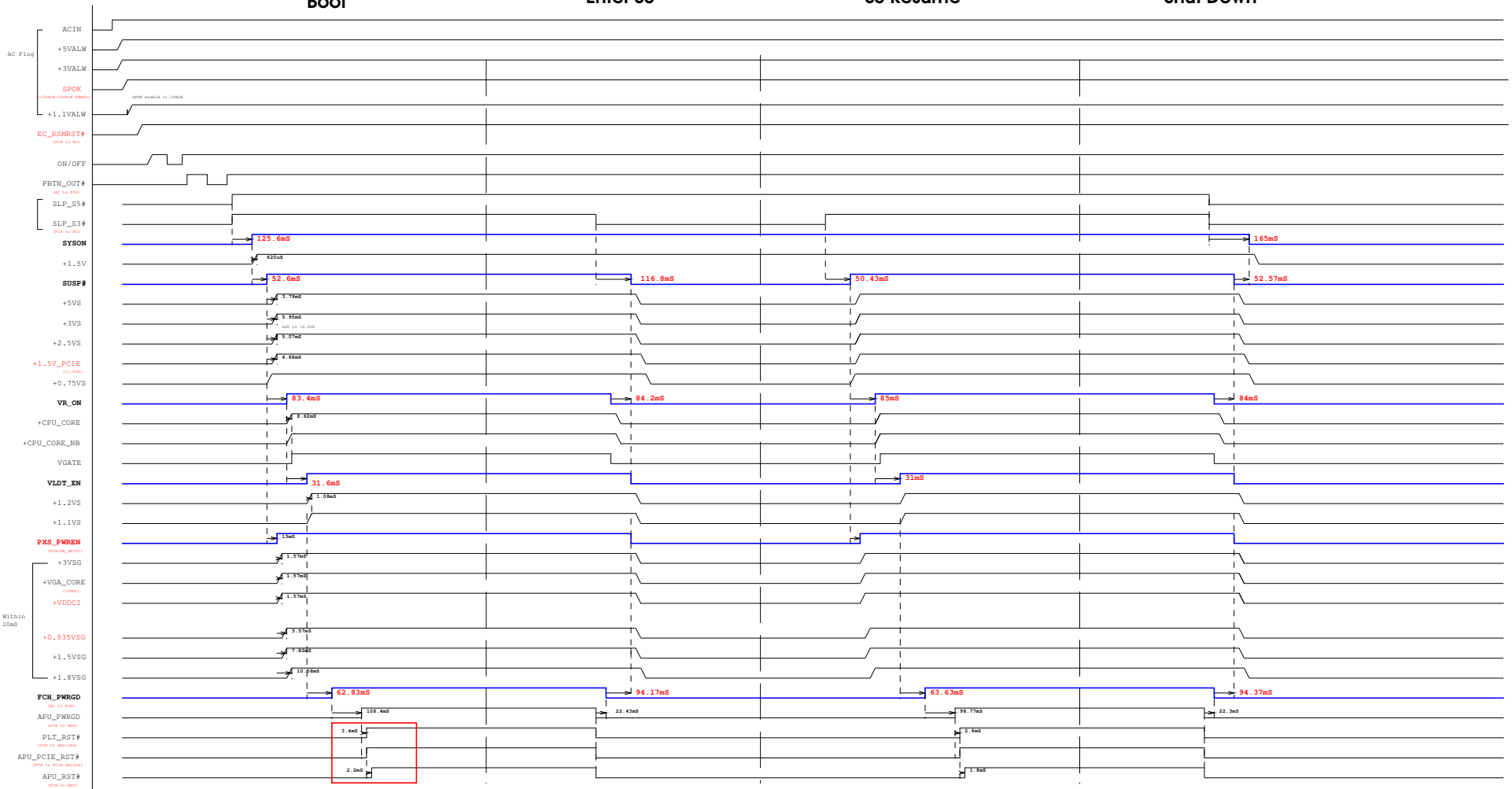


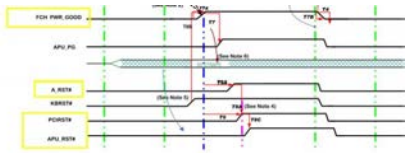
Compal Electronics, Inc.

Title: DC Interface

Size: B | Document Number: QCL51 LA-8712P | Rev: 0.1

Date: Monday, November 28, 2011 | Sheet 42 of 56



| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/07/08 | Deciphered Date | 2015/07/08 |

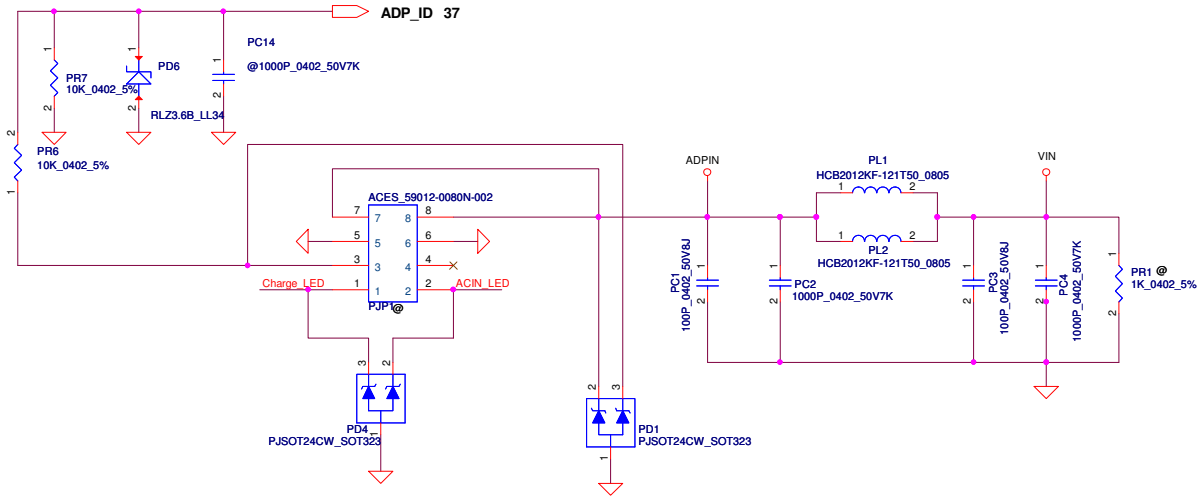


Compal Electronics, Inc.

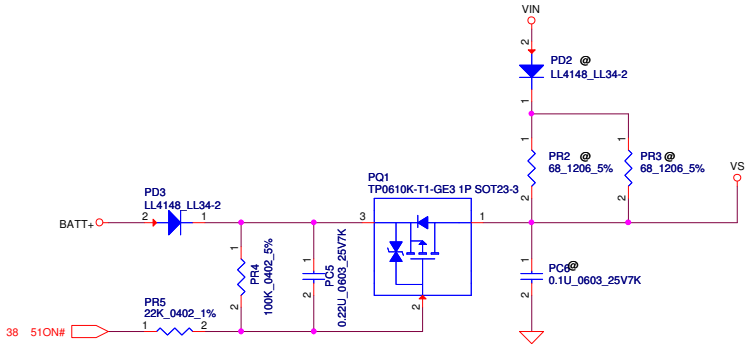
Title: DC Interface

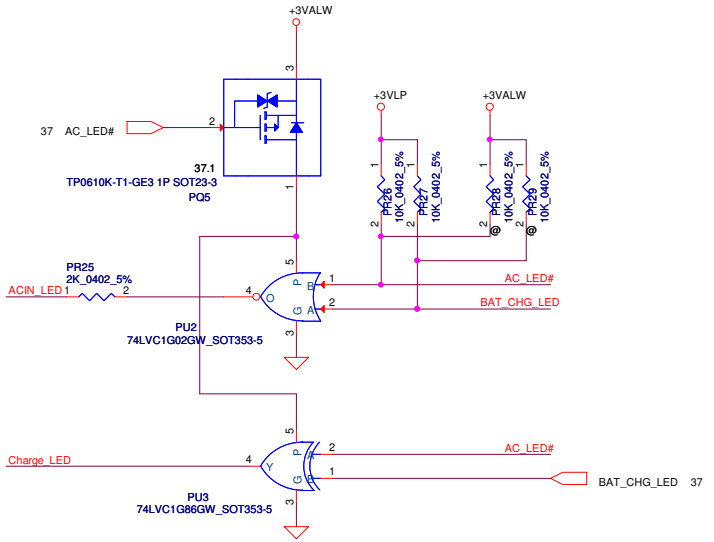
Size: Custom | Document Number: QCL51 LA-8712P | Rev: 0.1

Date: Monday, November 26, 2012 | Sheet 43 of 56




**ESD diode : SCA00001G00**





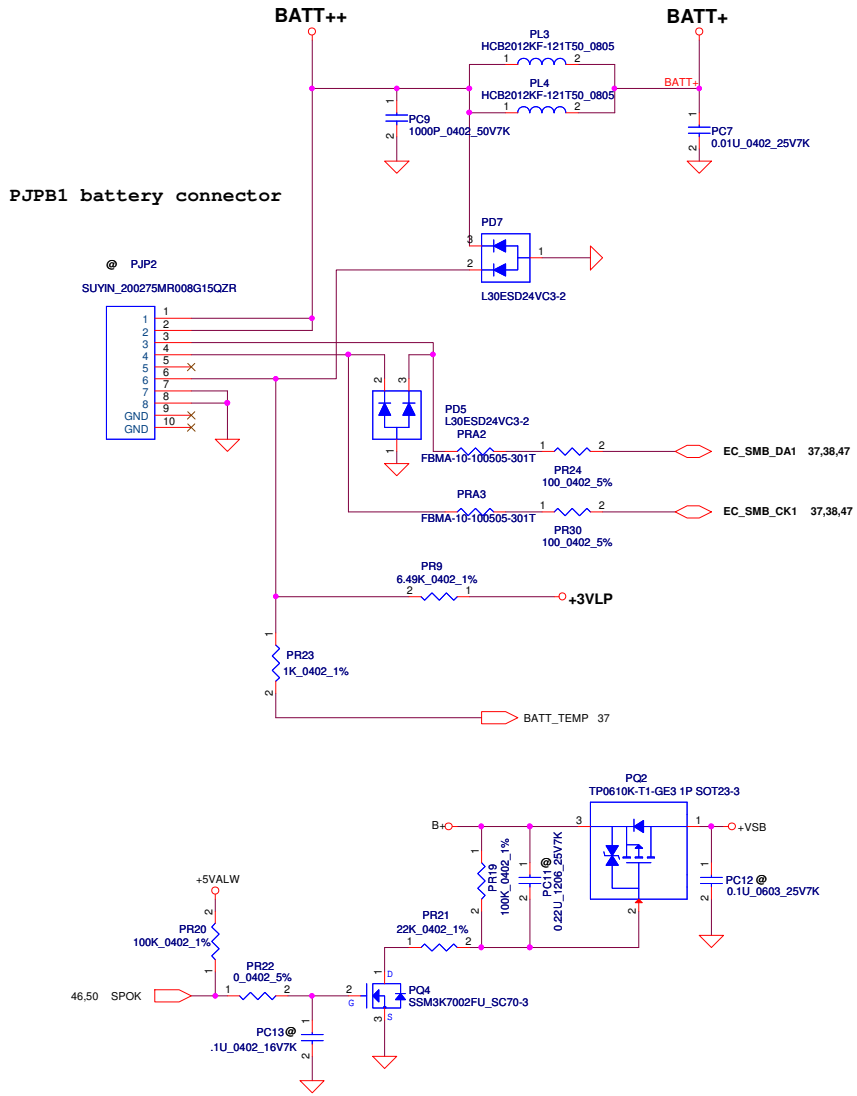

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/10/03 | Deciphered Date | 2014/12/31 |

Compal Electronics, Inc.

Title: PWR- DCIN / Vin Detector

Size: Custom | Document Number: QCL51 LA-8712P | Rev: 0.1

Date: Monday, November 28, 2011 | Sheet 44 of 56

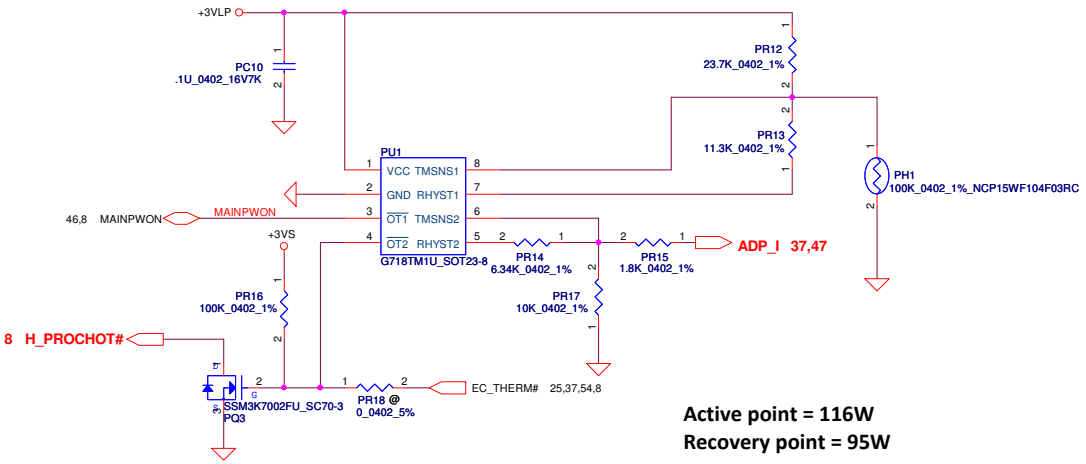



**For KB930 --> Keep PU1 circuit**
**(Vth = 0.825V)**

**PH1 under CPU botten side :**
**CPU thermal protection at 90 +-3 degree C**
**Recovery at 56 +-3 degree C**

**Rset = 3 * Rtmh**
**Rhyst = (Rset* Rtml) / (3*Rtml - Rset)**

**Rtmh at 90C = 7.8K, Rtml at 56C = 26.1K**
**Rset = 3 * 7.8K = 23.4K ==> 23.7K**
**Rhyst = (23.4K * 26.1K) / (3 * 26.1K - 23.4K) = 11.12K ==> 11.3K**

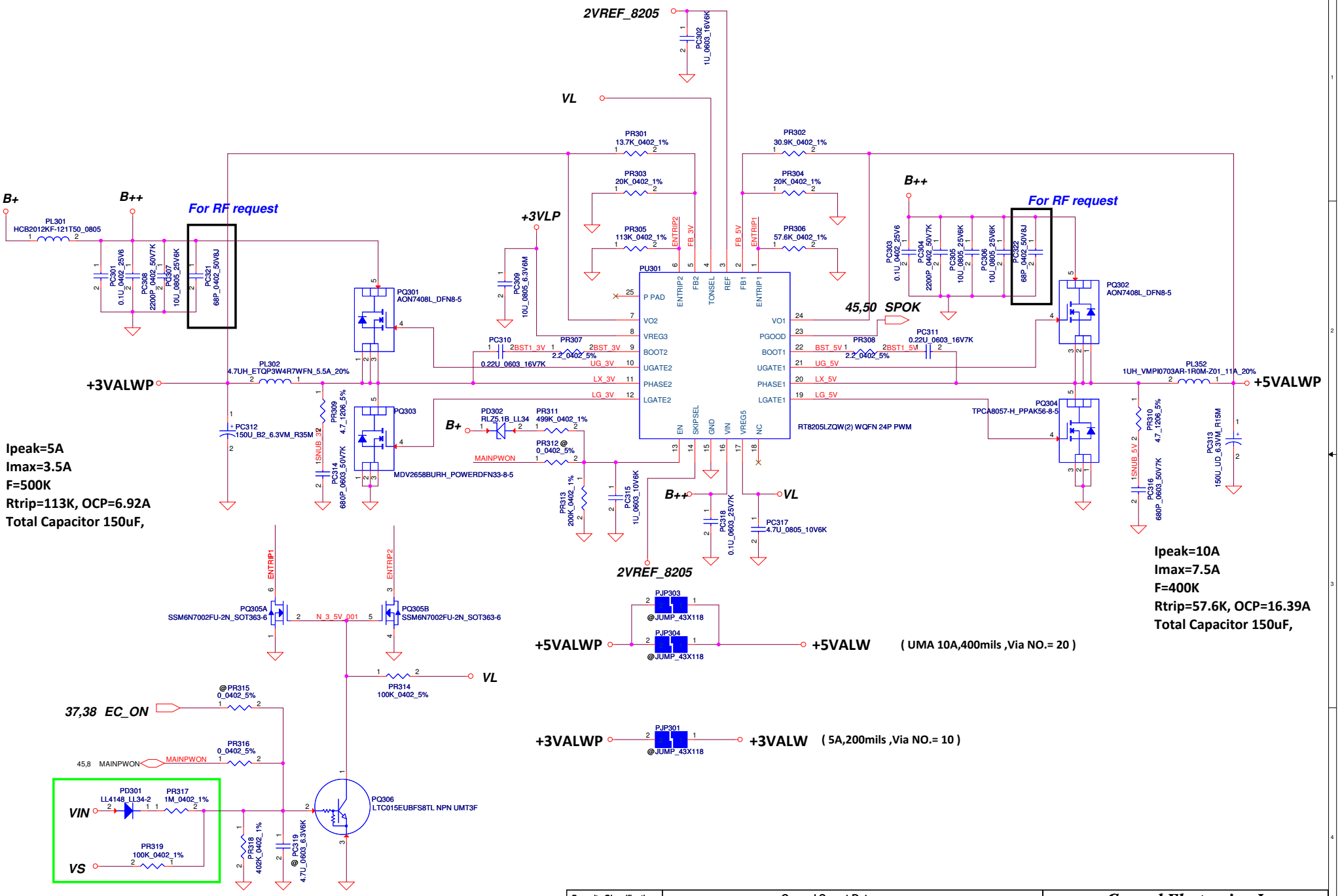



**Active point = 116W**
**Recovery point = 95W**

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/10/03 | Deciphered Date | 2014/12/31 |



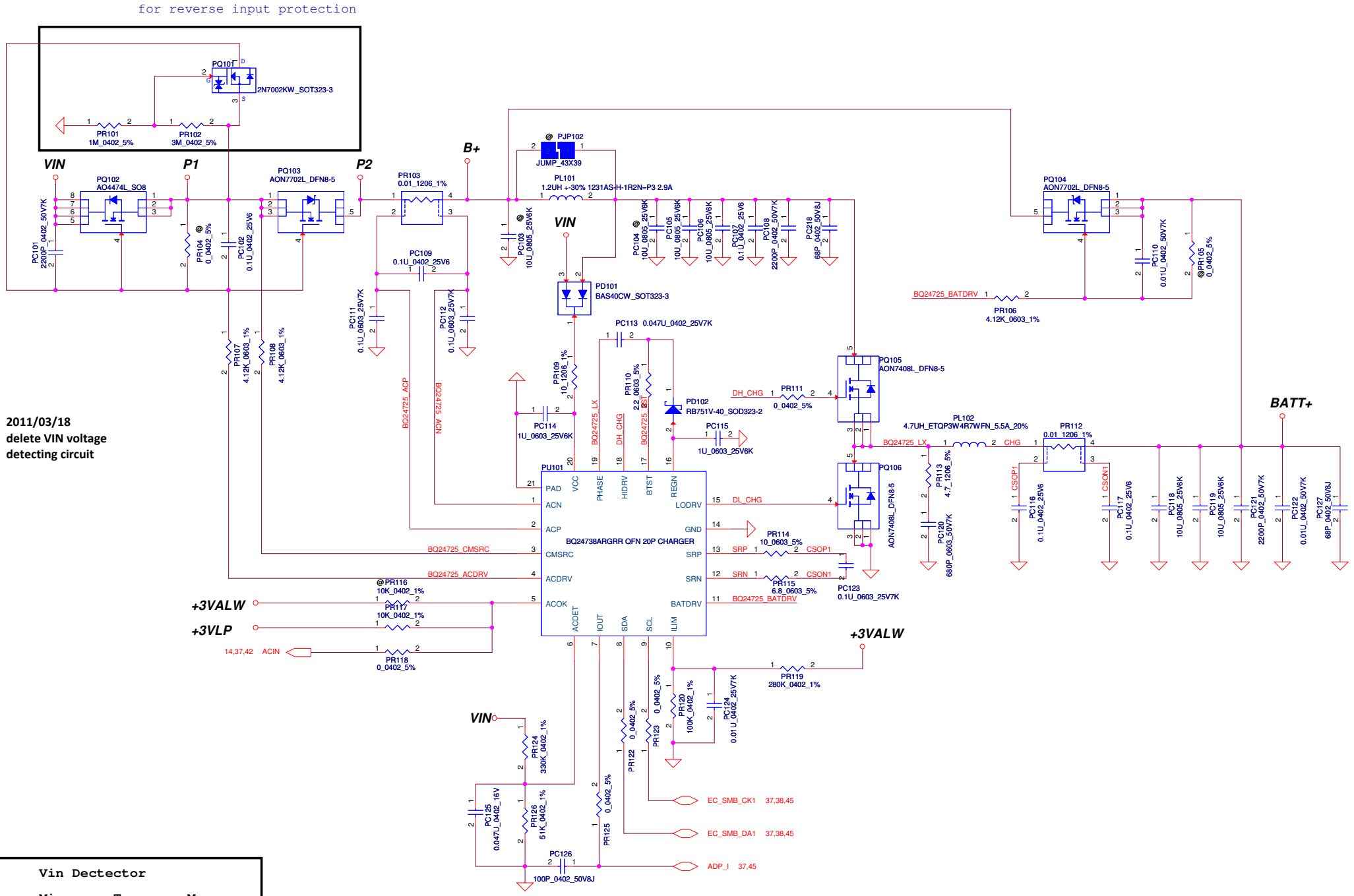
| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title: PWR- BATTERY CONN | | | |
| Size: Custom | Document Number: QCL51 LA-8712P | | Rev: 0.1 |
| Date: Monday, November 28, 2011 | Sheet 45 of 56 | | |




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/10/03 | Deciphered Date | 2014/12/31 |



| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title: PWR- 3VALWP/5VALWP | | | |
| Size: Custom | Document Number: QCL51 LA-8712P | | Rev: 0.1 |
| Date: Monday, November 28, 2011 | Sheet 46 of 56 | | |




2011/03/18
delete VIN voltage
detecting circuit

Vin Dectector

| | Min. | Typ | Max. |
|---|---|---|---|
| H-->L | | 17.33V | |
| L-->H | | 16.98V | |

ILIM and external DPM
4.36A

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/10/03 | Deciphered Date | 2014/12/31 |



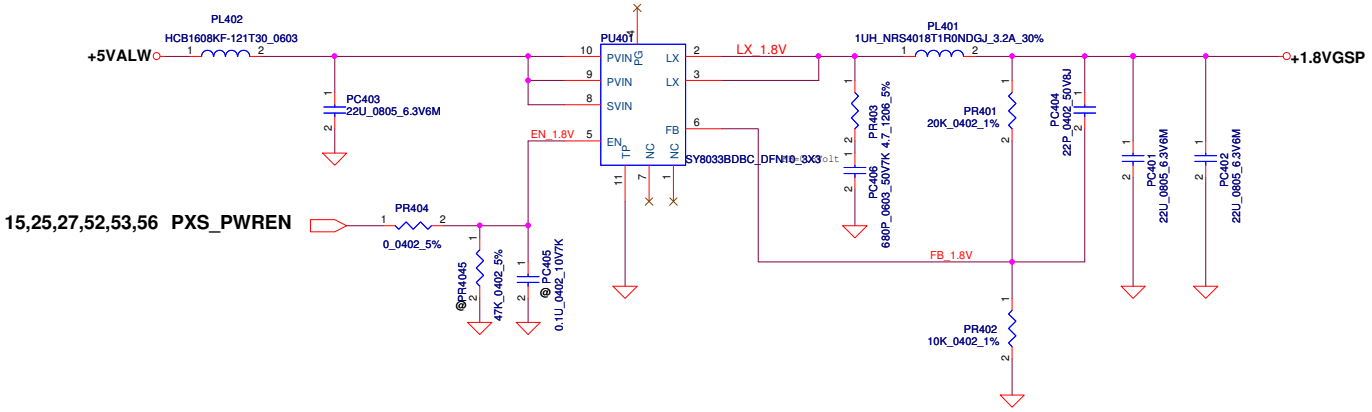
Compal Electronics, Inc.

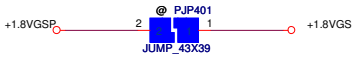
Title: PWR- CHARGER

Size: | Document Number: LA-8712P | Rev: 0.1

Date: Monday, November 28, 2011 | Sheet 47 of 56

1.8VGSP
Peak Current 1.4A
OCP current 3A



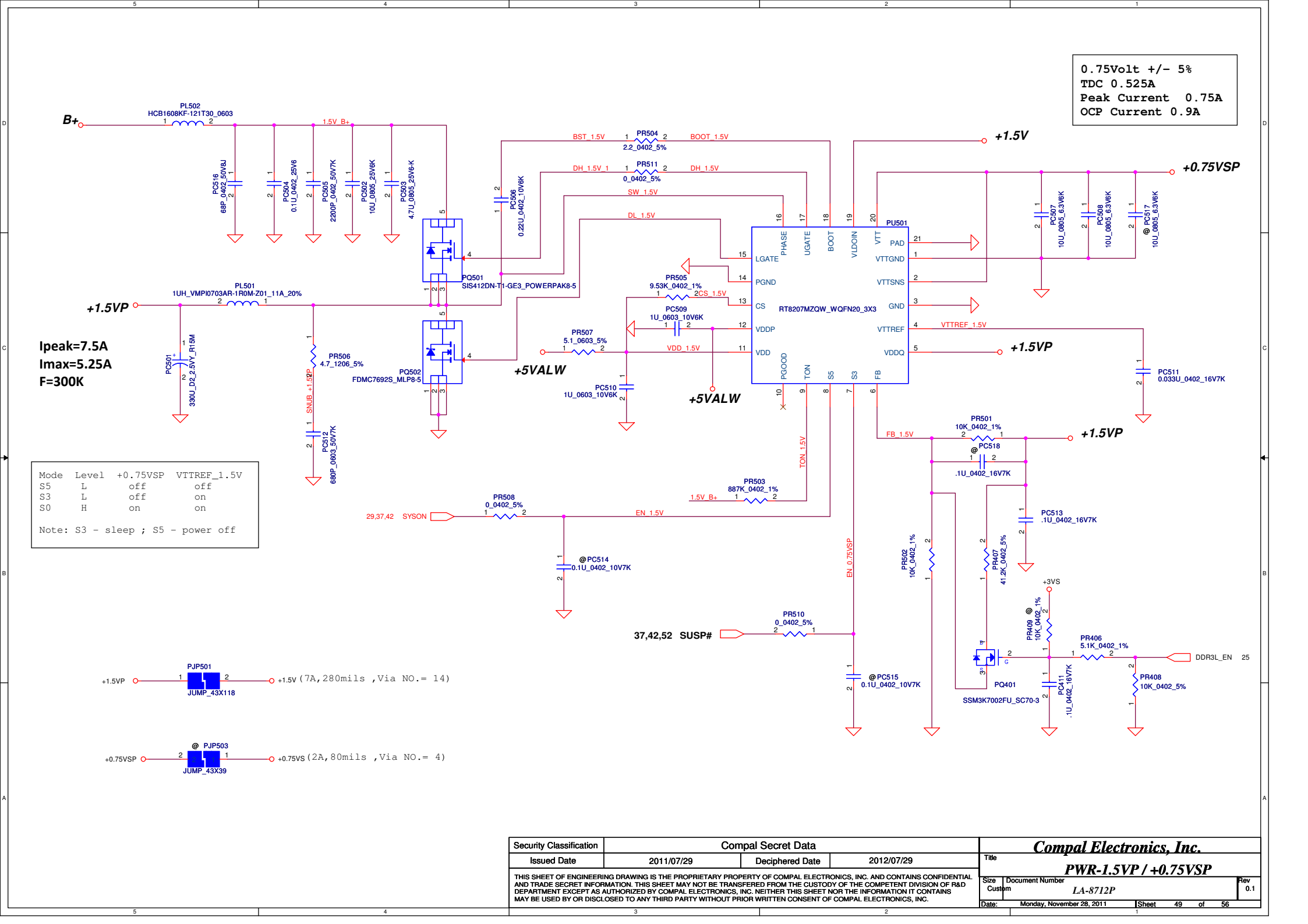




(4A,240mils ,Via NO.= 8)

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | Compal Electronics, Inc. |
| Issued Date | 2011/07/29 | Deciphered Date | Title: +1.8VP |



| | | | |
|---|---|---|---|
| Size | Document Number: LA-8712P | | Rev: 0.1 |
| Date: Monday, November 28, 2011 | Sheet 48 of 56 | | |




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/07/29 | Deciphered Date | 2012/07/29 |

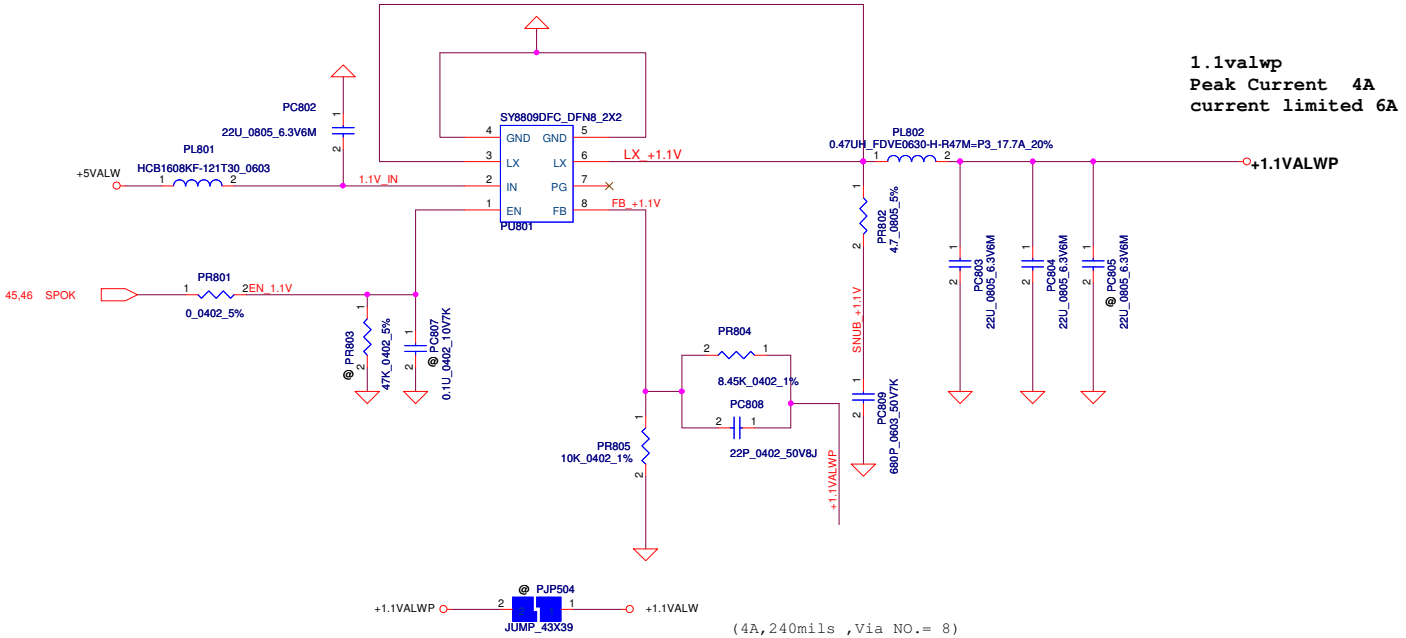


Compal Electronics, Inc.

Title: PWR-1.5VP / +0.75VSP

Size: Custom | Document Number: LA-8712P | Rev: 0.1

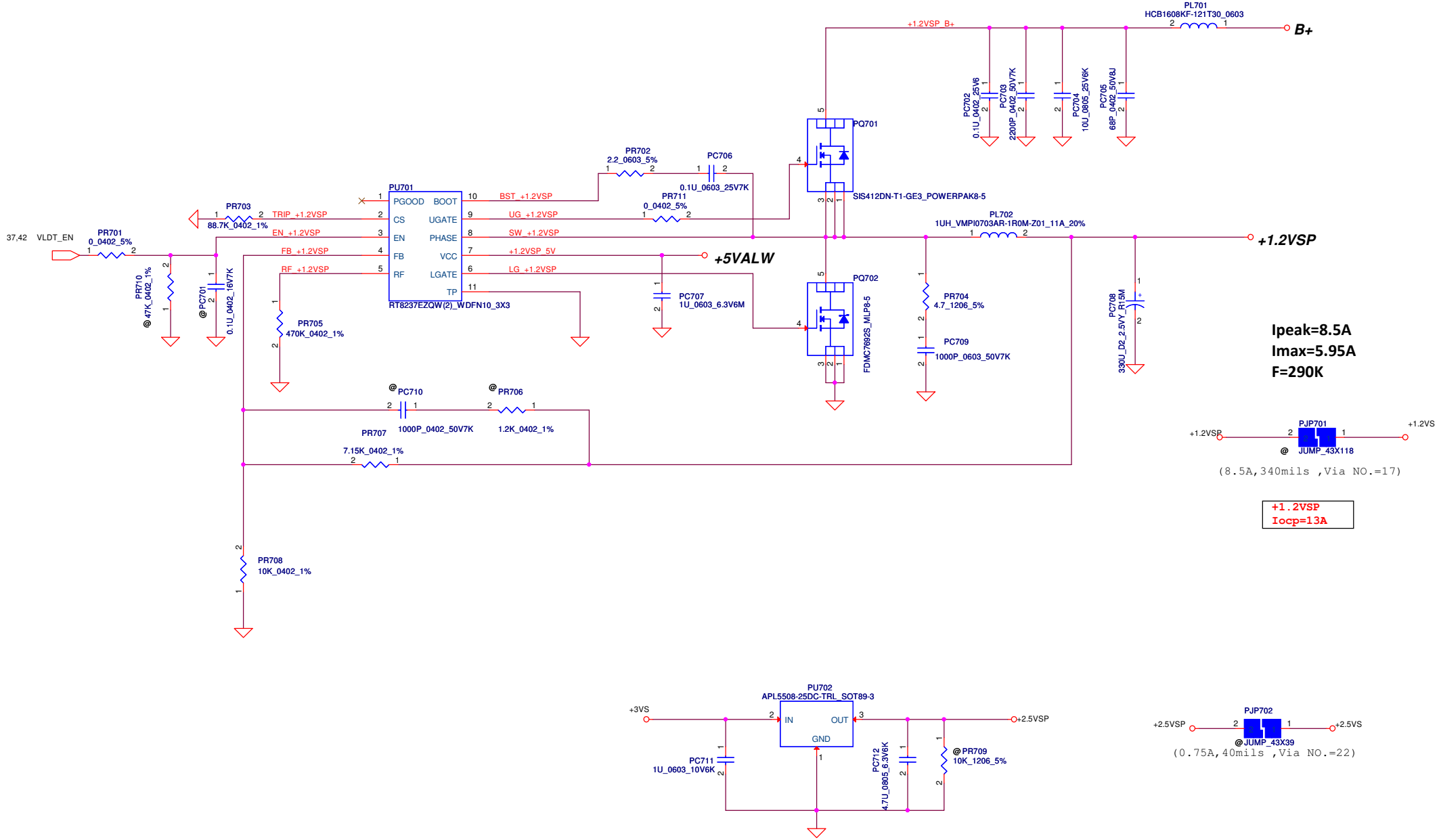
Date: Monday, November 28, 2011 | Sheet 49 of 56




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | Compal Electronics, Inc. |
| Issued Date | 2011/07/29 | Deciphered Date | Title: +1.1VALWP |



| | | | |
|---|---|---|---|
| Size: B5/5 | Document Number: LA-8712P | | Rev: 0.1 |
| Date: Monday, November 28, 2011 | Sheet 50 of 56 | | |




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/07/29 | Deciphered Date | |

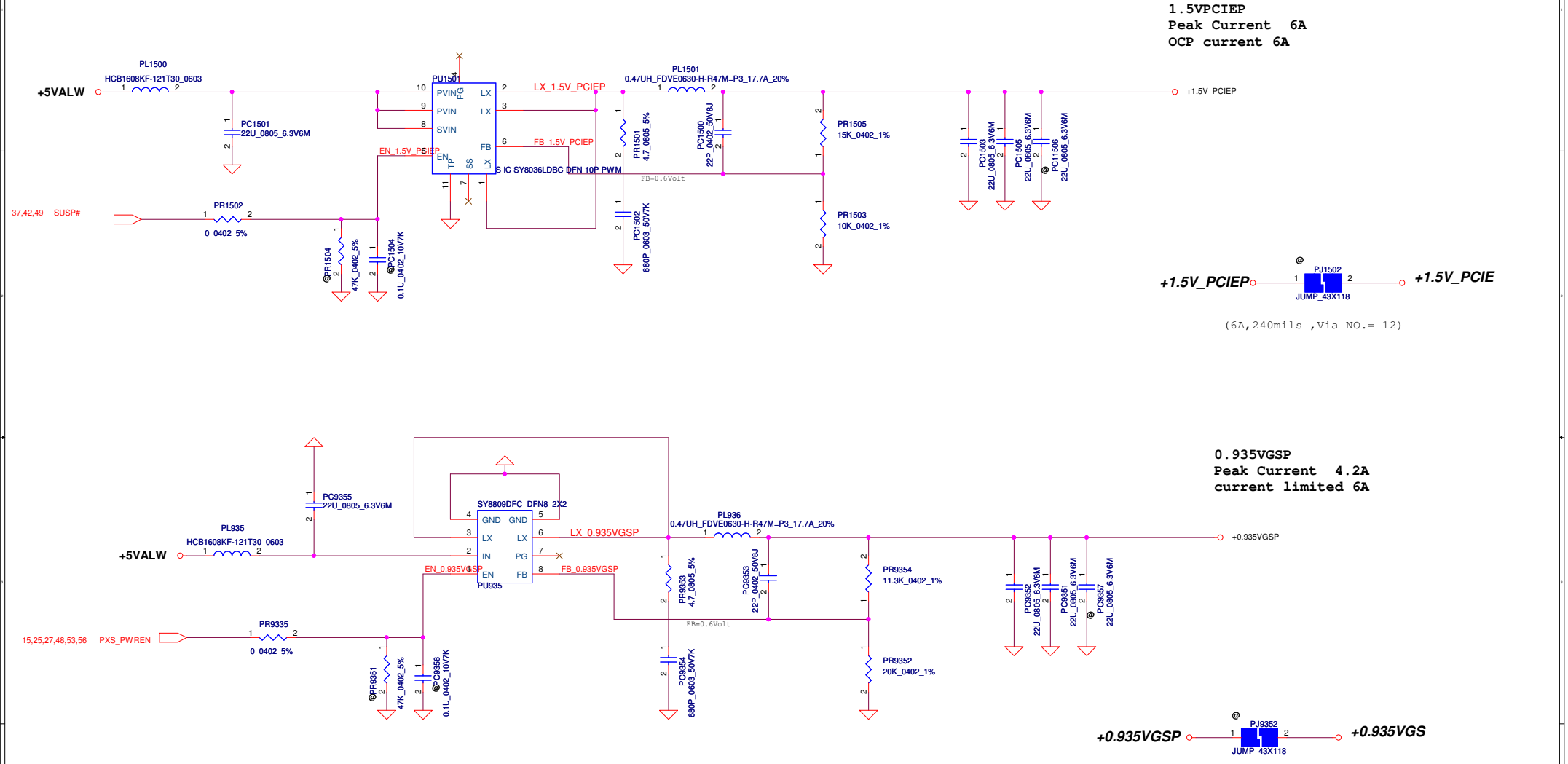


**Compal Electronics, Inc.**

Title: +1.2VSP/+2.5VSP

| Size | Document Number | Rev |
|---|---|---|
| | LA-8712P | 0.1 |

Date: Monday, November 28, 2011 | Sheet 51 of 56




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/08/16 | Deciphered Date | 2012/08/15 |



Compal Electronics, Inc.

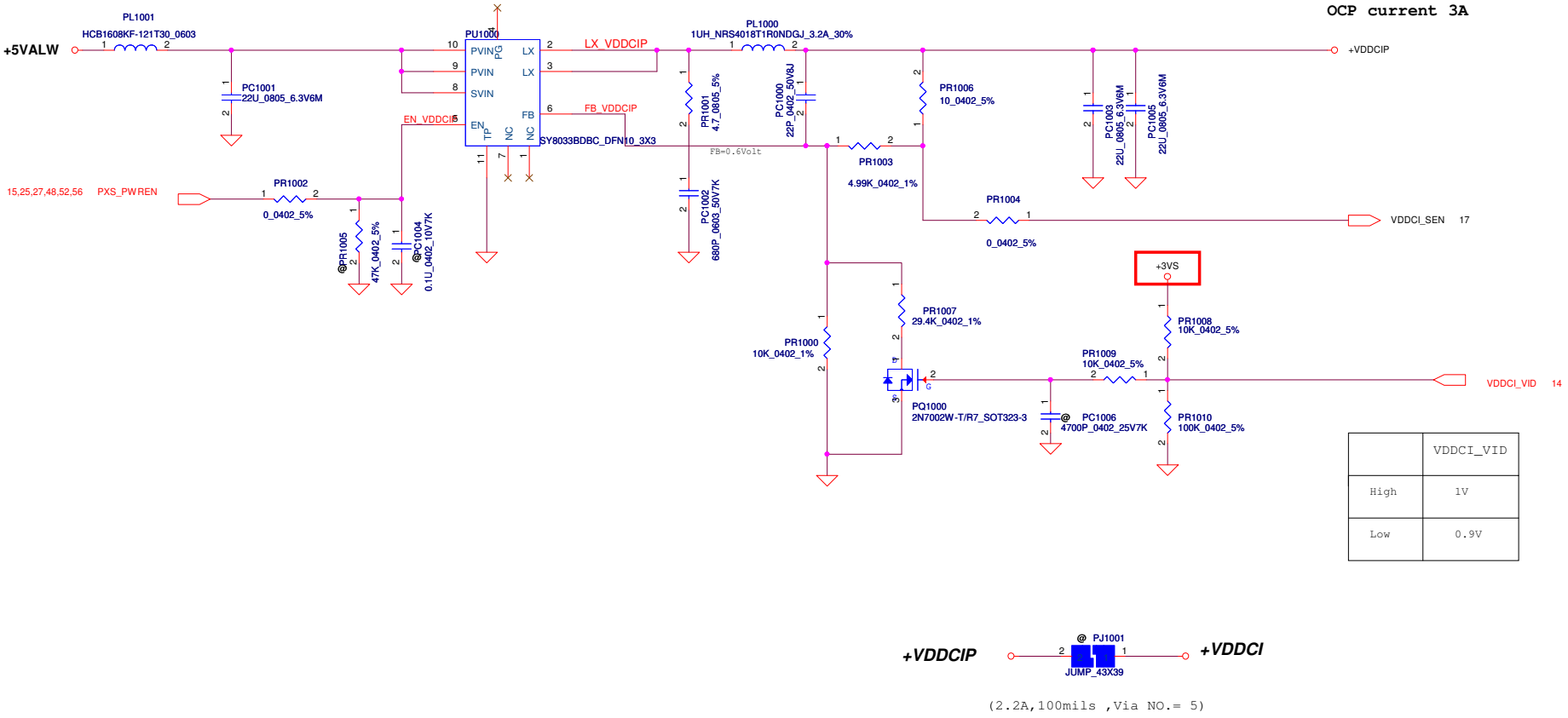
Title: +1.5VPCIE/0.935V

Size | Document Number: QCL51 LA-8712P | Rev: 0.1

Date: Monday, November 28, 2011 | Sheet 52 of 56

+VDDCI
TDC 2.2A

OCP current 3A




| | VDDCI_VID |
|---|---|
| High | 1V |
| Low | 0.9V |

+VDDCIP @ PJ1001 JUMP_43X39 +VDDCI

(2.2A,100mils ,Via NO.= 5)

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/08/16 | Deciphered Date | 2012/08/15 |

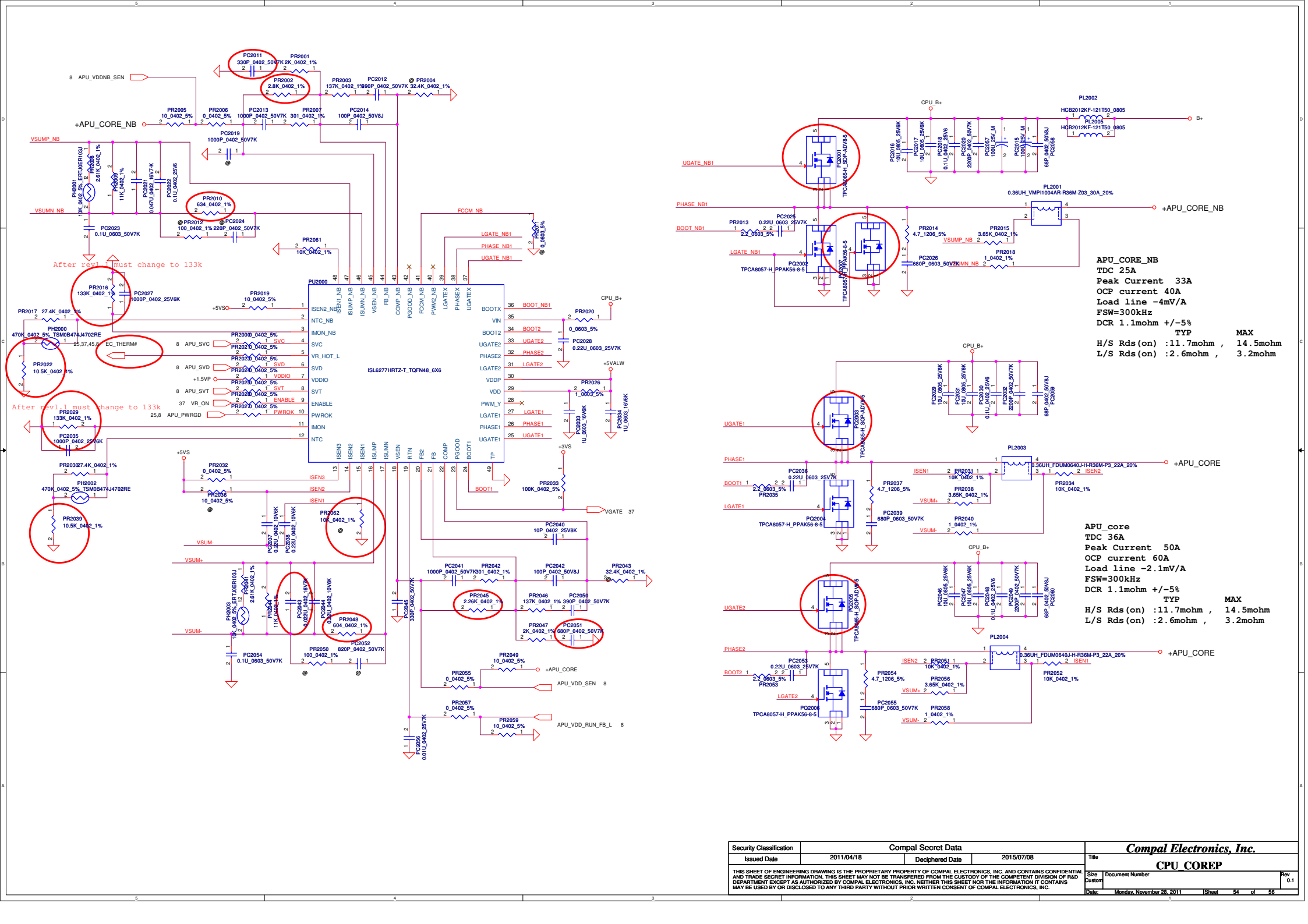


Compal Electronics, Inc.

Title: +VDDCIP

Size | Document Number: QCL51 LA-8712P | Rev: 0.1

Date: Monday, November 28, 2011 | Sheet 53 of 56

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| Issued Date | 2011/04/18 | Deciphered Date | 2015/07/08 |

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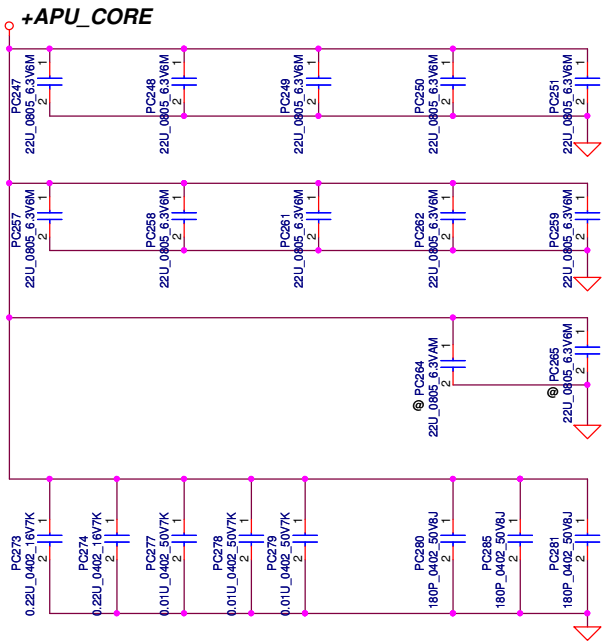
**Compal Electronics, Inc.**

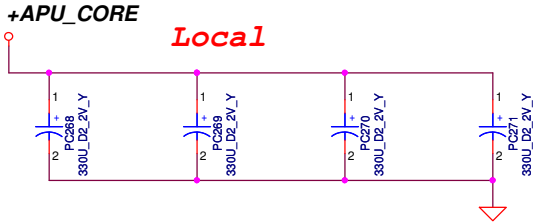
Title: CPU_COREP

Size: Custom | Document Number | Rev: 0.1

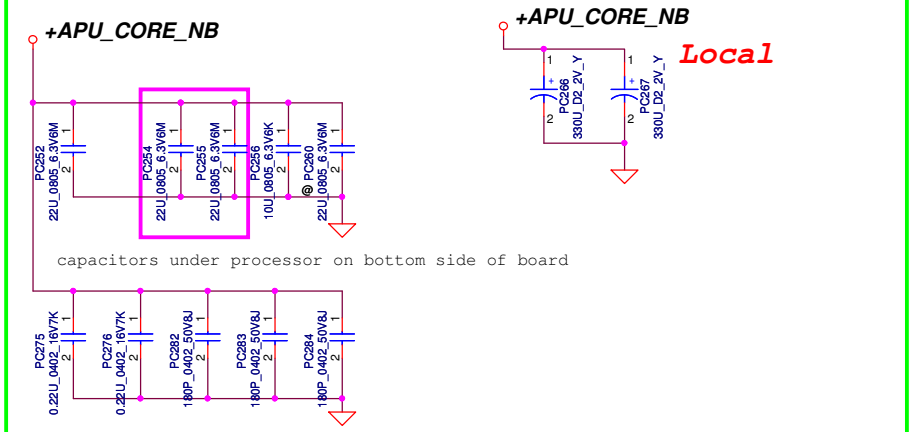
Date: Monday, November 28, 2011 | Sheet 54 of 56

# +APU_CORE

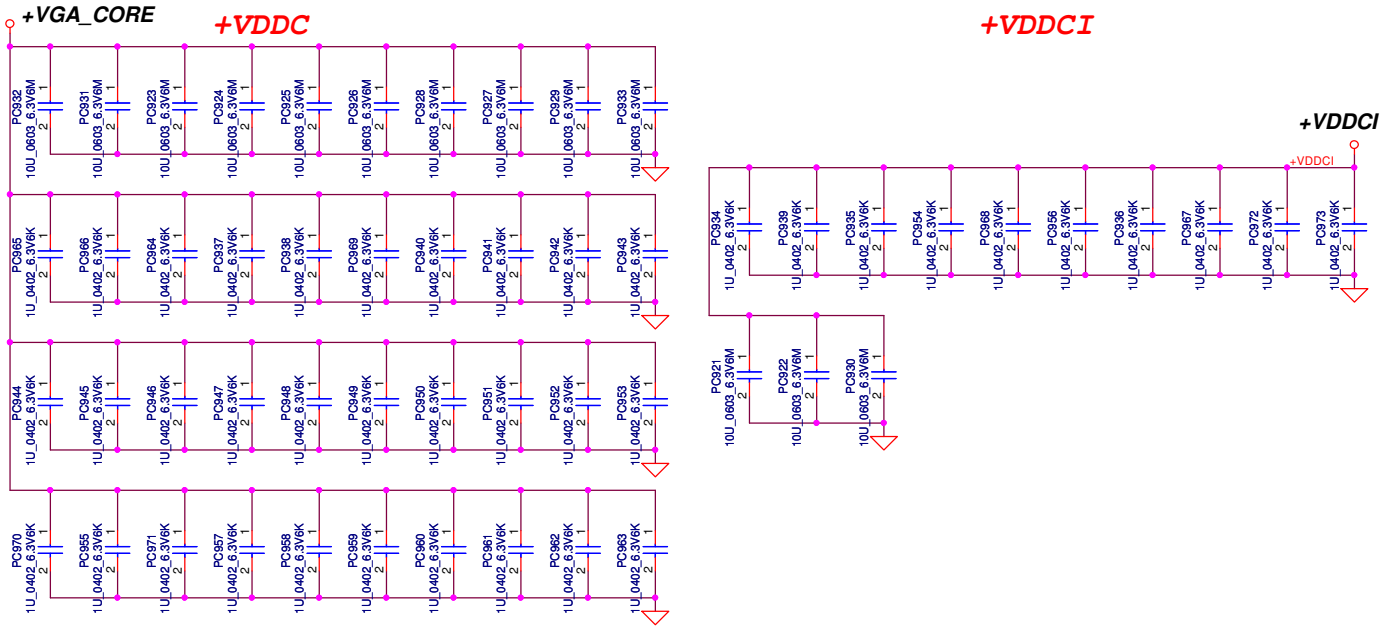



# +APU_CORE_NB



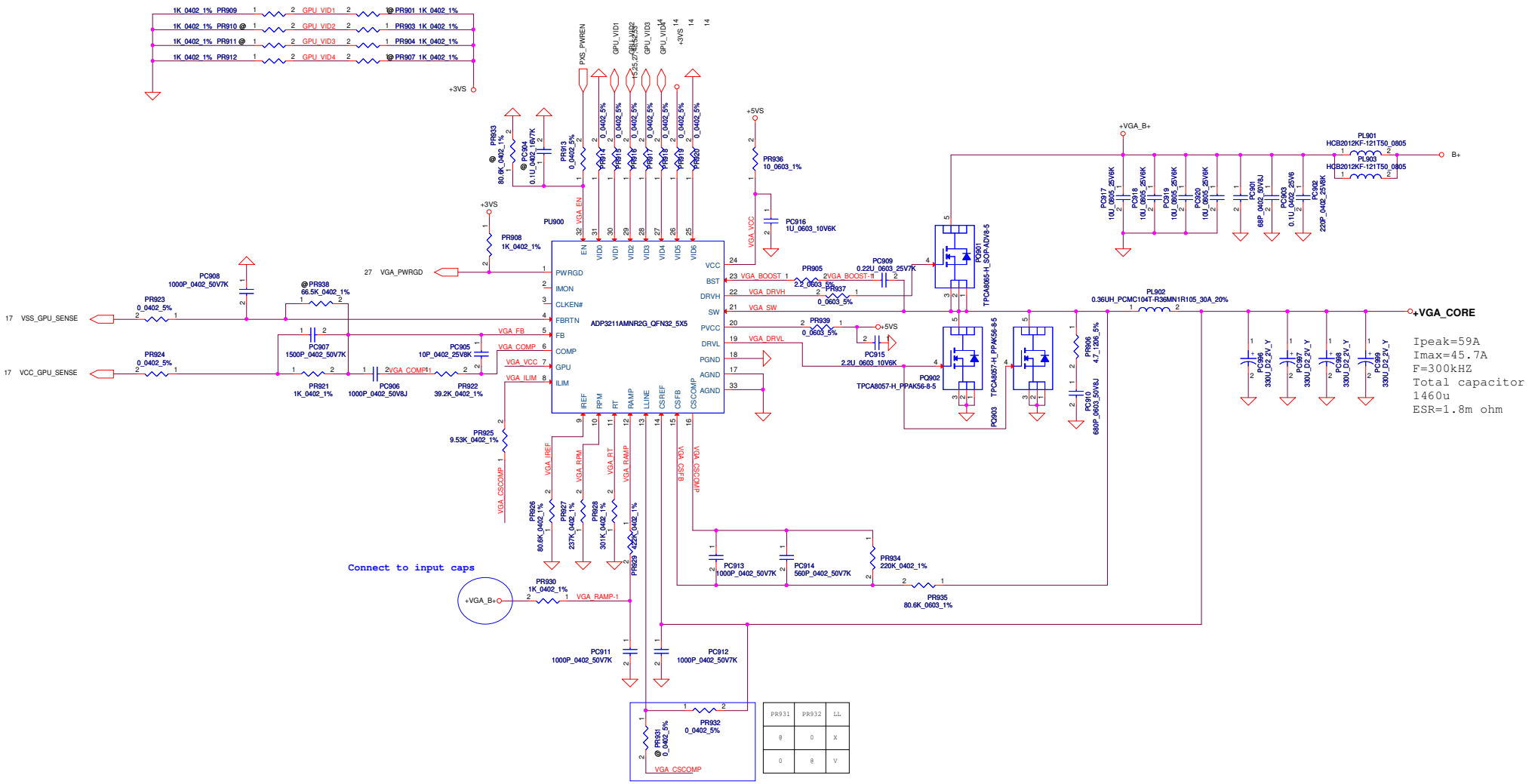

# +VGA_CORE




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/07/29 | Deciphered Date | |



| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title: PROCESSOR DECOUPLING | | | |
| Size: A3 | Document Number: LA-8712P | | Rev: 0.1 |
| Date: Monday, November 28, 2011 | | Sheet 55 of 56 | |




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2009/10/02 | Deciphered Date | 2010/10/02 |



**Compal Electronics, Inc.**

Title: **+VGA_COREP**

| Size | Document Number | Rev |
|---|---|---|
| | LA-8712P | 0.1 |

Date: Monday, November 28, 2011 | Sheet 56 of 56