

Compal Confidential

Huayra DIS (QCL51) Schematics Document

AMD Comal Platform

AMD Trinity APU / Hudson FCH / ATI Thames XT M2

Muxless/UMA / PX 5.0

2012-01-04

LA-8712P REV: 0.3

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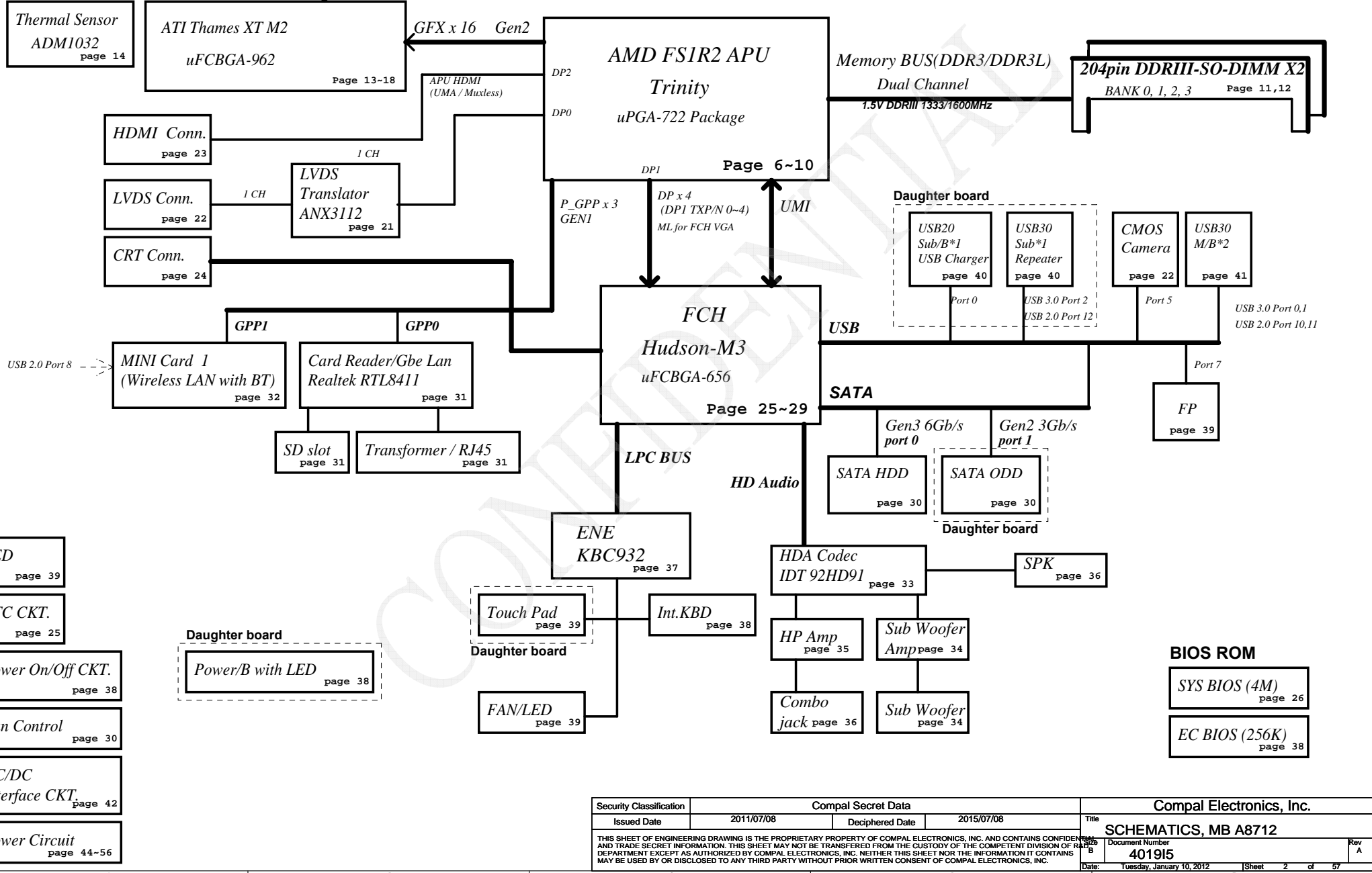
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Model Name : QCL51 AMD
Board Name : LA-8712P

64M x16
128M x 16
VRAM DDR3
page 19, 20

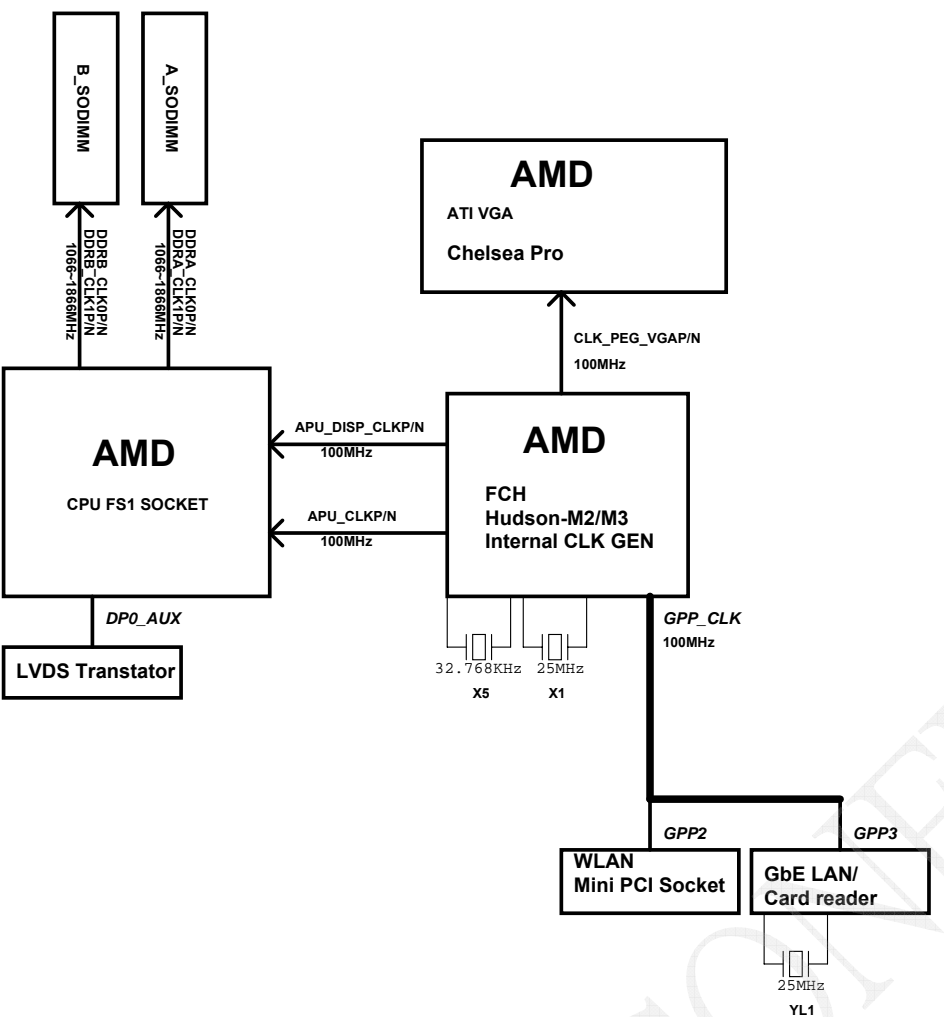
DDR3

AMD Comal

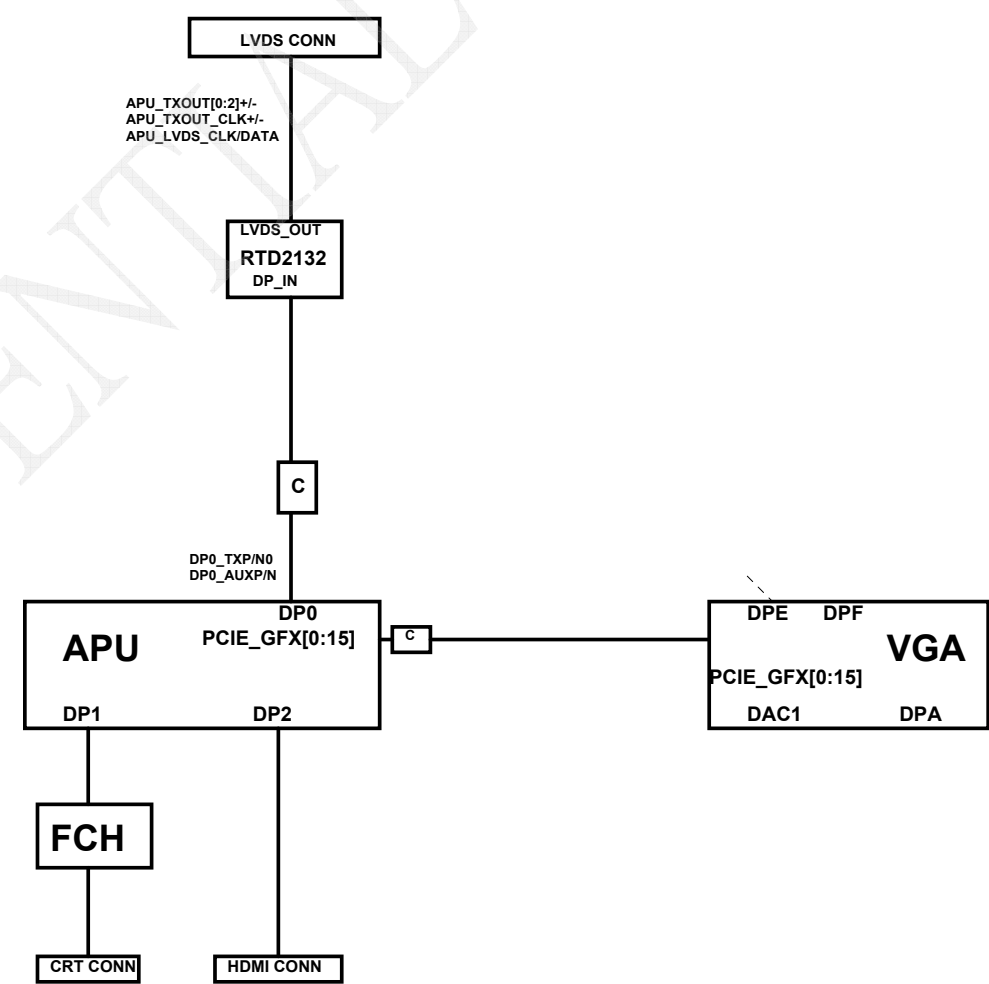


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CLOCK DISTRIBUTION



DISPLAY OUTPUT



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				Rev	A

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for CPU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+VDDCI	0.95-1.2V switched power rail	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	ON	OFF
+0.935VGS	0.935V switched power rail for VGA	ON	OFF	OFF
+1.1ALW	1.1V switched power rail for FCH	ON	ON	ON*
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF
+1.2VS	1.2V switched power rail for APU	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.5V_PCIE	1.5V switched power rail	ON	OFF	OFF
+1.8VGS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+LAN_VDD_3V3	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

x = 1 is read cmd, x= 0 is write cmd.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

EC SM Bus2 address

Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	ADI ADM1032 (GPU)	1001 101X b	9AH
			SB-TSI (APU)	1001 100X b	98H
			LVDS TR	1010 100X b	A8H
			VGA Internal Thermal	1000 001X b	82H

FCH (S0)

SM Bus 0 address

FCH (S0~S5)

SM Bus 1 address

Device	Address	HEX	Device	Address	HEX
DDR DIMM1	1010 000X b	A0	Touch pad		
DDR DIMM2	1010 001X b	A2			
Amplifier					

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rb	100K +/- 5%			
Board ID	Ra / Rb	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	1.8K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOM Option Table

BOM Structure	Description	DIS	PX@ DIS@ Tha@
PX@	PX function	UMA	UMA@
DIS@			
UMA@			
Tha@			

BOM Config

ZZZ1
DIS@
PCB
Part Number = DA8000SH00
PCB 00H LA-8712P REV0 M/B

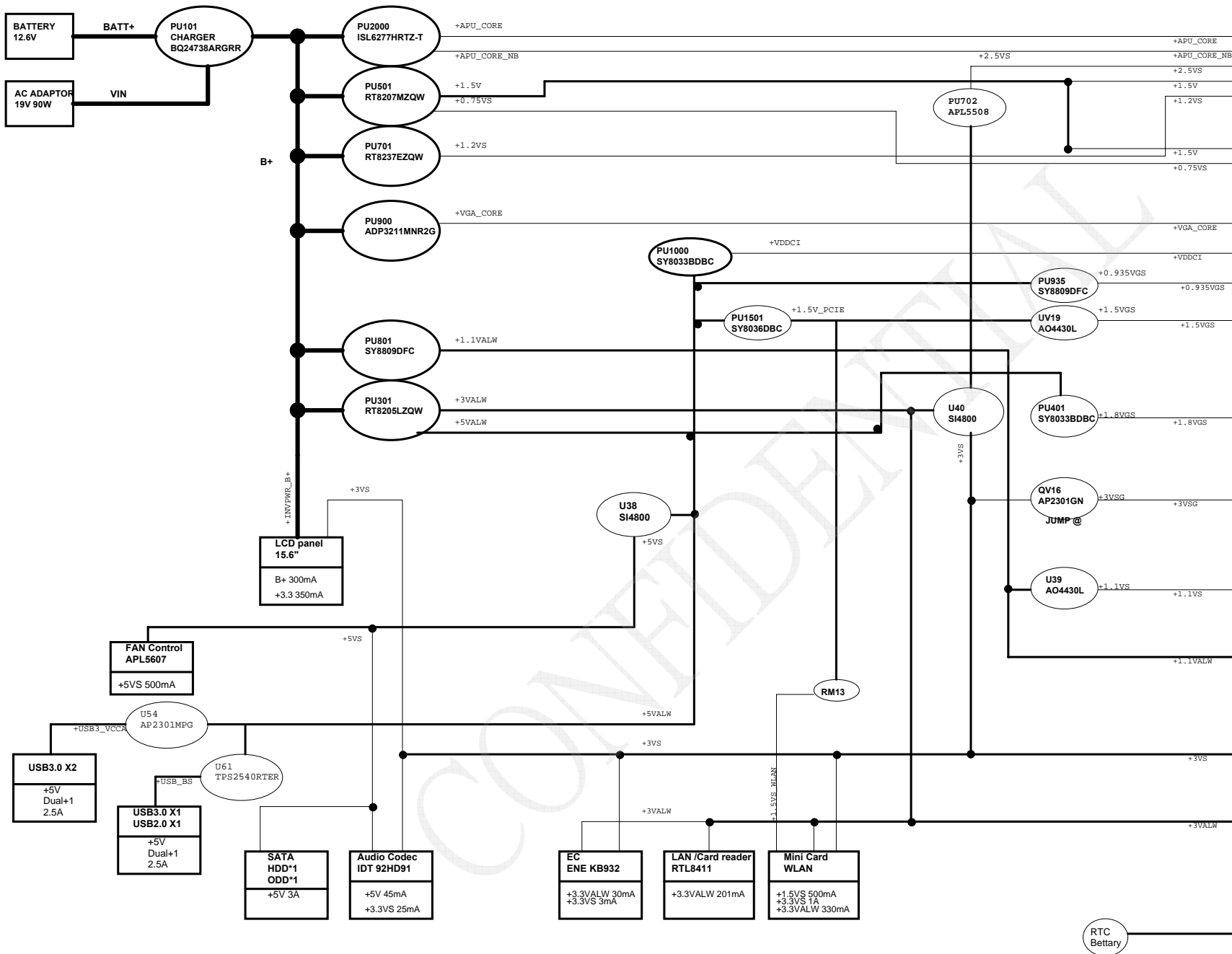
ZZZ2
UMA@
PCB
Part Number = DA6000T500
PCB 00H LA-8712P REV0 M/B

ZZZ3
DIS@
X7638732L01
Part Number = X7638732L01

BOARD ID Table

Board ID	PCB Revision
0	DB
1	SI

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AMD APU FS1R2	
0.7-1.475V	VDD CORE 60A
0.7-1.475V	VDDNB 44A
+2.5VS	VDDA 0.5A
+1.5V	VDDIO 3.2A
+1.2VS	VDDR 8.5A



RAM DDRIII SODIMMX2	
+1.5V	VDD_MEM 4A
+0.75VS	VTT_MEM 0.5A

VGA ATI Chelsea Pro	
0.85-1.1V	VDDC 28A
0.9-1.0V	VDDCI 4.6A
+0.935VGS	DPLL_VDDC: 125 mA SPV10: 100 mA PCI_E_VDDC: 1100 mA DP[A,E]_VDD10: 880 mA
+1.5VGS	VDDR1: 1200 mA
+1.8VGS	PLL_PVDD: 75 mA TSVDD: 5 mA AVDD: 70 mA VDD1DI: 45 mA VDD_CT: 17mA PCI_E_VDDR: 440 mA DP[A,F]_VDD18: 990 mA SPV18: 50mA MPV18: 150mA
+3VGS	VDDR3: 60 mA

VRAM 512/1GB/2GB 64M / 128Mx16 * 4 / 8	
+1.5VGS	2.4 A

FCH AMD Hudson M3	
+1.1VS	VDDPL_11_DAC: 7 mA VDDAN_11_ML: 226 mA VDDCR_11: 1007 mA VDDAN_11_CLK: 340 mA VDDAN_11_PCIE: 1088 mA VDDAN_11_SATA: 1337 mA
+1.1VALW	VDDAN_11_USB_S: 140 mA VDDCR_11_USB_S: 42 mA VDDAN_11_SSUSB_S: 282 mA VDDCR_11_SSUSB_S: 424 mA VDDCR_11_S: 187 mA VDDPL_11_SYS: 70 mA VDDCR_11_GBE_S: 63mA
+3VS	VDDIO_33_PCIGP: 102 mA VDDPL_33_SYS: 47 mA VDDPL_33_DAC: 20 mA VDDPL_33_ML: 12 mA VDDAN_33_DAC: 30 mA VDDCR_33_PCIE: 11 mA VDDPL_33_SATA: 12 mA VDDPL_33_USB_S: 14 mA
+3VALW	VDDPL_33_SSUSB_S: 11 mA VDDIO_AZ_S: 26 mA VDDAN_33_USB_S: 470 mA VDDIO_33_S: 59 mA VDDXL_33_S: 5 mA VDDAN_33_HWM_S: 12 mA VDDIO_GBE_S: 145mA VDDIO_33_GBE_S: 2mA
GND	VDDIO_33_GBE_S VDDCR_11_GBE_S VDDIO_GBE_S
RTC BAT	VDDBT_RTC_G

13 PCIE_GTX_C_FRX_P[0..15] 
 13 PCIE_GTX_C_FRX_N[0..15] 

 PCIE_FTX_C_GRX_P[0..15] 13
 PCIE_FTX_C_GRX_N[0..15] 13

GPU

GPU

JCPU1A
 PCI EXPRESS

PCIE GTX C FRX	PCIE GTX C FRX	P_GFX_RXP	P_GFX_RXN	P_GFX_TXP	P_GFX_TXN
P0	AB8	P_GFX_RXP0	P_GFX_RXN0	P_GFX_TXP0	P_GFX_TXN0
P1	AB7	P_GFX_RXP1	P_GFX_RXN1	P_GFX_TXP1	P_GFX_TXN1
P2	AA8	P_GFX_RXP2	P_GFX_RXN2	P_GFX_TXP2	P_GFX_TXN2
P3	AA5	P_GFX_RXP3	P_GFX_RXN3	P_GFX_TXP3	P_GFX_TXN3
P4	AA6	P_GFX_RXP4	P_GFX_RXN4	P_GFX_TXP4	P_GFX_TXN4
P5	Y8	P_GFX_RXP5	P_GFX_RXN5	P_GFX_TXP5	P_GFX_TXN5
P6	Y7	P_GFX_RXP6	P_GFX_RXN6	P_GFX_TXP6	P_GFX_TXN6
P7	Y8	P_GFX_RXP7	P_GFX_RXN7	P_GFX_TXP7	P_GFX_TXN7
P8	Y7	P_GFX_RXP8	P_GFX_RXN8	P_GFX_TXP8	P_GFX_TXN8
P9	Y8	P_GFX_RXP9	P_GFX_RXN9	P_GFX_TXP9	P_GFX_TXN9
P10	Y7	P_GFX_RXP10	P_GFX_RXN10	P_GFX_TXP10	P_GFX_TXN10
P11	Y8	P_GFX_RXP11	P_GFX_RXN11	P_GFX_TXP11	P_GFX_TXN11
P12	Y7	P_GFX_RXP12	P_GFX_RXN12	P_GFX_TXP12	P_GFX_TXN12
P13	Y8	P_GFX_RXP13	P_GFX_RXN13	P_GFX_TXP13	P_GFX_TXN13
P14	Y7	P_GFX_RXP14	P_GFX_RXN14	P_GFX_TXP14	P_GFX_TXN14
P15	Y8	P_GFX_RXP15	P_GFX_RXN15	P_GFX_TXP15	P_GFX_TXN15

GRAPHICS

GLAN/Card reader
WLAN

GLAN/Card reader
WLAN

P_GPP_RXP	P_GPP_RXN	P_GPP_TXP	P_GPP_TXN
P_GPP_RXP0	P_GPP_RXN0	P_GPP_TXP0	P_GPP_TXN0
P_GPP_RXP1	P_GPP_RXN1	P_GPP_TXP1	P_GPP_TXN1
P_GPP_RXP2	P_GPP_RXN2	P_GPP_TXP2	P_GPP_TXN2
P_GPP_RXP3	P_GPP_RXN3	P_GPP_TXP3	P_GPP_TXN3

GPP

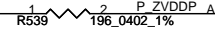
UMI


UMI

UMI_MTX_C_FRX	UMI_MTX_C_FRX	UMI_RXP	UMI_RXN	UMI_TXP	UMI_TXN
P0	AG8	UMI_RXP0	UMI_RXN0	UMI_TXP0	UMI_TXN0
P1	AG9	UMI_RXP1	UMI_RXN1	UMI_TXP1	UMI_TXN1
P2	AG6	UMI_RXP2	UMI_RXN2	UMI_TXP2	UMI_TXN2
P3	AG5	UMI_RXP3	UMI_RXN3	UMI_TXP3	UMI_TXN3

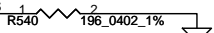
UMI


+1.2VS O



 P_ZVDDP W/S=8/12 mil, <3000mil

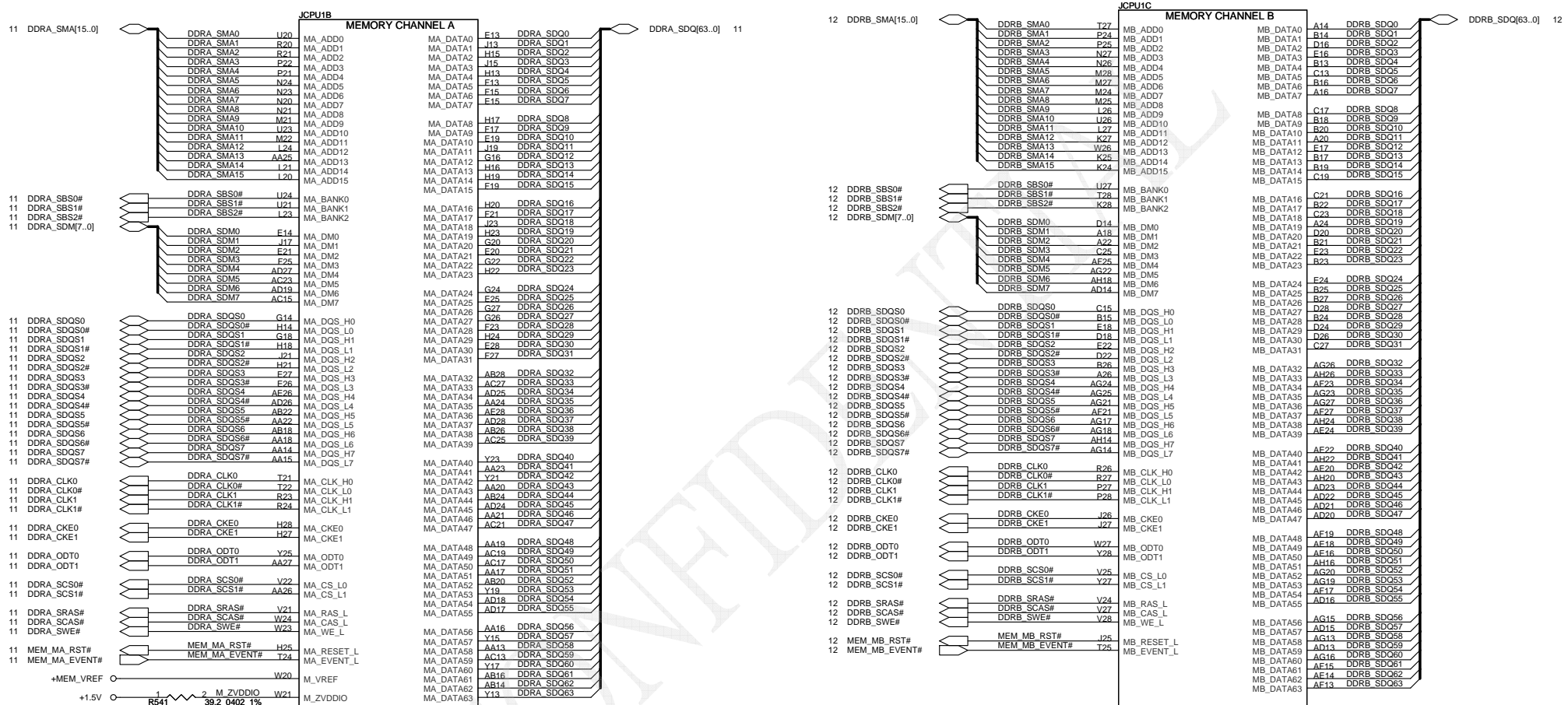
P_ZVSS



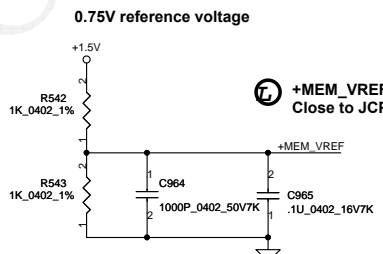
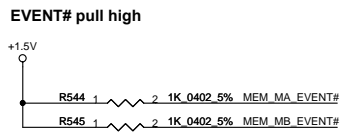
 P_ZVSS W/S=8/12 mil, <3000mil

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CONN@

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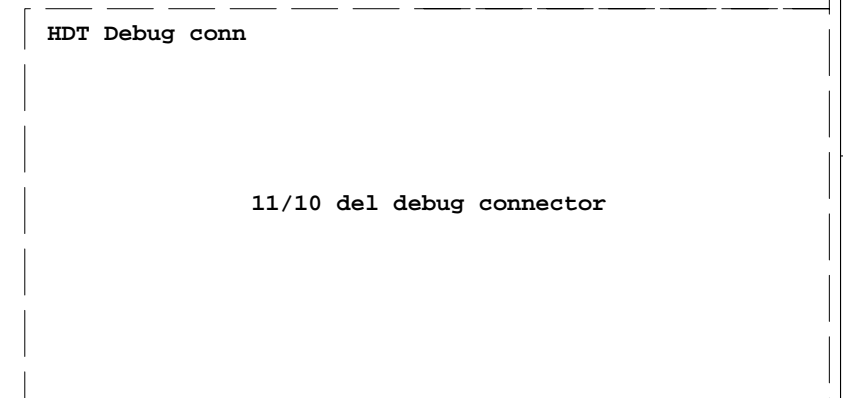
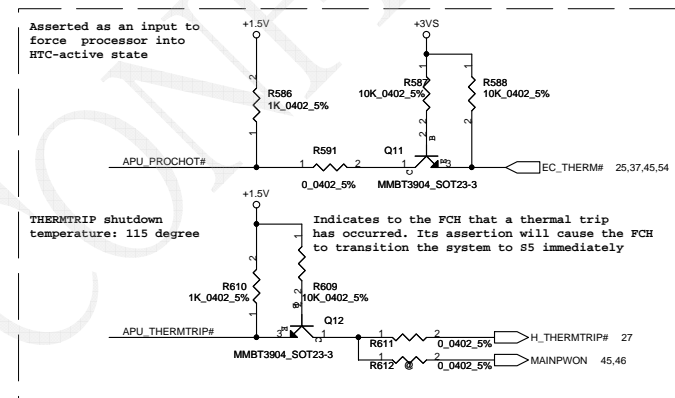
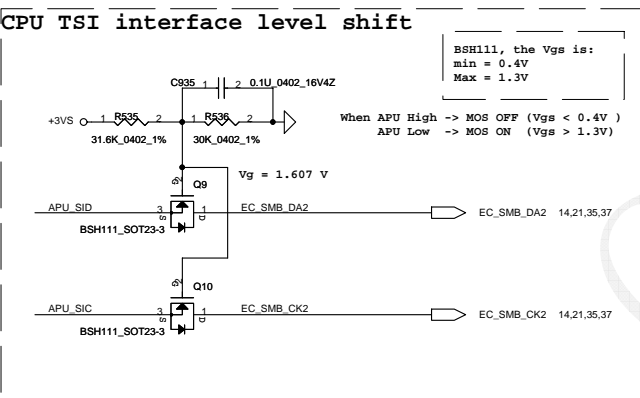
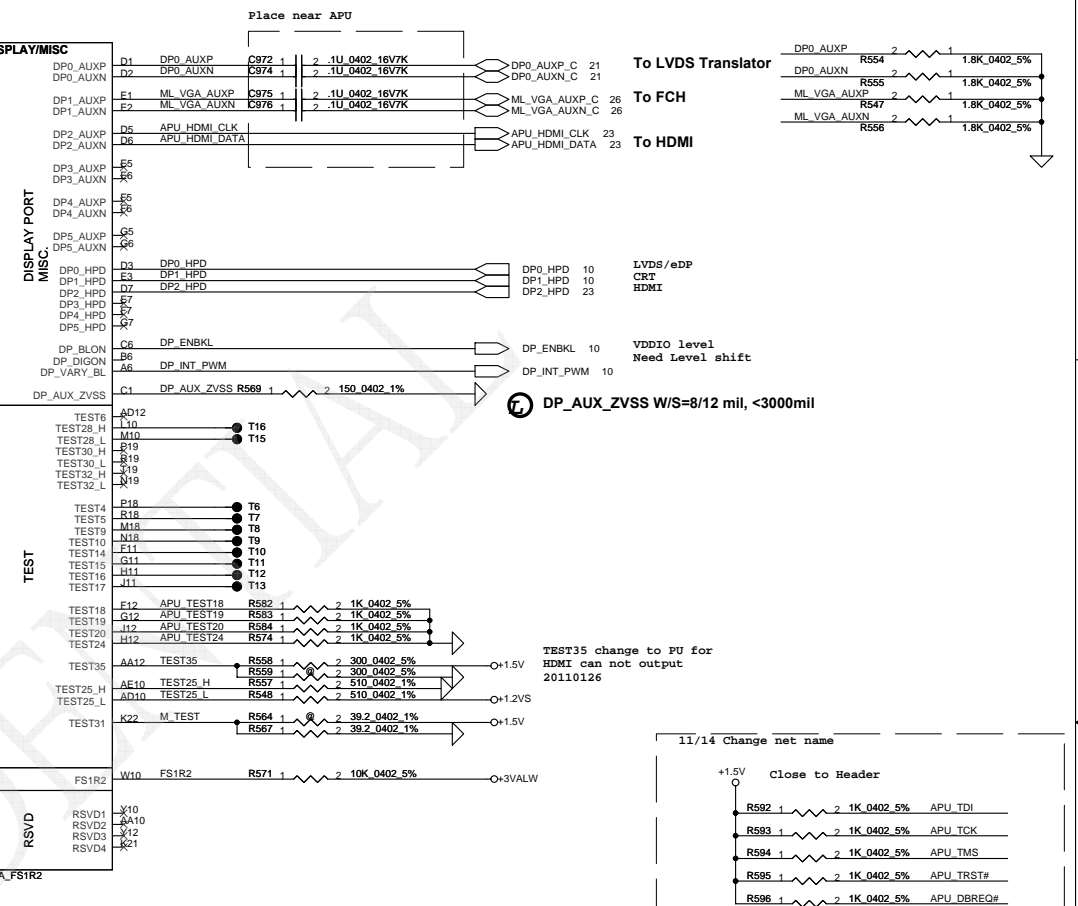
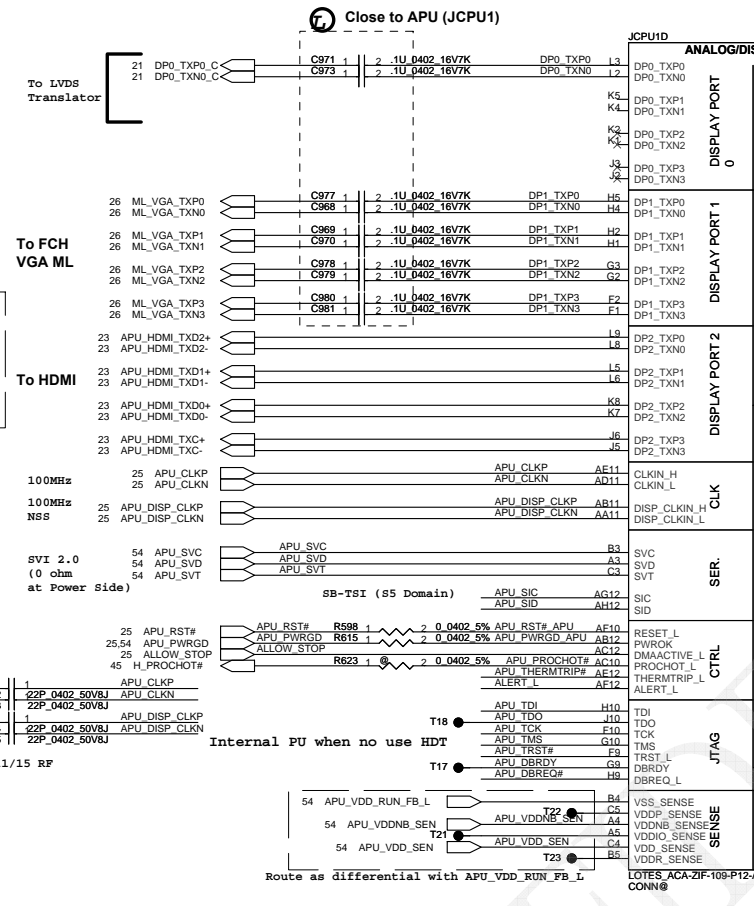
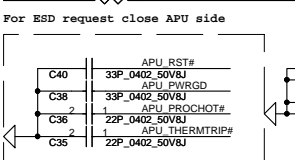
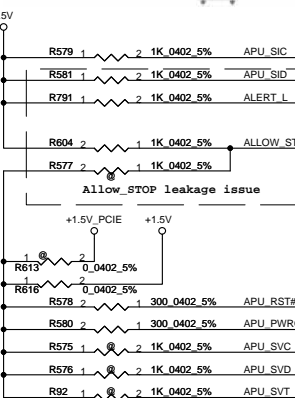
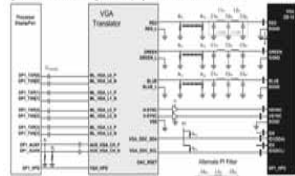


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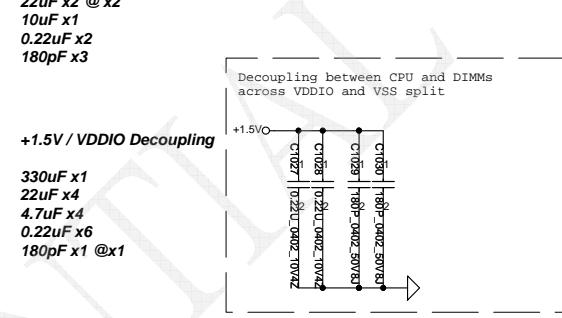
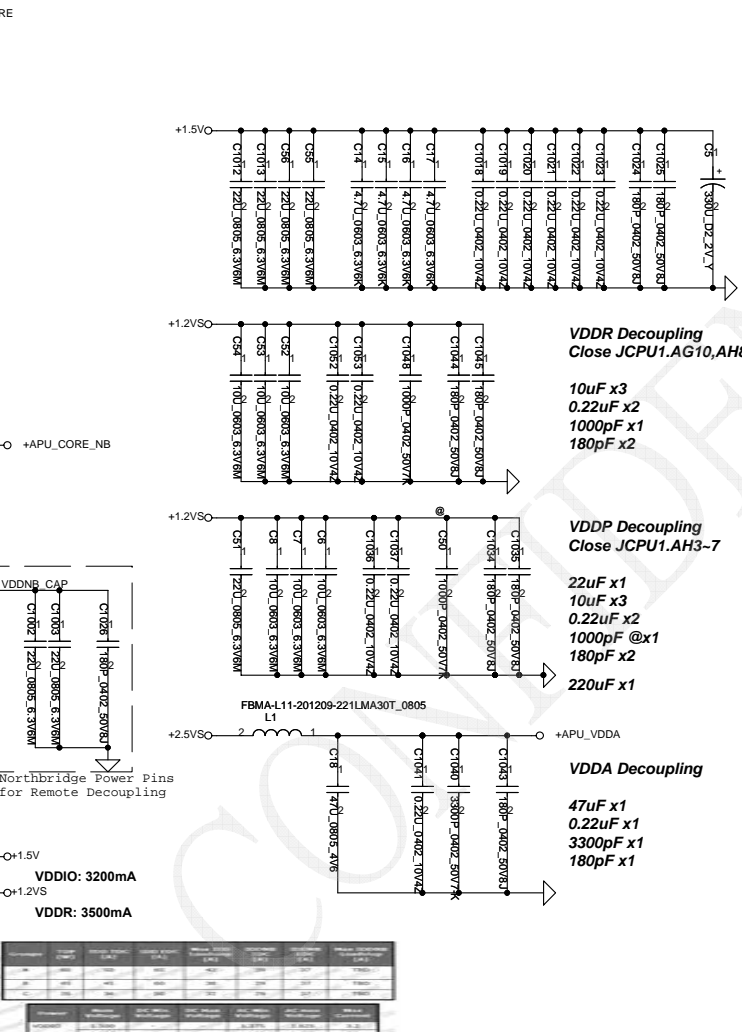
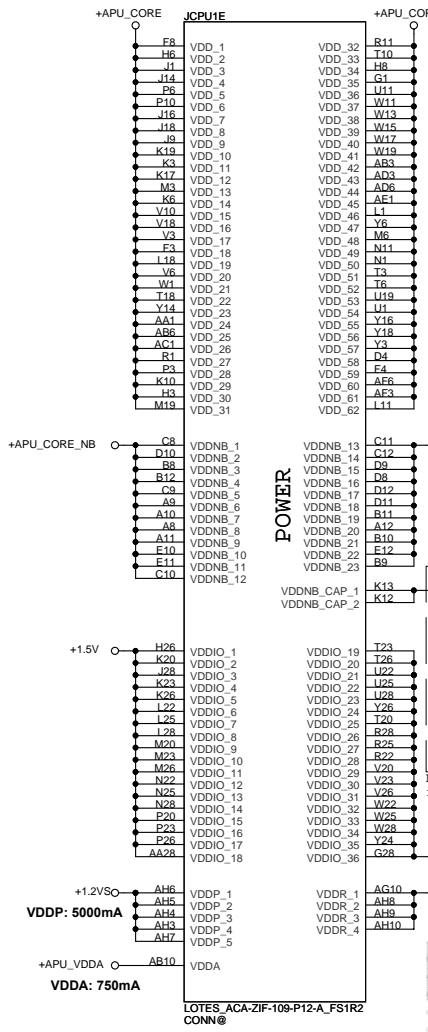
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Figure 44: Schematic Diagram—DisplayPort, Transistor and VGA



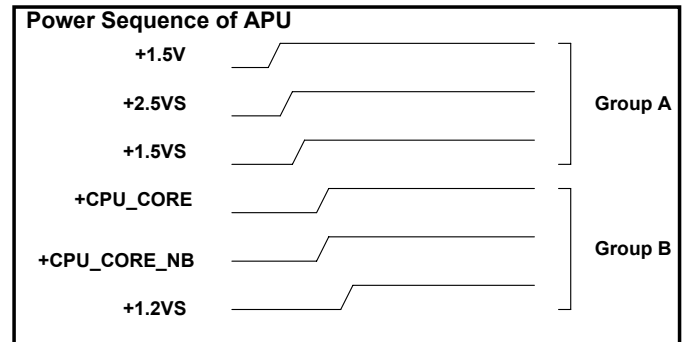
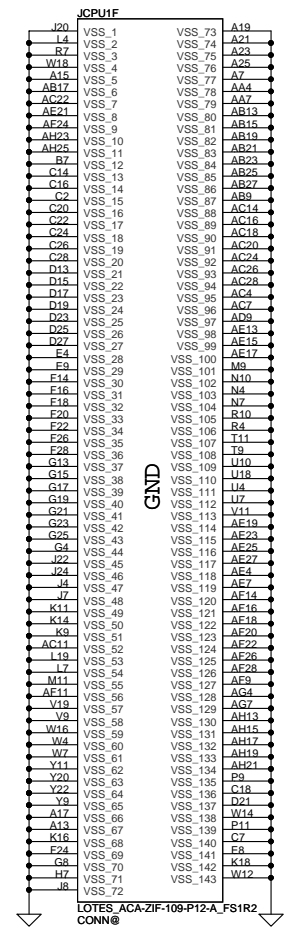
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Power Name	Consumption
VDD +CPU_CORE	60A
VDDNB +CPU_CORE_NB	37A
VDDIO +1.5V	3.2A
VDDP / VDDR +1.2VS	5A / 3.5A
VDDA +2.5VS	0.75A



+CPU_CORE Decoupling

330uF x 4 @ x1
22uF x 10
0.22uF x2
0.01uF x3
180pF x2 @ x1



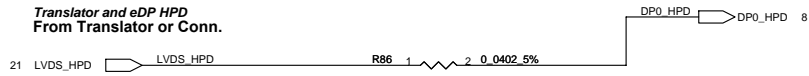
Decoupling Caps.

Pop / @	330uF	220uF	47uF	22uF	10uF	4.7uF	0.22uF	0.01uF	3300pF	1nF	180pF
Pumori 2.0	0	19/11	7	5	17	3	1	1 / 1	13/3		
Comal	7 / 2	1	1	19/11	7	4	17	3	1	1 / 1	14/2
P5WS5	7 / 2	1	1	13	3	8	19	3	1	4	16

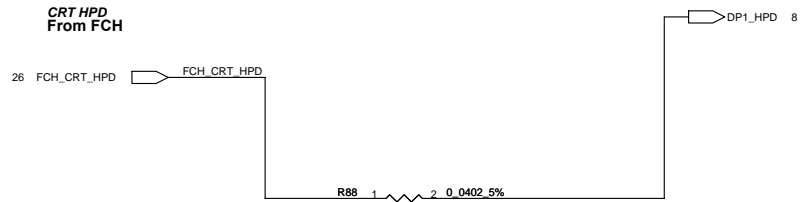
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HPD

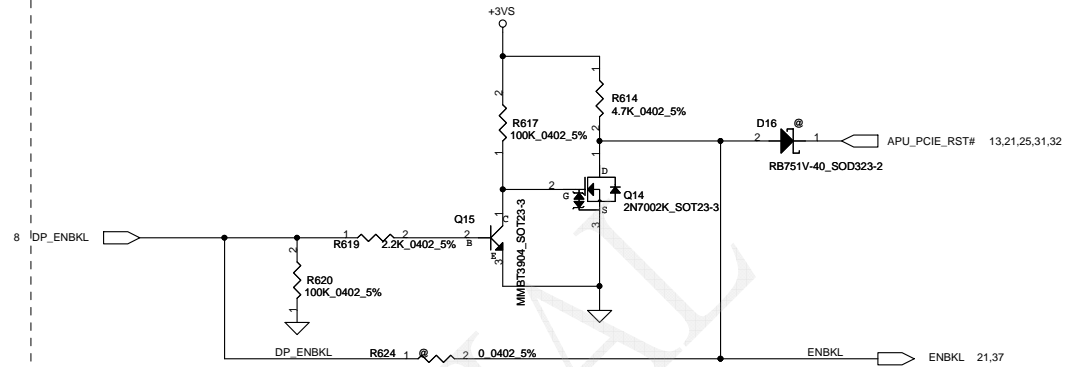
Translator and eDP HPD
From Translator or Conn.



CRT HPD
From FCH

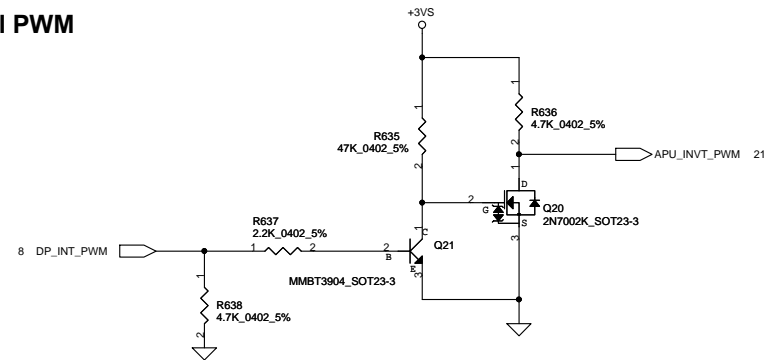


Panel ENBKL

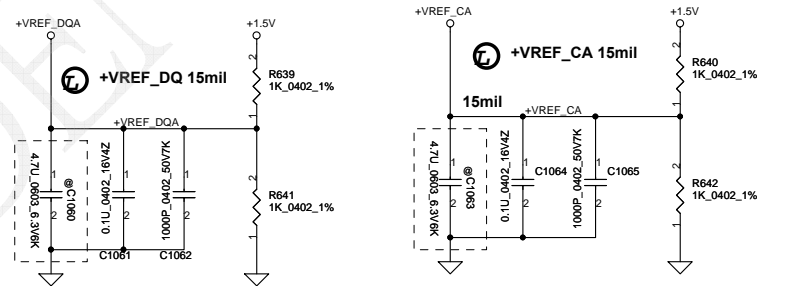
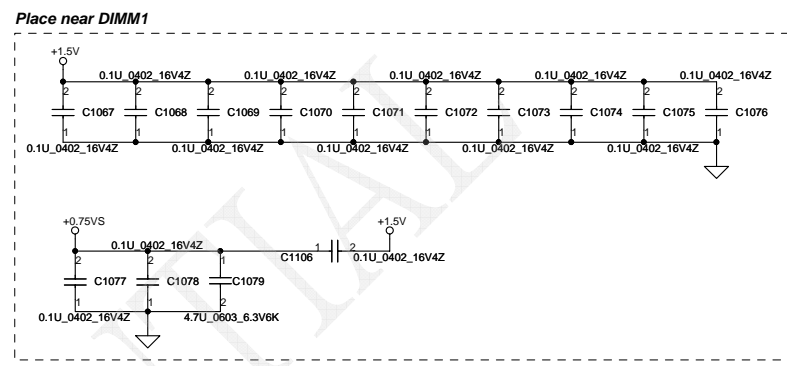
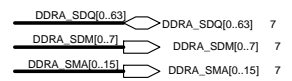
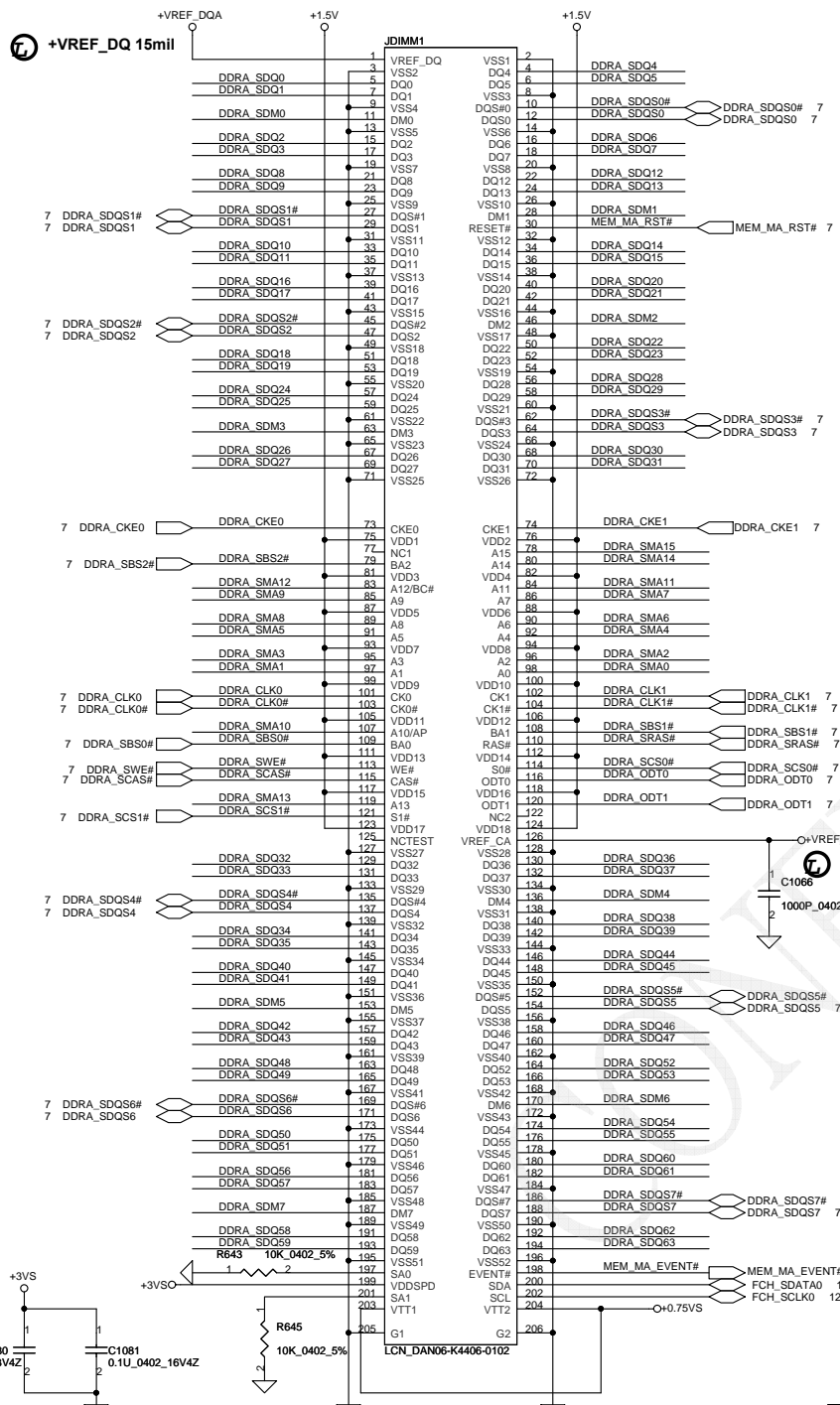


eDP Panel ENVDD

Panel PWM

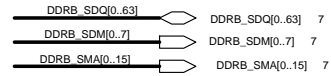
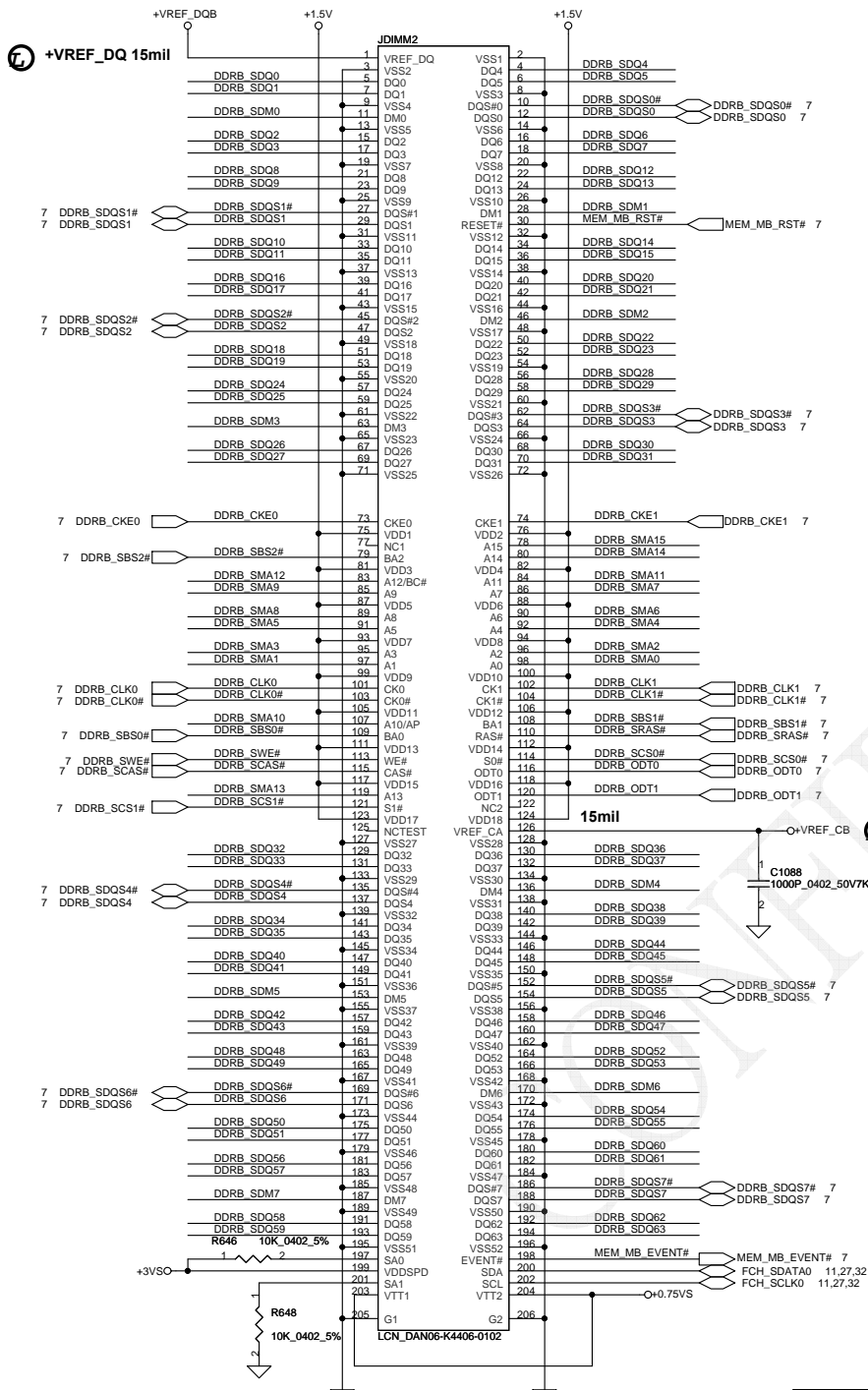


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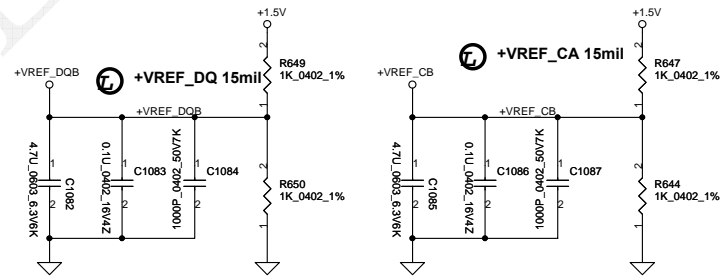
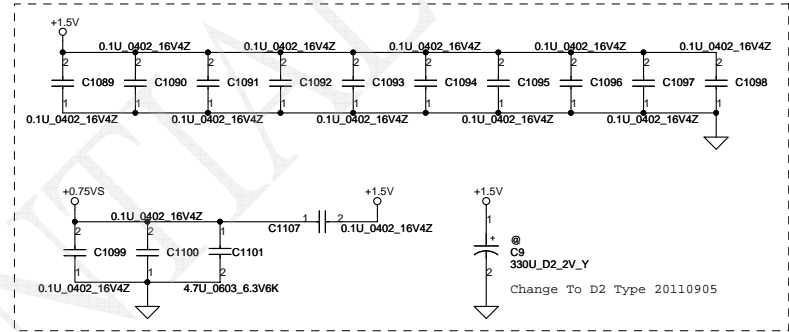


DIMM_A REV H:4mm
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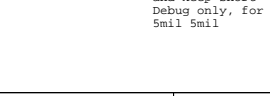
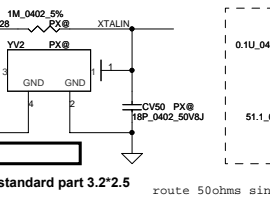
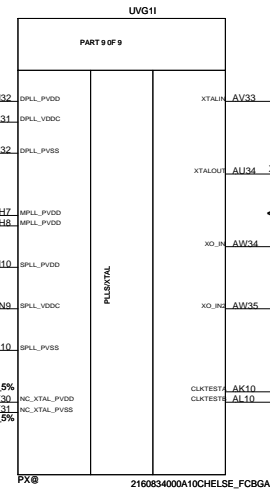
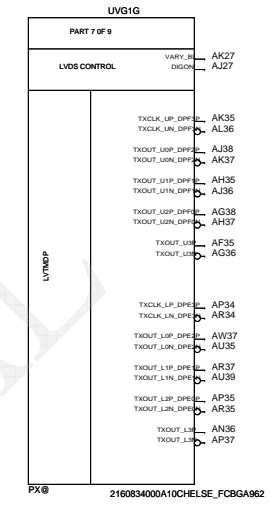
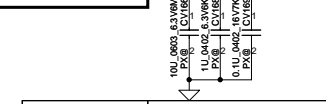
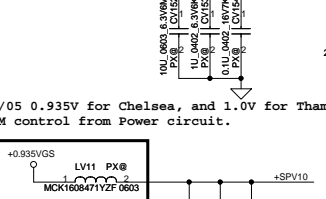
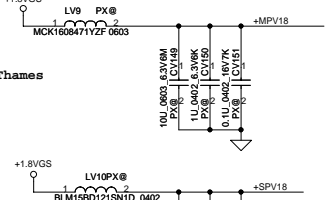
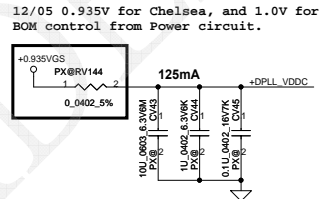
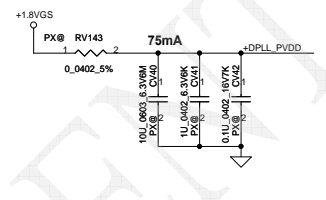
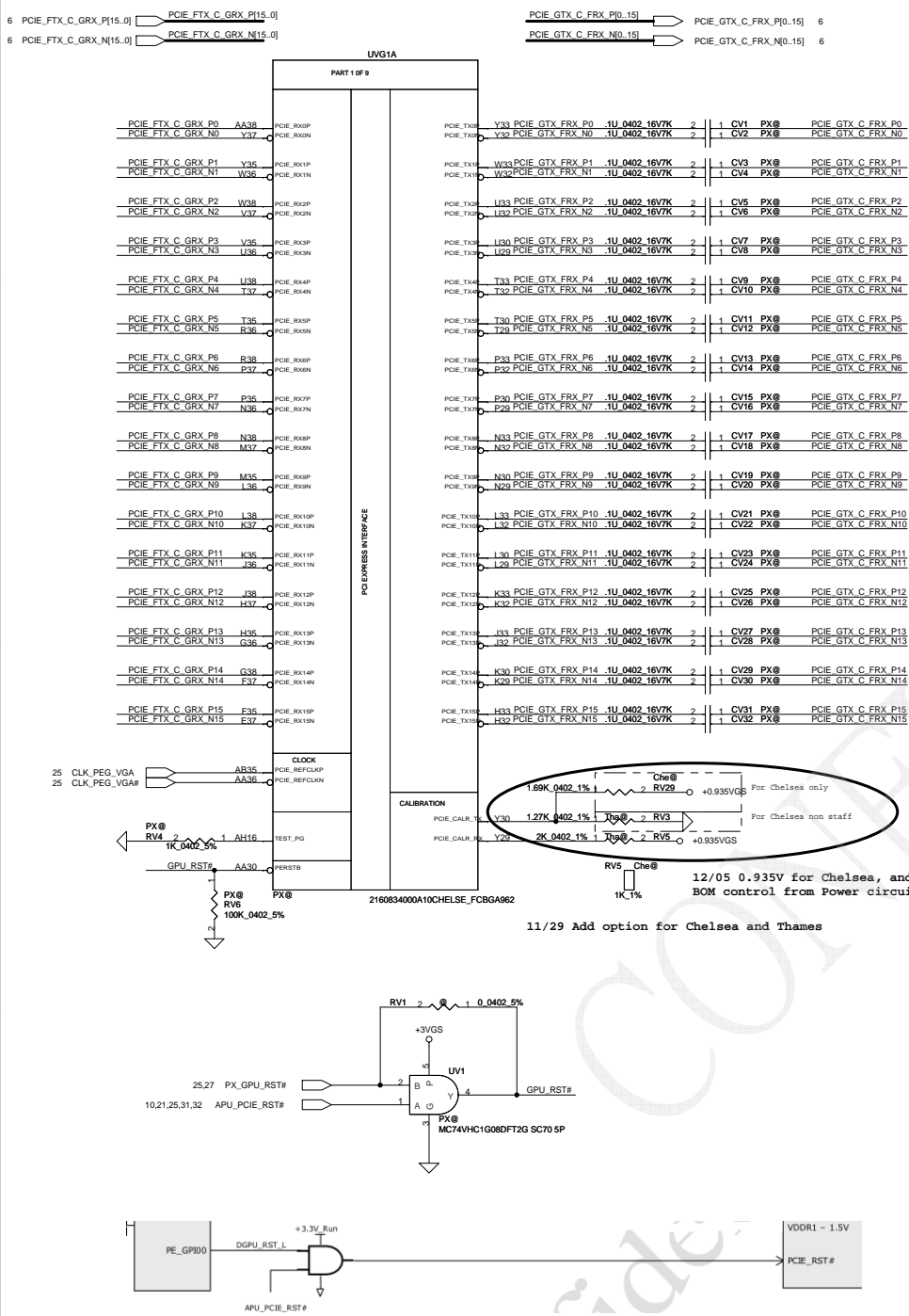
Place near DIMM2



DIMM_B REV H:8mm
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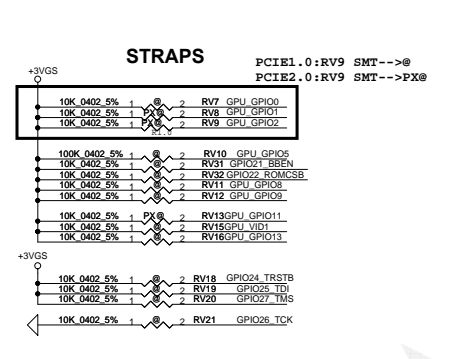
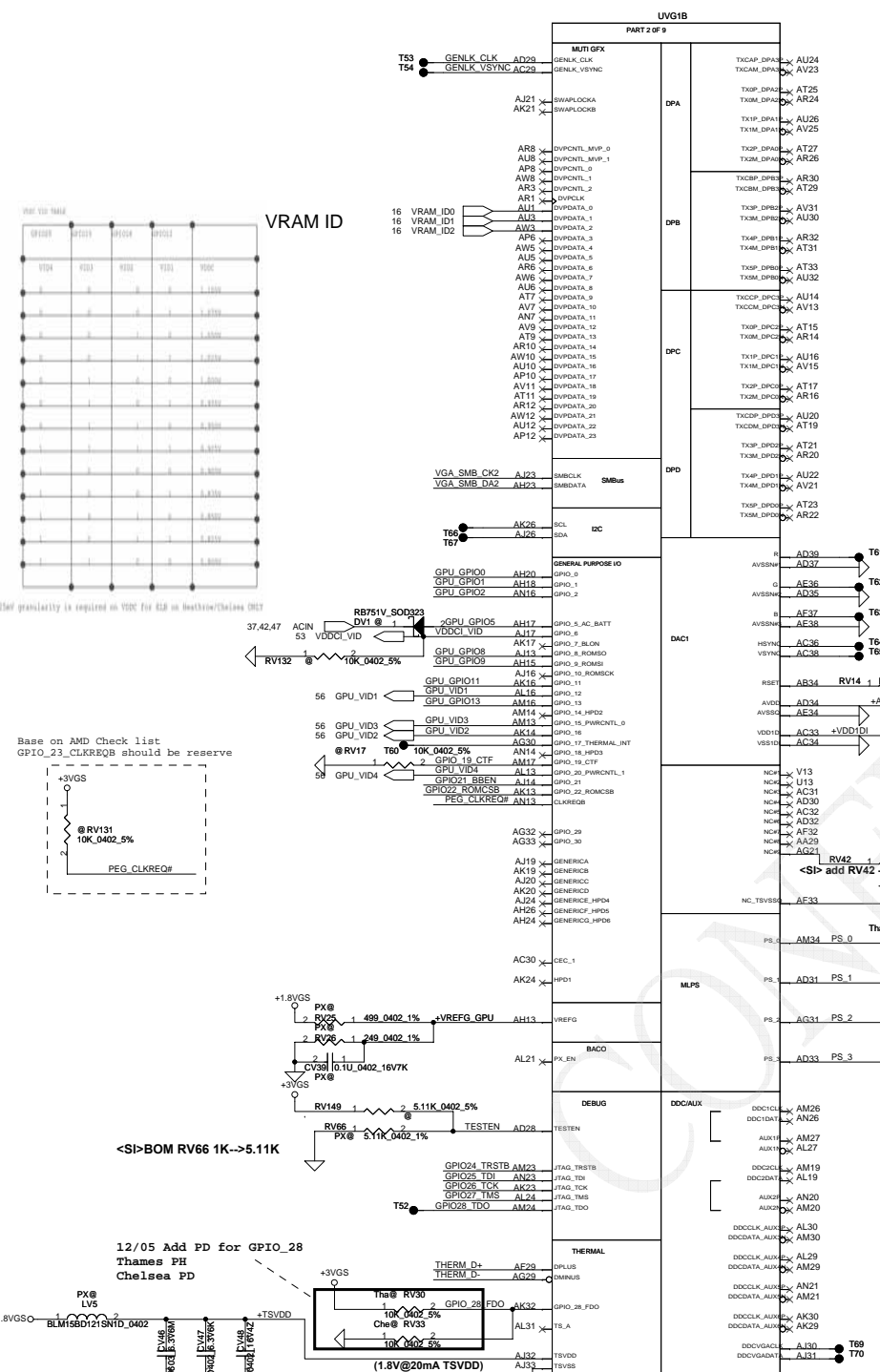
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LVDS Interface



route 50ohms single-ended/100ohms diff and keep short
Debug only, for clock observation, if not needed, DNI
5mil 5mil

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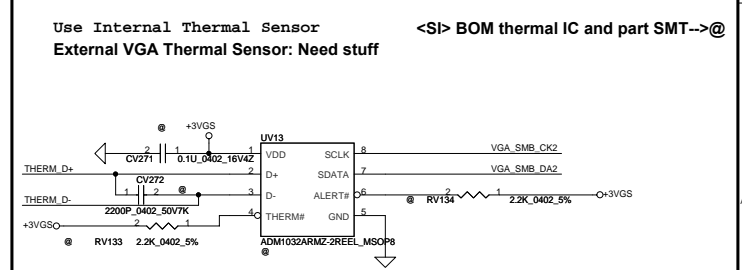
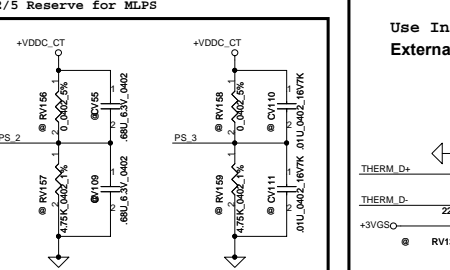
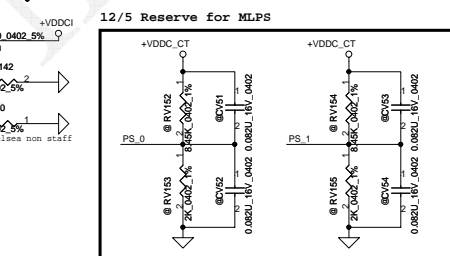
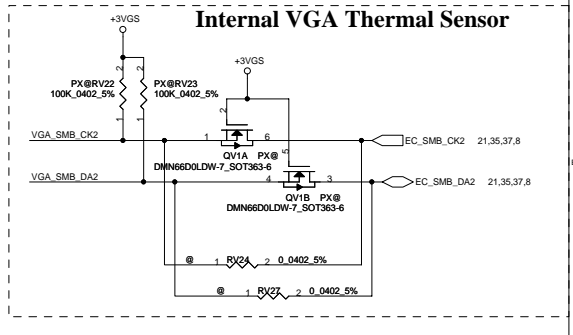


CONFIGURATION STRAPS			
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET			
RECOMMENDED SETTINGS (= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE)			
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS <all internal PD>	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE TRANSMITTER Power Saving Enable	0: 50% swing 1: Full swing X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS	0: disable 1: enable X
RSVD	GPIO2	Advertises PCIe speed when compliance test	0: 2.50T/s 1: 50T/s 0
RSVD	GPIO8	Internal use only. This Pad has an internal PD and Must be 0V at reset.	0
RSVD	H2SYNC	Internal use only. This Pad has an internal PD and Must be 0V at reset.	0
RSVD	GPIO21		0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0: disable 1: enable X
ROMIDCFG(z:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT GPIO13,12,11(config 2,1,0): internal PD. a) BIOS_ROM_EN=1, the config(z:0) defines the ROM type. b) BIOS_ROM_EN=0, the config(z:0) defines the primary aperture size. Memory apertures: 384MB 0:01 128MB 0:00 256MB 0:01 64MB 0:10	XXX
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GENERICC		0
AUD[1]	HSYNC	AUD[1] AUD[0] 0:0 No audio function 0:1 Audio for DisplayPort and HDMI if dongle is detected	11
AUD[0]	VSYN	1:0 Audio for DisplayPort only 1:1 Audio for both DisplayPort and HDMI	

AMD RESERVED CONFIGURATION STRAPS
ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET

GPIO21 H2SYNC GENERICC GPIO2 GPIO8

TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)

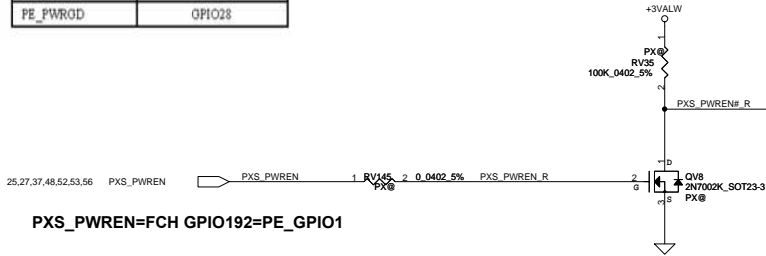


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Name	FCH Pin Assignments
PE_GPIO0	GPIO191
PE_GPIO1	GPIO192
PE_PWRGD	GPIO28

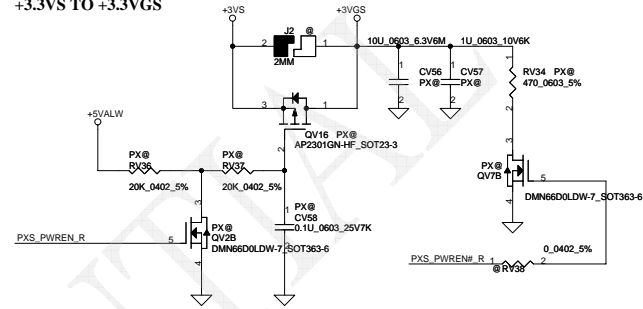
GPU_Reset

PWREN



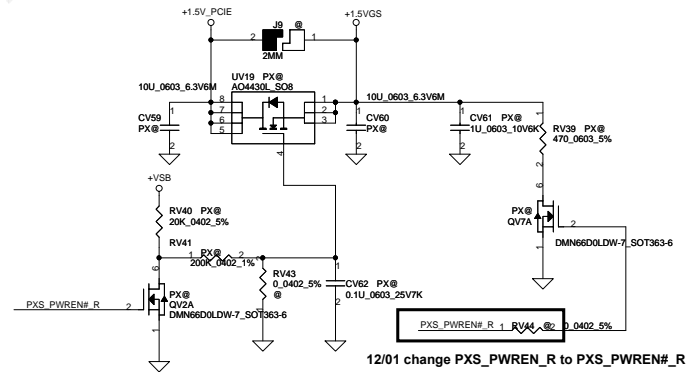
PXS_PWREN=FCH GPIO192=PE_GPIO1

+3.3VS TO +3.3VGS



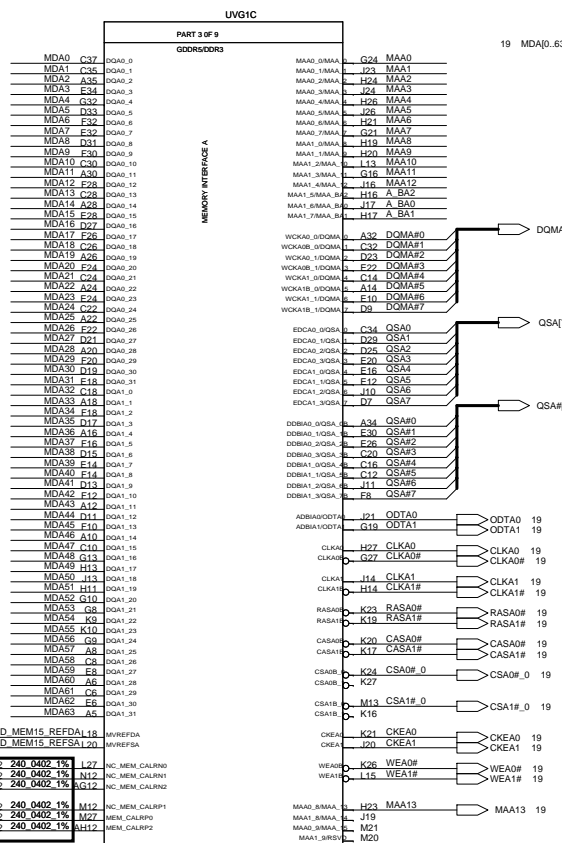
+1.5V_PCIE TO +1.5VGS

Add +1.5VGS DC DC

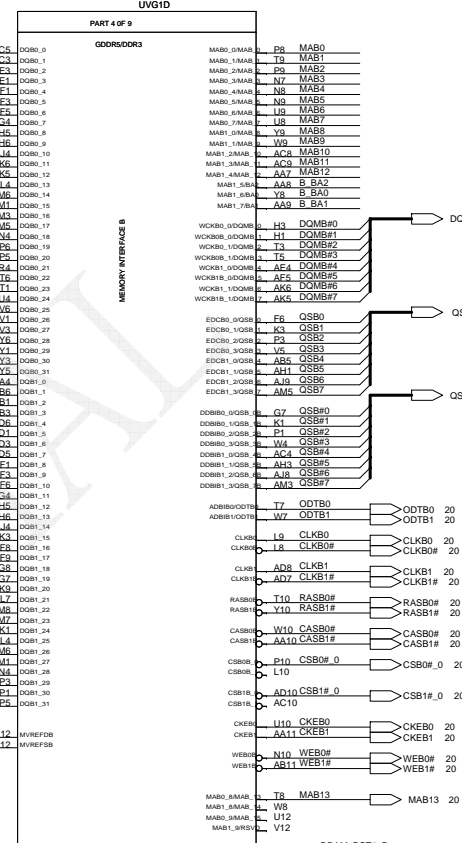


12/01 change PXS_PWREN_R to PXS_PWREN#_R

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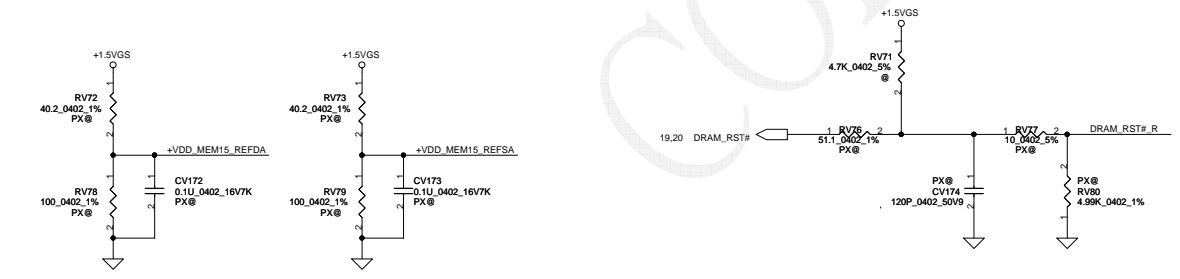
Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2
Samsung 2GB PN:SA000047Q00	RV56	RV58	RV60
Hynix 2GB PN:SA00003YO70	RV59	RV58	RV60
Samsung 1GB PN:SA00004GS00	RV56	RV57	RV61
Hynix 1GB PN:SA000041S20	RV59	RV57	RV61

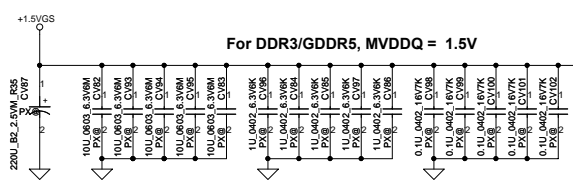


For Thramet: PX# 2160834000A10CHELSE_FCBGA962
RV63, RV64 non staff
RV65, RV66 from 240ohm
change to 120ohm



This basic topology should be used for DRAM_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory, DRAM Load and board to pass Reset Signal Spec.
Place all these components very close to GPU (Within 25mm) and keep all component close to each other (within 5mm) except Rser2





VDDR1	CRB	Design
0.1u	6	6
1u	10	5
10u	6	5

VDD_CT	CRB	Design
0.1u	1	1
1u	3	3
10u	1	1

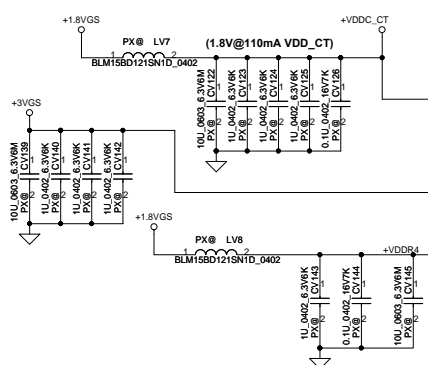
VDDR3	CRB	Design
1u	3	3
10u	1	1

VDDR4	CRB	Design
0.1u	1	1
1u	1	1

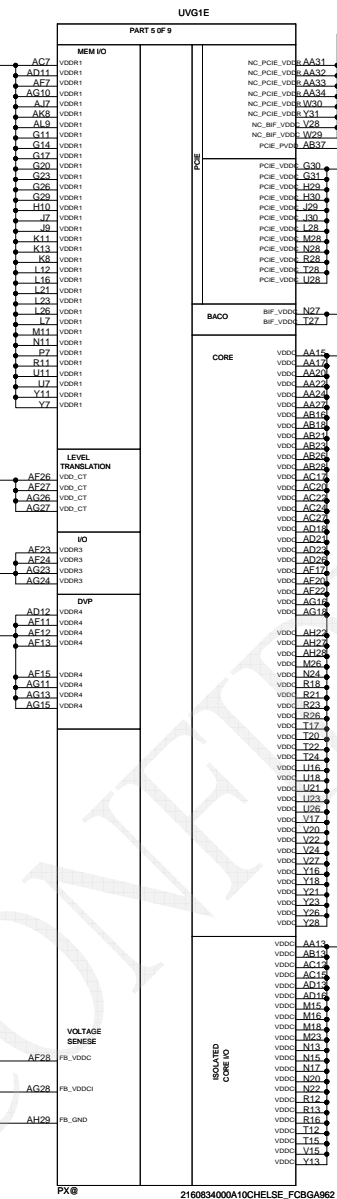
MPV18	CRB	Design
0.1u	2	1
1u	2	1
10u	1	1

SPV18	CRB	Design
0.1u	1	1
1u	1	1
10u	1	1

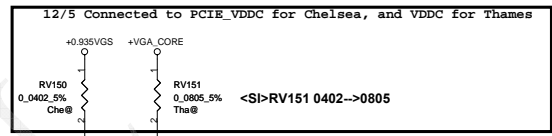
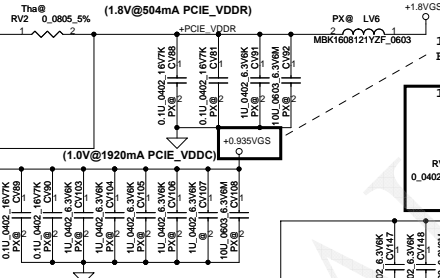
SPV10	CRB	Design
0.1u	1	1
1u	1	1
10u	1	1



VCC_GPU_SENSE & VSS_GPU_SENSE needs to be routed as differential pair



2160834000A10CHELSE_FCBGA862



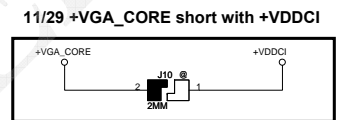
Change power rail same as PCIE_VDDC
Must be connected to PCIE_VDDC (0.935 V) on "Heathrow"/"Chelsea" for both BACO and non-BACO designs

For Chelsea, Delete 2*1U

PCIE_VDDR	CRB	Design
0.1u	2	2
1u	1	1
10u	1	1

PCIE_VDDC	CRB	Design
1u	7	5 (1@)
10u	1	1

VDDC	CRB	Design
1u	30	25
10u	10	1
22u	0	1

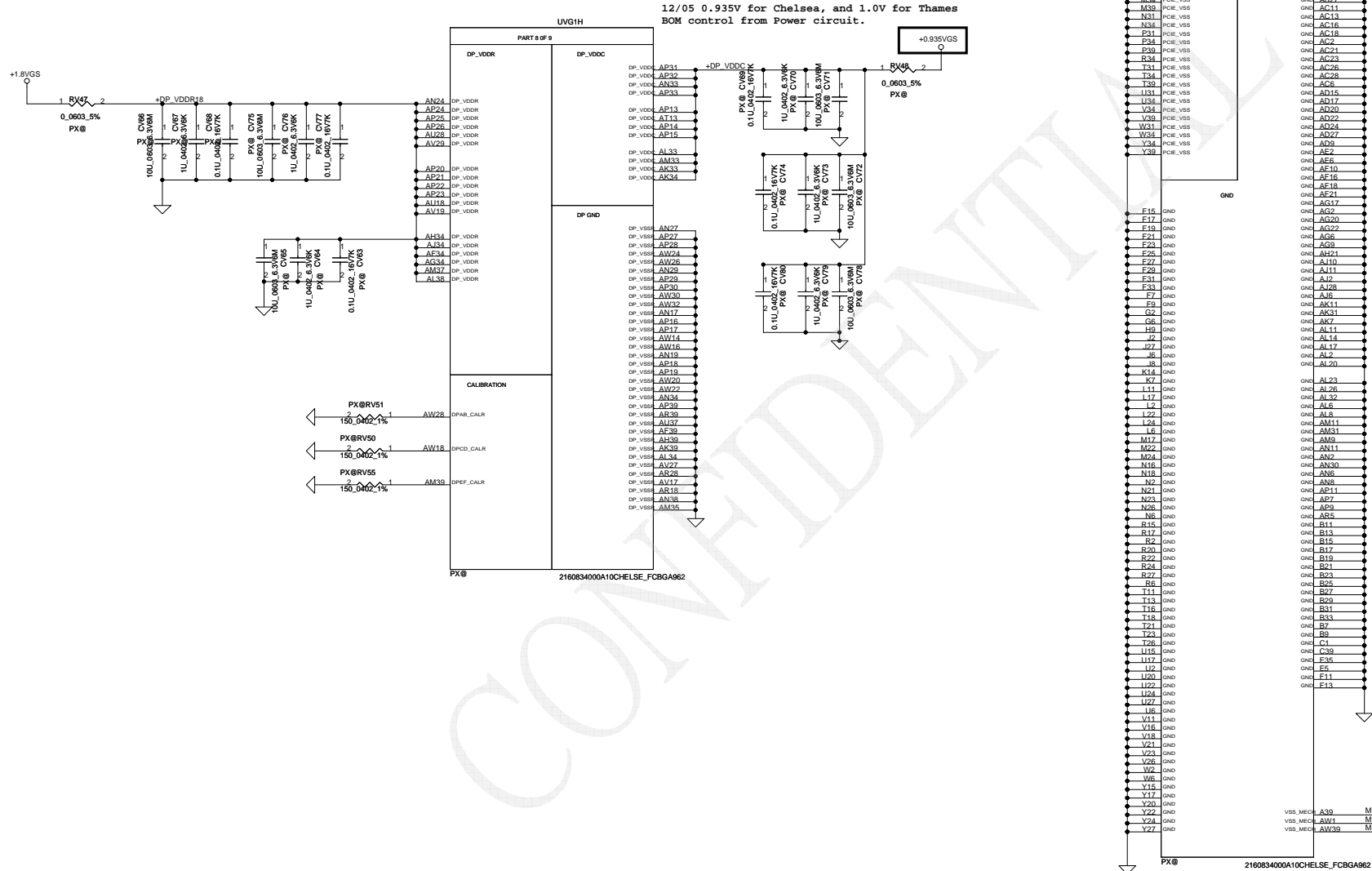


11/29 +VGA_CORE short with +VDDCI

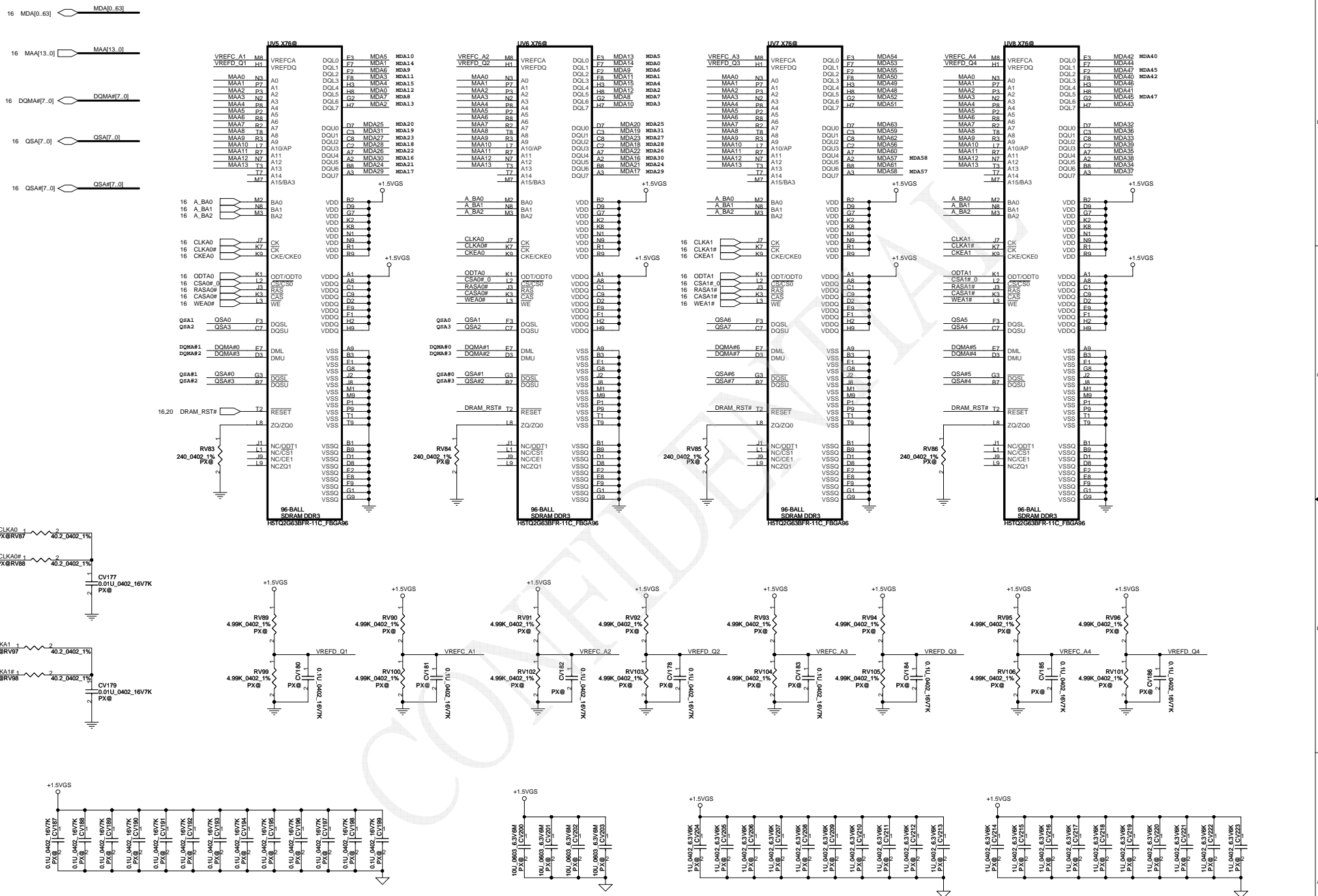
(GDDR3/DDR3 1.12V@4A VDDCI)
(GDDR5 1.12V@16A VDDCI)

VDDCI	CRB	Design
1u	10	9
10u	3	2
22u	0	1

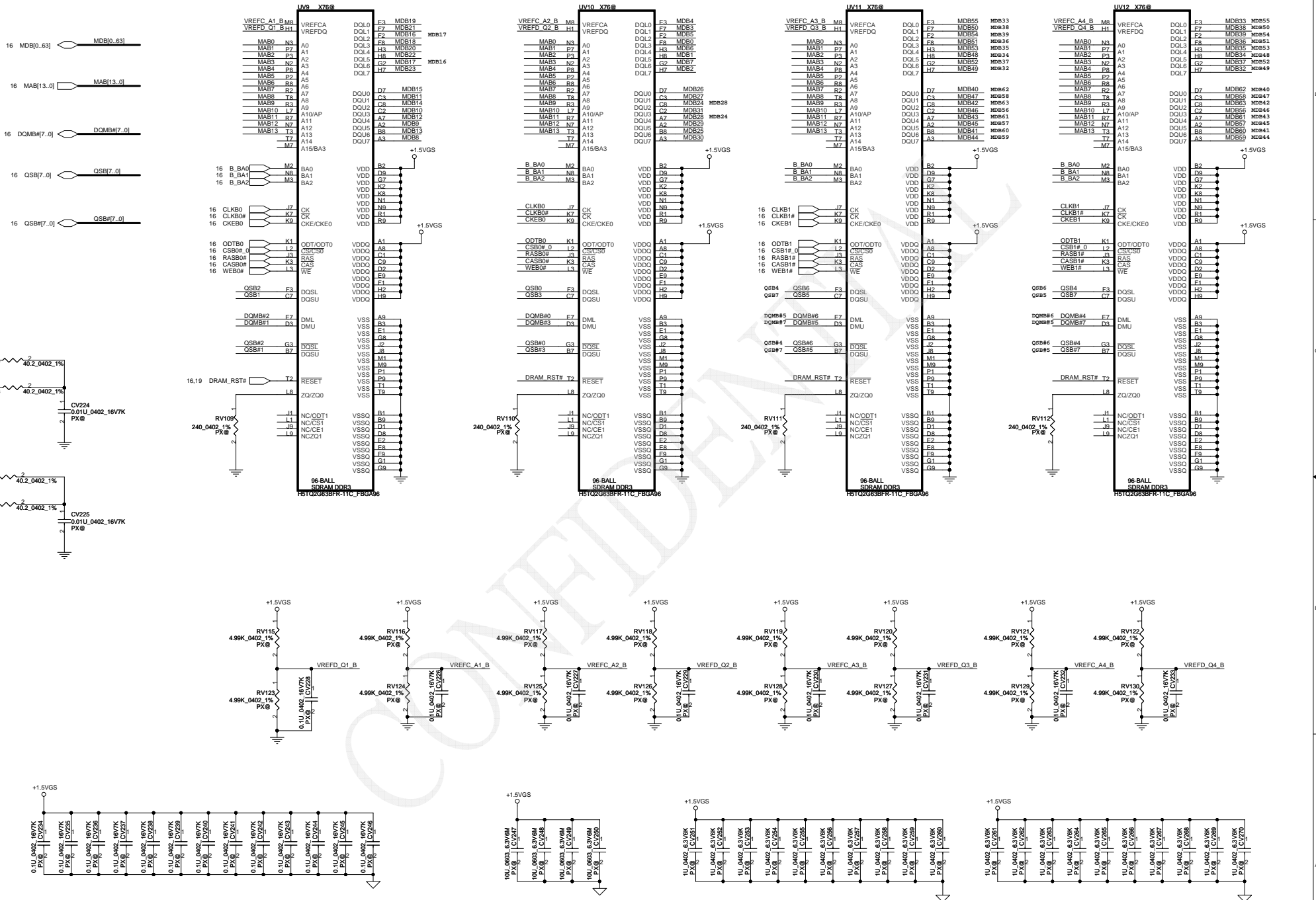
VDDCI and VDDC should have separate regulators with a merge option on PCB
For Madison, Park, Capilano, Robson, Seymour and Whistler, VDDCI and VDDC can share one common regulator



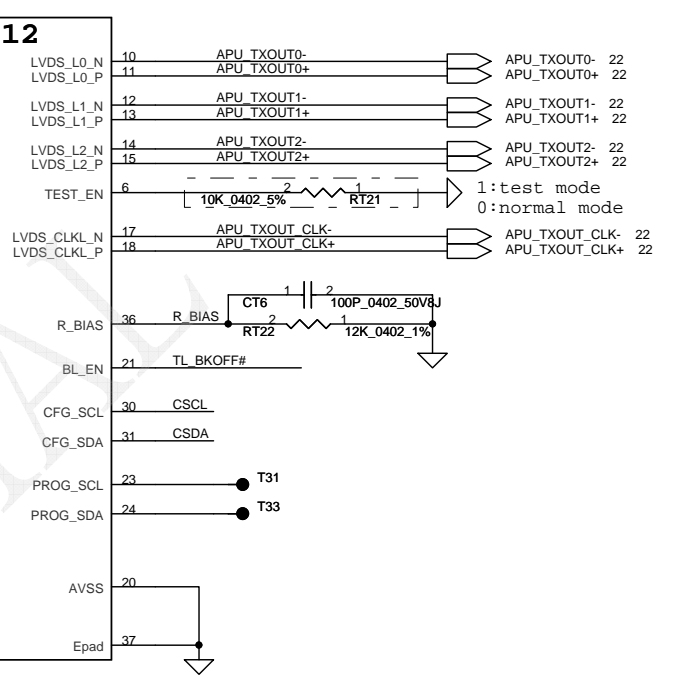
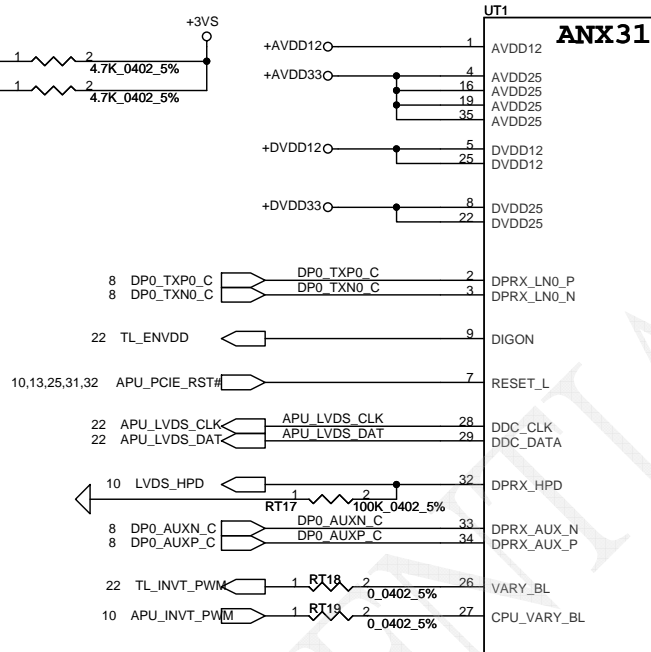
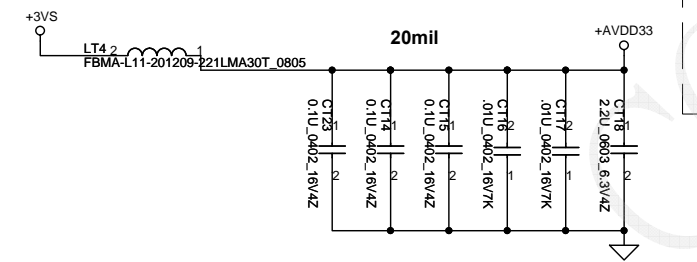
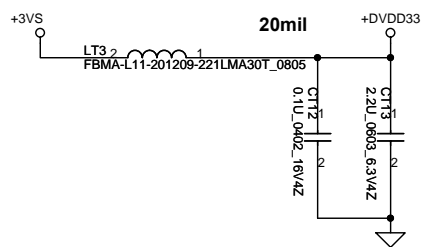
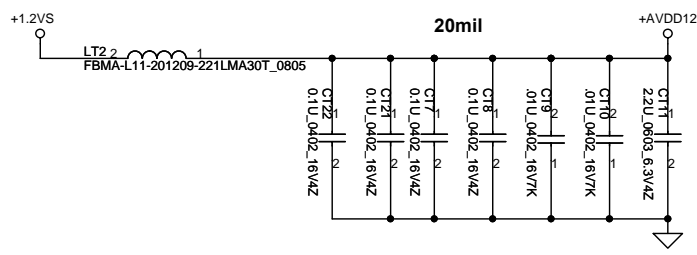
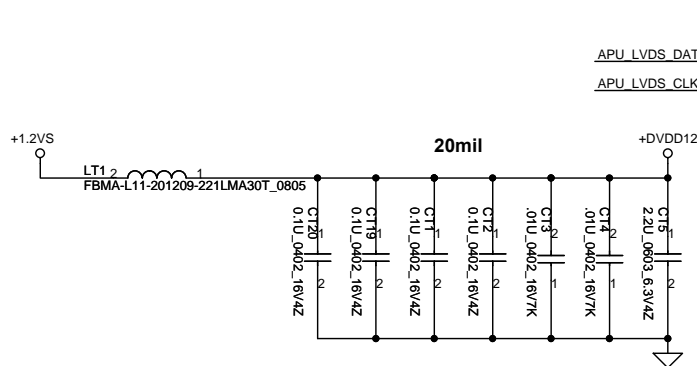
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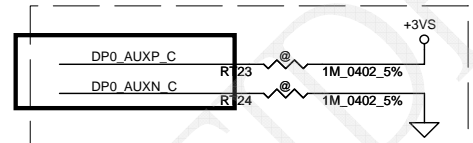
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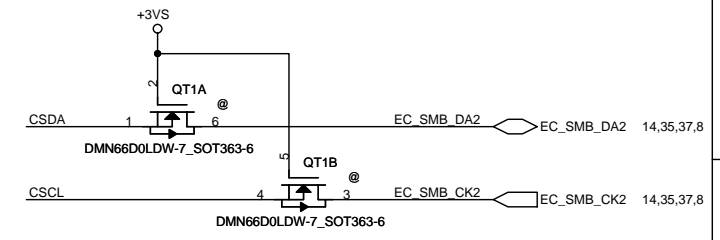
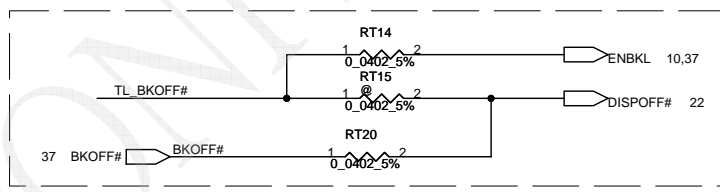
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12/01 Swap DPO_AUXP_C/DPO_AUXN_C for vender guideline

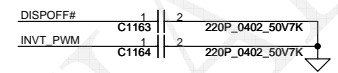
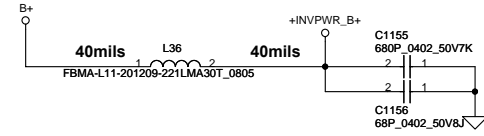
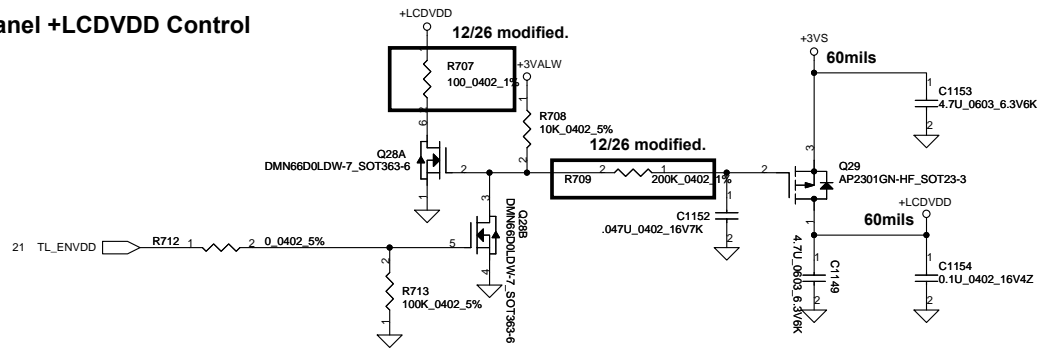


Place via on each trace bus and let resistor very close the via

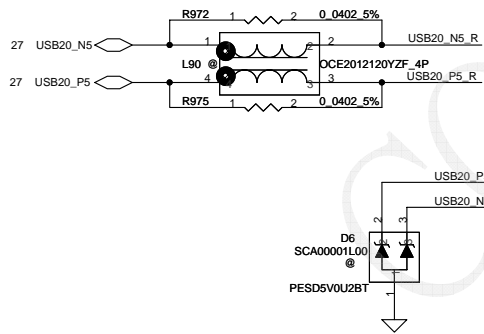
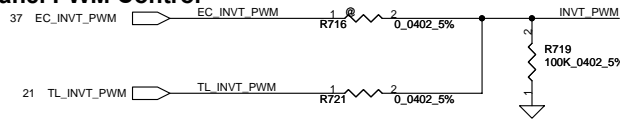


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Panel +LCDVDD Control

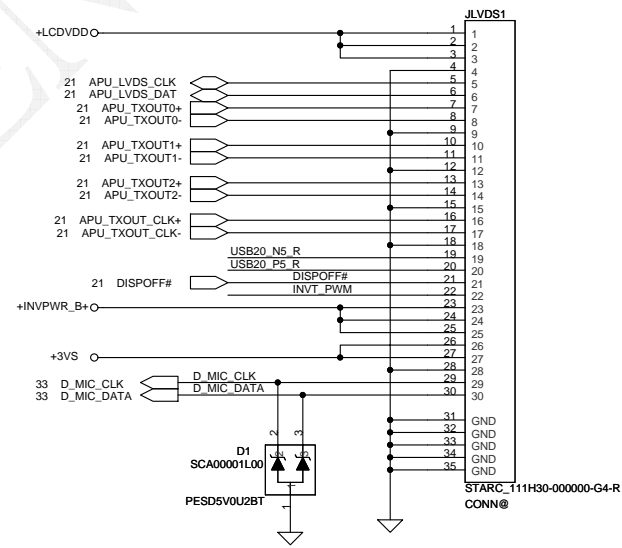


Panel PWM Control



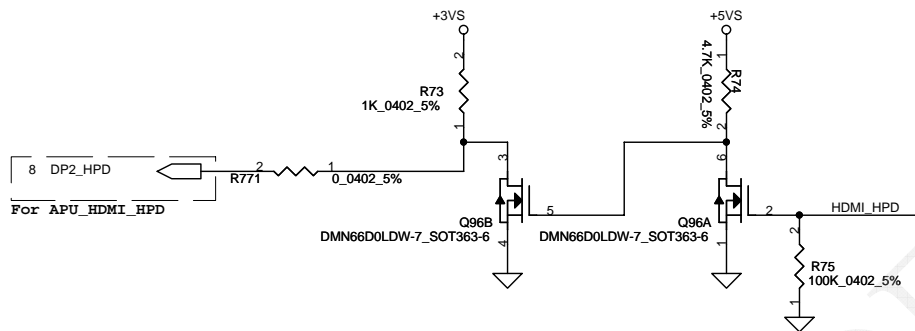
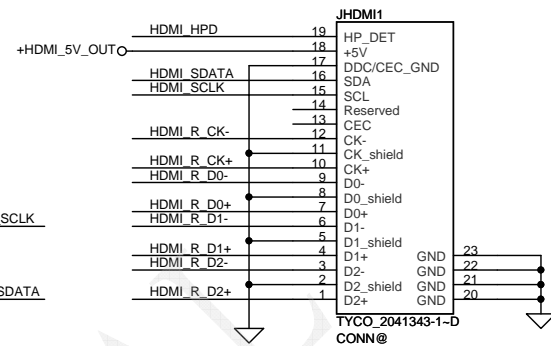
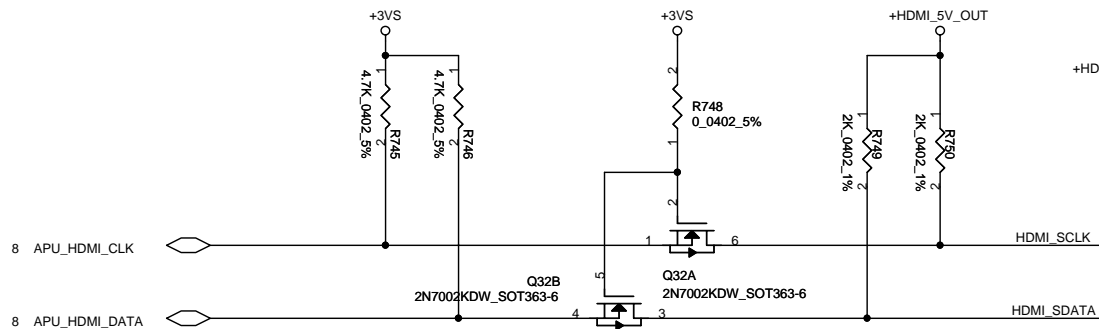
<Translator LVDS Output>

LVDS Connector

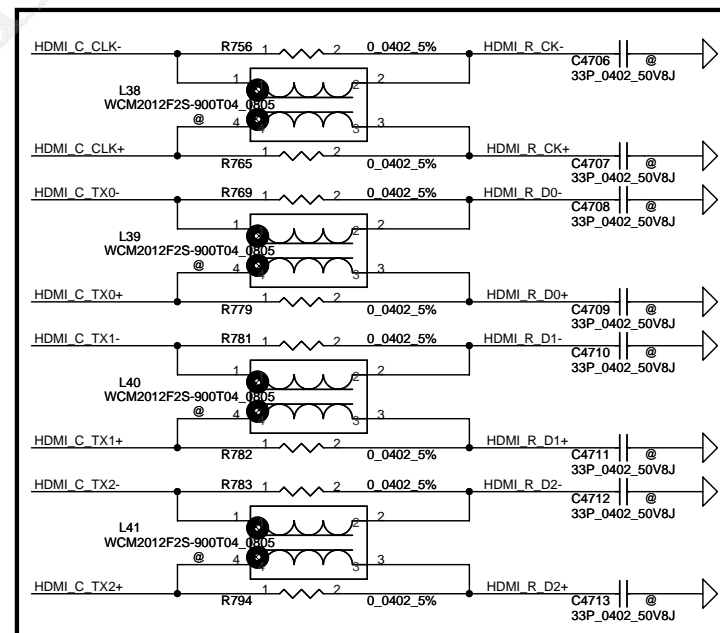


no updated.
11/10 follow QCL50

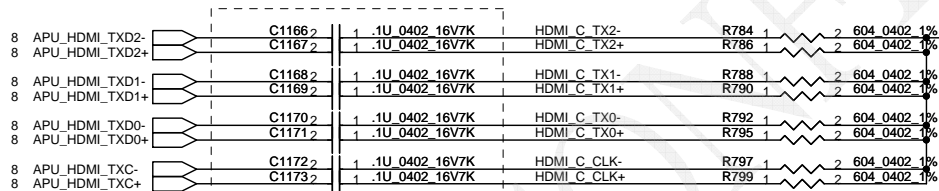
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12/7 Swap signals for routing smoothly

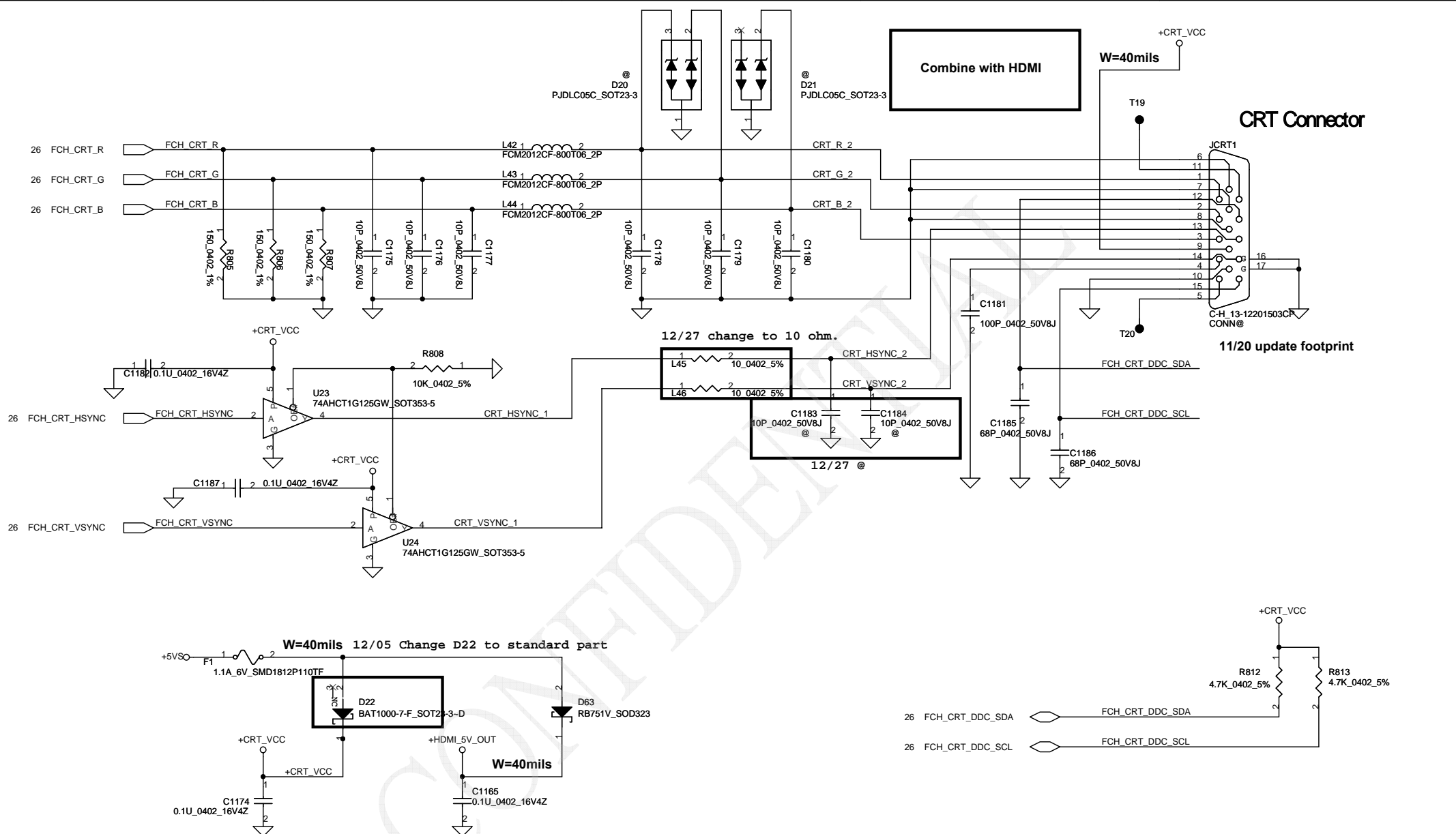


Close to HDMI conn

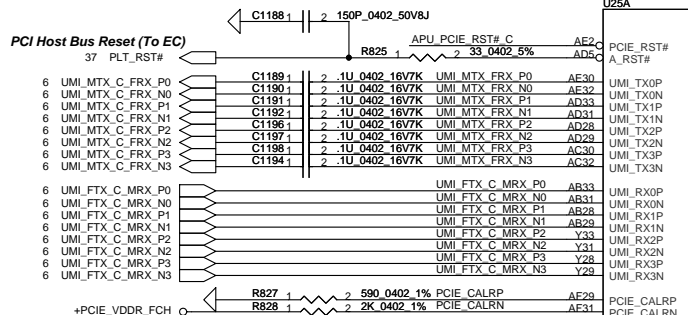


From APU

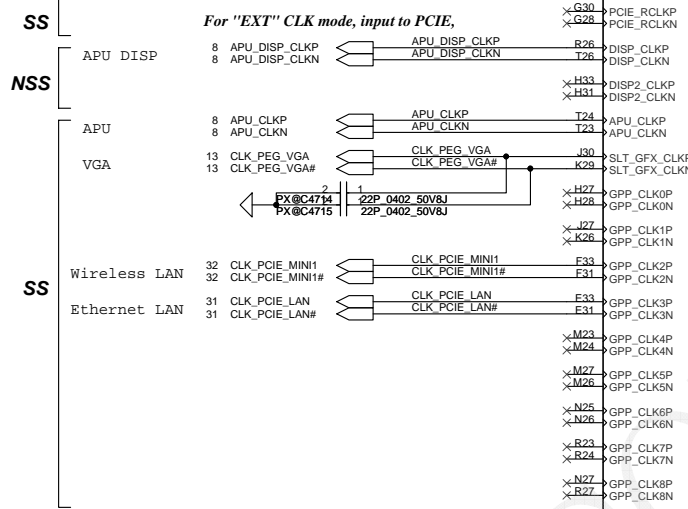
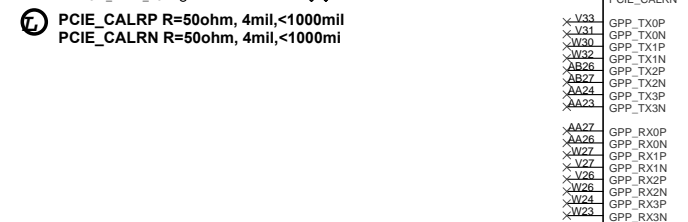
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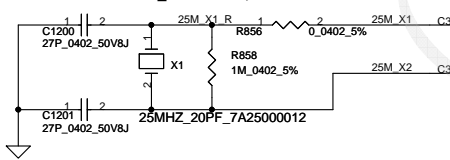
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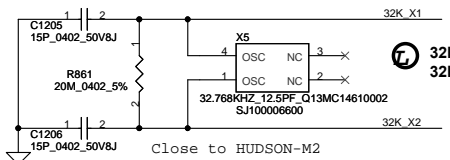
PCI_CALRN R=50ohm, 4mil, <1000mil
 PCI_CALRN R=50ohm, 4mil, <1000mil



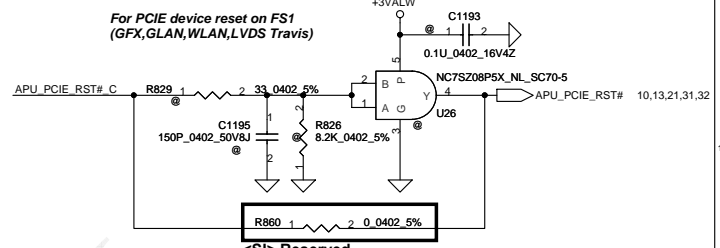
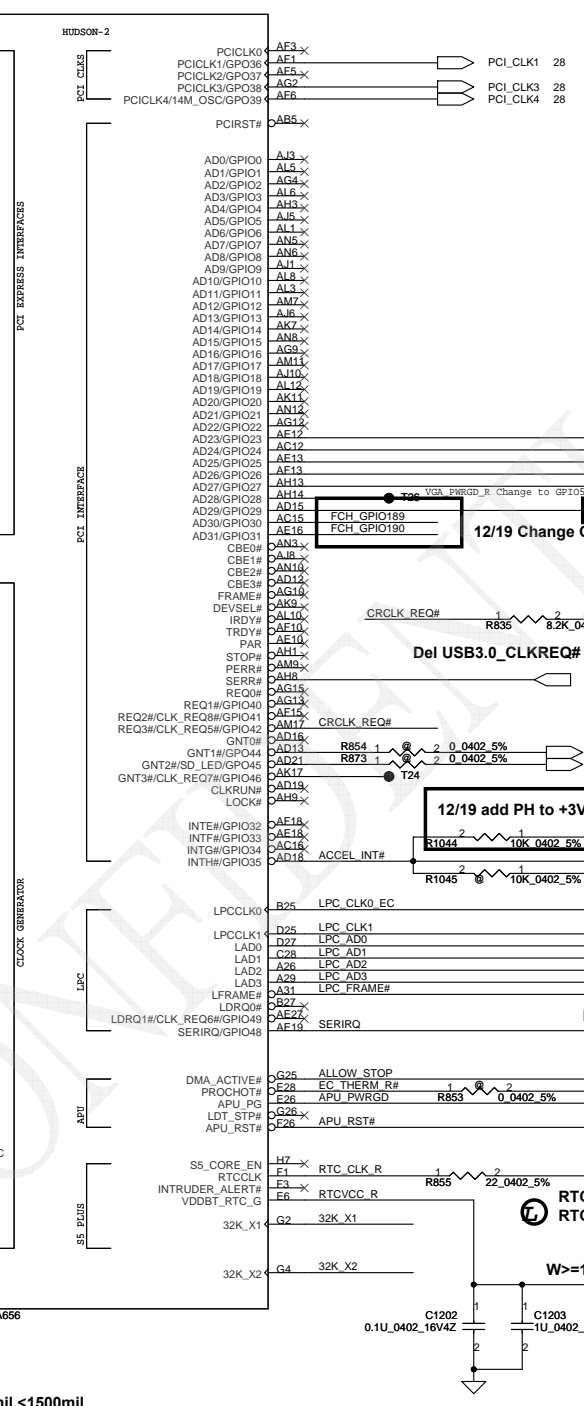
25M_X1 and 25M_X1_R=50ohm, 4mil
 25M_X2=50ohm, 4mil



C1205, C1206
 Change for G3
 RTC timing issue
 <improve amplitude>



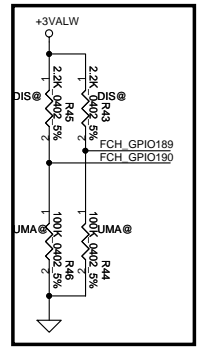
32K_X1=50ohm, 4mil, <1500mil
 32K_X2=50ohm, 4mil, <1500mil



Project SKU ID

GPIO189 (use VGA)	L(N)	R44	H(Y)	R43
GPIO190 (use PX)	L(N)	R46	H(Y)	R45

DIS is High
 DIS is High

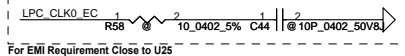


12/19 Change GPIO pin.

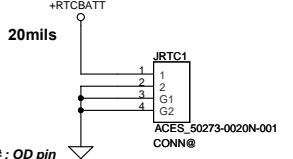
12/19 Change GPIO pin.

12/19 add PH to +3VS.

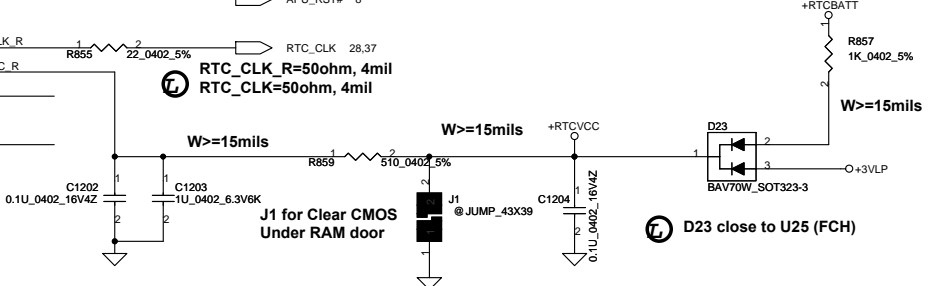
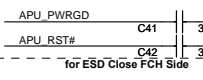
12/01 change to INTH for BIOS request



For EMI Requirement Close to U25



APU_PG/APU_RST#/LDT_STP#: OD pin
 DMA_ACTIVE#: INVD, 0.8V threshold
 PROCHOT#: IN, 0.8V threshold
 LDT_STP#: No use, NC
 DMA active. The FCH drives the DMA_ACTIVE# to APU to notify DMA activity. This will cause the APU to reestablish the UMI link quicker.



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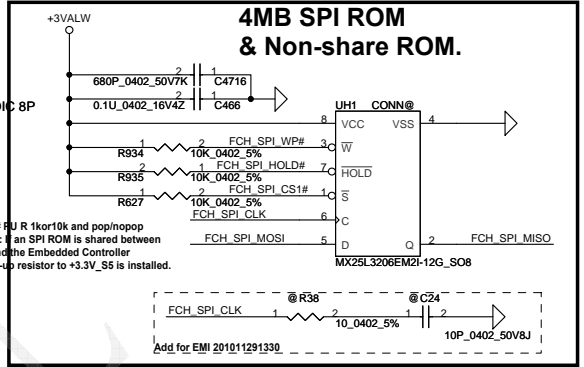
HDD1
 30 SATA_STX_DRX_P0
 30 SATA_STX_DRX_N0
 30 SATA_DTX_SRX_N0
 30 SATA_DTX_SRX_P0
ODD
 30 SATA_STX_DRX_P1
 30 SATA_STX_DRX_N1
 30 SATA_DTX_SRX_N1
 30 SATA_DTX_SRX_P1

SATA STX DRX P0 AK19
 SATA STX DRX N0 AM19
 SATA DTX SRX N0 AL20
 SATA DTX SRX P0 AN20
 SATA STX DRX P1 AN22
 SATA STX DRX N1 AL22
 SATA DTX SRX N1 AH20
 SATA DTX SRX P1 AJ20

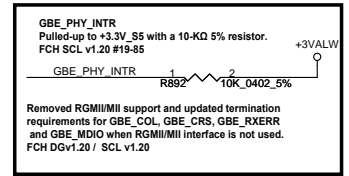
U25B
 SATA_TX0P
 SATA_TX0N
 SATA_RX0N
 SATA_RX0P
 SATA_TX1P
 SATA_TX1N
 SATA_RX1N
 SATA_RX1P
 SATA_TX2P
 SATA_TX2N
 SATA_RX2N
 SATA_RX2P
 SATA_TX3P
 SATA_TX3N
 SATA_RX3N
 SATA_RX3P
 SATA_TX4P
 SATA_TX4N
 SATA_RX4N
 SATA_RX4P
 SATA_TX5P
 SATA_TX5N
 SATA_RX5N
 SATA_RX5P
 NC6
 NC7
 NC8
 NC9
 NC10
 NC11
 NC12
 NC13
 SATA_CALRP
 SATA_CALRN
 SATA_LED#
 SATA_LED#
 SATA_ACT#/GPIO67
 SATA_X1
 SATA_X2
 FANOUT0/GPIO52
 FANOUT1/GPIO53
 FANOUT2/GPIO54
 FANIN0/GPIO56
 FANIN1/GPIO57
 FANIN2/GPIO58
 ODD_PWR
 TEMPIN0/GPIO171
 TEMPIN1/GPIO172
 TEMPIN2/GPIO173
 TEMPIN3/TALERT#/GPIO174
 VIN0/GPIO175
 VIN1/GPIO176
 VIN2/SDAT1#/GPIO177
 VIN3/SDATO#/GPIO178
 VIN4/SLOAD_1/GPIO179
 VIN5/SCLK_1/GPIO180
 VIN6/GBE_STAT3/GPIO181
 VIN7/GBE_LED3/GPIO182
 NC1
 NC2
 NC3
 NC4
 NC5

HUDSON-2
 SD_CLK/CLK_2/GPIO73
 SD_CMD/LOAD_2/GPIO74
 SD_CD/GPIO75
 SD_WP/GPIO76
 SD_DATA0/SDAT1_2/GPIO77
 SD_DATA1/SDATO_2/GPIO78
 SD_DATA2/GPIO79
 SD_DATA3/GPIO80
 GBE_COL
 GBE_CRS
 GBE_MDCK
 GBE_MDIO
 GBE_RXCLK
 GBE_RXD3
 GBE_RXD0
 GBE_RXD1
 GBE_RXD0
 GBE_RXCTL/RXDV
 GBE_RXERR
 GBE_TXCLK
 GBE_TXD3
 GBE_TXD2
 GBE_TXD1
 GBE_TXD0
 GBE_TXCTL/TXEN
 GBE_PHY_PD
 GBE_PHY_RST#
 GBE_PHY_INTR
 V6 FCH_SPI_MISO
 V5 FCH_SPI_MOSI
 V3 FCH_SPI_CLK_R
 T6 FCH_SPI_CS#
 C1 FCH_SPI_WP#
 FCH_CRT_R
 FCH_CRT_G
 FCH_CRT_B
 FCH_CRT_HSYNC
 FCH_CRT_VSYNC
 FCH_CRT_DDC_SDA
 FCH_CRT_DDC_SCL
 FCH_CRT_HPDP
 R5
 R6
 R7
 R8
 R9
 P3
 P1
 M1
 M5
 AG18
 AH15
 A28
 NC3
 G27
 L4

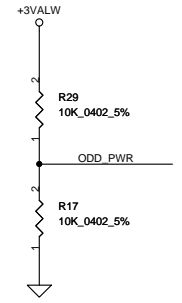
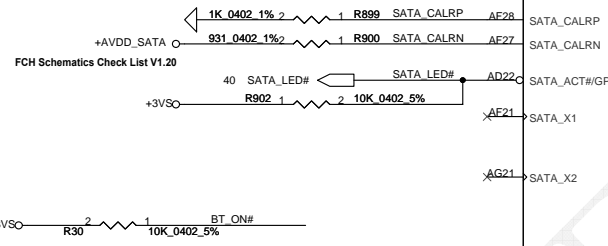
W25Q32BVSSIG 8P
 AL14
 AN14
 AH12
 AH13
 AH14
 AH15
 AH16
 AC4
 AD3
 AD9
 AW0
 AB8
 AH7
 AE7
 AD7
 AG8
 AD1
 AB7
 AE9
 AG6
 AE8
 AD8
 AB9
 AC2
 AA7
 W9
 GBE_COL / GBE_CRS / GBE_MDIO
 GBE_RXERR / Left unconnected.
 FCH_SCL V1.20 19-35
 R35 1 2 0 0402 5% FCH_SPI_CLK
 R896 1 2 150 0402 1% FCH_CRT_R
 R897 1 2 150 0402 1% FCH_CRT_G
 R898 1 2 150 0402 1% FCH_CRT_B
 R301 1 2 715 0402 1%
 R903 1 2 100 0402 1%
 R904 1 2 10K 0402 5%
 R10
 R11
 R12



Check CS# for R 1k or 10k and pop/nopop
 SCL v1.20: If an SPI ROM is shared between
 the FCH and the Embedded Controller
 a 10-K pull-up resistor to +3.3V_S5 is installed.



SATA_CALRP=35ohm,<1000mil
SATA_CALRN=35ohm,<1000mi



AUXCAL <1000mil

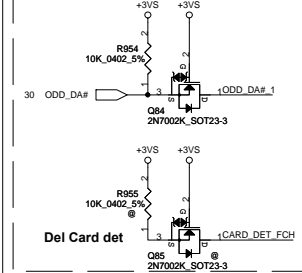
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FCH_PCIE_RST# IS FOR PCIE DEVICES ON Hudson-M2/M3

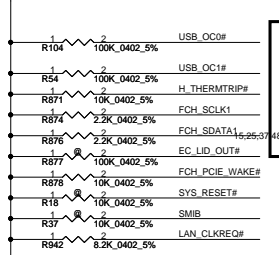
THERMTRIP: Need level shift from +3VALW to +1.5V Note: Ensure FCH internal pull-up resistor to +3.3V S5 is disabled to prevent leakage when APU is powered down.

SM bus 0->S0 PWR domain SM bus 1->S5 PWR domain

FCH GEVENT (S5 domain) with isolation circuit to avoid leakage



Change GPIO fellow Pinout



For FCH internal debug use

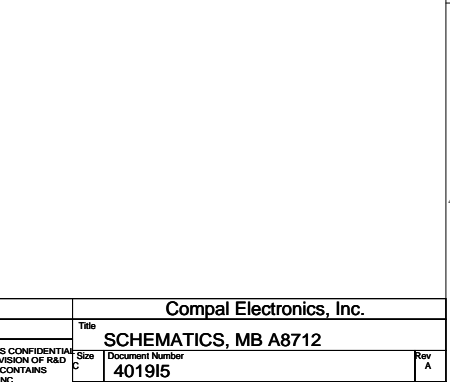
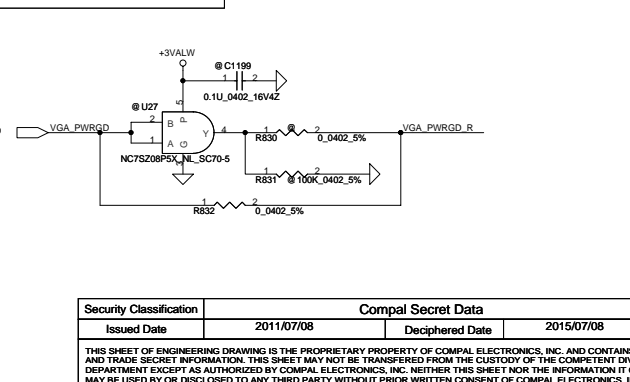
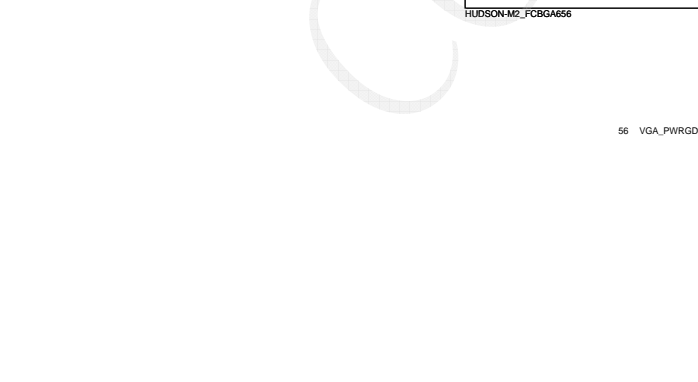
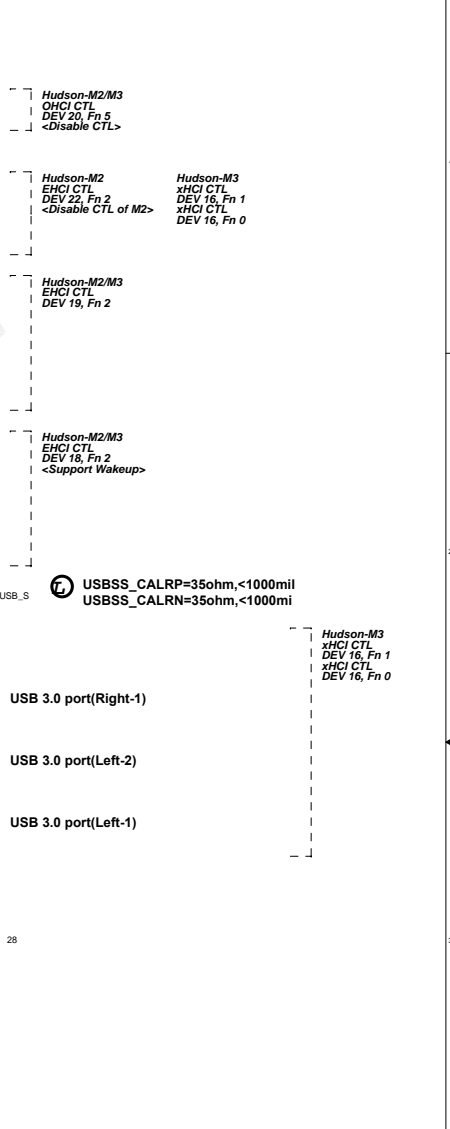
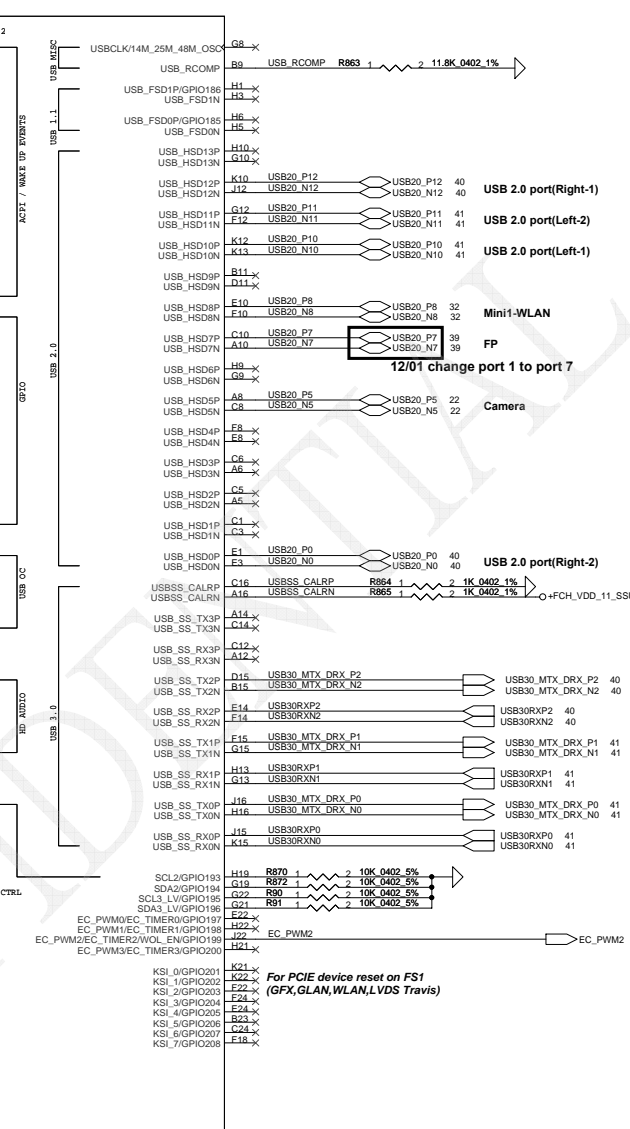
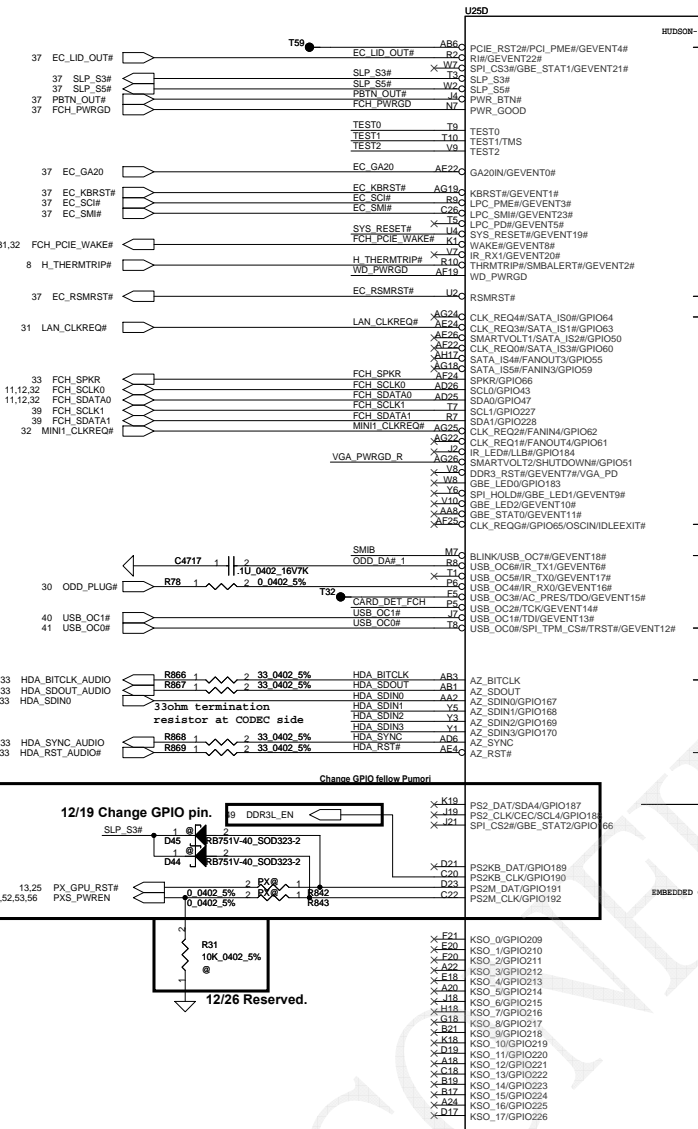
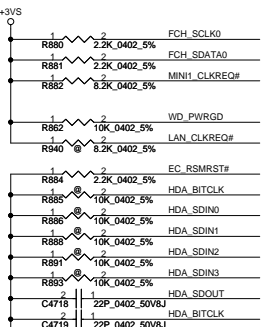
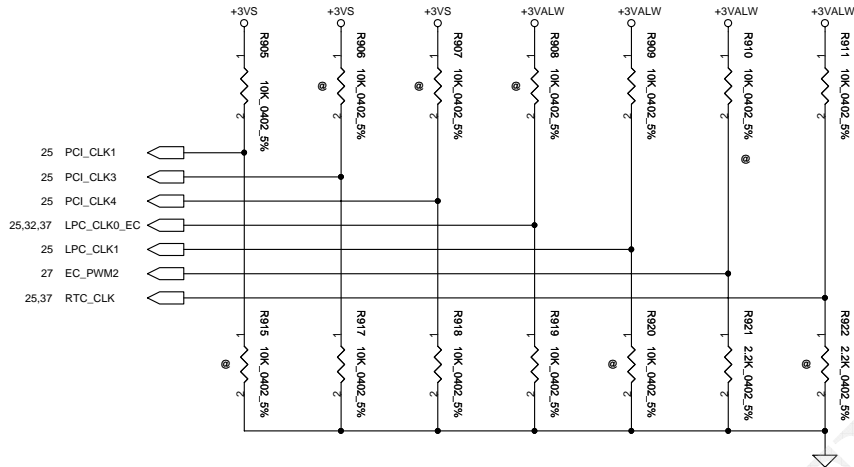


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STRAP PINS

Change to SPI

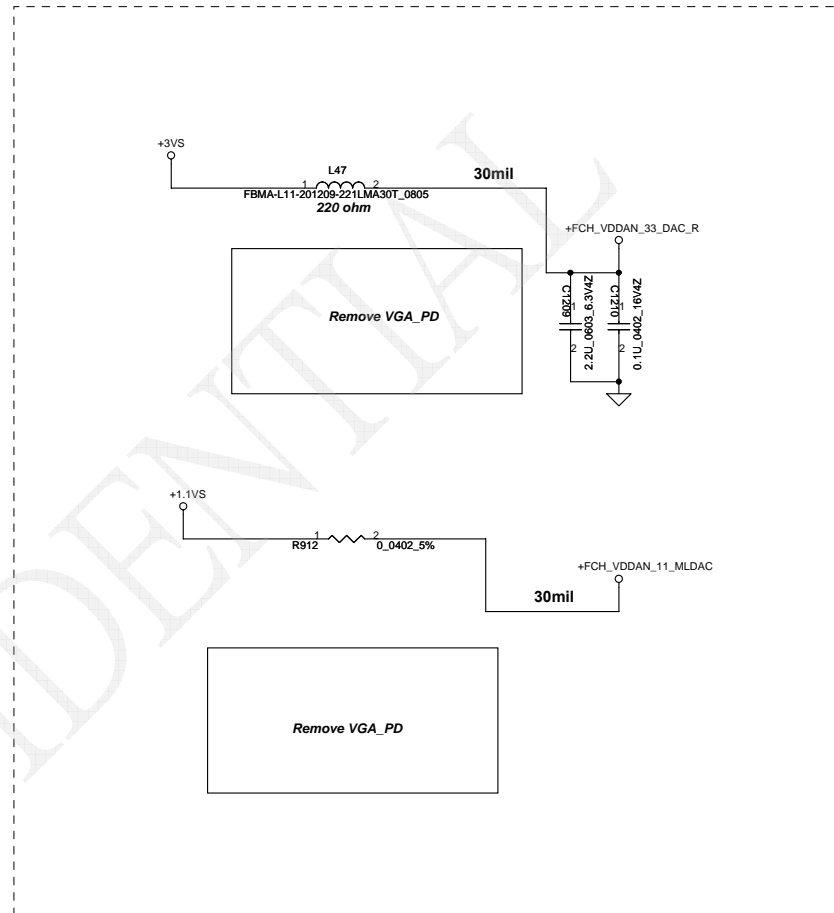
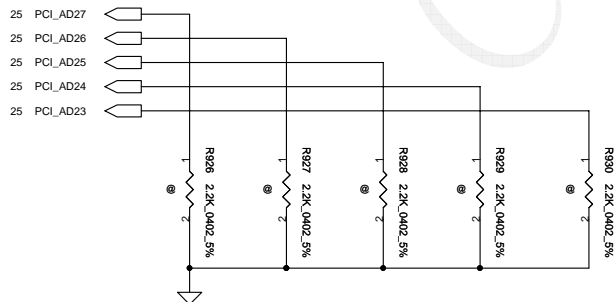
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

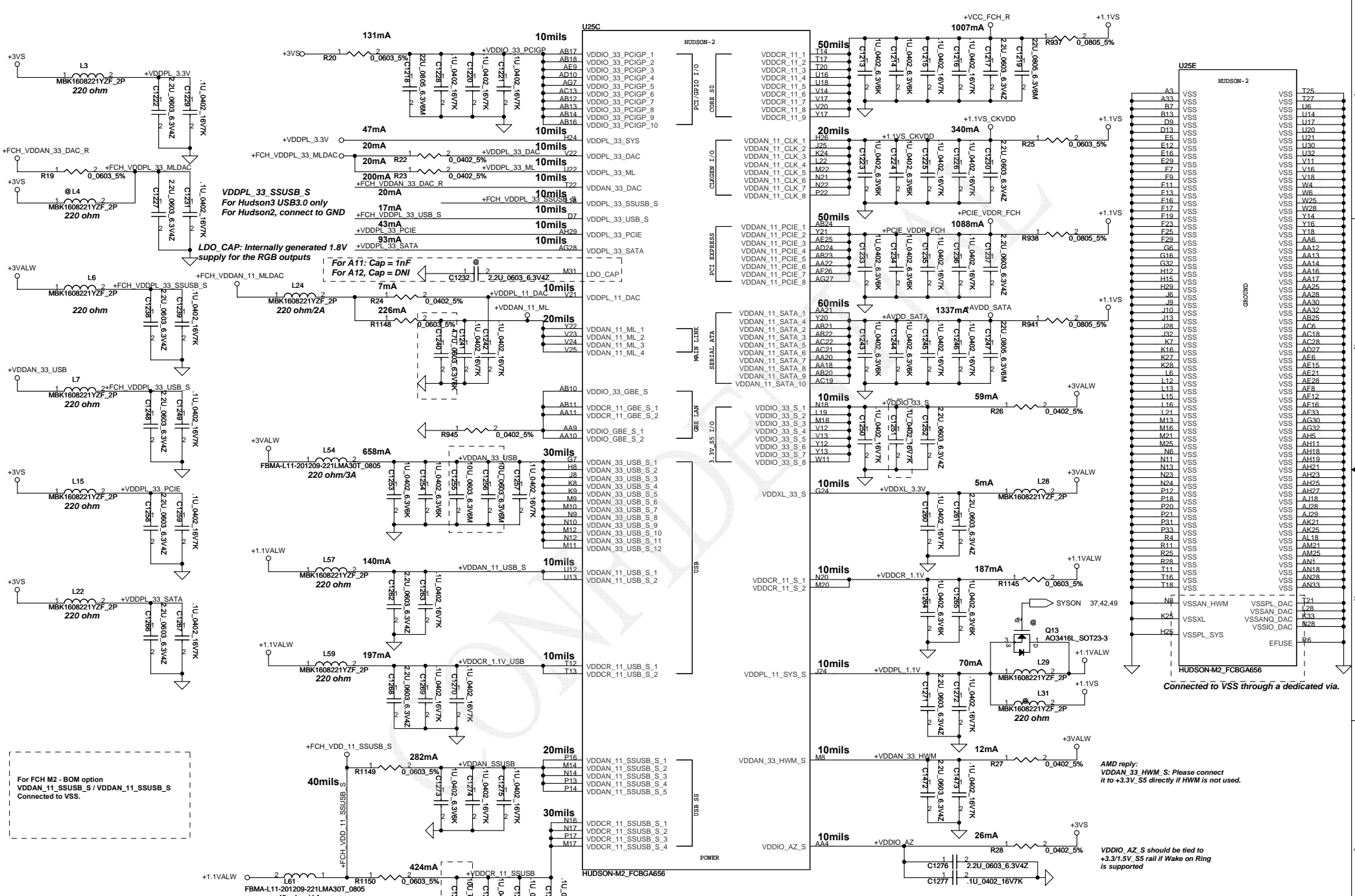


DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD25	PCI_AD24	PCI_AD23
No external R	USE PCI PLL DEFAULT	Normal REFCLK termination DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	Inverted REFCLK termination	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT





For FCH M2 - BOM option
VDDAN_11_SSUSB_S / VDDAN_11_SSUSB_S
Connected to VSS.

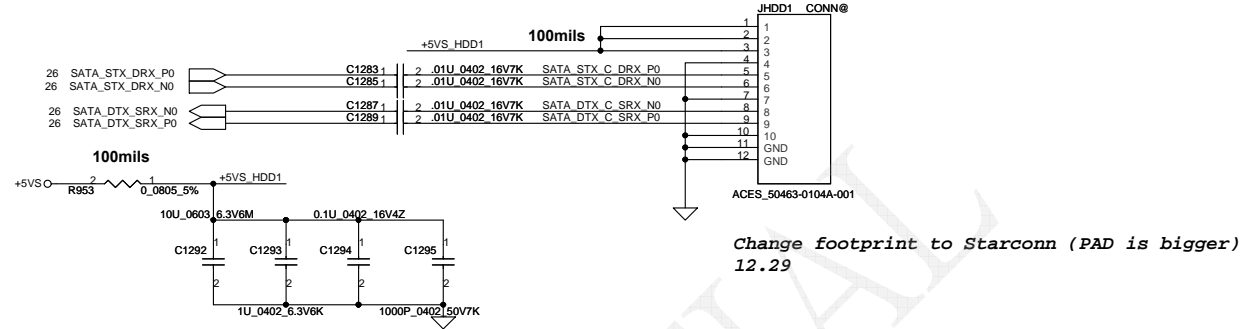
AMD reply:
VDDAN_33_HWM_S: Please connect
it to +3.3V_S5 directly if HWM is not used.

VDDIO_AZ_S should be tied to
+3.3/1.5V_S5 rail if Wake on Ring
is supported

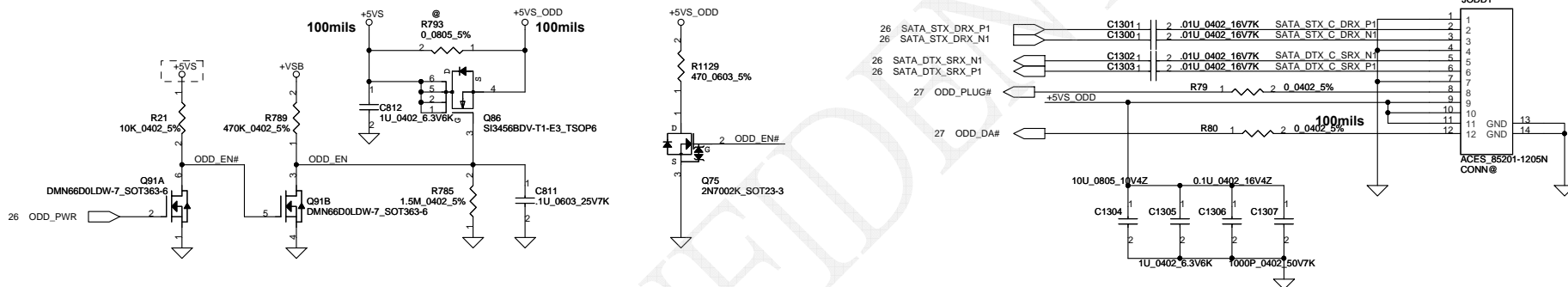
Connected to VSS through a dedicated via.

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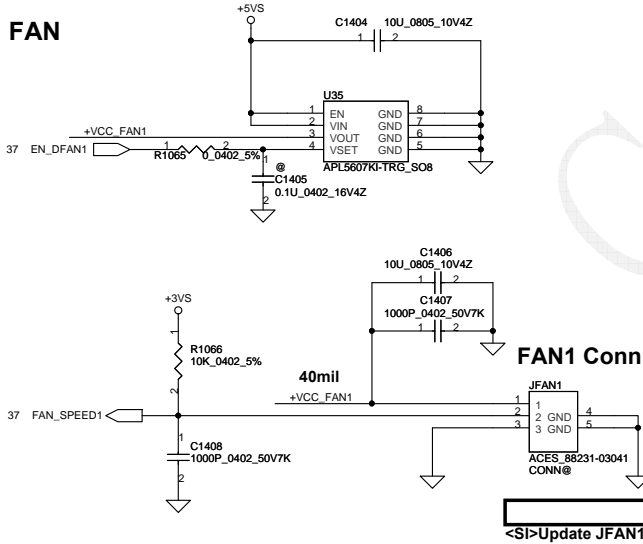
SATA HDD1 Conn.



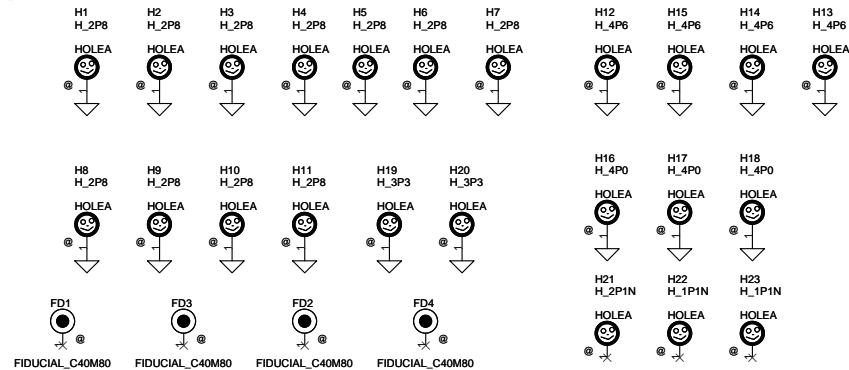
ODD conn



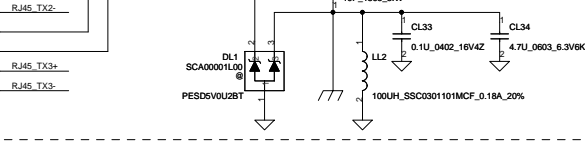
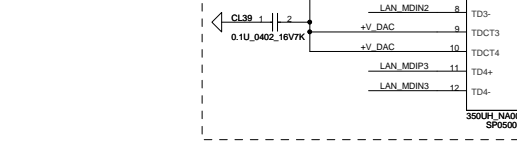
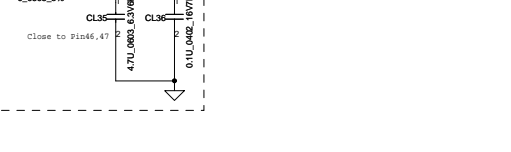
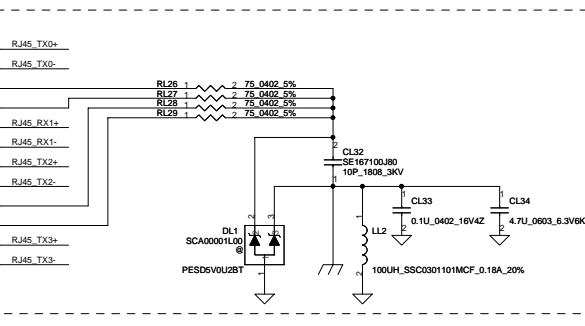
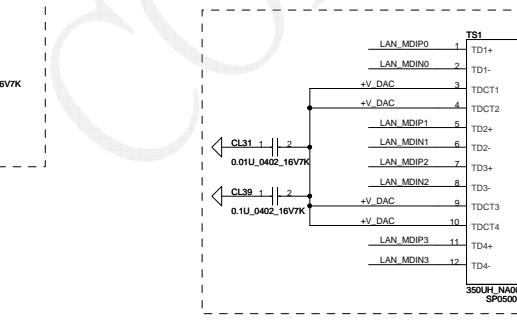
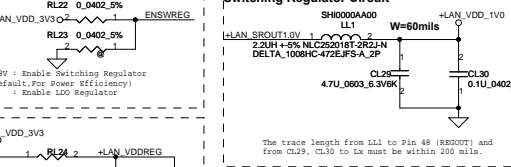
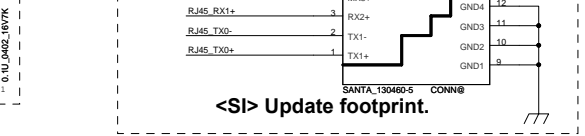
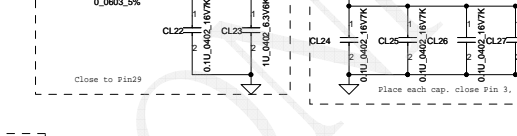
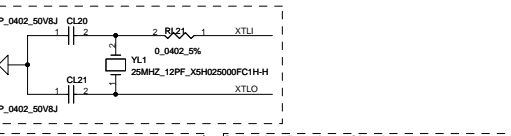
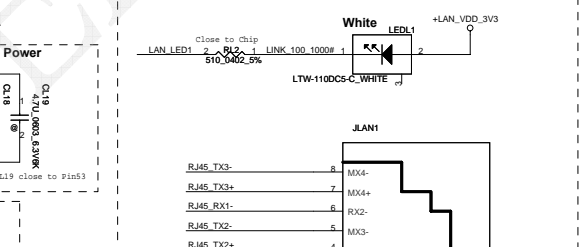
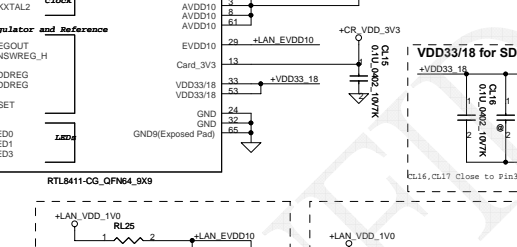
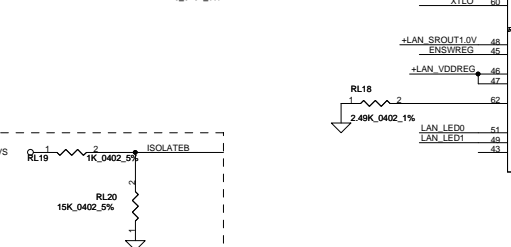
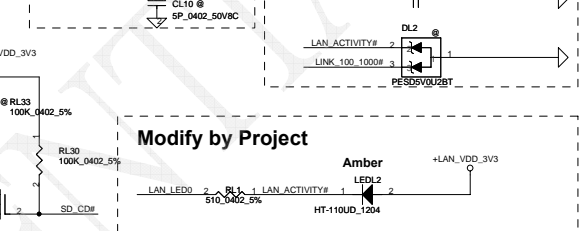
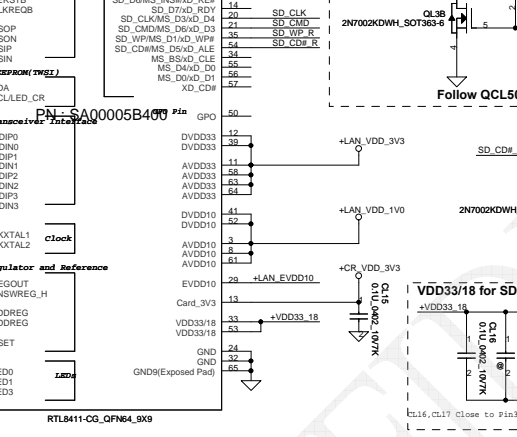
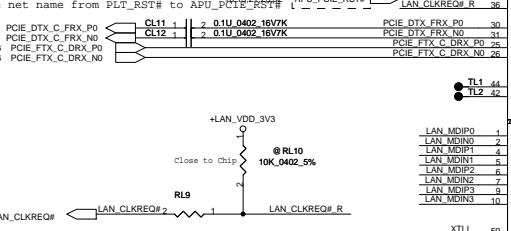
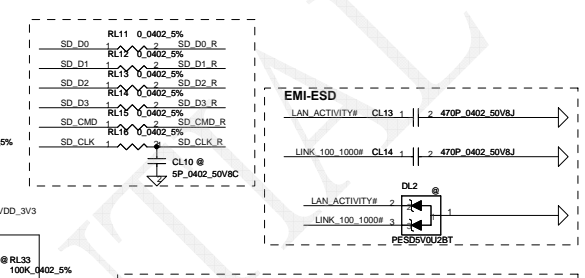
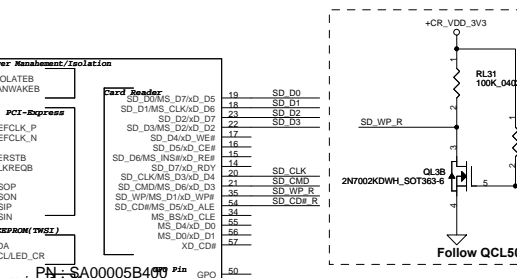
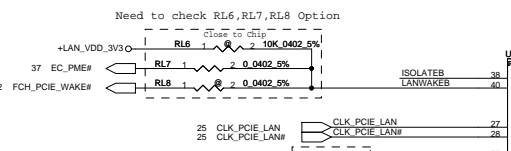
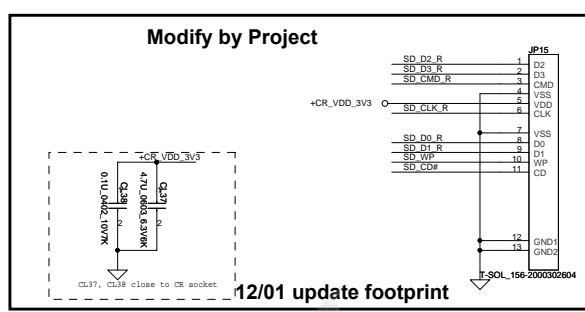
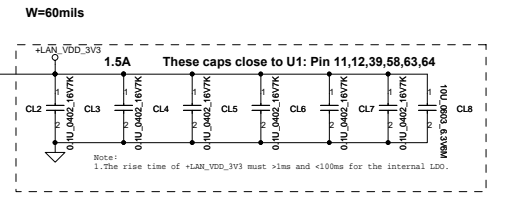
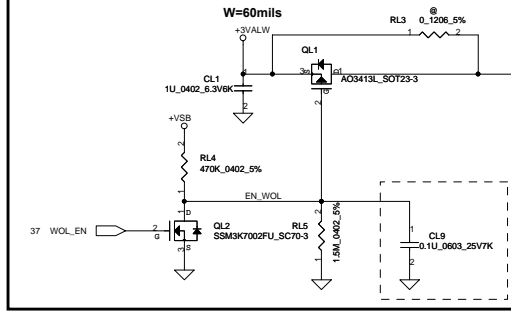
FAN



Screw Hole

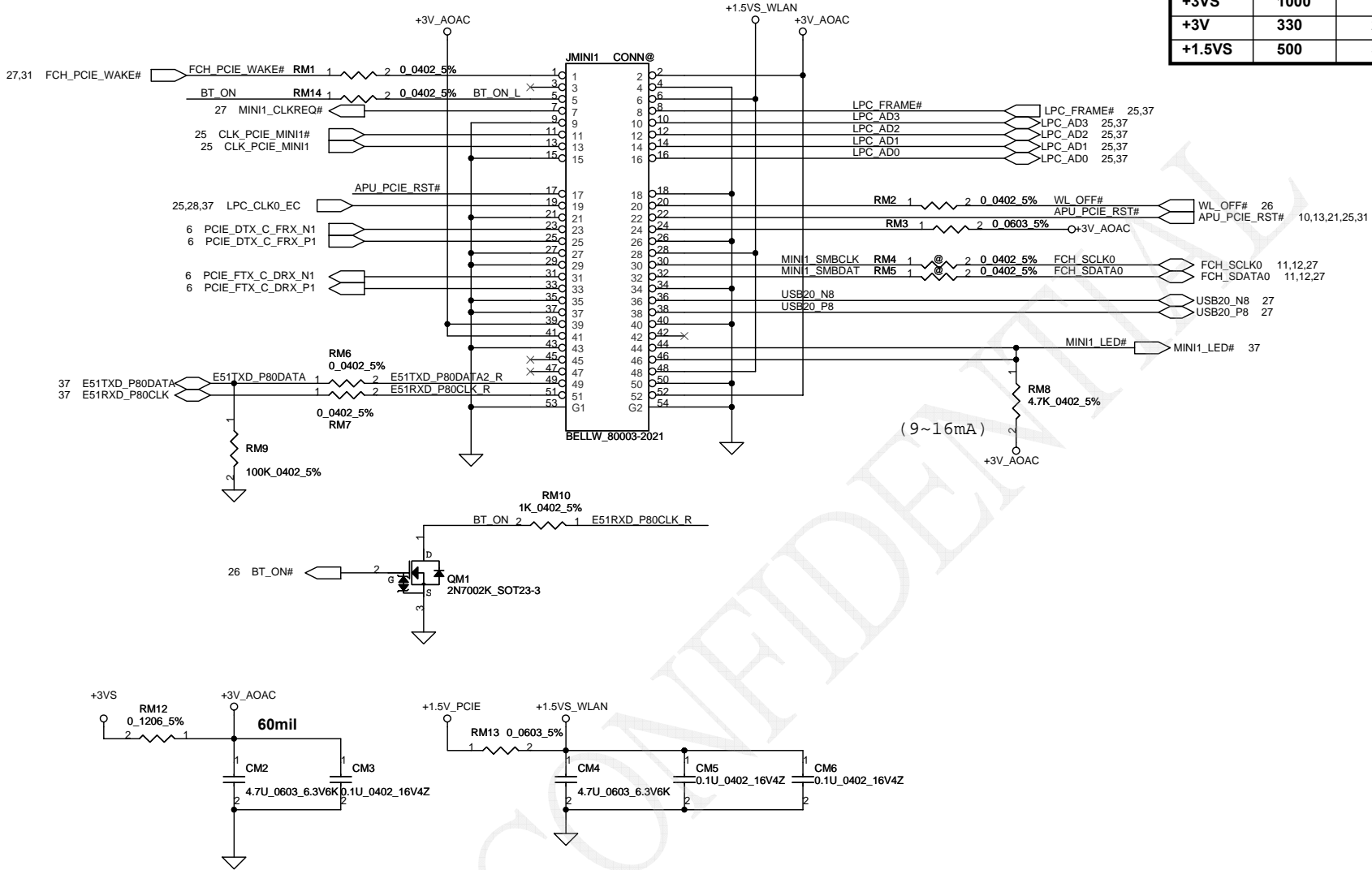


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WLAN

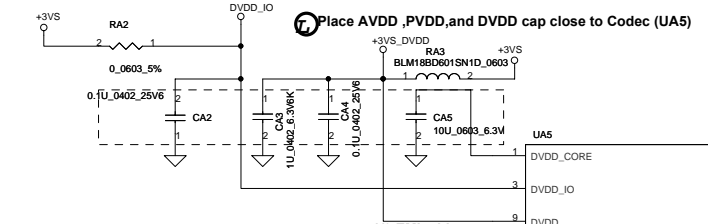


Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

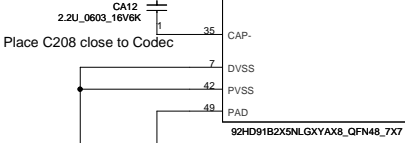
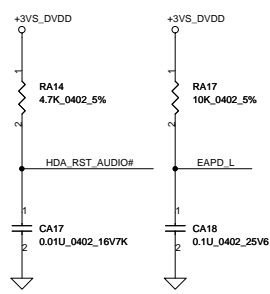
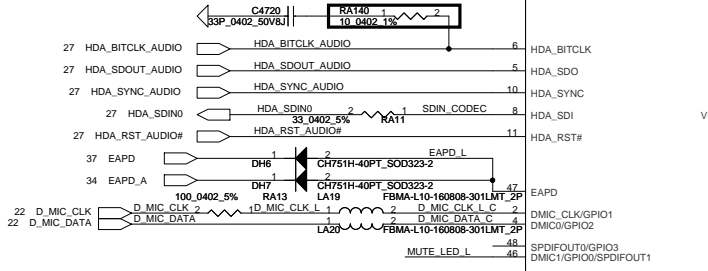
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Notes:
 Keep PVDD supply and speaker traces routed on the DGND plane.
 Keep away from AGND and other analog signals

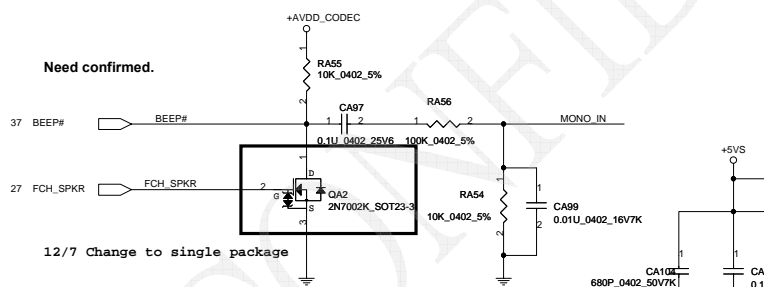
Place AVDD, PVDD, and DVDD cap close to Codec (UA5)



1/3 EMI add

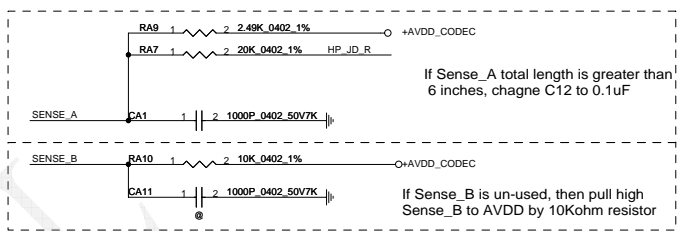


C209, C210, CA87, CA89 close to Codec (UA5)



RA53 need under or near UA5

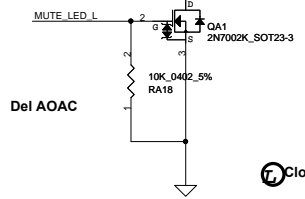
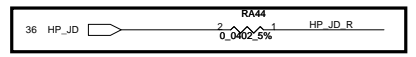
PLACE CLOSE TO UA5 PIN 13



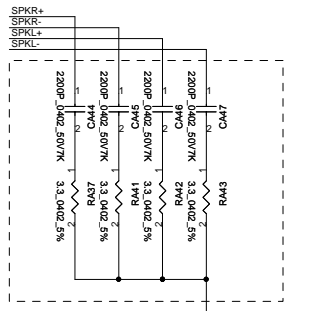
PLACE CLOSE TO UA5 PIN 14



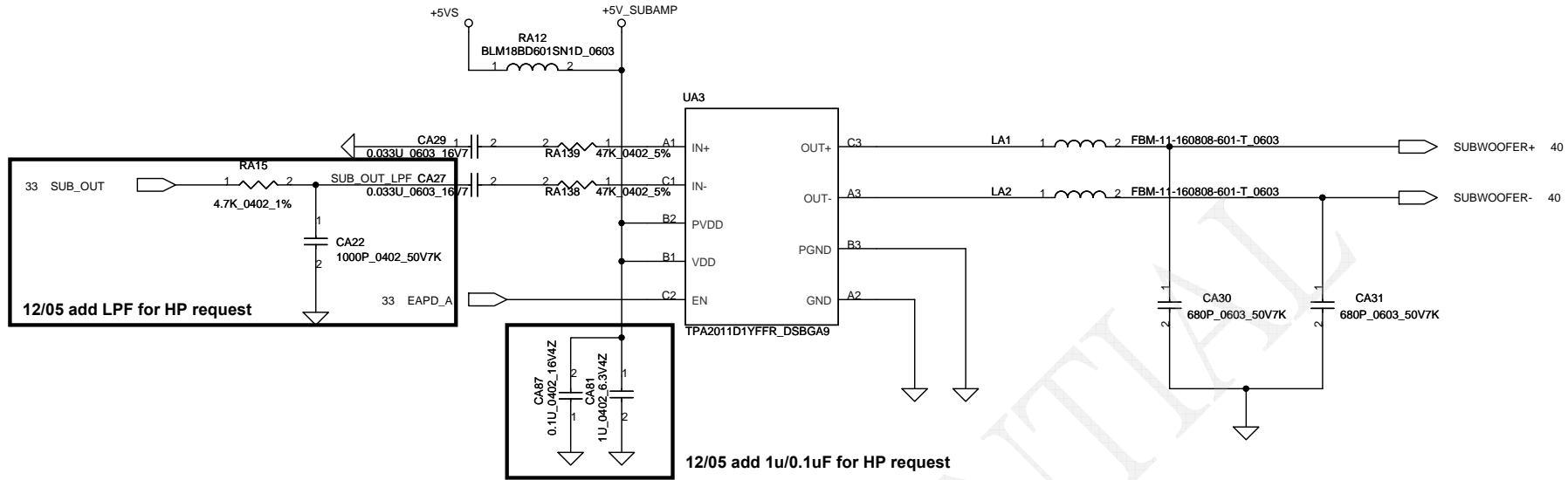
12/5 Audio jack change to normal open, so remove MOS



Close to Audio Codec (UA5)



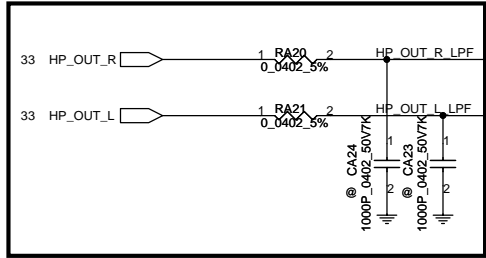
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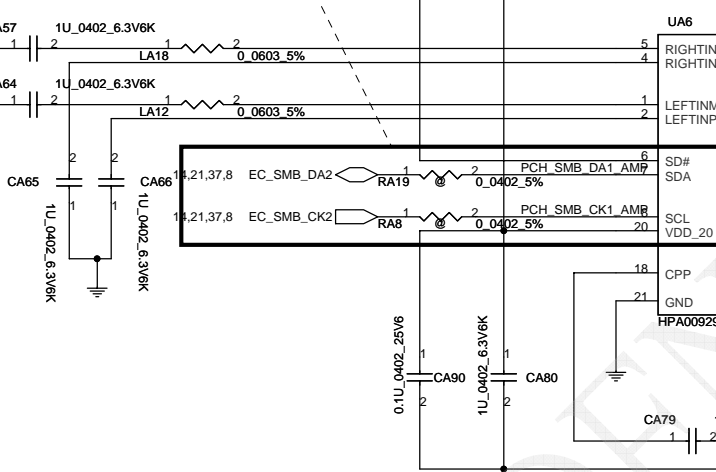
Headphone amplifier

12/05 Add LPF for HP requirement

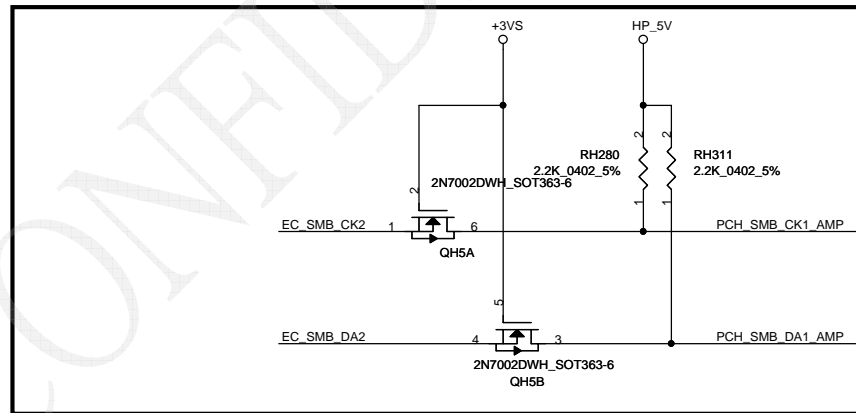


<SI> BOM update :RA20,RA21 4.7K-->0
CA24,CA23 SMT-->@

12/05 Connect HP AMP SMBus to EC

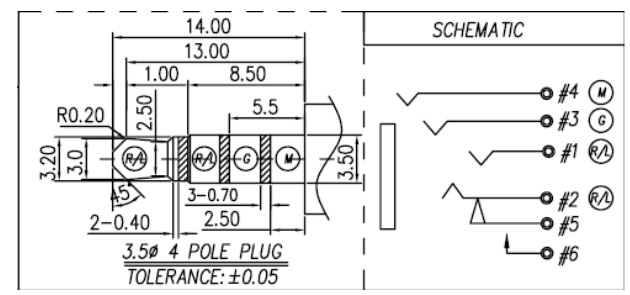
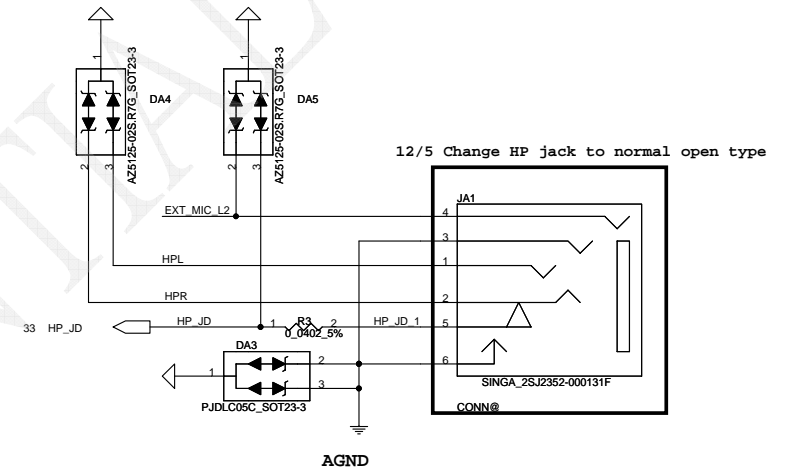
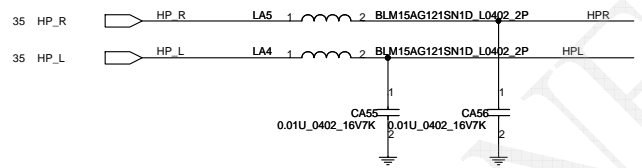
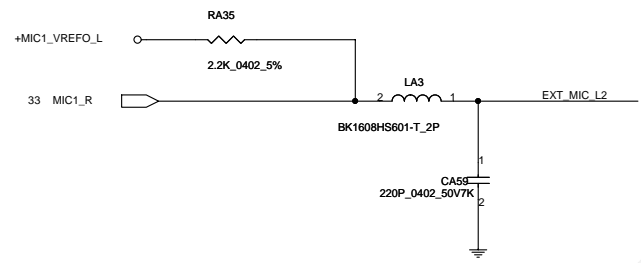
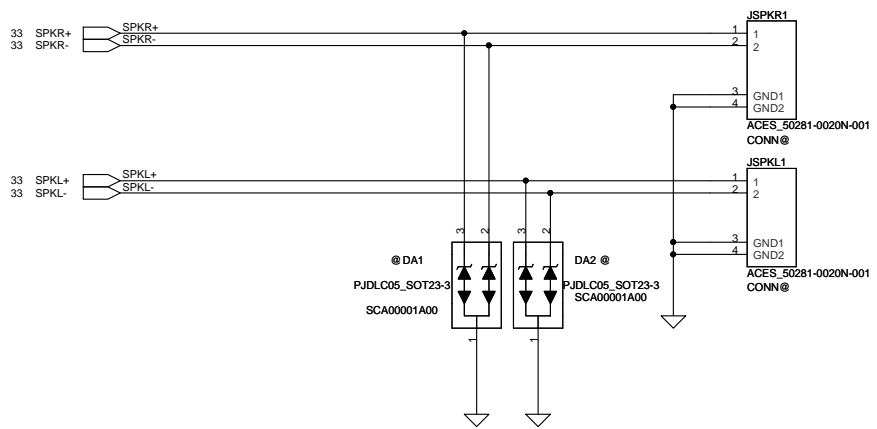


12/05 Reserve level shift Connect to EC

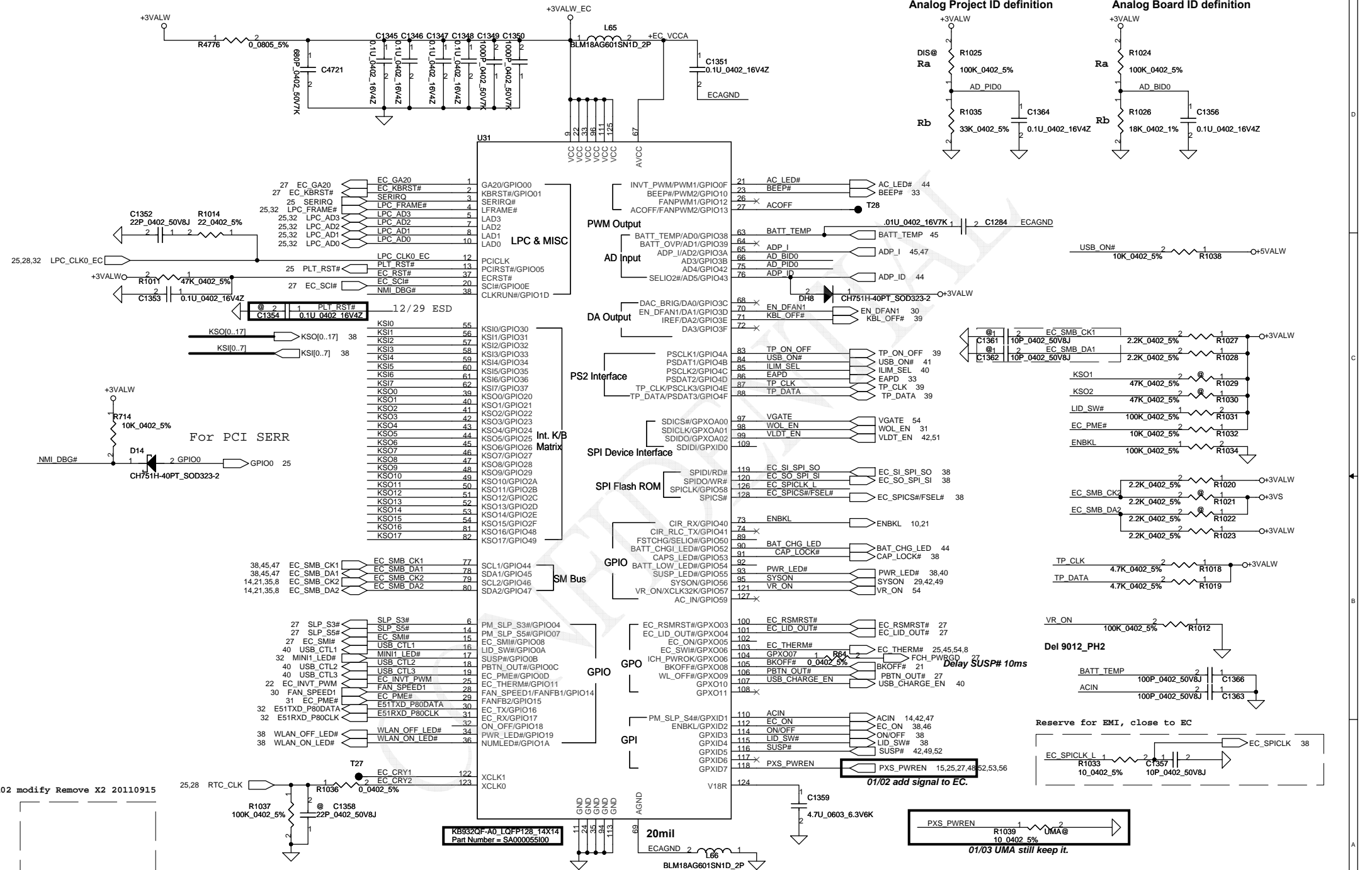


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SPK conn



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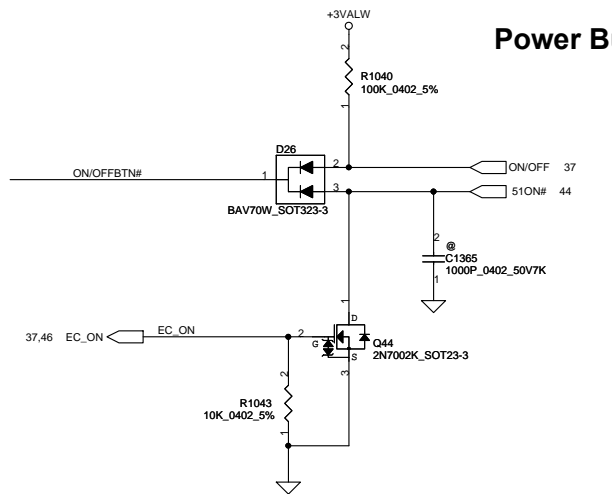
R02 modify Remove X2 20110915

K8932QF-A0 LQFP128_14X14
Part Number = SA000055100

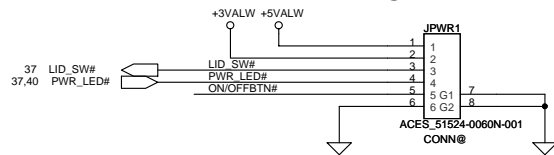
PXS_PWREN
R1039 10_0402_5% UMA@
01/03 UMA still keep it.

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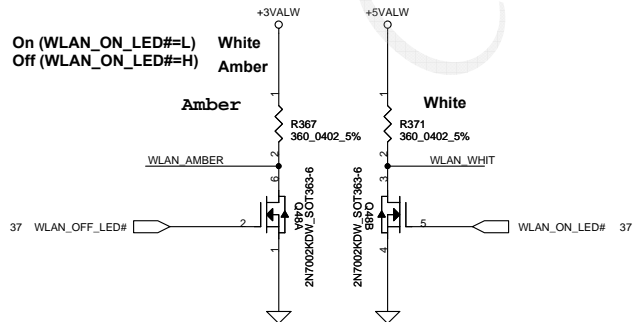
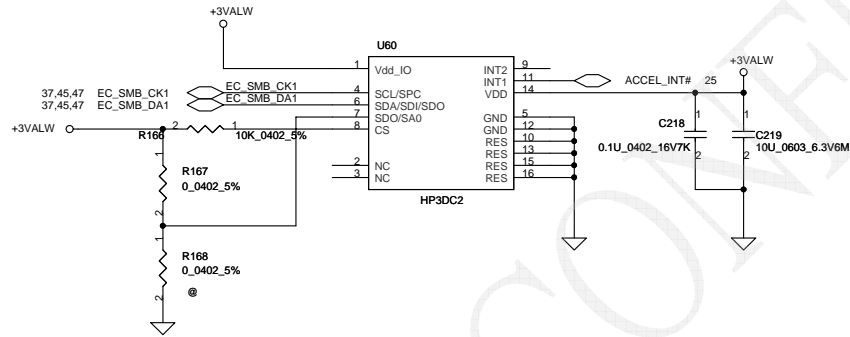
Power Button



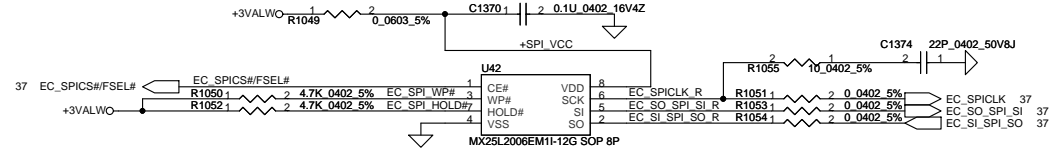
POWER/B



ACCELEROMETER

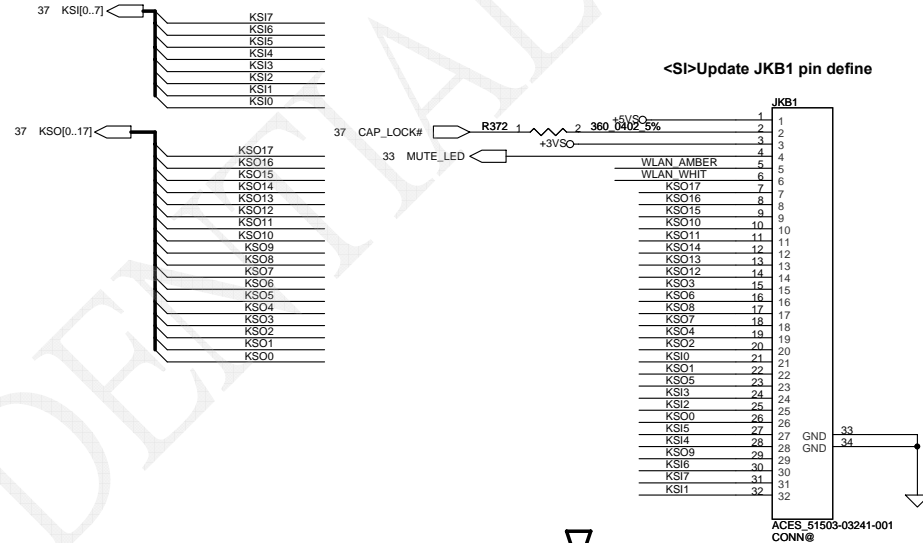


EC BIOS ROM

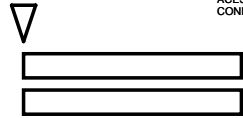


KB conn

<SI>Update JKB1 pin define



Membrane Down contact



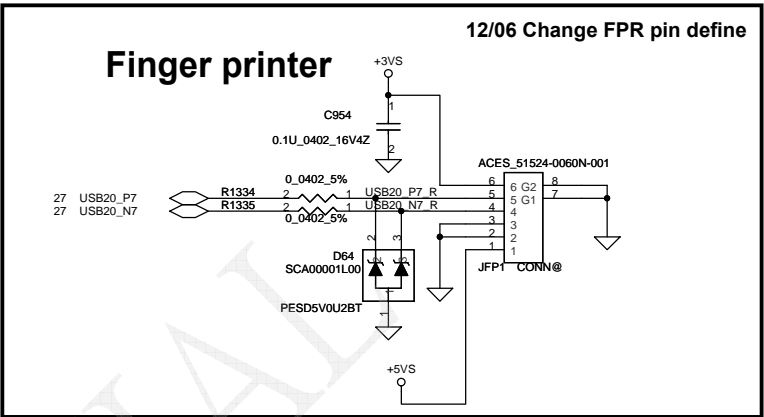
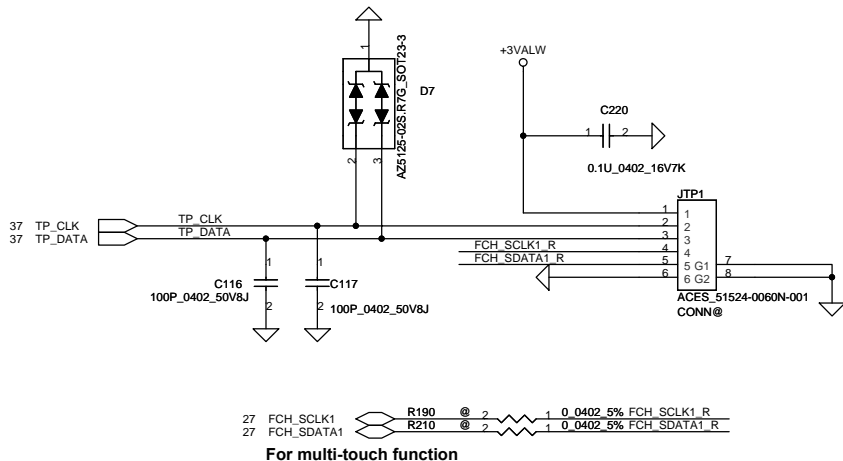
The KB pin define must opposite

KSO15	C1380	1	2	100P_0402_50V8J
KSO14	C1383	1	2	100P_0402_50V8J
KSO13	C1384	1	2	100P_0402_50V8J
KSO12	C1386	1	2	100P_0402_50V8J
KSO10	C1392	1	2	100P_0402_50V8J
KSO11	C1390	1	2	100P_0402_50V8J
KSO10	C1392	1	2	100P_0402_50V8J
KSI1	C1394	1	2	100P_0402_50V8J
KSI2	C1396	1	2	100P_0402_50V8J
KSO9	C1398	1	2	100P_0402_50V8J
KSI3	C1400	1	2	100P_0402_50V8J
KSO8	C1402	1	2	100P_0402_50V8J
KSO3	C1389	1	2	100P_0402_50V8J
KSI4	C1391	1	2	100P_0402_50V8J
KSO2	C1393	1	2	100P_0402_50V8J
KSO1	C1395	1	2	100P_0402_50V8J

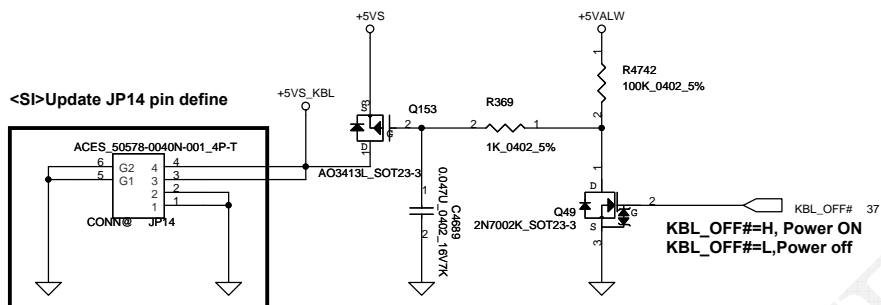
KSO16	C1378	1	2	100P_0402_50V8J
KSO17	C1379	1	2	100P_0402_50V8J
KSO7	C1381	1	2	100P_0402_50V8J
KSO6	C1382	1	2	100P_0402_50V8J
KSO5	C1385	1	2	100P_0402_50V8J
KSO4	C1387	1	2	100P_0402_50V8J
KSO0	C1397	1	2	100P_0402_50V8J
KSI5	C1399	1	2	100P_0402_50V8J
KSI6	C1401	1	2	100P_0402_50V8J
KSI7	C1403	1	2	100P_0402_50V8J

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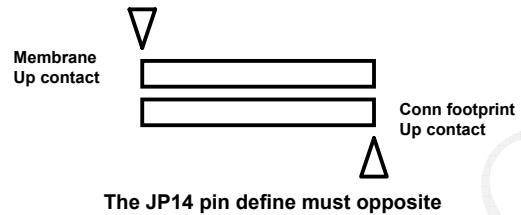
TP Conn



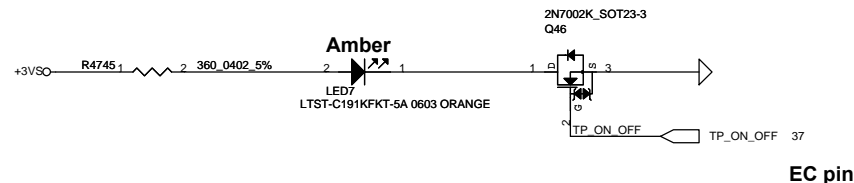
Keyboard backlight Conn



12/06 Change keyboard back light conn

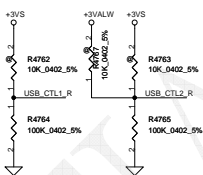
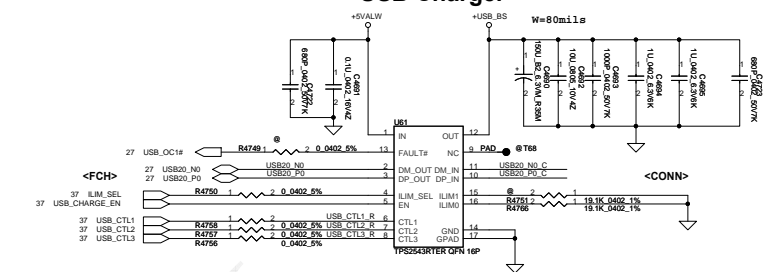


T/P On/Off LED



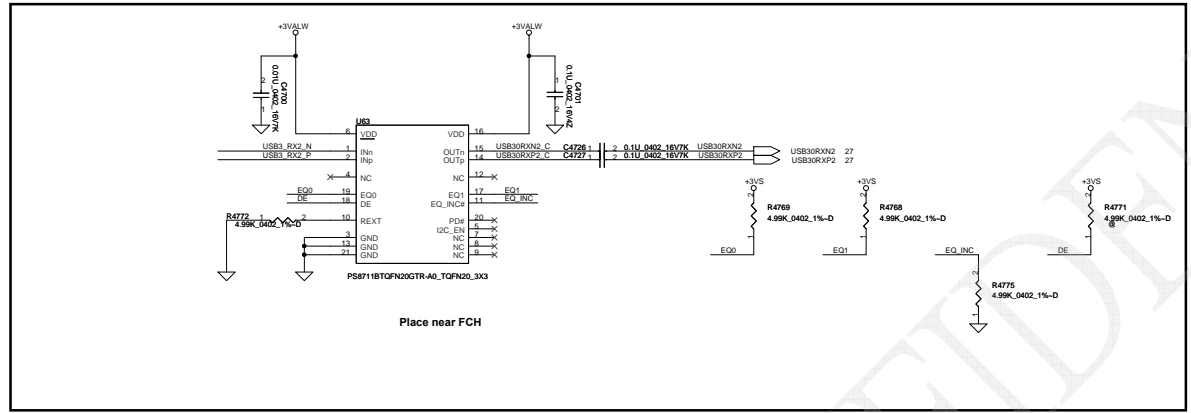
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USB Charger

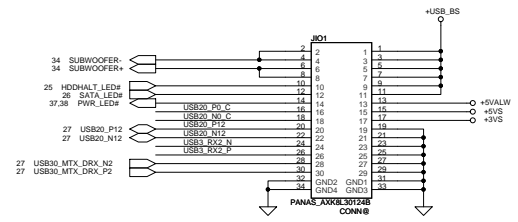
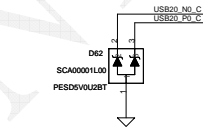


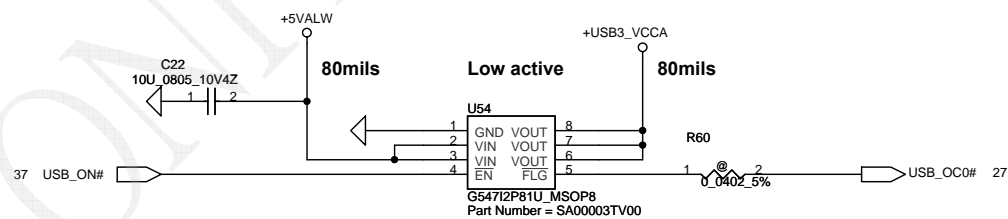
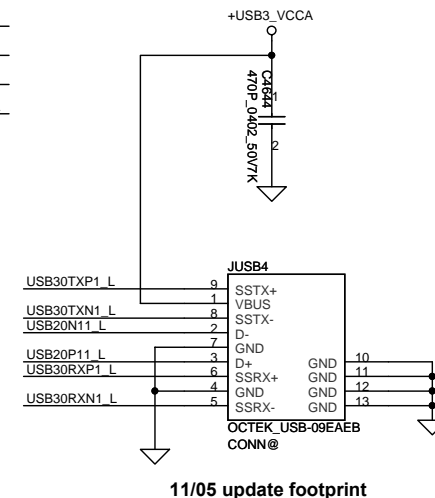
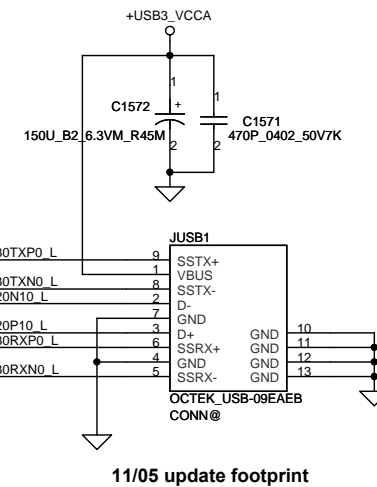
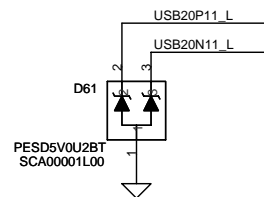
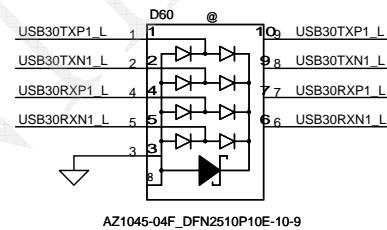
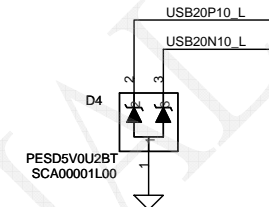
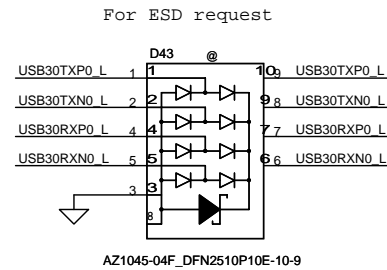
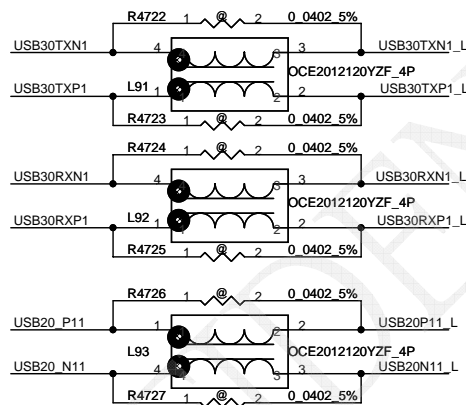
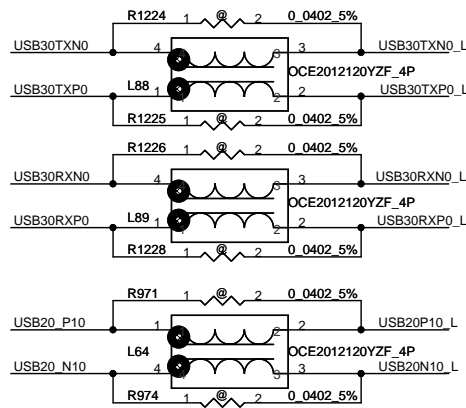
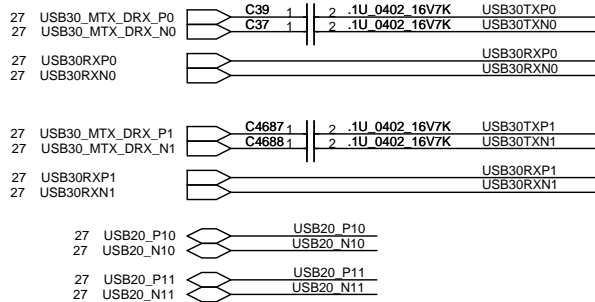
State	S0				S3, S4, S5			
Mode	CDP				DCP			
Control pin	CTL1	CTL2	CTL3	ILIM_SEL	CTL1	CTL2	CTL3	ILIM_SEL
	1	1	1	1	0	0	1	1

USB3.0 Repeater



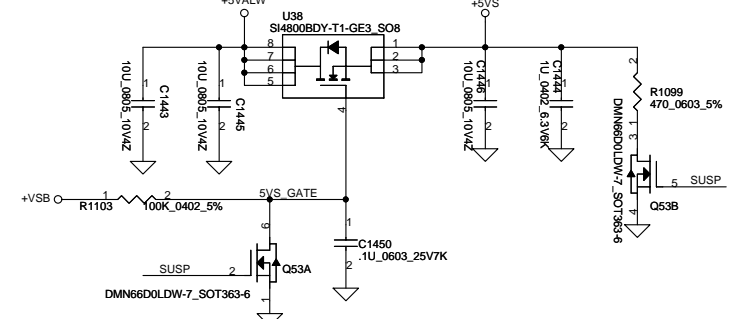
Place near FCH



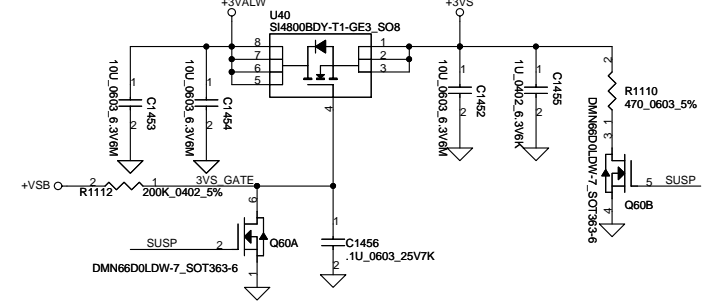


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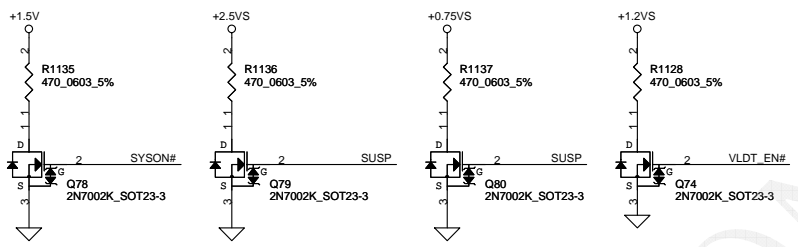
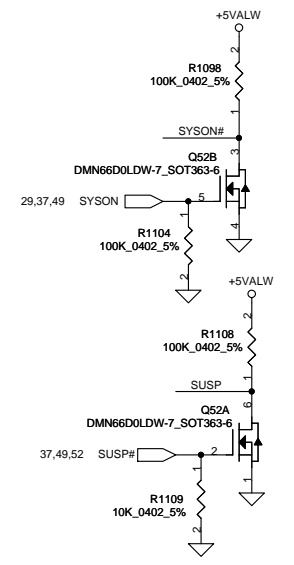
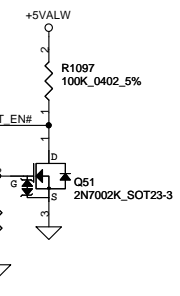
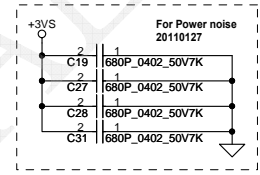
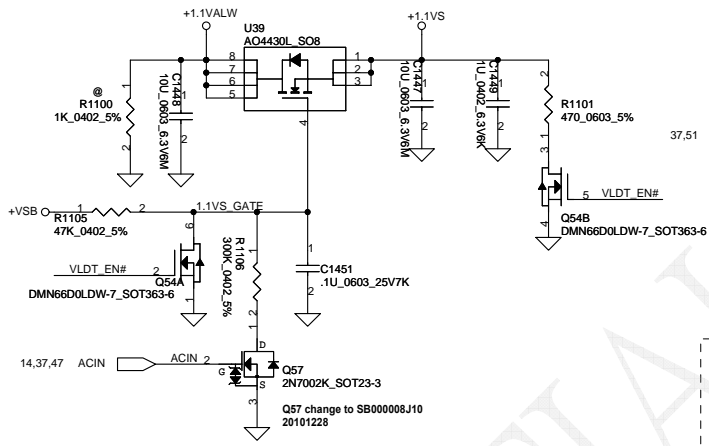
+5VALW TO +5VS (5A)



+3VALW TO +3VS (3.3A)



+1.1VALW TO +1.1VS (1.1A)



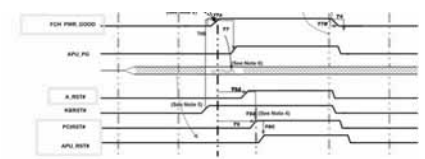
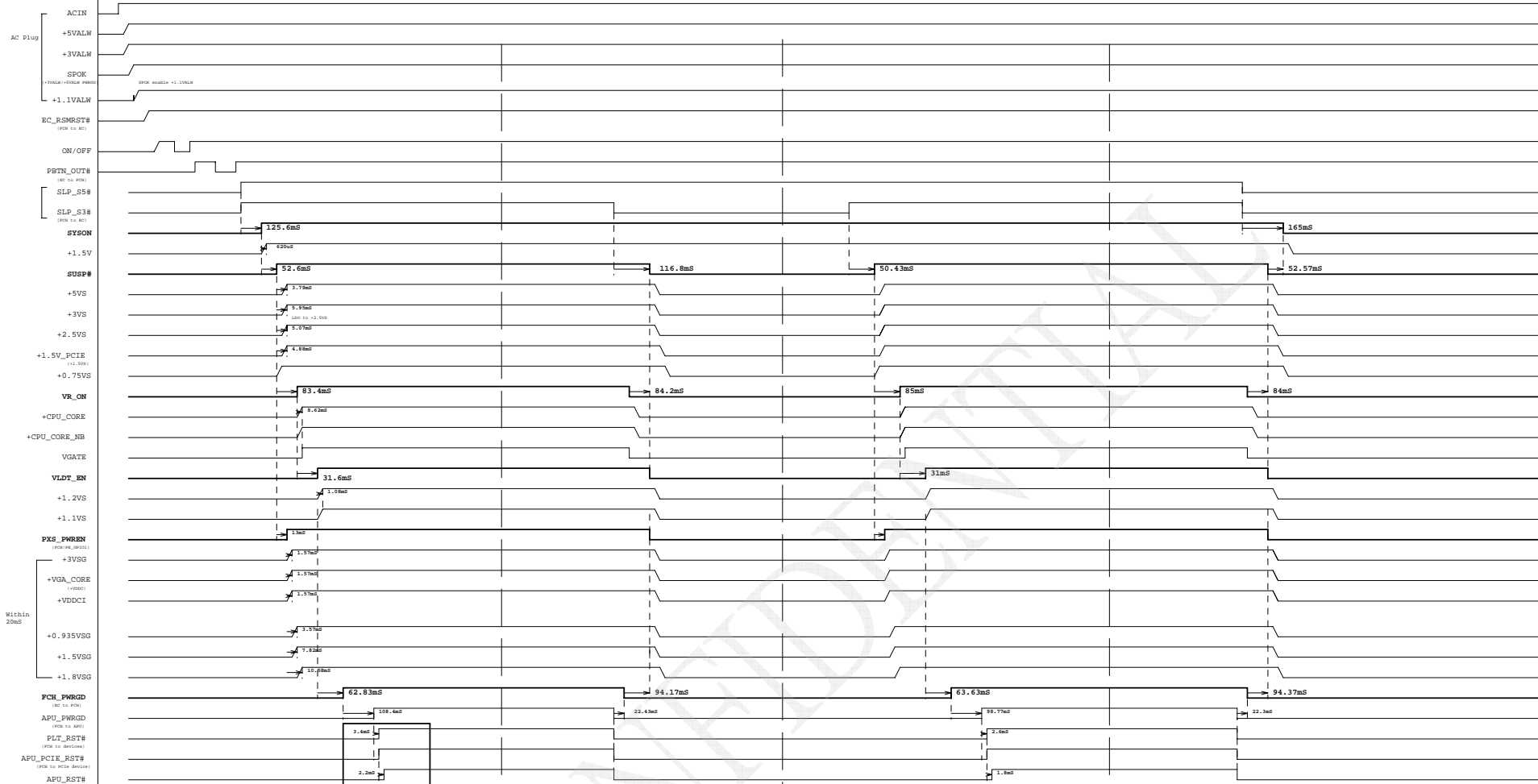
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Boot

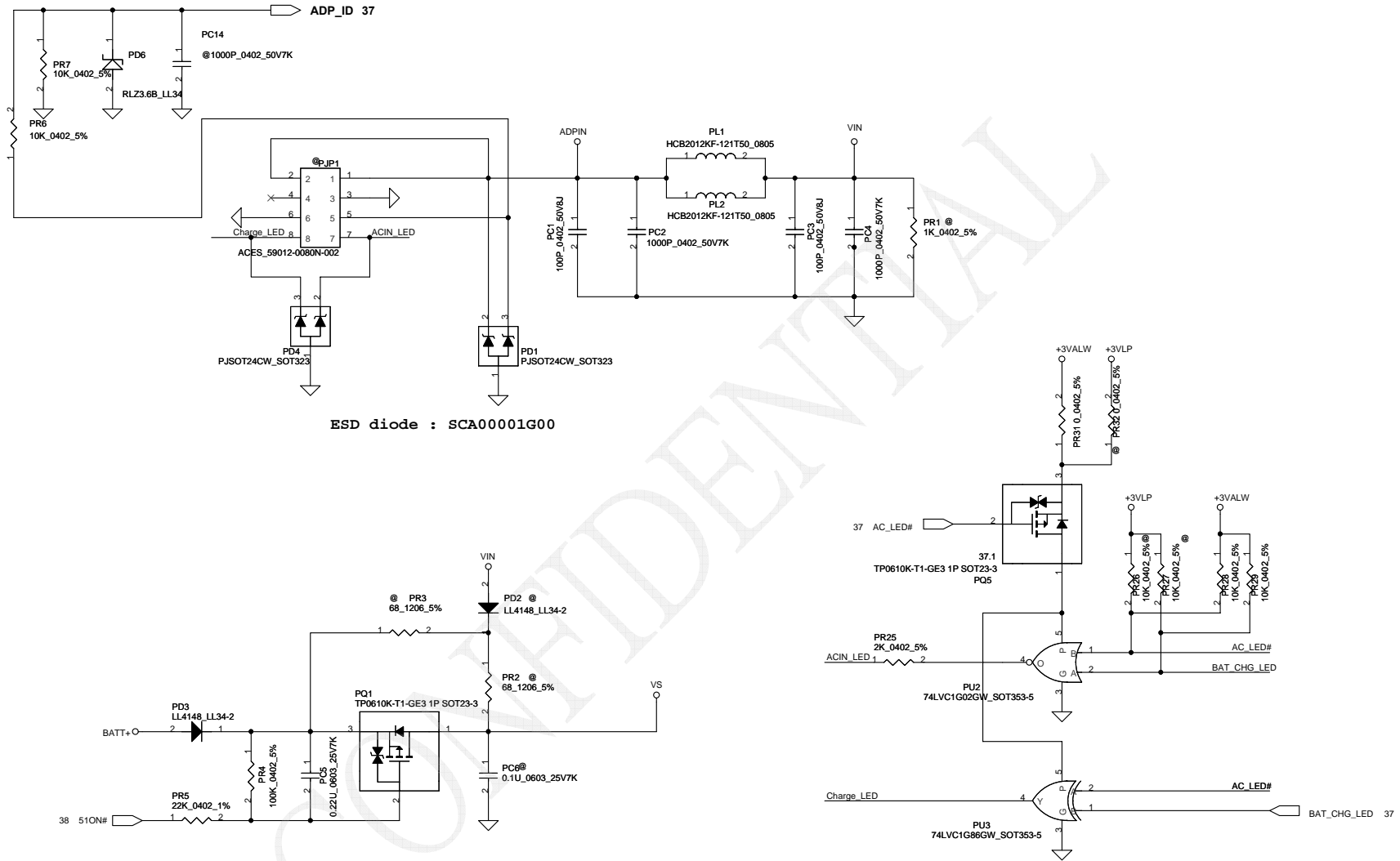
Enter S3

S3 Resume

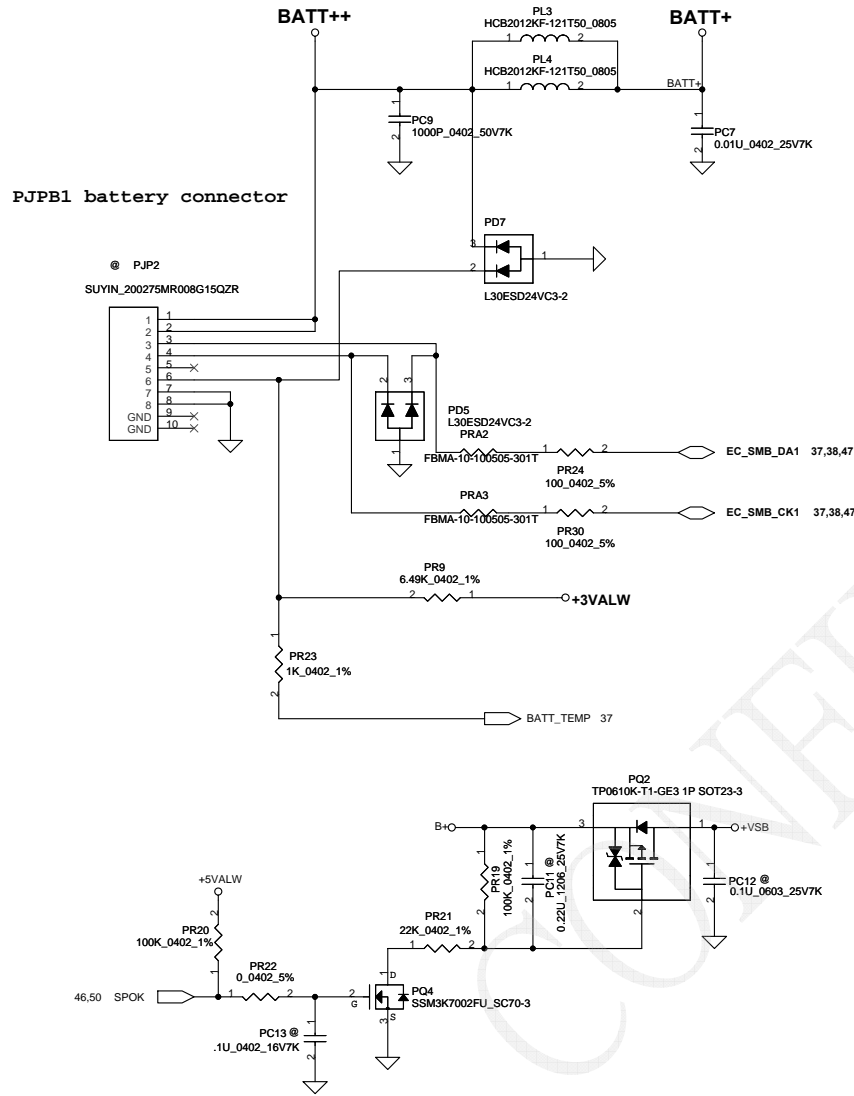
Shut Down



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For KB930 --> Keep PU1 circuit
(Vth = 0.825V)

PH1 under CPU bottom side :
CPU thermal protection at 90 +3 degree C
Recovery at 56 +3 degree C

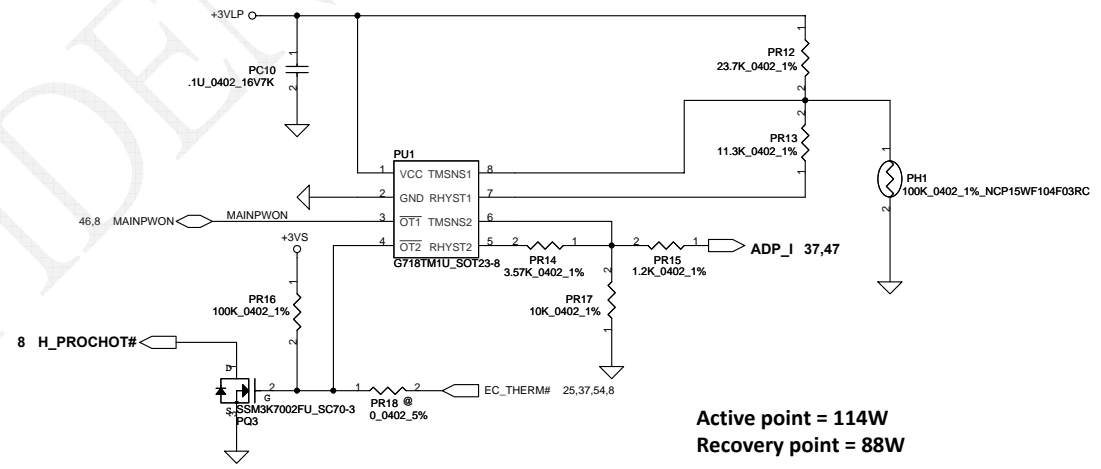
$$Rset = 3 * Rtmh$$

$$Rhyst = (Rset * Rtml) / (3 * Rtml - Rset)$$

$$Rtmh \text{ at } 90C = 7.8K, Rtml \text{ at } 56C = 26.1K$$

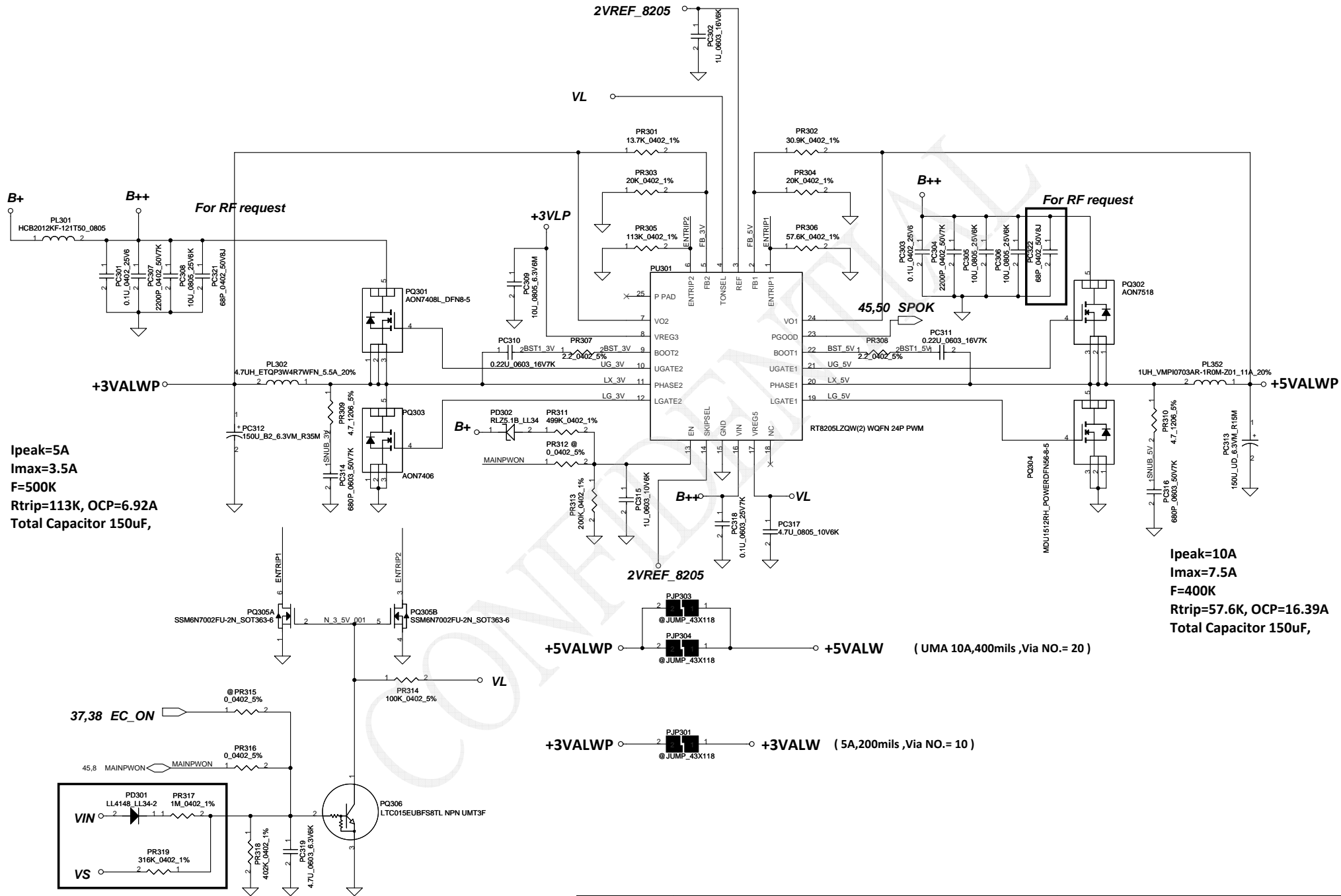
$$Rset = 3 * 7.8K = 23.4K \implies 23.7K$$

$$Rhyst = (23.4K * 26.1K) / (3 * 26.1K - 23.4K) = 11.12K \implies 11.3K$$



Active point = 114W
Recovery point = 88W

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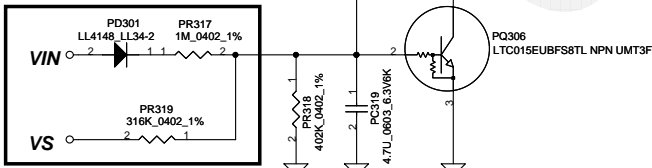


Ipeak=5A
 Imax=3.5A
 F=500K
 Rtrip=113K, OCP=6.92A
 Total Capacitor 150uF,

Ipeak=10A
 Imax=7.5A
 F=400K
 Rtrip=57.6K, OCP=16.39A
 Total Capacitor 150uF,

(UMA 10A,400mils ,Via NO.= 20)

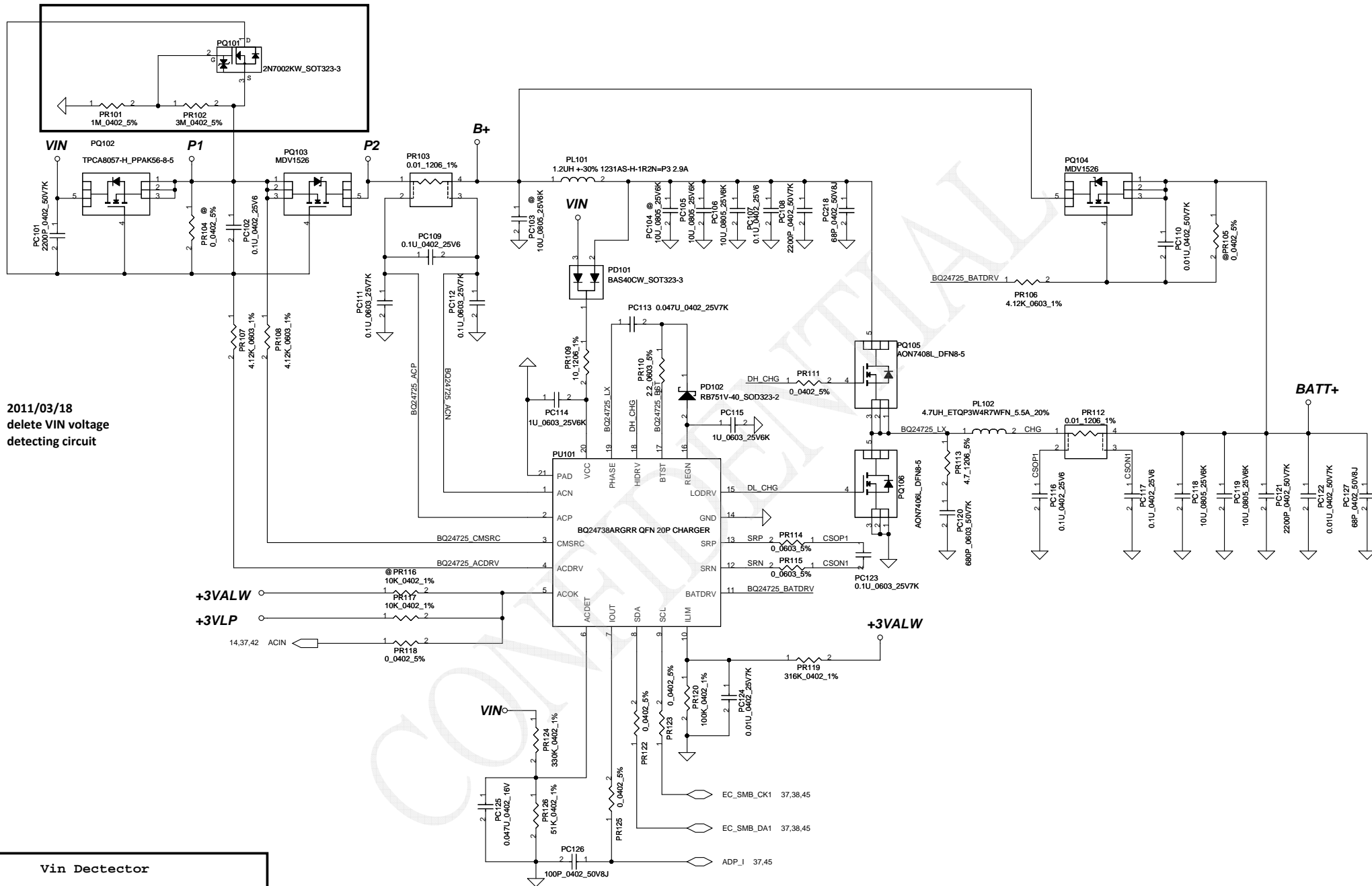
(5A,200mils ,Via NO.= 10)



For KB930 --> Keep PD301, PR317, PR319

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for reverse input protection



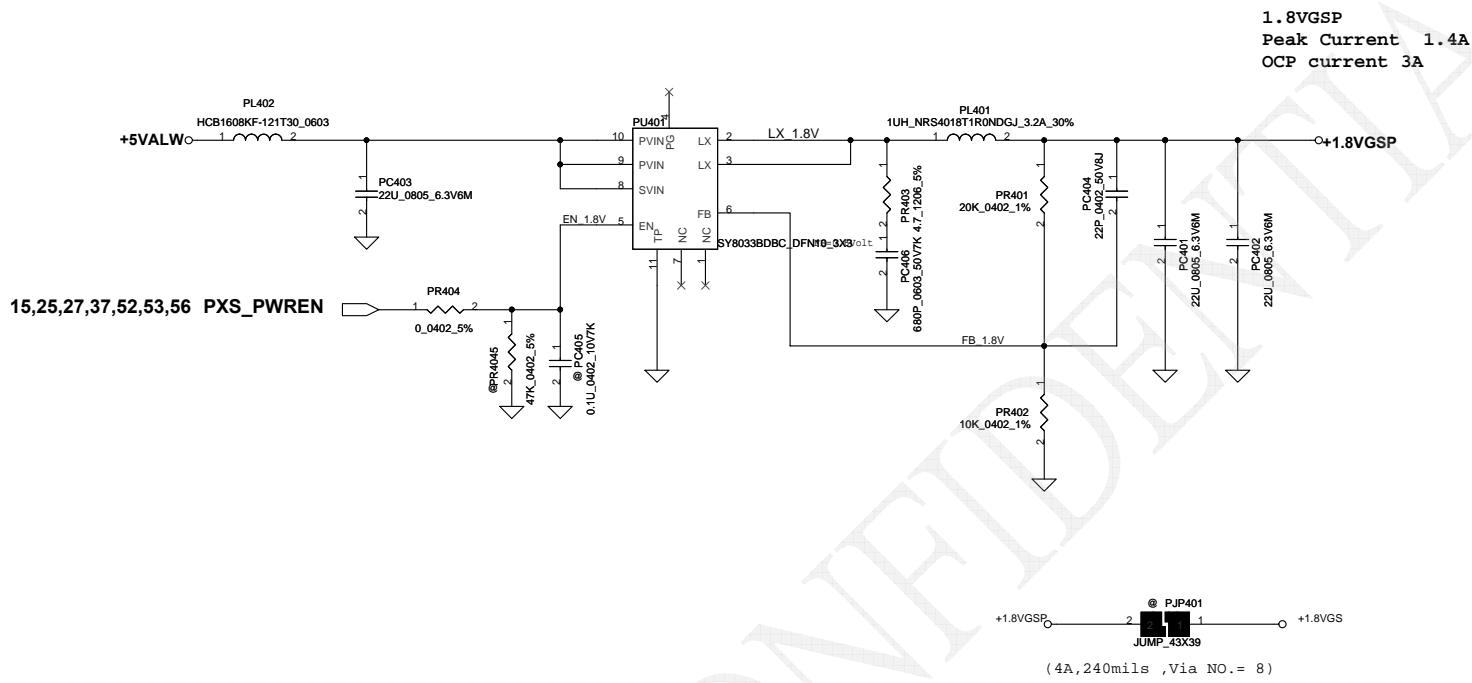
2011/03/18
delete VIN voltage
detecting circuit

Vin Detector

	Min.	Typ	Max.
H-->L		17.33V	
L-->H		16.98V	

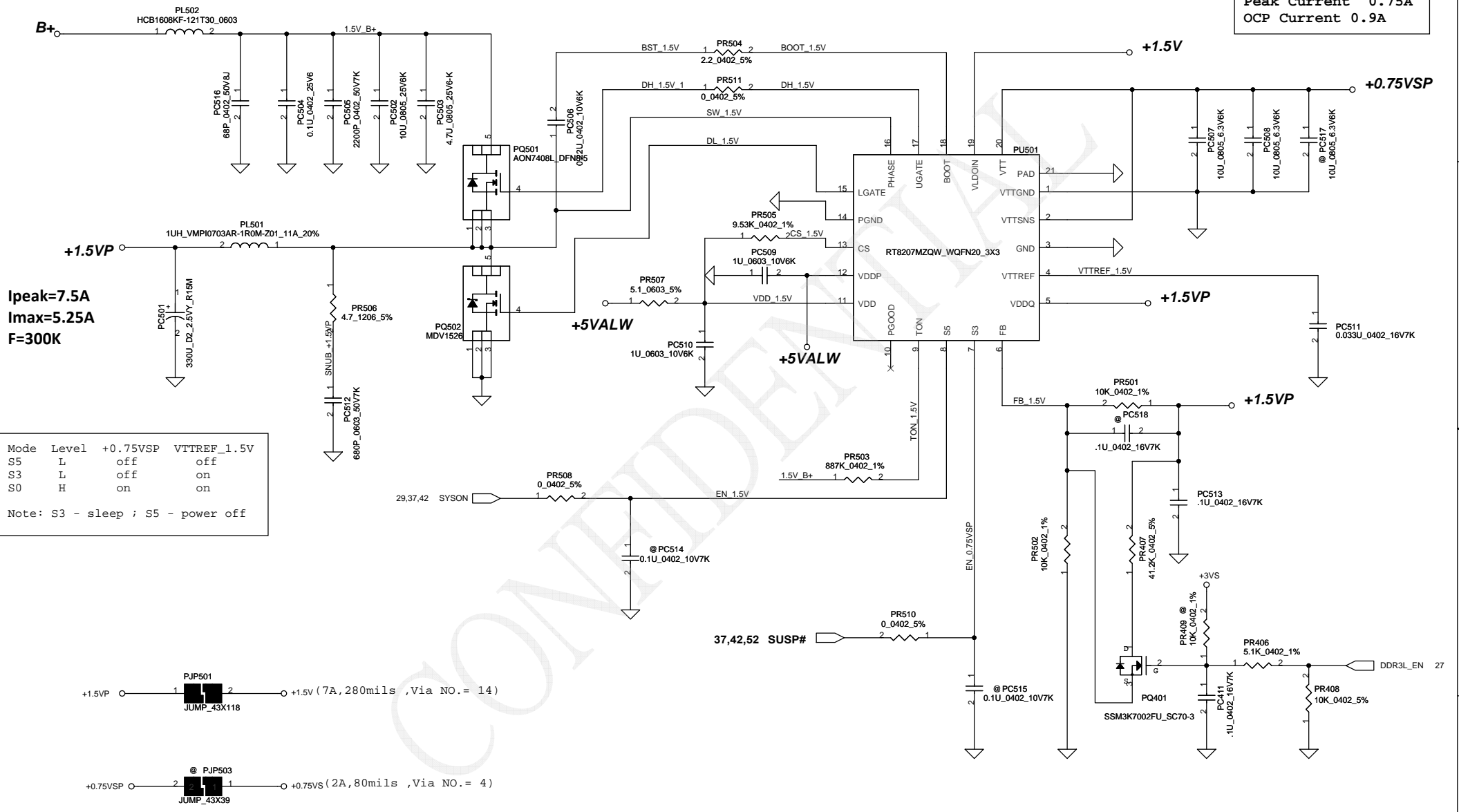
ILIM and external DPM
4.36A

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0.75Volt +/- 5%
 TDC 0.525A
 Peak Current 0.75A
 OCP Current 0.9A

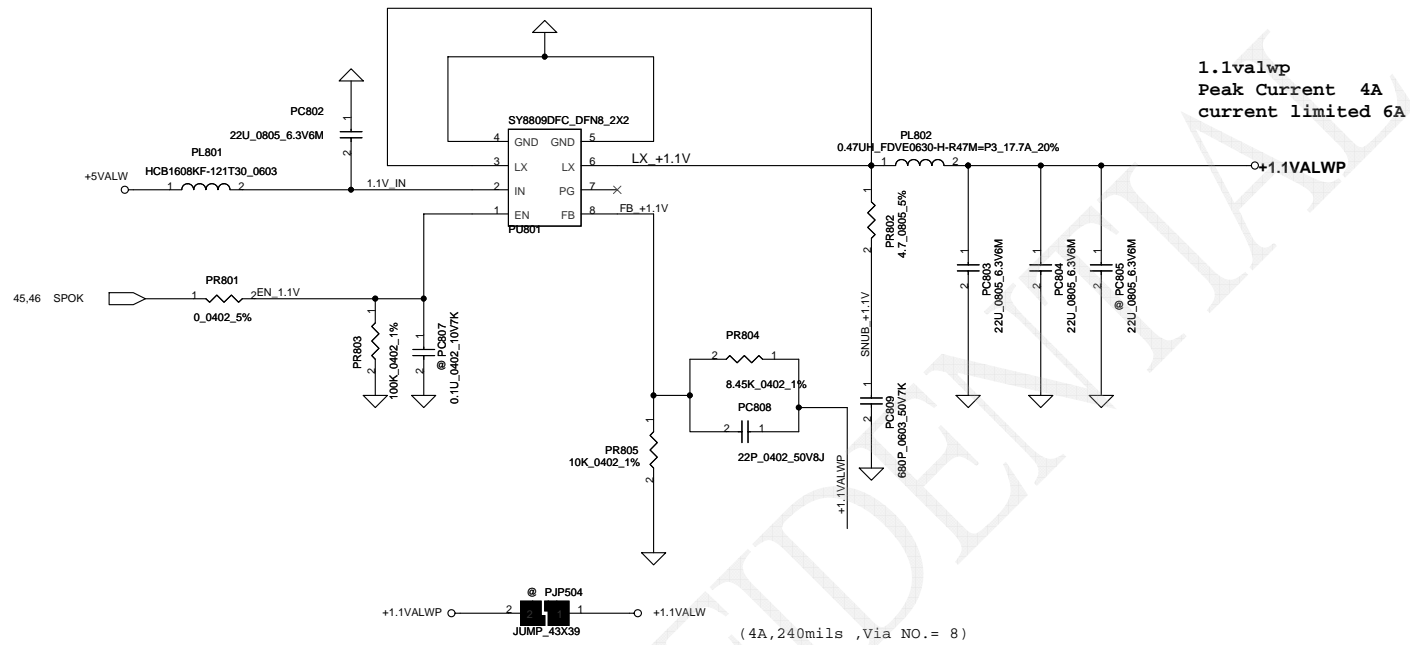


I_{peak}=7.5A
 I_{max}=5.25A
 F=300K

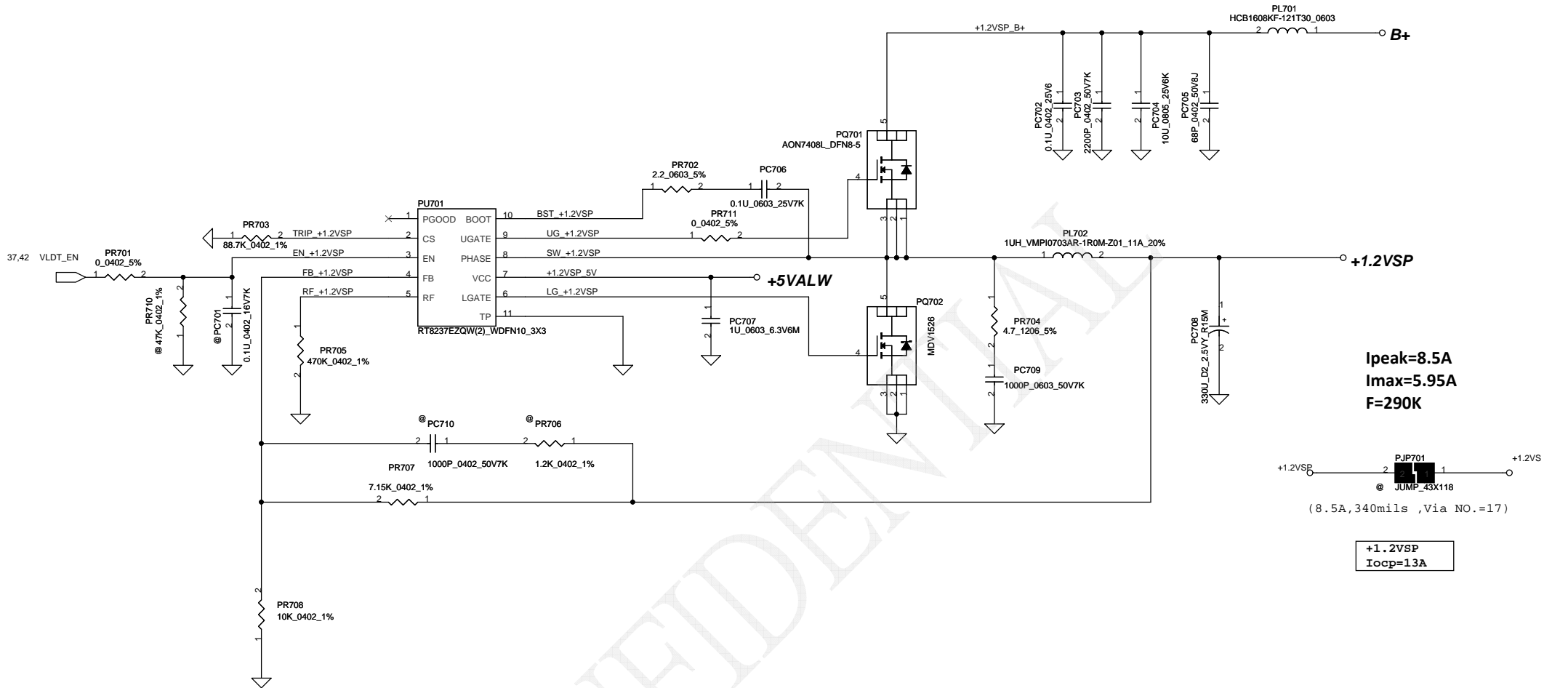
Mode	Level	+0.75VSP	VTTREF_1.5V
S5	L	off	off
S3	L	off	off
S0	H	on	on

Note: S3 - sleep ; S5 - power off

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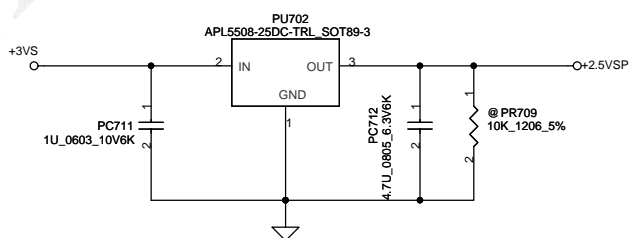


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I_{peak}=8.5A
I_{max}=5.95A
F=290K

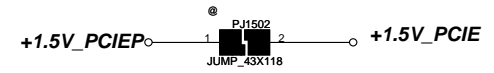
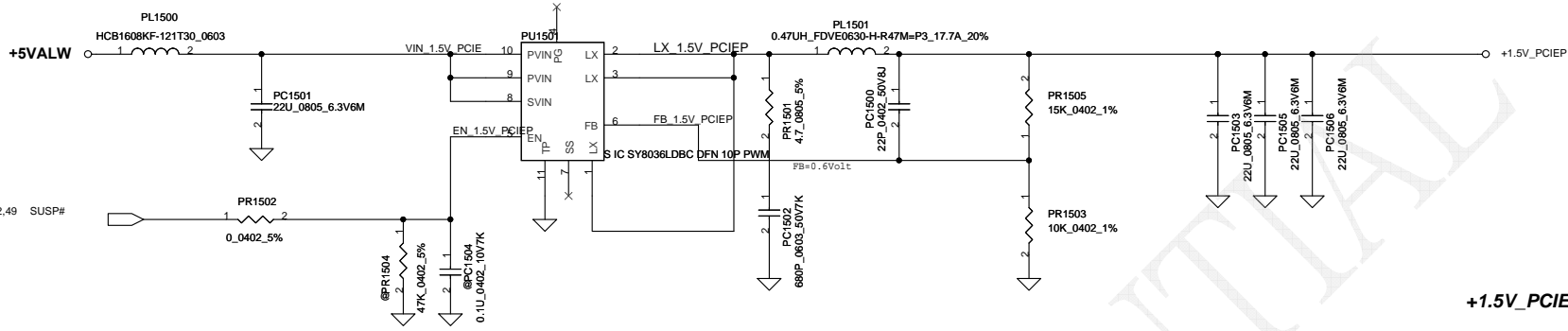
+1.2VSP
I_{ocp}=13A



+2.5VSP
I_{ocp}=13A

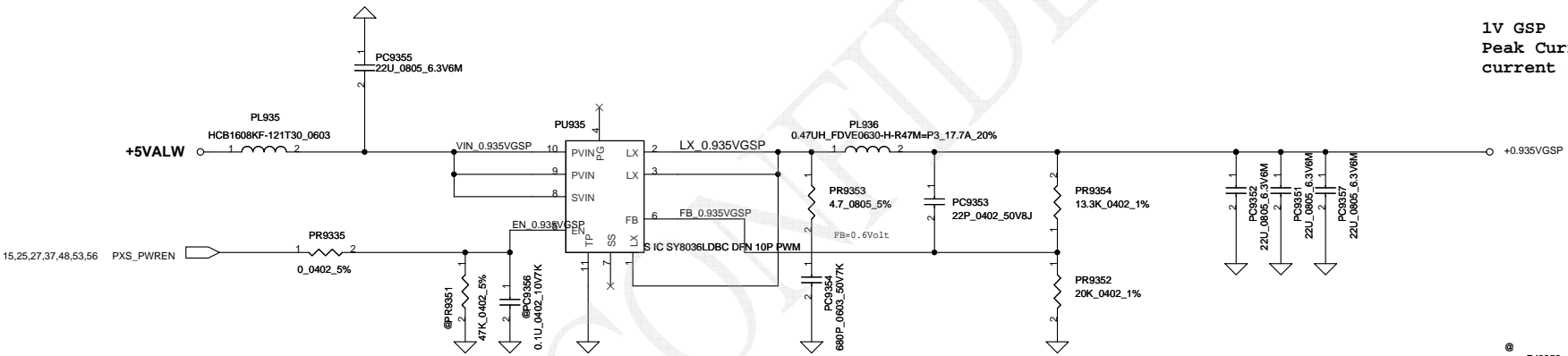
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1.5VPCIEP
Peak Current 6A
OCP current 6A



(6A,240mils ,Via NO.= 12)

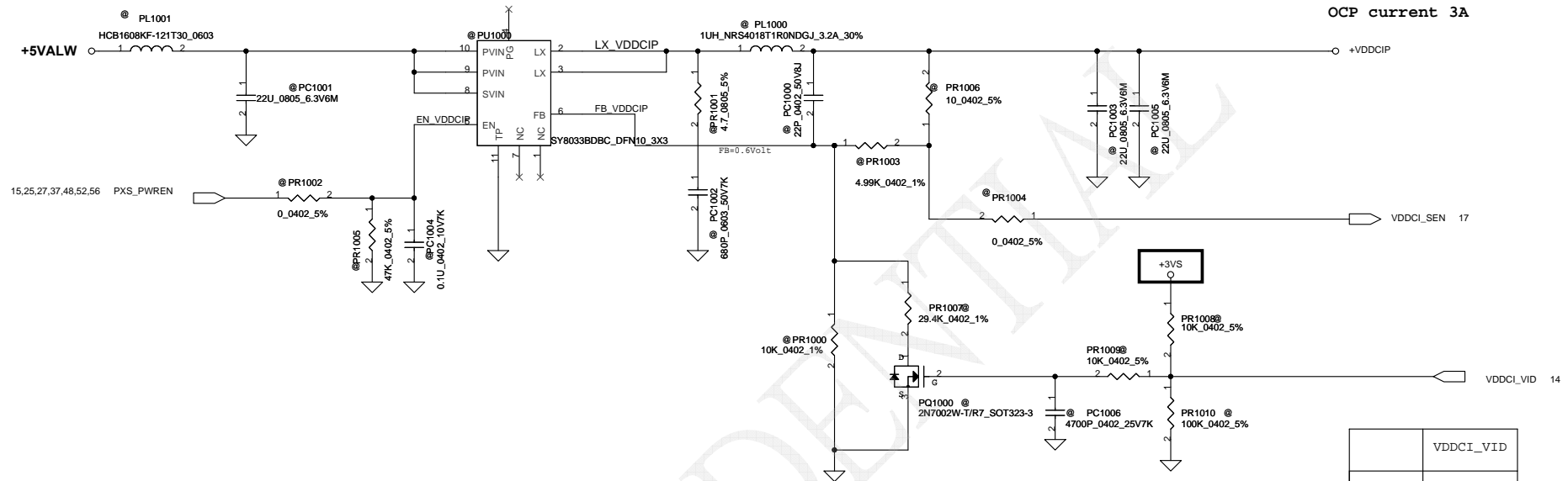
1V GSP
Peak Current 4.2A
current limited 6A



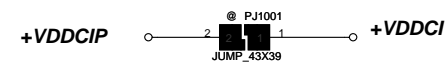
(4.2A,460mils ,Via NO.= 8.4)

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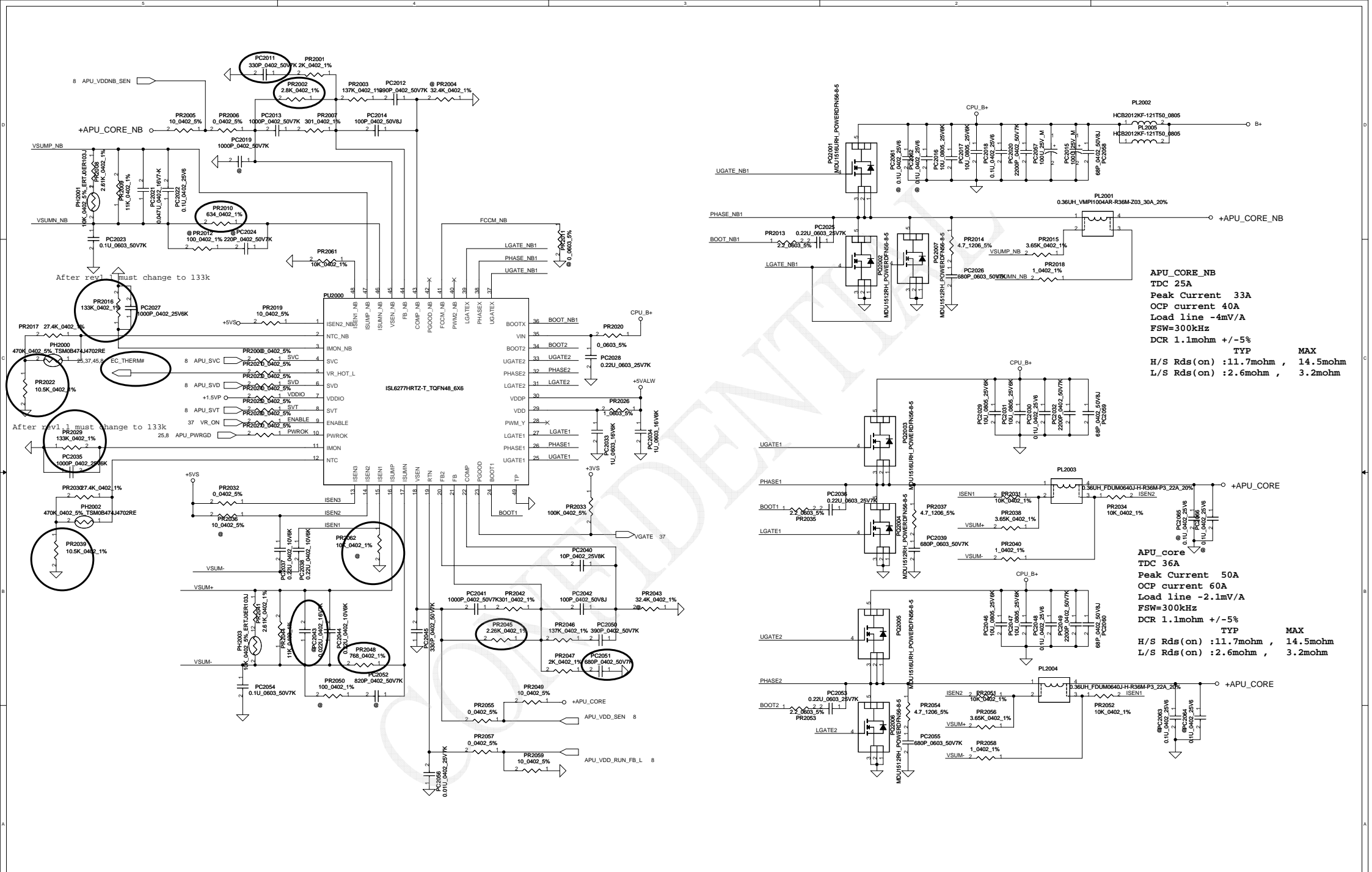
+VDDCI
TDC 2.2A
OCP current 3A



	VDDCI_VID
High	1V
Low	0.9V



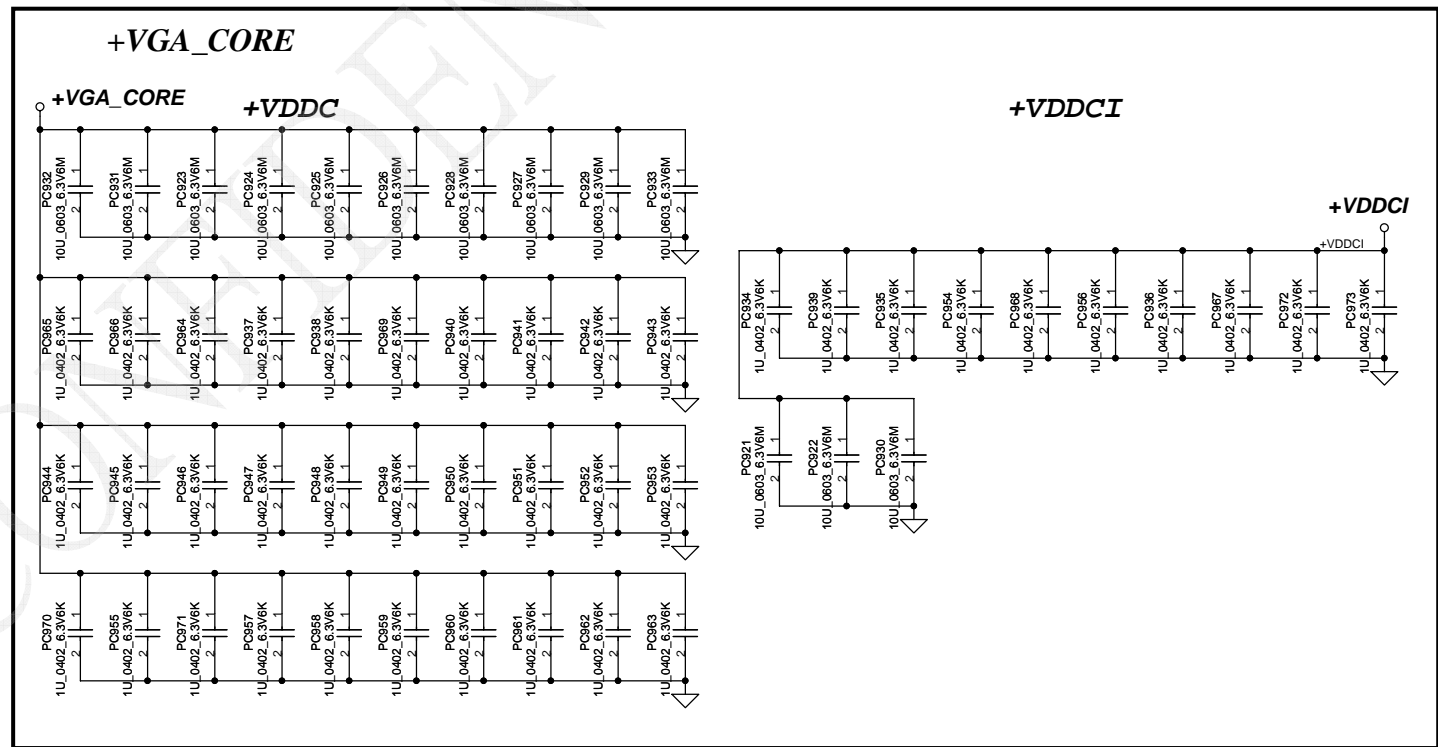
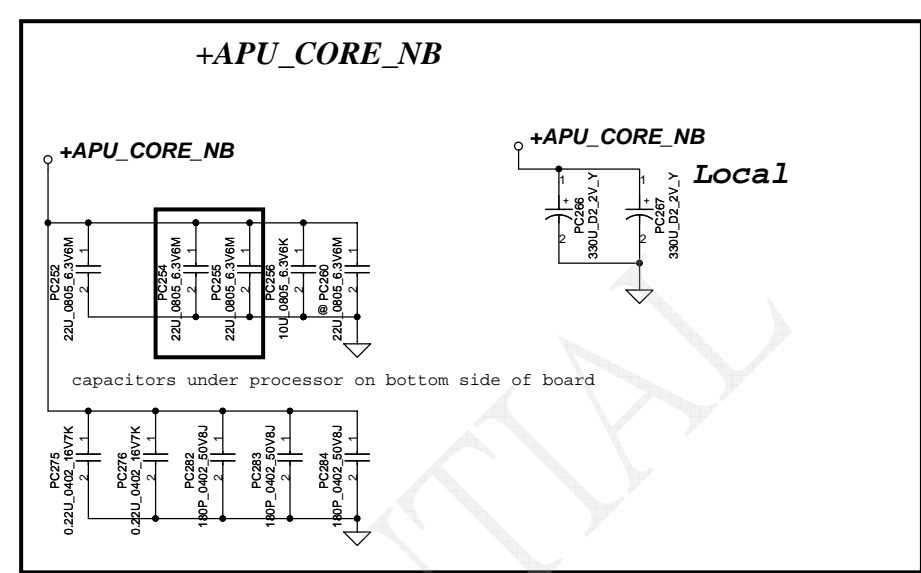
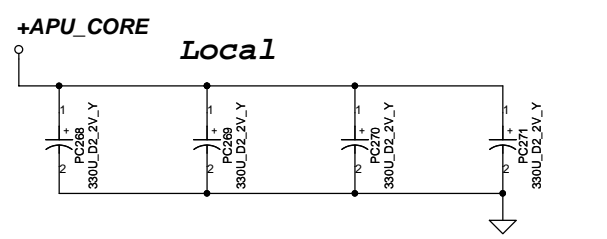
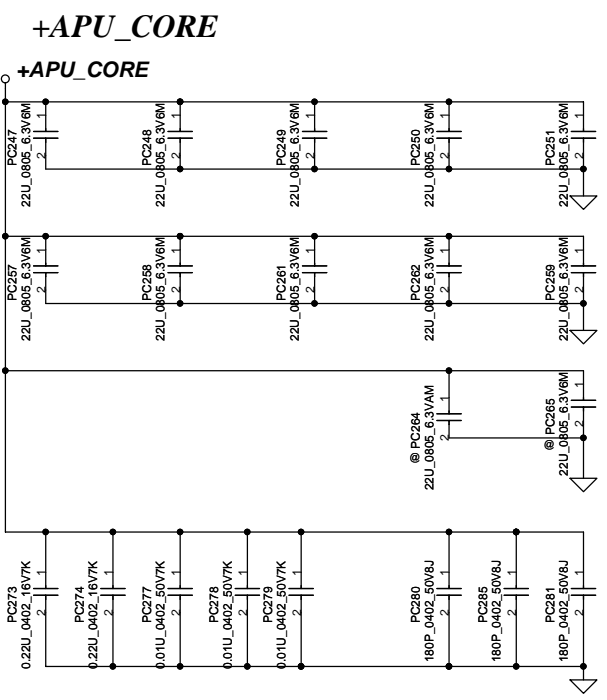
(2.2A,100mils ,Via NO.= 5)



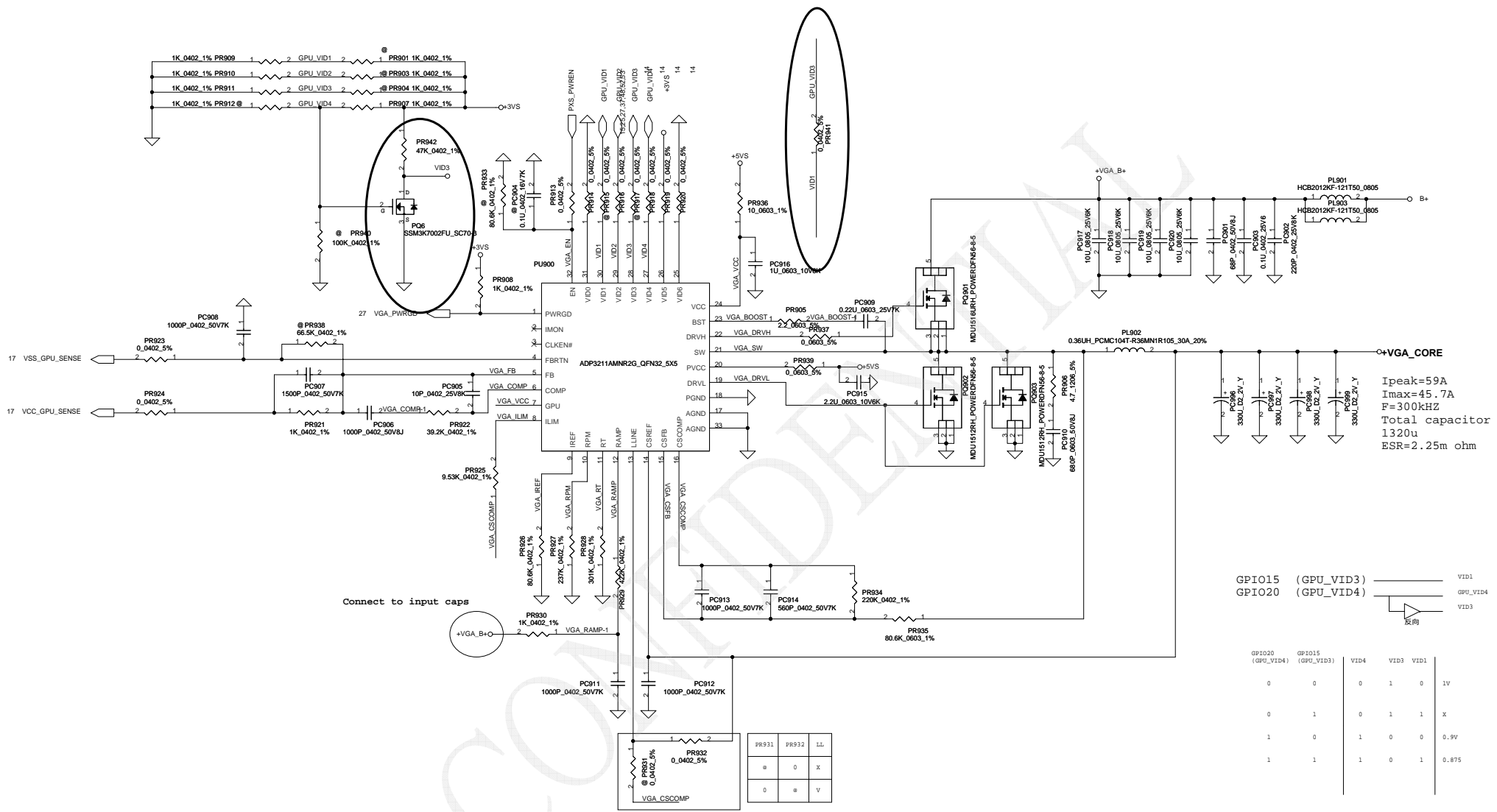
APU_CORE_NB
 TDC 25A
 Peak Current 33A
 OCP current 40A
 Load line -4mV/A
 FSW=300kHz
 DCR 1.1mohm +/-5%
 TYP MAX
 H/S Rds(on) : 11.7mohm , 14.5mohm
 L/S Rds(on) : 2.6mohm , 3.2mohm

APU_core
 TDC 36A
 Peak Current 50A
 OCP current 60A
 Load line -2.1mV/A
 FSW=300kHz
 DCR 1.1mohm +/-5%
 TYP MAX
 H/S Rds(on) : 11.7mohm , 14.5mohm
 L/S Rds(on) : 2.6mohm , 3.2mohm

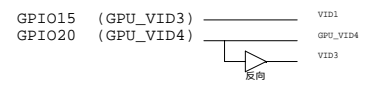
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Ipeak=59A
 Imax=45.7A
 F=300kHz
 Total capacitor
 1320u
 ESR=2.25m ohm



GPIO20 (GPU_VID4)	GPIO15 (GPU_VID3)	VID4	VID3	VID1	
0	0	0	1	0	1V
0	1	0	1	1	X
1	0	1	0	0	0.9V
1	1	1	0	1	0.875

PR931	PR932	LL
#	0	X
0	#	V

NO DATE	PAGE	MODIFICATION LIST	PURPOSE
DB-2(12/2)	P52-PWR-+1.5VPCIE/0.935V	Change PU935 SY8809 to SY8036	For co-lay cost down
DB-2(12/2)	P56-PWR_VGA_CORE	Add PQ6,PR941,PR942,PR940	For co-lay Thames and Chelsea
DB-2(12/2)	P44-PWR-DCIN / Vin Detector	Change to PJP1 pine define	DC-IN jack buy and sale define does not change
DB-2(12/8)	P45-PWR-BATTERY CONN	Pin 7 power source change +3VLP to +3VALW	EC command
DB-2(12/8)	P52-PWR-+1.5VPCIE/0.935V	PC11506 loaction change to PC1156	CIC SMT command
DB-2(12/12)	P52-PWR-+1.5VPCIE/1V	Change PR9352 11.3K to 13.3K (0.935V to 1V)	HW comand
DB-2(12/12)	P53-PWR-+VDDCIP	Reserver the VDDCI component	For thames GPU
DB-2(12/12)	P56-PWR_VGA_CORE	Add PR940,PR942,PQ6 ,reserve PR915 and PR917	For thames GPU
DB-2(12/13)	P50-PWR-1.1VALWP	Add PR803 =10K	SY8809 enbale pin issue
SI(12/30)	P54-PWR-CPU_CORE/CPU_CORE_NB	PC2057 change 33u 6.3*4.5	ME height limited
SI(12/30)	P54-PWR-CPU_CORE/CPU_CORE_NB	Add PC2061,PC2062,PC2063,PC2064,PC2065&PC2066,	EMI command

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Security Classification		Compal Secret Data		Title	
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