

SP7(Nikita) BLOCK DIAGRAM PV

01

PCB STACK UP 12L Dis.

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(High)
LAYER 5 : SGND
LAYER 6 : IN3(High)
LAYER 7 : SVCC1
LAYER 8 : SVCC2
LAYER 9 : IN4
LAYER10 : IN5(High)
LAYER11 : GND
LAYER12 : BOT

A Channel
DDR3-SODIMM1
DDR3-SODIMM2
PAGE 13,14

B Channel
DDR3-SODIMM3
DDR3-SODIMM4
PAGE 15,16

USB3.0 Port x2
PAGE 26

NEC USB3.0 Controller
PAGE 26

Intel Clarksfield
CPU 45Watt
4 Core
(rPGA 989)
PAGE 3-6

VRAM DDR3*8 (1Gb)
PAGE 23-24

ATI M97/Broadway/Madison (128bit) (FCBGA) 962p 29X29mm
PAGE 18-22

HDMI CON (1920*1200)
PAGE 25

LCD CONN for dual channel (15.6")
PAGE 25

PCH 3.5Watt
Platform Controller Hub
PAGE 7-12

CLOCK GEN 9LRS3197
PAGE 02

Braiwood (NAND Flash Memory)
PAGE 34

CPU THERMAL SENSOR
PAGE 27

SATA 2.5" HDD / SATA 1.8" SSD1
PAGE 30

SATA 1.8" SSD2
PAGE 30

E-SATA(USB2.0)
PAGE 26

Accelerometer
LIS3LV02DL PAGE 31

Keyboard Touch Pad / Light Sensor
PAGE 31

GMT G9931P1U SYSTEM/VGA FAN
PAGE 27

SPI (SYSTEM BIOS)
PAGE 33

BATTERY SELECTOR
PAGE 42

SYSTEM CHARGER(BQ24704)
PAGE 41

SYSTEM POWER ISL6237IRZ-T
PAGE 35

DDR III SMD DR_VTERM 1.8V/1.8VSUS(VT356/VT357)
PAGE 39

VCCP +1.5V AND GMCH 1.05V(RT8204)
PAGE 36

VGACORE RT8208
PAGE 38

CPU CORE VT1312M/VT1317
PAGE 37

ENE KBC KB3926 C2
PAGE 33

Audio IDT92HD75B2
PAGE 28

AUDIO Amplifier TPA6047A4
PAGE 29

LAN Atheros PCIE-LAN AR8131(M) GigaLAN
PAGE 32

RJ45
PAGE 32

half size mini-card (Wireless LAN Shirley Peak 802.11a/b/g/n)
PAGE 34

Card Reader
Realtek RTS5159
PAGE 30

2-in-1 flash media slot(SD/MMC)
PAGE 30

Internal Microphones (MEMS)
PAGE 31

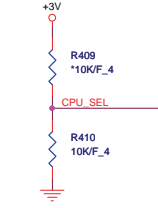
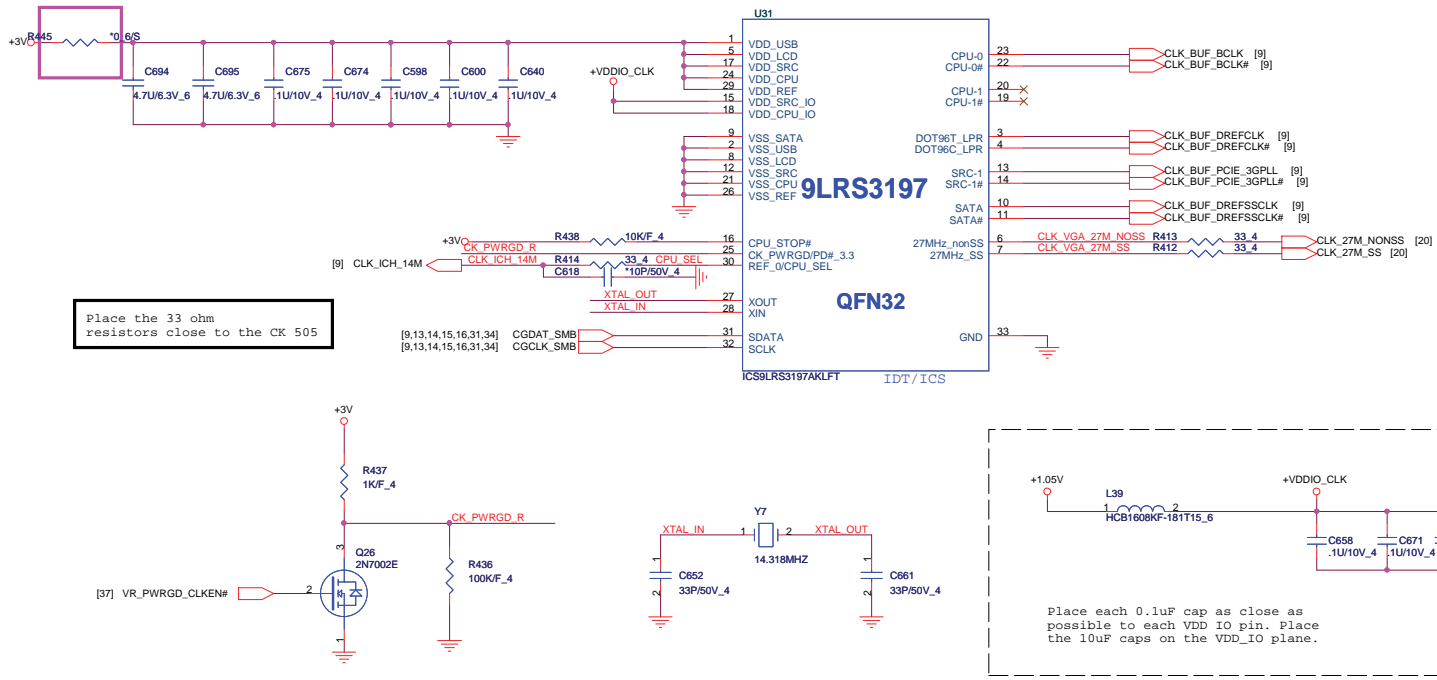
Combo Jack (Headphone/MIC)
PAGE 28

Jack to Speaker
PAGE 29

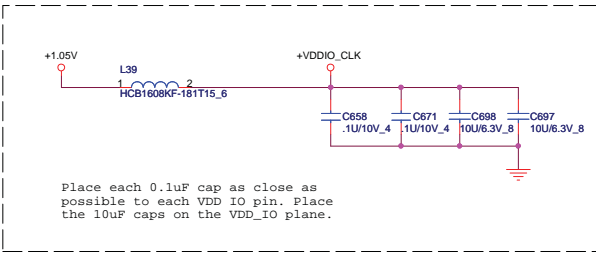


PROJECT : SP7
Quanta Computer Inc.

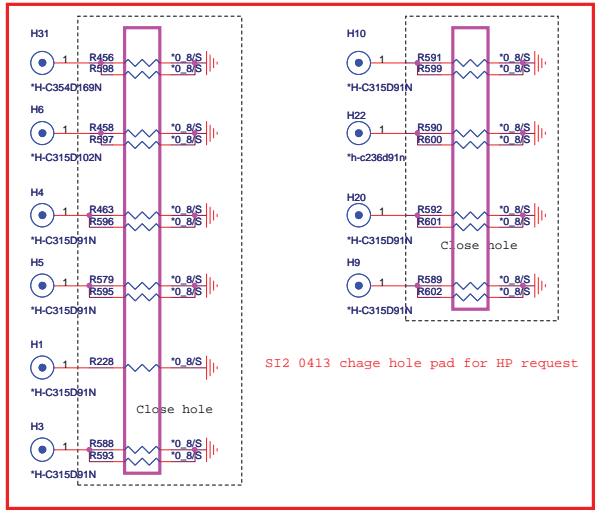
Size Custom	Document Number	Rev 1A
Block Diagram		
Date: Friday, July 10, 2009	Sheet 1 of 42	



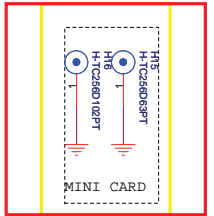
CPU_SEL	0	1
	CPU0/1=133MHz (default)	CPU0/1=100MHz



M/B Screw Hole

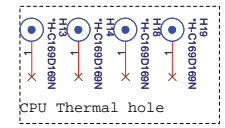


MINI CARD

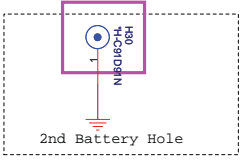


SI 0223 change footprint
SI2 0413 change BOM

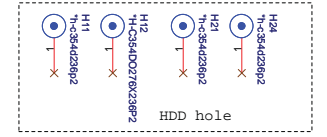
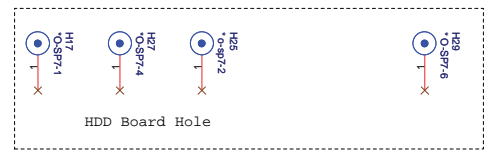
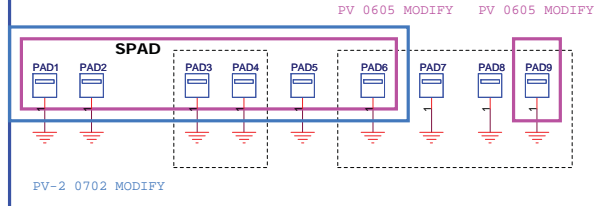
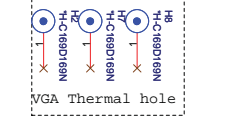
CPU Thermal hole



2nd Battery Hole



VGA Thermal hole



[3,7,8,9,10,11,13,14,15,16,18,25,26,27,28,29,30,31,32,33,34,37,40]
[7,8,9,11,26,27,36,37] +3V +1.05V

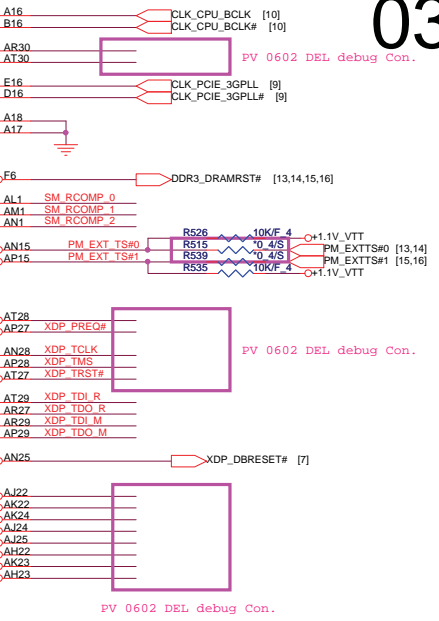
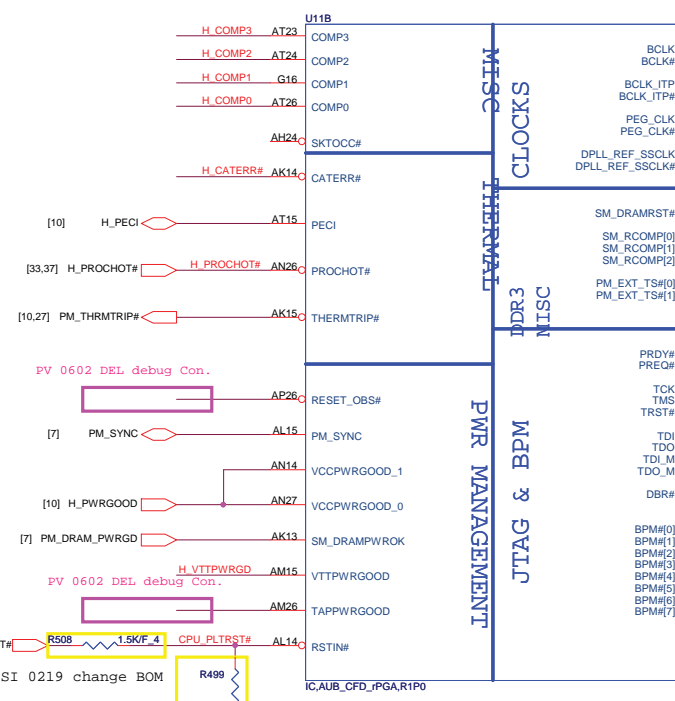
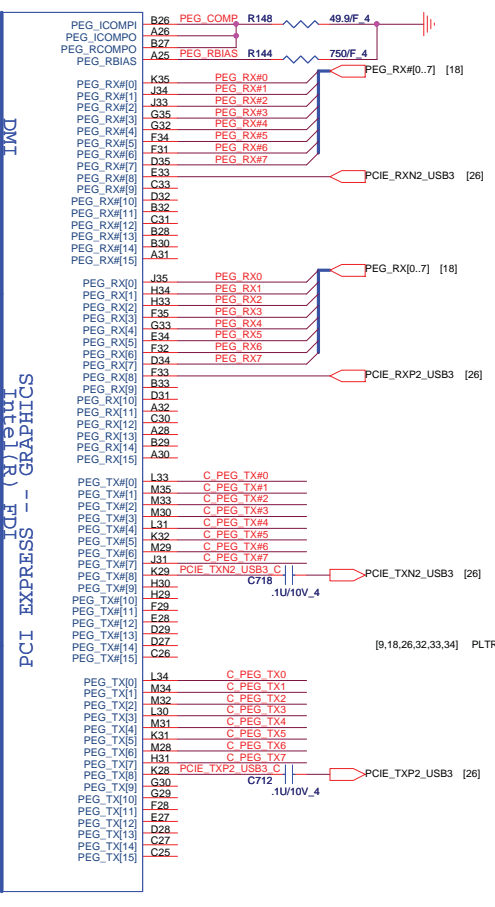
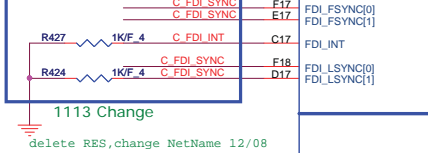
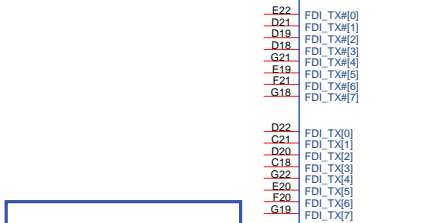
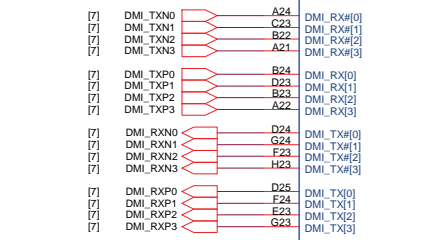
	PROJECT : SP7		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number CLOCK & Screw Holes	
Sheet 2 of 42			

U11A

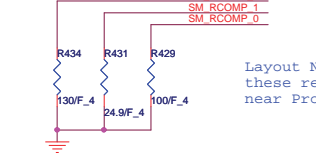
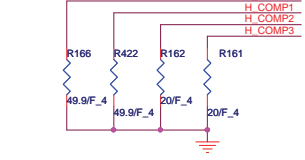
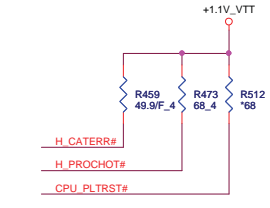
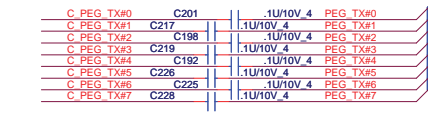
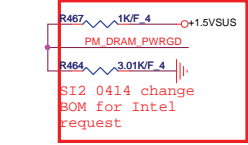
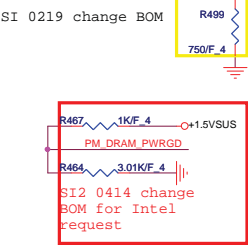
U11B

ICF (R) IEM (M) PCI EXPRESS - GRAPHICS

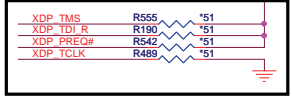
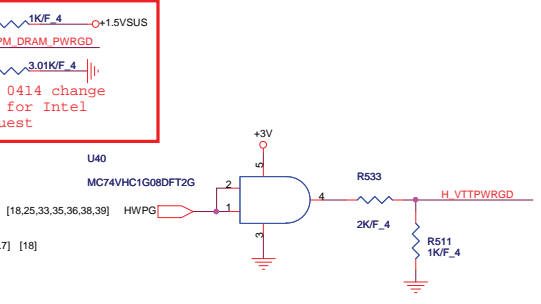
CLOCKS
INTERNAL
DDR3
MISC
JTAG & BPM
PWR MANAGEMENT



1113 Change
delete RES, change NetName 12/08



Layout Note: Place these resistors near Processor



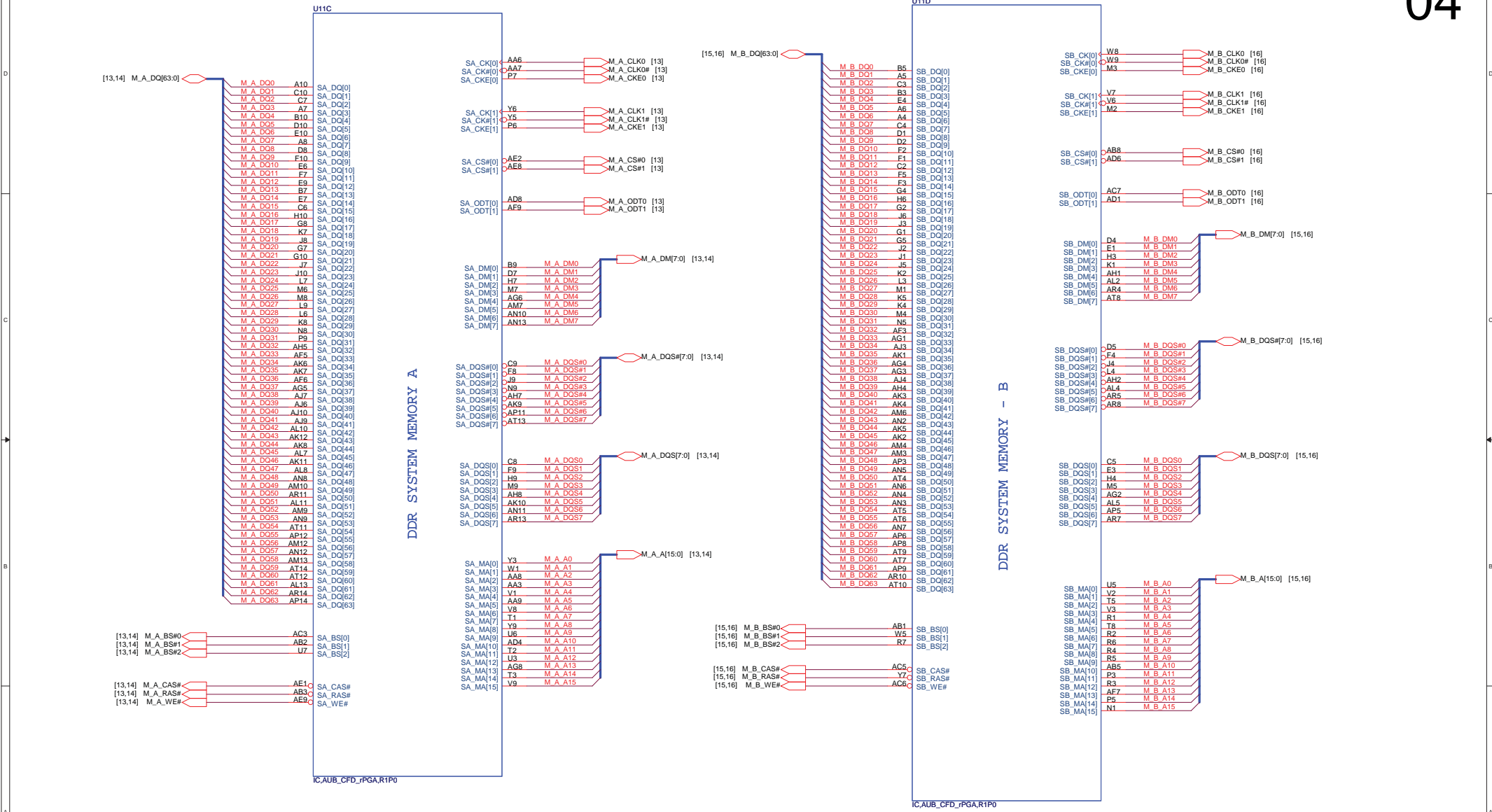
JTAG MAPPING
PV 0602 DEL debug Con.

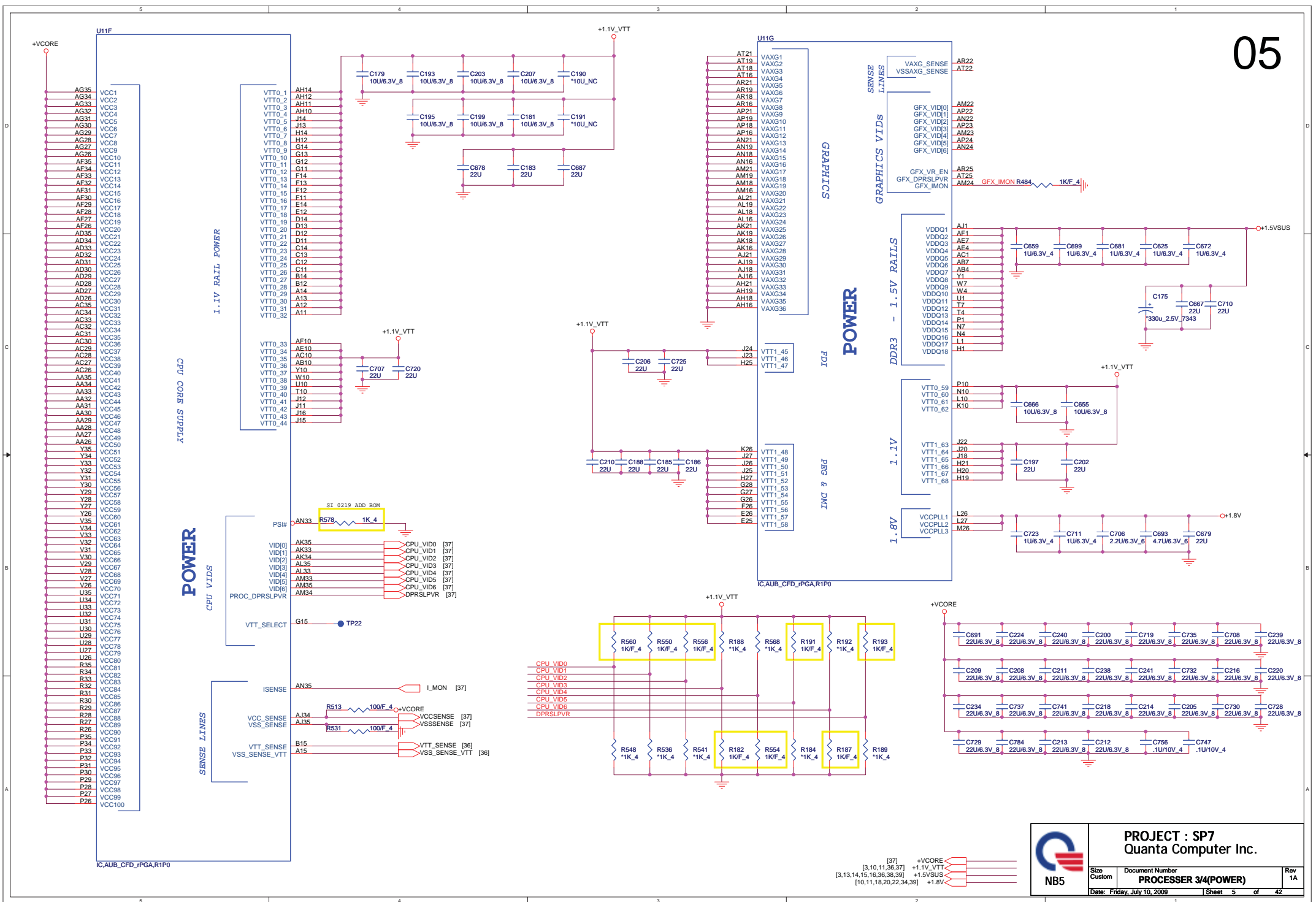
Scan Chain (Default)	STUFF -> R97, R89, R90 NO STUFF -> R84, R512
CPU Only	STUFF -> R97, R84 NO STUFF -> R89, R512, R90
GMCH Only	STUFF -> R512, R90 NO STUFF -> R97, R84, R89

PROJECT : SP7
Quanta Computer Inc.

NB5	Size Custom	Document Number	Rev 1A
		PROCESSOR 1/4(HOST&PEX)	
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AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)





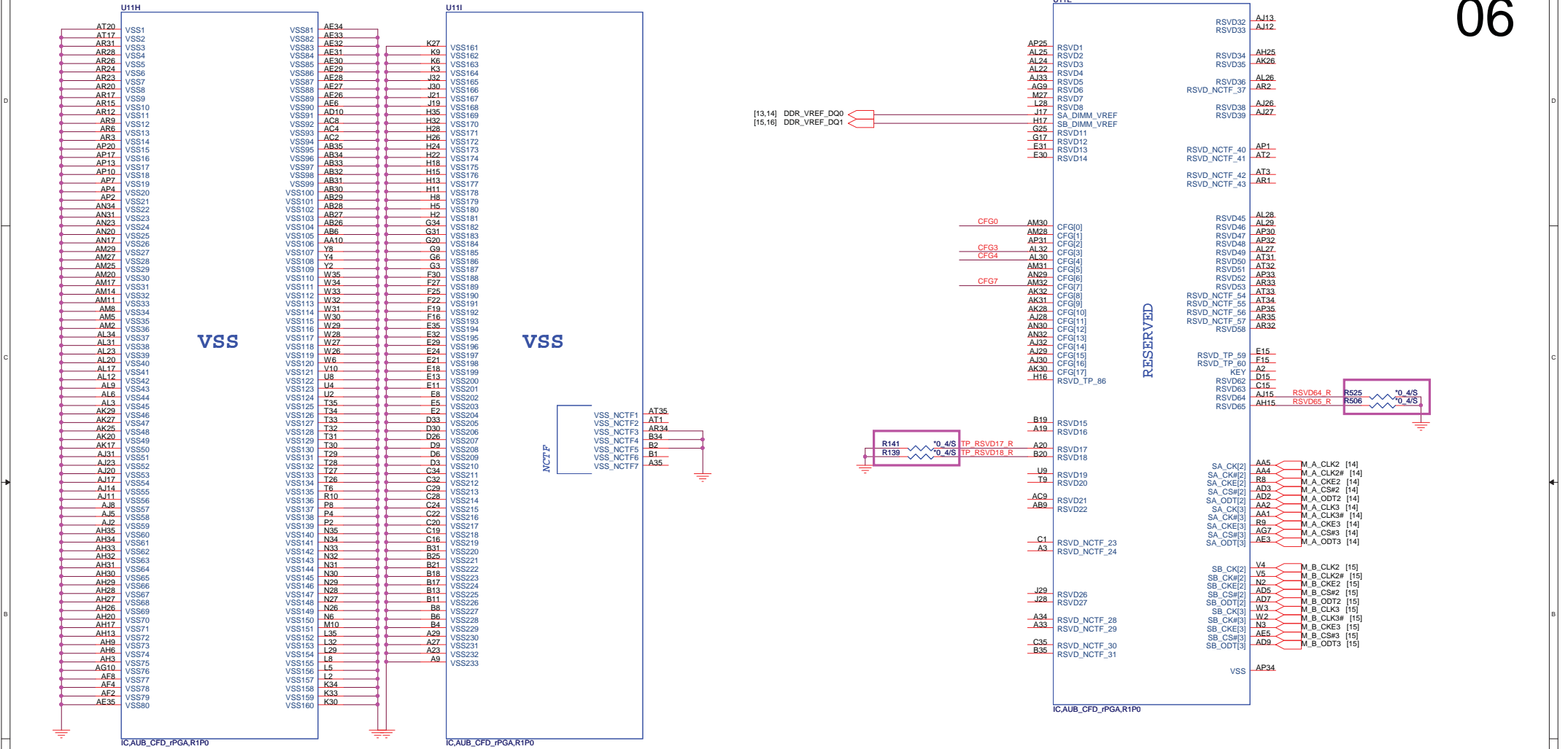
	PROJECT : SP7			Size Custom Date: Friday, July 10, 2009
	Quanta Computer Inc.			
	PROCESSOR 3/4(POWER)			
	Document Number PROCESSOR 3/4(POWER)	Rev 1A		

[37]	+VCORE	[37]
[3,13,14,15,16,36,38,39]	+1.1V_VTT	[37]
[10,11,16,20,22,34,39]	+1.5VSUS	[37]
	+1.8V	[37]

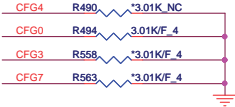
AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)

06



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG7[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.



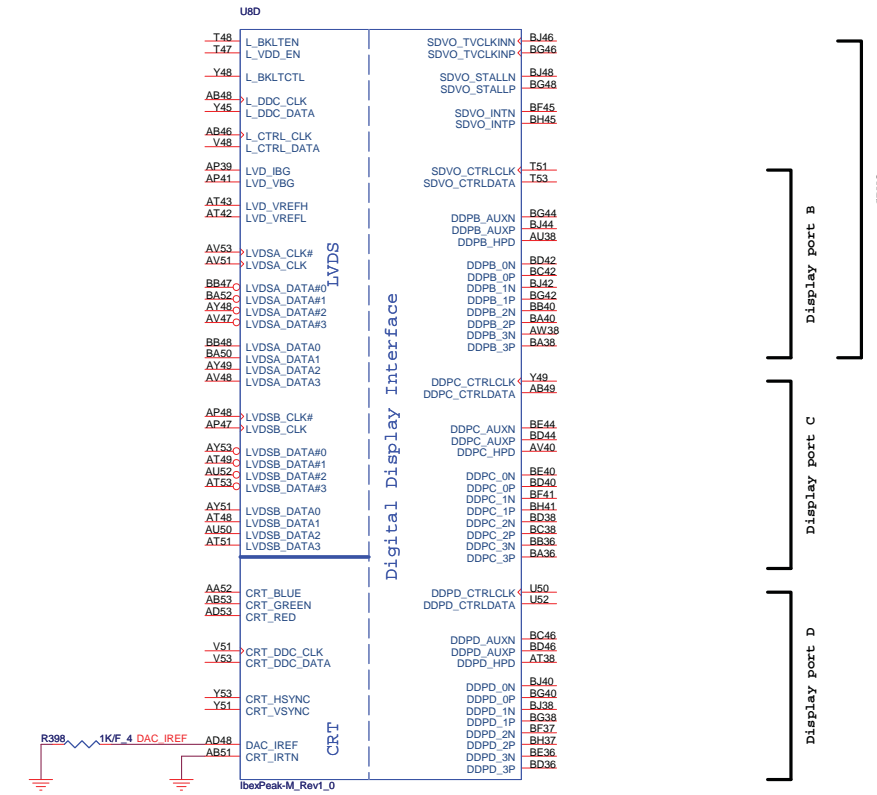
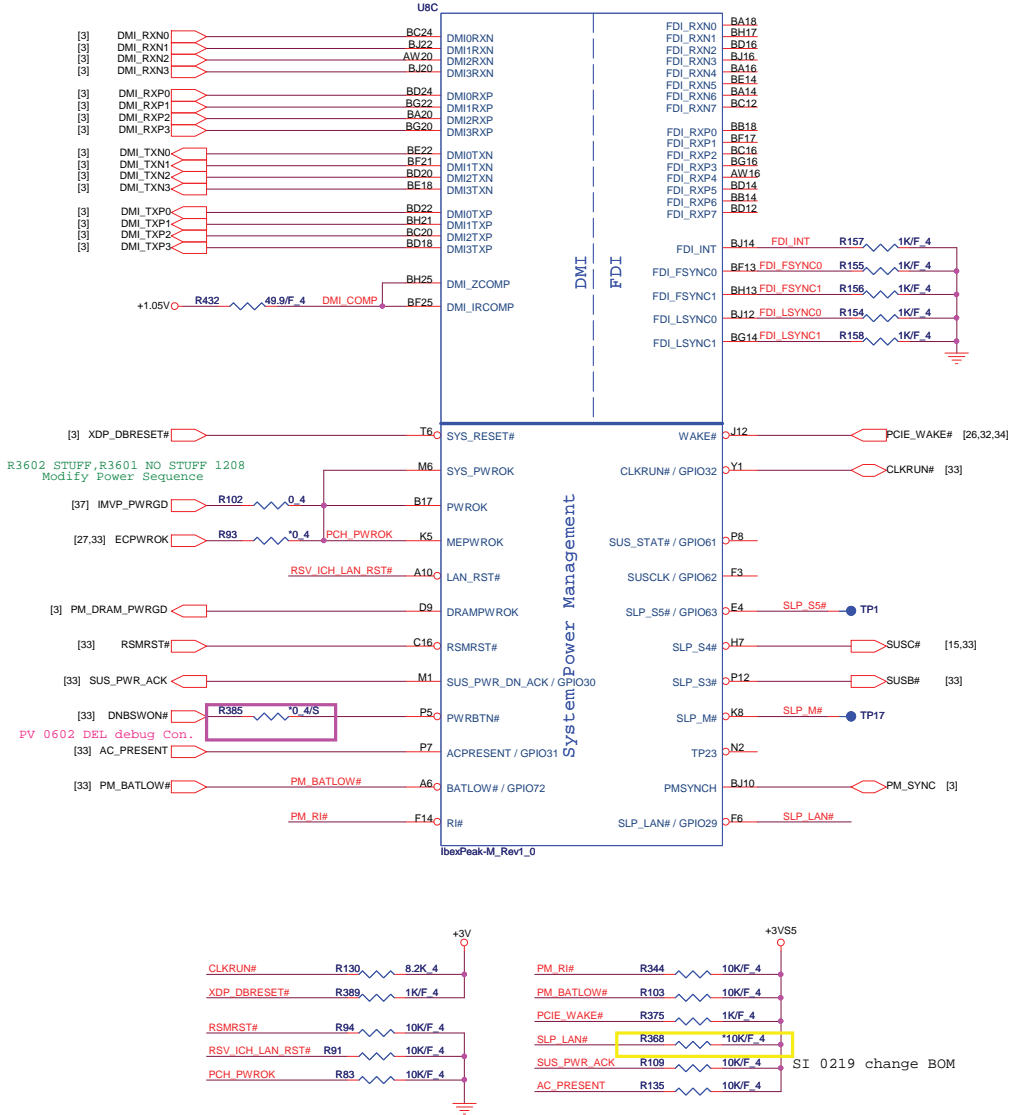
	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

PROJECT : SP7
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Size Custom	Document Number	Rev 1A
PROCESSOR 4/4(GND)		
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IBEX PEAK-M (DMI, FDI, GPIO)

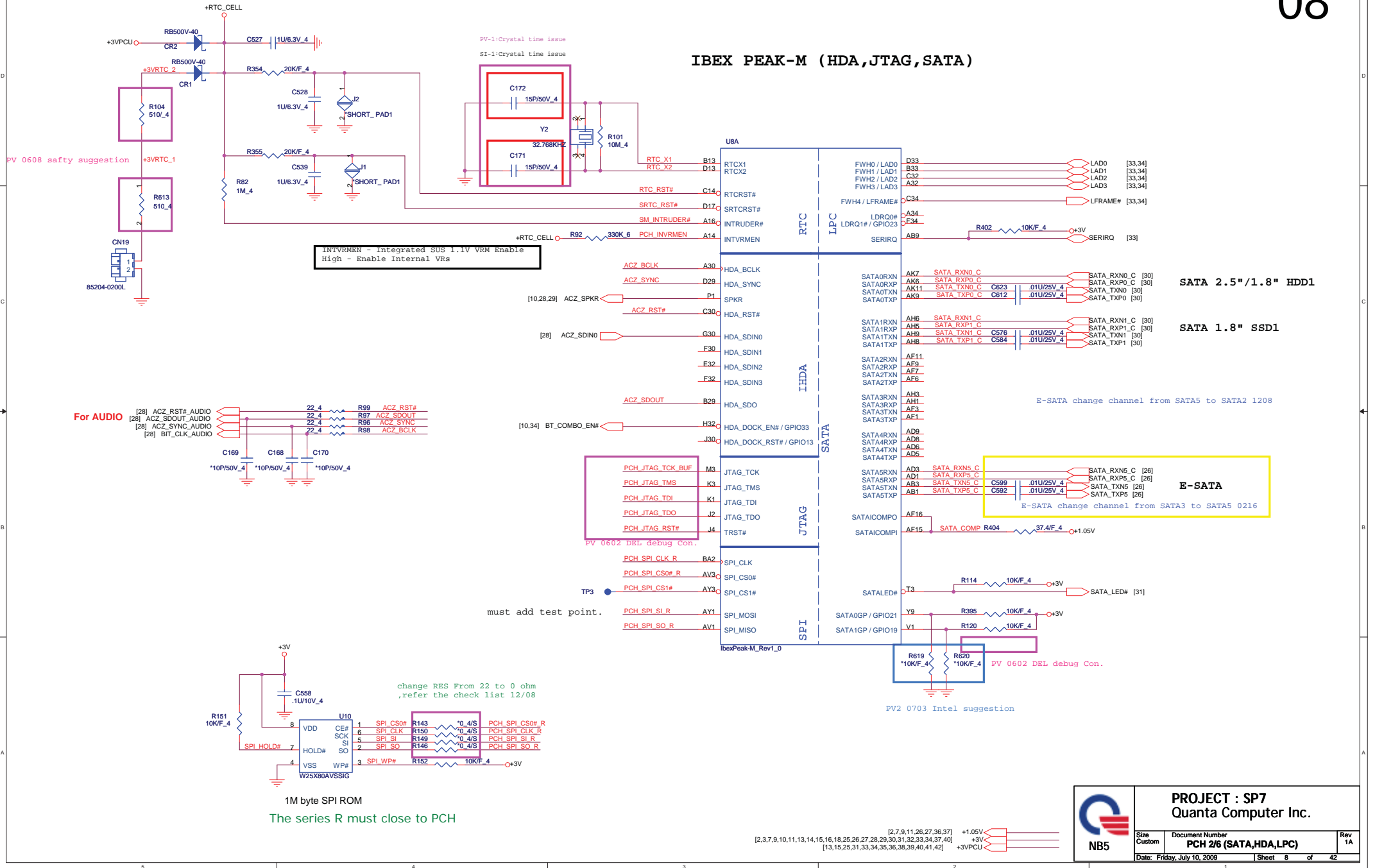
IBEX PEAK-M (LVDS, DDI)



	PROJECT : SP7	
	Quanta Computer Inc.	
Size Custom	Document Number PCH 1/6 (DMI,PM,VIDEO)	Rev 1A
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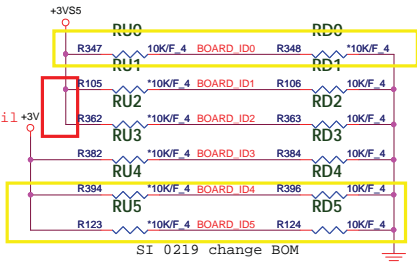
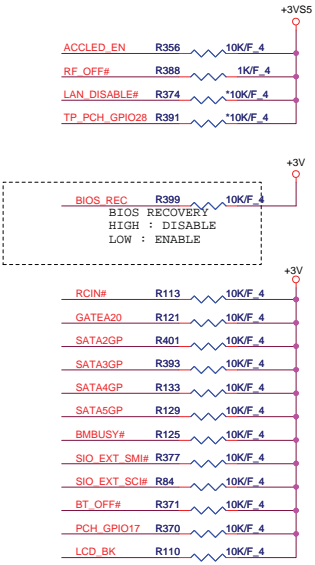
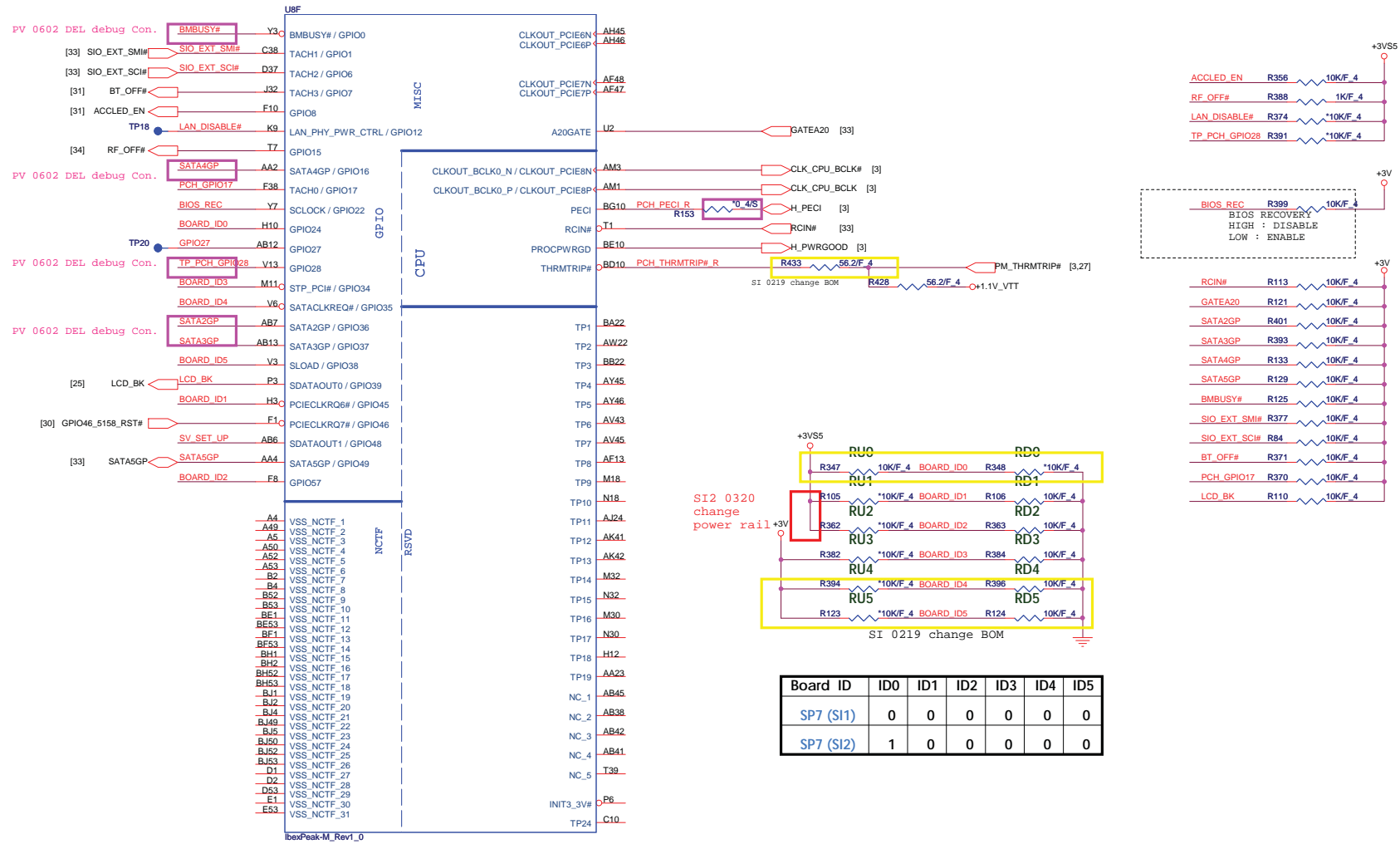
[2,8,9,11,26,27,36,37] +1.05V
 [2,3,8,9,10,11,13,14,15,16,18,25,26,27,28,29,30,31,32,33,34,37,40] +3V
 [9,10,11,25,40] +3VS5

IBEX PEAK-M (HDA, JTAG, SATA)



	PROJECT : SP7		Date: Friday, July 10, 2009
	Quanta Computer Inc.		
	Size Custom Document Number PCH 2/6 (SATA,HDA,LPC)	Rev 1A	
[2,3,7,9,10,11,13,14,15,16,18,25,26,27,28,29,30,31,32,33,34,37,40] [13,15,25,31,33,34,35,36,38,39,40,41,42]		+1.05V +3V +3VPCU	Sheet 8 of 42

IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



Board ID	ID0	ID1	ID2	ID3	ID4	ID5
SP7 (SI1)	0	0	0	0	0	0
SP7 (SI2)	1	0	0	0	0	0

A16 swap override Strap/Top-Block Swap Override jumper

GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default
-------	---

SV_SET_UP 1-X High = Strong (Default)



Boot BIOS Strap

PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

Danbury Technology Enabled

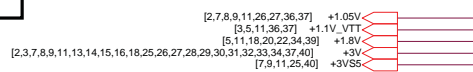
NV_ALE	High = Enable Low = Disable
--------	--------------------------------

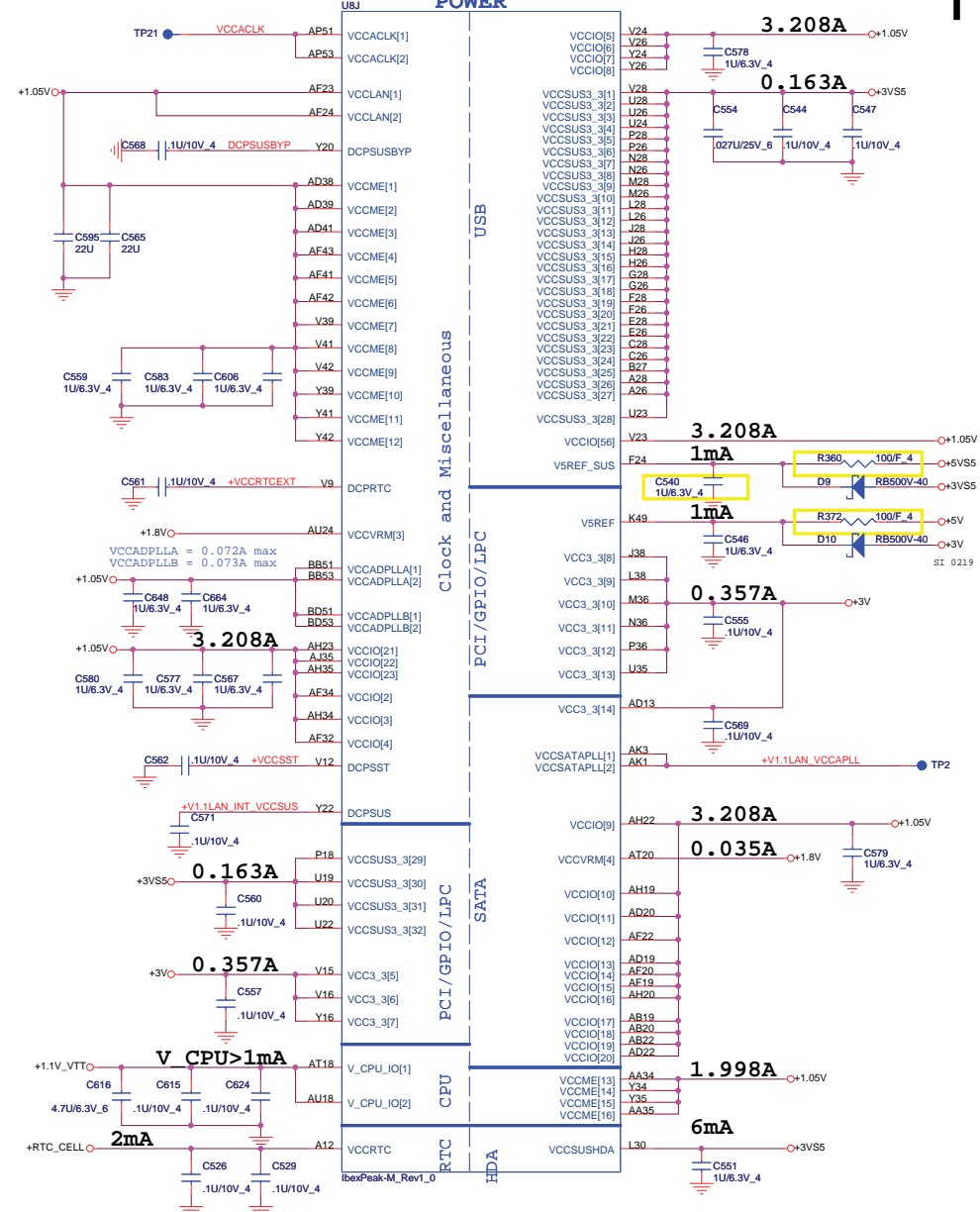
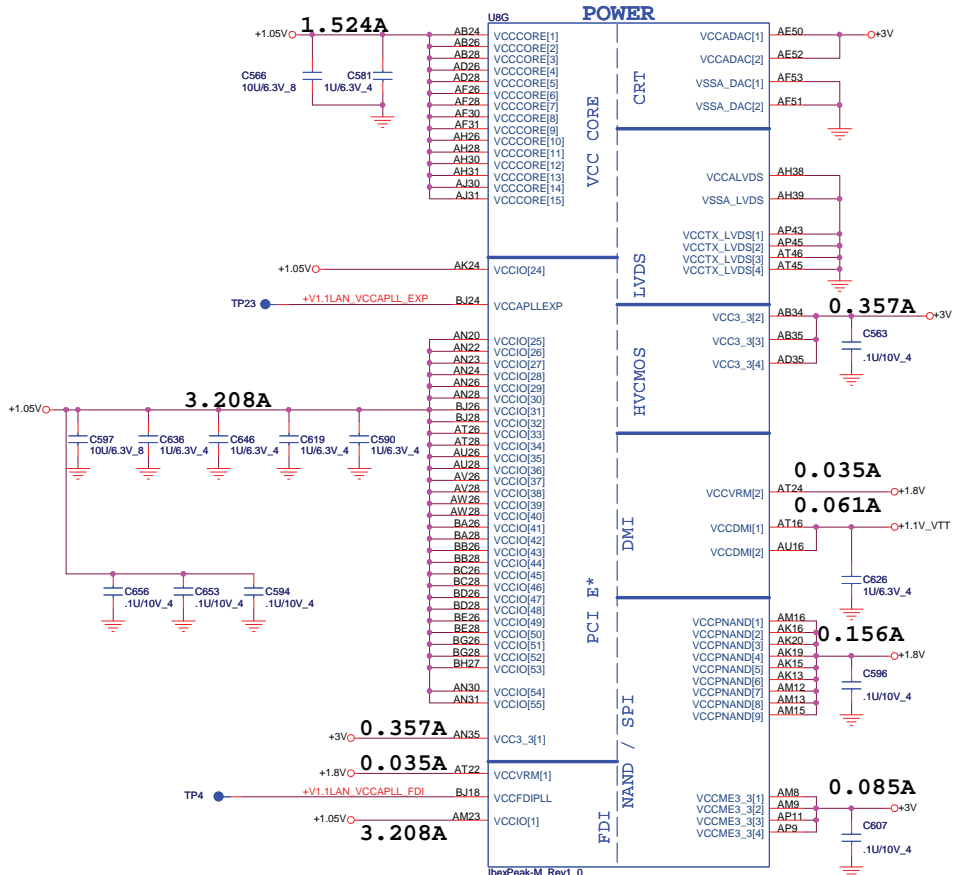
DMI Termination Voltage

NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH
--------	---

**PROJECT : SP7
Quanta Computer Inc.**

Size Custom	Document Number PCH 4/6 (GPIO & Strap)	Rev 1A
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[2,7,8,9,26,27,36,37]	+1.05V
[3,5,10,36,37]	+1.1V_VTT
[5,10,16,20,22,34,39]	+1.8V
[2,3,7,8,9,10,13,14,15,16,18,25,26,27,28,29,30,31,32,33,34,37,40]	+3V
[7,9,10,25,40]	+3V5S
[8]	+RTC_CELL
[25,27,29,30,37,40]	+5V
[40]	+5V5S

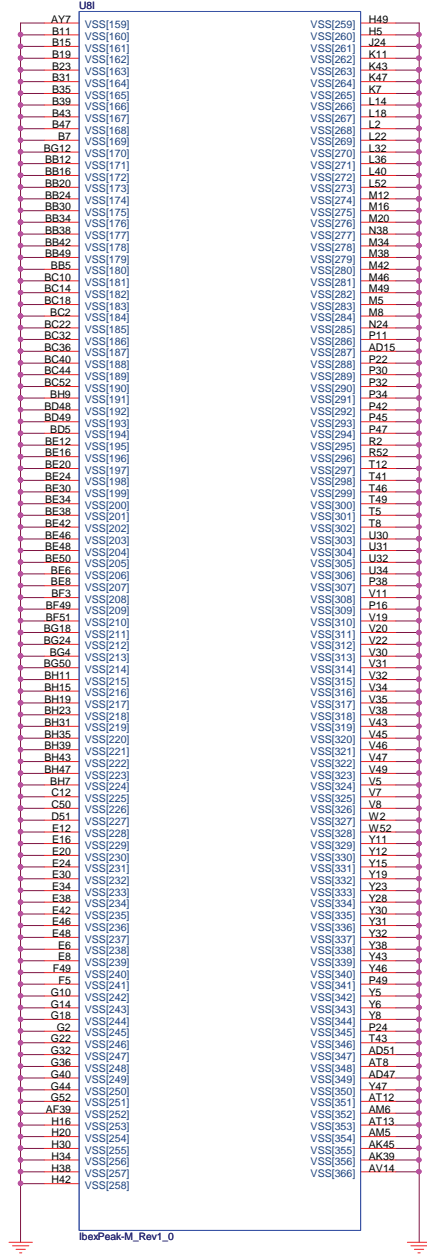
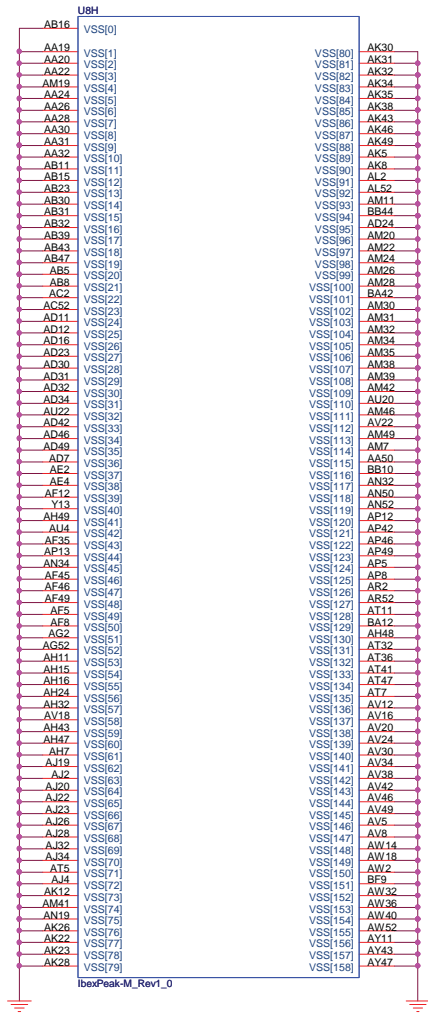
PROJECT : SP7

Quanta Computer Inc.

Size Custom	Document Number PCH 5/6 (POWER)	Rev 1A
Date: Friday, July 10, 2009 Sheet 11 of 42		

IBEX PEAK-M (GND)

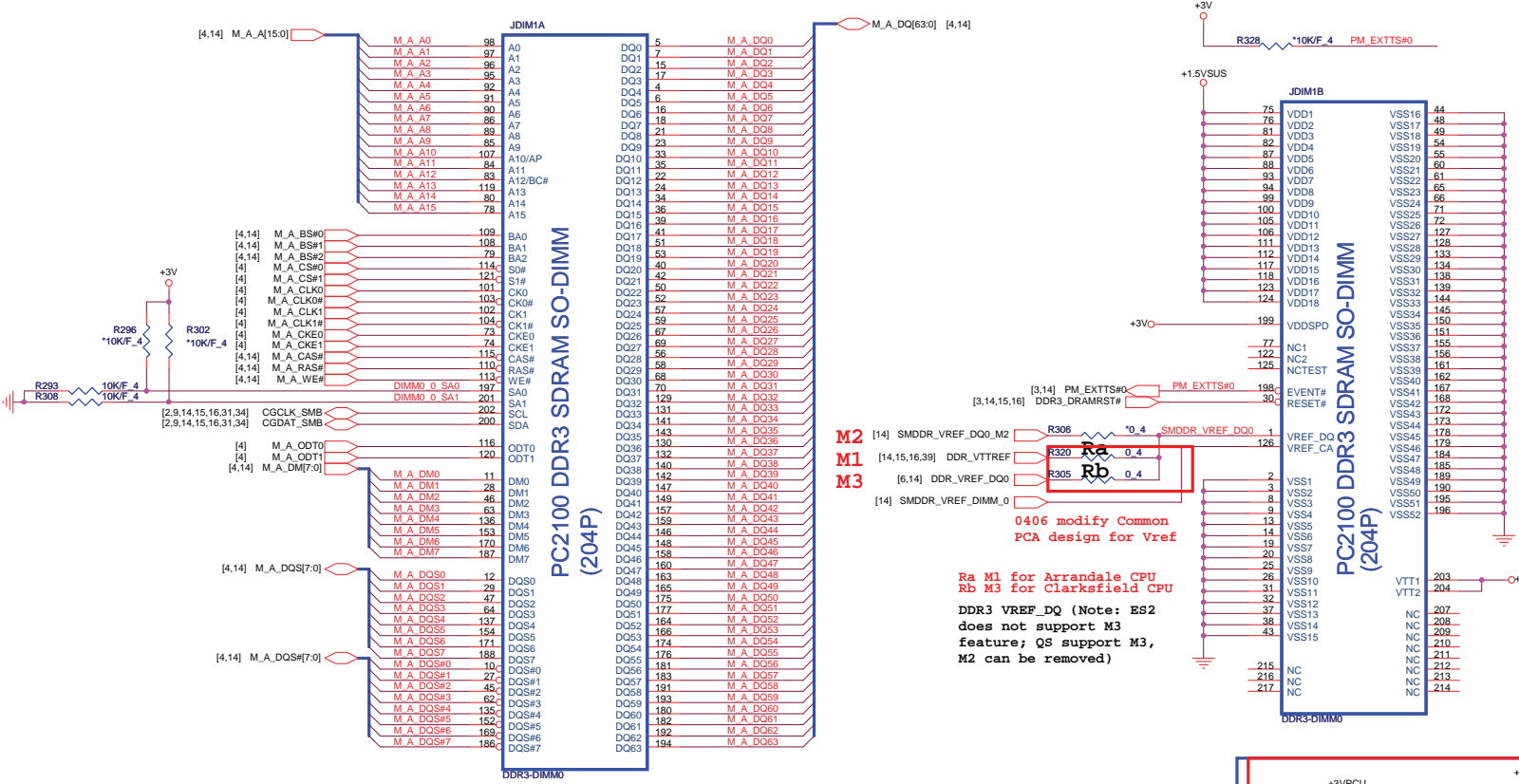
Move to Page 37



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Size Custom	Document Number PCH 6/6 (GND)	Rev 1A
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DDR3 -SODIMM 1 A0

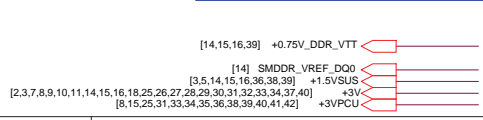
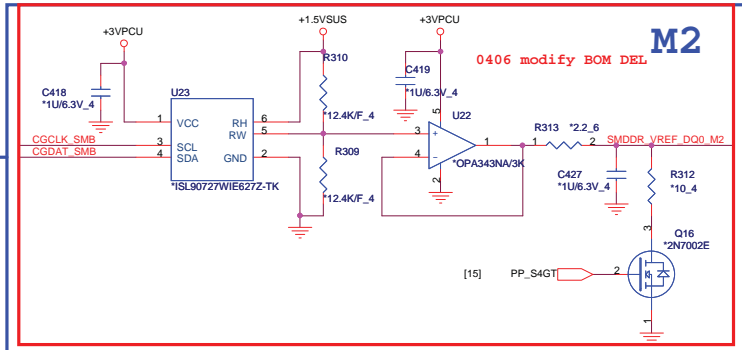
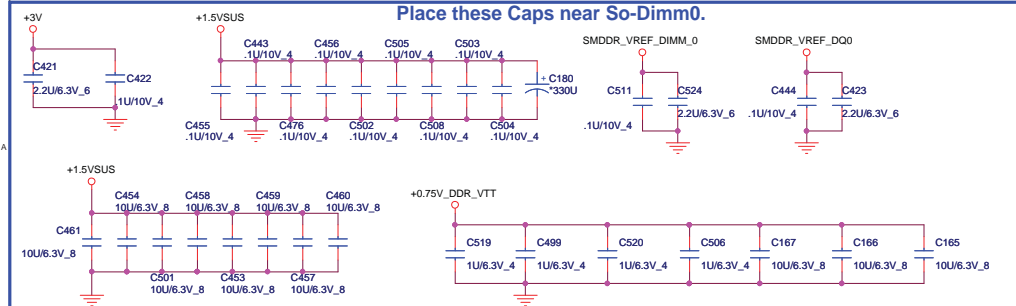


M2 [14] SMDRR_VREF_DQ0_M2
M1 [14,15,16,39] DDR_VTTRF#
M3 [6,14] DDR_VREF_DQ0
 [14] SMDRR_VREF_DIMM_0

0406 modify Common PCA design for Vref

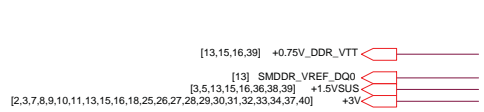
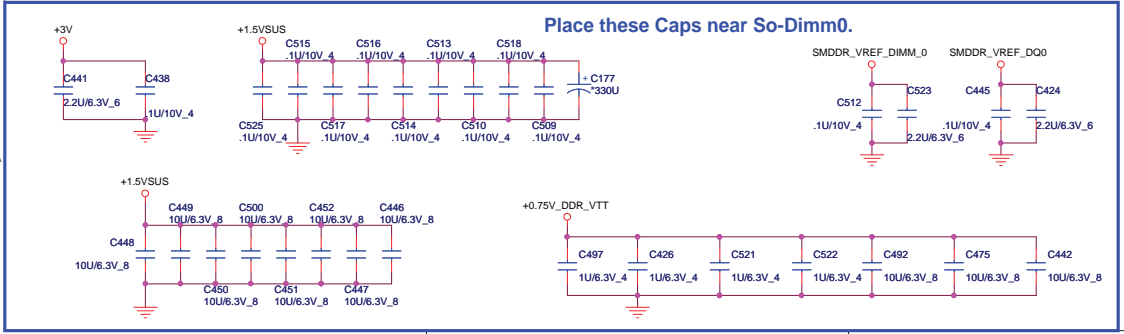
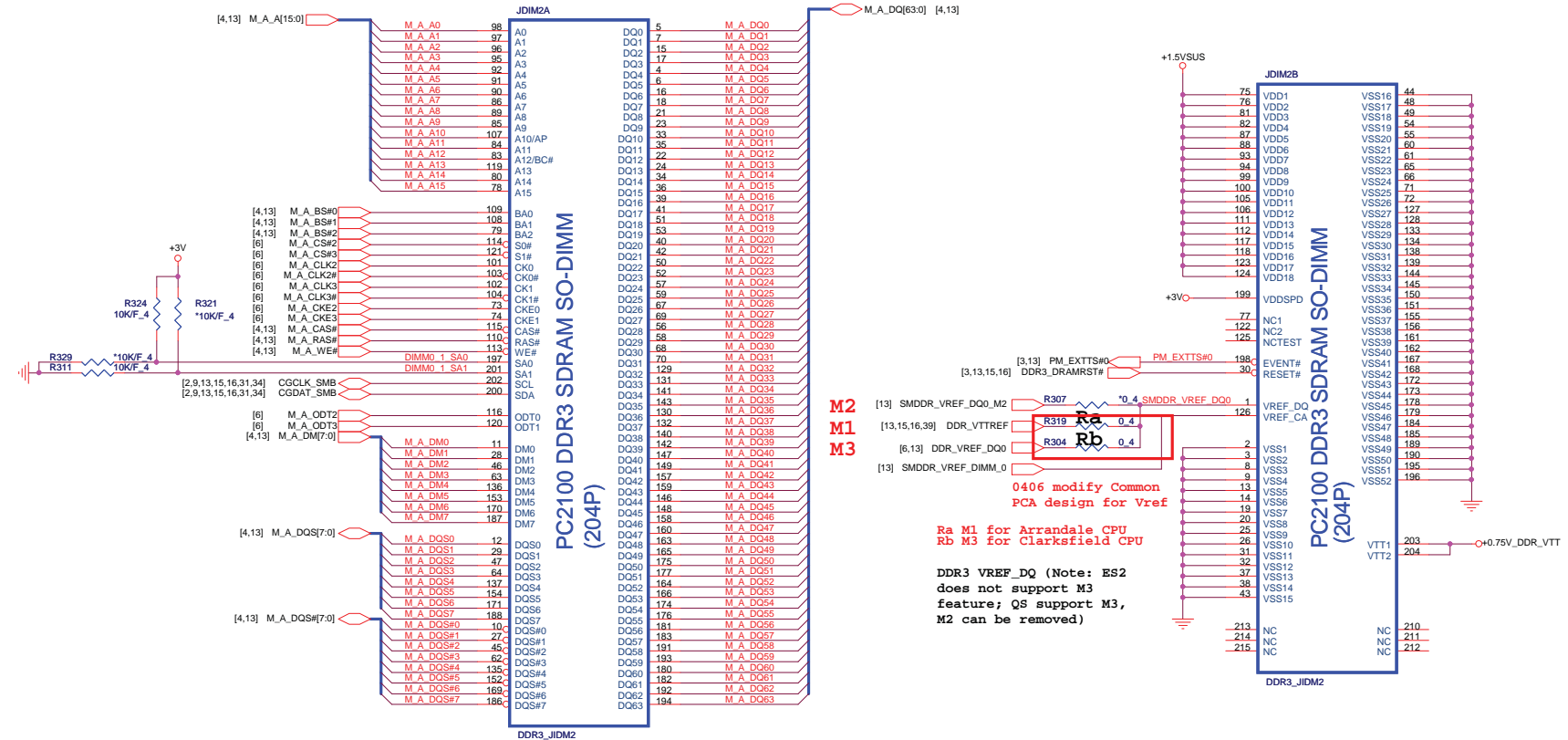
**Ra M1 for Arrandale CPU
 Rb M3 for Clarkfield CPU**

DDR3 VREF_DQ (Note: ES2 does not support M3 feature; Q5 support M3, M2 can be removed)



	PROJECT : SP7 Quanta Computer Inc.		Rev 1A Date: Friday, July 10, 2009	
	Size Custom	Document Number DDR3 DIMM-1		Sheet 13 of 42
	[14,15,16,39] +0.75V_DDR_VTT [14] SMDRR_VREF_DQ0 [3,5,14,15,16,39,39] +1.5VSUS [2,3,7,8,9,10,11,14,15,16,18,25,26,27,28,29,30,31,32,33,34,37,40] +3V [8,15,25,31,33,34,35,36,38,39,40,41,42] +3VPCU			

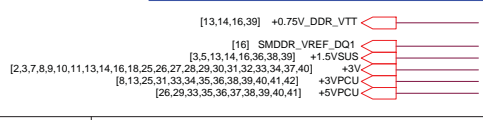
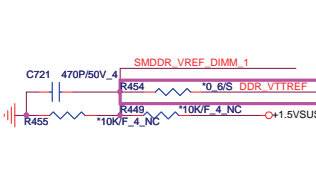
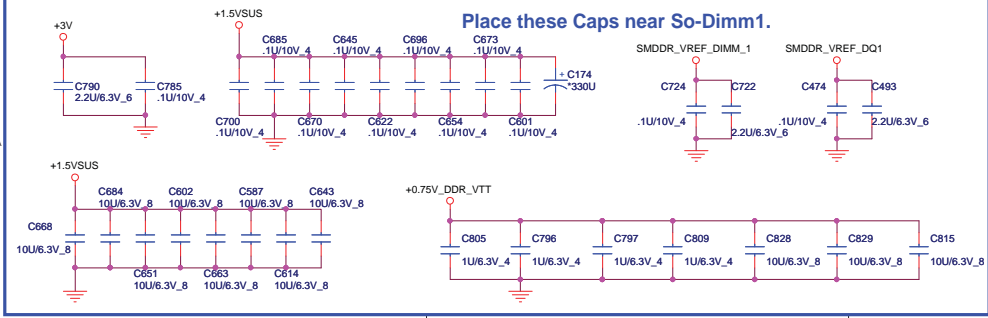
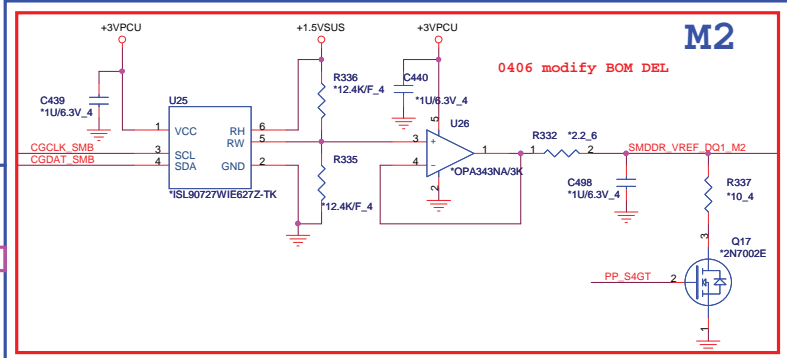
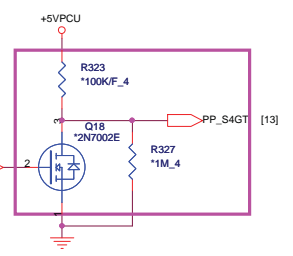
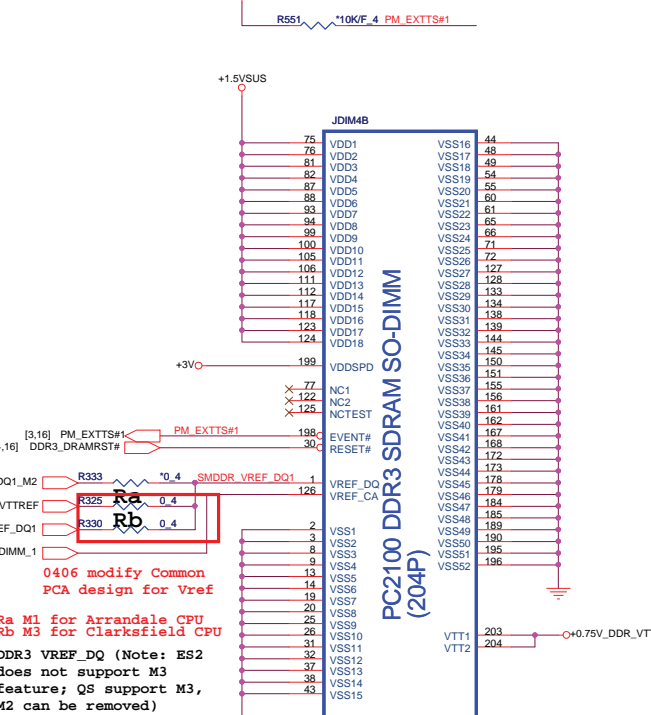
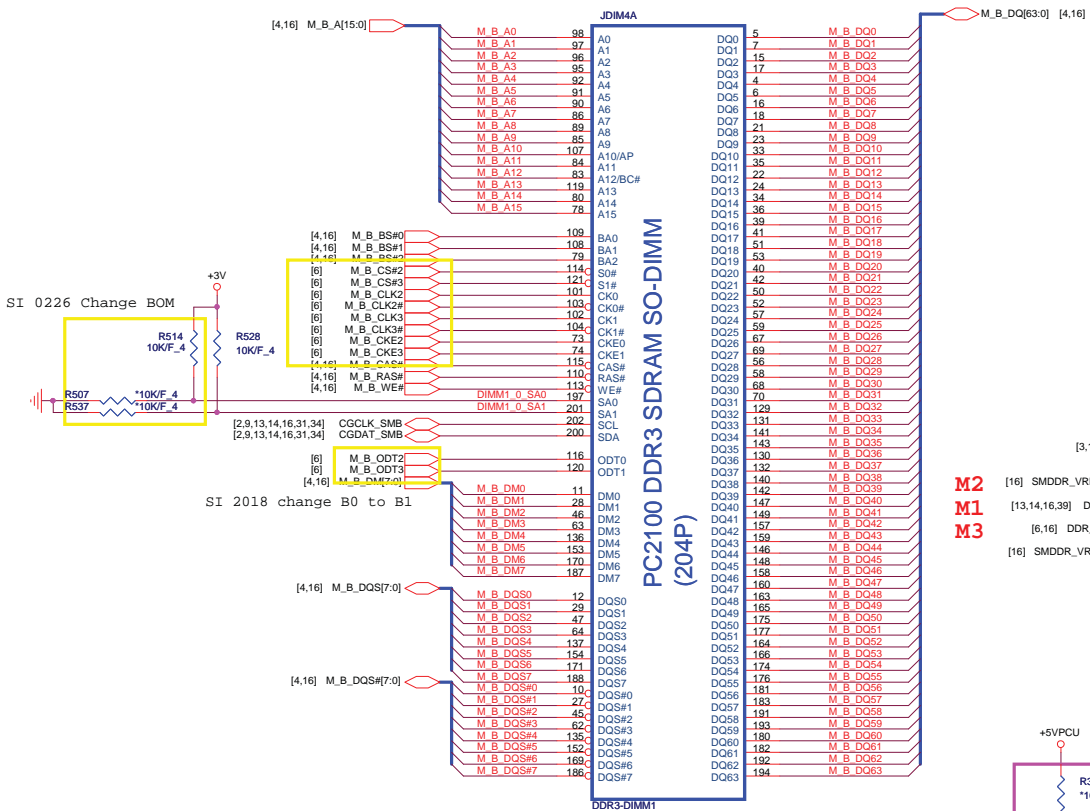
DDR3 -SODIMM 2 A1



PROJECT : SP7
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Size Custom	Document Number DDR3 DIMM-2	Rev 1A
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Sheet 14 of 42		

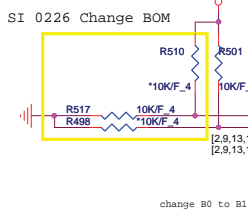
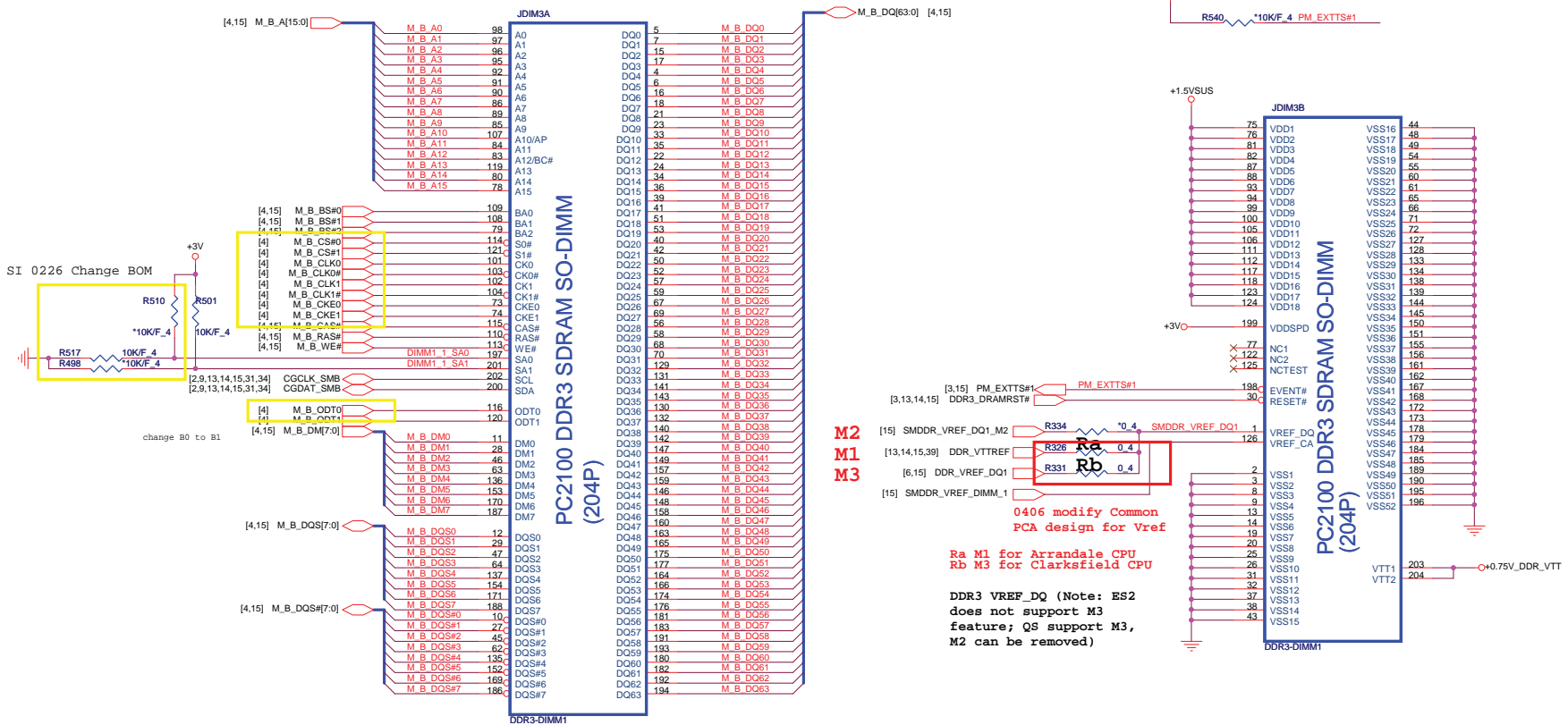
DDR3 -SODIMM 3 B1



PROJECT : SP7
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Size Custom	Document Number	Rev 1A
DDR3 DIMM-3		
Date: Friday, July 10, 2009		

DDR3 -SODIMM 4 B0



M2
M1
M3

[15] SMDR_VREF_DQ1_M2
[13,14,15,39] DDR_VTTREF
[6,15] DDR_VREF_DQ1
[15] SMDR_VREF_DIMM_1

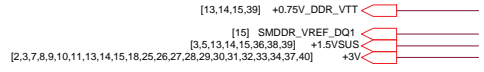
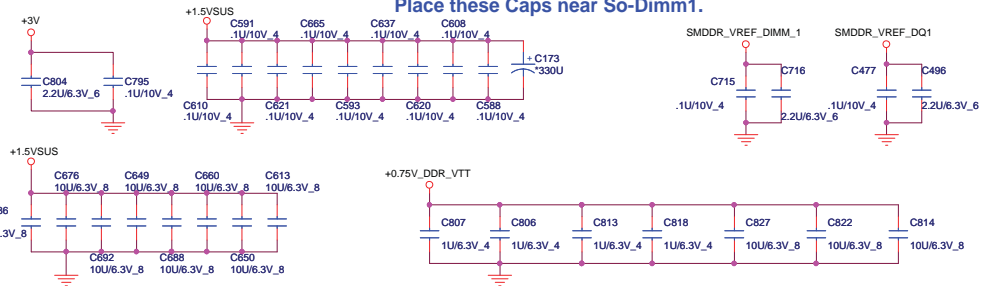
R334 0.4
R326 Ra 0.4
R331 Rb 0.4

0406 modify Common
PCA design for Vref

Ra M1 for Arrandale CPU
Rb M3 for Clarkfield CPU

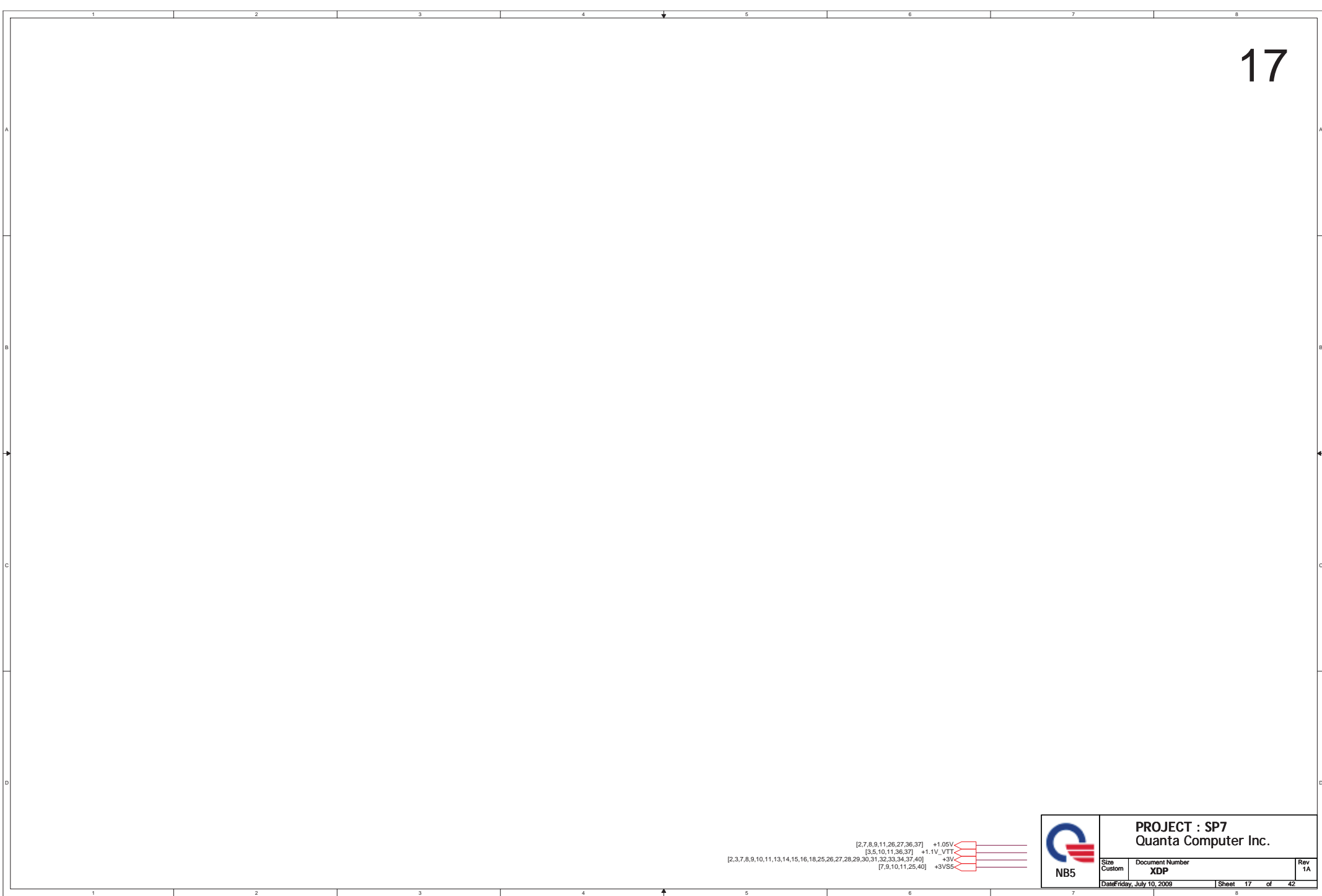
DDR3 VREF DQ (Note: ES2
does not support M3
feature; Q5 support M3,
M2 can be removed)

Place these Caps near So-Dimm1.




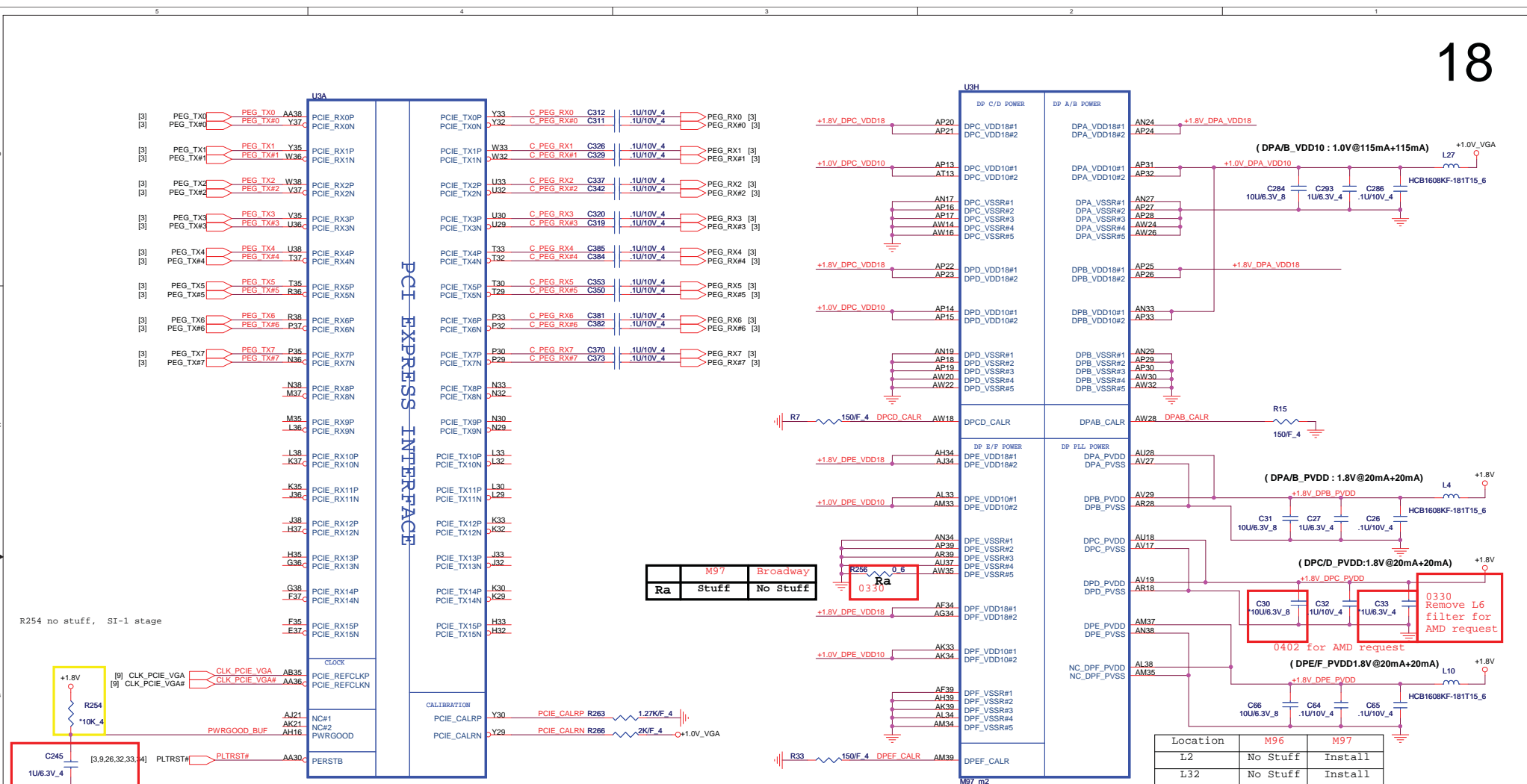
PROJECT : SP7
Quanta Computer Inc.

Size Custom	Document Number DDR3 DIMM-4	Rev 1A
Date: Friday, July 10, 2009 Sheet 16 of 42		

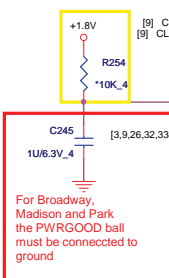


[2,7,8,9,11,26,27,36,37] +1.05V
[3,5,10,11,36,37] +1.1V_VTT
[2,3,7,8,9,10,11,13,14,15,16,18,25,26,27,28,29,30,31,32,33,34,37,40] +3V<
[7,9,10,11,25,40] +3VS5<

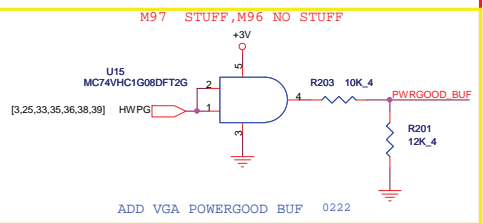
	PROJECT : SP7 Quanta Computer Inc.	
	Size Custom	Document Number XDP
Date Friday, July 10, 2009	Sheet 17 of 42	Rev 1A



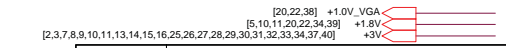
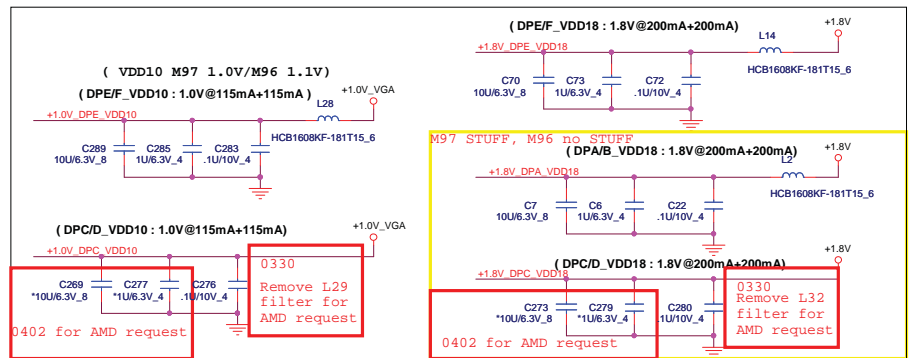
R254 no stuff, SI-1 stage



For M97 ONLY
For future ASIC, PWRGOOD_BUF not required
should be pulled to ground

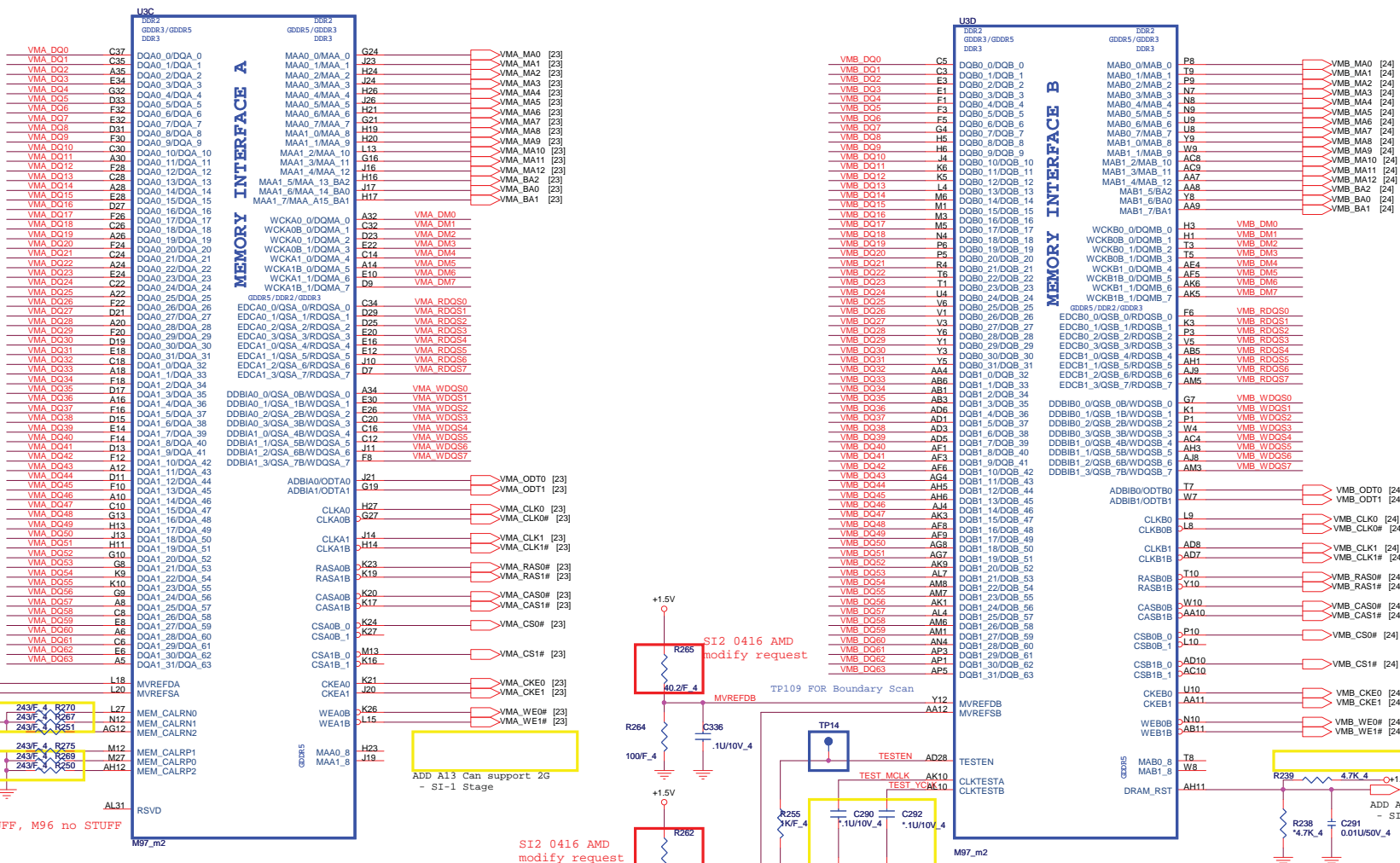


Location	M96	M97
L2	No Stuff	Install
L32	No Stuff	Install
C7	No Stuff	Install
C6	No Stuff	Install
C22	No Stuff	Install
C273	No Stuff	Install
C279	No Stuff	Install
C280	No Stuff	Install
U15	No Stuff	No Stuff
R203	No Stuff	No Stuff
R201	No Stuff	No Stuff
R254	No Stuff	Install
C245	No Stuff	Install



PROJECT : SP7
Quanta Computer Inc.

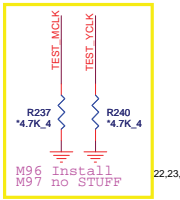
Size	Document Number	Rev
Custom	ATI M97-M2 (PCI E /F) 1/5	1A
Date: Friday, July 10, 2009	Sheet 18 of 42	



Location	M96	M97
R270	No Stuff	Install
R267	No Stuff	Install
R251	No Stuff	Install
R269	No Stuff	Install
R250	No Stuff	Install
R275	Install	Install
R232	No Stuff	No Stuff
R234	No Stuff	No Stuff
C290	No Stuff	No Stuff
C292	No Stuff	No Stuff
R237	Install	No Stuff
R240	Install	No Stuff

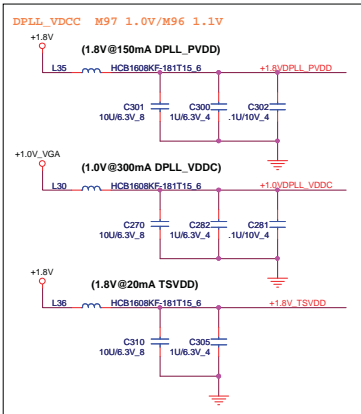
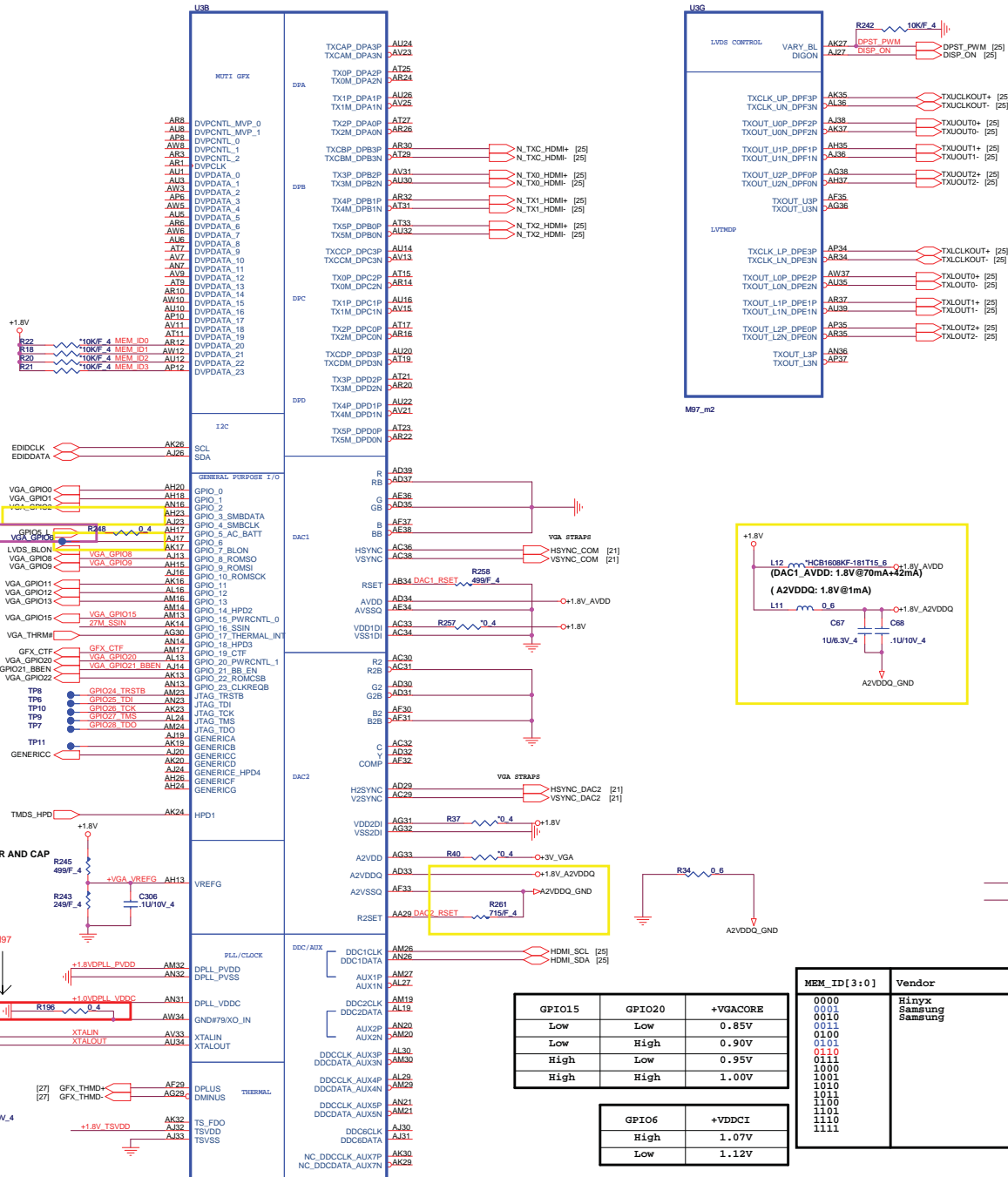
- [23] VMA_DQ[63..0]
- [23] VMA_DM[7..0]
- [23] VMA_WDQS[7..0]
- [23] VMA_RDQS[7..0]

- [24] VMB_DQ[63..0]
- [24] VMB_DM[7..0]
- [24] VMB_WDQS[7..0]
- [24] VMB_RDQS[7..0]



PROJECT : SP7
Quanta Computer Inc.

Size Custom	Document Number ATI M97-M2 (MEM I/F) 2/5	Rev 1A
Date: Friday, July 10, 2009	Sheet 19 of 42	



Delete SMB_CLK_MBI1 / SMB_DATA_MBI1 =>SI-1 Stage
ADD VDDCI Control Pin - SI-1 Stage

PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC

S12 modify Q326 For Broadway, Madison and Park

GPIO15	GPIO20	+VGACORE
Low	Low	0.85V
Low	High	0.90V
High	Low	0.95V
High	High	1.00V

GPIO6	+VDDCI
High	1.07V
Low	1.12V

MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Hynix	64*16-800MHZ	H5TQ1G63BFR-12C
0001	Samsung	64*16-800MHZ	K4W1G1646E-HC12
0010	Samsung	64*16-800MHZ	K4W1G1646E-HC12
0101	Reserved	Reserved	Reserved
0100	Reserved	Reserved	Reserved
0101	Reserved	Reserved	Reserved
1000	Reserved	Reserved	Reserved
1001	Reserved	Reserved	Reserved
1010	Reserved	Reserved	Reserved
1011	Reserved	Reserved	Reserved
1100	Reserved	Reserved	Reserved
1101	Reserved	Reserved	Reserved
1110	Reserved	Reserved	Reserved
1111	Reserved	Reserved	Reserved

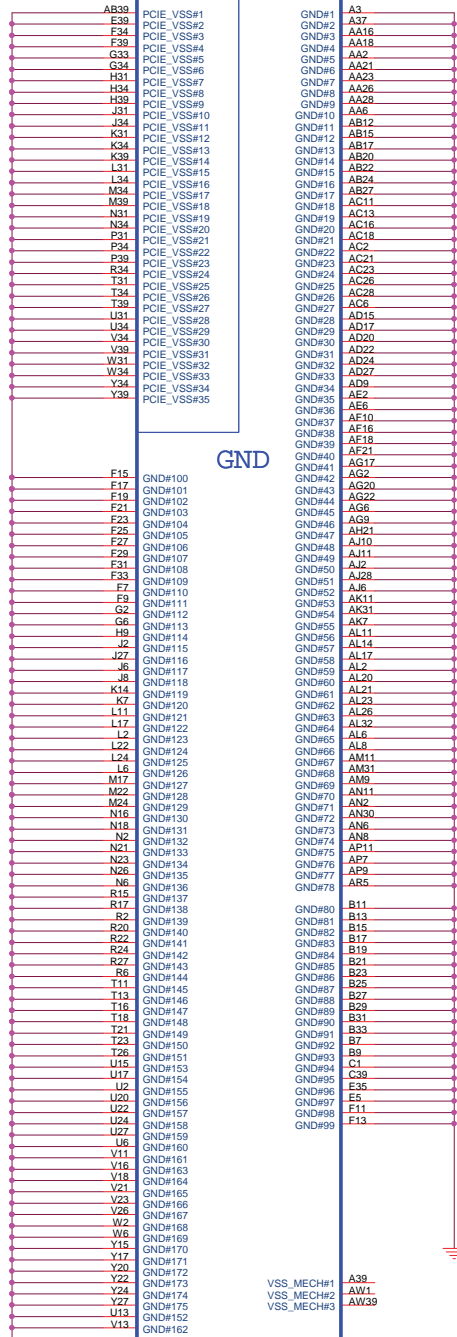
PROJECT : SP7
Quanta Computer Inc.

Size Custom Document Number **ATI M97-M2 (DISPLAY) 3/5** Rev 1A

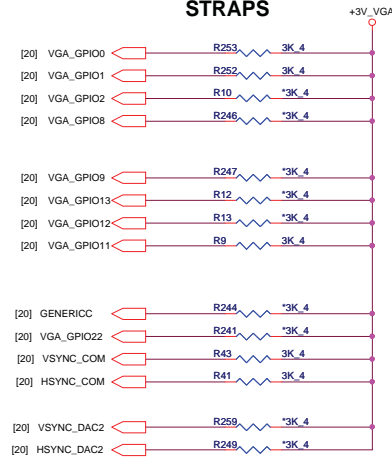
Date: Friday, July 10, 2009 1 Sheet 20 of 42



USF

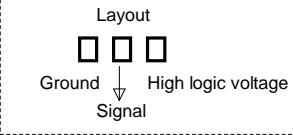


STRAPS



Location	M96	M97
pull-up for straps	10K (CS31002FB26)	3K (CS23002FB11)

Overlap pads to save space and to prevent assembly of both resistors.

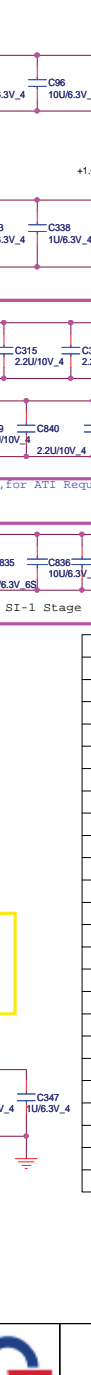
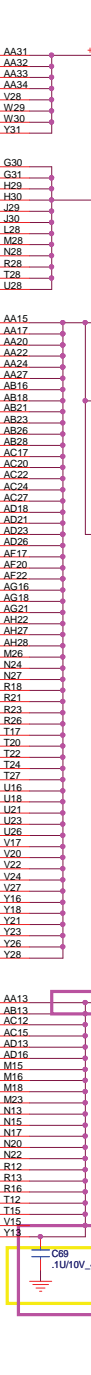
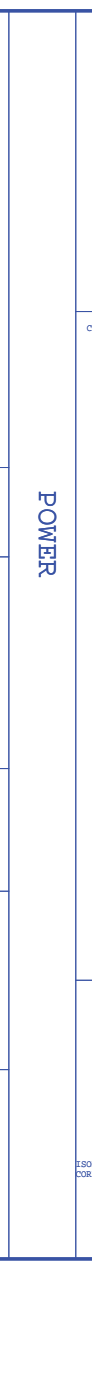
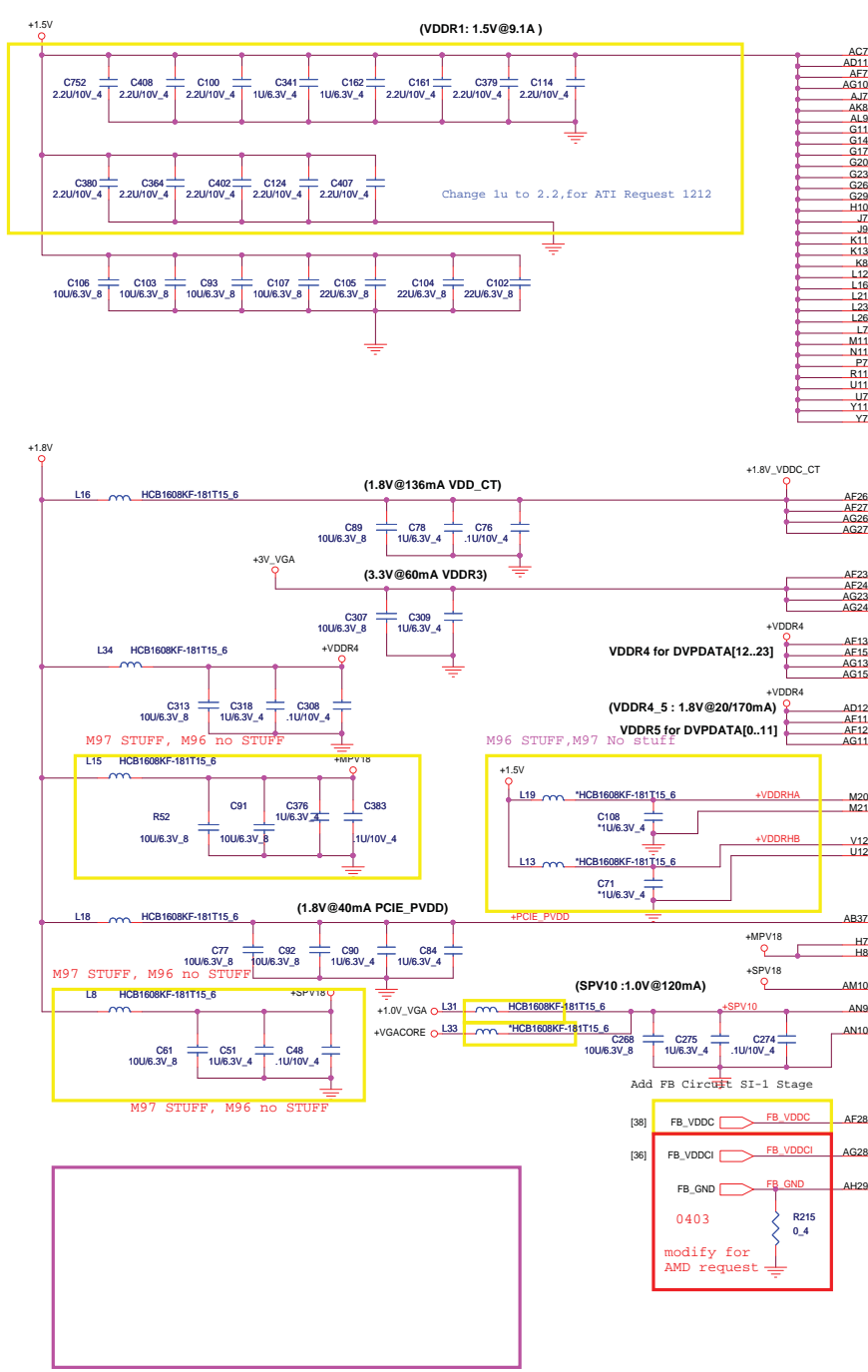


Strap Name	Pin	Straps description	Default Value
TX_PWR5_ENB	GPI00	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: Full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPI01	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN	GPI02	0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on. 1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on. 5.0 GT/s capability will be controlled by software.	1
STRAP_BIF_CLK_PM_EN	GPI08	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
CONFIG[3]	GPI09	GPI09,13,12,11 (config 3.2.1.0): a- If BIOS_ROM_EN = 1, then Config[3] defines the ROM Type: b- If BIOS_ROM_EN = 0, then Config[3] defines the Aperture size: Size of the primary memory apertures claimed in PCI configuration space 000 = 128MB 001 = 256MB 010 = 64MB 011 = 32MB 100 = 512MB 101 = 1GB 110 = 2GB 111 = 4GB	0001
CONFIG[2]	GPI013		
CONFIG[1]	GPI012		
CONFIG[0]	GPI011		
BIOS_ROM_EN	GPI022	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	0
AUDIO[0]	VSYNC		0
AUD(1)	HSYNC	HSYNC - HDMI_EN HDMI connector presence. 0 ?No HDMI connector is present on PCB 1 - HDMI connector is present on the PCB HDMI	1
VSYNC_DAC2	V2SYNC	If VIP_DEVICE_STRAP_EN is set to ?? then this pin is used to sense whether a VIP slave device is connected to the VIP Host interface. If VIP_DEVICE_STRAP_EN is set to ?? then this pin is not used as a strap at all (i.e. its value during reset is unimportant), and it can be used as a regular GPIO	0
HSYNC_DAC2	H2SYNC		0
GENERICC			0

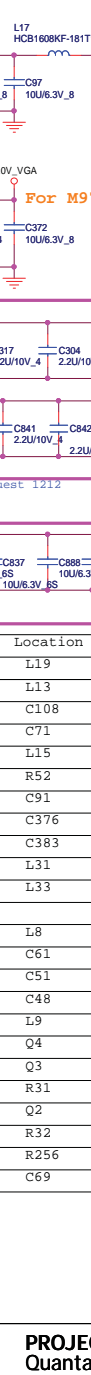
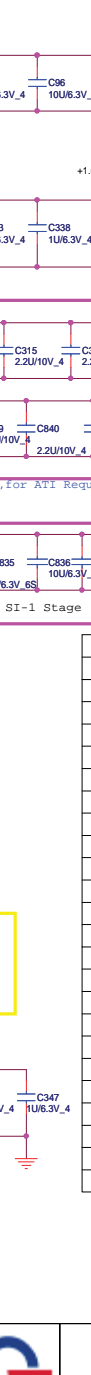
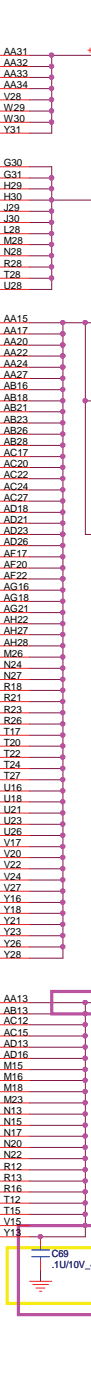


PROJECT : SP7
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
	ATI M97(GND&Str&Ther)4/5	
Date: Friday, July 10, 2009	Sheet 21	of 42



POWER



Location	M96	M97
L19	Install	No Stuff
L13	Install	No Stuff
C108	Install	No Stuff
C71	Install	No Stuff
L15	No Stuff	Install
R52	No Stuff	Install
C91	No Stuff	Install
C376	No Stuff	Install
C383	No Stuff	Install
L31	No Stuff	Install
L33	Install	No Stuff
L8	No Stuff	Install
C61	No Stuff	Install
C51	No Stuff	Install
C48	No Stuff	Install
L9	No Stuff	Install
Q4	Install	No Stuff
Q3	Install	No Stuff
R31	Install	No Stuff
Q2	Install	No Stuff
R32	Install	No Stuff
R256	Install	No Stuff
C69	Install	No Stuff

Change power Netname to +VDDCI (SI-1 Stage)
(For MP7, 1.12V@4A VDDCI).



- [18,20,38] +1.0V_VGA
- [8] +VGACORE
- [19,23,24,34,36,40] +1.5V
- [5,10,11,18,20,34,39] +1.8V
- [20,21,25,40] +3V_VGA

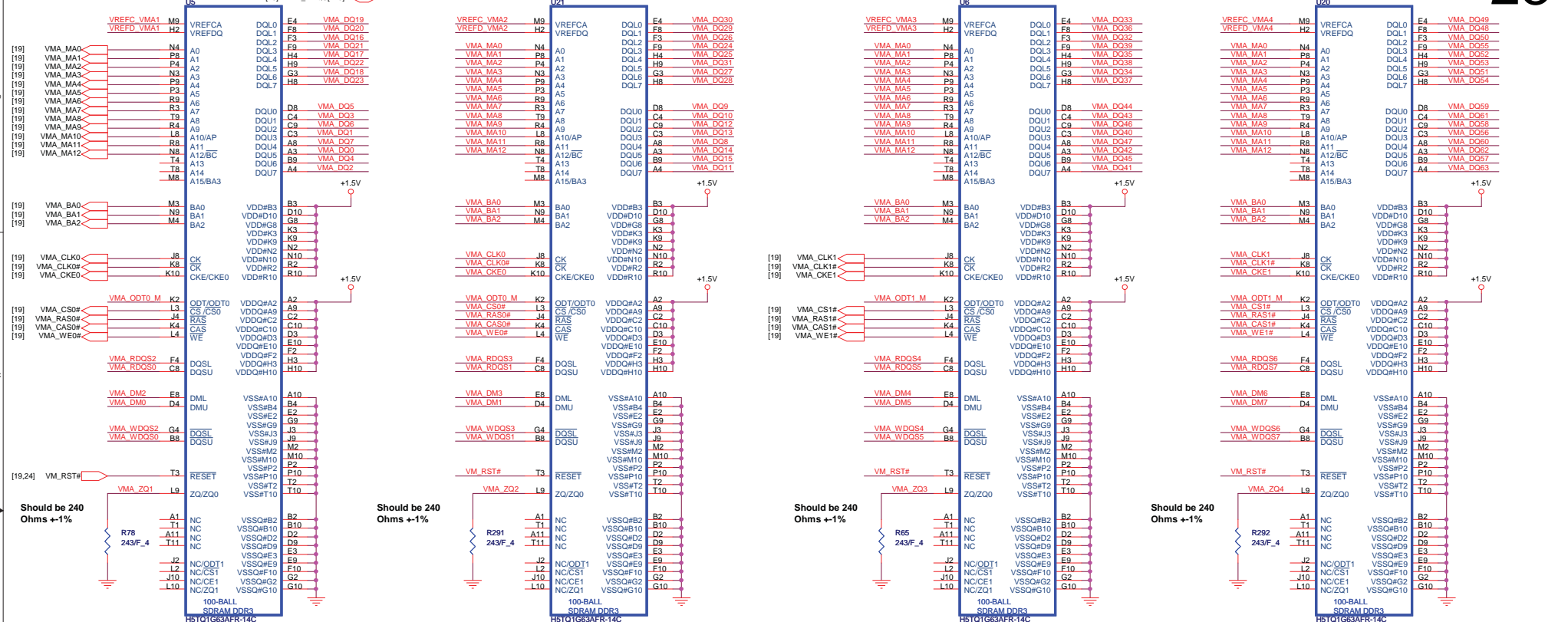


PROJECT : SP7
Quanta Computer Inc.

Size Custom Document Number **ATI M97-M2 (POWER) 5/5** Rev 1A
Date: Friday, July 10, 2009 Sheet 22 of 42

CHANNEL A: 256MB/512MB DDR3

[19] VMA_DQ[63..0]
 [19] VMA_DM[7..0]
 [19] VMA_WDQS[7..0]
 [19] VMA_RDQS[7..0]

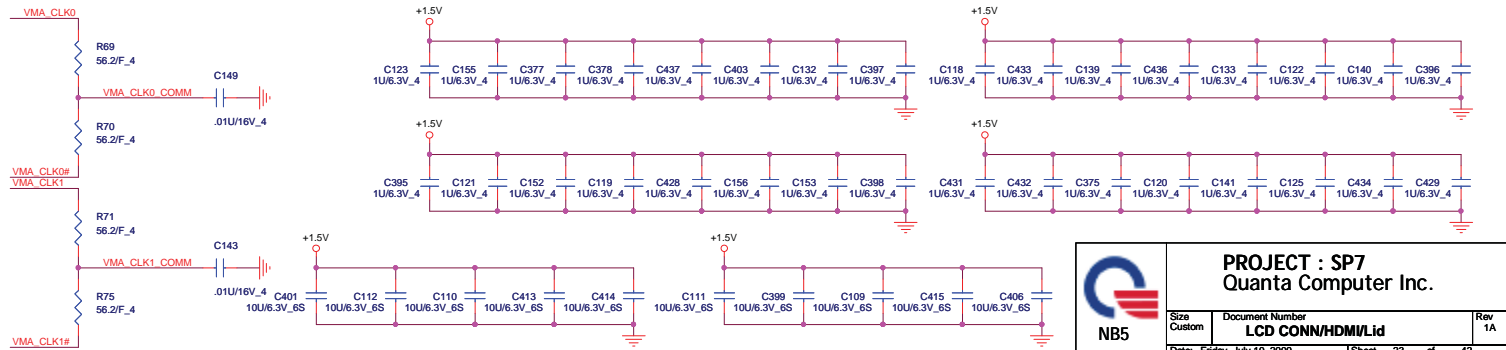
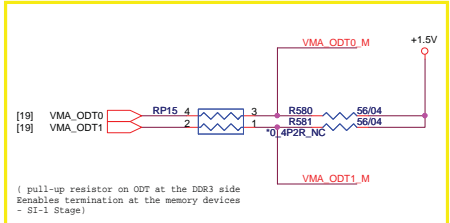


Should be 240 Ohms +/-1%

Should be 240 Ohms +/-1%

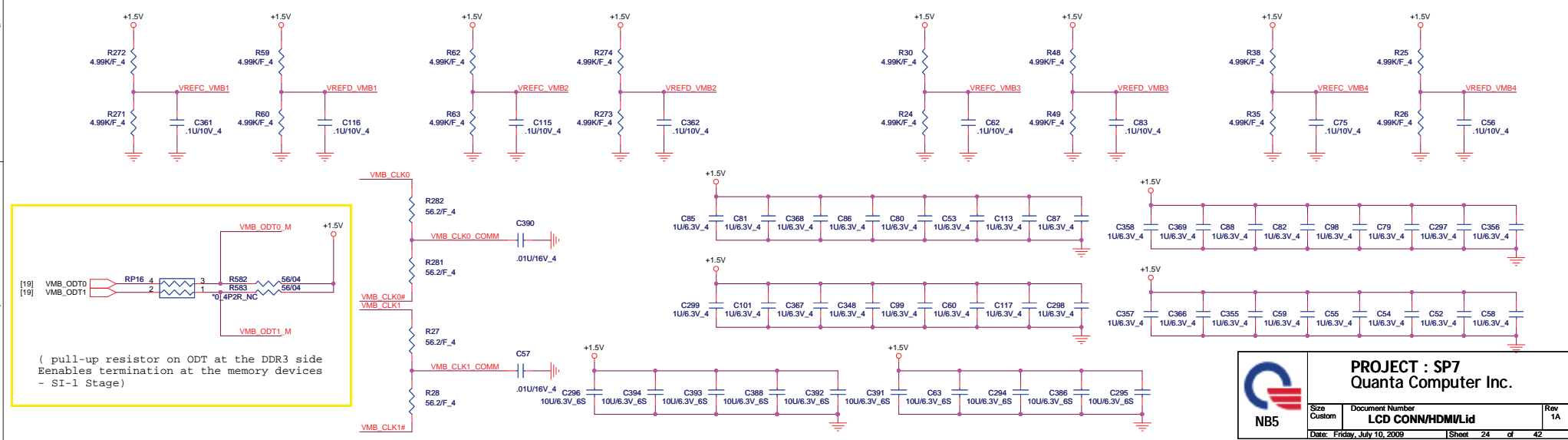
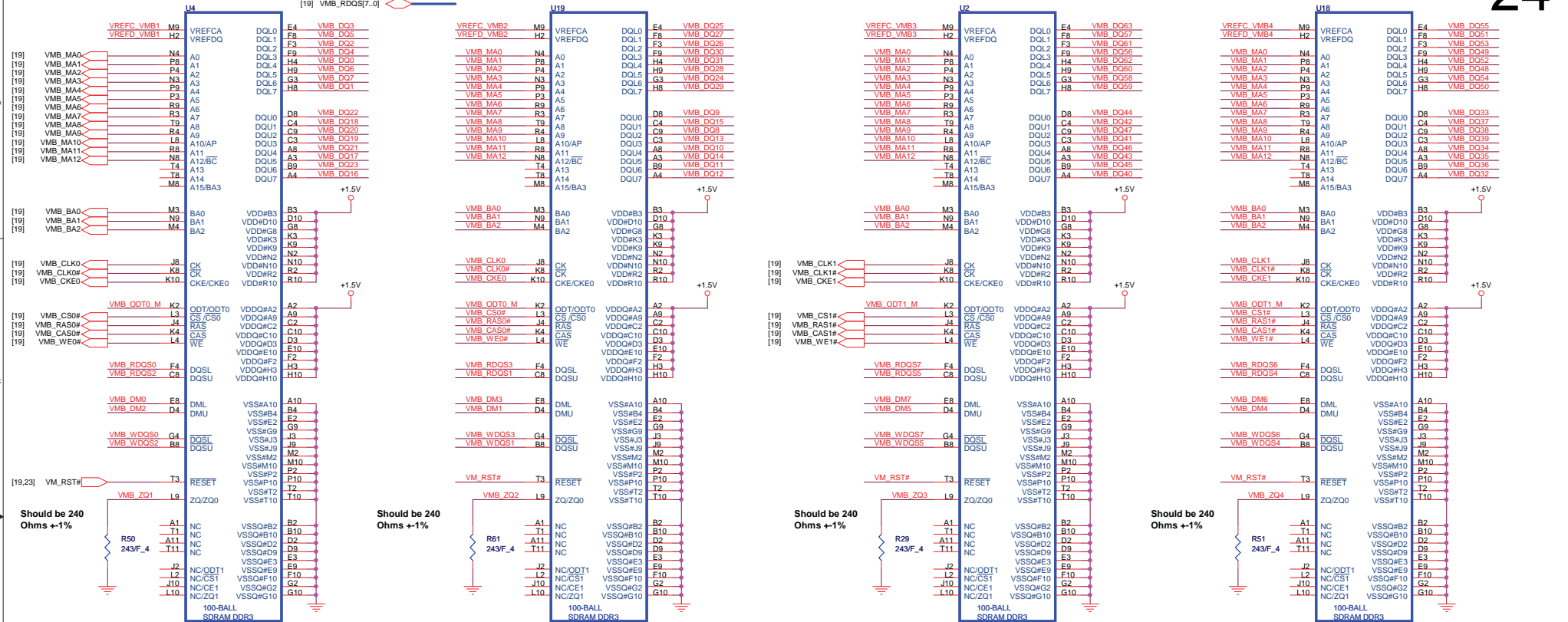
Should be 240 Ohms +/-1%

Should be 240 Ohms +/-1%



CHANNEL B: 256MB/512MB DDR3

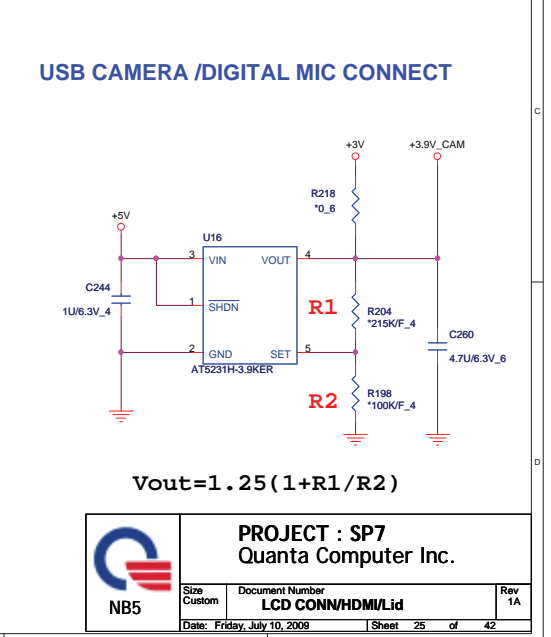
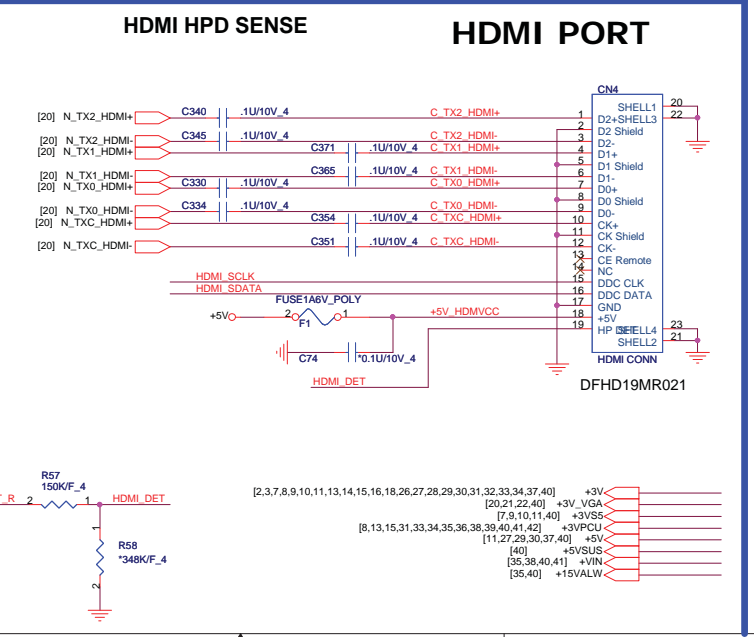
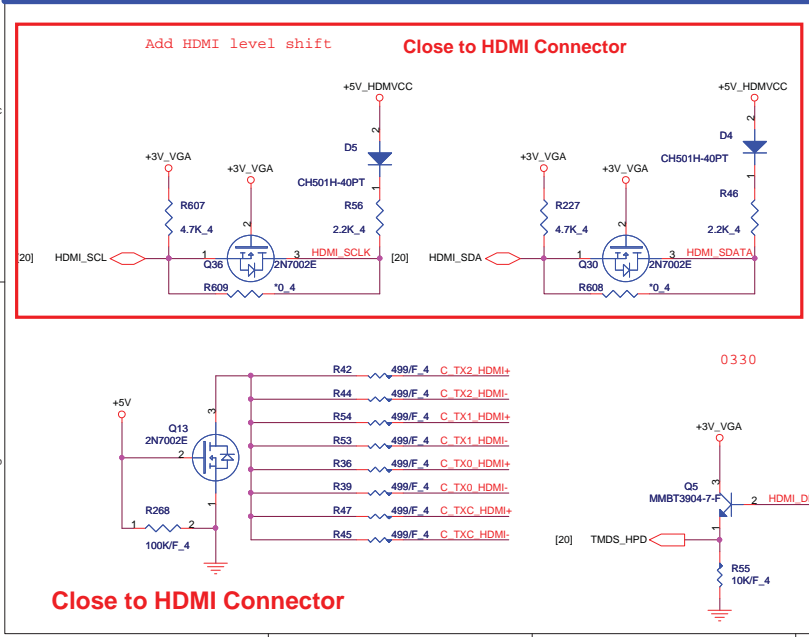
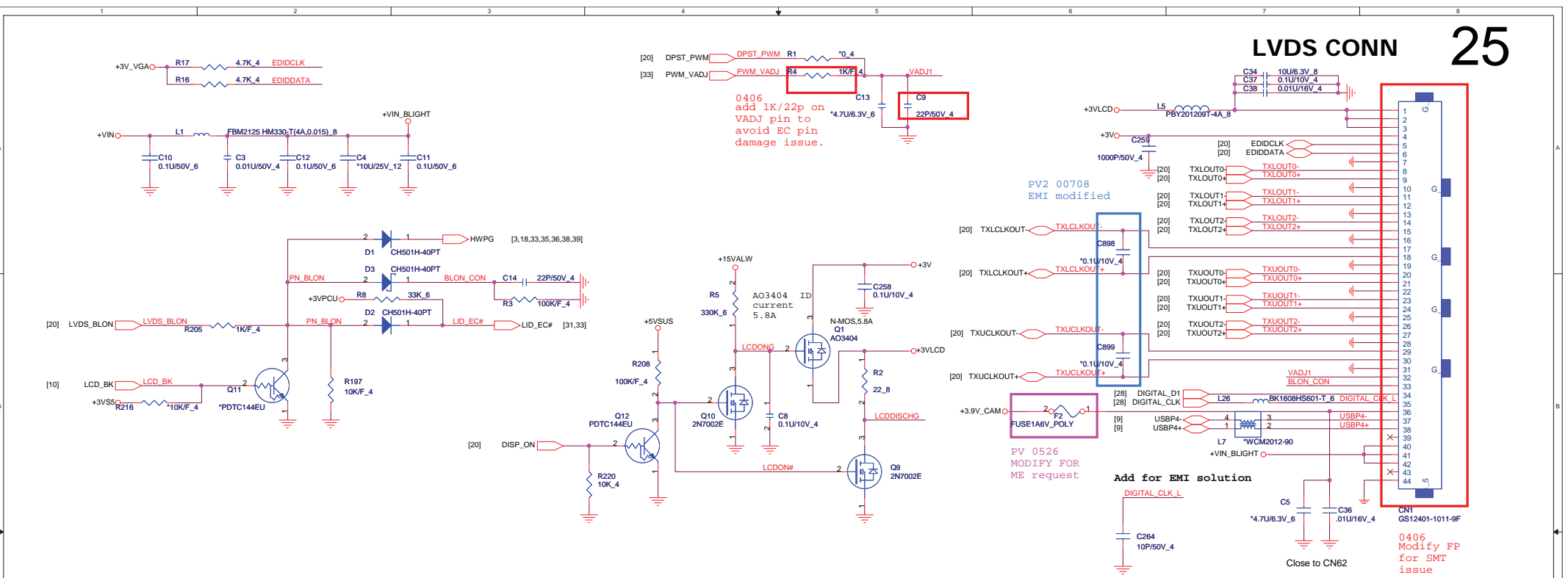
- [19] VMB_DQ[63..0]
- [19] VMB_DM[7..0]
- [19] VMB_WDQS[7..0]
- [19] VMB_RDQS[7..0]



(pull-up resistor on ODT at the DDR3 side Enables termination at the memory devices - SI-1 Stage)

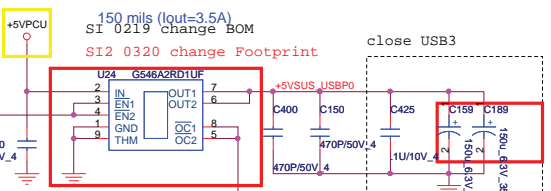
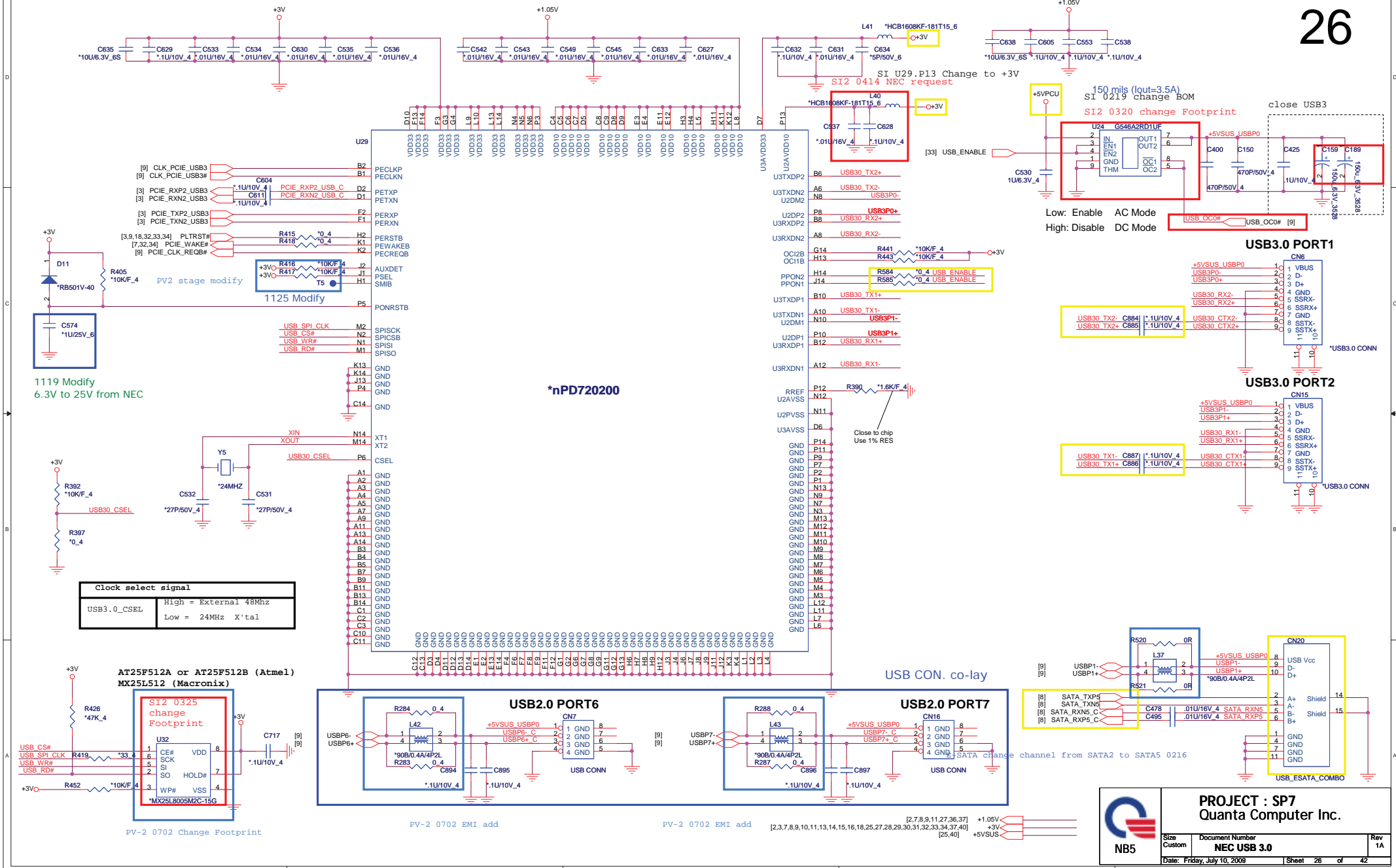
PROJECT : SP7
Quanta Computer Inc.

Size Custom	Document Number LCD CONN/HDMI/Lid	Rev 1A
Date: Friday, July 10, 2009	Sheet 24 of 42	

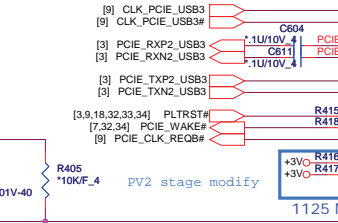
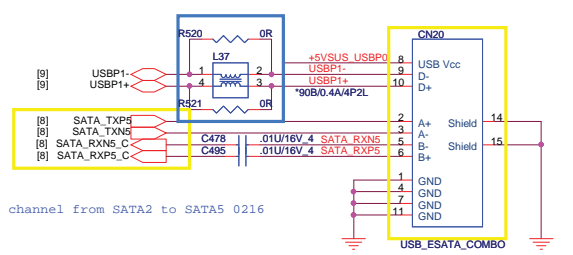
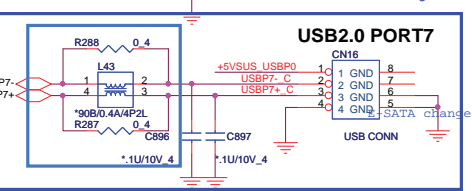
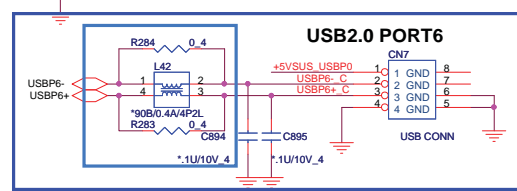
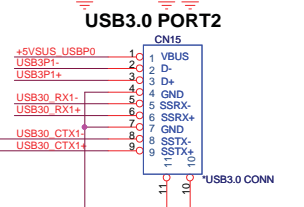
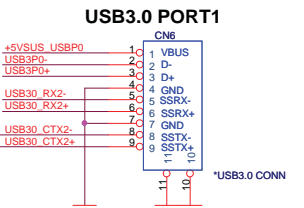


USB3.0 X 2 and E-SATA/USB2.0 COMBO

26



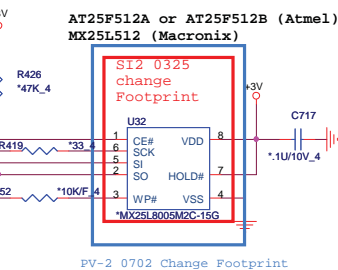
Low: Enable AC Mode
High: Disable DC Mode



1119 Modify
6.3V to 25V from NEC

Clock select signal

USB3.0_CSEL	High = External 48MHz
	Low = 24MHz X'tal

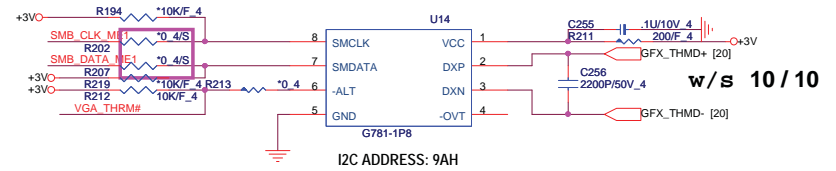
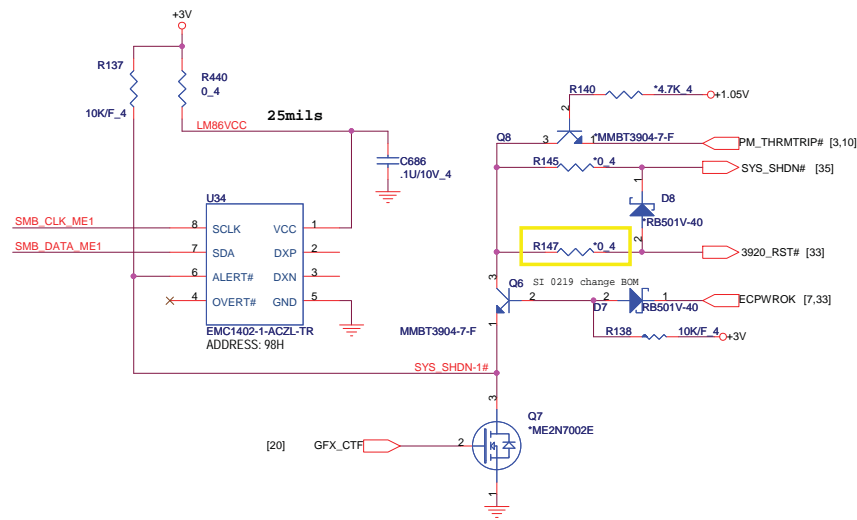


PROJECT : SP7
Quanta Computer Inc.

Size Custom	Document Number NEC USB 3.0	Rev 1A
Date: Friday, July 10, 2009		Sheet 26 of 42

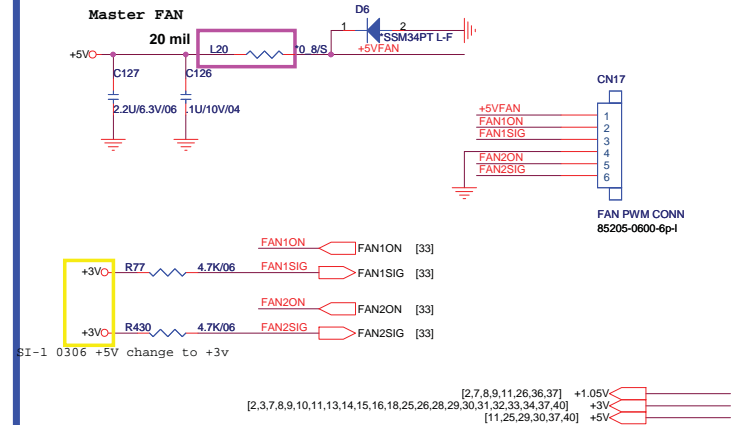
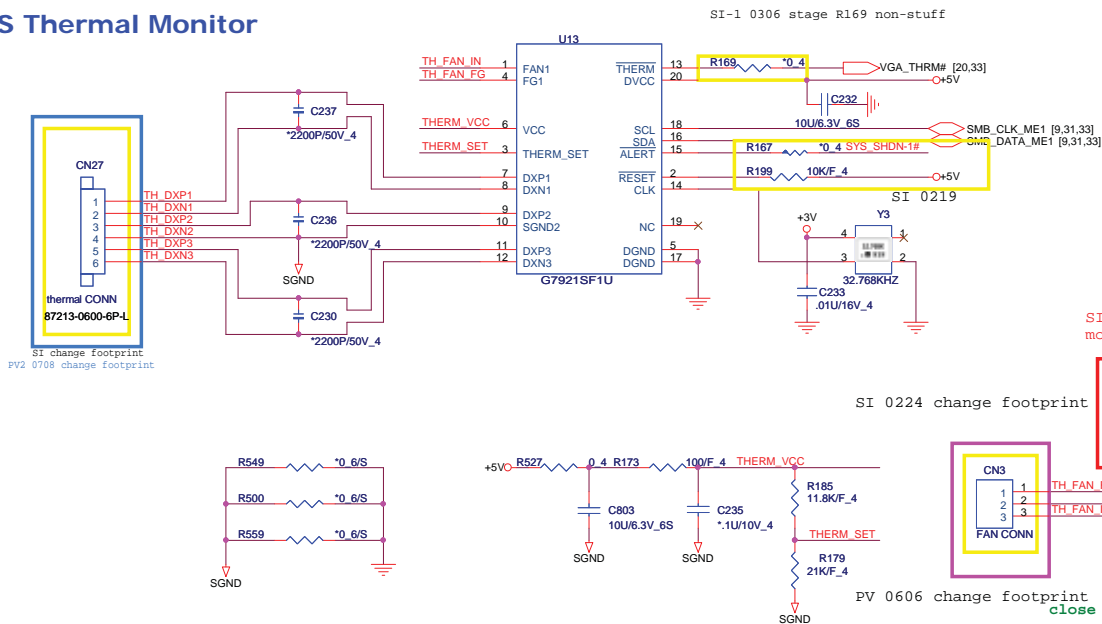
CPU THERMAL MONITOR

GPU Thermal Sensor

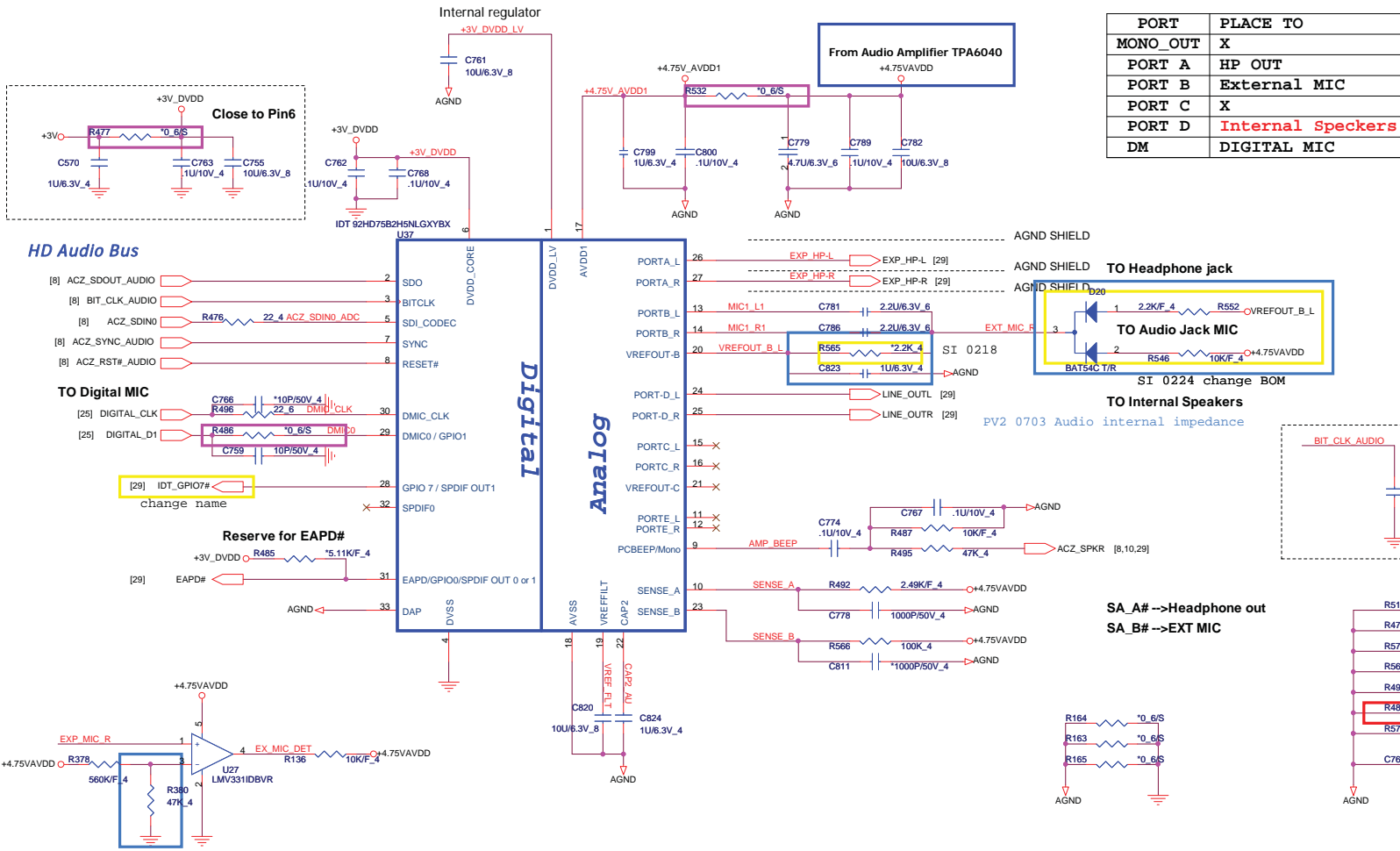


SYS Thermal Monitor

CPU FAN1/2 CONN
RPM Control

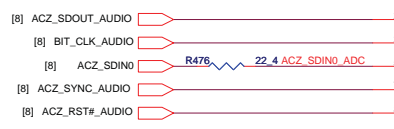


	PROJECT : SP7 Quanta Computer Inc.		
	Size Custom	Document Number CPU/GA/SYSTEM THERMAL	Rev 1A
	Date: Friday, July 10, 2009 Sheet 27 of 42		

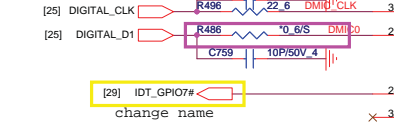


PORT	PLACE TO
MONO_OUT	X
PORT A	HP OUT
PORT B	External MIC
PORT C	X
PORT D	Internal Speakers
DM	DIGITAL MIC

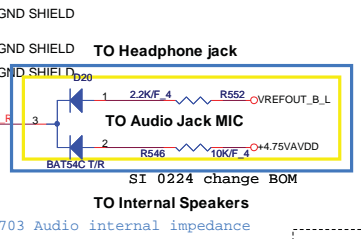
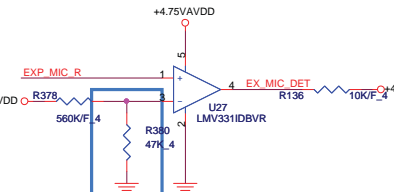
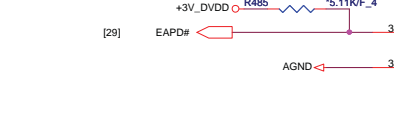
HD Audio Bus



TO Digital MIC

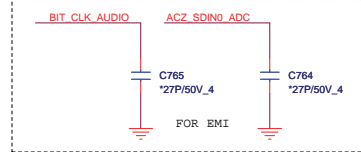


Reserve for EAPD#

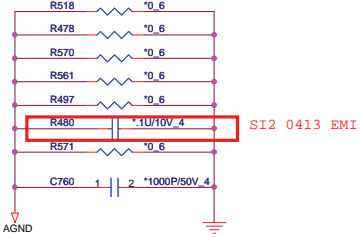
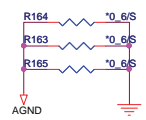


TO Internal Speakers

PV2 0703 Audio internal impedance



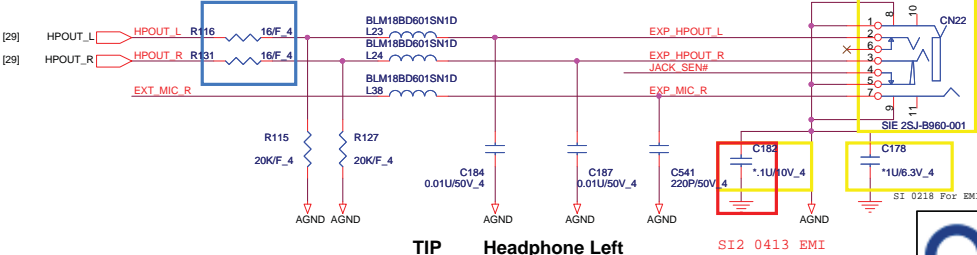
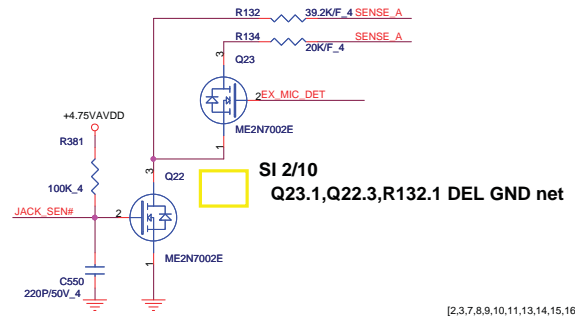
SA_A# --> Headphone out
SA_B# --> EXT MIC



Combo Jack (Headphone/MIC)

Normal Close

SI 0227 Change footprint



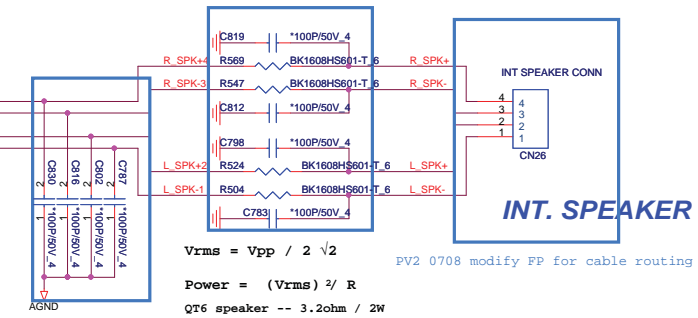
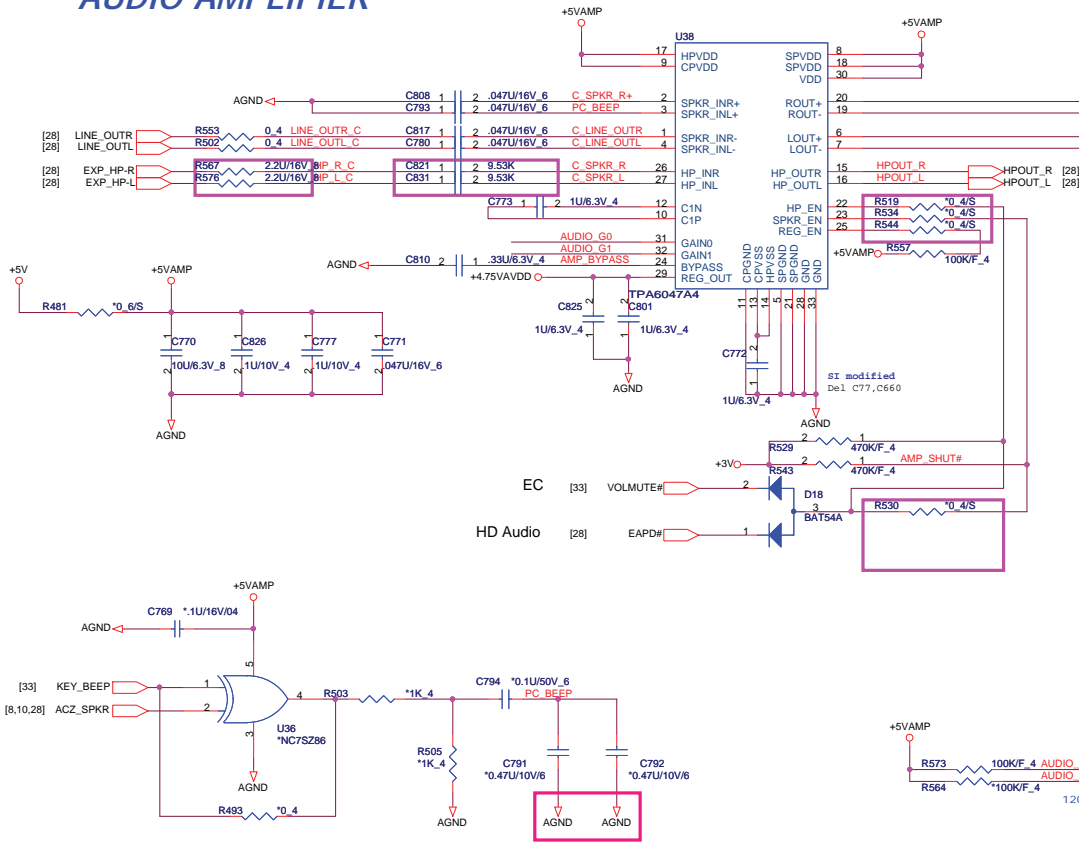
SI 2/10
CN22.8, CN22.9 connect to AGND

TIP Headphone Left
R1 Headphone Right
R2 GND
BASE MIC

SI2 0413 EMI

	PROJECT : SP7		Rev 1A
	Quanta Computer Inc.		
	Size Custom Document Number Azalia 92HD75	Date: Friday, July 10, 2009	

AUDIO AMPLIFIER



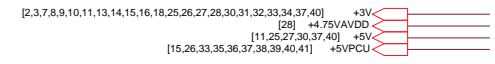
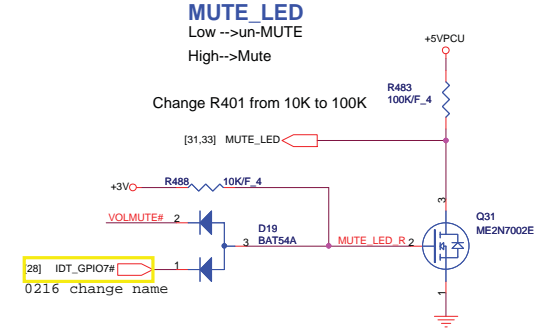
$V_{rms} = V_{pp} / 2 \sqrt{2}$
 $Power = (V_{rms})^2 / R$
 QT6 speaker -- 3.2ohm / 2W

PIN23 SPKR_EN

TPA6040A4	Low enable
TPA6047A4	High enable

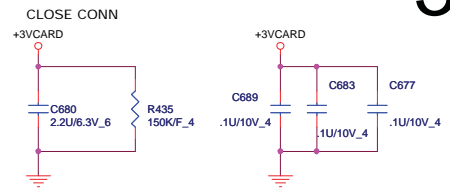
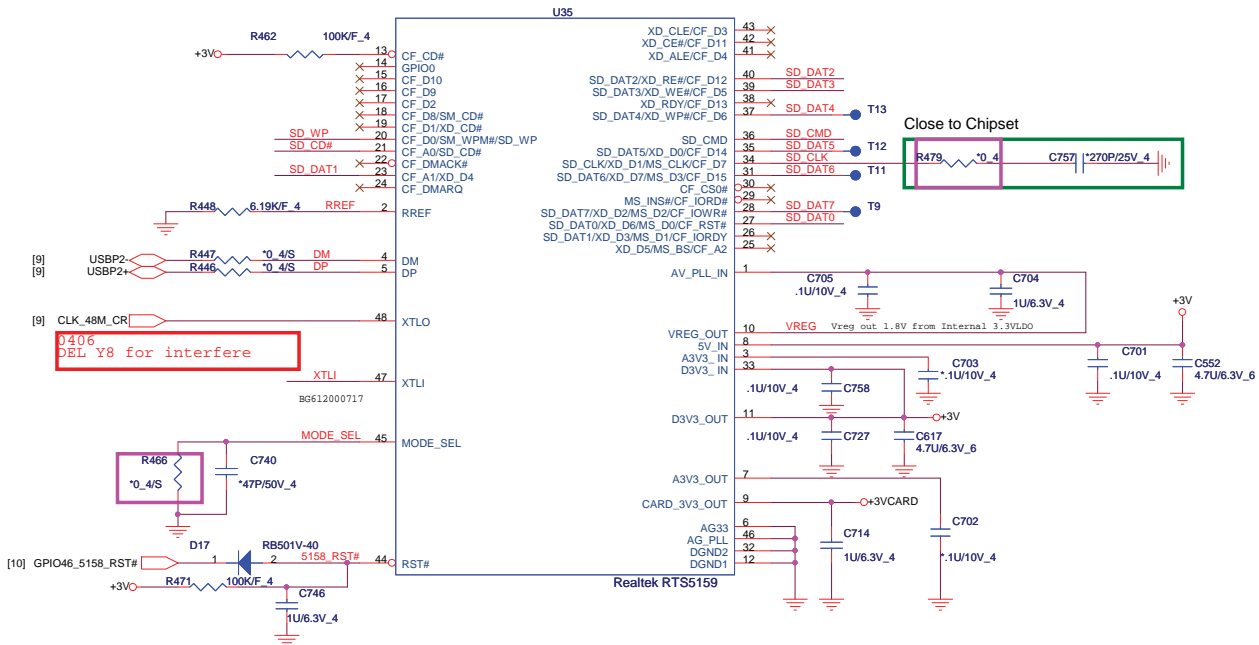
6047A2 Gain Table

GAIN0	GAIN1	AV	RIN
0	0	6dB	90K
0	1	10dB	70K
1	0	15.6dB	45K
1	1	21.6dB	25K

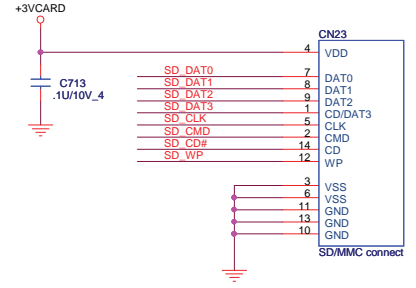


PROJECT : SP7
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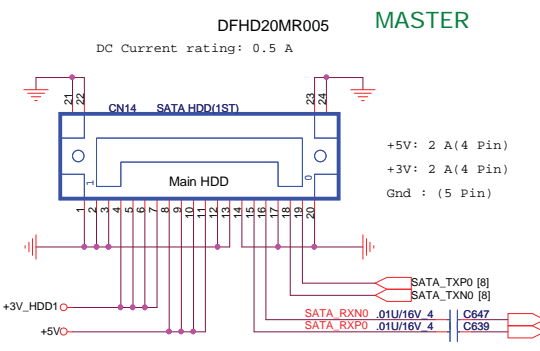
Size Custom	Document Number AMP_TPA6047	Rev 1A
Date: Friday, July 10, 2009		Sheet 29 of 42



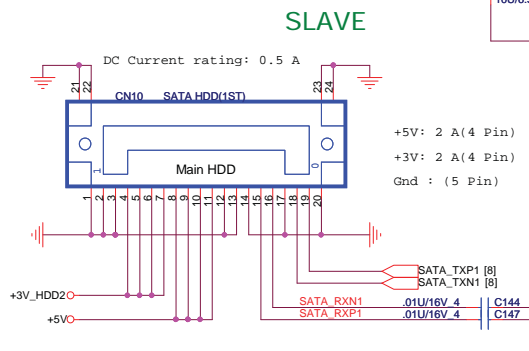
2 IN1 CARD READER SD/MMC



SATA 1.8"/2.5" HDD CONNECTOR MASTER



SSD(1) 1.8" CONNECTOR SLAVE



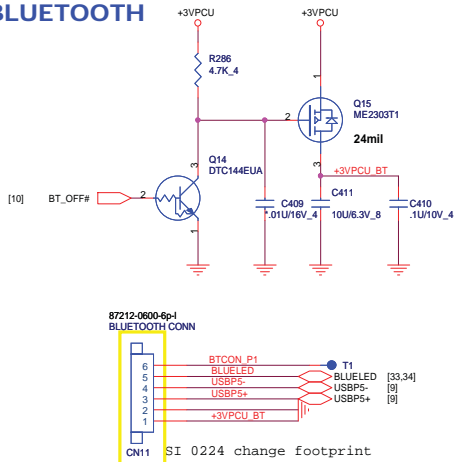
[2,3,7,8,9,10,11,13,14,15,16,18,25,26,27,28,29,31,32,33,34,37,40] +3V
 [11,25,27,29,37,40] +5V

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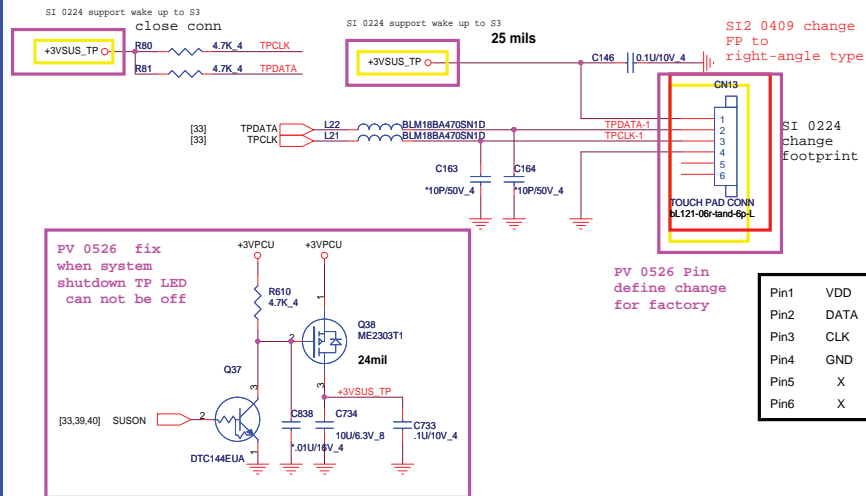
NBS

Size Custom	Document Number RTS5159 & CR SOCKET	Rev 1A
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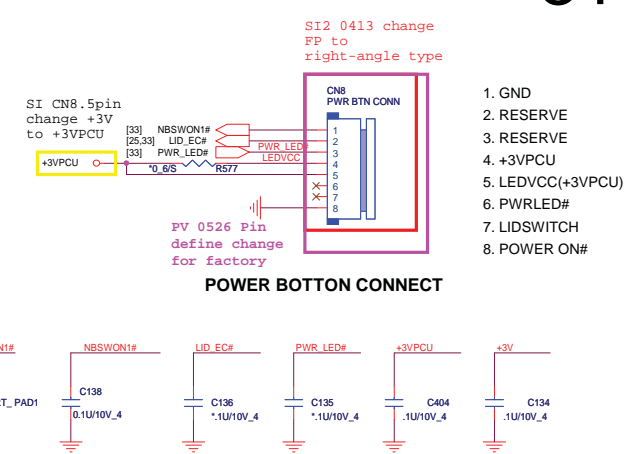
BLUETOOTH



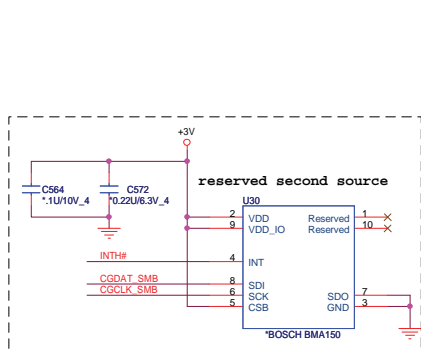
TOUCH PAD CONNECTOR



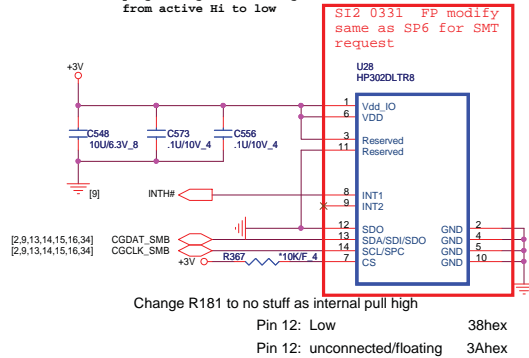
Power Button



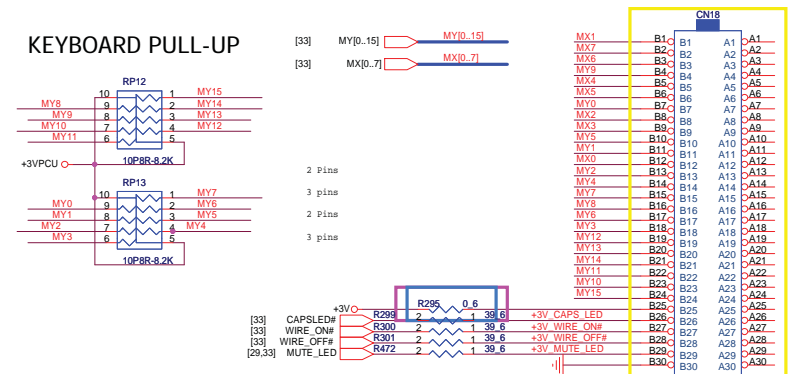
Accelerometer Sensor



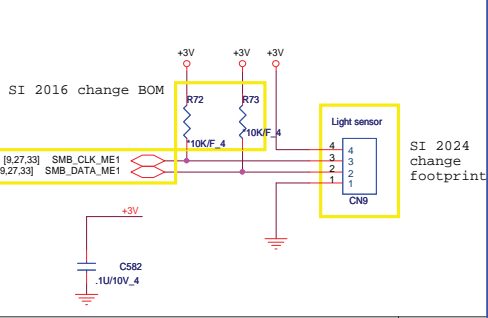
SGT-LI6302DLTR interrupt pin default is low / active Hi , BIOS need to programming 22h to change status from active Hi to low



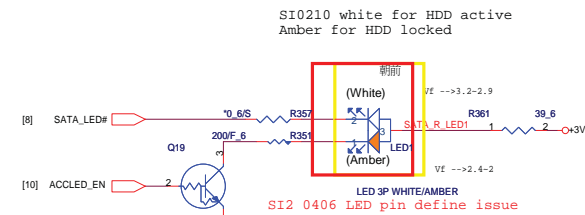
Key Board CONN



Ambient Light Sensor



LED

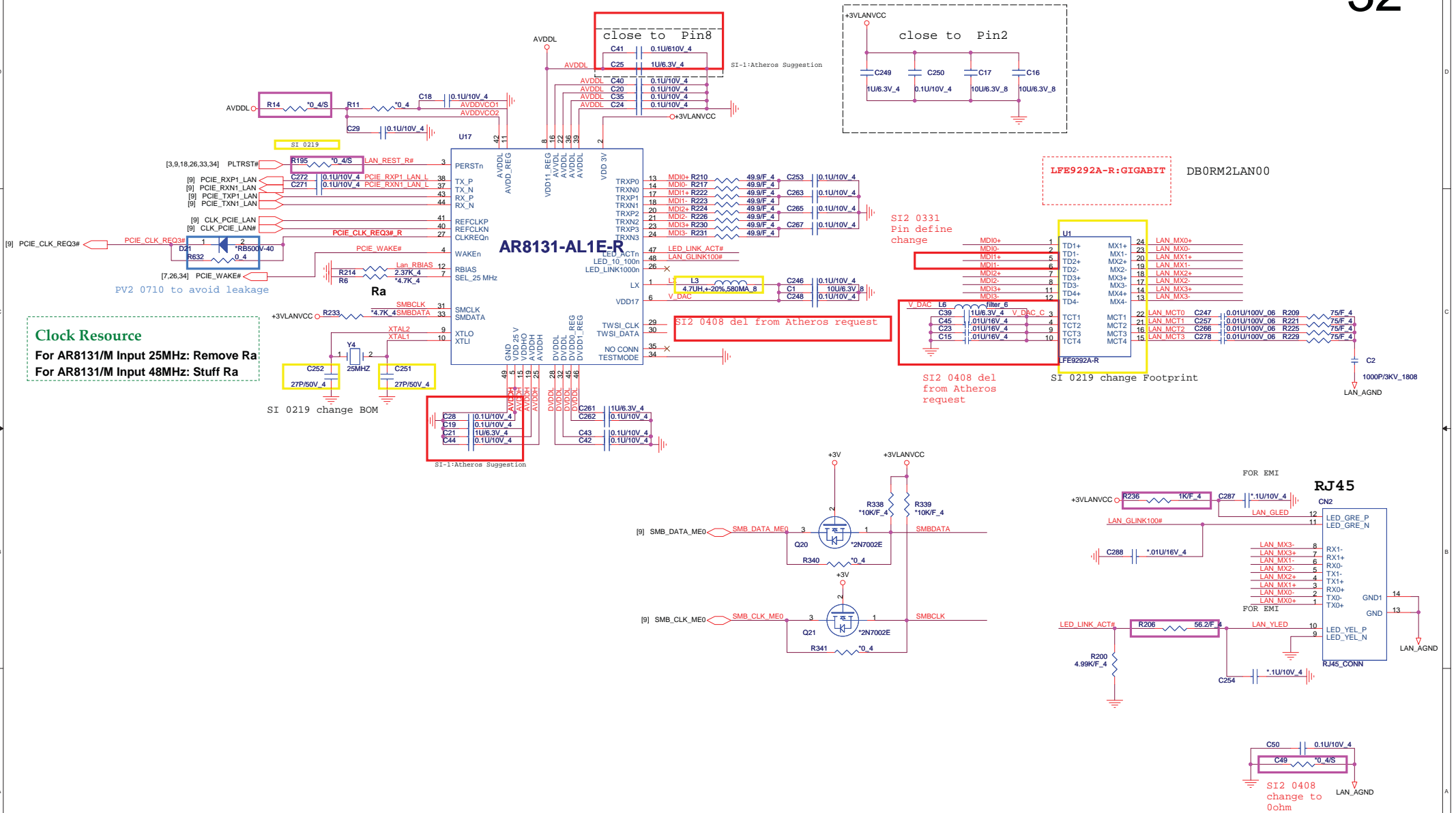


[2,3,7,8,9,10,11,13,14,15,16,18,25,26,27,28,29,30,32,33,34,37,40] [8,13,15,25,33,34,35,36,38,39,40,41,42]

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Quanta Computer Inc.

NB5	Size Custom	Document Number	Rev 1A
	Date: Friday, July 10, 2009	BT/TP/PW BN/Key CON/Acc/LED/LAS	

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Clock Resource
For AR8131/M Input 25MHz: Remove Ra
For AR8131/M Input 48MHz: Stuff Ra

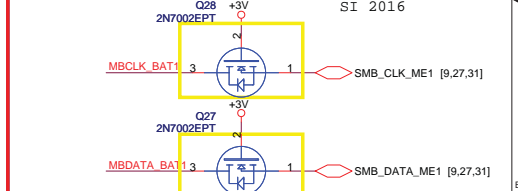
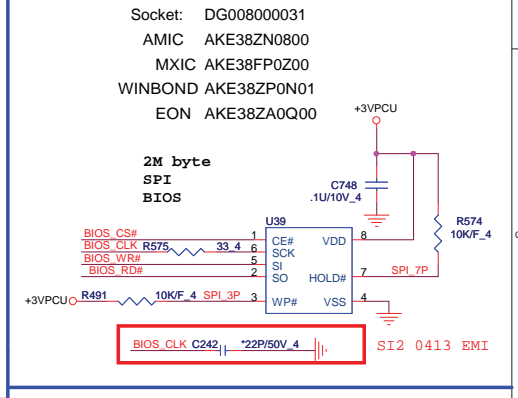
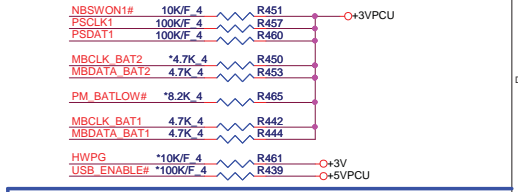
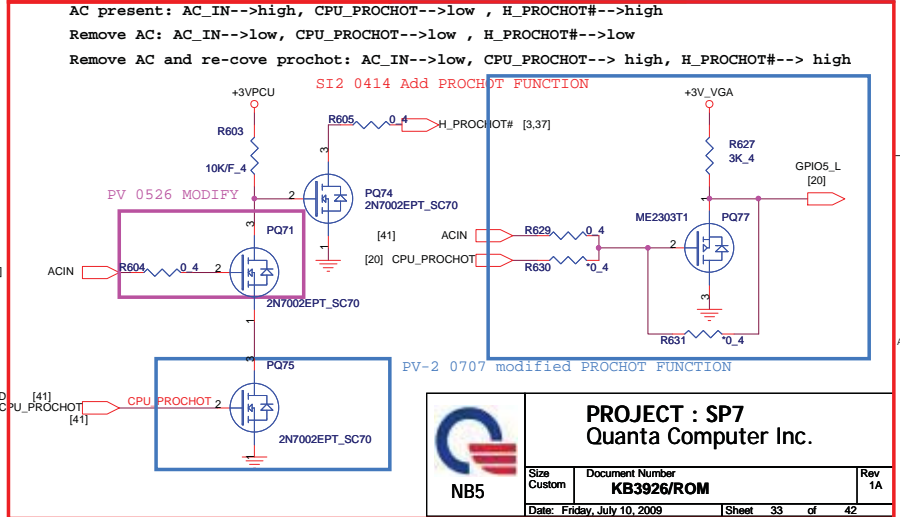
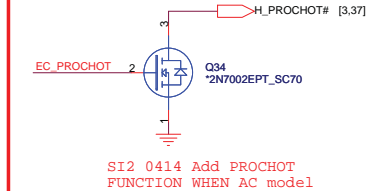
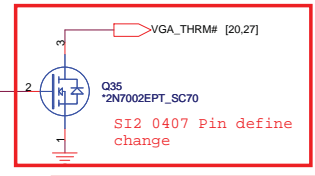
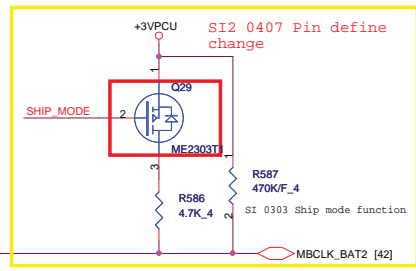
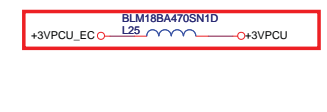
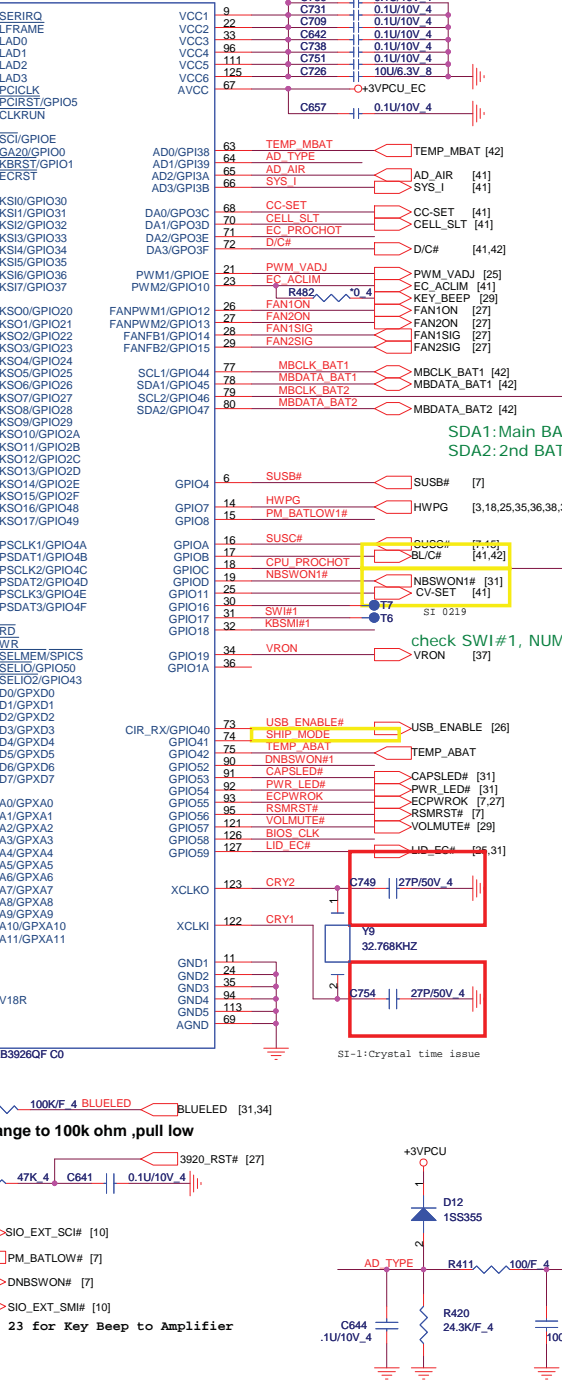
	PROJECT : SP7 Quanta Computer Inc.	
	Document Number Block Diagram	Rev 1A
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[2,3,7,8,9,10,11,13,14,15,16,18,25,26,27,28,29,30,31,33,34,37,40]
+3V
+3VLAVCC

Change U20 layout footprint to LQFP128-16X16-4-AA1

[15,26,29,35,36,37,38,39,40,41] +5VPCU- [8,13,15,25,31,34,35,36,38,39,40,41,42] +3VPCU- [2,3,7,8,9,10,11,13,14,15,16,18,25,26,27,28,29,30,31,32,34,37,40] +3V

[8]	SERRIQ	LFRAME#	3	SERRIQ	VCC1	9	C736	0.1U/10V_4
[8,34]	LFRAME#	LAD0	4	LFRAME	VCC2	22	C731	0.1U/10V_4
[8,34]	VAD0	LAD1	8	VAD0	VCC3	33	C709	0.1U/10V_4
[8,34]	LAD1	LAD2	7	LAD1	VCC5	96	C642	0.1U/10V_4
[8,34]	LAD2	LAD3	5	LAD2	VCC4	111	C738	0.1U/10V_4
[8,34]	LAD3	LAD3	12	LAD3	VCC6	125	C751	0.1U/10V_4
[9]	CLK_33M_KBC	PLTRST#	13	CLK	AVCC	67	C726	10U/6.3V_8
[3,9,18,26,32,34]	CLKRUN#	CLKRUN#	38	CLKRUN			C657	0.1U/10V_4
[7]	CLKRUN#	CLKRUN#	38	CLKRUN				
[31]	MX0	MX0	55	KS10/GPIO30				
[31]	MX1	MX1	56	KS11/GPIO31				
[31]	MX2	MX2	57	KS12/GPIO32				
[31]	MX3	MX3	58	KS13/GPIO33				
[31]	MX4	MX4	59	KS14/GPIO34				
[31]	MX5	MX5	60	KS15/GPIO35				
[31]	MX6	MX6	61	KS16/GPIO36				
[31]	MX7	MX7	62	KS17/GPIO37				
[31]	MY0	MY0	39	KS00/GPIO20				
[31]	MY1	MY1	40	KS01/GPIO21				
[31]	MY2	MY2	41	KS02/GPIO22				
[31]	MY3	MY3	42	KS03/GPIO23				
[31]	MY4	MY4	43	KS04/GPIO24				
[31]	MY5	MY5	44	KS05/GPIO25				
[31]	MY6	MY6	45	KS06/GPIO26				
[31]	MY7	MY7	46	KS07/GPIO27				
[31]	MY8	MY8	47	KS08/GPIO28				
[31]	MY9	MY9	48	KS09/GPIO29				
[31]	MY10	MY10	49	KS10/GPIO2A				
[31]	MY11	MY11	50	KS11/GPIO2B				
[31]	MY12	MY12	51	KS12/GPIO2C				
[31]	MY13	MY13	52	KS13/GPIO2D				
[31]	MY14	MY14	53	KS14/GPIO2E				
[31]	MY15	MY15	54	KS15/GPIO2F				
[31]	PSCLK1	PSCLK1	83	PSCLK1/GPIO4A				
[31]	PSCLK2	PSCLK2	84	PSCLK2/GPIO4B				
[31]	PSCLK3	PSCLK3	85	PSCLK3/GPIO4D				
[31]	PSCLK4	PSCLK4	86	PSCLK4/GPIO4E				
[31]	PSCLK5	PSCLK5	87	PSCLK5/GPIO4F				
[31]	PSCLK6	PSCLK6	88	PSCLK6/GPIO4F				
[10]	BIOS_RD#	BIOS_RD#	119	RD				
[10]	BIOS_WR#	BIOS_WR#	120	WR				
[10]	BIOS_CS#	BIOS_CS#	128	CS				
[9]	PCL_SERR#	PCL_SERR#	99	SELMEMSPICS				
[7]	SUS_PWR_ACK	MUTE_LED	112	SELIO2/GPIO43				
[29,31]	MUTE_LED	MUTE_LED	113	D1/GPXD0				
[34]	RF_LINK#	LAN_CABLE_DETECT	116	D2/GPXD1				
[42]	M/A#	M/A#	97	D3/GPXD2				
[31,39,40]	SUSON	LAN_POWER	98	D4/GPXD3				
[36,38,39,40,41]	MAINON	LAN_POWER	99	D5/GPXD4				
[40]	LAN_POWER	SS_ON	101	D6/GPXD5				
[41]	SS_ON	CHARGE_EN#	102	D7/GPXD6				
[41]	CHARGE_EN#	CHARGE_EN#	103	D8/GPXD7				
[41]	MBATLED0#	AC_LED_ON#	106	A0/GPXA0				
[31]	WIRE_ON#	WIRE_ON#	107	A1/GPXA1				
[31]	WIRE_OFF#	WIRE_OFF#	108	A2/GPXA2				
[7]	AC_PRESENT	AC_PRESENT	124	A3/GPXA3				
[41]	AC_LED_ON#	AC_LED_ON#	106	A4/GPXA4				
[31]	WIRE_ON#	WIRE_ON#	107	A5/GPXA5				
[31]	WIRE_OFF#	WIRE_OFF#	108	A6/GPXA6				
[41]	AC_LED_ON#	AC_LED_ON#	106	A7/GPXA7				
[31]	WIRE_ON#	WIRE_ON#	107	A8/GPXA8				
[31]	WIRE_OFF#	WIRE_OFF#	108	A9/GPXA9				
[31]	WIRE_ON#	WIRE_ON#	107	A10/GPXA10				
[31]	WIRE_OFF#	WIRE_OFF#	108	A11/GPXA11				



ADD LAN_POWER 11/23
 ADD CHARGE_EN# 11/23
 ADD CV-SET 11/23
 Change to RB501V-40
 Add Pin 117,103 for DSM,116 for Bluetooth,Pin 23 for Key Beep to Amplifier
 Add T37,T38,T39 for EC
 Delete T10 and tie pin 117 for Lan for DSM

Socket: DG008000031
 AMIC AKE38ZN0800
 MXIC AKE38FP0200
 WINBOND AKE38ZP0N01
 EON AKE38ZA0Q00

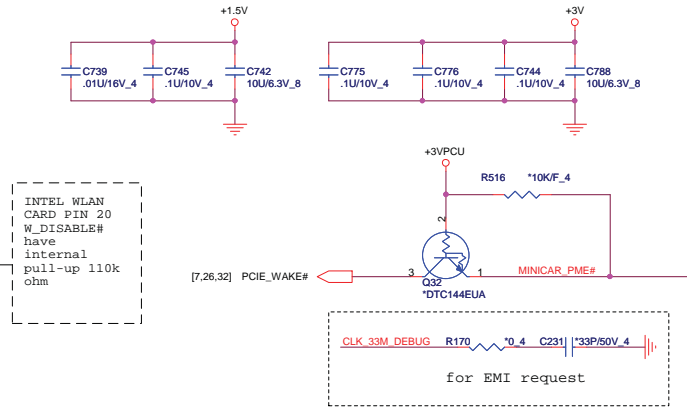
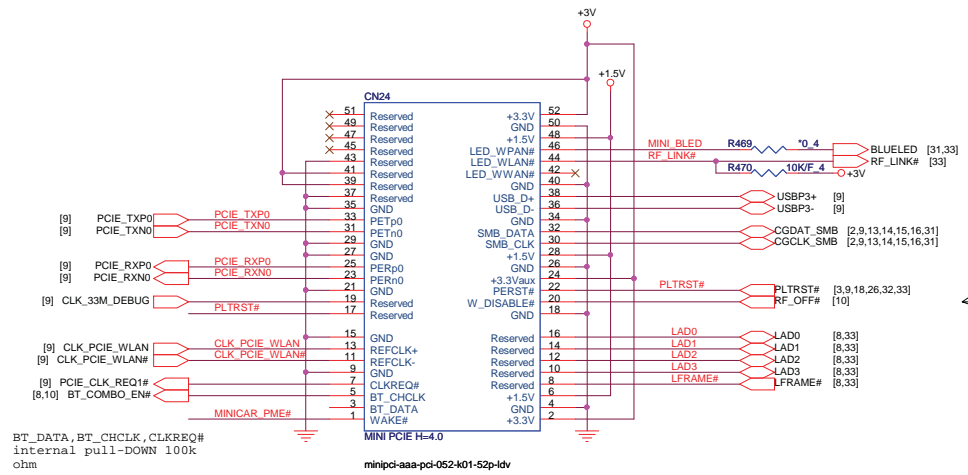
2M byte
 SPI
 BIOS

AC present: AC_IN-->high, CPU_PROCHOT-->low, H_PROCHOT#-->high
 Remove AC: AC_IN-->low, CPU_PROCHOT-->low, H_PROCHOT#-->low
 Remove AC and re-cove proshot: AC_IN-->low, CPU_PROCHOT--> high, H_PROCHOT#--> high

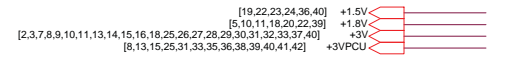
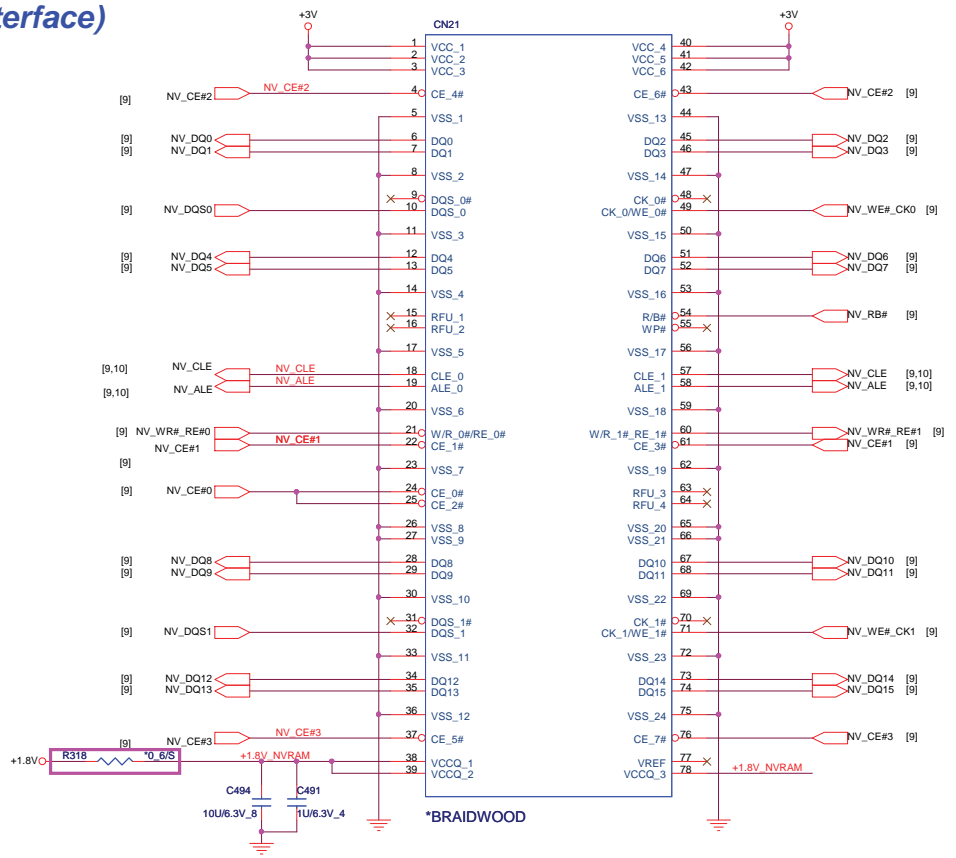
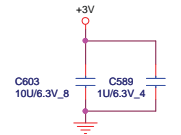
PROJECT : SP7
 Quanta Computer Inc.

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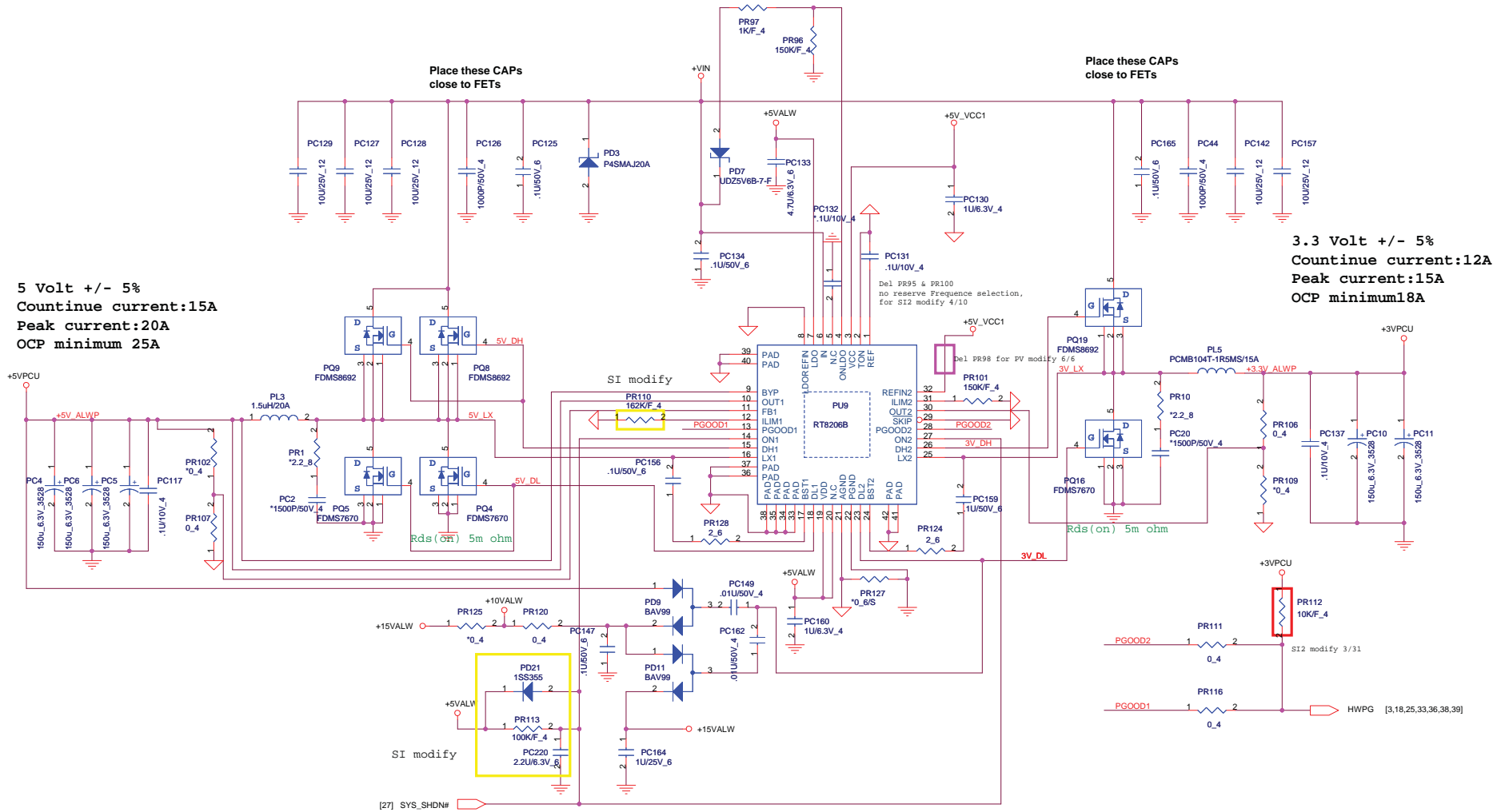
Half size mini card(802.11a/b/g/n)

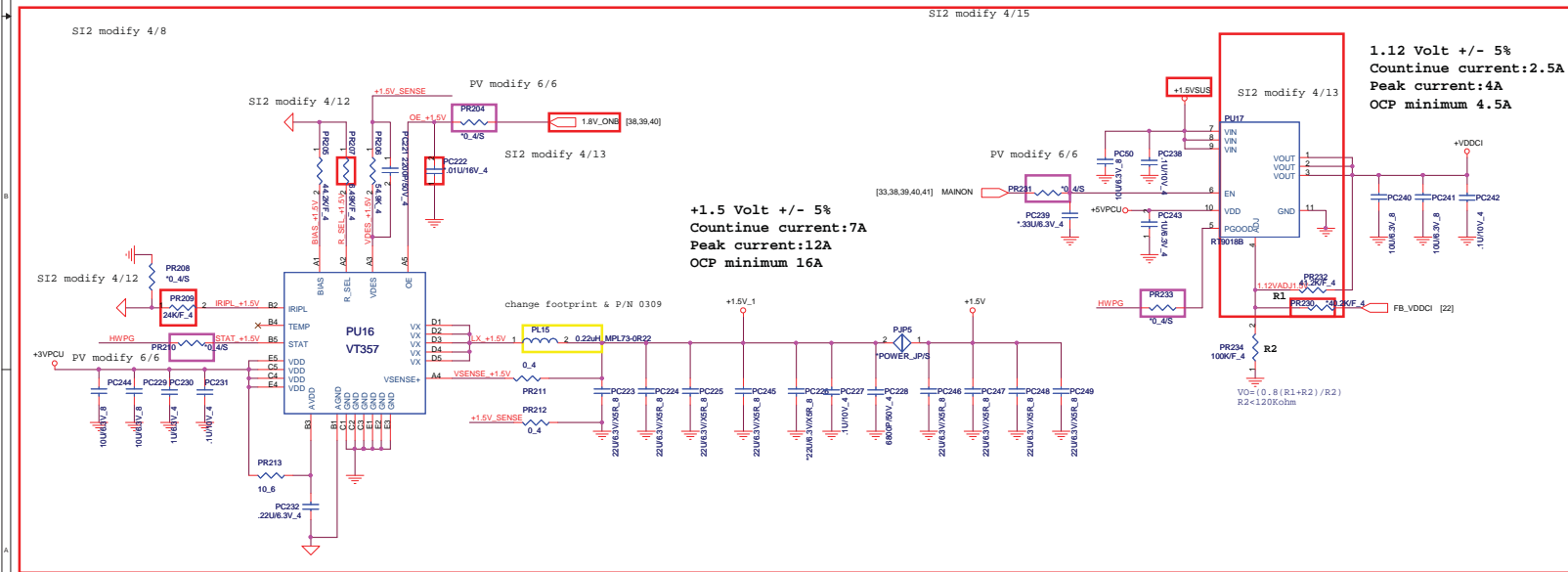
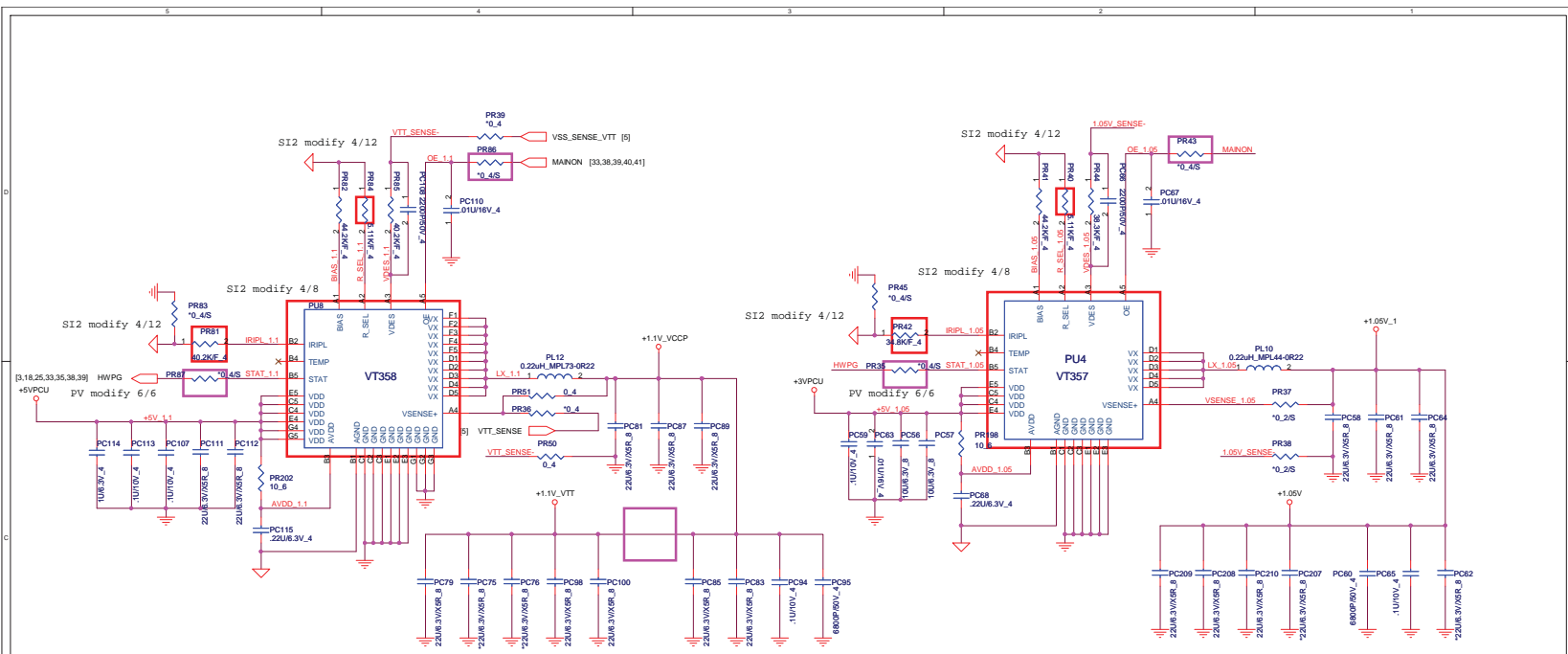


Braidwood(Open Nand Flash Interface)



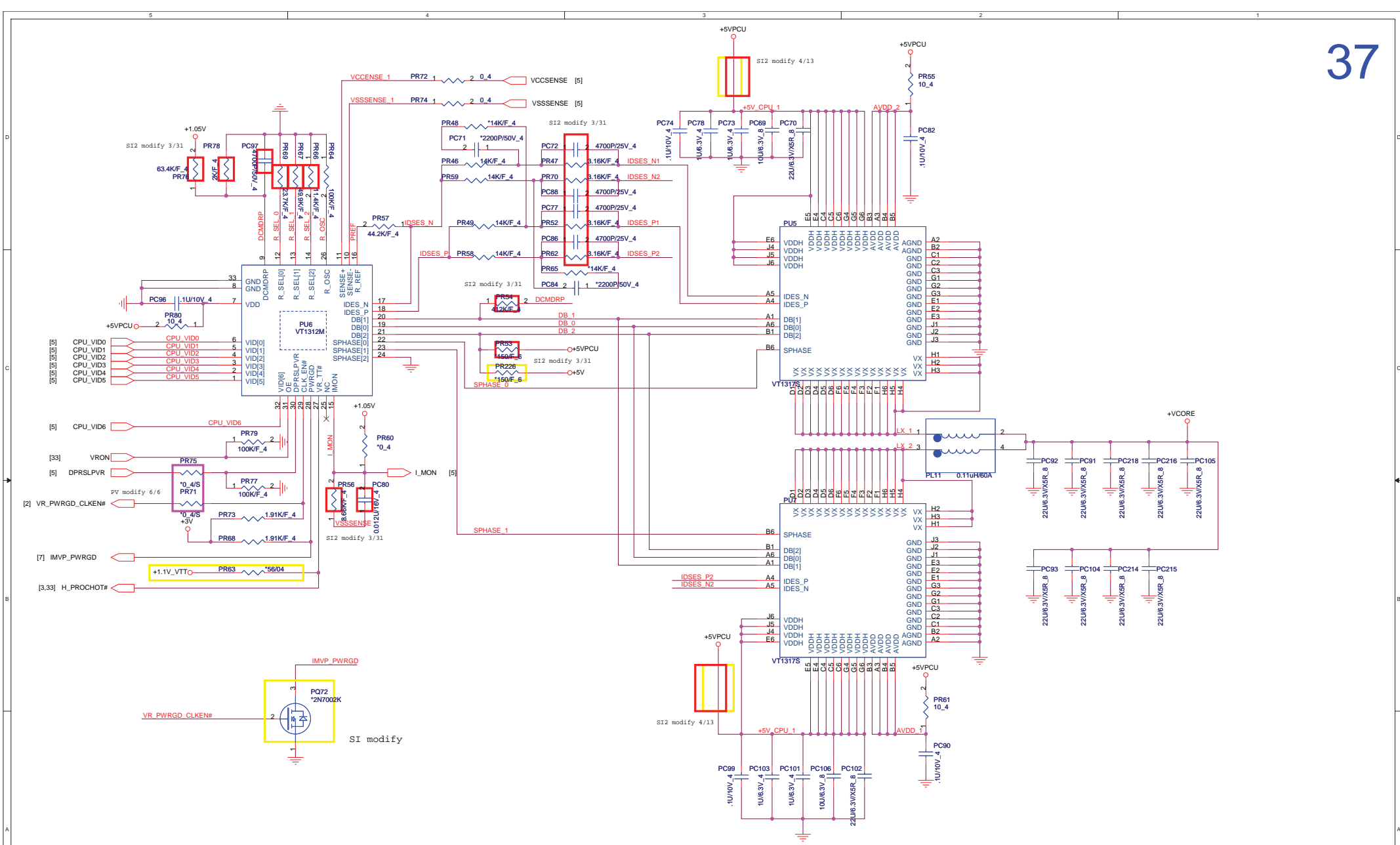
	PROJECT : SP7 Quanta Computer Inc.	
	Size Custom Document Number Half size mini card/Braidwood	Rev 1A
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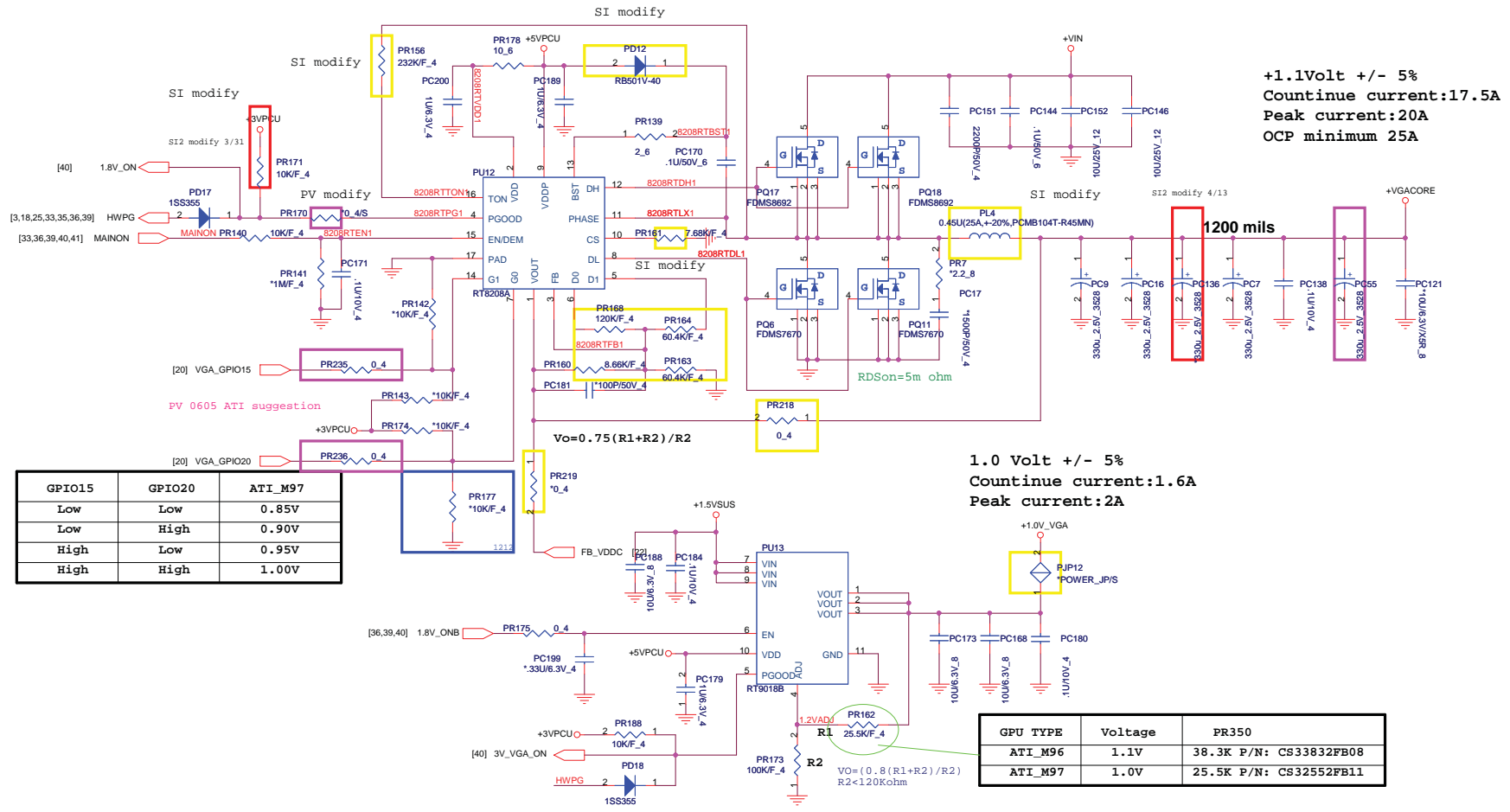


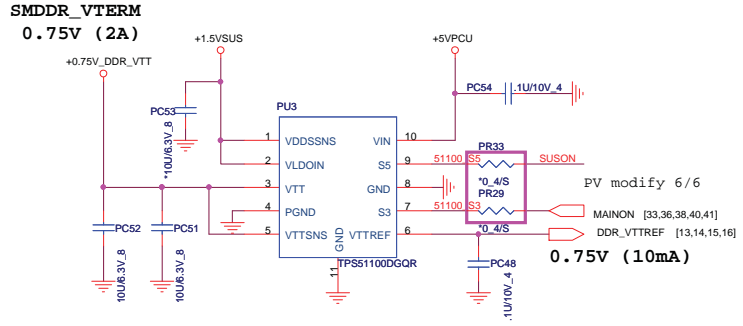
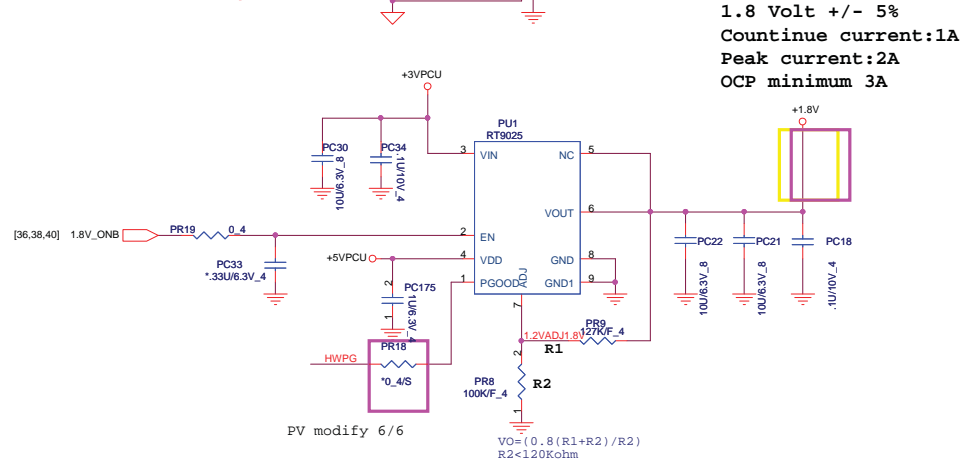
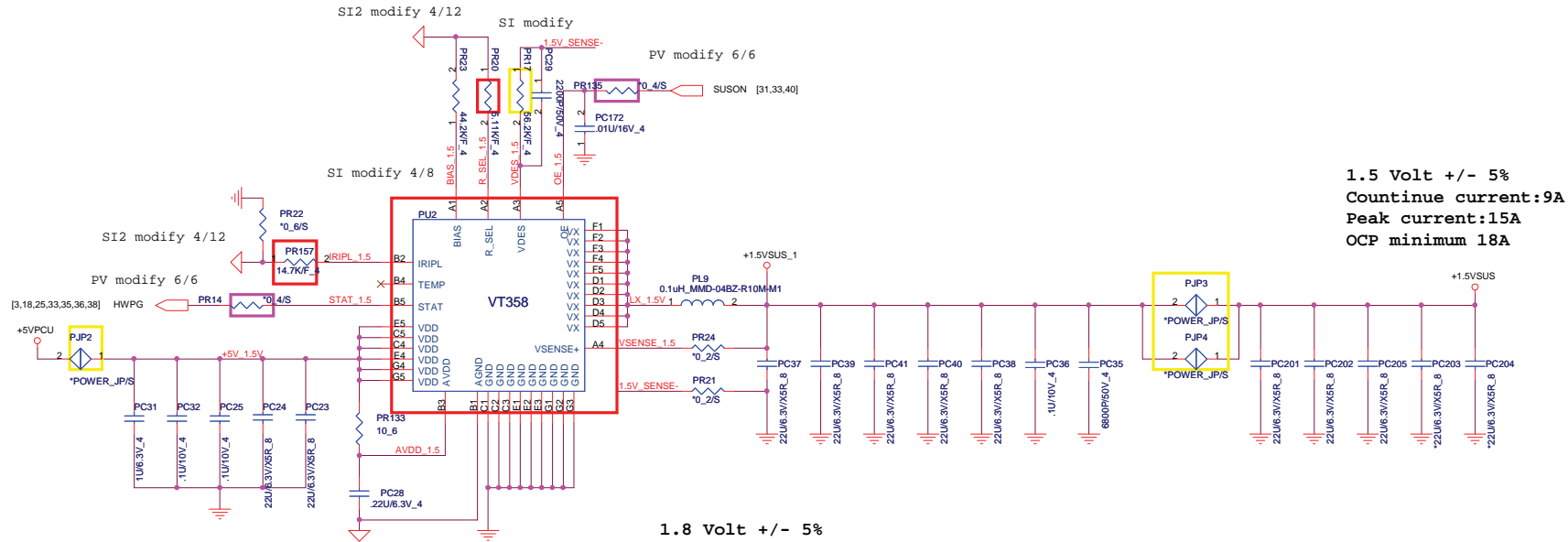
+1.5 Volt +/- 5%
Continue current:7A
Peak current:12A
OCF minimum 16A

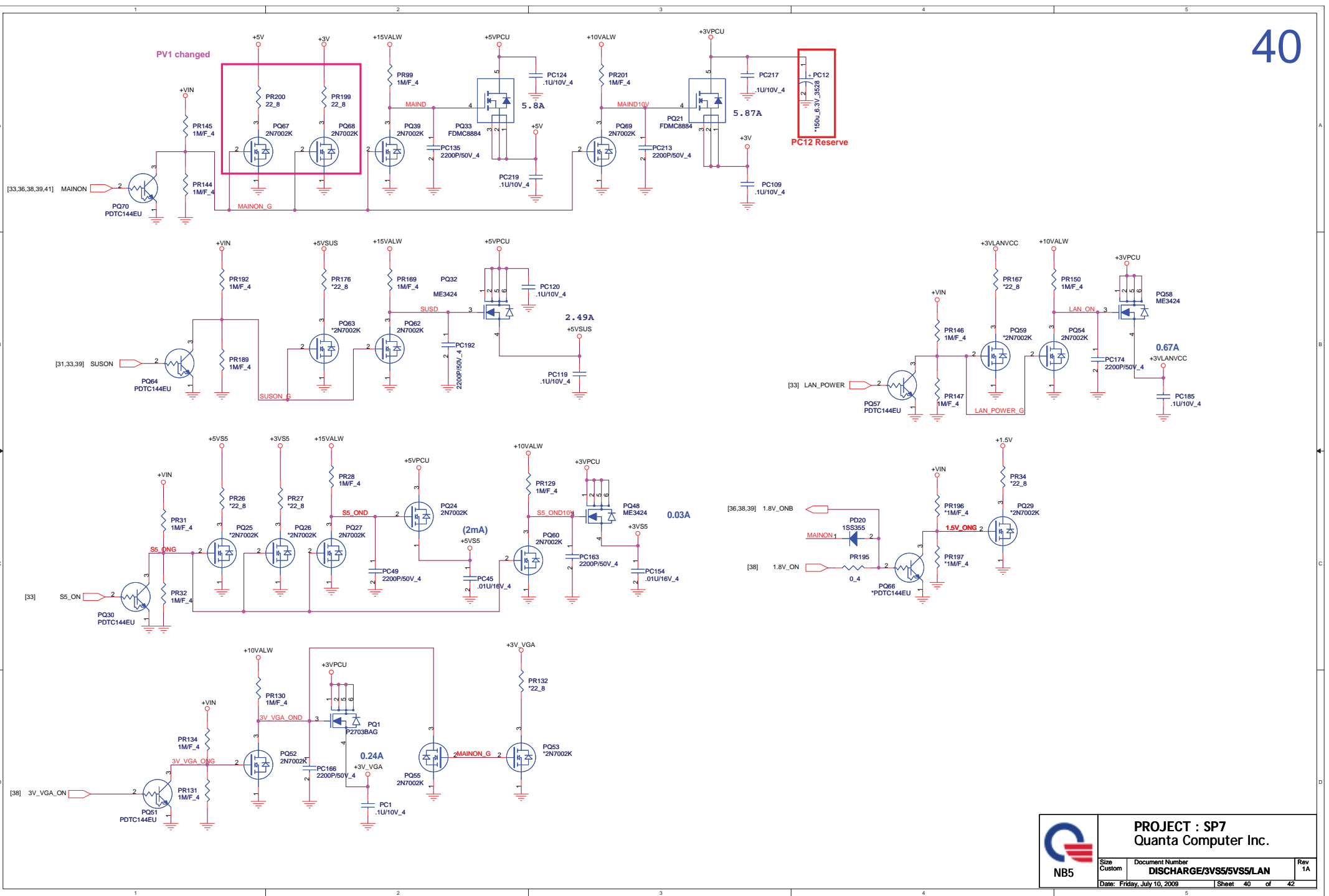
1.12 Volt +/- 5%
Continue current:2.5A
Peak current:4A
OCF minimum 4.5A




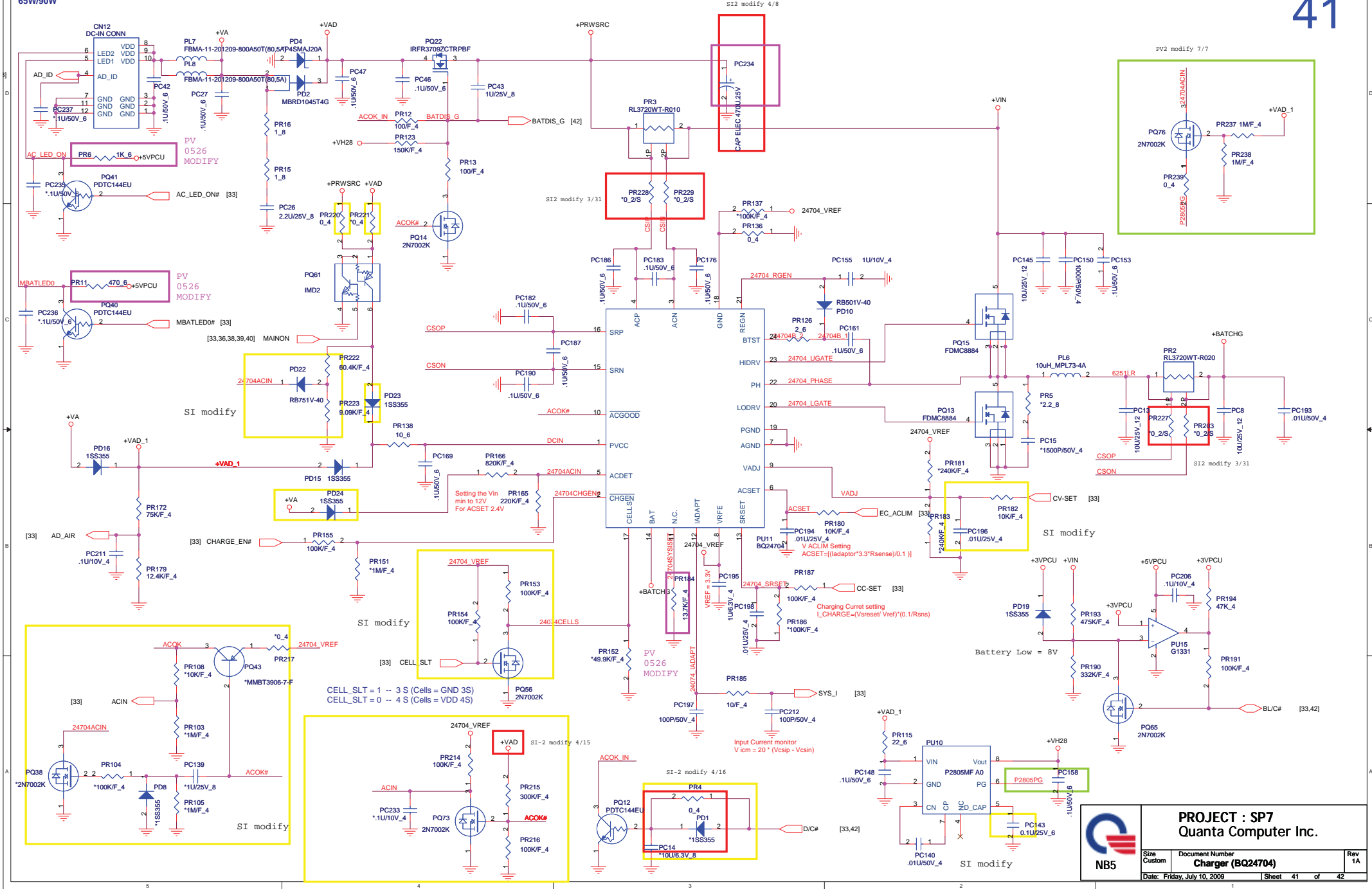
VGA Core & VCC1.1





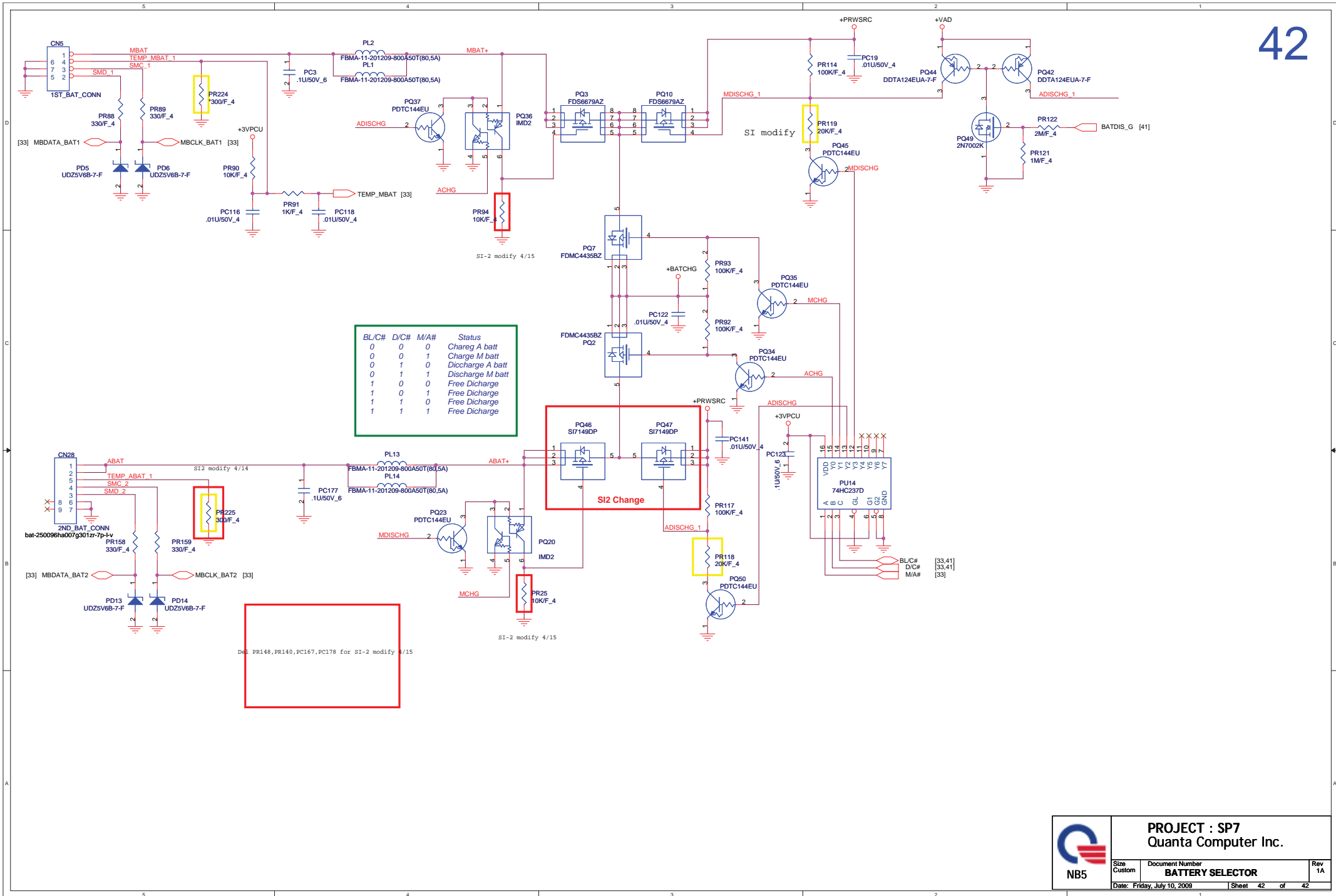


	PROJECT : SP7 Quanta Computer Inc.	
	Size Custom Document Number DISCHARGE/3VS5/5VS5/LAN	Rev 1A
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	PROJECT : SP7 Quanta Computer Inc.	
	Size Custom	Document Number Charger (BQ24704)
	Date: Friday, July 10, 2009	Rev 1A

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