

Compal confidential

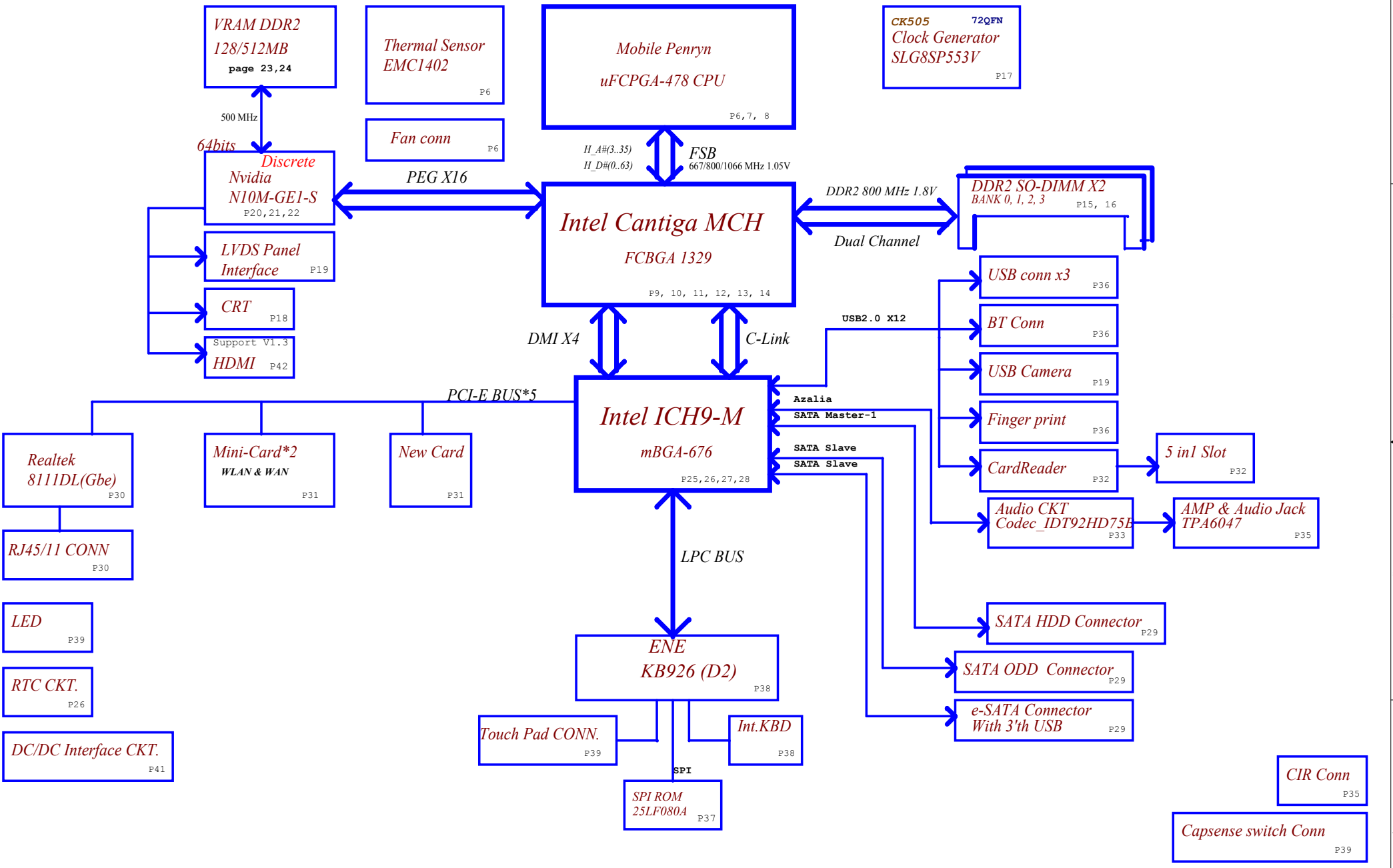
Schematics Document

Mobile Penryn uFCPGA with Intel
Cantiga_PM+ICH9-M core logic

2009-02-13

REV : 1.0

Security Classification	Compal Secret Data			Title Compal Electronics, Inc.		
Issued Date	2008/12/10	Deciphered Date	2008/12/10	Size Document Number Custort LA-4731P Rhett discrete		Rev 0.1
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Issued Date	2008/11/04	Deciphered Date	2008/11/04	Block Diagram	
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Voltage Rails

O MEANS ON

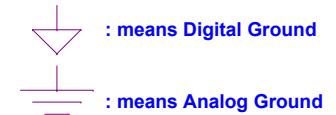
X MEANS OFF

power plane	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +2.5VS +1.8VS +NVVDD +PCIE
State				
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

BOM

NB	SA00002JJ80	R1	FRU
NB	SA00002JJE0	R3	
SB	SA00002JH50	R1	FRU
SB	SA00002JHB0	R3	

Symbol Note :



@ :	means just reserve , no build
45@ :	means need be mounted when 45 level assy or rework stage.
DEBUG@ :	means just reserve for debug.
BATT @ :	means need be mounted when 45 level assy or rework stage.
CONN@ :	means ME part
ESATA @ :	means just reserve for ESATA
GS @ :	means just reserve for G sensor
FP @ :	means just reserve for Finger Print
NewC@ :	means just reserve for New card
Main@ :	means just reserve for Main stream
OPP@ :	means just reserve for OPP
2MiniC@ :	means just reserve for 2nd Mini card slot
PA @ :	means just reserve for PA
PR @ :	means just reserve for PR

USB assignment:

- USB-0 Right side(with ESATA)
- USB-1 Left side
- USB-2 Left side
- USB-3 Dock
- USB-4 Camera
- USB-5 WLAN
- USB-6 Bluetooth
- USB-7 Finger Printer
- USB-8 MiniCard(WWAN/TV)
- USB-9 Express card
- USB-10 X
- USB-11 X

PCIe assignment:

- PCIe-1 TV tuner/WWAN/Robeson
- PCIe-2 X
- PCIe-3 WLAN
- PCIe-4 GLAN (Marvell)
- PCIe-6 New Card

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	Thermal Sensor	SODIMM	CLK CHIP	MINI CARD	Sensor board	N10M Thermal Sensor	N10M	G-sensor
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	V	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X	V	V	X
ICH_SMBCLK ICH_SMBDATA	ICH9	X	X	X	X	V	V	V	X	X	X	V

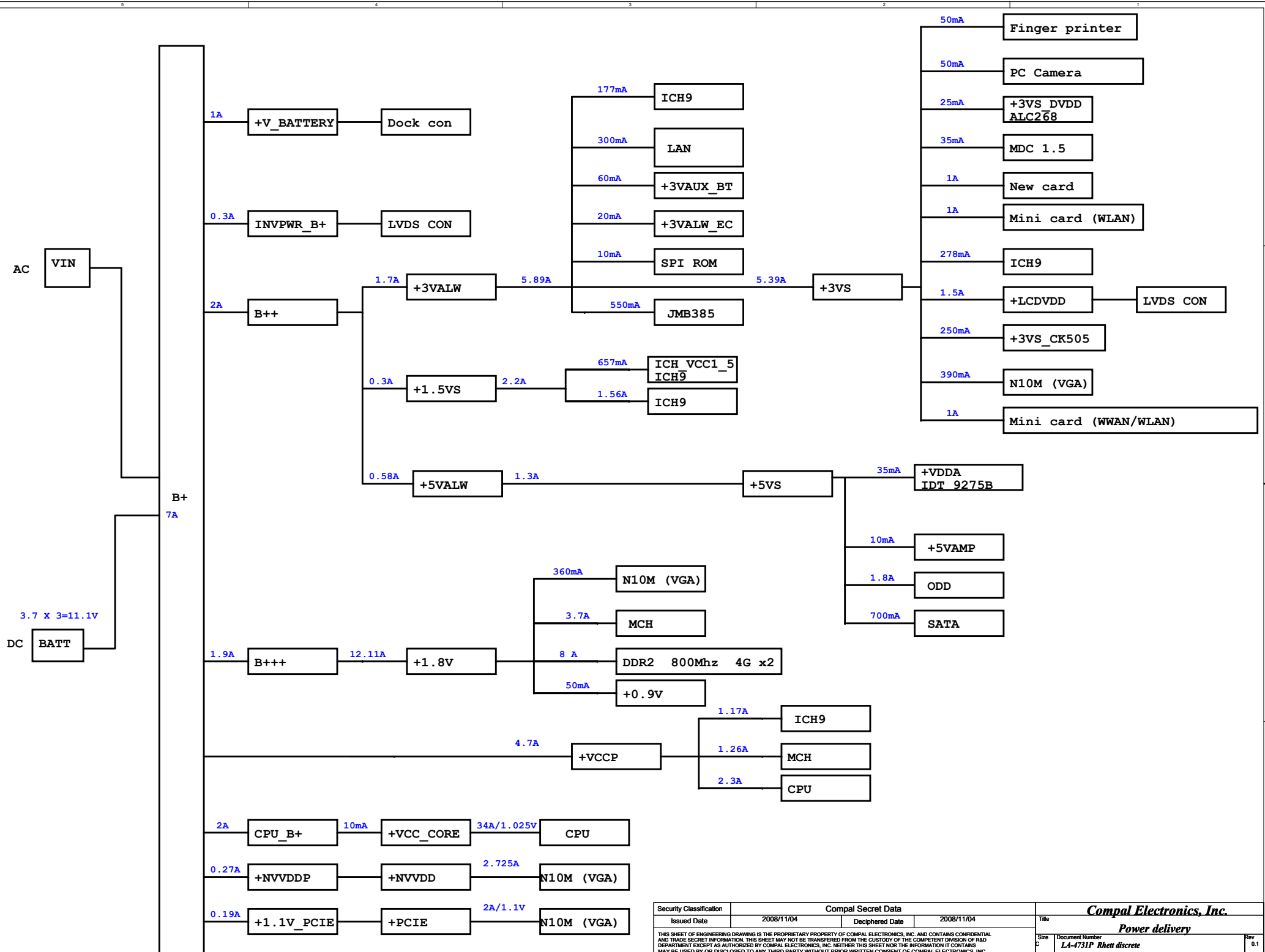
NB9M SMBUS Control Table

	SOURCE	LVDS	CRT	HDMI	HDCP
DDC2_DATA DDC2_CLK	N10M	V	X	X	X
3VDDCDA 3VDDCCL	N10M	X	V	X	X
HDMIDAT_VGA HDMICLK_VGA	N10M	X	X	V	X
HDCP_SDA HDCP_SCL	N10M	X	X	X	V

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

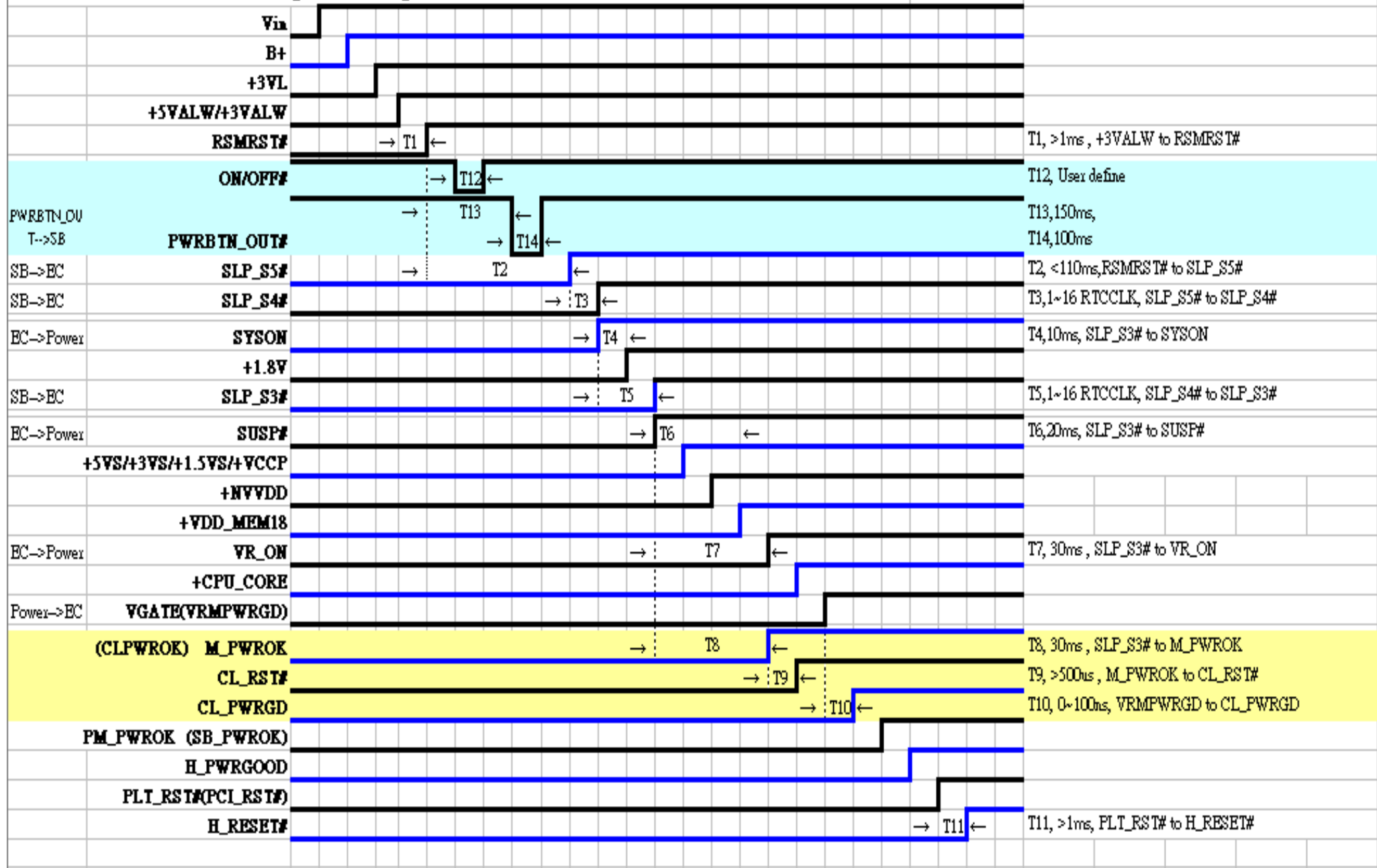
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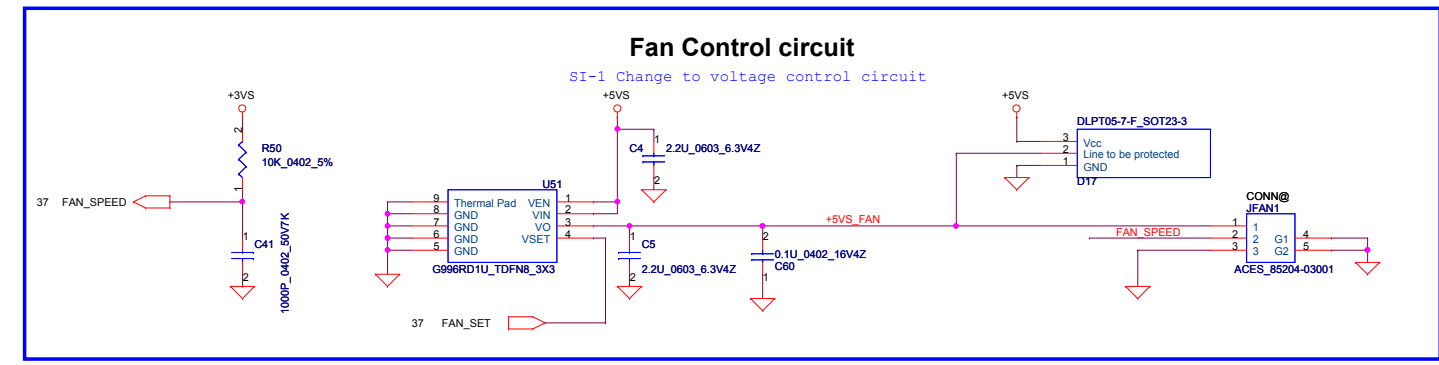
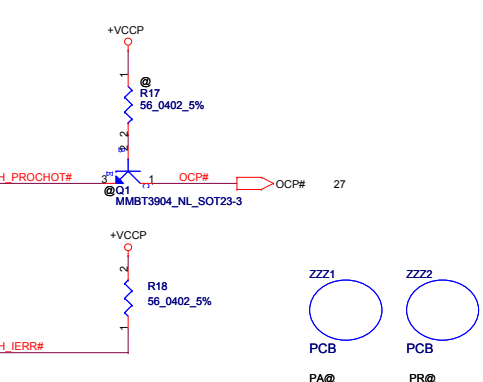
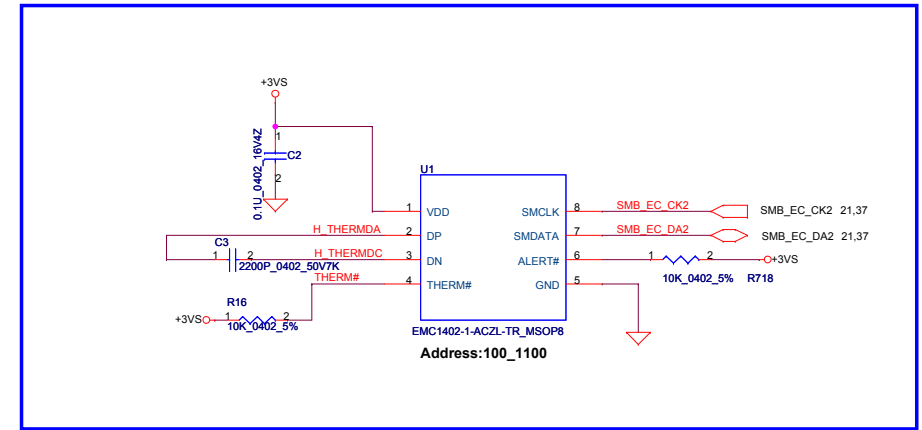
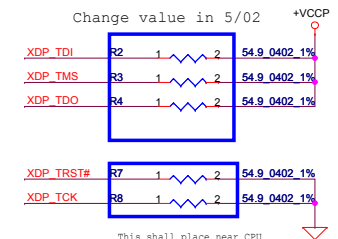
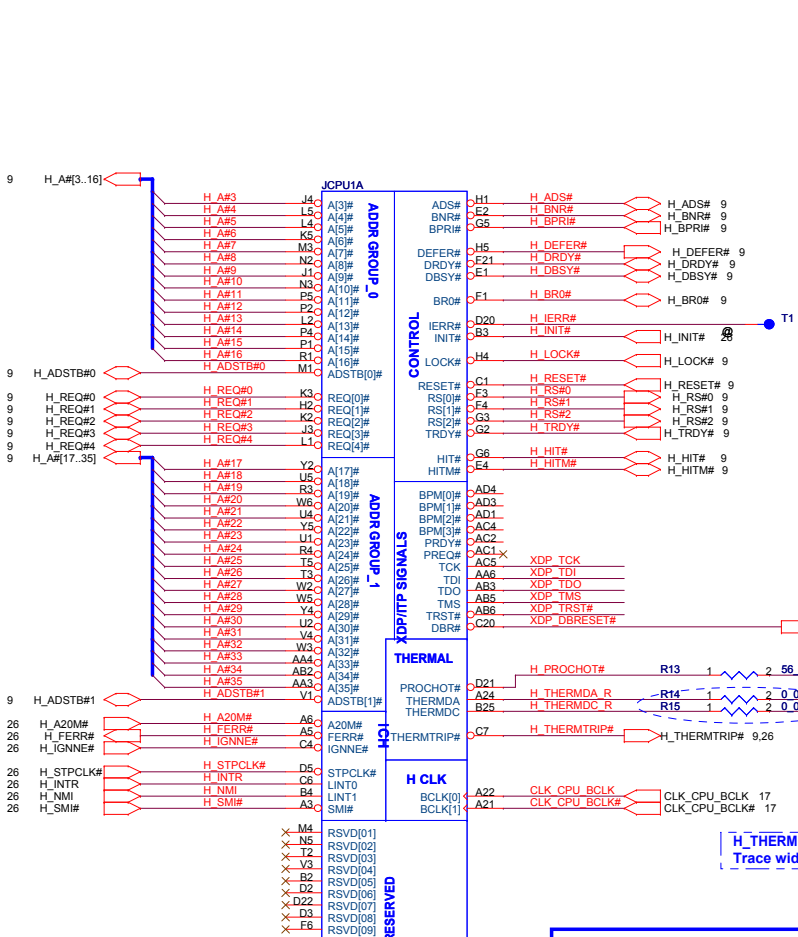


Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/11/04	Deciphered Date	2008/11/04	Title
				Power delivery
Size	Document Number	Rev		
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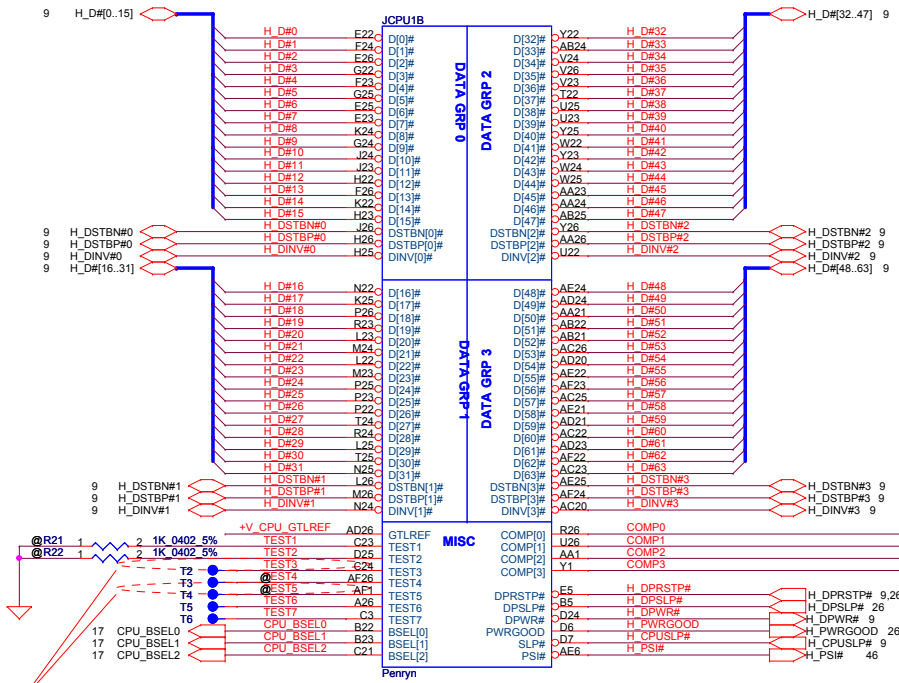
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JAL50 Discrete power sequence AC mode





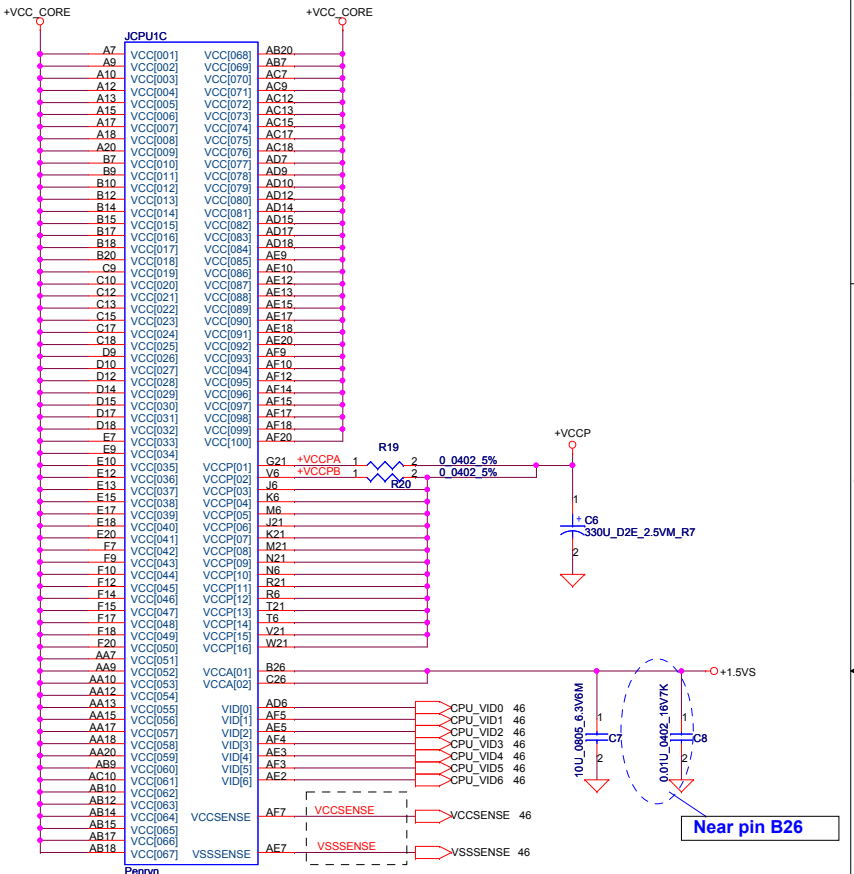
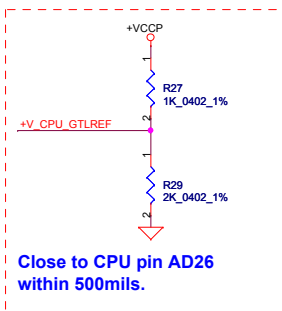
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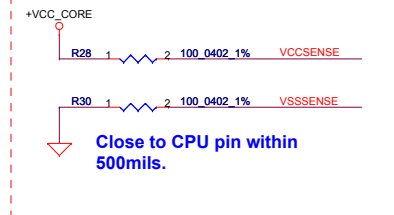
* Route the TEST3 and TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

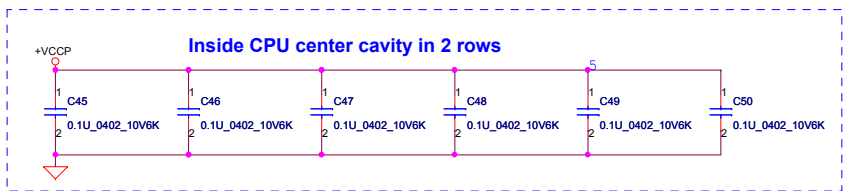
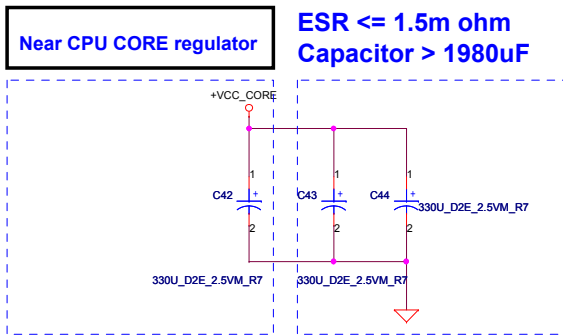
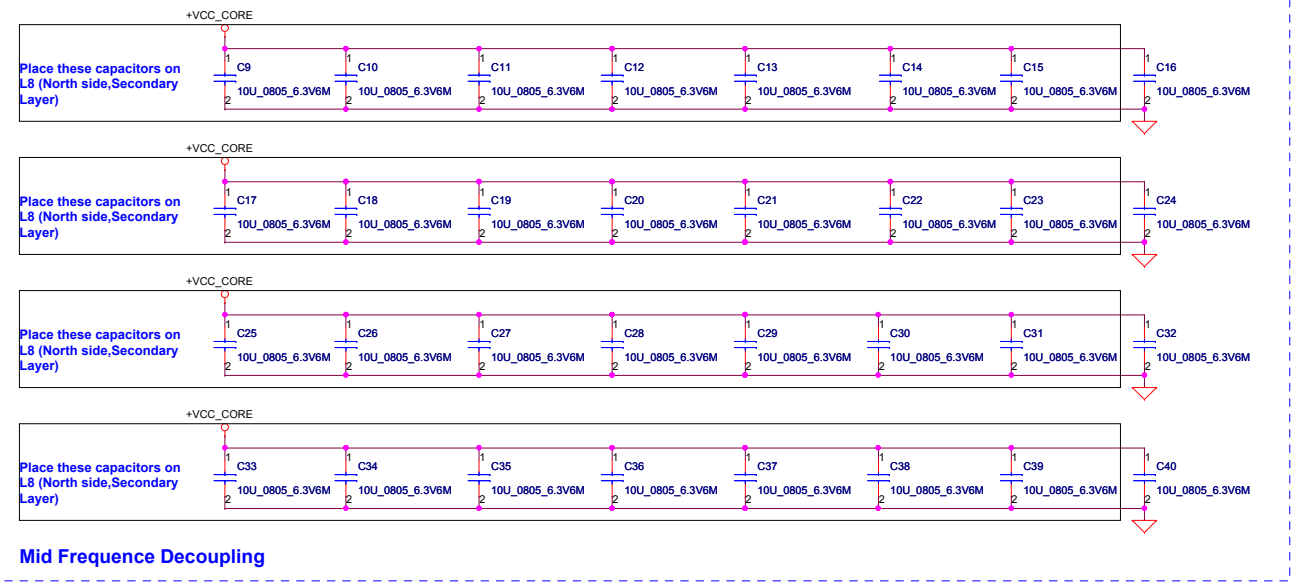
Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



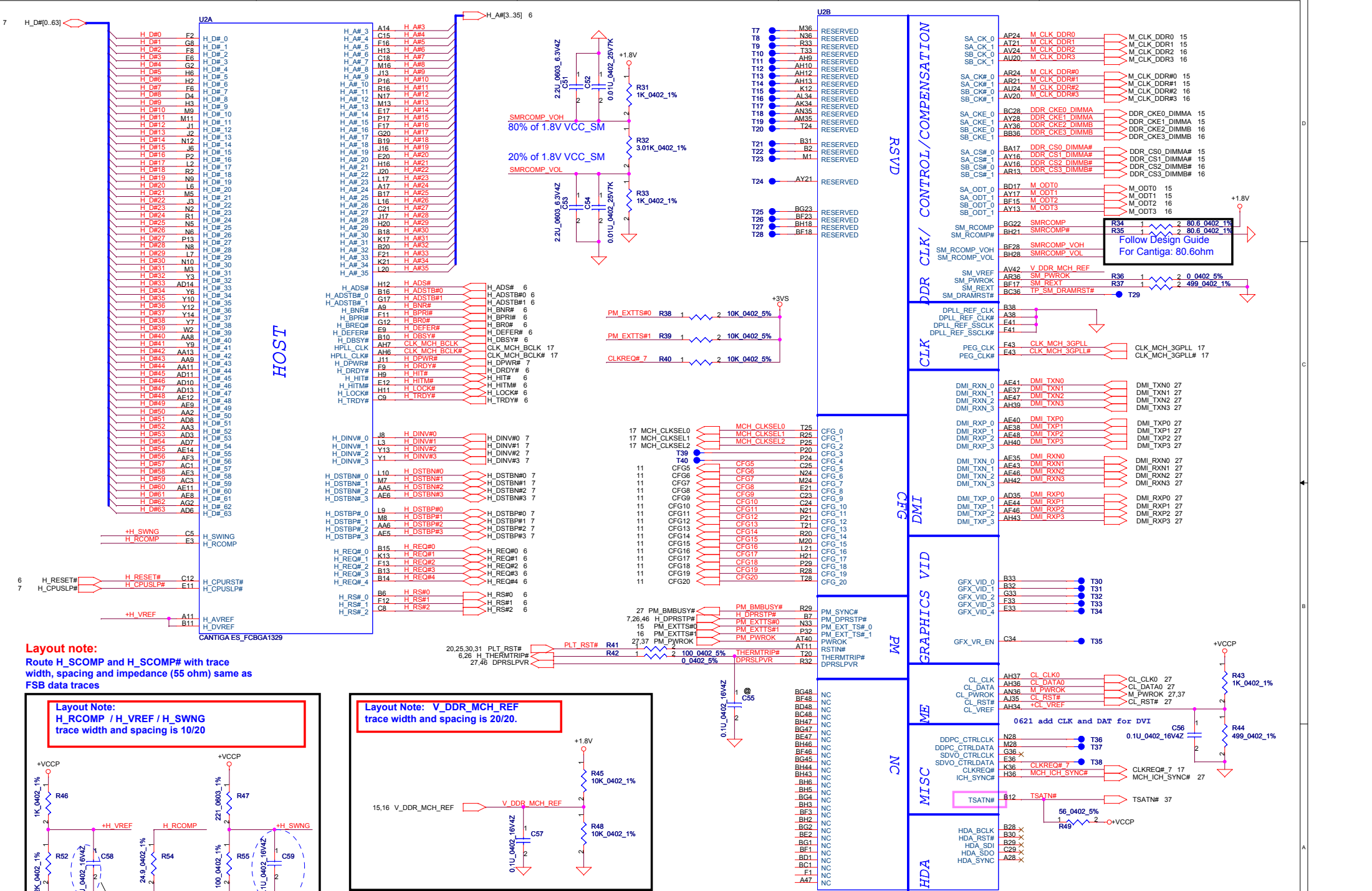
Length match within 25 mils. The trace width/space/other is 20/7/25.



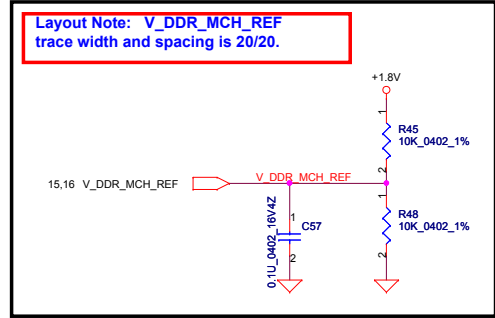
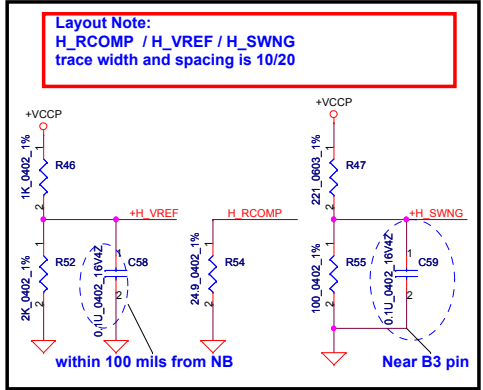
JCPU1D		
A4	VSS(001)	VSS(082)
A8	VSS(002)	VSS(083)
A11	VSS(003)	VSS(084)
A14	VSS(004)	VSS(085)
A16	VSS(005)	VSS(086)
A19	VSS(006)	VSS(087)
A23	VSS(007)	VSS(088)
AF2	VSS(008)	VSS(089)
B6	VSS(009)	VSS(090)
B8	VSS(010)	VSS(091)
B11	VSS(011)	VSS(092)
B13	VSS(012)	VSS(093)
B19	VSS(013)	VSS(094)
B21	VSS(014)	VSS(095)
B24	VSS(015)	VSS(096)
C5	VSS(016)	VSS(097)
C8	VSS(017)	VSS(098)
C11	VSS(018)	VSS(099)
C14	VSS(019)	VSS(100)
C16	VSS(020)	VSS(101)
C19	VSS(021)	VSS(102)
C2	VSS(022)	VSS(103)
C22	VSS(024)	VSS(105)
C25	VSS(025)	VSS(106)
D4	VSS(026)	VSS(107)
D8	VSS(027)	VSS(108)
D11	VSS(028)	VSS(109)
D13	VSS(029)	VSS(110)
D16	VSS(030)	VSS(111)
D19	VSS(031)	VSS(112)
D23	VSS(032)	VSS(113)
D26	VSS(033)	VSS(114)
E3	VSS(034)	VSS(115)
E6	VSS(035)	VSS(116)
E8	VSS(036)	VSS(117)
E11	VSS(037)	VSS(118)
E14	VSS(038)	VSS(119)
E16	VSS(039)	VSS(120)
E19	VSS(040)	VSS(121)
E21	VSS(041)	VSS(122)
E24	VSS(042)	VSS(123)
F5	VSS(043)	VSS(124)
F8	VSS(044)	VSS(125)
F11	VSS(045)	VSS(126)
F13	VSS(046)	VSS(127)
F16	VSS(047)	VSS(128)
F19	VSS(048)	VSS(129)
F22	VSS(049)	VSS(130)
F25	VSS(050)	VSS(131)
G4	VSS(051)	VSS(132)
G1	VSS(052)	VSS(133)
G23	VSS(053)	VSS(134)
G26	VSS(054)	VSS(135)
H3	VSS(055)	VSS(136)
H6	VSS(056)	VSS(137)
H21	VSS(057)	VSS(138)
H24	VSS(058)	VSS(139)
J2	VSS(059)	VSS(140)
J5	VSS(060)	VSS(141)
J22	VSS(061)	VSS(142)
J25	VSS(062)	VSS(143)
K1	VSS(063)	VSS(144)
K4	VSS(064)	VSS(145)
K23	VSS(065)	VSS(146)
K26	VSS(066)	VSS(147)
L3	VSS(067)	VSS(148)
L6	VSS(068)	VSS(149)
L24	VSS(069)	VSS(150)
L21	VSS(070)	VSS(151)
M2	VSS(071)	VSS(152)
M5	VSS(072)	VSS(153)
M22	VSS(073)	VSS(154)
M25	VSS(074)	VSS(155)
N1	VSS(075)	VSS(156)
N4	VSS(076)	VSS(157)
N11	VSS(077)	VSS(158)
N23	VSS(078)	VSS(159)
N26	VSS(079)	VSS(160)
P3	VSS(080)	VSS(161)
P6	VSS(081)	VSS(162)
P6	VSS(082)	VSS(163)



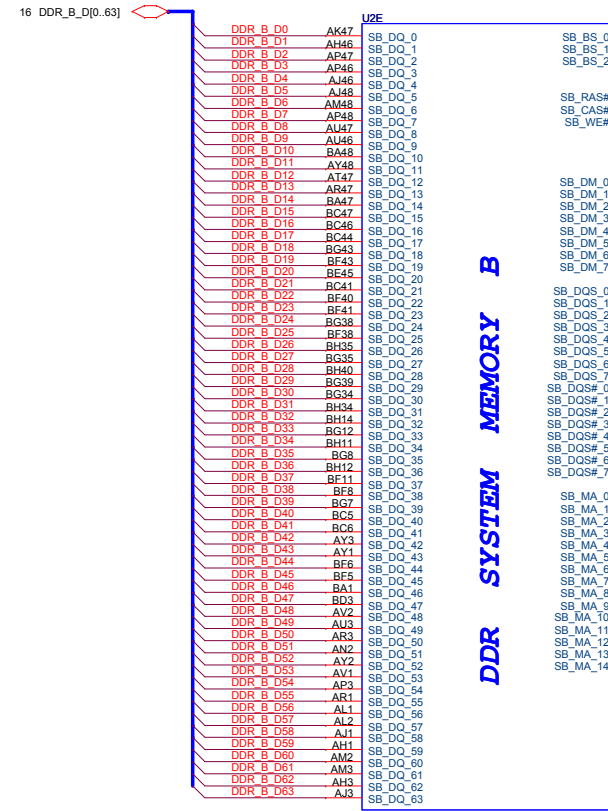
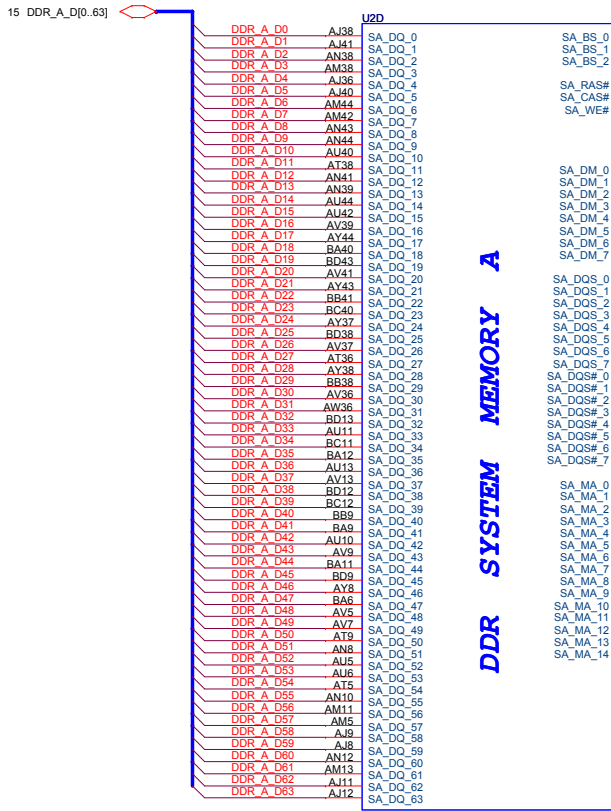
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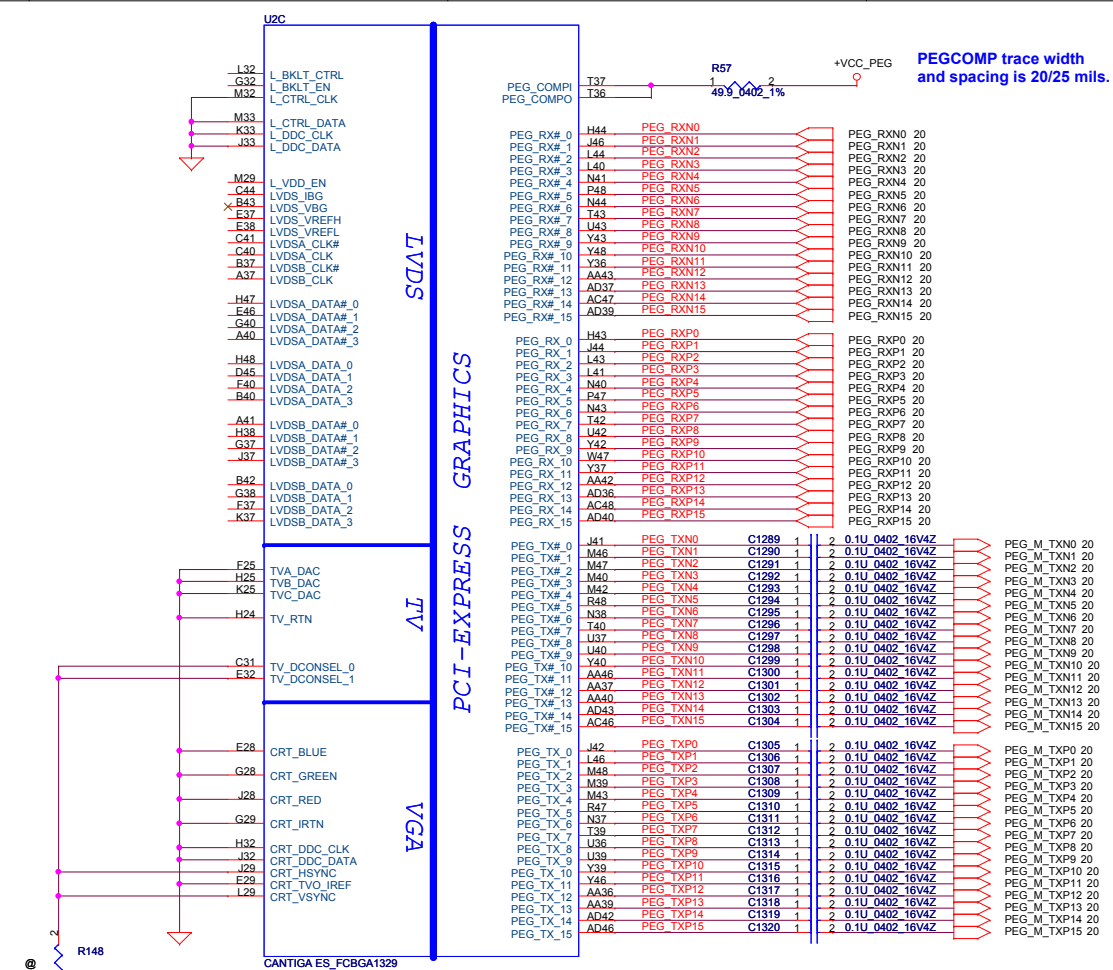
Layout note:
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces



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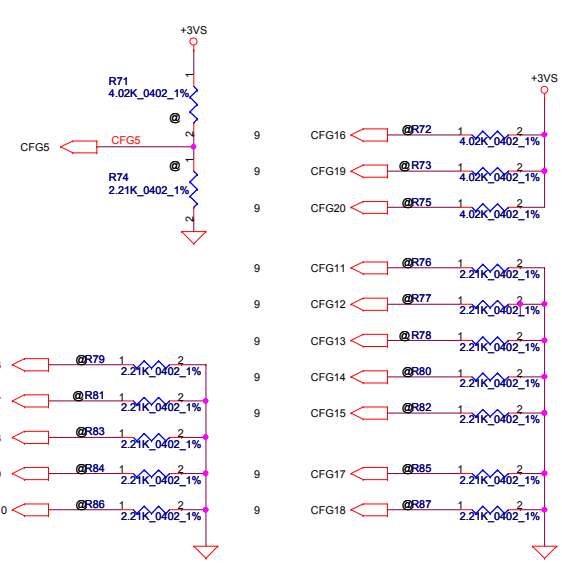


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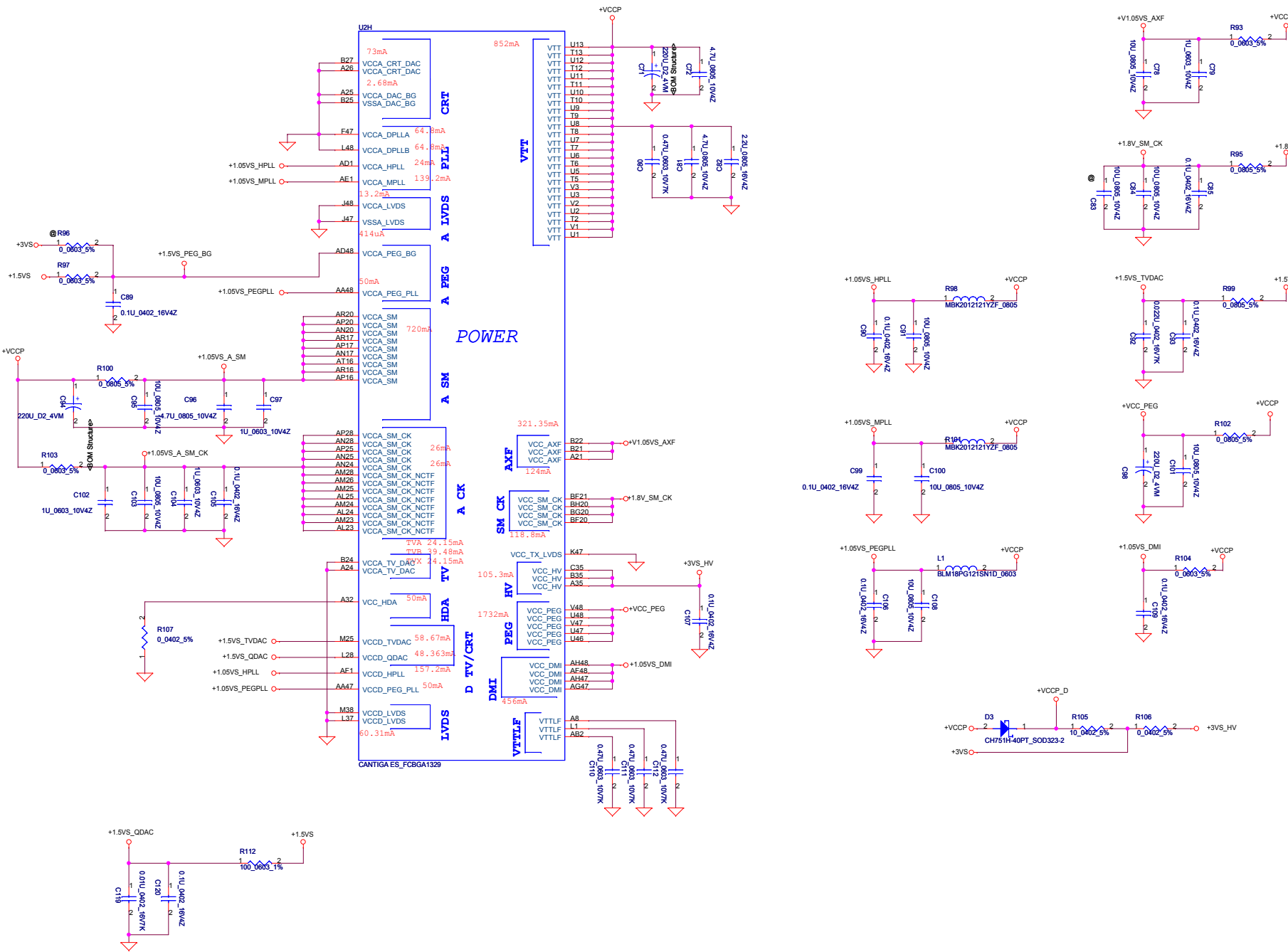


Strap Pin Table

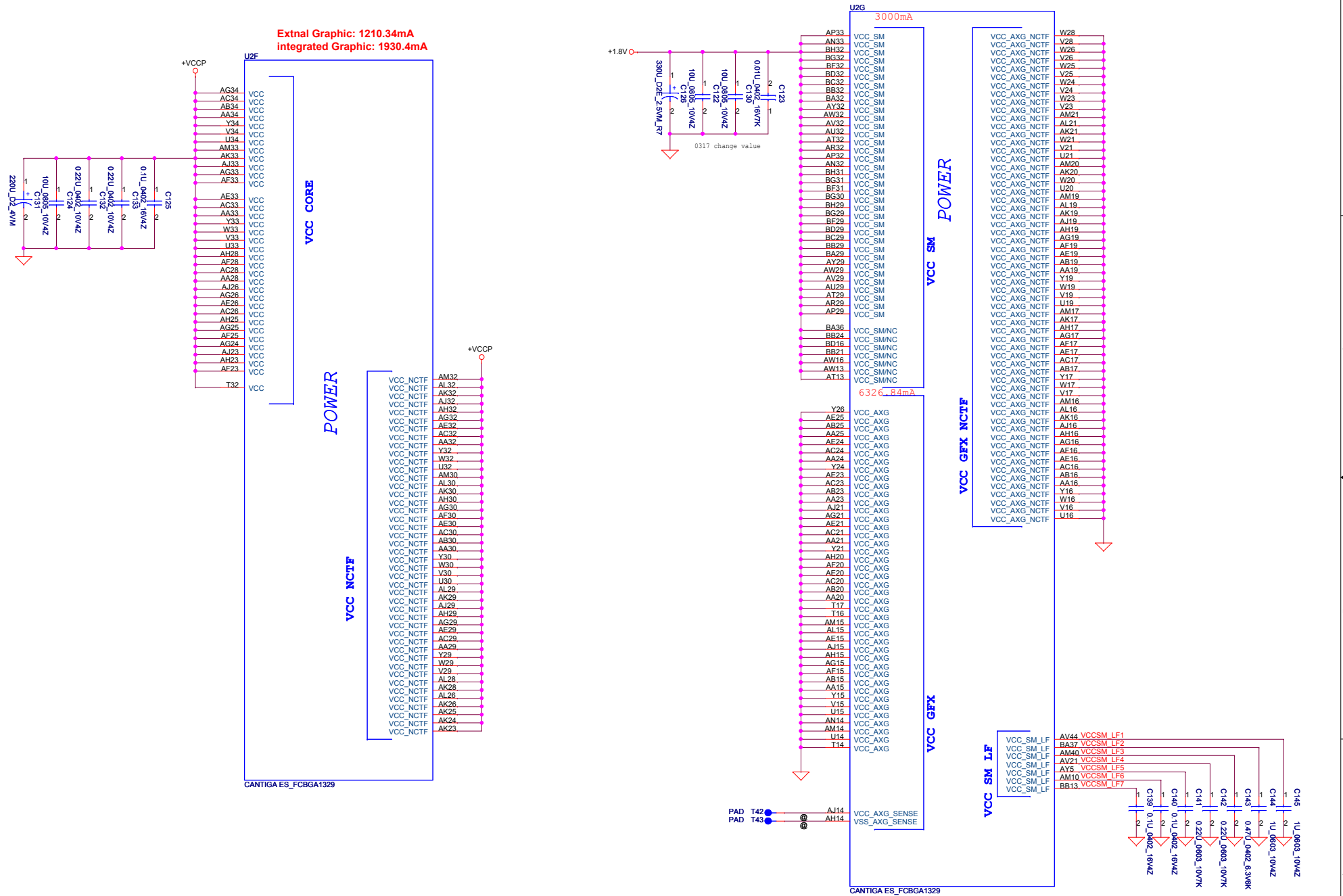
CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The ITPM Host Interface is enable 1 = The ITPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0=(TLS)chiper suite with no confidentiality 1=(TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu. *



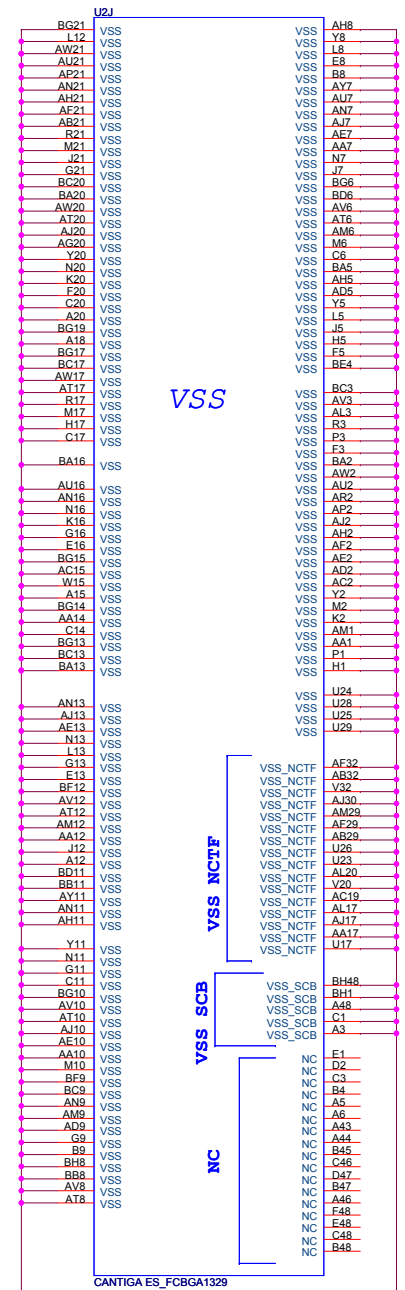
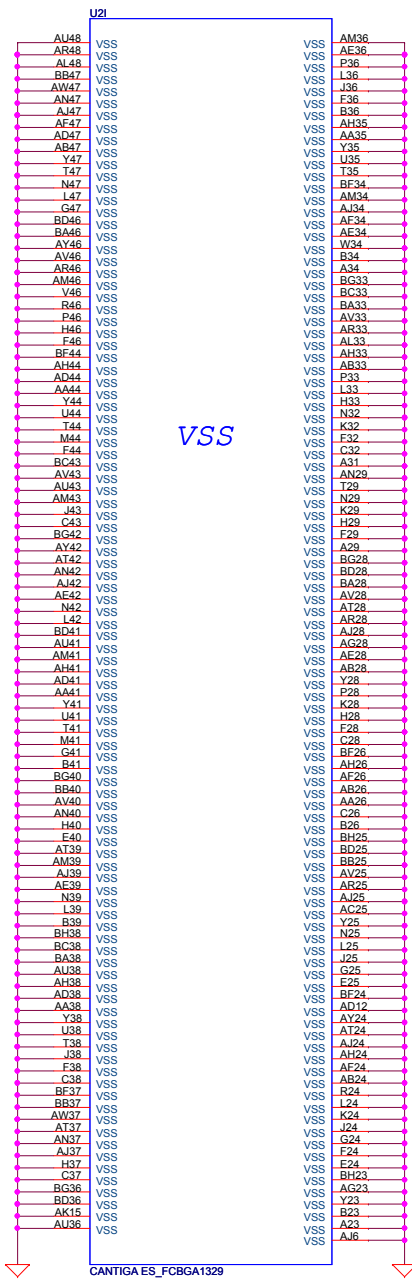
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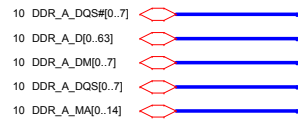
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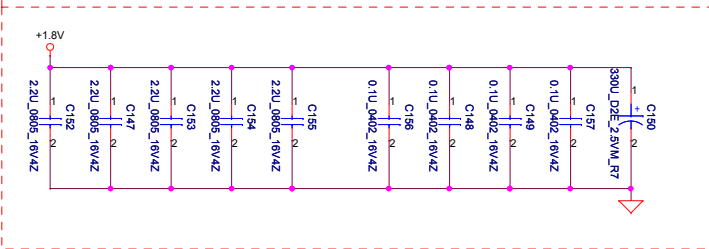
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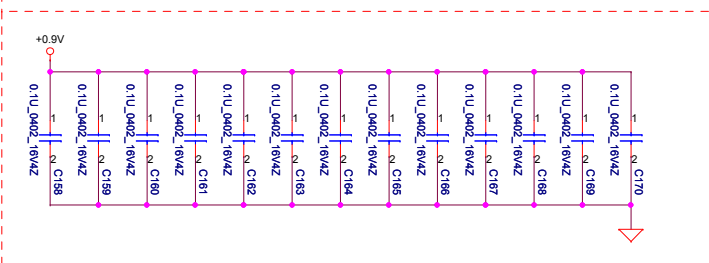
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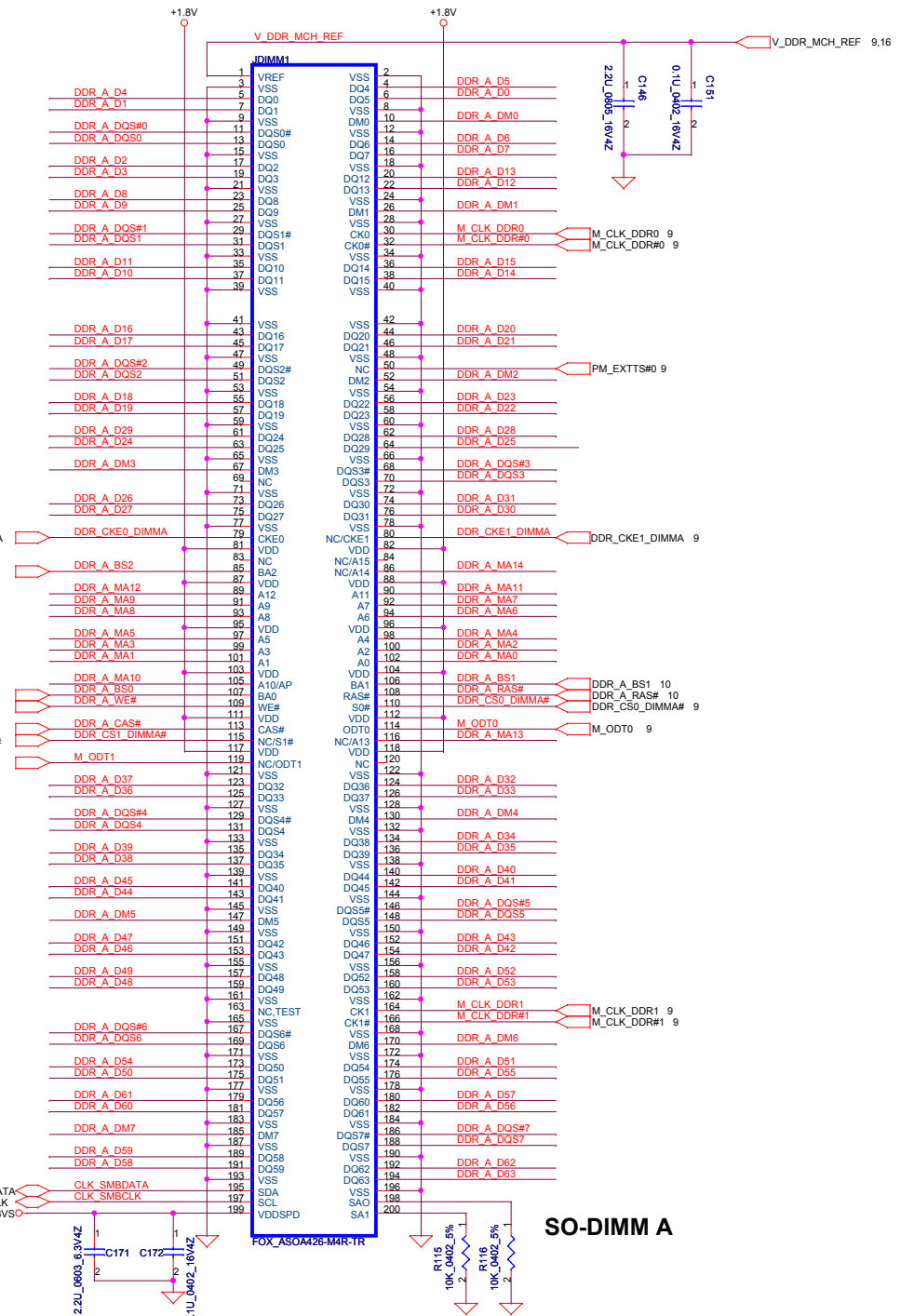
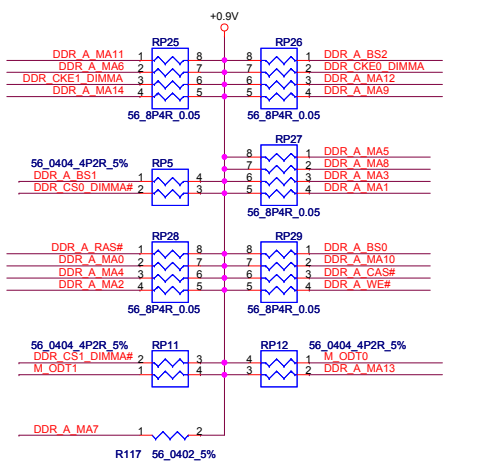
Layout Note:
Place near JP3



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

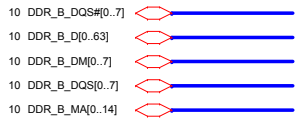


Layout Note:
Place these resistor closely JP3, all trace length Max=1.5"

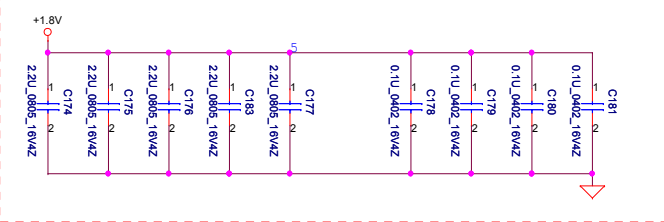


SO-DIMM A

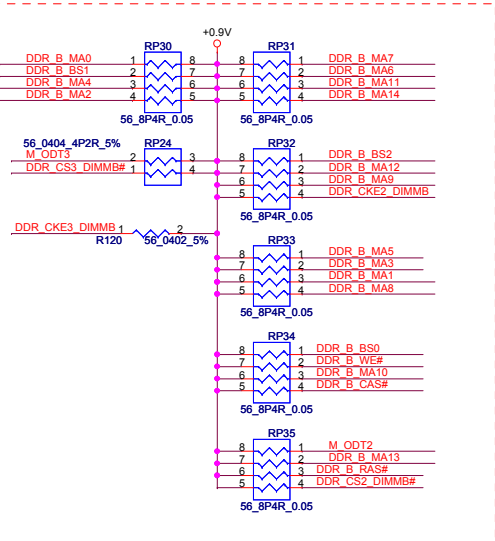
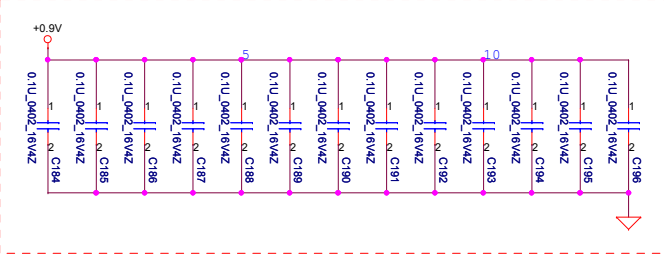
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Issued Date	2008/11/04	Deciphered Date	2008/11/04	Title	
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			Customer	L4-4731P Rhett discrete	0.1
			Date	Monday, February 16, 2009	Sheet 15 of 51



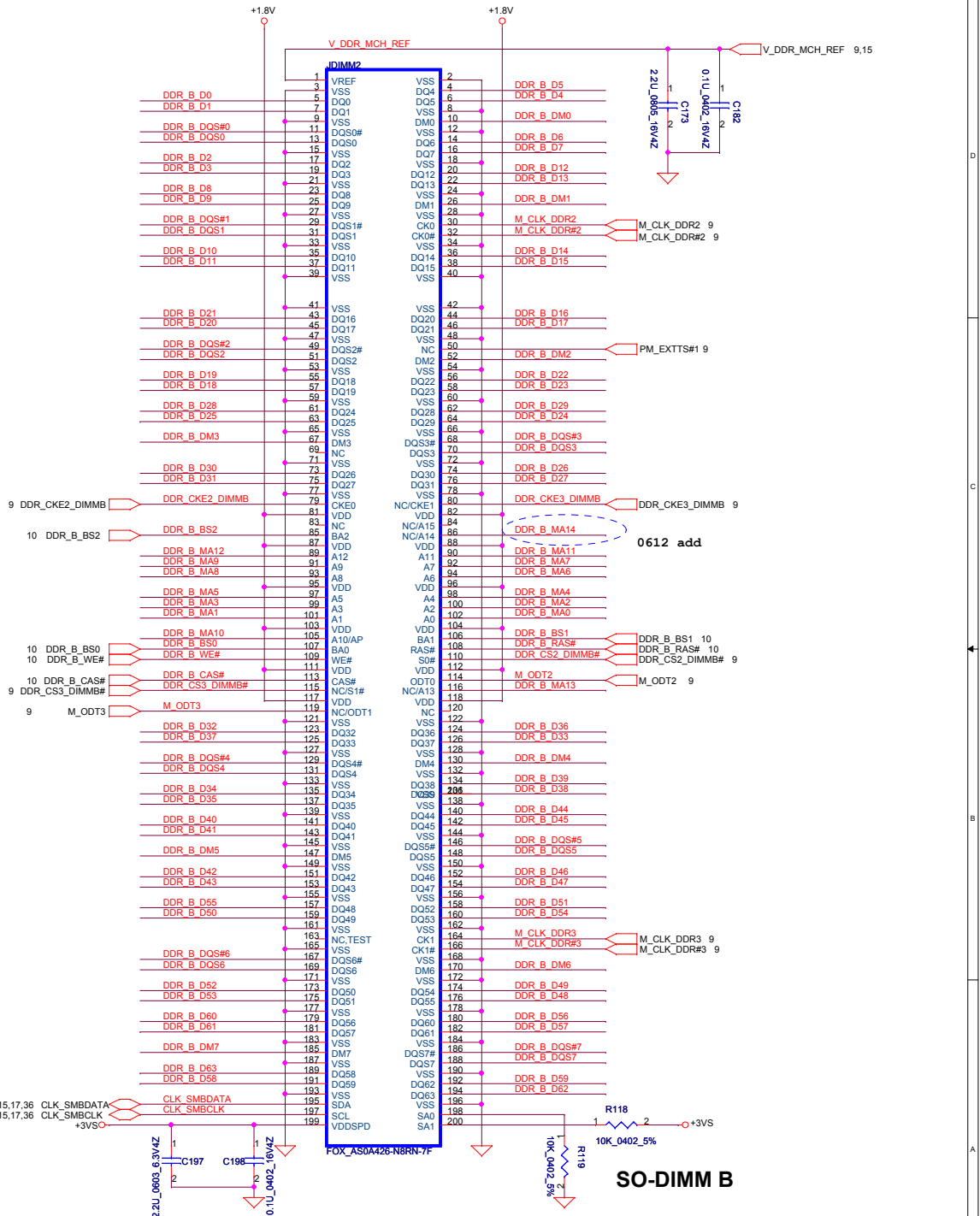
Layout Note:
Place near JP10



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



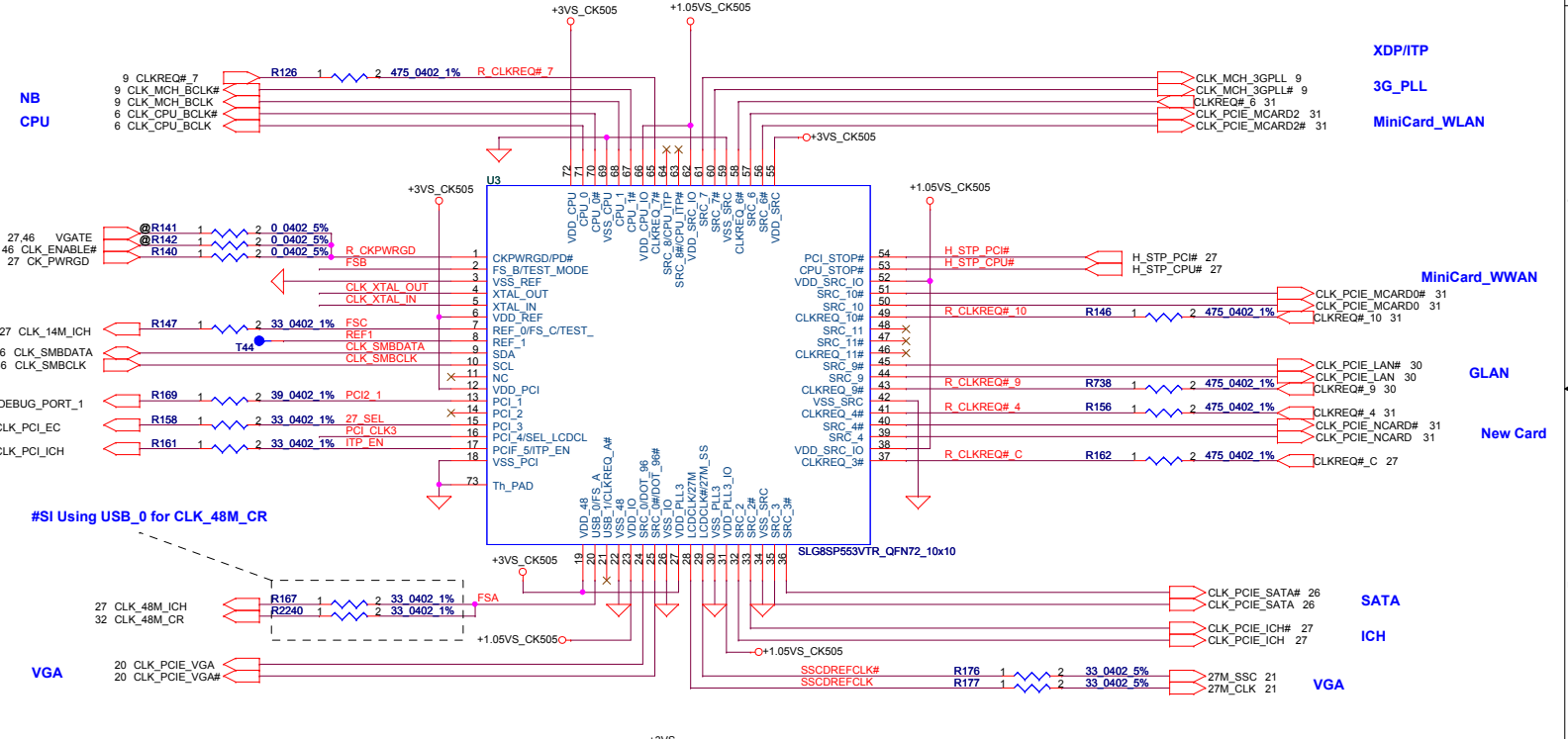
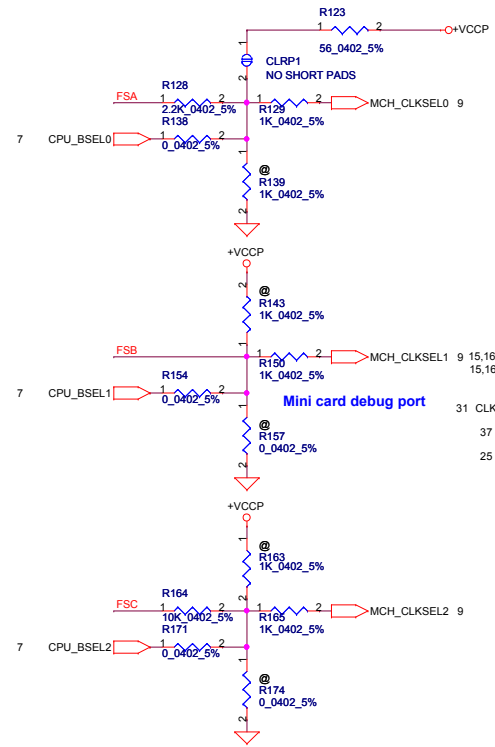
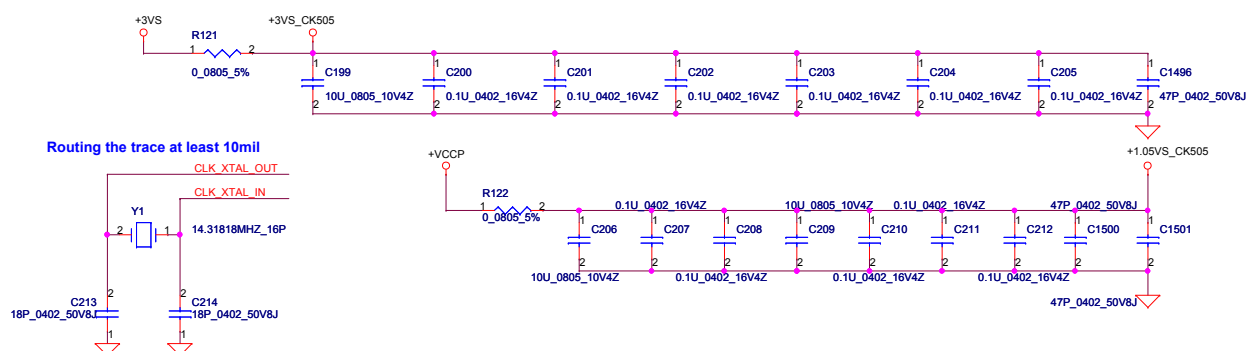
Layout Note:
Place these resistor closely JP3, all trace length Max=1.5"



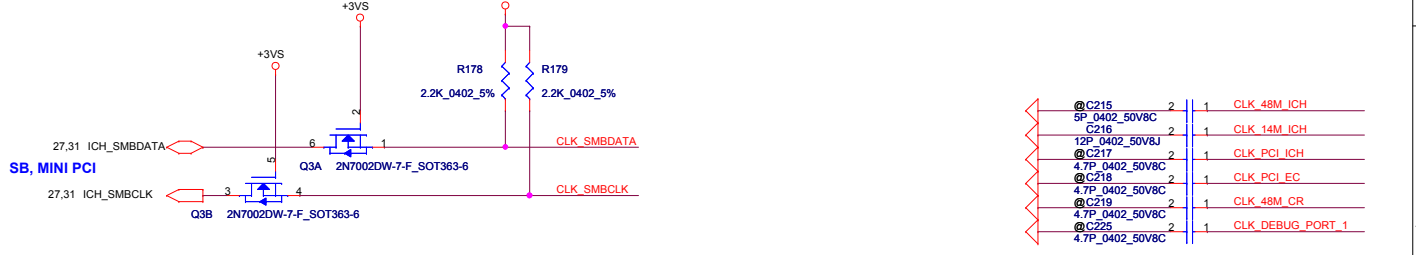
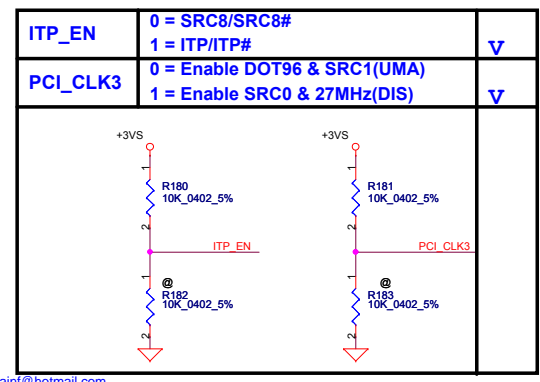
Security Classification		Compal Secret Data		Title	
Issued Date	2008/11/04	Deciphered Date	2008/11/04	Compal Electronics, Inc.	
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Date:	Monday, February 16, 2009	Sheet	16	of 51	

FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1						

Reserved



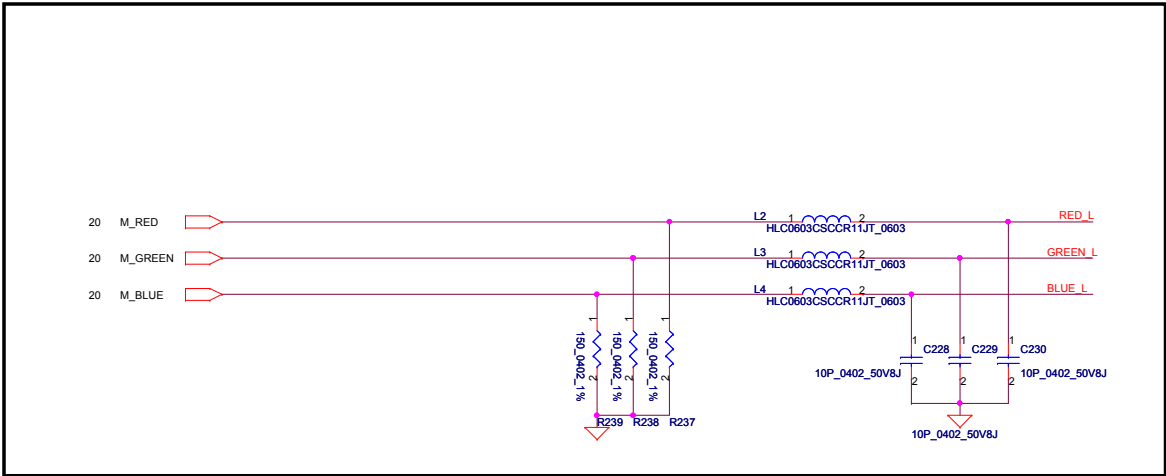
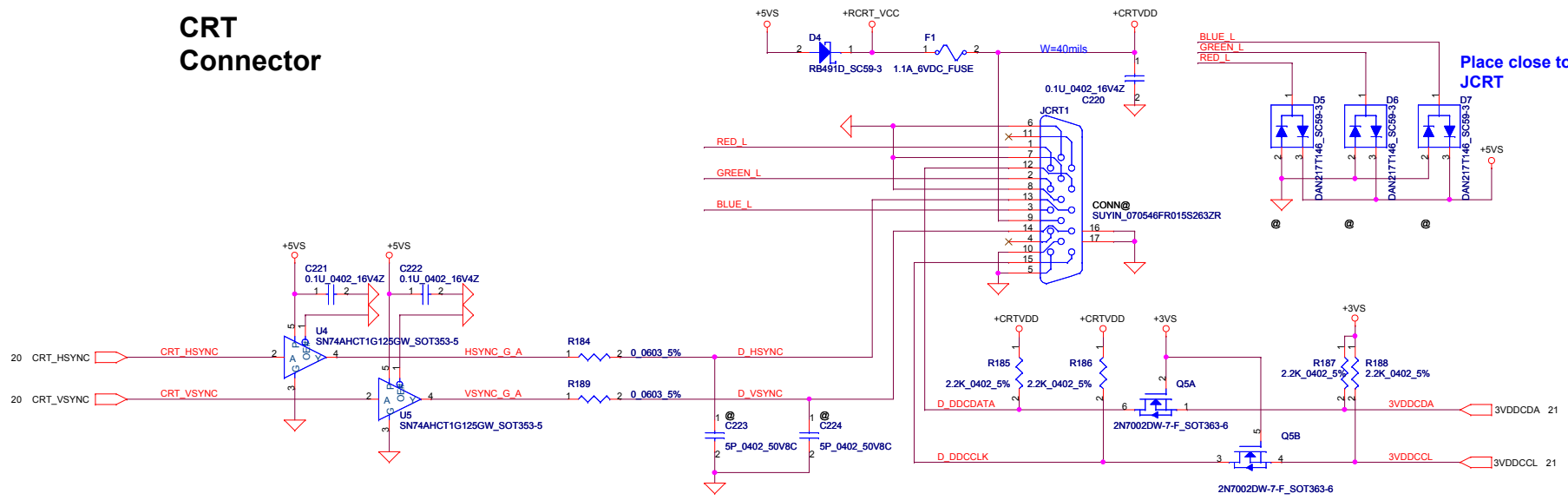
- XDP/ITP
- 3G_PLL
- MiniCard_WLAN
- MiniCard_WWAN
- GLAN
- New Card
- SATA
- ICH
- VGA



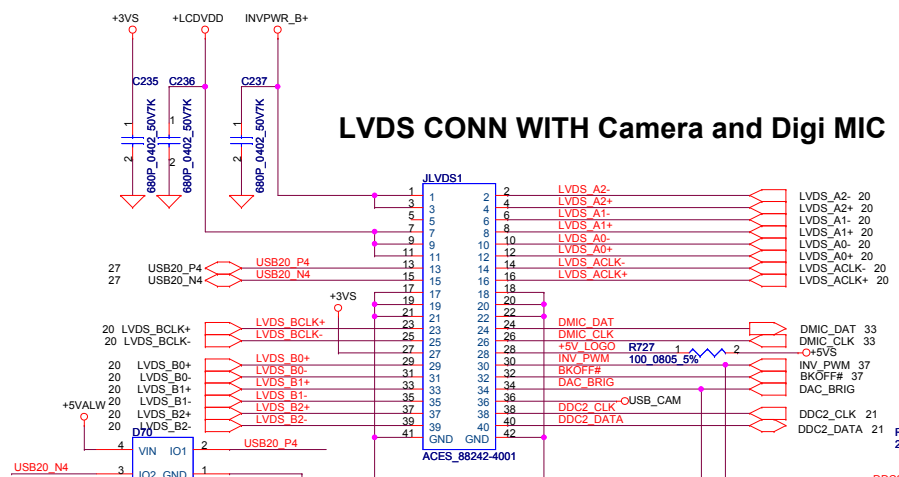
- @C215 5P_0402_50V8C 1 CLK_48M_ICH
- C216 2 1 CLK_14M_ICH
- @C217 12P_0402_50V8J 2 1 CLK_14M_ICH
- @C218 4.7P_0402_50V8C 2 1 CLK_PCI_EC
- @C219 4.7P_0402_50V8C 2 1 CLK_PCI_EC
- @C225 4.7P_0402_50V8C 2 1 CLK_DEBUG_PORT_1

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Size	Document Number	Date	Monday, February 16, 2009	Sheet	17 of 51
	LA-4731P Rhett discreate				Rev 0.1

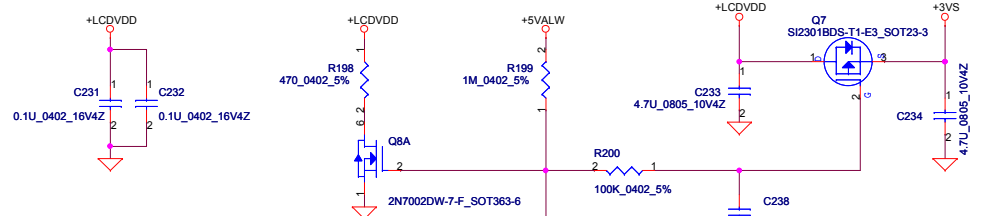
CRT Connector



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Size	Document Number	Date	Monday, February 16, 2009	Rev 0.1
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LVDS CONN WITH Camera and Digi MIC



Limited Current < 1A

21 ENAVDD

2N7002DW-7-F_SOT363-6

Q8B

R201 2.2K_0402_5%

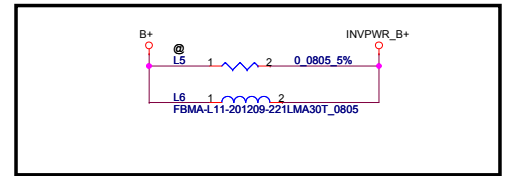
C239 0.22U_0603_10V7K

20 +5VALW

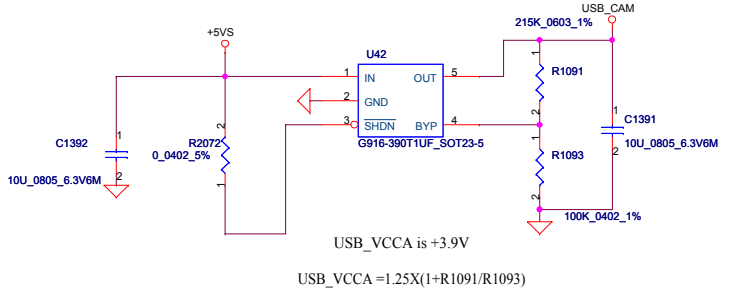
R200 100K_0402_5%

20 +3VS

Avoid Panel display garbage after power on.

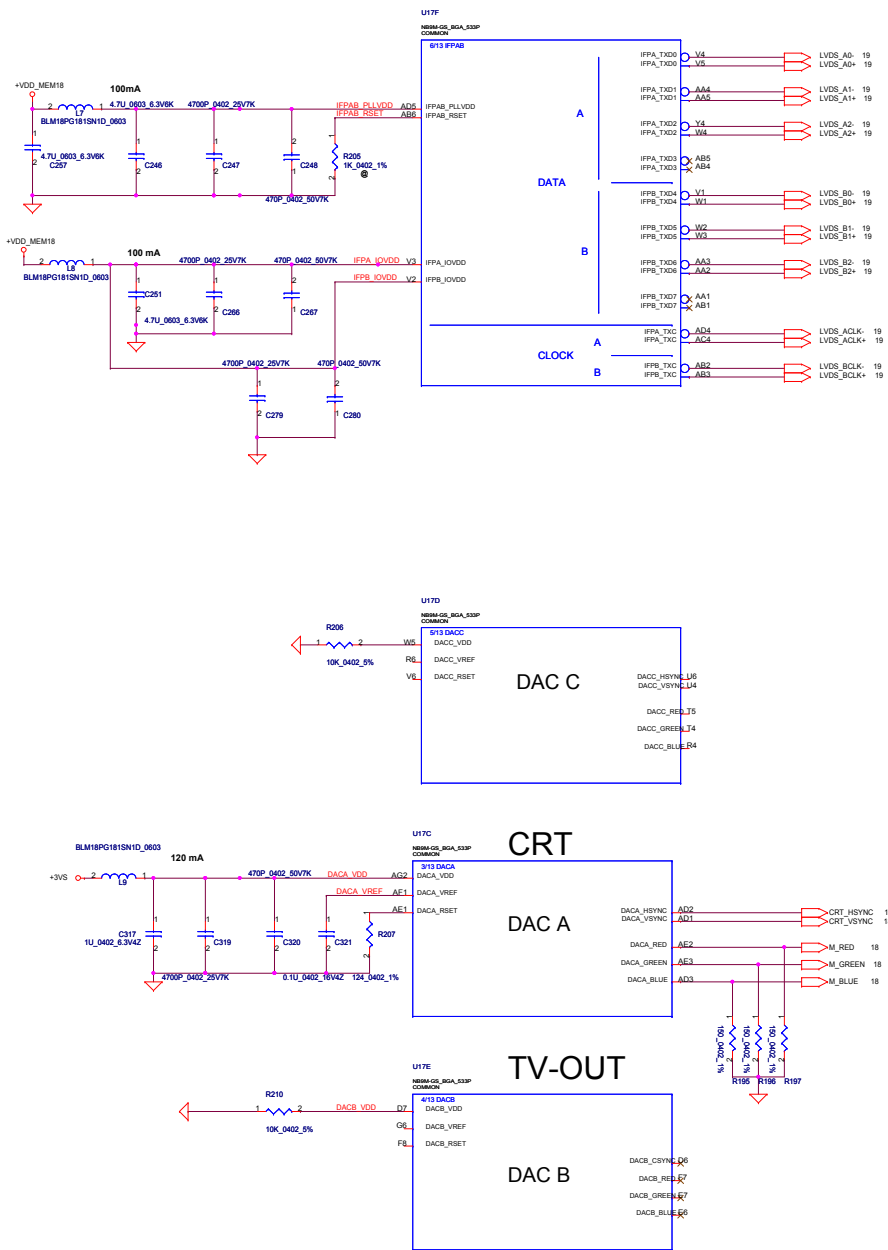


Blue Camera Power

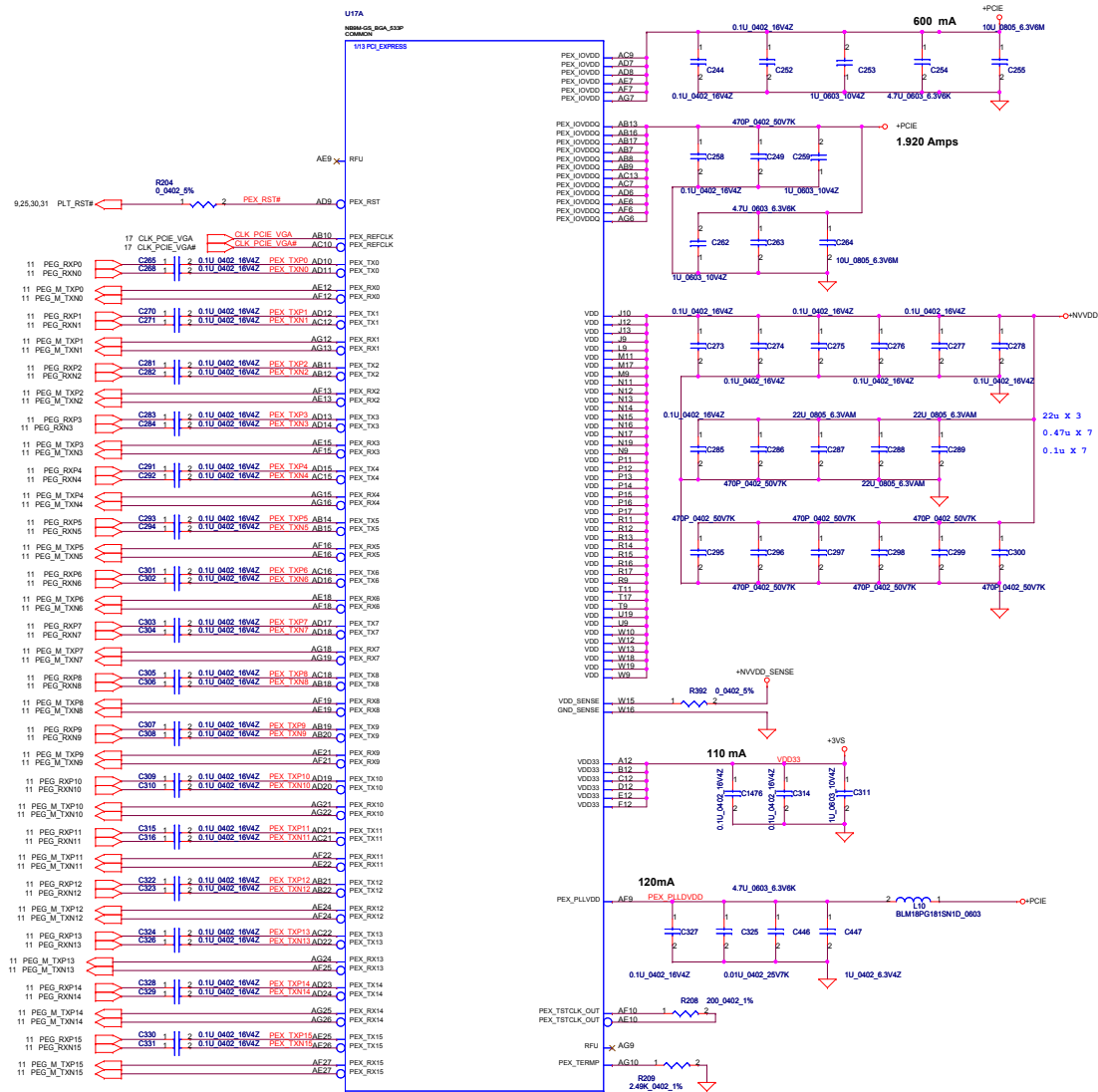


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Issued Date	2008/11/04	Deciphered Date	2008/11/04	LA-4731P <i>Rhetu discrete</i>
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Date:	Monday, February 16, 2009	Sheet	19	of 51

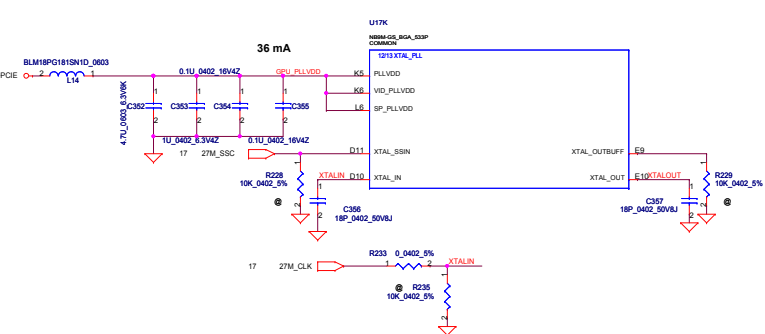
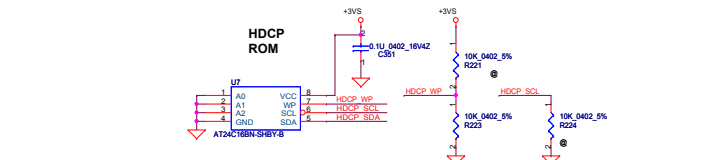
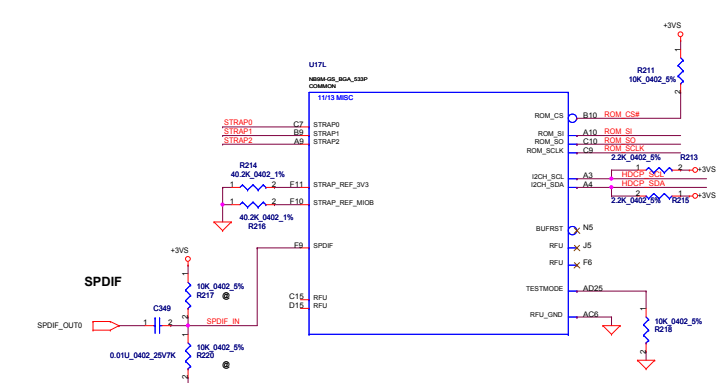
LVDS & DAC Interface



PEG Interface

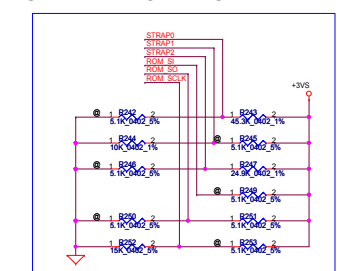


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2008/1/04		2008/1/04
Compal Electronics, Inc. PEG & LVDS & DAC		
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Size	Document Number	Rev
Custom	LA-4731P Rheti discrete	0.1
Date	Monday, February 18, 2009	Sheet 20 of 81



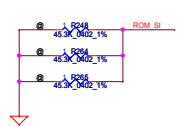
Straps

MULTI LEVEL STRAPS

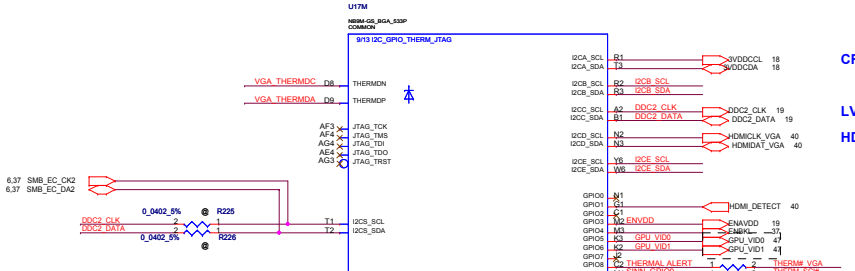
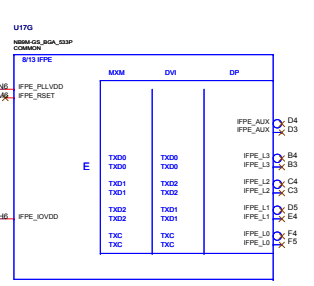
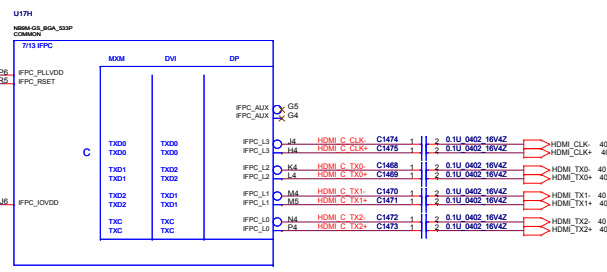
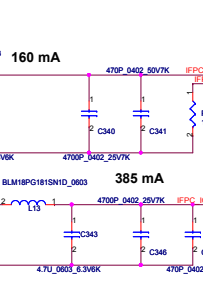
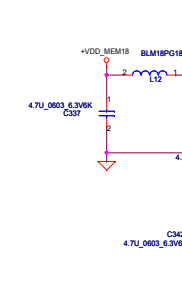
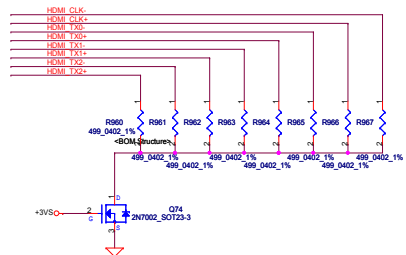


VRAM VENDOR STRAPS

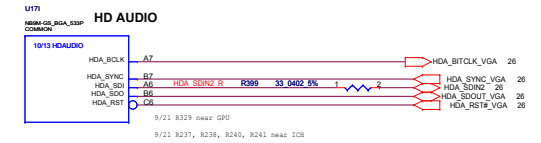
BAMX16 Hynix	R248	R254	R255
BAMX16 Micron	5 Kohms		
BAMX16 Samsung	15 Kohms		
BAMX16 Samsung	10 Kohms		



GPIO	I/O	ACTIVE	USAGE
GPIO0	IN	N/A	Primary DVI Hot-plug
GPIO1	IN	N/A	2nd DVI Hot-plug
GPIO2	OUT	H	Panel Back-Light PWM
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light Enable
GPIO5	OUT	N/A	NVDD VDD0
GPIO6	OUT	N/A	NVDD VID1
GPIO7	OUT	N/A	FBVDD VDD0
GPIO8	IN	L	Thermal Alert
GPIO9	OUT	L	FAN PWM
GPIO10	OUT	N/A	FBVref Select
GPIO11	OUT	N/A	SLI SYNCO
GPIO12	IN	N/A	AC Detect
GPIO13	OUT	L	PS Control or HDMI_CEC
GPIO14	OUT	H	PS Control



GPU_VID1	GPU_VID0	+NVDD
0	0	0.9V
0	1	1.09V
1	0	unused

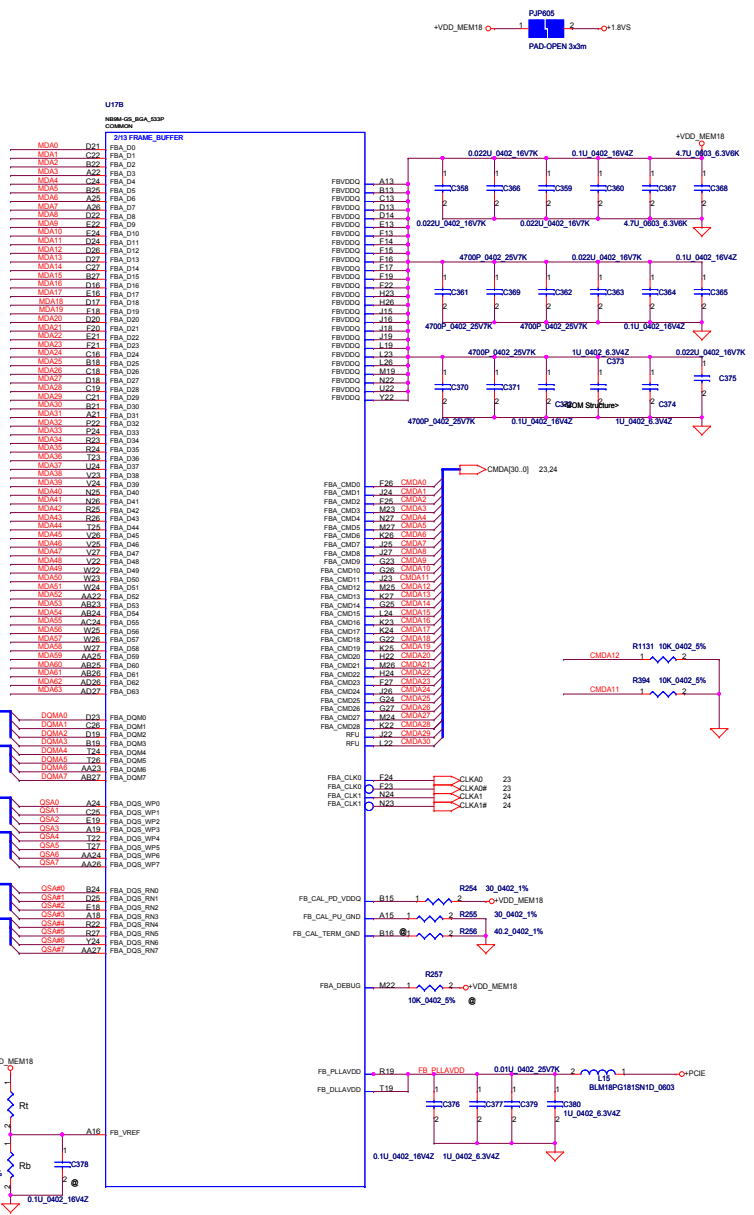


CRT
LVDS
HDMI

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Date	Monday, February 18, 2009	ISheet	21	of	51

VRAM Interface

- 23 MDA[15:0] ← MDA[15_0]
- 23 MDA[31:16] ← MDA[31_16]
- 24 MDA[47:32] ← MDA[47_32]
- 24 MDA[63:48] ← MDA[63_48]

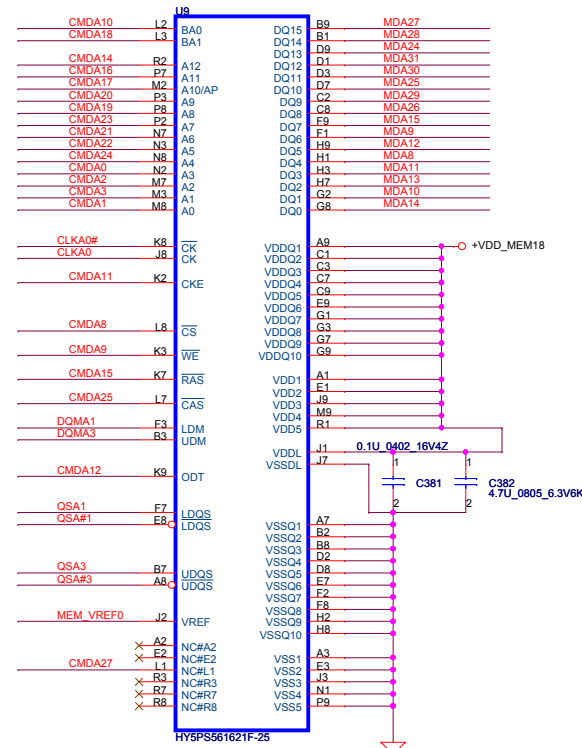
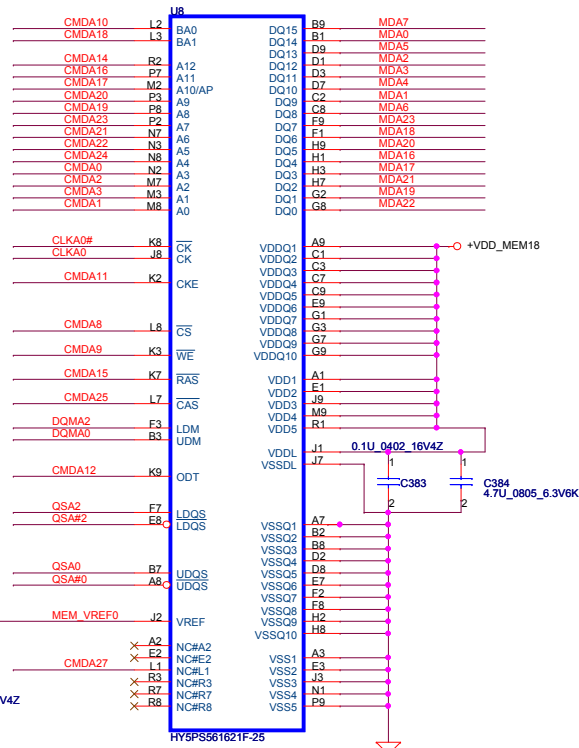
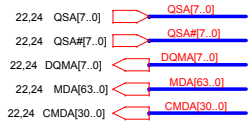


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Size	Document Number	Rev		
Custom	LA-4731P	Rhet discrete	0.1	
Date	Monday, February 18, 2009	Sheet	22	of 81

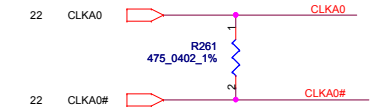
VRAM DDR2 chips (256MB & 512MB)

32Mx16 DDR2 400MHz *4==>256MB

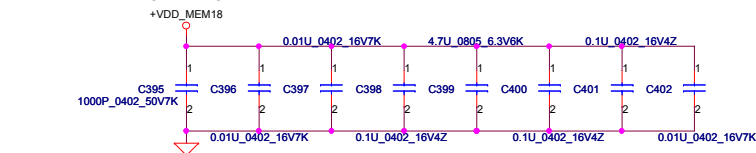
64Mx16 DDR2 400MHz*4==>512MB



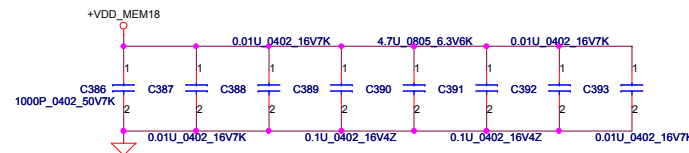
Address	DATA Bus	
	0..31	32..63
CMD0	A3	
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		



DDR2 BGA MEMORY



DDR BGA MEMORY

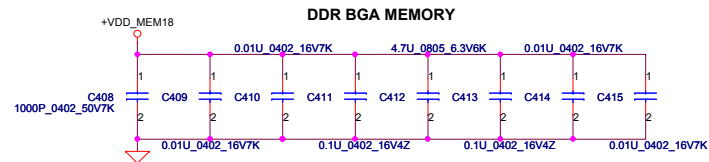
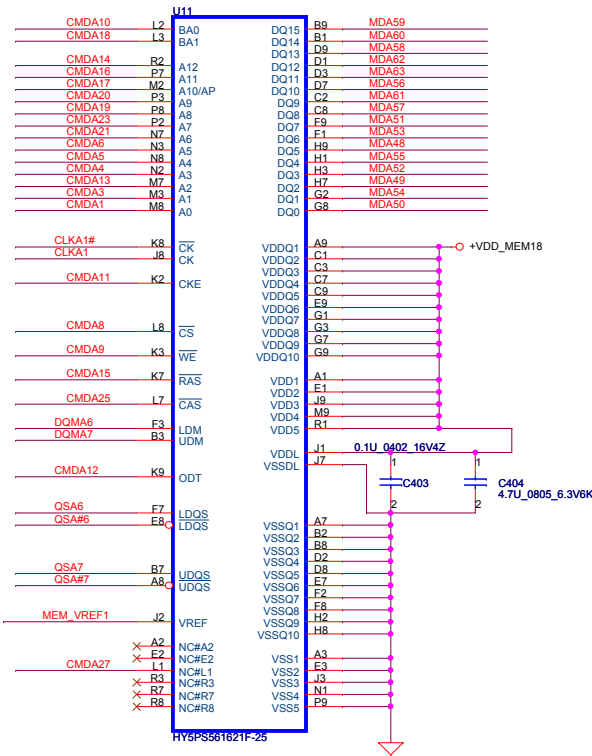
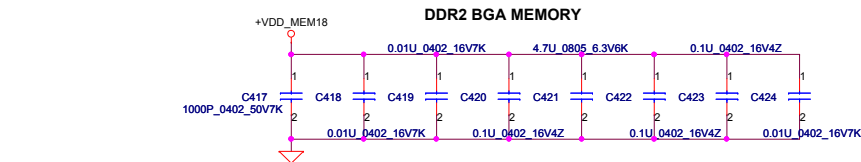
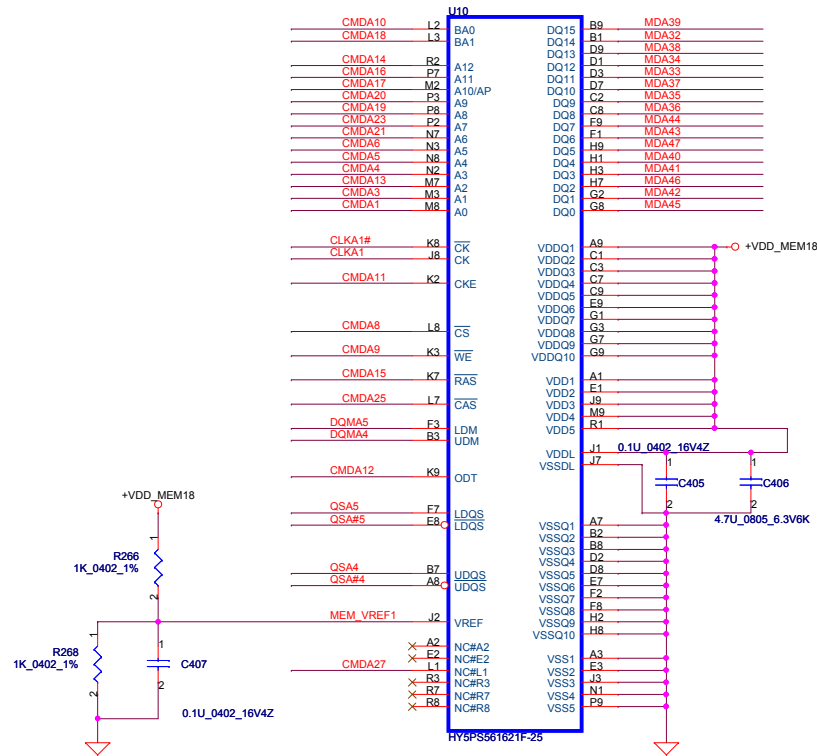
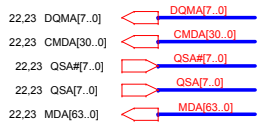


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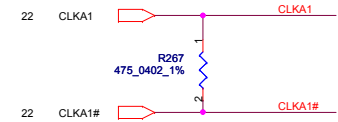
VRAM DDR2 chips (256MB & 512MB)

32Mx16 DDR2 400MHz *4==>256MB

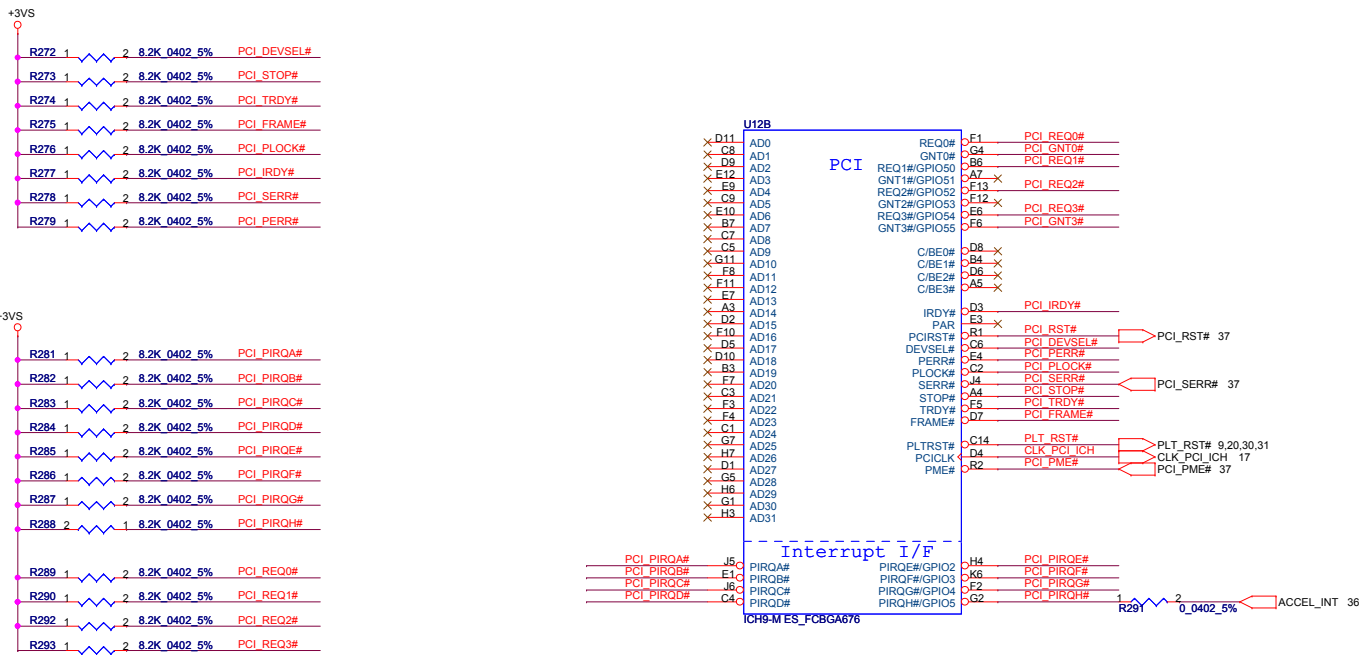
64Mx16 DDR2 400MHz*4==>512MB



	DATA Bus	
Address	0..31	32..63
CMD0	A3	
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		

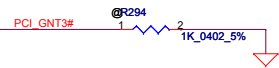


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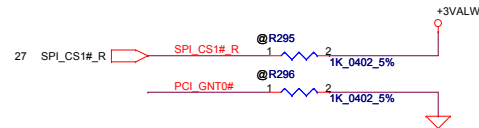
A16 swap override Strap

PCI_GNT3# Low= A16 swap override Enable
High= Default *

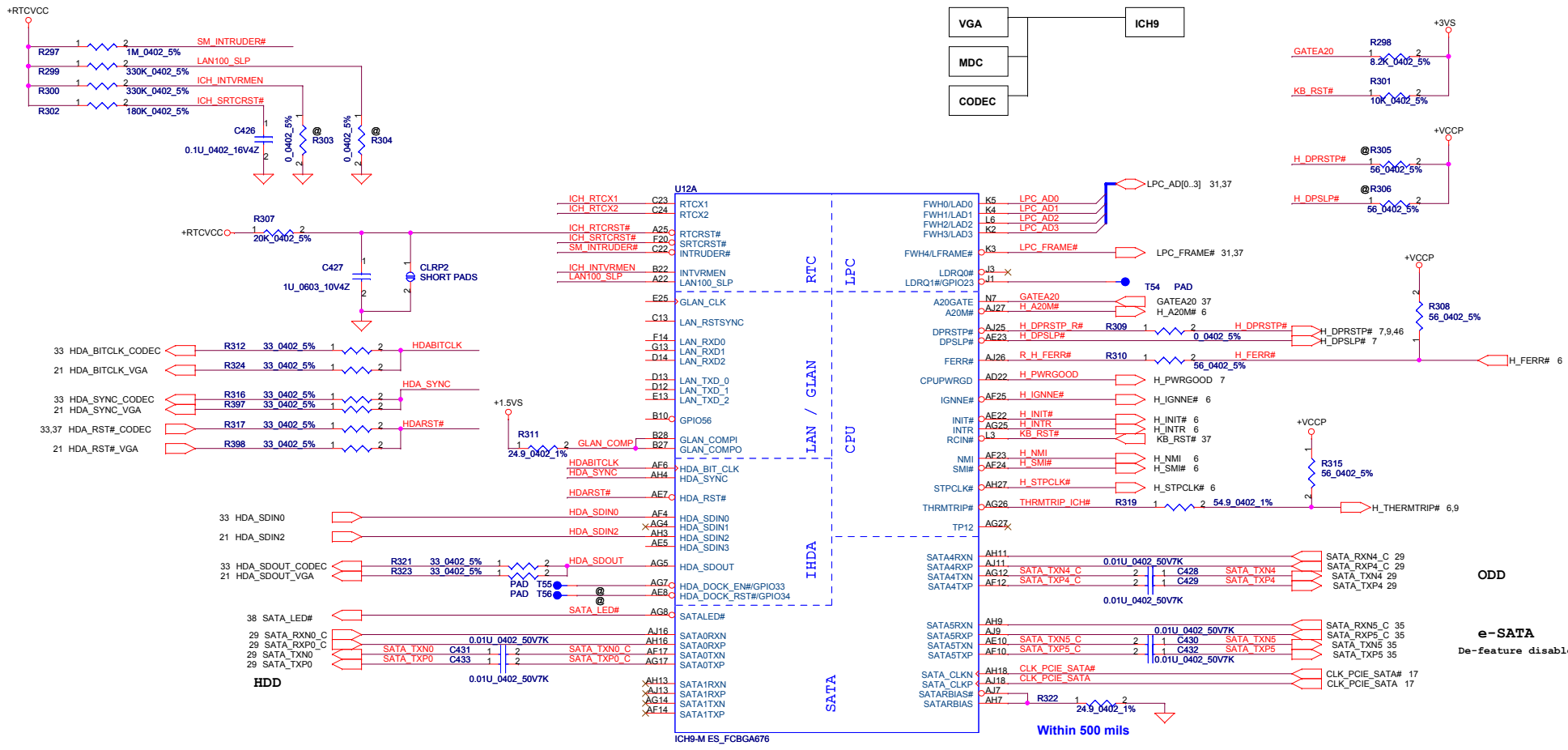


Boot BIOS Strap

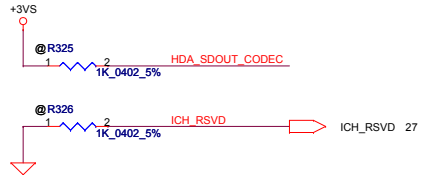
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1	0	PCI
1	1	LPC *



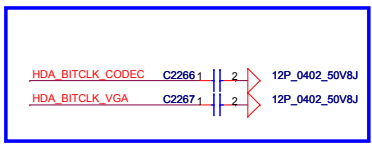
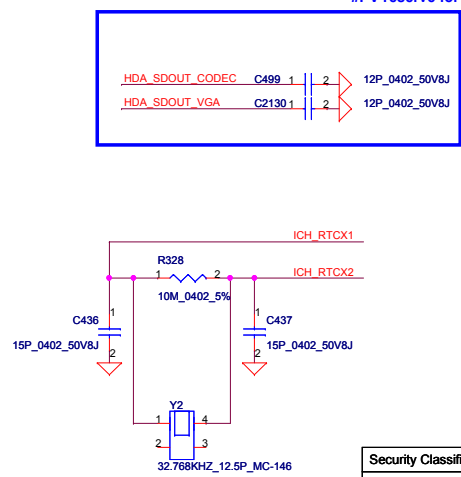
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		Sheet	25	of 51



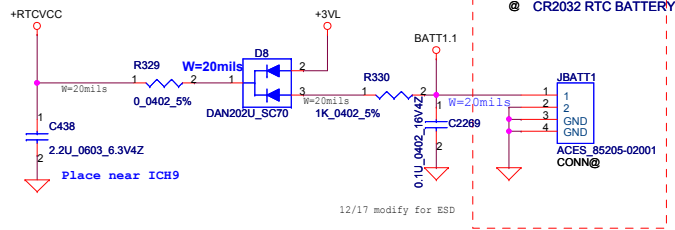
XOR CHAIN ENTRANCE STRAP:RSVD



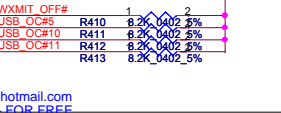
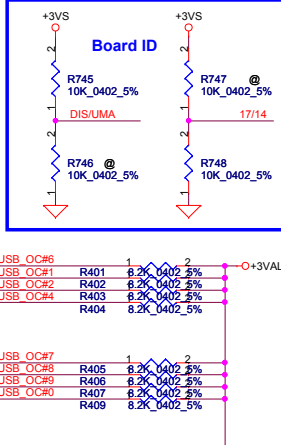
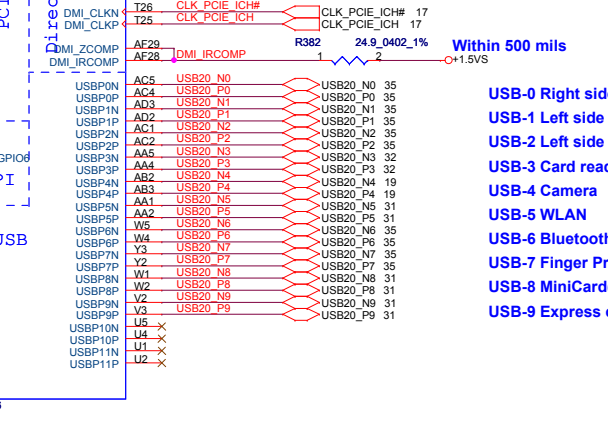
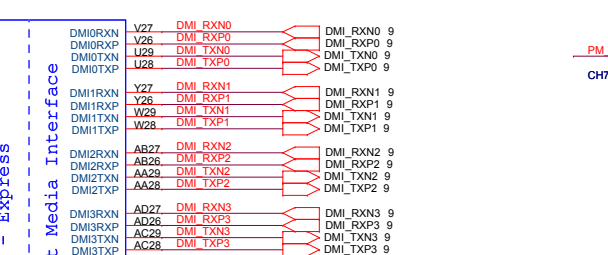
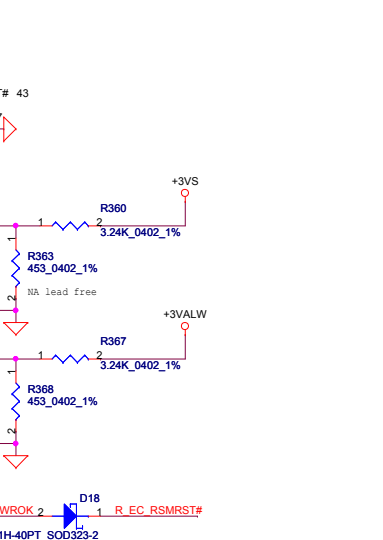
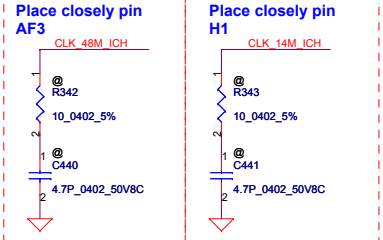
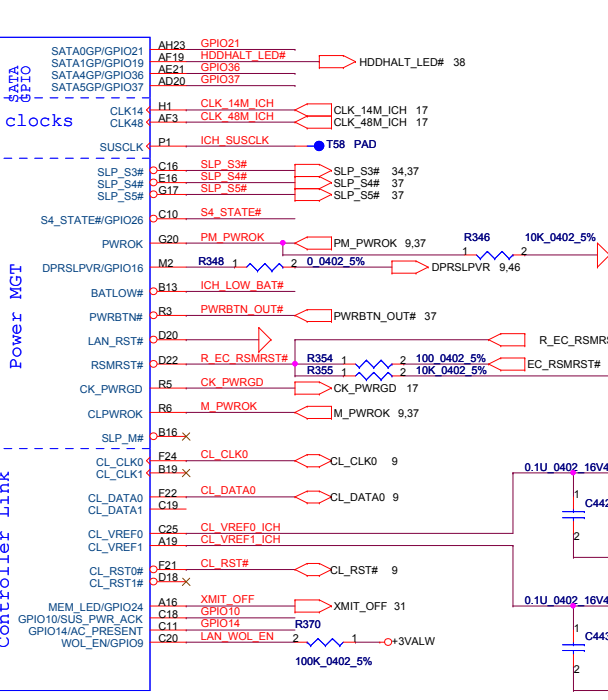
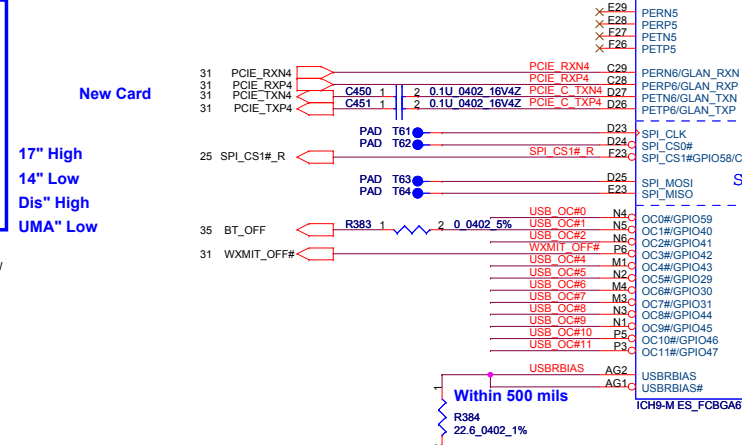
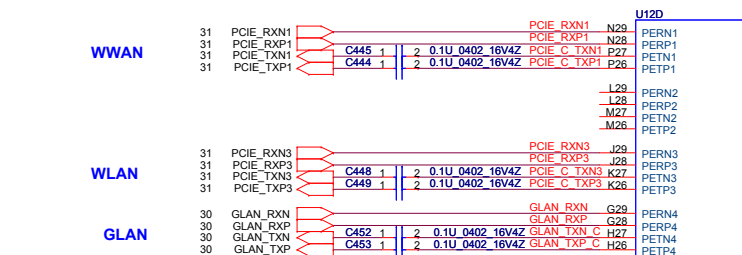
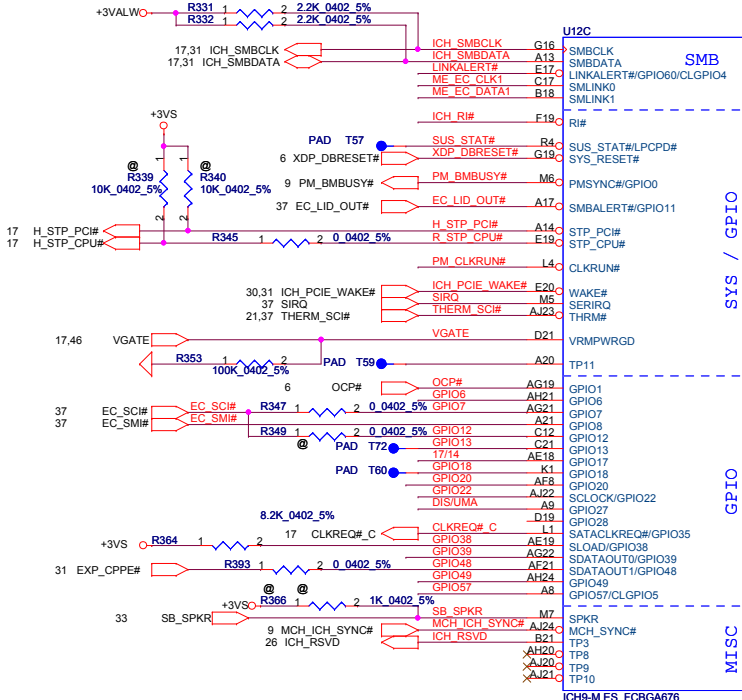
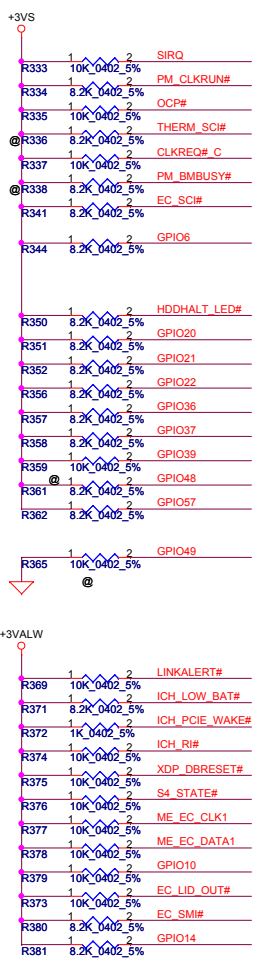
ICH_RSVD	HDA_SDOUT_CODEC	
0	0	
0	1	
1	0	
1	1	



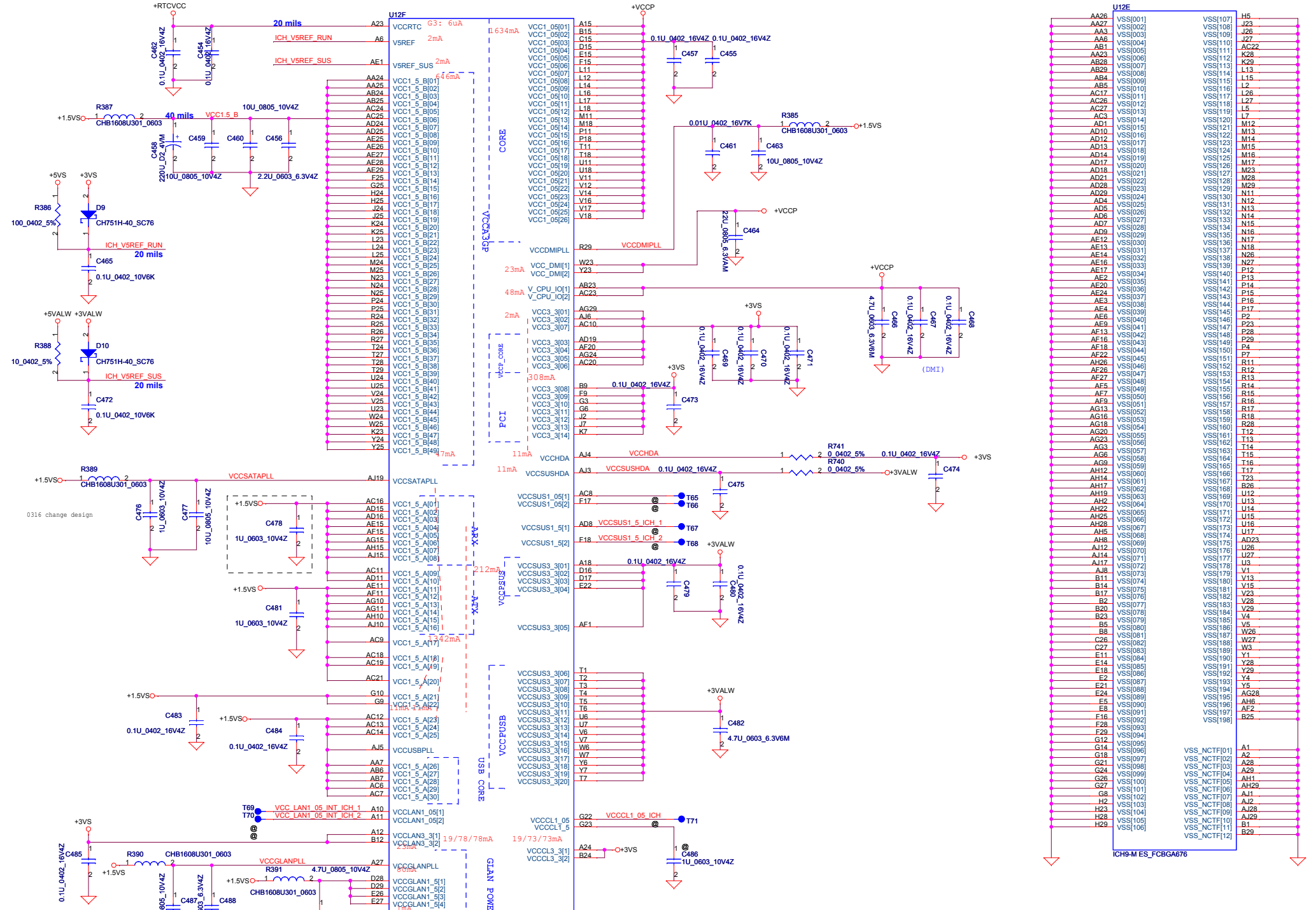
12/12 MODIFY



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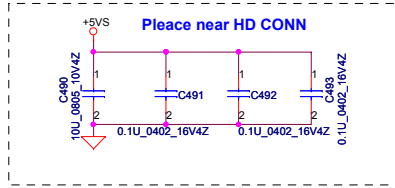
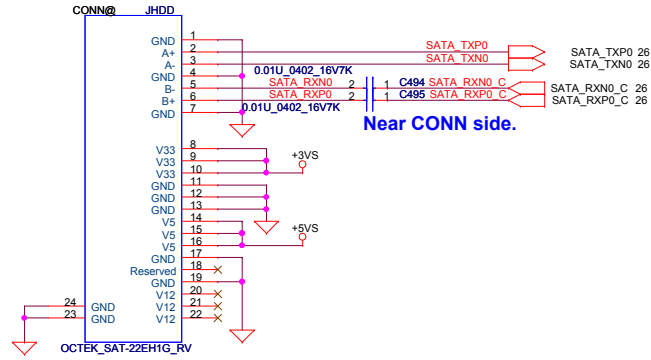
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Issued Date	2008/11/04	Deciphered Date	2008/11/04	Compal Electronics, Inc.	
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Size	Document Number	Title		Rev	
Customer	L4-4731P	Rhetu discrete		0.1	
Date:	Monday, February 16, 2009	Sheet	27	of	51



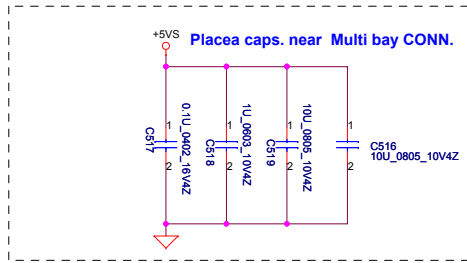
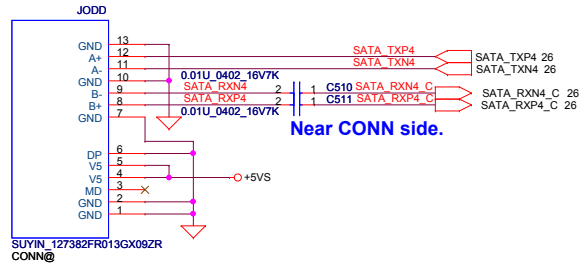
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Size		ICH9(4/4) POWER&GND	
Document Number	Customer	Rev	
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Date:	Thursday, February 12, 2009	Sheet	28 of 51

HDD Connector



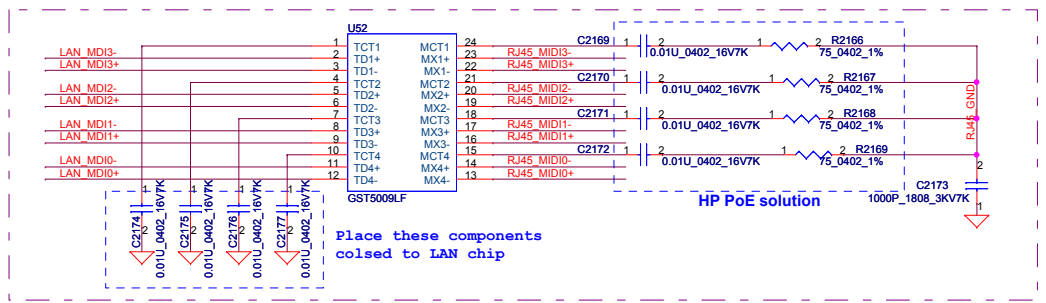
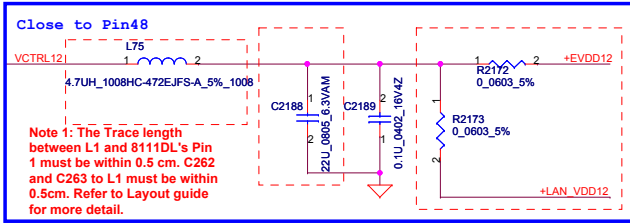
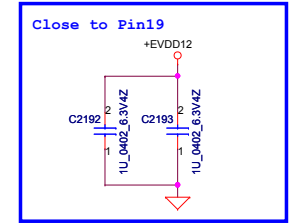
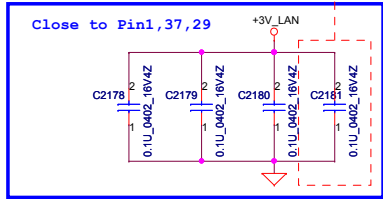
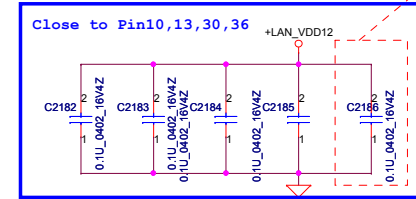
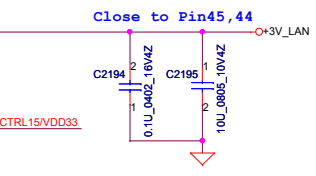
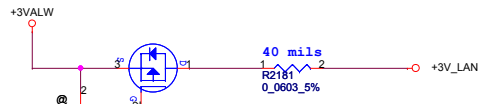
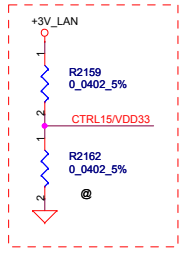
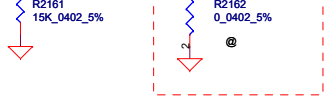
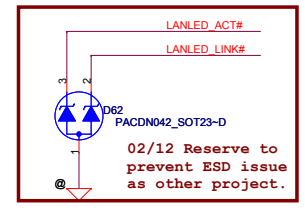
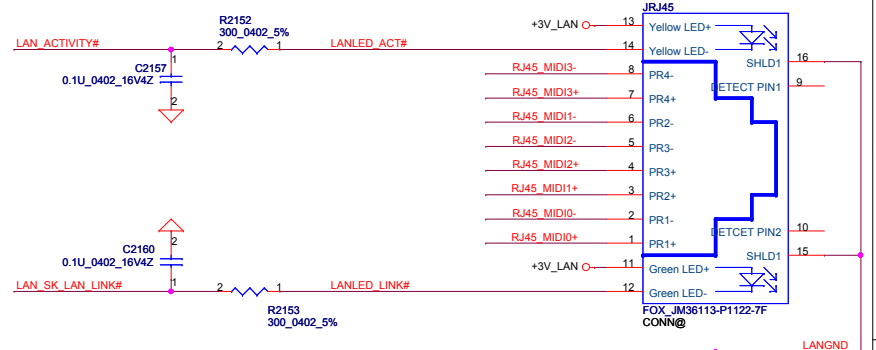
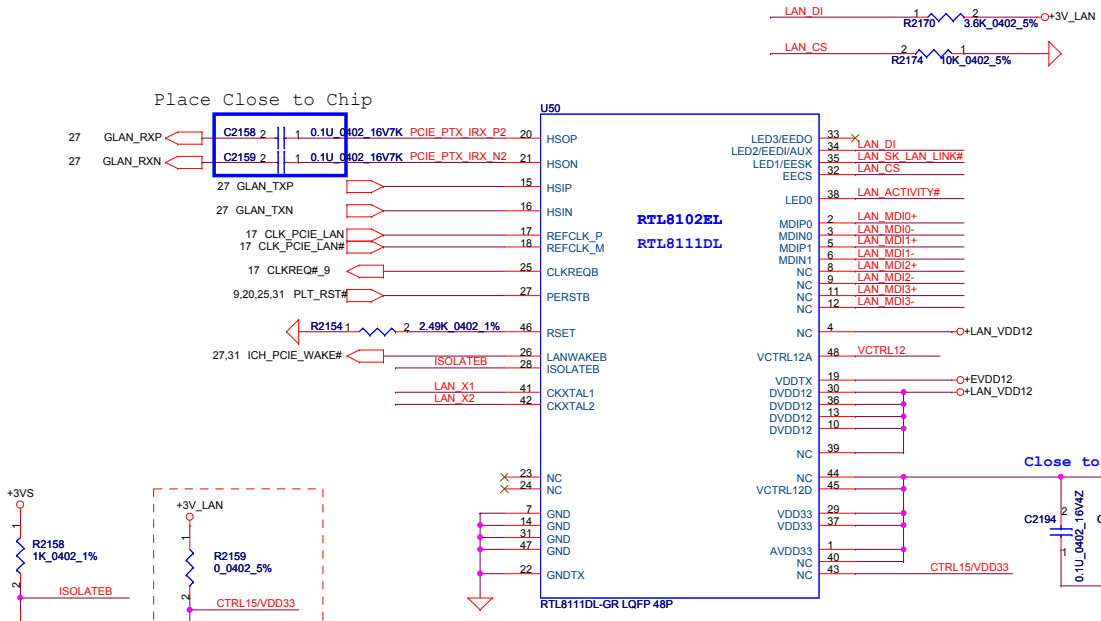
CD-ROM Connector



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Date: Monday, February 16, 2009			Sheet	29 of 51

LAN Conn.

Place Close to Chip



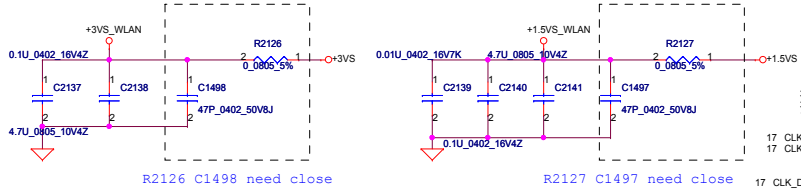
Place these components close to LAN chip

Note 1: The Trace length between L1 and 8111DL's Pin 1 must be within 0.5 cm. C262 and C263 to L1 must be within 0.5cm. Refer to Layout guide for more detail.

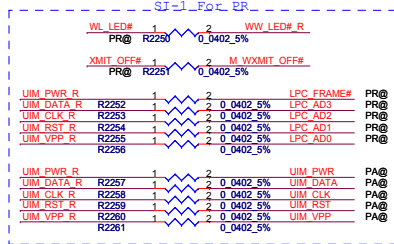
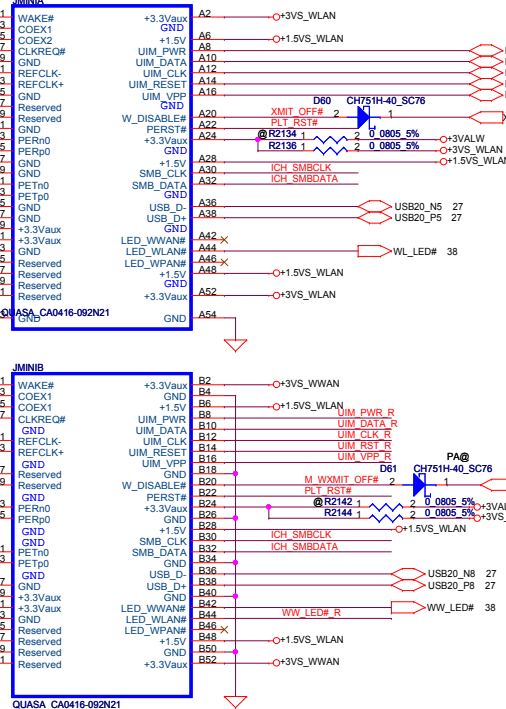
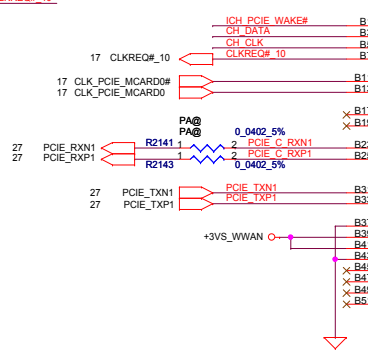
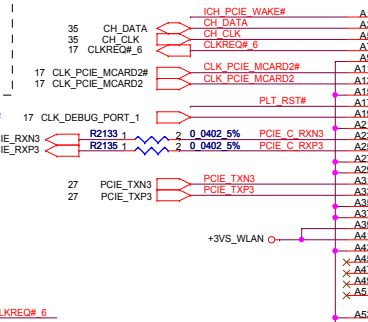
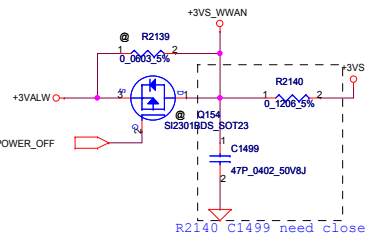
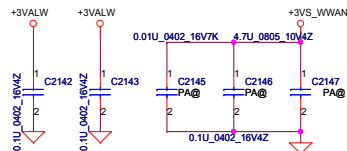
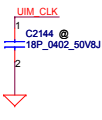
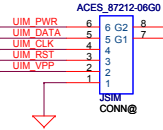
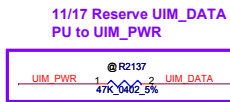
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Compal Electronics, Inc.		
Title		
Realtek 8111DL Giga_LAN		
Size	Document Number	Rev
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Mini Card Slot ---WLAN,WWAN

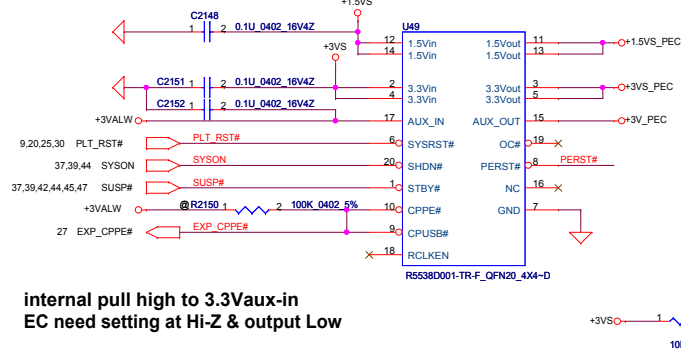


SIM card Connector

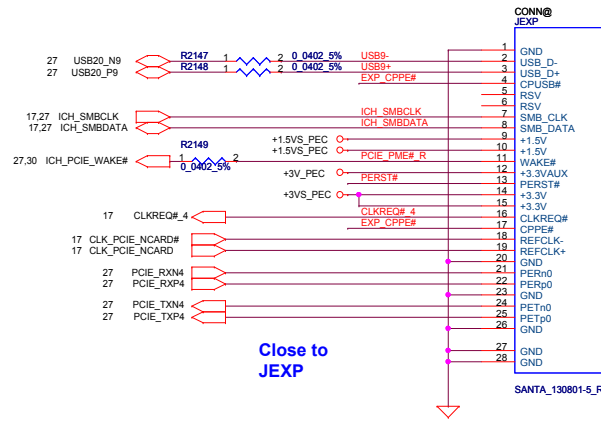
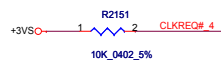


New Card

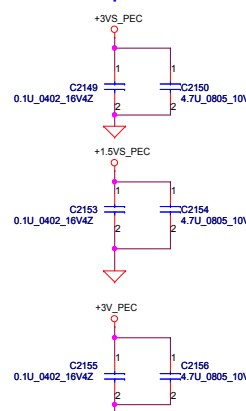
Express Card Power Switch



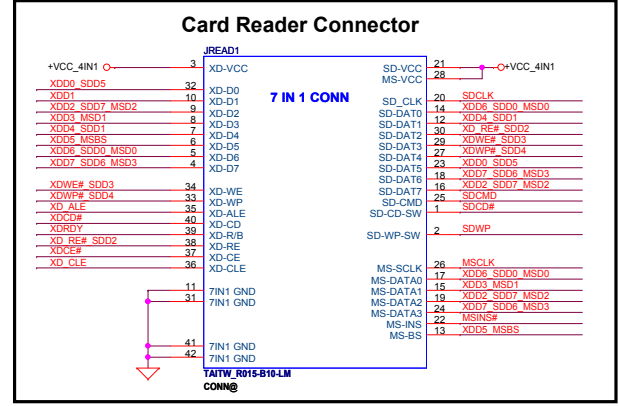
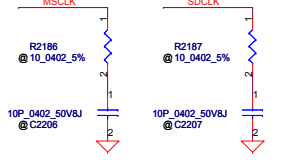
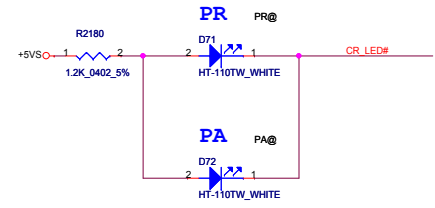
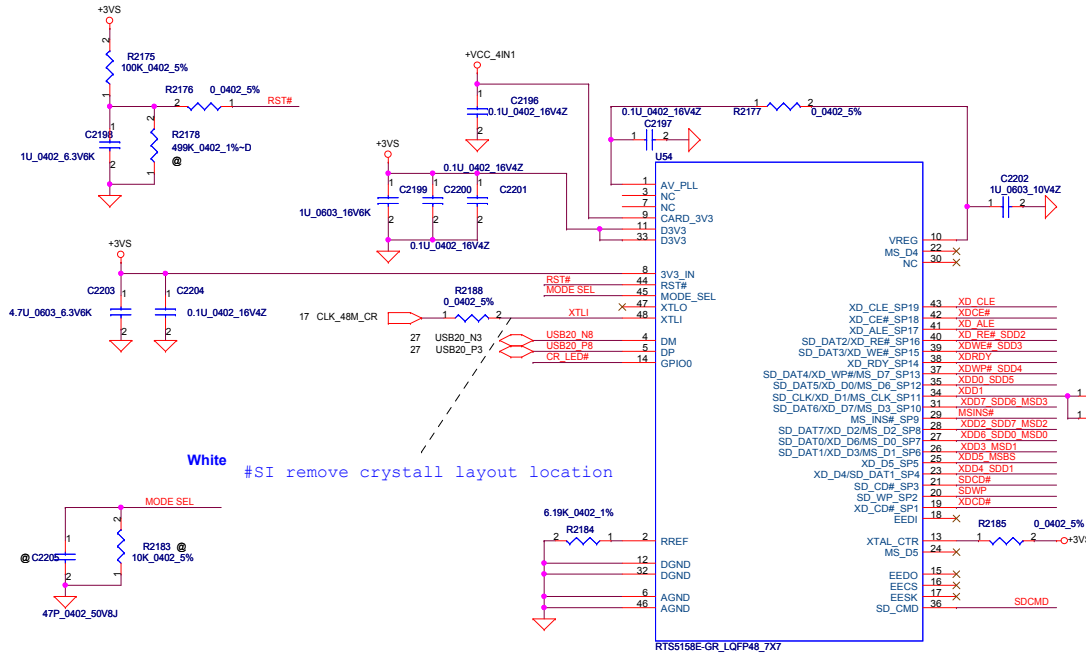
internal pull high to 3.3Vaux-in
EC need setting at Hi-Z & output Low



Near to Express Card slot.



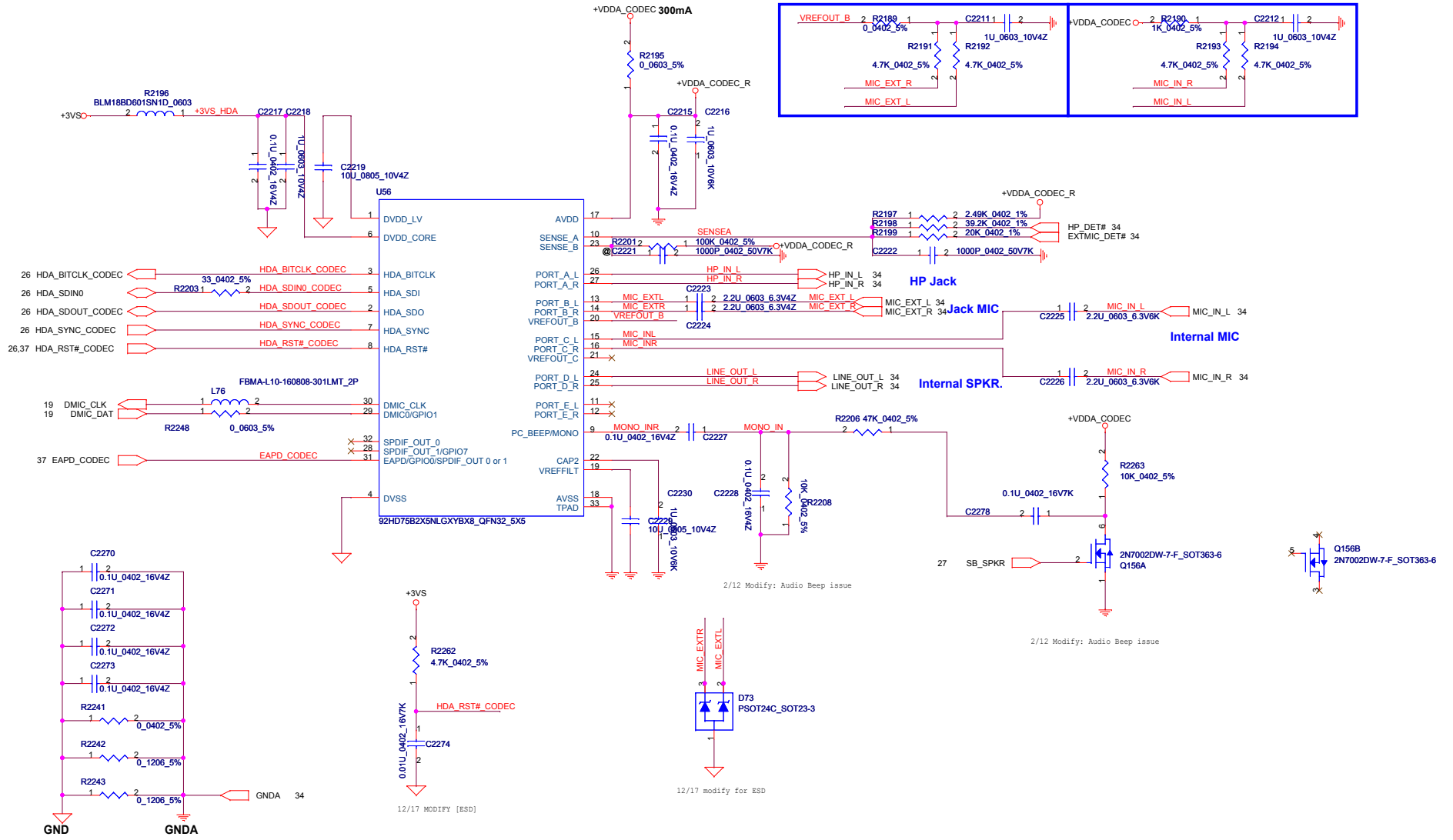
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Issued Date	2008/11/04	Deciphered Date	2008/11/04	Title
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					Document Number LA-4731P Rhett discrete
					Rev 0.1
					Date: Monday, February 16, 2009
					Sheet 32 of 51

CODEC POWER

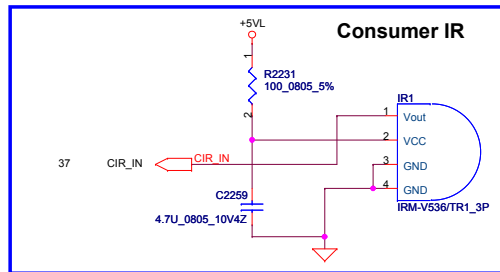
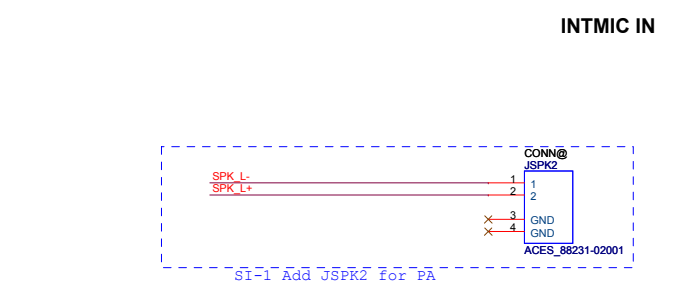
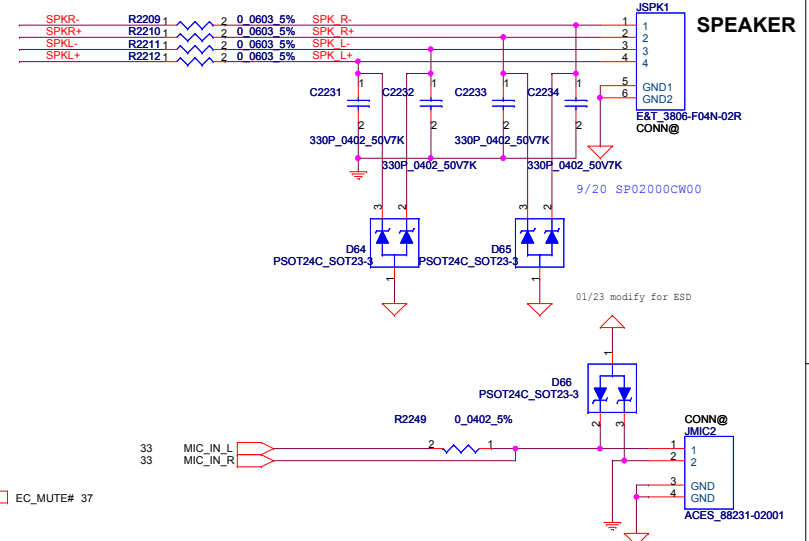
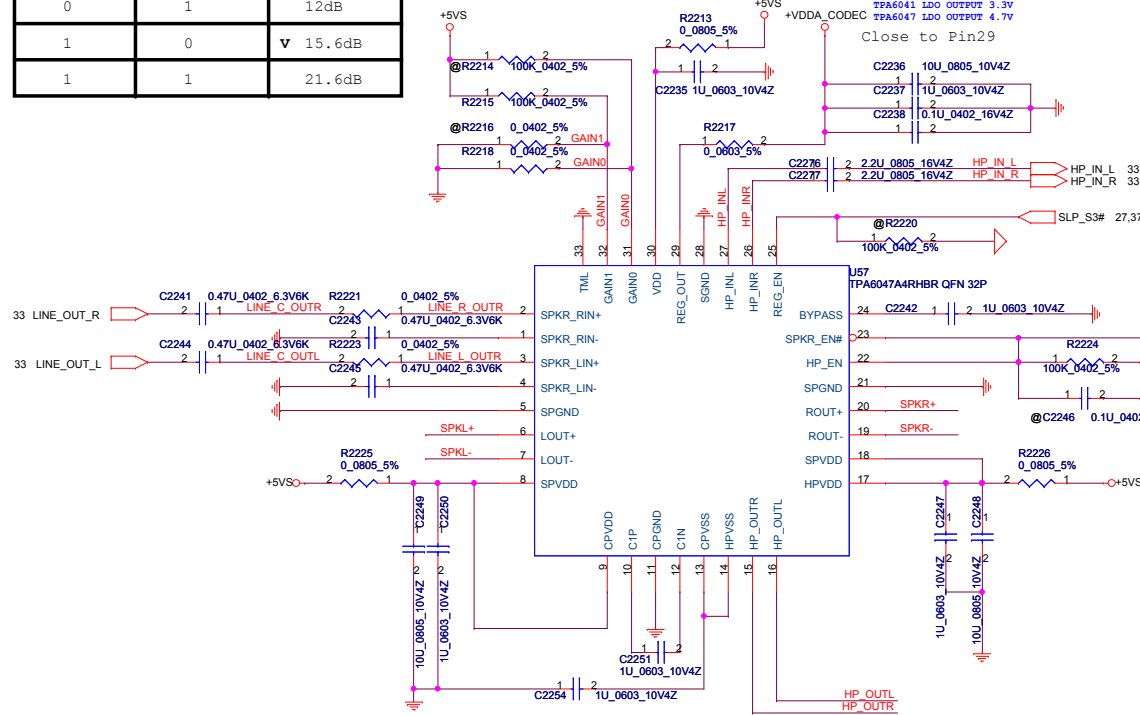
(4.75V(4.56~4.94V))



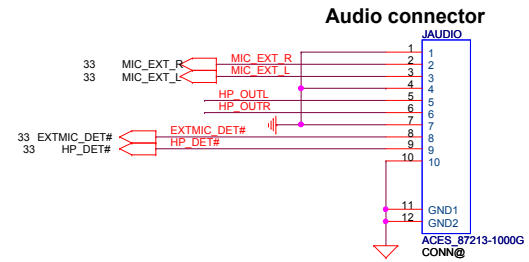
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AMP. FOR INTERNAL SPEAKER

GAIN1	GAIN0	Av (inv)
0	0	10dB
0	1	12dB
1	0	15.6dB
1	1	21.6dB

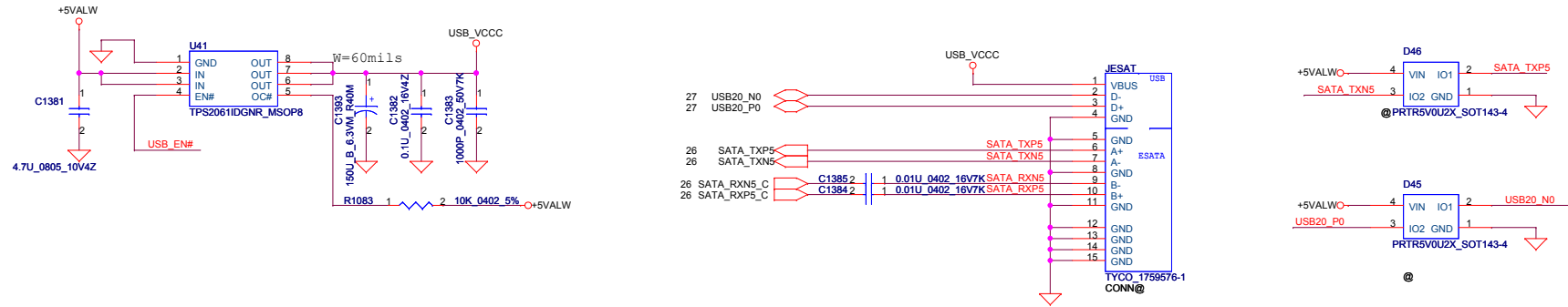


SI-1 Add Audio board connector

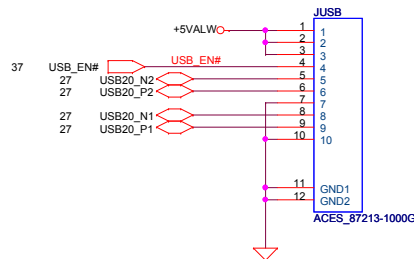


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				Custom	LA-4731P Rhett discrete
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				Rev	0.1

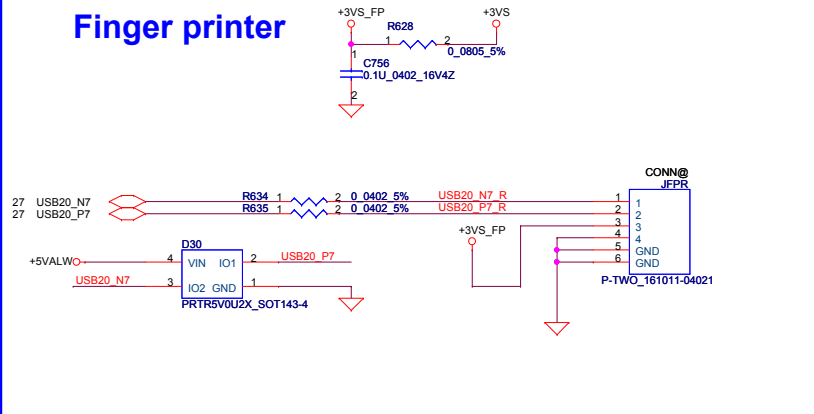
Right side ESATA/USB combination Connector



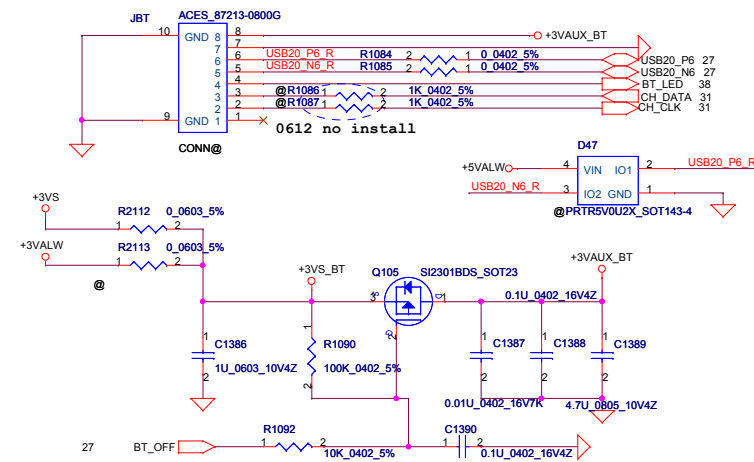
USB cable connector for Right side



Finger printer

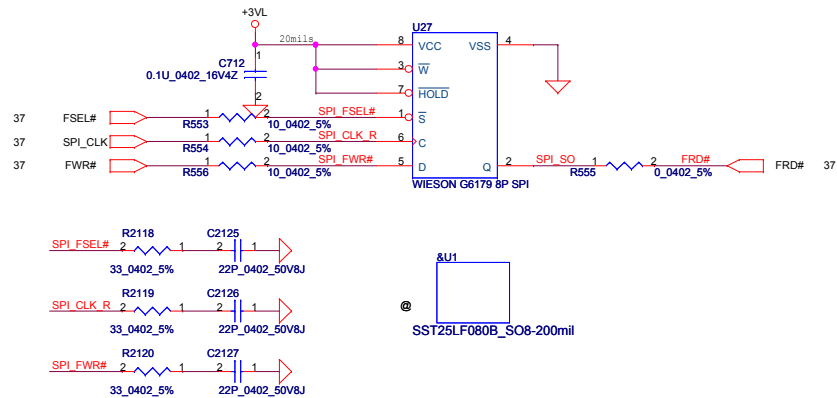


BT Connector

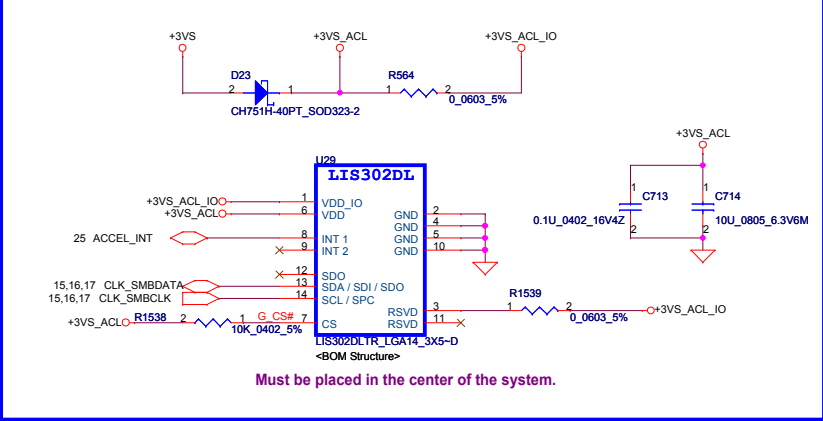


Security Classification		Compal Secret Data		Title	
Issued Date	2008/11/04	Deciphered Date	2008/11/04	USB, BT, eSATA	
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Date: Monday, February 16, 2009				Sheet 35 of 51	

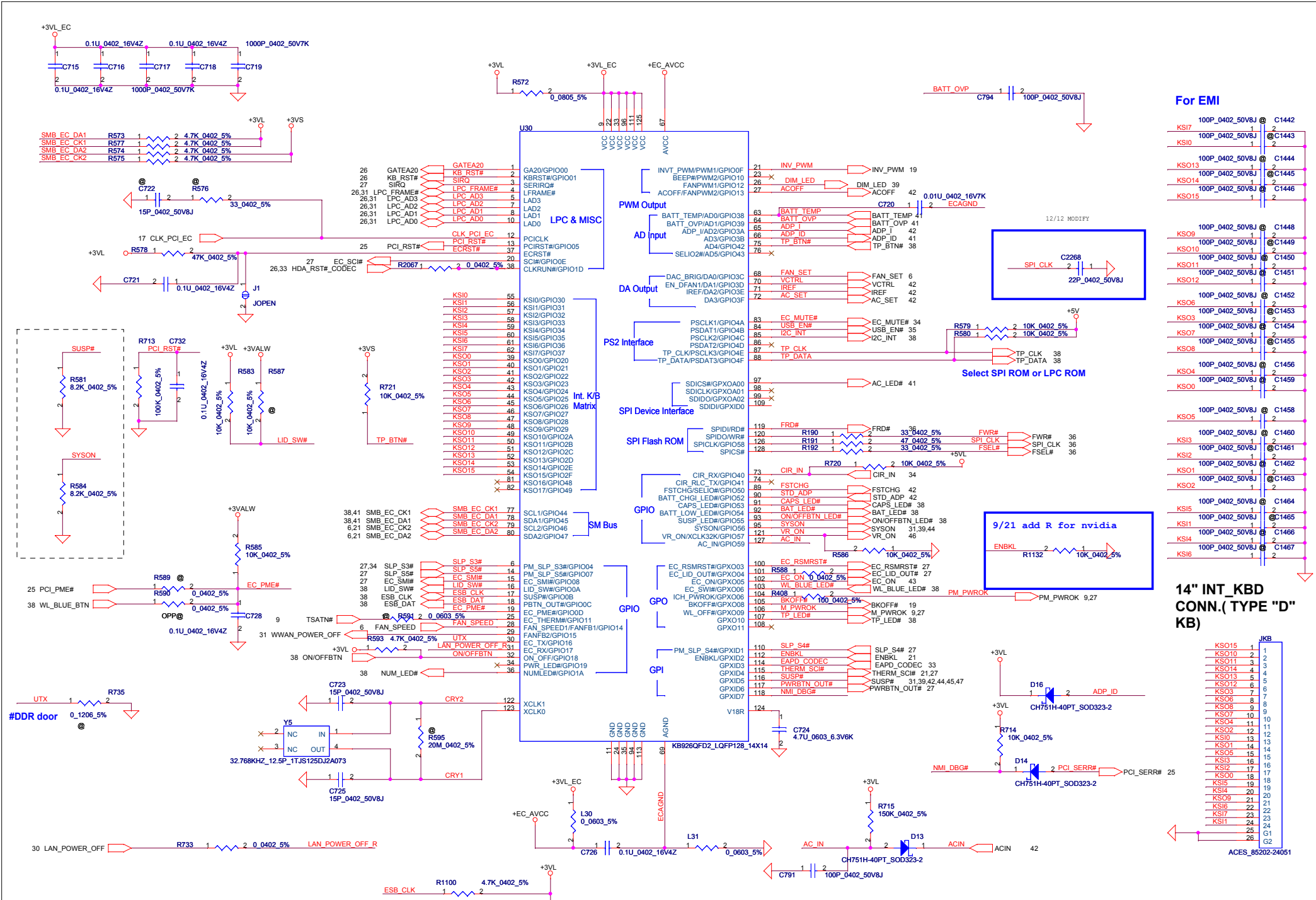
SPI ROM



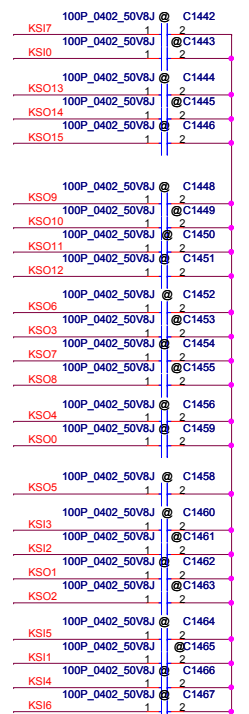
Acceleromter-1



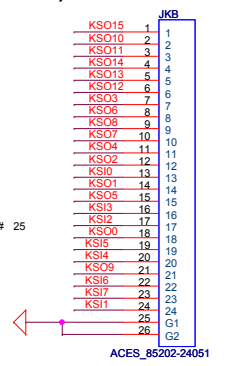
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2008/11/04	Deciphered Date	2008/11/04	Title BIOS ROM		
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				Date	Monday, February 16, 2009	Sheet 36 of 51



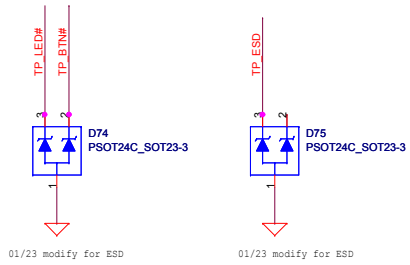
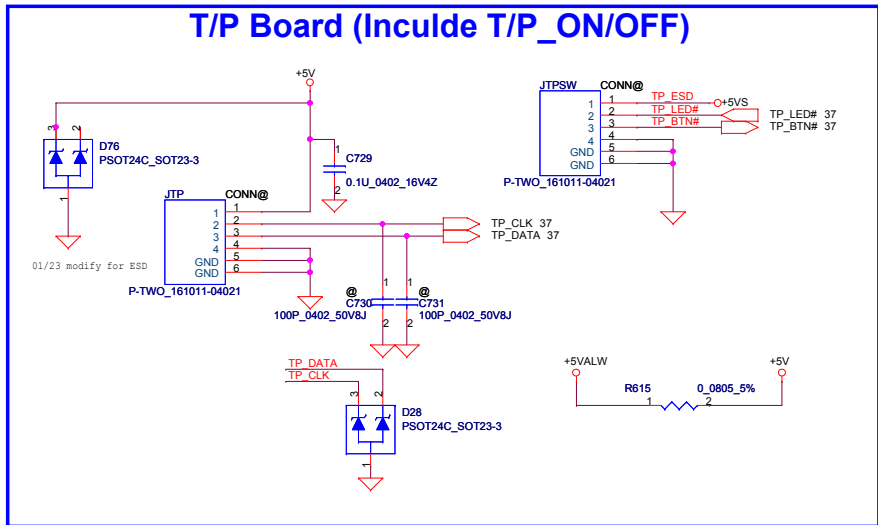
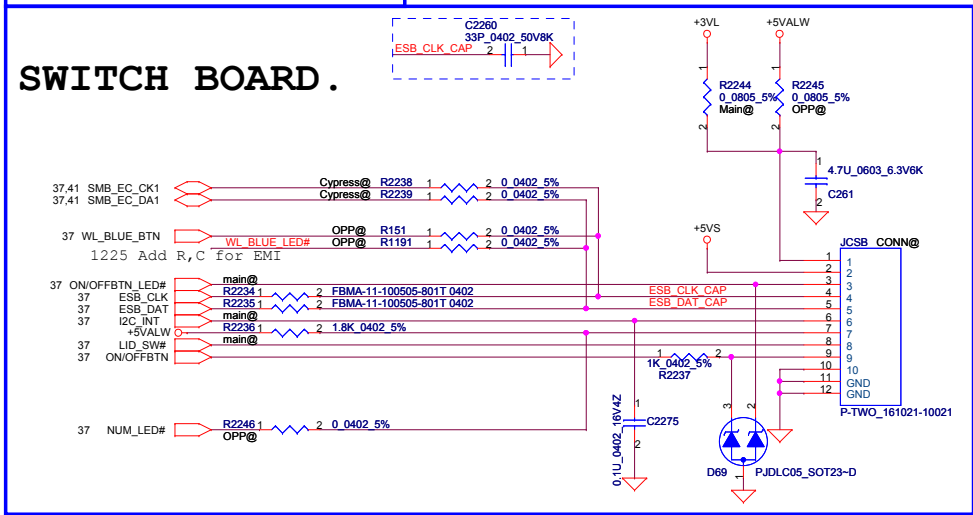
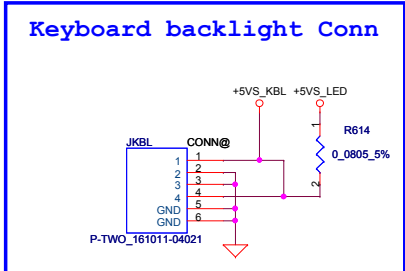
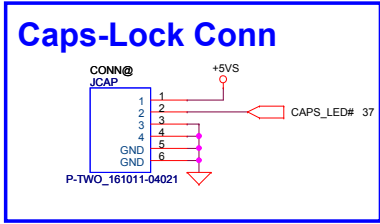
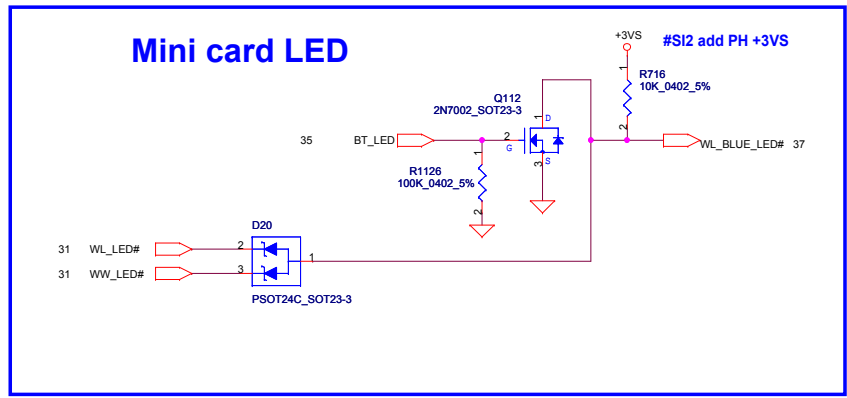
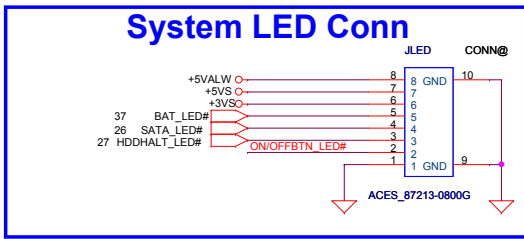
For EMI



14" INT_KBD CONN. (TYPE "D" KB)



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Issued Date	2008/11/04	Deciphered Date	2008/11/04	Compal Electronics, Inc.	
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Size	Document Number	Rev		Date	
	LA-4731P Rhett discrete	0.1		Monday, February 16, 2009	
		Sheet	37	of 51	

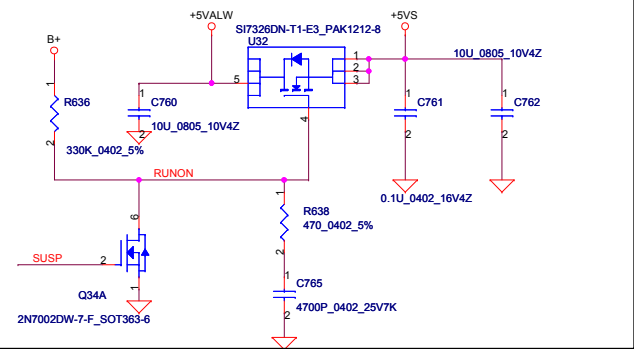


01/23 modify for ESD

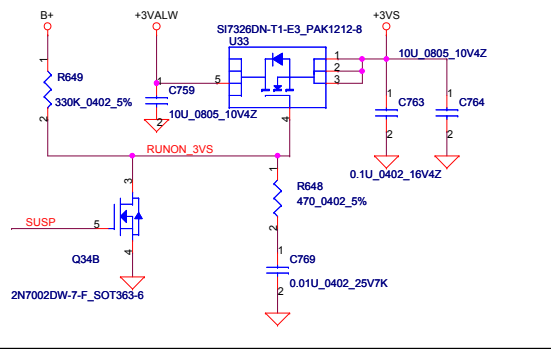
01/23 modify for ESD

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Issued Date	2008/11/04	Deciphered Date	2008/11/04	Compal Electronics, Inc.	
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Size	Document Number	Date		Rev	0.1
	LA-4731P Rhett discrete	Monday, February 16, 2009		Sheet	38 of 51

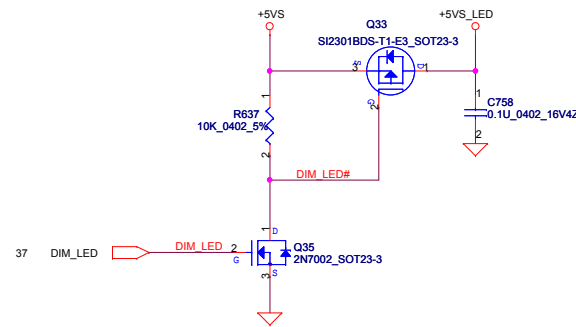
+5VALW to +5VS Transfer



+3VALW to +3VS Transfer

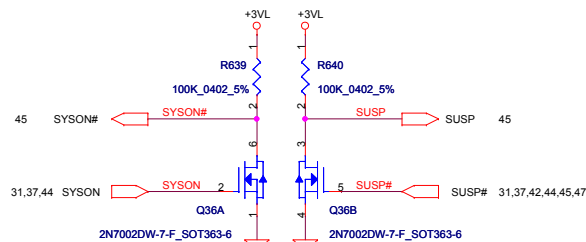
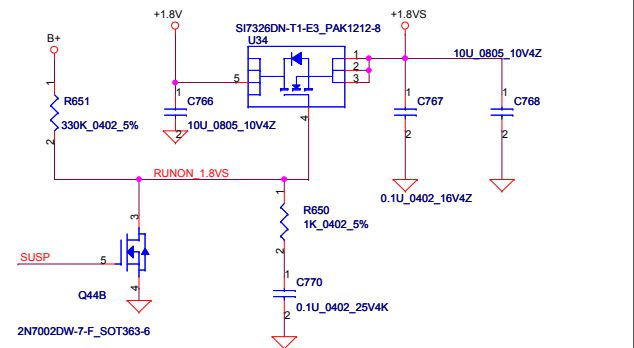


DIM LED

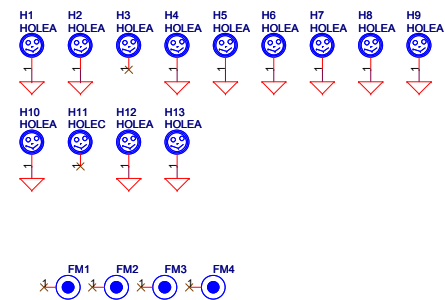
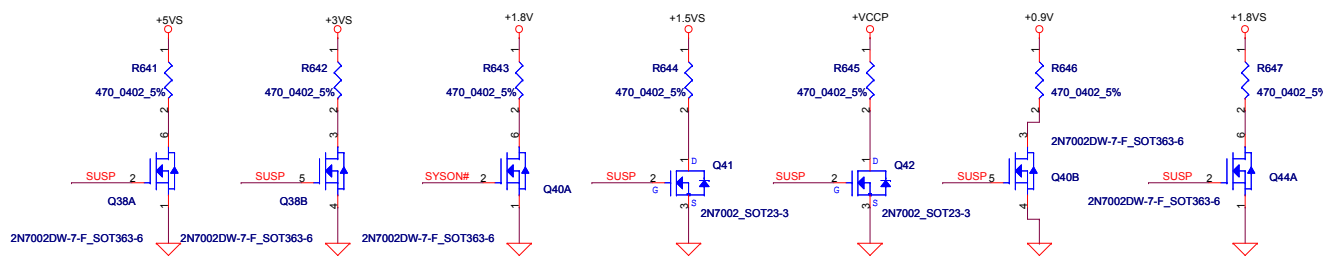


- T73
- T74
- T75
- T76
- T77
- T78
- T79
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- T90

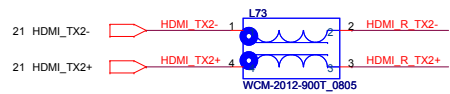
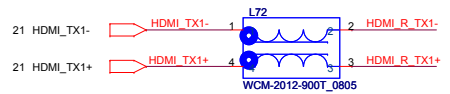
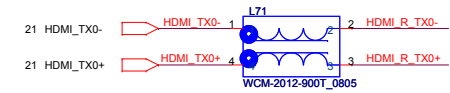
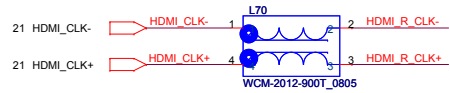
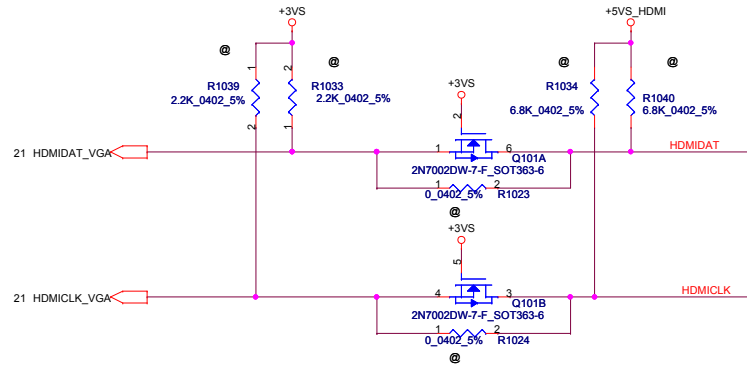
+1.8V to +1.8VS Transfer



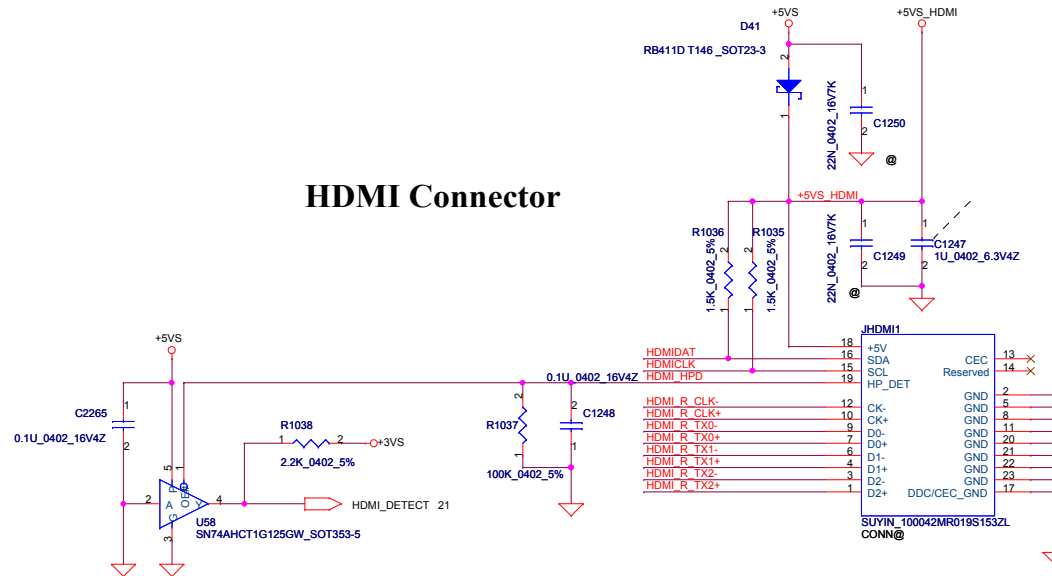
Discharge circuit



Security Classification		Compal Secret Data		Title	
Issued Date	2008/11/04	Deciphered Date	2008/11/04	DC/DC Interface	
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				LA-4731P Rhett discrete	Rev 0.1
Date: Monday, February 16, 2009				Sheet 39	of 51

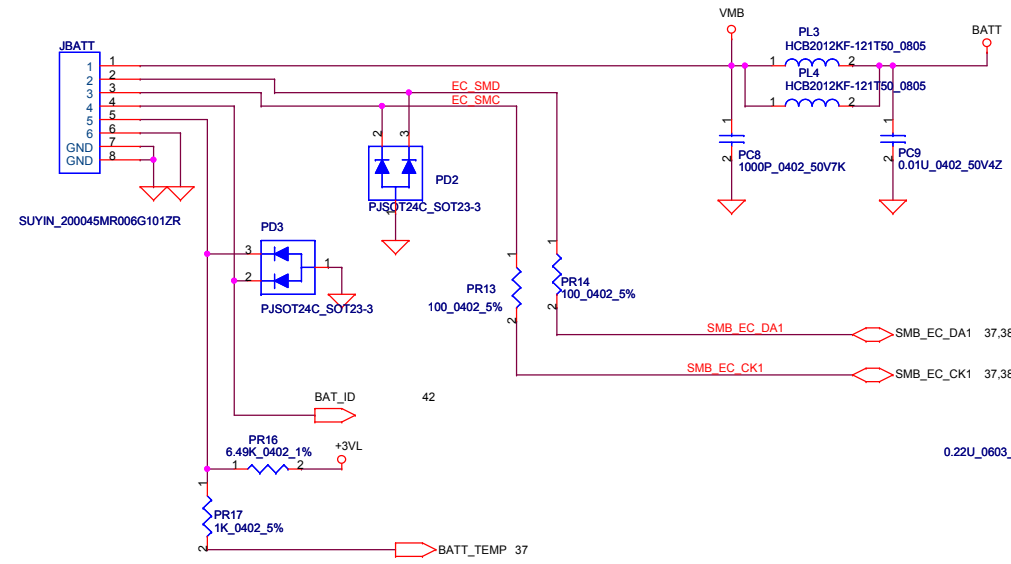
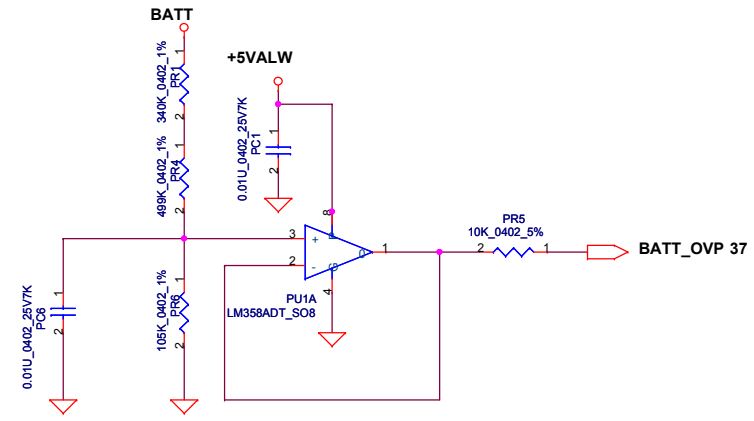
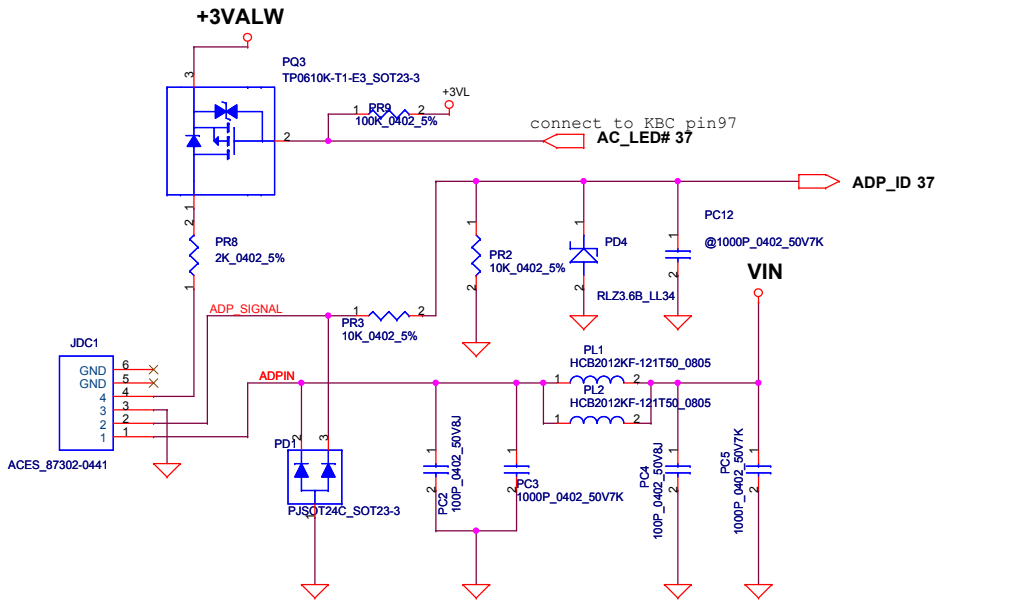


HDMI Connector

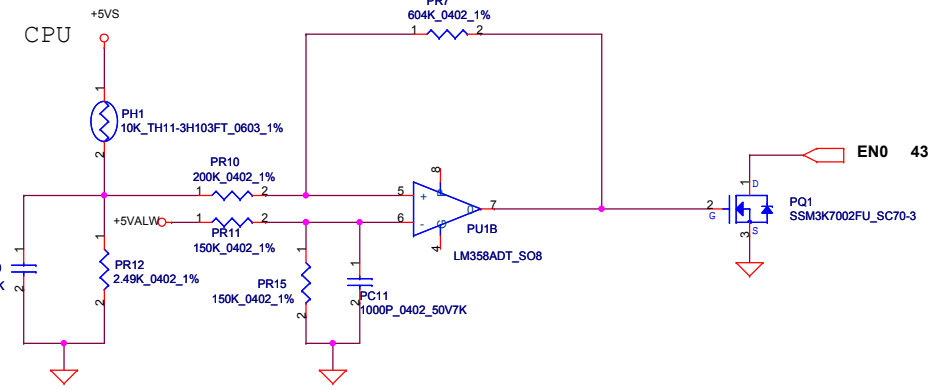


for HDMI certification

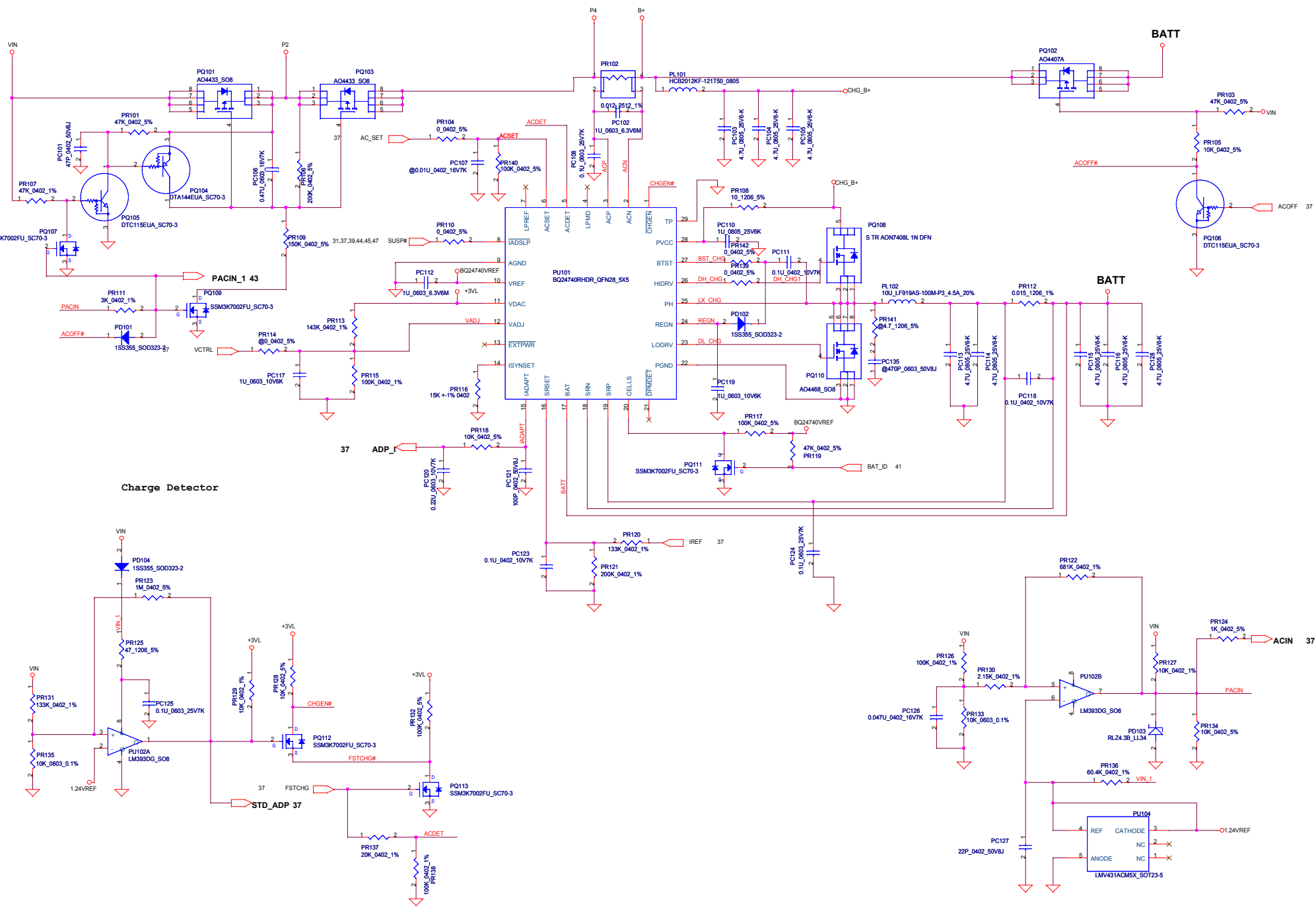
Security Classification	Compal Secret Data		Title	
Issued Date	2008/11/04	Deciphered Date	2008/11/04	Compal Electronics, Inc.
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Size	Document Number	Rev		
Custom	LA-4731P Rhett discrete	0.1		
Date:	Monday, February 16, 2009	Sheet	40	of 51



PH1 under CPU bottom side :
CPU thermal protection at 90 +/-3 degree C

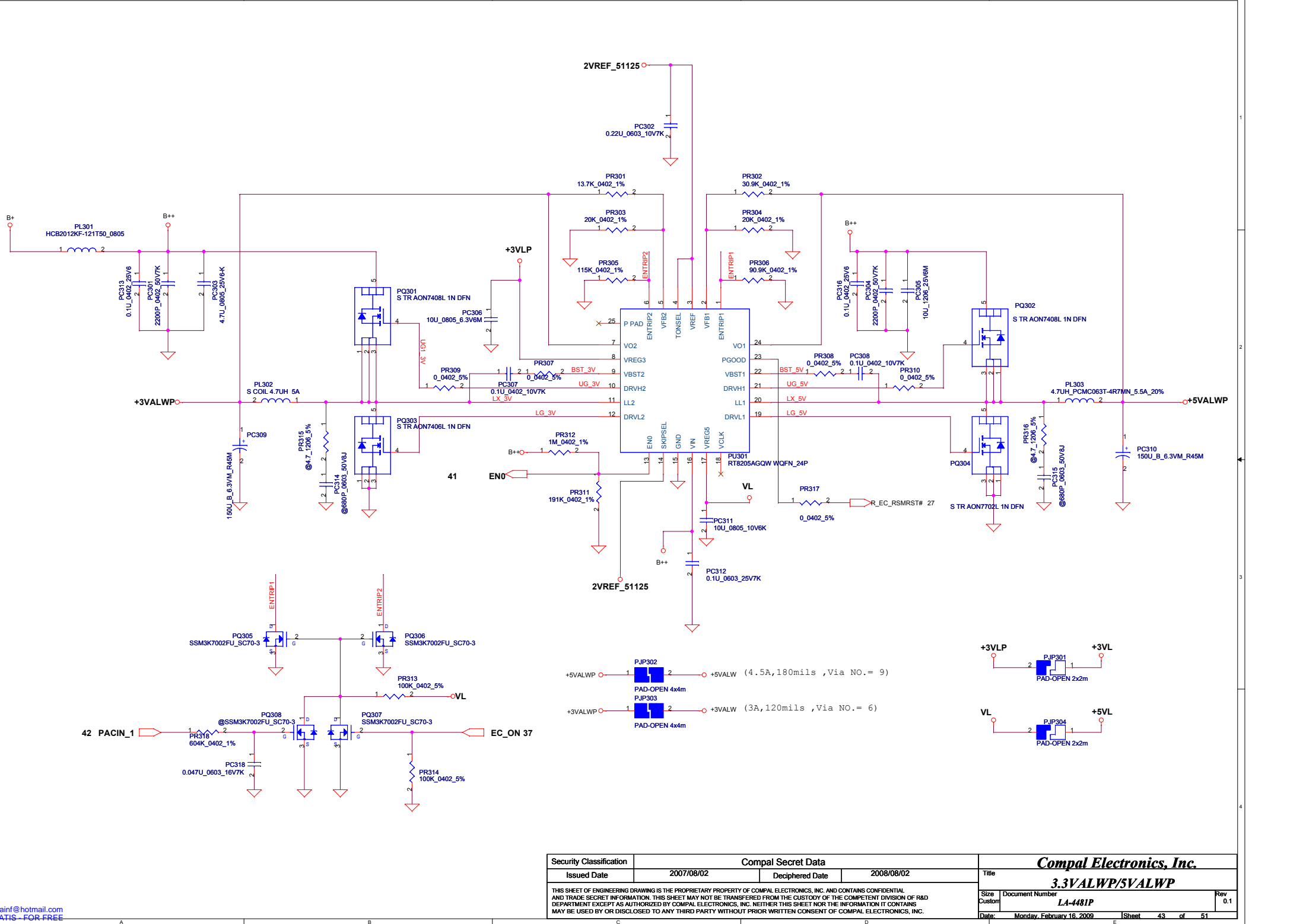


Security Classification		Compal Secret Data		Title	
Issued Date	2007/05/29	Deciphered Date	2008/05/29	DC Connector/CPU OTP	
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				Montevina Consumer Discrete	
				Date:	Monday, February 16, 2009
				Sheet	41 of 51
				Rev	0.1



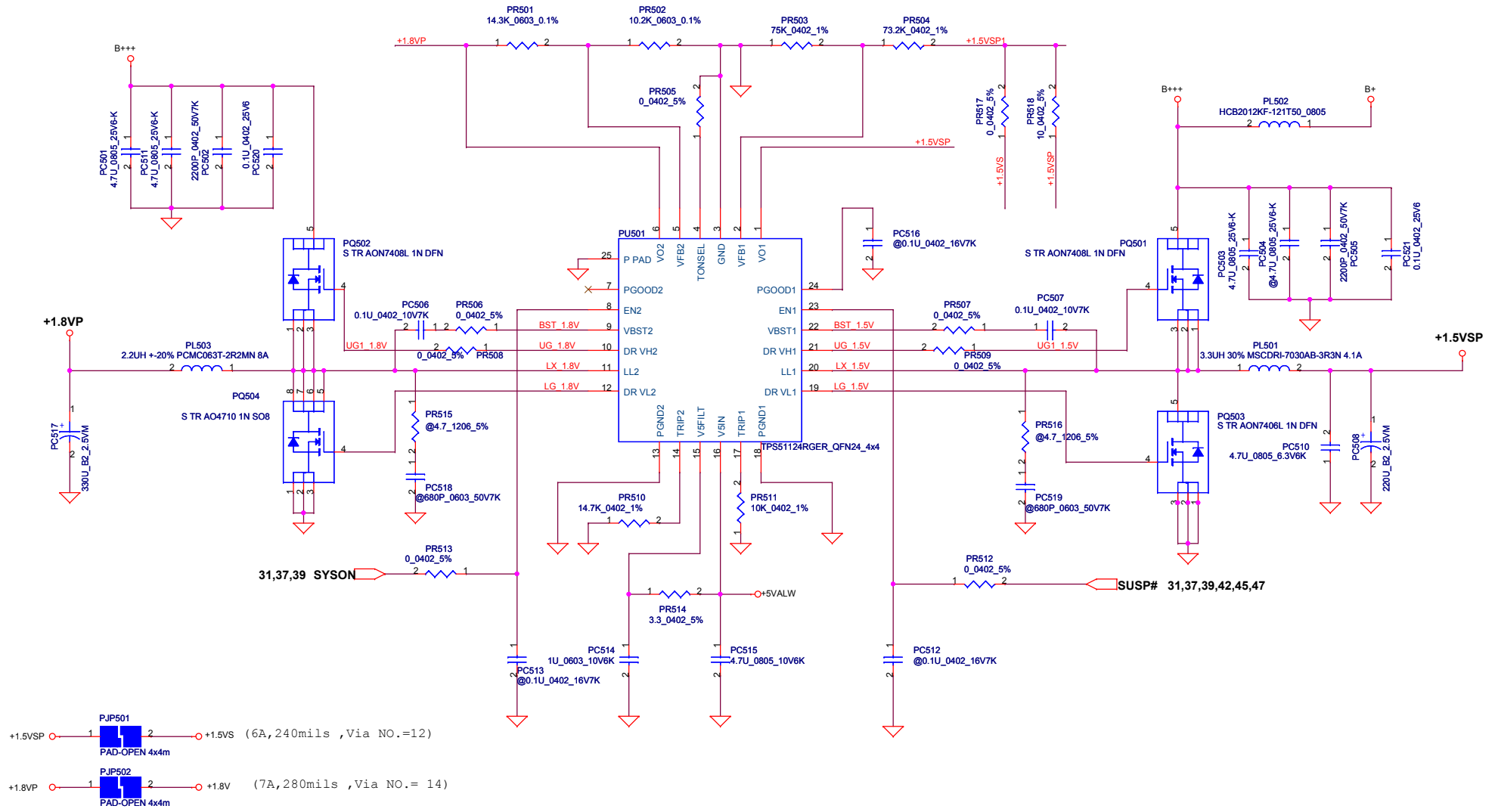
Charge Detector

Security Classification	Compal Secret Data		Title	
Issued Date	2007/05/29	Deciphered Date	2008/05/29	Charger
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Size	Document Number	Rev	0.1	
Date:	Monday, February 16, 2009	Sheet	42	of 51

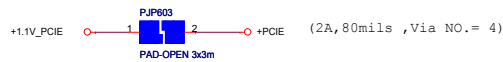
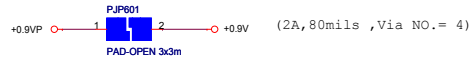
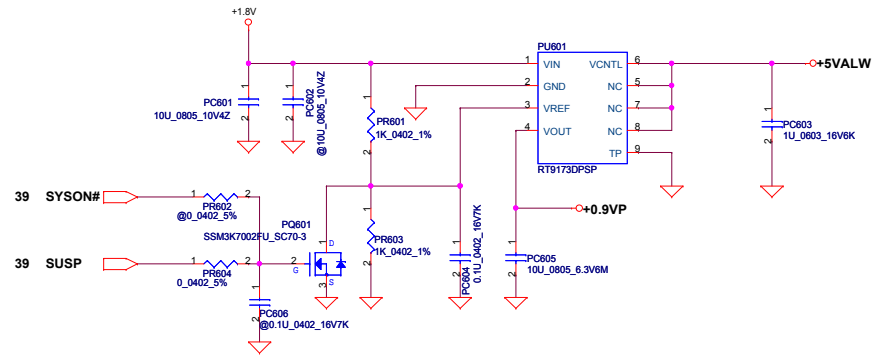


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Issued Date	2007/08/02	Deciphered Date
		2008/08/02
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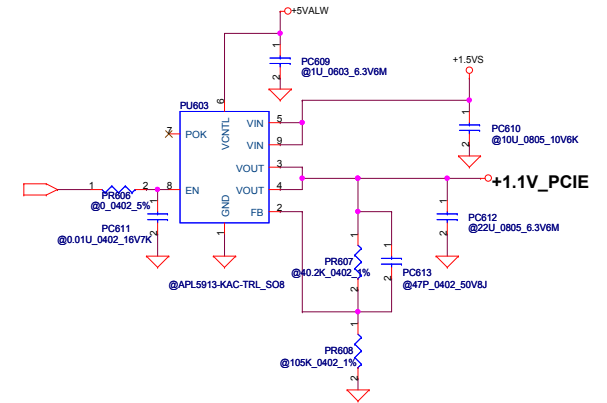
Title		
Compal Electronics, Inc.		
3.3VALWP/5VALWP		
Size	Document Number	Rev
Custom	LA-4481P	0.1
Date:	Monday, February 16, 2009	Sheet 43 of 51



Security Classification		Compal Secret Data		Title		
Issued Date	2007/05/29	Deciphered Date	2008/05/29	1.5VSP/1.8VP		
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				Montevina Consumer Discrete		0.1
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31,37,39,42,44,47 SUSP#

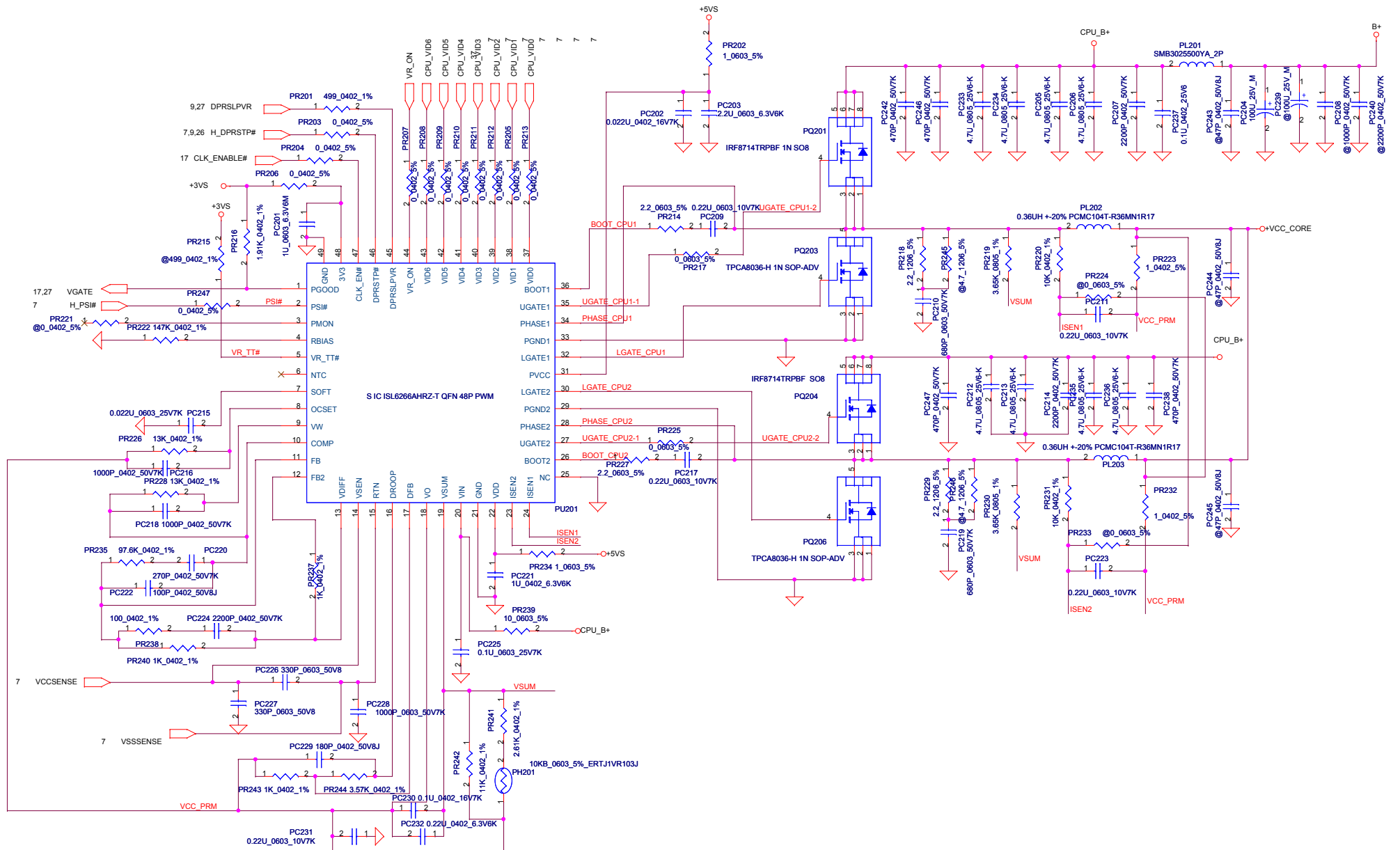


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Compal Electronics, Inc.

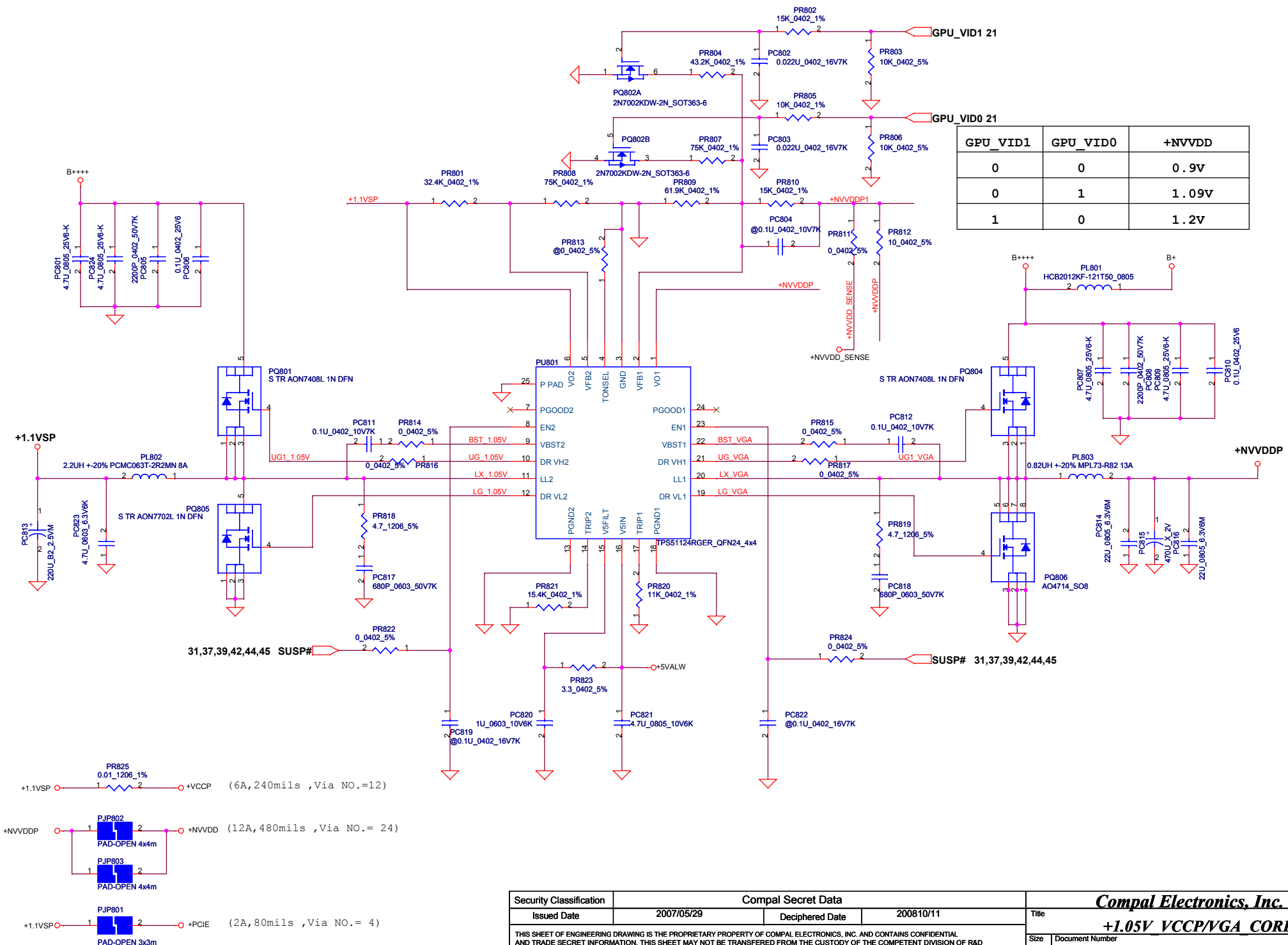
0.9VP/1.1V_PCIE

LA-4102P Blade discrete



Compal Electronics, Inc.		
Title		
+CPU_CORE		
Size	Document Number	Rev
Custom		0.1
Date:	Monday, February 16, 2009	Sheet 46 of 51

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GPU_VID1	GPU_VID0	+NVVDD
0	0	0.9V
0	1	1.09V
1	0	1.2V

Security Classification	Compal Secret Data	
Issued Date	2007/05/29	Deciphered Date
		2008/10/11

Compal Electronics, Inc.		
+1.05V VCCP/VGA CORE		
Title	LA-4112P	
Size	Document Number	Rev
		0.1
Date:	Monday, February 16, 2009	Sheet 47 of 51

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Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
1	CardReader clock issue	17	Using USB_0 for CLK_48M_CR	2008/10/08	SI-1
2	Debug Card issue	31	Connect PLT_RST# to JP7.A17	2008/10/08	SI-1
3	delete VGA external thermal sensor layout location for layout space limitation	29	Del U6,C348,C350	2008/10/08	SI-1
4	Add Audio board	34	Add JAUDIO connecter for audio board	2008/10/08	SI-1
5	delete VGA JTAG for layou space limitation	29	Delete T47,T48,T49,T50,T51	2008/10/08	SI-1
6	Cap board issue	38	Change Cap board power rail to +3VL	2008/10/08	SI-1
7	Change JFPR to 6 pin connector	35	change JFPR	2008/10/08	SI-1
8	Change FAN control circuit to voltage control	6	Add U51,D17,R50,C41	2008/10/08	SI-1
9	Delete HDA SSC	26	Remove U44 for layout spacing	2008/10/08	SI-1
10	For PR mini card connector	31	Add R2252 -- R2261	2008/10/08	SI-1
11	PA/PR CardReader LED	32	D72 for PA, D71 for PR	2008/10/08	SI-1
12	EMI request	33	Change R2205 to L76	2008/10/08	SI-1
13	change MIC to 2pin and add SPK connector	34		2008/10/08	SI-1
14	Speaker L & R reverse	34		2008/11/20	SI-2
15	JFPR change to 4 pin	40	Add U58,C2265	2008/11/20	SI-2
16	add buffer on detect pin for certification item 7-12	34		2008/11/20	SI-2
17	<i>Bom Error [Bug: BT led fail]</i>	<i>38</i>	<i>Change D20's Part number to SCA00000G00</i>	2008/12/10	PV
18	<i>Realtek suggest us to change Cap value</i>	<i>30</i>	<i>Change C2193 value from 0.1uF to 1uF</i>	2008/12/10	PV
19	<i>Slove WWLAN Noise : Add Cap X4 [to GND]</i>	<i>26</i>	<i>C499 and C2130 default mount, Add C2266 and C2267 [12 PF]</i>	2008/12/10	PV
20	<i>Slove WWLAN Noise:Add Cap,change R191va</i>	<i>37</i>	<i>Add C2268 [22PF] on R191.2 to GND and R191 change to 47 ohm</i>	2008/12/10	PV
21	<i>Slove WWLAN Noise:C356,C357 default mou</i>	<i>21</i>	<i>C356 and C357 default mount</i>	2008/12/10	PV
22	<i>Slove SMT issue</i>	<i>37</i>	<i>Change U30 FOOTPRINT [fromKB926QFA1_LQFP128_14X14 change to ECE5028-NU_VTQFP128_14X14]</i>		PV
23	<i>Slove SMT issue</i>	<i>37</i>	<i>Change JKB FOOTPRINT [from ACES_85202-24051_24P change to ACES_85202-24051_24P-S]</i>	2008/12/10	PV
24	<i>Slove ESD issue</i>	<i>26</i>	<i>ADD C2269 [0.1uF] on BATT1.1 trace (pin 1)</i>	2008/12/17	PV
25	<i>Slove ESD issue</i>	<i>33</i>	<i>Add one Diode [D73] on MIC_EXTR, MIC_EXTL (near chip side)</i>	2008/12/17	PV
26	<i>Slove ESD issue</i>	<i>33</i>	<i>Change cap value [C2270,C2271,C2272,C2273] to 0.1uF</i>	2008/12/17	PV
27	<i>Slove Audio issue</i>	<i>34</i>	<i>Change cap value to 2.2uF [C2239,C2240]</i>	2008/12/17	PV
28	<i>Slove non-RoHS Part</i>	<i>30</i>	<i>Change C2157,C2160,C2215 and C2217 Part number [from SE070104Z00 to SE070104Z80]</i>	2008/12/17	PV

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Issued Date	2008/11/04	Deciphered Date	2008/11/04		
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				LA-4731P Rhett discrete	
				Date:	Thursday, February 12, 2009
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				Rev	0.1

Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
29	Slove ESD ISSUE	30	ADD R2262 [4.7K] and C2274 [0.01 uF] [Default unmount]	2008/12/17	PV
30	Slov Audio EISSUE	34	Change JAUDIO [Audio conn] pin defination	2008/12/17	PV
31	Slove Audio ISSUE	33	DEL R2204	2008/12/17	PV
32	Slove Q Die and E Die		Just use Qim and Hynix VRAM on PV		
33	ESD Request	38	ADD C2275,D74,D75 and D76		
34	ESD Request	34	Modify D66 location		
35	ESD Request	18	Do not moundt D5,D6 and D7		
36	ESD Request	30	Do not mount D62		
37	ESD Request	35	Do not mount D45 and D46		
38	ESD Request	35	Do not mount D47		
38					
38					

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