

Compal Confidential

2014 S-series(400series) Rolo/Reeses/Raisinet

INTEL Sharkbay & Crescent bay ULT –U processor with DDR3L

Date : 2014/02/18

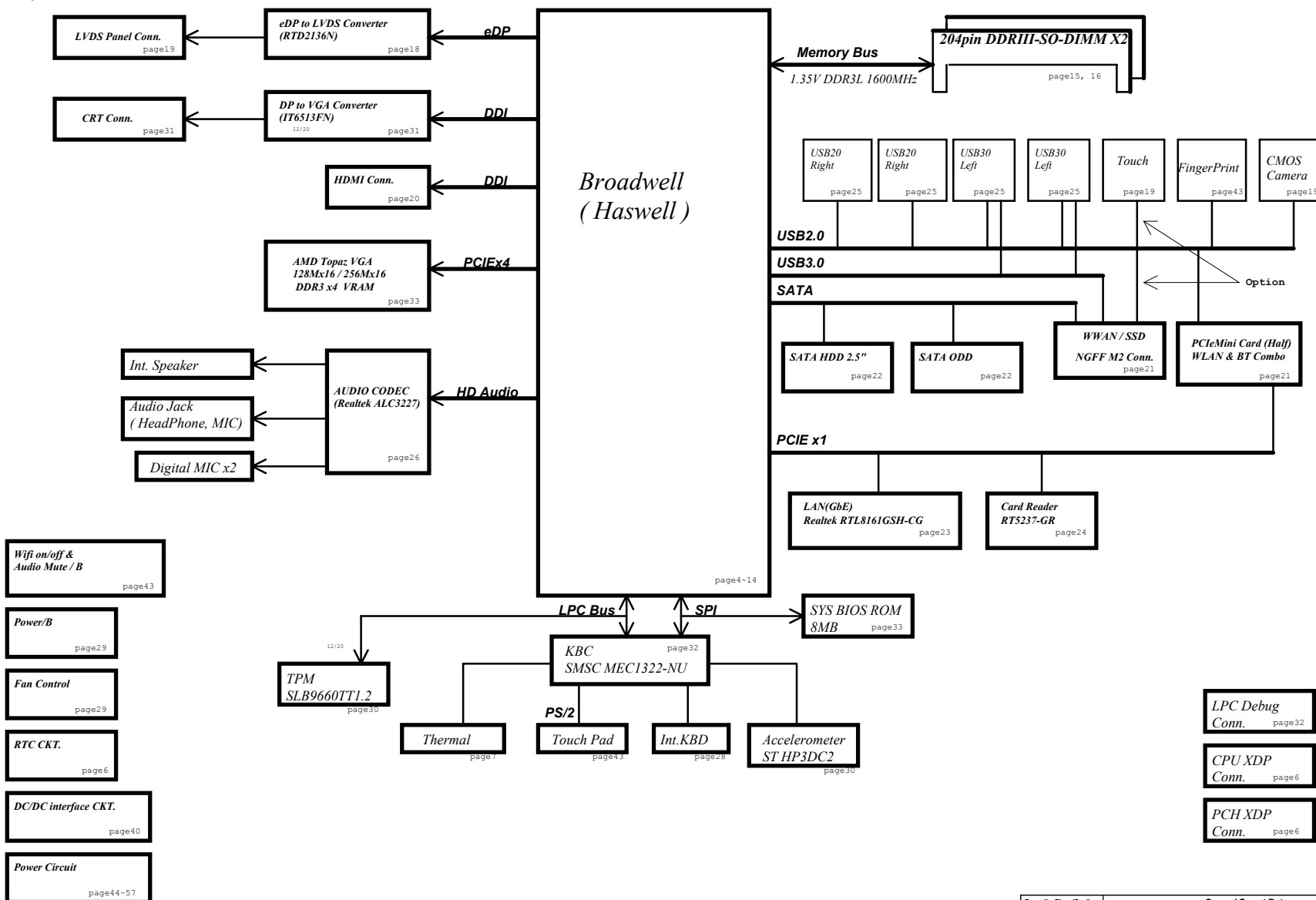
Version 0.5

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Model Name :

Intel Broadwell U / Haswell Block Diagram

Project Name :



CPU DC/DC	
TPS51622ARSMR	50~51
INPUTS	OUTPUTS
B+	VCC VORE
SYSTEM DC/DC	
RT8243AZQW	47
INPUTS	OUTPUTS
B+	3VDS/5VDS
SYSTEM DC/DC	
RT8207MZQW	48
INPUTS	OUTPUTS
B+	1.35V_VDDQ 0.675VS
SYSTEM DC/DC	
SY8206DQNC	49
INPUTS	OUTPUTS
B+	1.05VS
SYSTEM DC/DC	
SY8003DFC	52
INPUTS	OUTPUTS
B+	1.5VS
SYSTEM DC/DC	
RT8880BGQW	54~55
INPUTS	OUTPUTS
B+	+VGA_CORE
SYSTEM DC/DC	
SY8003DFC	56
INPUTS	OUTPUTS
B+	+1.8VS_VGA
SYSTEM DC/DC	
SY8003DFC	57
INPUTS	OUTPUTS
B+	+0.95VS_VGA

@ is NO SMT part (empty)

short@ : short pad , don't pop.

@EMI@, @ESD@, @RF@ : Reserve , don't pop.

RF@ : RF team request, must add.

EMI@ : EMI team request, must add.

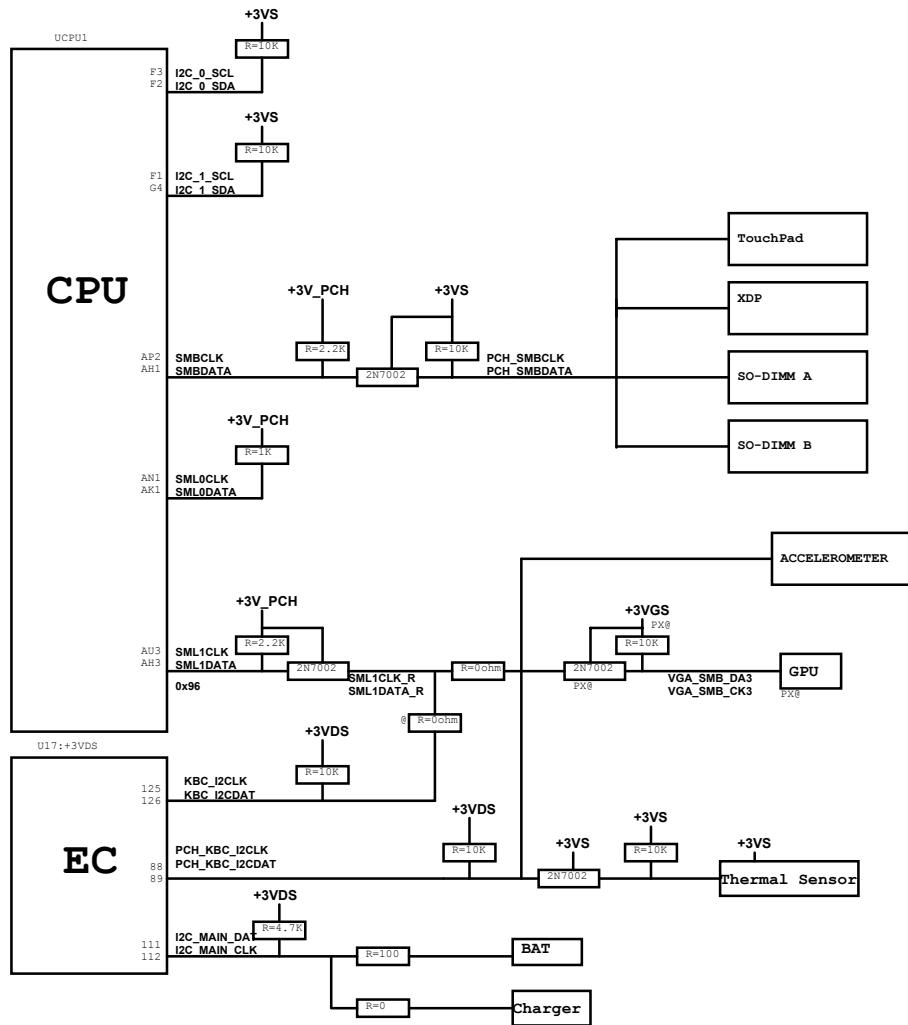
ESD@ : ESD team request, must add.

LVDS@ : Support LVDS panel.

WWAN@ : For WWAN function.

PX@ : GPU BOM config.

eDP@ : Support eDP panel.



<USB2.0 port>

USB2.0 port	DESTINATION
0	CS
1	USB 2.0(Right side)
2	USB 2.0(Left side)
3	WLAN/BT
4	Finger Print
5	WWAN Touch (Option)
6	Camera
7	USB 2.0(Left side)

<PCI-E,SATA,USB3.0>

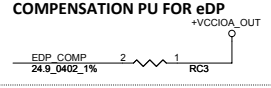
Lane#	PCI-E	SATA	USB3.0	DESTINATION
1			0	CS
2			1	USB3.0
3	1		2	WWAN (M.2)
4	2		3	Card reader(PCI-E)
5	3			10/100/1000 LAN
6	4			WLAN (M.2)
7				GPU(DIS only)
8				GPU(DIS only)
9				GPU(DIS only)
10				GPU(DIS only)
11	L3	3		2.5"HDD
12	L2	2		ODD
13	L1	1		
14	L0	0		SSD(NGFF)

CC97-CC102 must closed to connector not CPU

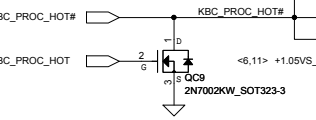
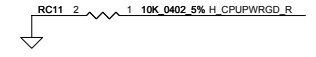
<HDMI>

<eDP>

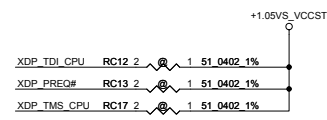
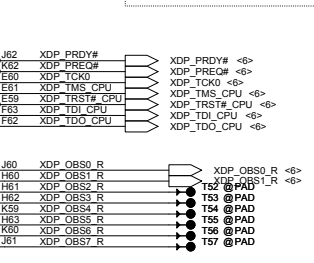
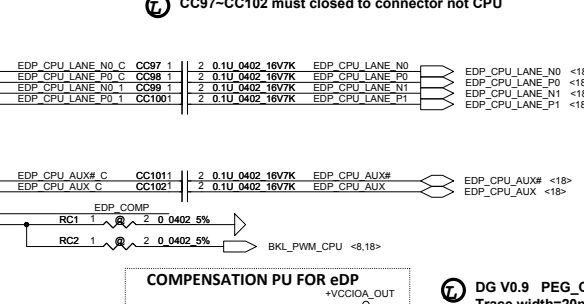
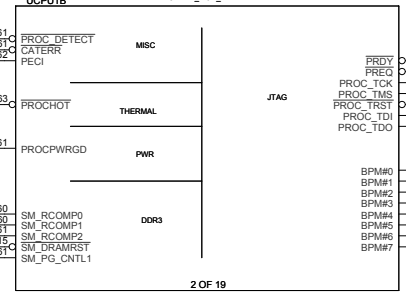
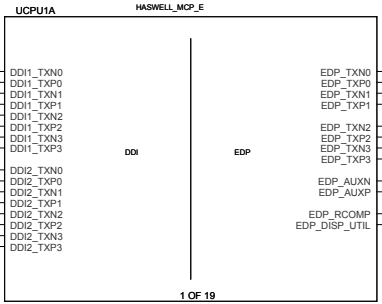
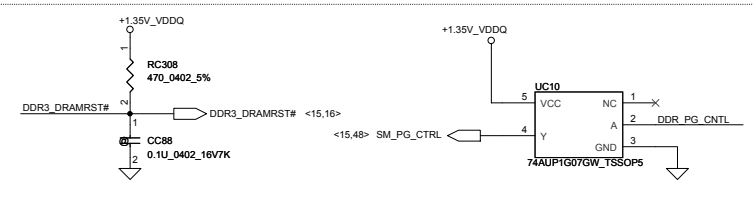
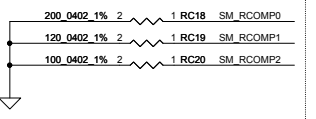
<eDP>



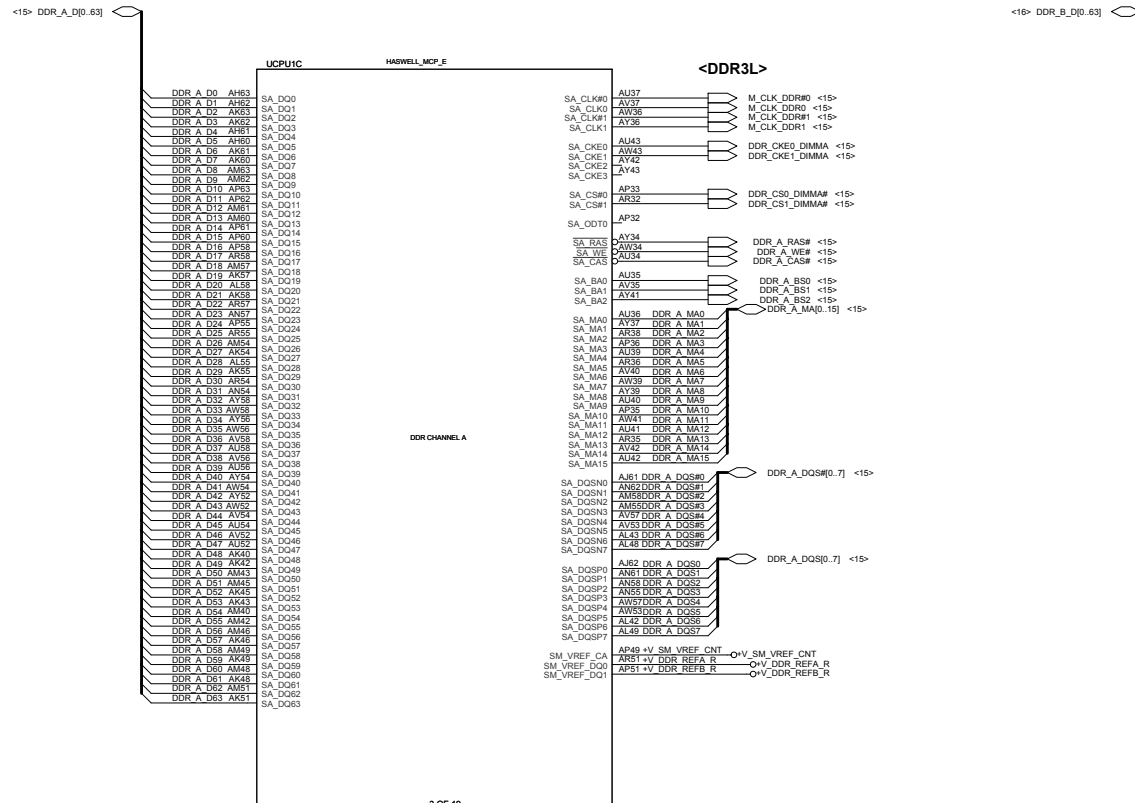
DG V0.9 PEG_COMP
 Trace width=20mil and spacing=25mil
 Max length=100mil



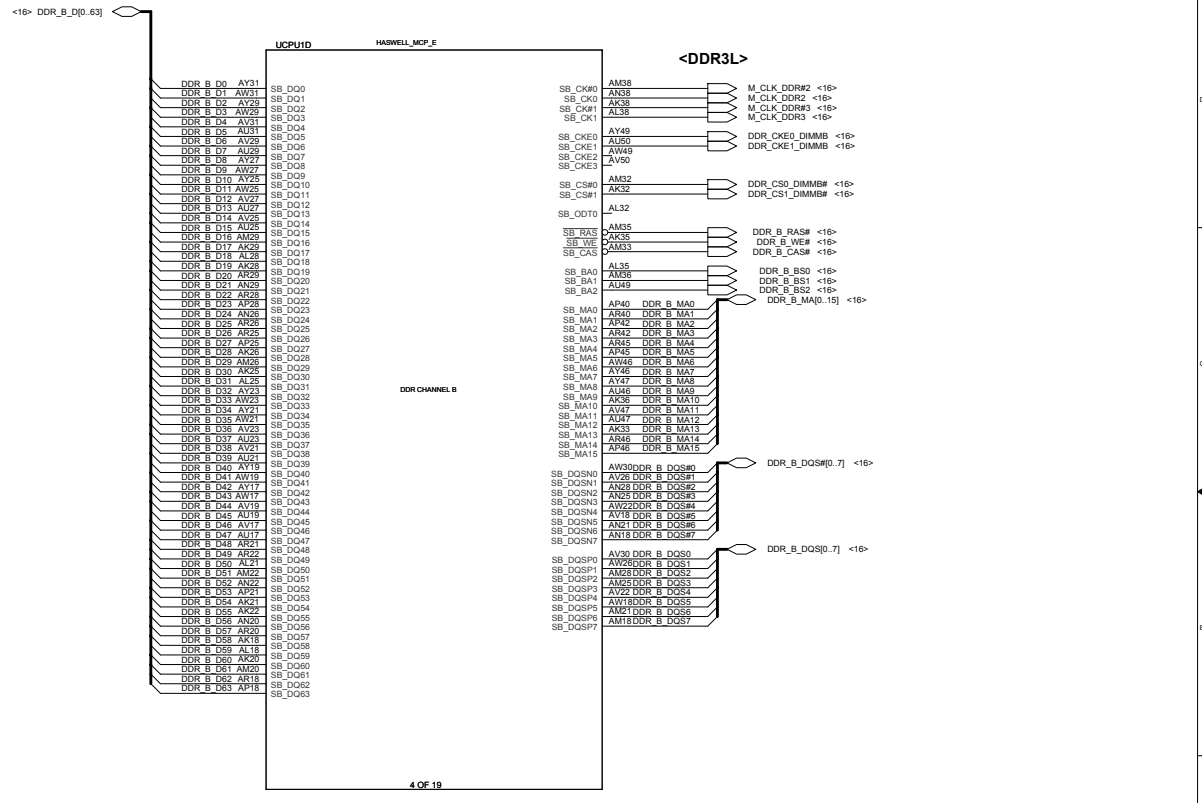
DG V0.5 Trace width=12-15 mil
 Max length=500mil
DDR3 COMPENSATION SIGNALS



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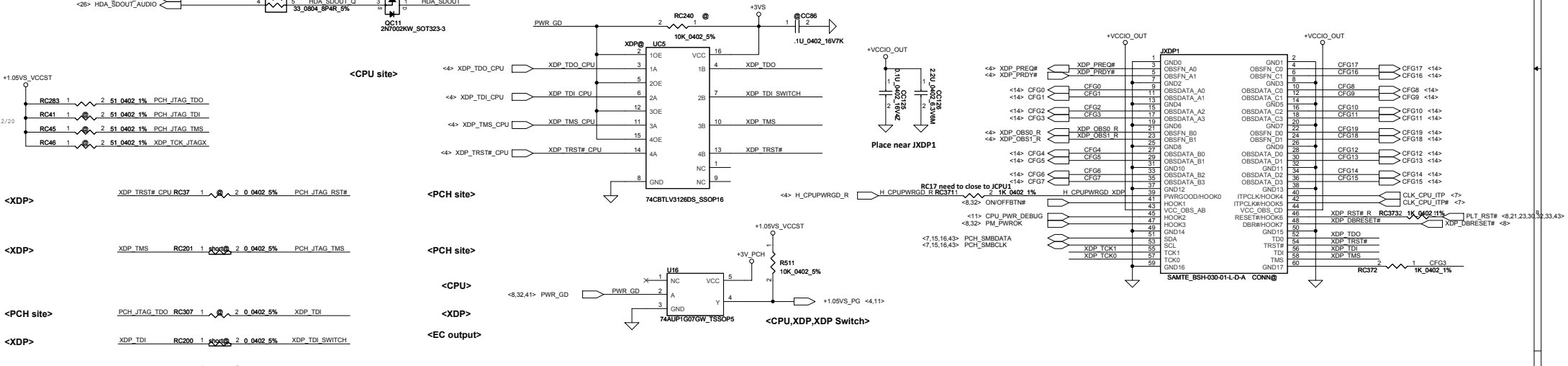
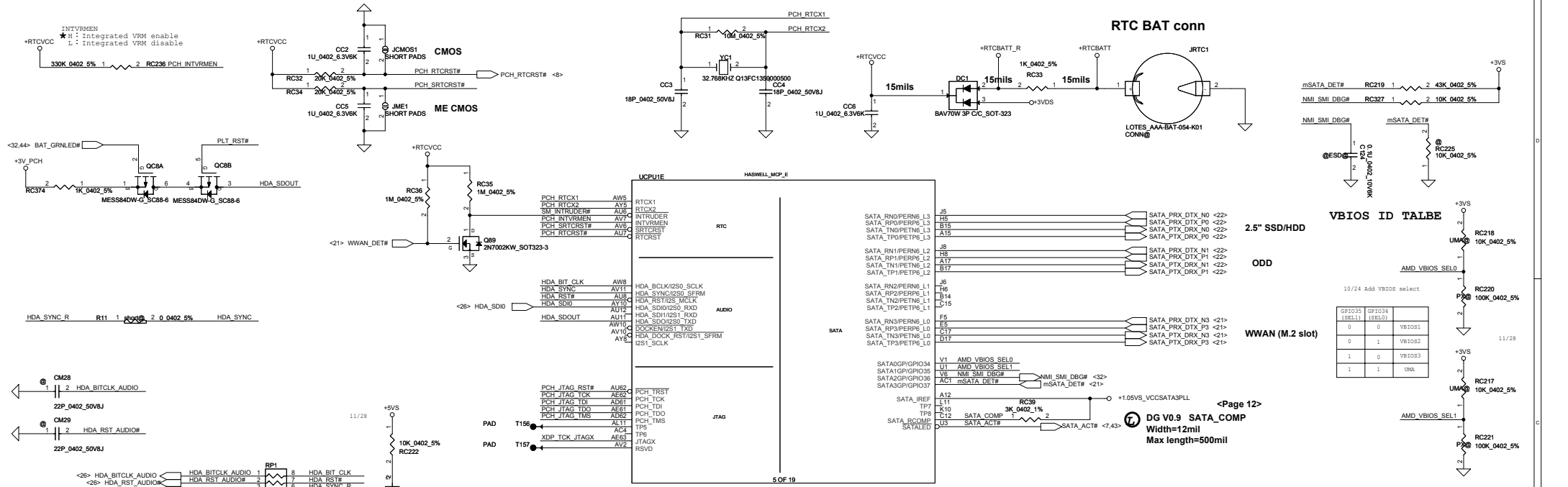
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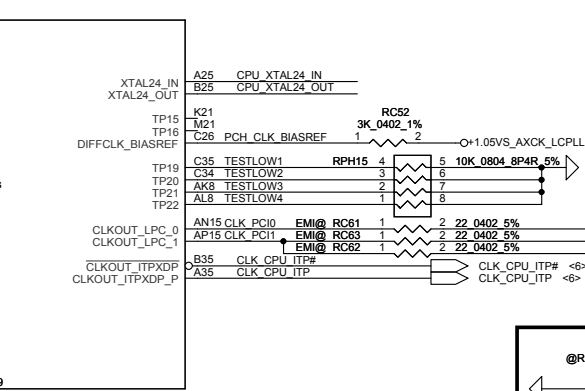
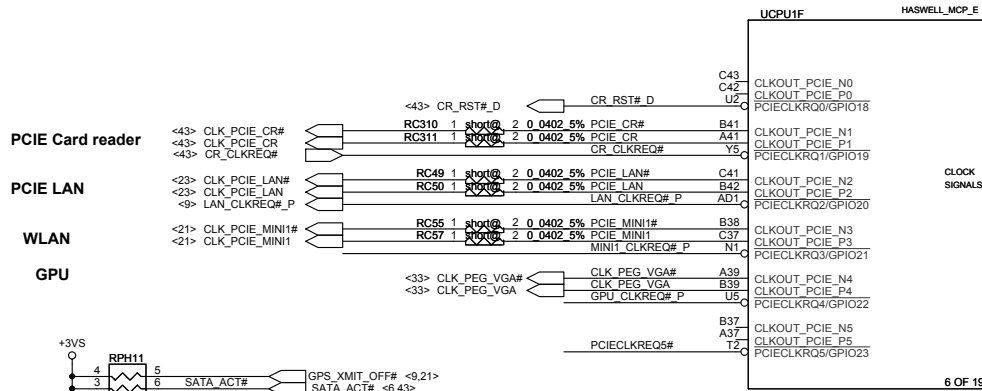
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Topolog	Description	Best Use for	Resistors Stuffed	Resistors uStuffed
Default Setting: Dual TCK Scan Chains (also known as "Shared JTAG" in other document)	In this topology, the CPU JTAG chain will be controlled by TCK0 and TCK1 will control the PCH JTAG chain.	- Run control oper. - ME/Sx debug	R1d,R2,R3d, R4,R5,J1d J2d,J3d* J4d and Rs5*	J1s, J2s, J3s R6,R7,R8,R9
Single TCK scan chain (also known as "Common JTAG" in other document)	In this topology, PCH TDI-TDO and CPU TDI-TDO will be chained to form one JTAG scan chain controlled by TCK0	- Boundary Scan/ - Manufacturing test	J1s, J2s, J3s** R2, R4, R5, R5s**	R1d, R3d, J1d, J2d J3d**, J4d, R6, R7, R8, R9

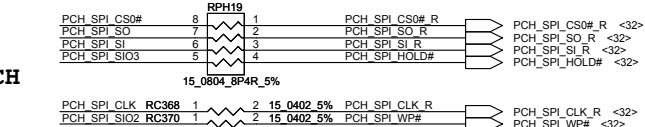
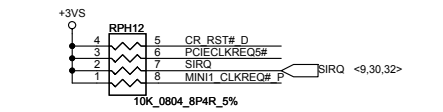
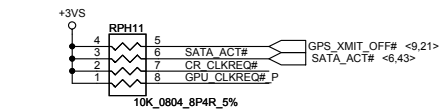
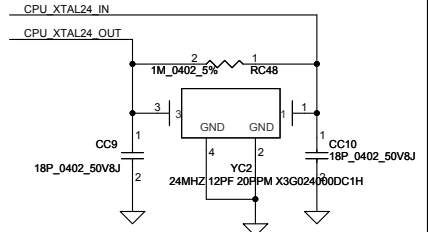


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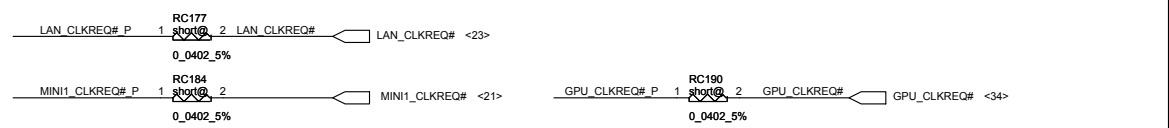
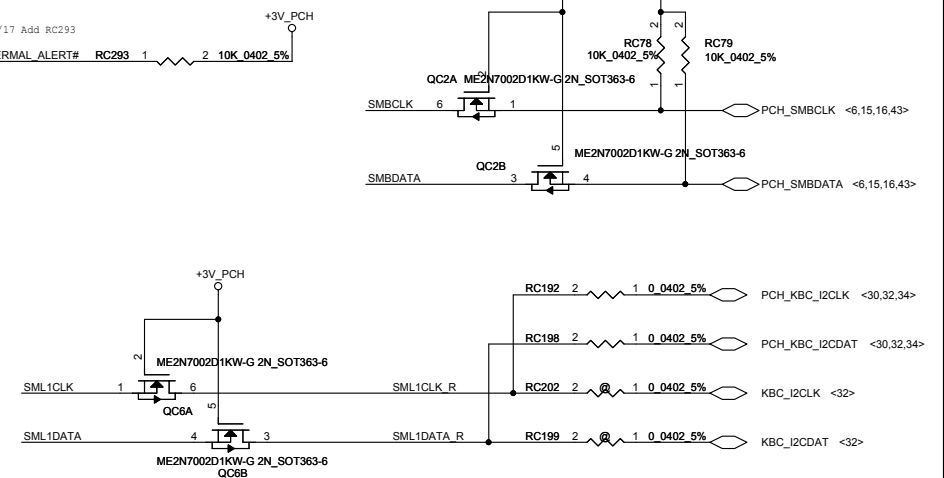
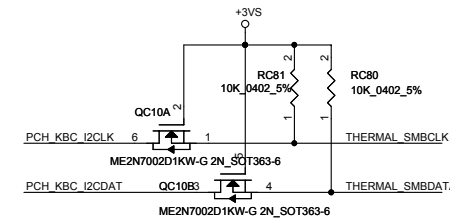
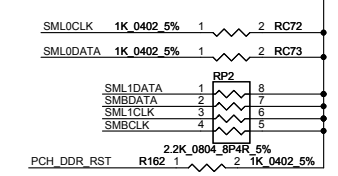
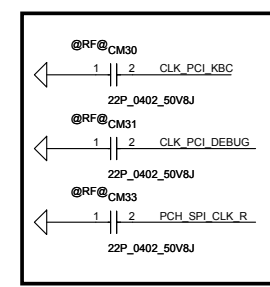
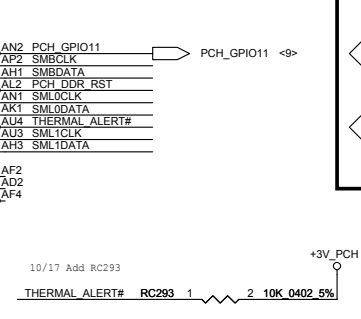
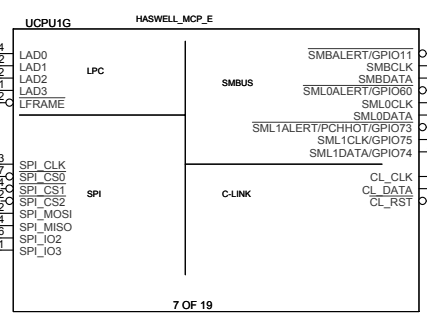
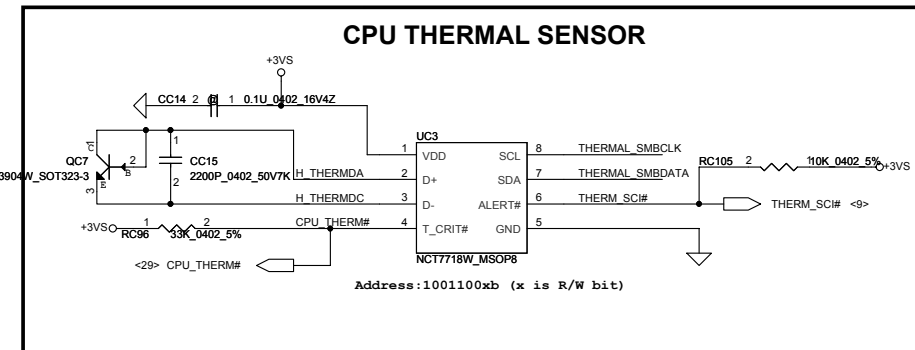
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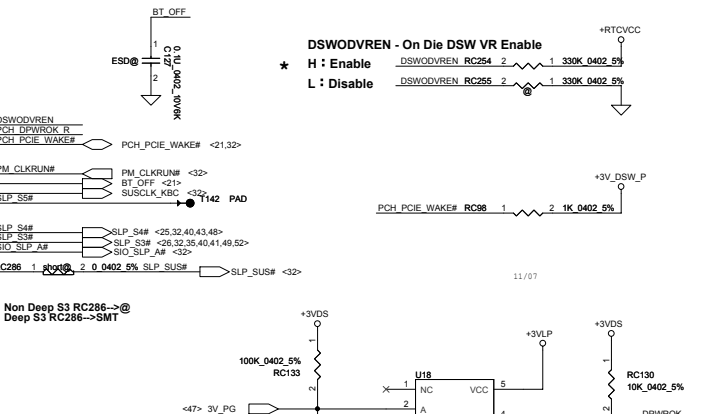
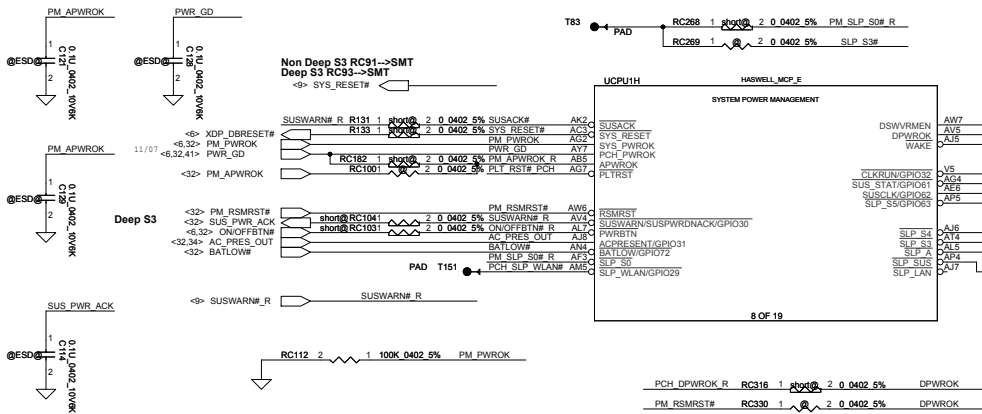


<PCH>

<KBC>

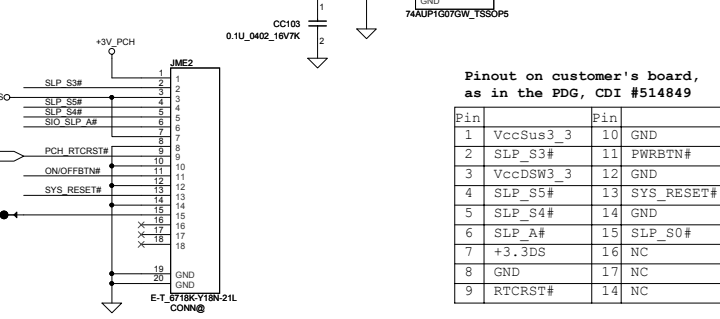


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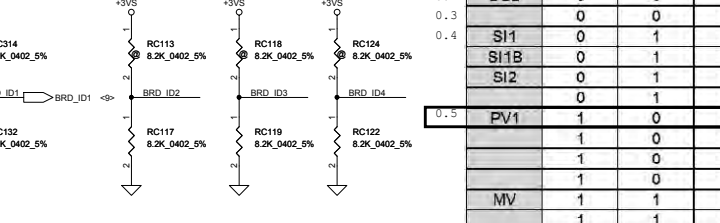
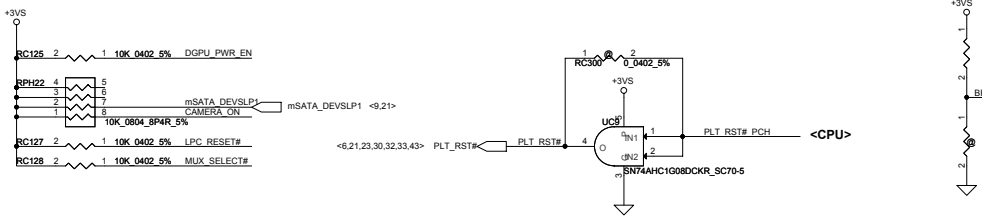
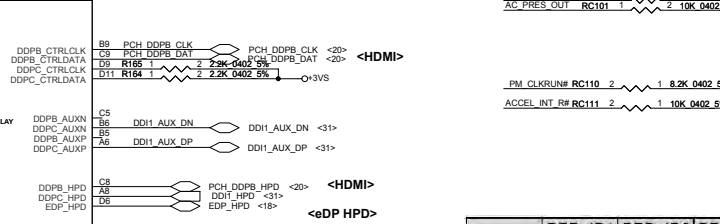
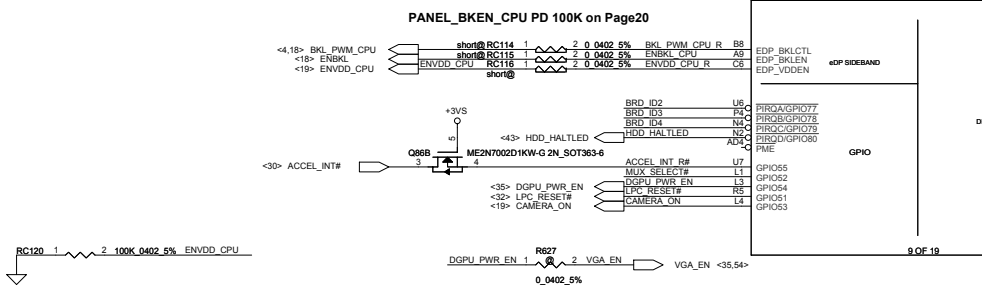
Intel ME-EC Interaction Signal List with and without M3 support

Signal Name	Platform With M3 Support (e.g., Intel AMT)	Platform Without M3 Support
SUSWRDNACK (GPIO3)	Required	Required
ACPRESENT (GPIO31)	Required	Required
SLP_A#	Required	[Tie to SLP_S3#] Note: If SLP_S3# is not routed from FCH to EC, then SLP_A# becomes required from Intel ME-EC perspective.

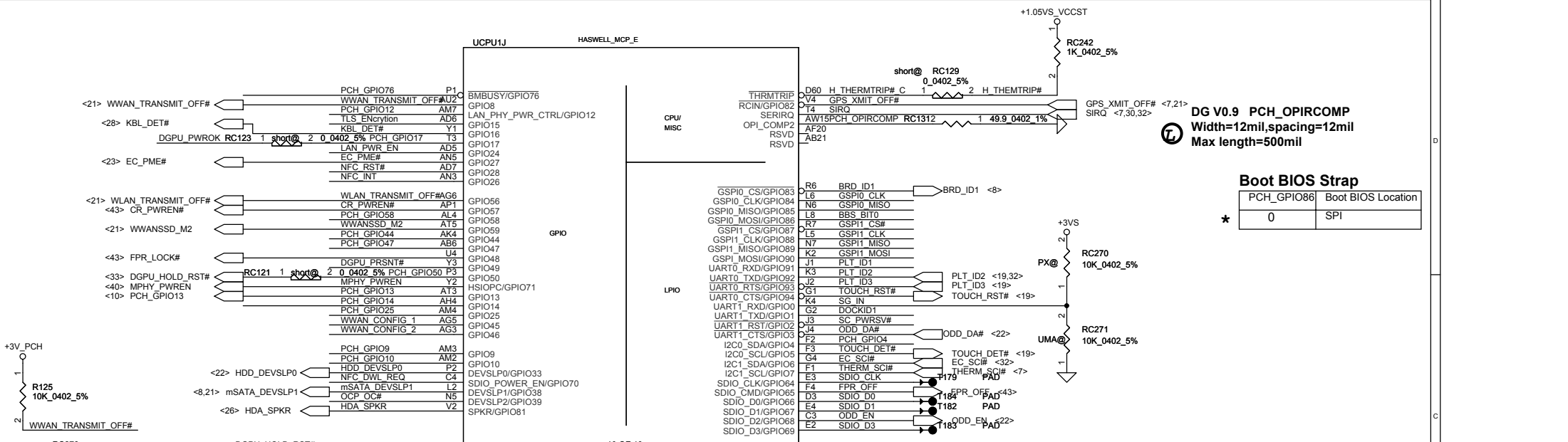


Pinout on customer's board, as in the PDG, CDI #514849

Pin	Pin
1	VccSus3_3
2	SLP_S3#
3	VccDSW3_3
4	SLP_S5#
5	SLP_S4#
6	SLP_A#
7	+3.3DS
8	GND
9	RTCRST#
10	GND
11	PWRBTN#
12	GND
13	SYS_RESET#
14	GND
15	SLP_S0#
16	NC
17	NC
18	NC



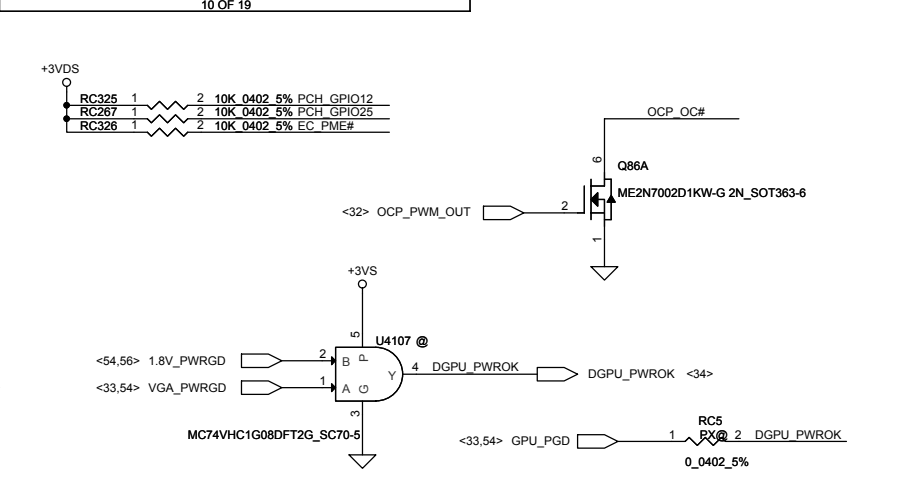
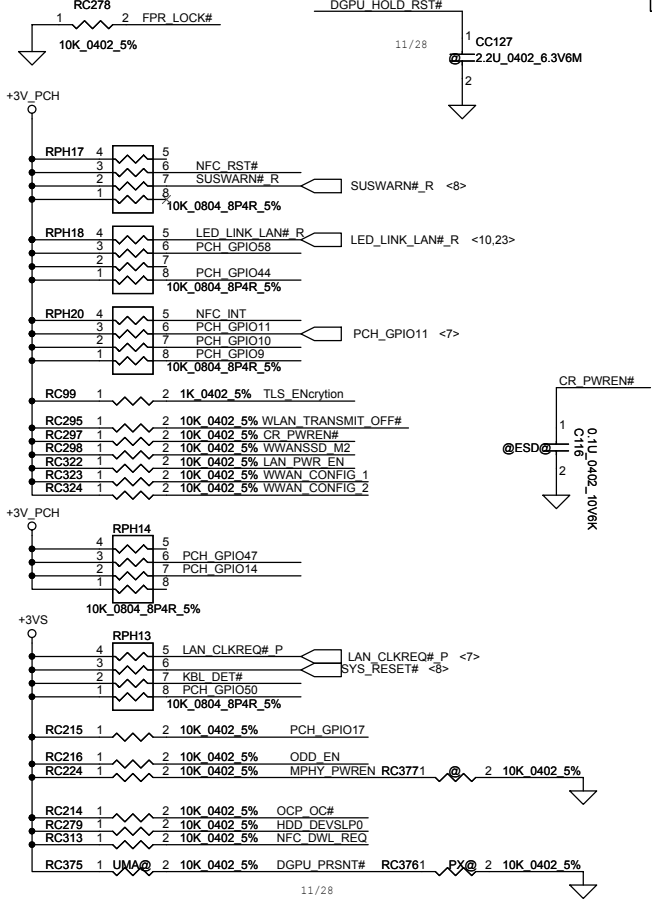
	BRD ID1	BRD ID2	BRD ID3	BRD ID4
Board				
Reversion	GPIO76	GPIO77	GPIO78	GPIO79
0.1	DB0	0	0	0
	DB1	0	0	1
0.2	DB2	0	1	0
0.3		0	1	1
0.4	SI1	0	1	0
	SI1B	0	1	1
	SI2	0	1	0
		0	1	1
0.5	PV1	1	0	0
		1	0	1
		1	0	1
		1	1	0
		1	1	0
		1	1	0
		1	1	1



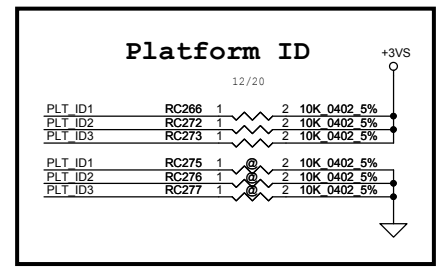
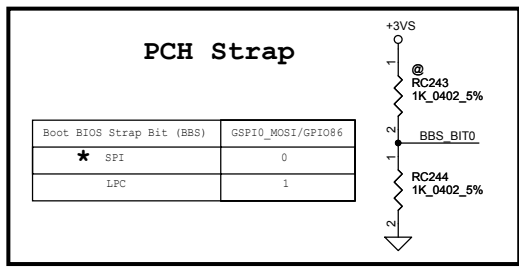
DG V0.9 PCH_OPIRCOMP
 Width=12mil,spacing=12mil
 Max length=500mil

Boot BIOS Strap

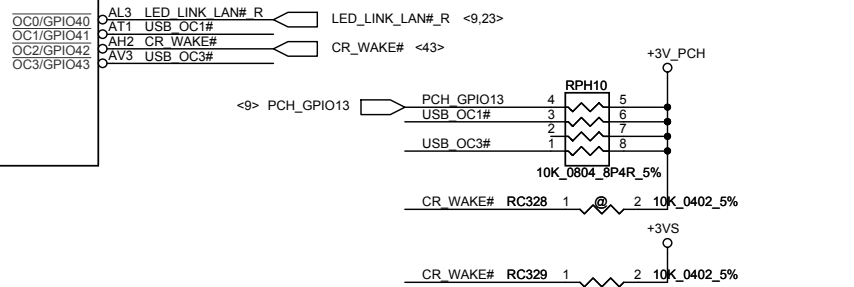
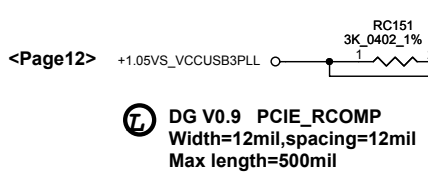
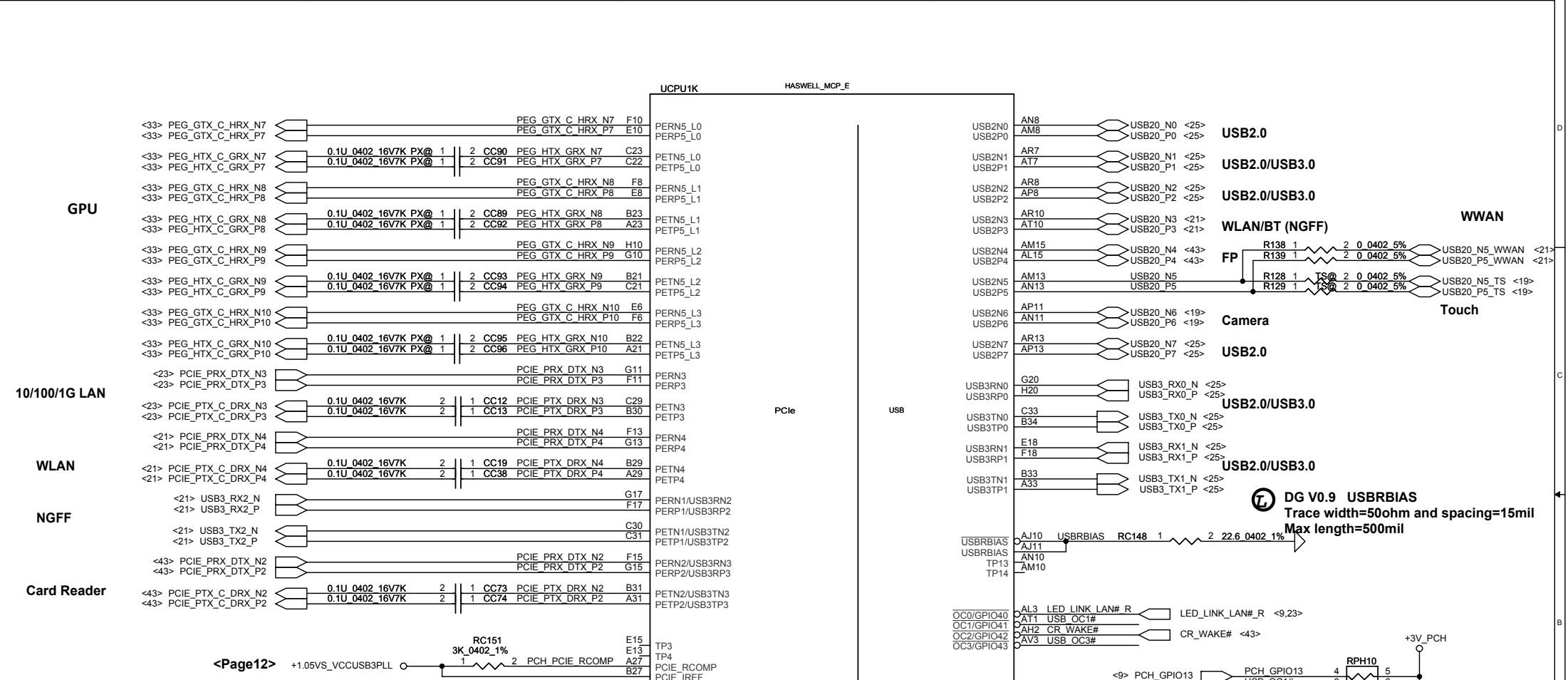
PCH_GPIO86	Boot BIOS Location
0	SPI



TOUCH_RST#	RC274	1	2	10K 0402 5%
DOCKID1	RC284	1	2	10K 0402 5%
SC_PWRSV#	RC287	1	2	10K 0402 5%
SC_PWRSV#	RC289	1	2	10K 0402 5%
ODD_DA#	RC291	1	2	10K 0402 5%
PCH_GPIO4	RC290	1	2	10K 0402 5%
TOUCH_DET#	RC291	1	2	10K 0402 5%
EC_SCI#	RC292	1	2	10K 0402 5%
SDIO_CLK	RC299	1	2	10K 0402 5%
FPR_OFF	RC305	1	2	10K 0402 5%
SDIO D1	RC308	1	2	10K 0402 5%
SDIO D3	RC312	1	2	10K 0402 5%
PCH_GPIO76	RC126	1	2	10K 0402 5%
GSPI0_CLK	RC315	1	2	10K 0402 5%
GSPI0_MISO	RC317	1	2	10K 0402 5%
GSPI1_CS#	RC318	1	2	10K 0402 5%
GSPI1_CLK	RC319	1	2	10K 0402 5%
GSPI1_MISO	RC320	1	2	10K 0402 5%
GSPI1_MOSI	RC321	1	2	10K 0402 5%

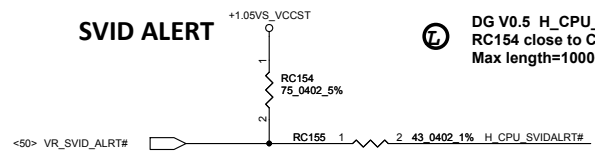


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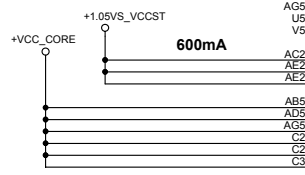
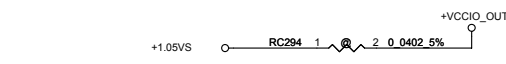
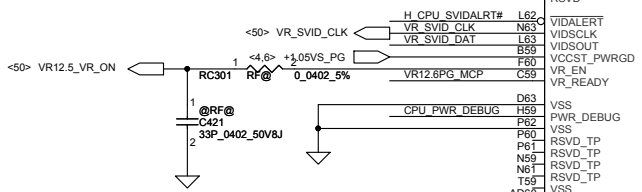
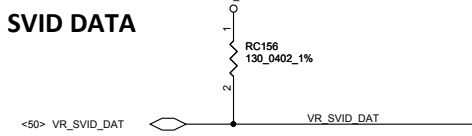
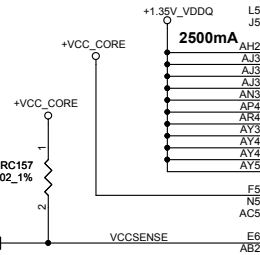
+VCC_CORE@1000mA



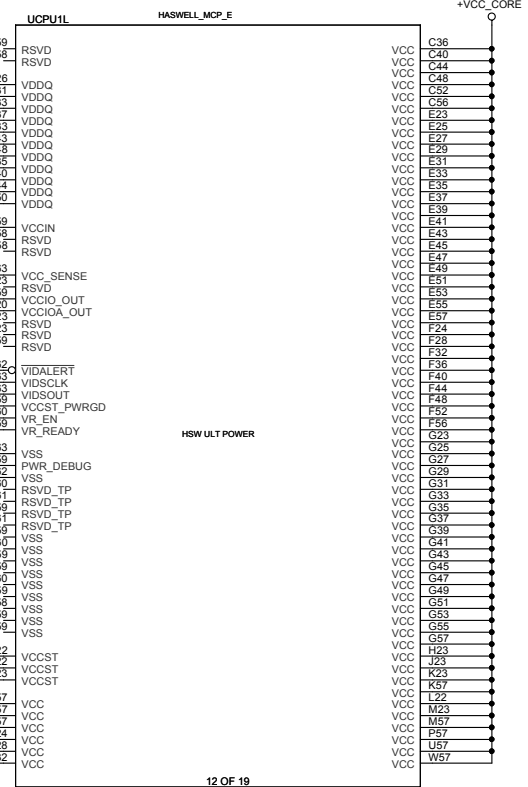
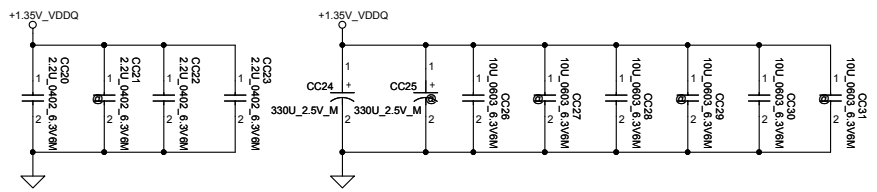
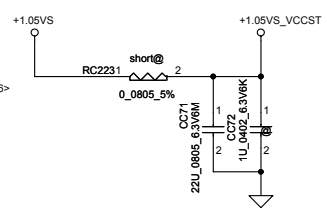
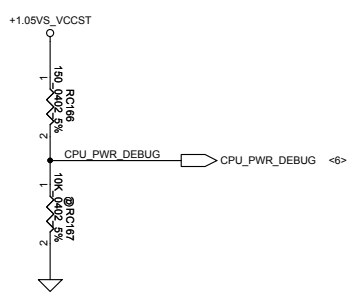
DG V0.5 H_CPU_SVIDALRT#
RC154 close to CPU<300mil
Max length=1000-2000mil

VCC_SENSE

<50> VCCSENSE

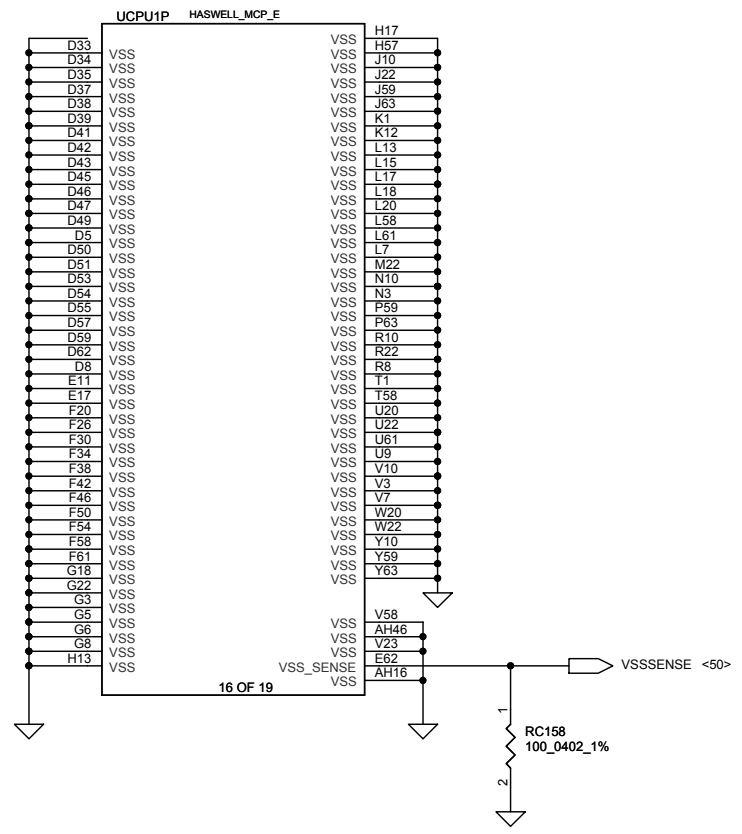
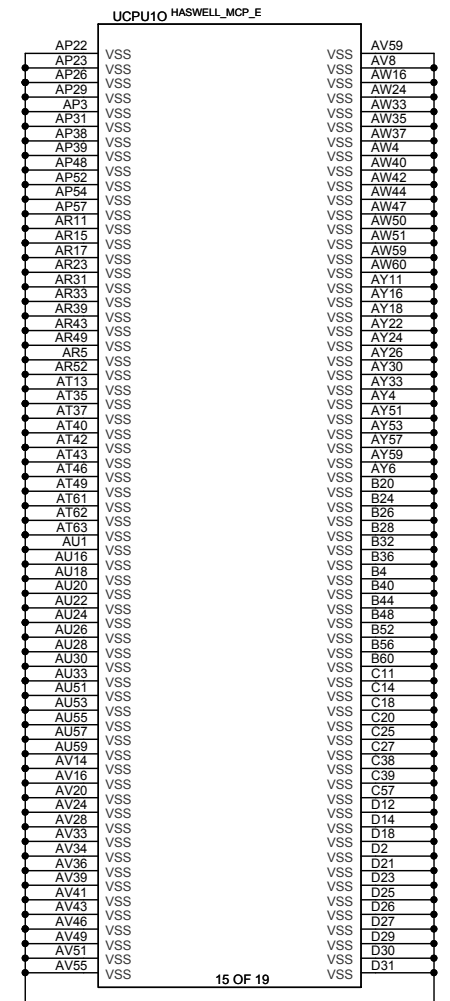
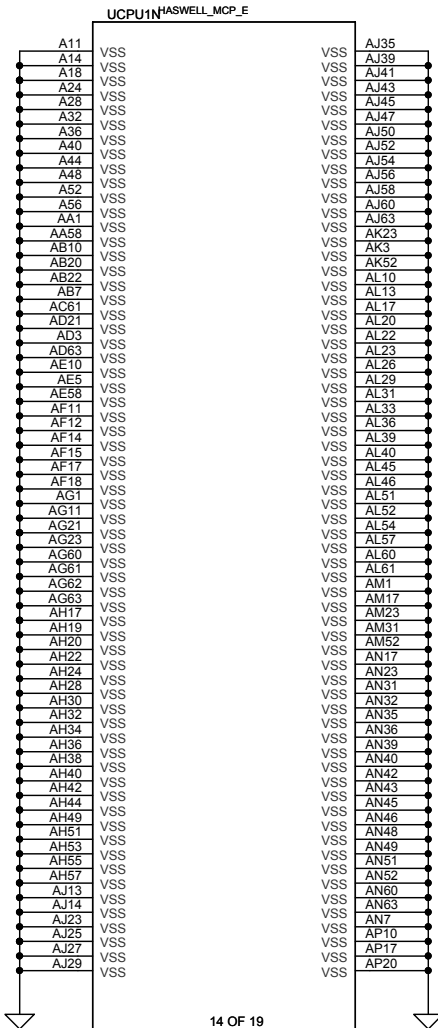


DG V0.5 VIDSOUT
RC156 close to CPU<500mil
Max length=1000-2000mil

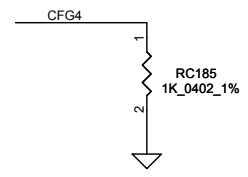
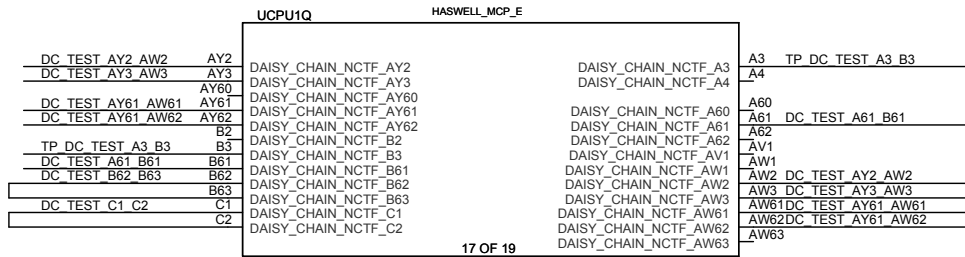


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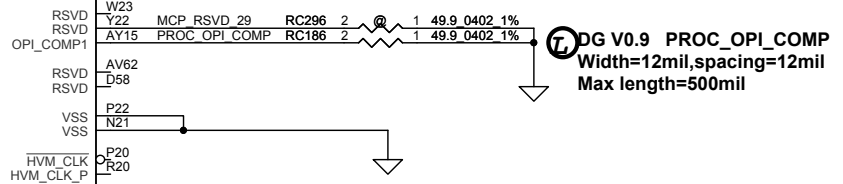
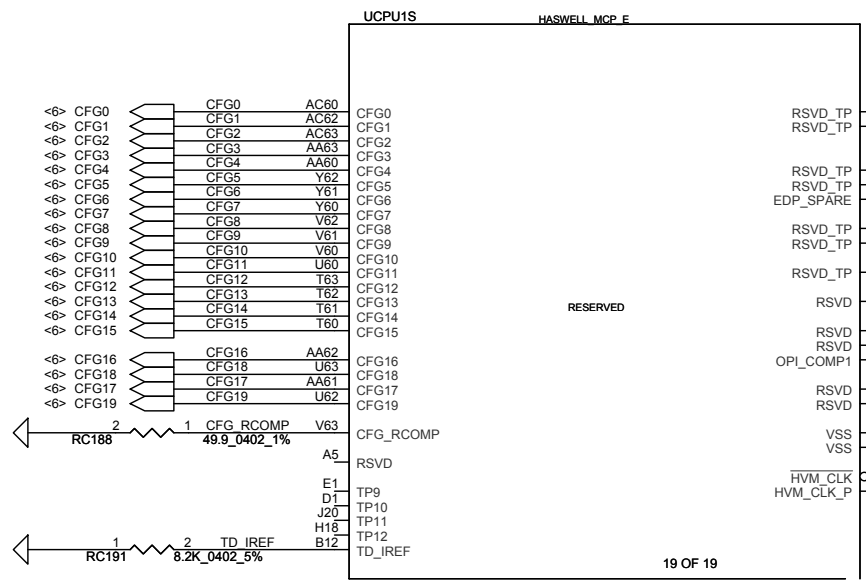
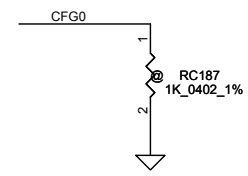
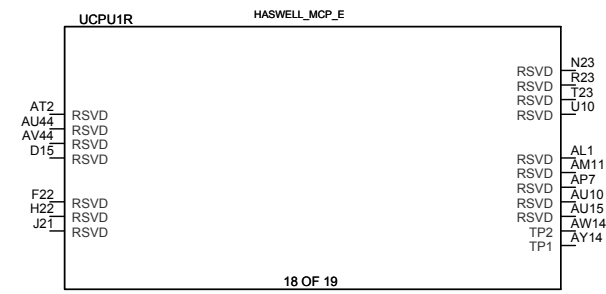


Display Port Presence Strap

CFG4



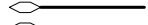

1 : Disabled; No Physical Display Port attached to Embedded Display Port

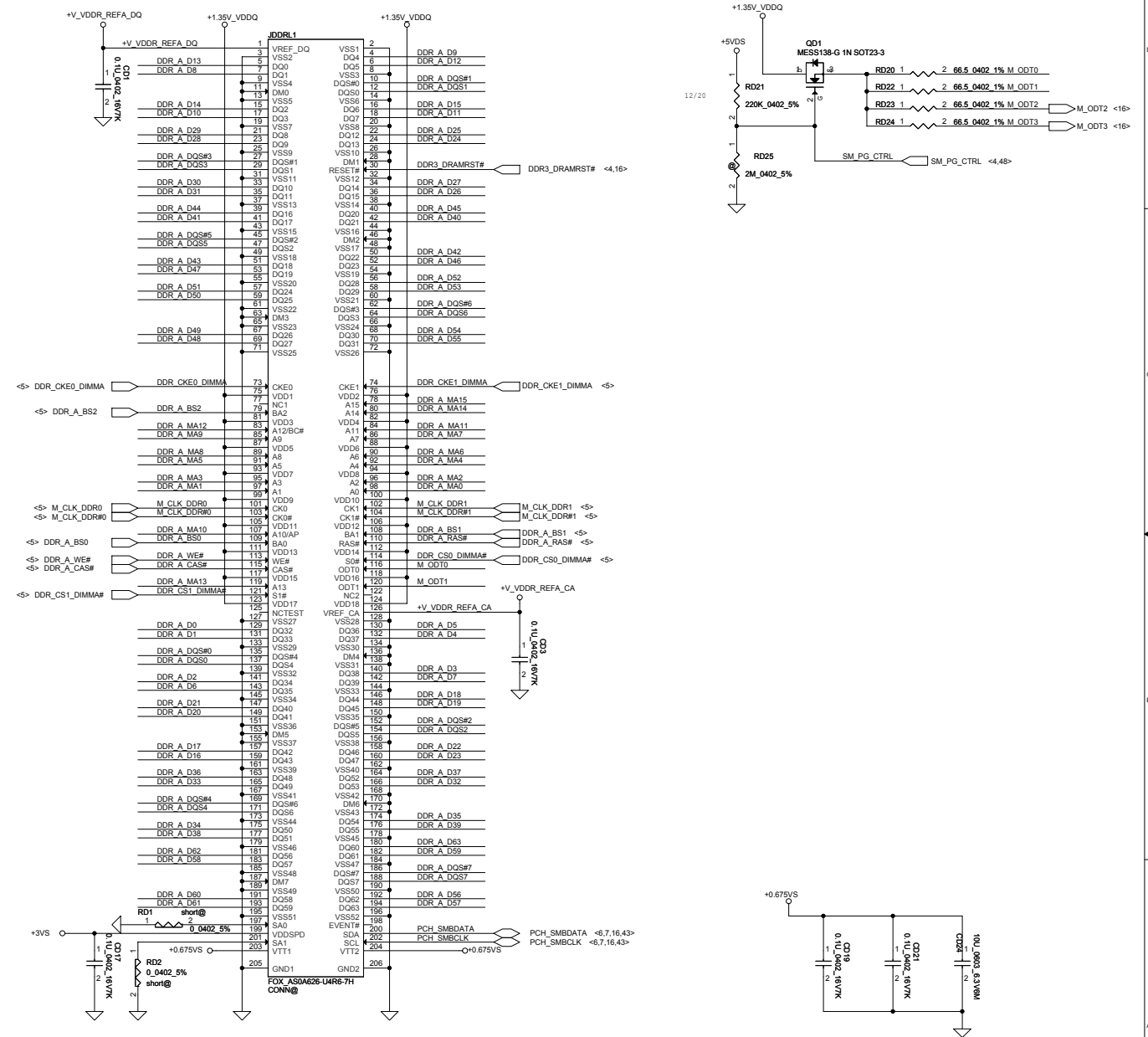
* 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



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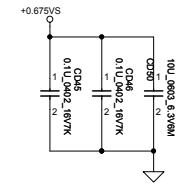
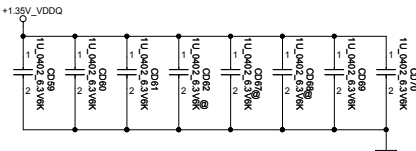
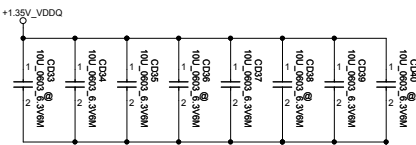
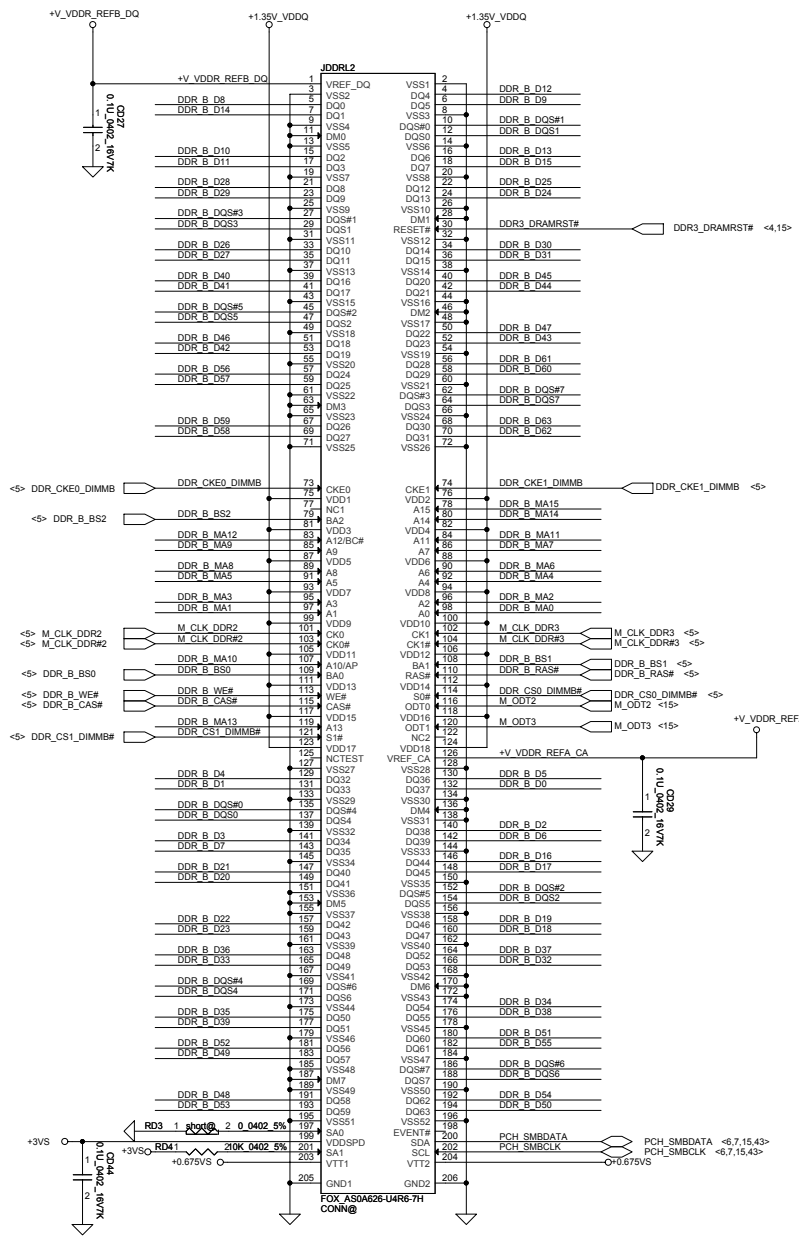
Rev 0.5

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 <S> DDR_A_DQS[0..7] 
 <S> DDR_A_MA[0..7] 
 <S> DDR_A_MA[0..15] 



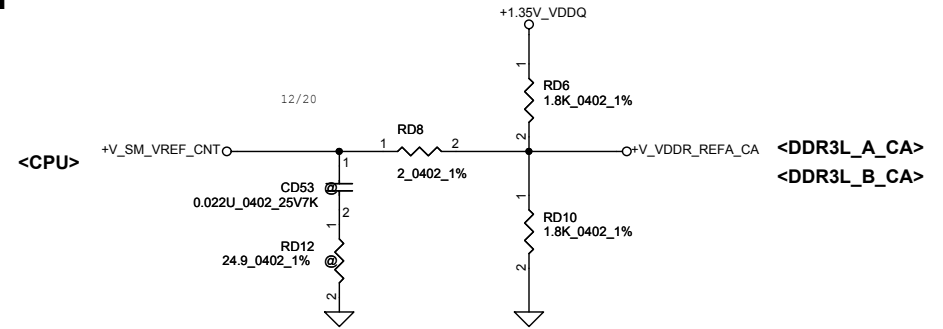
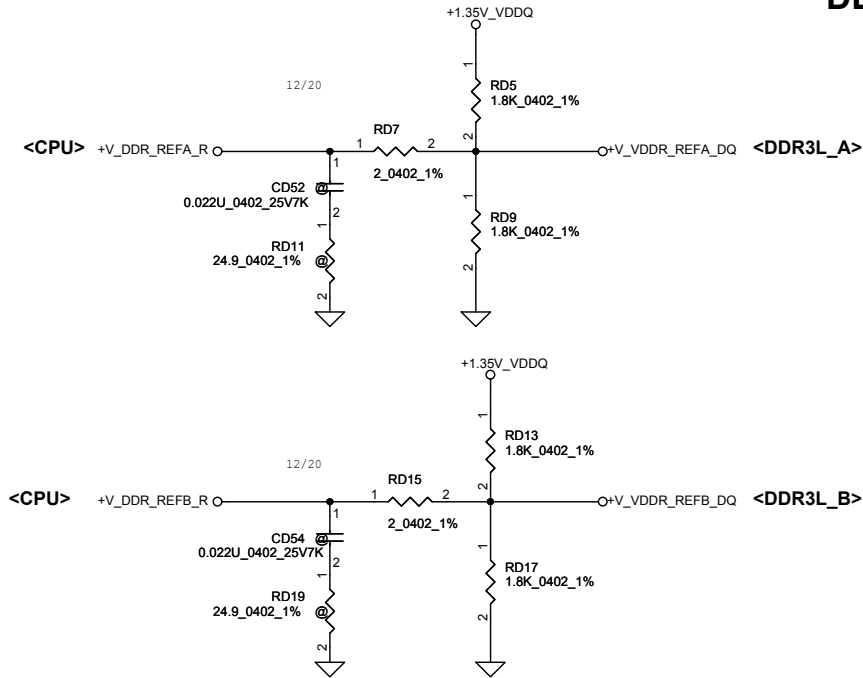
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Issued Date	2011/06/29	Deciphered Date	2011/06/29
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- <-> DDR_B_D[0..63]
- <-> DDR_B_DQS[0..7]
- <-> DDR_B_DQS#[0..7]
- <-> DDR_B_MA[0..15]

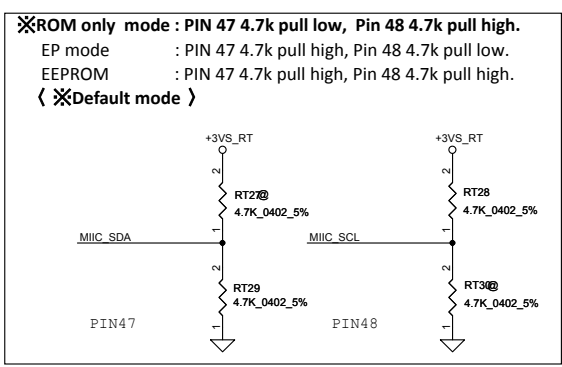
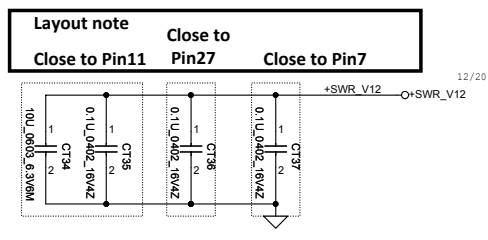
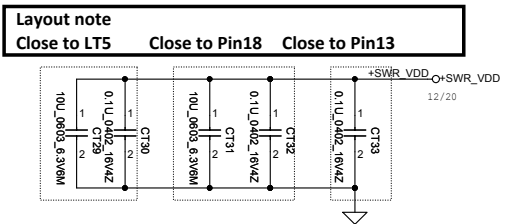
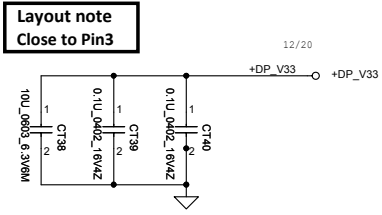
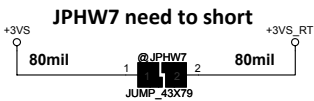


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DDR3L VREF



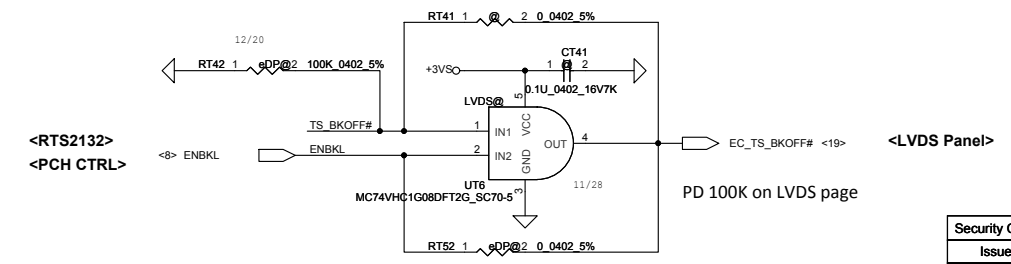
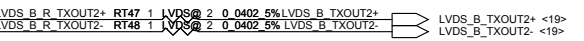
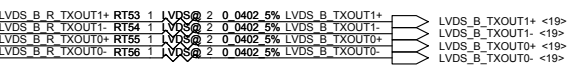
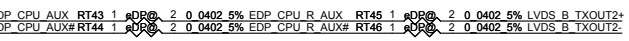
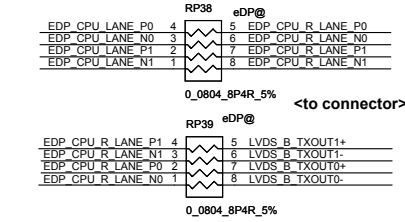
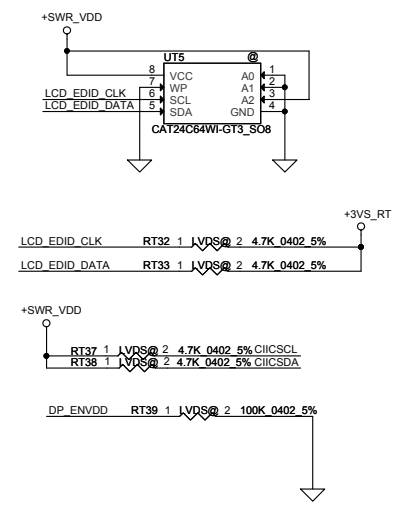
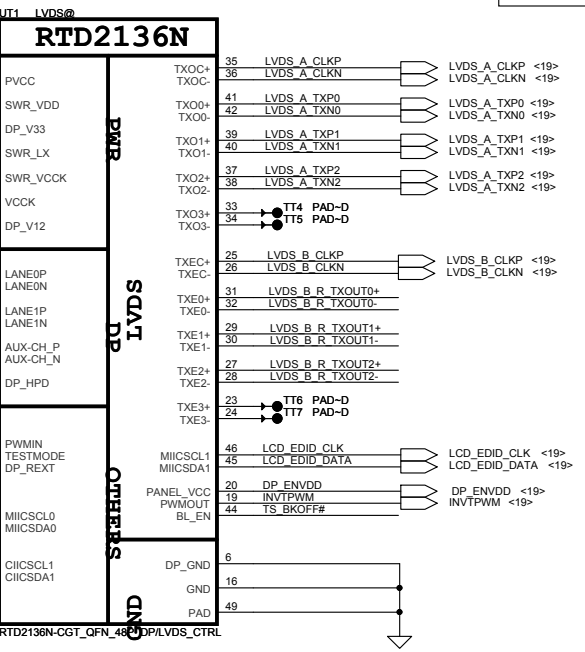
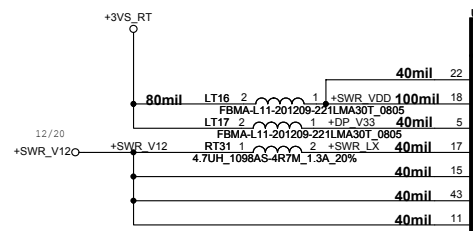
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Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	DDR3L VREF
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SWR / LDO Mode select

	LDO	SWR
2132S	Do not support	mount LT7
2132R	Use 0 ohm	mount LT7

⊗ If use 2132R, please select LDO mode as default.



	PIN15	PIN16	Accept voltage input (high level)
2132S	TL_ENVDD	2132S	3.3V
2132R	+LCD_VDD *	2132R	1.5-3.3V

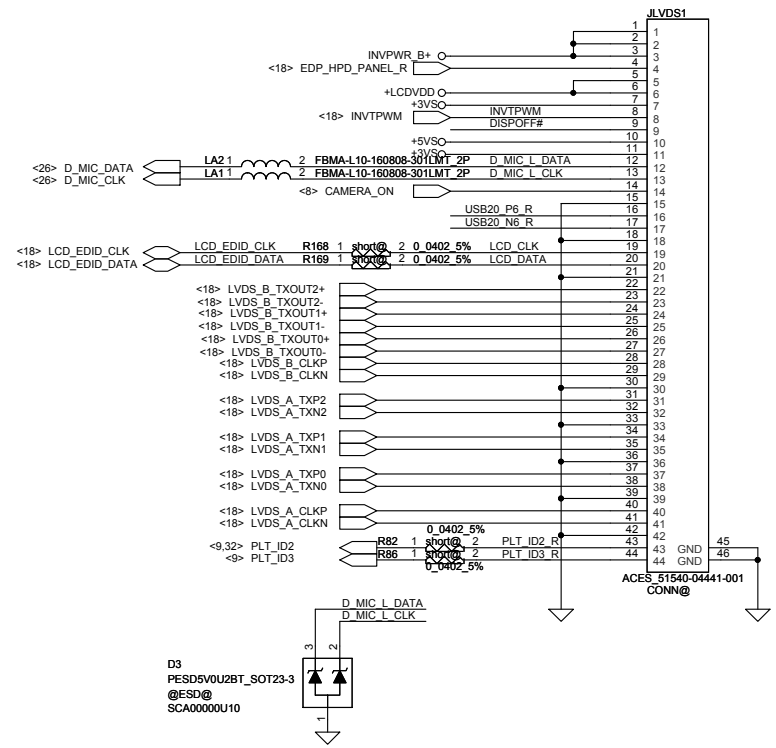
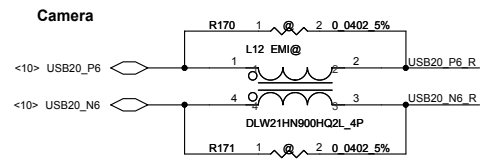
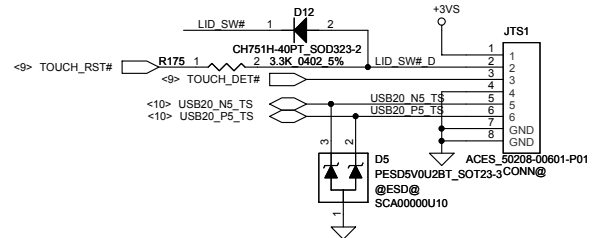
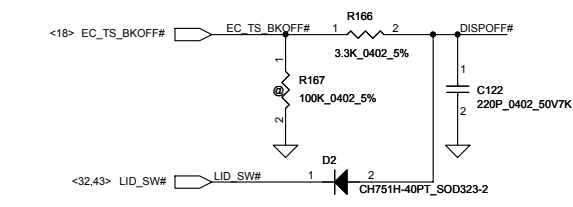
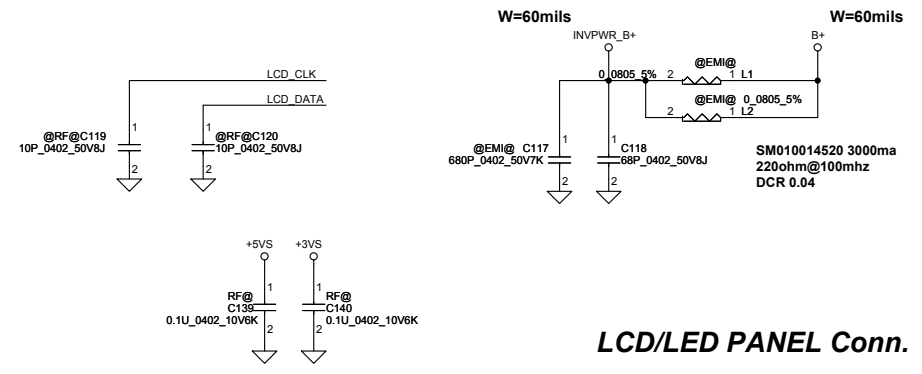
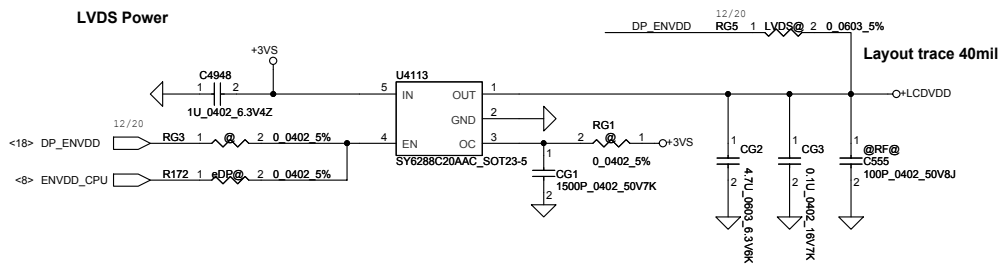
* Version R internal Power Switch, can output 1A, Rds(on)=0.2 ohm

* Version R has internal level shifter, remove level shifter circuit on AMD platform

Different between 2132S and 2132R

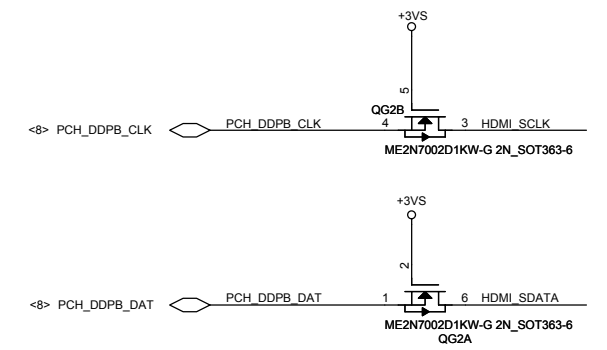
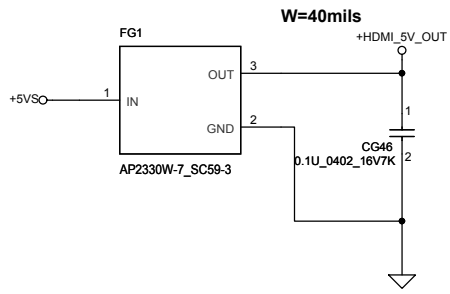
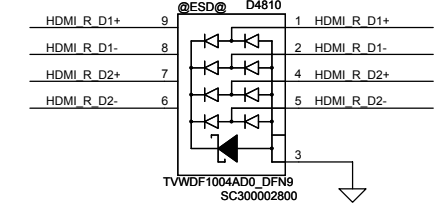
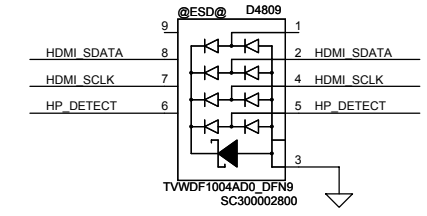
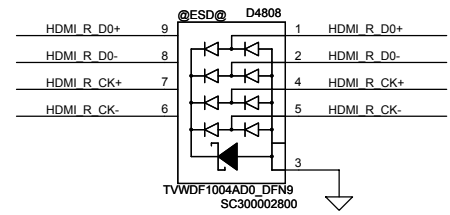
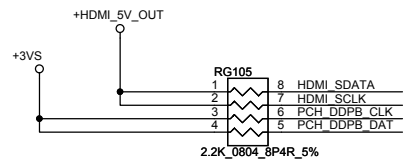
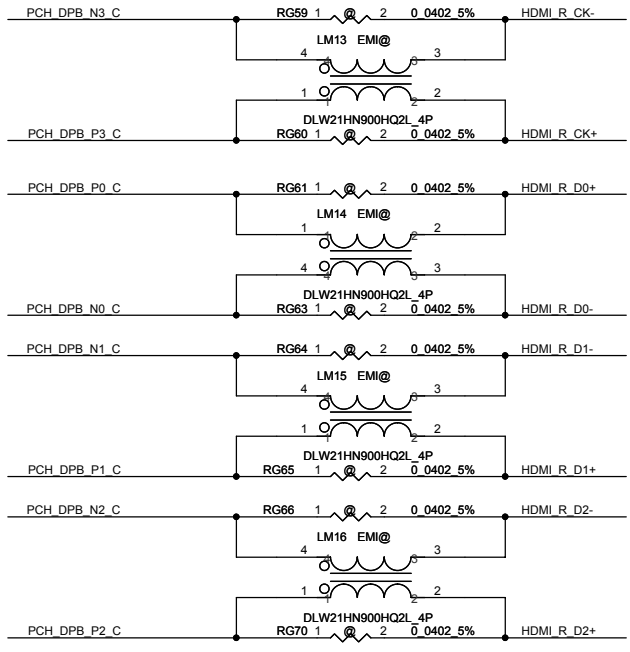
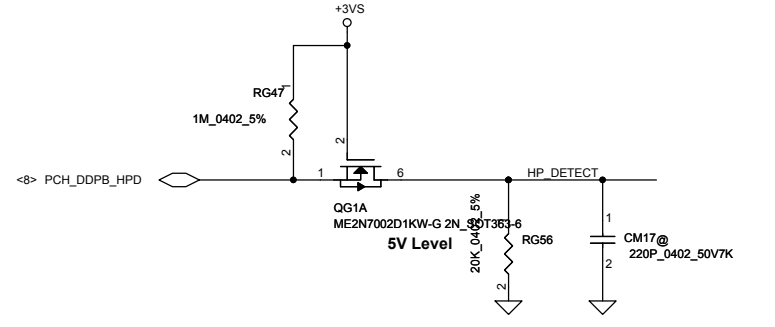
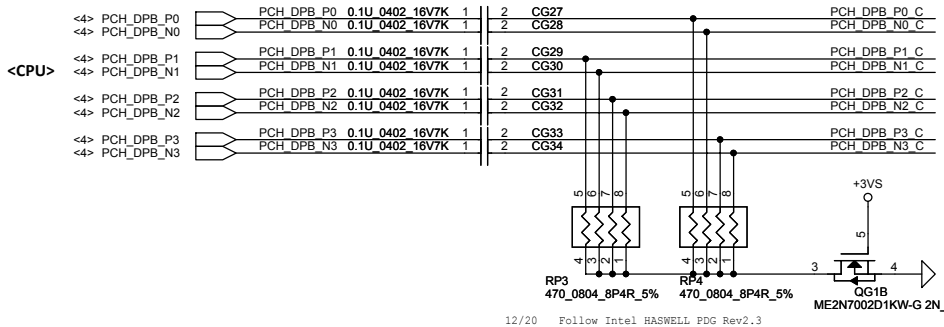
2132S	2132R
1. Support SWR mode	1. Support LDO mode and SWR mode 2. Internal ROM 3. Support LCD_VDD(internal Power switch) 4. Integrates Level shifter

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				LVDS Translator-RTD2132R
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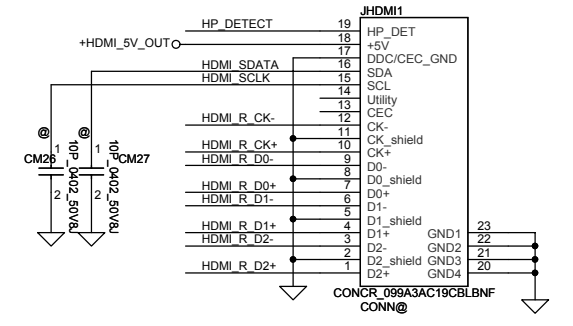
	GPI092 PLT_ID2	GPI093 PLT_ID3
Rolo 14"	0	1
Reeses 15"	1	0
Raisinnet 17"	1	1

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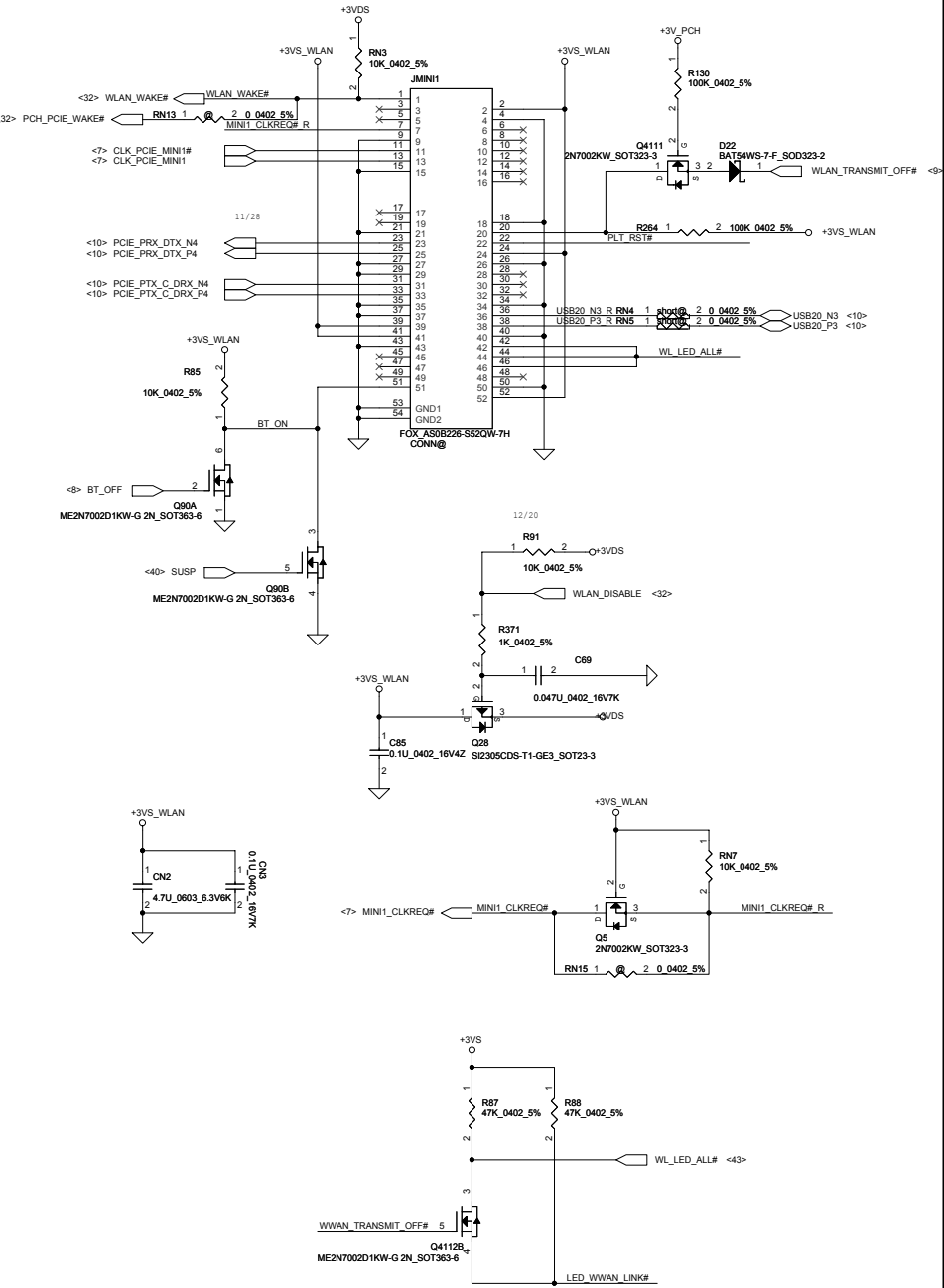
5V PULL UP IN CONNECTER SIDE

HDMI Conn.

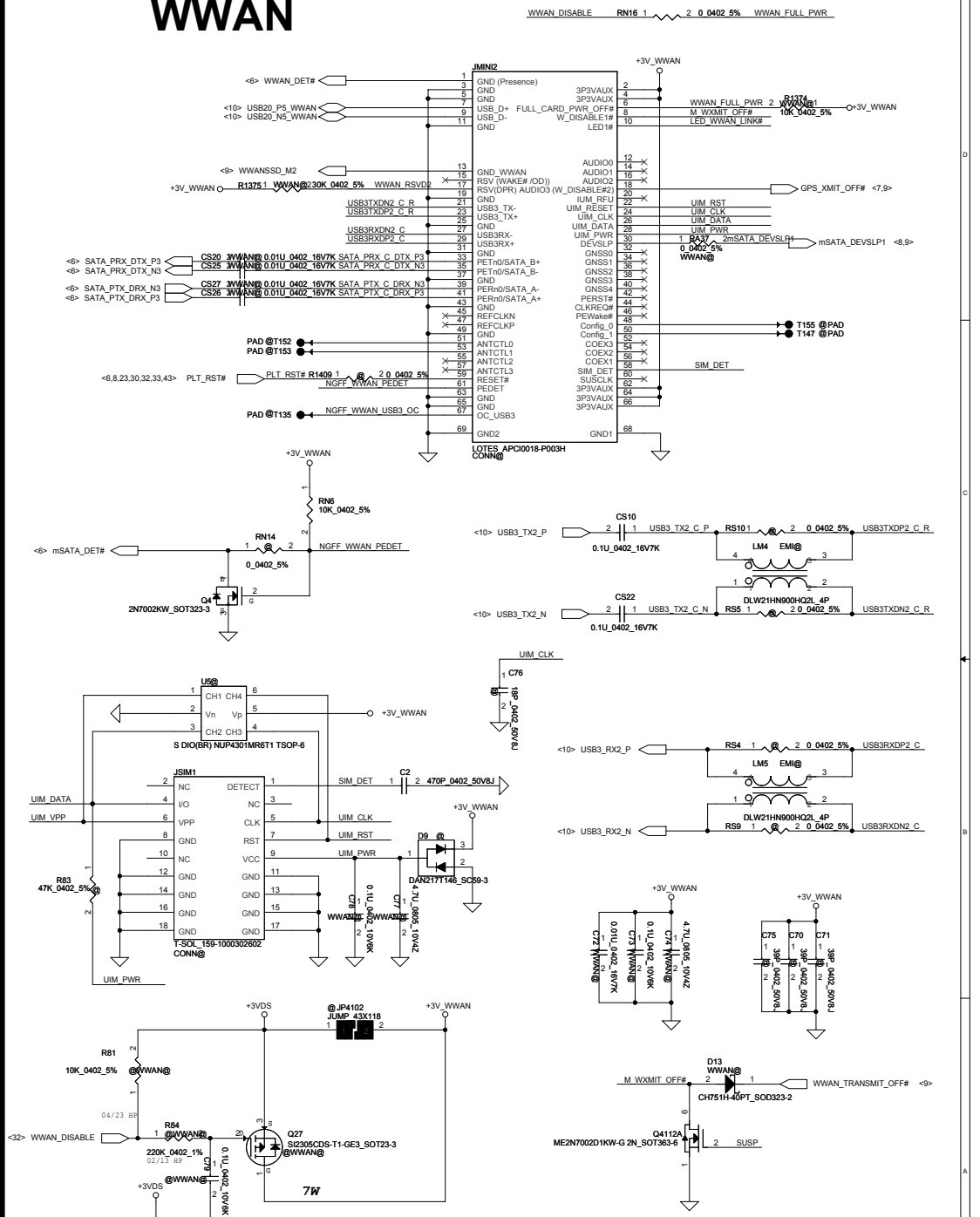


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Issued Date	2011/06/29	Deciphered Date	2011/06/29	HDMI Conn/Level shift	
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WLAN

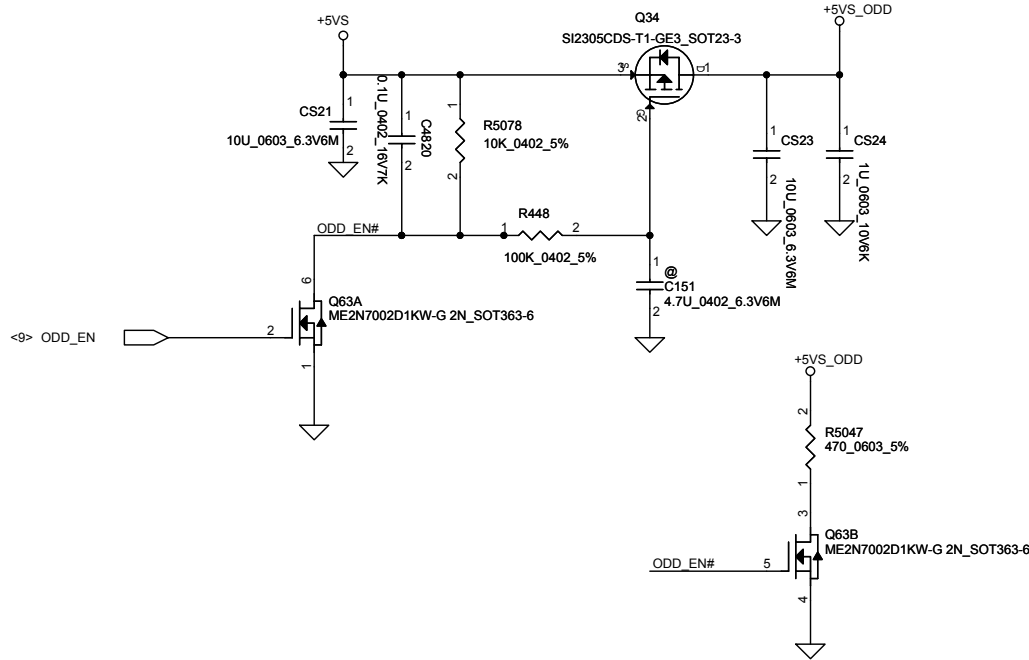
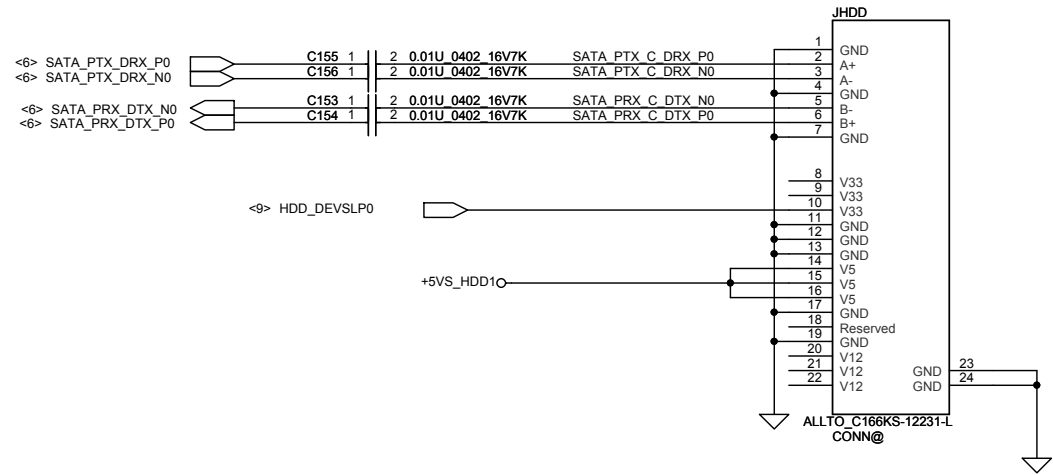
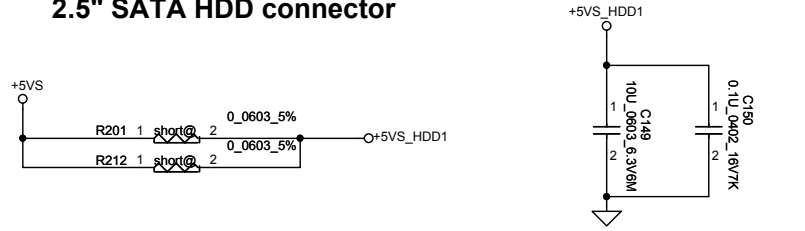


WWAN

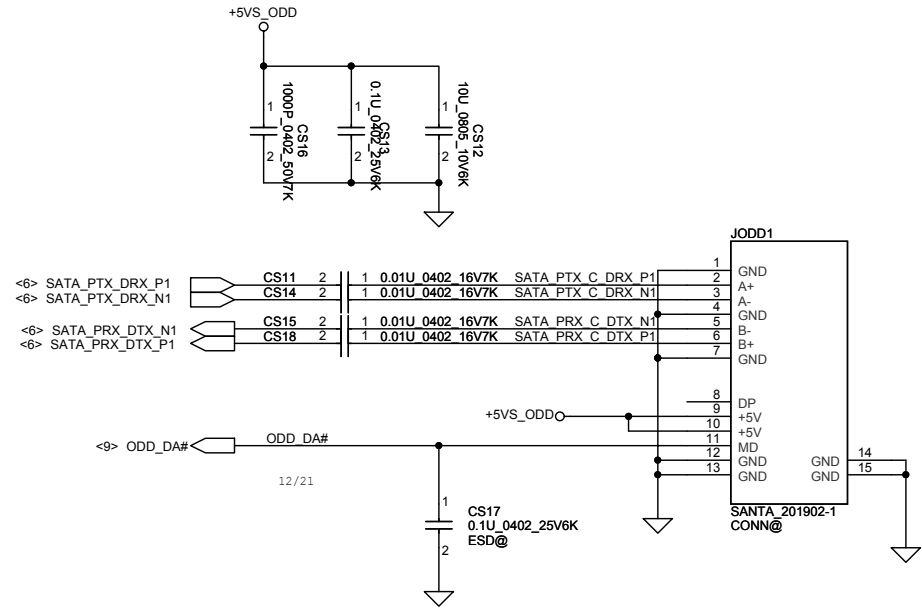


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				WLAN	Rev 0.5
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2.5" SATA HDD connector

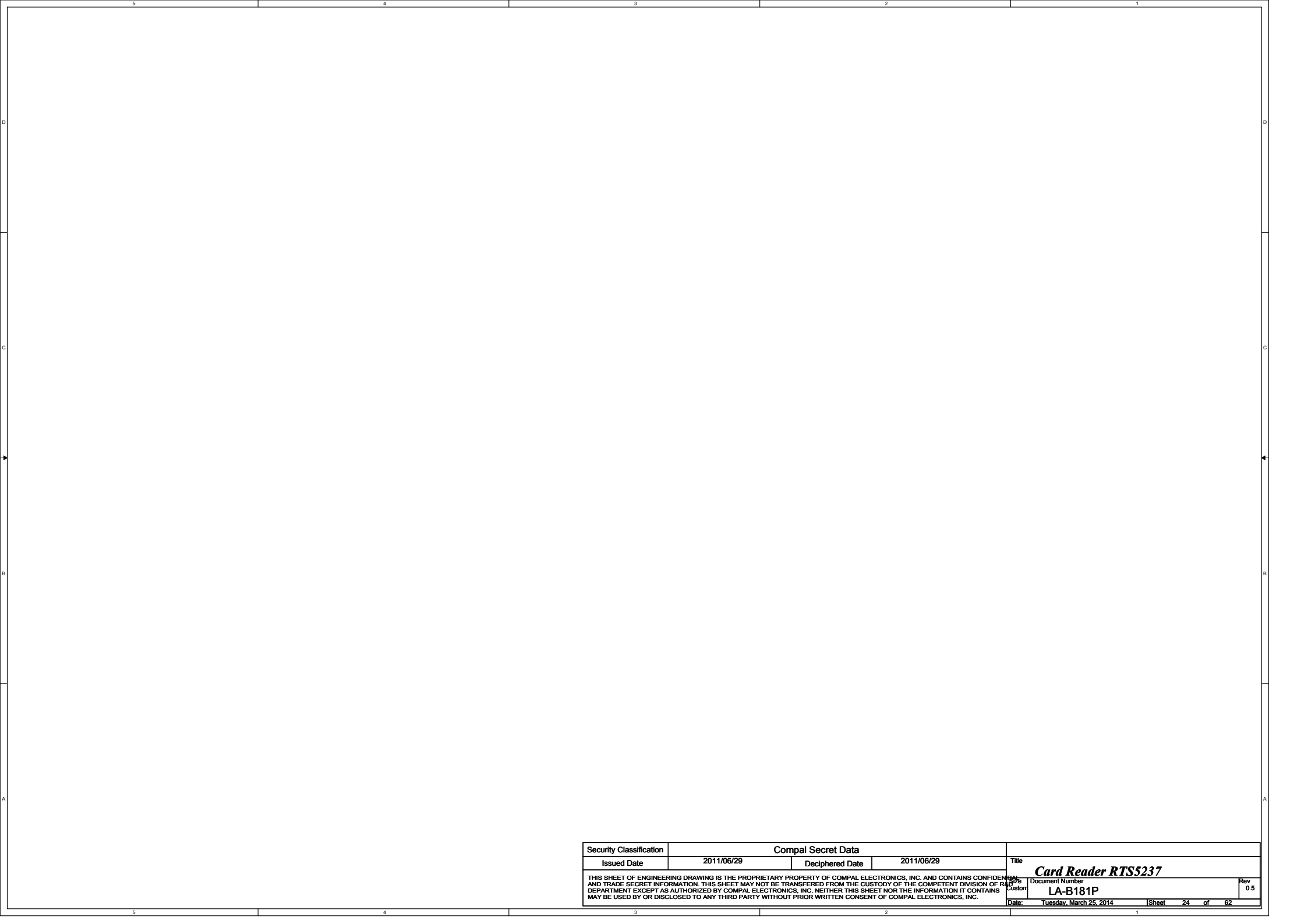


Place near ODD Connector



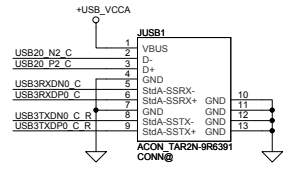
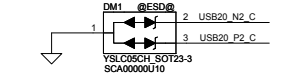
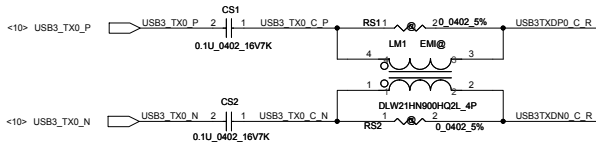
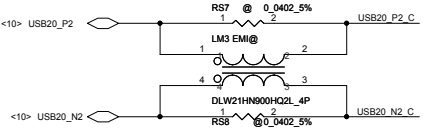
12/20 Customer change GPIO table

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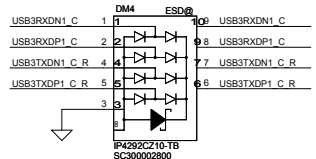
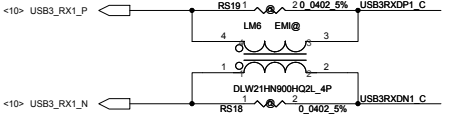
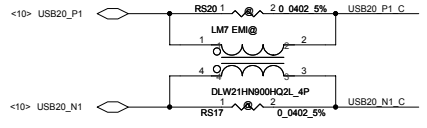
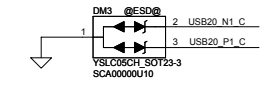
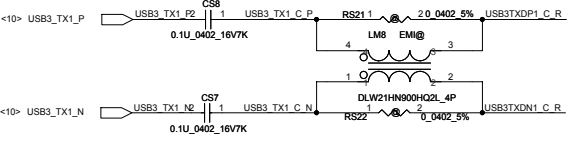
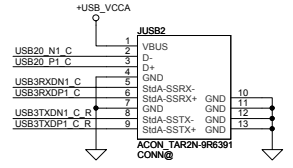
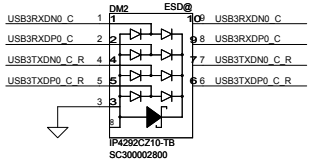
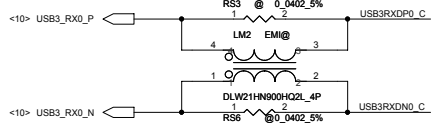
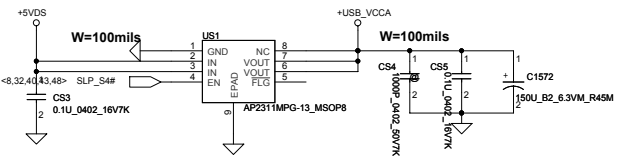


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<small>Date:</small> Tuesday, March 25, 2014			<small>Rev</small> 0.5 <small>Sheet</small> 24 of 62

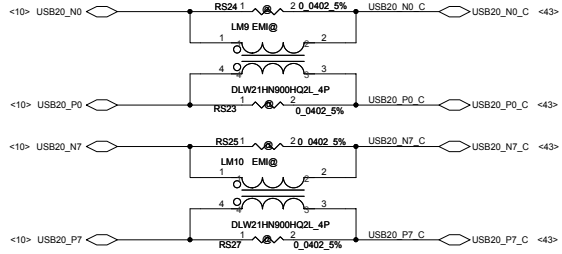
USB3.0



USB3.0 need support 2.5A
change USB PWR SW SA00003TV00
low active



USB2.0



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Issued Date	2012/03/23	Deciphered Date	2012/10/21	Title
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4

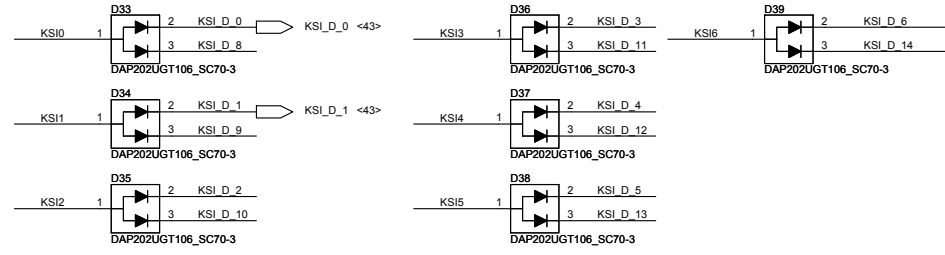
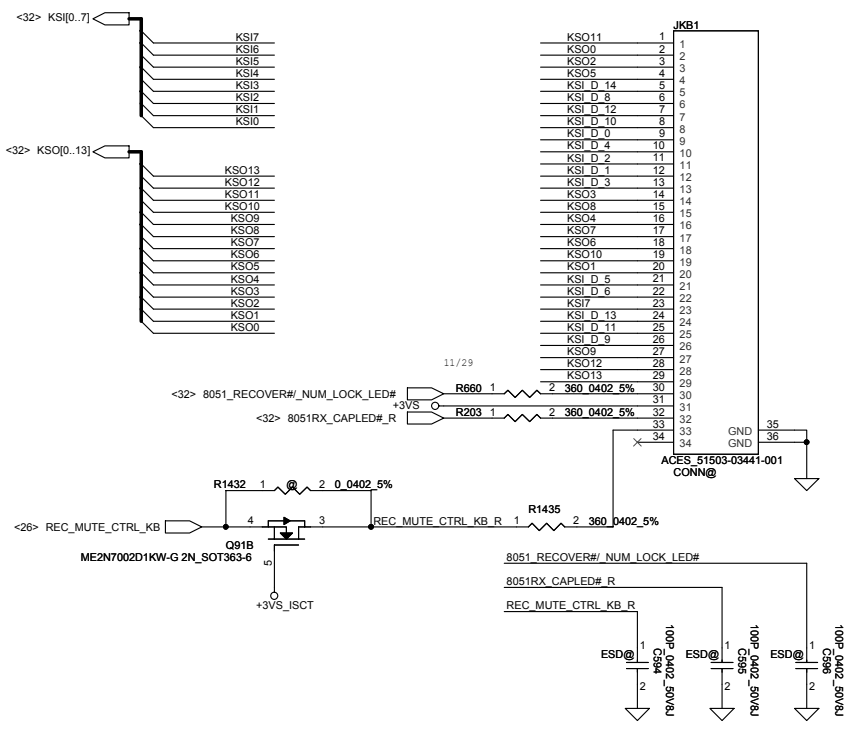
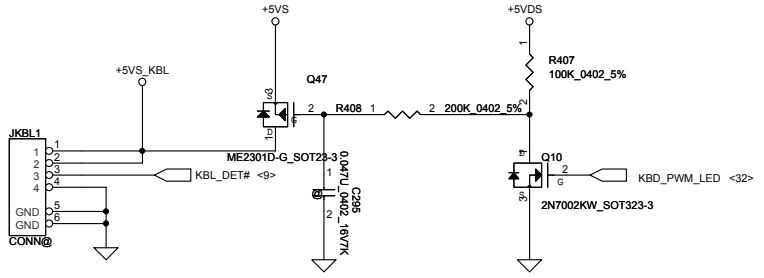
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2

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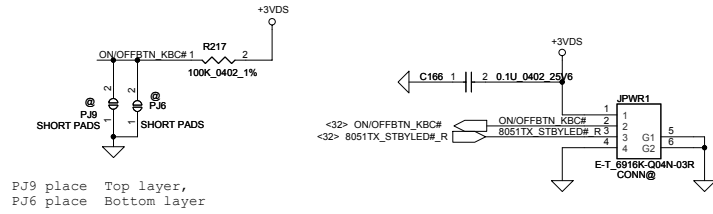
Keyboard conn

KB backlight Conn

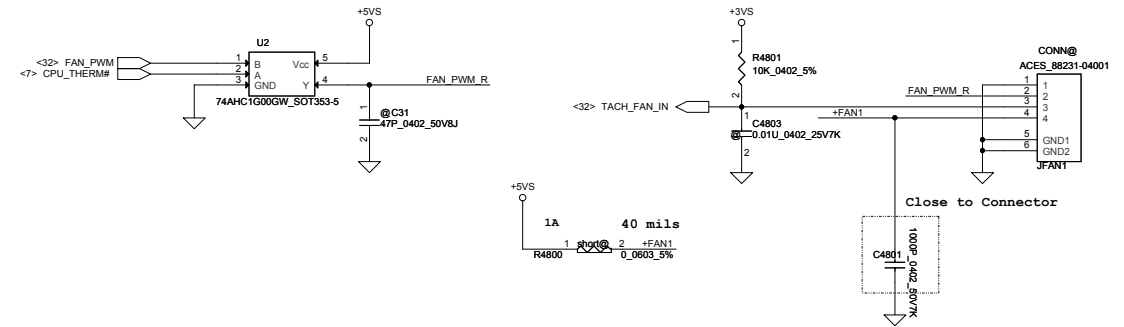


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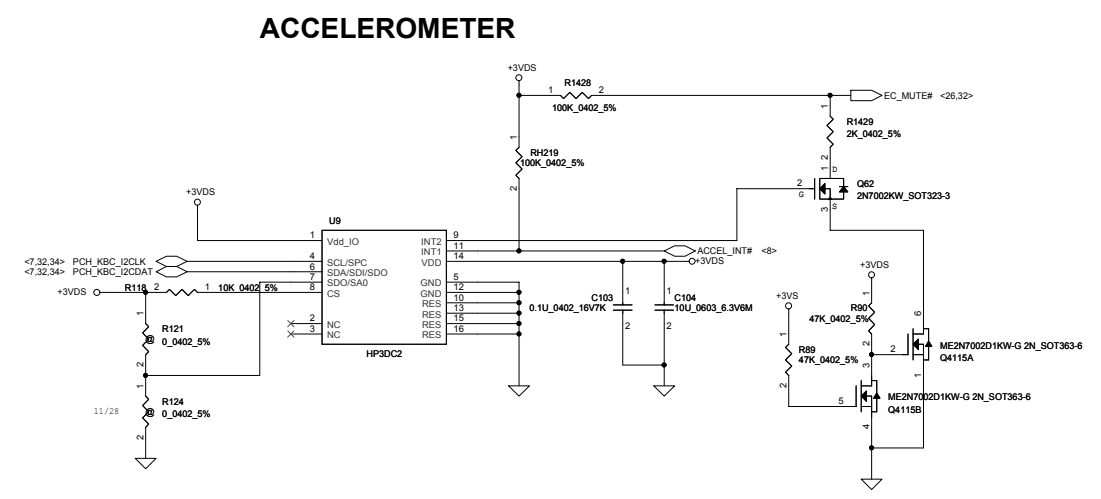
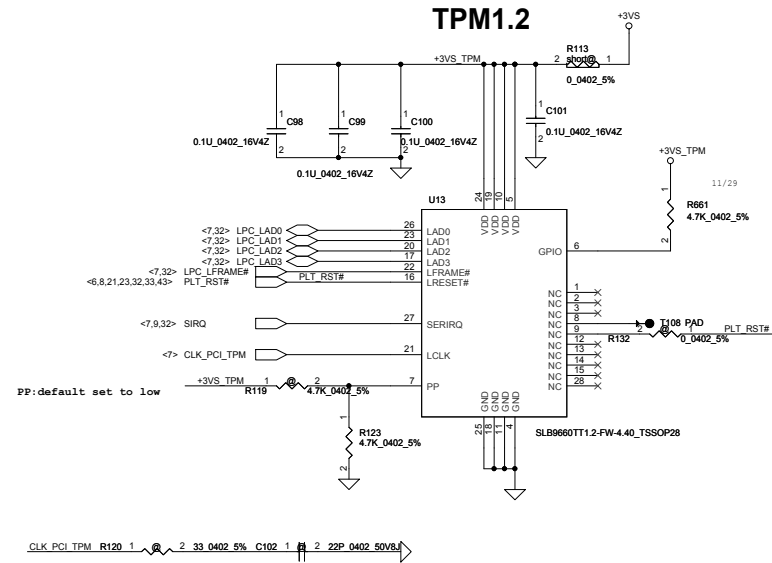
Power Button Connector



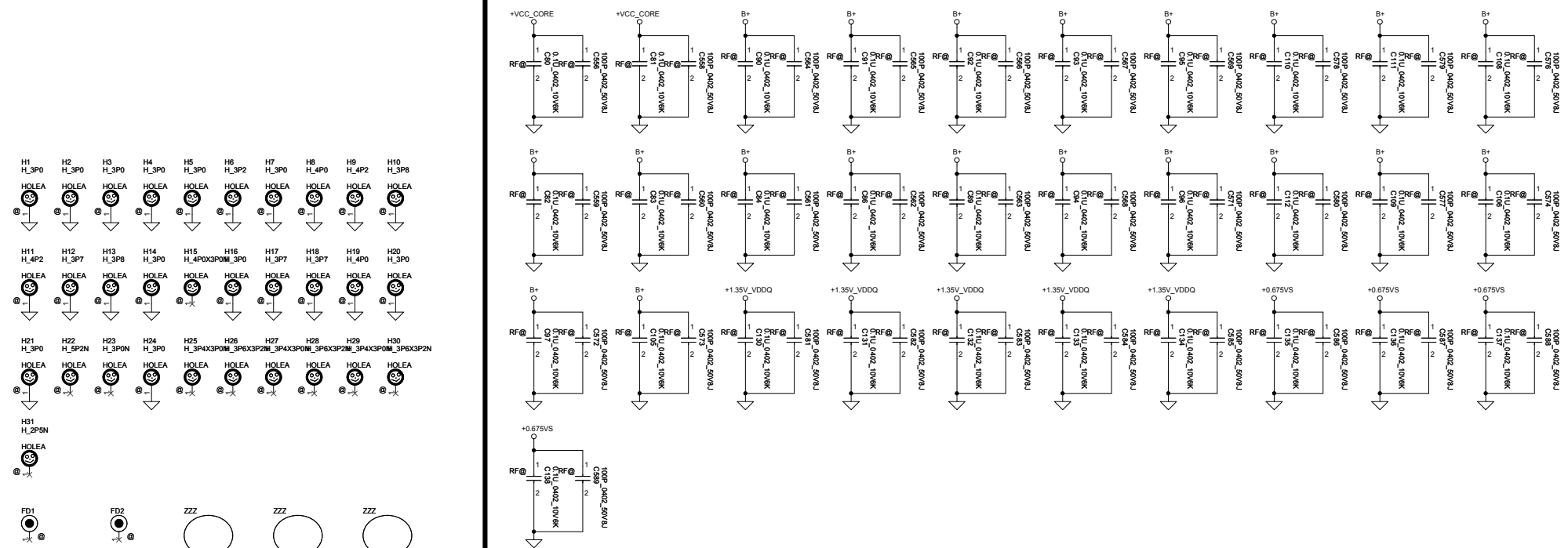
Fan Control Circuit



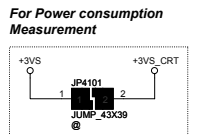
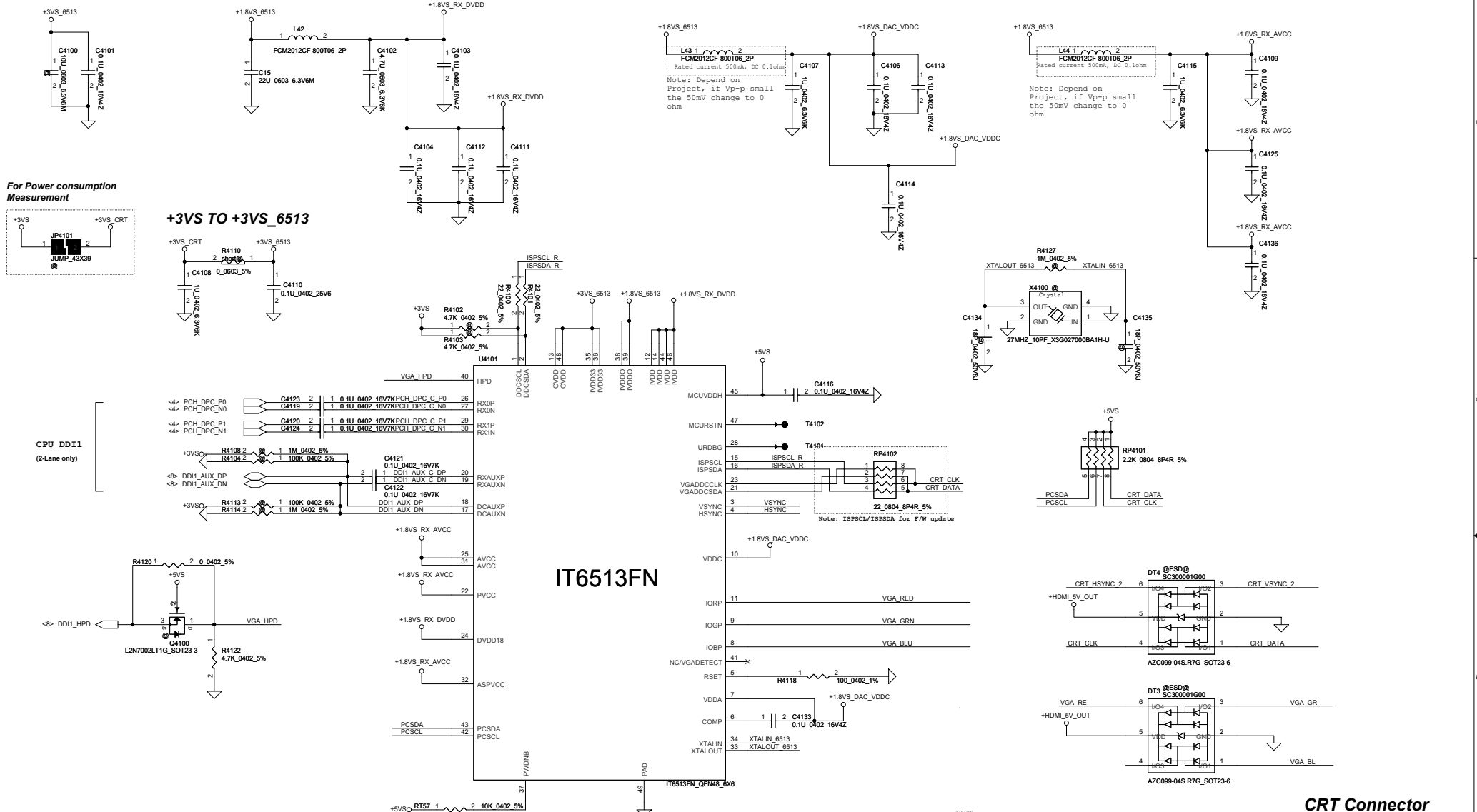
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RF CAP



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CPU DD11 (2-Lane only)

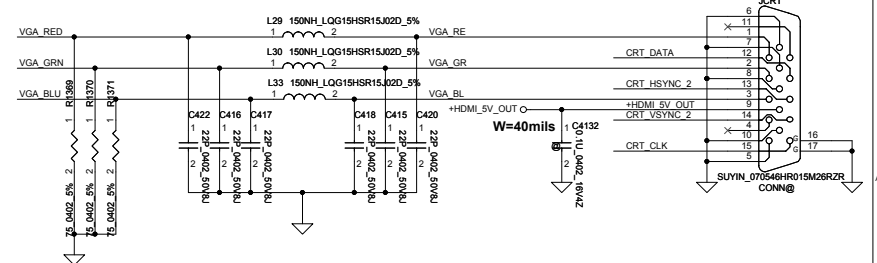
<8> DD11_HPDP

12/20

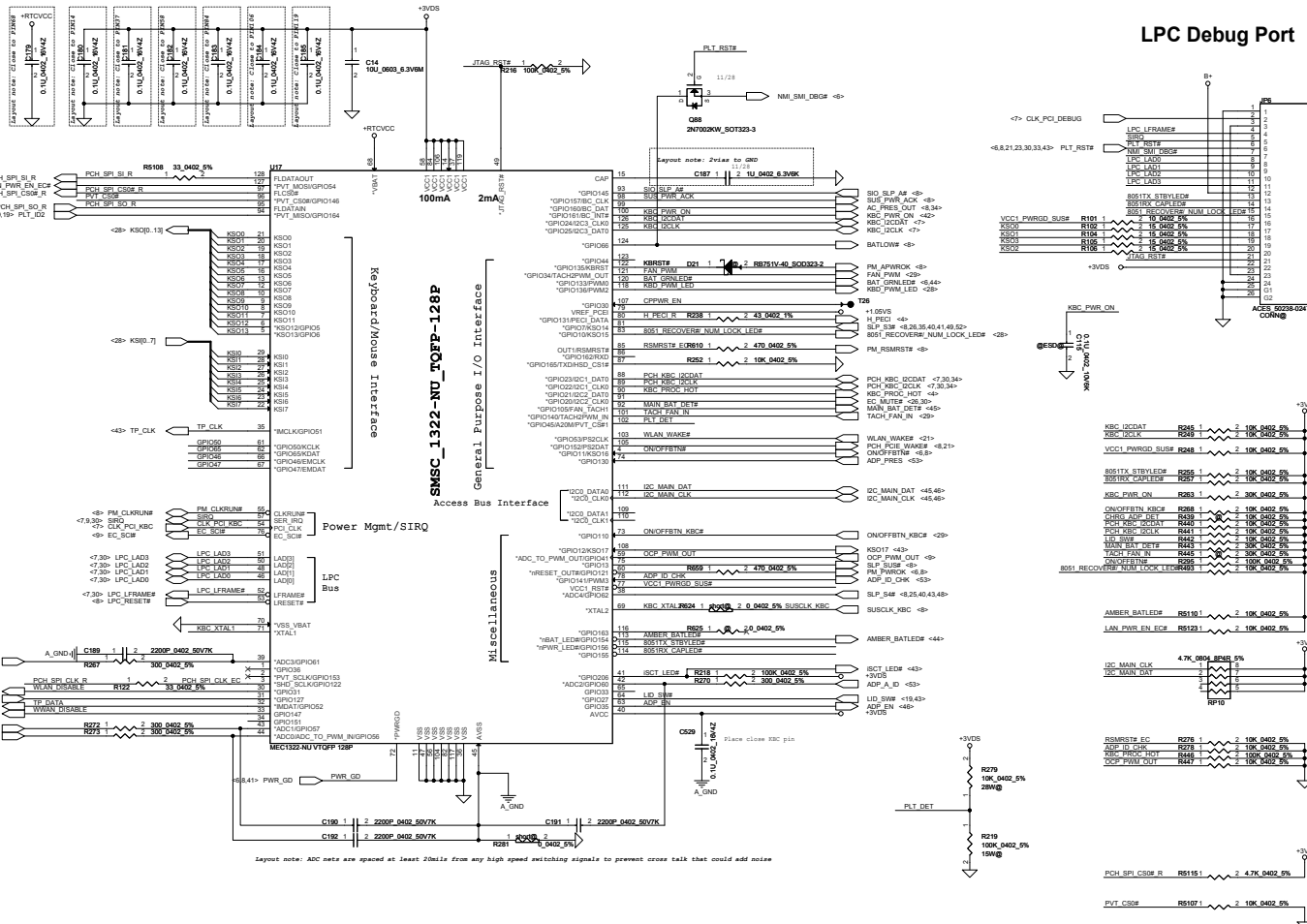
12/20

IT6513FN

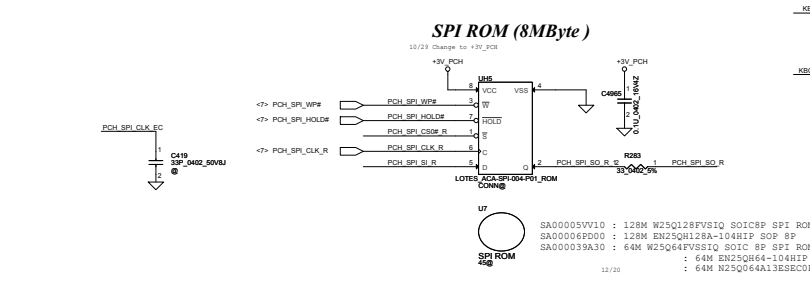
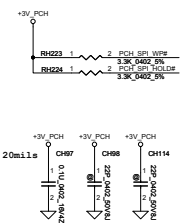
CRT Connector



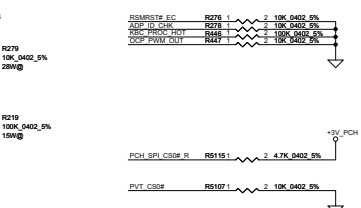
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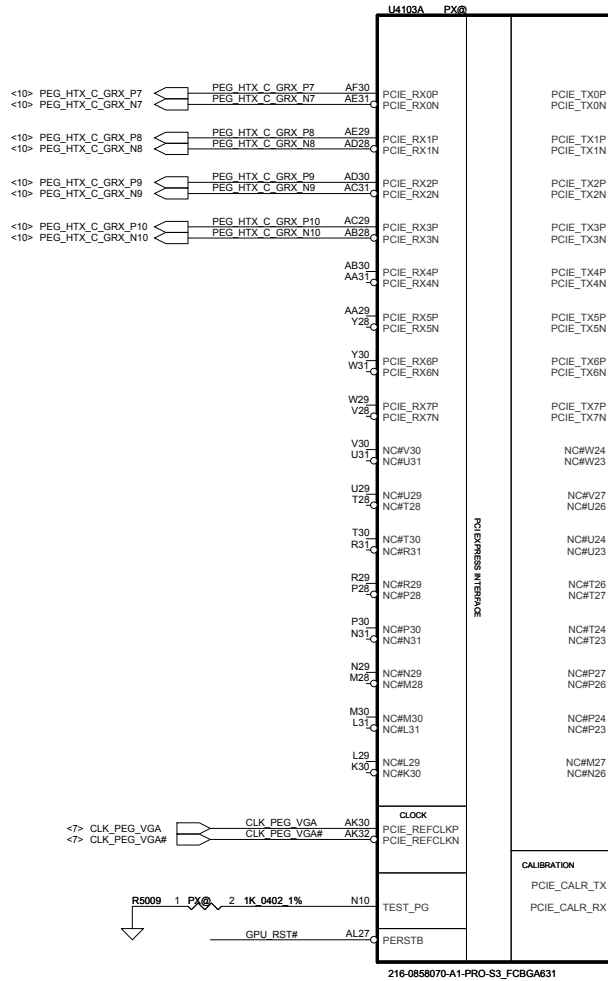
Layout note: ADC nets are spaced at least 20mil from any high speed switching signals to prevent cross talk that could add noise



SA00005V10 : 128M W25Q128FVSIQ SOIC8P 8P ROM
 SA00006P00 : 128M N25Q64128A-10481P SOP 8P
 SA000039A30 : 64M W25Q64FVSIQ SOIC 8P SPI ROM
 : 64M N25Q64-10481P
 : 64M N25Q64A13B3E0P

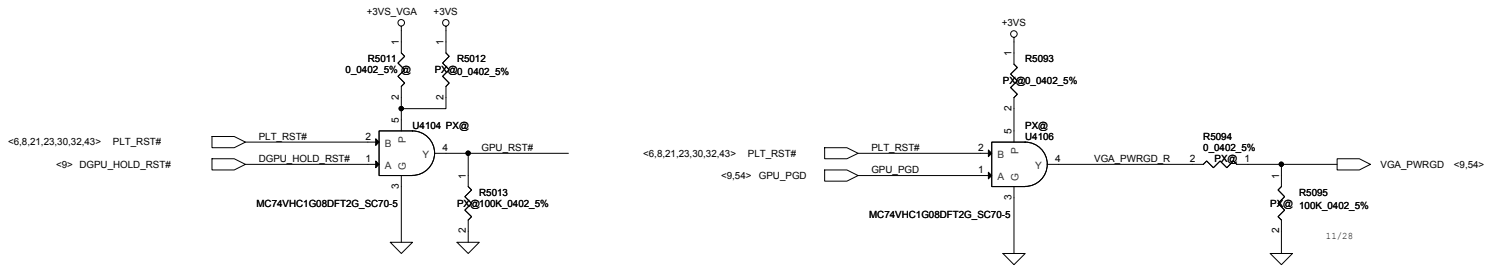
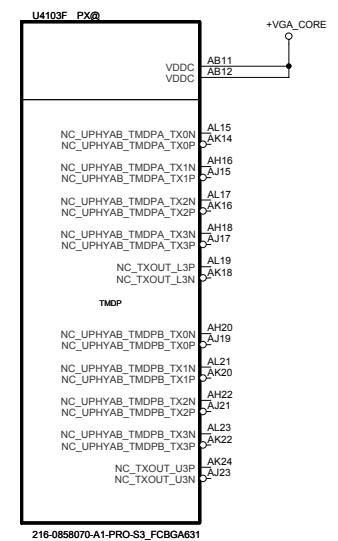


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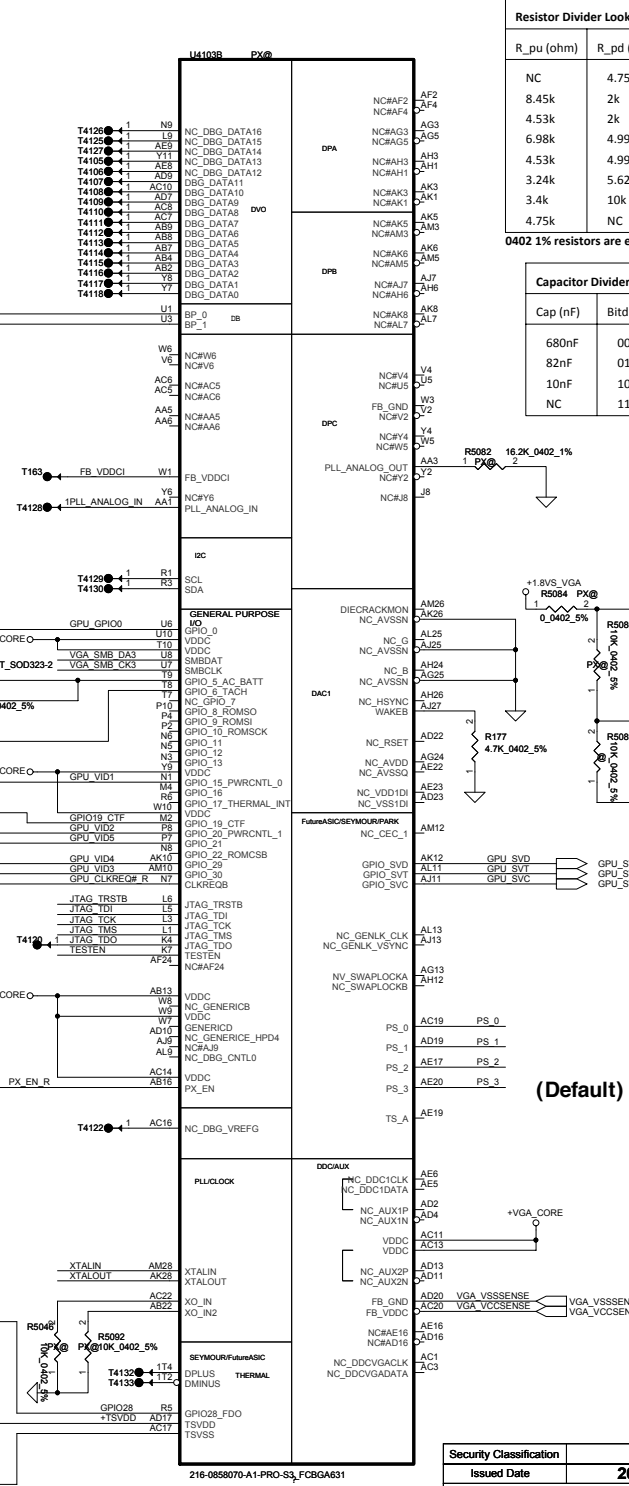
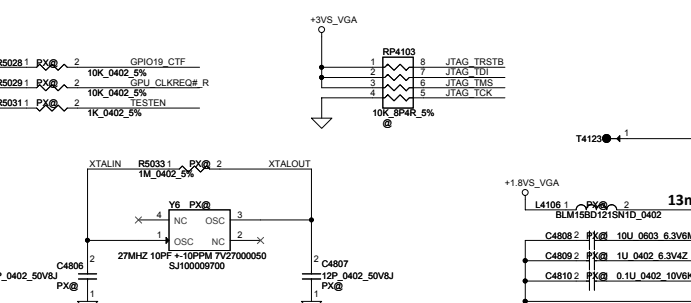
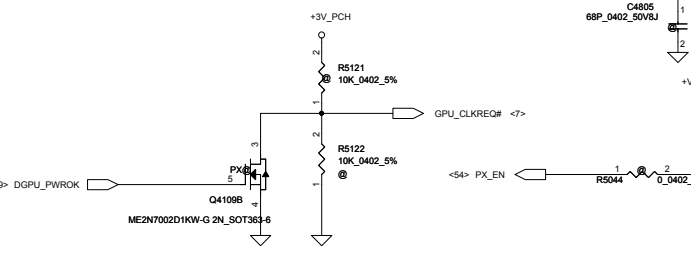
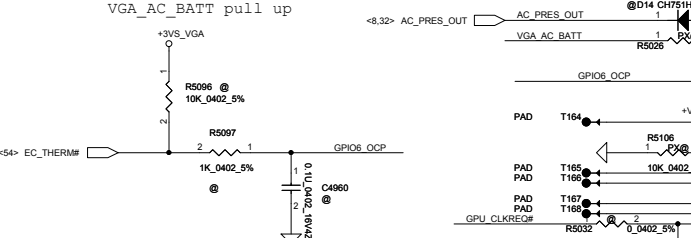
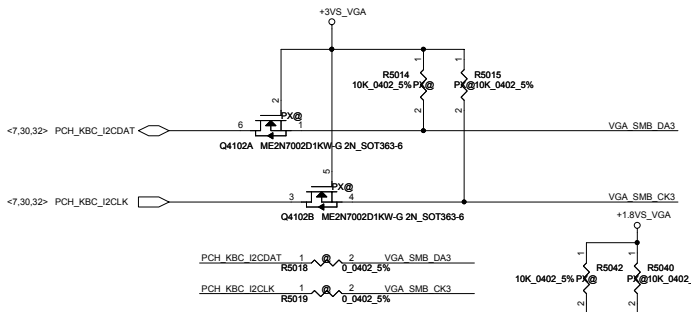


AC Coupling Capacitor
 PCIe Gen3: Recommended value is 220 nF
 PCIe Gen1 and Gen2 only: Recommended value is 100 nF

No Use GPU Display Port output

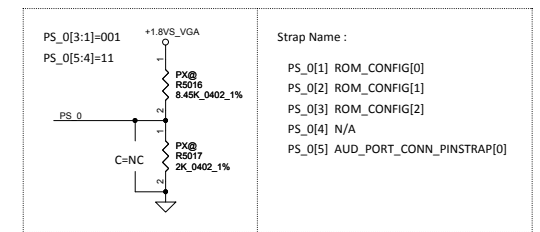


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				Topaz PCIe/DP	
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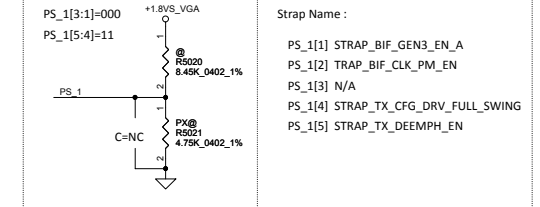


R_pu (ohm)	R_pd (ohm)	Bitd [3:1]
NC	4.75k	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

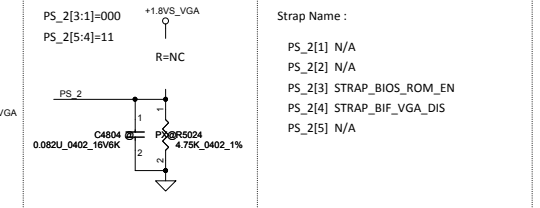
Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11



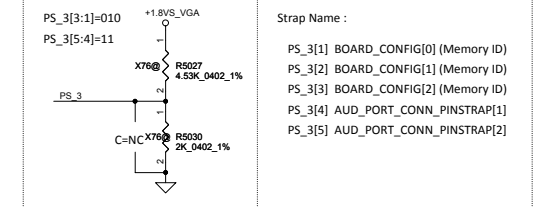
Strap Name :
PS_0[1] ROM_CONFIG[0]
PS_0[2] ROM_CONFIG[1]
PS_0[3] ROM_CONFIG[2]
PS_0[4] N/A
PS_0[5] AUD_PORT_CONN_PINSTRAP[0]



Strap Name :
PS_1[1] STRAP_BIF_GEN3_EN_A
PS_1[2] TRAP_BIF_CLK_PM_EN
PS_1[3] N/A
PS_1[4] STRAP_TX_CFG_DRV_FULL_SWING
PS_1[5] STRAP_TX_DEEMPH_EN

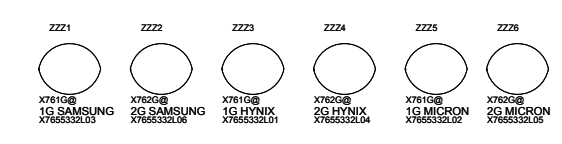


Strap Name :
PS_2[1] N/A
PS_2[2] N/A
PS_2[3] STRAP_BIOS_ROM_EN
PS_2[4] STRAP_BIF_VGA_DIS
PS_2[5] N/A



Strap Name :
PS_3[1] BOARD_CONFIG[0] (Memory ID)
PS_3[2] BOARD_CONFIG[1] (Memory ID)
PS_3[3] BOARD_CONFIG[2] (Memory ID)
PS_3[4] AUD_PORT_CONN_PINSTRAP[1]
PS_3[5] AUD_PORT_CONN_PINSTRAP[2]

Memory ID	Memory Type	Configuration	Size	R5027	R5030	X76 P/N
000	SA000068U80	Samsung K4W2G1646Q-BC1A	1GB	NC	4.75k	X7655332L03
001	SA000076P00	Samsung K4W4G1646D-BC1A	2GB	8.45k	2k	X7655332L06
010	SA00006H440	Hynix H5TC2G63FFR-11C	1GB	4.53k	2k	X7655332L01
011	SA00006E800	Hynix H5TC4G63AFR-11C	2GB	6.98k	4.99k	X7655332L04
100	SA000067540	Micron MT41J128M16JT-093G:K	1GB	4.53k	4.99k	X7655332L02
101	SA000077K00	Micron MT41J256M16HA-093G:E	2GB	3.24k	5.62k	X7655332L05
110		Nanya 128x16 NT5CB128M16FP	1GB	3.4k	10k	
111		Nanya 256x16 NT5CB256M16CP	2GB	4.75k	NC	



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Compal Electronics, Inc. **Topaz_MSIC**

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+VGA_CORE	10uF	1uF	0.1uF
VDDC	TBD	5 (1@)	10 (2@)
VDDCI	3.5A	1	3

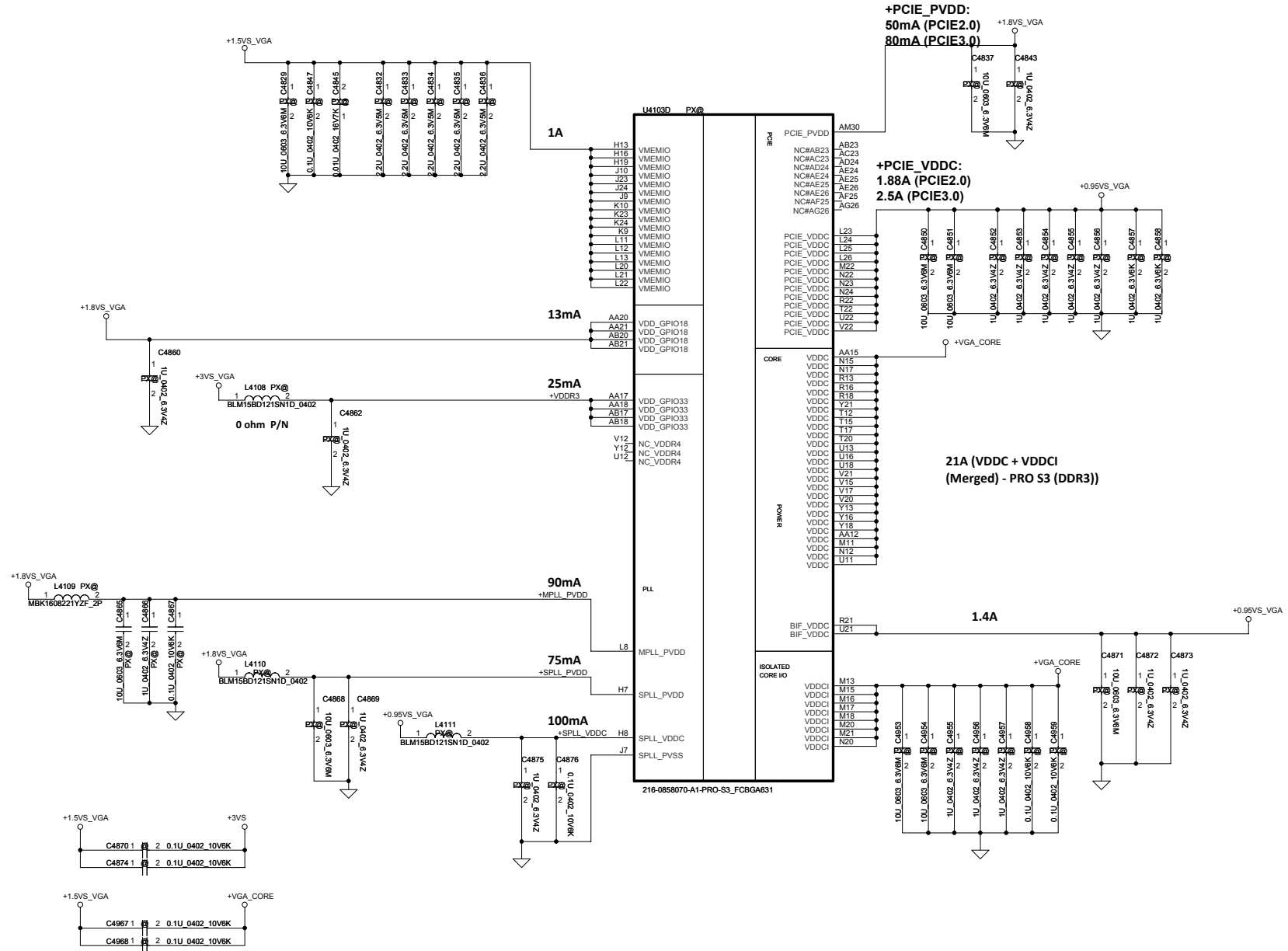
+0.95VS_VGA	10uF	1uF	0.1uF
PCIE_VDDC	2.5A	2 (1@)	5 (1@)
BIF_VDDC	1.4A	0	0
SPLL_VDDC	100mA	1	1

+1.5VS_VGA	10uF	1uF	0.1uF
VDDR1	1.5A	3	5

+1.8VS_VGA	10uF	1uF	0.1uF
PCIE_PVDD	100mA	1	1
MPLL_PVDD	130mA	1	1
SPLL_PVDD	75mA	1	1
VDDR4	(300mA)	0	0

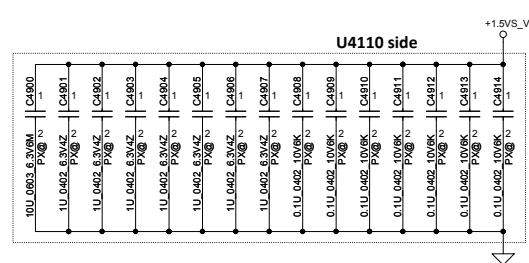
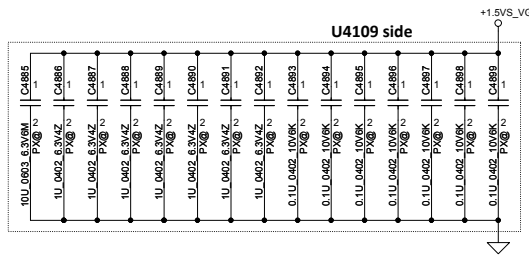
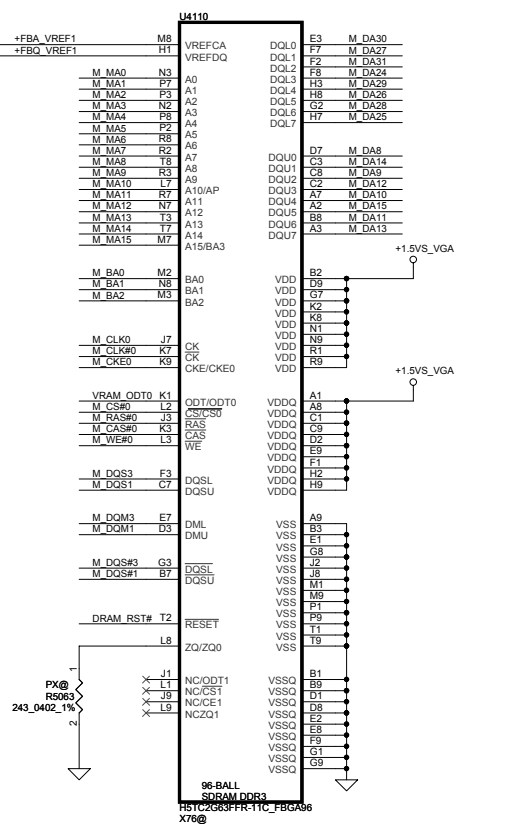
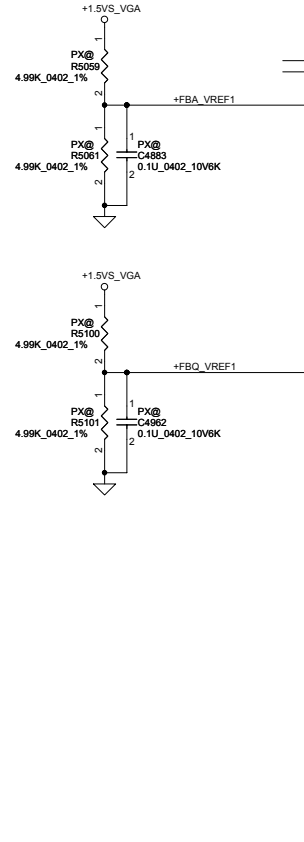
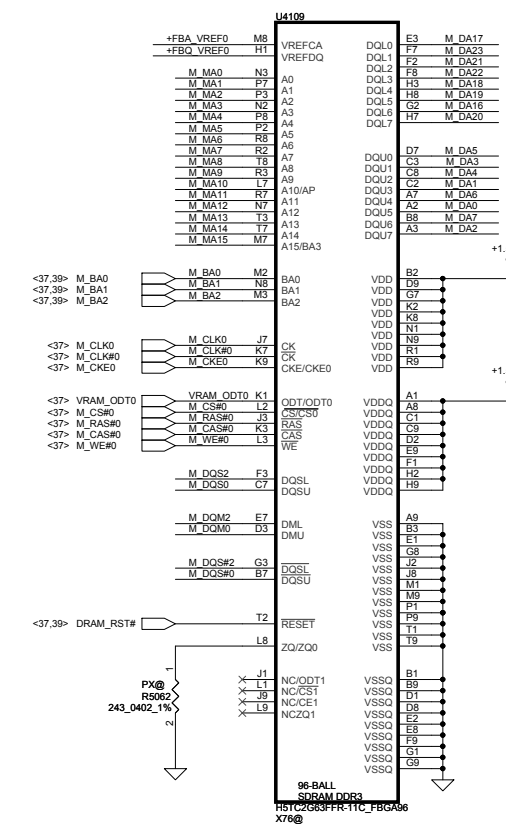
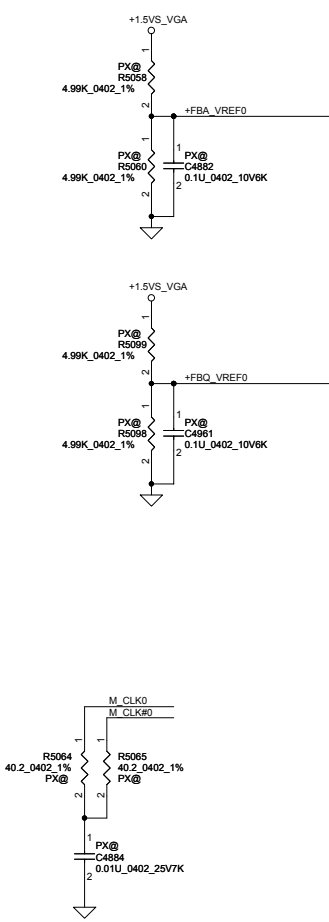
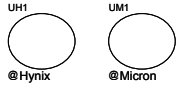
VDD_CT	13mA	1	1
+TSVDD	13mA	1	1
+DP_VDDR	0	0	0
+DP_VDDC	0	0	0

+3VS_VGA	10uF	1uF	0.1uF
VDDR3	25mA	0	2 (1@)



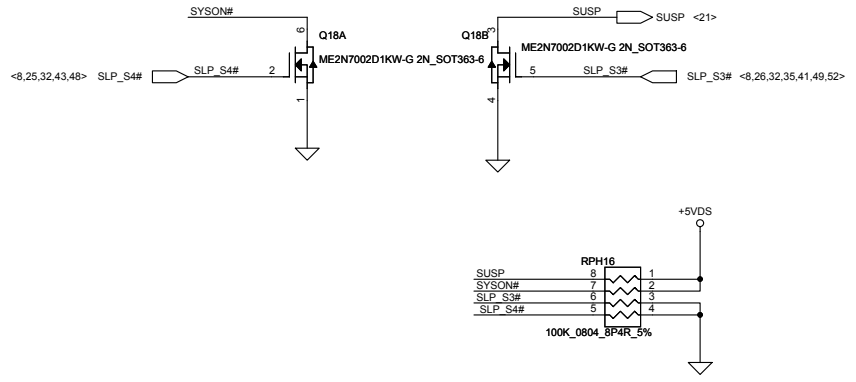
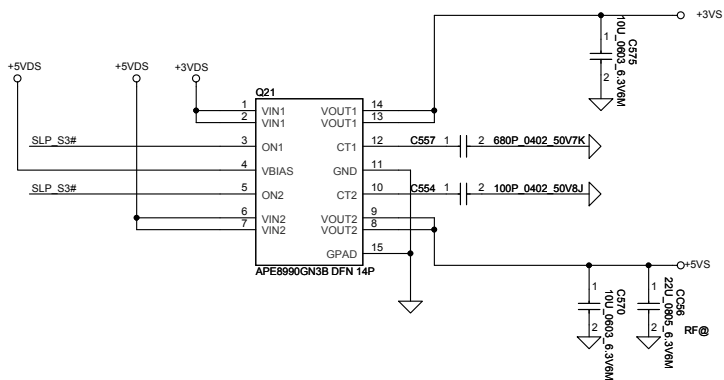
Memory Partition A - Lower 32 bits

- <37,39> M_DA[63..0]  M_DA[63..0]
- <37,39> M_MA[15..0]  M_MA[15..0]
- <37,39> M_DOM[7..0]  M_DOM[7..0]
- <37,39> M_DQS[7..0]  M_DQS[7..0]
- <37,39> M_DQS# [7..0]  M_DQS# [7..0]

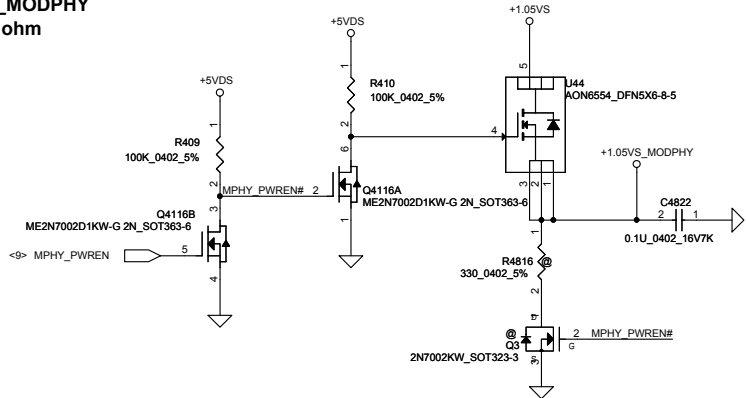


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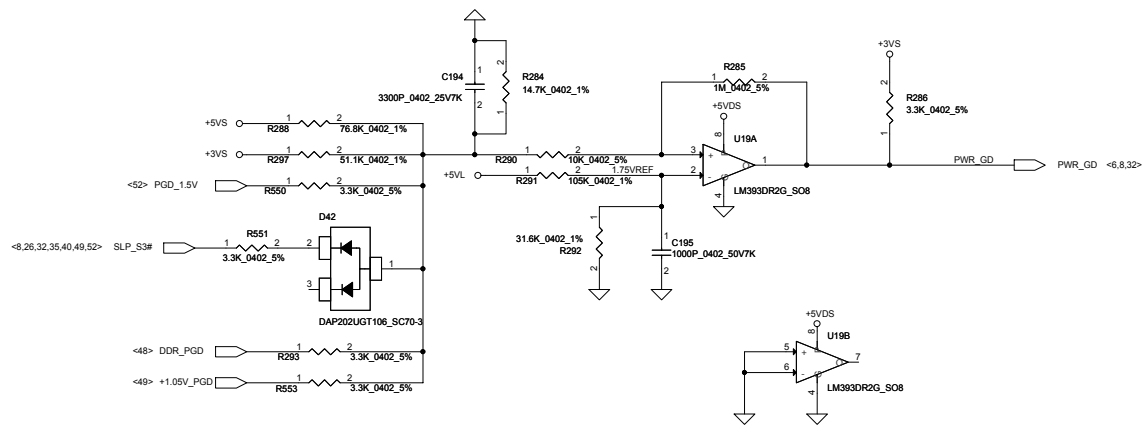
Topaz VRAM A Lower
LA-B181P



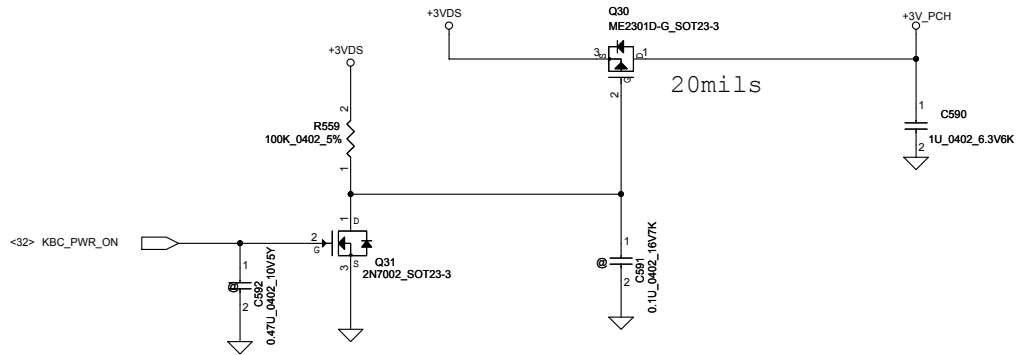
CPU +V1.05DX_MODPHY
 Max Rdson <6m ohm
 1840mA



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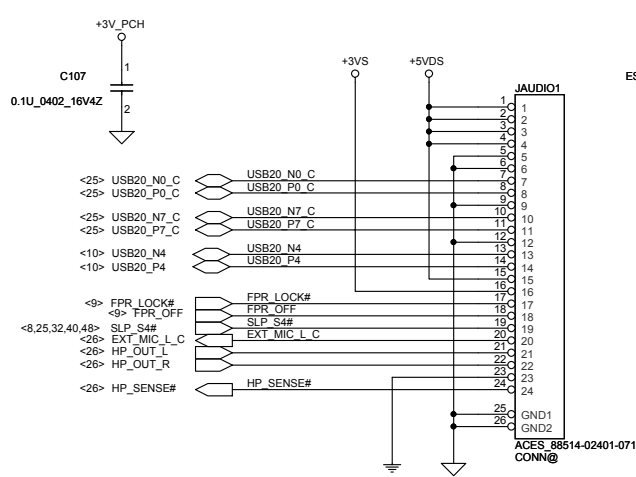


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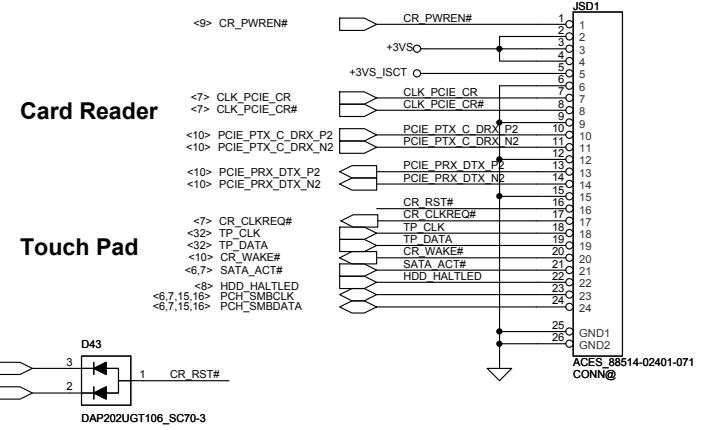


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Audio Board



Card Reader Board



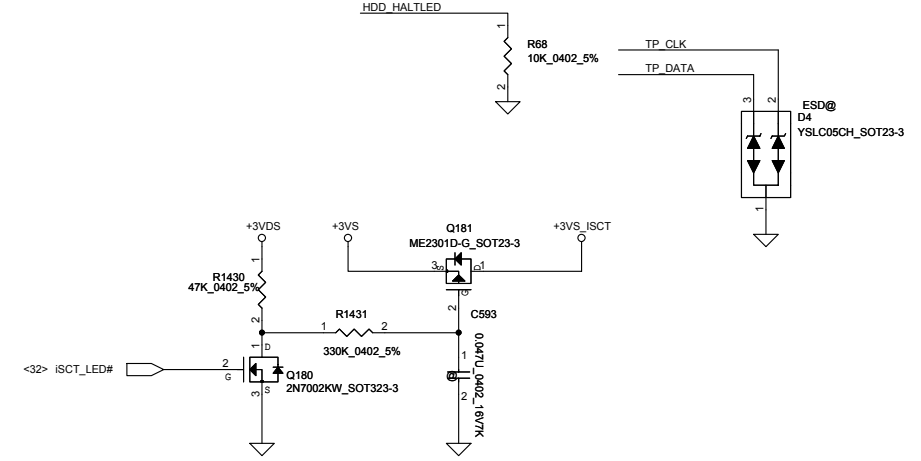
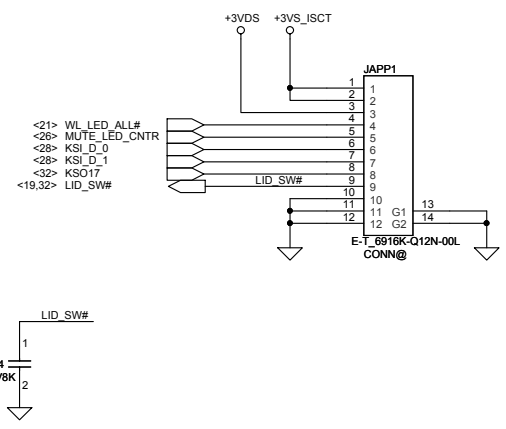
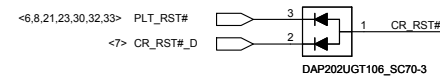
USB CONN

Finger printer

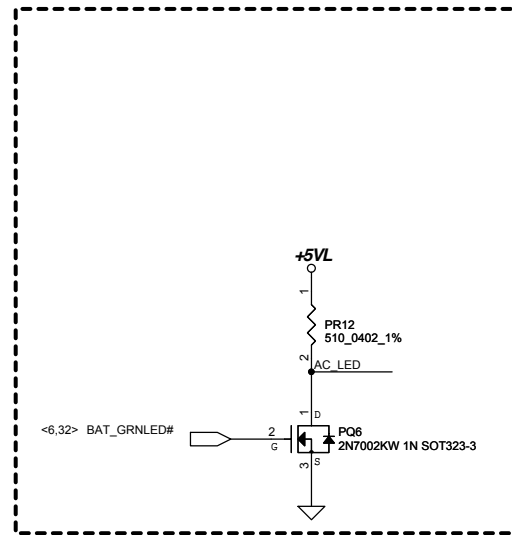
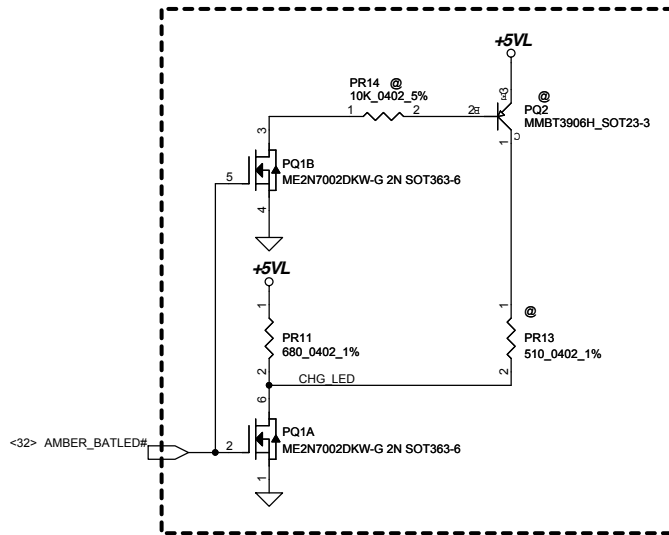
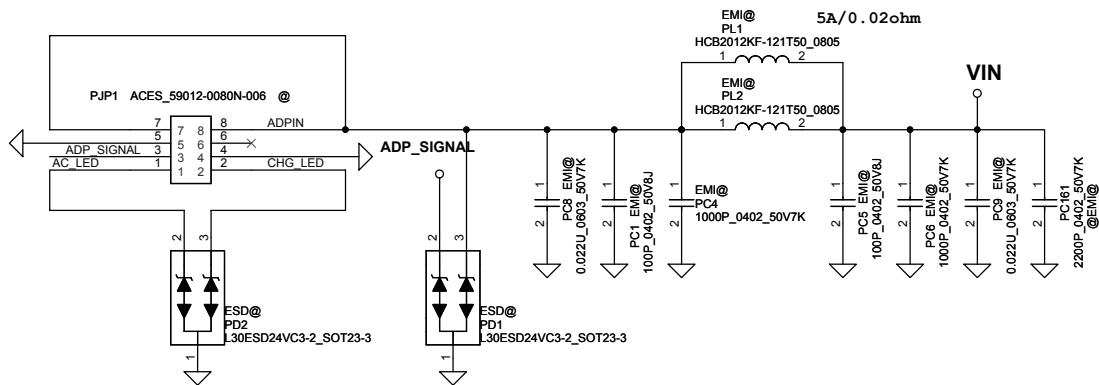
Combo Jack

Card Reader

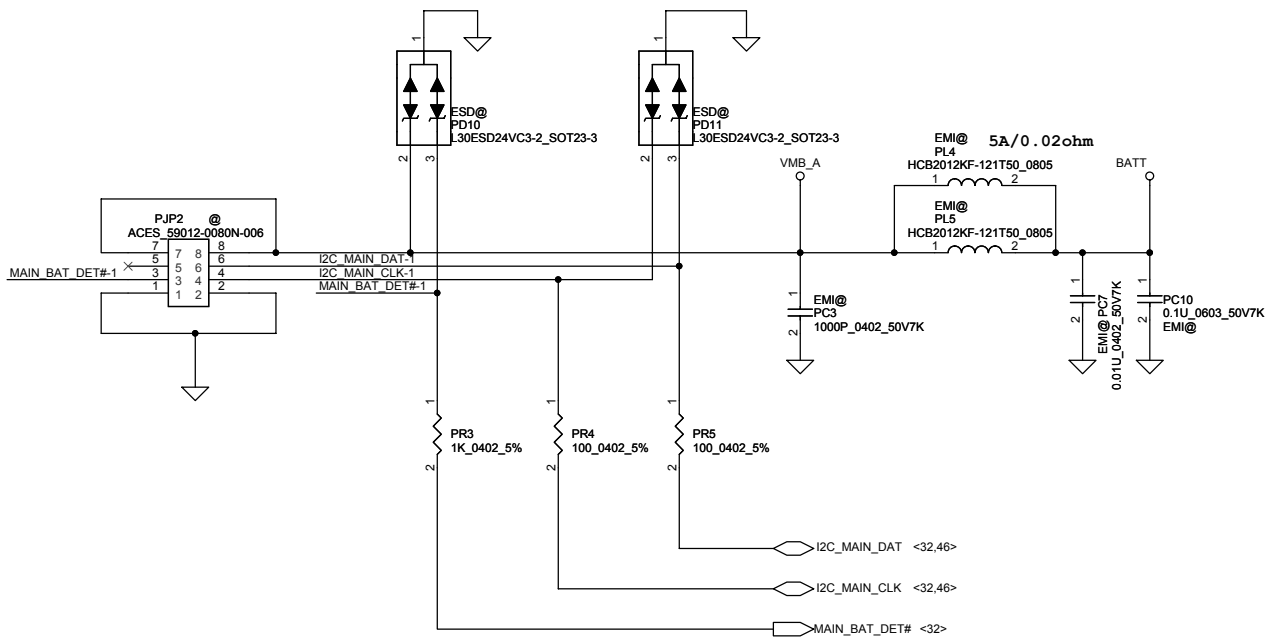
Touch Pad



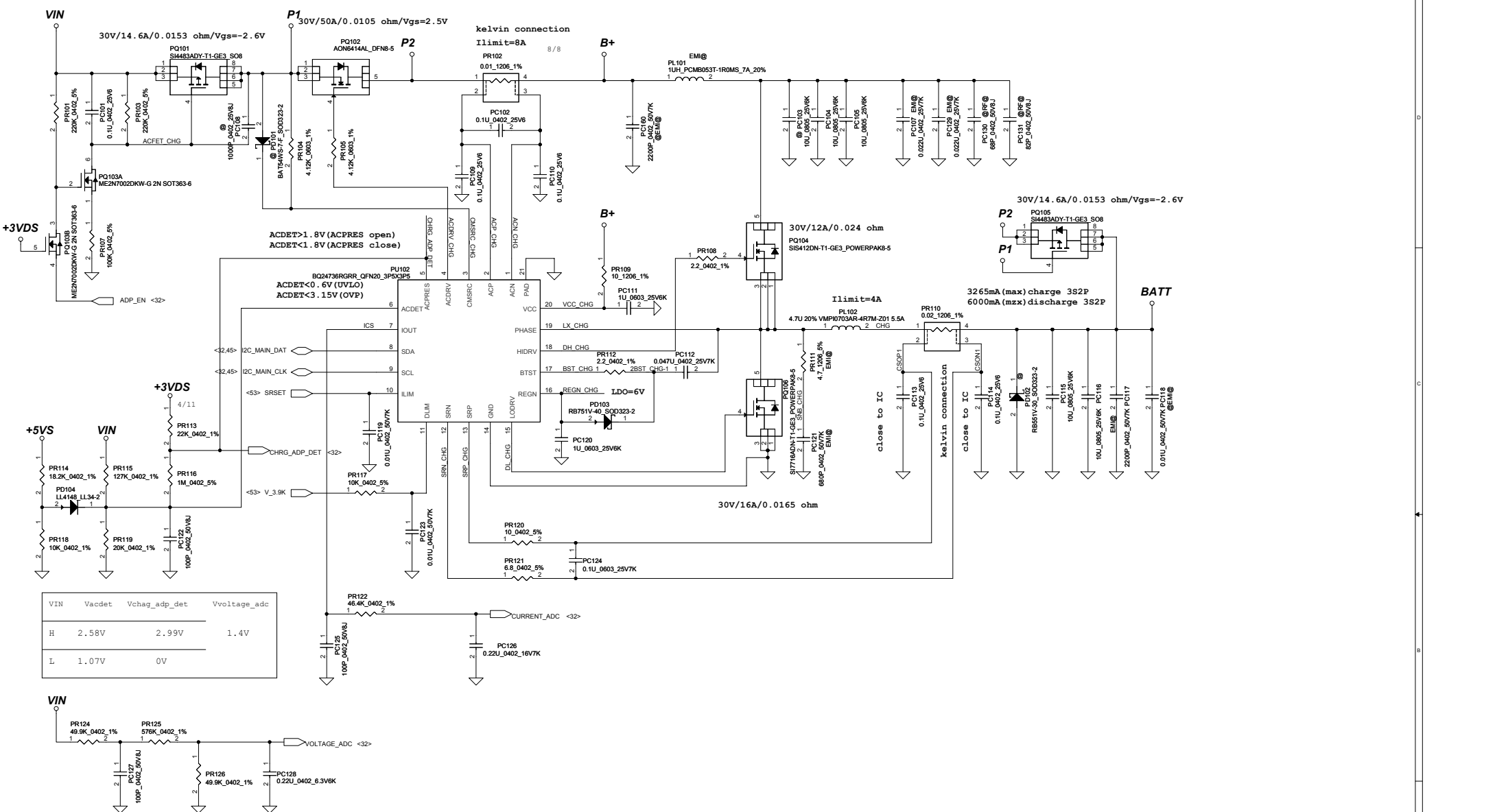
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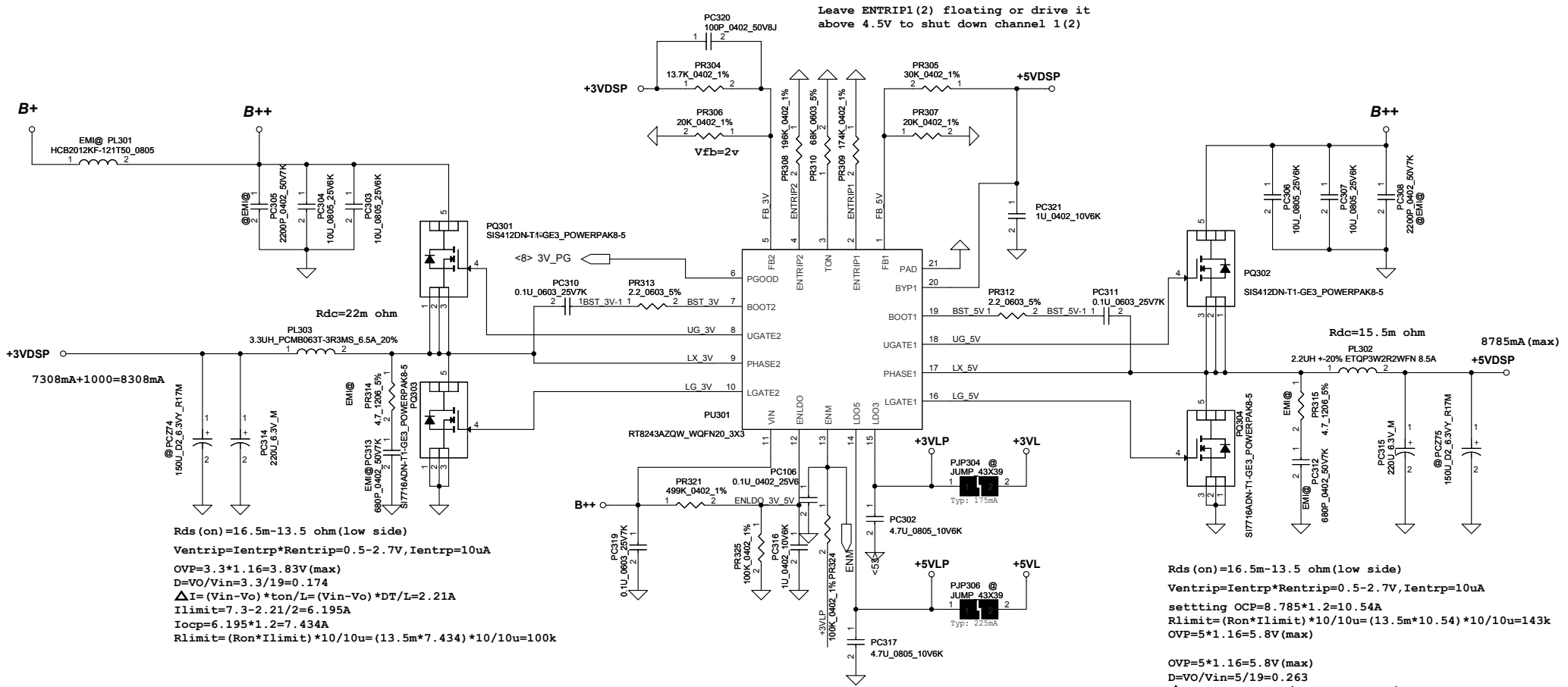
VIN	Vacdet	Vchag_adp_det	Vvoltage_adc
H	2.58V	2.99V	1.4V
L	1.07V	0V	

$I_{limit} = 20 * (V_{srp} - V_{srn}) = 20 * I_{ch} * R_{ch}$
 up to $I_{limit} = 1.6V$ (disable)
 $R = 1.0m \text{ ohm}$ $I = 8A$
 $R = 2.0m \text{ ohm}$ $I = 4A$
 $f_s = 750k$
 $I_{ripple} = V_{in} * D * (1 - D) / (f_s * L)$,
 $D = 0.5$ (worst)
 $I_{ripple} = 1.418A$
 $I_{sat}(L) = I_{ch} * 0.5 * I_{ripple} = 4 + 0.5 * 1.418 = 4.709A$

ILIM > 1.6V disable
ILIM < 75mV disable
ILIM > 105mV enable

DLIM > 1.1V disable
DLIM < 870mV disable
DLIM > 996mV enable (buck to boost)
 default discharger current limit 4.096A

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				CHARGER
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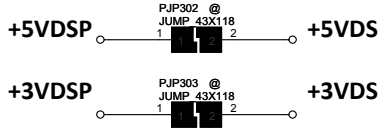


Leave ENTRIP1(2) floating or drive it above 4.5V to shut down channel 1(2)

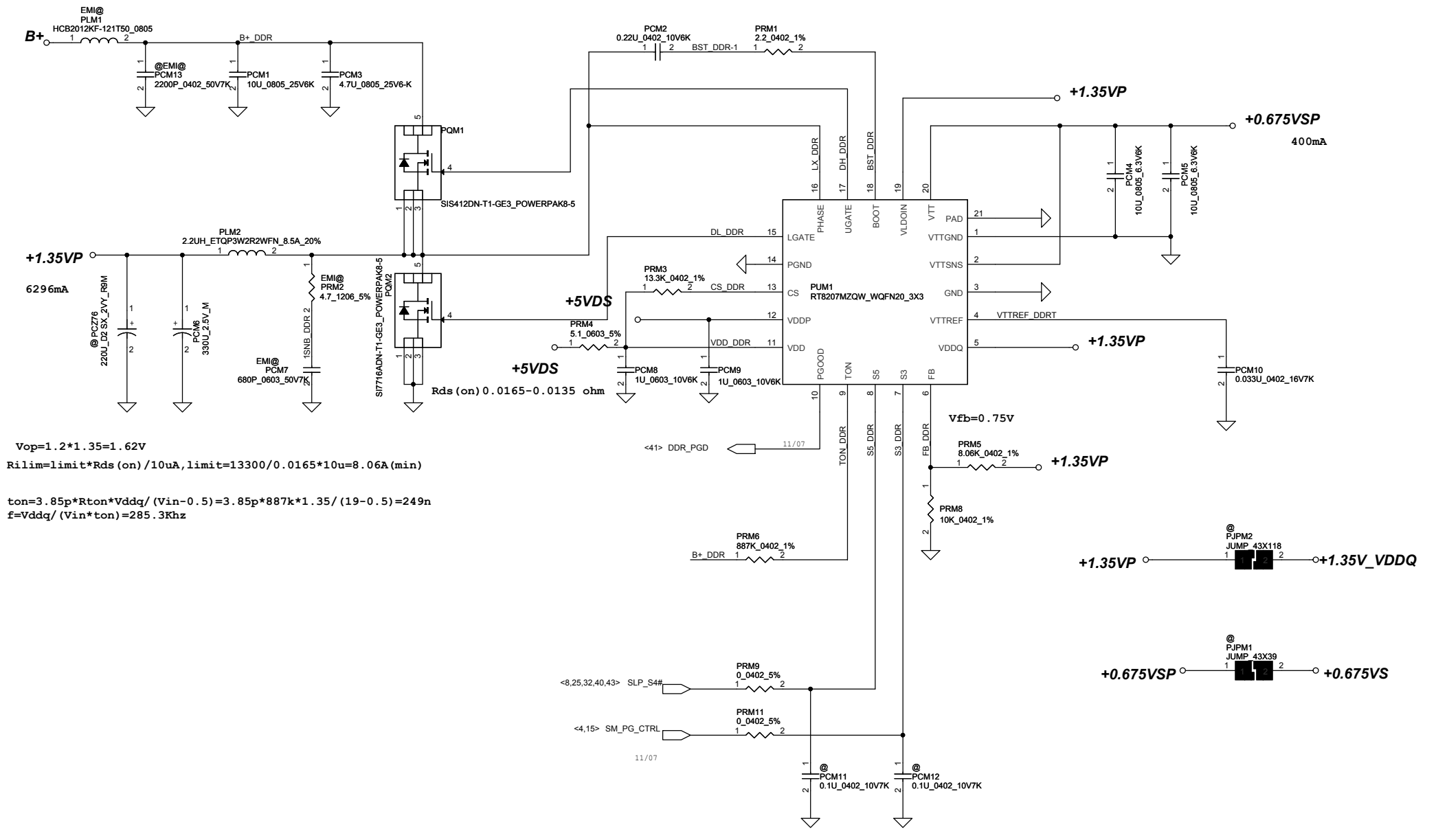
Rdc=22m ohm
 Ventrip=Ientrp*Rentrip=0.5-2.7V, Ientrp=10uA
 OVP=3.3*1.16=3.83V (max)
 D=VO/Vin=3.3/19=0.174
 $\Delta I = (V_{in}-V_o) * t_{on} / L = (V_{in}-V_o) * DT / L = 2.21A$
 Ilimit=7.3-2.21/2=6.195A
 Iocp=6.195*1.2=7.434A
 Rlimit=(Ron*Ilimit)*10/10u=(13.5m*7.434)*10/10u=100k

Rdc=15.5m ohm
 Ventrip=Ientrp*Rentrip=0.5-2.7V, Ientrp=10uA
 setting OCP=8.785*1.2=10.54A
 Rlimit=(Ron*Ilimit)*10/10u=(13.5m*10.54)*10/10u=143k
 OVP=5*1.16=5.8V (max)
 D=VO/Vin=5/19=0.263
 $\Delta I = (V_{in}-V_o) * t_{on} / L = (V_{in}-V_o) * DT / L = 5.21A$
 Ilimit=8.785-5.21/2=6.18A
 Iocp=6.195*1.2=7.416A
 Rlimit=(Ron*Ilimit)*10/10u=(13.5m*7.416)*10/10u=100k

<1>5V=283KHz 3V=330KHz (Vin=6.5 ~ 12v)
 <2>5V=321KHz 3V=375KHz (Vin=12 ~ 25v)
 (By Rton= 68K ohm)

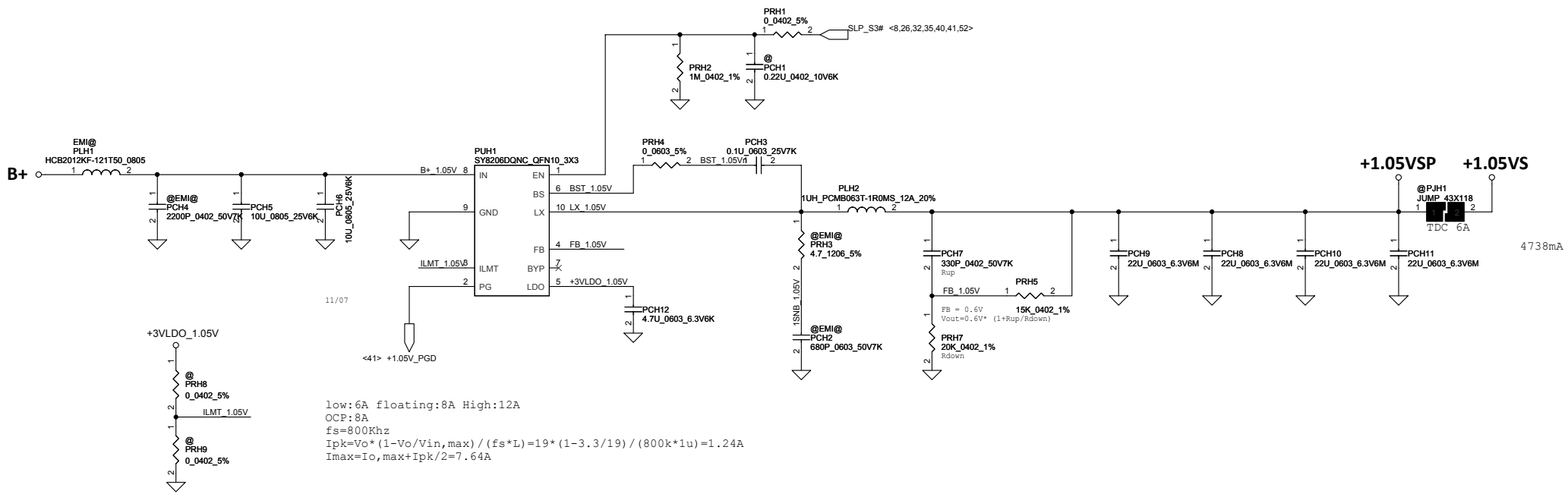


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$V_{op} = 1.2 * 1.35 = 1.62V$
 $R_{lim} = \text{limit} * R_{ds(on)} / 10uA, \text{limit} = 13300 / 0.0165 * 10u = 8.06A(\text{min})$
 $t_{on} = 3.85p * R_{ton} * V_{ddq} / (V_{in} - 0.5) = 3.85p * 887k * 1.35 / (19 - 0.5) = 249n$
 $f = V_{ddq} / (V_{in} * t_{on}) = 285.3Khz$

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PRZ5:Vo-usr=1.7*(150/(150+9.53))=1.598V
 Vusr=540mV
 PRZ11:disable OSR&PT,Rosr=150K
 PRZ10:setting fs R=150=>1Mhz
 Ramp setting:
 PRZ9=100K type:160mV
 PRZ9>=150K type:40mV
 boot voltage setting:
 Vb-ram=1V=>2V
 Vb-ram=0V=>1.7V
 Vb-ram>1.525V=>0V

Iccmax=32A (15w) ,Iccmax=40A (28w)
 IccTDC=10A (15w) ,IccTDC=16A (28w)
 IccDyn=27A (15w) ,IccDyn=32A (28w)

OCP voatge seeting:
 PRZ8=39K ==>18.9mV
 Vimom=1.7V

Rp_n=10.74k Rcs(eff)=0.6m ohm
 1.7V=10*(1+Rimom/39k)*0.6m*32,Rimom=345k

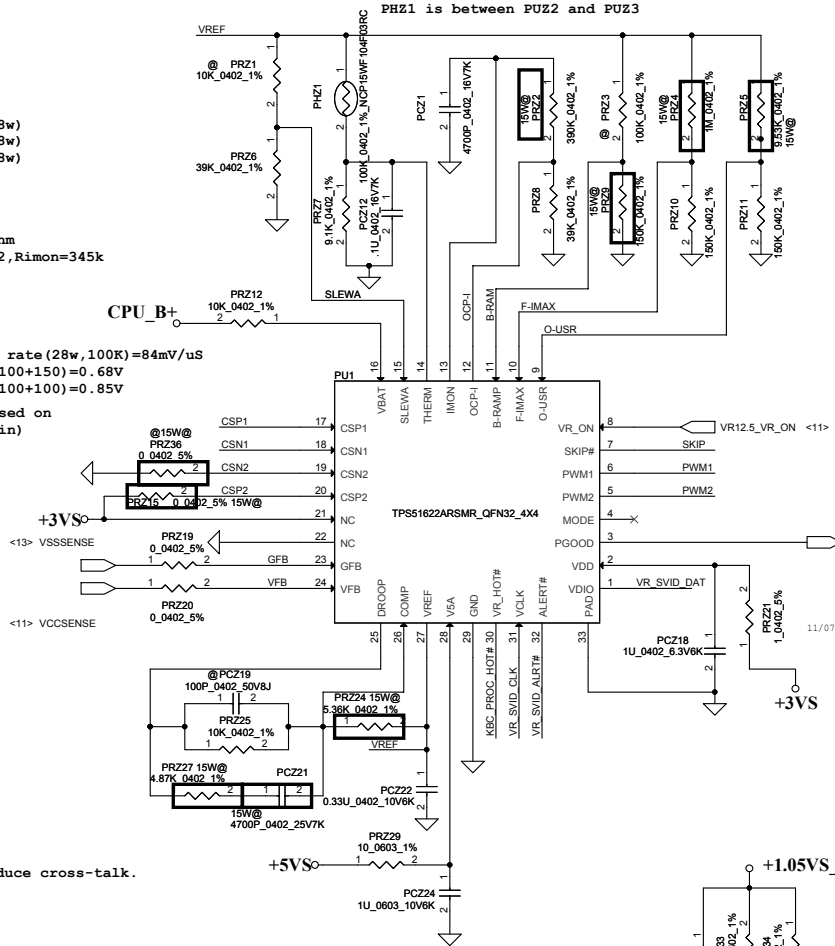
ALERT goes low,THERM=1.08V
 VR_HOT goes low,THERM=1.1V

slew rate(15w,150K)=96mV/uS,slew rate(28w,100K)=84mV/uS
 address selection(15w):1.7*100/(100+150)=0.68V
 address selection(28w):1.7*100/(100+100)=0.85V

On-tome(ton):ON-time is fixed based on
 the input voltage (at the VBAT pin)

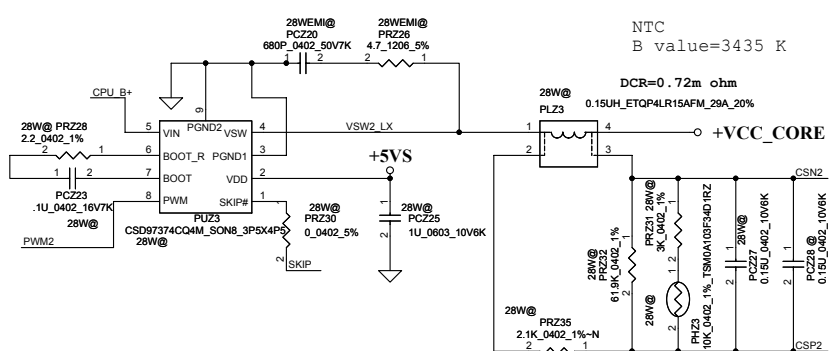
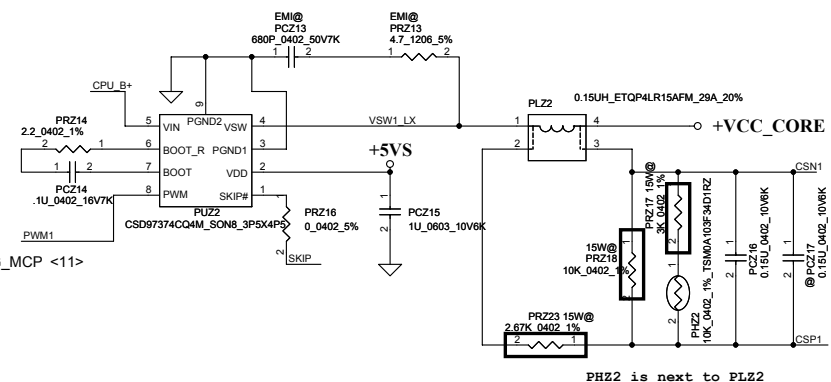
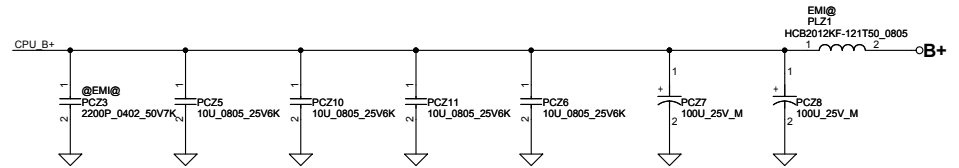
Vssense and Vccsense need to be
 difference pair

Drop:Error amplifier output.

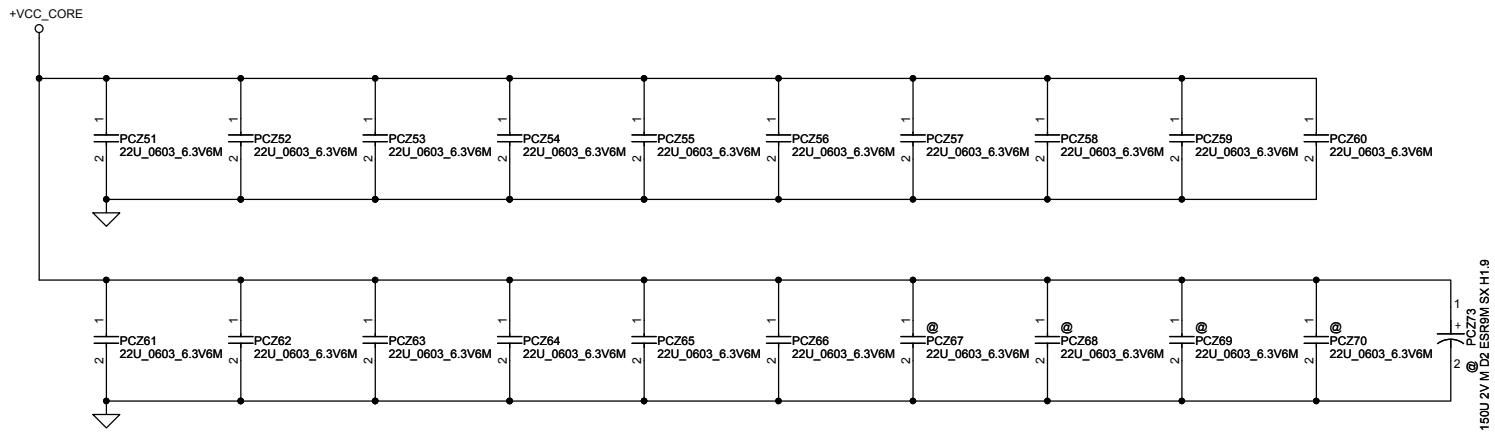


- 28W@ PRZ27 10K_0402_1%
- 28W@ PCZ21 1500P_0402_50V7K
- 28W@ PRZ24 4.12K_0402_1%
- 28W@ PRZ2 187K_0402_1%
- 28W@ PRZ4 806K_0402_1%
- 28W@ PRZ5 280K_0402_1%
- 28W@ PRZ9 100K_0402_1%
- 28W@ PRZ17 3K_0402_1%
- 28W@ PRZ23 2.1K_0402_1%
- 28W@ PRZ18 61.9K_0402_1%

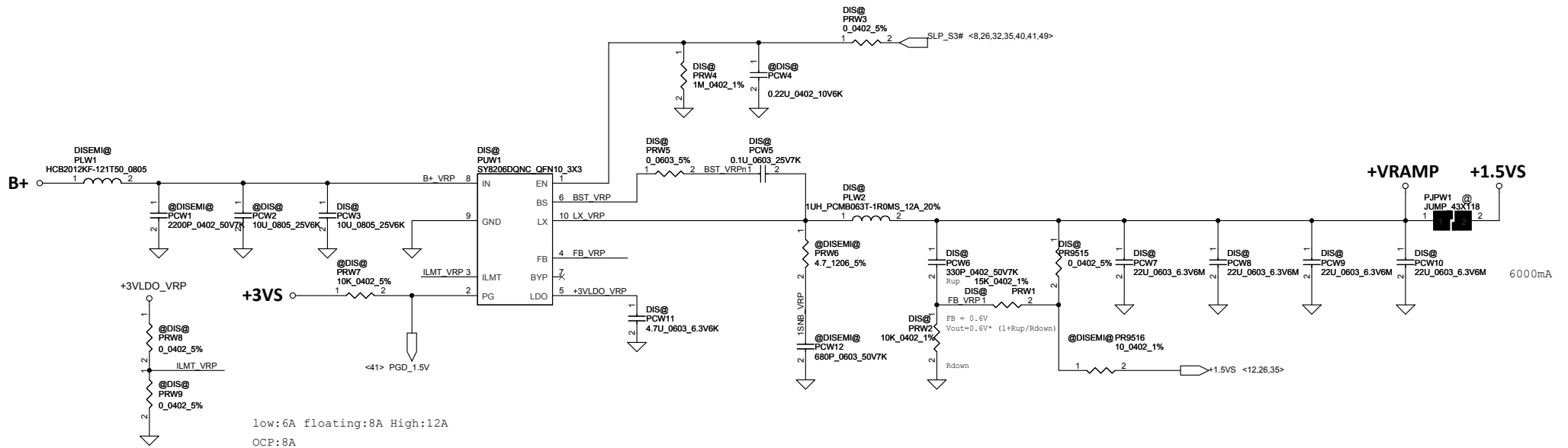
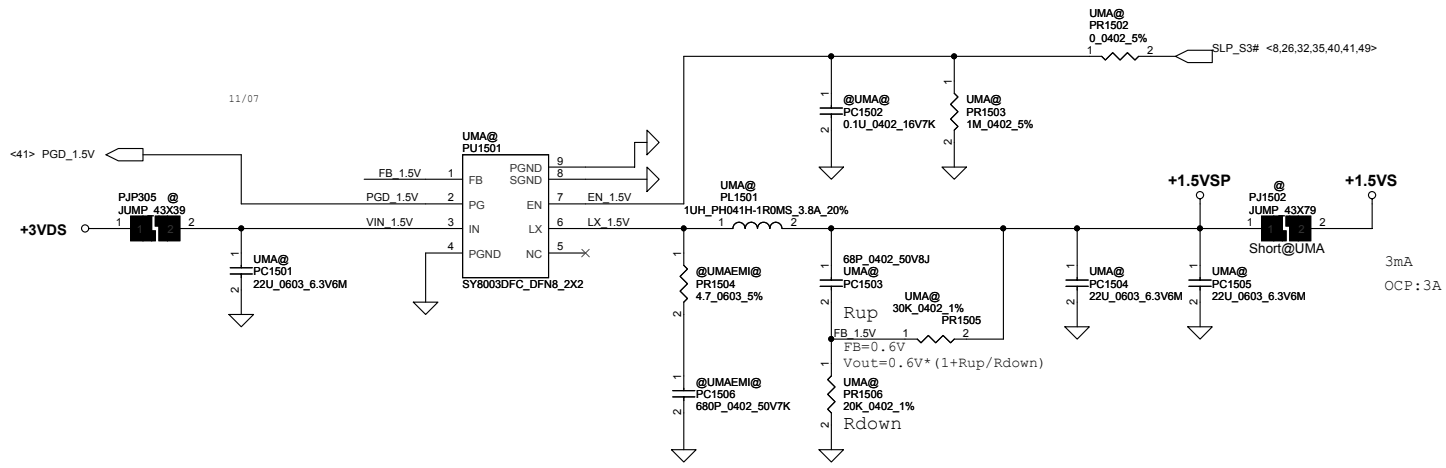
not mount 需特别注意 (15w@,28w@)



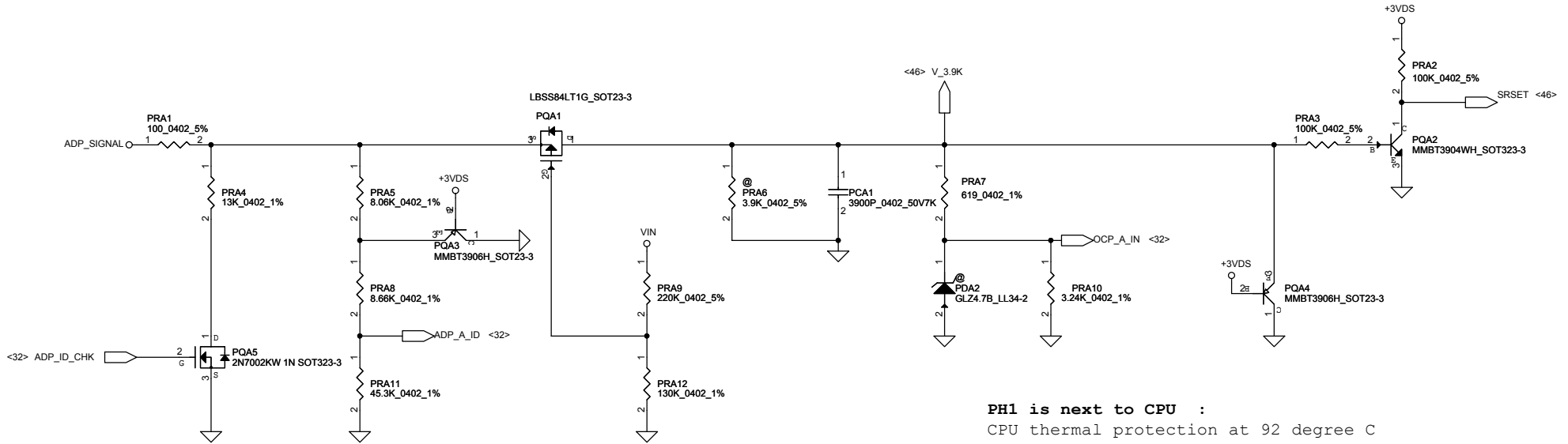
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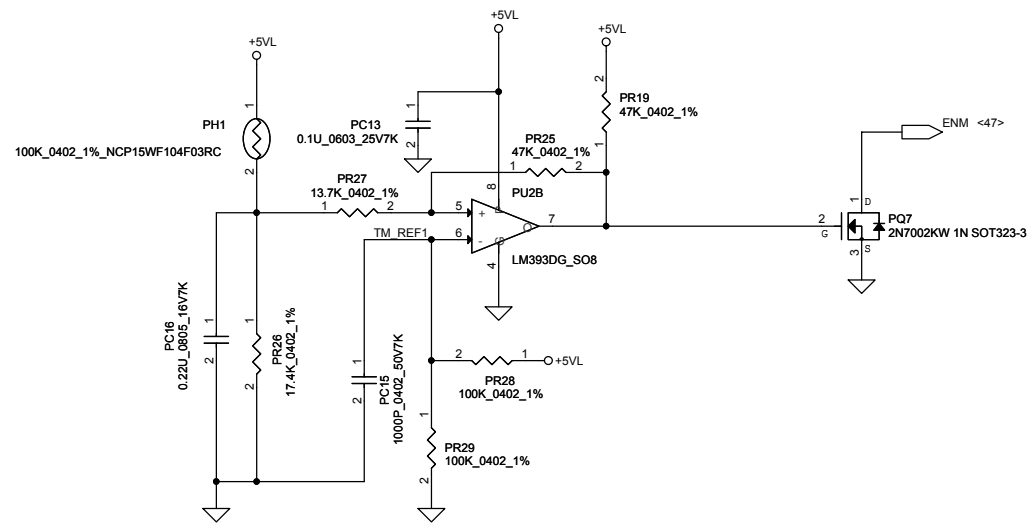
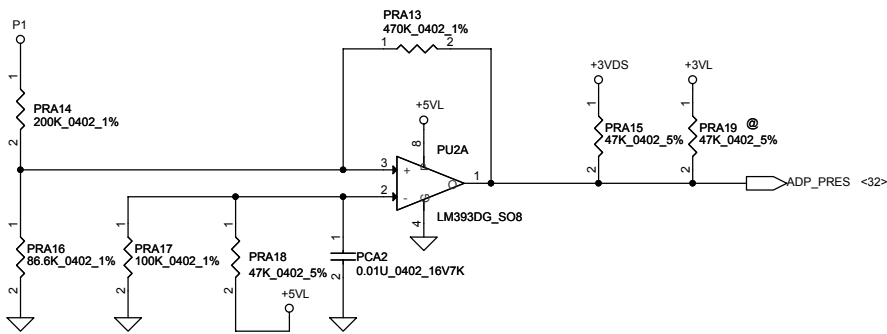


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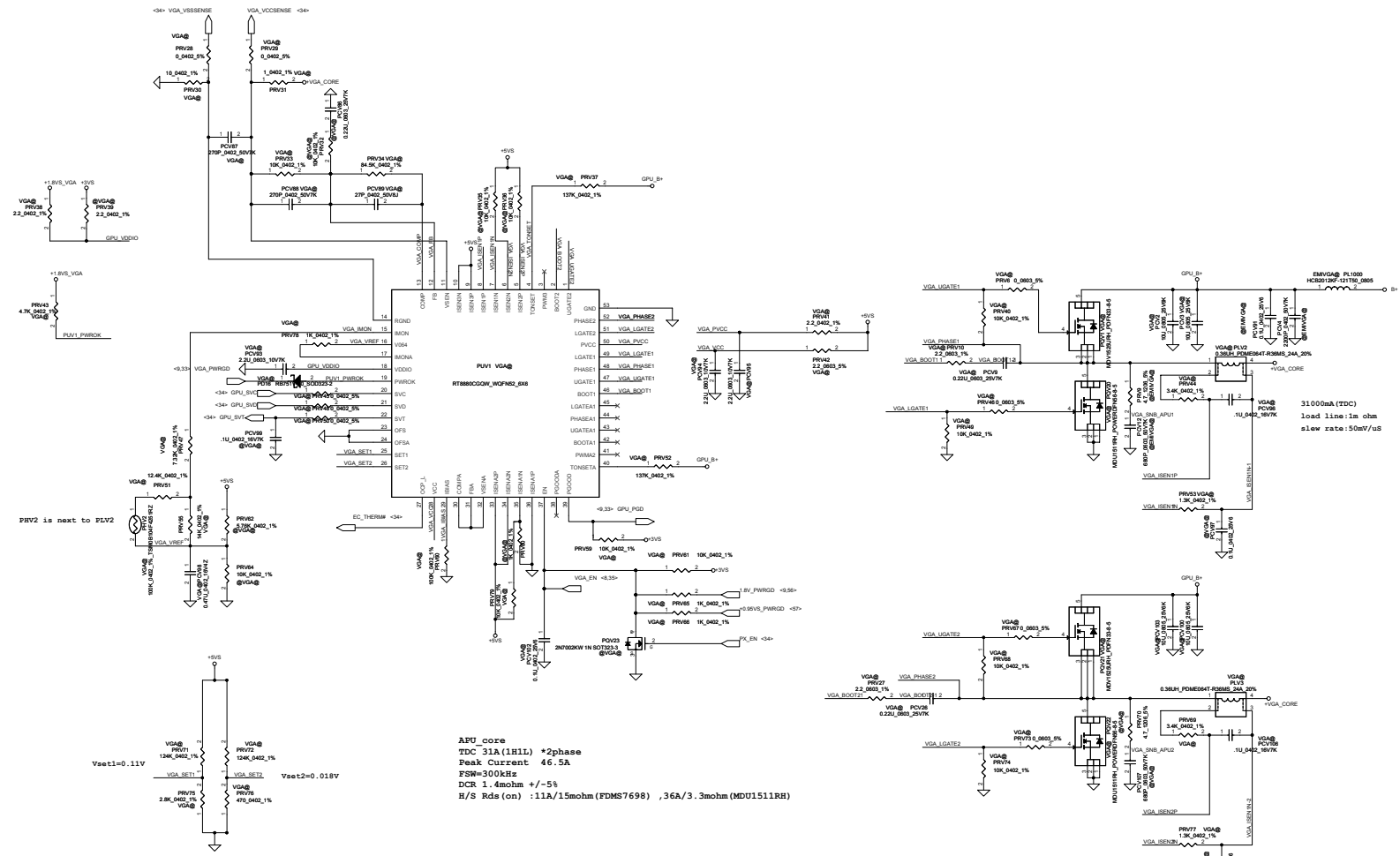


MEMO:PRA4 and PQA5 are not mount

PH1 is next to CPU :
CPU thermal protection at 92 degree C
Recovery at 56 degree C

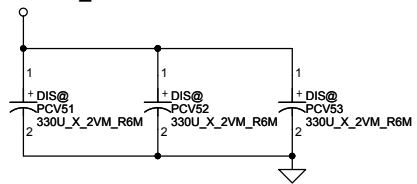


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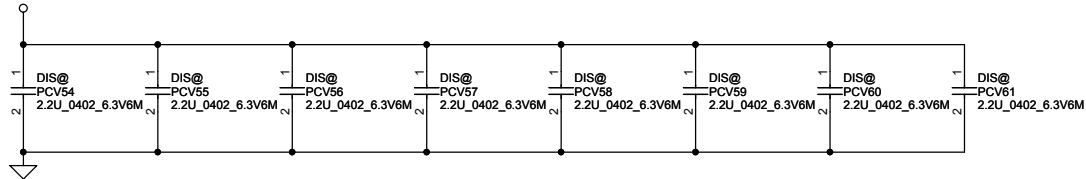


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<small>RT8888AGOW</small>			<small>LA-S181P</small>
<small>ISSUED: 2013.03.19</small>			<small>1/1</small>

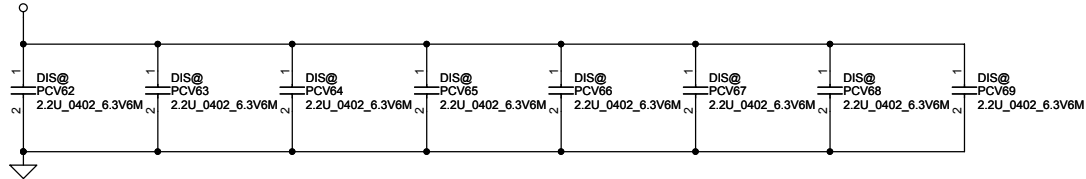
+VGA_CORE



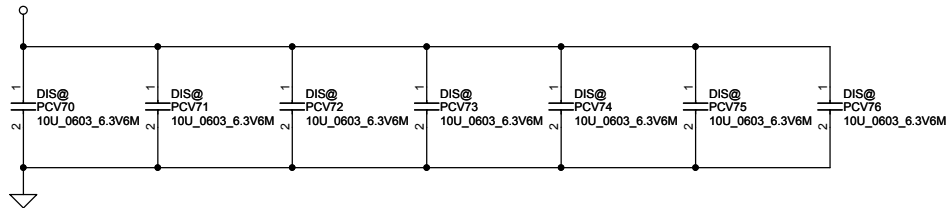
+VGA_CORE



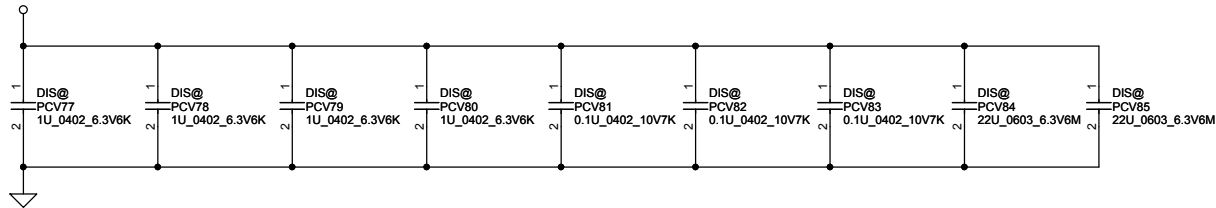
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+VGA_CORE

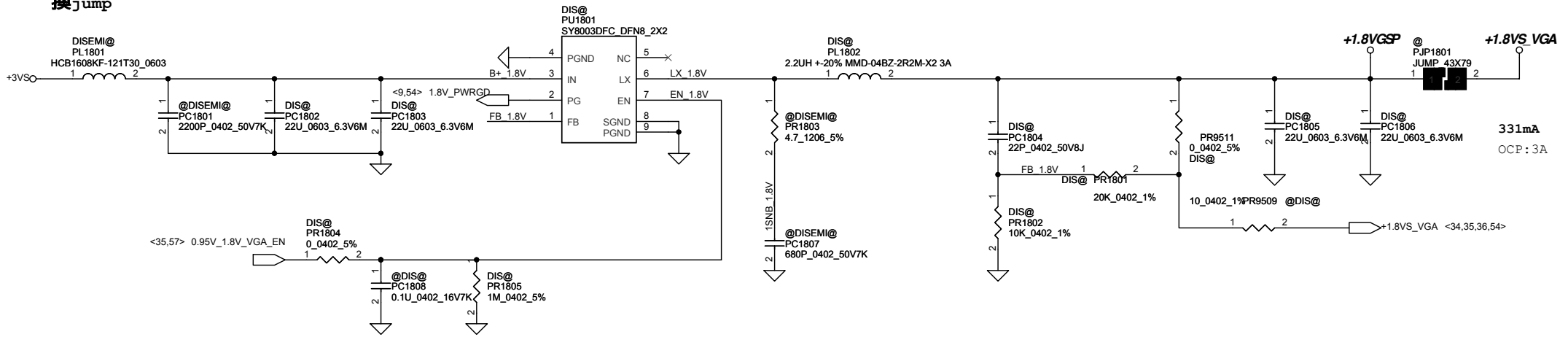


+VGA_CORE



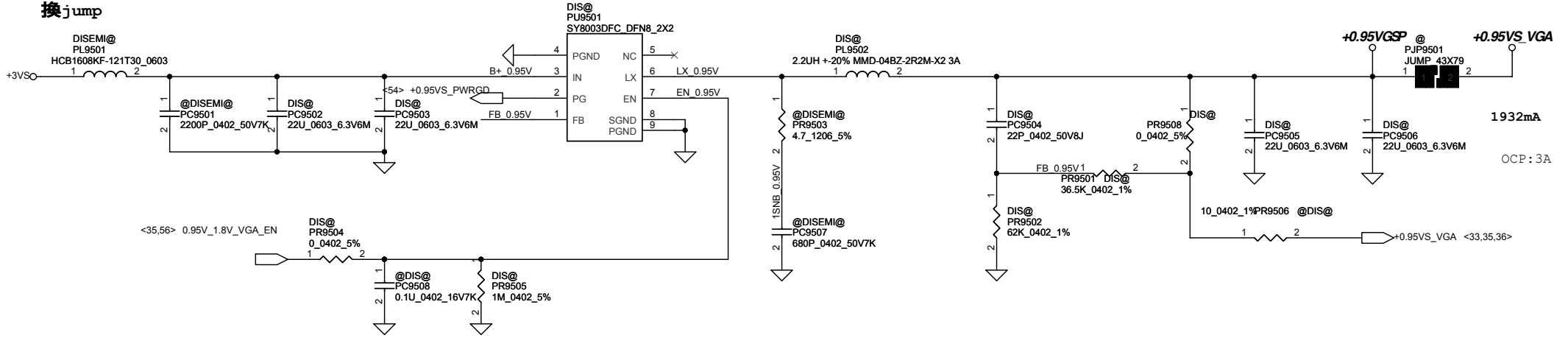
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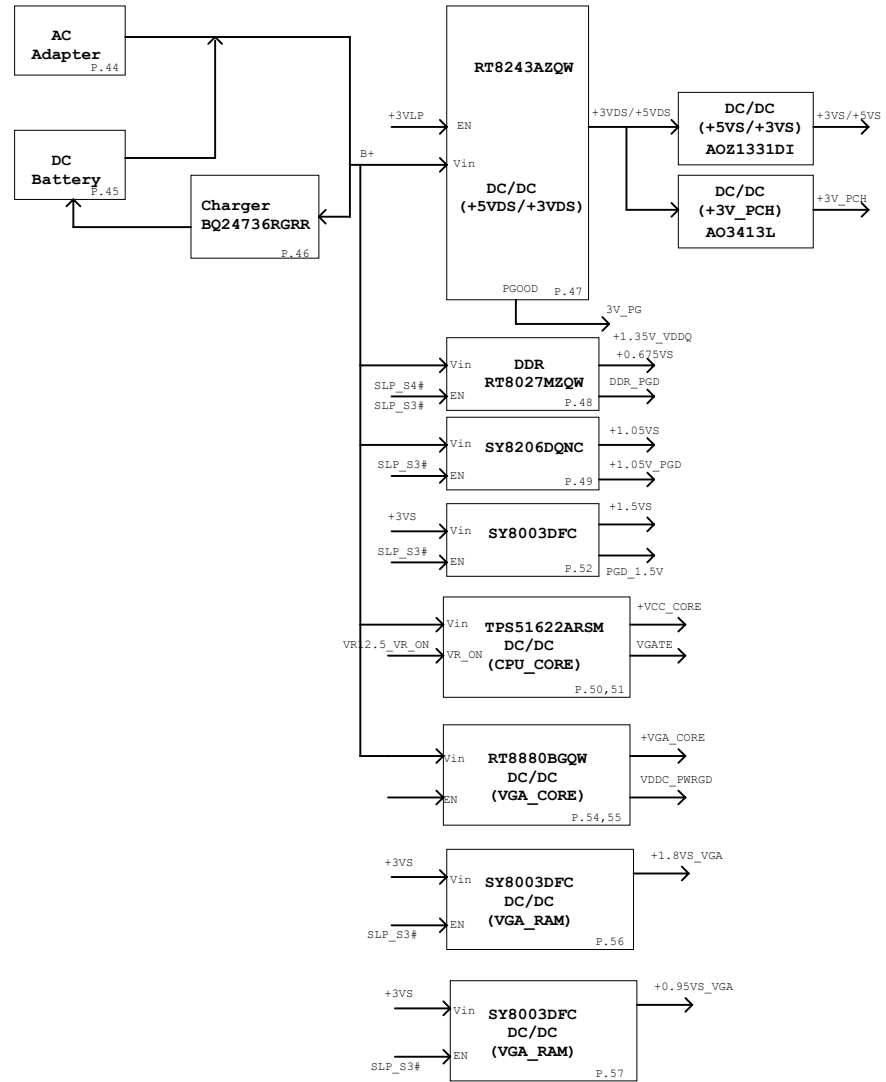


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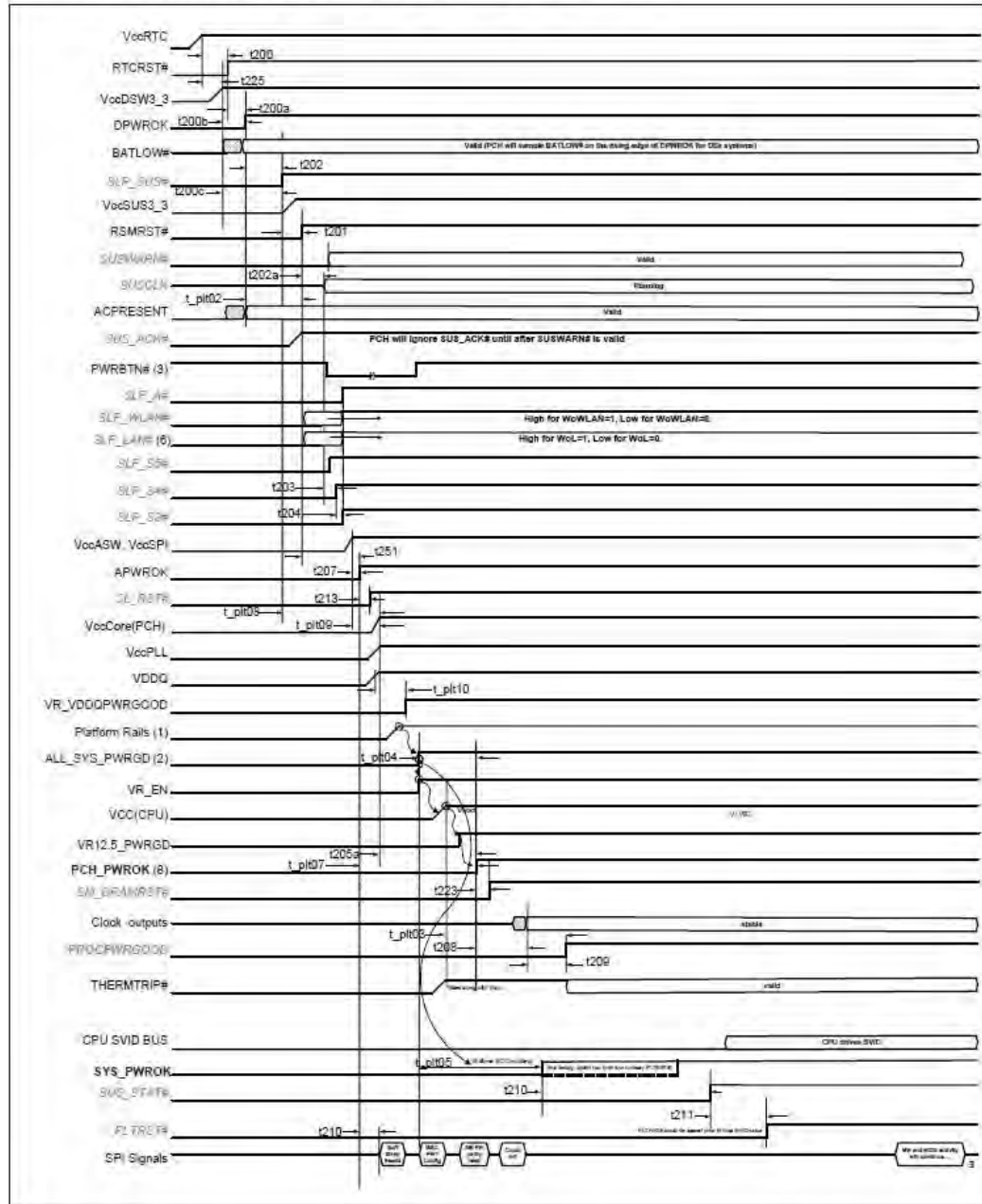
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CPU DC/DC	
TPS51622ARSMR 50-51	
INPUTS	OUTPUTS
B+	+VCC_CORE
SYSTEM DC/DC	
RT8243AZQW 47	
INPUTS	OUTPUTS
B+	+3VS/+5VS
SYSTEM DC/DC	
RT8207MZQW 48	
INPUTS	OUTPUTS
B+	+1.35V_VDDQ +0.675VS
SYSTEM DC/DC	
SY8206DQNC 49	
INPUTS	OUTPUTS
B+	+1.05VS
SYSTEM DC/DC	
SY8003DFC 52	
INPUTS	OUTPUTS
B+	+1.5VS
SYSTEM DC/DC	
RT8880BGQW 54-55	
INPUTS	OUTPUTS
B+	+VGA_CORE
SYSTEM DC/DC	
SY8003DFC 56	
INPUTS	OUTPUTS
B+	+1.8VS_VGA
SYSTEM DC/DC	
SY8003DFC 57	
INPUTS	OUTPUTS
B+	+0.95VS_VGA

Power ON Sequence

Timing Diagram for G3 to S0/M0 [Deep Sx Platform]



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Version change list (P.I.R. List)

Item	Date	Fixed Issue	Reason for change	Modify List	Phase
1	20131030		Delete 1.PQ307 2.charger air line power circuit 3.change AON7506 to SI7716(PQ106) 4.change NDS0610 to LBSS84L 5.change AON7506 to SI7716 6.change 47U 6.3V to 22U 6.3V (PCH8,PCH9) 7.PR9512 mount	1.customer request 2.customer request 3.customer common part 4.compal change 5.customer common part 6.vender reveiw	DB0 DB0 DB0 DB0
2	20131031		1.10U_0805_25V==>2200p_0402_50V not mount(PC160) 2.PC107,PR111,PC121,PC305,PR314 PC313,PC308,PR315,PC312,PCH4,PCZ3,PRZ13,PCZ13 PCZ20,PCZ26,PCW1,PCV4,PRV70,PCV107 3.change 147K_0402_1% to 237K_0402_1% (PRV34) change 560P_0402_50V7K to 470P_0402_50V7 (PCV88) change 10.7K_0402_1% to 22.6K_0402_1%(PRV47) change 9.76K_0402_1% to 5.6K_0402_1%(PRV51) change 15K_0402_1% to 19.1K_0402_1%(PRV55) change 910K_0402_5% to 20.5K_0402_1%(PRV75) change 910k_0402_1% to 910_0402_1%(PRV53) change 3.48K_0402_1% to 3.4K_0402_1%(PRV69) change 910k_0402_1% to 910_0402_1%(PRV77) 4.remove PR9510,PR9512,PR9514,PR9513 5.remove PC318,PRH10,PRW10,PCW13 6. PRH8,PRW8 not mount 7.22u/0805 6.3V to 22u/0603 6.3V PC1504,PC1501 PC1505,PC1802,PC1803,PC1805,PC1806,PC9502,PC9503, PC9505,PC9506,PCH9,PCH10,PCH11,PCH8 8.0.22U_0402_6.3V6K to 0.22U_0603_50V7K (PC128)	1.EMI feedback 2.EMI feedback 3.power vender feedback 4.power change fb sense 5.for compal module design 6.current limit design	DB0 DB0 DB0 DB1 DB1 DB1 DB1 DB1 DB1 SI1 SI1 SI1
3	20131101		1.remove PRW11	1.HW request	
4	20131112		1.not mount PRW7 2.change 0_0402_1% to 0_0402_5%(PR1502,PR1804, PR9504,PR9508,PR9511,PR9515)	2.AMD request	
5	20131202		1.not mount PRZ36,PRV32 and PCV86 2.PC128 change 0.22U_0603_25V to 0.22U_0402_6.3V6K 3.add PD16,PRV43 4.add PRV45,PRV48,PCV99 and PRV50	1.PWR request 2.PWR request 3. customer request 4.richtek request	SI1 SI1 SI2 SI2

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Version change list (P.I.R. List)

Item	Date	Fixed Issue	Reason for change	Modify List	Phase
6	20131210		add PRV78 1K_0402_1% PRV62 5.76K_0402_1% PRV64 10K_0402_1% PRV80 1K_0402_1% PRV79 10K_0402_1% PRV52 137K_0402_1%	RITCHTEK issue request	DB0 DB0 DB0 DB0
	20131221		PRM2 Change 4.7_1206_5% to 0_1206_5% PCM7 Change 680P_0603_50V7K to 1000P_0603_50V7K PR314 not mount==>mount PC313 not mount==>mount PR315 not mount==>mount PC312 not mount==>mount PCZ13 not mount==>mount PRZ13 not mount==>mount PCZ20 not mount==>mount (28W) PRZ26 not mount==>mount (28W)	EMI request	DB0 DB0 DB0 DB1 DB1
	20131226		PRV31 Change 10_0402_1% to 1_0402_1% PRV34 Change 127K_0402_1% to 84.5K_0402_1% PRV47 Change 22.6K_0402_1% to 7.32K_0402_1% PRV51 Change 5.6K_0402_1% to 12.4K_0402_1% PRV55 Change 19.1K_0402_1% to 14K_0402_1% PRV75 Change 20.5K_0402_1% to 2.8K_0402_1% PRV77 Change 910_0402_1% to 1.3K_0402_1% PRV53 Change 910_0402_1% to 1.3K_0402_1% PC128 Change 0.22U_0603_6.3V to 0.22U_0402_6.3V	RITCHTEK issue request	DB1 DB1 DB1 DB1 SI1
	20140102		PRM2 Change 0_1206_5% to 4.7_1206_5% PCM7 Change 1000P_0603_50V7K to 680P_0603_50V7K PUV1 change RT8880BGQW to RT8880CGQW	EMI request RITCHTEK request	SI1 SI1
	20140103		PR14,PQ2 and PR13 are not mount. PR11 Change 330_0402_1% to 680_0402_1%	Customer request	
	20140106		PRV80 mount==>not mount PRV79 not mount==>mount	RITCHTEK issue request	
	20140213		add PC8,PC9 and PC10 mount PR111,PC121,PC107 and PC129 PC107 2200P_0402_50V7K==>0.022_0402_25V PC129 0.1U_0402_50V7K==>0.022_0402_25V	EMC request EMC request	
	20140214		add PC161 2200P_0402_50V7K not mount	EMC request	SI1 SI1 SI2 SI2

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ZPL40/50/70 from DB-R to DB-R LA-B181P REV:0.1 -> 0.3 Modify <2013.11.28 - 2013.12.03>

Table with 5 columns: Rev, Item, Date, Intent, Change Cause, Modify Description. Contains change records for items 0.2.1 to 0.2.20.

ZPL40/50/70 from DB-R to SI LA-B181P REV:0.2 -> 0.3 Modify <2013.12.04 - 2013.12.17>

Table with 5 columns: Rev, Item, Date, Intent, Change Cause, Modify Description. Contains change records for items 0.3.1 to 0.3.29.

ZPL40/50/70 from DB-R to SI LA-B181P REV:0.3 -> 0.4 Modify <2013.12.18 - 2013.12.25>

Table with 5 columns: Rev, Item, Date, Intent, Change Cause, Modify Description. Contains change records for items 0.4.1 to 0.4.14.

ZPL40/50/70 from SI to P1-1 LA-B181P REV:0.3 -> 0.4 Modify <2014.02.05-2014>

Table with 5 columns: Rev, Item, Date, Intent, Change Cause, Modify Description. Contains change records for items 0.5.1 to 0.5.13.

Security Classification table and Compal Electronics, Inc. logo. Includes fields for Classification, Date, and Document Number.