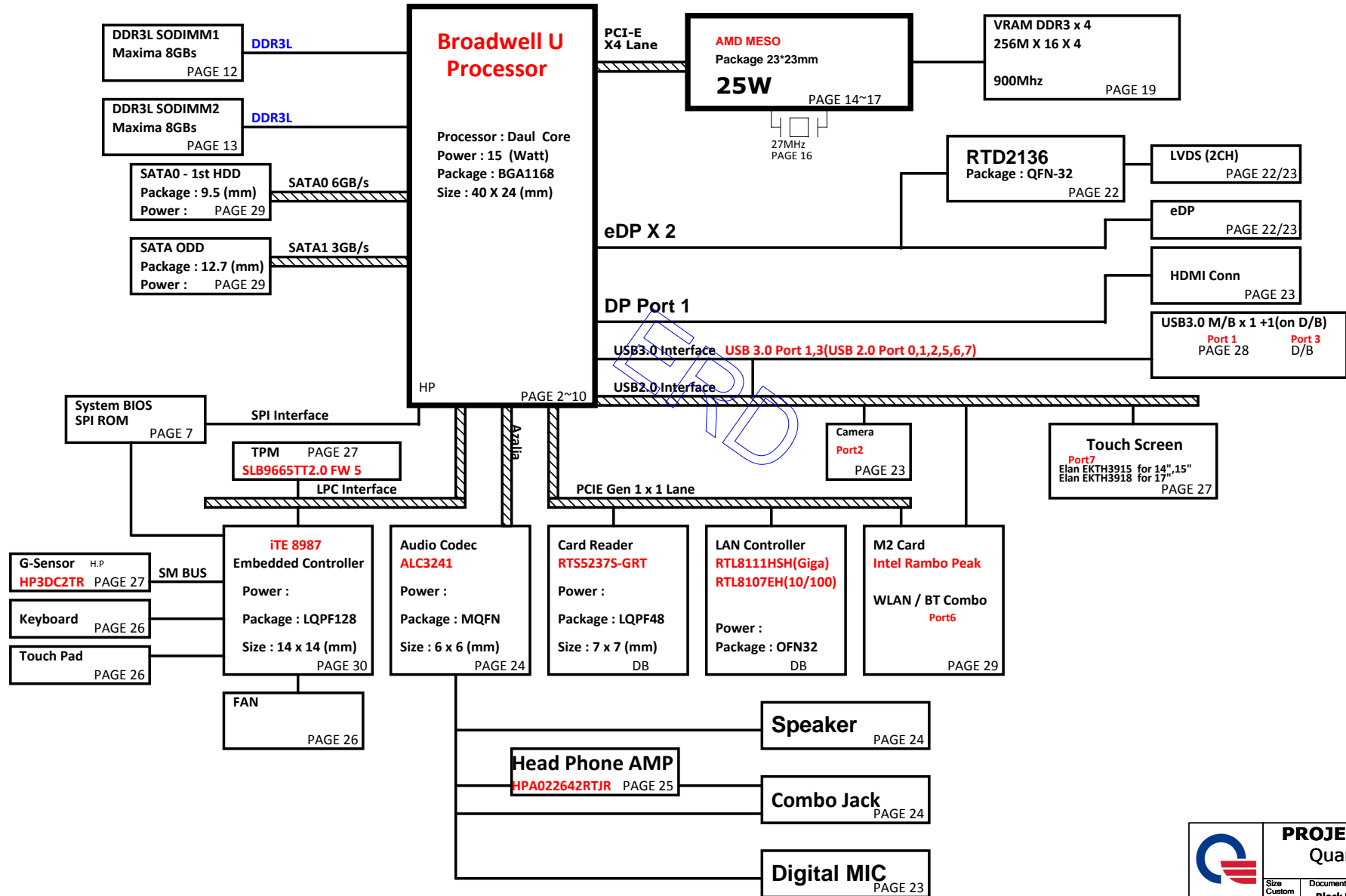

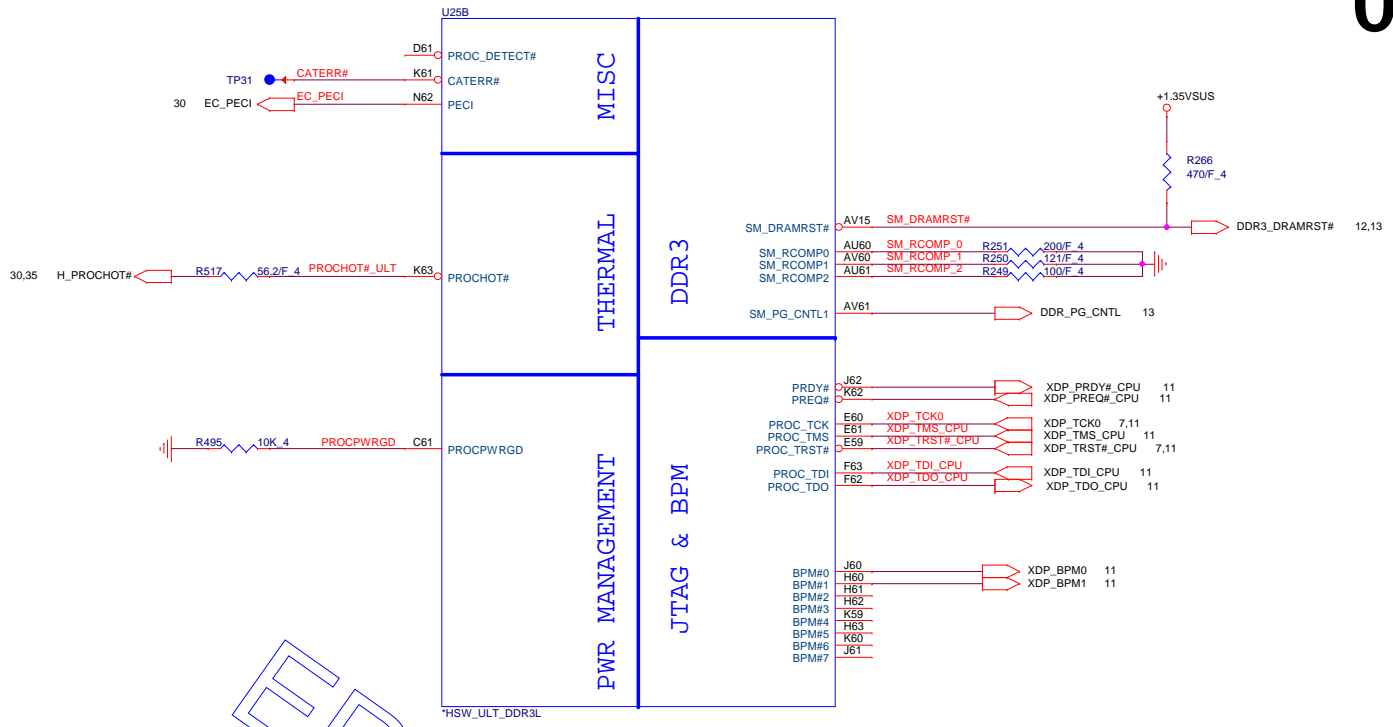
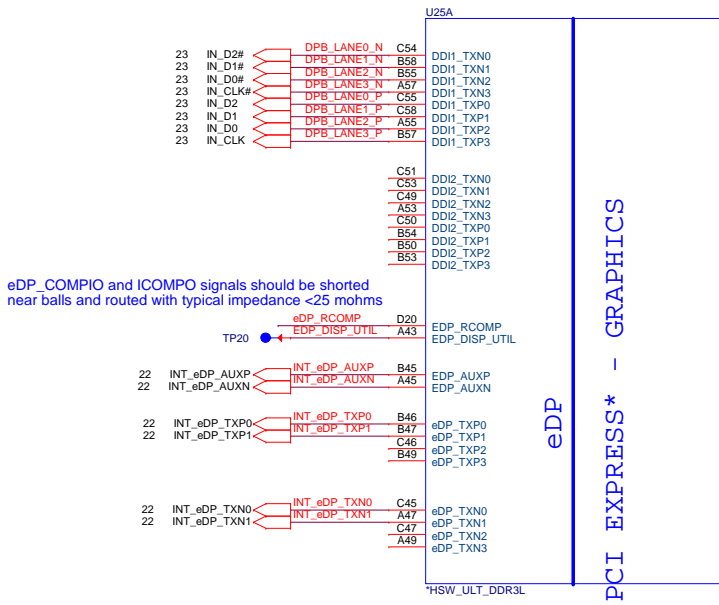


# X11 DIS (14" / 15" / 17") Chocolate X11 Intel Crescent Bay ULT Platform Block Diagram

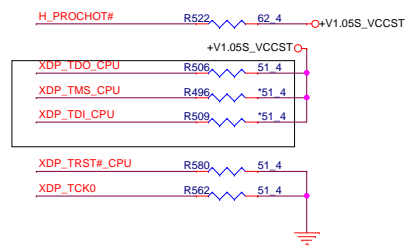


Note  
VGA/CPU need check PW

 <b>PROJECT : X11</b> Quanta Computer Inc.		
Size Custom	Document Number <b>Block Diagram</b>	Rev 1A
Date: Monday, January 05, 2015	Sheet	1 of 40



Processor pull-up (CPU)



ERD

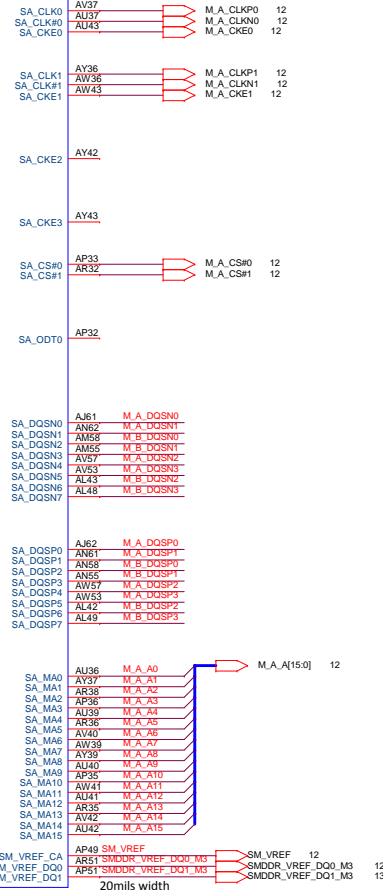
# Haswell ULT Processor (DDR3L)

- 12 M\_A\_DO[6:3:0]
- 13 M\_B\_DO[6:3:0]
- 12 M\_A\_DOSN[7:0]
- 12 M\_A\_DOSN[7:0]
- 13 M\_B\_DOSN[7:0]
- 13 M\_B\_DOSN[7:0]

U25C

- M\_A\_D00 AH63 SA\_D00
- M\_A\_D01 AH62 SA\_D01
- M\_A\_D02 AK63 SA\_D02
- M\_A\_D03 AR62 SA\_D03
- M\_A\_D04 AH61 SA\_D04
- M\_A\_D05 AH60 SA\_D05
- M\_A\_D06 AK61 SA\_D06
- M\_A\_D07 AR60 SA\_D07
- M\_A\_D08 AM63 SA\_D08
- M\_A\_D09 AM62 SA\_D09
- M\_A\_D10 AR63 SA\_D10
- M\_A\_D11 AP62 SA\_D11
- M\_A\_D12 AM61 SA\_D12
- M\_A\_D13 AM60 SA\_D13
- M\_A\_D14 AP61 SA\_D14
- M\_A\_D15 AP60 SA\_D15
- M\_B\_D01 AR58 SA\_D16
- M\_B\_D02 AM57 SA\_D17
- M\_B\_D03 AK57 SA\_D18
- M\_B\_D04 AL58 SA\_D19
- M\_B\_D05 AK58 SA\_D20
- M\_B\_D06 AR57 SA\_D21
- M\_B\_D07 AN57 SA\_D22
- M\_B\_D08 AP55 SA\_D23
- M\_B\_D09 AR55 SA\_D24
- M\_B\_D10 AM54 SA\_D25
- M\_B\_D11 AK54 SA\_D26
- M\_B\_D12 AL55 SA\_D27
- M\_B\_D13 AK55 SA\_D28
- M\_B\_D14 AK54 SA\_D29
- M\_B\_D15 AK54 SA\_D30
- M\_A\_D16 AY58 SA\_D31
- M\_A\_D17 AV58 SA\_D32
- M\_A\_D18 AV56 SA\_D33
- M\_A\_D19 AW56 SA\_D34
- M\_A\_D20 AV58 SA\_D35
- M\_A\_D21 AR58 SA\_D36
- M\_A\_D22 AV56 SA\_D37
- M\_A\_D23 AU56 SA\_D38
- M\_A\_D24 AV54 SA\_D39
- M\_A\_D25 AW54 SA\_D40
- M\_A\_D26 AV52 SA\_D41
- M\_A\_D27 AV52 SA\_D42
- M\_A\_D28 AV54 SA\_D43
- M\_A\_D29 AU54 SA\_D44
- M\_A\_D30 AR52 SA\_D45
- M\_A\_D31 AU52 SA\_D46
- M\_B\_D16 AK40 SA\_D47
- M\_B\_D17 AK42 SA\_D48
- M\_B\_D18 AM43 SA\_D49
- M\_B\_D19 AM45 SA\_D50
- M\_B\_D20 AK46 SA\_D51
- M\_B\_D21 AK43 SA\_D52
- M\_B\_D22 AM40 SA\_D53
- M\_B\_D23 AK42 SA\_D54
- M\_B\_D24 AM46 SA\_D55
- M\_B\_D25 AK46 SA\_D56
- M\_B\_D26 AM48 SA\_D57
- M\_B\_D27 AK49 SA\_D58
- M\_B\_D28 AM48 SA\_D59
- M\_B\_D29 AK46 SA\_D60
- M\_B\_D30 AM51 SA\_D61
- M\_B\_D31 AK51 SA\_D62
- SA\_D63

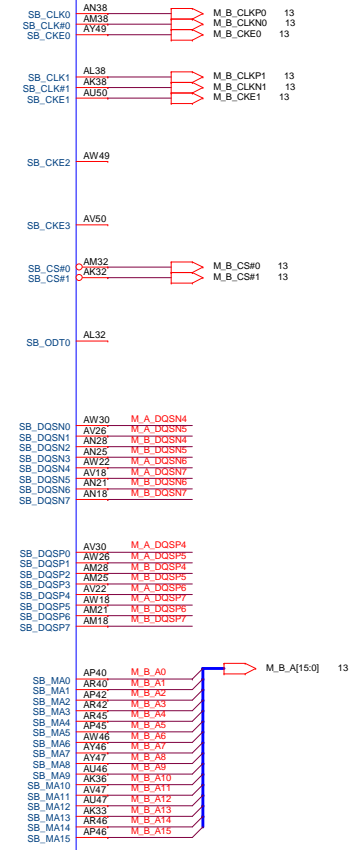
DDR SYSTEM MEMORY A



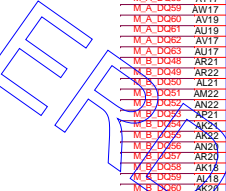
U25D

- M\_A\_D032 AY31 SB\_D00
- M\_A\_D033 AW31 SB\_D01
- M\_A\_D034 AY29 SB\_D02
- M\_A\_D035 AW29 SB\_D03
- M\_A\_D037 AU31 SB\_D04
- M\_A\_D038 AV29 SB\_D05
- M\_A\_D039 AU29 SB\_D06
- M\_A\_D040 AY27 SB\_D07
- M\_A\_D041 AW27 SB\_D08
- M\_A\_D042 AY25 SB\_D09
- M\_A\_D043 AW25 SB\_D10
- M\_A\_D045 AU27 SB\_D11
- M\_A\_D046 AV25 SB\_D12
- M\_A\_D047 AU25 SB\_D13
- M\_B\_D032 AM29 SB\_D14
- M\_B\_D033 AK29 SB\_D15
- M\_B\_D035 AK28 SB\_D16
- M\_B\_D036 AR29 SB\_D17
- M\_B\_D037 AR29 SB\_D18
- M\_B\_D038 AR28 SB\_D19
- M\_B\_D039 AP28 SB\_D20
- M\_B\_D040 AK26 SB\_D21
- M\_B\_D041 AR26 SB\_D22
- M\_B\_D042 AR25 SB\_D23
- M\_B\_D043 AP25 SB\_D24
- M\_B\_D044 AK26 SB\_D25
- M\_B\_D045 AM26 SB\_D26
- M\_B\_D046 AK25 SB\_D27
- M\_B\_D047 AL25 SB\_D28
- M\_A\_D048 AY23 SB\_D29
- M\_A\_D049 AW23 SB\_D30
- M\_A\_D050 AY21 SB\_D31
- M\_A\_D051 AW21 SB\_D32
- M\_A\_D053 AU23 SB\_D33
- M\_A\_D054 AV21 SB\_D34
- M\_A\_D056 AY19 SB\_D35
- M\_A\_D057 AW19 SB\_D36
- M\_A\_D058 AY17 SB\_D37
- M\_A\_D059 AW17 SB\_D38
- M\_A\_D060 AV19 SB\_D39
- M\_A\_D061 AU19 SB\_D40
- M\_A\_D062 AV17 SB\_D41
- M\_A\_D063 AR21 SB\_D42
- M\_B\_D063 AR21 SB\_D43
- M\_B\_D064 AK18 SB\_D44
- M\_B\_D065 AL18 SB\_D45
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- M\_B\_D071 AK22 SB\_D51
- M\_B\_D072 AK21 SB\_D52
- M\_B\_D073 AK21 SB\_D53
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- M\_B\_D080 AK21 SB\_D60
- M\_B\_D081 AK21 SB\_D61
- M\_B\_D082 AK21 SB\_D62
- M\_B\_D083 AP18 SB\_D63

DDR SYSTEM MEMORY B



- 12 M\_A\_BS#0 AU35 SA\_BA0
- 12 M\_A\_BS#1 AU35 SA\_BA1
- 12 M\_A\_BS#2 AU35 SA\_BA2
- 12 M\_A\_CAS# AY34 SA\_CAS#
- 12 M\_A\_RAS# AY34 SA\_RAS#
- 12 M\_A\_WE# AW34 SA\_WE#



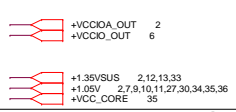
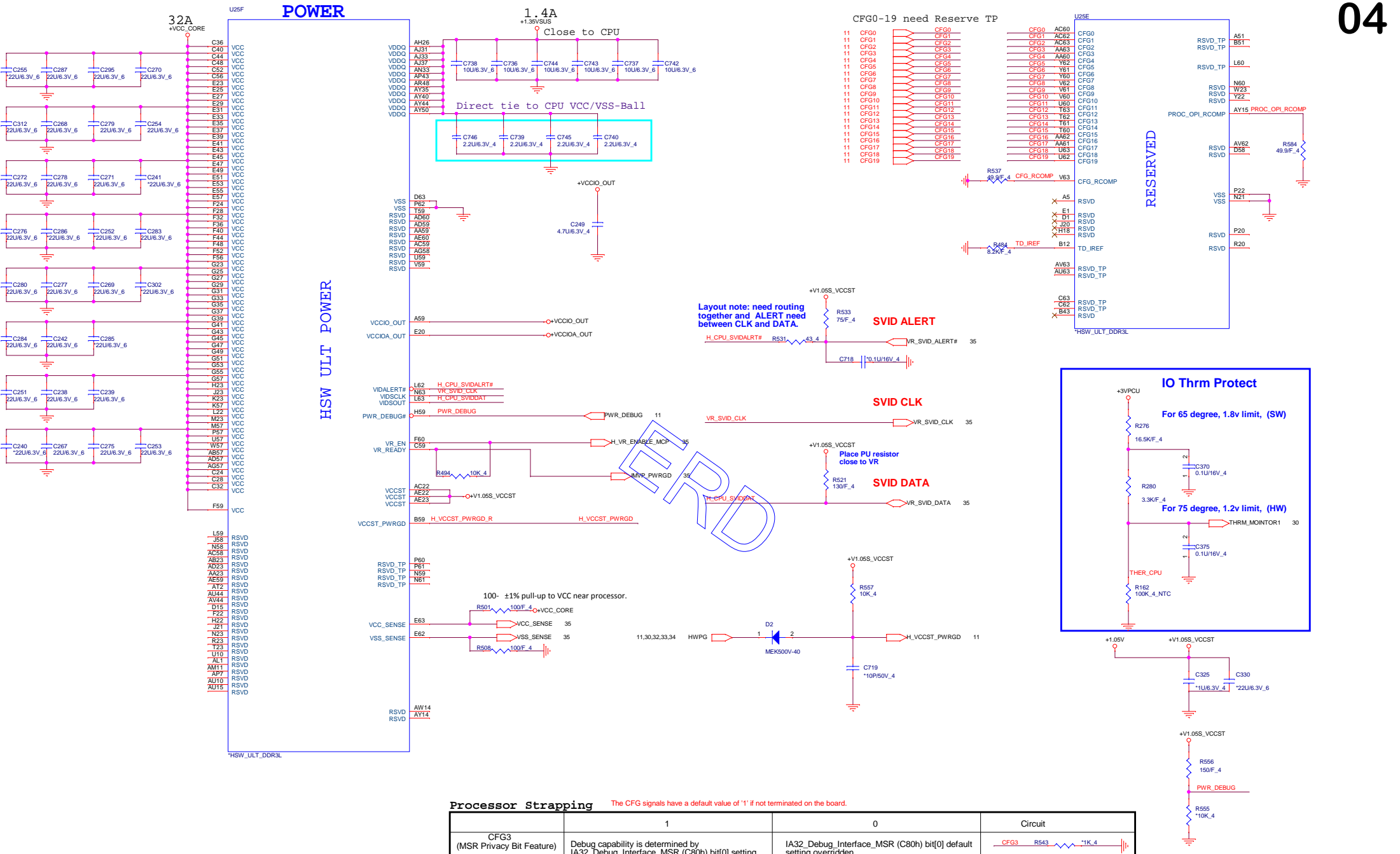
\*HSW\_ULT\_DDR3L

20mils width

INT HSW\_ULT\_DDR3L

**PROJECT : X11**  
**Quanta Computer Inc.**

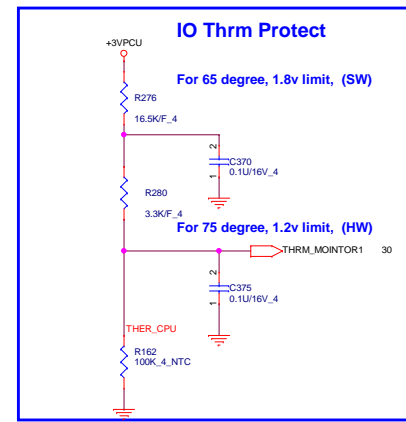
Size	Document Number	Rev
Custom	ULT 2/9 (DDR3 I/F)	1A
Date: Monday, January 05, 2015		Sheet 3 of 40



**Processor Strapping**

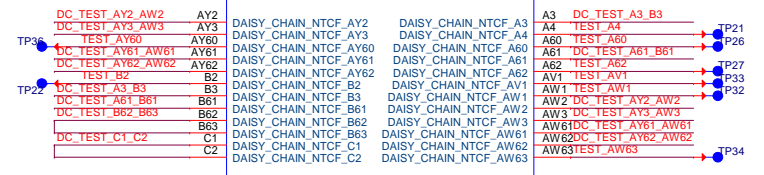
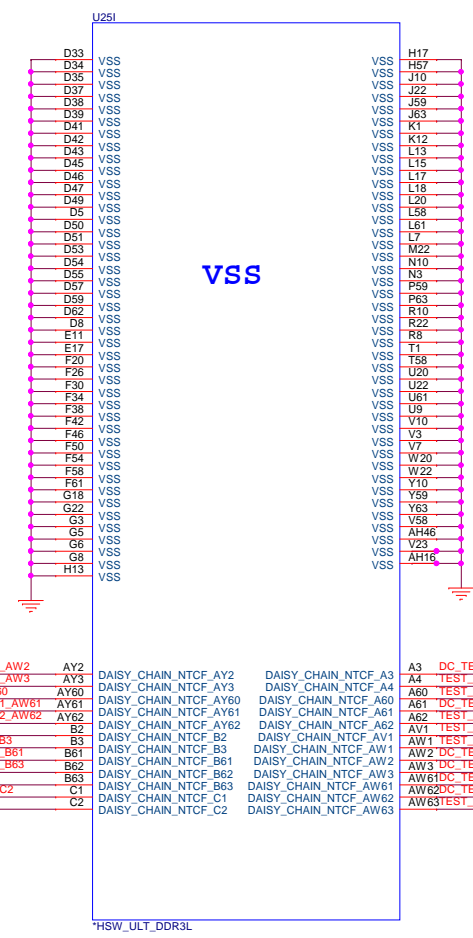
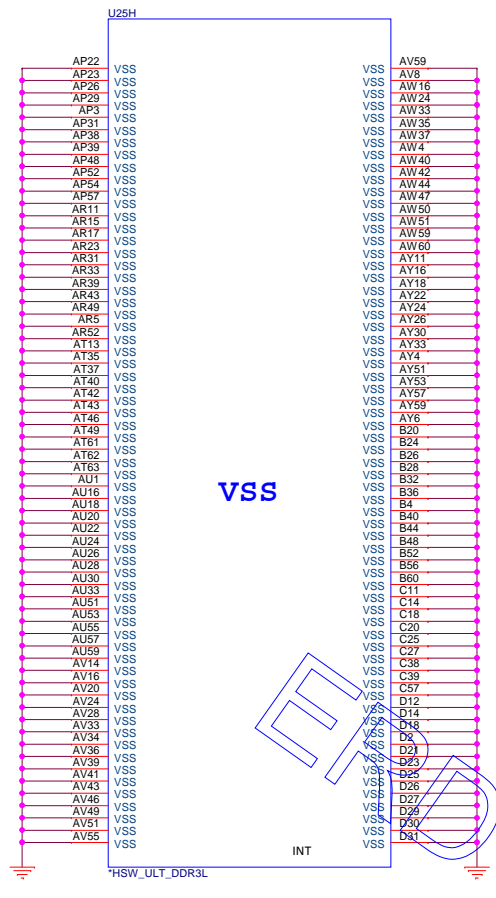
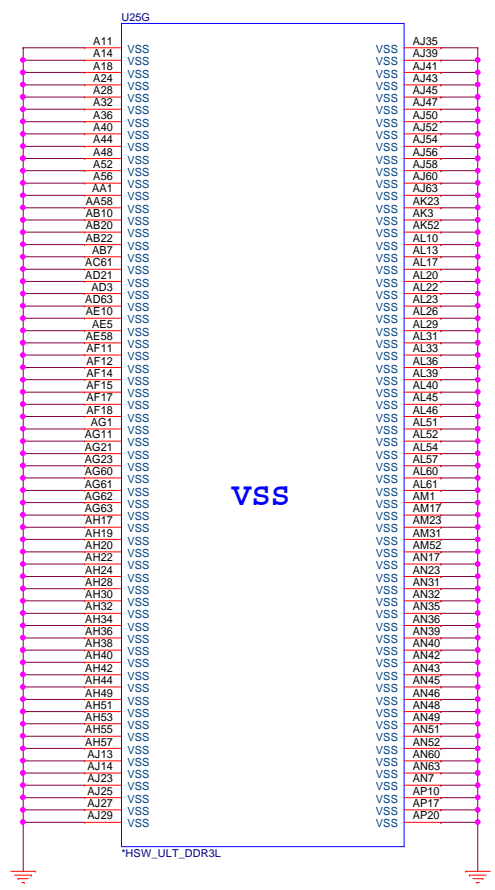
The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (MSR Privacy Bit Feature)	Debug capability is determined by IA32_Debug_Interface_MSR (C80h) bit[0] setting	IA32_Debug_Interface_MSR (C80h) bit[0] default setting overridden	
CFG4 (eDP enable)	Disabled	Enabled	



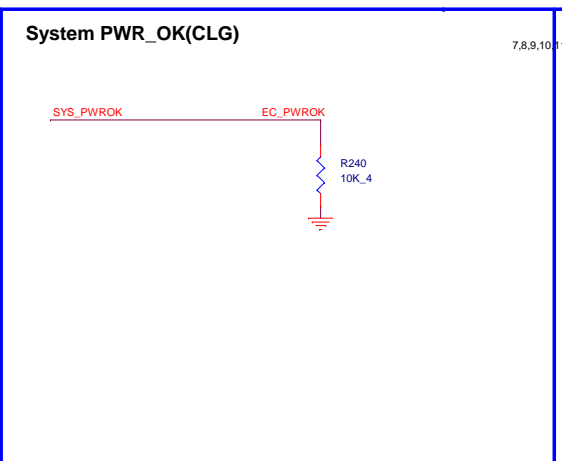
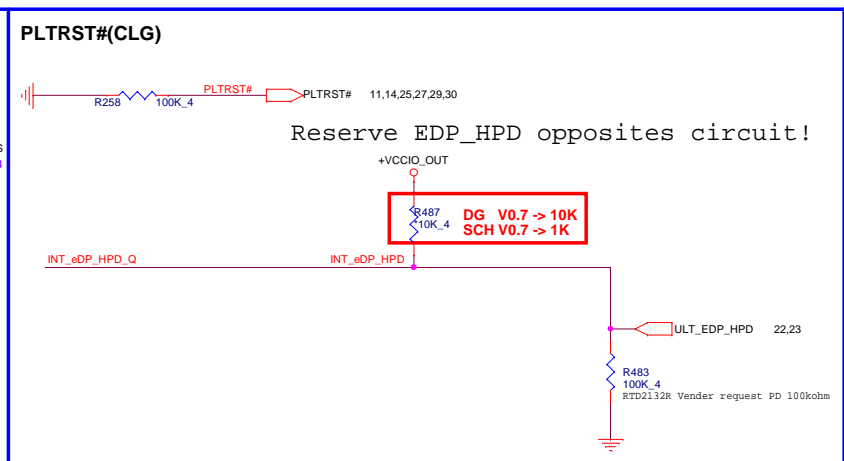
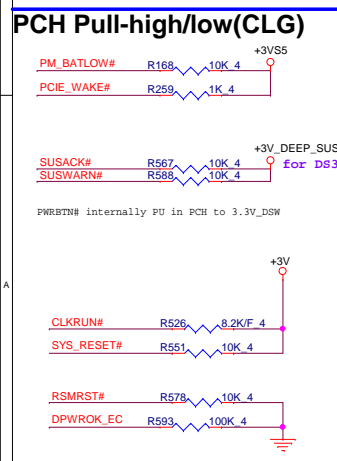
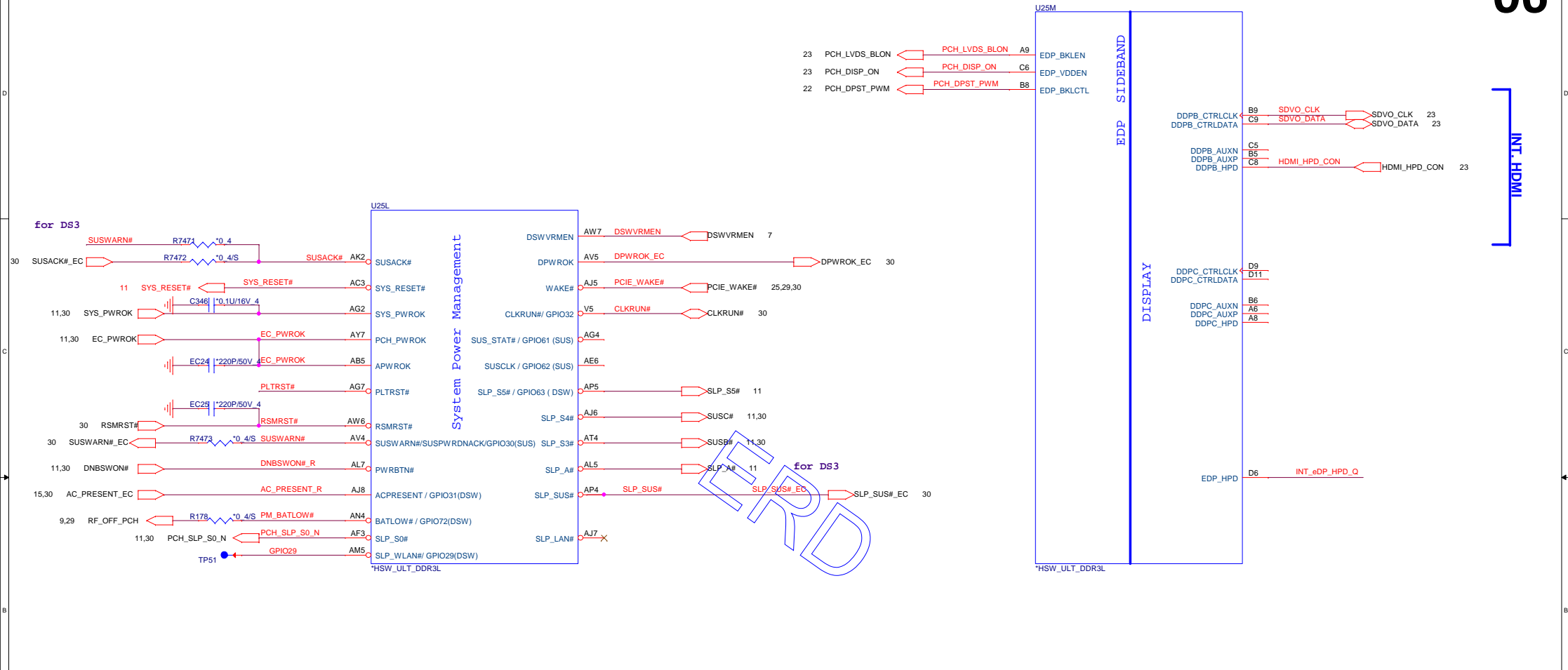
**PROJECT : X11**  
**Quanta Computer Inc.**

Size Custom Document Number 04 - ULT 3/9 (POWER-1) Rev 1A  
 Date: Monday, January 05, 2015 Sheet 4 of 40



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Quanta Computer Inc.

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7,8,9,10,11,12,13,22,23,24,25,26,27,29,30,35,36,39

+3V

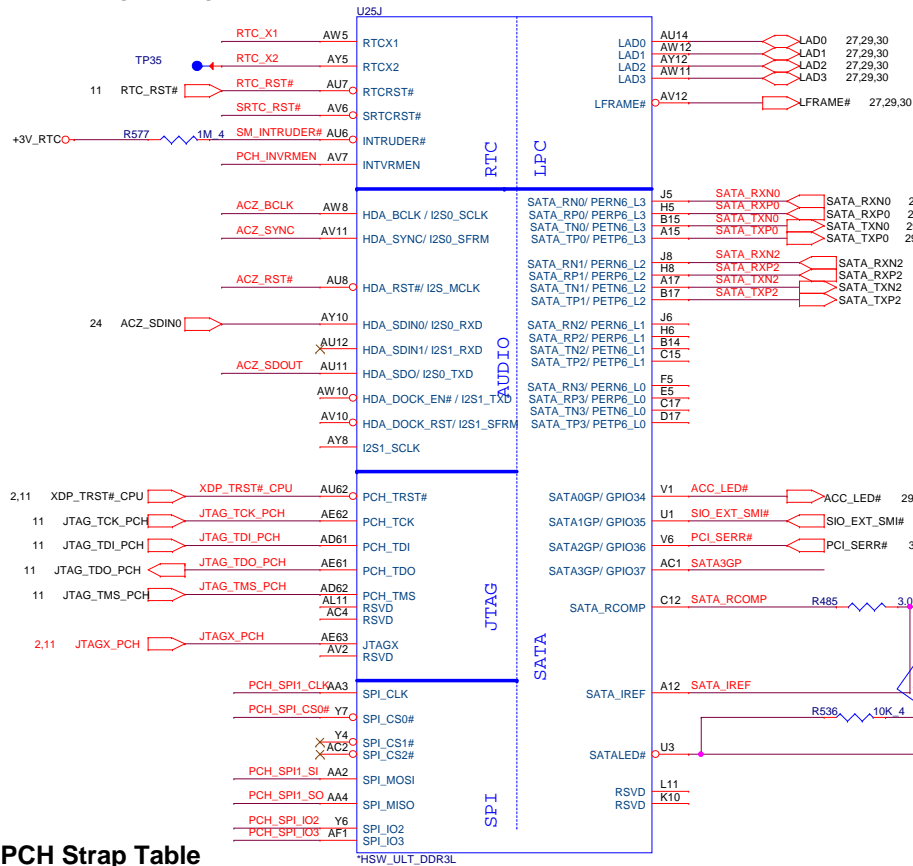
+3VS5

**PROJECT : X11**

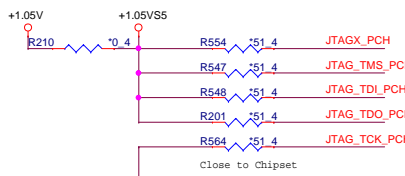
**Quanta Computer Inc.**

Size Custom	Document Number <b>ULT 5/9(Power Manger)</b>	Rev 1A
Date: Monday, January 05, 2015	Sheet 6 of	40

# Lynx Point-LP Platform Controller Hub (HDA, JTAG, SATA)



**HDD (SATA3 6.0Gb/s)**  
**ODD (SATA2 3.0Gb/s)**

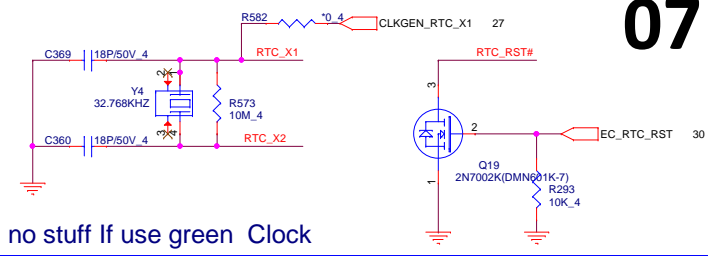


**DG recommended that SATA AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.**

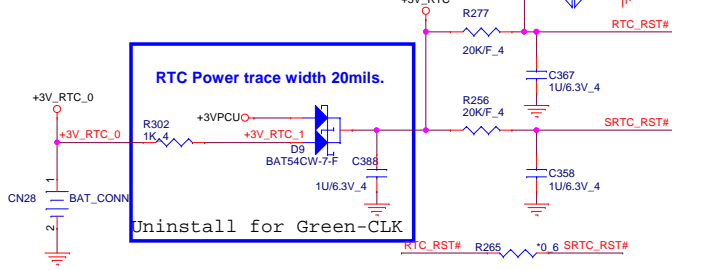
## PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit												
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode													
SDIO_D0 / GPIO66	Top-Block Swap	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)													
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC0 - R575 - 330K 4 - PCH_INVRMEN												
HDA_SDO /I2S0_TXD	Flash Descriptor Security Only for Interposer	PWROK	0 = Default (weak pull-down 20K) 1 = Can be Overriden	30 GPIO33_EC - R581 - 1K 4 - ACZ_SDOOUT												
GSPI0_MOSI / GPIO86	Boot BIOS Selection	PWROK	<table border="1"> <tr> <th>GNT0#</th> <th>Boot Location</th> </tr> <tr> <td>1</td> <td>LPC</td> </tr> <tr> <td>0</td> <td>SPI(Default)</td> </tr> </table>	GNT0#	Boot Location	1	LPC	0	SPI(Default)							
GNT0#	Boot Location															
1	LPC															
0	SPI(Default)															
GPIO15	TLS Confidentiality	PWROK	0 = ME Crypto Transport Layer Security cipher suite with no confidentiality(Default) 1 = Intel ME Crypto TLS cipher suite with confidentiality													
DSWVRMEN	Deep Sx Well On-Die Voltage Regulator Enable	ALWAYS	Should be always pull-up	+3V_RTC0 - R576 - 330K 4 - DSWVRMEN 6												
				<table border="1"> <tr> <td>30</td> <td>PCH_SPL_CS0#_R</td> <td>PCH_SPL_CS0#_R</td> </tr> <tr> <td>30</td> <td>PCH_SPL_CLK#_R</td> <td>PCH_SPL_CLK#_R</td> </tr> <tr> <td>30</td> <td>PCH_SPL_SI#_R</td> <td>PCH_SPL_SI#_R</td> </tr> <tr> <td>30</td> <td>PCH_SPL_SO#_R</td> <td>PCH_SPL_SO#_R</td> </tr> </table>	30	PCH_SPL_CS0#_R	PCH_SPL_CS0#_R	30	PCH_SPL_CLK#_R	PCH_SPL_CLK#_R	30	PCH_SPL_SI#_R	PCH_SPL_SI#_R	30	PCH_SPL_SO#_R	PCH_SPL_SO#_R
30	PCH_SPL_CS0#_R	PCH_SPL_CS0#_R														
30	PCH_SPL_CLK#_R	PCH_SPL_CLK#_R														
30	PCH_SPL_SI#_R	PCH_SPL_SI#_R														
30	PCH_SPL_SO#_R	PCH_SPL_SO#_R														

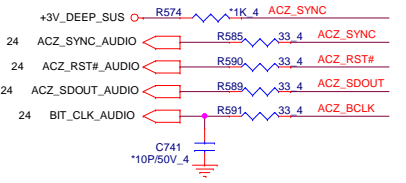
## RTC Clock 32.768KHz



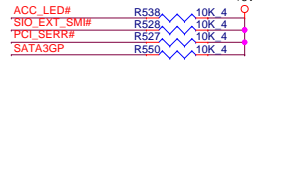
## RTC Circuitry(RTC)



## HDA Bus(CLG)

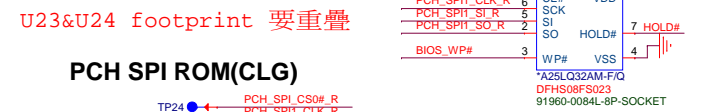


## GPIO Pull UP

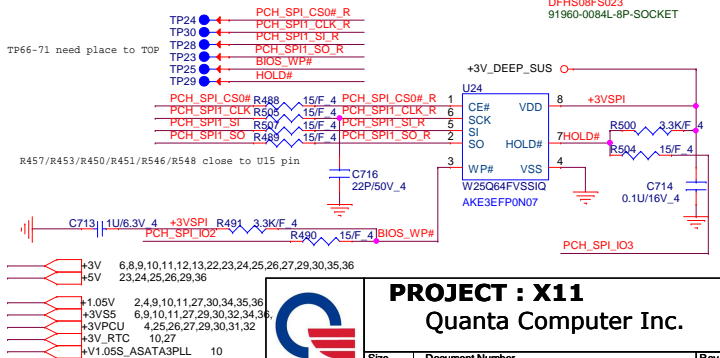


Vender	Size	P/N
EON	8MB	AKE3EZN0Q01 (EN25QH64-104HIP)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)
Socket		DFHS08FS023

## 4M SPI ROM Socket



## PCH SPI ROM(CLG)

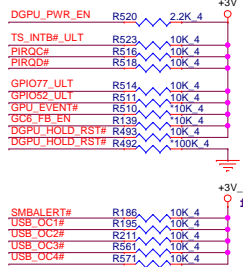


**PROJECT : X11**  
**Quanta Computer Inc.**

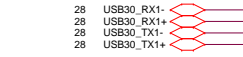
Size	Document Number	Rev
Custom	ULT 6/9(SATA/HDA)	1A
Date: Tuesday, January 06, 2015	Sheet 7 of	40

# Lynx Point-LP Platform Controller Hub (HDA, JTAG, SATA)

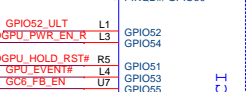
## PCI/USBOC# Pull-up(CLG)



## USB3.0 M/B



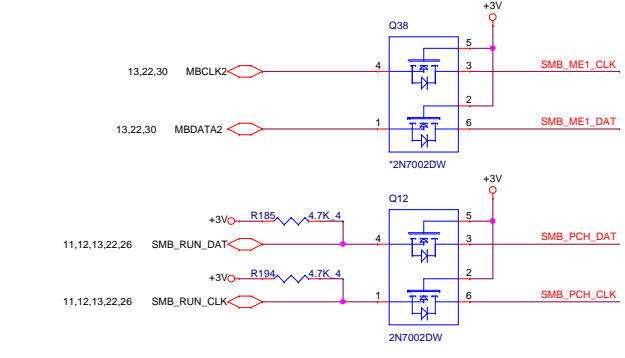
## GPIO77\_ULT



## OC0# / GPIO40(SUS)



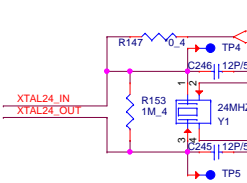
## SMBus/Pull-up(CLG)



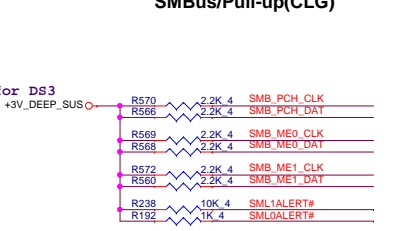
## CLK\_REQ/Strap Pin(CLG)



## CLK\_REQ/Strap Pin(CLG)

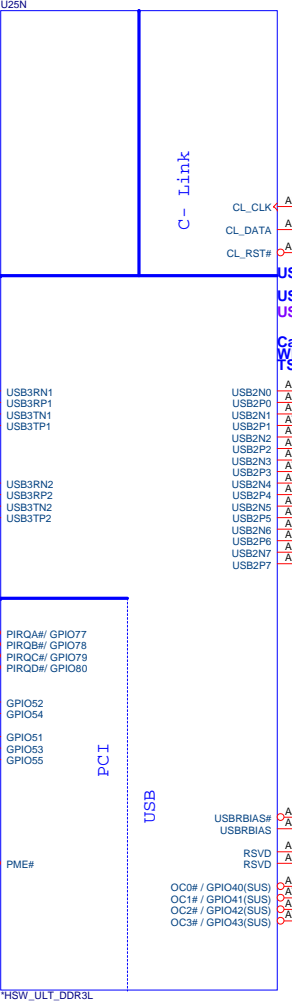


## SMBus/Pull-up(CLG)



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Quanta Computer Inc.

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ULT 7/9 (PCIe/USB/CLK)		
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## Cardreader



## WLAN



## LAN



## VGA



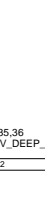
## SMBUS



## PCI \*



## CLOCK SIGNALS

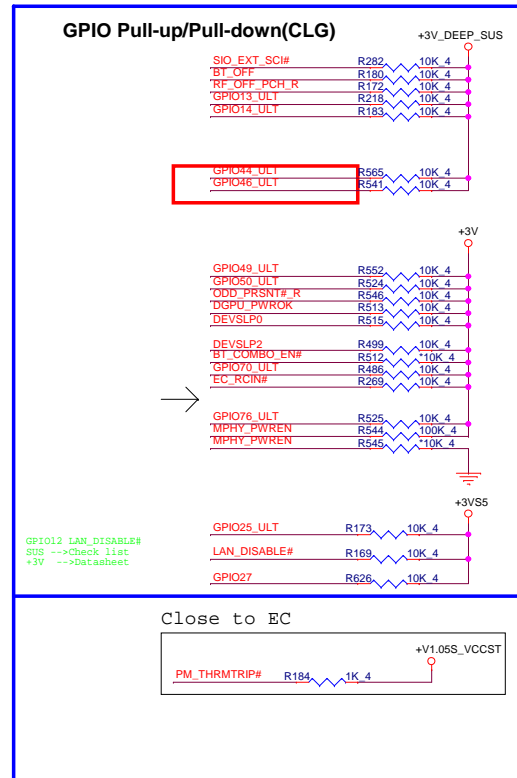
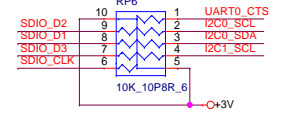
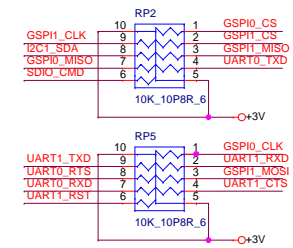
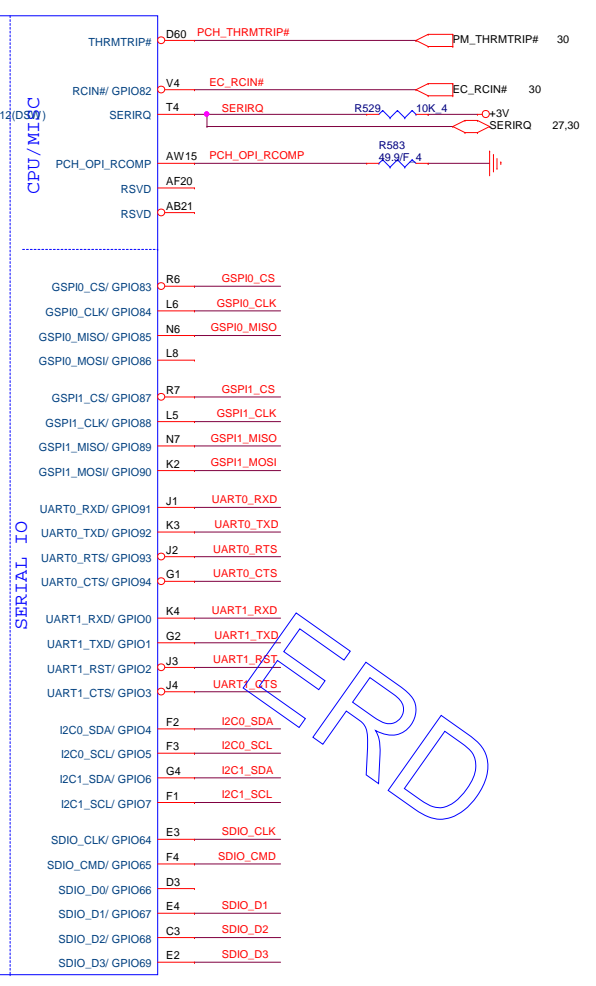
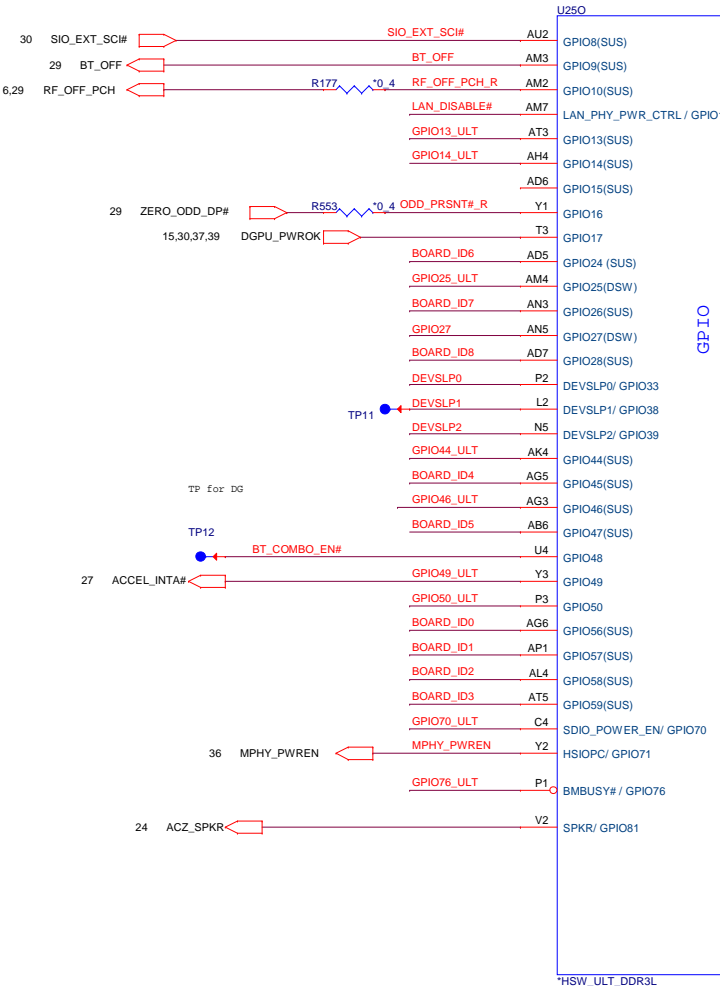


**PROJECT : X11**  
Quanta Computer Inc.

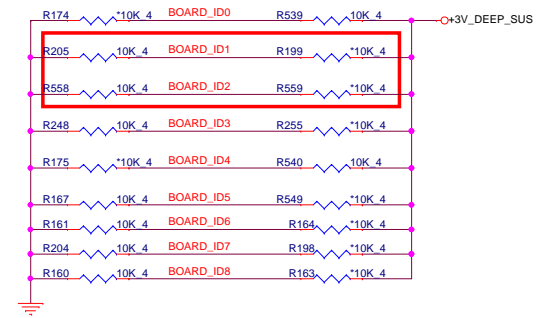
Size Custom	Document Number	Rev 1A
ULT 7/9 (PCIe/USB/CLK)		
Date: Monday, January 05, 2015	Sheet 8 of 40	



# Lynx Point-LP Controller Hub (HDA,JTAG,SATA) Haswell (GPIO)



Model	BOARD_ID[8:7]	BOARD_ID[6:5]	Board ID [4:3]	BOARD_ID[2:1]	BOARD_ID0
Definition	Reserve (Default = 00)	Reserve (Default = 00)	00 Single Rank (x12) 01 Dual Rank (x12) 10 Meso-AMD (x11) 11 Reserve	00 14" 01 15" 10 17"	0 : UMA 1 : DIS

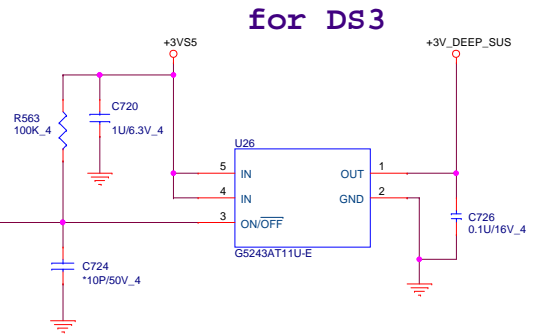
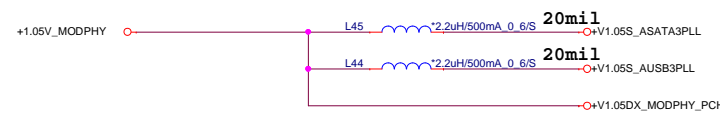
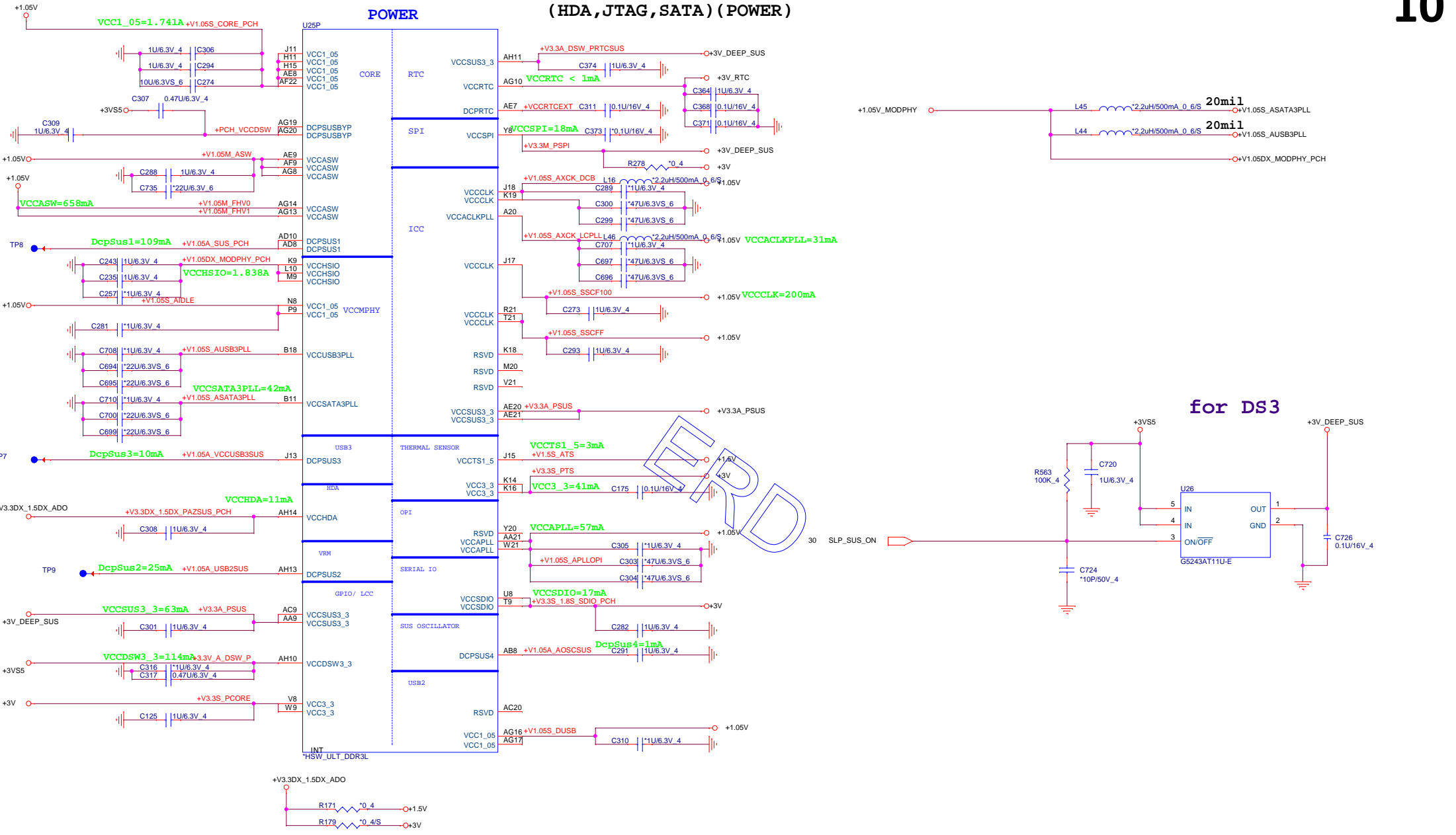


6,7,8,10,11,12,13,22,23,24,25,26,27,29,30,35,36  
6,10,11,27,29,30,32,34,36,37,39

PROJECT : X11  
Quanta Computer Inc.

Size Custom Document Number ULT 8/9 (GPIO/MISC) Rev 1A  
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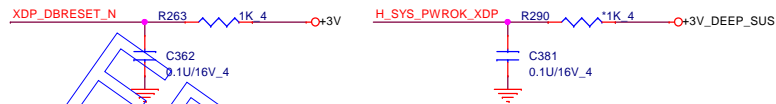
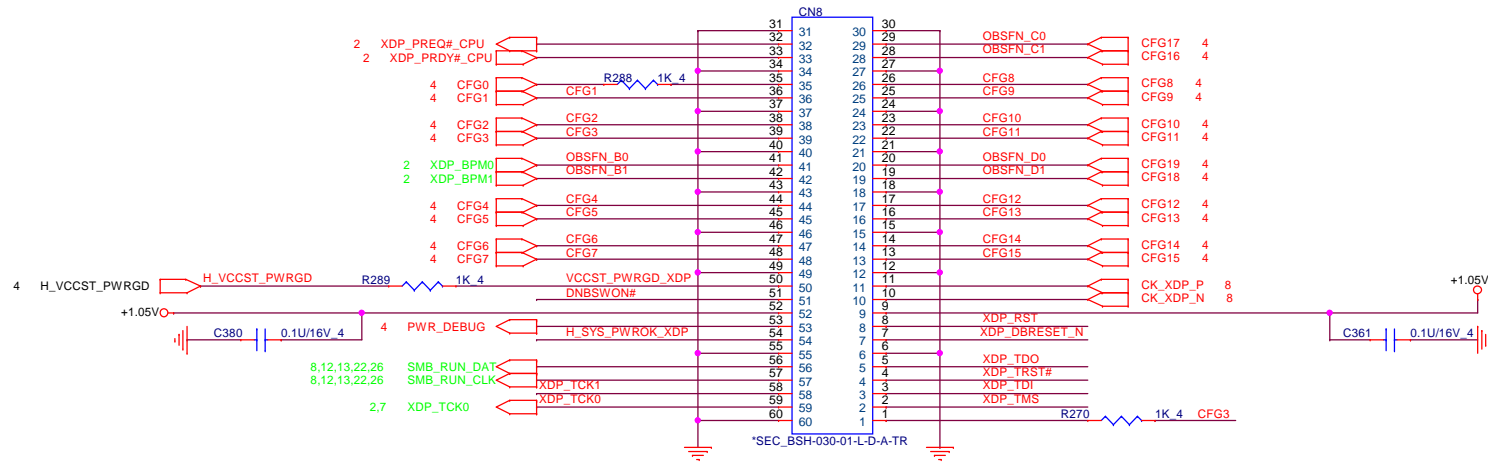
# Lynx Point-LP Platform Controller Hub (HDA, JTAG, SATA) (POWER)



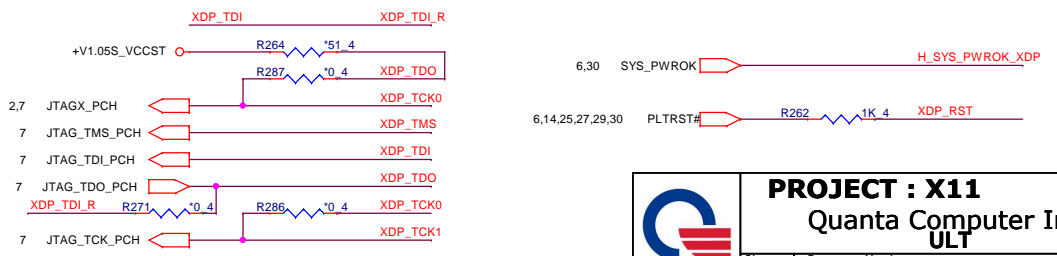
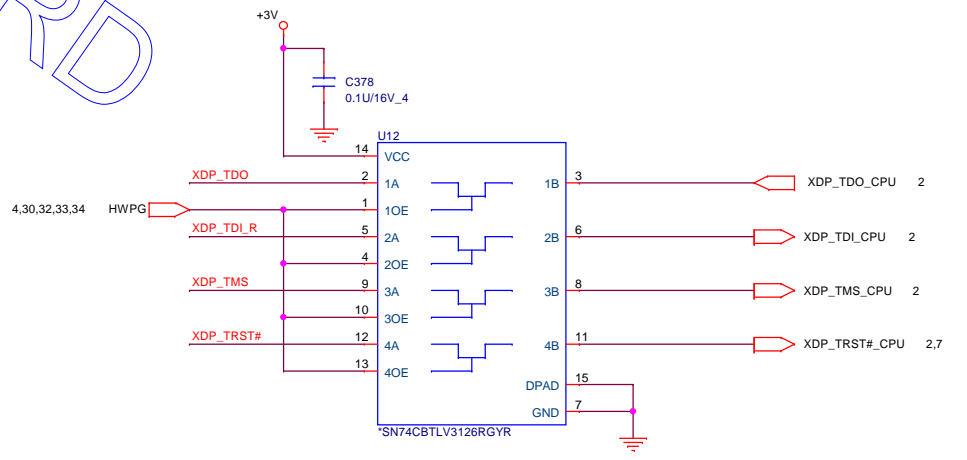
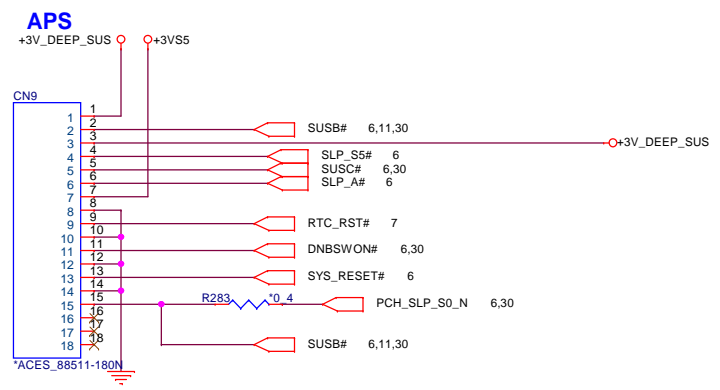
6,7,8,9,11,12,13,22,23,24,25,26,27,29,30,35,36	+3V
23,24,25,26,29,36	+5V
2,4,7,9,11,27,30,34,35,36	+1.05V
6,9,11,27,29,30,32,34,36,37,39	+3VS5
13,25,28,32,33,34,35,36,37,39	+5VS5
8	+1.05S_AUSB3PLL
7	+1.05S_ASATA3PLL
8	+1.05S_AXCK_LCPDLL
7,27	+3V_RTC
2,4,12,13,33	+1.35VSUS

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Quanta Computer Inc.

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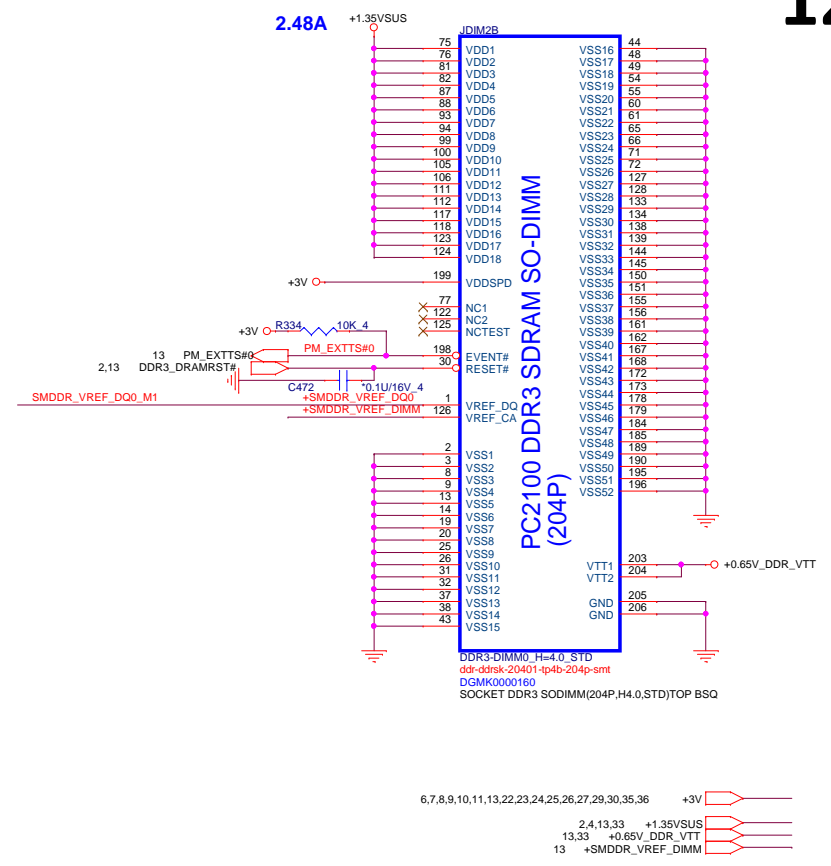
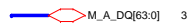
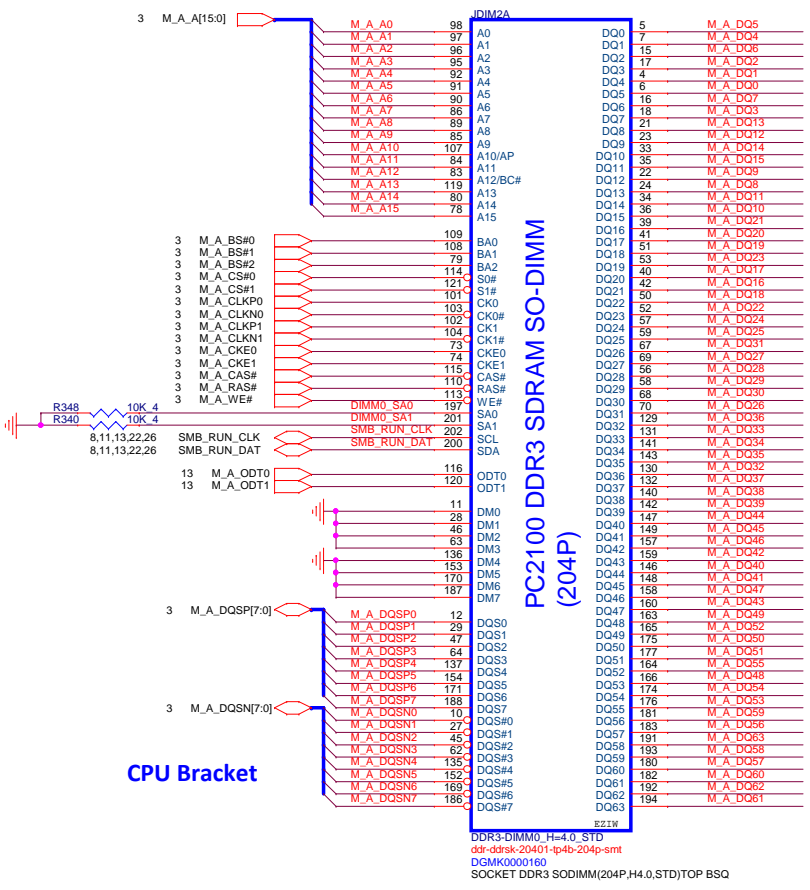


ERD

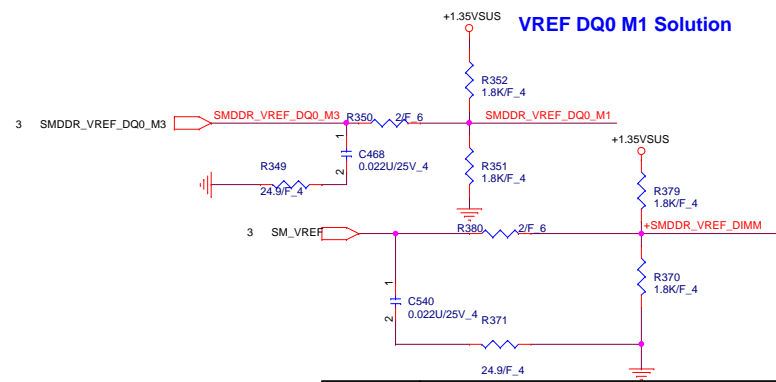
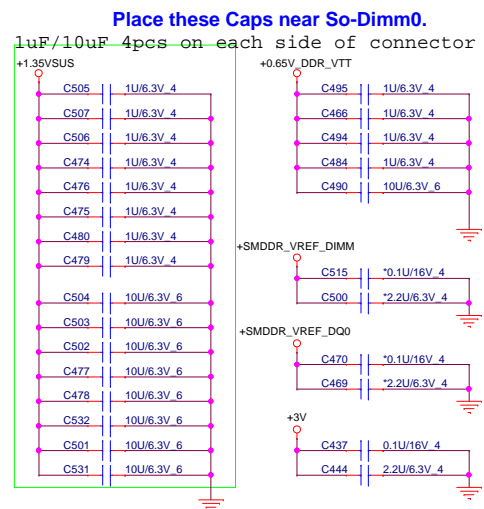
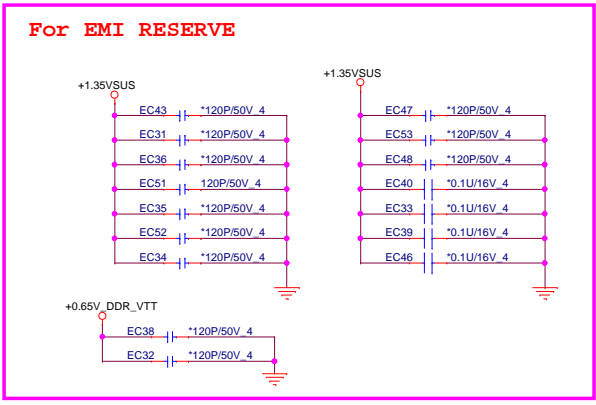


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**Quanta Computer Inc.**  
**ULT**  
 Size Document Number Rev  
**HSW XDP & APS** 1A  
 Date: Monday, January 05, 2015 Sheet 11 of 40

DIMM & Footprint 同Joshua提供



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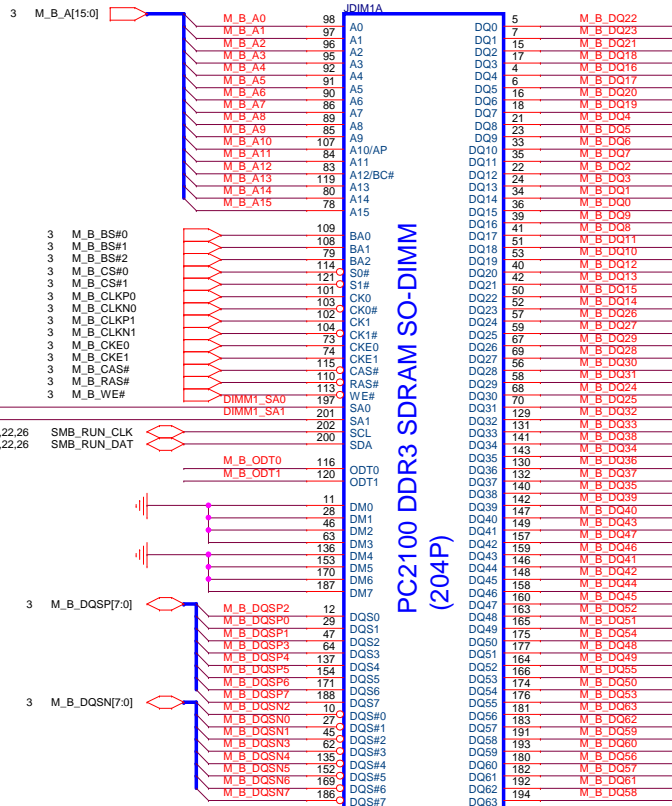


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Quanta Computer Inc.

Size Custom	Document Number <b>DDR3 DIMM0-STD(4.0H)</b>	Rev 1A
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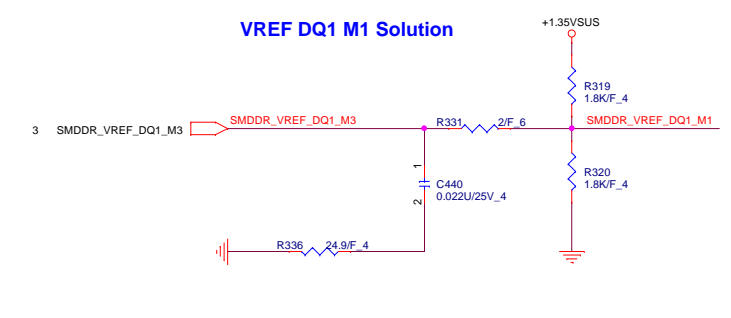
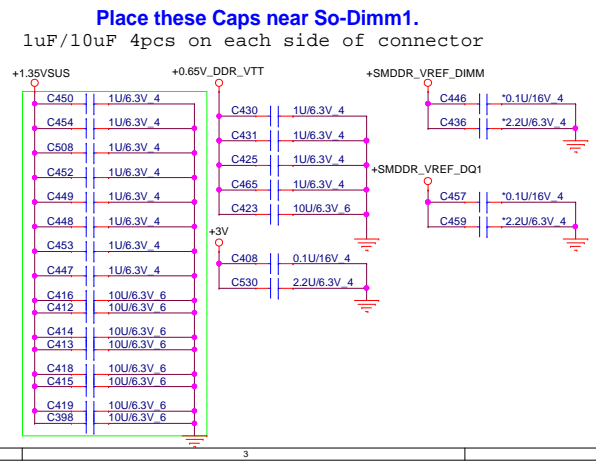
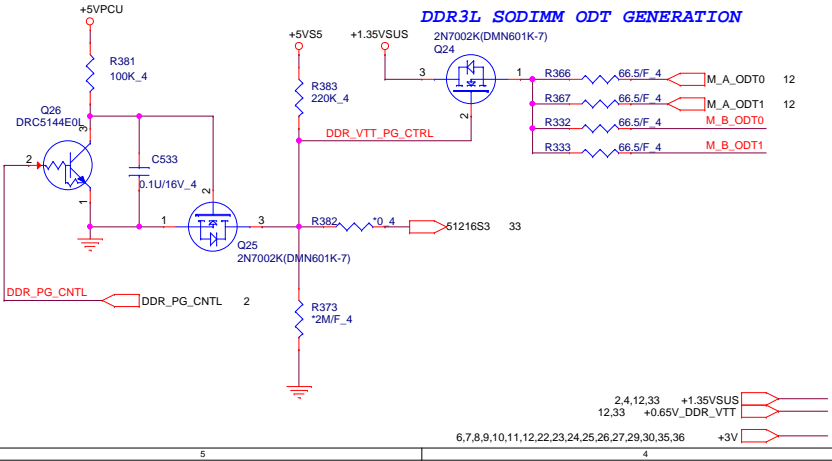
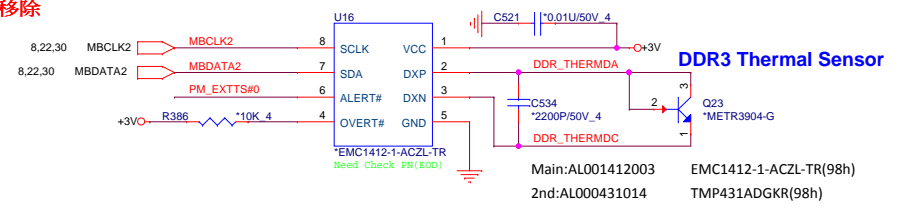
DIMM & Footprint 同Joshua提供

M\_B\_DQ[63:0] 3



ERD

Local Thermal Sensor mv可移除

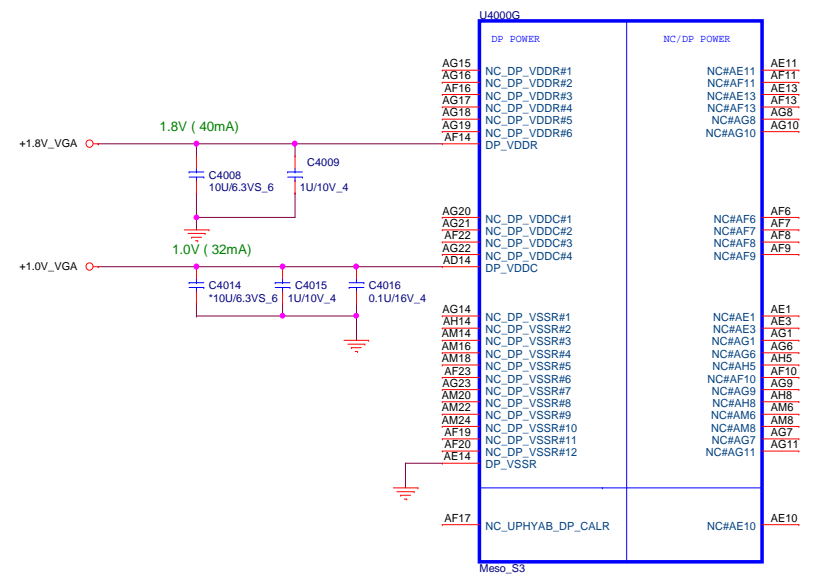
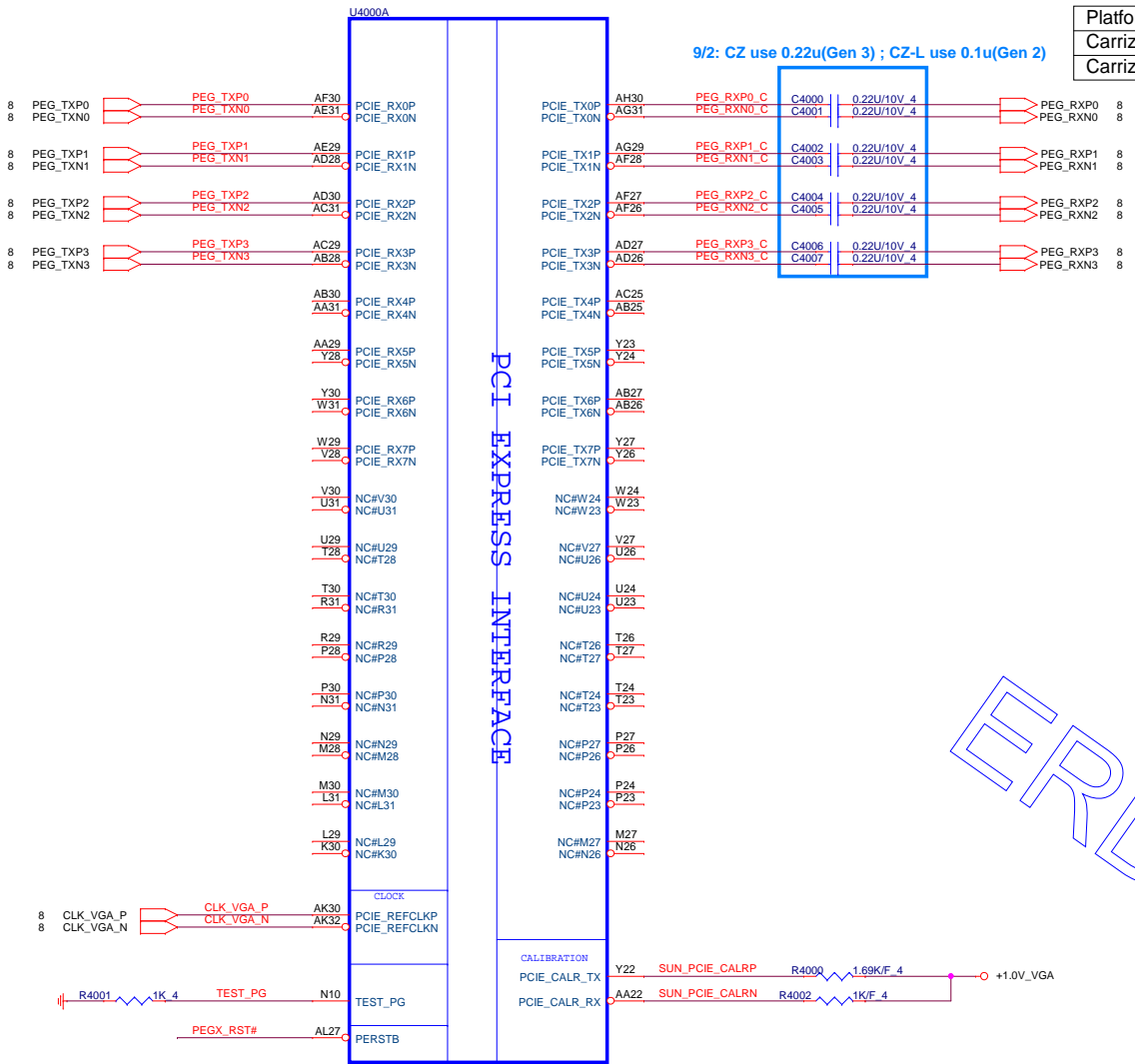


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Quanta Computer Inc.

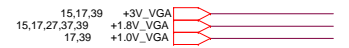
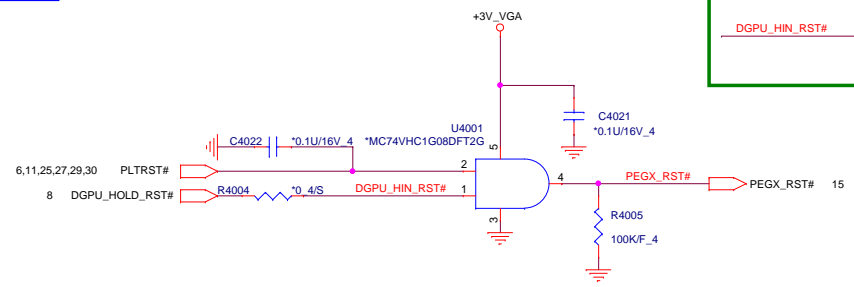
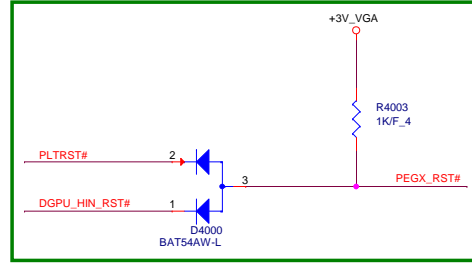
Size Custom	Document Number	Rev 1A
	<b>DDR3 DIMM1-RV5(4.0H)</b>	
Date: Monday, January 05, 2015	Sheet	13 of 40

Platform	Type	P/N
Carrizo_HP	Gen 3	CH4222K9B04_RD
Carrizo-L	Gen 1/Gen 2	CH4102K1B03

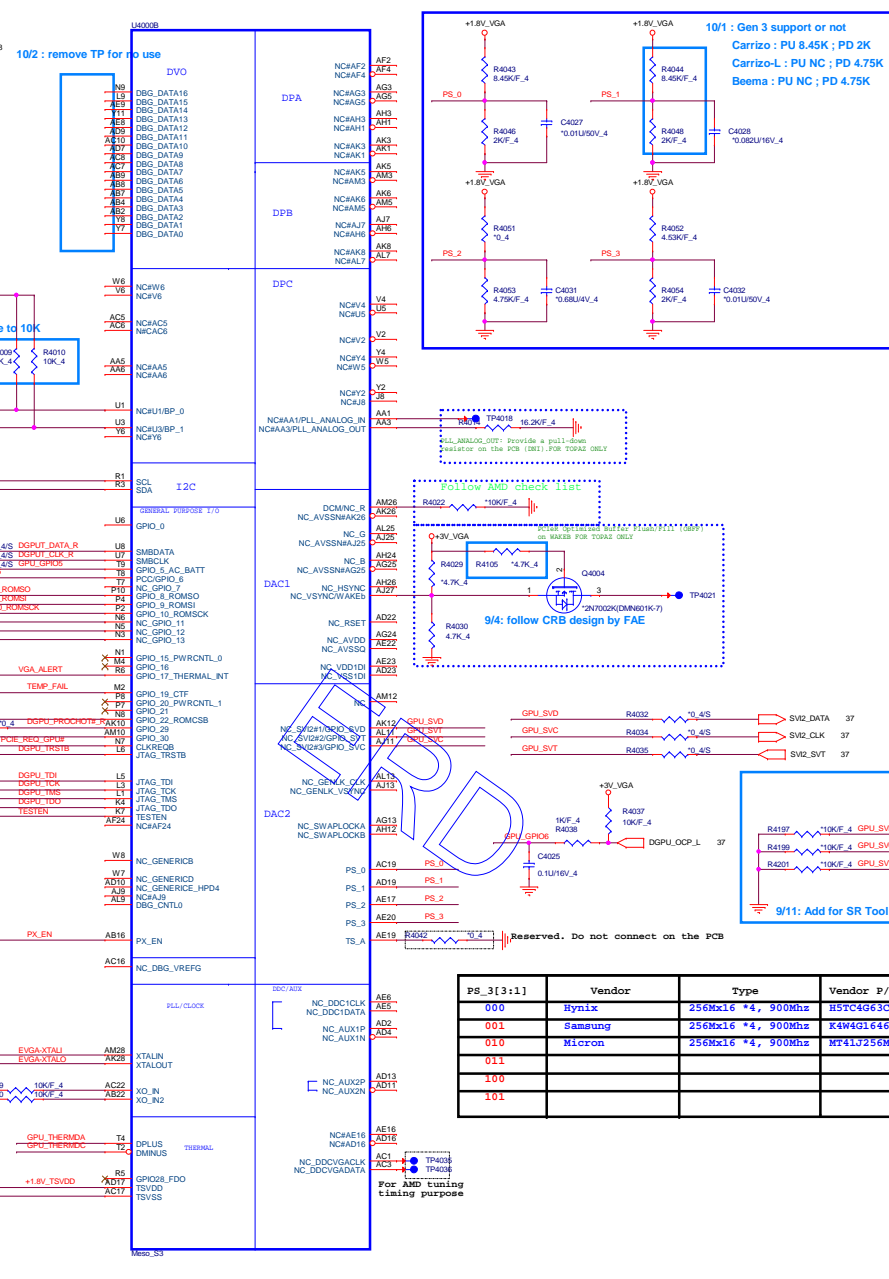
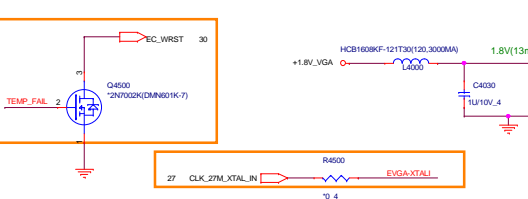
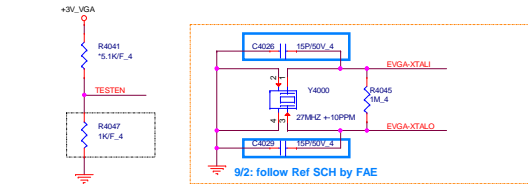
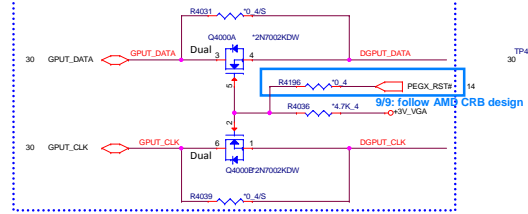
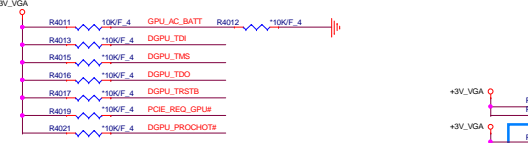
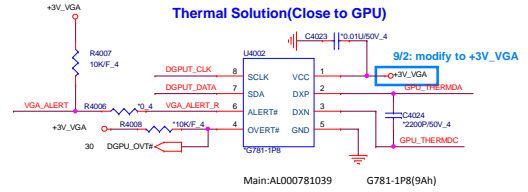
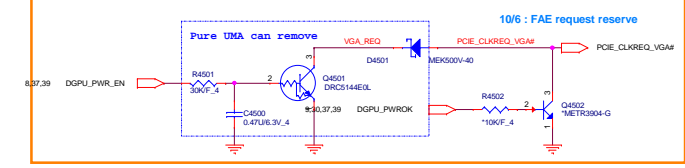
9/2: CZ use 0.22u(Gen 3) ; CZ-L use 0.1u(Gen 2)



12/10:reserve for verify



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	<b>TOPAZ S3 PCIE/DP power</b>		
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**MLPS Implementation**

- Connect GPIO\_28 to 10K pulldown to enable MLPS
- If any of PS\_0/1/2/3 is not used, leave "no connect"
- R\_pu, R\_pd and C must be properly populated per tables below
- Place MLPS circuit components as close to the ASIC as possible
- Total DC resistance of trace between PS pin and C should be less than 2 ohms
- Total DC resistance of trace between C and ground should be less than 2 ohms
- Trace capacitance should be less than 100pF. Resistors should be +/-1% tolerance

C (pF)	BIS(C,4)	R_pu (Ohm)	R_pd (Ohm)	BIS(C,2,1)
680	00	NC	4750	000
82	01	8450	2000	001
10	10	4530	2000	010
NC	11	6980	4990	011
		4530	4990	100
		3240	5620	101
		3400	10000	110
		4750	NC	111

C (pF)	BIS(C,4)	R_pu (Ohm)	R_pd (Ohm)	BIS(C,2,1)
680	00	NC	4750	000
82	01	8450	2000	001
10	10	4530	2000	010
NC	11	6980	4990	011
		4530	4990	100
		3240	5620	101
		3400	10000	110
		4750	NC	111

**MLPS Bit**

MLPS Bit	Strap Name	Description	Recommended Settings
PS_011	ROM_CONFIG[0]	If STRAP_BIOS_ROM_EN = 1, ROM_CONFIG[0] defines the ROM type.	Design dependent, see the description.
PS_012	ROM_CONFIG[1]	If STRAP_BIOS_ROM_EN = 0, ROM_CONFIG[1] defines the primary memory aperture size, see Primary Memory Aperture Size (p. 29)	Design dependent, see the description.
PS_013	ROM_CONFIG[2]		Design dependent, see the description.
PS_014	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_015	N/A	Reserved.	1
PS_111	STRAP_BIF_GEN3_EN_A	PCIe GEN3 capability. 1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported.	Design dependent, see the description.
PS_112	STRAP_BIF_CLK_PM_EN	Defines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQ#).	0
PS_113	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_114	STRAP_TX_CFG_DRV_FULL_SWING	Control the transmitter full-half swing mode. 0 = The transmitter full-half swing is enabled. 1 = The transmitter full-half swing is disabled.	1
PS_115	STRAP_TX_DEEMPH_EN	PCI EXPRESS transmitter, deemphasis enable. 0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled.	Design dependent, see the description.
PS_211	N/A	Reserved.	0
PS_212	N/A	Reserved.	0
PS_213	STRAP_BIOS_ROM_EN	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	Design dependent, see the description.
PS_214	N/A	Reserved.	1
PS_215	N/A	Reserved.	1
PS_311	BOARD_CONFIG[0]	Board configuration related strapings, such as for memory ID device.	Design dependent, see the description.
PS_312	BOARD_CONFIG[1]		Design dependent, see the description.
PS_313	BOARD_CONFIG[2]		Design dependent, see the description.
PS_314	N/A	Reserved.	1
PS_315	N/A	Reserved.	1

**BITS => BIT0**

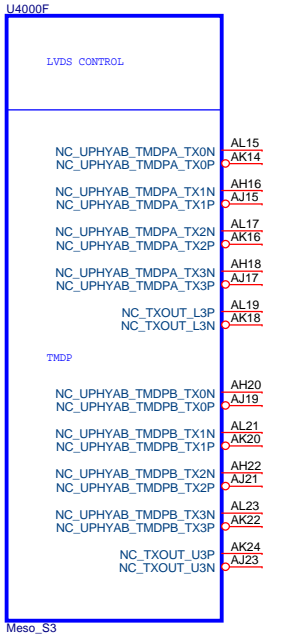
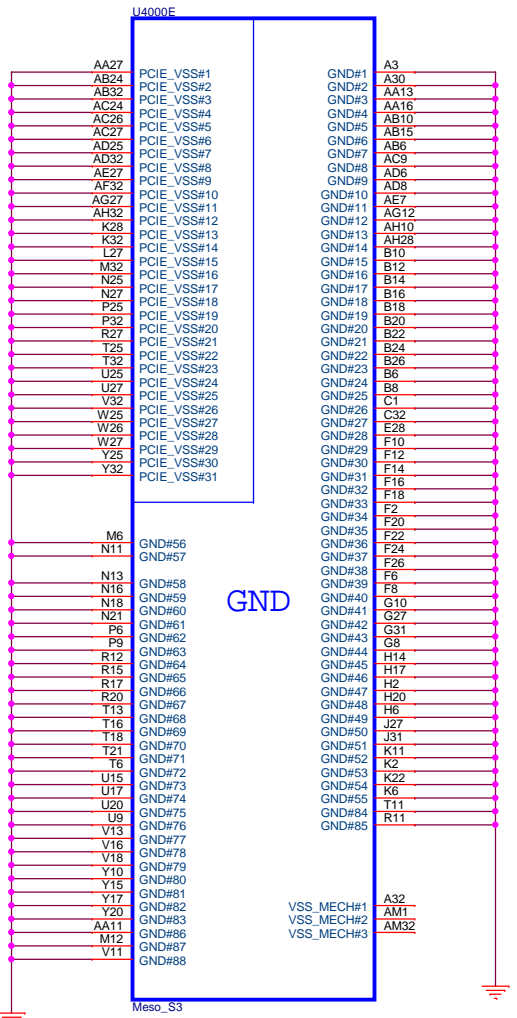
PS0 => 11001  
 PS1 => 11000  
 PS2 => 11000  
 PS3 => 11000

PS_3[3:1]	Vendor	Type	Vendor P/N	PU	PD
000	Hynix	256Mx16 *4, 900Mhz	H5TC4G63CFR-N0C	NC	4.75K
001	Samsung	256Mx16 *4, 900Mhz	K4W4G1646E-BC1A	8.45K	2K
010	Micron	256Mx16 *4, 900Mhz	MT41J256M16HA-093G:E	4.53K	2K
011					
100					
101					

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### CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS  
0= DO NOT INSTALL RESISTOR  
1= INSTALL 3K RESISTOR  
X = DESIGN DEPENDANT  
NA = NOT APPLICABLE

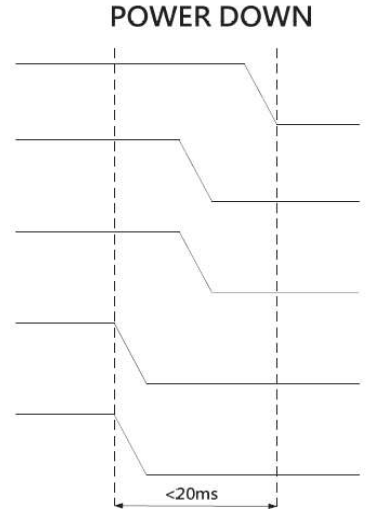
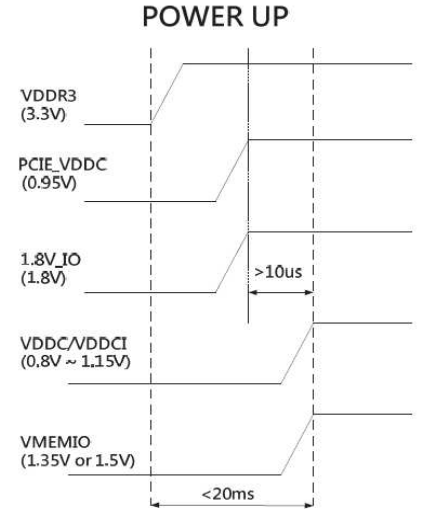
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/W/histler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSYN	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

### NOTE1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21 H2SYNC GENERICC GPIO8 GPIO2

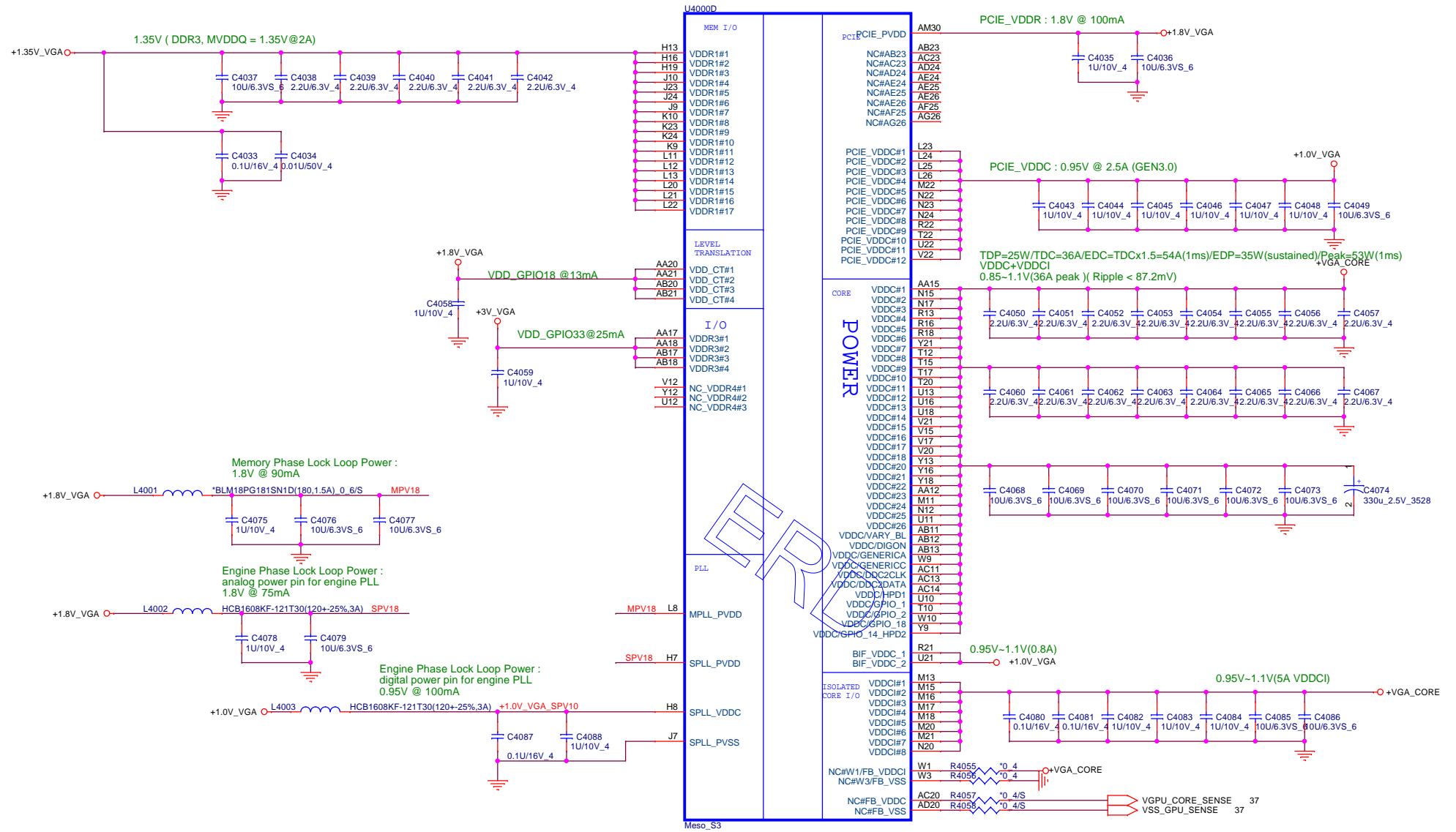
### POWER UP / POWER DOWN SEQUENCE



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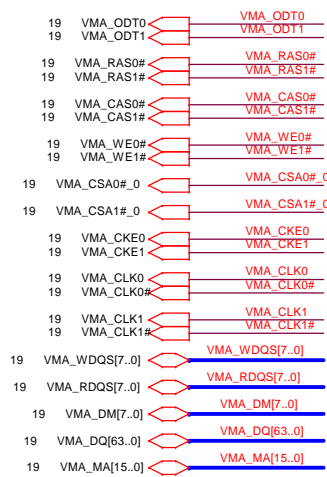
Size	Document Number	Rev
	<b>TOPAZ_S3_GND/LVDS/Strap</b>	<b>1A</b>
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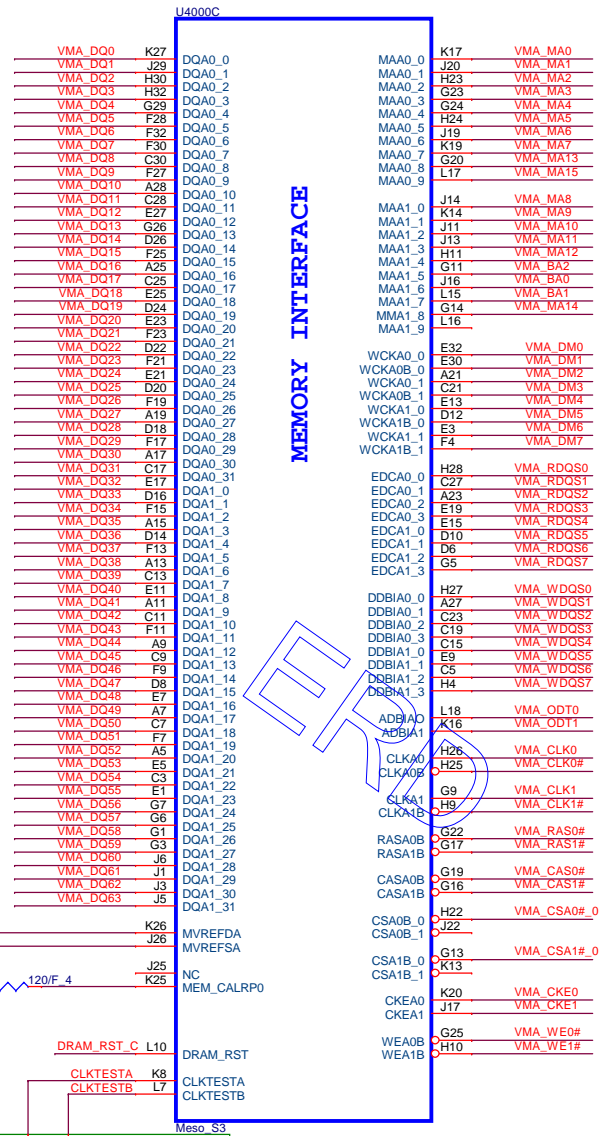


- +1.35V\_VGA 18,19,37
- +1.8V\_VGA 14,15,27,37,39
- +1.0V\_VGA 14,39
- +VGA\_CORE 37,38

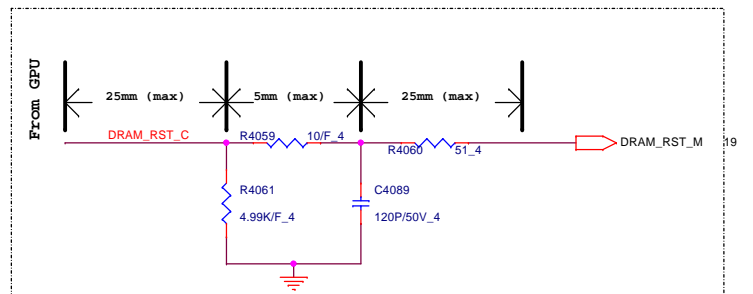
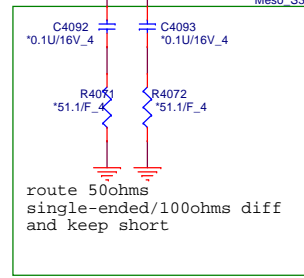
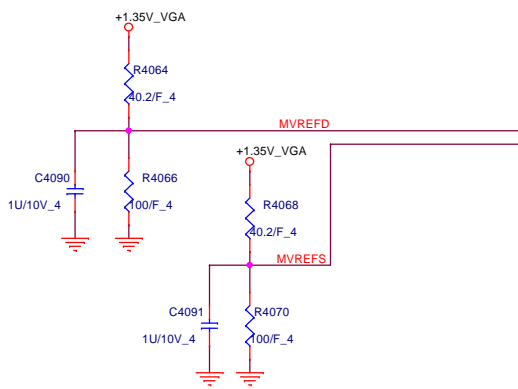
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	Quanta Computer Inc.	
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	<b>TOPAZ S3 Power</b>	<b>1A</b>
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support 1Gbit  
VRAM ( 64M X 16 )



MEMORY INTERFACE

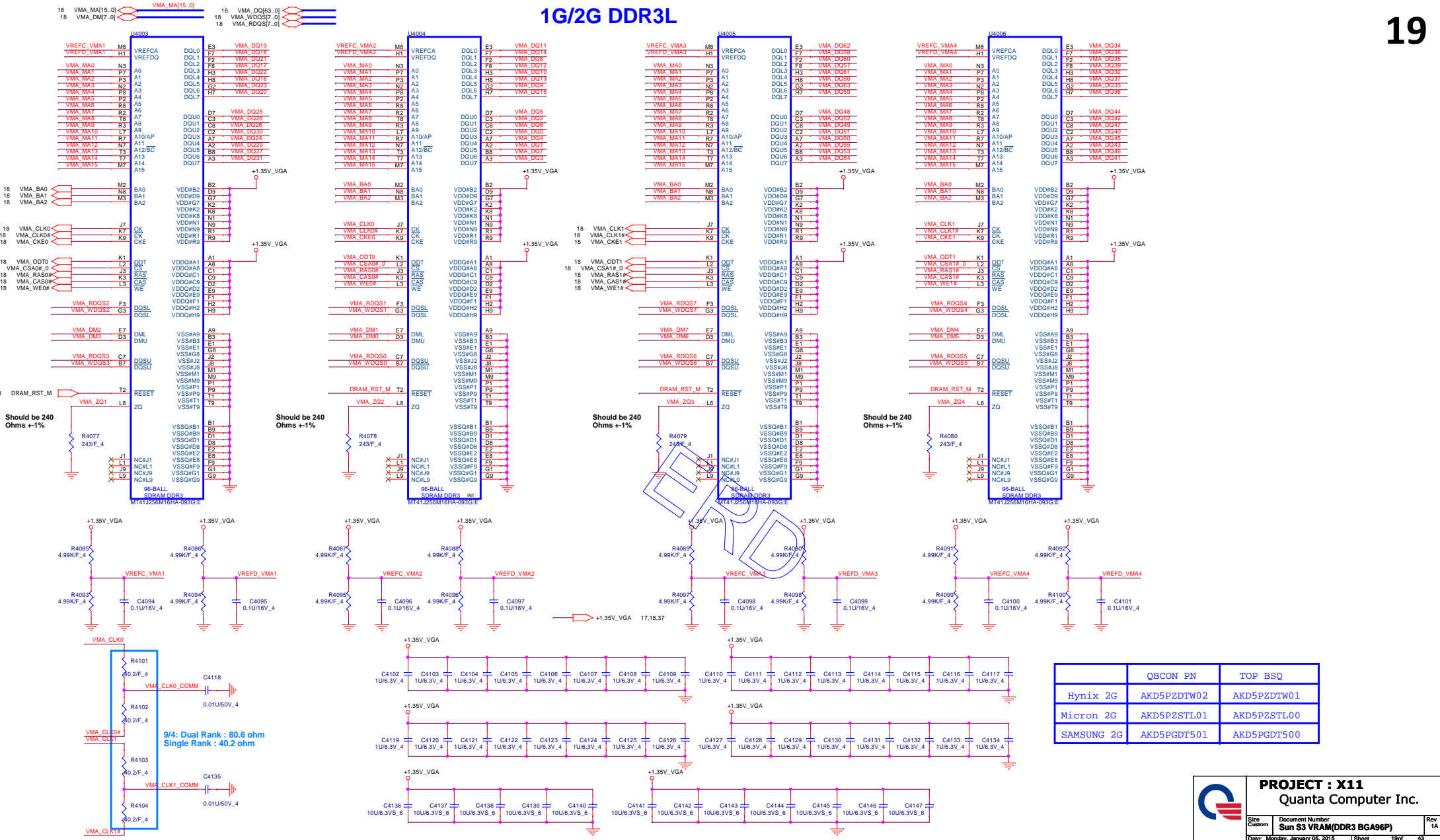


Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

This basic topology should be used for DRAM\_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

		<b>PROJECT : X11</b>	
		Quanta Computer Inc.	
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	<b>TPOAZ_S3_MEM_Interface</b>	<b>1A</b>	
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1G/2G DDR3L




	QBCON PN	TOP BSQ
Hynix 2G	AKD5PZDTW02	AKD5PZDTW01
Micron 2G	AKD5PZSTL01	AKD5PZSTL00
SAMSUNG 2G	AKD5PGDT501	AKD5PGDT500


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**Quanta Computer Inc.**

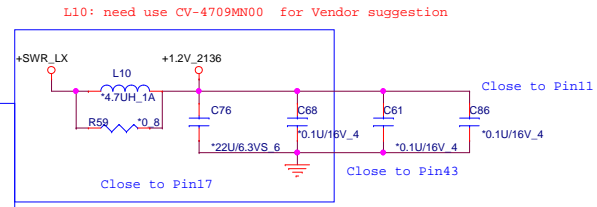
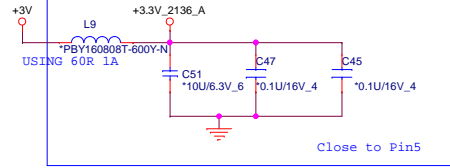
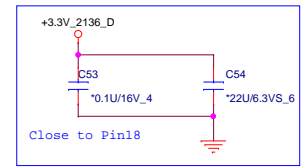
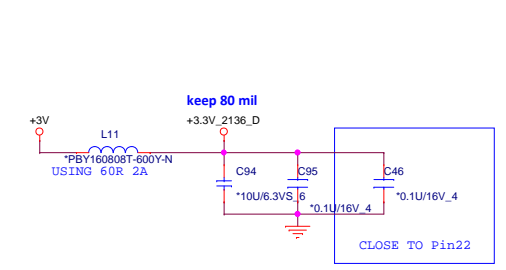
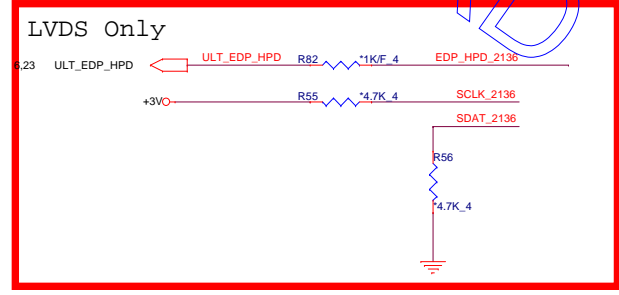
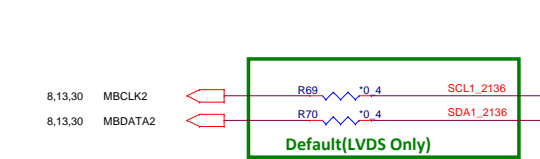
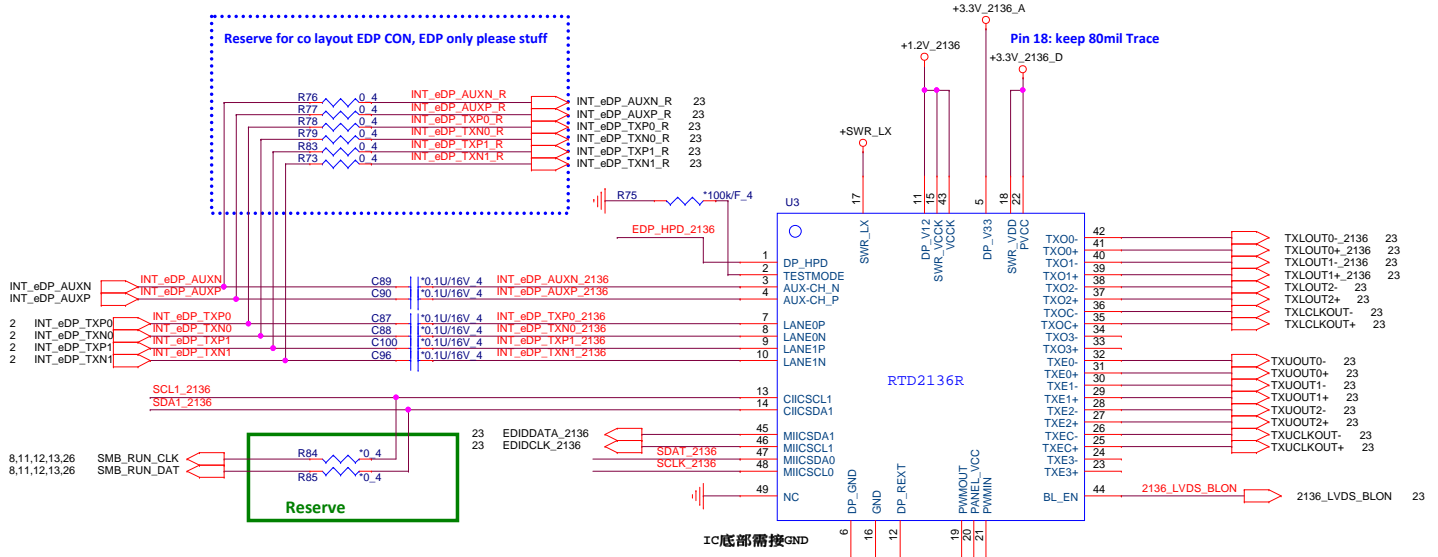
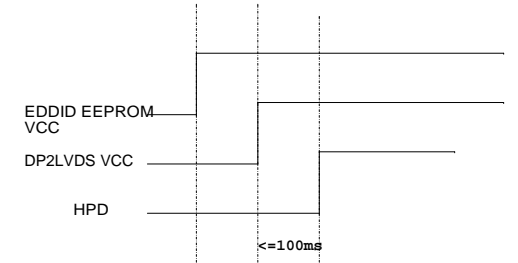
Size Custom	Document Number Sun S3 VRAM(DDR3 BGA96P)	Rev 1A
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	<b>PROJECT : X11</b>	
	Quanta Computer Inc.	
	Size Custom	Document Number <b>Sun S3 VRAM(DDR3 BGA96P)</b>
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	<b>PROJECT : X11</b>	
	Quanta Computer Inc.	
	Size Custom	Document Number <b>Sun S3 VRAM(DDR3 BGA96P)</b>
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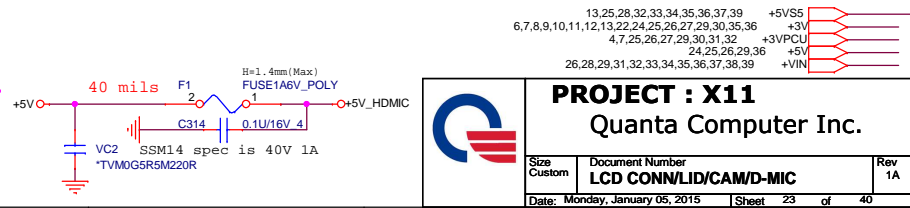
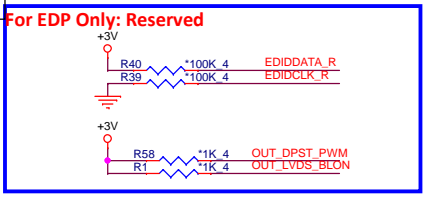
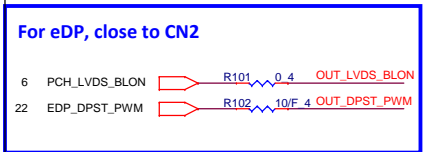
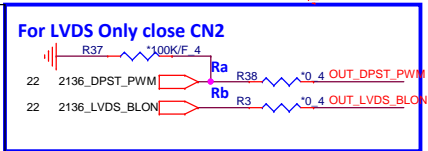
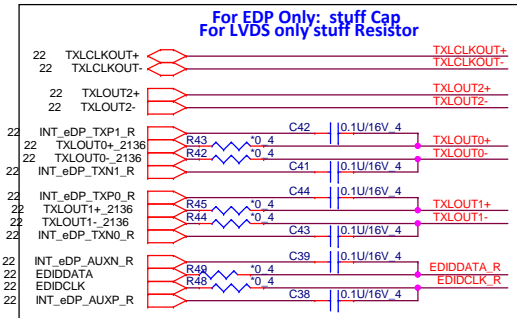
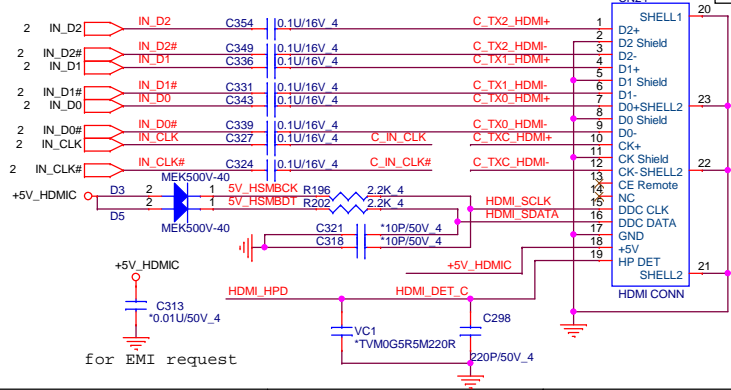
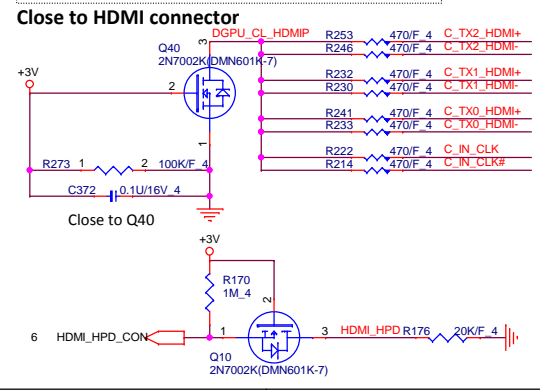
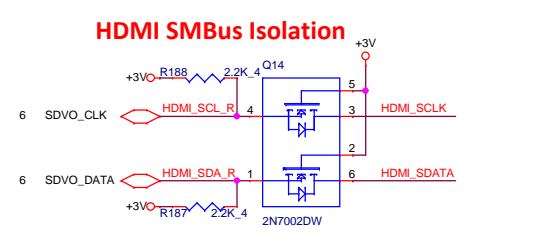
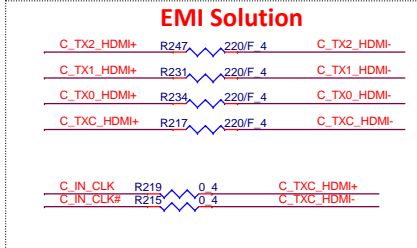
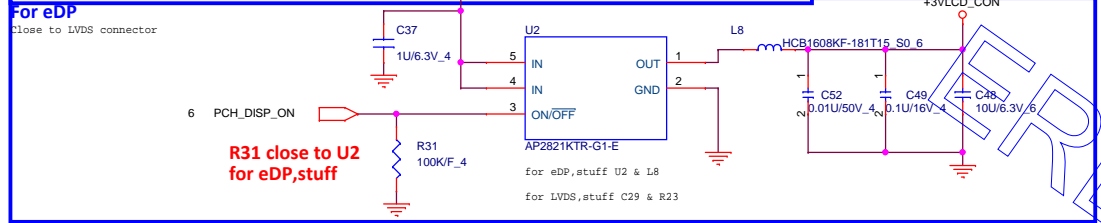
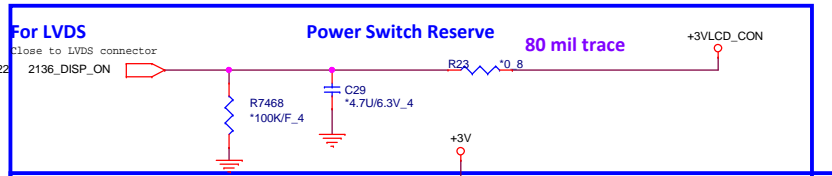
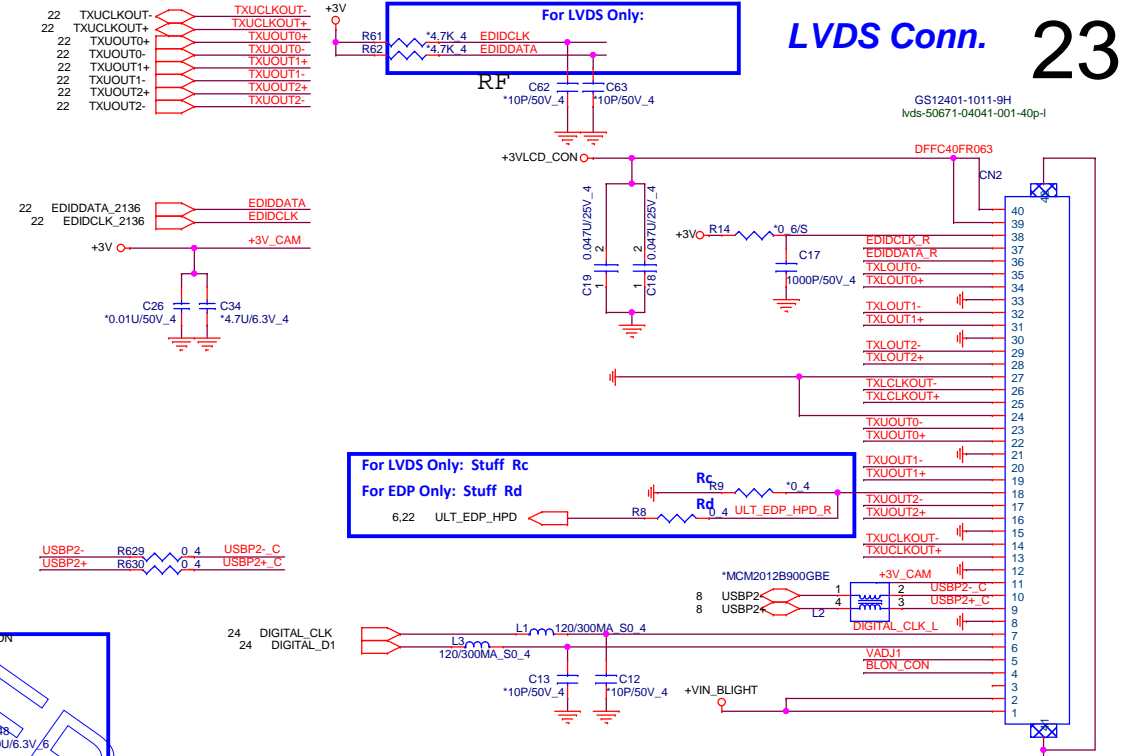
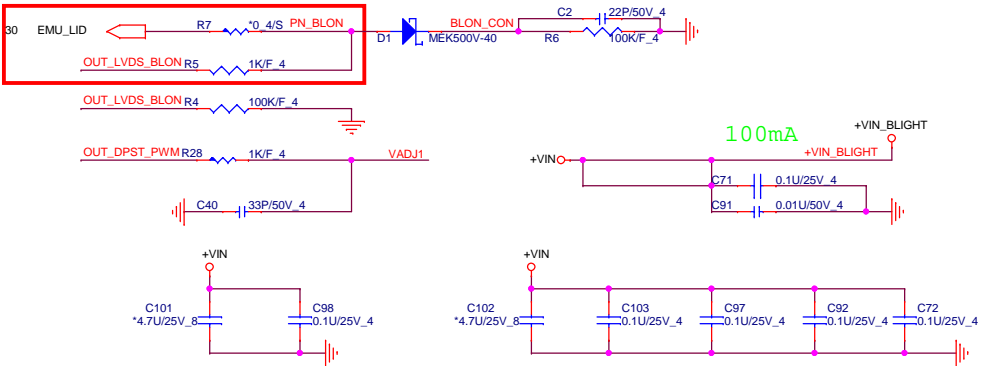


SWR MODE	LDO MODE
Stuff L10	Stuff R59

**PROJECT : X11**  
**Quanta Computer Inc.**

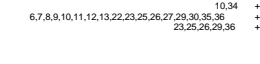
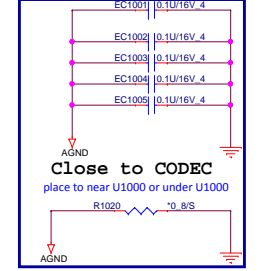
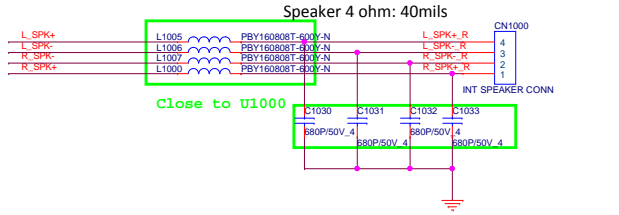
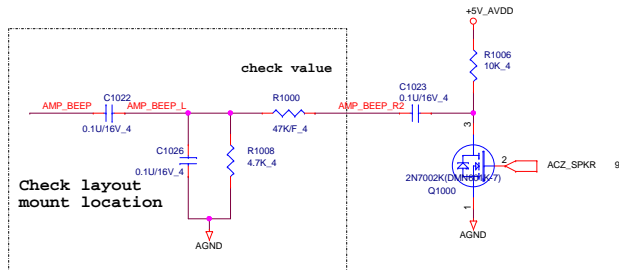
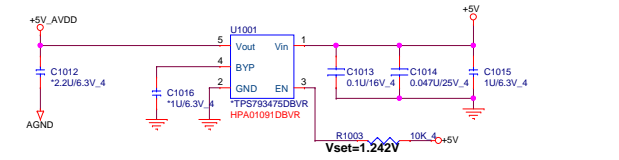
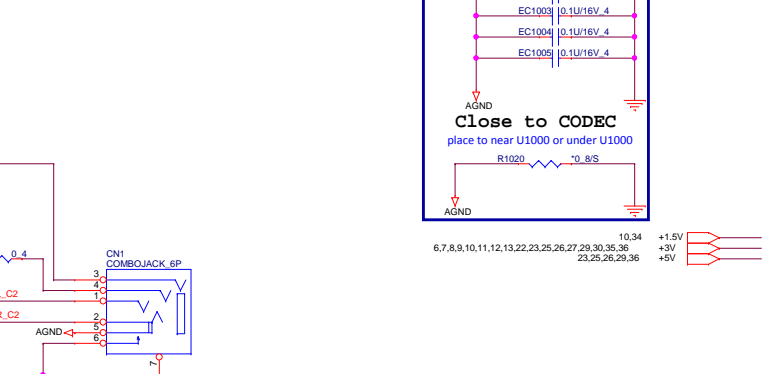
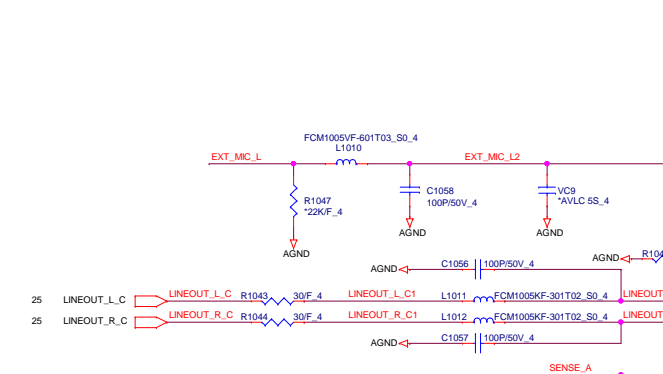
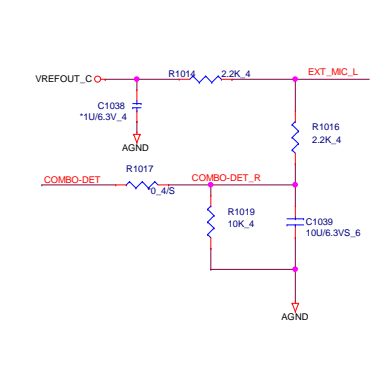
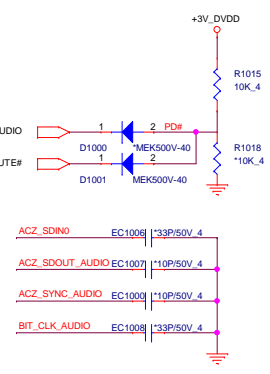
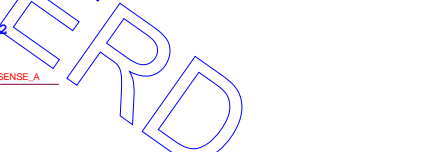
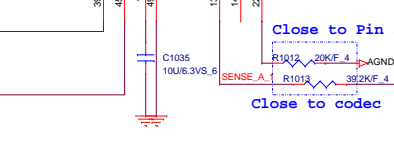
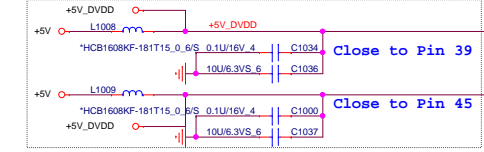
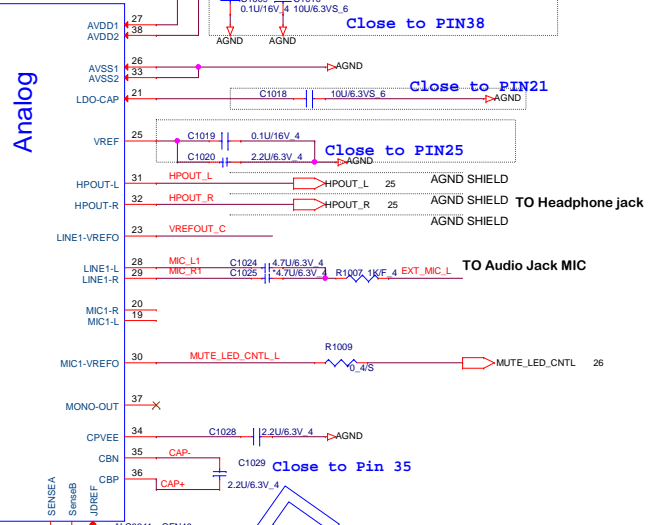
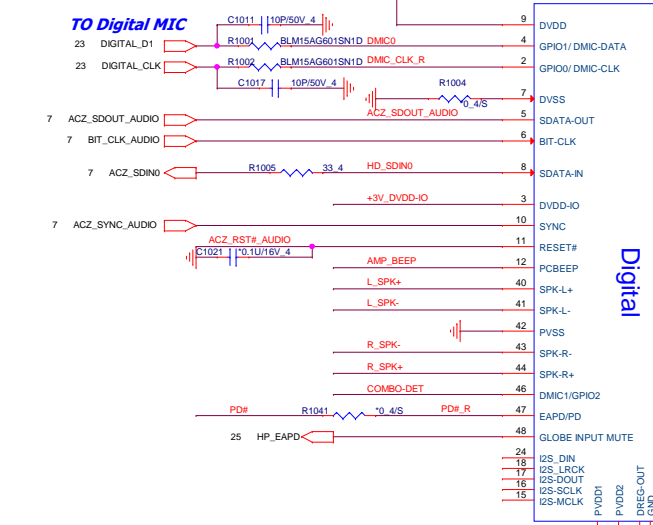
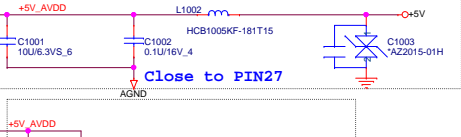
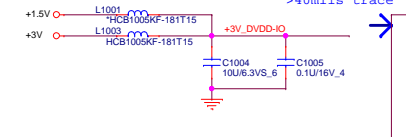
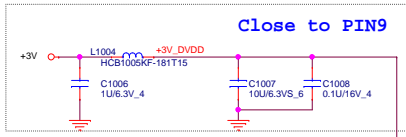
Size Custom	Document Number <b>RTD2136</b>	Rev 1A
Date: Monday, January 05, 2015	Sheet 22 of 40	

# LID Switch

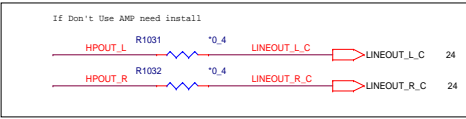
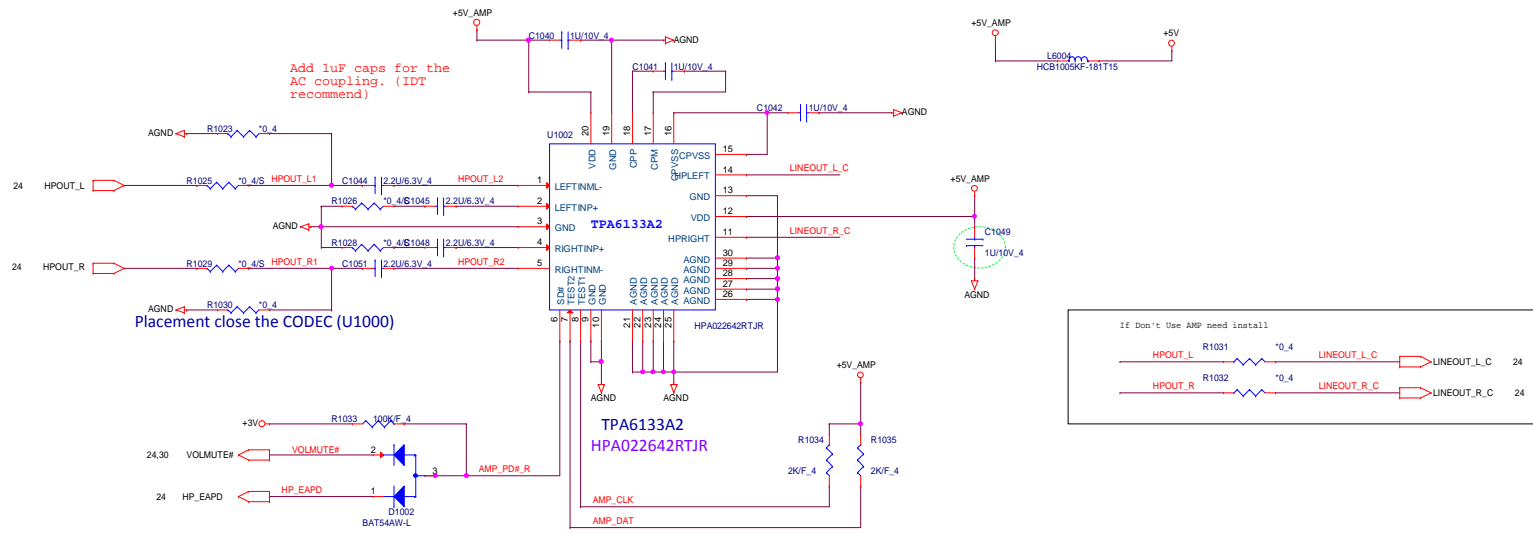


**PROJECT : X11**  
Quanta Computer Inc.

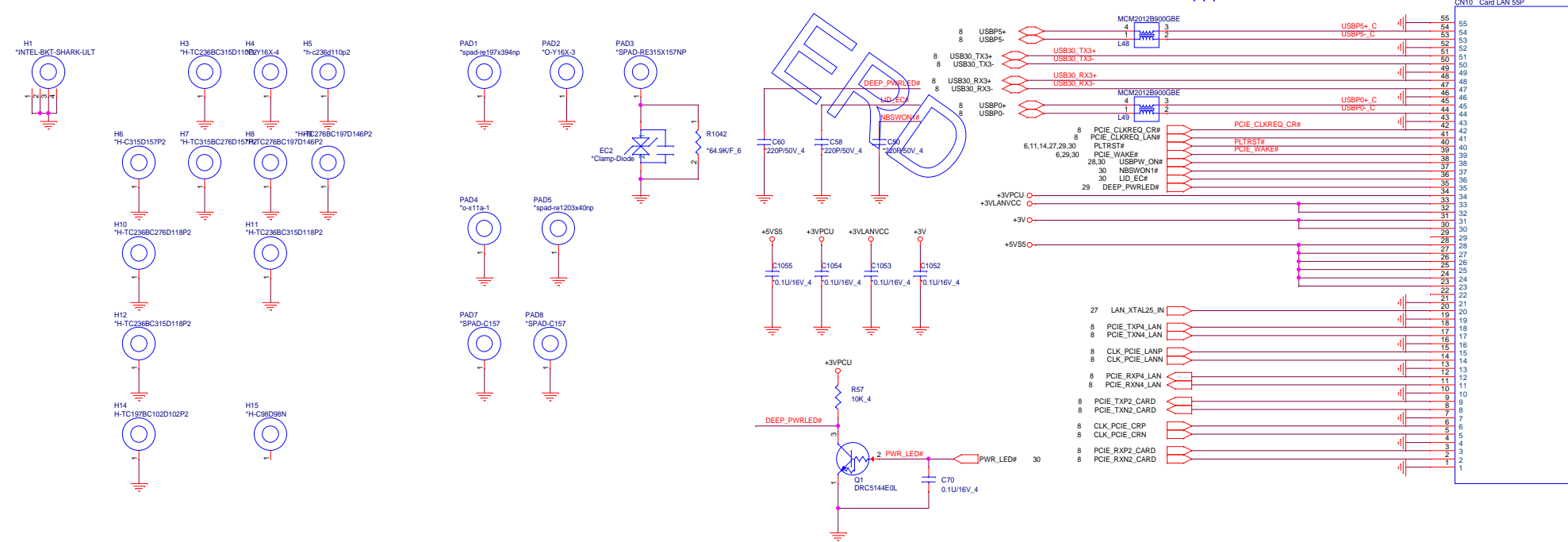
Size Custom	Document Number LCD CONN/LID/CAM/D-MIC	Rev 1A
Date: Monday, January 05, 2015		Sheet 23 of 40



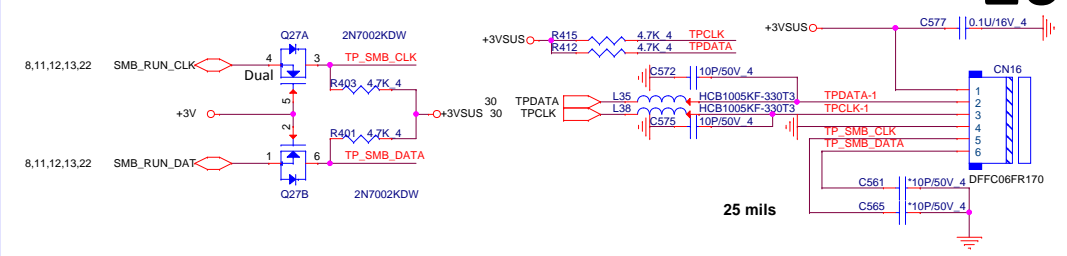




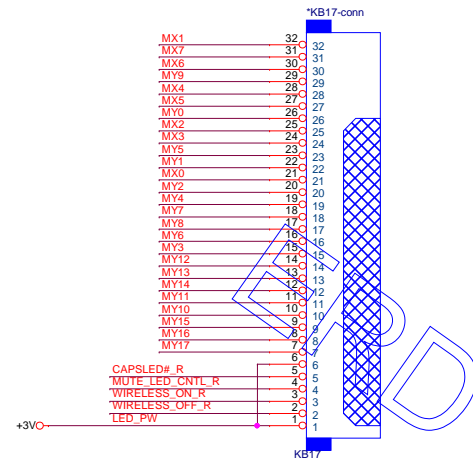
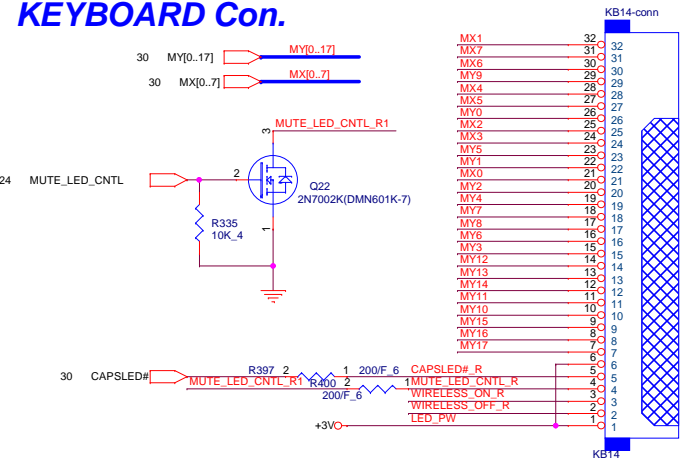
HOLE



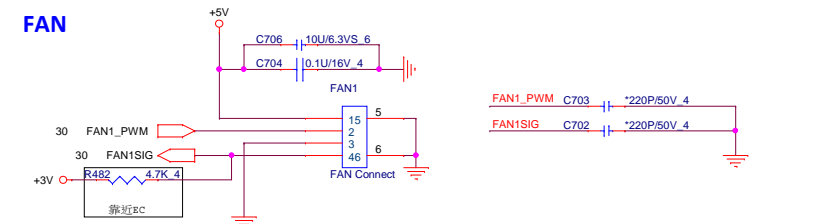
Touch Pad Connector



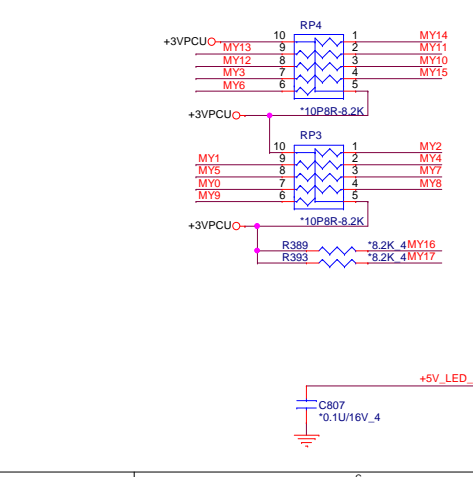
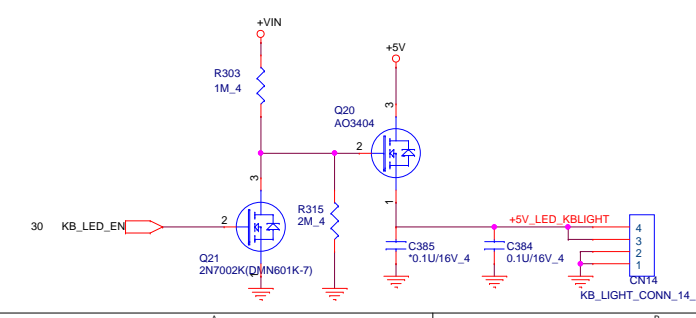
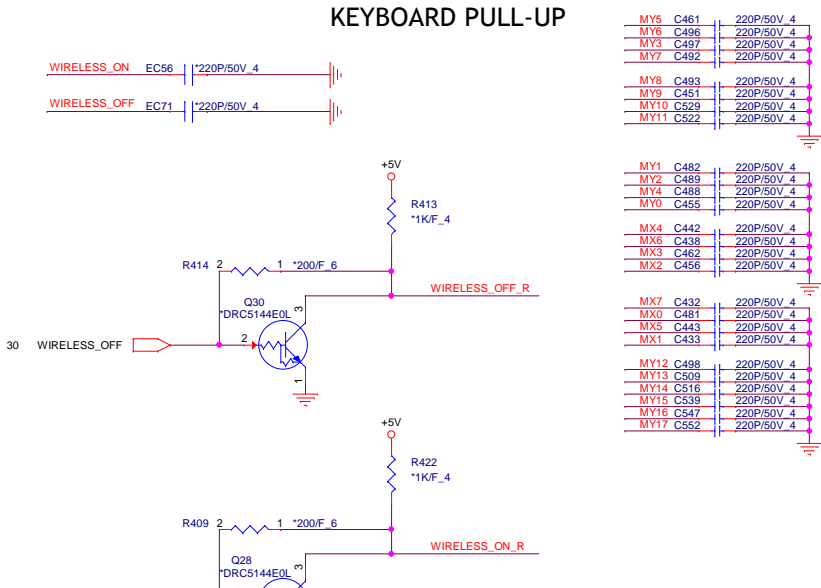
KEYBOARD Con.



FAN



KEYBOARD PULL-UP



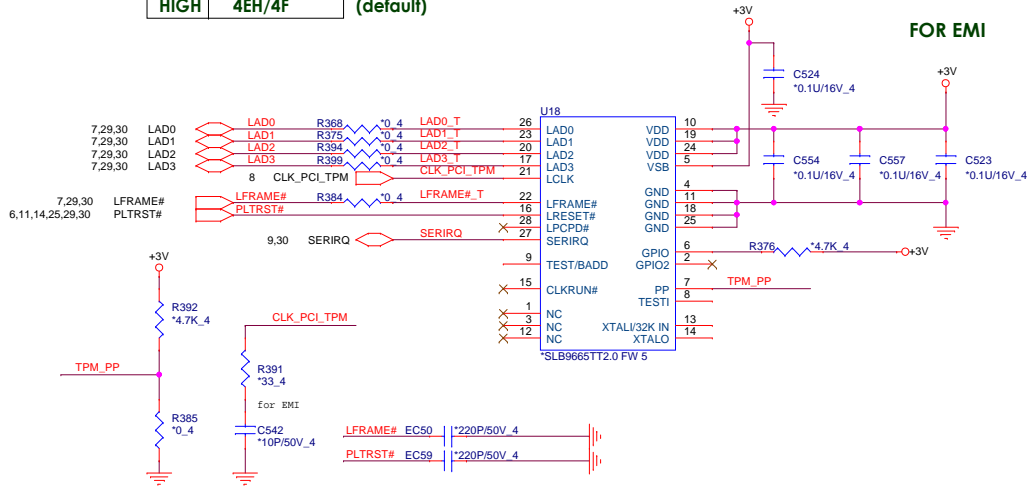
**PROJECT : X11**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	PB/TP/KB/FAN/EMI Cap	1A
Date: Monday, January 05, 2015	Sheet 26 of 40	

TPM (2.0)

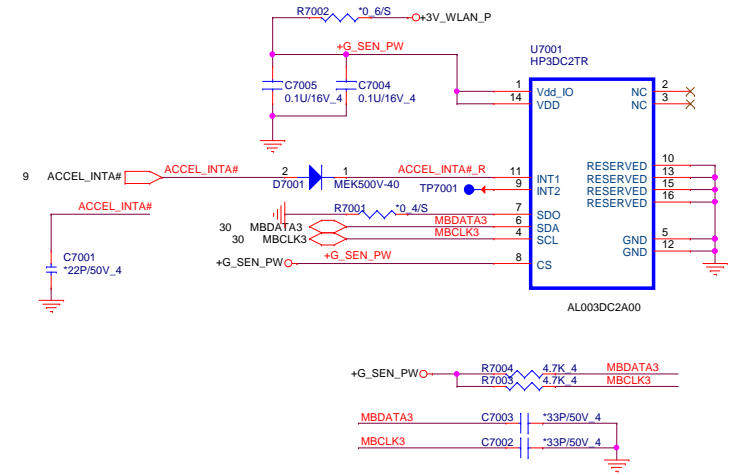
Address

	BADD	
HIGH	4EH/4F	(default)

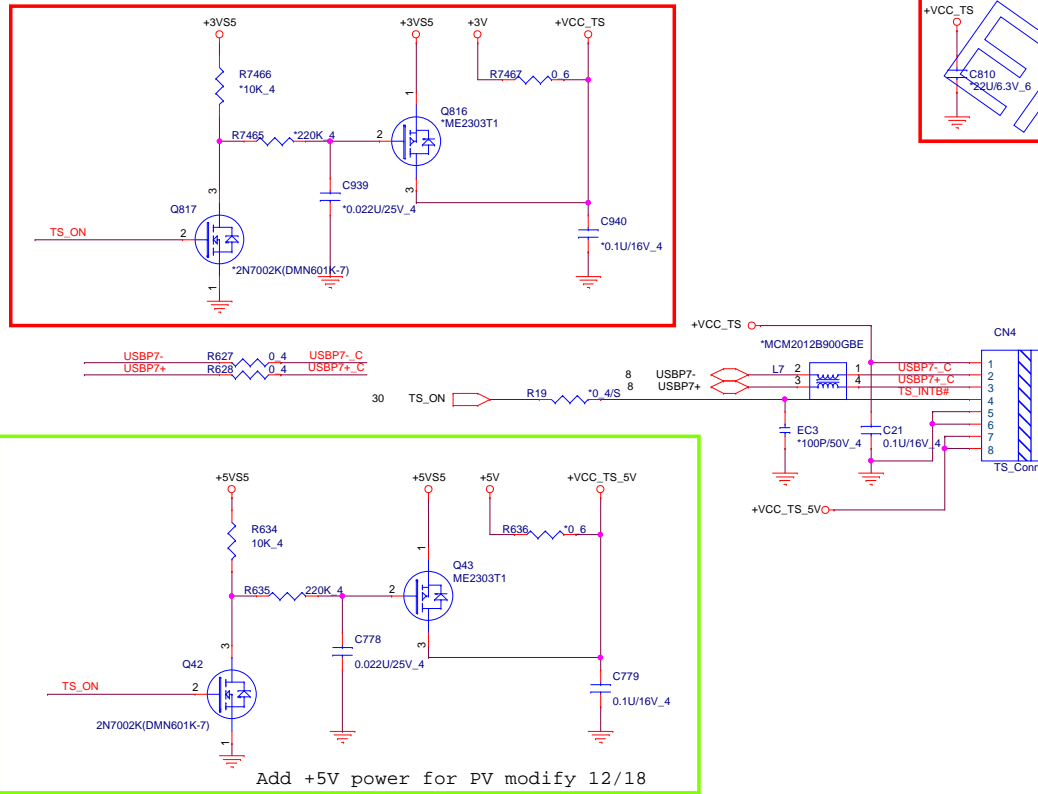


Accelerometer Sensor

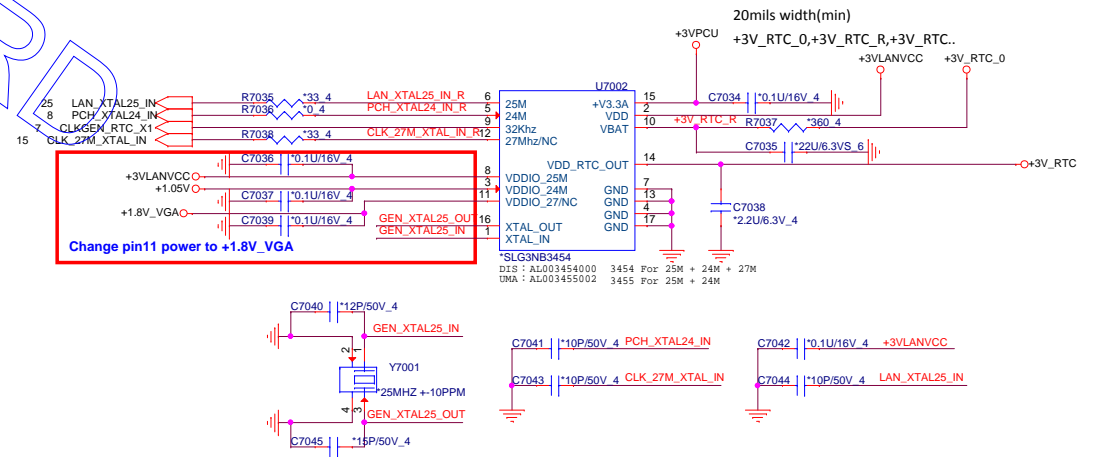
G-Sensor Power need check



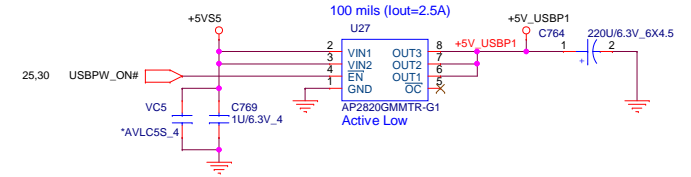
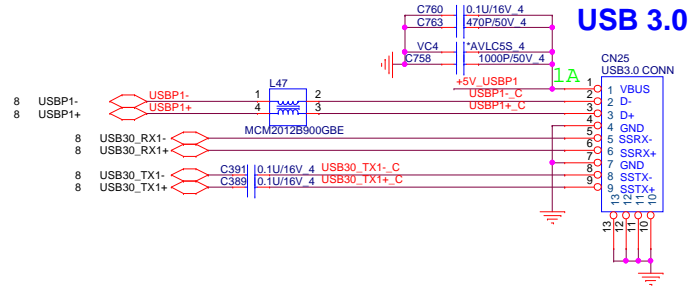
Touch screen



Green CLK Circuitry

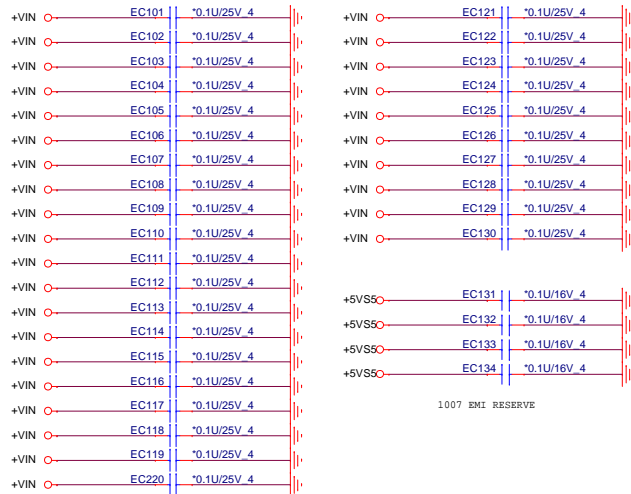



			<b>PROJECT : X11</b>	
			Quanta Computer Inc.	
Size	Document Number	Rev		
Custom	TPM/G-Sensor/G-CLK/TS/FP	1A		
Date:	Monday, January 05, 2015	Sheet	27 of	40



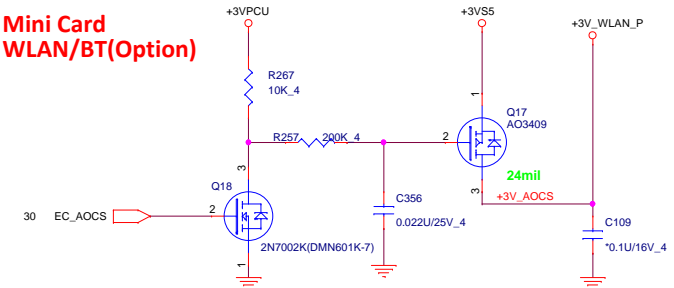
ERD

# EMI CAP

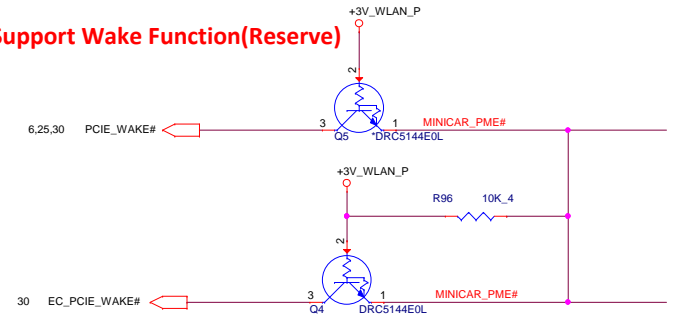


	<b>PROJECT : X11</b> Quanta Computer Inc.	
	Size Custom	Document Number <b>USB 3.0</b>
Date: Monday, January 05, 2015		Sheet 28 of 40

**Mini Card WLAN/BT(Optional)**

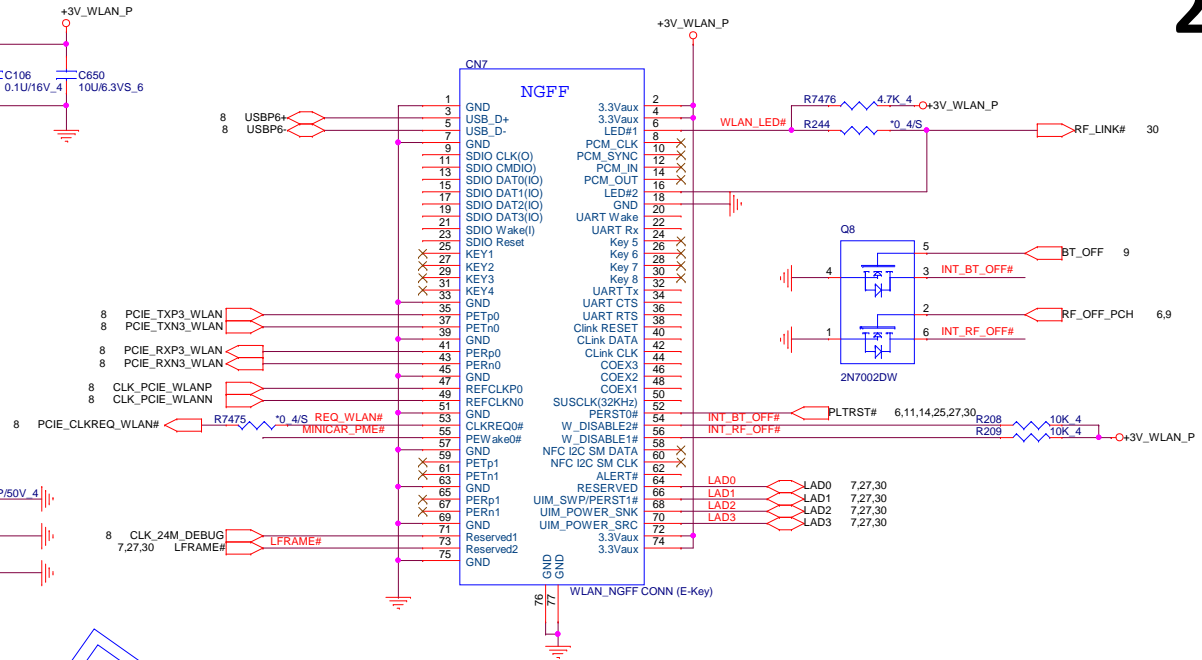


**Support Wake Function(Reserve)**

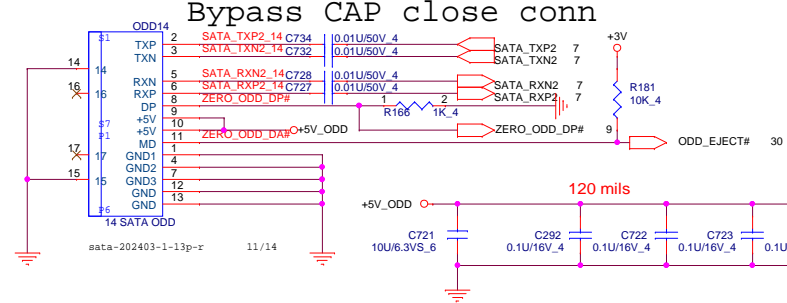


**For EMI Suggestion**

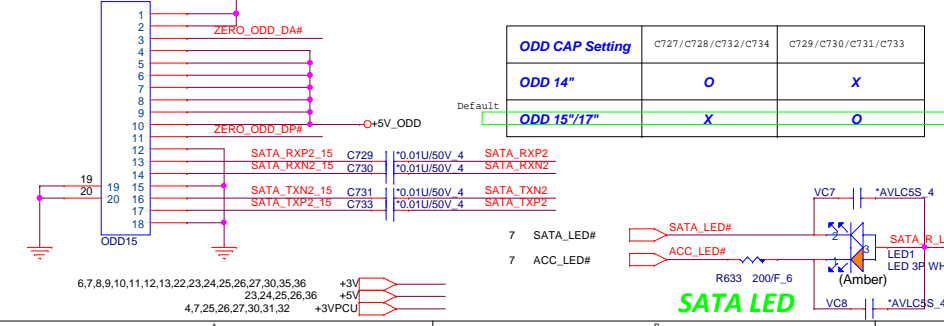
- CLK\_24M\_DEBUG EC10 || \*33P/50V\_4
- PCIE\_WAKE# EC12 || \*220P/50V\_4
- EC\_PCIE\_WAKE# EC13 || \*220P/50V\_4



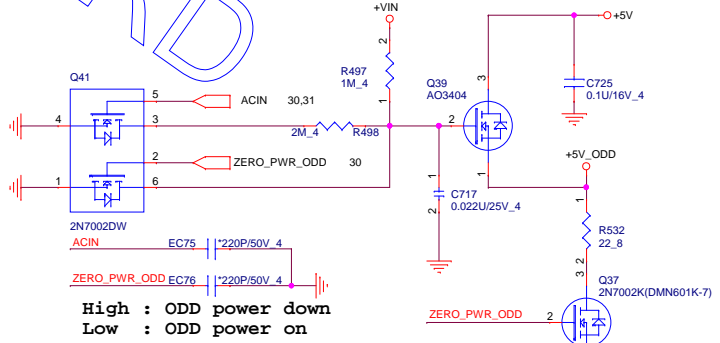
**14" SATA ODD**



**15" SATA ODD**

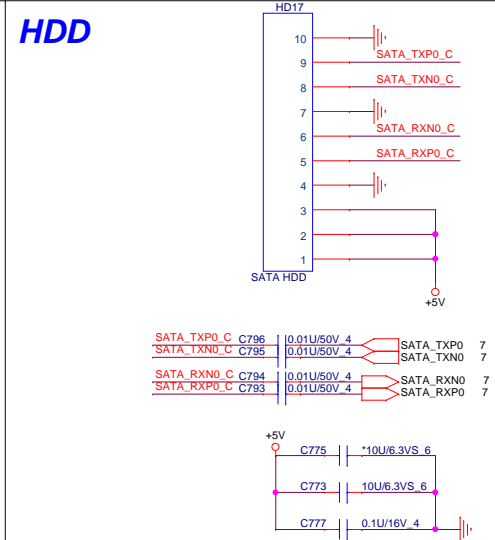


ERD

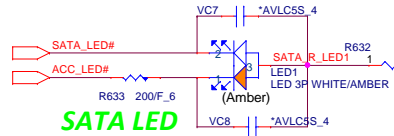


**High : ODD power down**  
**Low : ODD power on**

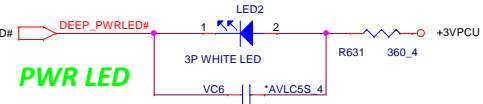
**HDD**



**SATA LED**

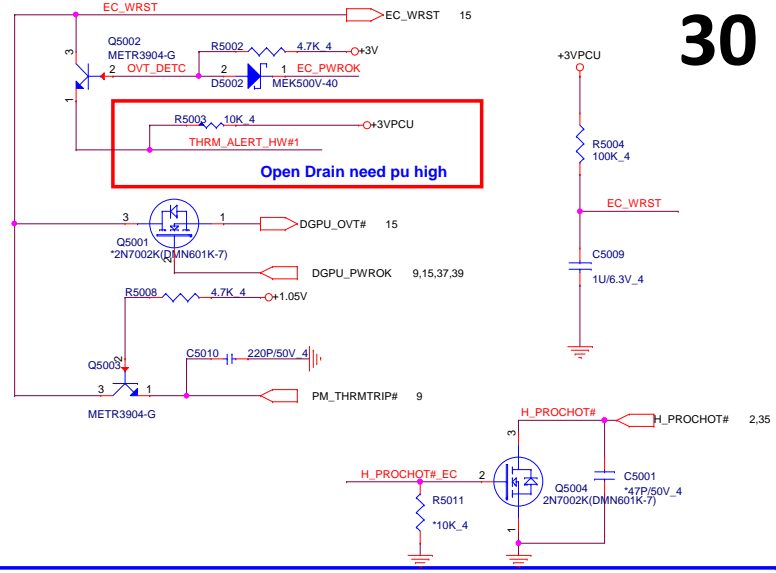
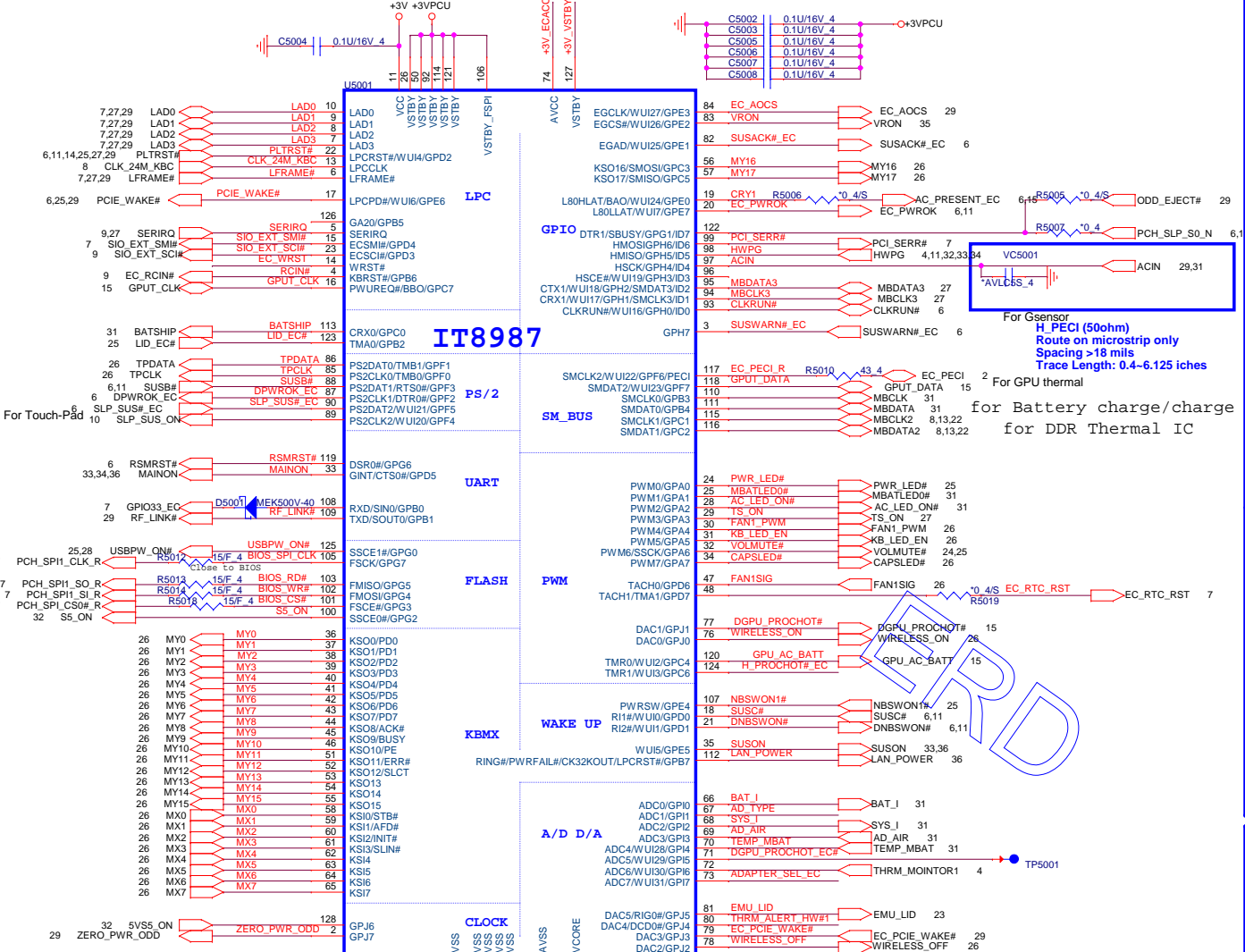


**PWR LED**



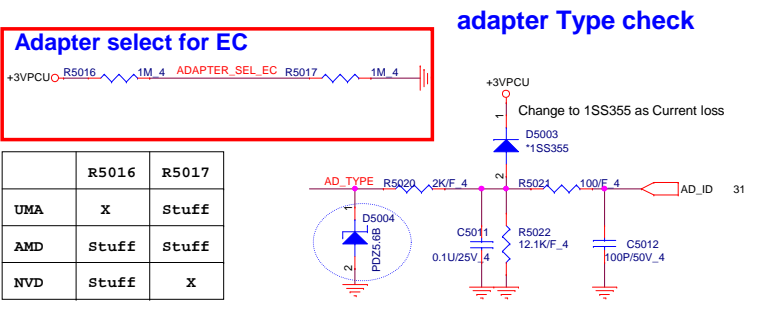
**PROJECT : X11**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	<b>WLAN/NGFF/MSATA</b>	1A
Date: Monday, January 05, 2015		Sheet 29 of 40

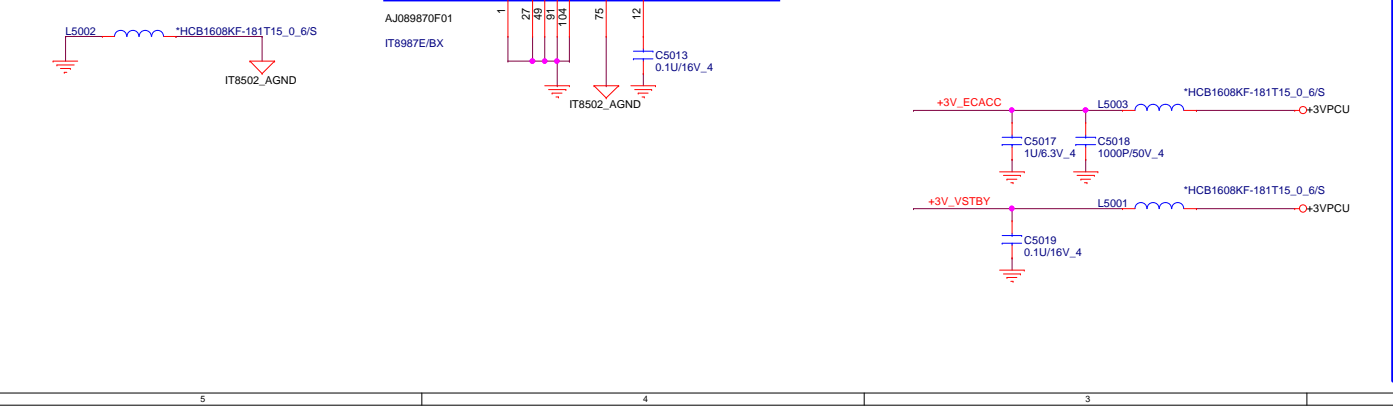
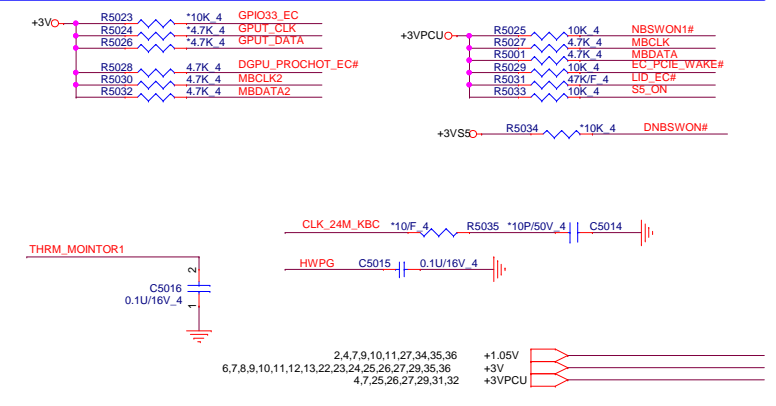


For Gsensor  
H\_PECI (50ohm)  
Route on microstrip only  
Spacing > 18 mils  
Trace Length: 0.4-6.125 inches

For GPU thermal  
for Battery charge/charge  
for DDR Thermal IC



	R5016	R5017
UMA	X	Stuff
AMD	Stuff	Stuff
NVD	Stuff	X

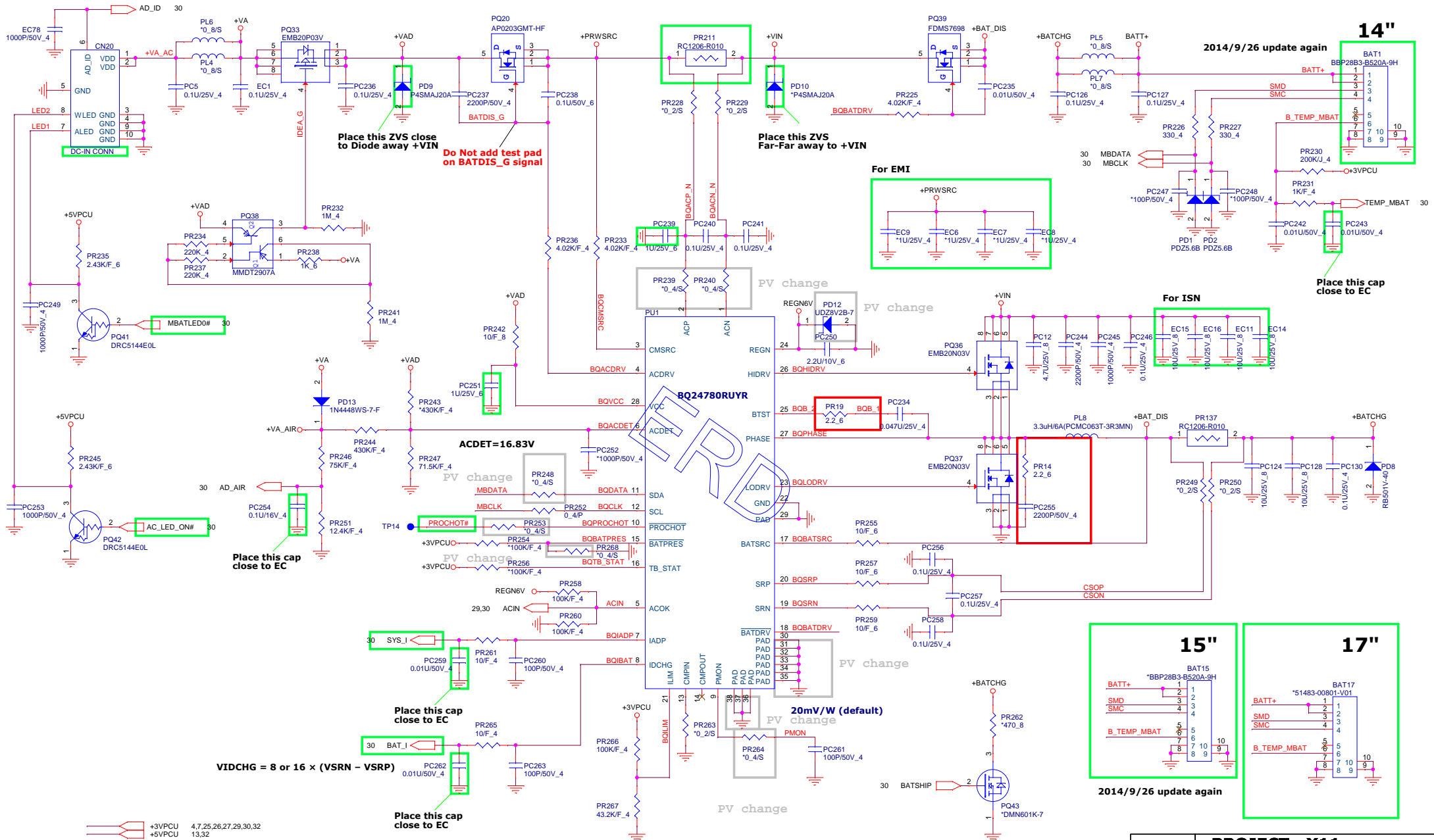


**PROJECT : X11**

**Quanta Computer Inc.**

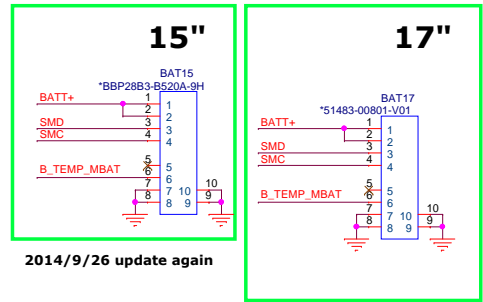
Size	Custom	Document Number	WLAN/G-Sensor/G-CLK/TS	Rev	1A
Date:	Tuesday, January 06, 2015	Sheet	30 of		40

90W DC\_JACK



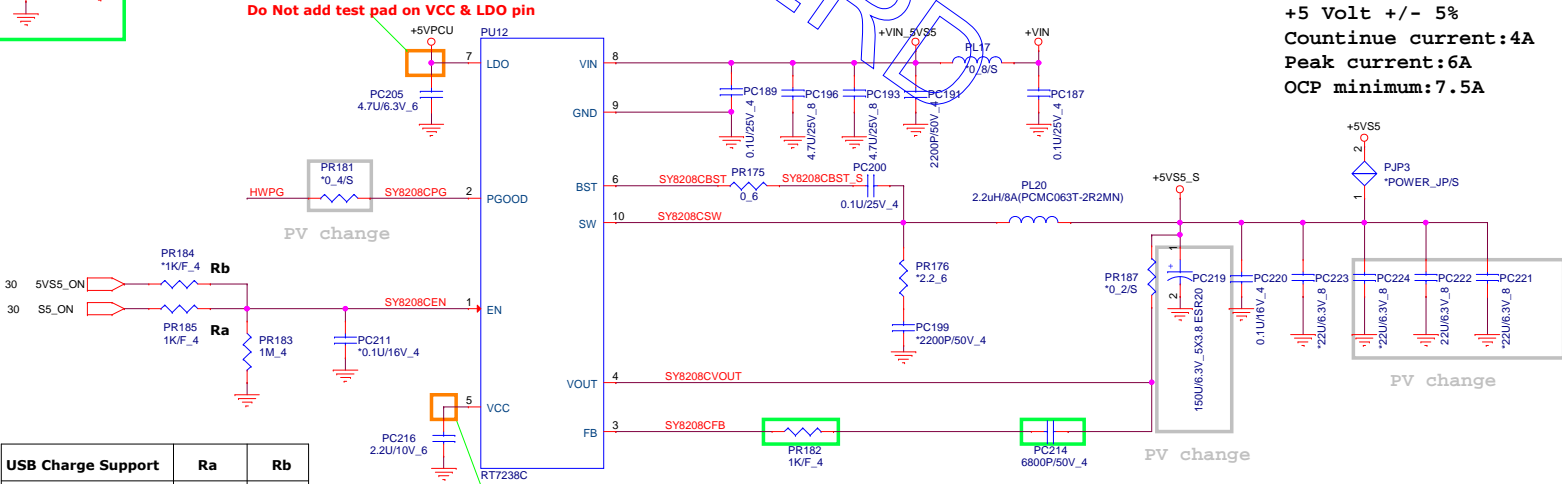
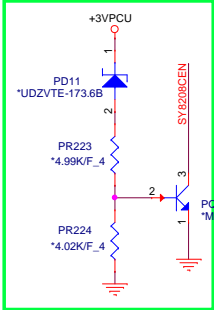
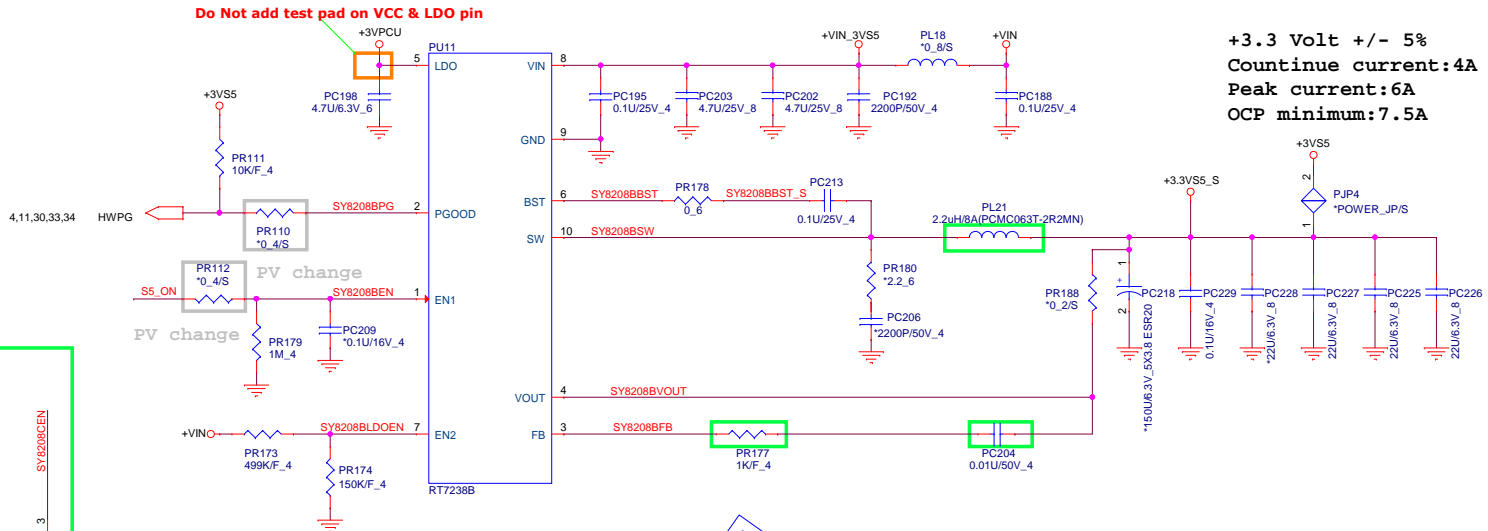
VIDCHG = 8 or 16 x (VSRN - VSRP)

+3VPCU 4.7,25,26,27,29,30,32  
 +5VPCU 13,32



			<b>PROJECT : X11</b>		
			Quanta Computer Inc.		
Size Custom	Document Number	Charger (BQ24780)		Rev 1A	
Date: Monday, January 05, 2015   Sheet 31 of 40					

+3VS5 6,9,10,11,27,29,30,34,36,37,39  
 +5VS5 13,25,28,33,34,35,36,37,39



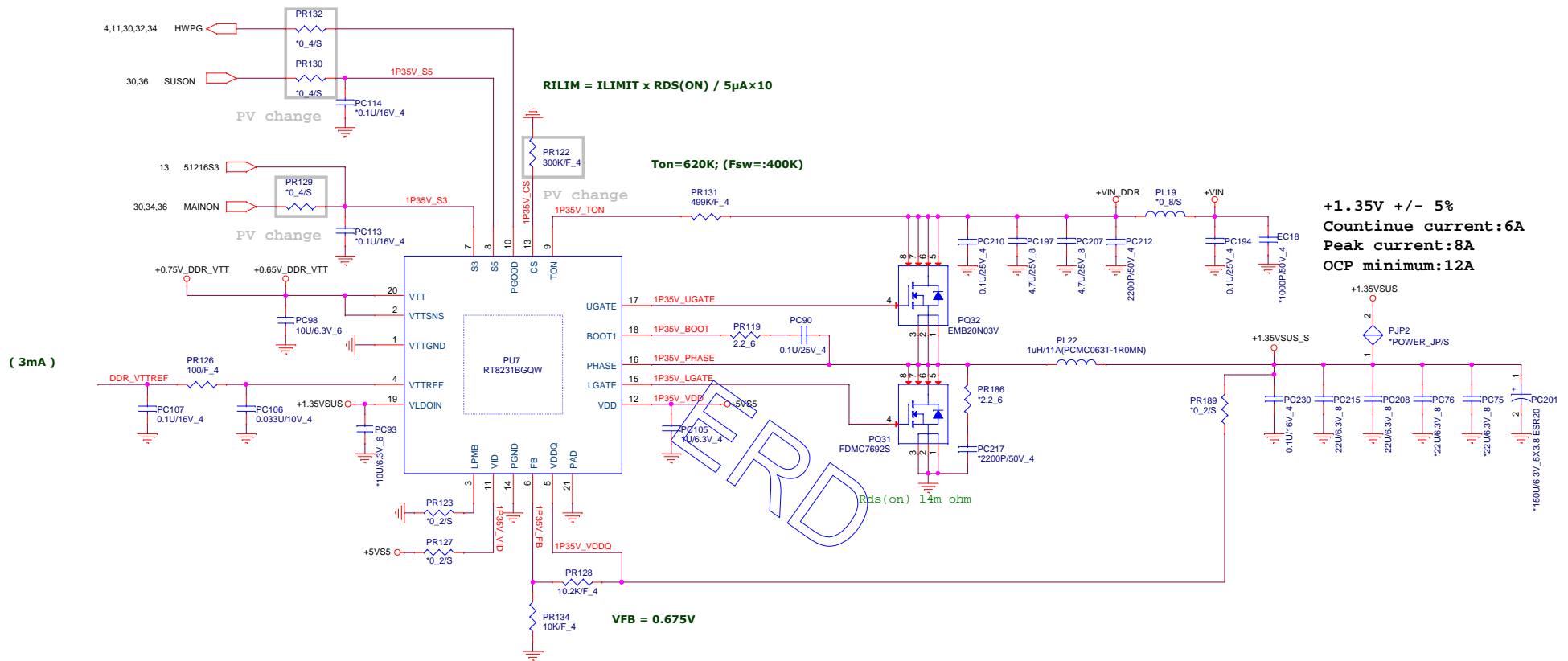
USB Charge Support	Ra	Rb
VINE (No support)	Stuff	NA
ENVY (Support) <sub>HP</sub>	NA	Stuff

**Do Not add test pad on VCC & LDO pin**

**PROJECT : X11**  
 Quanta Computer Inc.

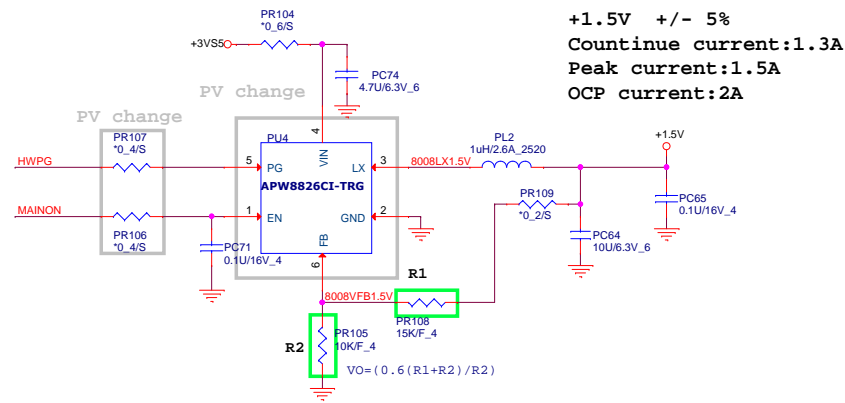
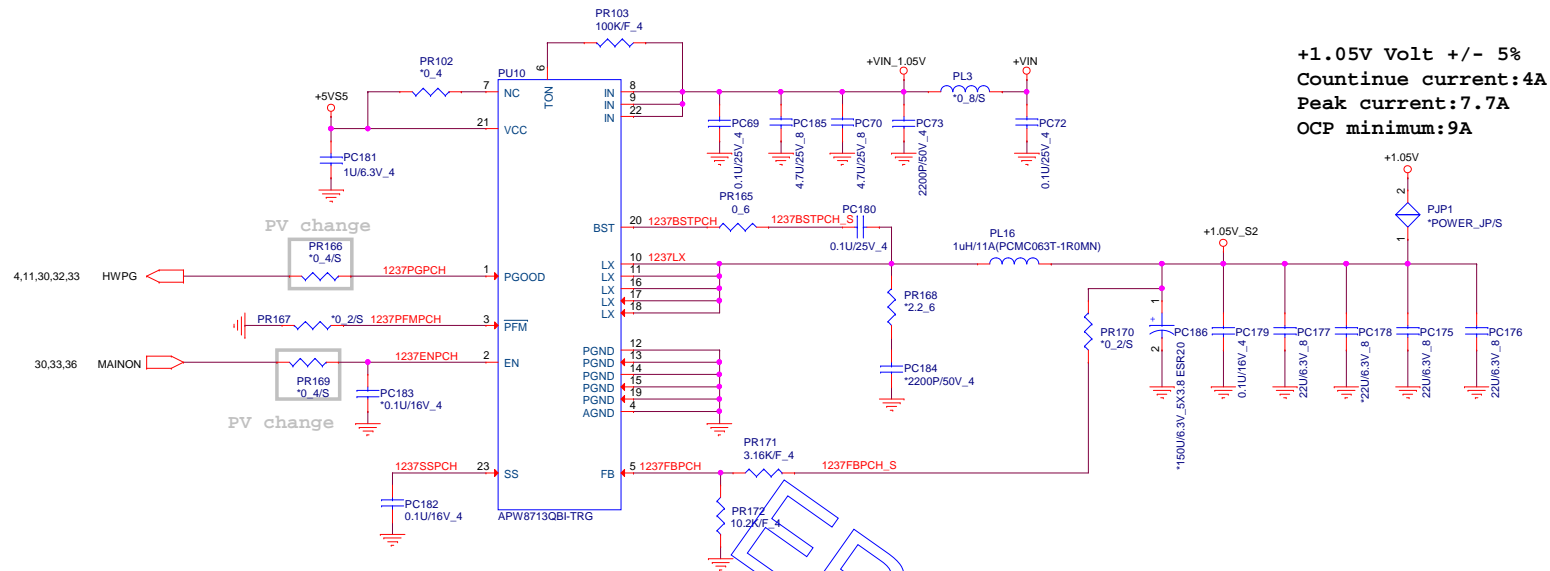
Size Custom	Document Number <b>3/5VPCU(RT8243A)</b>	Rev 1A
Date: Monday, January 05, 2015	Sheet	32 of 40





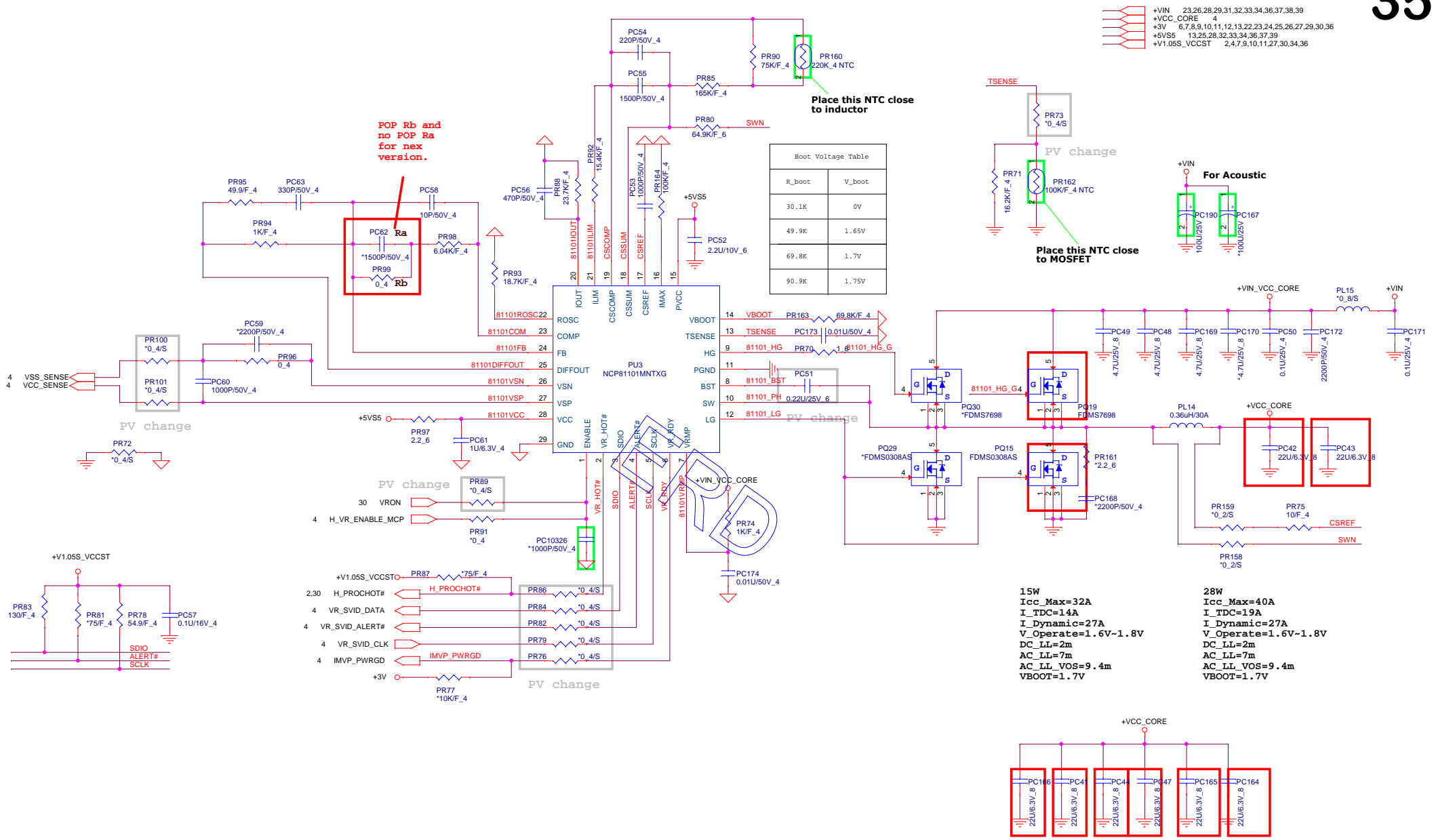
- +0.65V\_DDR\_VTT 12,13
- +5VS5 13,25,28,32,34,35,36,37,39
- +VIN 23,26,29,31,32,34,35,36,37,38,39
- +1.35VSUS 2,4,12,13

	<b>PROJECT : X11</b>		
	Quanta Computer Inc.		
Size Custom	Document Number	Rev 1A	
DDR3 (RT8231A)/1.8V55			
Date: Monday, January 05, 2015	Sheet 33	of 40	



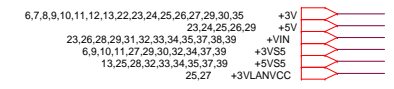
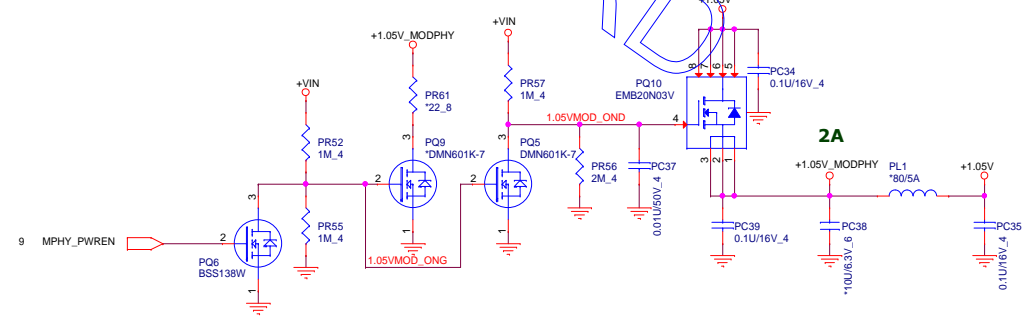
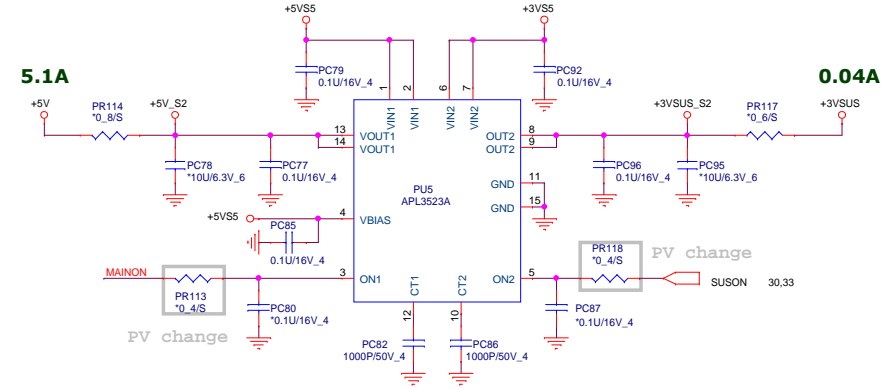
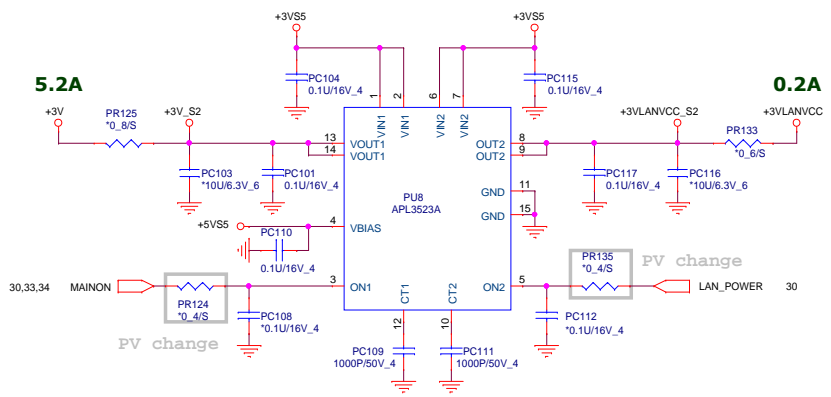
- +VIN 23,26,28,29,31,32,33,35,36,37,38,39
- +3VSS 6,9,10,11,27,29,30,32,36,37,39
- +5VSS 13,25,28,32,33,35,36,37,39

	<b>PROJECT : X11</b>	
	Quanta Computer Inc.	
Size Custom	Document Number <b>+1.1VS5 (RT8228)/2.5V</b>	Rev 1A
Date: Monday, January 05, 2015		Sheet 34 of 40

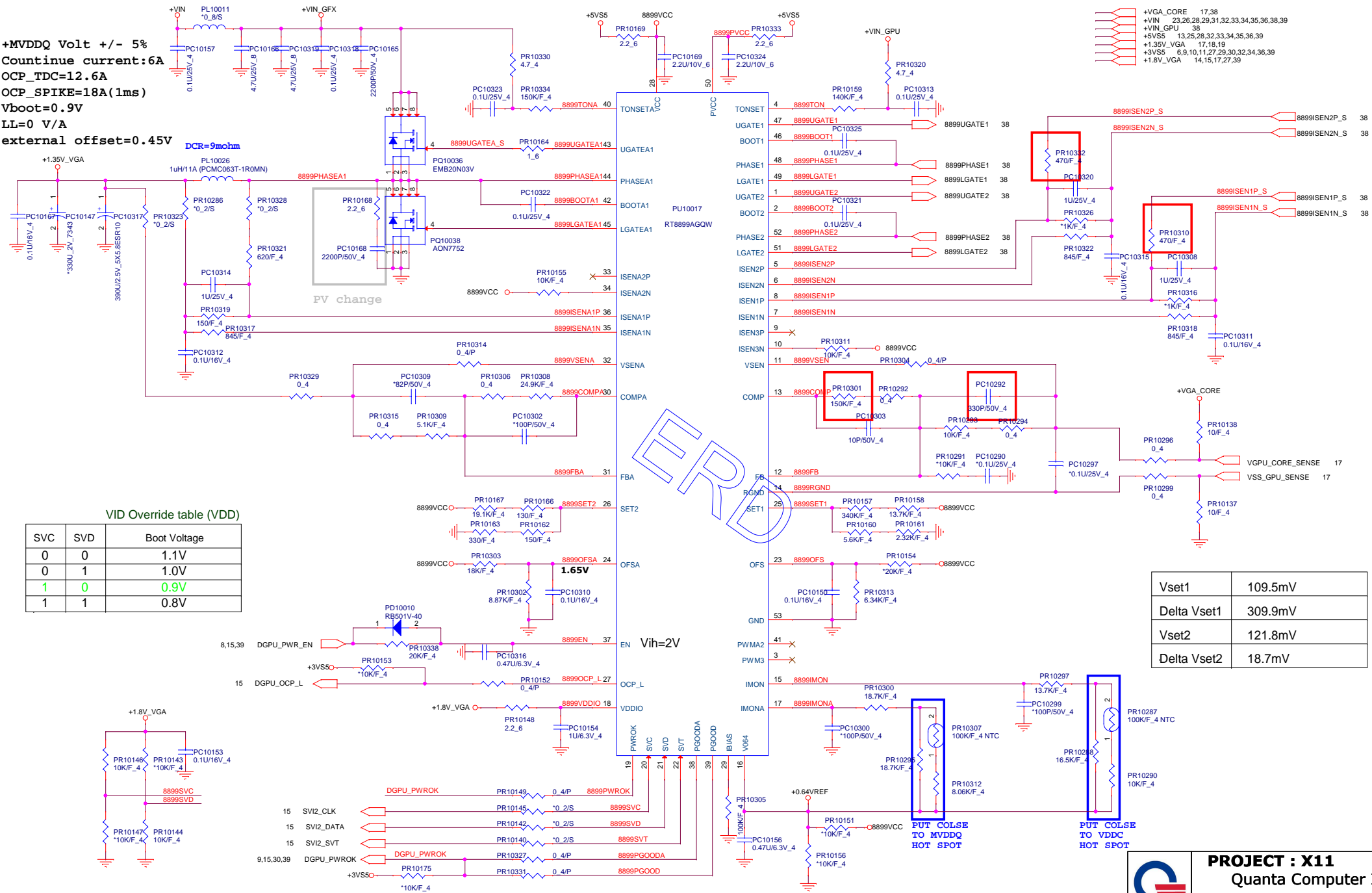


**PROJECT : X11**  
**Quanta Computer Inc.**

Size Custom	Document Number CPU Core (NCP81101)ULT	Rev 1A
Date: Monday, January 05, 2015    Sheet 35 of 40		



+MVDDQ Volt +/- 5%  
 Countinue current:6A  
 OCP\_TDC=12.6A  
 OCP\_SPIKE=18A(1ms)  
 Vboot=0.9V  
 LL=0 V/A  
 external offset=0.45V



- +VGA\_CORE 17,38
- +VIN 23,26,28,29,31,32,33,34,35,36,38,39
- +VIN\_GPU 38
- +VS5 13,25,28,32,33,34,35,36,39
- +1.35V\_VGA 17,18,19
- +3VS5 6,9,10,11,27,29,30,32,34,36,39
- +1.8V\_VGA 14,15,17,27,39

VID Override table (VDD)

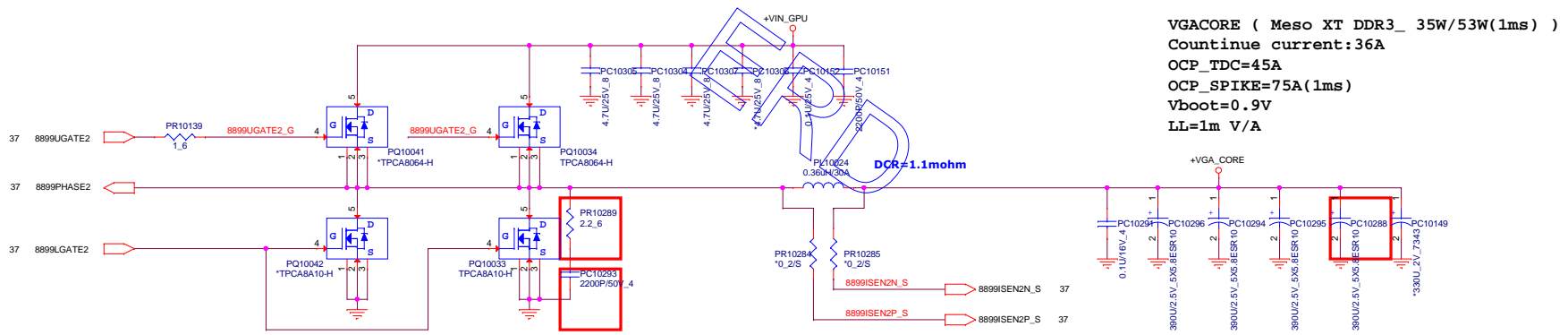
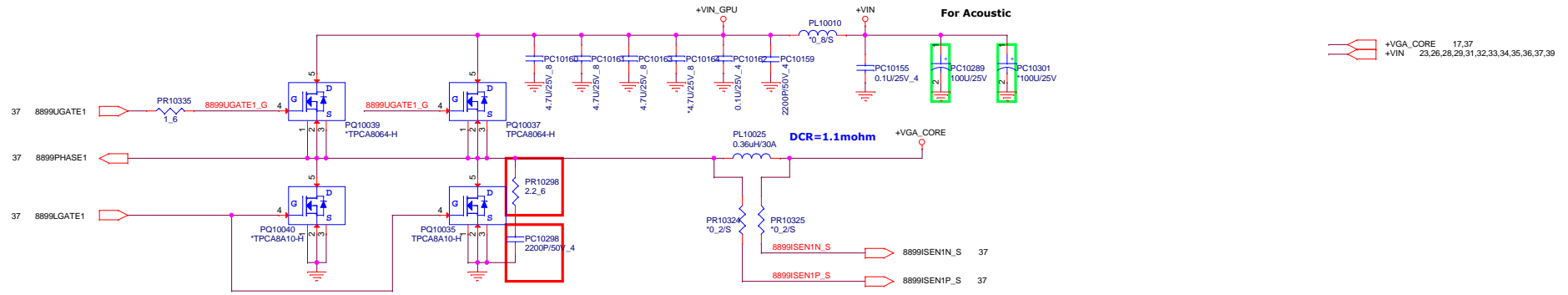
SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V


Vset1	109.5mV
Delta Vset1	309.9mV
Vset2	121.8mV
Delta Vset2	18.7mV

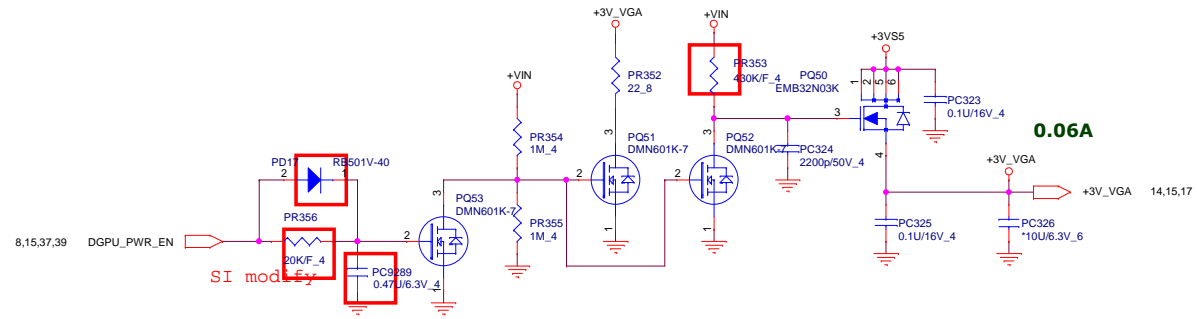
**PROJECT : X11**  
 Quanta Computer Inc.

Size	Document Number	Rev
Custom	Vcore( RT8899A)	1A

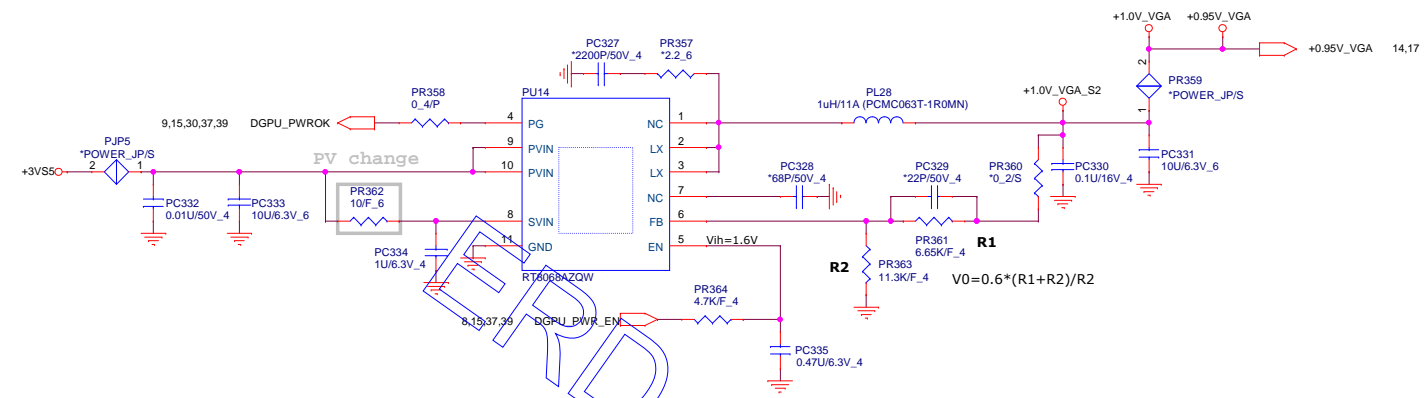
Date: Monday, January 05, 2015 Sheet 37 of 43



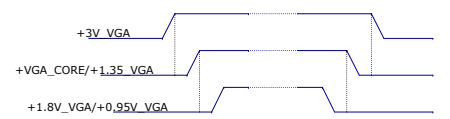
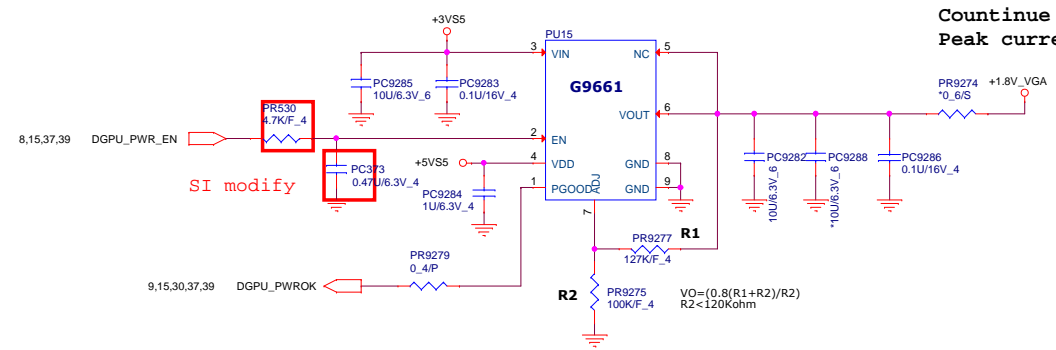
	<b>PROJECT : X11</b>		
	Quanta Computer Inc.		
Size Custom	Document Number <b>CPU Core2</b>	Rev 1A	
Date: Monday, January 05, 2015	Sheet 38 of 43		




**+0.95V +/- 3%**  
**Countinue current:2A**  
**Peak current:3A**  
**OCP minimum:4A<sup>HP</sup>**



**+1.8V\_VGA +/- 5%**  
**Countinue current:0.5A**  
**Peak current:2A**




 <b>PROJECT : X11</b> Quanta Computer Inc.		
Date: Monday, January 05, 2015		
Sheet 39		of 9

Battery Connector	Pavillion	ENVY
14"	-	-
15"	-	-
17"	-	-

USB Charge Support	PR185	PR184
Pavillion	Stuff	NA
ENVY (USB charge)	NA	Stuff

UMA	Disable Page 41 、 42 、 43 ,but keep below location
Page 41	PC161 、 PC162
Page 42	PC138 、 PC144 、 PC4 、 PC148
Page 43	PC84 、 PC102 、 PC88 、 PC97 、 PC40 、 PC33

Discrete	Location	Part Number
N15S (25W)	PR155	CS29532FB10
	PC151 、 PC160	NA
	PQ21 、 PQ23 、 PQ25 、 PQ28	NA
N15P (35W)	PR155	CS31242FB13
	PC151 、 PC160	Stuff
	PQ21 、 PQ23 、 PQ25 、 PQ28	Stuff

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