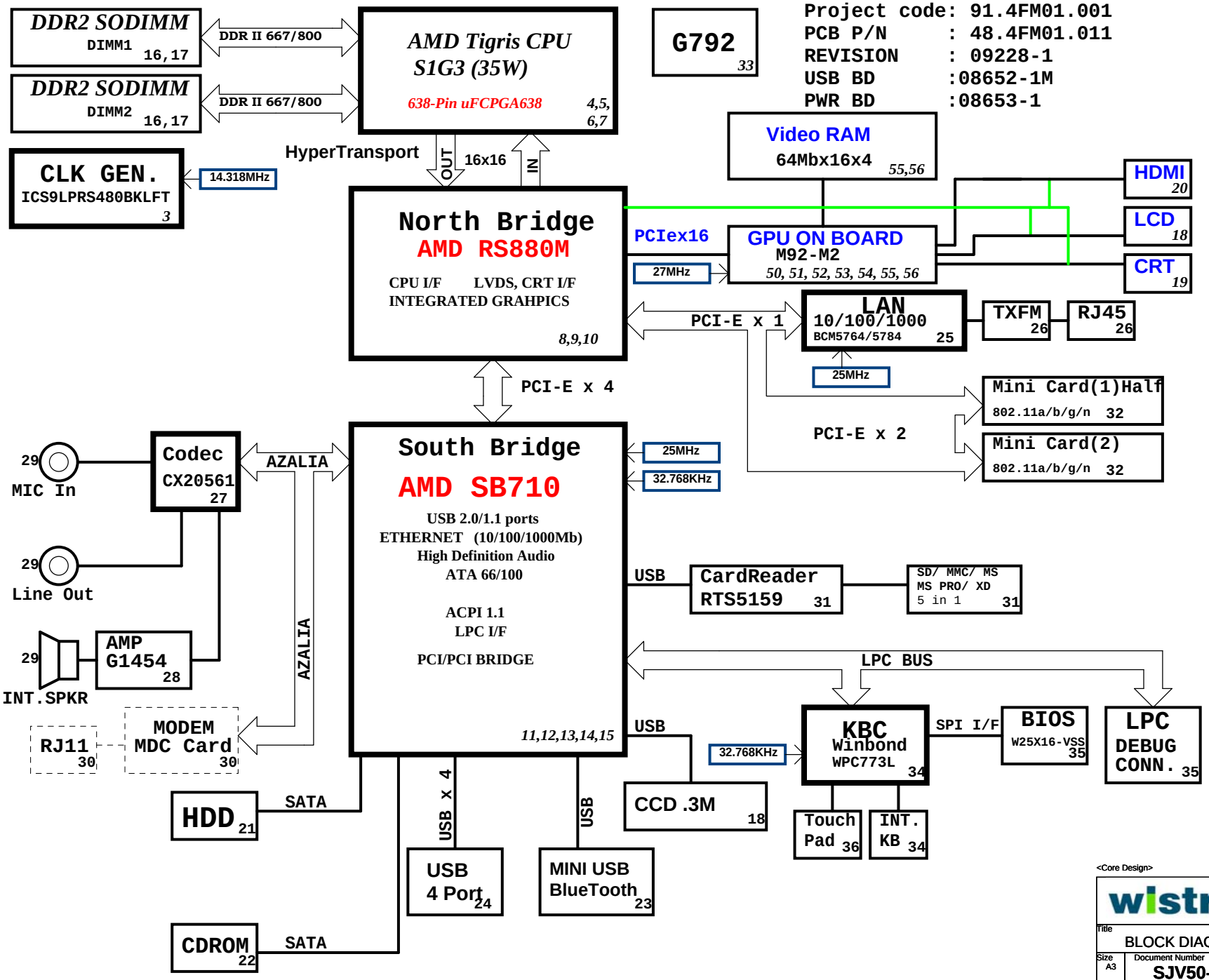
SJV50-TR Block Diagram



PCB Layer Stackup
L1: Signal 1
L2: VCC
L3: Inner Signal 2
L4: Inner Signal 3
L5: GND
L6: Signal 4

CPU V_CORE

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	1D1V_S0 1D2V_S0 1D8V_S3

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

SYSTEM LDO

INPUT	OUTPUT
1D8V_S3	0D9V_S3

SYSTEM LDO

INPUT	OUTPUT
3D3V_S5 3D3V_S0 3D3V_S0	1D2V_S5 2D5V_S0 1D5V_S0

SYSTEM LDO

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

Battery Charger

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

<Core Design>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: BLOCK DIAGRAM

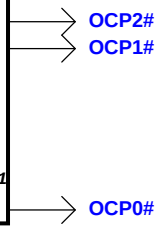
Size: A3 | Document Number: SJV50-TR | Rev: -1

Date: Monday, June 29, 2009 | Sheet 1 of 59

PCIE

PCIE0	LAN
PCIE1	MINICARD1
PCIE2	MINICARD2
PCIE3	

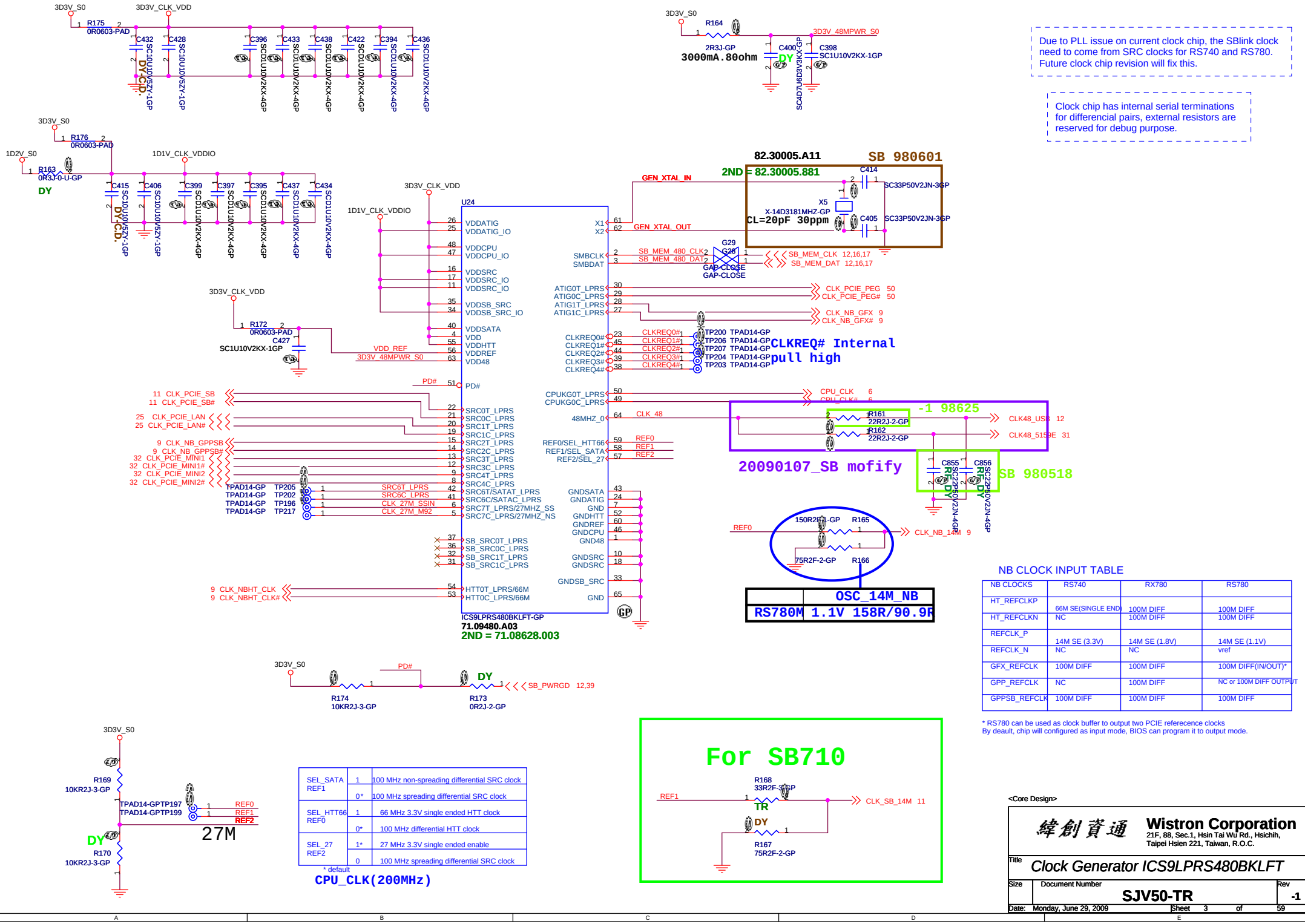
USB	
Pair	Device
11	CardReader
10	CCD
9	Mini Card2
8	USB4
7	USB1
6	USB2
5	BlueTooth
4	NC
3	NC
2	NC
1	Mini Card1
0	USB3



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB&PCIE ROUTING		
Size: A3	Document Number: SJV50-TR	Rev: -1
Date: Monday, June 29, 2009	Sheet 2 of 59	


3D3V_S0
3D3V_CLK_VDD
R175 0R0603-PAD
C432 SC10U10V5ZY-1GP
C428 SC10U10V5ZY-1GP
C396 SC1U10V2KX-4GP
C433 SC1U10V2KX-4GP
C438 SC1U10V2KX-4GP
C422 SC1U10V2KX-4GP
C394 SC1U10V2KX-4GP
C436 SC1U10V2KX-4GP
DY C.D.
3D3V_S0
R164 2R3J-GP
3000mA.80ohm
3D3V_48MPWR_S0
C400 DY
C398 SC1U10V2KX-1GP
SC4D7U6D3V3KX-GP
Due to PLL issue on current clock chip, the SBlink clock need to come from SRC clocks for RS740 and RS780. Future clock chip revision will fix this.
Clock chip has internal serial terminations for differencial pairs, external resistors are reserved for debug purpose.
3D3V_S0
R176 0R0603-PAD
1D2V_S0
R163 0R3J-0-U-GP
DY
1D1V_CLK_VDDIO
C415 SC10U10V5ZY-1GP
C406 SC10U10V5ZY-1GP
C399 SC1U10V2KX-4GP
C397 SC1U10V2KX-4GP
C395 SC1U10V2KX-4GP
C437 SC1U10V2KX-4GP
C434 SC1U10V2KX-4GP
DY C.D.
82.30005.A11
SB 980601
2ND = 82.30005.881
GEN_XTAL_IN
GEN_XTAL_OUT
X5 X-14D3181MHZ-GP
CL=20pF 30ppm
C414 SC33P50V2JN-3GP
C405 SC33P50V2JN-3GP
3D3V_CLK_VDD
1D1V_CLK_VDDIO
U24
VDDATIG
VDDATIG_IO
VDDCPU
VDDCPU_IO
VDDSRC
VDDSRC_IO
VDDSRC_IO
VDDSB_SRC
VDDSB_SRC_IO
VDDSATA
VDD
VDDHTT
VDDREF
VDD48
X1
X2
SMBCLK
SMBDAT
SB_MEM_480_CLK
SB_MEM_480_DAT
G29 GAP-CLOSE
G28 GAP-CLOSE
SB_MEM_CLK 12,16,17
SB_MEM_DAT 12,16,17
ATIG0T_LPRS
ATIG0C_LPRS
ATIG1T_LPRS
ATIG1C_LPRS
CLK_PCIE_PEG 50
CLK_PCIE_PEG# 50
CLK_NB_GFX 9
CLK_NB_GFX# 9
CLKREQ0#
CLKREQ1#
CLKREQ2#
CLKREQ3#
CLKREQ4#
TP200 TPAD14-GP
TP206 TPAD14-GP
TP207 TPAD14-GP
TP204 TPAD14-GP
TP203 TPAD14-GP
CLKREQ# Internal pull high
3D3V_CLK_VDD
R172 0R0603-PAD
C427 SC1U10V2KX-1GP
VDD_REF
3D3V_48MPWR_S0
PD#
CPUKG0T_LPRS
CPUKG0C_LPRS
CPU_CLK 6
CPU_CLK# 6
48MHZ_0
CLK_48
-1 98625
R161 22R2J-2-GP
R162 22R2J-2-GP
CLK48_USB 12
CLK48_515E 31
20090107_SB mofify
C855 SC22P50V2JN-4GP
C856 SC22P50V2JN-4GP
DY
SB 980518
REF0
REF1
REF2
REF1/SEL_SATA
REF2/SEL_27
11 CLK_PCIE_SB
11 CLK_PCIE_SB#
25 CLK_PCIE_LAN
25 CLK_PCIE_LAN#
9 CLK_NB_GPPSB
9 CLK_NB_GPPSB#
32 CLK_PCIE_MINI1
32 CLK_PCIE_MINI1#
32 CLK_PCIE_MINI2
32 CLK_PCIE_MINI2#
SRC0T_LPRS
SRC0C_LPRS
SRC1T_LPRS
SRC1C_LPRS
SRC2T_LPRS
SRC2C_LPRS
SRC3T_LPRS
SRC3C_LPRS
SRC4T_LPRS
SRC4C_LPRS
SRC6T/SATAT_LPRS
SRC6C/SATAC_LPRS
SRC7T_LPRS/27MHZ_SS
SRC7C_LPRS/27MHZ_NS
TPAD14-GP TP205
TPAD14-GP TP202
TPAD14-GP TP196
TPAD14-GP TP217
SRC6T_LPRS
SRC6C_LPRS
CLK_27M_SSIN
CLK_27M_M92
SB_SRC0T_LPRS
SB_SRC0C_LPRS
SB_SRC1T_LPRS
SB_SRC1C_LPRS
9 CLK_NBHT_CLK
9 CLK_NBHT_CLK#
HTT0T_LPRS/66M
HTT0C_LPRS/66M
GNDSATA
GNDATIG
GND
GNDHTT
GNDREF
GNDCPU
GND48
GNDSRC
GNDSRC
GNDSB_SRC
GND
ICS9LPRS480BKLFT-GP
71.09480.A03
2ND = 71.08628.003
150R2F-GP R165
75R2F-2-GP R166
CLK_NB_14M 9
OSC_14M_NB
RS780M 1.1V 158R/90.9R
3D3V_S0
PD#
DY
SB_PWRGD 12,39
R174 10KR2J-3-GP
R173 0R2J-2-GP
NB CLOCK INPUT TABLE
NB CLOCKS | RS740 | RX780 | RS780
HT_REFCLKP | 66M SE(SINGLE END) | 100M DIFF | 100M DIFF
HT_REFCLKN | NC | 100M DIFF | 100M DIFF
REFCLK_P | 14M SE (3.3V) | 14M SE (1.8V) | 14M SE (1.1V)
REFCLK_N | NC | NC | vref
GFX_REFCLK | 100M DIFF | 100M DIFF | 100M DIFF(IN/OUT)*
GPP_REFCLK | NC | 100M DIFF | NC or 100M DIFF OUTPUT
GPPSB_REFCLK | 100M DIFF | 100M DIFF | 100M DIFF
* RS780 can be used as clock buffer to output two PCIE referecence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.
3D3V_S0
R169 10KR2J-3-GP
TPAD14-GPTP197
TPAD14-GPTP199
REF0
REF1
REF2
27M
DY
R170 10KR2J-3-GP
SEL_SATA REF1
1 100 MHz non-spreading differential SRC clock
0* 100 MHz spreading differential SRC clock
SEL_HTT66 REF0
1 66 MHz 3.3V single ended HTT clock
0* 100 MHz differential HTT clock
SEL_27 REF2
1* 27 MHz 3.3V single ended enable
0 100 MHz spreading differential SRC clock
* default
CPU_CLK(200MHz)
For SB710
REF1
R168 33R2F-GP
TR
DY
R167 75R2F-2-GP
CLK_SB_14M 11
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Clock Generator ICS9LPRS480BKLFT
Size
Document Number
SJV50-TR
Rev
-1
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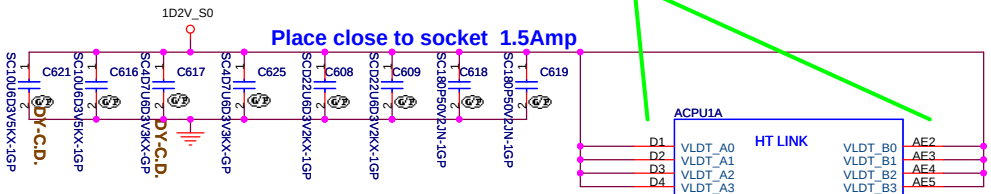
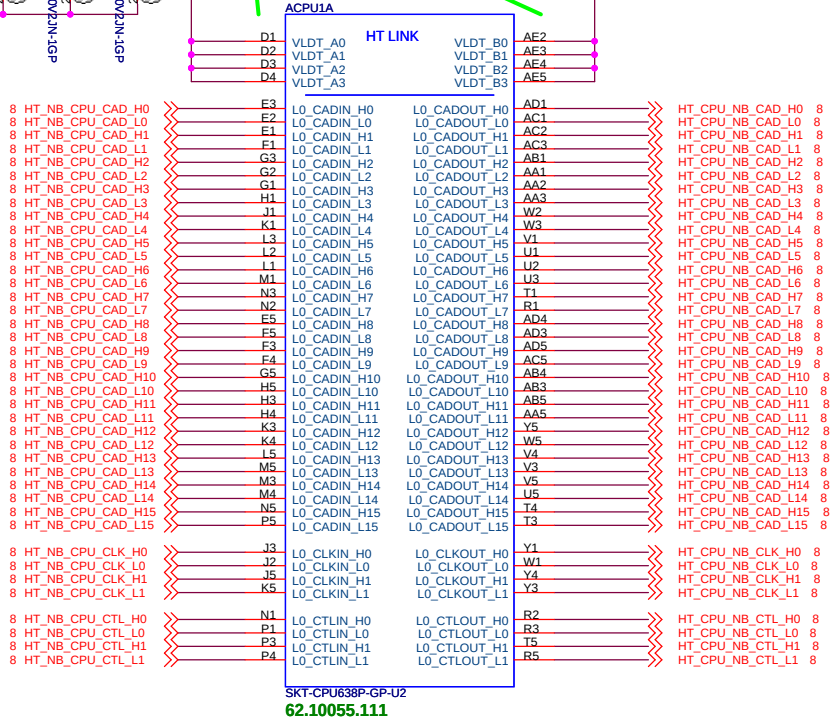
Placement note:
10ux1,4.7ux1,0.22ux1,180px1 for each group





SKT-BGA638H176

State	Specification	Notes	2M200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P2	CPU COF	1	1500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P3	CPU COF	1	1300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P4	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P6	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P7	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V

<Core Design>

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Title: ***CPU (1 of 4)***

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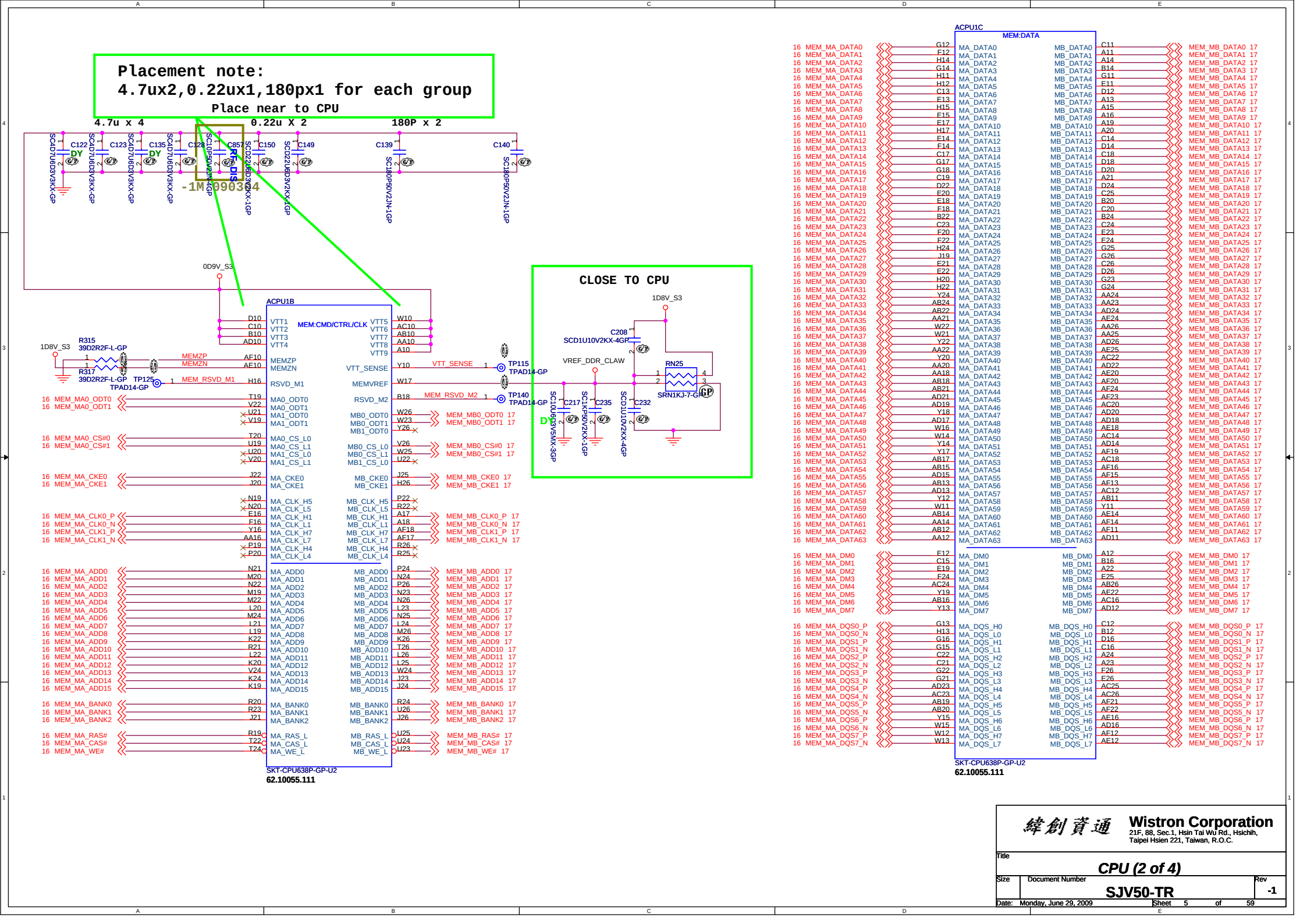
Placement note:
4.7ux2,0.22ux1,180px1 for each group
Place near to CPU
4.7u x 4
0.22u X 2
180P x 2
-1M090334
CLOSE TO CPU
ACPU1B
MEM:CMD/CTRL/CLK
ACPU1C
MEM:DATA
SKT-CPU638P-GP-U2
62.10055.111
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CPU (2 of 4)
SJV50-TR
-1
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The Processor has reached a preset maximum operating temperature. 100℃
I=Active HTC
O=FAN

LYAOUT:ROUTE VDDA TRACE APPROX. 50mils WIDE(USE 2X25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491

SB_980430

Cloce To CPU

For HDT DBG

internal pull high 300 ohm

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

R614,R615
PU use 300R
TR use 510R

SA_980326

SB_980511

SA_20081030

CPU exceeds to 125℃

84.T3904.C11
2ND = 84.03904.L06
3RD = 84.03904.P11

SKT-CPU638P-GP-U2
62.10055.111

HDT Connectors

SMC-CONN26A-FP

<Core Design>

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Title	***CPU (3 of 4)***	
Size	Document Number **SJV50-TR**	Rev -1
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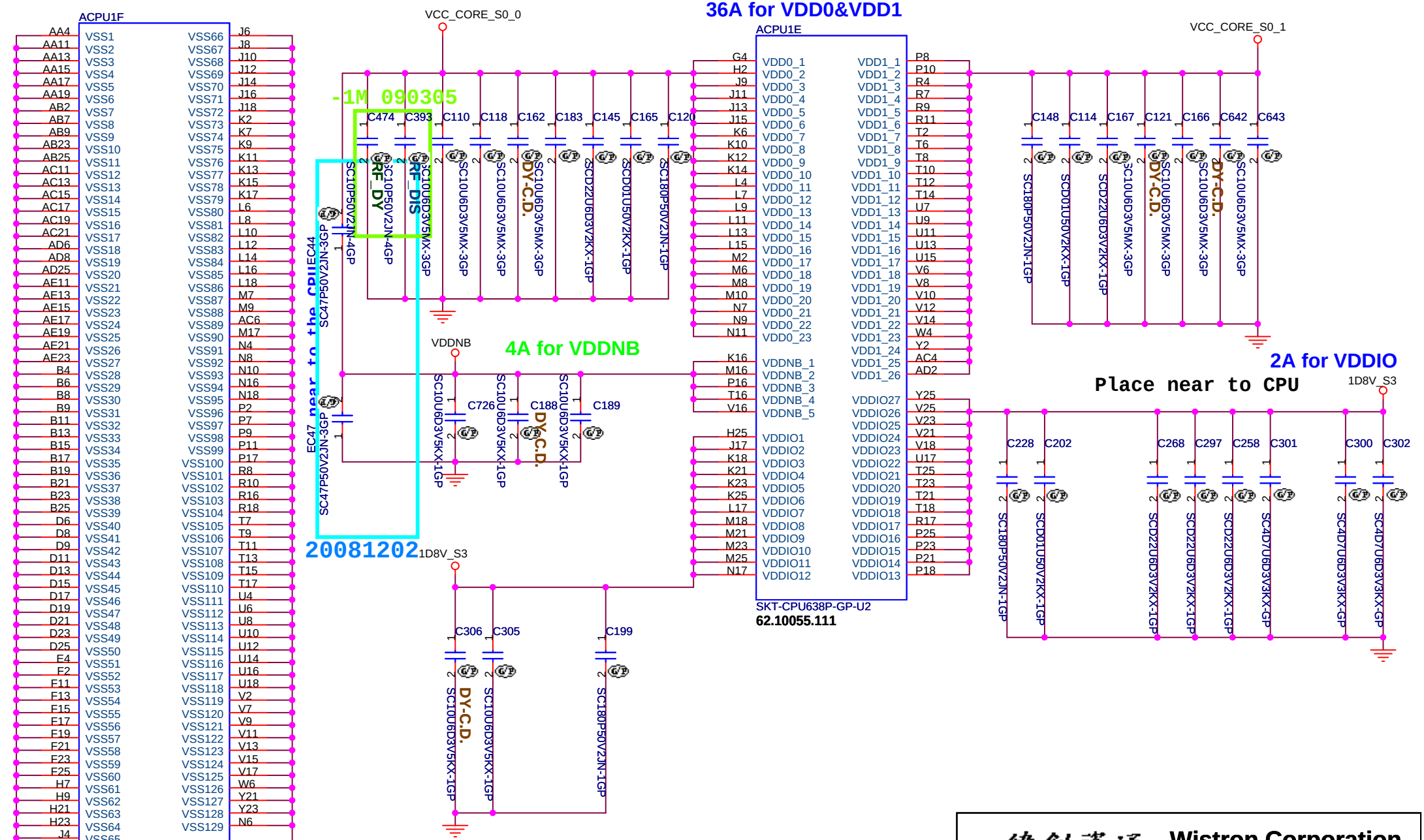

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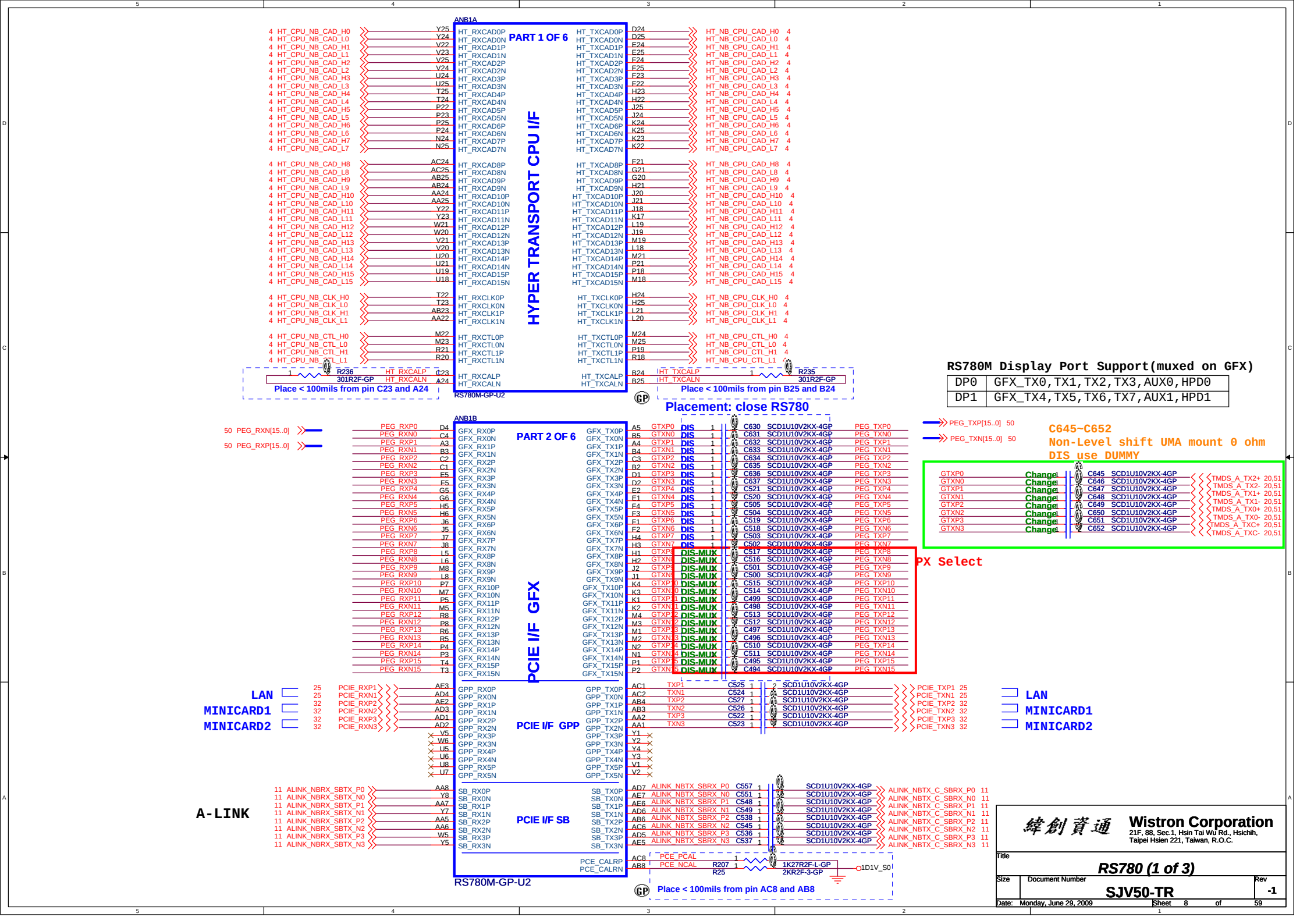
Title	CPU (4 of 4)	
Size	Document Number: SJV50-TR	Rev: -1
Date: Monday, June 29, 2009	Sheet 7 of 59	



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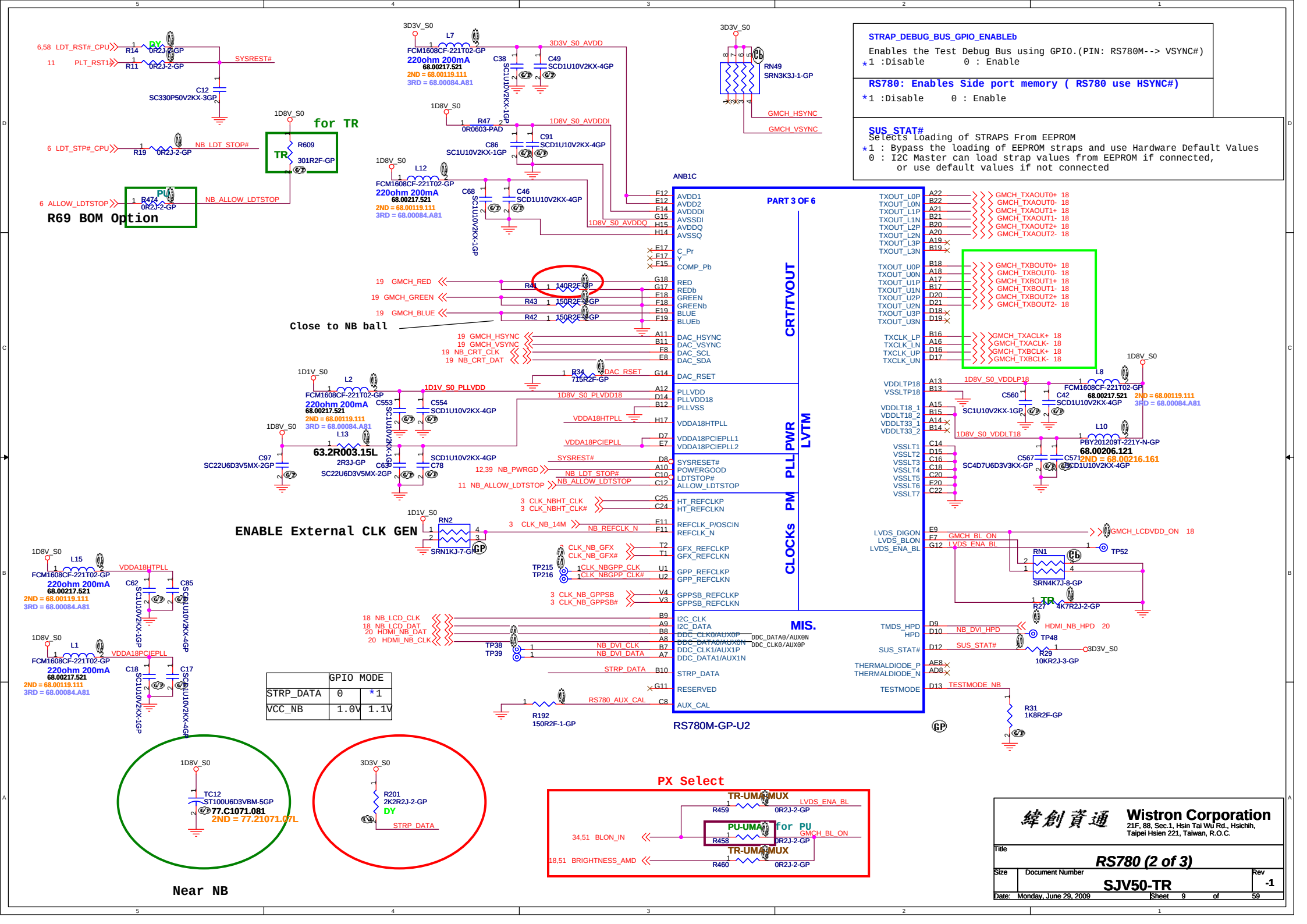
Title	RS780 (1 of 3)
Size	Document Number: SJV50-TR
Rev	-1
Date: Monday, June 29, 2009	Sheet 8 of 59


STRAP_DEBUG_BUS_GPIO_ENABLEb
Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC#)
*1 :Disable 0 : Enable
RS780: Enables Side port memory (RS780 use HSYNC#)
*1 :Disable 0 : Enable
SUS_STAT#
Selects Loading of STRAPS From EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected,
or use default values if not connected
R69 BOM Option
for TR
Close to NB ball
ENABLE External CLK GEN
ANB1C
PART 3 OF 6
CRT/TVOUT
PLL/PWR
LVTM
CLOCKs
PM
MIS.
RS780M-GP-U2
GPIO MODE
STRP_DATA 0 *1
VCC_NB 1.0V 1.1V
PX Select
TR-UMA-MUX
PU-UMA
for PU
Near NB
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
RS780 (2 of 3)
SJV50-TR
Rev -1
Date: Monday, June 29, 2009
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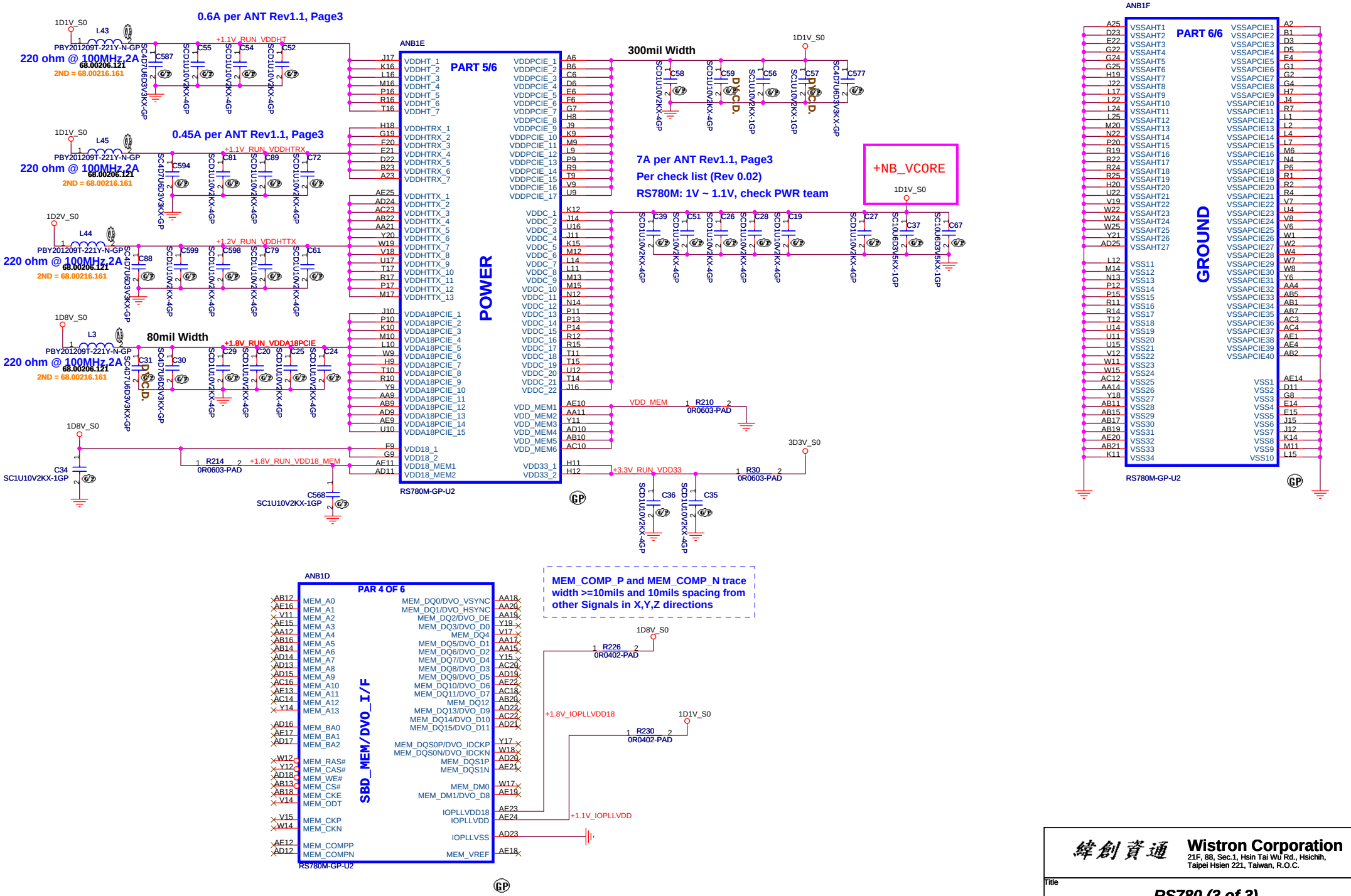
0.6A per ANT Rev1.1, Page3
0.45A per ANT Rev1.1, Page3
80mil Width
300mil Width
7A per ANT Rev1.1, Page3
Per check list (Rev 0.02)
RS780M: 1V ~ 1.1V, check PWR team
+NB_VCORE
ANB1E
PART 5/6
POWER
RS780M-GP-U2
ANB1F
PART 6/6
GROUND
RS780M-GP-U2
ANB1D
PAR 4 OF 6
SBD_MEM/DVO_I/F
RS780M-GP-U2
MEM_COMP_P and MEM_COMP_N trace width >=10mils and 10mils spacing from other Signals in X,Y,Z directions
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.
RS780 (3 of 3)
SJV50-TR
Rev -1
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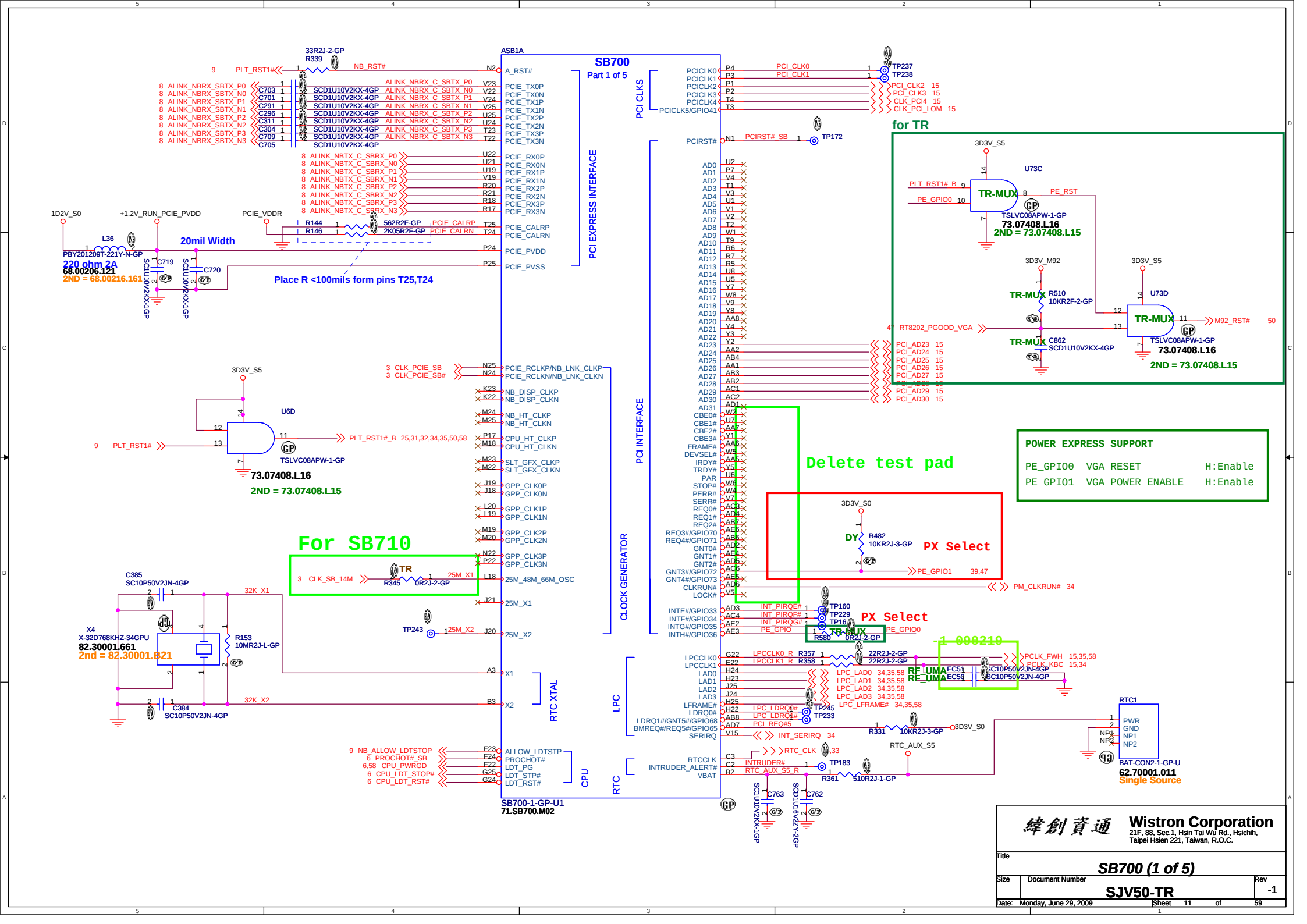
SB700
Part 1 of 5
ASB1A
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
CLOCK GENERATOR
LPC
RTC
CPU
RTC XTAL
for TR
TR-MUX
TSLVC08APW-1-GP
73.07408.L16
2ND = 73.07408.L15
Delete test pad
PX Select
For SB710
POWER EXPRESS SUPPORT
PE_GPIO0 VGA RESET H:Enable
PE_GPIO1 VGA POWER ENABLE H:Enable
20mil Width
Place R <100mils form pins T25,T24
220 ohm 2A
68.00206.121
2ND = 68.00216.161
X4
X-32D768KHZ-34GPU
82.30001.661
2nd = 82.30001.821
SB700-1-GP-U1
71.SB700.M02
RTC1
BAT-CON2-1-GP-U
62.70001.011
Single Source
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
SB700 (1 of 5)
SJV50-TR
Rev -1
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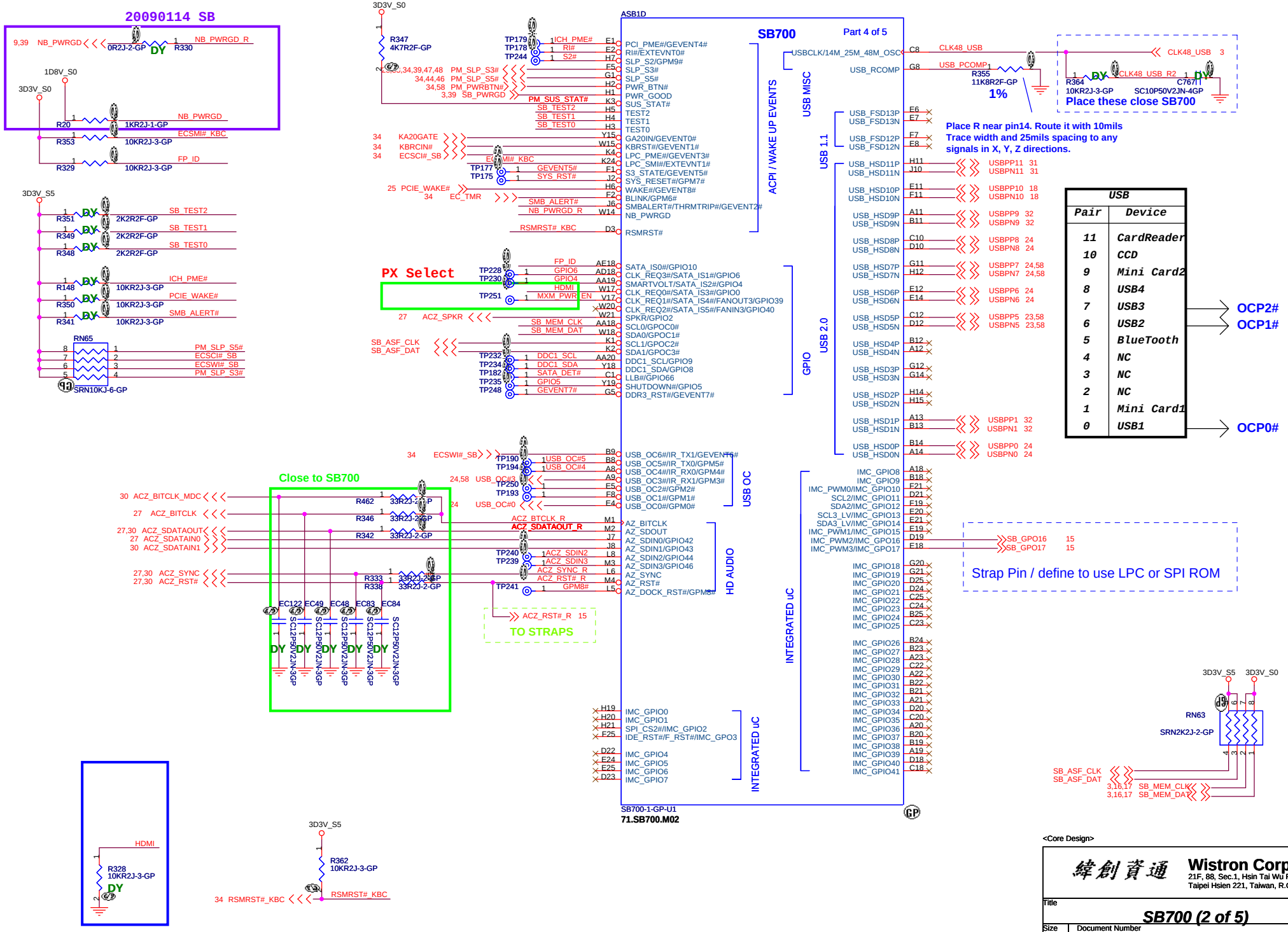

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: SB700 (2 of 5)

Size | Document Number: SJV50-TR | Rev: -1

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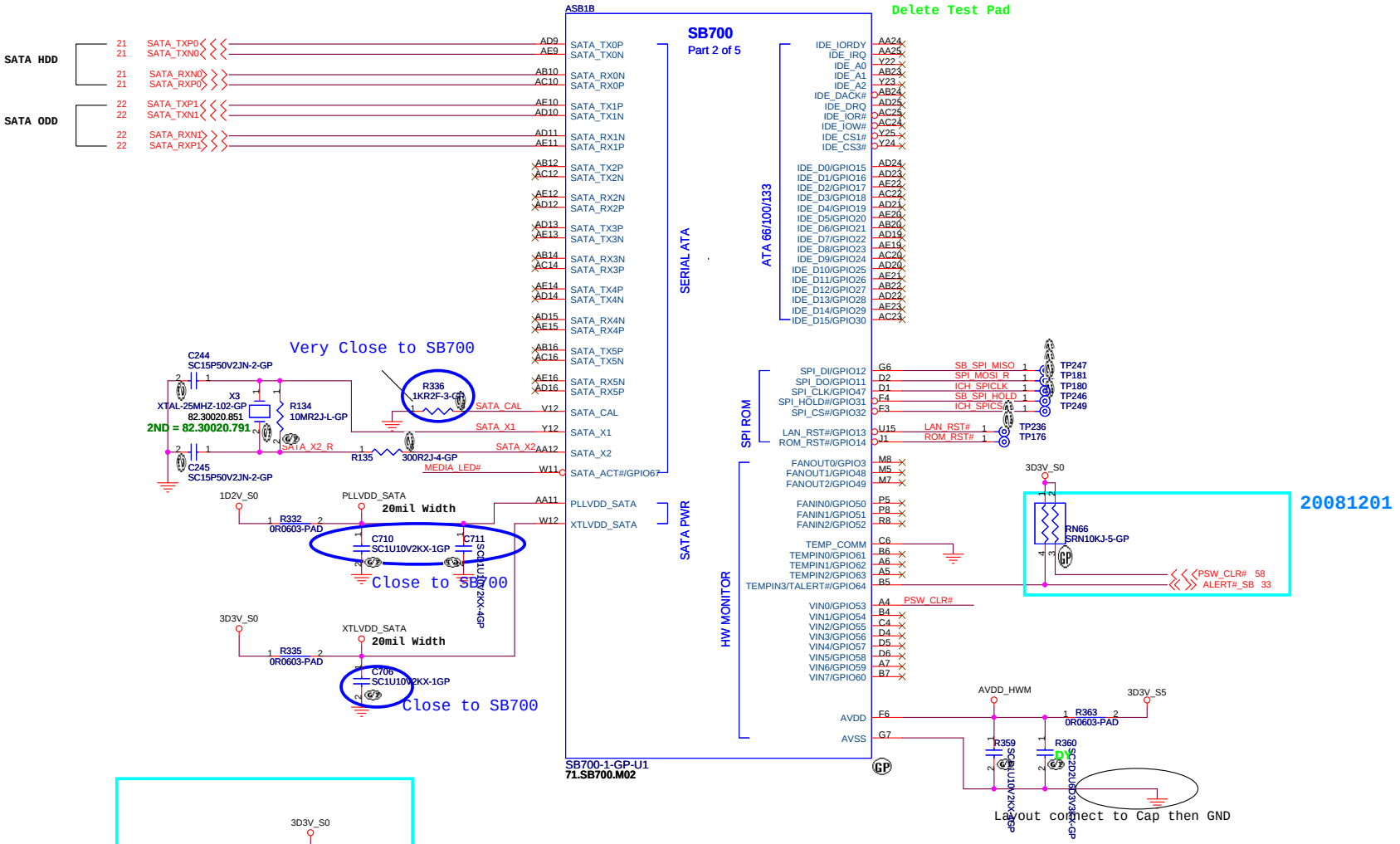

<Core Design>

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Title: SB700 (3 of 5)

Size | Document Number: SJV50-TR | Rev: -1

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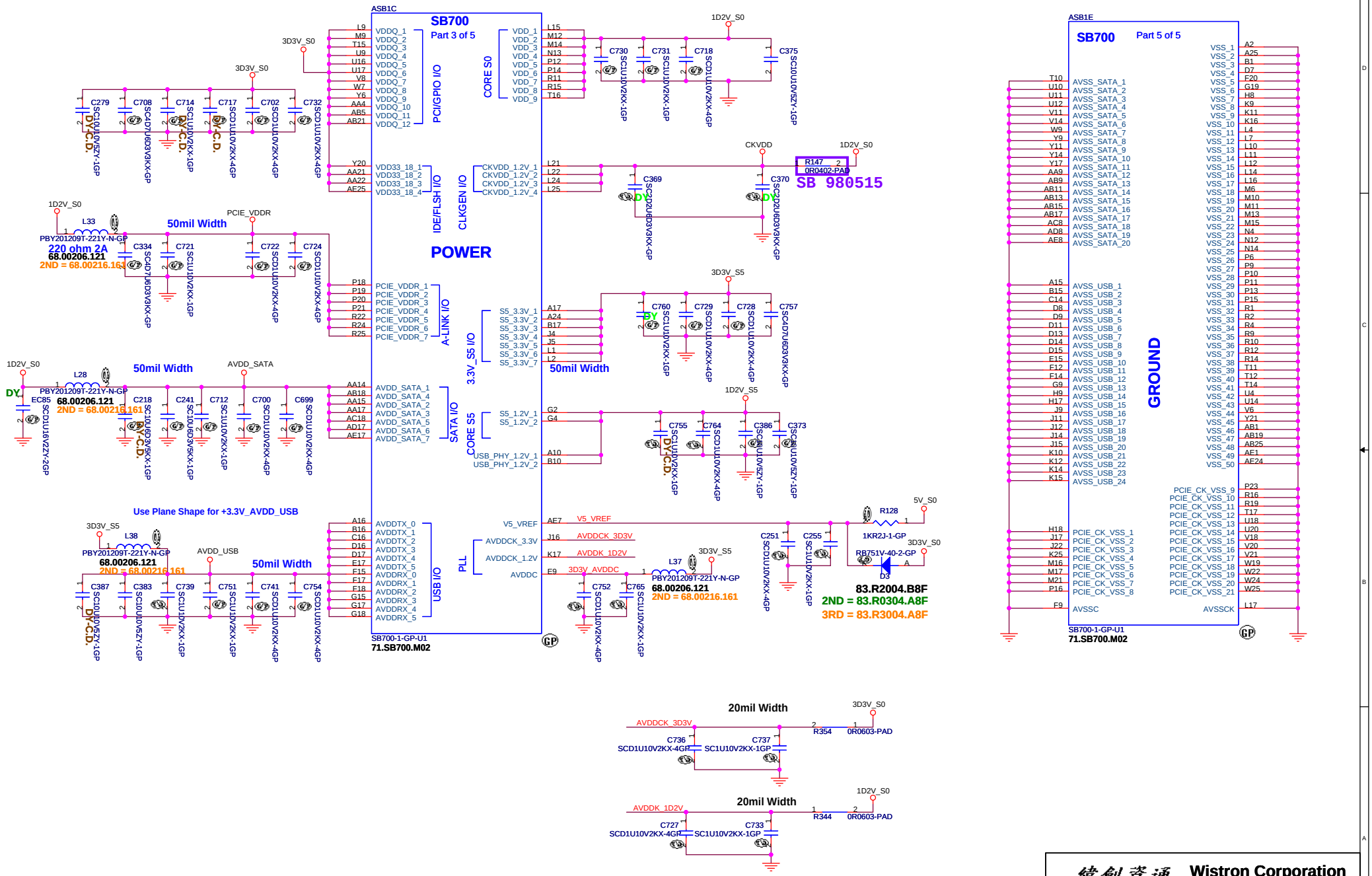
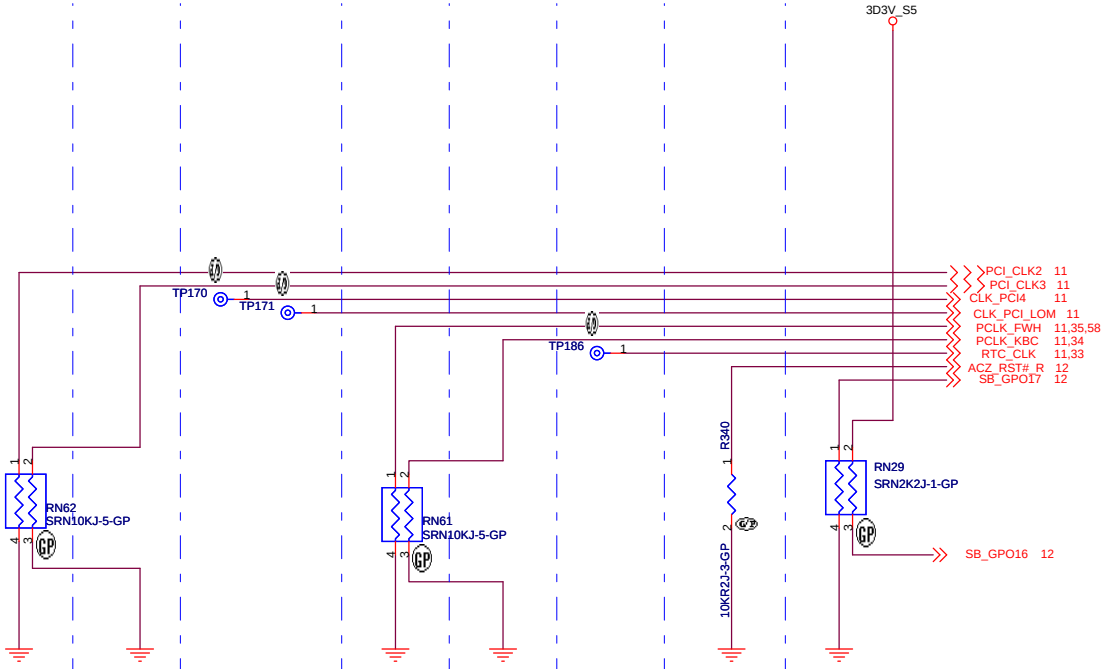

ASB1C
SB700
Part 3 of 5
POWER
PCI/GPIO I/O
CORE S0
IDE/FLSH I/O
CLKGEN I/O
A-LINK I/O
3.3V_S5 I/O
SATA I/O
USB I/O
PLL
50mil Width
220 ohm 2A
68.00206.121
2ND = 68.00216.161
Use Plane Shape for +3.3V_AVDD_USB
SB700-1-GP-U1
71.SB700.M02
ASB1E
SB700
Part 5 of 5
GROUND
SB700-1-GP-U1
71.SB700.M02
SB 980515
20mil Width
83.R2004.B8F
2ND = 83.R0304.A8F
3RD = 83.R3004.A8F
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
SB700 (4 of 5)
SJV50-TR
Rev -1
Date: Monday, June 29, 2009
Sheet 14 of 59

Delete DY Parts

REQUIRED STRAPS

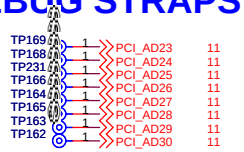
REQUIRED SYSTEM STRAPS



	PCI_CLK2	PCI_CLK3	CLK_PCI_LOM CLK_PCI4	PCLK_FWH	PCLK_KBC	RTCCLK	AZ_RST#	SB_GPO17 , SB_GPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT	ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	L, H = LPC ROM L, L = FWH ROM

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

DEBUG STRAPS



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: SB700 (5 of 5)

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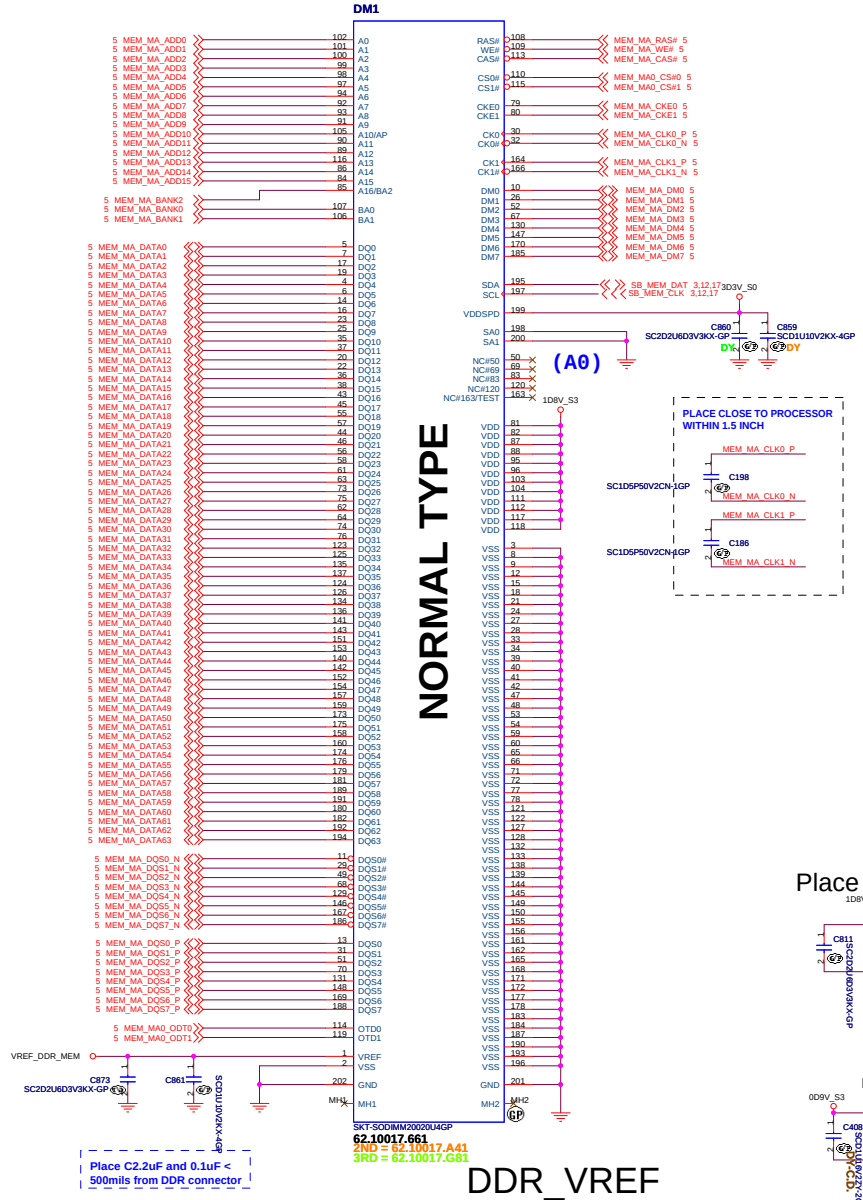
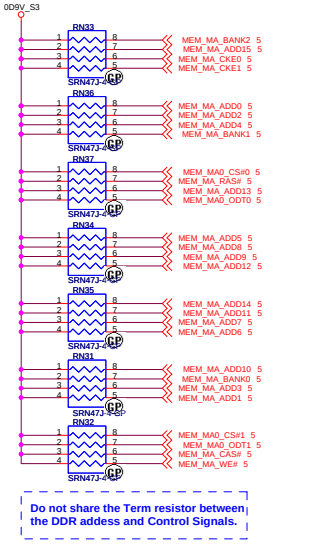
DDR2 SOCKET_1 (5.2mm)



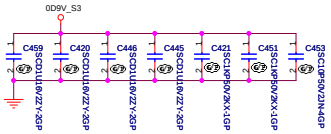
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

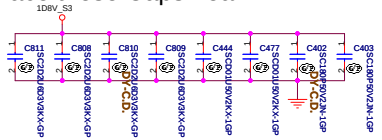


Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

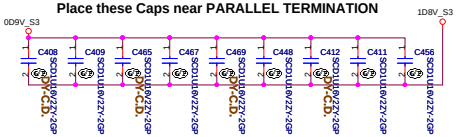


Place these Caps near DM2

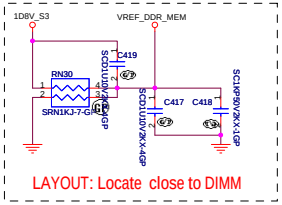


Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near PARALLEL TERMINATION



DDR_VREF



Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: DDR2 Socket_1	
Size	Document Number: SJV50-TR
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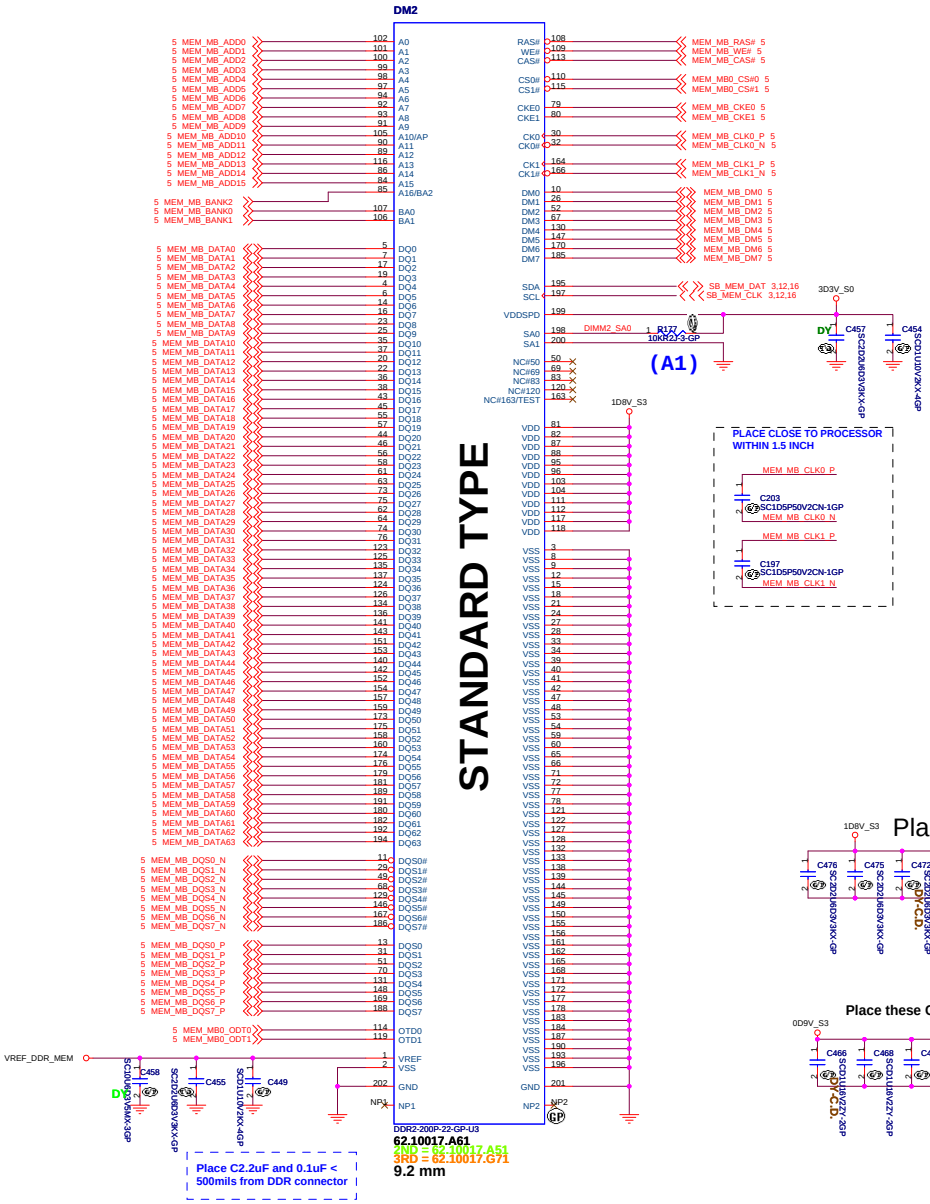
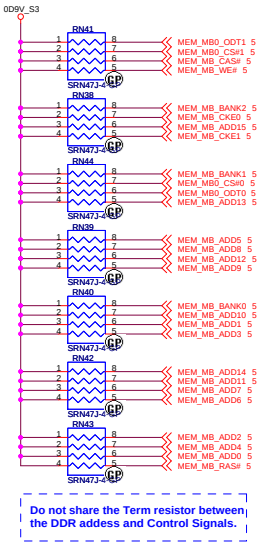
DDR2 SOCKET_2 (9.2mm)



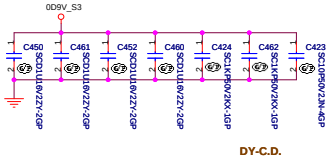
PARALLEL TERMINATION

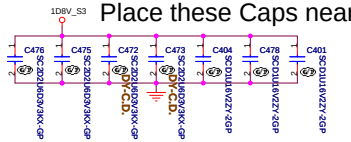
Put decap near power(0.9V) and pull-up resistor



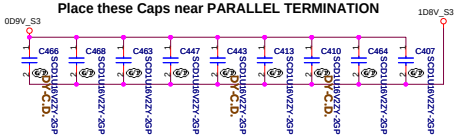
Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor





Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3



緯創資通 Wistron Corporation		
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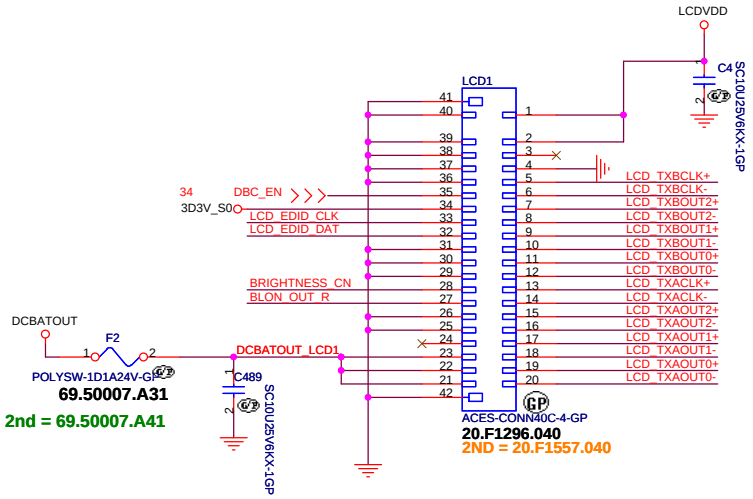
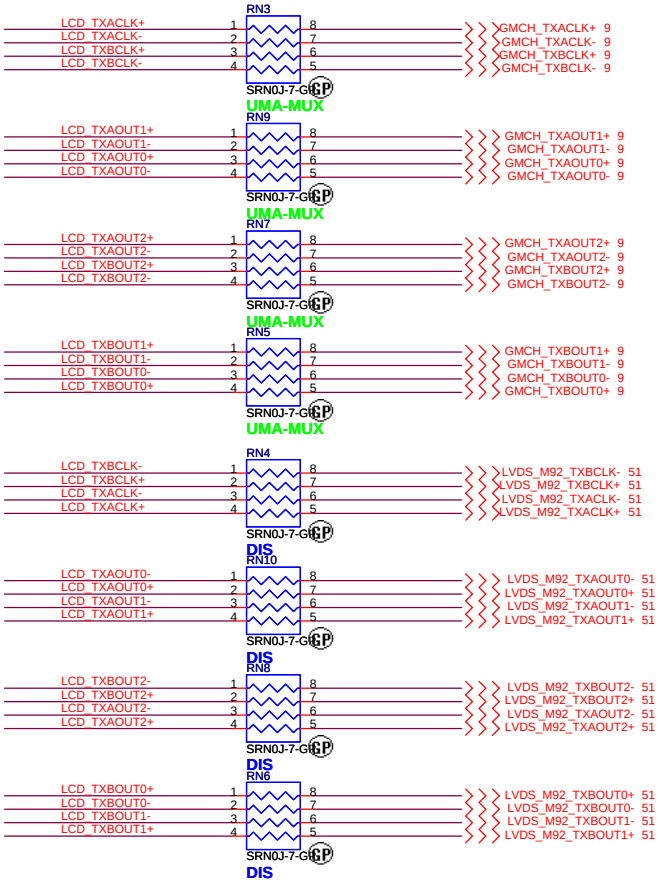
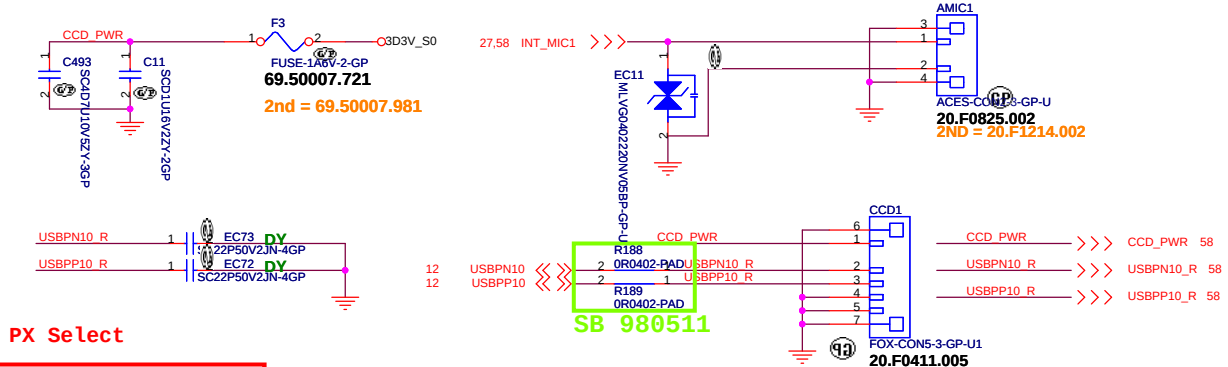
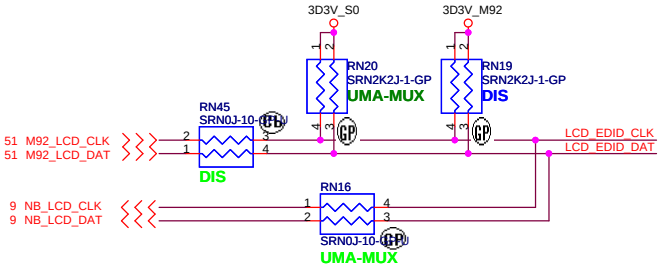
Title: DDR2 Socket_2		
Size	Document Number: SJV50-TR	Rev: -1
Date: Monday, June 29, 2009	Sheet 17 of 59	

LCD/CCD CONN

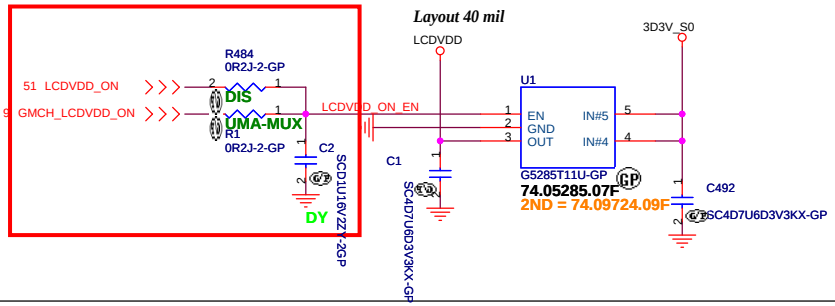


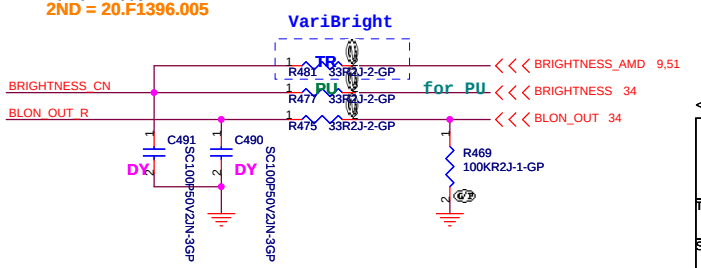






PX Select





<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: LED & LCD CONN / CCD

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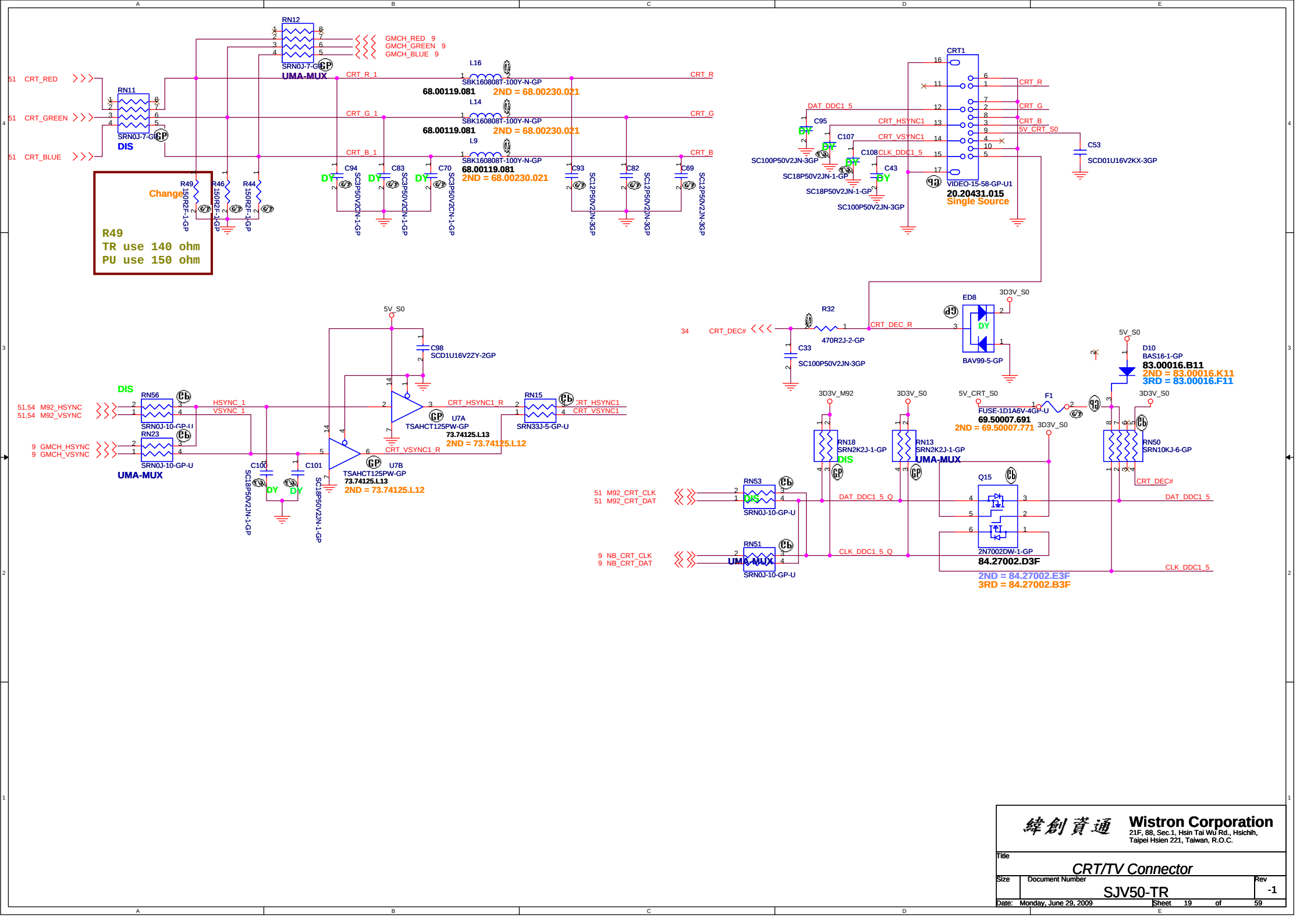

緯創資通	**Wistron Corporation**
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Title	*CRT/TV Connector*
Size	Document Number: SJV50-TR
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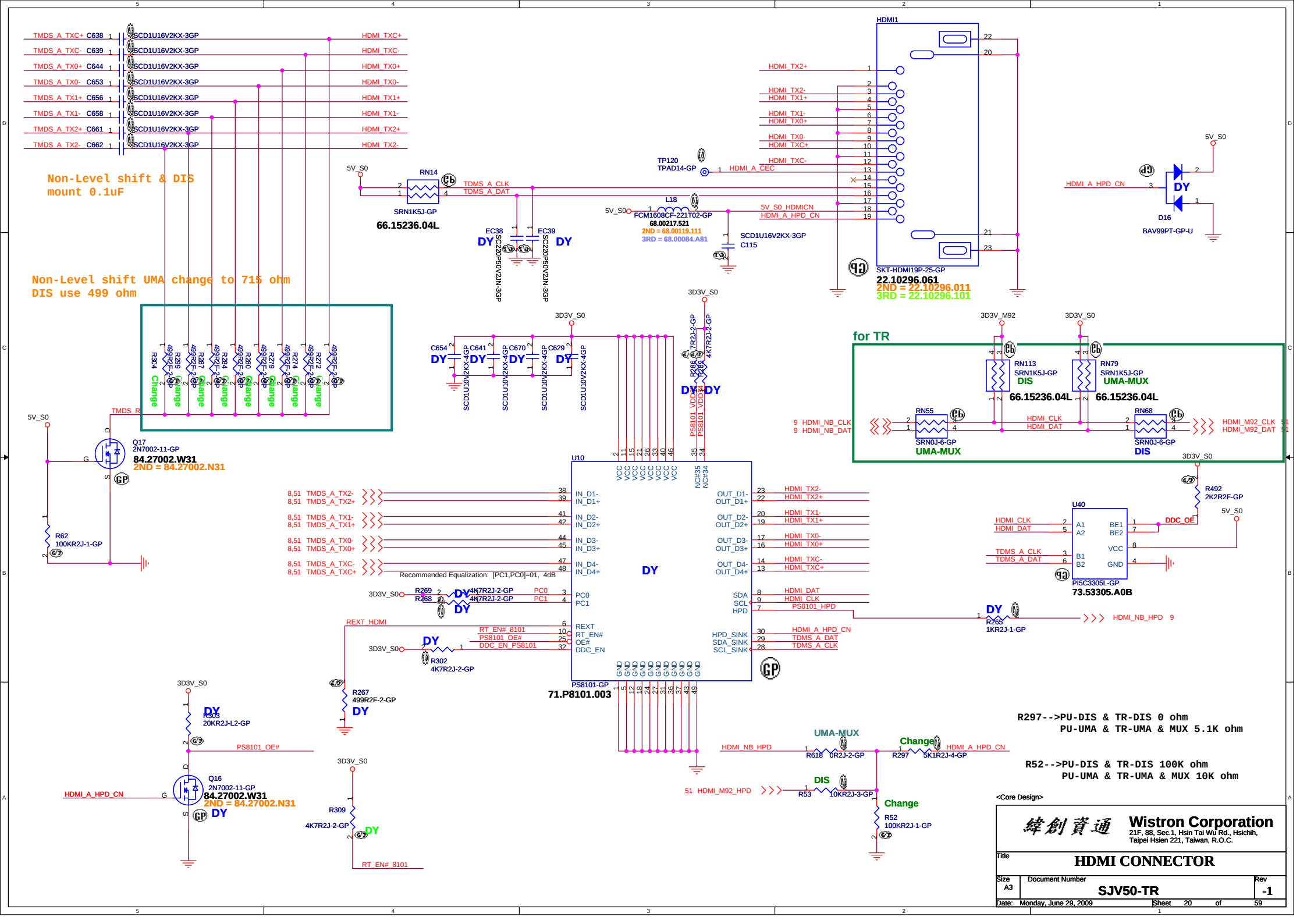
Non-Level shift & DIS mount 0.1uF
Non-Level shift UMA change to 715 ohm
DIS use 499 ohm
for TR
HDMI1
SKT-HDMI19P-25-GP
22.10296.061
2ND = 22.10296.011
3RD = 22.10296.101
RN14
SRN1K5J-GP
66.15236.04L
L18
FCM1608CF-221T02-GP
68.00217.521
2ND = 68.00119.111
3RD = 68.00084.A81
TP120
TPAD14-GP
D16
BAV99PT-GP-U
Q17
2N7002-11-GP
84.27002.W31
2ND = 84.27002.N31
Q16
2N7002-11-GP
84.27002.W31
2ND = 84.27002.N31
U10
PS8101-GP
71.P8101.003
RN113
SRN1K5J-GP
DIS
66.15236.04L
RN79
SRN1K5J-GP
UMA-MUX
66.15236.04L
RN55
SRN0J-6-GP
UMA-MUX
RN68
SRN0J-6-GP
DIS
U40
PI5C3305L-GP
73.53305.A0B
Recommended Equalization: [PC1,PC0]=01, 4dB
R297-->PU-DIS & TR-DIS 0 ohm
PU-UMA & TR-UMA & MUX 5.1K ohm
R52-->PU-DIS & TR-DIS 100K ohm
PU-UMA & TR-UMA & MUX 10K ohm
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
HDMI CONNECTOR
Size A3
Document Number
SJV50-TR
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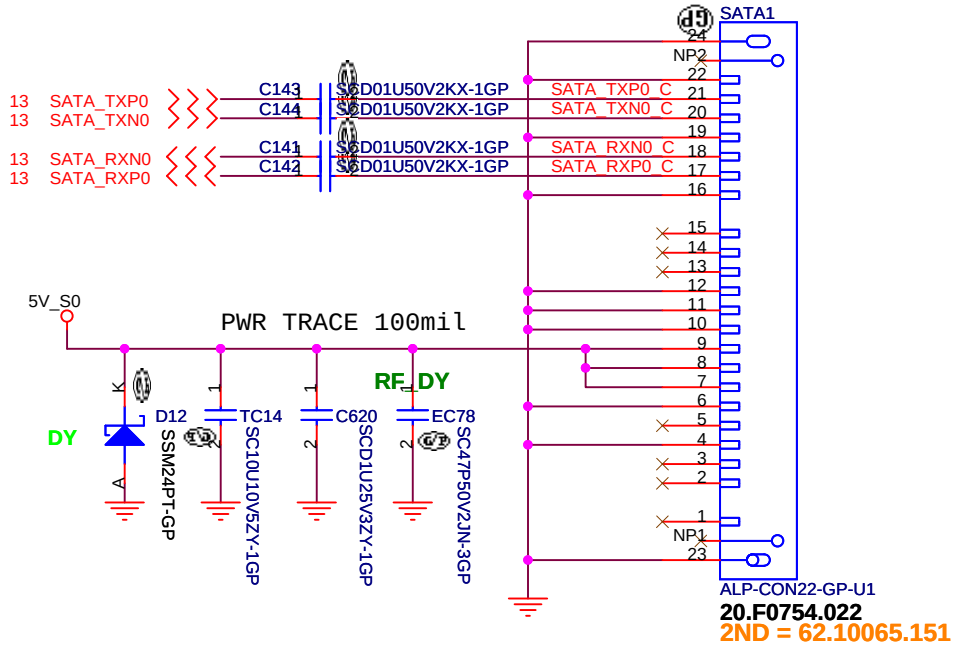
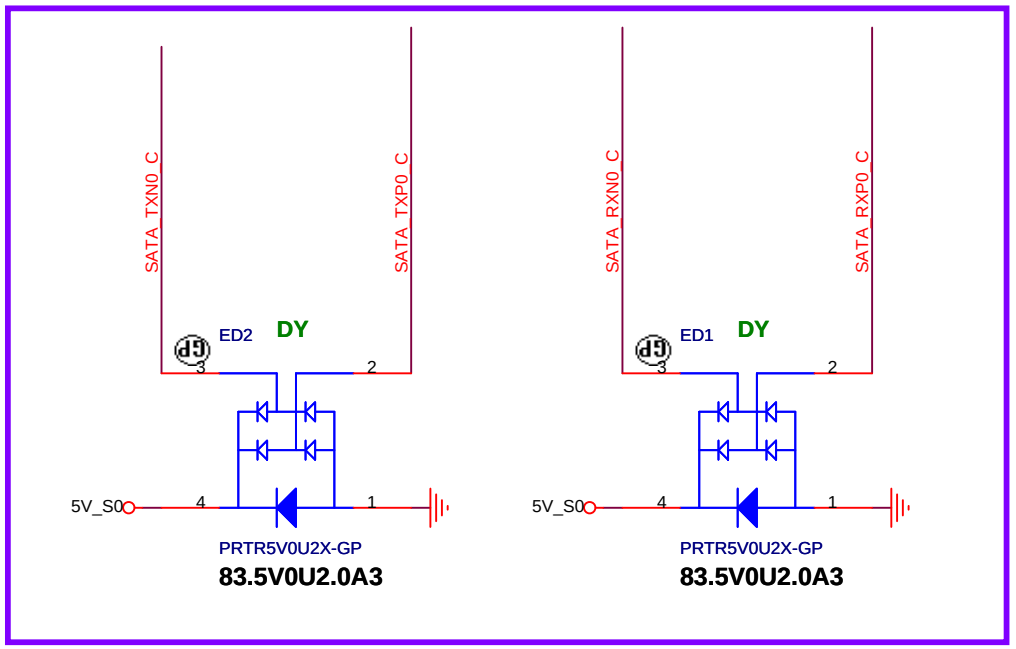
SATA HDD Connector





SA_20081112

<Core Design>

緯創資通 **Wistron Corporation**
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Title	***HDD***	
Size	Document Number **SJV50-TR**	Rev -1
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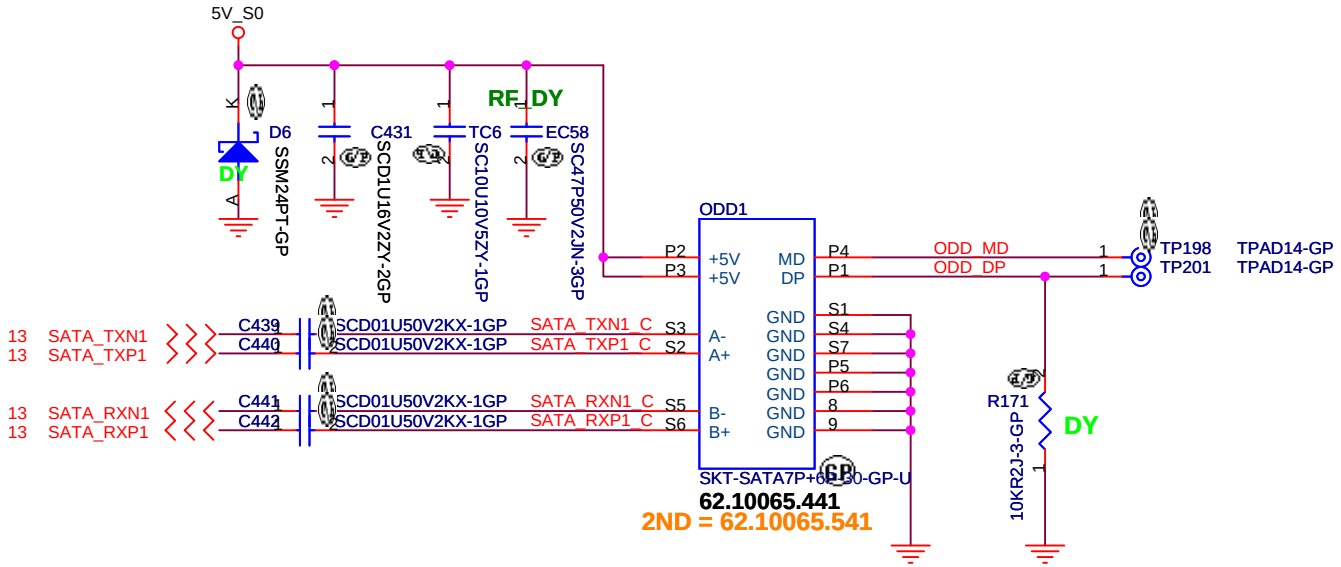
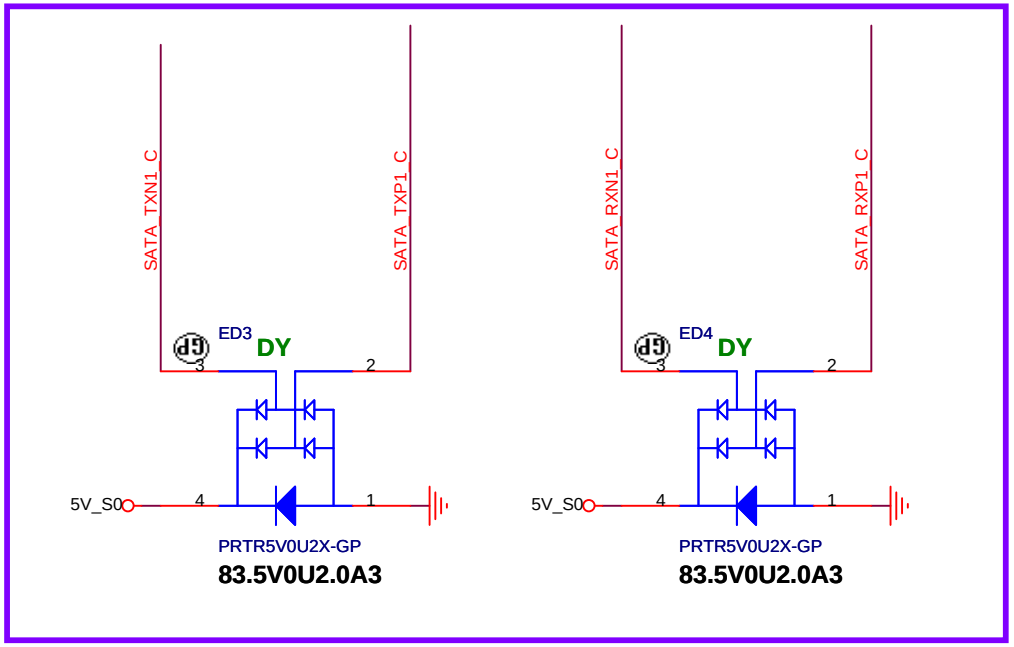
SATA ODD Connector





SA_20081112

<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ODD		
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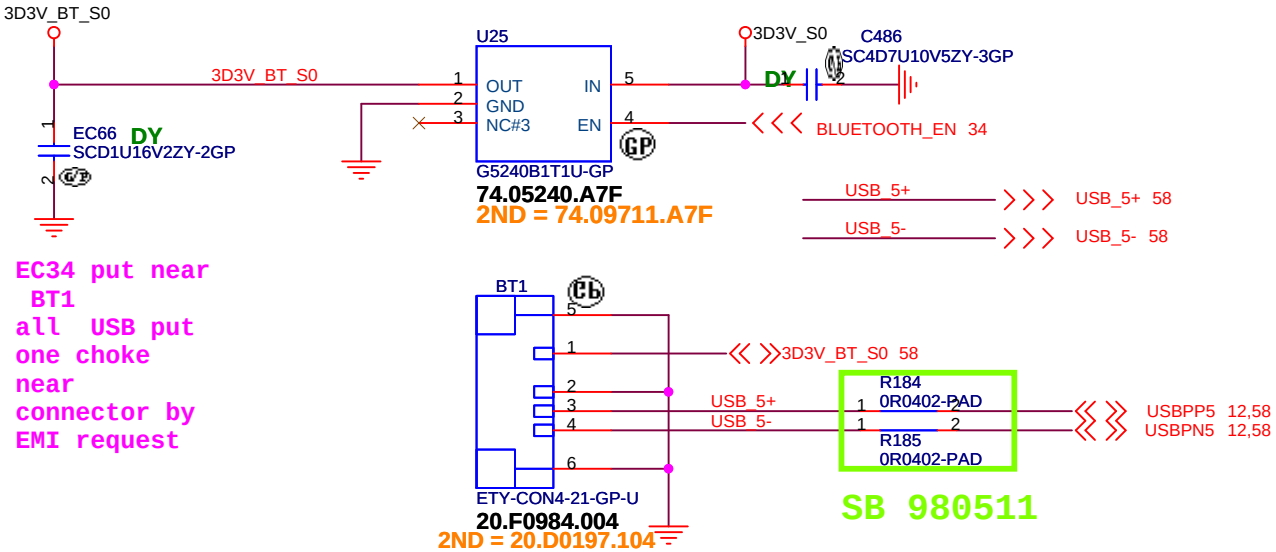
BLUETOOTH MODULE



<Core Design>

緯創資通 **Wistron Corporation**
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Title: ***BLUETOOTH***

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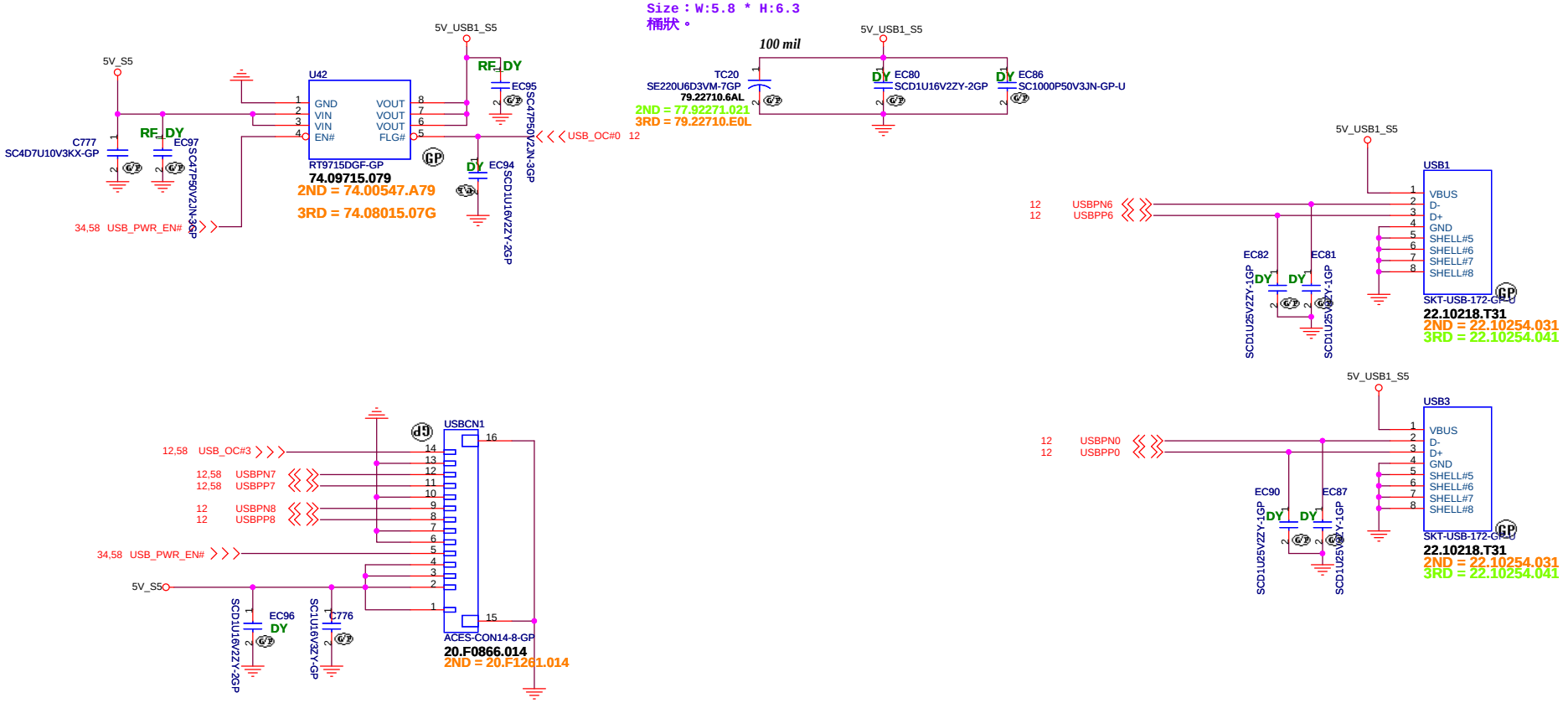

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB Connector

Size | Document Number: SJV50-TR | Rev: -1

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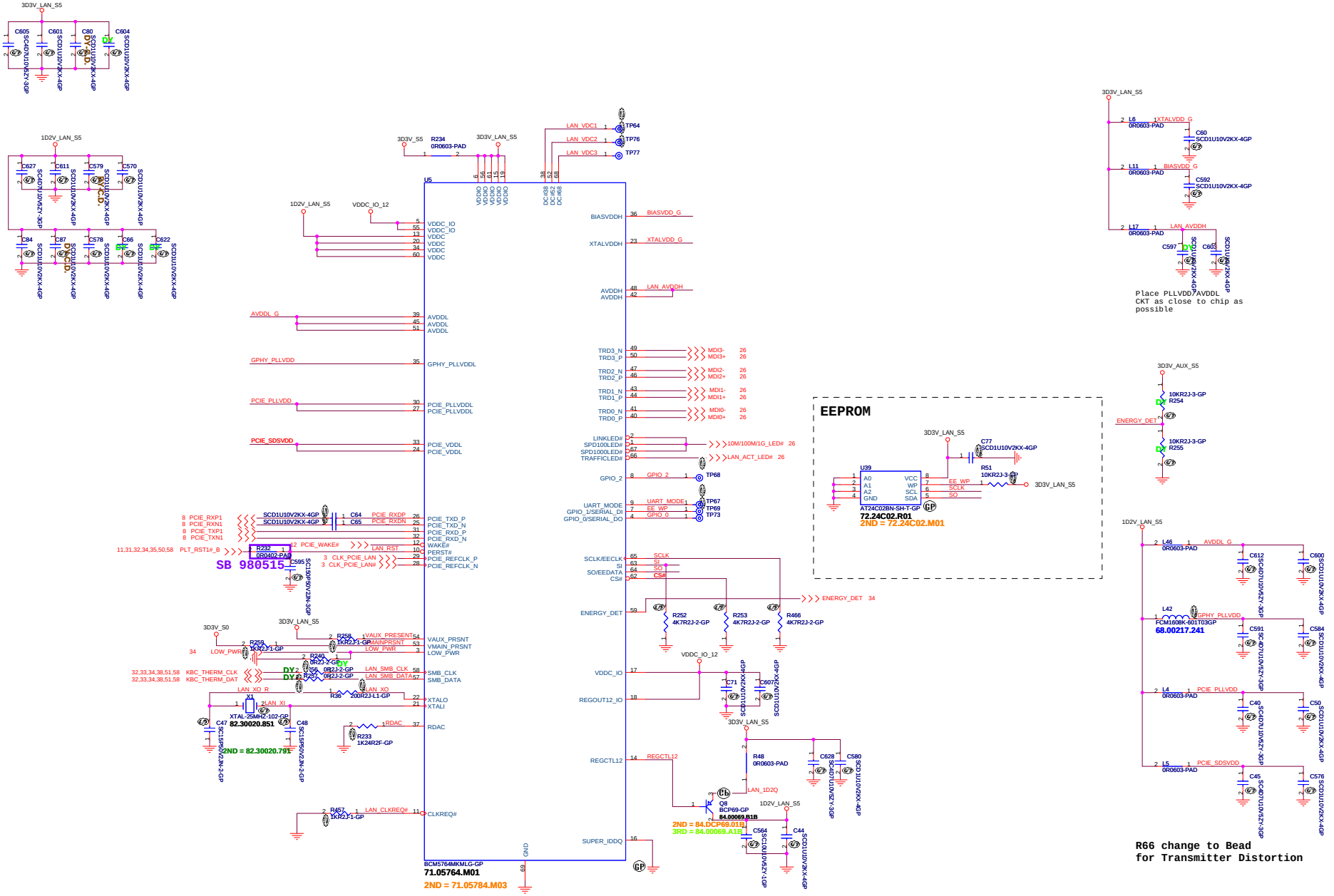

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BCM 5764

Size: A2 | Document Number: SJV50-TR | Rev: -1

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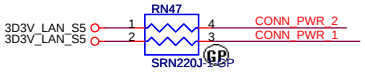
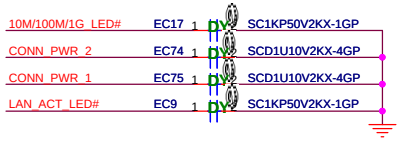
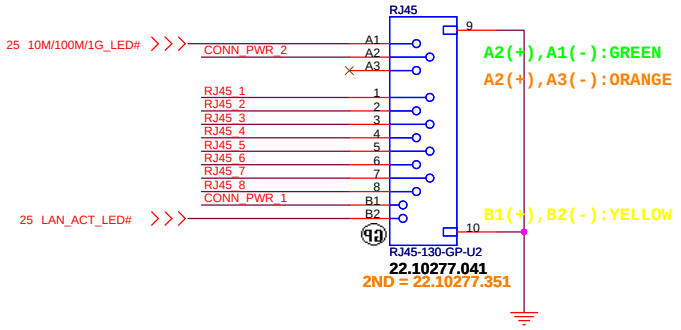
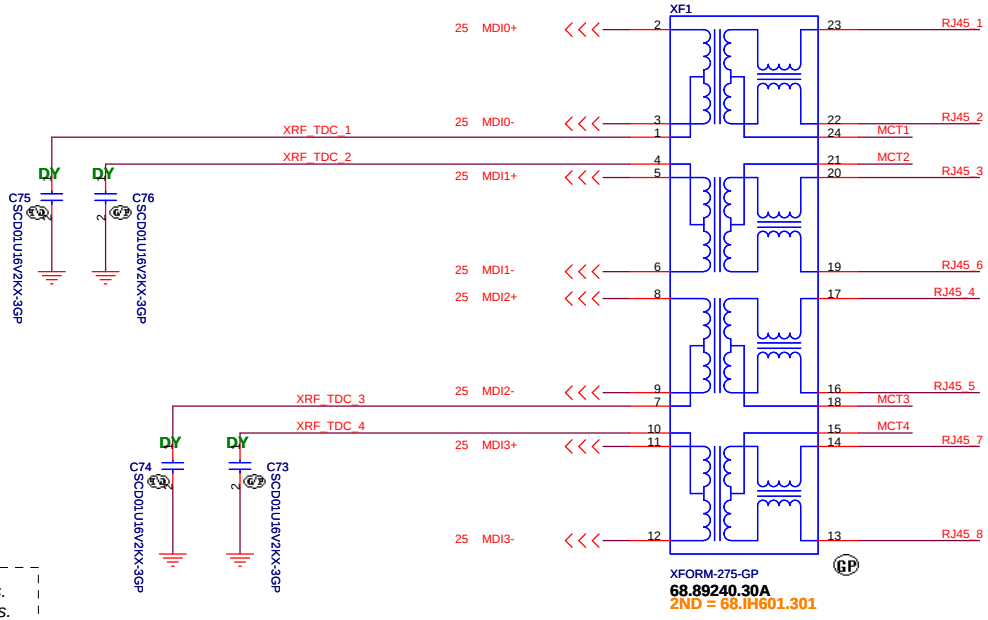
LAN Connector



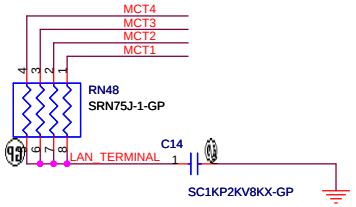




GIGA Lan Transformer



1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.



10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN Connector
Size: A3 | Document Number: SJV50-TR | Rev: -1
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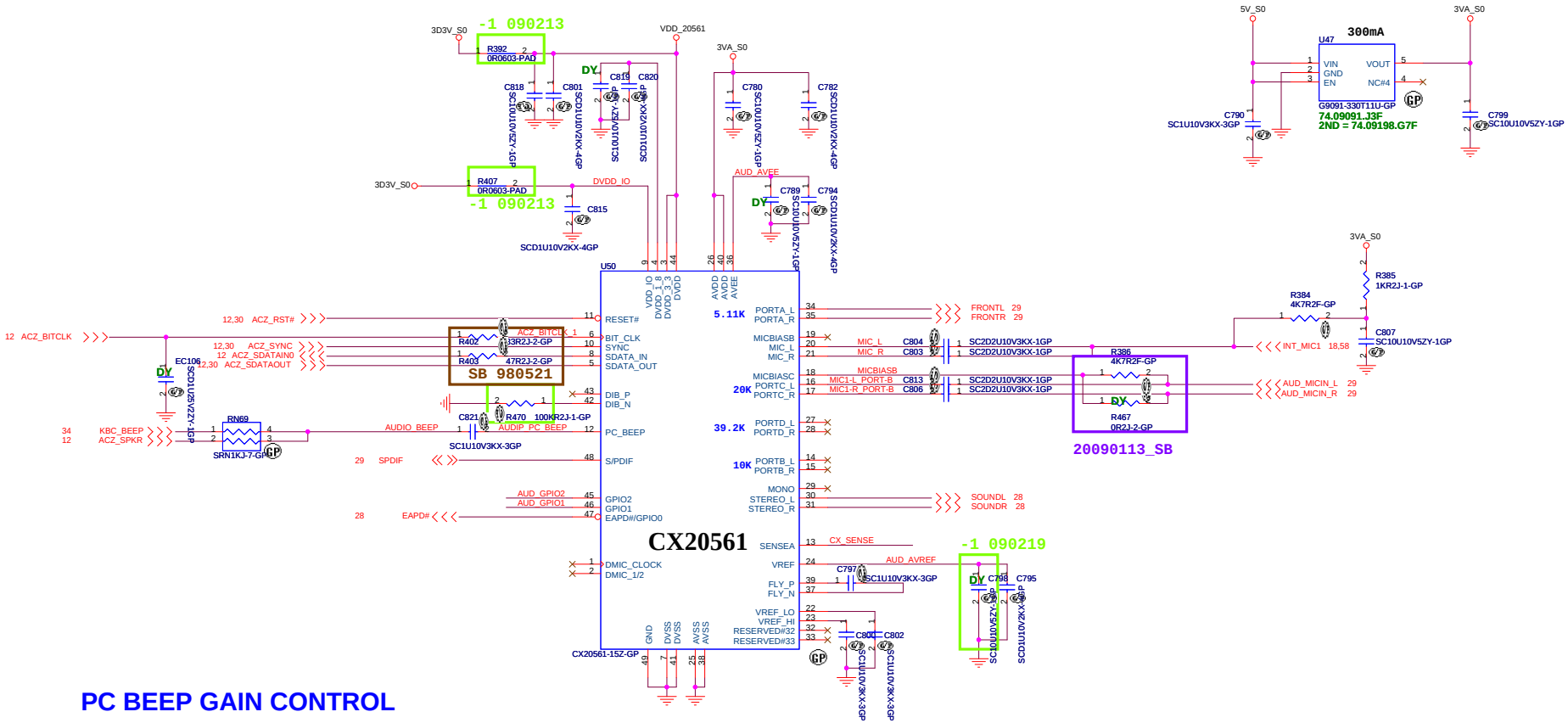
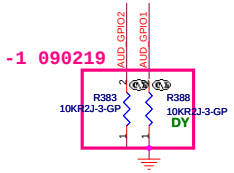
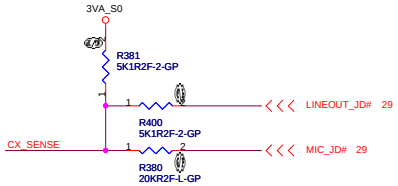


PC BEEP GAIN CONTROL



GAIN	10K GPIO RESISTORS	
	R388	R383
0dB	Populate	Populate
-6dB	Omit	Omit
-12dB	Populate	Omit
-18dB	Omit	Populate

Default gain is -6dB without populating the 10K-ohms pull-down resistors going to GPIO1 and GPIO2.



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AZALIA CODEC - CX20561

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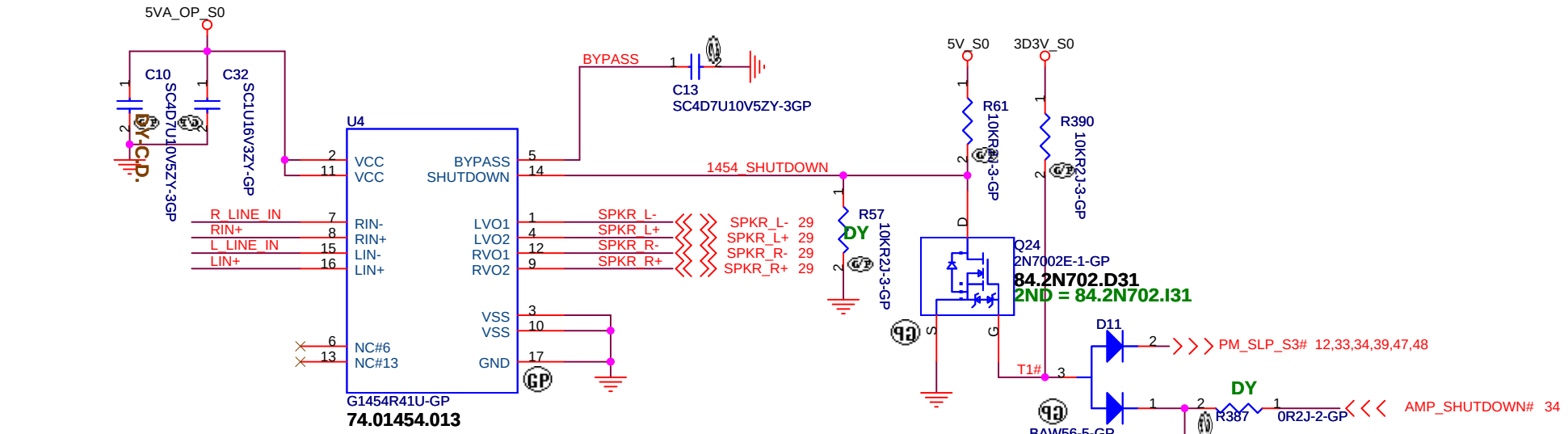
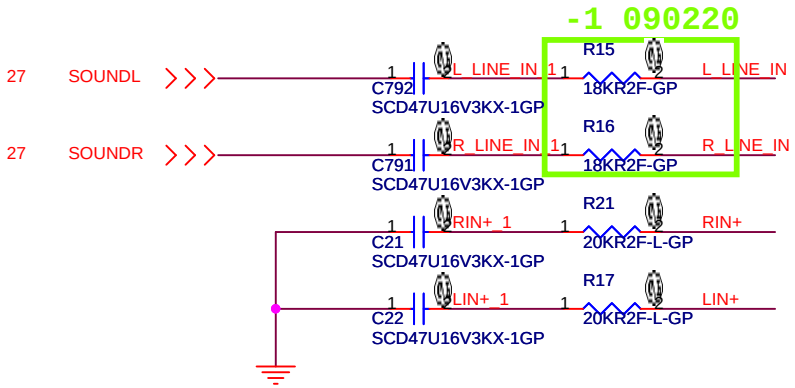
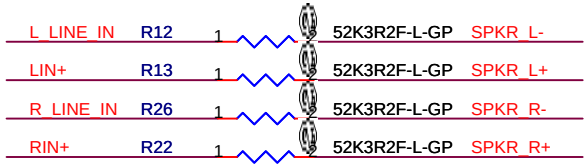
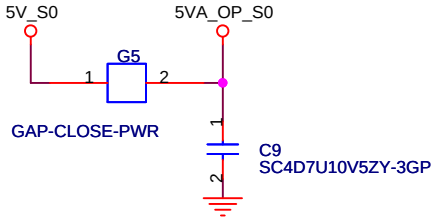
AUDIO OP AMPLIFIER









<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO AMP (G1454)**

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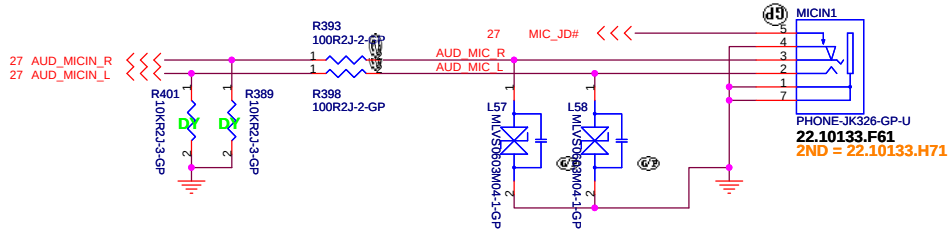
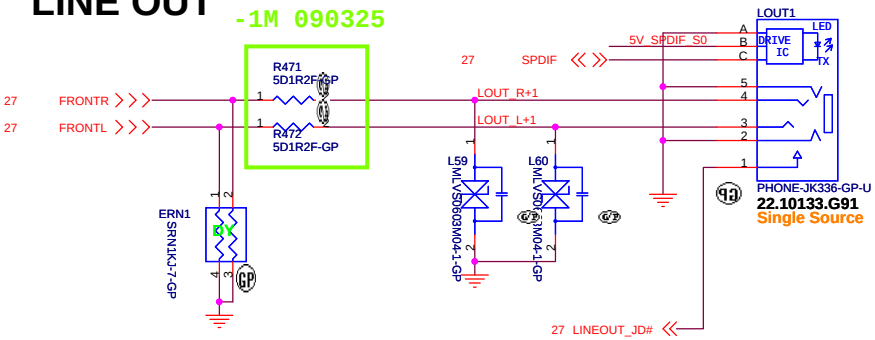
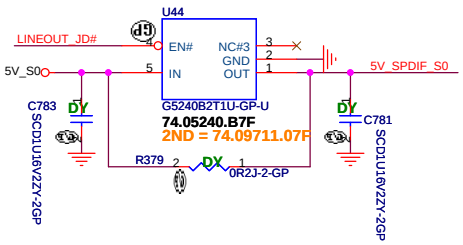
MIC IN



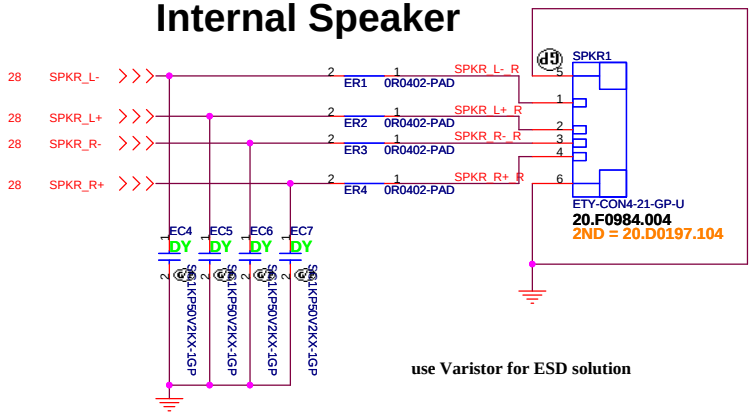
LINE OUT

-1M 090325





Internal Speaker



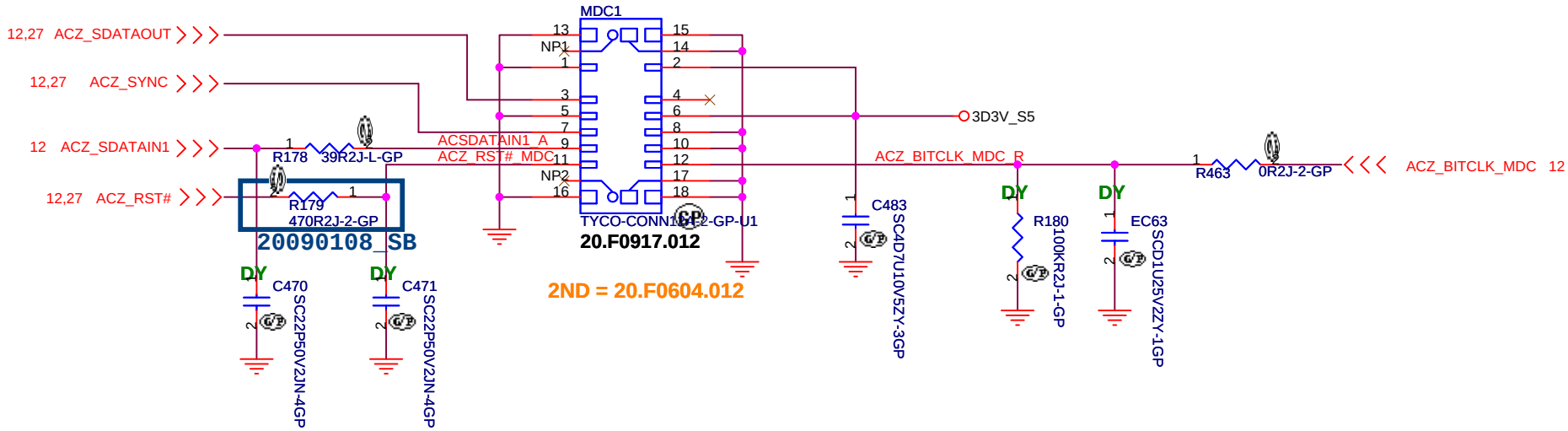
use Varistor for ESD solution

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

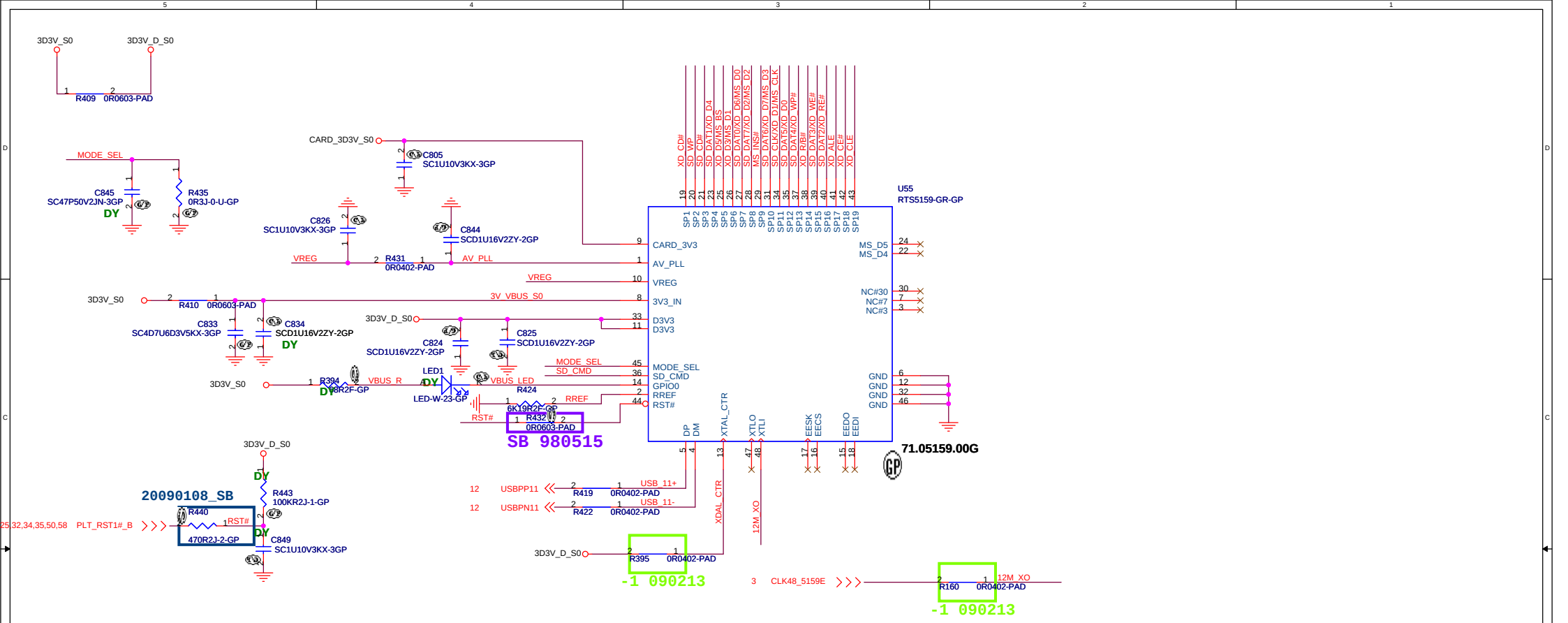
Title	Audio Jack	
Size	Document Number SJV50-TR	Rev -1
Date: Monday, June 29, 2009	Sheet 29 of 59	

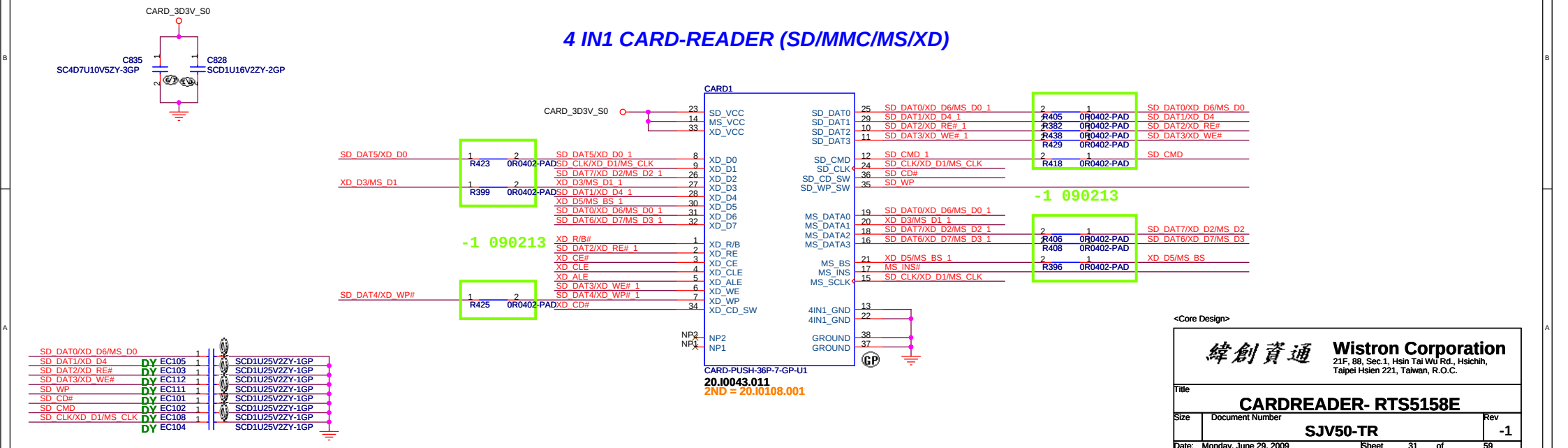
MDC 1.5 CONN



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***USB Connector***
Size	Document Number: **SJV50-TR** Rev: -1
Date: Monday, June 29, 2009	Sheet 30 of 59





<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

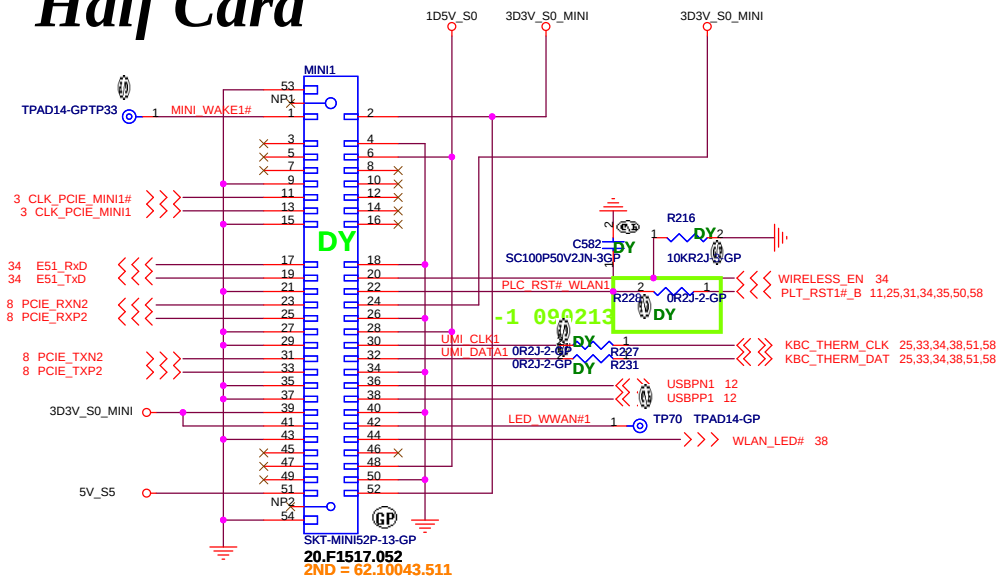
Title: CARDREADER- RTS5158E

Size | Document Number: SJV50-TR | Rev: -1

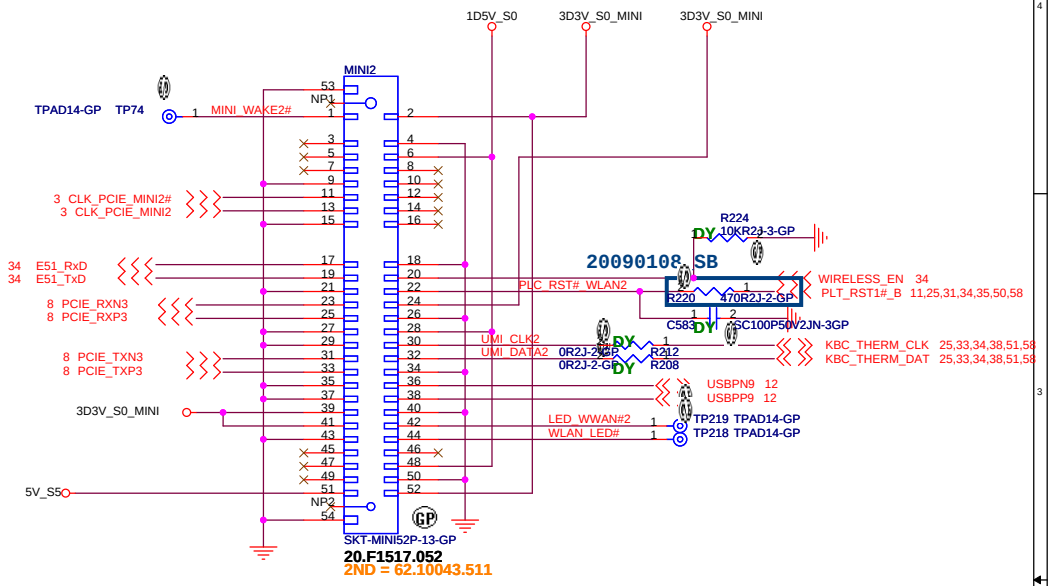
Date: Monday, June 29, 2009 | Sheet 31 of 59

Mini Card Connector

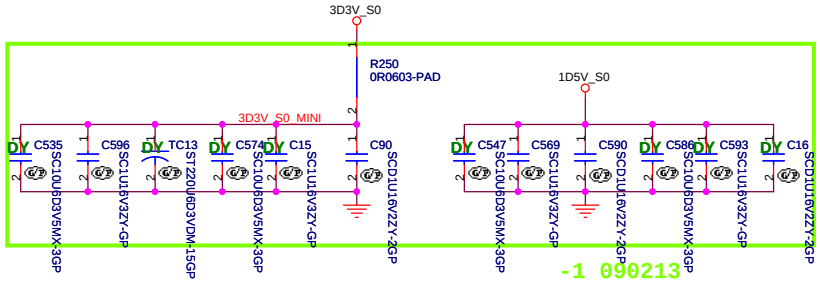
Half Card



Symbol use 62.10043.461

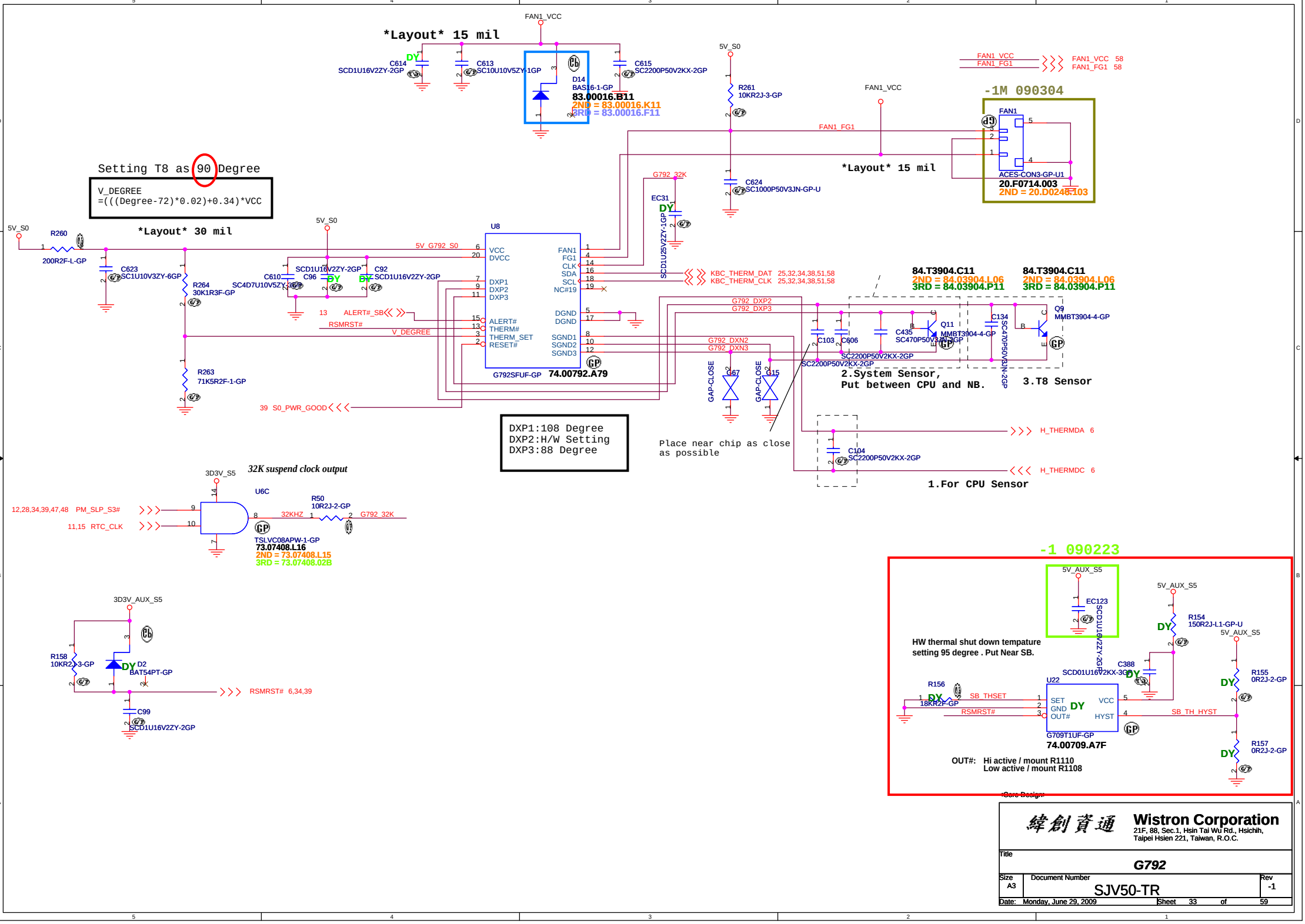


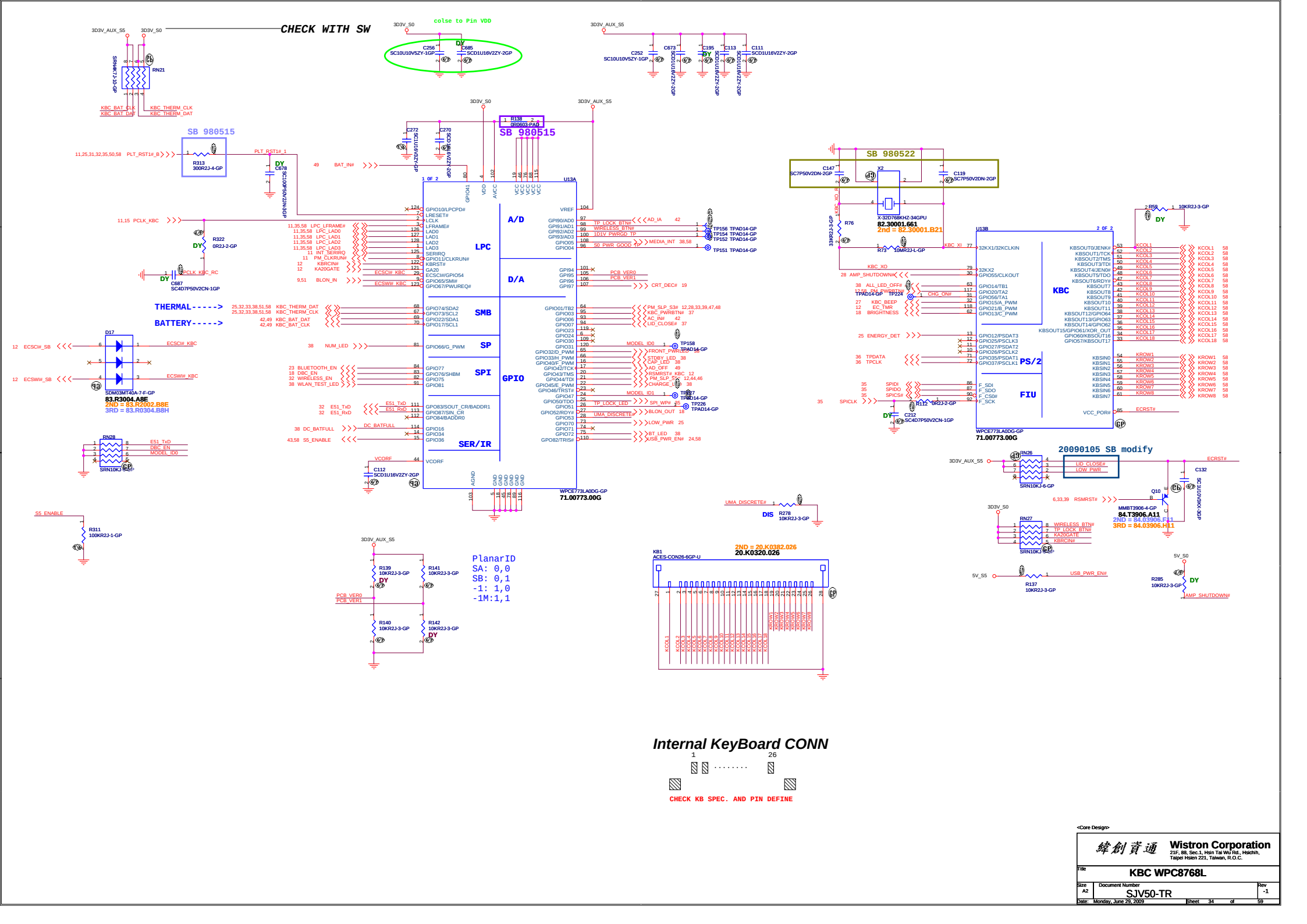
Symbol use 62.10043.461

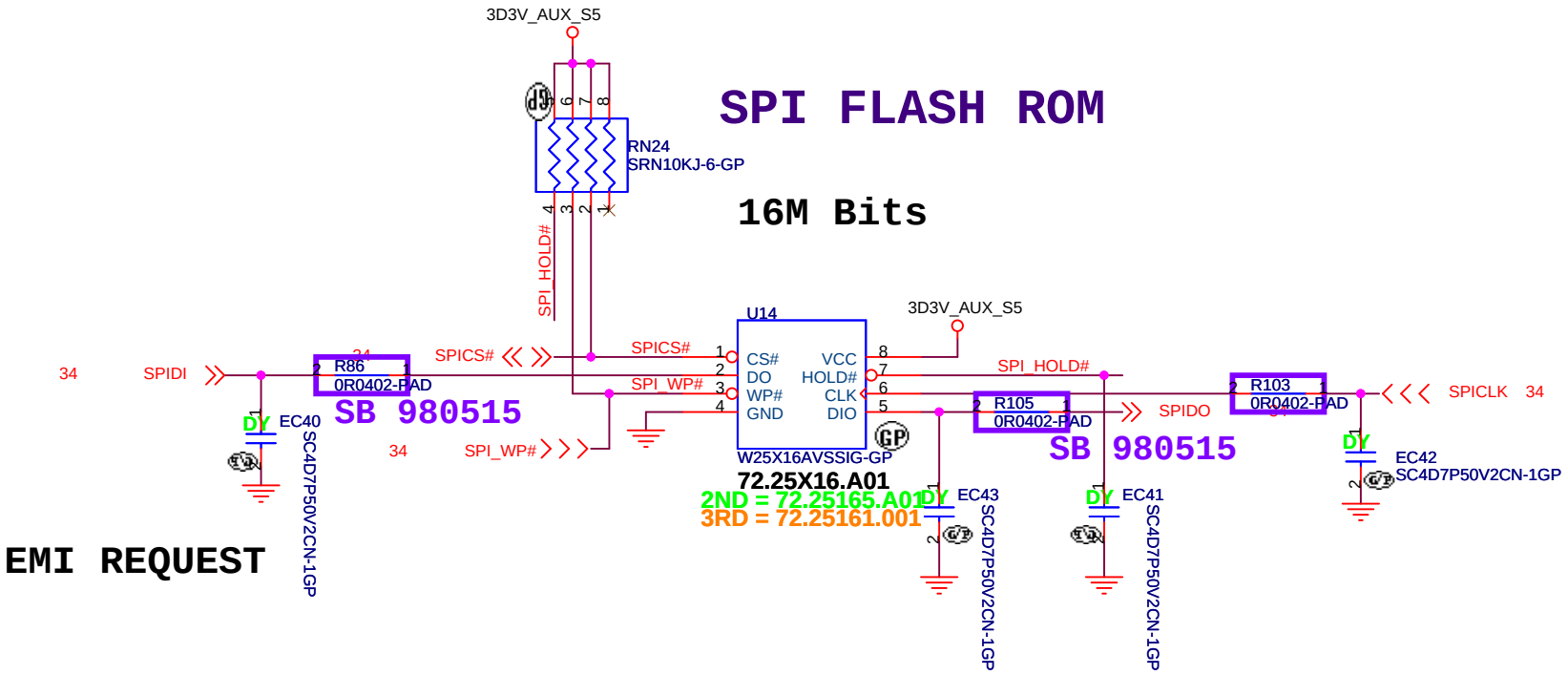


<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MINI CARD		
Size	Document Number: SJV50-TR	Rev: -1
Date: Monday, June 29, 2009	Sheet 32 of 59	

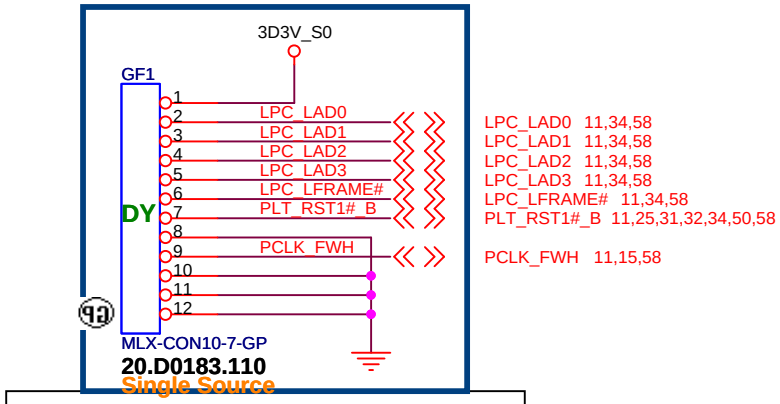

Layout 15 mil
FAN1_VCC
C614 SCD1U16V2ZY-2GP
C613 SC10U10V5ZY-1GP
C615 SC2200P50V2KX-2GP
D14 BAS16-1-GP
83.00016.B11
2ND = 83.00016.K11
3RD = 83.00016.F11
5V_S0
R261 10KR2J-3-GP
FAN1_VCC 58
FAN1_FG1 58
-1M 090304
FAN1
ACES-CON3-GP-U1
20.F0714.003
2ND = 20.D0246.003
FAN1_FG1
Layout 15 mil
C624 SC1000P50V3JN-GP-U
G792_32K
EC31 SCD1U25V2ZY-1GP
Setting T8 as 90 Degree
V_DEGREE
=(((Degree-72)*0.02)+0.34)*VCC
Layout 30 mil
5V_S0
R260 200R2F-L-GP
C623 SC1U10V3ZY-6GP
R264 30K1R3F-GP
R263 71K5R2F-1-GP
C610 SCD1U16V2ZY-2GP
C96 SC4D7U10V5ZY-1GP
C92 SCD1U16V2ZY-2GP
5V_G792_S0
U8
VCC
DVCC
DXP1
DXP2
DXP3
ALERT#
THERM#
THERM_SET
RESET#
FAN1
FG1
CLK
SDA
SCL
NC#19
DGND
DGND
SGND1
SGND2
SGND3
G792SFUF-GP
74.00792.A79
13 ALERT#_SB
RSMRST#
V_DEGREE
39 S0_PWR_GOOD
KBC_THERM_DAT 25,32,34,38,51,58
KBC_THERM_CLK 25,32,34,38,51,58
84.T3904.C11
2ND = 84.03904.L06
3RD = 84.03904.P11
84.T3904.C11
2ND = 84.03904.L06
3RD = 84.03904.P11
G792_DXP2
G792_DXP3
G792_DXN2
G792_DXN3
C103
C606
C435 SC470P50V3JN-2GP
Q11 MMBT3904-4-GP
C134 SC470P50V3JN-2GP
Q9 MMBT3904-4-GP
SC2200P50V2KX-2GP
SC2200P50V2KX-2GP
GAP-CLOSE
G67
GAP-CLOSE
C15
2.System Sensor,
Put between CPU and NB.
3.T8 Sensor
DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree
Place near chip as close as possible
H_THERMDA 6
C104 SC2200P50V2KX-2GP
H_THERMDC 6
1.For CPU Sensor
3D3V_S5
32K suspend clock output
U6C
12,28,34,39,47,48 PM_SLP_S3#
11,15 RTC_CLK
R50 10R2J-2-GP
32KHZ
G792_32K
TSLVC08APW-1-GP
73.07408.L16
2ND = 73.07408.L15
3RD = 73.07408.02B
3D3V_AUX_S5
R158 10KR2J-3-GP
D2 BAT54PT-GP
RSMRST# 6,34,39
C99 SCD1U16V2ZY-2GP
-1 090223
5V_AUX_S5
EC123 SCD1U16V2ZY-2GP
HW thermal shut down tempature setting 95 degree . Put Near SB.
R156 18KR2F-GP
SB_THSET
RSMRST#
U22
SET
GND
OUT#
VCC
HYST
G709T1UF-GP
74.00709.A7F
C388 SCD01U16V2KX-3GP
R154 150R2J-L1-GP-U
R155 0R2J-2-GP
R157 0R2J-2-GP
SB_TH_HYST
OUT#: Hi active / mount R1110
Low active / mount R1108
Core Design
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
G792
Size A3
Document Number
SJV50-TR
Rev -1
Date: Monday, June 29, 2009
Sheet 33 of 59


CHECK WITH SW
colse to Pin VDD
SB 980515
SB 980522
U13A
U13B
WPCE773LA0DG-GP
71.00773.00G
A/D
D/A
LPC
SMB
SP
SPI
GPIO
SER/IR
KBC
PS/2
FIU
THERMAL----->
BATTERY----->
20090105 SB modify
PlanarID
SA: 0,0
SB: 0,1
-1: 1,0
-1M:1,1
Internal KeyBoard CONN
CHECK KB SPEC. AND PIN DEFINE
Wistron Corporation
KBC WPC8768L
SJV50-TR



Connector FOR DEBUG BOARD

20081219



LPC_LAD0 11,34,58
LPC_LAD1 11,34,58
LPC_LAD2 11,34,58
LPC_LAD3 11,34,58
LPC_LFRAME# 11,34,58
PLT_RST1#_B 11,25,31,32,34,50,58

PCLK_FWH 11,15,58

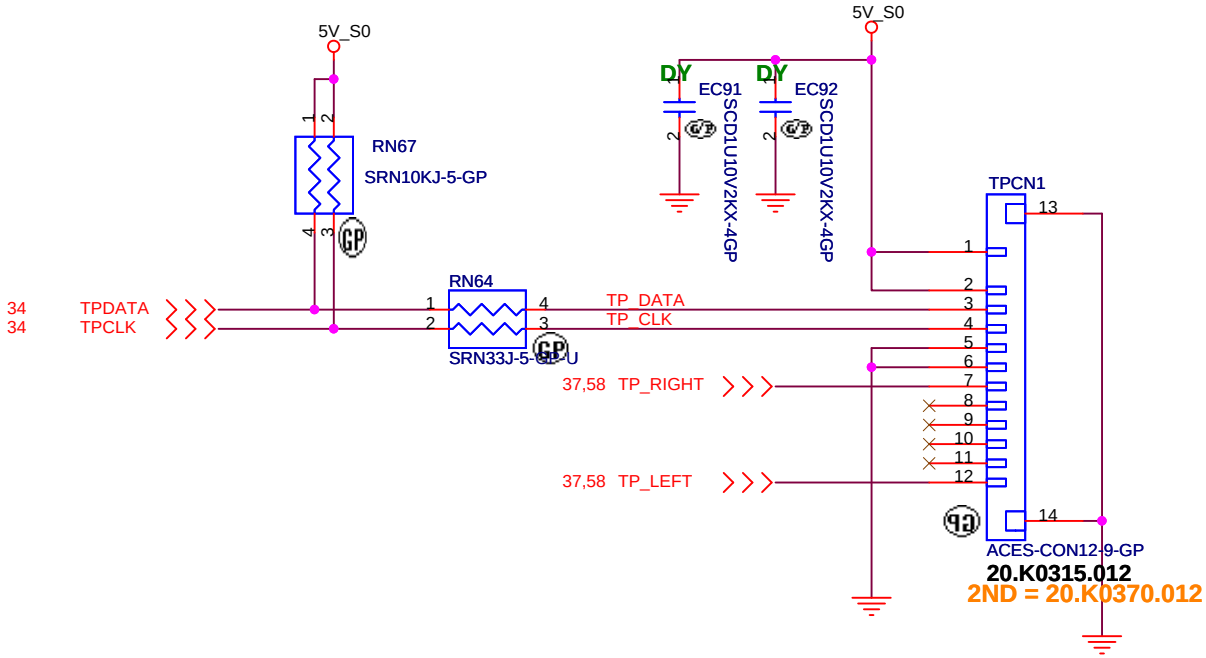
Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46

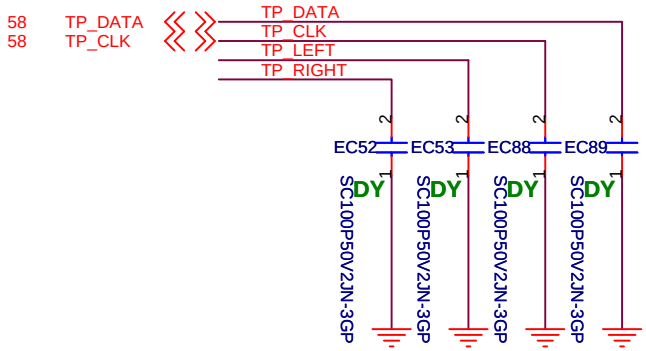
<Core Design>

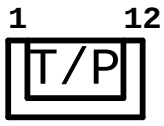
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BIOS		
Size: A4	Document Number: SJV50-TR	Rev: -1
Date: Monday, June 29, 2009	Sheet 35 of 59	

TOUCH PAD





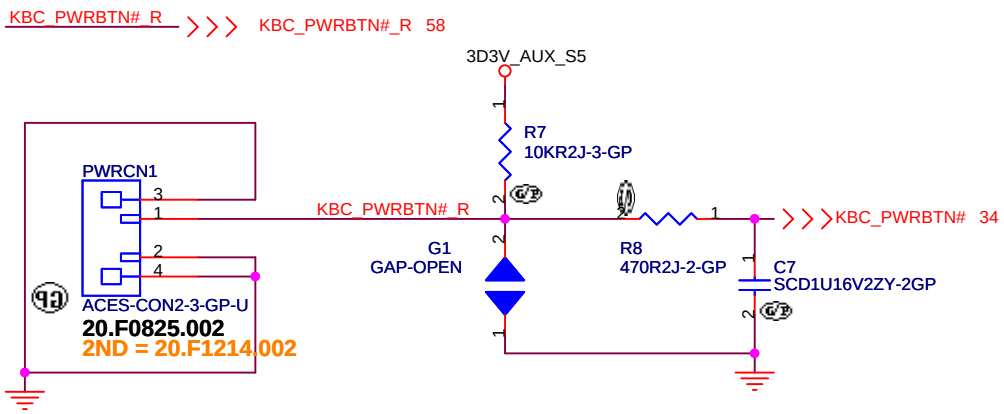


<Core Design>

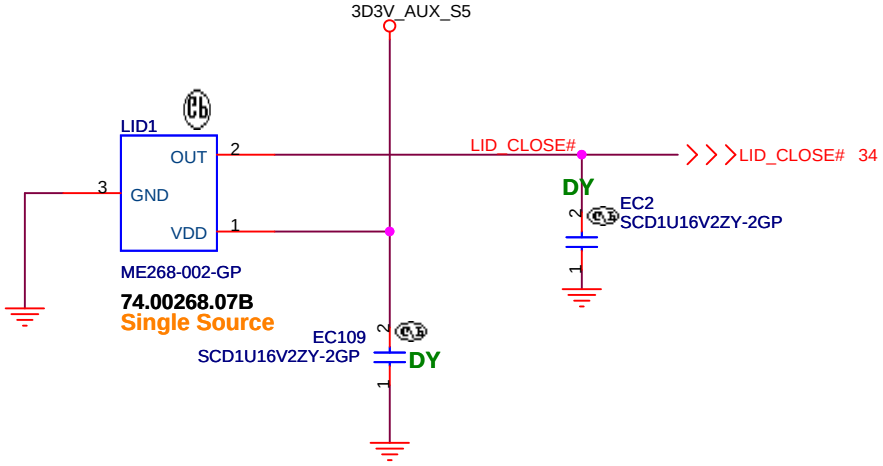
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***TouchPad***		
Size	Document Number: **SJV50-TR**	Rev: -1
Date: Monday, June 29, 2009	Sheet 36 of 59	

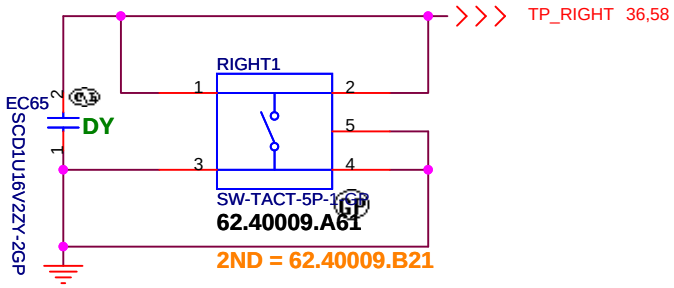
Power Button Board



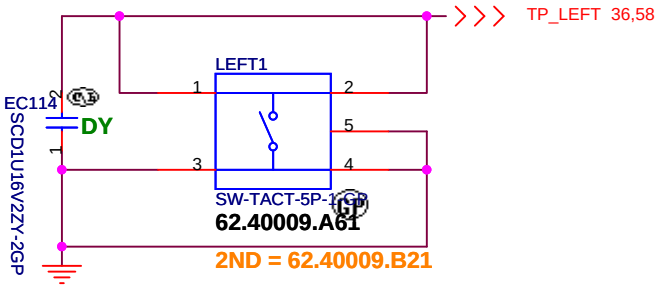
Cover Up Switch



RIGHT



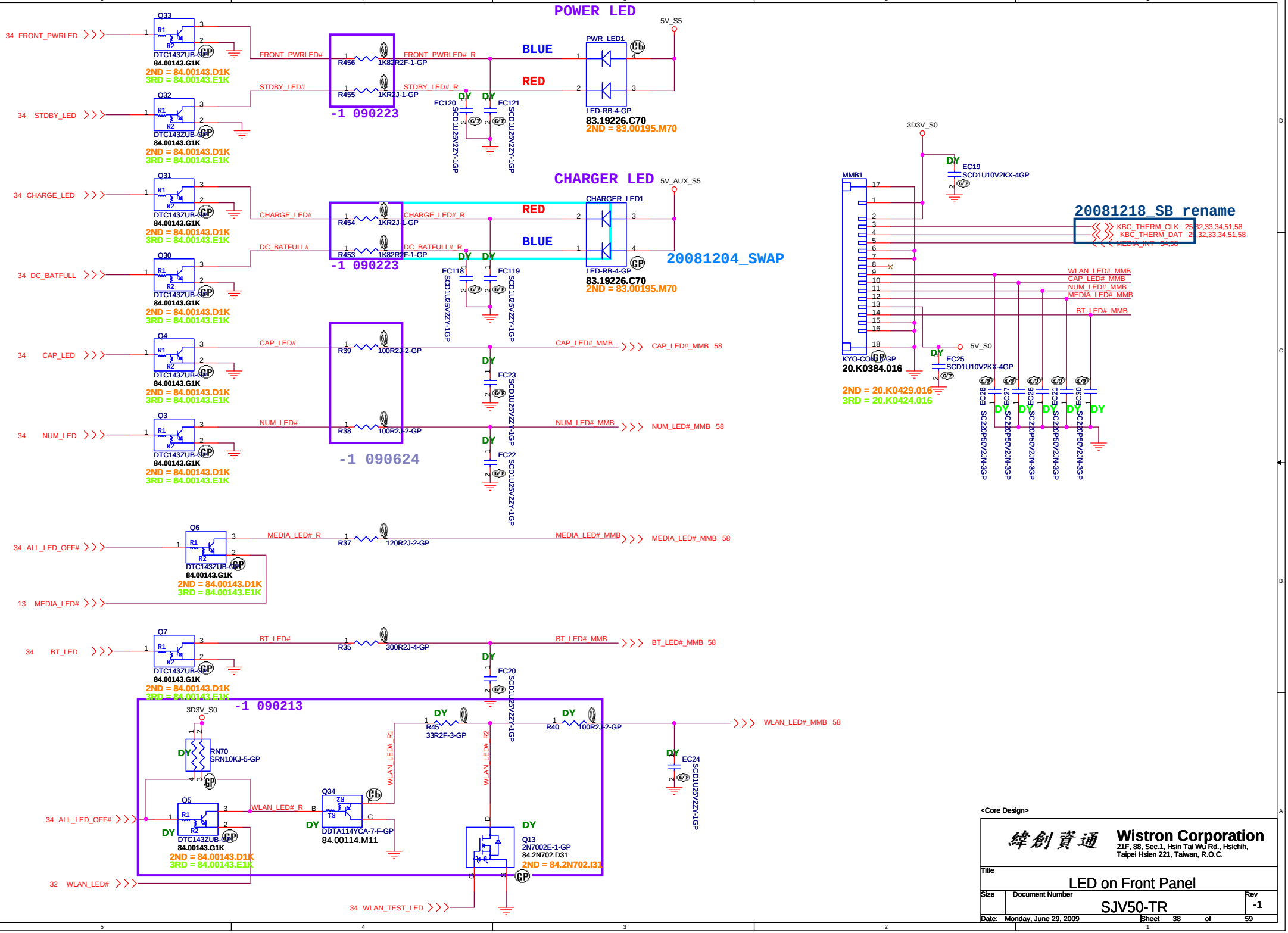
LEFT



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Switchs*		
Size	Document Number: SJV50-TR	Rev: -1
Date: Monday, June 29, 2009	Sheet 37 of 59	


POWER LED
CHARGER LED
20081204_SWAP
20081218_SB_rename
-1 090223
-1 090624
-1 090213
BLUE
RED
34 FRONT_PWRLED
34 STDBY_LED
34 CHARGE_LED
34 DC_BATFULL
34 CAP_LED
34 NUM_LED
34 ALL_LED_OFF#
13 MEDIA_LED#
34 BT_LED
32 WLAN_LED#
34 WLAN_TEST_LED
FRONT_PWRLED#
STDBY_LED#
CHARGE_LED#
DC_BATFULL#
CAP_LED#
NUM_LED#
MEDIA_LED# R
BT_LED#
WLAN_LED# R
FRONT_PWRLED# R
STDBY_LED# R
CHARGE_LED# R
DC_BATFULL# R
CAP_LED# MMB 58
NUM_LED# MMB 58
MEDIA_LED# MMB 58
BT_LED# MMB 58
WLAN_LED# MMB 58
5V_S5
5V_AUX_S5
3D3V_S0
5V_S0
PWR_LED1
CHARGER_LED1
LED-RB-4-GP
83.19226.C70
2ND = 83.00195.M70
DTC143ZUB-GP
84.00143.G1K
2ND = 84.00143.D1K
3RD = 84.00143.E1K
1K82R2F-1-GP
1KR2J-1-GP
100R2J-2-GP
120R2J-2-GP
300R2J-4-GP
33R2F-3-GP
SRN10KJ-5-GP
DDTA114YCA-7-F-GP
84.00114.M11
2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.I31
SCD1U25V2ZY-1GP
SCD1U10V2KX-4GP
SC220P50V2JN-3GP
MMB1
KYO-CONN-GP
20.K0384.016
2ND = 20.K0429.016
3RD = 20.K0424.016
KBC_THERM_CLK 25,32,33,34,51,58
KBC_THERM_DAT 25,32,33,34,51,58
WLAN_LED# MMB
CAP_LED# MMB
NUM_LED# MMB
MEDIA_LED# MMB
BT_LED# MMB
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
LED on Front Panel
Size
Document Number
SJV50-TR
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-1
Date: Monday, June 29, 2009
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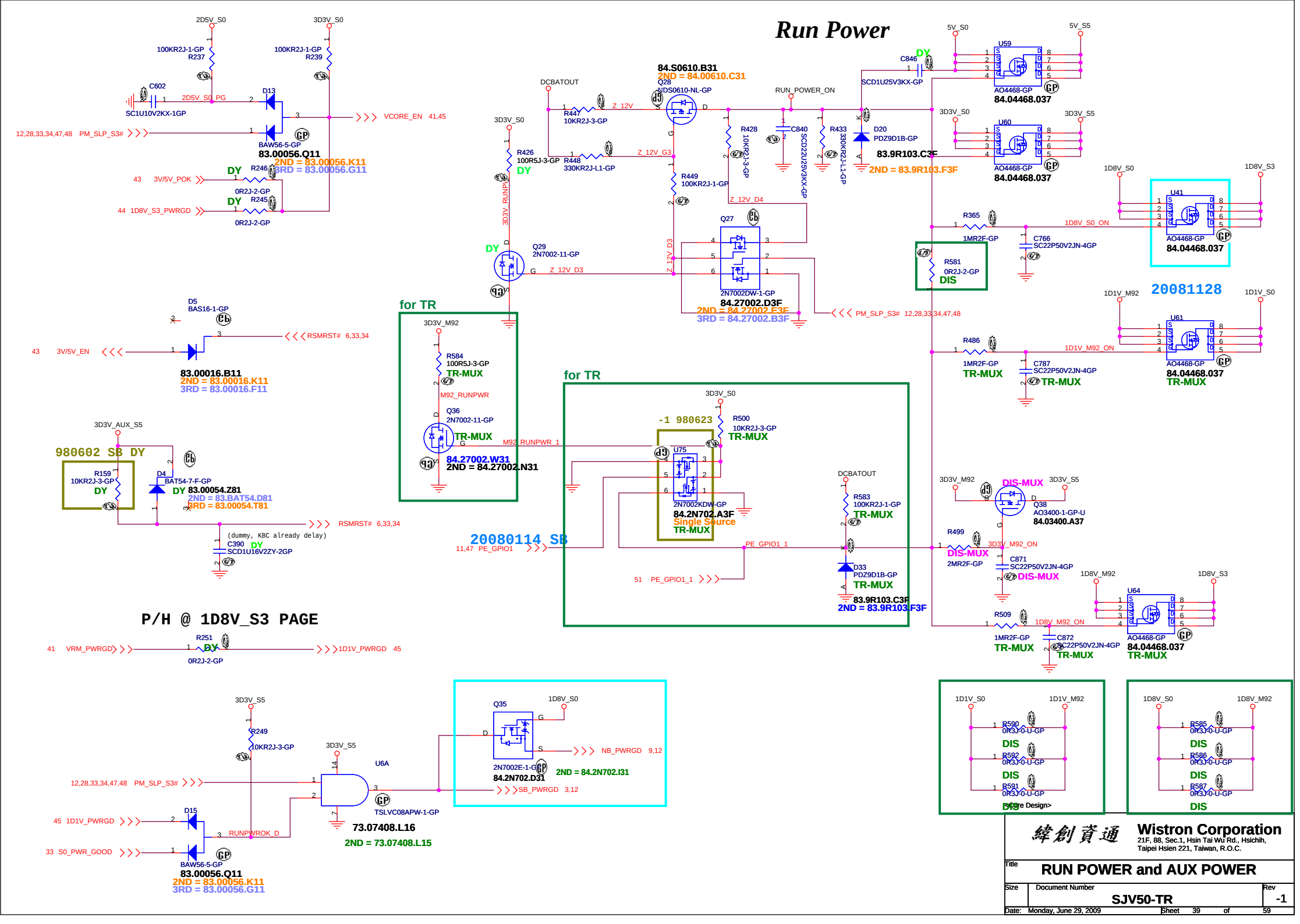
Run Power



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **RUN POWER and AUX POWER**

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	SJV50-TR	-1

Date: Monday, June 29, 2009 Sheet 39 of 59

CPU_CORE
ISL6264

VID0
VID1
VID2
VID3
VID4
VID5

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)

Output Signal
VROK()

MAX8760_VRM

Output Power
VCC_CORE_PWR(O)

VCC_CORE_S0(Imax=35A)

VCORE_EN

Input Signal
EN (I / 3.3V)

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

COREFB
COREFB#

Input Power
VCC(I)
VCC(I)
VCC(I)

DCBATOUT
5V_S0
3D3V_S0

TI TPS51125
3D3V/5V

Input Signal
51120_EN2 FOR 3.3V
51120_EN1 FOR 5.0V
VIN

Output Signal
PGOUT(OD / 5V)

Pull High (3D3V)

DCBATOUT_51120

Input Power
VIN
REG5V_IN(I / 5V)

DCBATOUT_51120

Output Power
5V(O)
3D3V(O)

5V_AUX_S5
3D3V_AUX_S5
5V_S5 (5.4A)
3D3V_S5 (4A)

1D5V_S0

3D3V_S0 → INPUT / OUT → 1D5V_S0

G957

1D2V_S5

3D3V_S5 → INPUT / OUT → 1D2V_S5

G9091

2D5V_S0

3D3V_S0 → INPUT / OUT → 2D5V_S0

G9091

0D9V_S3

5V_S5 → INPUT / OUT → 0D9V_S3

RT9026

Adapter

AD_OFF
AD_JK
5V_AUX_S5

Input Signal
(I)

Output Signal
(O)

AD_IN

Input Power
VCC(I)
VCC(I)

Output Power
VCC(O)

AD+

Charger_MAX8731

CHARGE_OFF
BT_TH
BAT+SENSE
BT_SCL_5
BT_SDA_5
FLASH_GPIO1
FLASH_GPIO2
AC_IN

AD+

Input Signal
CLS (I / 3.3V)
THM (I / 3.3V)
BATT (I / 3.3V)
SCL (IO / 5V)
SDA (IO / 5V)
RESET#/PB5 (I/5V)
PB0/MOSI/AIN0
PB0/MOSI/AIN0

Output Signal
LDO (O / 5.4V)
XTAL2/PB4 (O/5V)
XTAL1/PB3 (O/5V)

AD_IN
CHARGE_LED#
BL2#

Input Power
DCIN (I)

Output Power
VCC (O)
VCC (O)

DCBATOUT
BT+

TI TPS51124
1.8V / 1.2V

PM_SLP_S5#

Input Signal
S5
S3

Output Signal
PGOOD(OD / 3.3V)

1D8V_S3_PG

Input Power
VCC(I)
VCC(I)

DCBATOUT
5V_S5

Output Power
VCC(O)
VCC(O)

1.8V_S3
1.2V_S0

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power Block Diagram***

Size	Document Number	Rev
A3	SJV50-TR	-1

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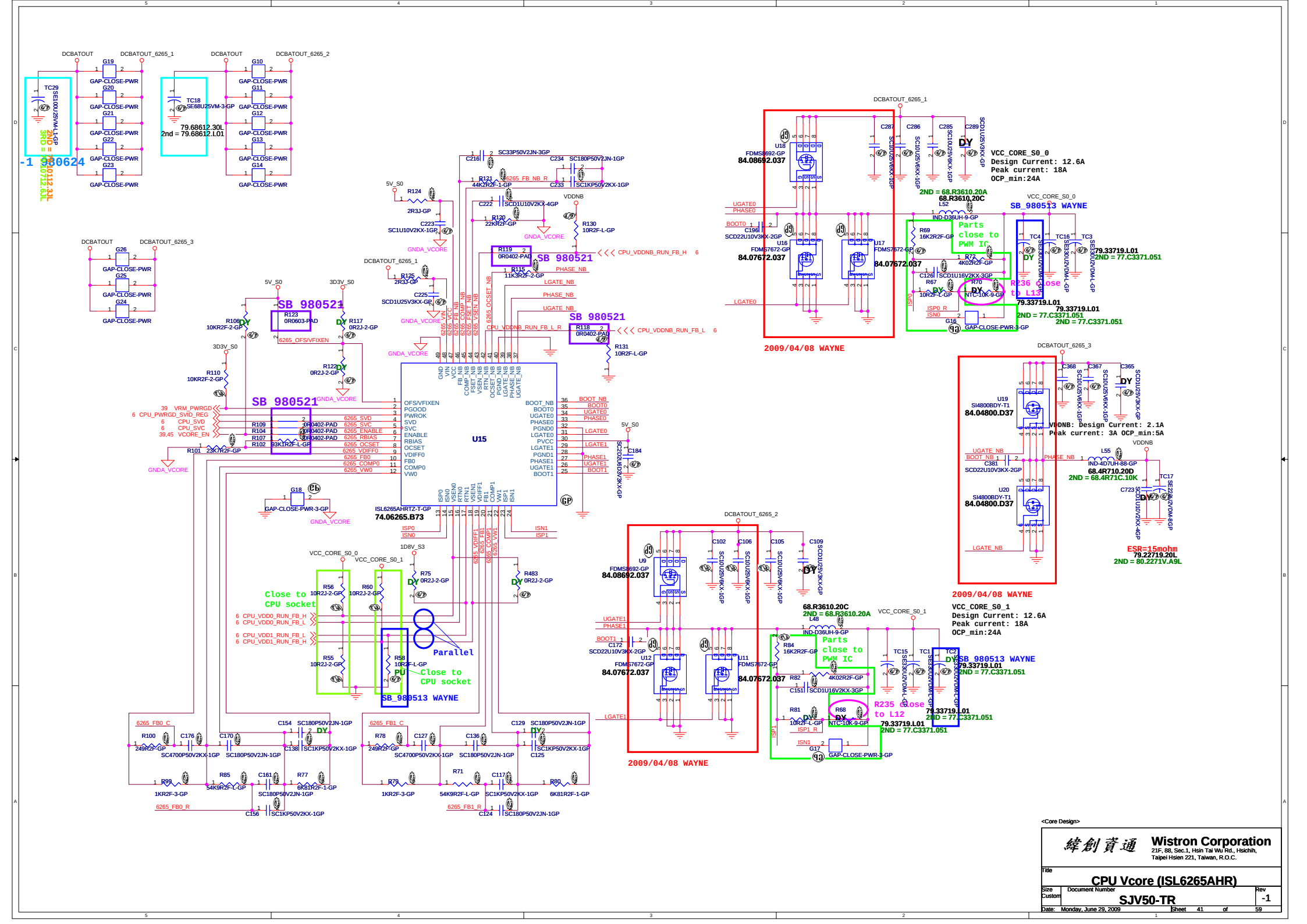
U15
ISL6265AHRTZ-T-GP
74.06265.B73
SB 980521
SB 980513 WAYNE
2009/04/08 WAYNE
Close to CPU socket
Parallel
Parts close to PWM IC
R235 Close to L12
R236 Close to L13
VCC_CORE_S0_0
Design Current: 12.6A
Peak current: 18A
OCP_min:24A
VCC_CORE_S0_1
Design Current: 12.6A
Peak current: 18A
OCP_min:24A
VDDNB: Design Current: 2.1A
Peak current: 3A OCP_min:5A
ESR=15mohm
79.22719.20L
2ND = 80.2271V.A9L
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CPU Vcore (ISL6265AHR)
SJV50-TR
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Monday, June 29, 2009
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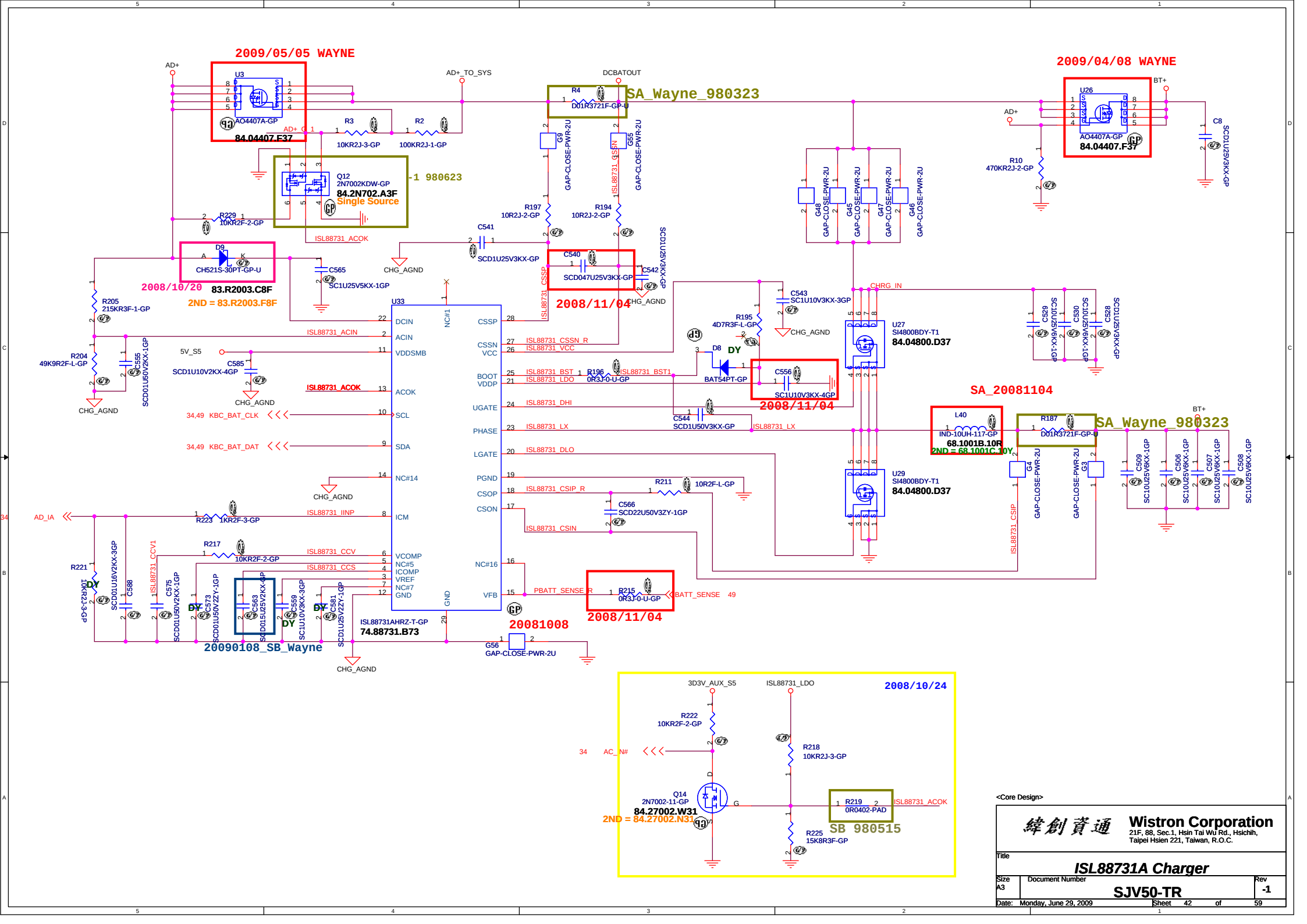
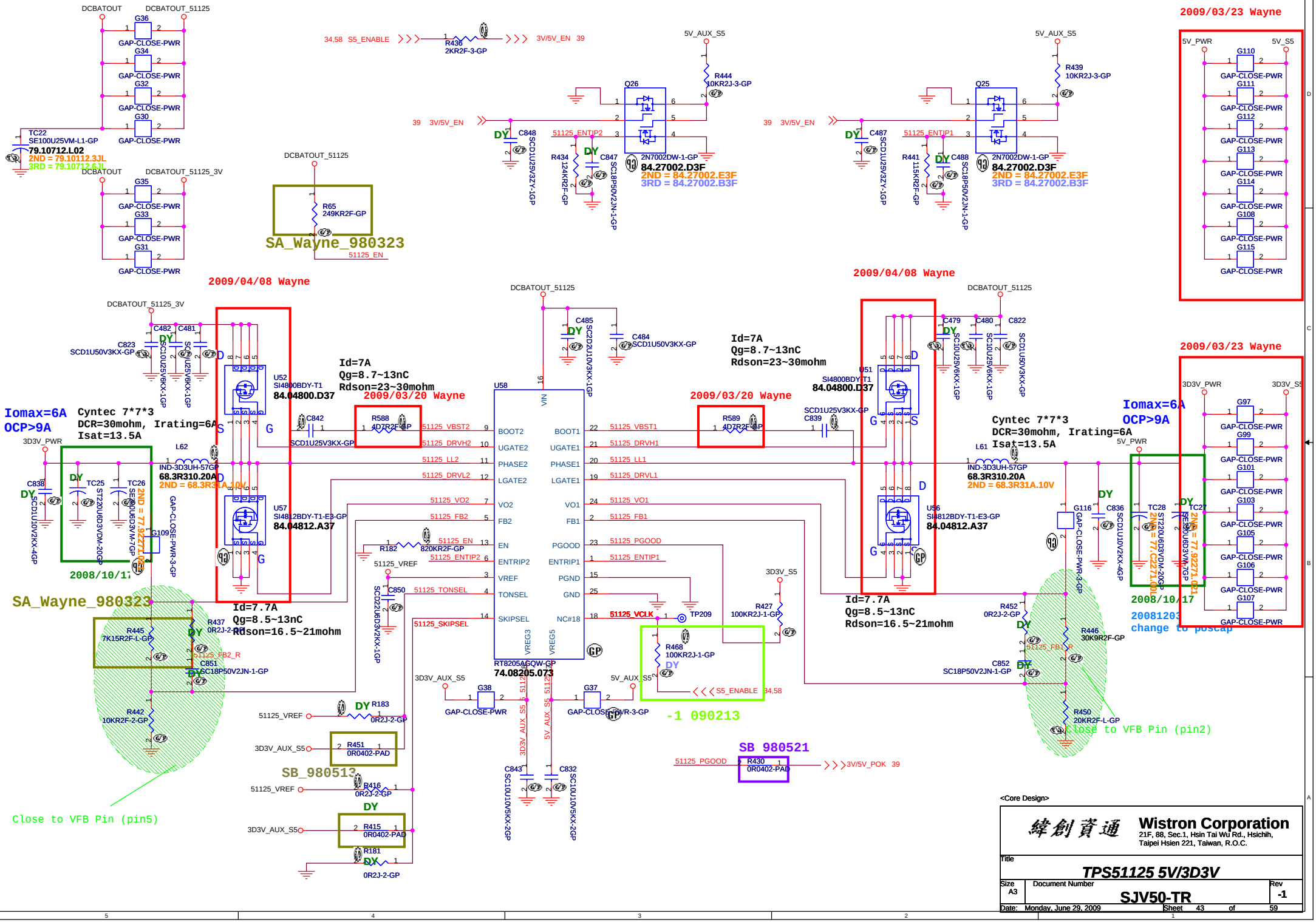

2009/05/05 WAYNE
2009/04/08 WAYNE
SA_Wayne_980323
SA_Wayne_980323
SA_20081104
U3
AO4407A-GP
84.04407.F37
U26
AO4407A-GP
84.04407.F37
Q12
2N7002KDW-GP
84.2N702.A3F
Single Source
-1 980623
D9
CH521S-30PT-GP-U
2008/10/20
83.R2003.C8F
2ND = 83.R2003.F8F
U33
ISL88731AHRZ-T-GP
74.88731.B73
20090108_SB_Wayne
20081008
2008/11/04
2008/11/04
2008/11/04
U27
SI4800BDY-T1
84.04800.D37
U29
SI4800BDY-T1
84.04800.D37
L40
IND-10UH-117-GP
68.1001B.10R
2ND = 68.1001C.10Y
D8
BAT54PT-GP
Q14
2N7002-11-GP
84.27002.W31
2ND = 84.27002.N31
2008/10/24
SB 980515
ISL88731A Charger
SJV50-TR
-1
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Monday, June 29, 2009
Sheet 42 of 59


2009/03/23 Wayne
2009/04/08 Wayne
2009/03/20 Wayne
SA_Wayne_980323
SA_Wayne_980513
SA_Wayne_980323
SB 980521
-1 090213
Iomax=6A
OCP>9A
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
Close to VFB Pin (pin5)
Close to VFB Pin (pin2)
RT8205AGQW-GP
74.08205.073
84.27002.D3F
2ND = 84.27002.E3F
3RD = 84.27002.B3F
84.04800.D37
84.04812.A37
68.3R310.20A
2ND = 68.3R31A.10V
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
TPS51125 5V/3D3V
SJV50-TR
Monday, June 29, 2009
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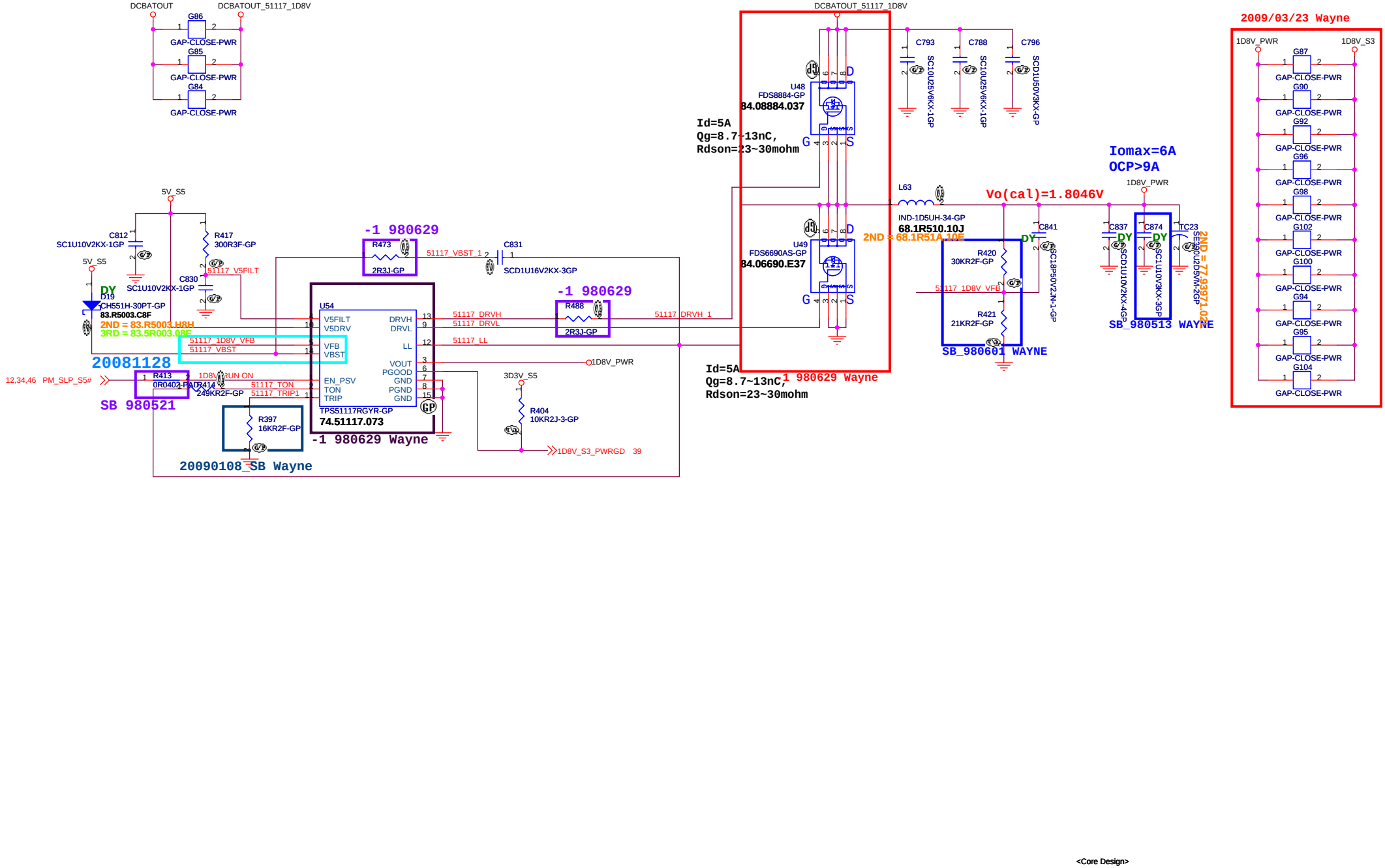


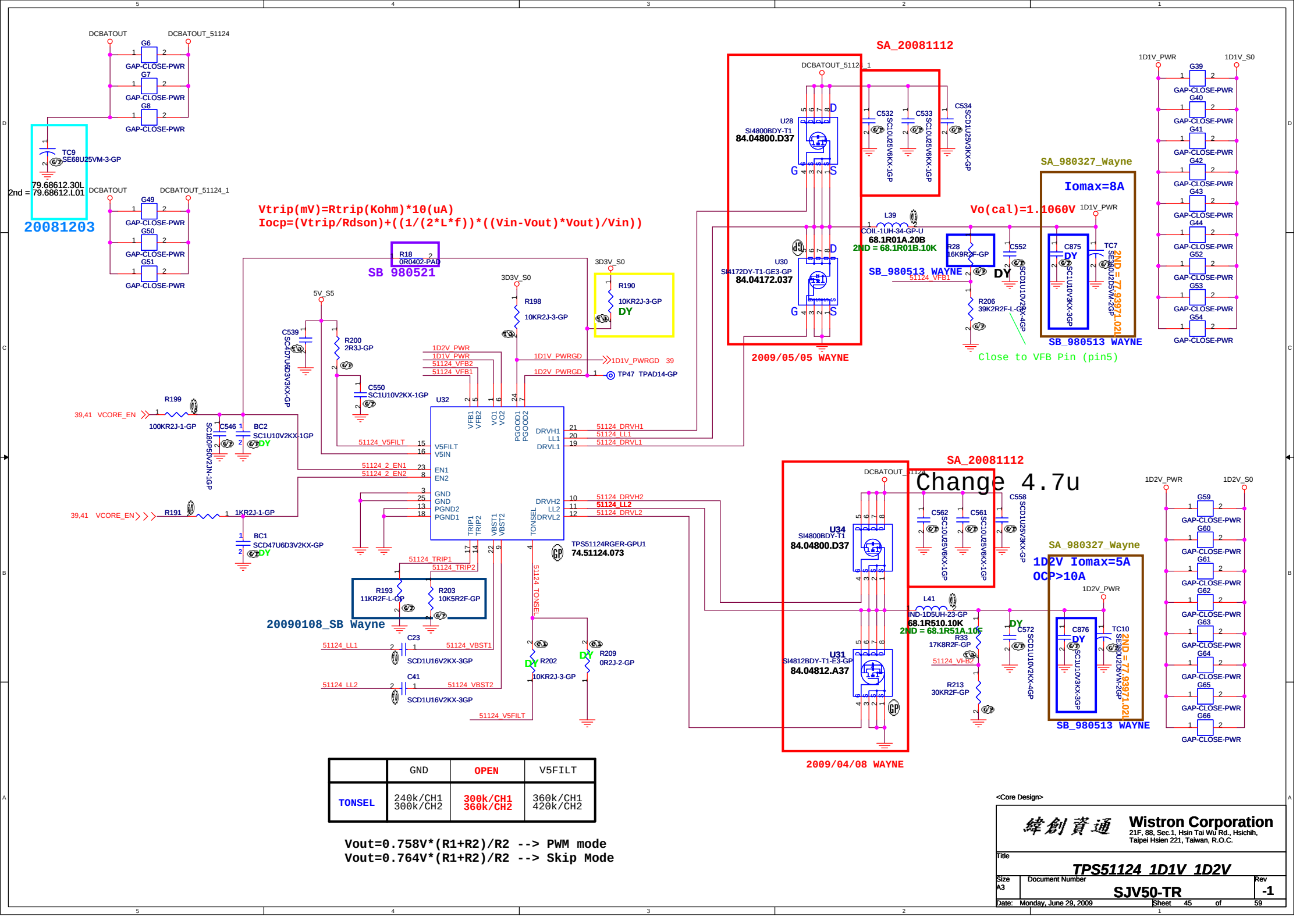
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***TPS51117_1D8V***

Size	Document Number	Rev
A3	SJV50-TR	-1

Date: Monday, June 29, 2009 Sheet 44 of 59



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

Vout=0.758V*(R1+R2)/R2 --> PWM mode
Vout=0.764V*(R1+R2)/R2 --> Skip Mode

<Core Design>

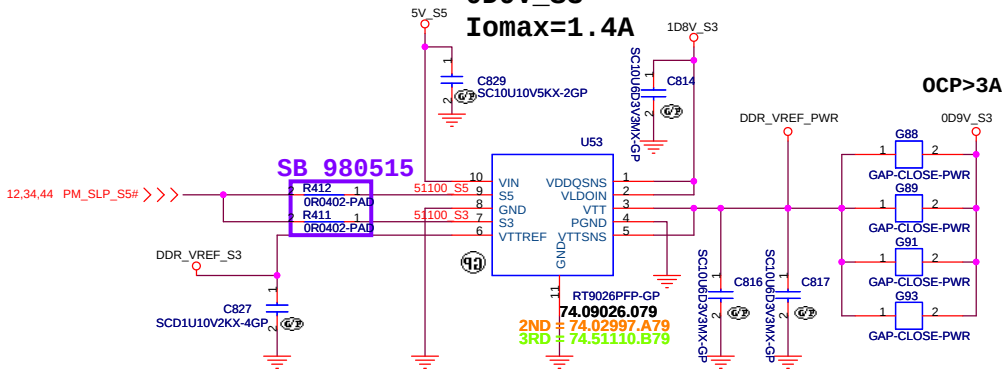
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124_1D1V_1D2V

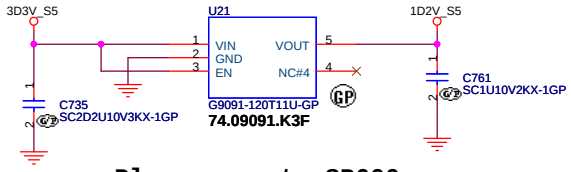
Size	Document Number	Rev
A3	SJV50-TR	-1

Date: Monday, June 29, 2009 Sheet 45 of 59

0D9V_S3
Iomax=1.4A



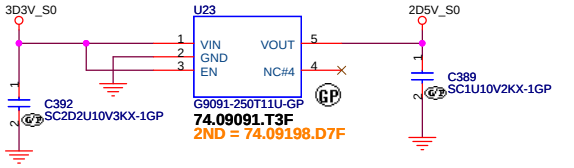
1D2V_S5
Iomax=0.2A



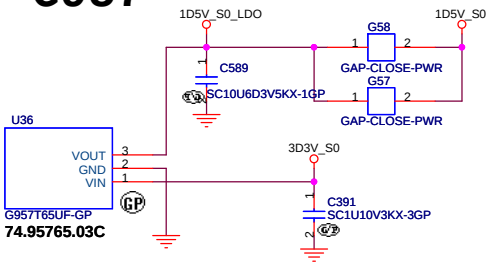
Place near to SB600

2D5V_S0
Iomax=200mA

OCP>430mA



G957
1D5V_S0
Iomax=1A

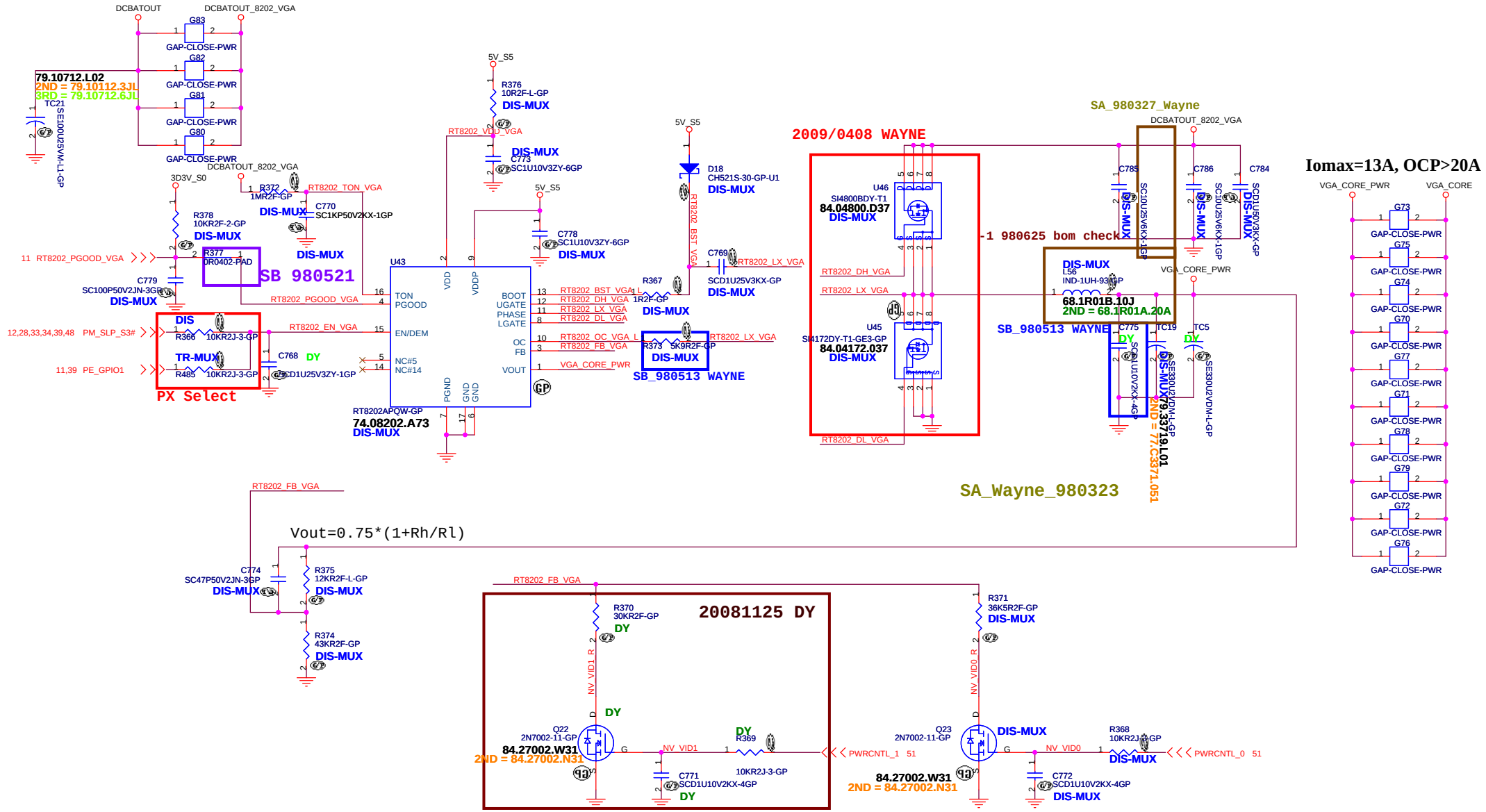


For MINI Card power SW

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	2D5V/1D5V0D9V	
Size A3	Document Number SJV50-TR	Rev -1
Date: Monday, June 29, 2009	Sheet 46 of 59	



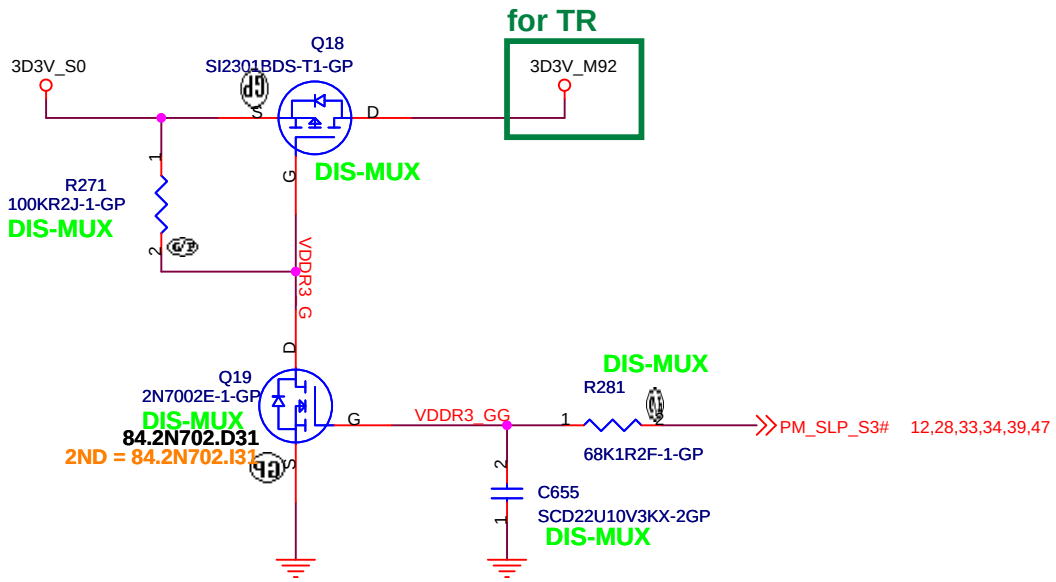
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8202A_VGA CORE

Size | Document Number: SJV50-TR | Rev: -1

Date: Monday, June 29, 2009 | Sheet 47 of 59

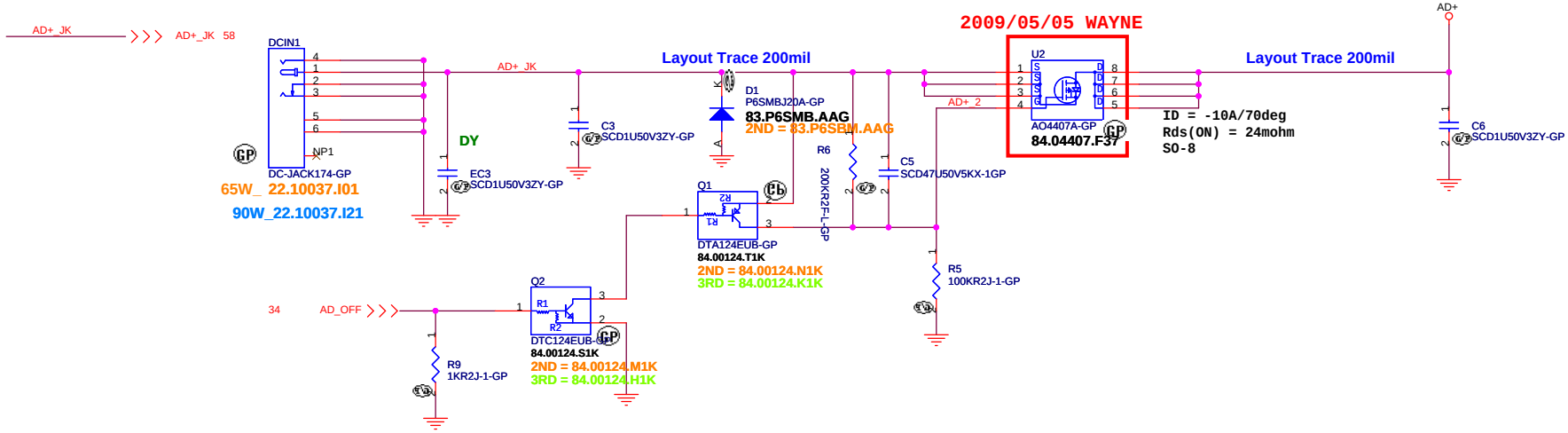


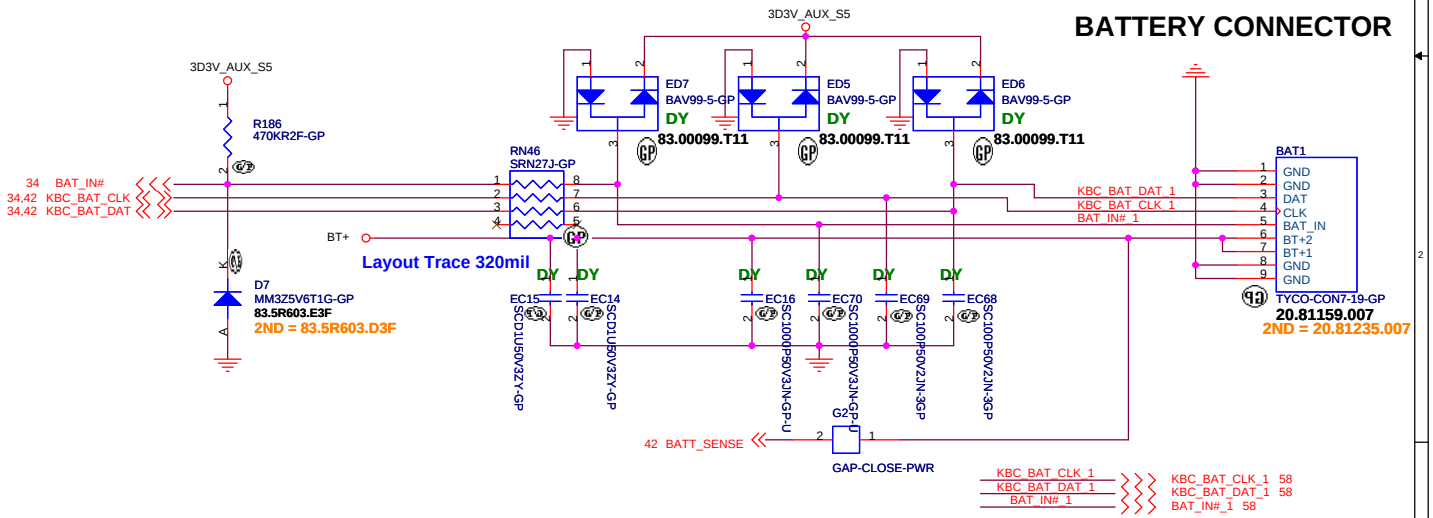
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***VDDR3***	
Size A4	Document Number **SJV50-TR**	Rev **-1**
Date: Monday, June 29, 2009	Sheet 48 of 59	

Adaptor in to generate DCBATOUT





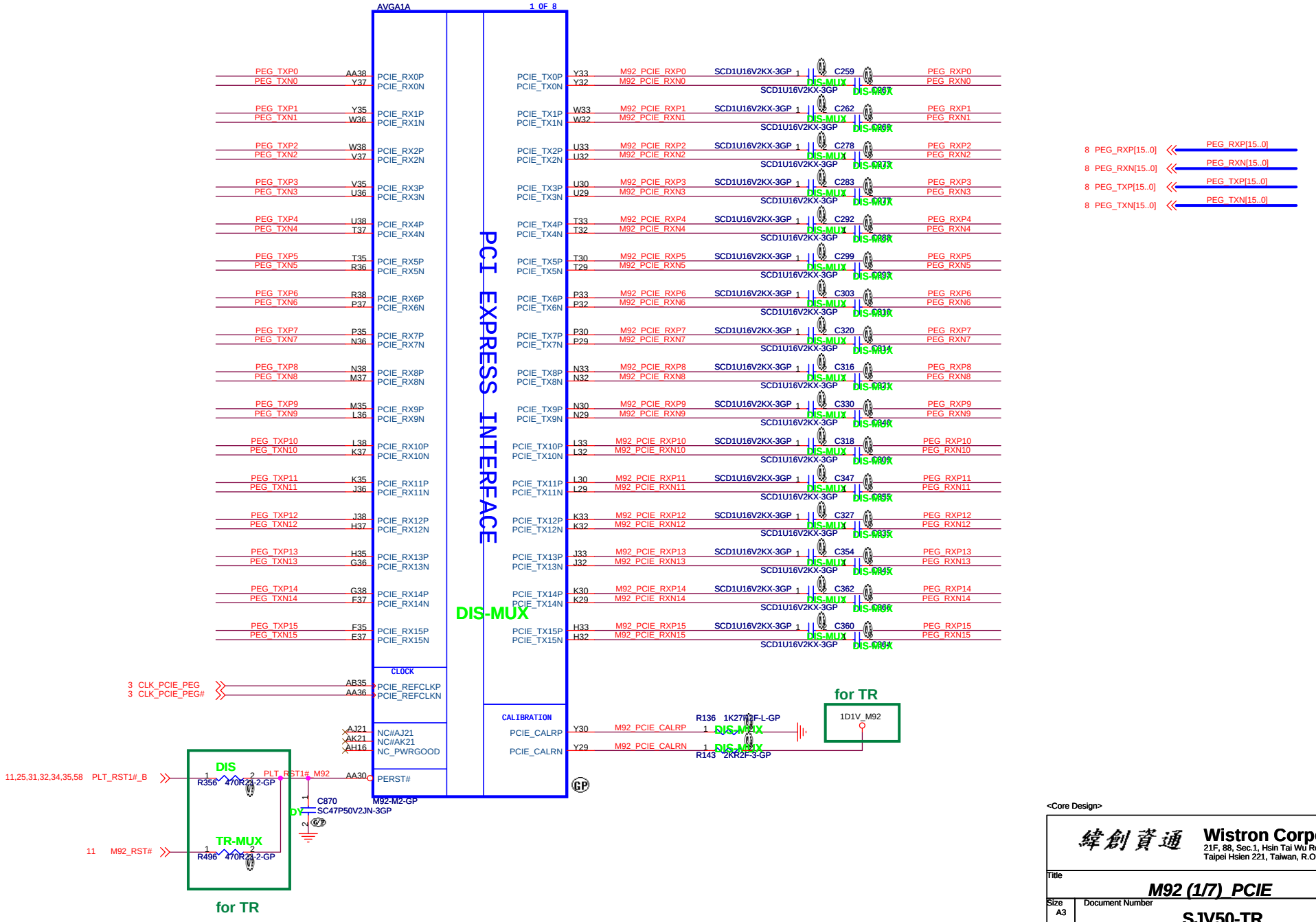
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AD/BATT CONN**

Size	Document Number	Rev
A3	SJV50-TR	-1

Date: Monday, June 29, 2009 Sheet 49 of 59



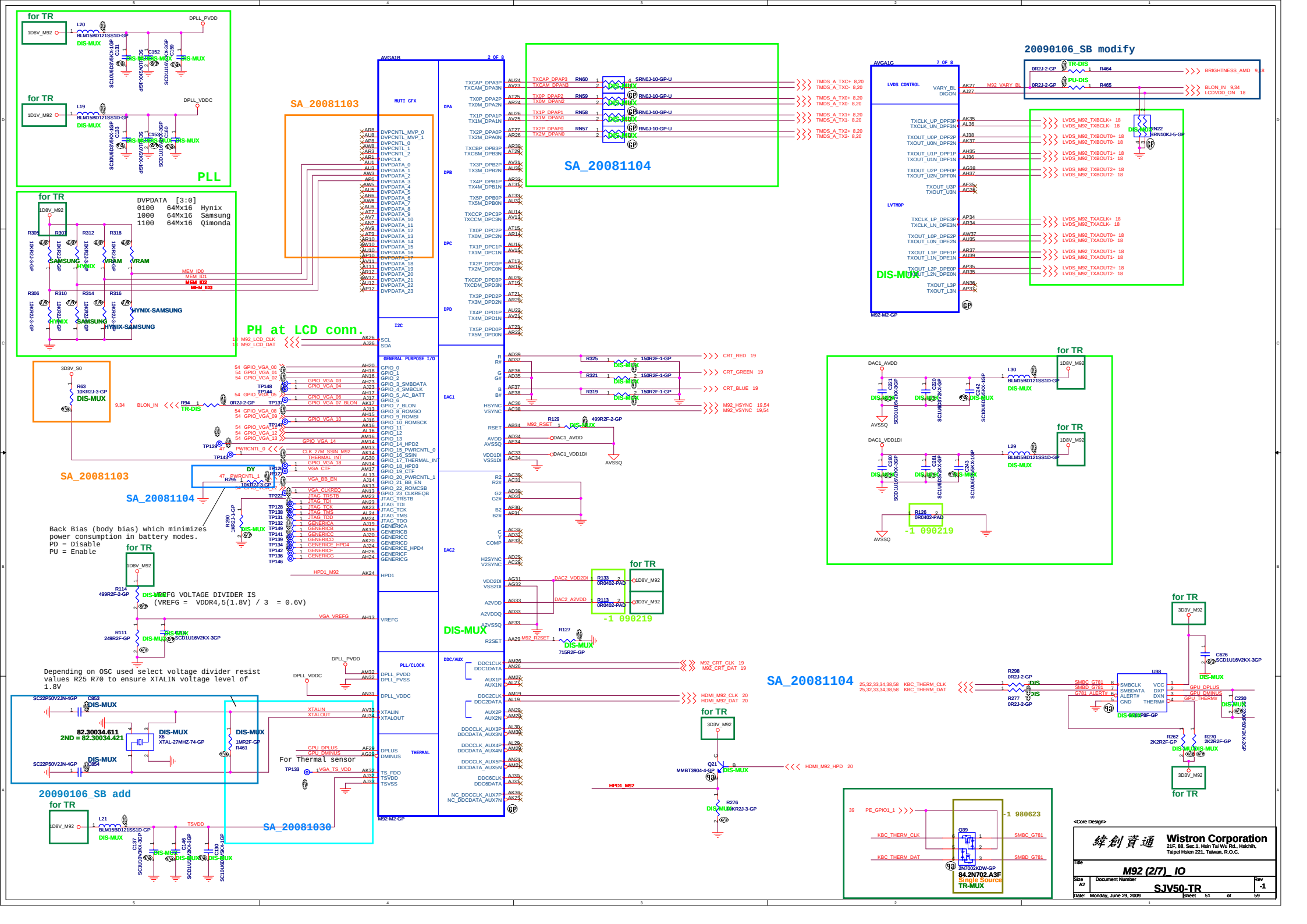
<Core Design>

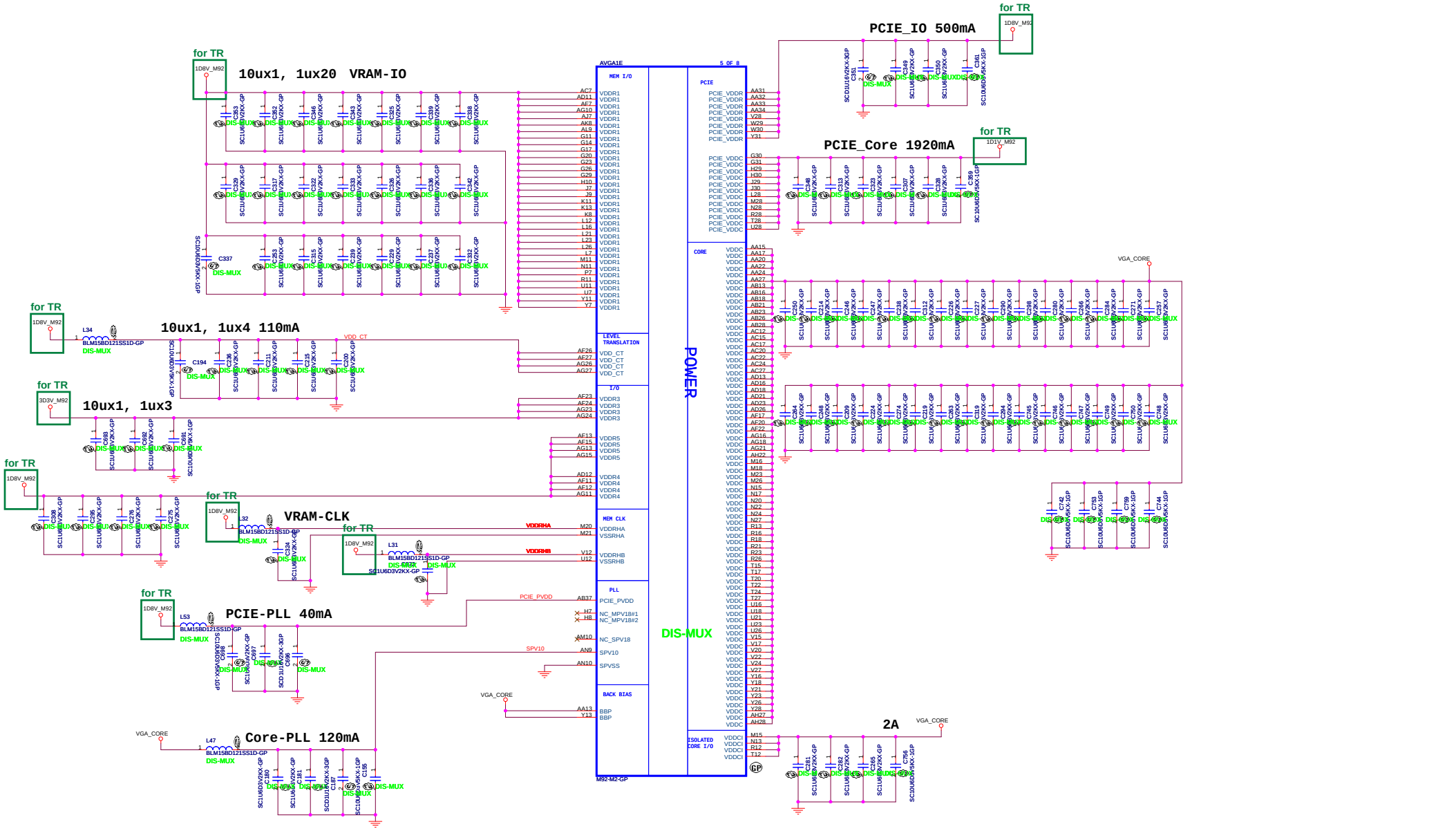
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: M92 (1/7) PCIE

Size	Document Number	Rev
A3	SJV50-TR	-1

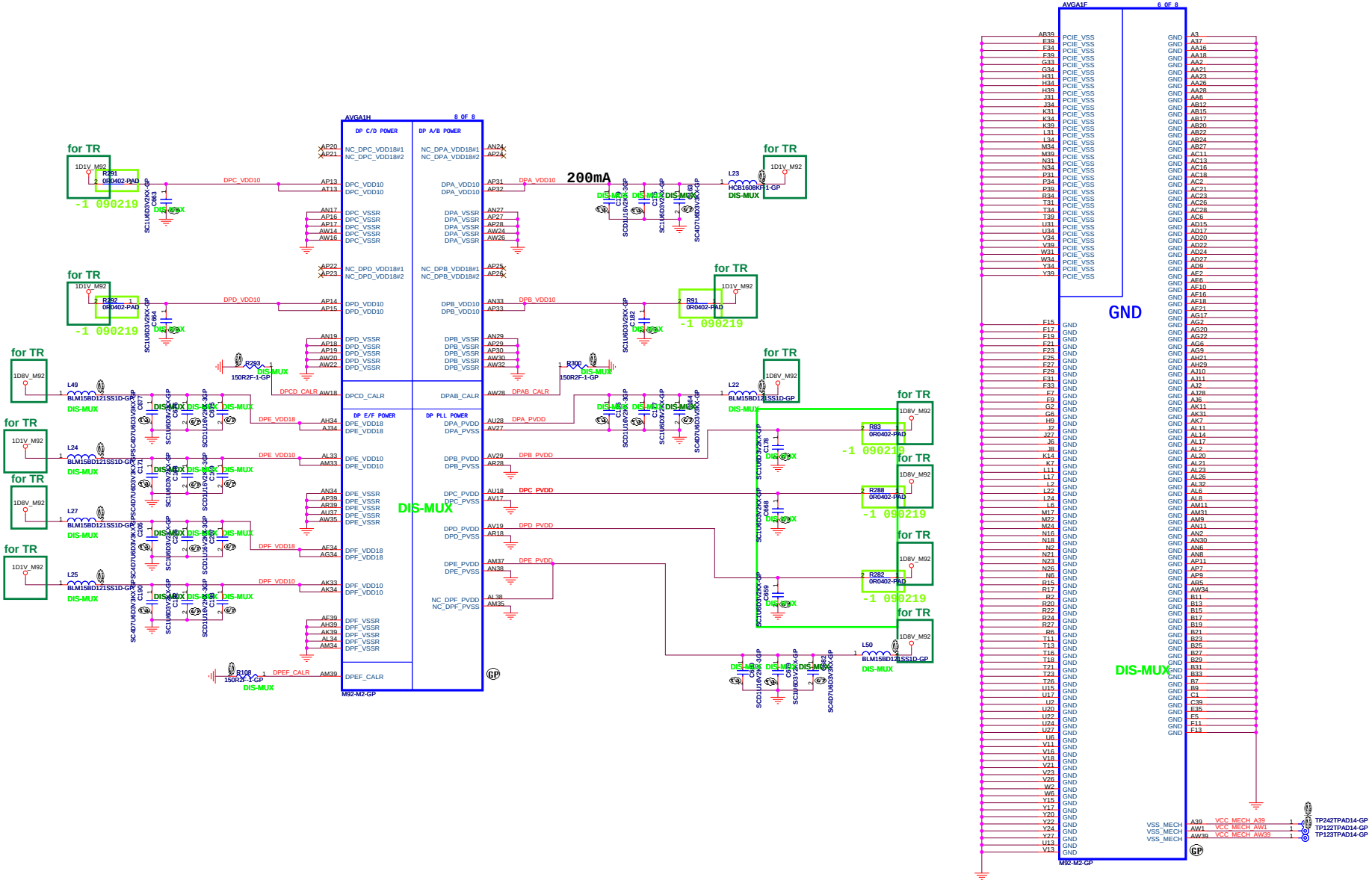
Date: Monday, June 29, 2009 Sheet 50 of 59


for TR
1D8V_M92
L20
BLM15BD121SS1D-GP
DIS-MUX
DPLL_PVDD
C131
C152
C159
1D1V_M92
L19
DPLL_VDDC
C133
C153
C160
PLL
DVPDATA [3:0]
0100 64Mx16 Hynix
1000 64Mx16 Samsung
1100 64Mx16 Qimonda
SAMSUNG
HYNIX
VRAM
HYNIX-SAMSUNG
MEM_ID1
MEM_ID2
MEM_ID3
SA_20081103
SA_20081104
PH at LCD conn.
M92_LCD_CLK
M92_LCD_DAT
3D3V_S0
R63
10KR2J-3-GP
BLON_IN
R94
TR-DIS
0R2J-2-GP
GPIO_VGA_00
GPIO_VGA_01
GPIO_VGA_02
GPIO_VGA_03
GPIO_VGA_04
GPIO_VGA_05
GPIO_VGA_06
GPIO_VGA_07_BLON
GPIO_VGA_08
GPIO_VGA_09
GPIO_VGA_10
GPIO_VGA_11
GPIO_VGA_12
GPIO_VGA_13
GPIO_VGA_14
PWRCNTL_0
CLK_27M_SSIN_M92
THERMAL_INT
GPIO_VGA_18
VGA_CTF
VGA_BB_EN
VGA_CLKREQ
JTAG_TRSTB
JTAG_TDI
JTAG_TCK
JTAG_TMS
JTAG_TDO
GENERICA
GENERICB
GENERICC
GENERICD
GENERICE_HPD4
GENERICF
GENERICG
HPD1_M92
DY
Back Bias (body bias) which minimizes
power consumption in battery modes.
PD = Disable
PU = Enable
VREFG VOLTAGE DIVIDER IS
(VREFG = VDDR4,5(1.8V) / 3 = 0.6V)
VGA_VREFG
Depending on OSC used select voltage divider resist
values R25 R70 to ensure XTALIN voltage level of
1.8V
82.30034.611
2ND = 82.30034.421
XTAL-27MHZ-74-GP
For Thermal sensor
VGA_TS_VDD
20090106_SB add
SA_20081030
AVGA1B
2 OF 8
MUTI GFX
I2C
GENERAL PURPOSE I/O
DAC1
DAC2
DDC/AUX
PLL/CLOCK
THERMAL
M92-M2-GP
SA_20081104
SRN0J-10-GP-U
RN0J-10-GP-U
TMDS_A_TXC+ 8,20
TMDS_A_TXC- 8,20
TMDS_A_TX0+ 8,20
TMDS_A_TX0- 8,20
TMDS_A_TX1+ 8,20
TMDS_A_TX1- 8,20
TMDS_A_TX2+ 8,20
TMDS_A_TX2- 8,20
20090106_SB modify
AVGA1G
7 OF 8
LVDS CONTROL
LVTMDP
DIS-MUX
M92-M2-GP
TR-DIS
PU-DIS
BRIGHTNESS_AMD 9,18
BLON_IN 9,34
LCDVDD_ON 18
SRN10KJ-5-GP
CRT_RED 19
CRT_GREEN 19
CRT_BLUE 19
M92_HSYNC 19,54
M92_VSYNC 19,54
499R2F-2-GP
150R2F-1-GP
DAC1_AVDD
DAC1_VDD1DI
AVSSQ
DAC2_VDD2DI
DAC2_A2VDD
0R0402-PAD
-1 090219
715R2F-GP
M92_CRT_CLK 19
M92_CRT_DAT 19
HDMI_M92_CLK 20
HDMI_M92_DAT 20
HDMI_M92_HPD 20
MMBT3904-4-GP
SA_20081104
KBC_THERM_CLK
KBC_THERM_DAT
SMBC_G781
SMBD_G781
GPU_DPLUS
GPU_DMINUS
GPU_THERM#
-1 980623
2N7002KDW-GP
84.2N702.A3F
Single Source
TR-MUX
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
M92 (2/7)_ IO
Size A2
Document Number
SJV50-TR
Rev -1
Date: Monday, June 29, 2009
Sheet 51 of 59



<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	M92 (3/7) Power	
Size: A2	Document Number: SJV50-TR	Rev: -1
Date: Monday, June 29, 2009	Sheet 52 of 59	



<Core Design>

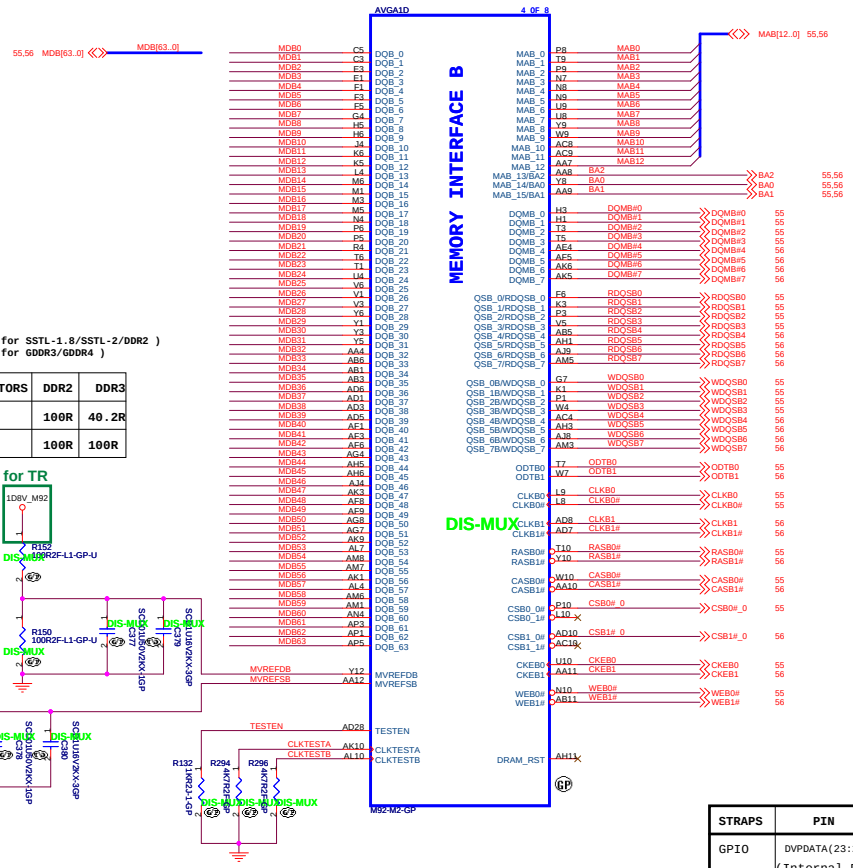
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: M92 (4/7) DP POWER GND

Size: A2 | Document Number: SJV50-TR | Rev: -1

Date: Monday, June 29, 2009 | Sheet 53 of 59

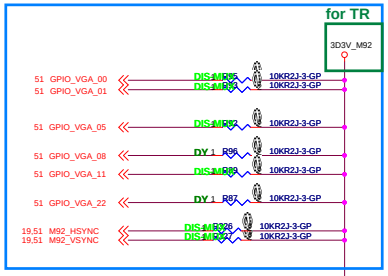
M92-M2 uses memory group B only



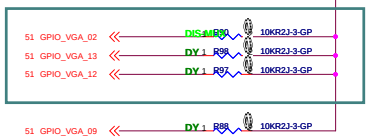
(0.5 * VDDR1) (for SSTL-1.8/SSTL-2/DDR2)
(0.7 * VDDR1) (for GDDR3/GDDR4)

DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

SA_20081104



SA_20081105



HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.

STRAPS	PIN	DESCRIPTION
GPIO	DVPDATA(23:20) (Internal PD)	Initialization Behavior: This signal is input during reset (no reference clock is required). After reset, the default state is output low (0 V). The signals above can be left unconnected if not used.

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC, GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO_28_TDO , GPIO21_BB_EN

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
V 128MB	x000	ST Microelectronics	M25P05A	0100
256MB	x001		M25P10A	0101
64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
2GB	x		Pm25LV010A	0101
4GB	x			

STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PWRS_ENB (Internal PD)	GPIO0	PCIE FULL TX OUTPUT SWING Tansmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	1
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	1
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED 0 = Advertises the PCI-E device as 2.5GT/s 1 = Advertises the PCI-E device as 5GT/s	1
AC_BATT	GPIO5	AC (Performance mode) = 3.3 V Battery saving mode = 0.0 V	
ROMSO	GPIO8	BIF_CLK_PM_EN Serial ROM Output from ROM	0
ROMSI	GPIO9	VGA ENABLED Serial ROM Input to ROM	0
ROMIDCFG[3:0] (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1, then Config[3:0] defines the ROM type if BIOS_ROM_EN=0, then Config[3:0] defines the primary memory apeture size	X X X
PWRCNTL_[1,0]	GPIO[15,20]	Power control signals to control the core voltage regulator	
BB_EN	GPIO21	Back Bias (body bias) which minimizes power consumption in battery modes. 0V = Disable 3D3V = Enable	0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI	1
CCBYPASS	GENERICC		0

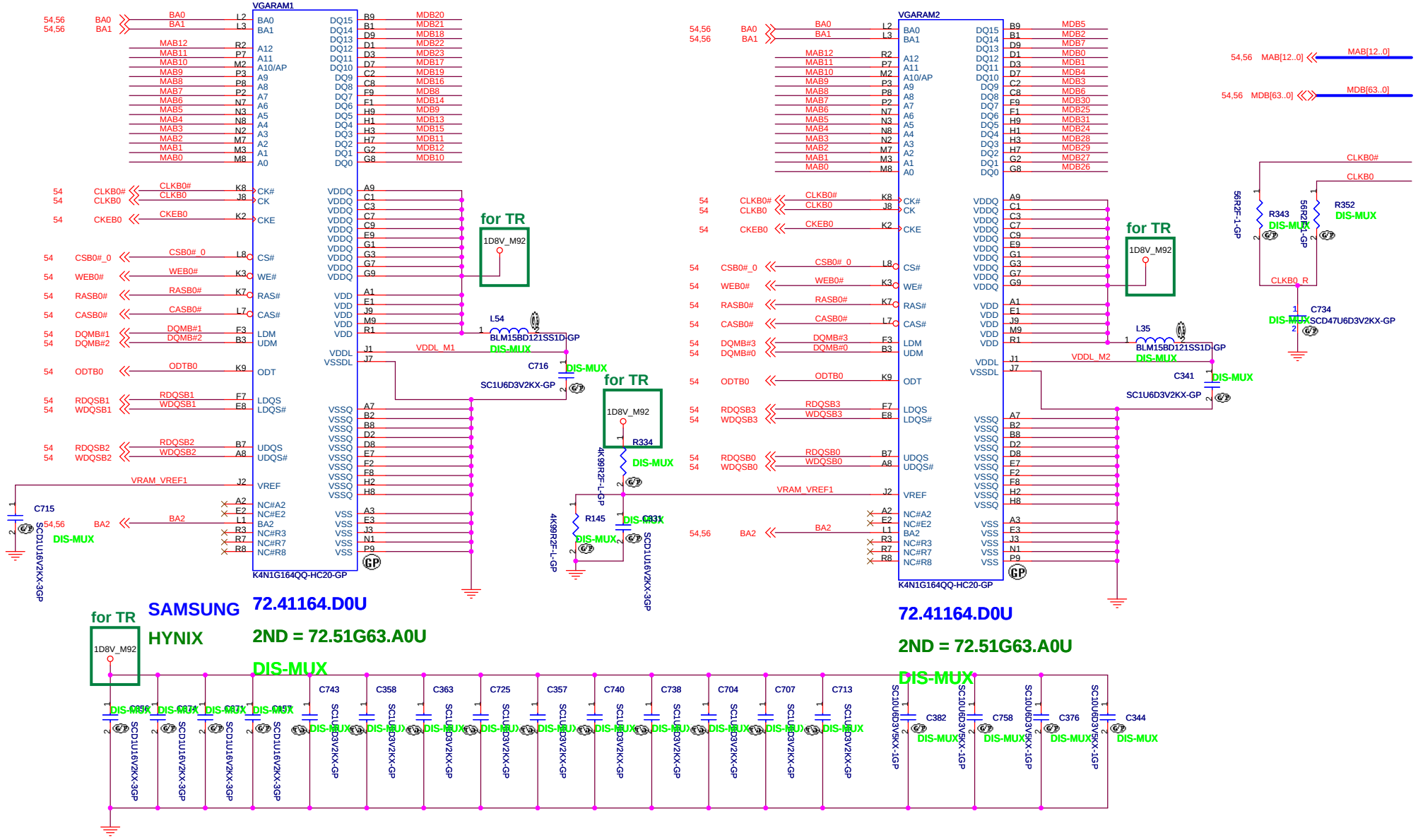
<Core Design>

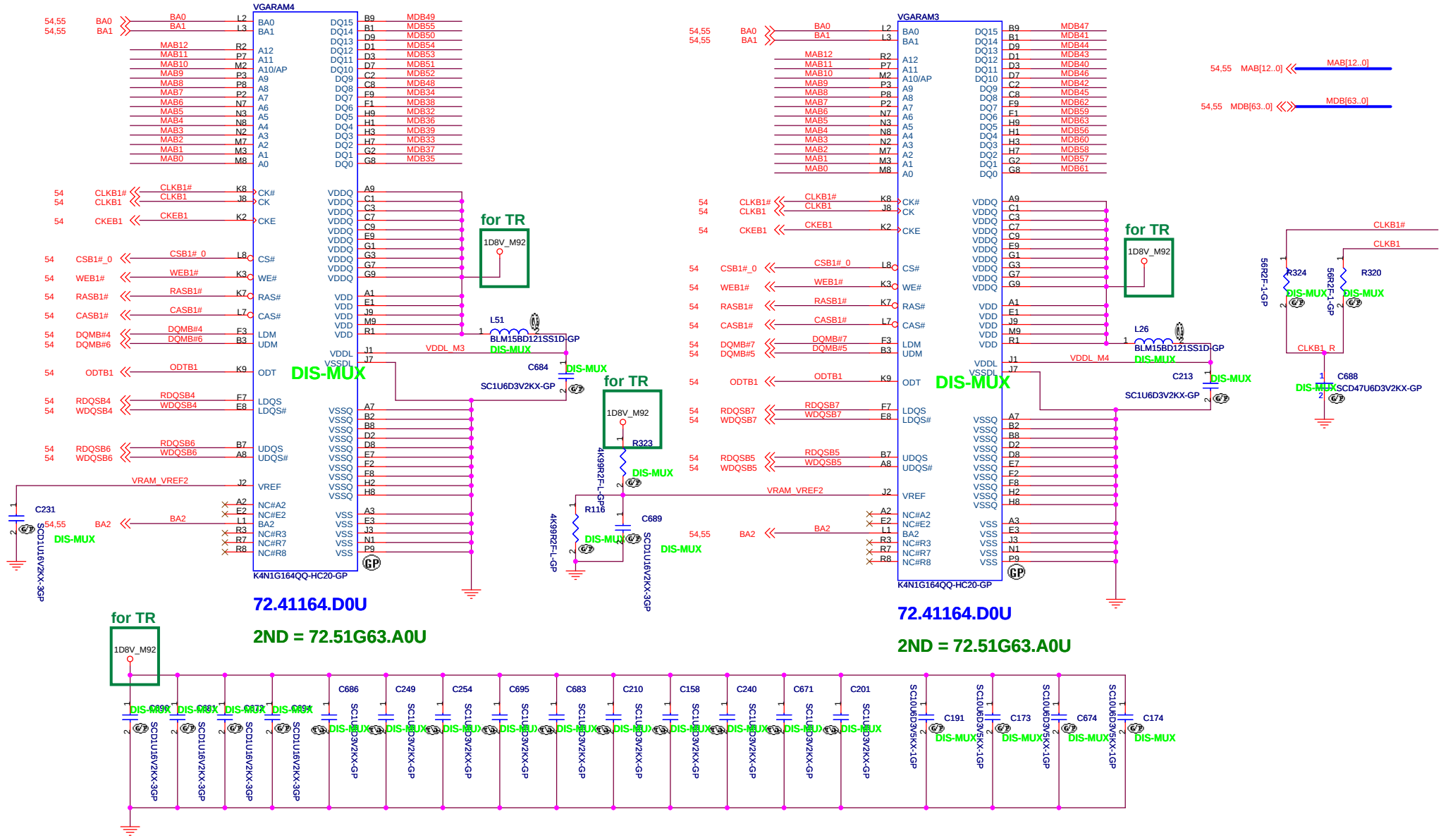
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: M92 (5/7) Memory Straps

Size: A2 | Document Number: SJV50-TR | Rev: -1

Date: Monday, June 29, 2009 | Sheet 54 of 59


VGARAM1
K4N1G164QQ-HC20-GP
VGARAM2
K4N1G164QQ-HC20-GP
for TR
1D8V_M92
DIS-MUX
SAMSUNG
HYNIX
72.41164.D0U
2ND = 72.51G63.A0U
DIS-MUX
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
M92 (6/7) VRAM B0
Size A3
Document Number
SJV50-TR
Rev -1
Date: Monday, June 29, 2009
Sheet 55 of 59



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: M92 (7/7) VRAM B1

Size: A3 | Document Number: SJV50-TR | Rev: -1

Date: Monday, June 29, 2009 | Sheet 56 of 59

SA

SB

-1

5V_S0

U7C
TSAHCT125PW-GP
73.74125.L13
2ND = 73.74125.L12

5V_S0

U7D
TSAHCT125PW-GP
73.74125.L13
2ND = 73.74125.L12

use 34.42Y01.031
M-STANDOFF
2nd 34.42Y01.021

H7 HOLE236R142
34.42Y01.031
Type-M

H8 HOLE236R142
34.42Y01.031
Type-M

use 34.4B804.011
S-STANDOFF
2nd 34.4B804.001

H15 HOLE276R110
34.4B804.011

H20 HOLE276R110
34.4B804.011

DY

GND1 GND2 GND3 GND4 GND5
GND6 GND7 GND8 GND9 GND10

H11 HOLE256R142-GP
34.42Y01.031
Type-I

H12 HOLE256R142-GP
34.42Y01.031
Type-I

H13 HOLE256R142-GP
34.42Y01.031
Type-I

H14 HOLE256R142-GP
34.42Y01.031
Type-I

H16 HOLE256R142-GP
34.42Y01.031
Type-I

H17 HOLE256R142-GP
34.42Y01.031
Type-I

use 34.42Y01.031/ZZ.00PAD.801
2nd 34.42Y01.021

SPR1 SPR2 SPR3
SPRING-71-GP
34.4H551.001

20081203 SB 980521 DEL

for TR

SB 980519_RF

20081202

DCBATOUT

-1 090223_EMI

-1 090223_EMI

1D1V_M92

1D8V_M92

RF_DY

C416 C425

5V_S5

5V_S0

3D3V_S0

<Core Design>

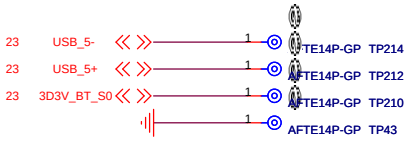
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: EMI/Spring/Boss

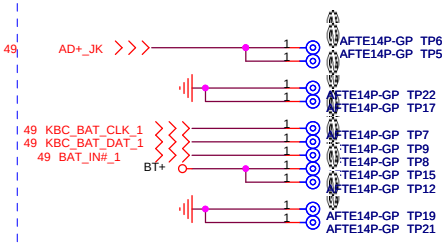
Size | Document Number: SJV50-TR | Rev: -1

Date: Monday, June 29, 2009 | Sheet 57 of 59

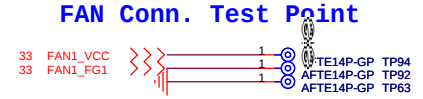
BT Conn. Test Point



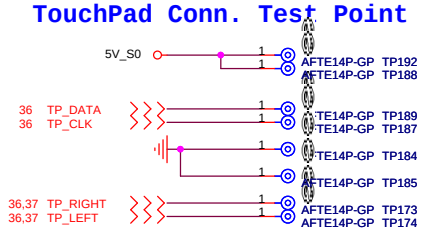
AD+, BAT Conn. Test Point



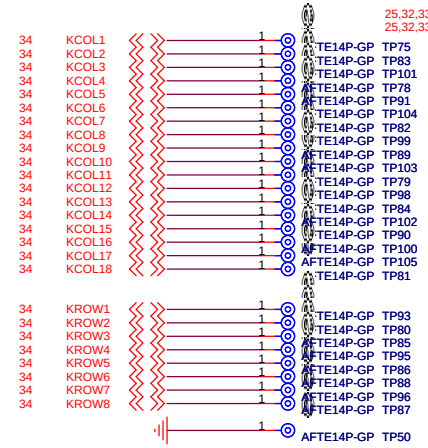
FAN Conn. Test Point



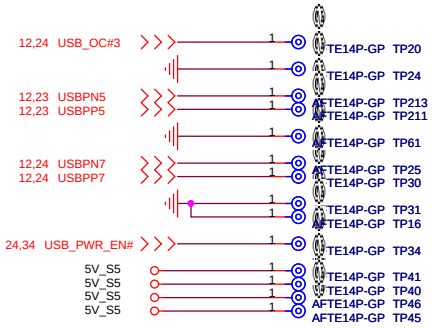
TouchPad Conn. Test Point



KB Conn. Test Point



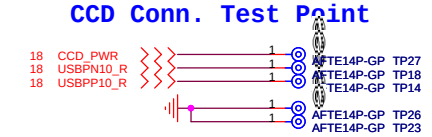
USBCN1 Conn. Test Point



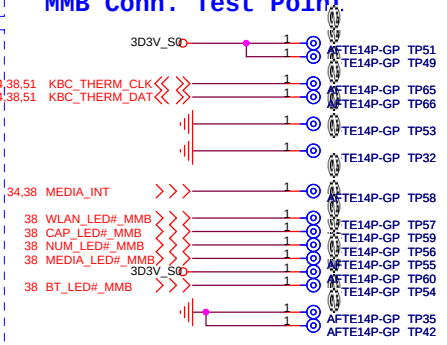
PowerButton Conn. Test Point

AMic Conn. Test Point

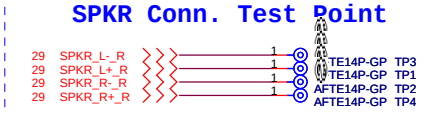
CCD Conn. Test Point



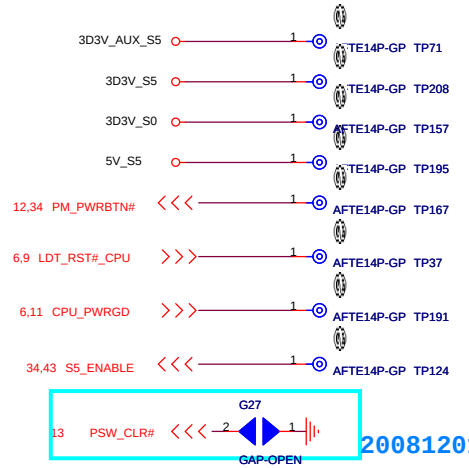
MMB Conn. Test Point



SPKR Conn. Test Point



Check test point



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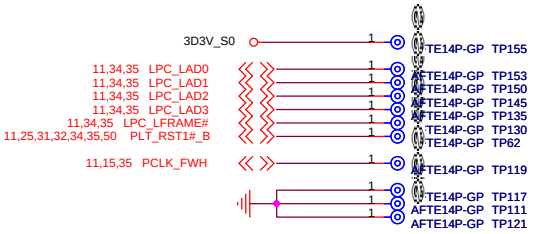
Test Point放在Dimm Door打開可量測處



<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Test point*		
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R297-->PU-DIS & TR-DIS 0 ohm
PU-UMA & TR-UMA & MUX 5.1K ohm

R52-->PU-DIS & TR-DIS 100K ohm
PU-UMA & TR-UMA & MUX 10K ohm

C645~C652
Non-Level shift UMA mount 0 ohm
DIS use DUMMY

<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Change List

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