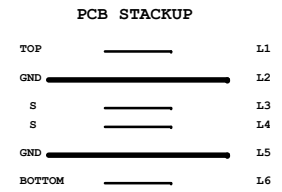
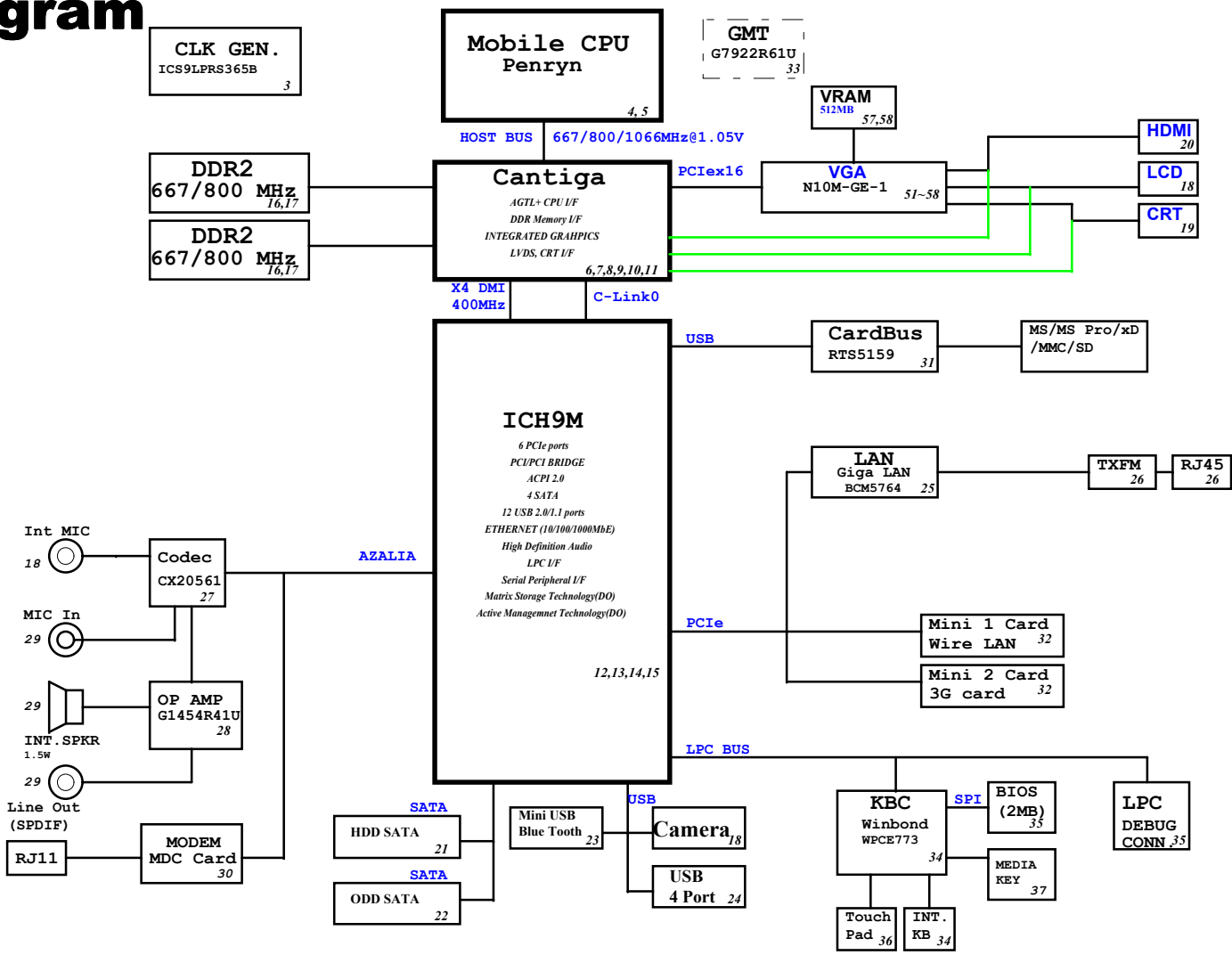


# SJV50 Block Diagram

Project code: 91.4BU01.001  
 PCB P/N : 48.4BU01.0SB  
 REVISION : 08244-SB



SYSTEM DC/DC ISL62392 41	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 (6A) 3D3V_S5 (7A) 5V_AUX_S5 3D3V_AUX_S5
SYSTEM DC/DC TFS51124 42	
INPUTS	OUTPUTS
DCBATOUT	ID05V_S0 (9A) ID8V_S3 (13A)
RT9026 43	
ID8V_S3	DDR_VREF_S3 (1.2A)
RT9018 44	
ID8V_S3	ID1V_S0 (2A)
RT9018 44	
ID8V_S3	ID5V_S0 (2.5A)
CHARGER ISL88731A 46	
INPUTS	OUTPUTS
DCBATOUT	BT+
CPU DC/DC ISL6266A 40	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 38A
VGA CORE RT8202 48	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE 13A
GFXCORE ISL6263A 45	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE (11A)

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# ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers: Offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage. Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resistor.

# ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native LAN DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

# Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) 1=The iTPM Host Interface is disabled(default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIe Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG10	PCIe Loopback enable	0 = Enable (Note 3) 1= Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	0 = Only Digital Display Port or PCIe is operational (Default) 1 = Digital display Port and PCIe are operating simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 =No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1= LFP Card Present; PCIe disabled

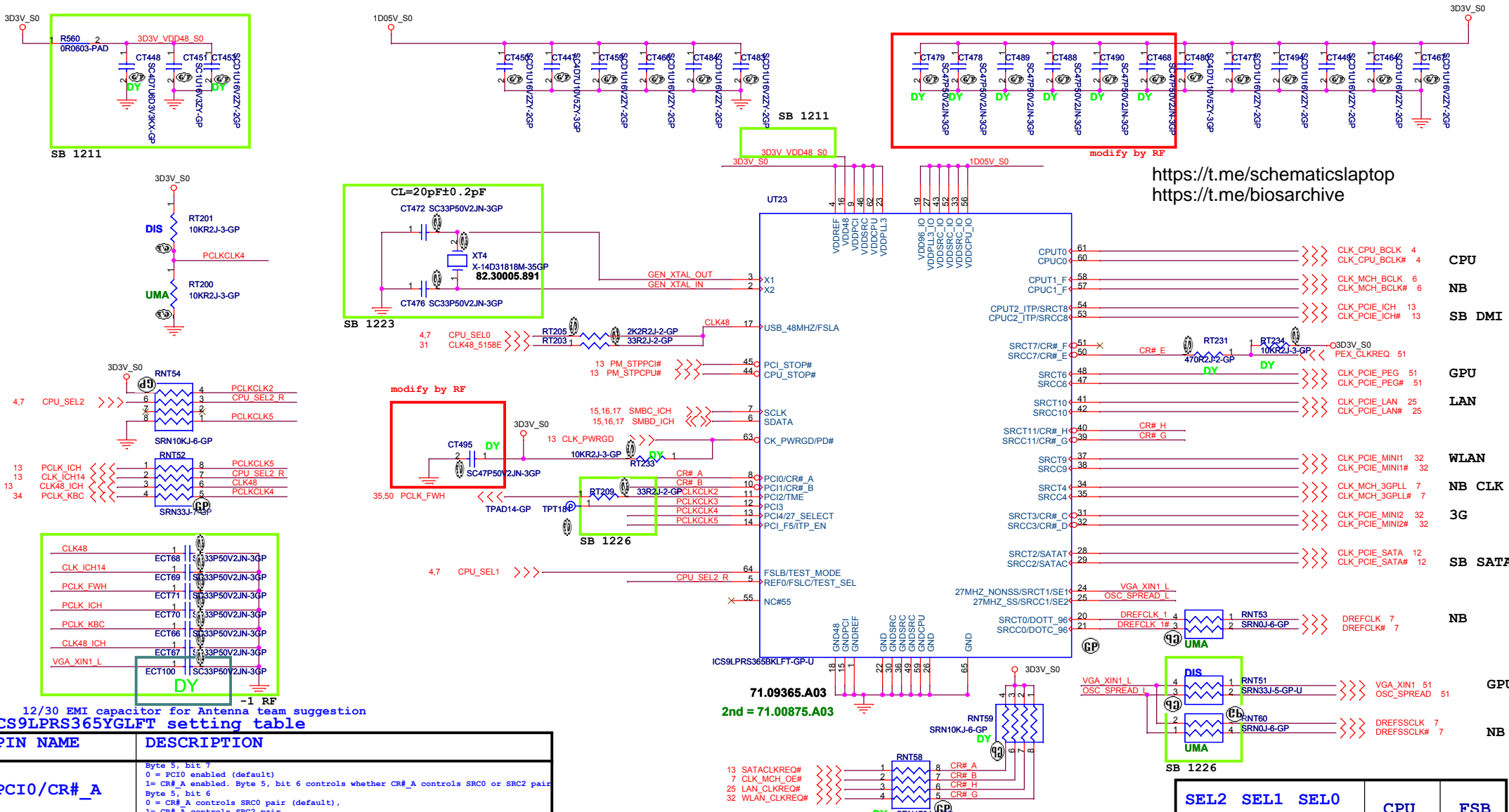
### NOTE:

- All strap signals are sampled with respect to the leading edge of the (GMCH Power OK (PWROK) signal.
- iTPM can be disabled by a 'Soft-Strap' option in the Flash-descriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

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SJV50

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<b>Reference</b>			
Size A3	Document Number	Rev SA	
<b>SJV50</b>			
Date: Monday, February 23, 2009	Sheet 2 of 59		



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12/30 EMI capacitor for Antenna team suggestion  
 ICS9LPRS365YGLFT setting table

PIN NAME	DESCRIPTION
<b>PCIO/CR#_A</b>	Byte 5, bit 7 0 = PCIO enabled (default) 1= CR# A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR# A controls SRC0 pair (default), 1= CR# A controls SRC2 pair
<b>PCII/CR#_B</b>	Byte 5, bit 5 0 = PCII enabled (default) 1= CR# B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR# B controls SRC1 pair (default) 1= CR# B controls SRC4 pair
<b>PCI2/TME</b>	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
<b>PCI3</b>	
<b>PCI4/27M_SEL</b>	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
<b>PCI_F5/ITP_EN</b>	0 = SRC8/SRC8# 1 = ITP/ITP#
<b>SRCT3/CR#_C</b>	Byte 5, bit 3 0 = SRC3 enabled (default) 1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1= CR#_C controls SRC2 pair

PIN NAME	DESCRIPTION
<b>SRCC3/CR#_D</b>	Byte 5, bit 1 0 = SRC3 enabled (default) 1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1= CR#_D controls SRC4 pair
<b>SRCC7/CR#_E</b>	Byte 6, bit 7 0 = SRC7# enabled (default) 1= CR#_F controls SRC6
<b>SRCT7/CR#_F</b>	Byte 6, bit 6 0 = SRC7 enabled (default) 1= CR#_F controls SRC8
<b>SRCC11/CR#_G</b>	Byte 6, bit 5 0 = SRC11# enabled (default) 1= CR#_G controls SRC9
<b>SRCT11/CR#_H</b>	Byte 6, bit 4 0 = SRC11 enabled (default) 1= CR#_H controls SRC10

SEL2	SEL1	SEL0	CPU	FSB
FSC	FSB	FSA		
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

SJV50

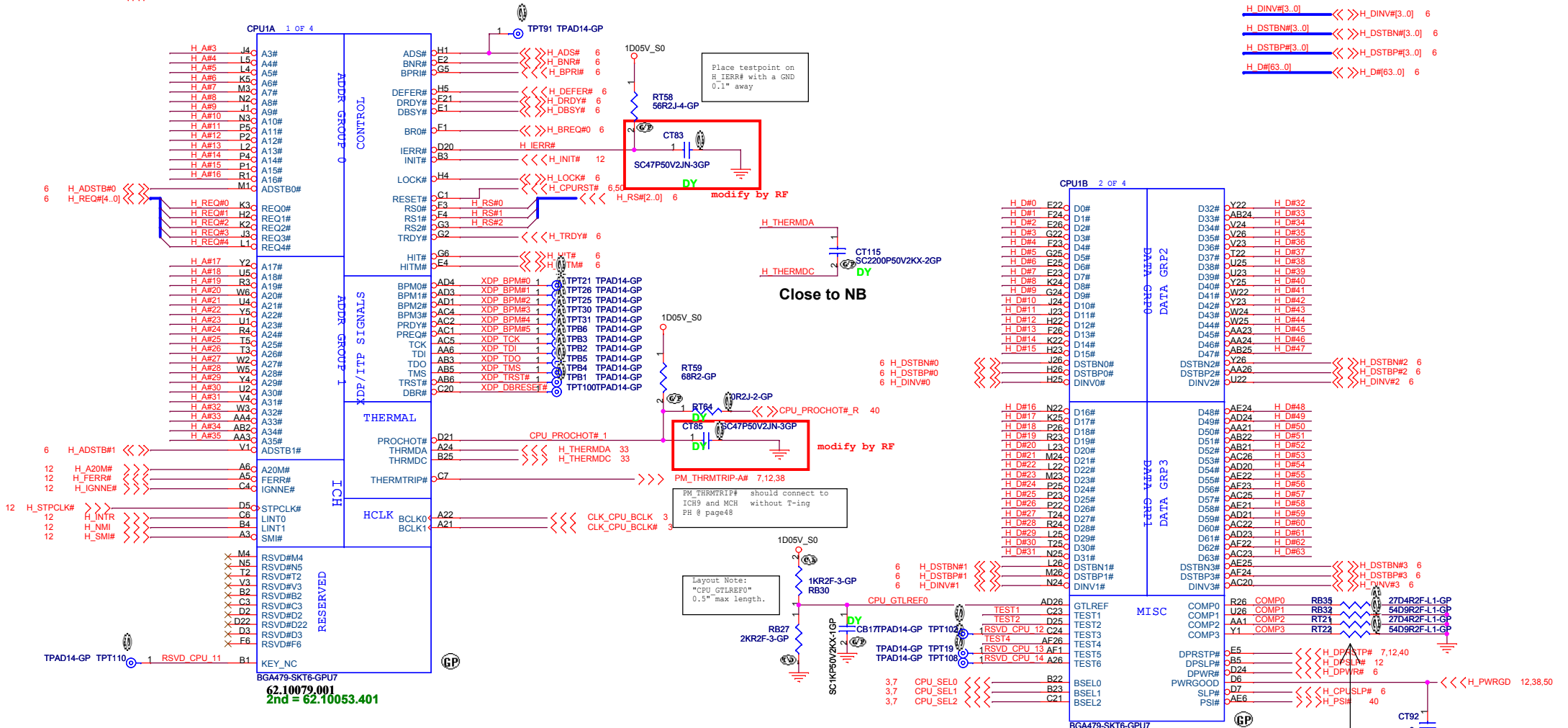
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Title: **Clock Generator**

Size	Document Number	Rev
	<b>SJV50</b>	<b>SA</b>

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6 H\_A#(35..3) <<<>> H\_A#(35..3)



6 H\_ADSTB#0 <<<>> H\_ADSTB#0  
 6 H\_REQ#(4..0) <<<>> H\_REQ#(4..0)

6 H\_ADSTB#1 <<<>> H\_ADSTB#1  
 12 H\_A20M# <<<>> H\_A20M#  
 12 H\_FERR# <<<>> H\_FERR#  
 12 H\_IGNNE# <<<>> H\_IGNNE#

12 H\_STPCLK# <<<>> H\_STPCLK#  
 12 H\_INTR <<<>> H\_INTR  
 12 H\_NMI <<<>> H\_NMI  
 12 H\_SMI# <<<>> H\_SMI#

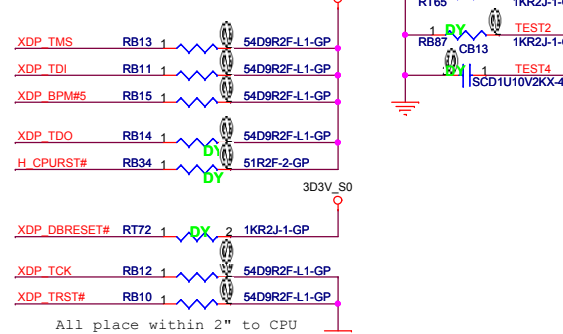
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RESERVED

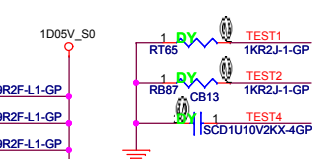
RSVD#M4 M4  
 RSVD#M5 N5  
 RSVD#T2 T2  
 RSVD#V3 V3  
 RSVD#B2 B2  
 RSVD#C3 C3  
 RSVD#D2 D2  
 RSVD#D22 D22  
 RSVD#D3 D3  
 RSVD#F6 F6

KEY\_NC

BGA479-SKT6-GPU7  
 62.10079.001  
 2nd = 62.10053.401



Layout Note:  
 "CPU\_GTLREF0"  
 0.5" max length.



Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals

H DPRSTP# 1 TPT92 TPAD14-GP  
 H DPSL# 1 TPT113 TPAD14-GP  
 H DPWR# 1 TPT95 TPAD14-GP  
 H\_PWRGD 1 TPT103 TPAD14-GP  
 H\_CPUSL# 1 TPT94 TPAD14-GP  
 H\_INIT# 1 TPT101 TPAD14-GP  
 H\_CPURST# 1 TPB7 TPAD14-GP

Place these TP on button-side, easy to measure.

Layout Note:  
 Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.1"  
 Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5"

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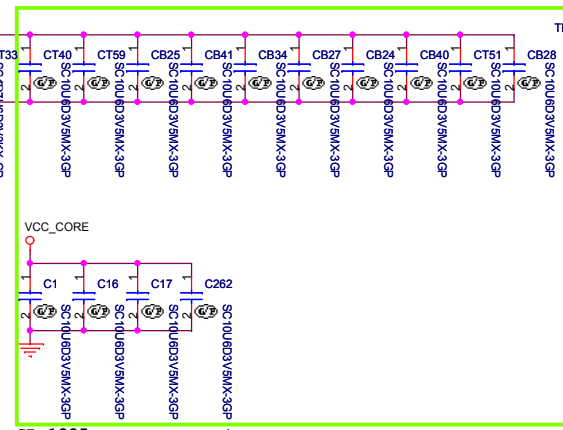
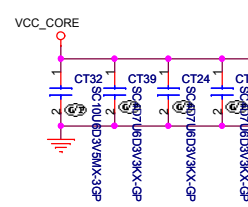
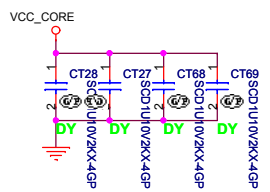
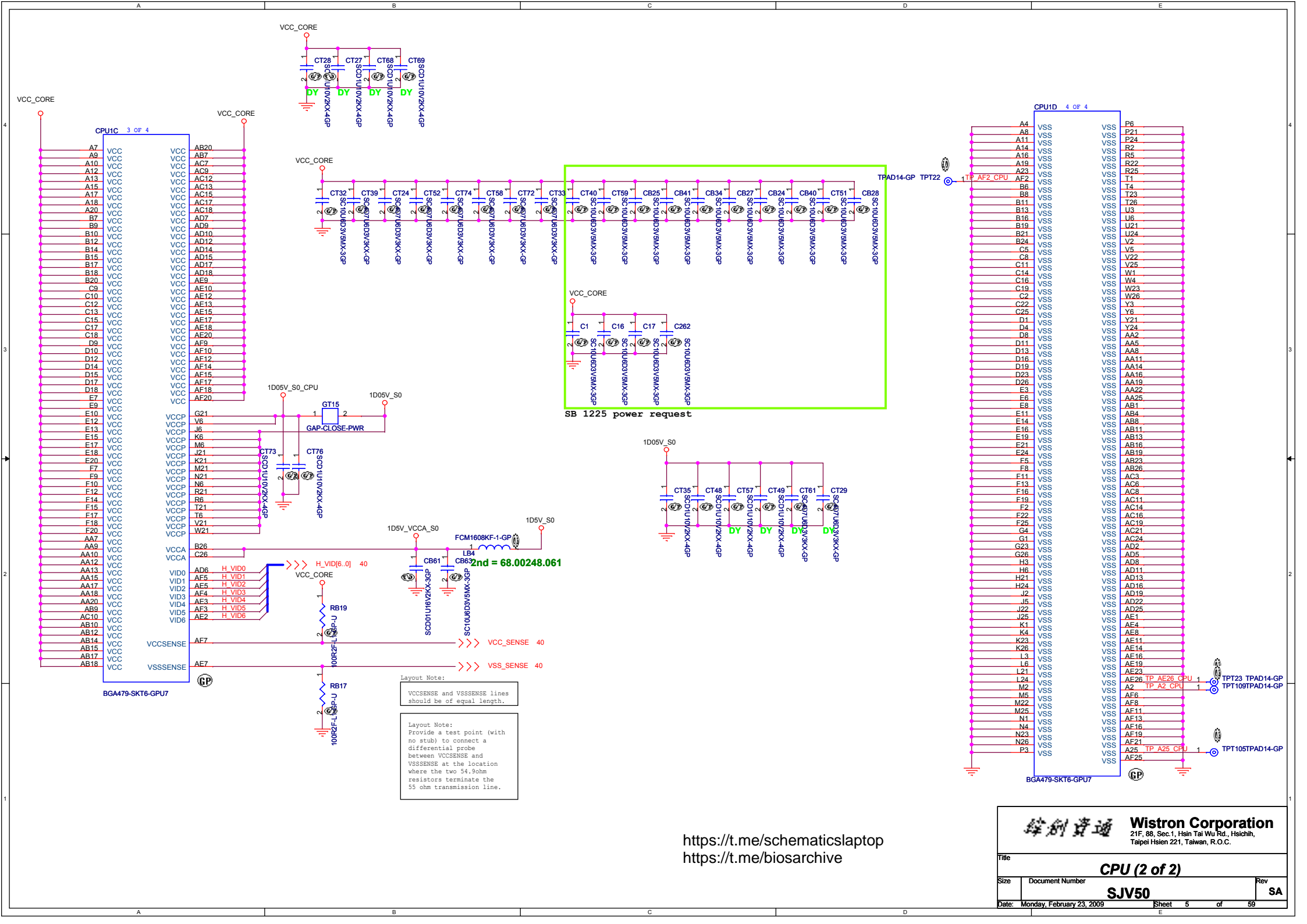
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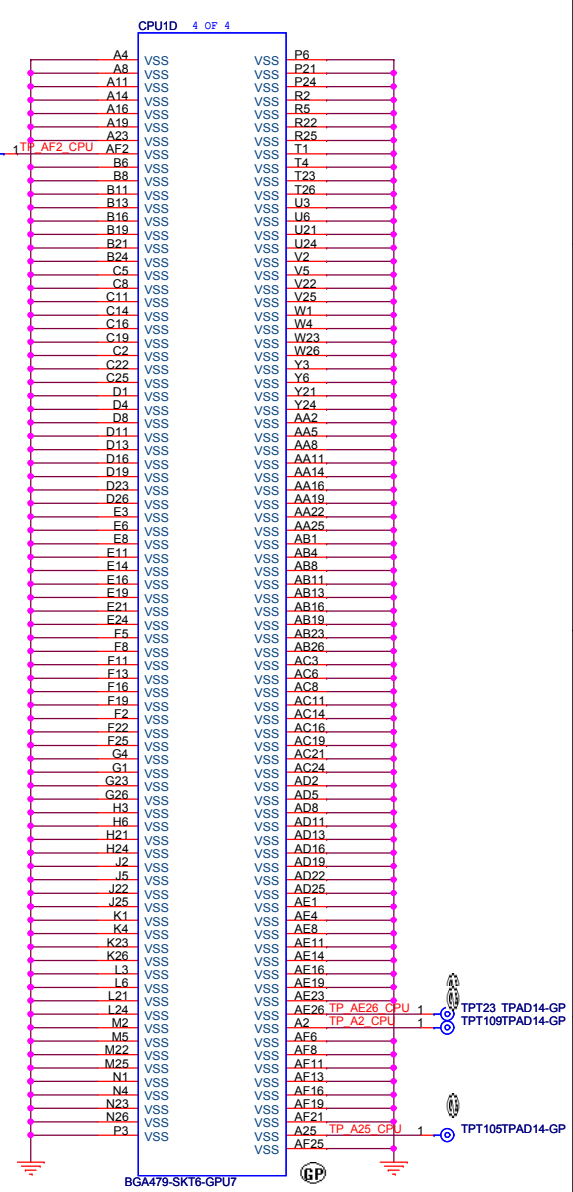
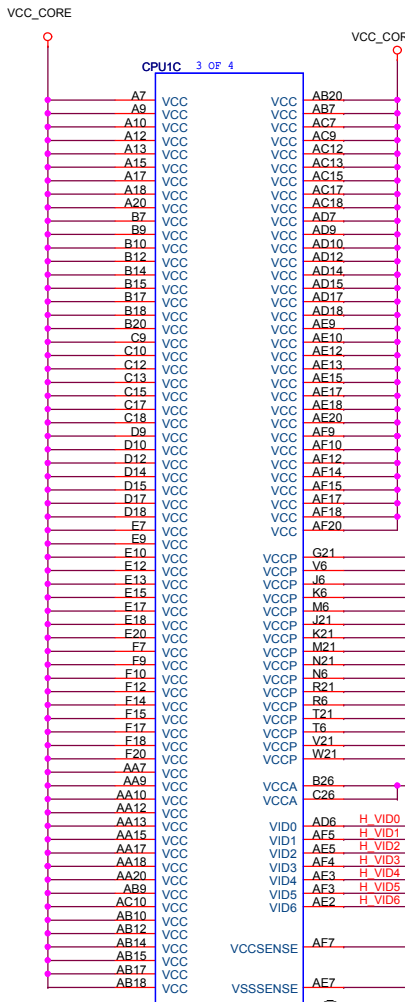
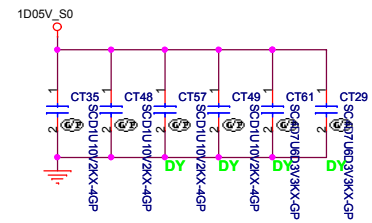
Title: CPU (1 of 2)

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		SA

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SB 1225 power request



BGA479-SKT6-GPU7

BGA479-SKT6-GPU7

Layout Note:  
 VCCSENSE and VSSSENSE lines should be of equal length.

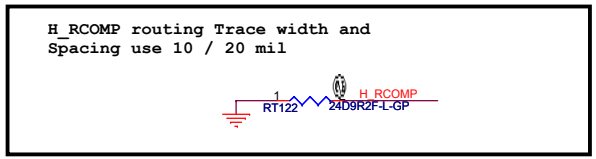
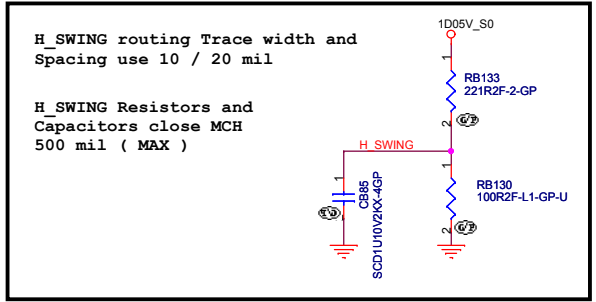
Layout Note:  
 Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.

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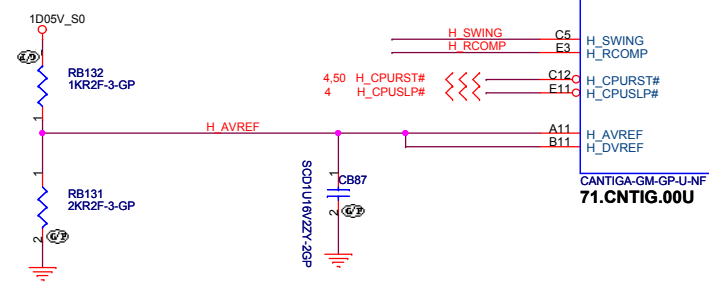
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Title		CPU (2 of 2)	
Size	Document Number	Rev	
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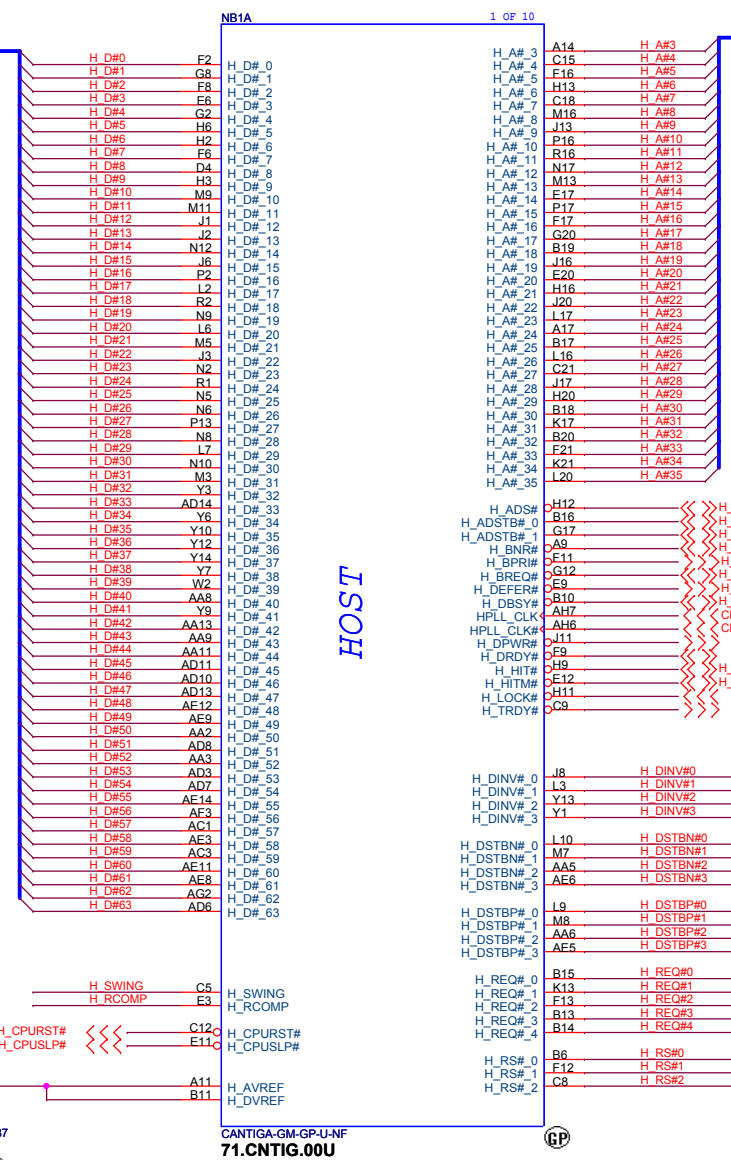
SA



Place them near to the chip ( < 0.5" )



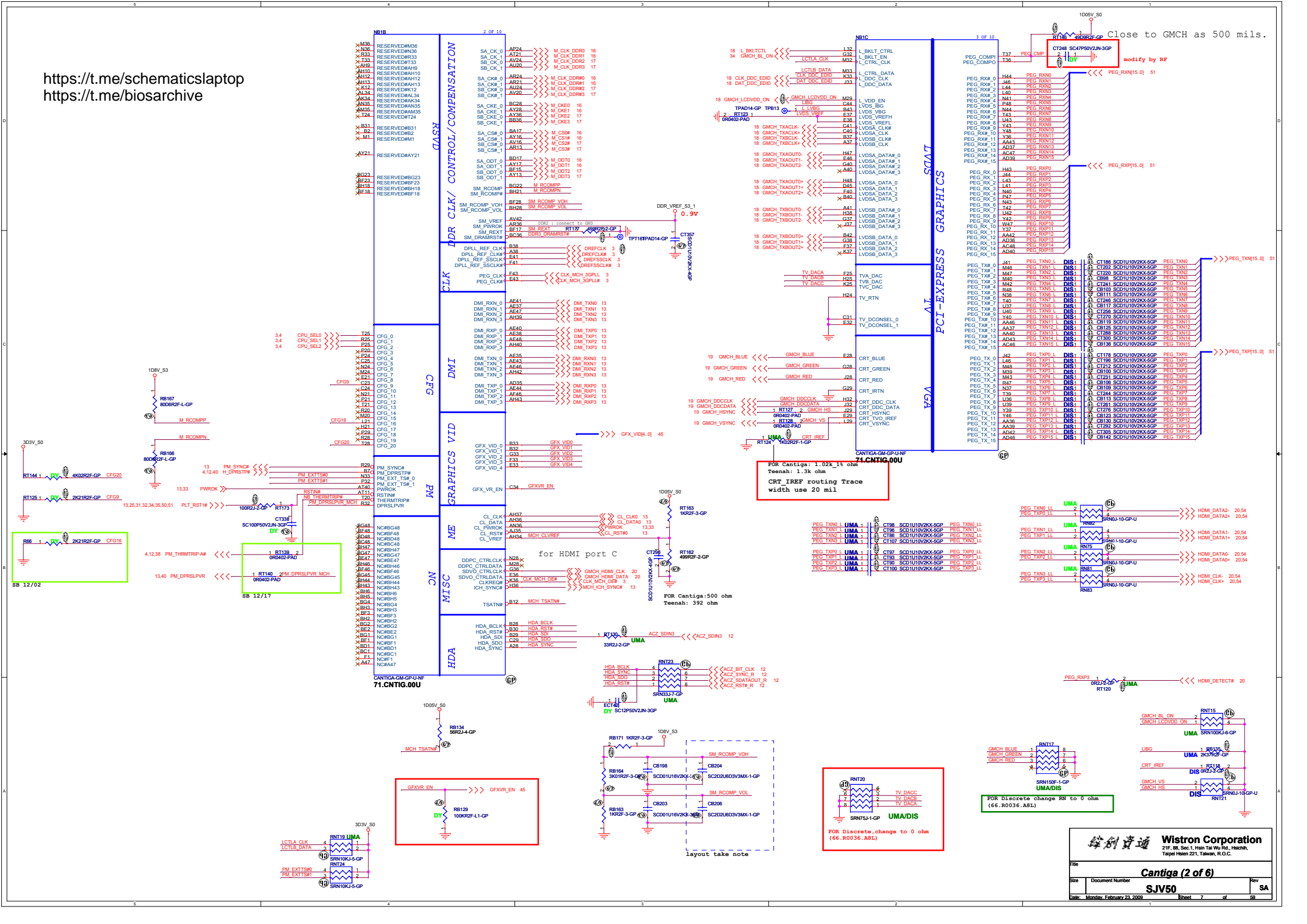
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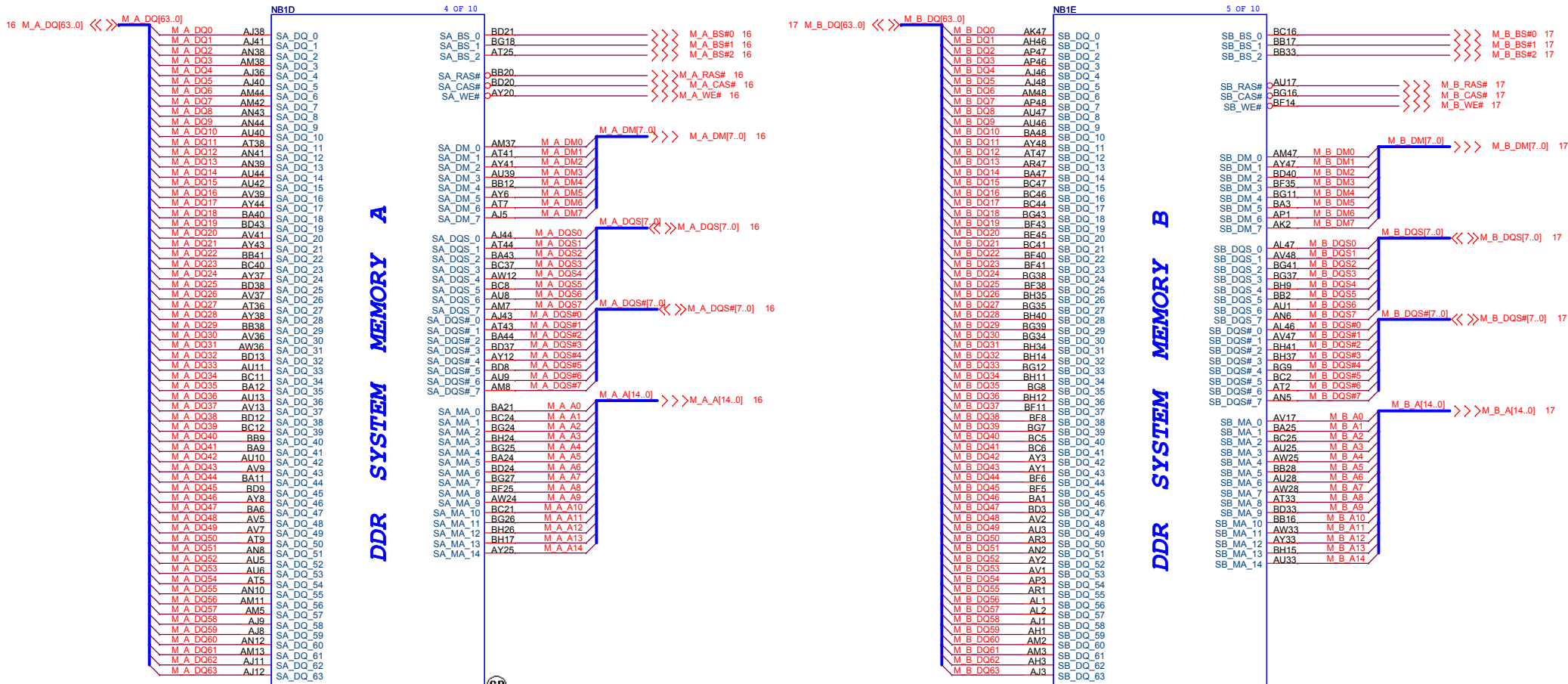


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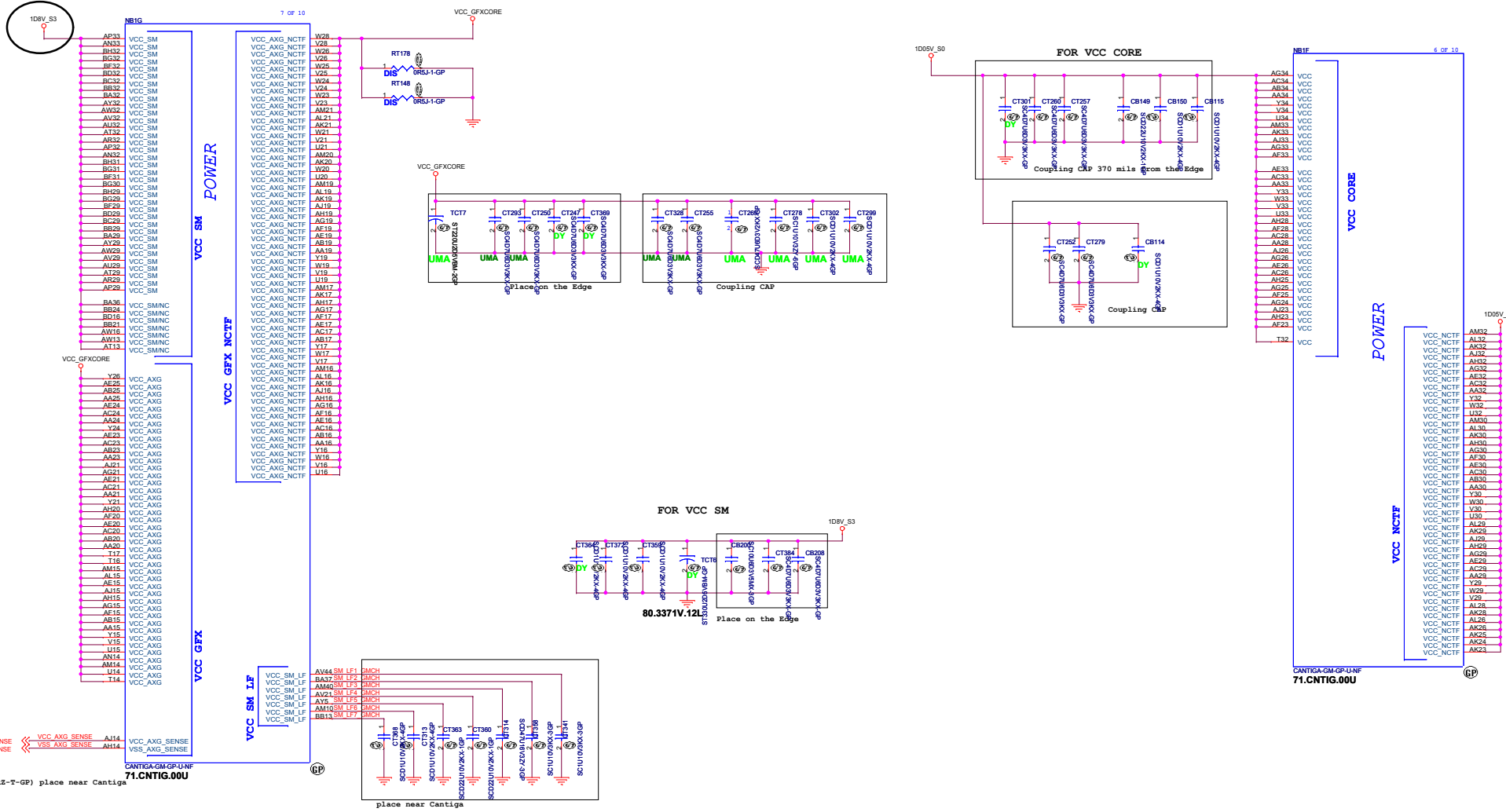




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Title: <b>Cantiga (3 of 6)</b>			
Size	Document Number	Rev	SA
<b>SJV50</b>			
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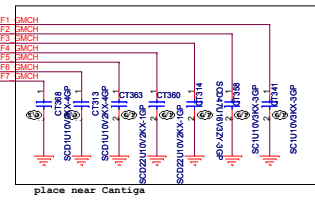




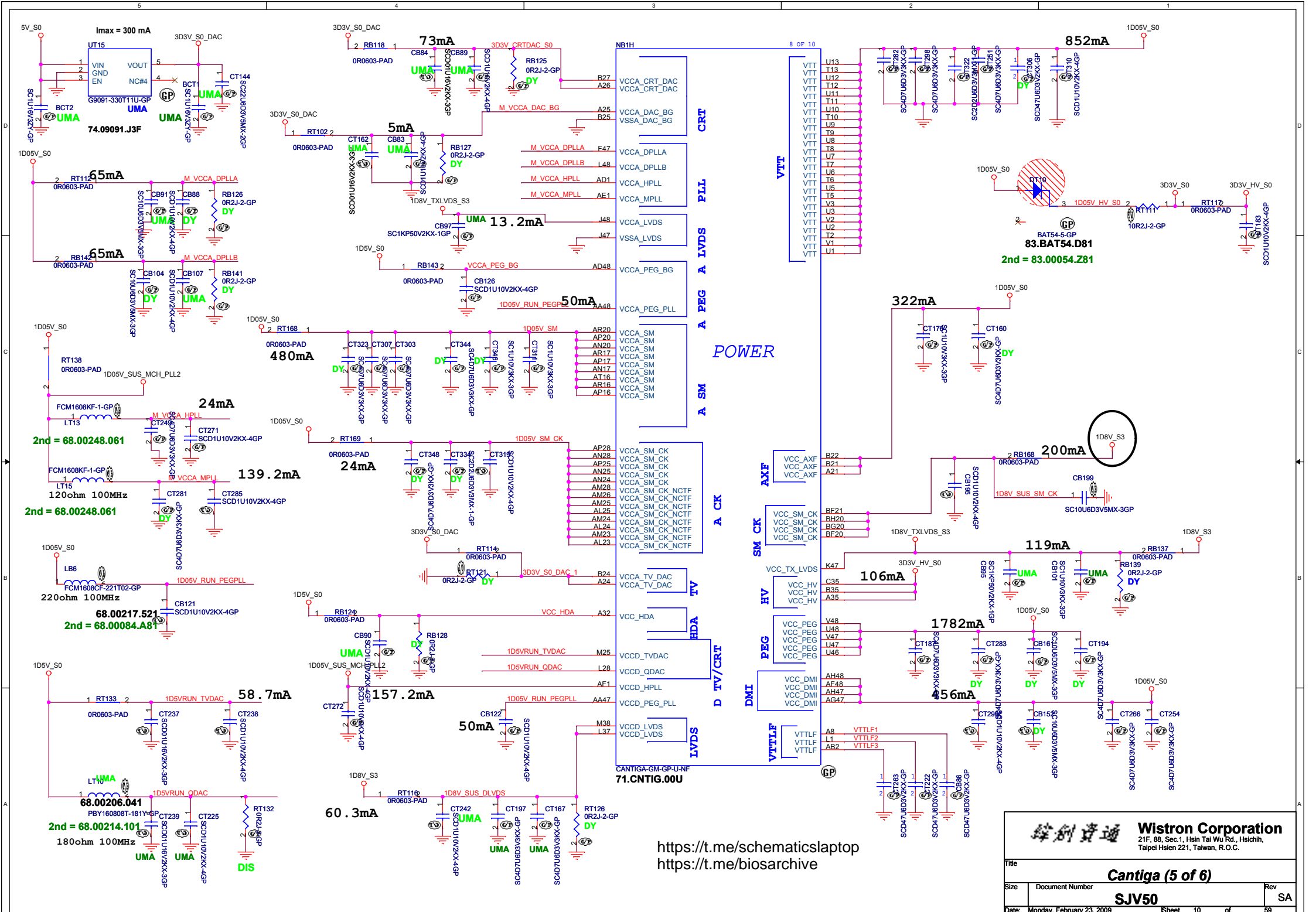
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 45 VSS\_AKG\_SENSE ← VSS\_AKG\_SENSE AH14

CANTIGA-GM-GP-L1NF  
**71.CNTIG.00U**

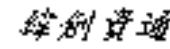
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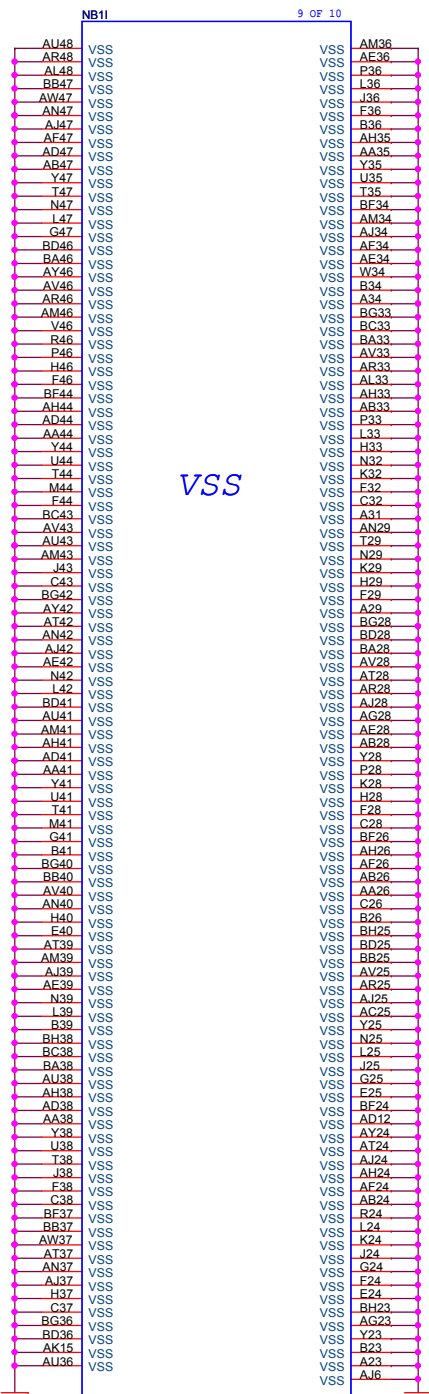
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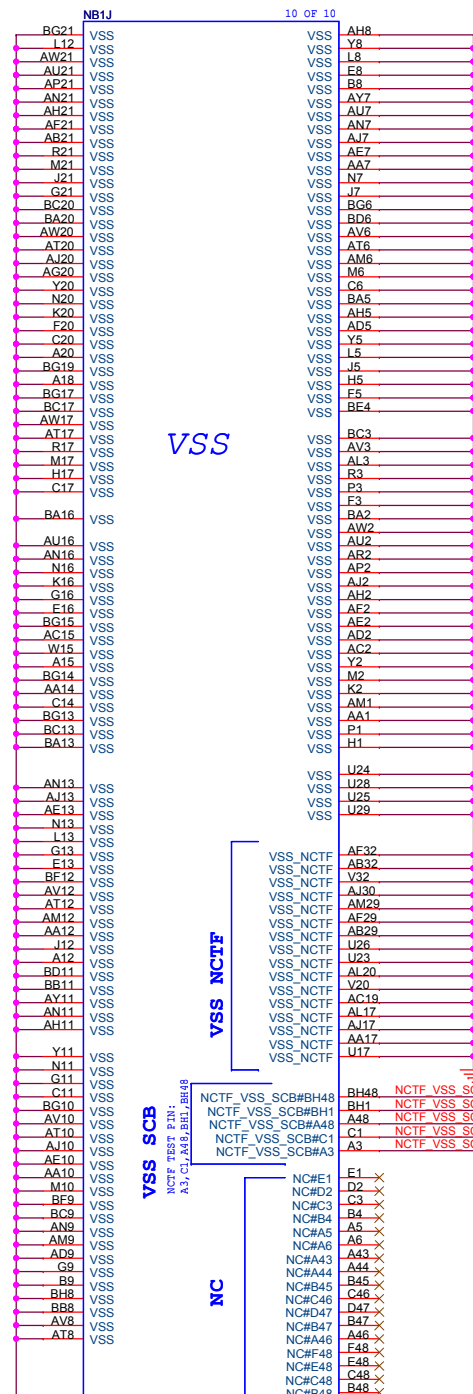
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<b>Cantiga (5 of 6)</b>		Rev
Title	<b>SJV50</b>	SA
Size	Document Number	Rev
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CANTIGA-GM-GP-U-NF  
**71.CNTIG.00U**

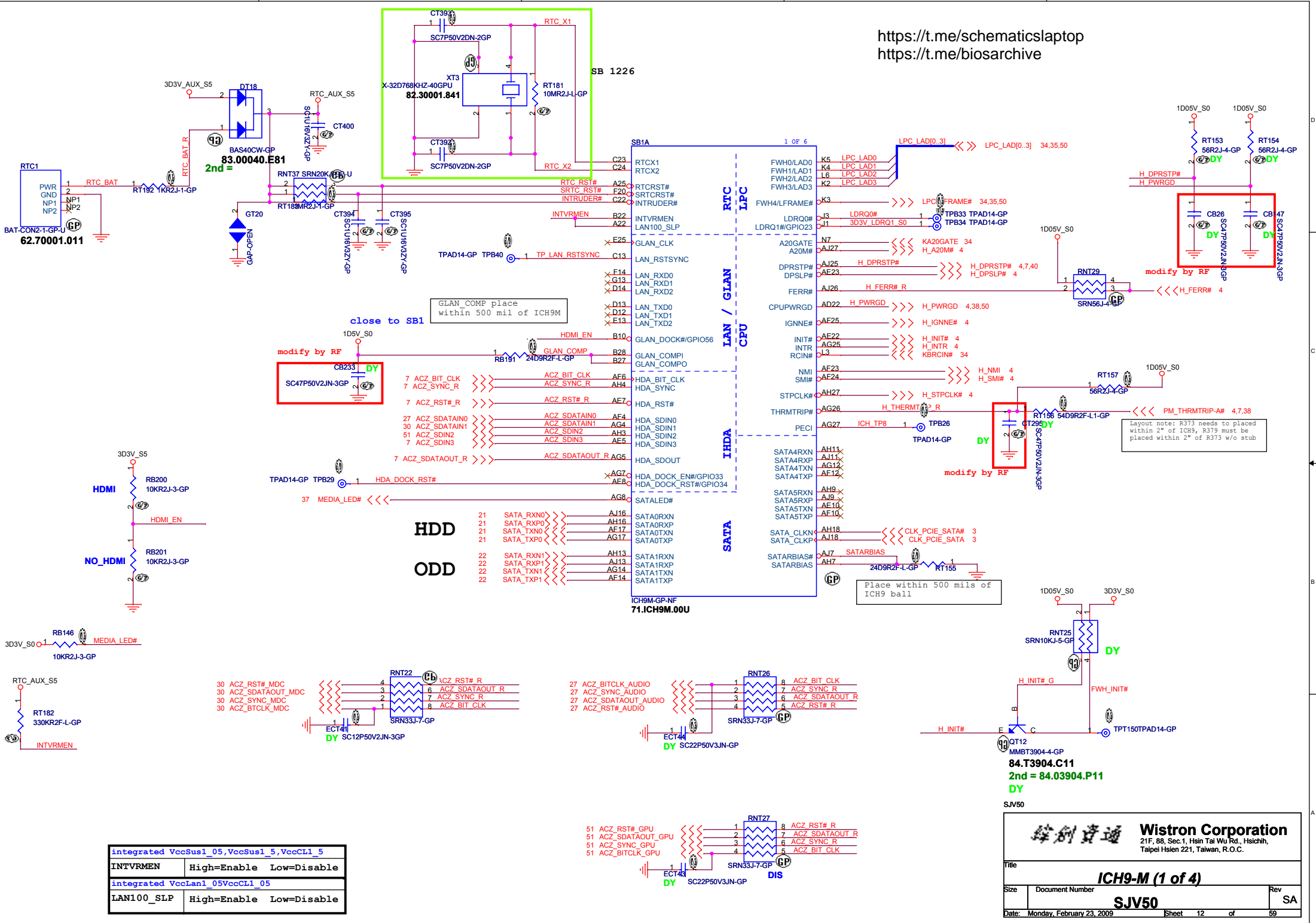


CANTIGA-GM-GP-U-NF  
**71.CNTIG.00U**

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Title		<b>Cantiga (6 of 6)</b>	
Size	Document Number	Rev	SA
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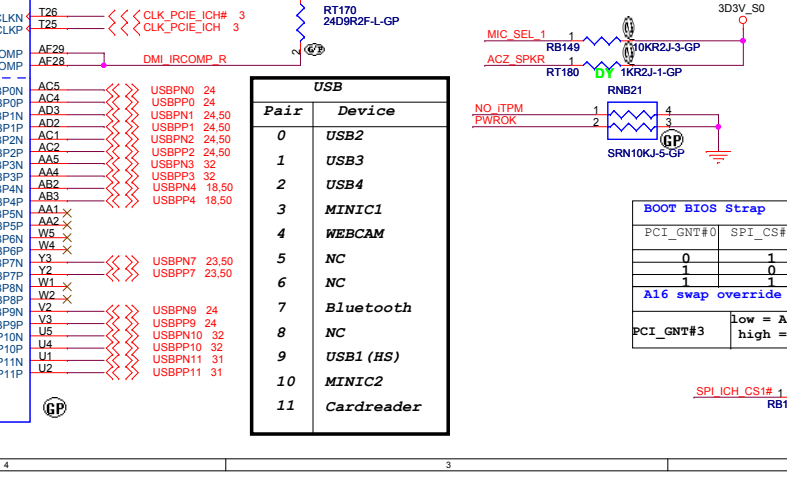
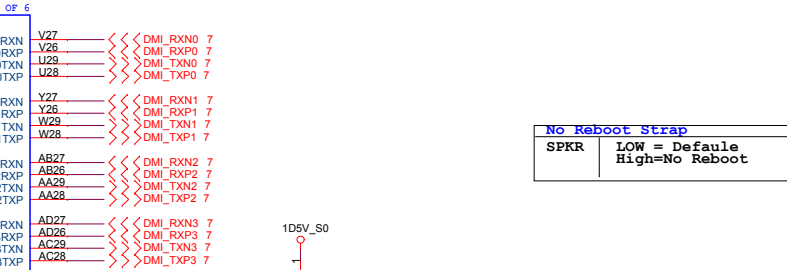
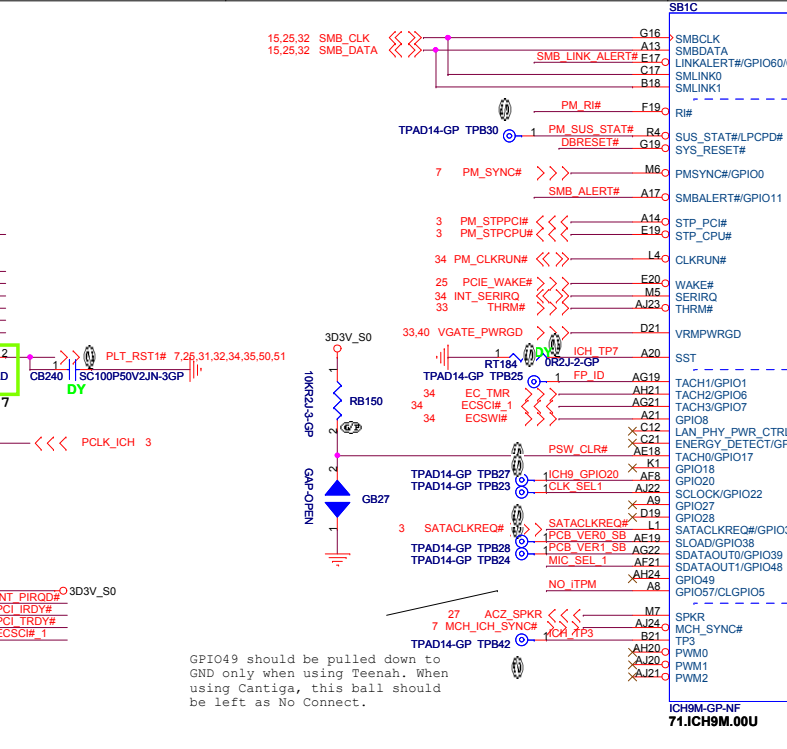
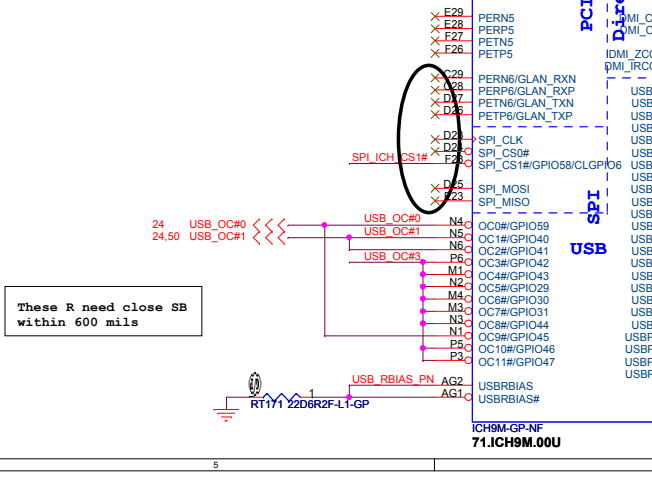
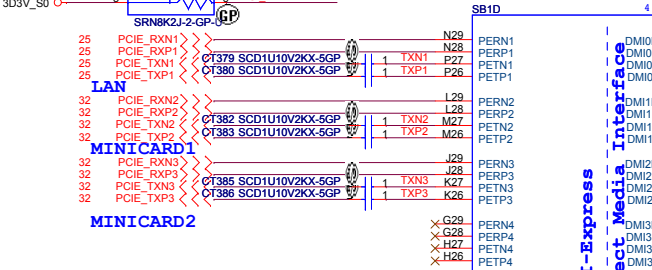
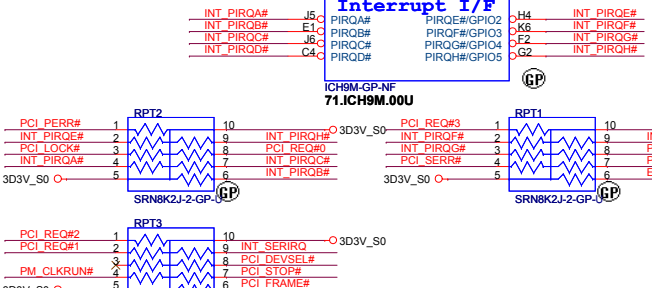
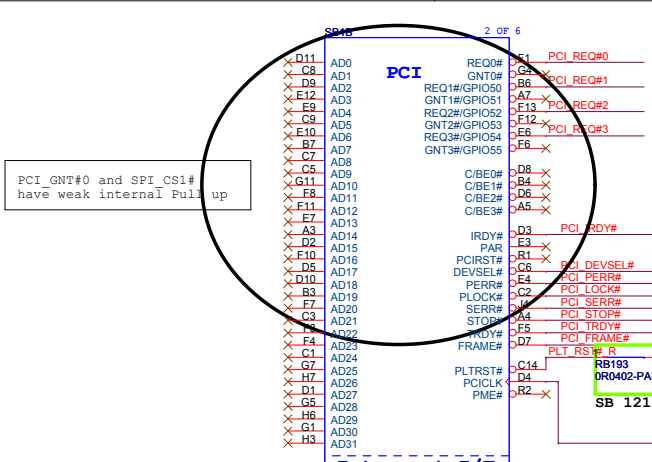
integrated VccSus1_05,VccSus1_5,VccCl1_5		
INTVRMEN	High=Enable	Low=Disable
integrated VccLan1_05VccCl1_05		
LAN100_SLP	High=Enable	Low=Disable

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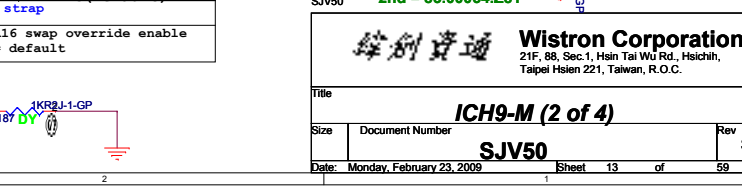
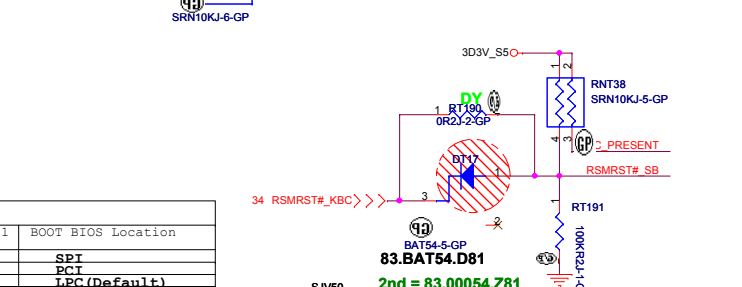
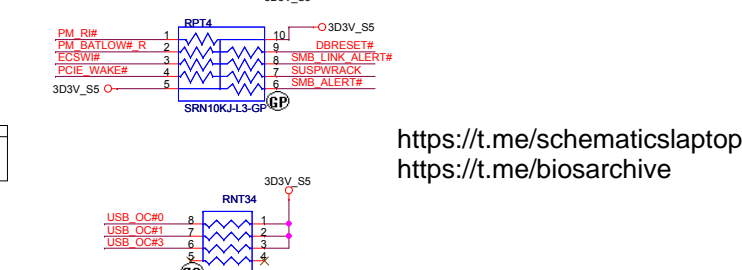
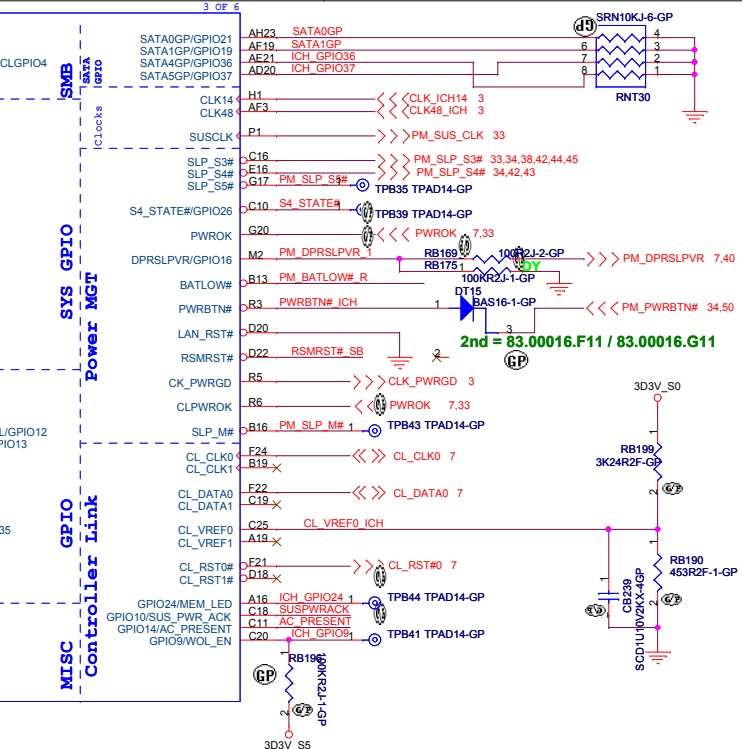
Title: **ICH9-M (1 of 4)**

Size: Document Number **SJV50** Rev: SA

Date: Monday, February 23, 2009 Sheet 12 of 59



Pair	Device
0	USB2
1	USB3
2	USB4
3	MINIC1
4	WEBCAM
5	NC
6	NC
7	Bluetooth
8	NC
9	USB1 (HS)
10	MINIC2
11	Cardreader



83.BAT54.D81  
2nd = 83.00054.281

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ICH9-M (2 of 4)  
SJV50  
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These R need close SB within 600 mils

GPIO49 should be pulled down to GND only when using Teenah. When using Cantiga, this ball should be left as No Connect.

No Reboot Strap  
SPKR Low = Default High = No Reboot

BOOT BIOS Strap  
PCI\_GNT#0 SPI\_CS#1 BOOT BIOS Location  
0 0 SPT  
1 0 PCI  
1 1 IPC (Default)  
A16 swap override strap  
low = A16 swap override enable  
high = default

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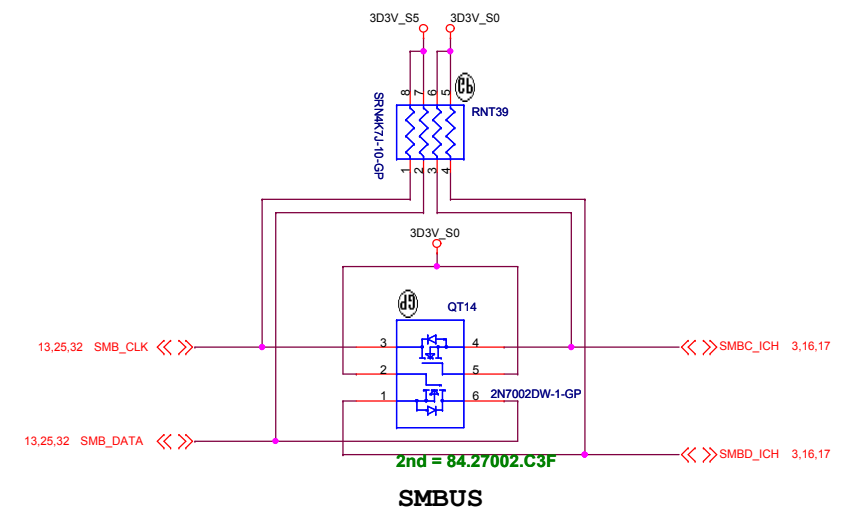


SB1E	5 OF 6				
AA26	VSS	VSS	J23	H5	
AA27	VSS	VSS	J26		
AA3	VSS	VSS	J27		
AA6	VSS	VSS	AC22		
AB1	VSS	VSS	K28		
AA23	VSS	VSS	K29		
AB28	VSS	VSS	L13		
AB29	VSS	VSS	L15		
AB4	VSS	VSS	L2		
AB5	VSS	VSS	L26		
AC17	VSS	VSS	L27		
AC26	VSS	VSS	L5		
AC27	VSS	VSS	L7		
AD3	VSS	VSS	M12		
AD1	VSS	VSS	M13		
AD10	VSS	VSS	M14		
AD12	VSS	VSS	M15		
AD13	VSS	VSS	M16		
AD14	VSS	VSS	M17		
AD17	VSS	VSS	M23		
AD18	VSS	VSS	M28		
AD21	VSS	VSS	M29		
AD28	VSS	VSS	N11		
AD29	VSS	VSS	N12		
AD4	VSS	VSS	N13		
AD5	VSS	VSS	N14		
AD6	VSS	VSS	N15		
AD7	VSS	VSS	N16		
AD9	VSS	VSS	N17		
AE12	VSS	VSS	N18		
AE13	VSS	VSS	N26		
AE14	VSS	VSS	N27		
AE16	VSS	VSS	P12		
AE17	VSS	VSS	P13		
AE2	VSS	VSS	P14		
AE20	VSS	VSS	P15		
AE24	VSS	VSS	P16		
AE3	VSS	VSS	P17		
AE4	VSS	VSS	P2		
AE6	VSS	VSS	P23		
AE9	VSS	VSS	P28		
AE13	VSS	VSS	P29		
AF16	VSS	VSS	P4		
AF18	VSS	VSS	P7		
AF22	VSS	VSS	R11		
AH26	VSS	VSS	R12		
AF28	VSS	VSS	R13		
AF27	VSS	VSS	R14		
AF5	VSS	VSS	R15		
AF7	VSS	VSS	R16		
AF9	VSS	VSS	R17		
AG13	VSS	VSS	R18		
AG16	VSS	VSS	R28		
AG18	VSS	VSS	T12		
AG20	VSS	VSS	T13		
AG23	VSS	VSS	T14		
AG3	VSS	VSS	T15		
AG6	VSS	VSS	T16		
AG9	VSS	VSS	T17		
AH12	VSS	VSS	T24		
AH14	VSS	VSS	B26		
AH17	VSS	VSS	U12		
AH19	VSS	VSS	U13		
AH2	VSS	VSS	U14		
AH22	VSS	VSS	U15		
AH25	VSS	VSS	U16		
AH28	VSS	VSS	U17		
AH5	VSS	VSS	AD23		
AH8	VSS	VSS	U26		
AJ12	VSS	VSS	U27		
AJ14	VSS	VSS	U3		
AJ17	VSS	VSS	V1		
AJ8	VSS	VSS	V13		
B11	VSS	VSS	V15		
B14	VSS	VSS	V23		
B17	VSS	VSS	V28		
B2	VSS	VSS	V29		
B20	VSS	VSS	V4		
B23	VSS	VSS	V5		
B5	VSS	VSS	W26		
B8	VSS	VSS	W27		
C26	VSS	VSS	W3		
C27	VSS	VSS	Y1		
E11	VSS	VSS	Y28		
E14	VSS	VSS	Y29		
E16	VSS	VSS	Y4		
E2	VSS	VSS	Y5		
E21	VSS	VSS	AG28		
E24	VSS	VSS	AH6		
E5	VSS	VSS	AF2		
E8	VSS	VSS	B25		
F16	VSS	VSS			
F28	VSS	VSS			
F29	VSS	VSS			
G12	VSS	VSS			
G14	VSS	VSS			
G18	VSS	VSS			
G21	VSS	VSS			
G24	VSS	VSS			
G26	VSS	VSS			
G27	VSS	VSS			
G8	VSS	VSS			
H2	VSS	VSS			
H23	VSS	VSS			
H28	VSS	VSS			
H29	VSS	VSS			

NCTF_VSS#A1	A1	TP A1	1	TPT175TPAD14-GP
NCTF_VSS#A2	A2	TP A2	1	TPT176TPAD14-GP
NCTF_VSS#B1	B1	TP B1	1	TPT172TPAD14-GP
NCTF_VSS#A29	A29	TP A29	1	TPT173TPAD14-GP
NCTF_VSS#A28	A28	TP A28	1	TPT174TPAD14-GP
NCTF_VSS#B29	B29	TP B29	1	TPT168TPAD14-GP
NCTF_VSS#B28	B28	TP B28	1	TPT152TPAD14-GP
NCTF_VSS#AJ1	AJ1	TP AJ1	1	TPT156TPAD14-GP
NCTF_VSS#AJ2	AJ2	TP AJ2	1	TPT160TPAD14-GP
NCTF_VSS#AH1	AH1	TP AH1	1	TPT157TPAD14-GP
NCTF_VSS#AJ28	AJ28	TP AJ28	1	TPT155TPAD14-GP
NCTF_VSS#AJ29	AJ29	TP AJ29	1	TPT159TPAD14-GP
NCTF_VSS#AH29	AH29	TP AH29	1	

ICH9M-GP-NF  
71.ICH9M.00U

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ICH9-M (4 of 4)  
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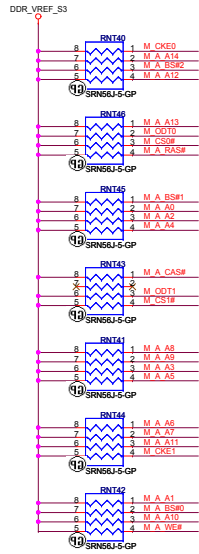
Monday, February 23, 2009

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SA

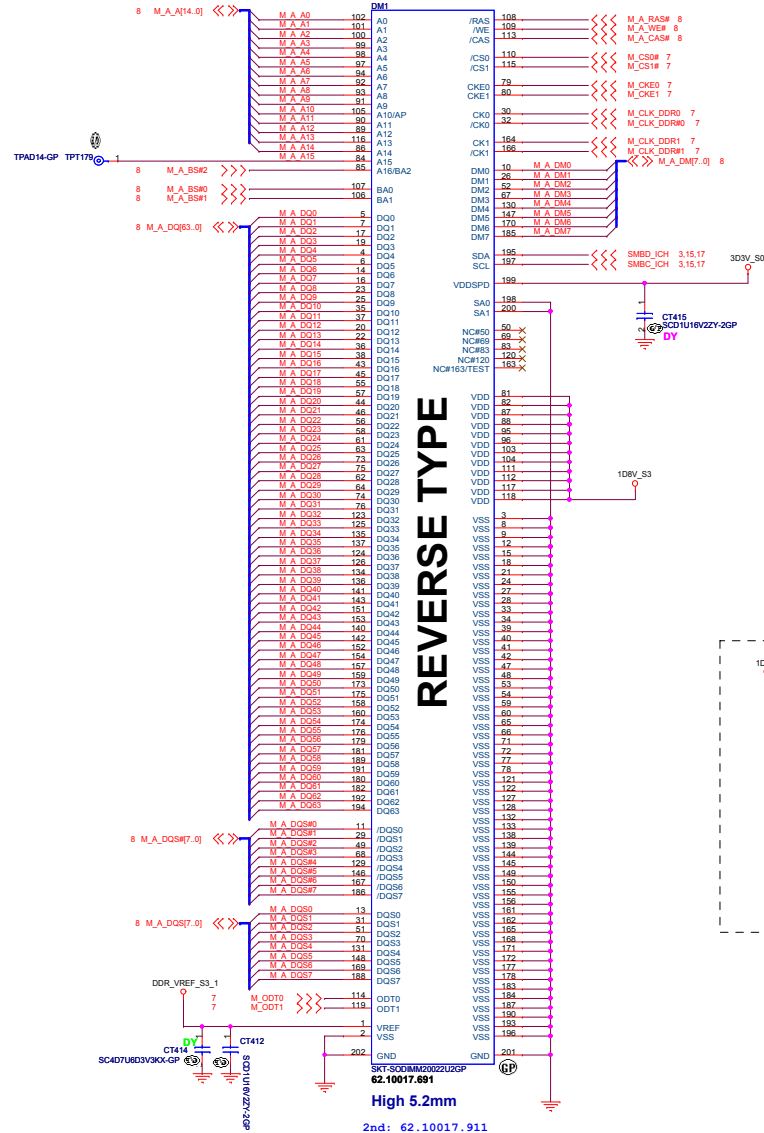
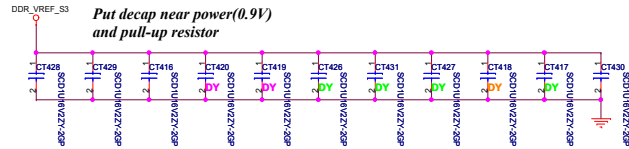
# PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

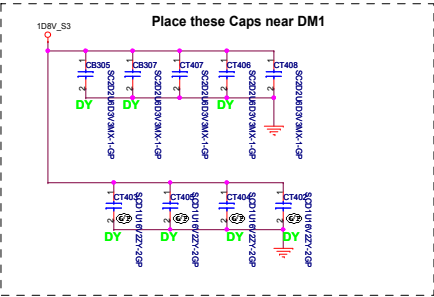


## Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor



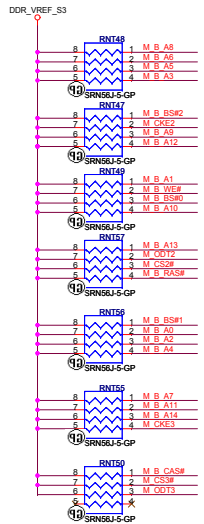
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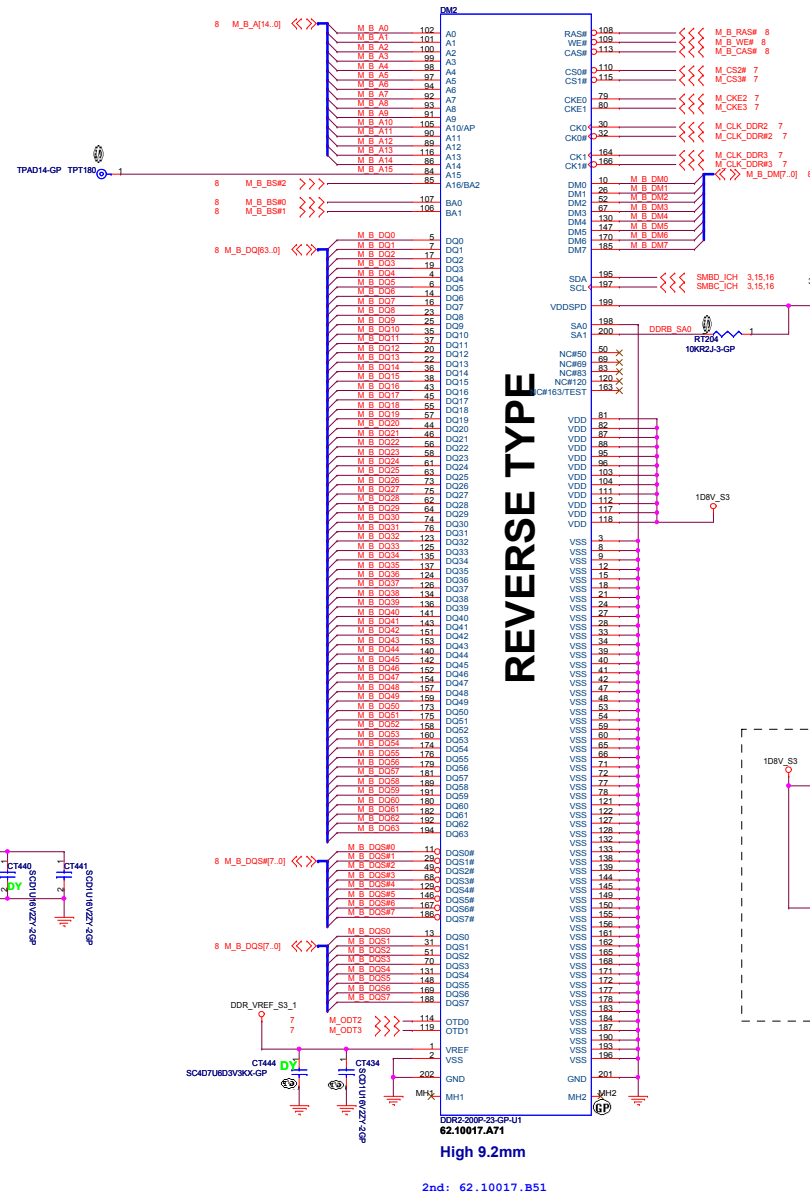
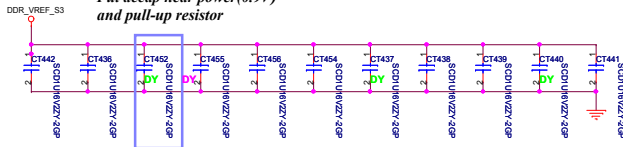
# PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

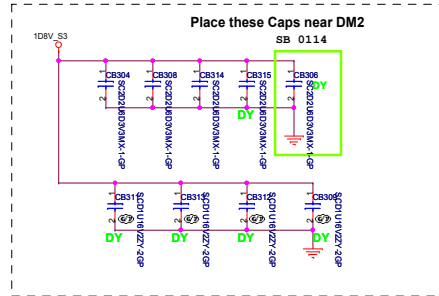


## Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor



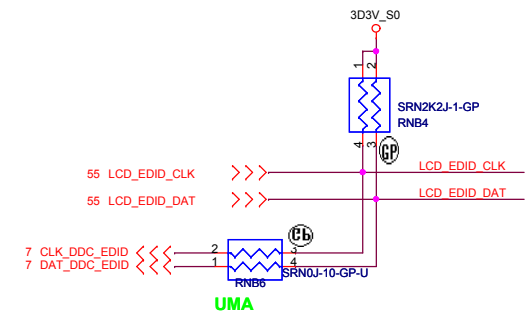
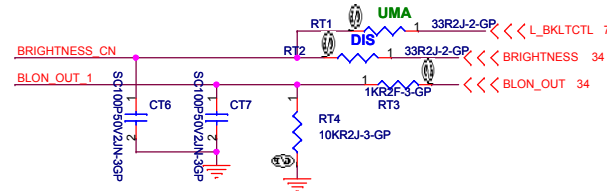
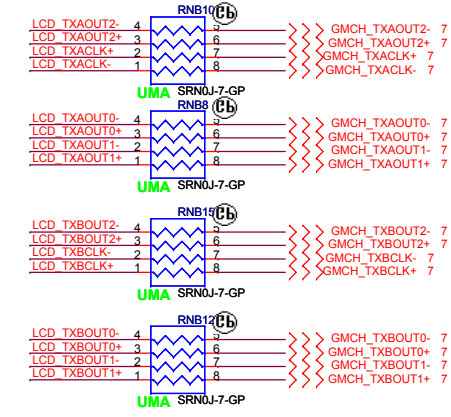
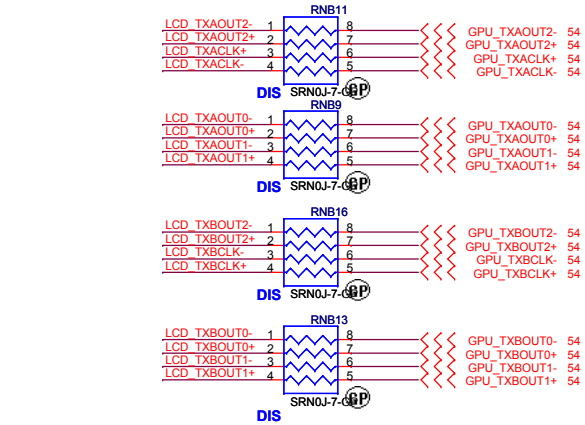
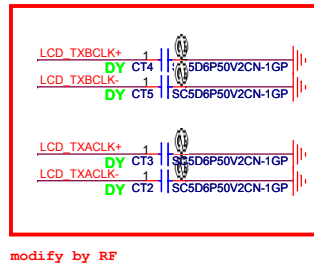
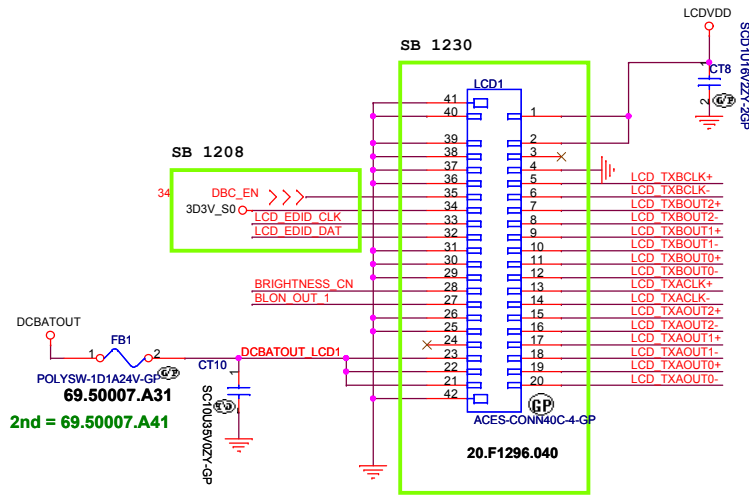
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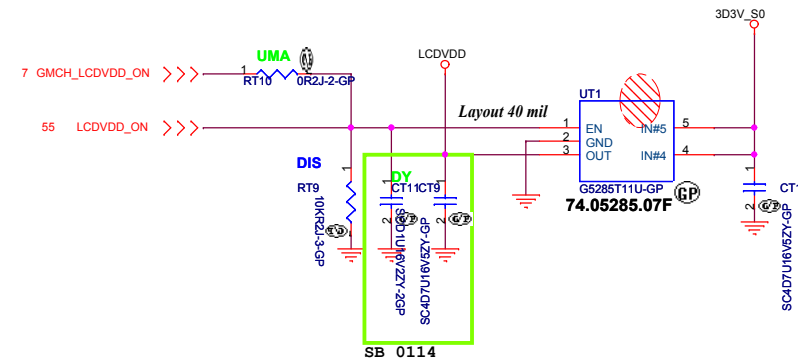
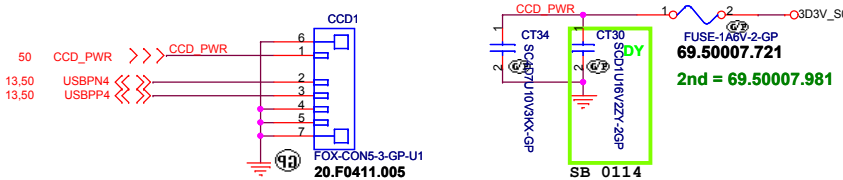
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# LCD/INVERTER/CCD CONN

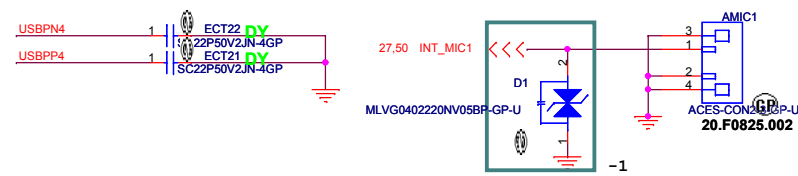
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## CCD



## Internal Mic



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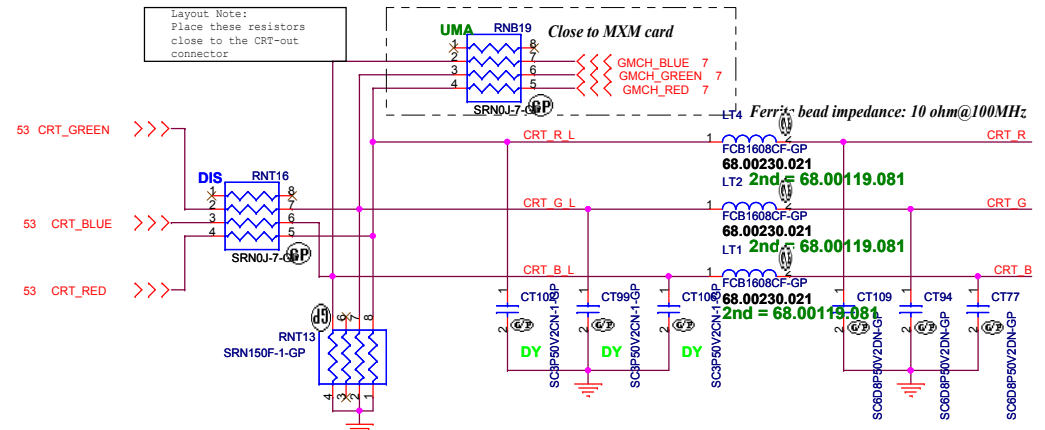
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 Taipei Hsien 221, Taiwan, R.O.C.

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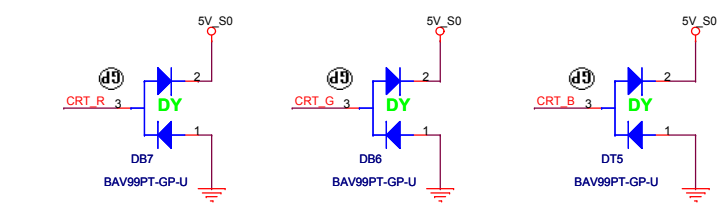
Size	Document Number	Rev
	<b>SJV50</b>	SA

Date: Monday, February 23, 2009 Sheet 18 of 59

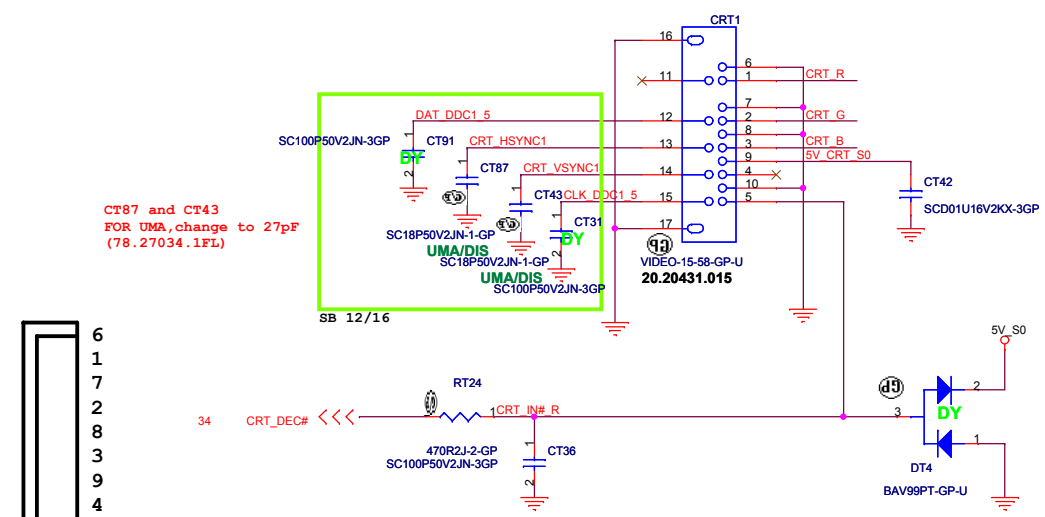




**Layout Note:**  
 \* Must be a ground return path between this ground and the ground on the VGA connector.  
 Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

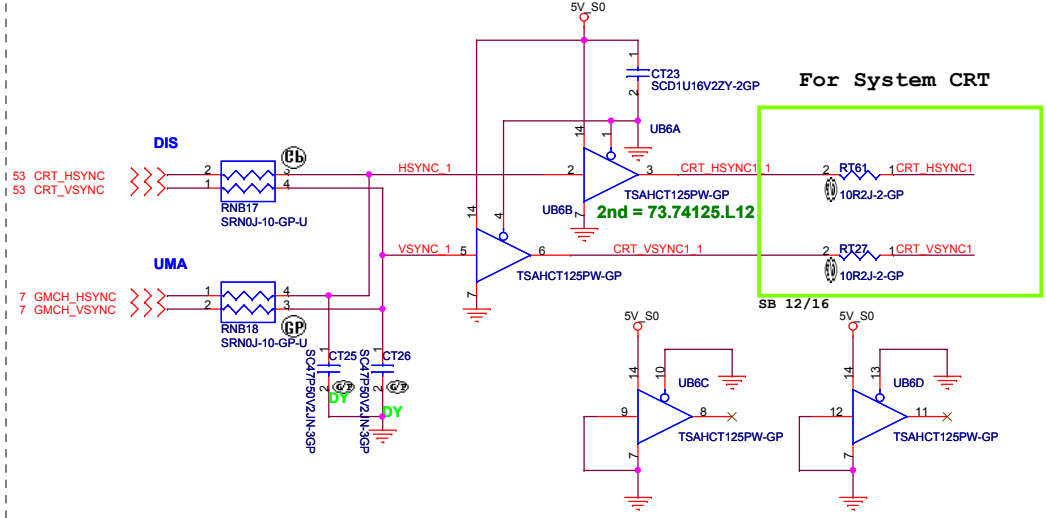


### CRT I/F & CONNECTOR

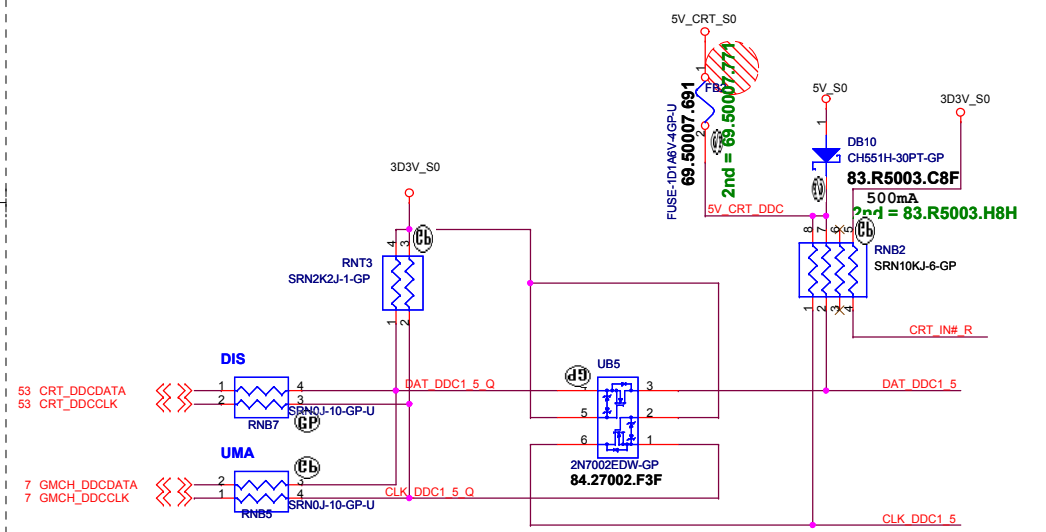


- 6
- 7
- 2
- 8
- 3
- 9
- 4
- 10
- 5

### Hsync & Vsync level shift



### DDC\_CLK & DATA level shift



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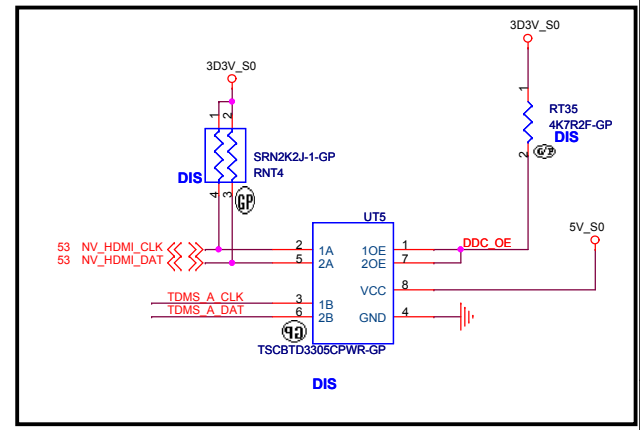
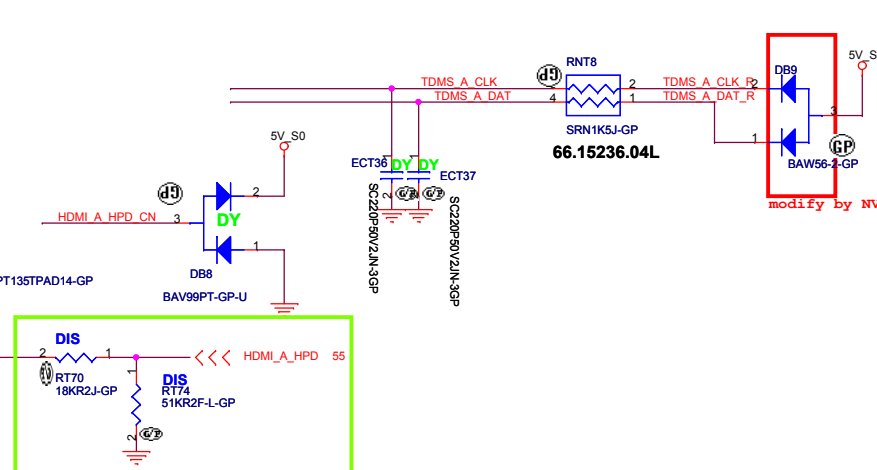
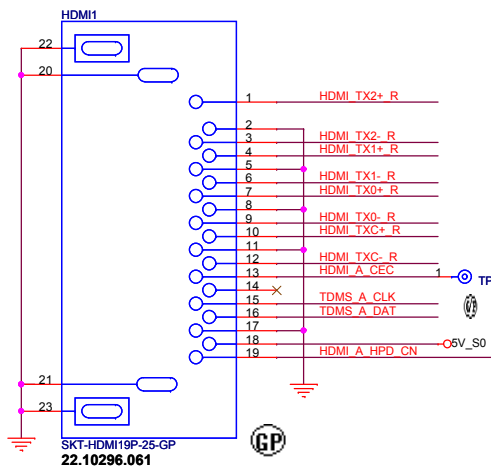
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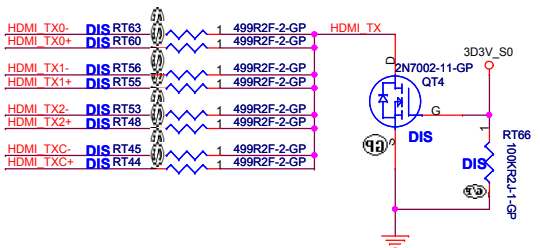
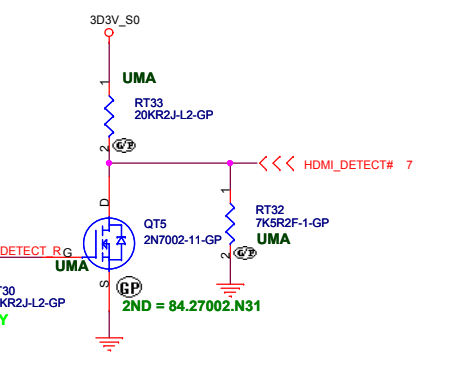
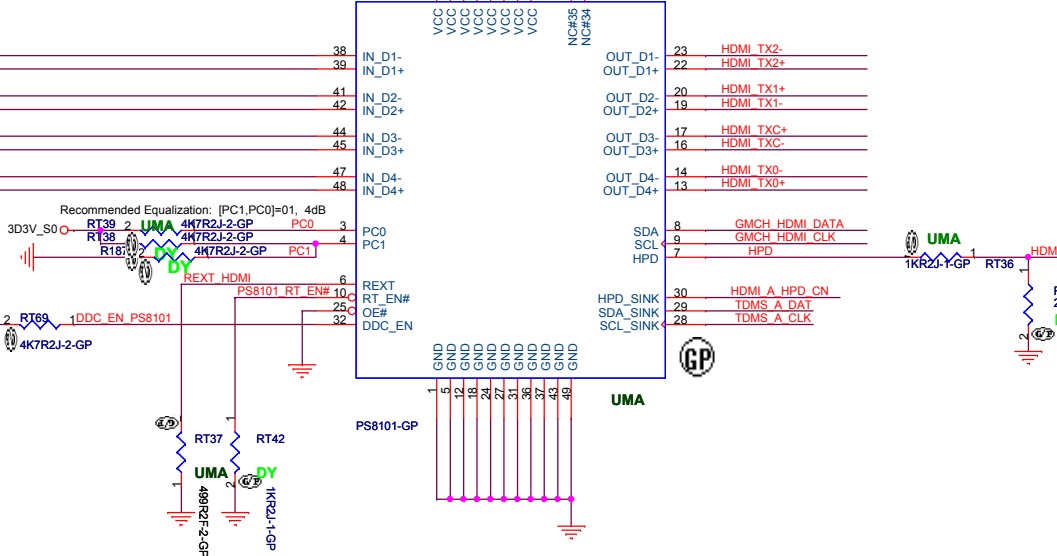
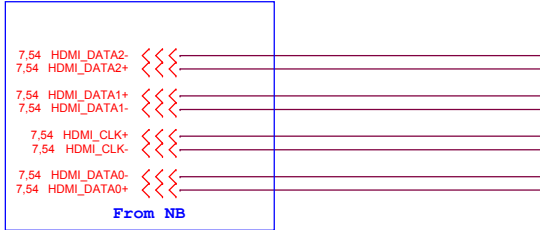
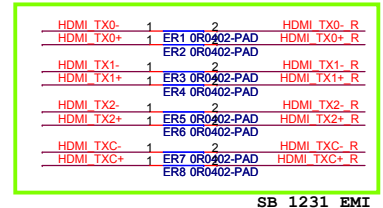
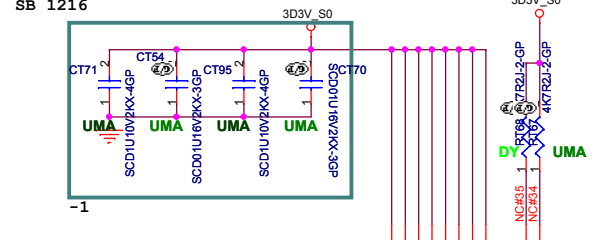
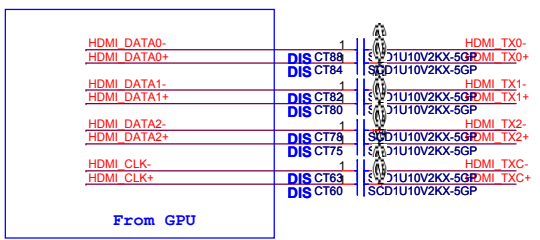
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Size Document Number **SJV50** Rev SA

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Close U6



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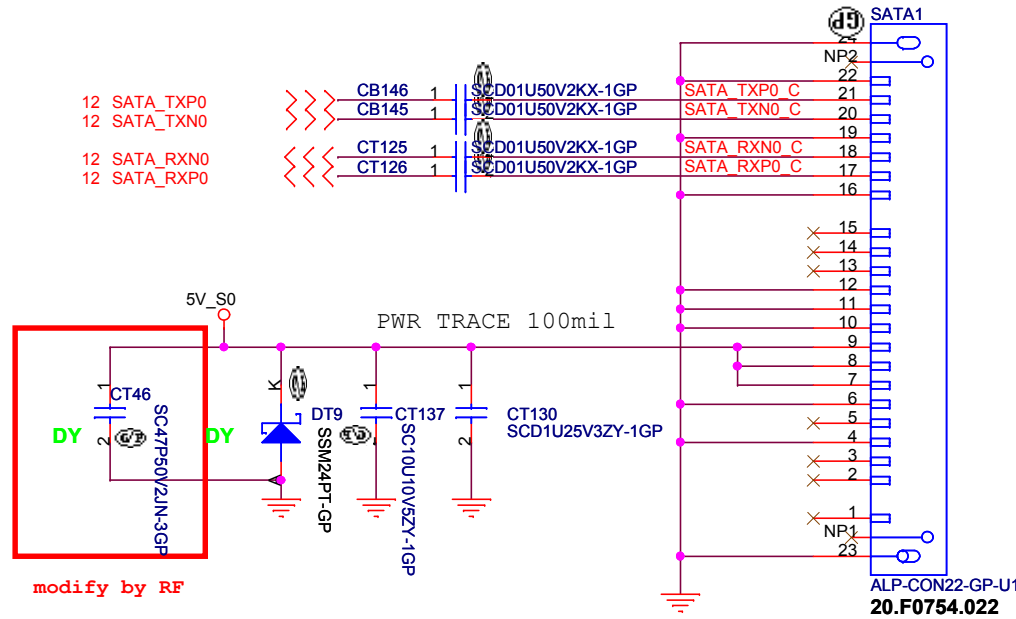
**HDMI CONNECTOR**

File: **SJV50**

Size: A3 | Document Number: **SJV50** | Rev: **SA**

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# SATA Connector

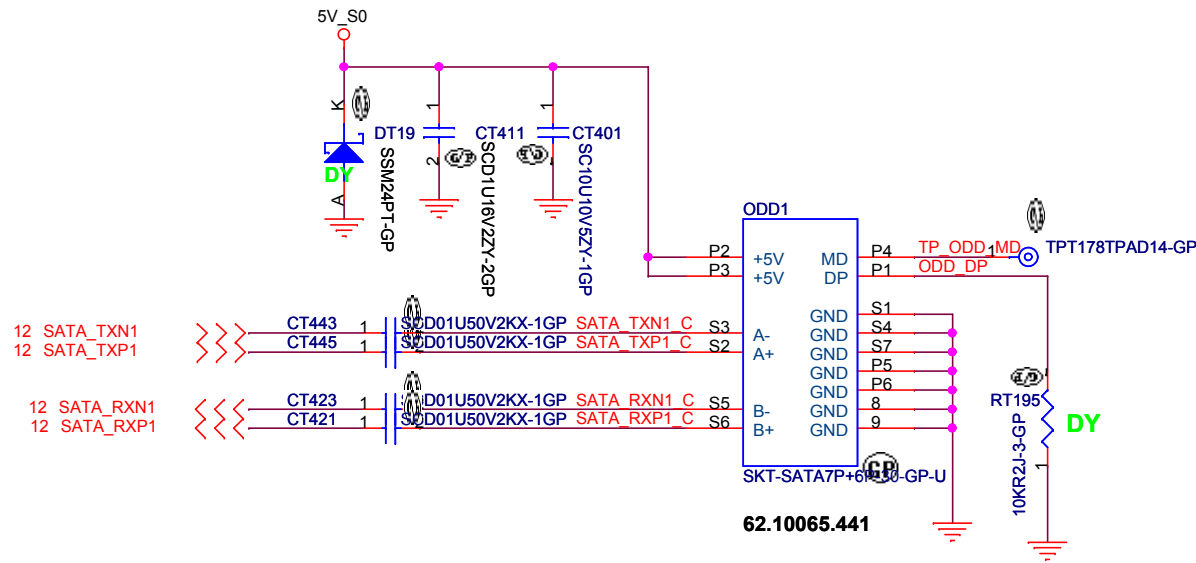


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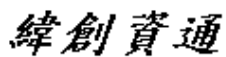
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	<b>SJV50</b>	SA
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# ODD Connector

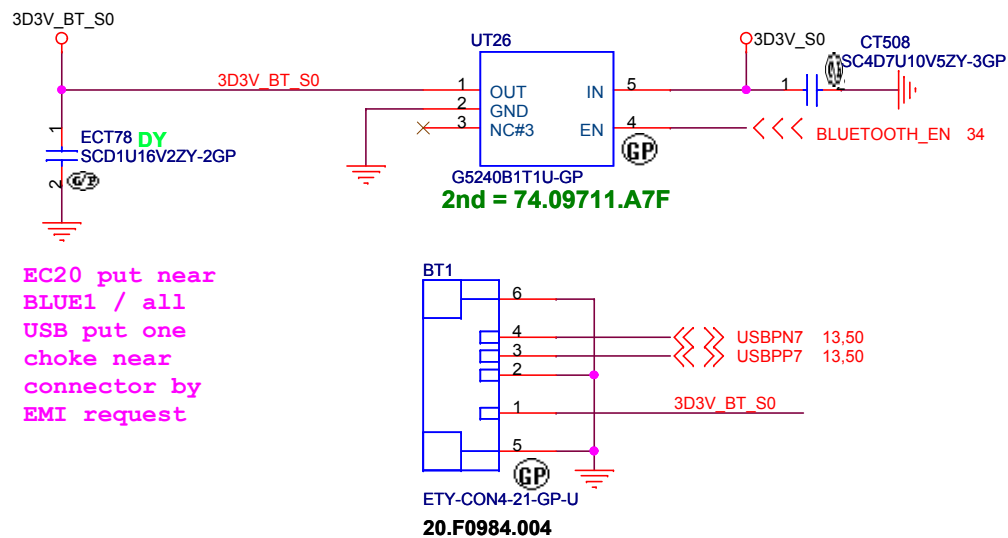


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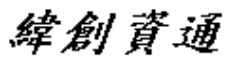
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<b>ODD</b>	
Size	Document Number
<b>SJV50</b>	
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# BLUETOOTH MODULE

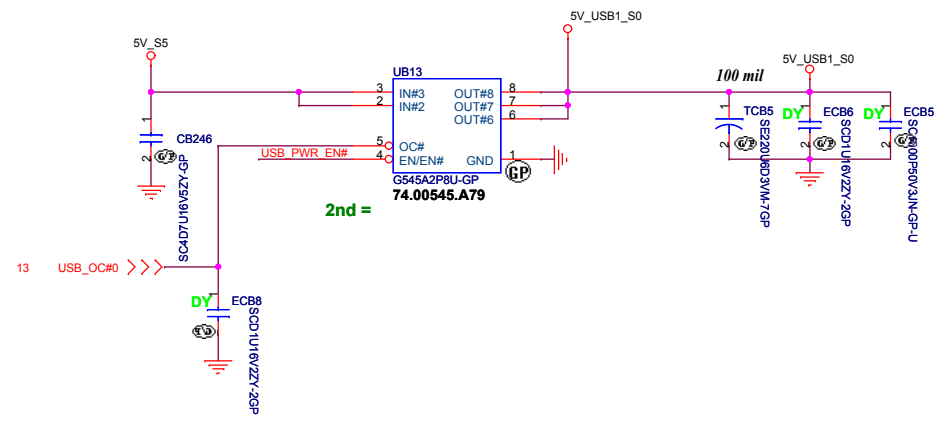
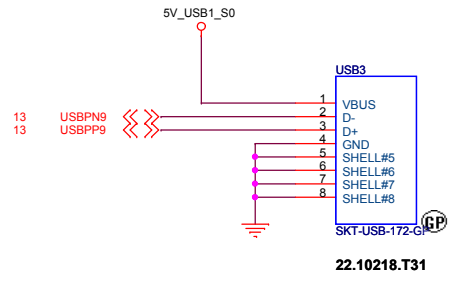
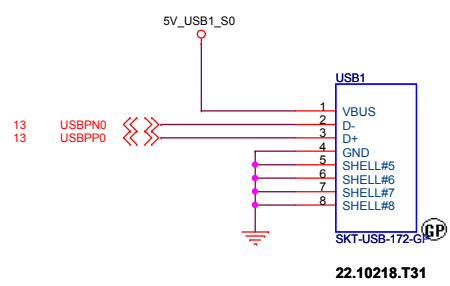


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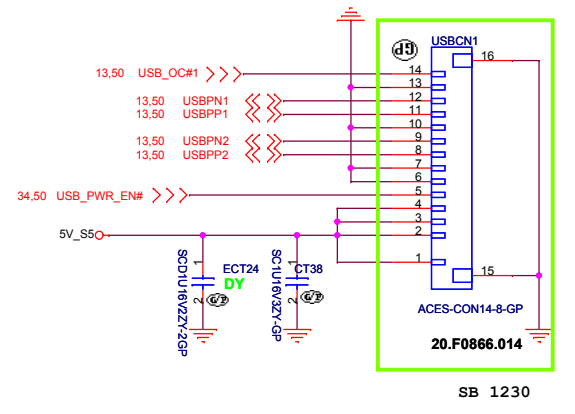
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Size	Document Number
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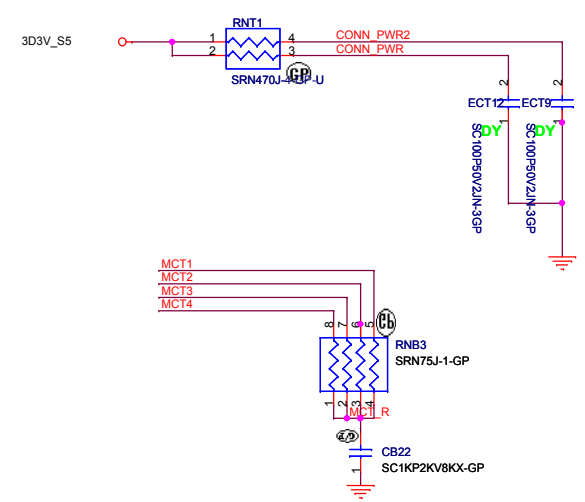
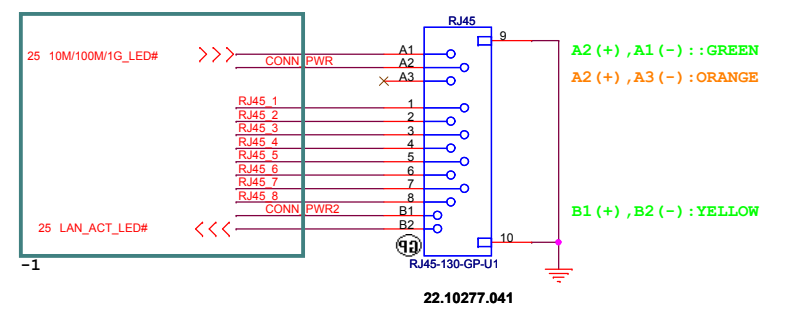
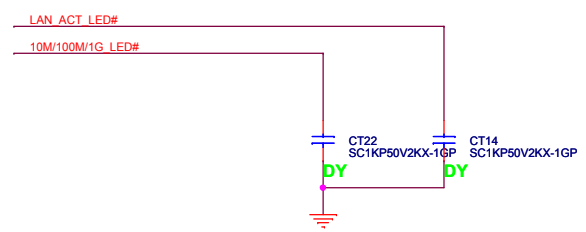
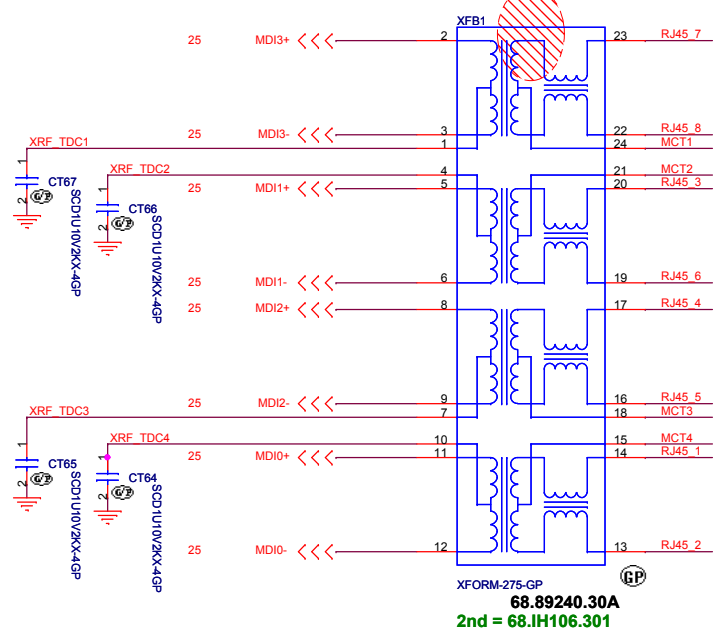


# LAN Connector

# LAN Connector

- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

## GIGA Lan Transformer



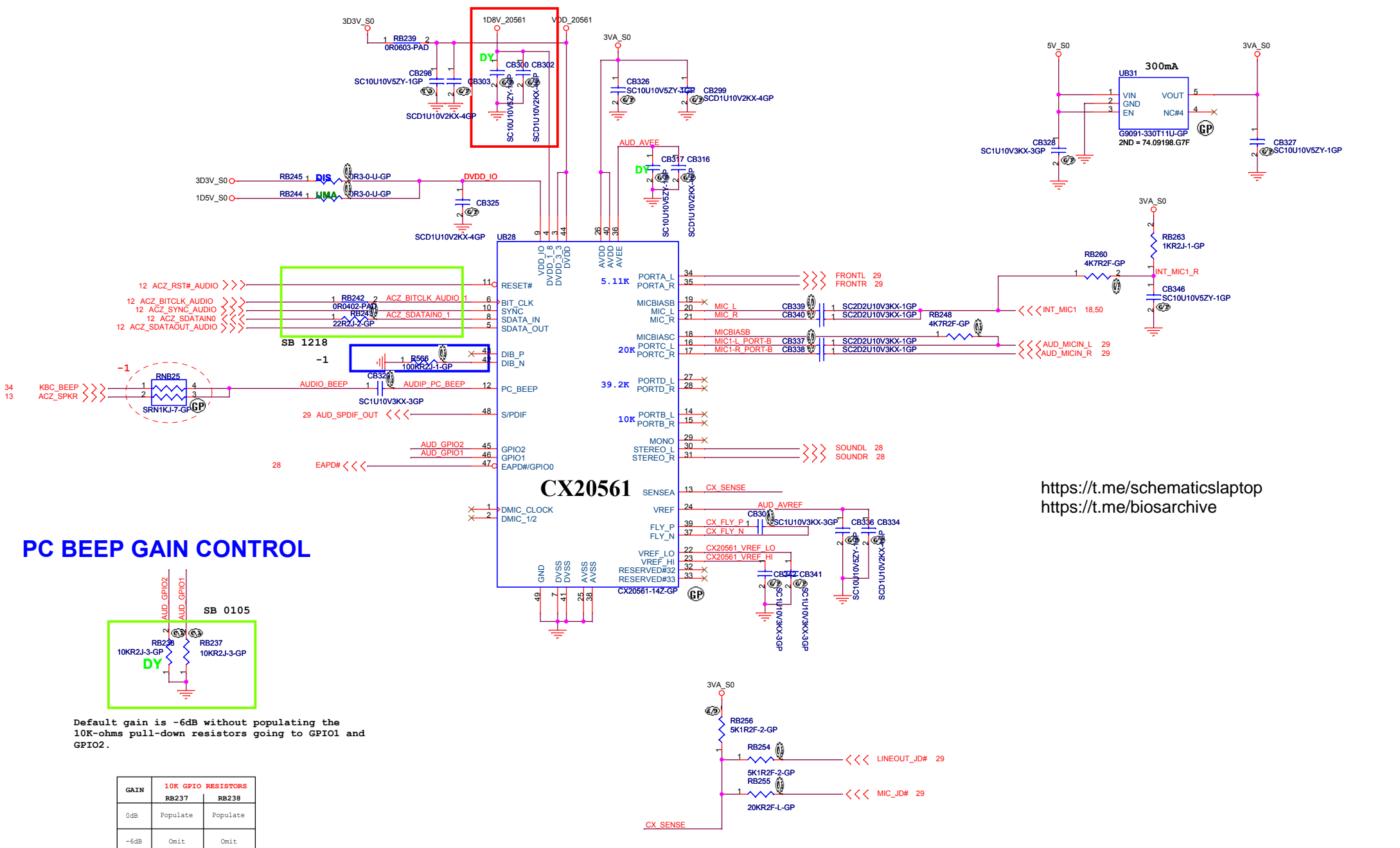
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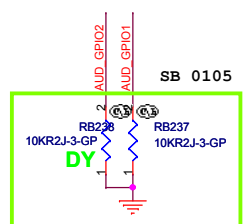
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 Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN CONN**

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Date: Monday, February 23, 2009	Sheet 26 of 59	



## PC BEEP GAIN CONTROL



Default gain is -6dB without populating the 10K-ohms pull-down resistors going to GPIO1 and GPIO2.

GAIN	10K GPIO RESISTORS	
	RB237	RB238
0dB	Populate	Populate
-6dB	Omit	Omit
-12dB	Populate	Omit
-18dB	Omit	Populate

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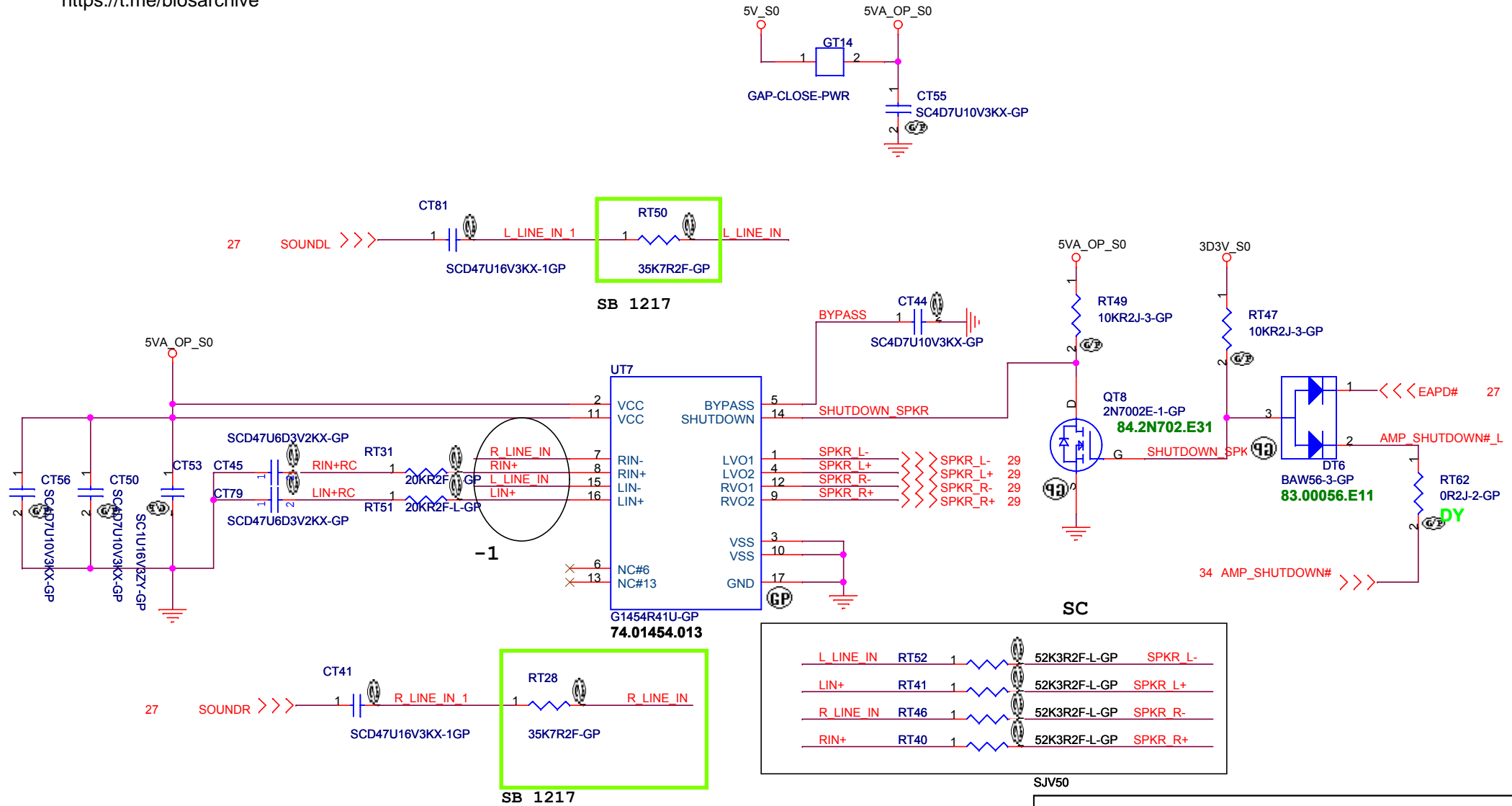
Title **Azalia codec CX20561**


Size A3	Document Number <b>SJV50</b>	Rev <b>SA</b>
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Date: Monday, February 23, 2009 Sheet 27 of 59

# AUDIO OP AMPLIFIER

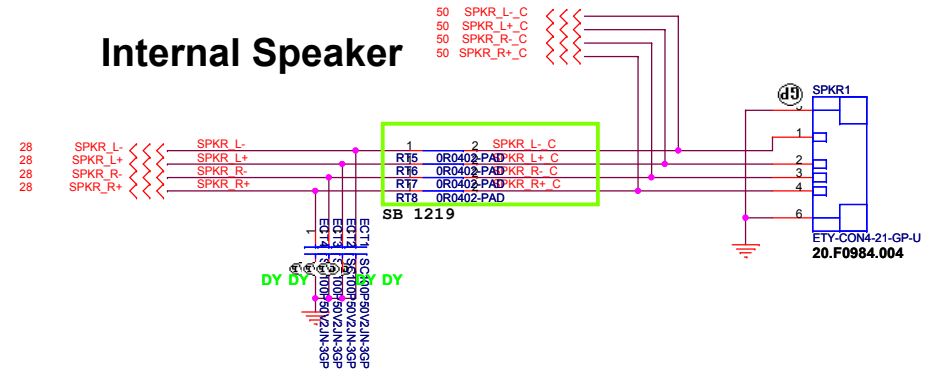
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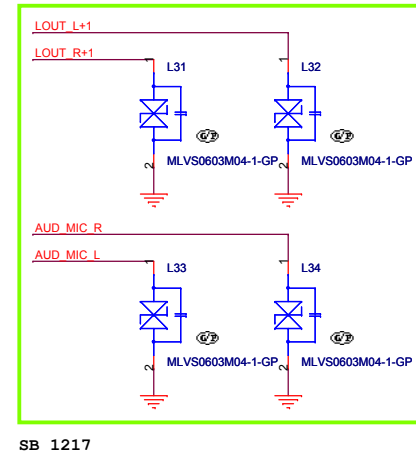
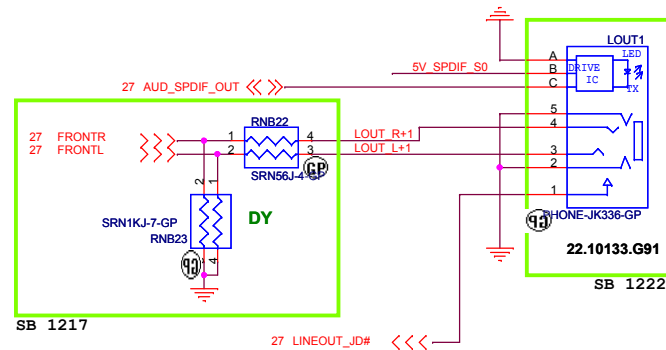
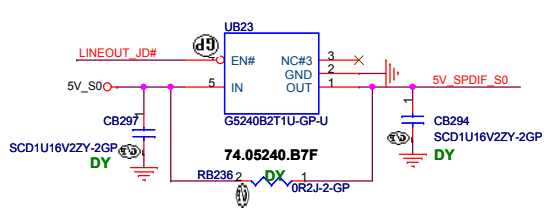
 <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>AUDIO AMP AND JACK</b>	
Size	Document Number
<b>SJV50</b>	
Date: Monday, February 23, 2009	Sheet 28 of 59
Rev	SA

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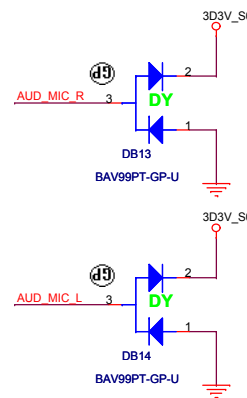
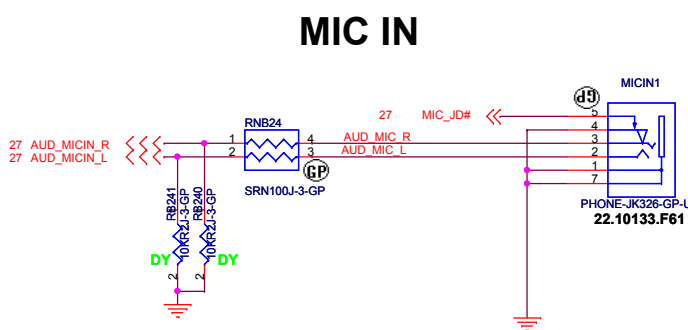
### Internal Speaker



### LINE OUT



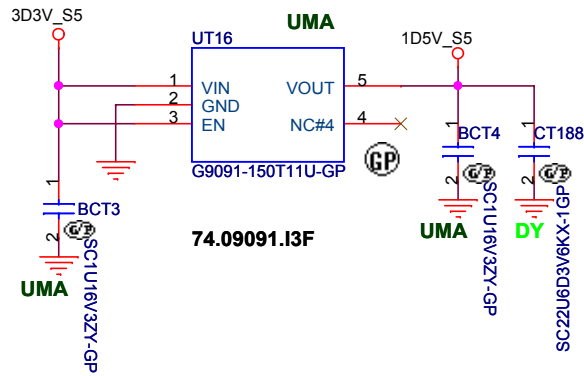
### MIC IN



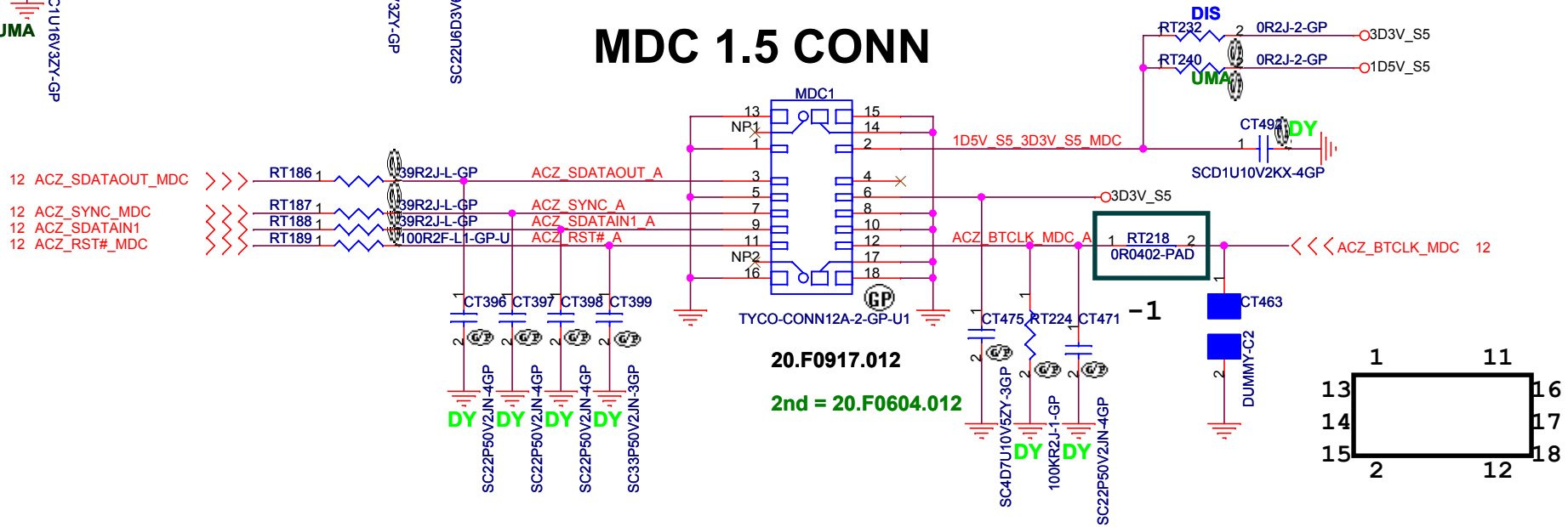
SJV50

<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>title</b> AUDIO jack	
<b>Size</b> Document Number	<b>Rev</b> SA
<b>SJV50</b>	
<b>Date:</b> Monday, February 23, 2009	<b>Sheet</b> 29 of 59



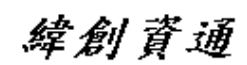


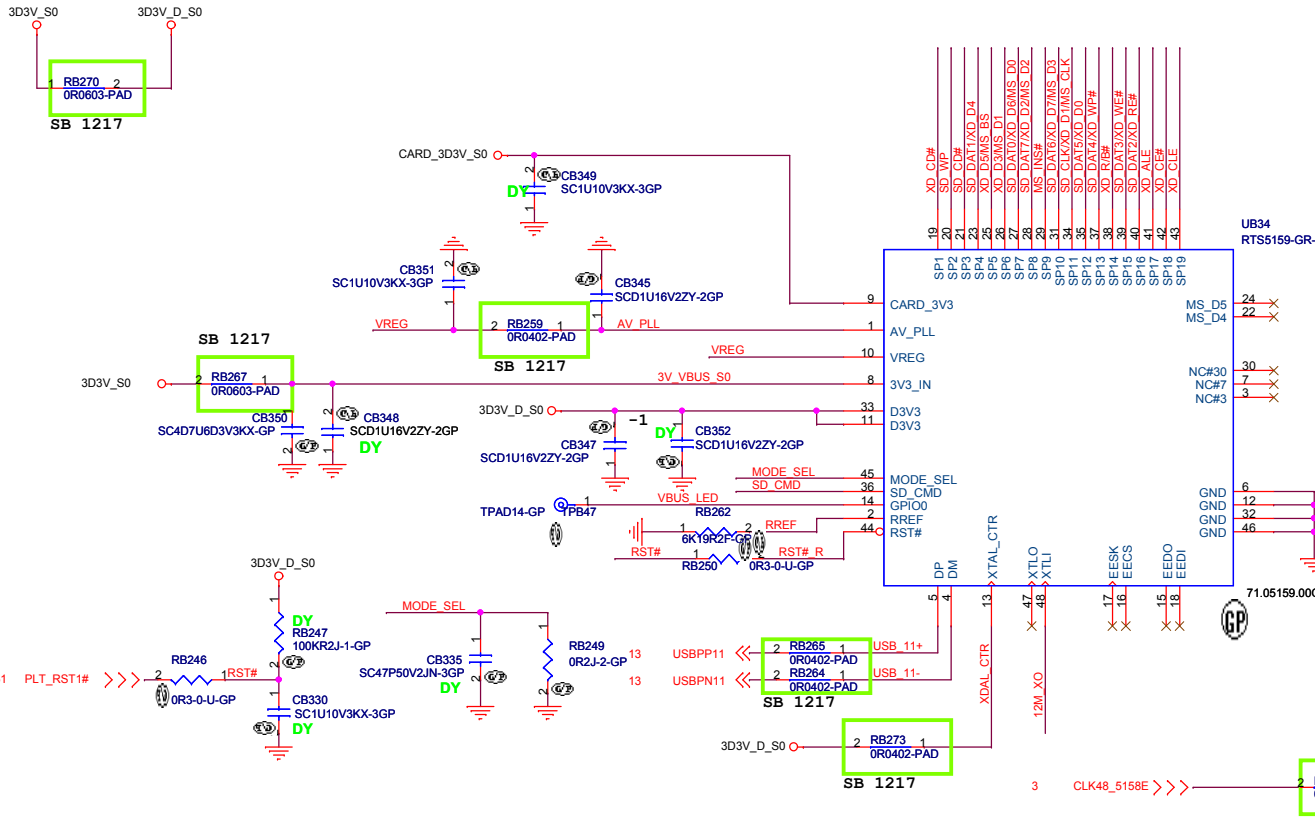
# MDC 1.5 CONN



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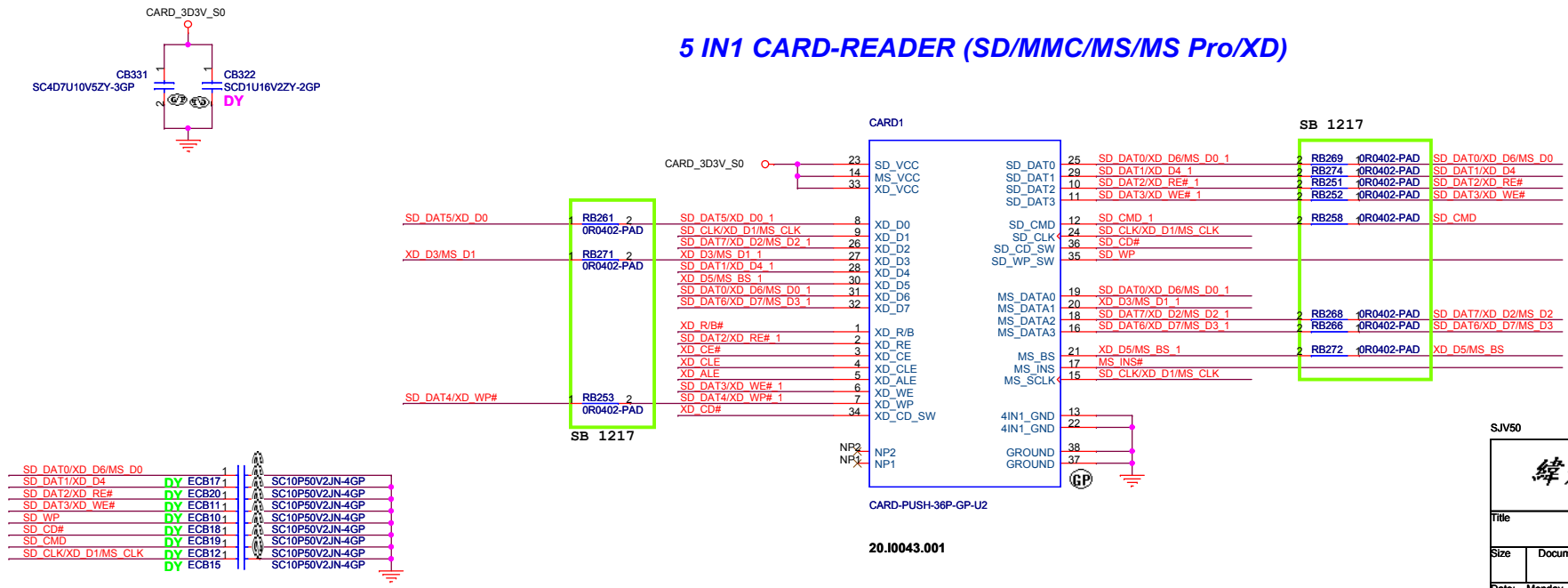
SJV50

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<b>Title</b> <b>MDC</b>			
Size	Document Number		Rev
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### 5 IN 1 CARD-READER (SD/MMC/MS/MS Pro/XD)



SJV50

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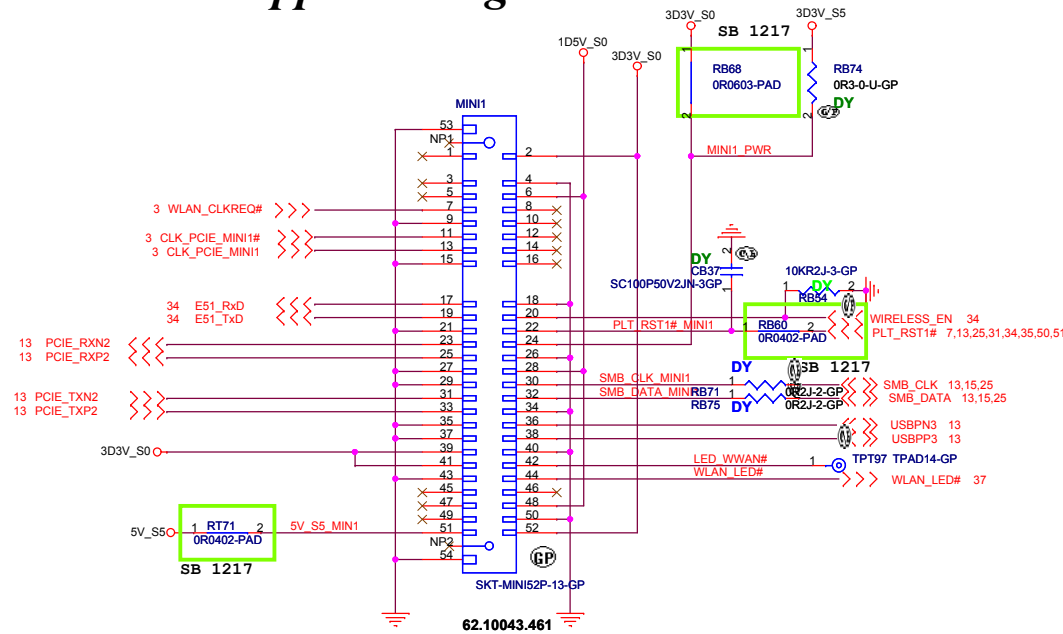
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Size: Document Number: **SJV50** Rev: SA

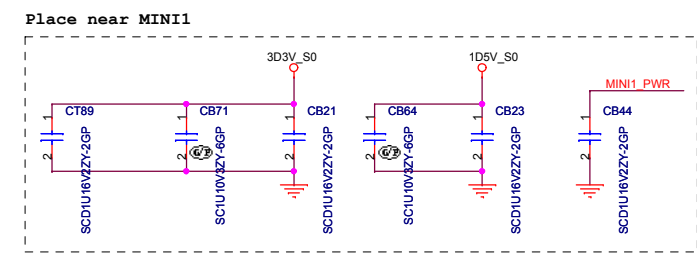
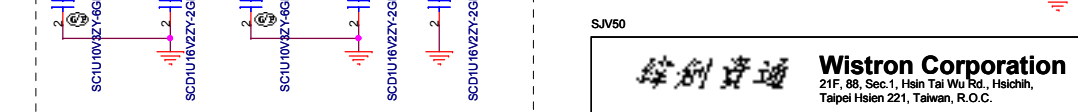
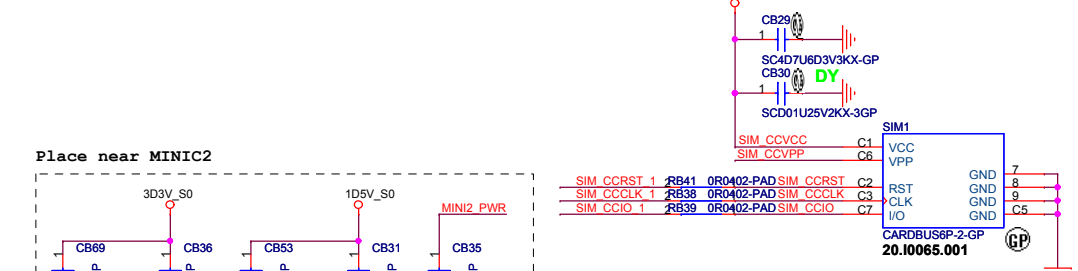
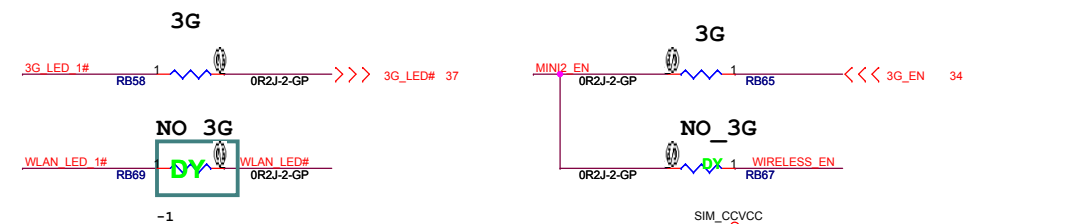
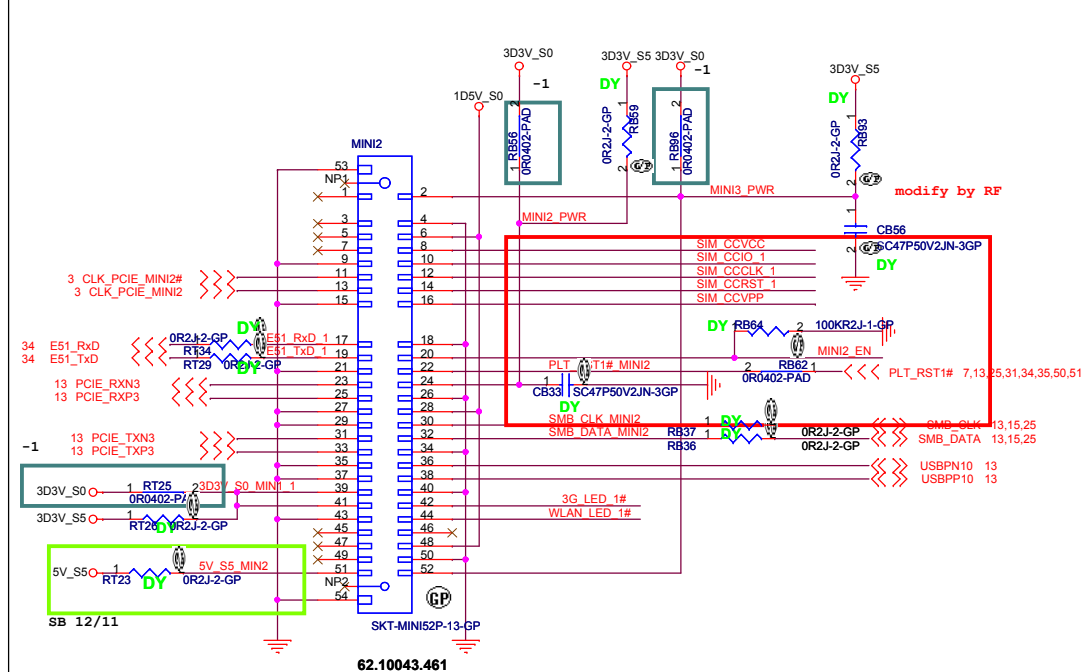
Date: Monday, February 23, 2009 Sheet: 31 of 59

20.10043.001

# Mini Card Connector(WLAN) Half Card Support debug-card



# Mini Card Connector(Robson2 and 3G)



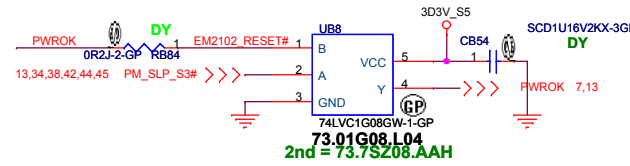
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Title: **MINI CARD**

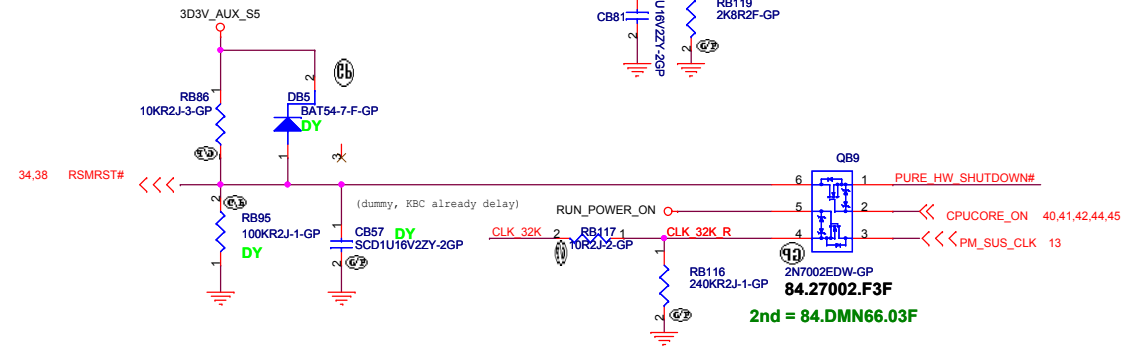
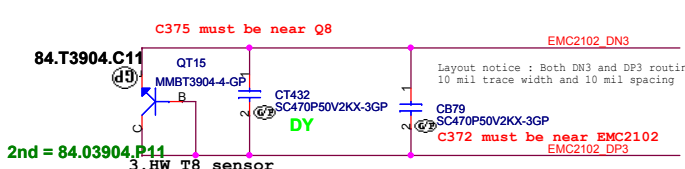
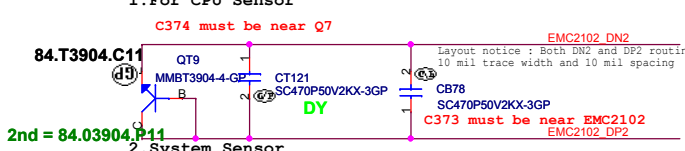
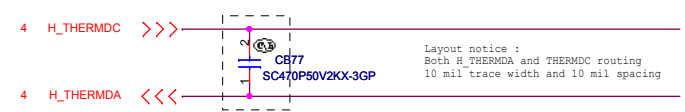
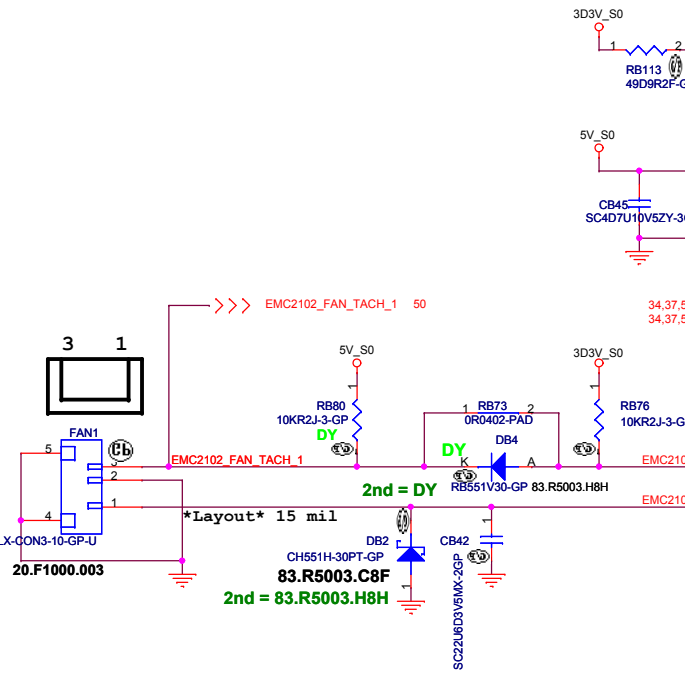
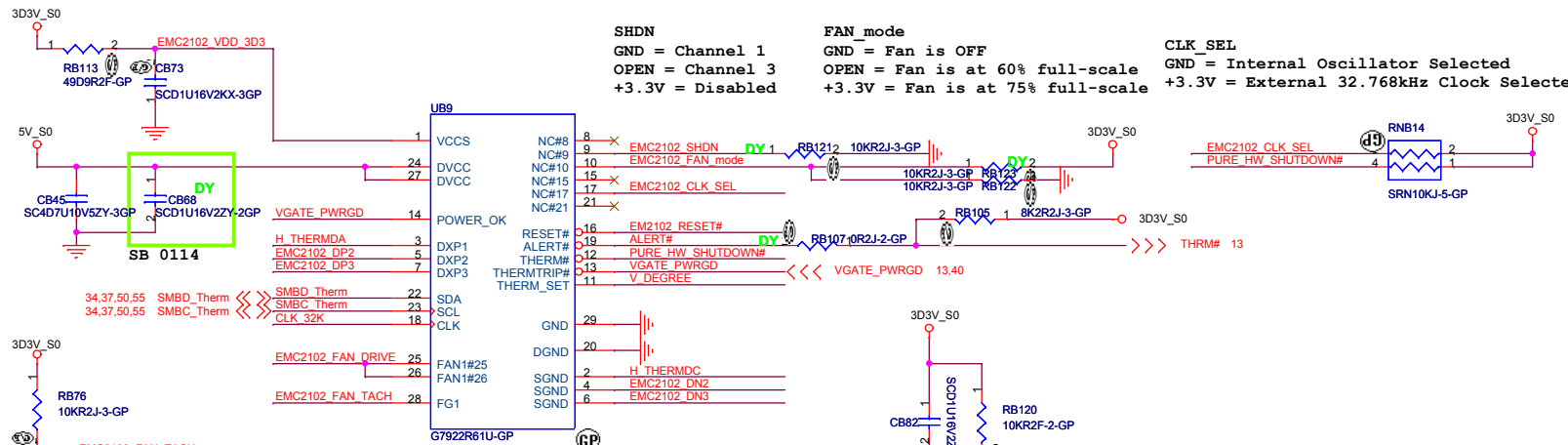
Size A3	Document Number	Rev SA
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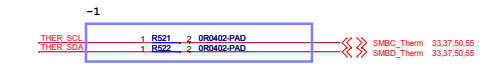
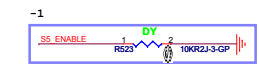
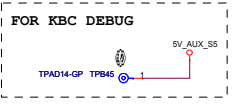
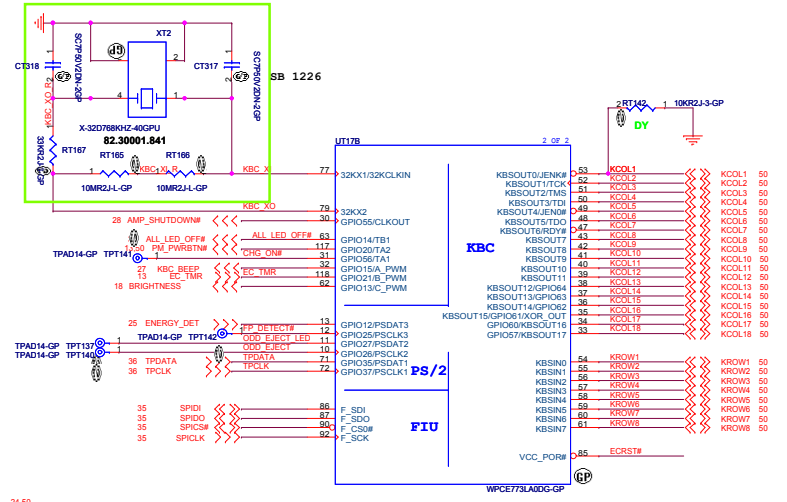
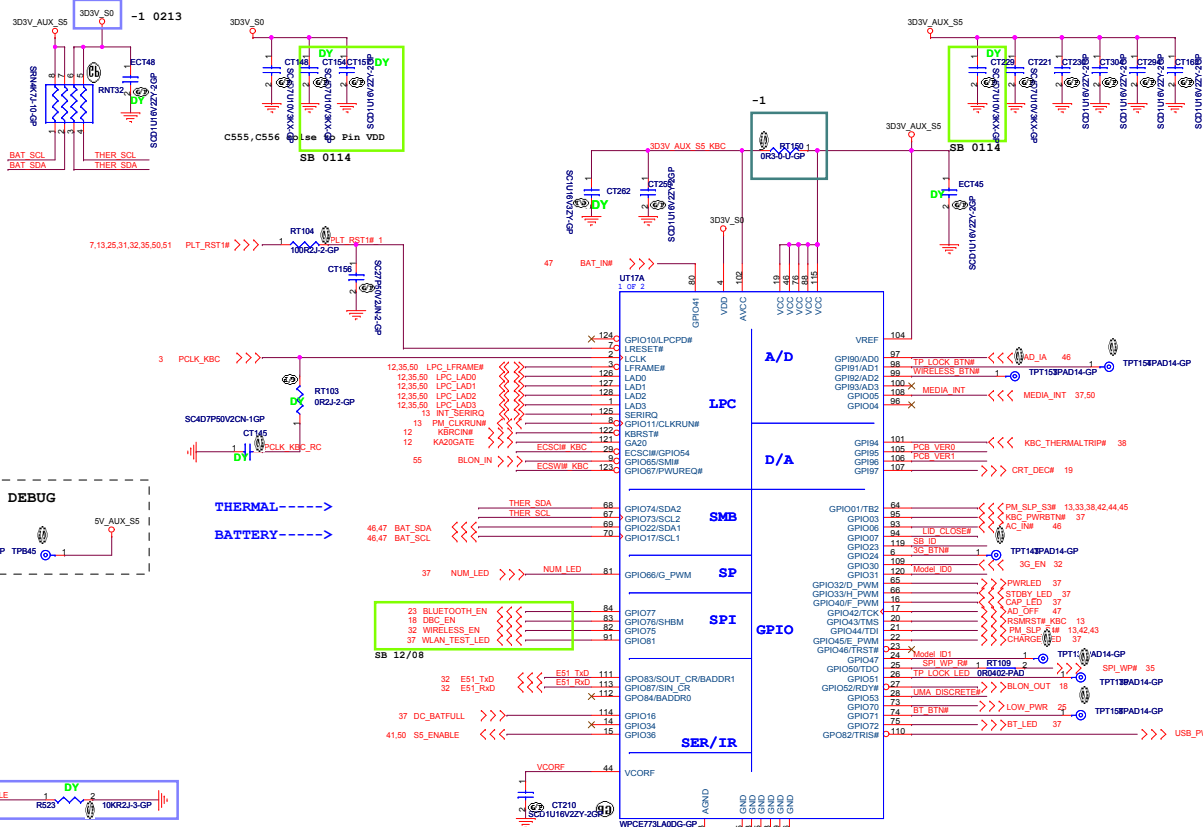


SHDN  
 GND = Channel 1  
 OPEN = Channel 3  
 +3.3V = Disabled

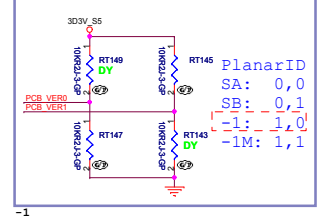
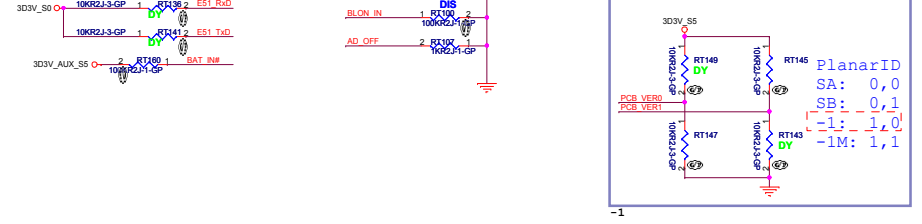
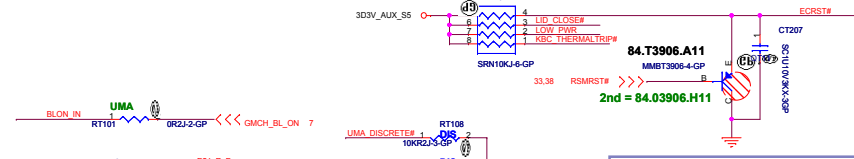
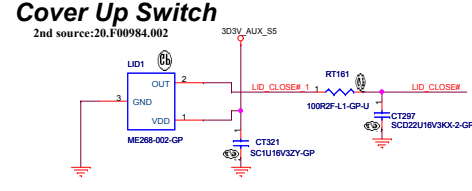
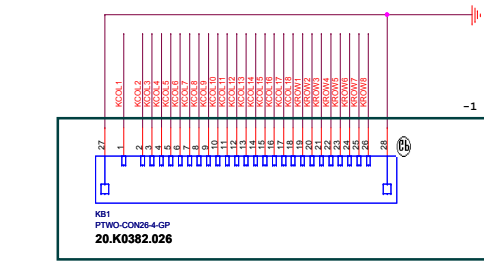
FAN\_mode  
 GND = Fan is OFF  
 OPEN = Fan is at 60% full-scale  
 +3.3V = Fan is at 75% full-scale

CLK\_SEL  
 GND = Internal Oscillator Selected  
 +3.3V = External 32.768kHz Clock Selected



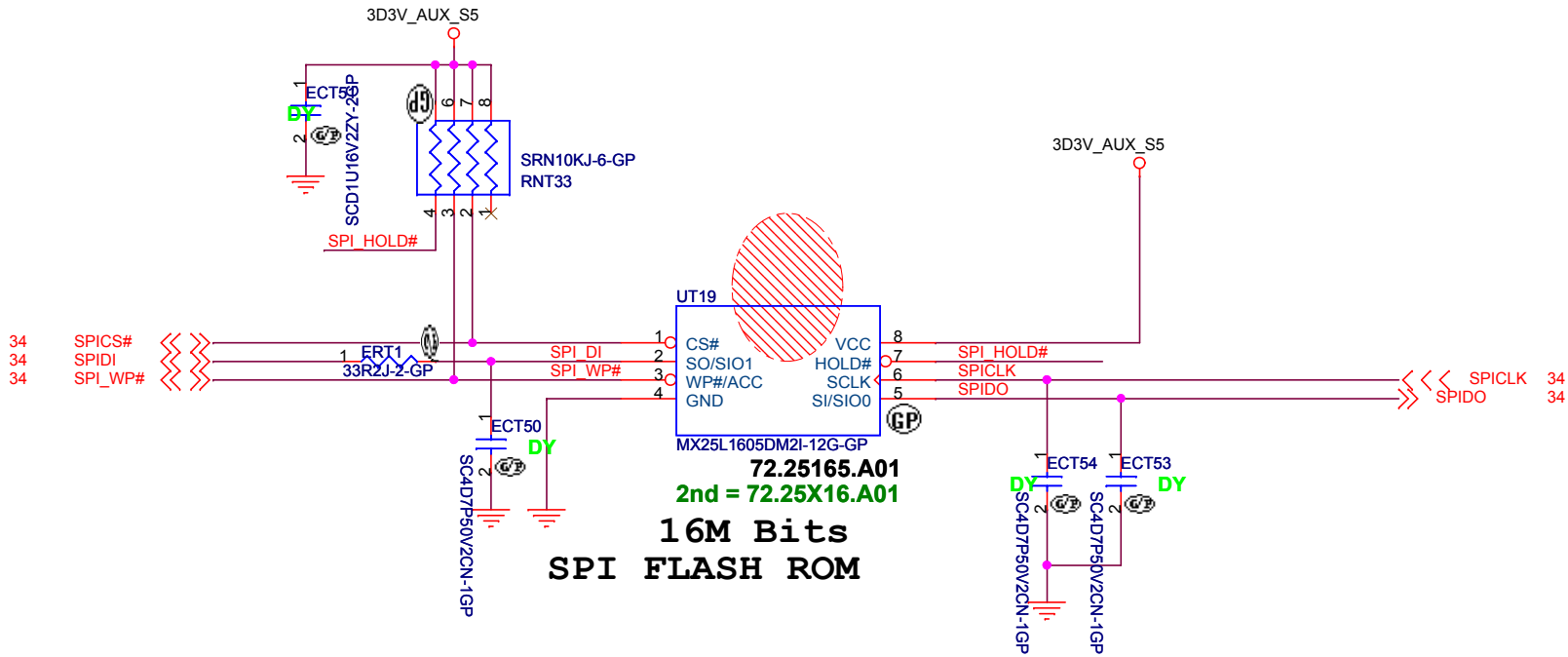


### Internal KeyBoard Connector



MB PIN DEFINE: 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1  
 KB PIN DEFINE: 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24

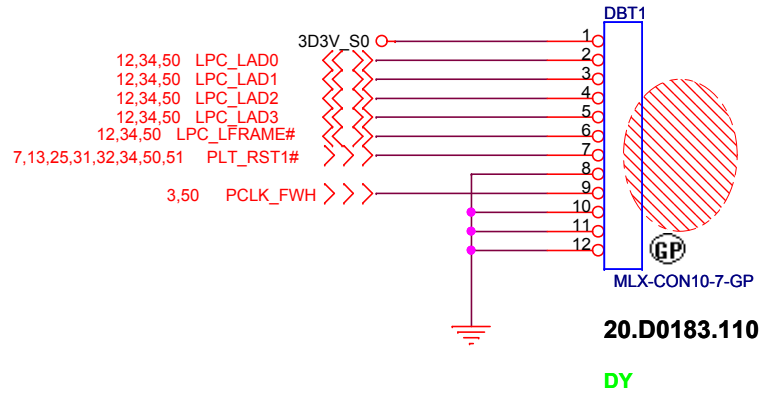
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**GOLDEN FINGER FOR DEBUG BOARD**

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12,34,50 LPC\_LAD[0..3] <<>> LPC\_LAD[0..3]

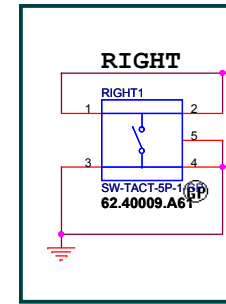
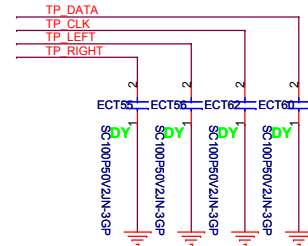
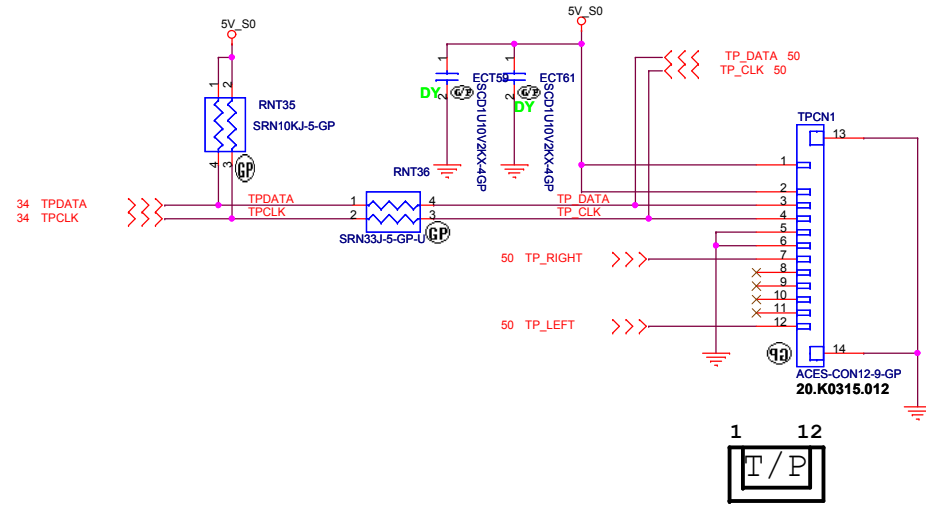


SJV50

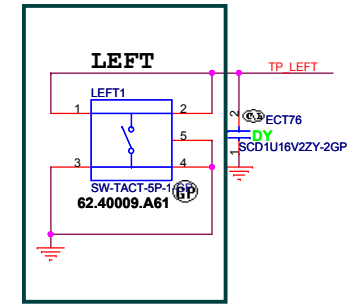
<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>Title</b>			
<b>BIOS</b>			
Size	Document Number	Rev	
	<b>SJV50</b>	<b>SA</b>	
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# TOUCH PAD



-1 ME 0220



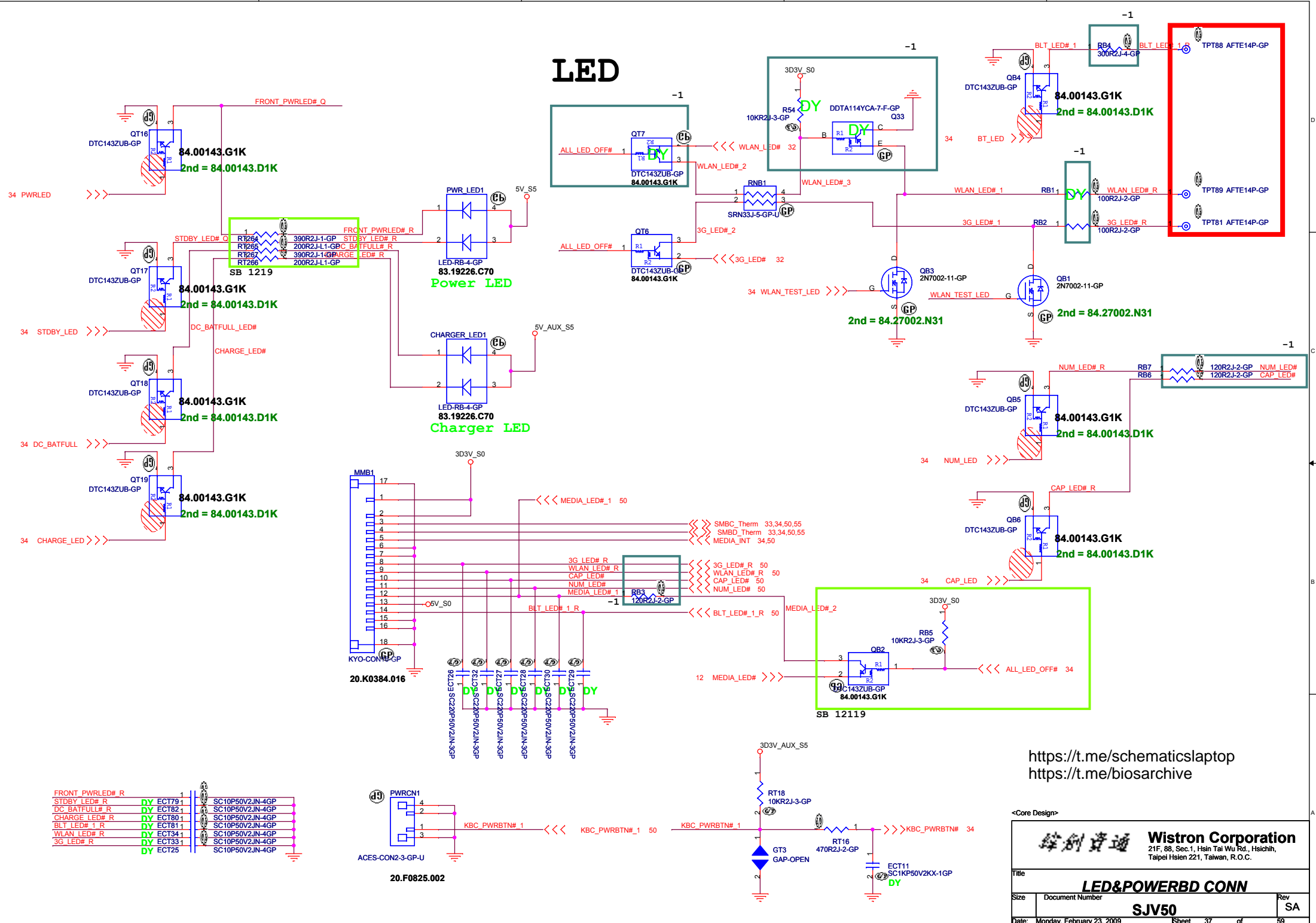
-1 ME 0220

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<https://t.me/biosarchive>

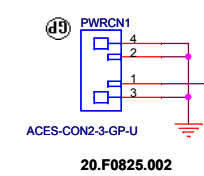
SJV50

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>Title</b> Touch PAD and FP			
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<b>SJV50</b>			
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# LED



FRONT_PWRLED#_R	DY	ECT79	1	SC10P50V2JN-4GP
STDBY_LED#_R	DY	ECT82	1	SC10P50V2JN-4GP
DC_BATFULL#_R	DY	ECT80	1	SC10P50V2JN-4GP
CHARGE_LED#_R	DY	ECT81	1	SC10P50V2JN-4GP
BLT_LED#_1_R	DY	ECT81	1	SC10P50V2JN-4GP
WLAN_LED#_R	DY	ECT34	1	SC10P50V2JN-4GP
3G_LED#_R	DY	ECT33	1	SC10P50V2JN-4GP
	DY	ECT25	1	SC10P50V2JN-4GP



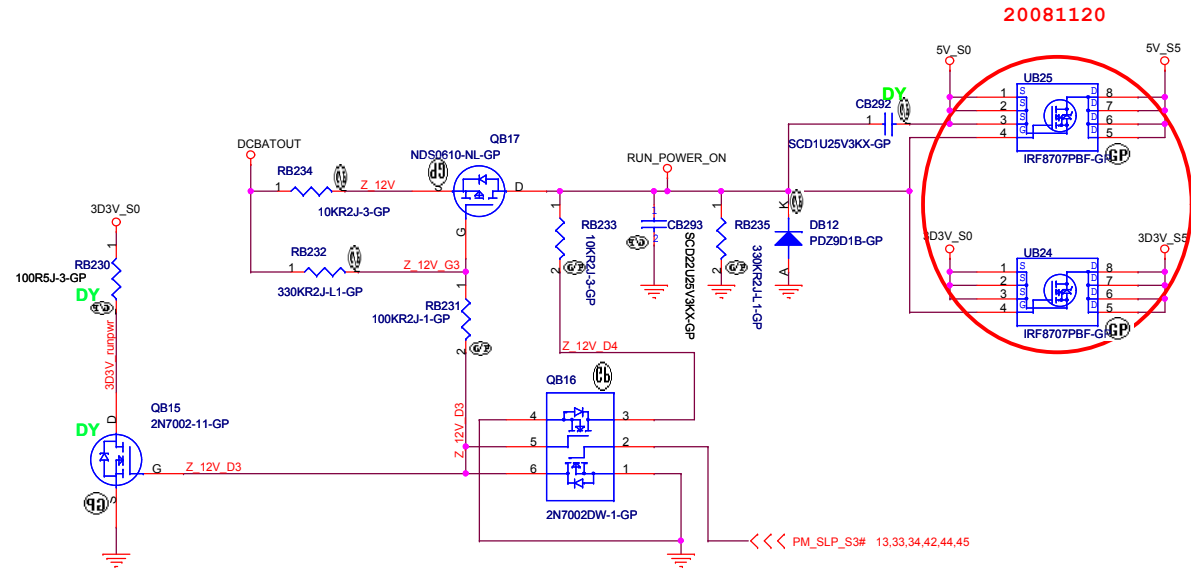
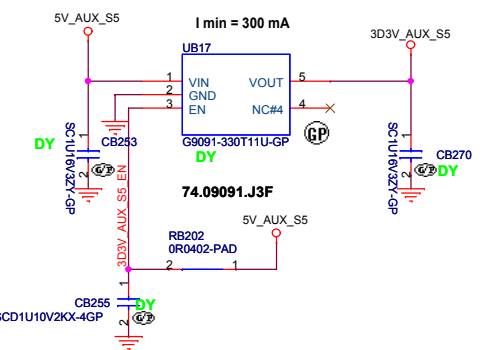
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File: **LED&POWERBD\_CONN**

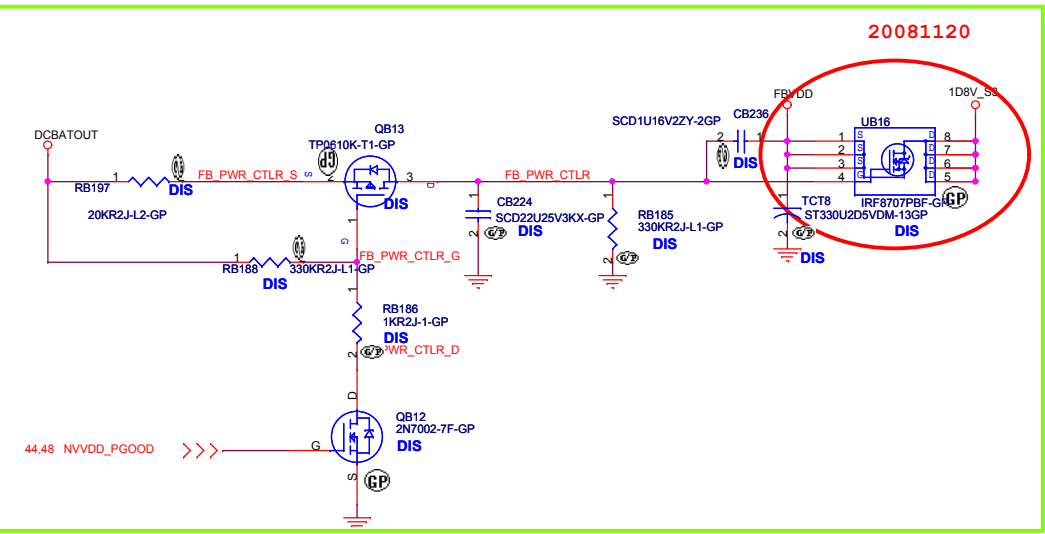
Size	Document Number	Rev
		SA

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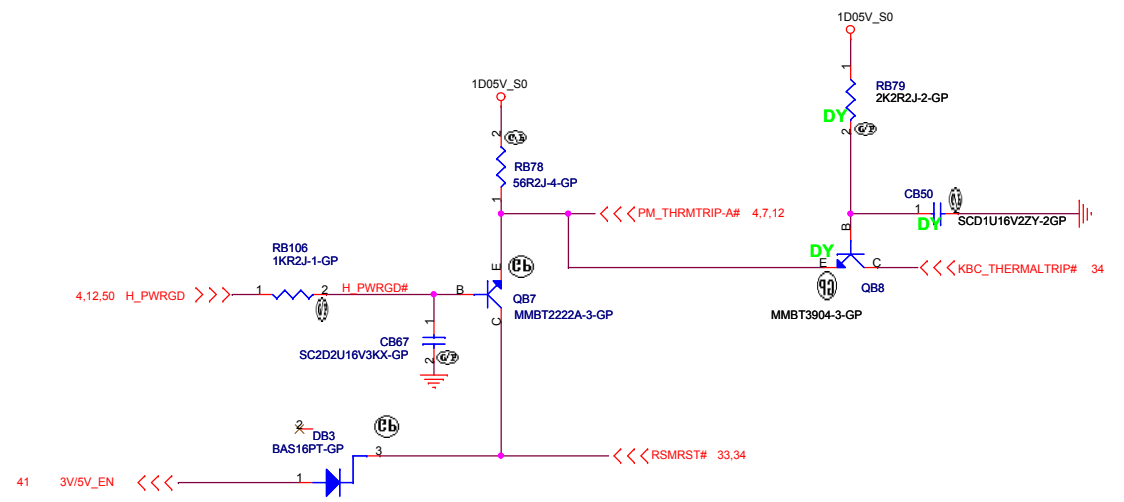


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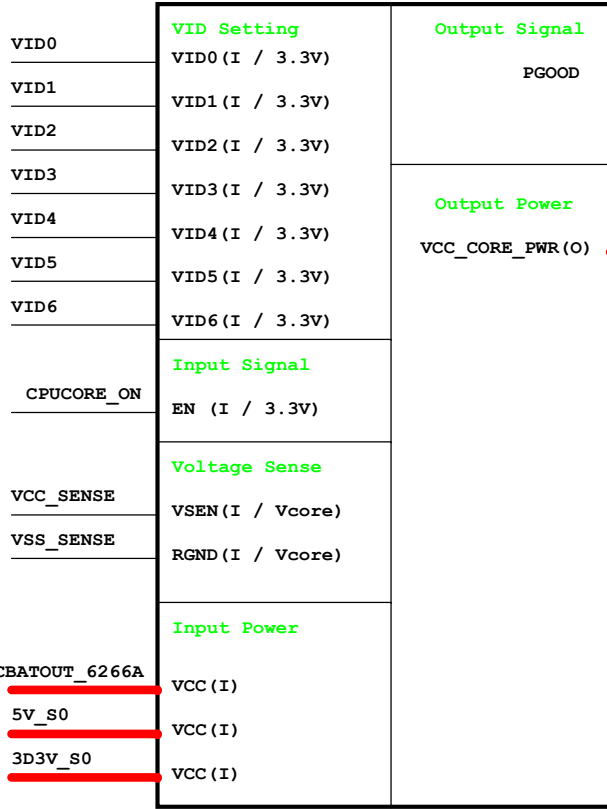
SB 12/11



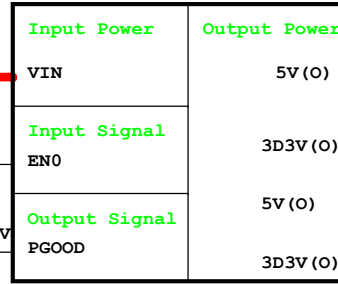
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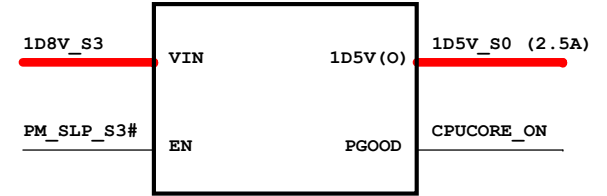
**CPU\_CORE**  
ISL6266A



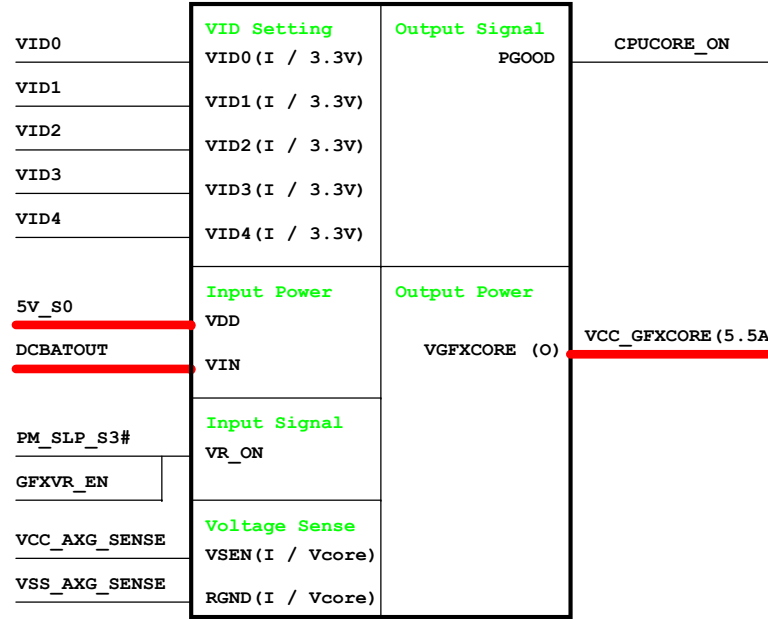
**TPS51125**  
5V/3D3V



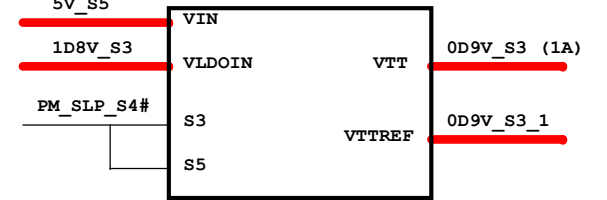
**RT9018A**  
1D5V\_S0



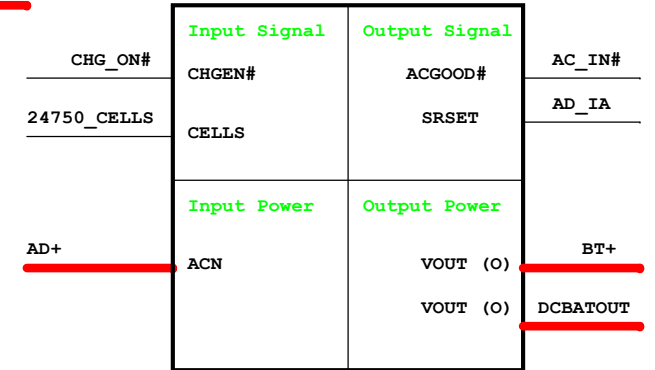
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ISL6263A



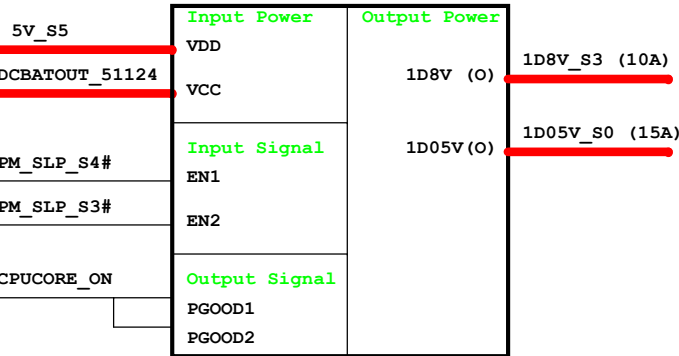
**RT9026** 0D9V\_S0



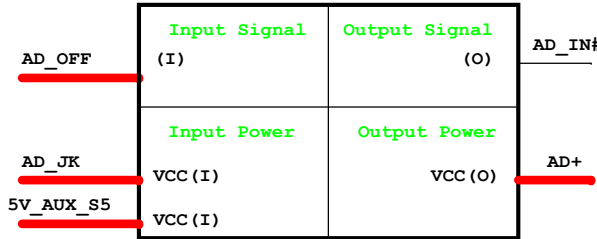
**Charger BQ24745**



**TPS51124**  
1D8V/1D05V

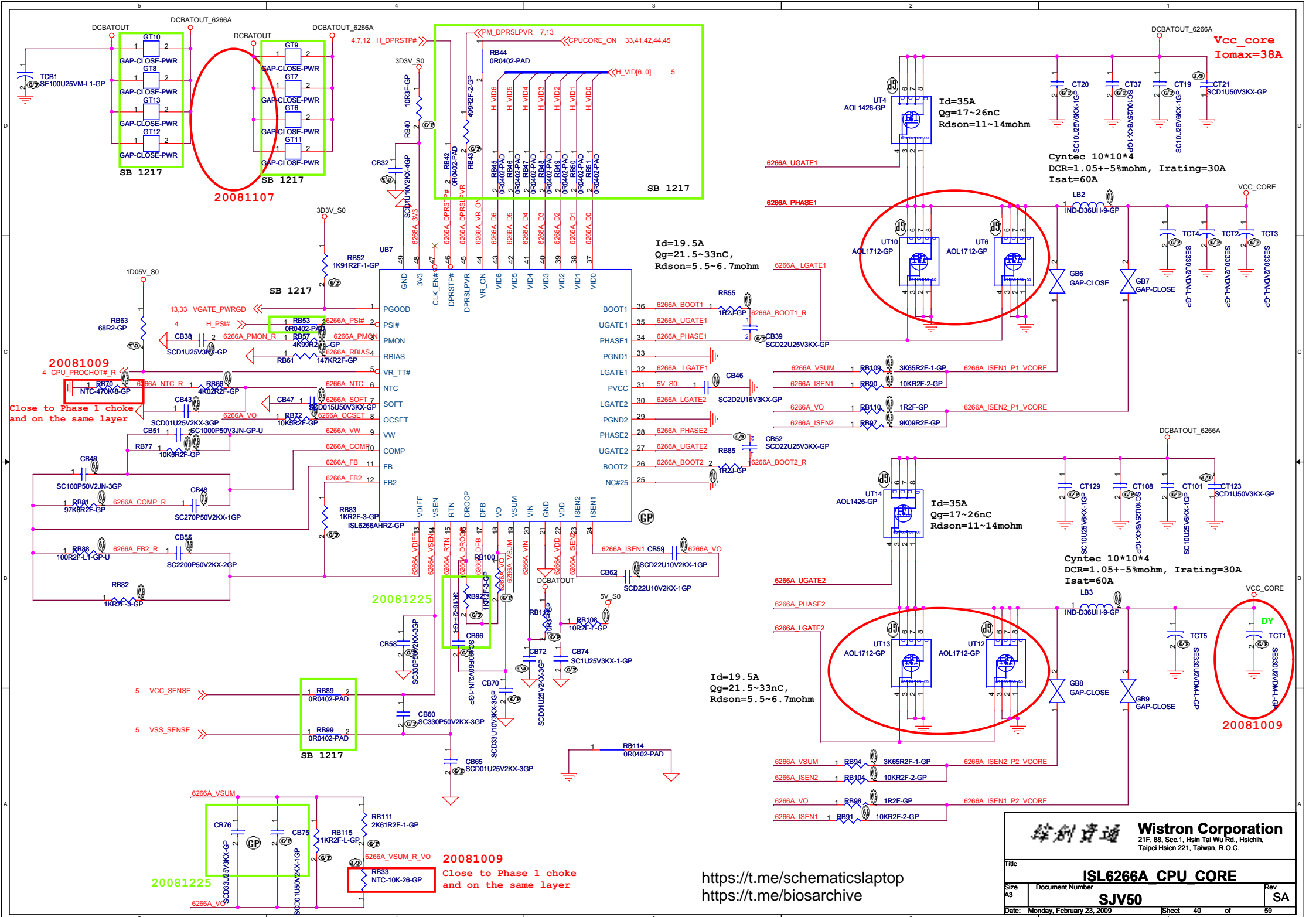


**Adapter**



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Taipei Hsien 221, Taiwan, R.O.C.

Title			<b>Power Sequence Logic</b>		
Size B	Document Number	<b>SJV50</b>		Rev	SA
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20081107

20081009

Close to Phase 1 choke and on the same layer

20081225

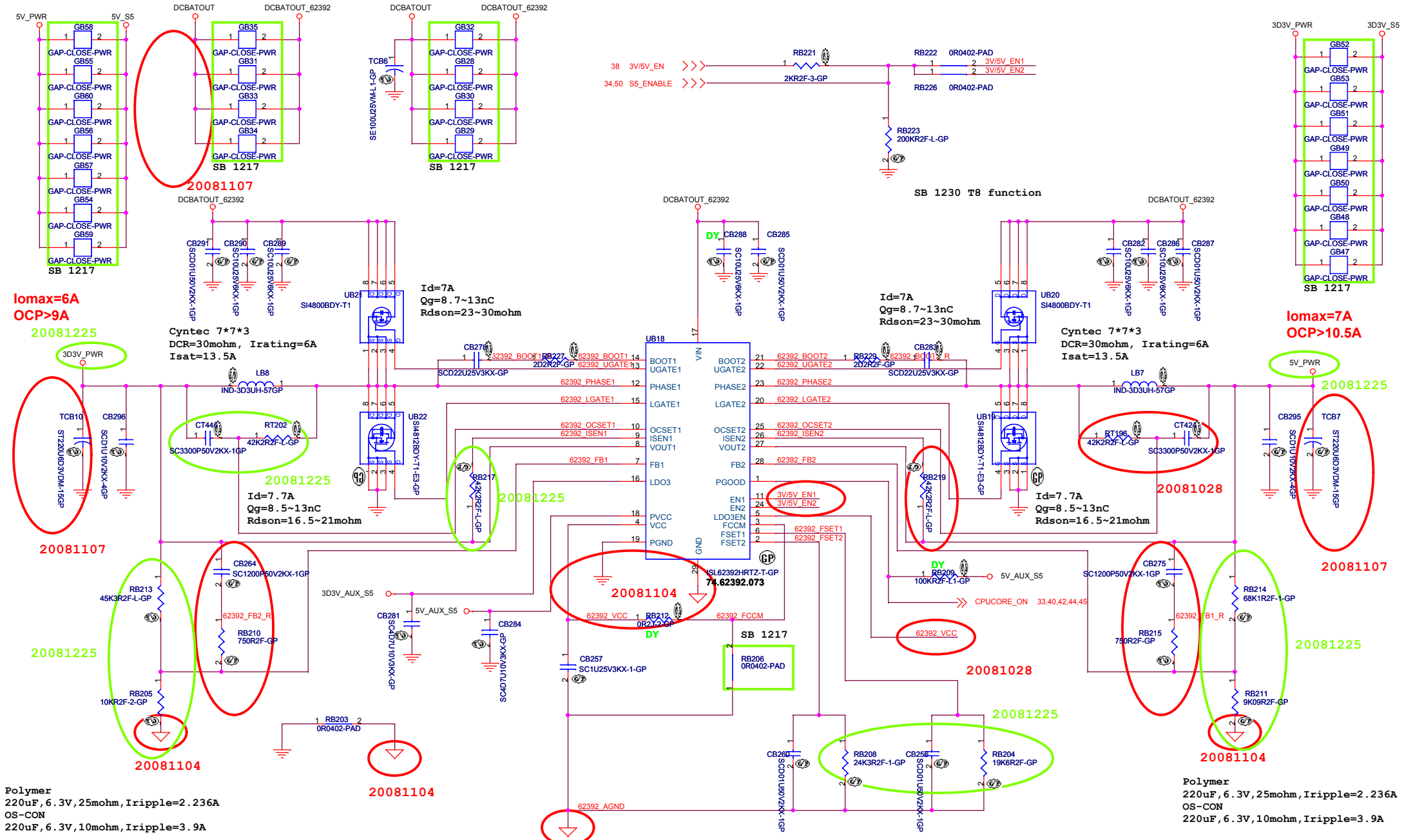
20081225

20081009  
Close to Phase 1 choke and on the same layer

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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title		ISL6266A CPU CORE
Size A3	Document Number	SA
Date: Monday, February 23, 2009		Rev
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Sheet 40	of 59	



Iomax=6A  
OCP>9A  
20081225

20081107

20081225

20081104

Polymer  
220uF, 6.3V, 25mohm, Iripple=2.236A  
OS-CON  
220uF, 6.3V, 10mohm, Iripple=3.9A

Cyntec 7\*7\*3  
DCR=30mohm, Irating=6A  
Isat=13.5A

20081225  
Id=7.7A  
Qg=8.5~13nC  
Rdson=16.5~21mohm

Id=7A  
Qg=8.7~13nC  
Rdson=23~30mohm

20081225

20081104

20081104  
Vout=0.6\*(1+R1/R2)

Id=7A  
Qg=8.7~13nC  
Rdson=23~30mohm

Id=7.7A  
Qg=8.5~13nC  
Rdson=16.5~21mohm

Cyntec 7\*7\*3  
DCR=30mohm, Irating=6A  
Isat=13.5A

Iomax=7A  
OCP>10.5A  
20081225

20081107

20081225

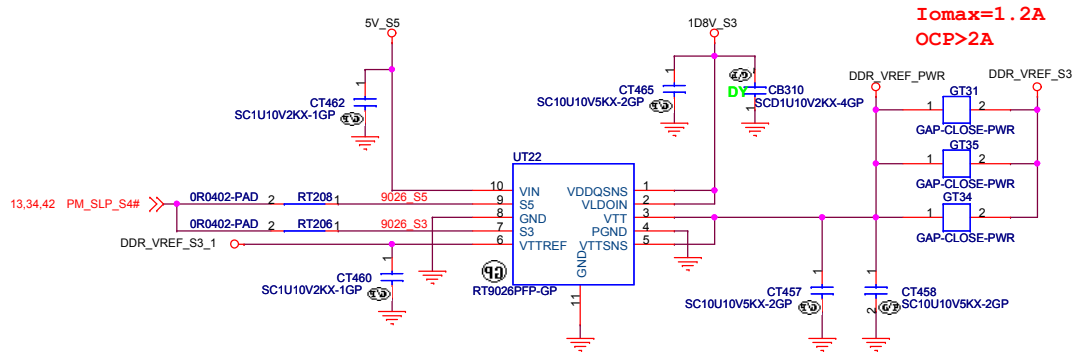
Polymer  
220uF, 6.3V, 25mohm, Iripple=2.236A  
OS-CON  
220uF, 6.3V, 10mohm, Iripple=3.9A

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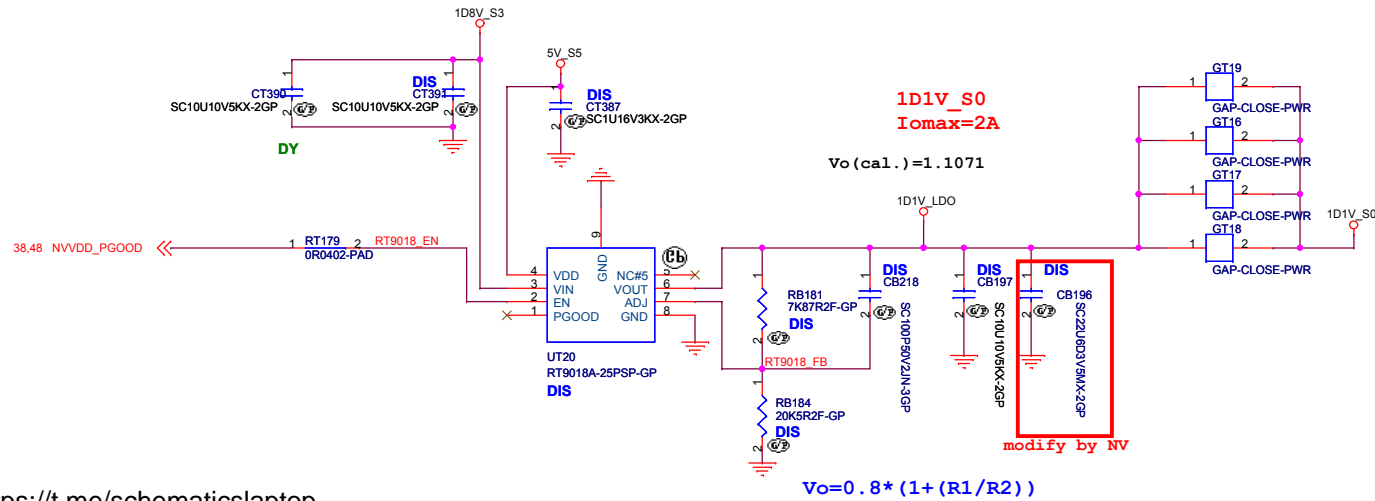
<b>緯創資通 Wistron Corporation</b>	
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<b>ISL62392 5V/3D3V</b>	
Size A3	Document Number
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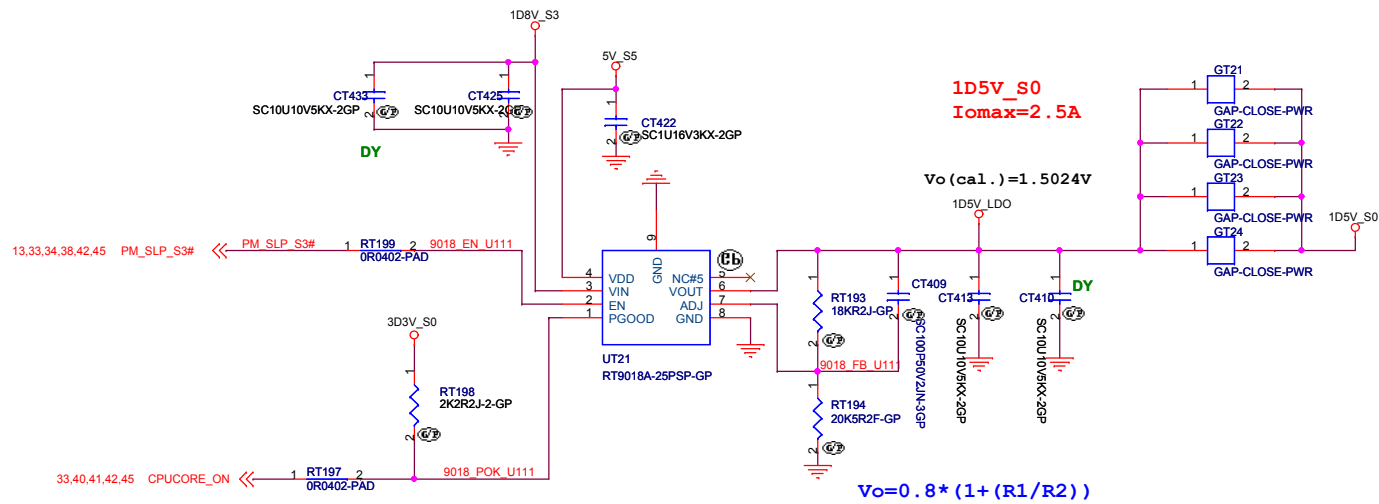




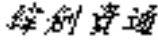
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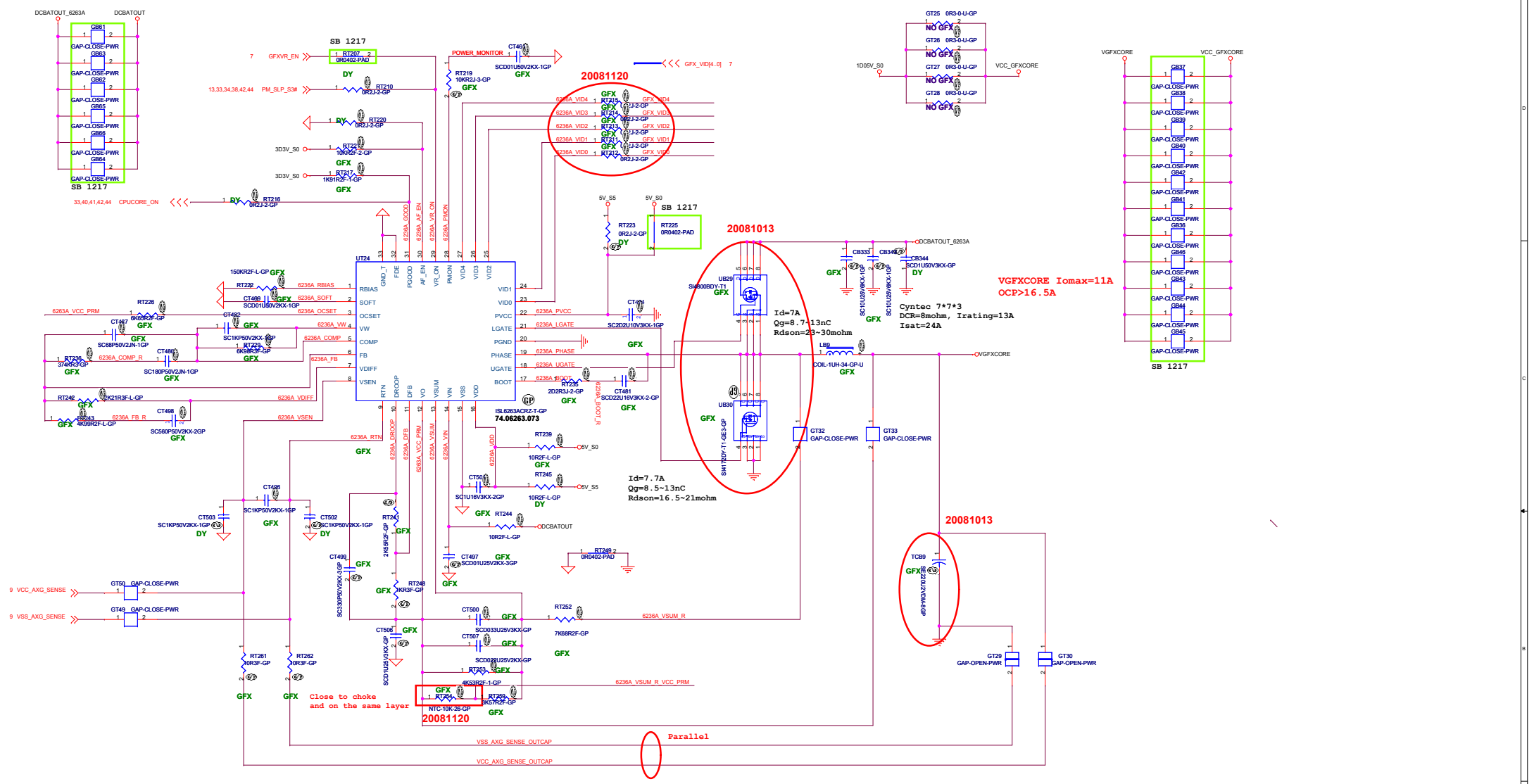


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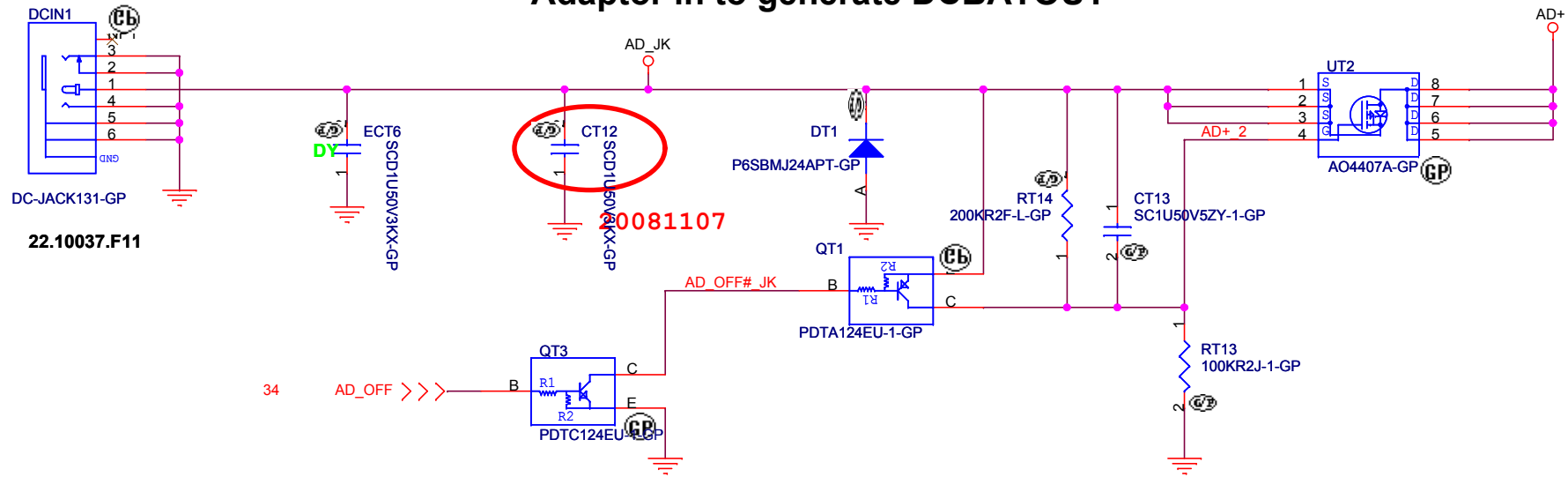
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Title	
<b>1D1V &amp; 1D5V</b>	
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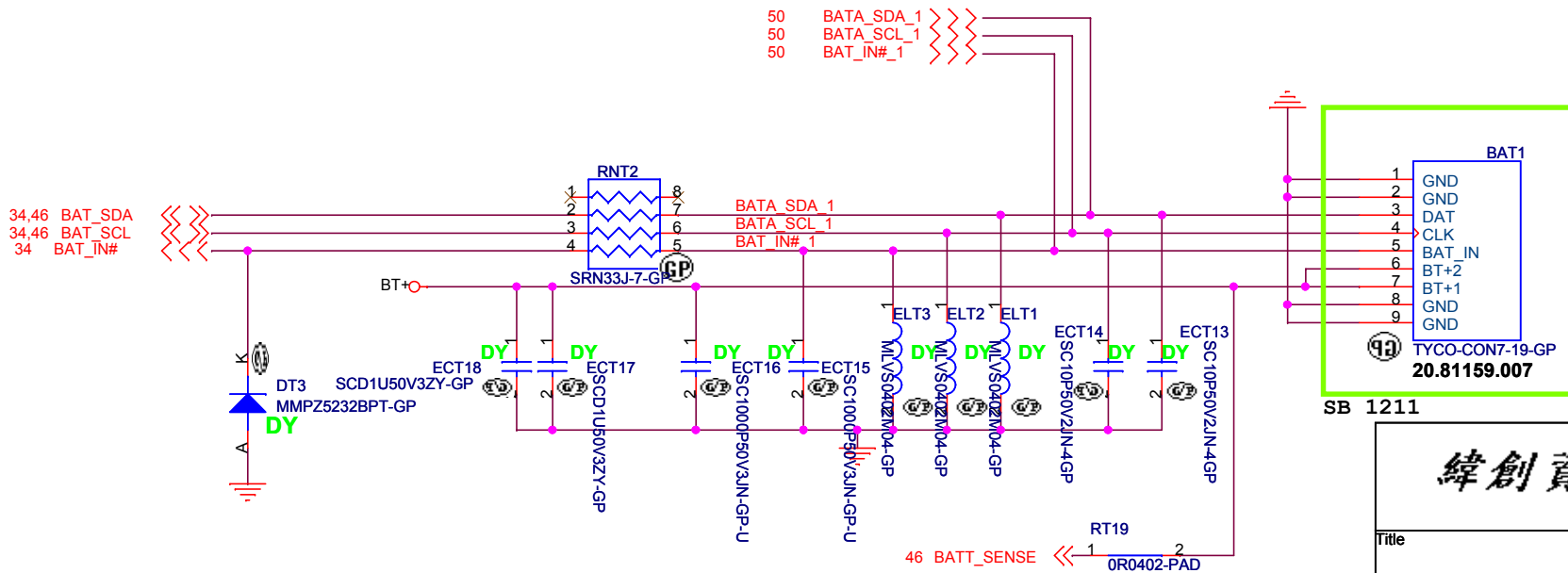


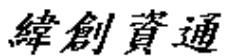
# Adaptor in to generate DCBATOUT



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# BATTERY CONNECTOR



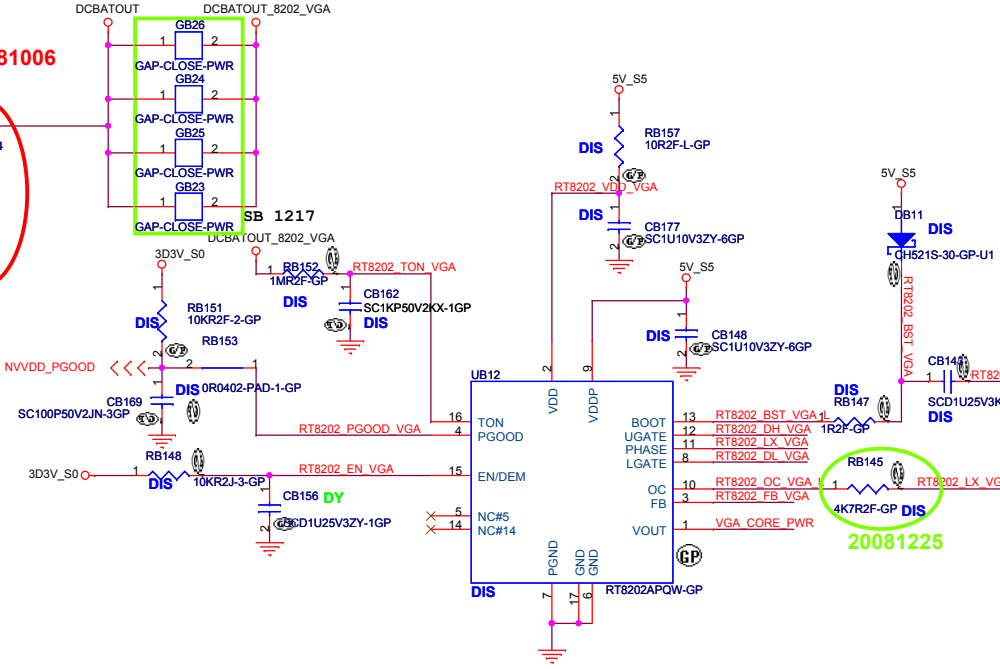
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20081006

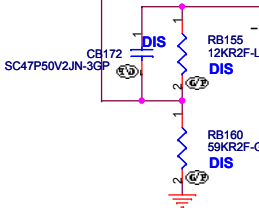


38.44 NVDD\_PGOOD

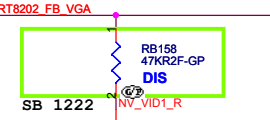


20081225

$$V_{out} = 0.75 * (1 + R_h / R_l)$$

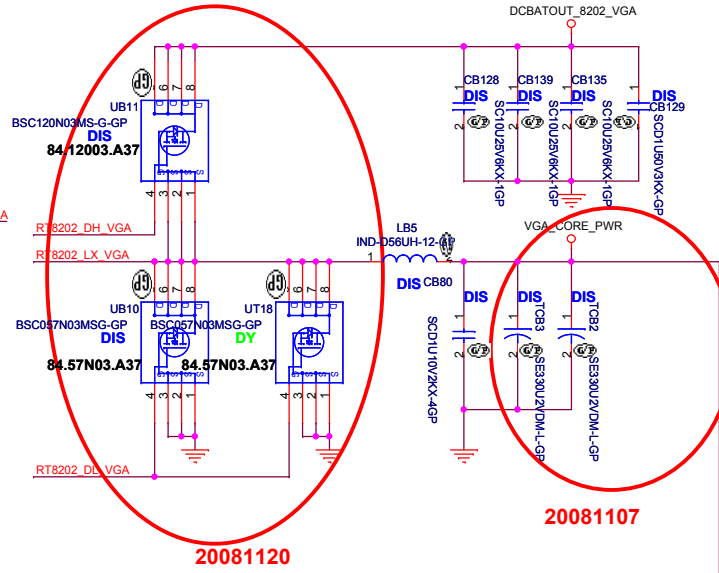


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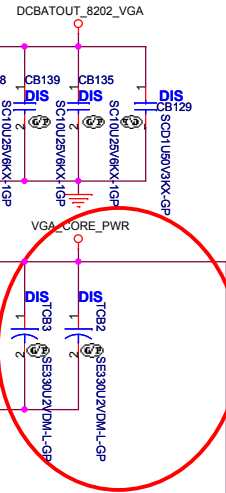


20081222

N10M-GE1		
ALTV1	ALTV0	Vout
0	0	0.90V
1	0	1.00V
0	1	1.20V



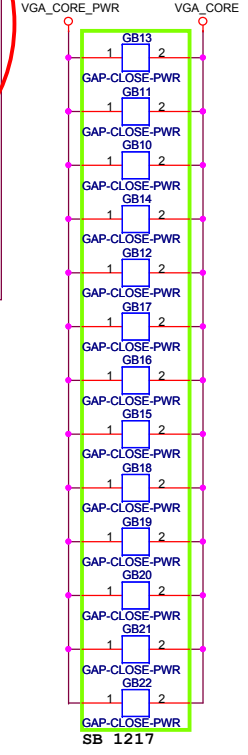
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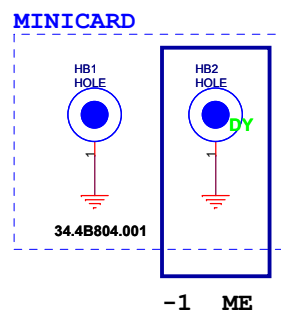
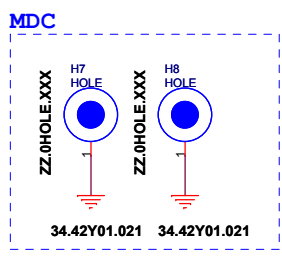
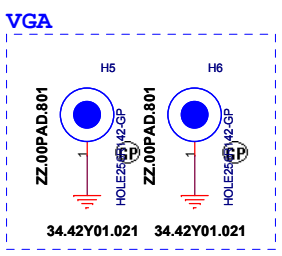
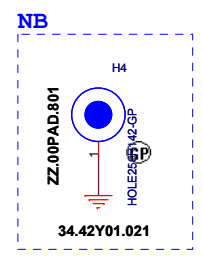
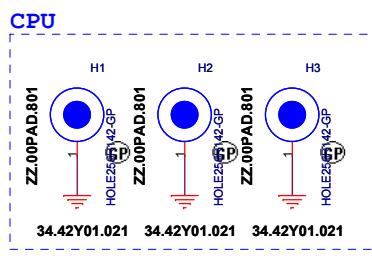
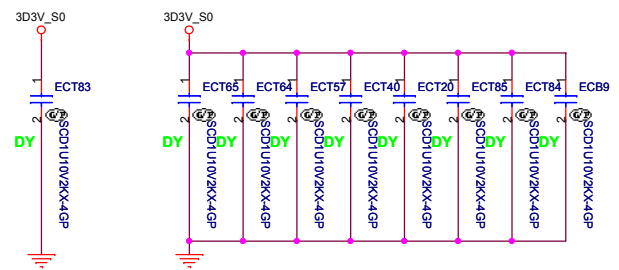
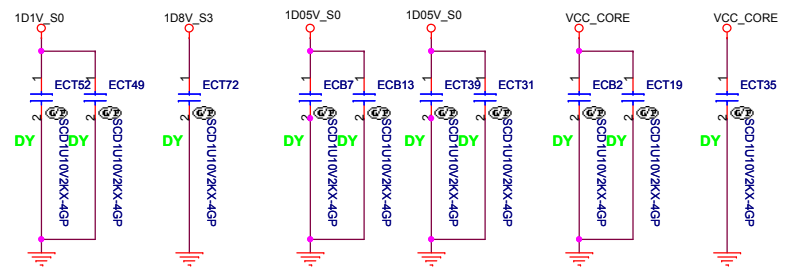
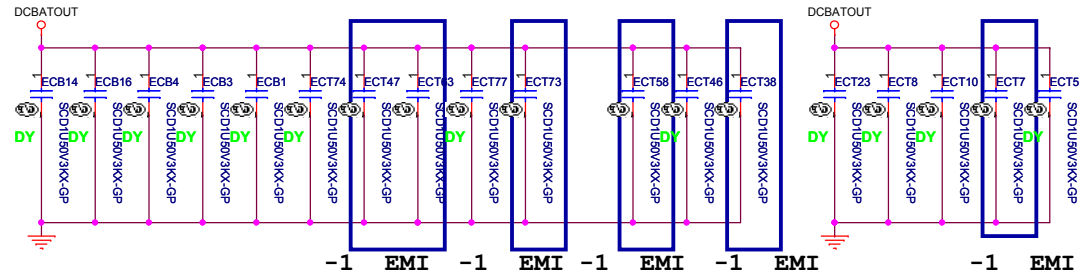
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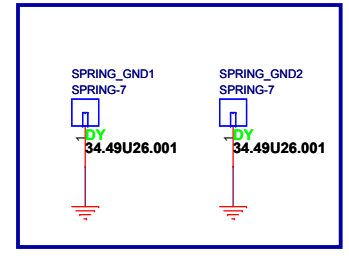
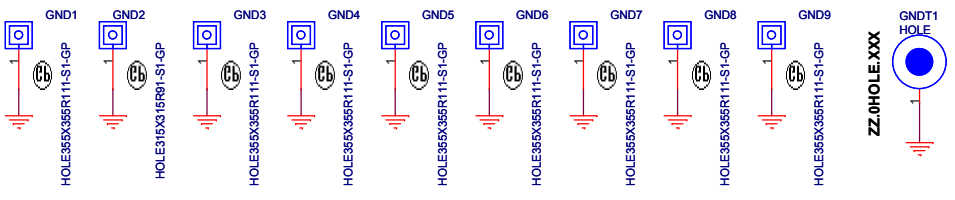


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-1 ME



-1 EMI

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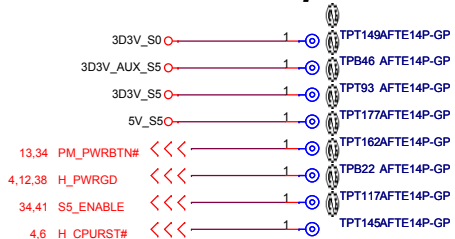
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Title: **EMI/Spring/Boss**

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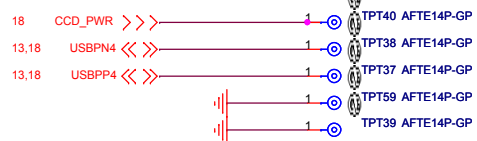
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### Check test point



Test Point放在Dimm Door打開可量測處

### CCD Conn. Test Point keep on connector side



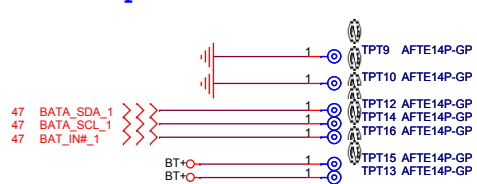
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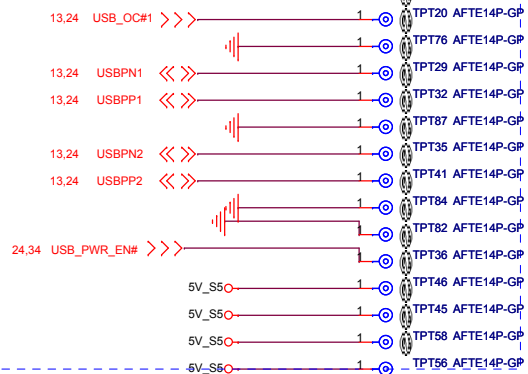
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### BAT Conn. Test Point keep on connector side



### USB\_CN1 Conn. Test Point keep on connector side



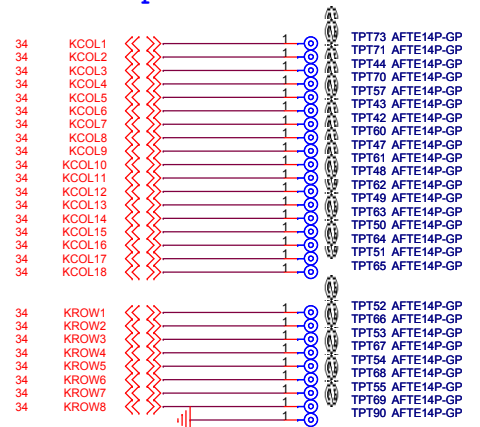
### Speaker Conn. Test Point keep on connector side



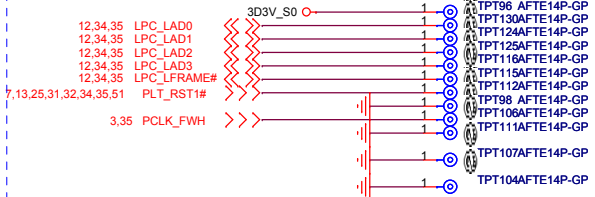
### FAN1 Conn. Test Point keep on connector side



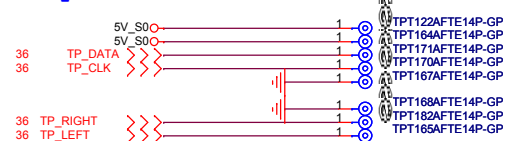
### KB1 Conn. Test Point keep on connector side



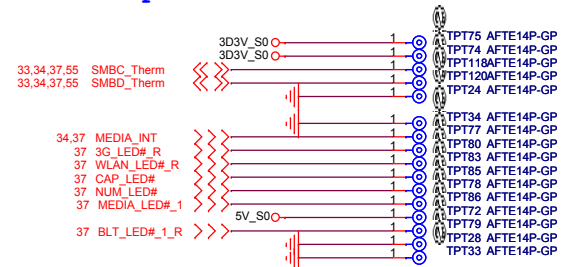
### DEBUG BOARD Conn. Test Point keep on connector side



### TOUCH PAD Conn. Test Point keep on connector side



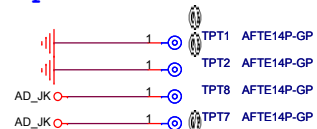
### MMB1 Conn. Test Point keep on connector side



### Powerbutton Conn. Test Point keep on connector side



### DC-IN Conn. Test Point keep on connector side



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Title

**AFTE TP**

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Rev

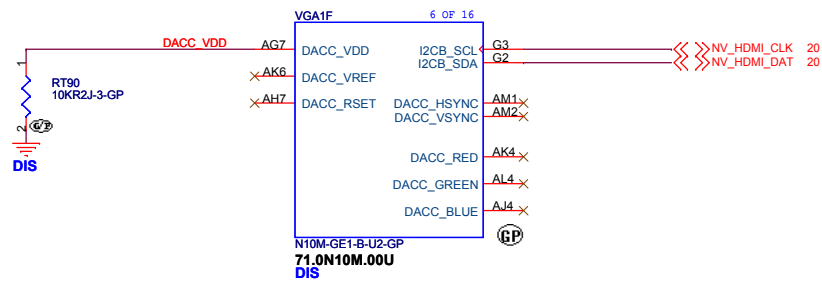
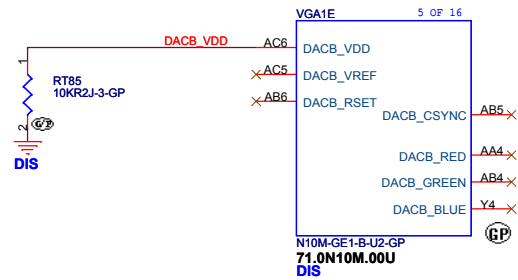
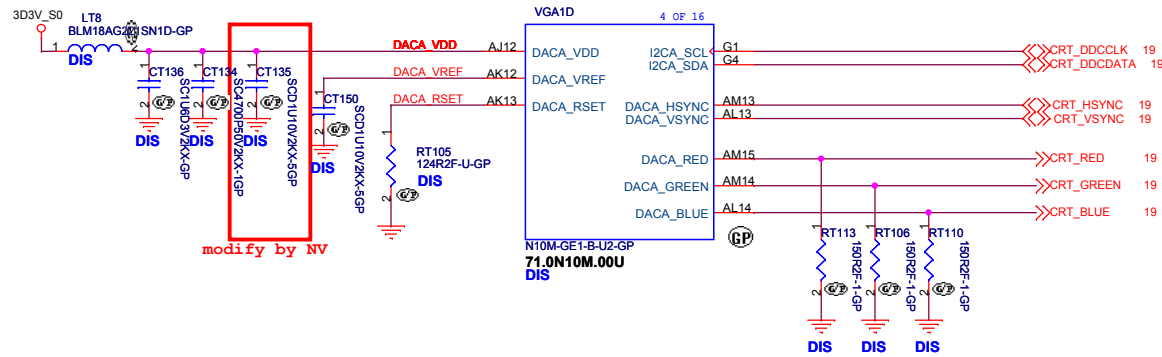
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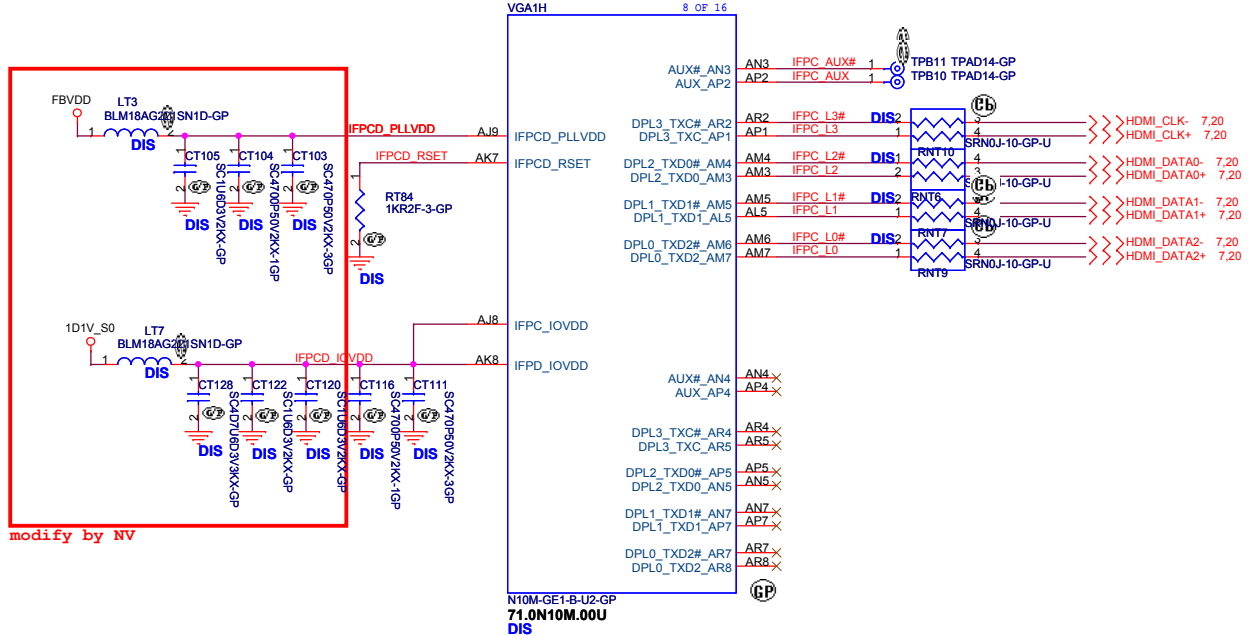
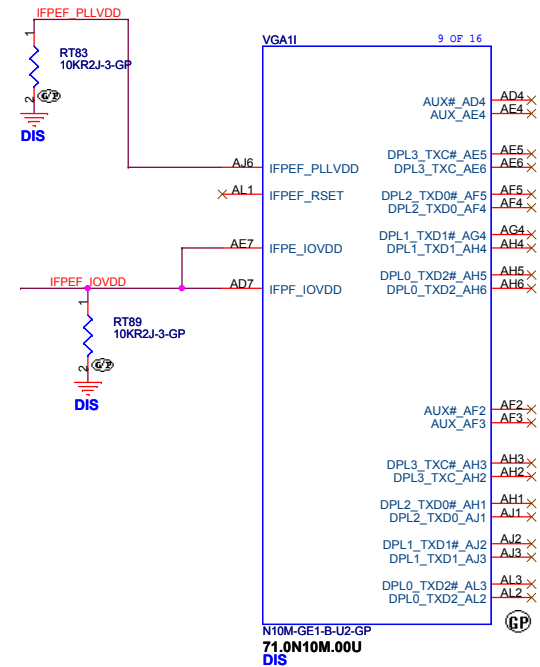
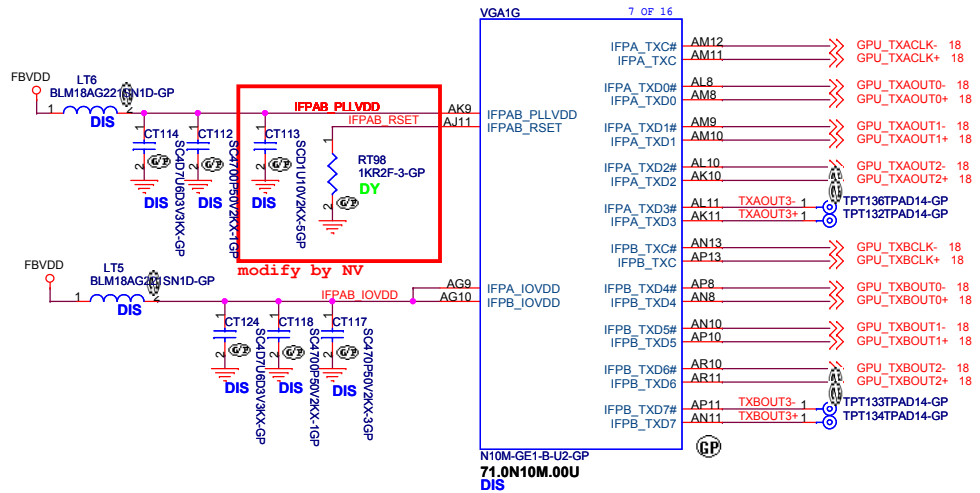
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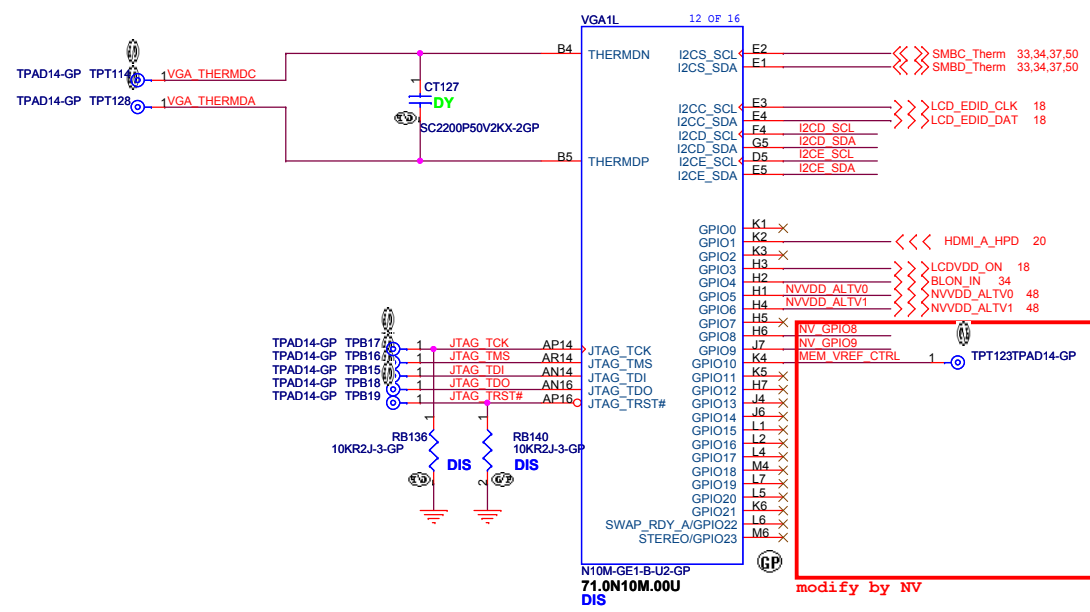
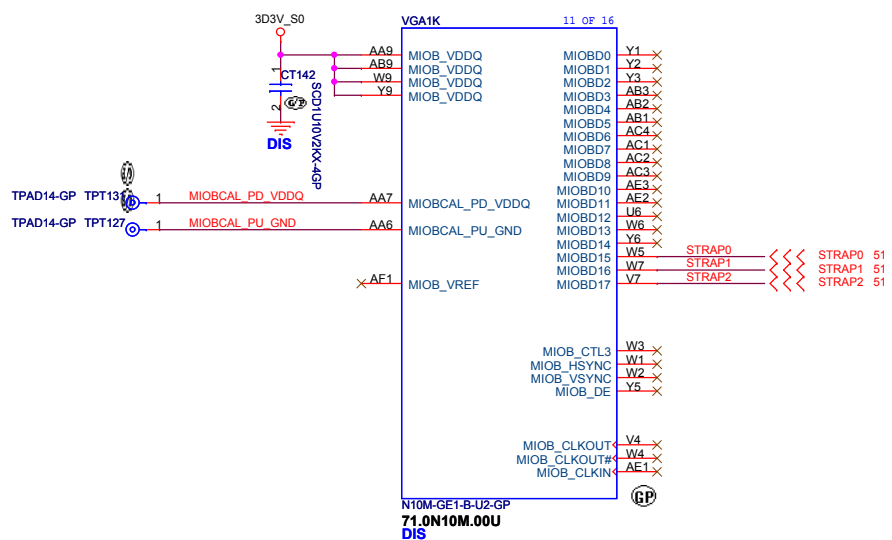
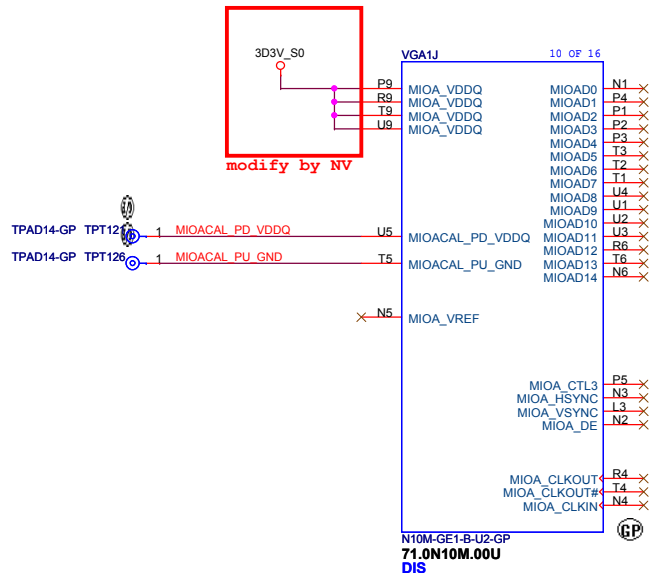


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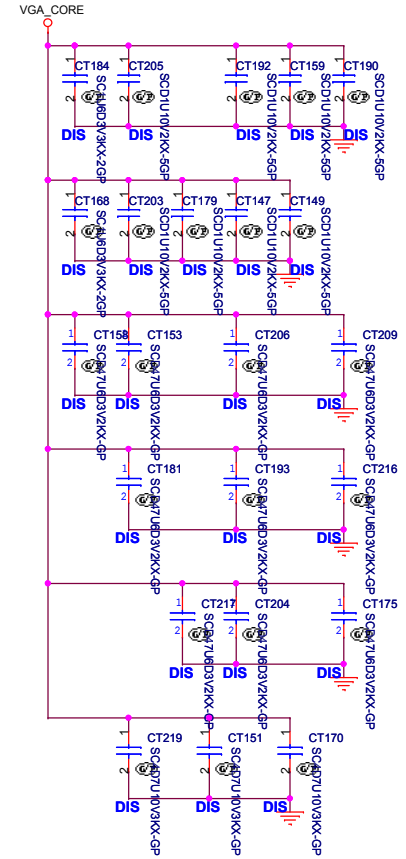
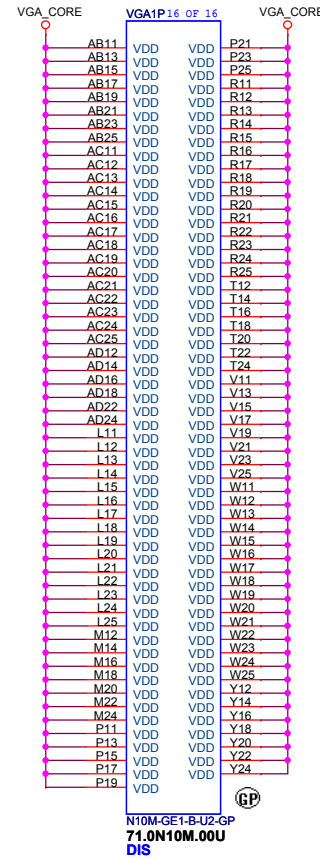
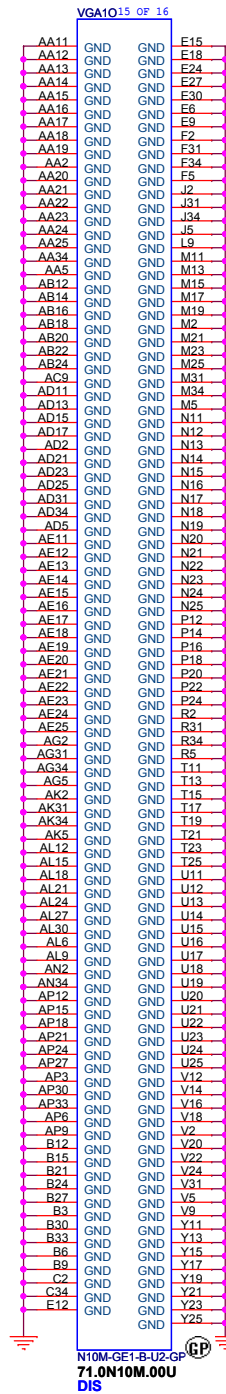
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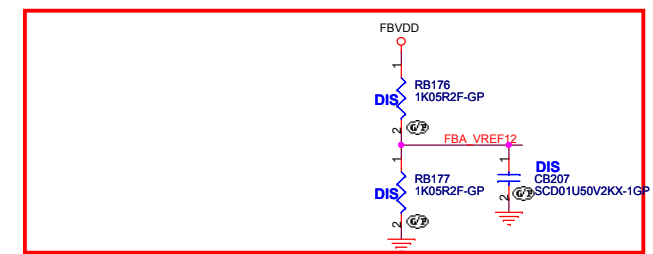
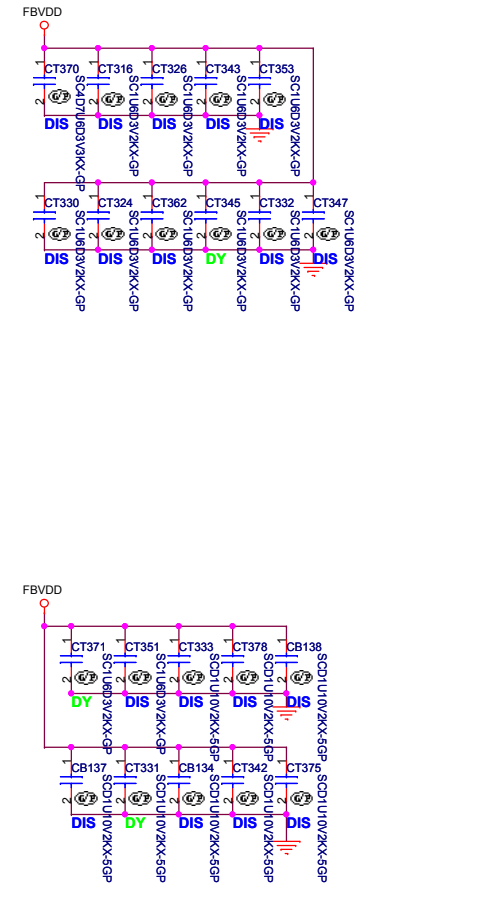
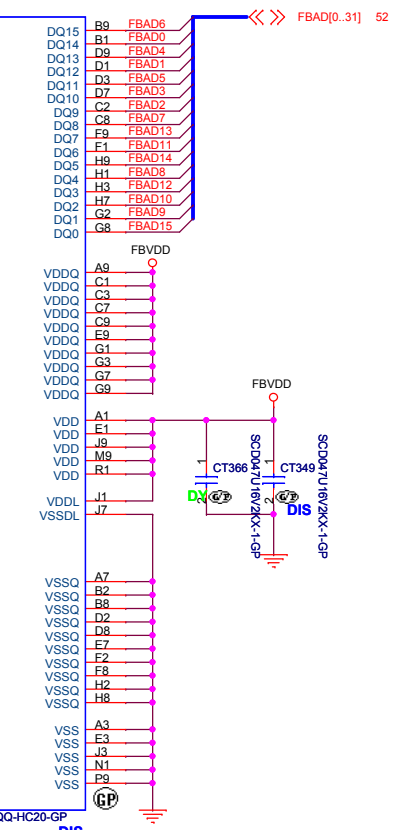
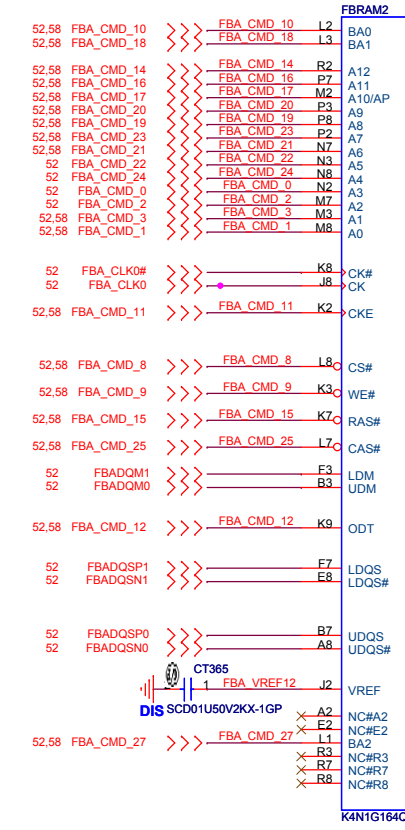
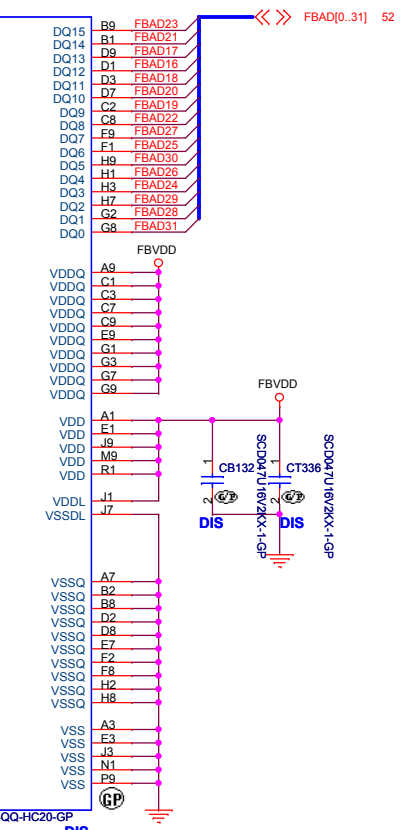
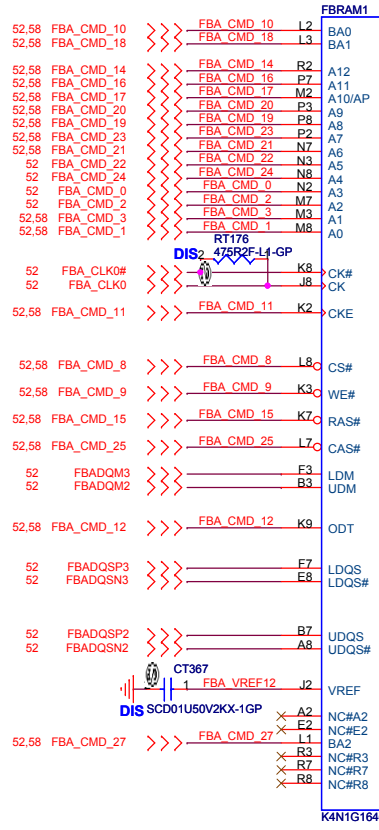
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<b>N10M(6/6) POWER</b>	
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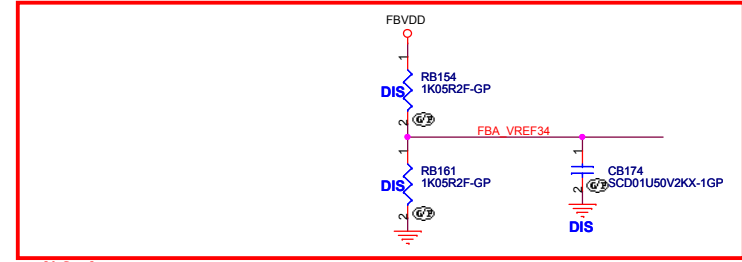
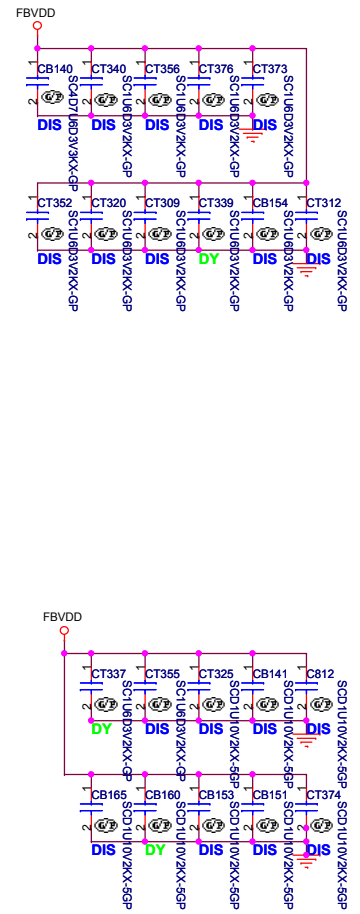
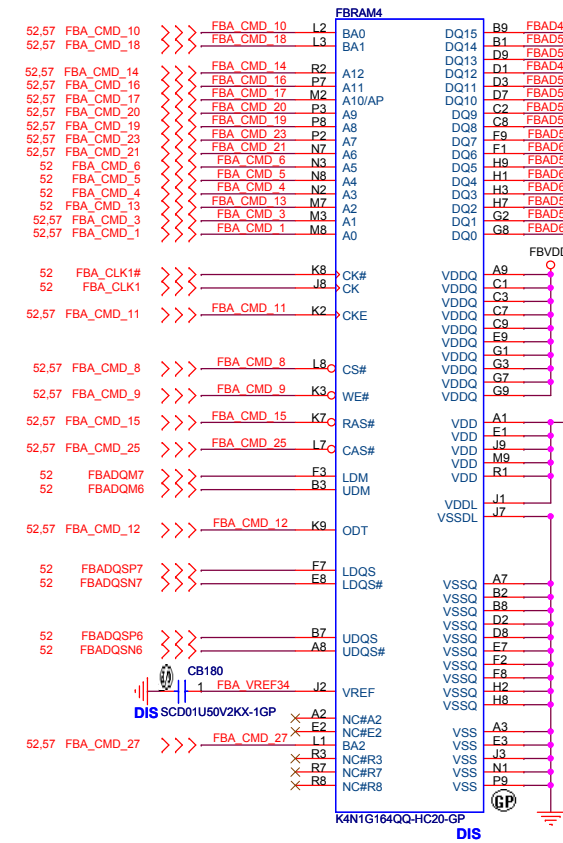
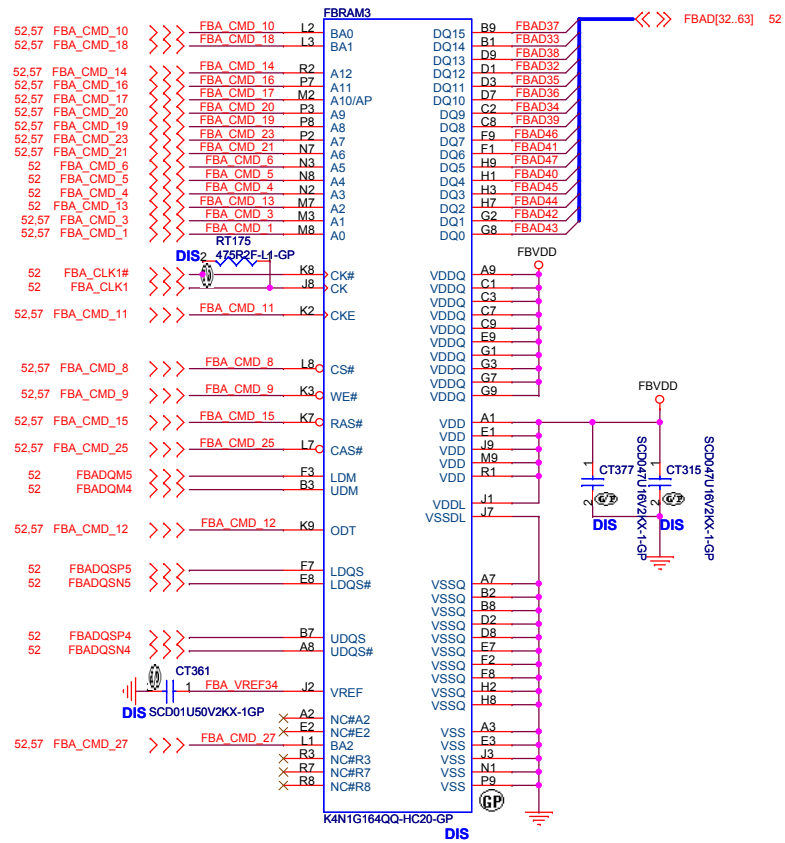
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Title: **VRAM(1/2)**

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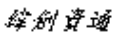


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Title		
<b>VRAM(2/2)</b>		
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<b>HISTORY</b>	
Size	Document Number
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