KIWA7/A8

Schematics Document

Mobile Penryn uFCPGA with Intel Cantiga_GM/PM+ICH9-M core logic

REV:0.4

Security Classification	Compal Secret Data		
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Title: **Cover Sheet**

Size	Document Number	Rev
B	KIWAX_LA-5082P	0.4

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Compal confidential
File Name :

ZZZ
15W_PCB_LA5082P

POWER Board

CAP SENSE LEDs Board

USB board

VRAM
64*16
DDRII page21,22

NV10M-GS
40nm page16,17,18,19,20

PCI-E X16

Mobile Penryn
uFCPGA-478 CPU
page5,6,7

H_A#(3..35)
H_D#(0..63)

FSB
667/800/1066MHz

Clock Gen.
SLG8SP556VTR
ICS9LPRS387AKLFT
page23

HDMI CONN page24

Parade 8101T page24

PCI-E

Intel Cantiga GMCH
PCBGA 1329
page 8,9,10,11,12,13

DDR3 -800
DDR3-1066

Dual Channel

DDR3-SO-DIMM X2
BANK 0, 1, 2, 3
page 14,15

CRT & TV OUT page26

LVDS I/F

LVDS Connector page25

DMI

C-Line

AMP&Audio Jack page36

PCI Express Mini card Slot page31

6*PCI-E BUS

Intel ICH9-M
mBGA-676
page27,28,29,30

AZALIA

12*USB2.0

Audio Codec
CX20561 page35

New Card page40

3.3V / 33 MHz

USB 2.0 BUS

4*SATA serial

BCM5906
10/100/LAN page32

Card Reader
RTS 5159 page38

LPC BUS

CMOS Camera page41

BlueTooth Conn page41

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Card reader(XD/SD
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HD SD) page38

EC
ENE KB926 page37

Int.KBD page39

BIOS page40

Touch Pad page39

SATA HDD Connector page34

SATA CDROM Connector page34

Key component
Manufacturer
Compal P/N
R1 Desc

Northbridge
Intel / Cantiga PM45
SA00002JJM0
S IC AC82PM45 QV11 A1 FCBGA 1329 PM C38

Intel / Cantiga GM 45
SA00002JTD0
S IC AC82GM45 SLB94 B3 FCBGA1329 GM C38!

SouthBridge
Intel / ICH9M
SA00002JH90
S IC AF82801IBM SLB8Q A3 676P ICH9M C38! (MP)

VGA Chip
Nvidia / N10M
SA00002V810
S IC N10M-GE1-S-U2(H) BGA 533P C38

VRAM
DDR2/512MB
SA00002MF00 (14")
S IC D2 64M16/500 HYB18T1G161C2F-20

SA00002UH00 (15.6")
S IC D2 64M16/500 H5PS1G63EFR-20L FBGA84

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Title: MB Block Diagram

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DDR3 Voltage Rails

power plane / State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +0.75V +VCCP +CPU_CORE +VGA_CORE +1.8VS
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

SMBUS, SPI and I2C Control Table

	SOURCE	HDMI	LVDS	CRT	HDCP	SERIAL EEPROM	NEW CARD	CLK GEN	CAP sensor	Mini CARD1	Mini CARD2	BATT	THERMAL SENSOR (VGA)	THERMAL SENSOR (CPU)
EC_SMB_CK1 EC_SMB_DA1	KB926	X	X	X	X	X	X	X	X	X	X	V	X	X
EC_SMB_CK2 EC_SMB_DA2	KB926	X	X	X	X	X	X	X	V	X	X	X	V	V
ICH_SMBCLK ICH_SMBDAT	ICH9	X	X	X	X	X	V	V	X	V	V	X	X	X
LVDS_SCL LVDS_SDA	Cantiga	X	V	X	X	X	X	X	X	X	X	X	X	X
GMCH_CRT_CLK GMCH_CRT_DAT	Cantiga	X	X	V	X	X	X	X	X	X	X	X	X	X
HDMICLK_NB HDMIDAT_NB	Cantiga	V	X	X	X	X	X	X	X	X	X	X	X	X
VGA_DDCCLK VGA_DDCDATA	VGA	X	X	V	X	X	X	X	X	X	X	X	X	X
VGA_LVDS_SCL VGA_LVDS_DAT	VGA	X	V	X	X	X	X	X	X	X	X	X	X	X
VGA_HDMI_SCL VGA_HDMI_DAT	VGA	V	X	X	X	X	X	X	X	X	X	X	X	X
HDCP_SMB_CK1 HDCP_SMB_DA1	VGA	X	X	X	V	X	X	X	X	X	X	X	X	X
FSEL#SPICS#_SB FRD#SPI_SO_SB SPI_CLK_SB FWR#SPI_SI_SB	ICH9	X	X	X	X	X	X	X	X	X	X	X	X	X
FSEL#SPICS# FRD#SPI_SO SPI_CLK FWR#SPI_SI	KB926	X	X	X	X	V	X	X	X	X	X	X	X	X

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Title: MB Notes List

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VGA and DDR2 Voltage Rails (N10M)

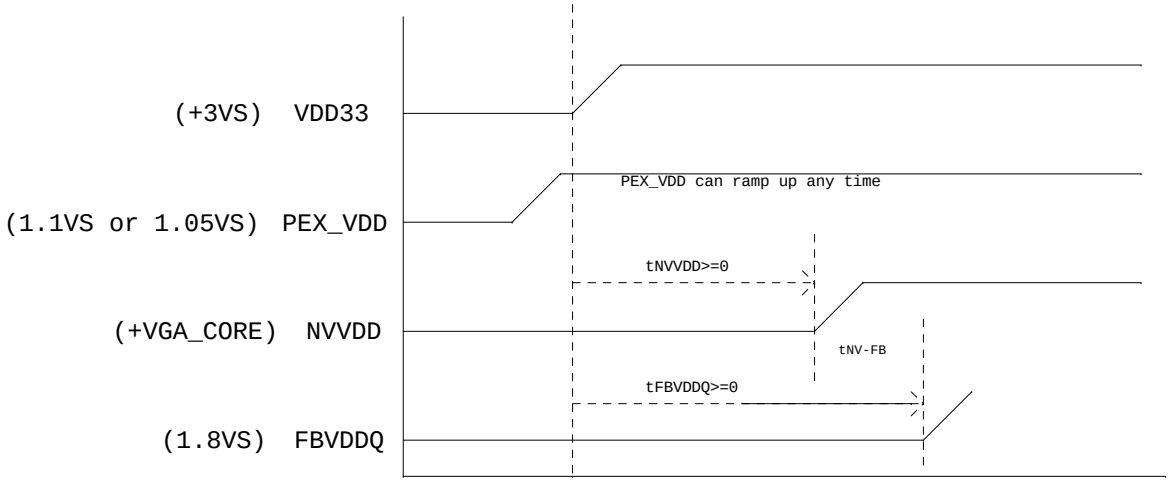
power plane / State				+3VS +VGA_CORE +1.1VS (for 55nm) +1.05VS (for 40nm) +1.8VS
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

EDP at Tj = 97C*

Power Supply Rail	(V)	NB9M-GS		N10M-GE1-S	
		GDDR3	DDR2	GDDR3	DDR2
NVVDD	Variable	11.22A	10.87A	13.56A	13.47A
FB_DLLAVDD	1.1	25mA		25mA	
FB_PLLAVDD	1.1	10mA		10mA	
IFPC_IOVDD	1.1	385mA		180mA	
IFPD_IOVDD	1.1	385mA		180mA	
IFPE_IOVDD	1.1	385mA		180mA	
IFPF_IOVDD	1.1	385mA		180mA	
PEX_IOVDD/Q	1.1	1550mA		1550mA	
PEX_PLLVDD	1.1	165mA		65mA	
PLLVDD	1.1	55mA		30mA	
SP_PLLVDD	1.1	25mA		10mA	
VID_PLLVDD	1.1	50mA		25mA	
TOTAL	1.1	3.425A		2.435A	
FBVDD/Q	1.8	2.24A	1.65A	2.24A	1.75A
IFPA_IOVDD	1.8	50mA		50mA	
IFPB_IOVDD	1.8	50mA		50mA	
IFPAB_PLLVDD	1.8	100mA		75mA	
IFPCD_PLLVDD	1.8	160mA		80mA	
IFPEF_PLLVDD	1.8	160mA		80mA	
TOTAL	1.8	2.76A	2.17A	2.575A	2.085A
DACA_VDD	3.3	110mA		110mA	
DACB_VDD	3.3	125mA		125mA	
DACC_VDD	3.3	110mA		110mA	
MIOA_VDDQ	3.3	10mA		10mA	
MIOB_VDDQ	3.3	10mA		10mA	
VDD33	3.3	80mA		80mA	
TOTAL	3.3	0.445A		0.445A	

POWER SQUENCE

The ramp time for any rail must be more than 40us



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Title: VGA Notes List

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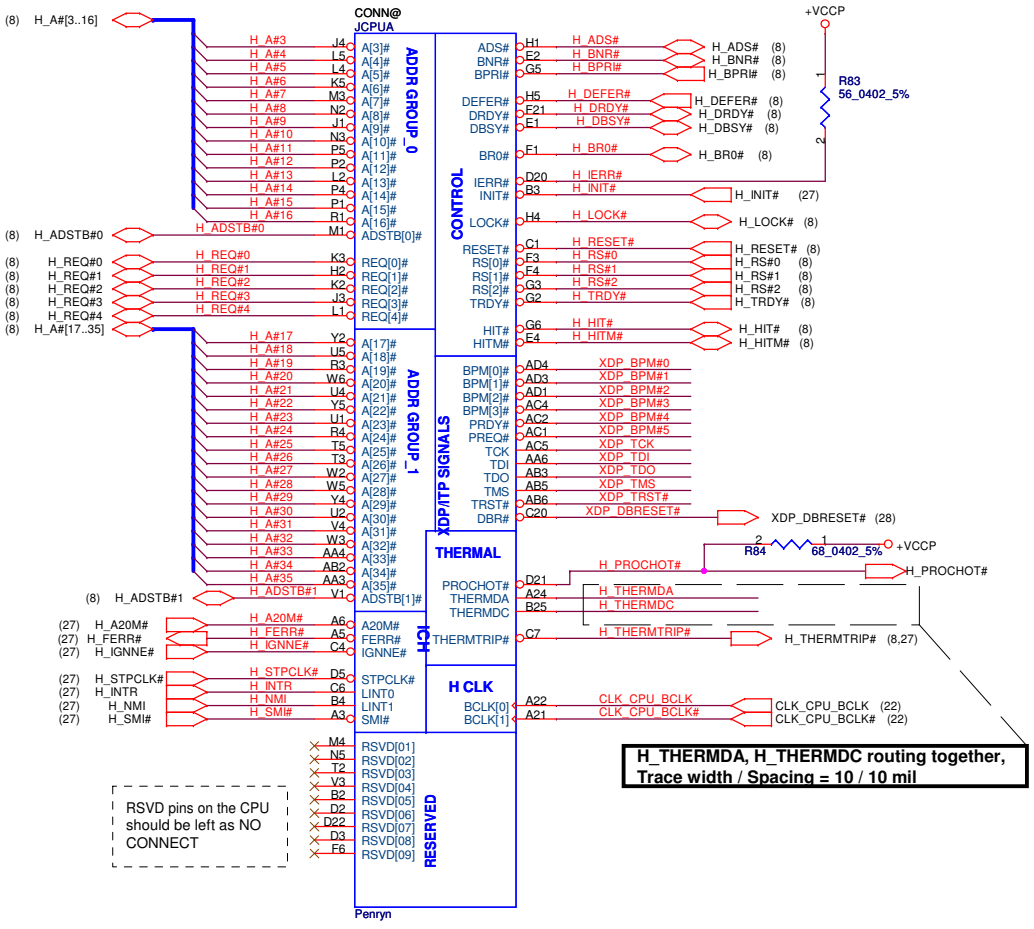
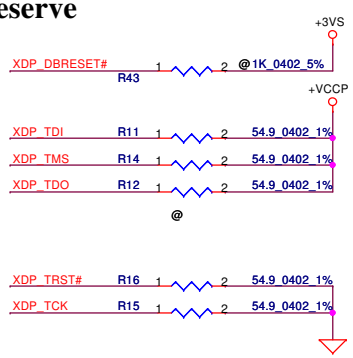
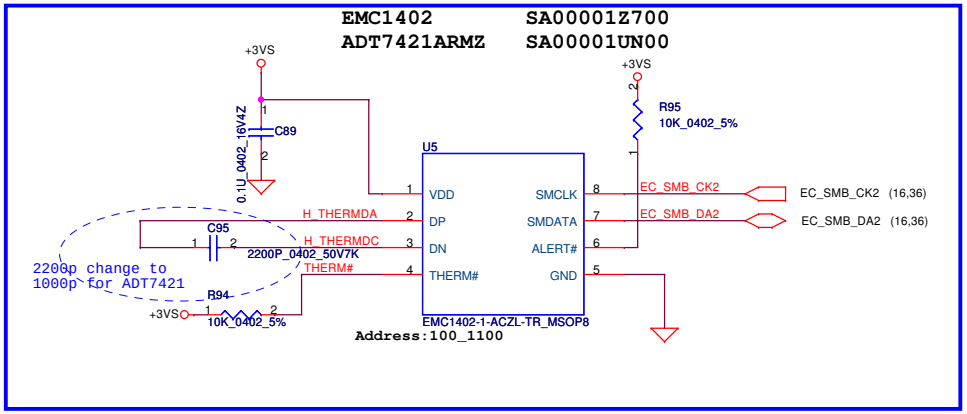
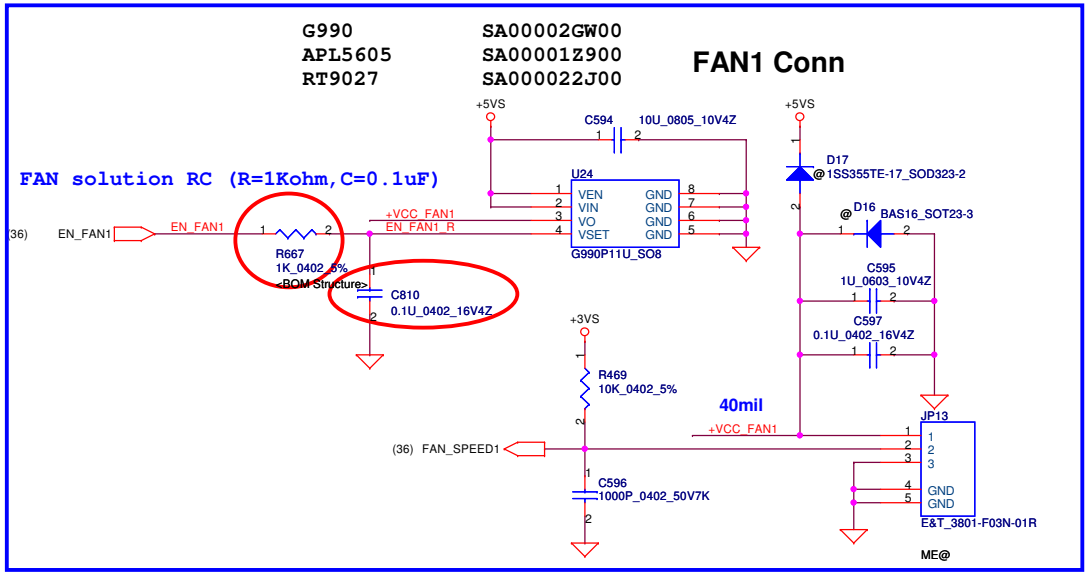


H_THERMDA, H_THERMDC routing together, Trace width / Spacing = 10 / 10 mil

XDP Reserve







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Compal Electronics, Inc.			
Title: Penryn (1/3)			
Size: B	Document Number: KIWAX_LA-5082P		Rev: 0.4
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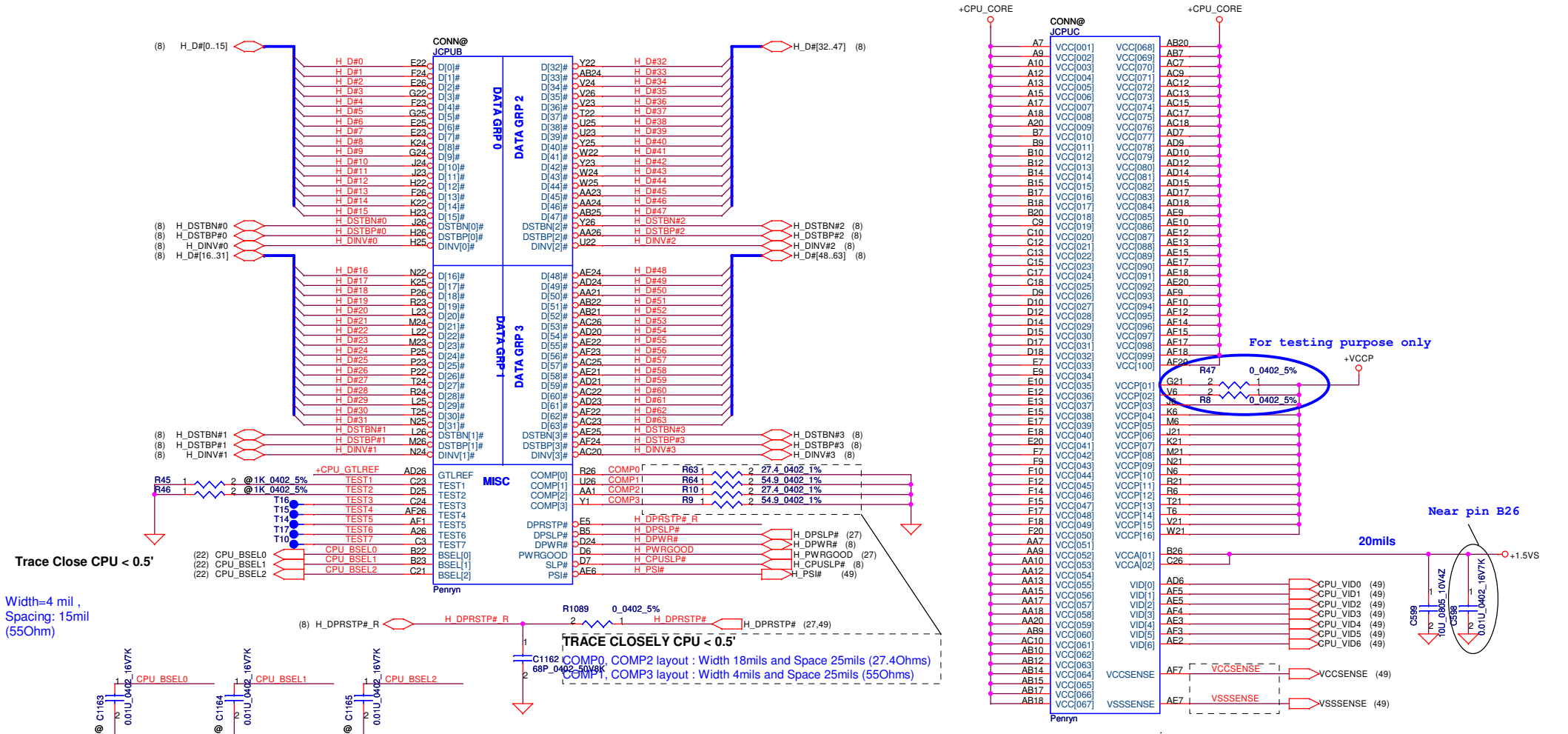

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0

Layout note: Z0=55 ohm
0.5" max for GTLREF.

Close to CPU pin AD26
within 500mils.

Length match within 25 mils.
The trace width/space/other is
16/7/25.

Layout Note:
Route VCCSENSE and VSSSENSE traces at
27.4 Ohms with 50 mil spacing.
Place PU and PD within 1 inch of CPU.
Length matched to within 25 mils.

Close to CPU pin
within 500mils.

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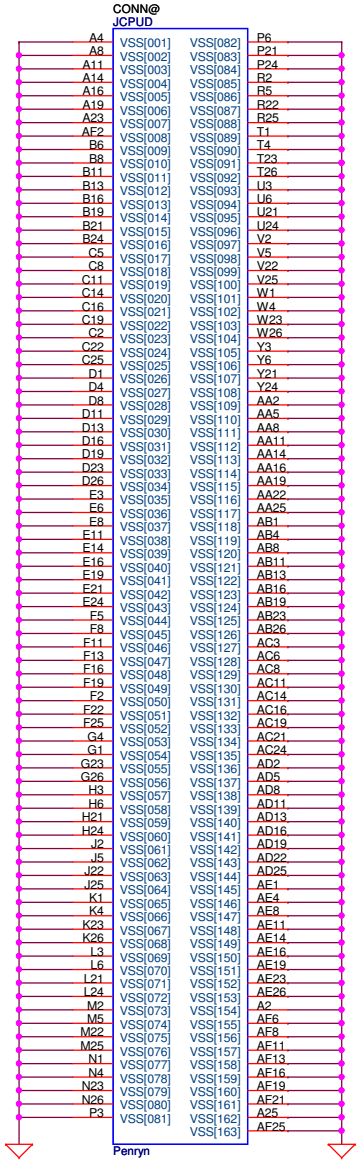
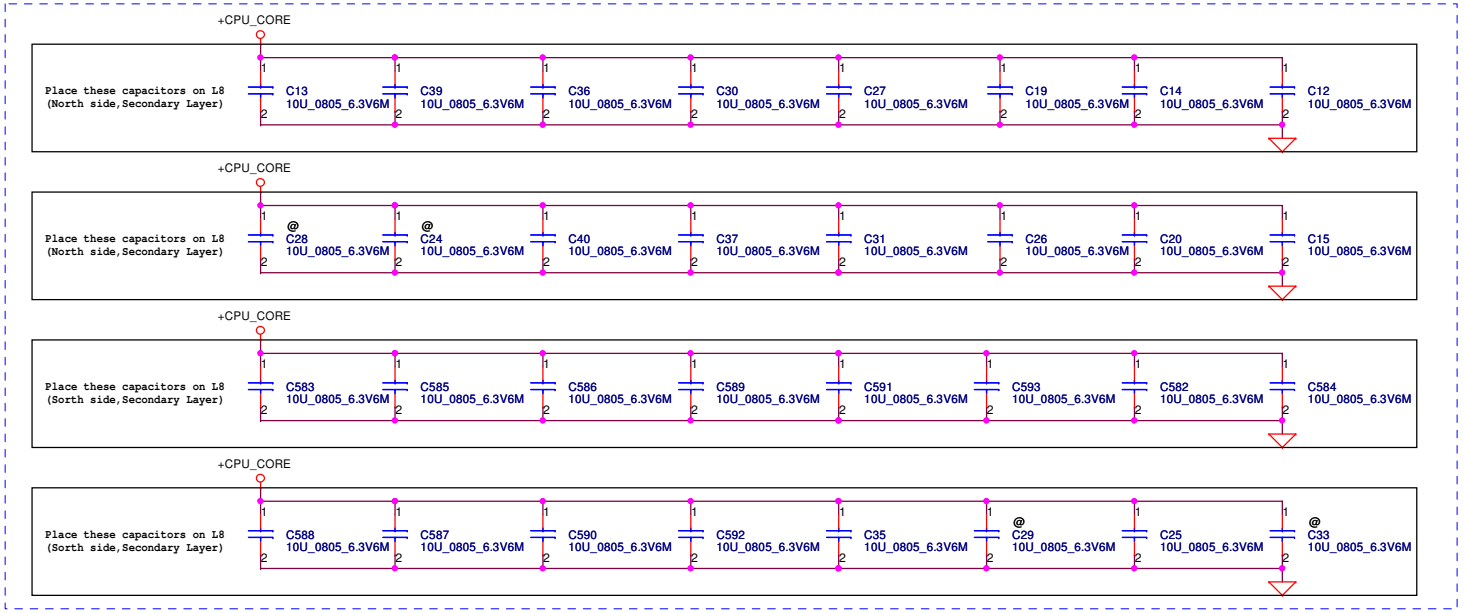
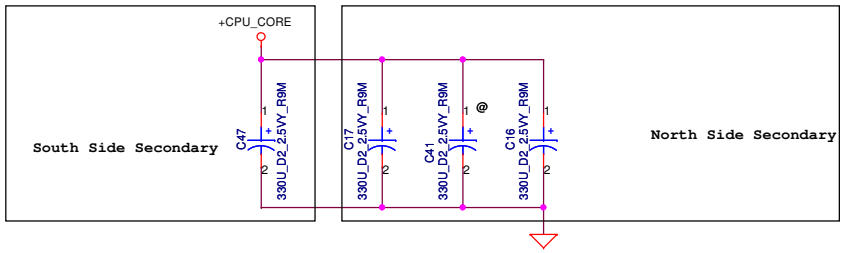
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.			
Title: Penryn (2/3)			
Size: B	Document Number: KIWAX_LA-5082P		Rev: 0.4
Date: Wednesday, March 18, 2009	Sheet 6 of 53		

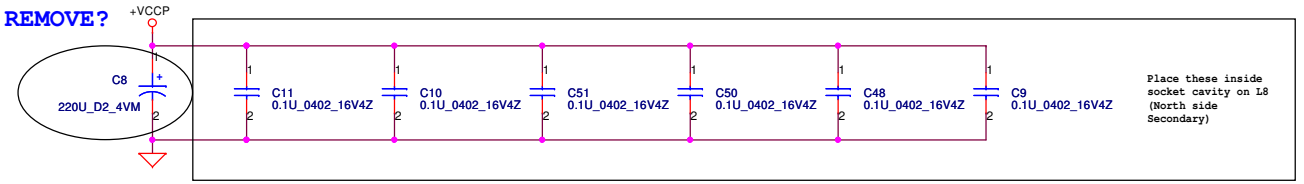




Mid Frequence Decoupling



ESR <= 1.5m ohm
Capacitor > 1980uF



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.			
Title: Penryn (3/3)			
Size: B	Document Number: KIWAX_LA-5082P		Rev: 0.4
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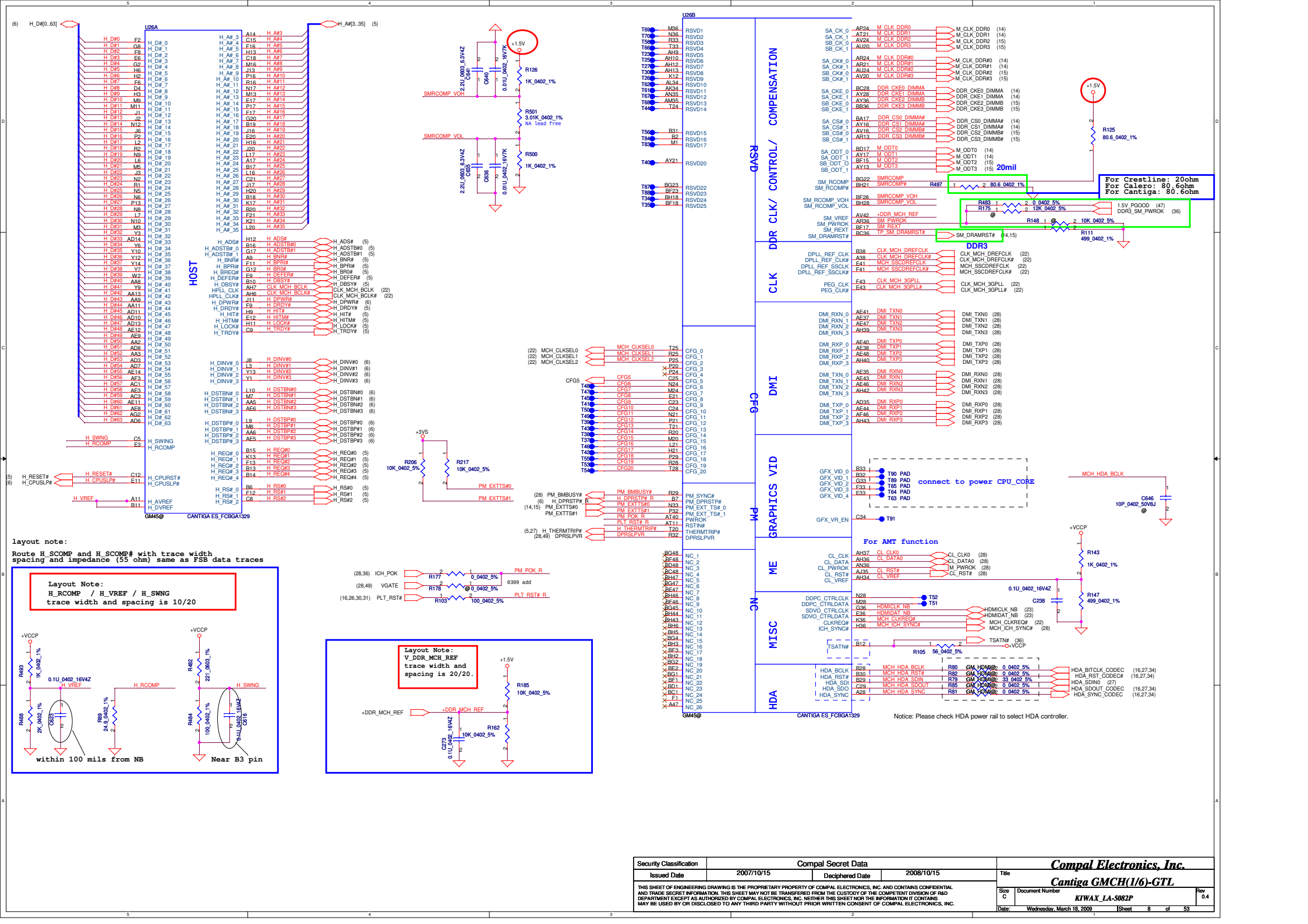

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: Cantiga GMCH(1/6)-GTL

Size	Document Number	Rev
C	KIWAX_LA-5082P	0.4

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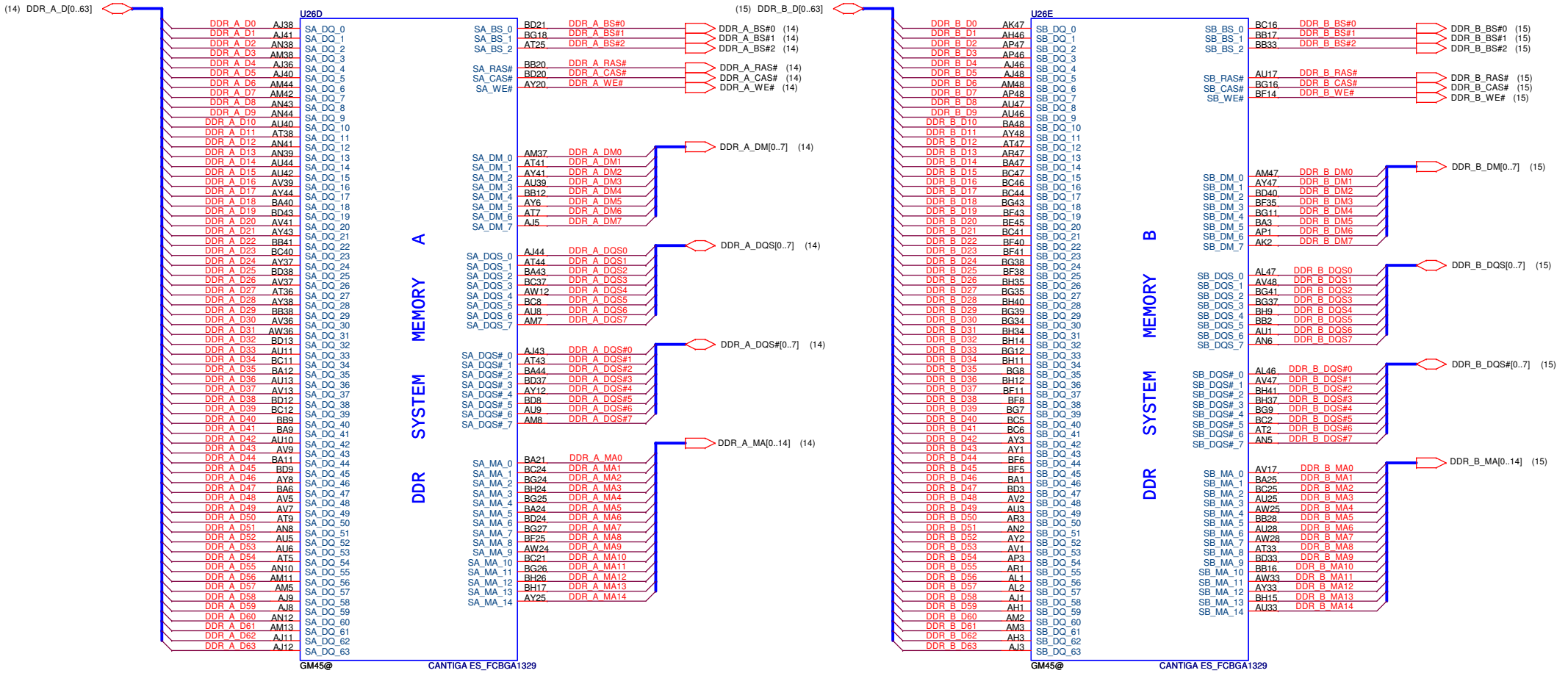

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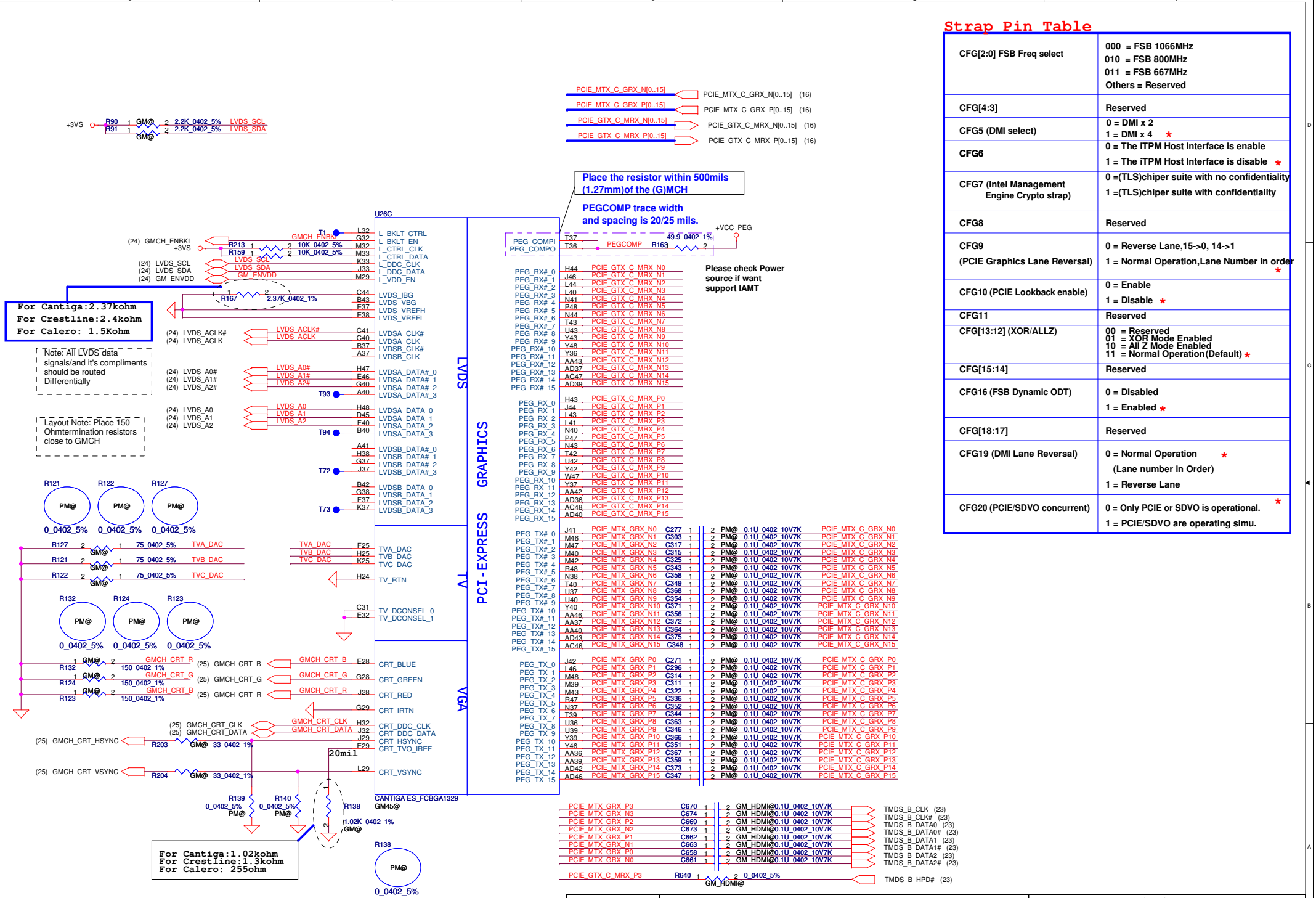
Title: **Cantiga GMCH (2/6)-DDRII**

Size	Document Number	Rev
B	KIWAX_LA-5082P	0.4

Date: Wednesday, March 18, 2009 Sheet 9 of 53



Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 =(TLS)chiper suite with no confidentiality 1 =(TLS)chiper suite with confidentiality
CFG8	Reserved
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIE Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.

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Title: **Cantiga GMCH (3/6)-VGA/LVDS/TV**

Size	Document Number	Rev
Custom	KIWAX_LA-5082P	0.4

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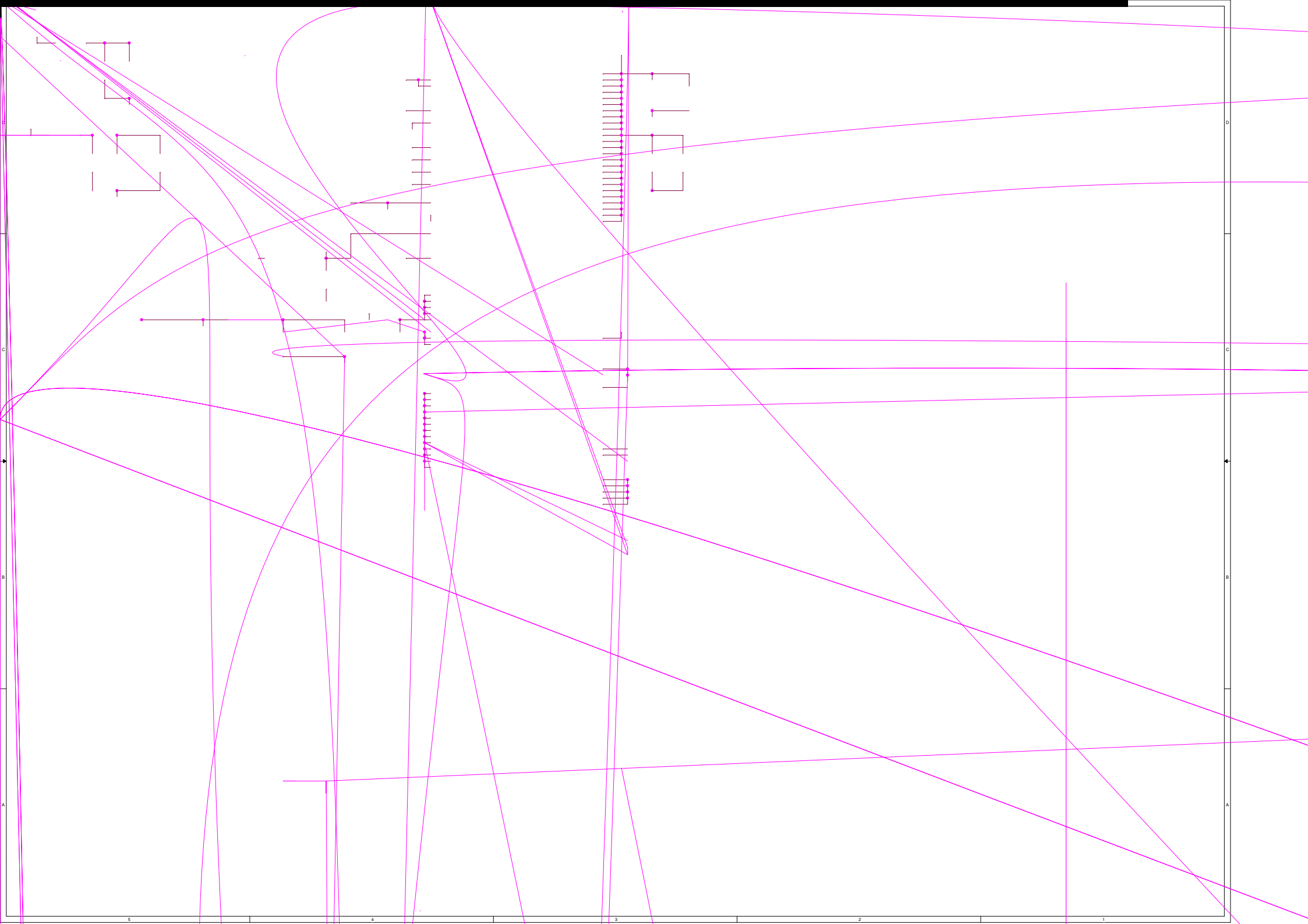

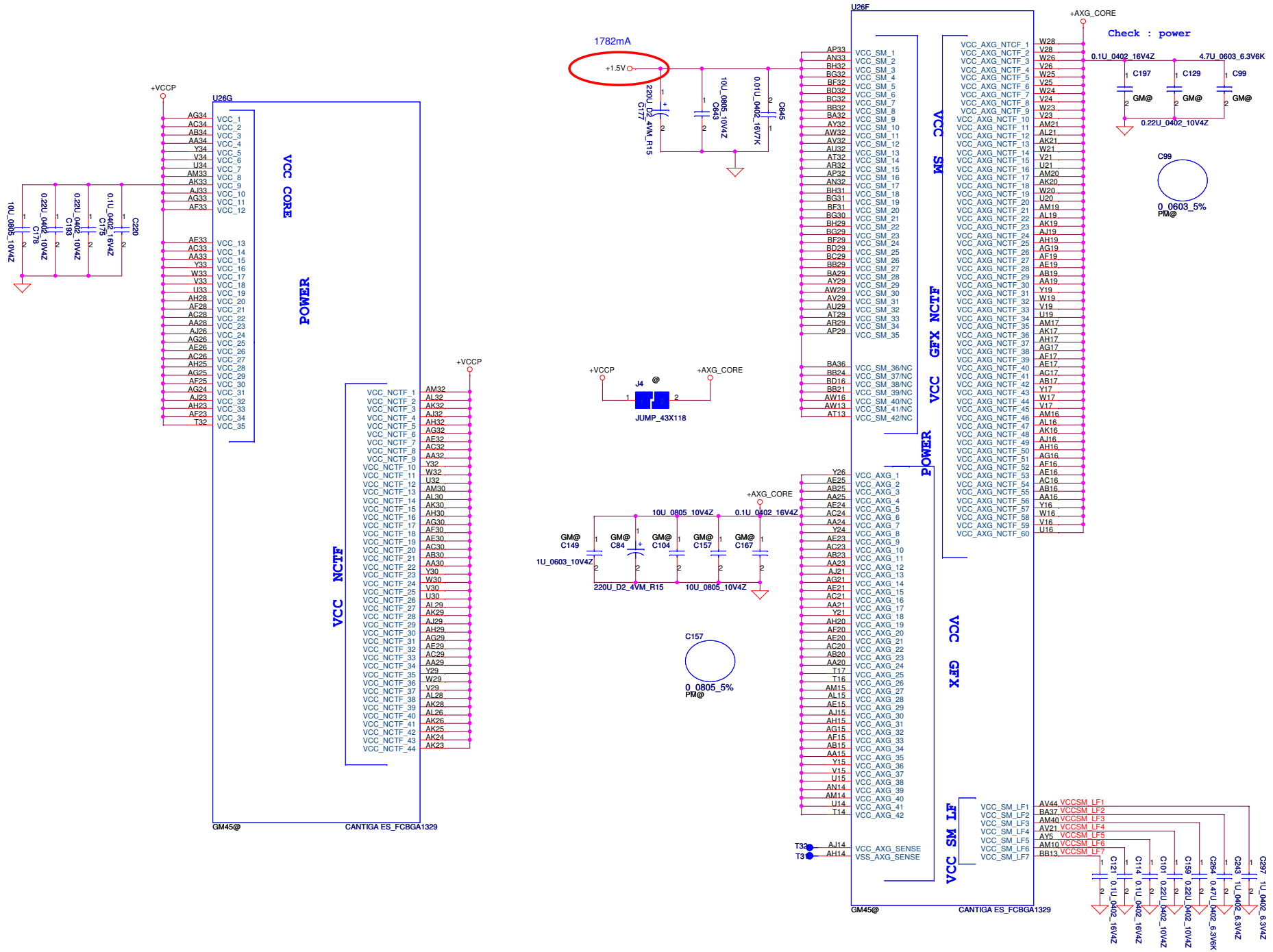

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Issued Date	2007/10/15	Deciphered Date	2008/10/15

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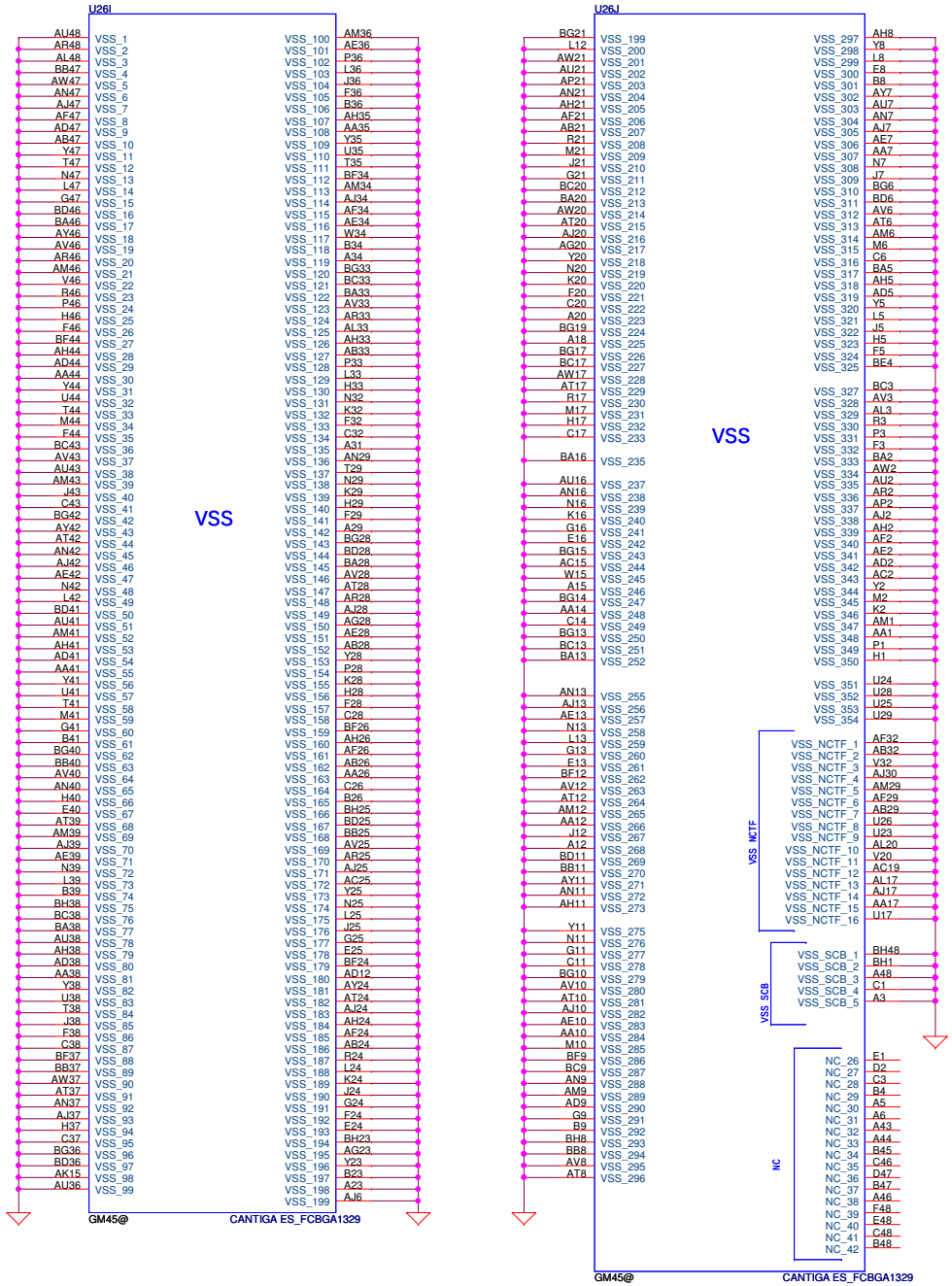
Title: **Crestline GMCH (5/6)-VCC**

Size	Document Number	Rev
Custom	KIWAX_LA-5082P	0.4

Date: Wednesday, March 18, 2009 | Sheet 12 of 53



Security Classification	Compal Secret Data		
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Title: **Cantiga GMCH (6/6)-GND**

Size	Document Number	Rev
Custom	KIWAX_LA-5082P	0.4

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(9) DDR_A_DQS#[0..7]
(9) DDR_A_D[0..63]
(9) DDR_A_DM[0..7]
(9) DDR_A_DQS[0..7]
(9) DDR_A_MA[0..14]

+1.5V
R625 100_0402_1%
+V_DDR3_DIMM_REF
R626 100_0402_1%
C755 0.1U_0402_16V4Z

Layout Note:
Place near JP4

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

+1.5V
C761 10U_0805_6.3V6M
C760 10U_0805_6.3V6M
C767 10U_0805_6.3V6M
C763 10U_0805_6.3V6M
C764 10U_0805_6.3V6M
C765 10U_0805_6.3V6M
C766 10U_0805_6.3V6M
C750 0.1U_0402_16V4Z
C752 0.1U_0402_16V4Z
C749 0.1U_0402_16V4Z
C753 0.1U_0402_16V4Z
C787 470U_D2_2.5VM_R15 @

<BOM Structure> <BOM Structure> <BOM Structure> <BOM Structure>

Layout Note:
Place near JP4.203 & JP4.204

+0.75VS
C778 1U_0603_10V4Z
C779 1U_0603_10V4Z
C776 1U_0603_10V4Z
C777 1U_0603_10V4Z
C762 10U_0805_6.3V6M

+1.5V
+V_DDR3_DIMM_REF
JP17

1	VREF_DQ	VSS1	2
3	VSS2	DQ4	4
5	DQ0	DQ5	6
7	DQ1	VSS3	8
9	VSS4	DQS#0	10
11	DM0	DQS0	12
13	VSS5	VSS6	14
15	DQ2	DQ6	16
17	DQ3	DQ7	18
19	VSS7	VSS8	20
21	DQ8	DQ12	22
23	DQ9	DQ13	24
25	VSS9	VSS10	26
27	DQS#1	DM1	28
29	DQS1	RESET#	30
31	VSS11	VSS12	32
33	DQ10	DQ14	34
35	DQ11	DQ15	36
37	VSS13	VSS14	38
39	DQ16	DQ20	40
41	DQ17	DQ21	42
43	VSS15	VSS16	44
45	DQS#2	DM2	46
47	DQS2	VSS17	48
49	VSS18	DQ22	50
51	DQ18	DQ23	52
53	DQ19	VSS19	54
55	VSS20	DQ28	56
57	DQ24	DQ29	58
59	DQ25	VSS21	60
61	VSS22	DQS#3	62
63	DM3	DQS3	64
65	VSS23	VSS24	66
67	DQ26	DQ30	68
69	DQ27	DQ31	70
71	VSS25	VSS26	72
73	CKE0	CKE1	74
75	VDD1	VDD2	76
77	NC1	A15	78
79	BA2	A14	80
81	VDD3	VDD4	82
83	A12/BC#	A11	84
85	A9	A7	86
87	VDD5	VDD6	88
89	A8	A6	90
91	A5	A4	92
93	VDD7	VDD8	94
95	A3	A2	96
97	A1	A0	98
99	VDD9	VDD10	100
101	CK0	CK1	102
103	CK0#	CK1#	104
105	VDD11	VDD12	106
107	A10/AP	BA1	108
109	BA0	RAS#	110
111	VDD13	VDD14	112
113	WE#	S0#	114
115	CAS#	ODT0	116
117	VDD15	VDD16	118
119	A13	ODT1	120
121	S1#	NC2	122
123	VDD17	VDD18	124
125	NCTEST	VREF_CA	126
127	VSS27	VSS28	128
129	DQ32	DQ36	130
131	DQ33	DQ37	132
133	VSS29	VSS30	134
135	DQS#4	DM4	136
137	DQS4	VSS31	138
139	VSS32	DQ38	140
141	DQ34	DQ39	142
143	DQ35	VSS33	144
145	VSS34	DQ44	146
147	DQ40	DQ45	148
149	DQ41	VSS35	150
151	VSS36	DQS#5	152
153	DM5	DQS5	154
155	VSS37	VSS38	156
157	DQ42	DQ46	158
159	DQ43	DQ47	160
161	VSS39	VSS40	162
163	DQ48	DQ52	164
165	DQ49	DQ53	166
167	VSS41	VSS42	168
169	DQS#6	DM6	170
171	DQS6	VSS43	172
173	VSS44	DQ54	174
175	DQ50	DQ55	176
177	DQ51	VSS45	178
179	VSS46	DQ60	180
181	DQ56	DQ61	182
183	DQ57	VSS47	184
185	VSS48	DQS#7	186
187	DM7	DQS7	188
189	VSS49	VSS50	190
191	DQ58	DQ62	192
193	DQ59	DQ63	194
195	VSS51	VSS52	196
197	SA0	EVENT#	198
199	VDDSPD	SDA	200
201	SA1	SCL	202
203	VTT1	VTT2	204
205	G1	G2	206

FOX_AS0A626-U2RN-7F
ME@

DDR_A_D0 DDR_A_D1 DDR_A_DM0 DDR_A_D2 DDR_A_D3 DDR_A_D8 DDR_A_D9 DDR_A_DQS#1 DDR_A_DQS1 DDR_A_D10 DDR_A_D11 DDR_A_D16 DDR_A_D17 DDR_A_DQS#2 DDR_A_DQS2 DDR_A_D18 DDR_A_D19 DDR_A_D24 DDR_A_D25 DDR_A_DM3 DDR_A_D26 DDR_A_D27
DDR_A_D4 DDR_A_D5 DDR_A_DQS#0 DDR_A_DQS0 DDR_A_D6 DDR_A_D7 DDR_A_D12 DDR_A_D13 DDR_A_DM1 SM_DRAMRST# (8,15) DDR_A_D14 DDR_A_D15 DDR_A_D20 DDR_A_D21 DDR_A_DM2 DDR_A_D22 DDR_A_D23 DDR_A_D28 DDR_A_D29 DDR_A_DQS#3 DDR_A_DQS3 DDR_A_D30 DDR_A_D31

(8) DDR_CKE0_DIMMA DDR_CKE0_DIMMA
DDR_CKE1_DIMMA DDR_CKE1_DIMMA (8)
(9) DDR_A_BS#2 DDR_A_BS2
DDR_A_MA12 DDR_A_MA9 DDR_A_MA8 DDR_A_MA5 DDR_A_MA3 DDR_A_MA1
DDR_A_MA14 DDR_A_MA11 DDR_A_MA7 DDR_A_MA6 DDR_A_MA4 DDR_A_MA2 DDR_A_MA0
(8) M_CLK_DDR0 (8) M_CLK_DDR#0 M_CLK_DDR0 M_CLK_DDR#0
M_CLK_DDR1 M_CLK_DDR#1
M_CLK_DDR1 (8) M_CLK_DDR#1 (8)
DDR_A_MA10 DDR_A_BS0
DDR_A_BS1 DDR_A_RAS#
(9) DDR_A_BS#0 DDR_A_BS#1 (9) DDR_A_RAS# (9)
(9) DDR_A_WE# (9) DDR_A_CAS# DDR_A_WE# DDR_A_CAS#
DDR_CS0_DIMMA# M_ODT0
DDR_CS0_DIMMA# (8) M_ODT0 (8)
DDR_A_MA13 DDR_CS1_DIMMA#
M_ODT1
M_ODT1 (8)
(8) DDR_CS1_DIMMA#
DDR_VREF_CA_DIMMA
R623 0_0402_5%
+V_DDR3_DIMM_REF
C785 2.2U_0603_6.3V4Z
C751 0.1U_0402_16V4Z
DDR_A_D32 DDR_A_D33 DDR_A_DQS#4 DDR_A_DQS4 DDR_A_D34 DDR_A_D35 DDR_A_D40 DDR_A_D41 DDR_A_DM5 DDR_A_D42 DDR_A_D43 DDR_A_D48 DDR_A_D49 DDR_A_DQS#6 DDR_A_DQS6 DDR_A_D50 DDR_A_D51 DDR_A_D56 DDR_A_D57 DDR_A_DM7 DDR_A_D58 DDR_A_D59
DDR_A_D36 DDR_A_D37 DDR_A_DM4 DDR_A_D38 DDR_A_D39 DDR_A_D44 DDR_A_D45 DDR_A_DQS#5 DDR_A_DQS5 DDR_A_D46 DDR_A_D47 DDR_A_D52 DDR_A_D53 DDR_A_DM6 DDR_A_D54 DDR_A_D55 DDR_A_D60 DDR_A_D61 DDR_A_DQS#7 DDR_A_DQS7 DDR_A_D62 DDR_A_D63
PM_EXTTS#0 (8,15)
CLK_SMBDATA (15,22)
CLK_SMBCLK (15,22)
+0.75VS
+3VS
R627 10K_0402_5%
C784 2.2U_0603_6.3V4Z
C754 0.1U_0402_16V4Z
R628 10K_0402_5%

DDR3 SO-DIMM A REVERSE

Security Classification	Compal Secret Data		
Issued Date	2007/09/29	Deciphered Date	2007/09/29

Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT1

Size	Document Number	Rev
Custom	KIWAX_LA-5082P	0.4

Date: Wednesday, March 18, 2009 Sheet 14 of 53

(9) DDR_B_DQS#[0..7]
(9) DDR_B_D[0..63]
(9) DDR_B_DM[0..7]
(9) DDR_B_DQS[0..7]
(9) DDR_B_MA[0..14]

Layout Note:
Place near JP5

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

+1.5V
C771 10U_0805_6.3V6M
C775 10U_0805_6.3V6M
C772 10U_0805_6.3V6M
C763 10U_0805_6.3V6M
C774 10U_0805_6.3V6M
C773 10U_0805_6.3V6M
C766 10U_0805_6.3V6M
C756 0.1U_0402_16V4Z
C757 0.1U_0402_16V4Z
C760 0.1U_0402_16V4Z
C759 0.1U_0402_16V4Z
C788 470U_D2_2.5VM_R15 @

<BOM Structure> <BOM Structure> <BOM Structure> <BOM Structure>

Layout Note:
Place near JP5.203 & JP5.204

+0.75VS
1U_0603_10V4Z C780
1U_0603_10V4Z C781
1U_0603_10V4Z C783
1U_0603_10V4Z C782
10U_0805_6.3V6M C770

+1.5V
+V_DDR3_DIMM_REF

JP16
FOX_AS0A626-UARN-7F
ME@

VREF_DQ	1	2	VSS1
VSS2	3	4	DQ4 DDR_B_D4
DQ0 DDR_B_D0	5	6	DQ5 DDR_B_D5
DQ1 DDR_B_D1	7	8	VSS3
VSS4	9	10	DQS#0 DDR_B_DQS#0
DM0 DDR_B_DM0	11	12	DQS0 DDR_B_DQS0
VSS5	13	14	VSS6
DQ2 DDR_B_D2	15	16	DQ6 DDR_B_D6
DQ3 DDR_B_D3	17	18	DQ7 DDR_B_D7
VSS7	19	20	VSS8
DQ8 DDR_B_D8	21	22	DQ12 DDR_B_D12
DQ9 DDR_B_D9	23	24	DQ13 DDR_B_D13
VSS9	25	26	VSS10
DQS#1 DDR_B_DQS#1	27	28	DM1 DDR_B_DM1
DQS1 DDR_B_DQS1	29	30	RESET# SM_DRAMRST# SM_DRAMRST# (8,14)
VSS11	31	32	VSS12
DQ10 DDR_B_D10	33	34	DQ14 DDR_B_D14
DQ11 DDR_B_D11	35	36	DQ15 DDR_B_D15
VSS13	37	38	VSS14
DQ16 DDR_B_D16	39	40	DQ20 DDR_B_D20
DQ17 DDR_B_D17	41	42	DQ21 DDR_B_D21
VSS15	43	44	VSS16
DQS#2 DDR_B_DQS#2	45	46	DM2 DDR_B_DM2
DQS2 DDR_B_DQS2	47	48	VSS17
VSS18	49	50	DQ22 DDR_B_D22
DQ18 DDR_B_D18	51	52	DQ23 DDR_B_D23
DQ19 DDR_B_D19	53	54	VSS19
VSS20	55	56	DQ28 DDR_B_D28
DQ24 DDR_B_D24	57	58	DQ29 DDR_B_D29
DQ25 DDR_B_D25	59	60	VSS21
VSS22	61	62	DQS#3 DDR_B_DQS#3
DM3 DDR_B_DM3	63	64	DQS3 DDR_B_DQS3
VSS23	65	66	VSS24
DQ26 DDR_B_D26	67	68	DQ30 DDR_B_D30
DQ27 DDR_B_D27	69	70	DQ31 DDR_B_D31
VSS25	71	72	VSS26
CKE0 (8) DDR_CKE2_DIMMB DDR_CKE2_DIMMB	73	74	CKE1 DDR_CKE3_DIMMB DDR_CKE3_DIMMB (8)
VDD1	75	76	VDD2
NC1	77	78	A15
BA2 (9) DDR_B_BS#2 DDR_B_BS2	79	80	A14 DDR_B_MA14
VDD3	81	82	VDD4
A12/BC# DDR_B_MA12	83	84	A11 DDR_B_MA11
A9 DDR_B_MA9	85	86	A7 DDR_B_MA7
VDD5	87	88	VDD6
A8 DDR_B_MA8	89	90	A6 DDR_B_MA6
A5 DDR_B_MA5	91	92	A4 DDR_B_MA4
VDD7	93	94	VDD8
A3 DDR_B_MA3	95	96	A2 DDR_B_MA2
A1 DDR_B_MA1	97	98	A0 DDR_B_MA0
VDD9	99	100	VDD10
CK0 (8) M_CLK_DDR2 M_CLK_DDR2	101	102	CK1 M_CLK_DDR3 M_CLK_DDR3 (8)
CK0# (8) M_CLK_DDR#2 M_CLK_DDR#2	103	104	CK1# M_CLK_DDR#3 M_CLK_DDR#3 (8)
VDD11	105	106	VDD12
A10/AP DDR_B_MA10	107	108	BA1 DDR_B_BS1 DDR_B_BS#1 (9)
BA0 (9) DDR_B_BS#0 DDR_B_BS0	109	110	RAS# DDR_B_RAS# DDR_B_RAS# (9)
VDD13	111	112	VDD14
WE# (9) DDR_B_WE# DDR_B_WE#	113	114	S0# DDR_CS2_DIMMB# DDR_CS2_DIMMB# (8)
CAS# (9) DDR_B_CAS# DDR_B_CAS#	115	116	ODT0 M_ODT2 M_ODT2 (8)
VDD15	117	118	VDD16
A13 DDR_B_MA13	119	120	ODT1 M_ODT3 M_ODT3 (8)
S1# (8) DDR_CS3_DIMMB# DDR_CS3_DIMMB#	121	122	NC2
VDD17	123	124	VDD18
NCTEST	125	126	VREF_CA DDR_VREF_CA_DIMMB
VSS27	127	128	VSS28
DQ32 DDR_B_D32	129	130	DQ36 DDR_B_D36
DQ33 DDR_B_D33	131	132	DQ37 DDR_B_D37
VSS29	133	134	VSS30
DQS#4 DDR_B_DQS#4	135	136	DM4 DDR_B_DM4
DQS4 DDR_B_DQS4	137	138	VSS31
VSS32	139	140	DQ38 DDR_B_D38
DQ34 DDR_B_D34	141	142	DQ39 DDR_B_D39
DQ35 DDR_B_D35	143	144	VSS33
VSS34	145	146	DQ44 DDR_B_D44
DQ40 DDR_B_D40	147	148	DQ45 DDR_B_D45
DQ41 DDR_B_D41	149	150	VSS35
VSS36	151	152	DQS#5 DDR_B_DQS#5
DM5 DDR_B_DM5	153	154	DQS5 DDR_B_DQS5
VSS37	155	156	VSS38
DQ42 DDR_B_D42	157	158	DQ46 DDR_B_D46
DQ43 DDR_B_D43	159	160	DQ47 DDR_B_D47
VSS39	161	162	VSS40
DQ48 DDR_B_D48	163	164	DQ52 DDR_B_D52
DQ49 DDR_B_D49	165	166	DQ53 DDR_B_D53
VSS41	167	168	VSS42
DQS#6 DDR_B_DQS#6	169	170	DM6 DDR_B_DM6
DQS6 DDR_B_DQS6	171	172	VSS43
VSS44	173	174	DQ54 DDR_B_D54
DQ50 DDR_B_D50	175	176	DQ55 DDR_B_D55
DQ51 DDR_B_D51	177	178	VSS45
VSS46	179	180	DQ60 DDR_B_D60
DQ56 DDR_B_D56	181	182	DQ61 DDR_B_D61
DQ57 DDR_B_D57	183	184	VSS47
VSS48	185	186	DQS#7 DDR_B_DQS#7
DM7 DDR_B_DM7	187	188	DQS7 DDR_B_DQS7
VSS49	189	190	VSS50
DQ58 DDR_B_D58	191	192	DQ62 DDR_B_D62
DQ59 DDR_B_D59	193	194	DQ63 DDR_B_D63
VSS51	195	196	VSS52
SA0	197	198	EVENT# PM_EXTTS#0 PM_EXTTS#0 (8,14)
VDDSPD	199	200	SDA CLK_SMBDATA CLK_SMBDATA (14,22)
SA1	201	202	SCL CLK_SMBCLK CLK_SMBCLK (14,22)
VTT1	203	204	VTT2 +0.75VS
G1	205	206	G2

R624 DDR_VREF_CA_DIMMB 1 2 0_0402_5%
+V_DDR3_DIMM_REF
C798 2.2U_0603_6.3V4Z
C758 0.1U_0402_16V4Z

+3VS
R630 1 2 10K_0402_5%
R629 1 2 10K_0402_5%
C761 0.1U_0402_16V4Z

same with intel DDR3 CRB connection

DDR3 SO-DIMM B
REVERSE

Security Classification	Compal Secret Data		
Issued Date	2007/09/29	Deciphered Date	2007/09/29

Compal Electronics, Inc.			
Title: DDRIII-SODIMM SLOT2			
Size	Document Number: KIWAX_LA-5082P		Rev: 0.4
Date: Wednesday, March 18, 2009	Sheet 15 of 53		

GPU_VID1	GPU_VID0	VGA_CORE	P-State
0	0	0.9V	10,12
1	1	1.20V	0
0	1	1.09V	8

	Device ID
NB9M-GS	0x06E9
N10M-GE1-S (55nm)	0x6EC

For N10M 40NM

U59A

Part 1 of 5

PCI EXPRESS

GPIO

DACA

DACB

DACC

I2C

TEST

CLK

HDA

NB9M-GS_BGA533

PM@

CRT OUT

EMI

External Spread Spectrum

If External Spread Spectrum not stuff than stuff resistor

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: N10M PCIE,LVDS,GPIO,CLK

Size	Document Number	Rev
B	KIWA5/6 LA-5081P	0.4

Date: Wednesday, March 18, 2009 | Sheet 16 of 53

FBAD[0..63] → FBAD[0..63] (20,21)
FBAA[0..13] → FBAA[0..13] (20,21)
FBBA[2..5] → FBBA[2..5] (21)
FBADQM#[0..7] → FBADQM#[0..7] (20,21)
FBADQS[0..7] → FBADQS[0..7] (20,21)
FBADQS#[0..7] → FBADQS#[0..7] (20,21)

CKEcs0ODT

R131 & R132 Pull-down for initialization
CKE & RESET/ODT

For N10M

U59B — MEMORY INTERFACE — Part 2 of 5 — NB9M-GS_BGA533 PM@

U59C — Part 3 of 5 — NB9M-GS_BGA533 PM@
- NC
- STRAP: STRAP0, STRAP1, STRAP2, STARP_REF_MIOB, STARP_REF_3V3
- GENERAL: BUFRST_N, THERMDN, THERMDP
- SERIAL: ROM_CS_N, ROM_SCLK, ROM_SI, ROM_SO
- LVDS/TMDS: IFPA_TXC, IFPA_TXC_N, IFPA_TXD0, IFPA_TXD0_N, IFPA_TXD1, IFPA_TXD1_N, IFPA_TXD2, IFPA_TXD2_N, IFPA_TXD3, IFPA_TXD3_N, IFPB_TXC, IFPB_TXC_N, IFPB_TXD4, IFPB_TXD4_N, IFPB_TXD5, IFPB_TXD5_N, IFPB_TXD6, IFPB_TXD6_N, IFPB_TXD7, IFPB_TXD7_N, IFPE_L0, IFPE_L0_N, IFPE_L1, IFPE_L1_N, IFPE_L2, IFPE_L2_N, IFPE_L3, IFPE_L3_N, IFPAB_RSET, IFPE_RSET, IFPC_RSET, IFPE_AUX_N, IFPE_AUX, IFPC_AUX_N, IFPC_AUX

R118 10K_0402_5% 40NM@ — FBB_CKE (21)
R119 10K_0402_5% PM@ — FBA_CKE (20,21)
R985 @1K_0402_5%, R986 @1K_0402_5%, R987 1K_0402_5% PM@
R130 10K_0402_5% 40NM@, R129 10K_0402_5%, R128 10K_0402_5%, R55 55NM@ 40NM@
R988 1.3K_0402_1% @, R991 1.3K_0402_1% @
C970 0.01U_0402_16V7K @
R992 60.4_0402_1% PM@
1.27V~0.9V
+1.8VS
+3VS
+1.1VS
+VGASENSE (16,48)
+FB_PLLAVDD
R974 40NM@ 0_0402_5%
R978 0_0402_5%
R975 0_0402_5% 40NM@
R976 0_0402_5% @
R982 40.2K_0402_1% PM@
R983 40.2K_0402_1% PM@
PAD T164, PAD T165, PAD T167
ROM_SCLK (19), ROM_SI (19), ROM_SO (19)
IFPC_AUX, IFPC_AUX_N

for GT21x request

R989 4.7K_0402_5% 40NM_HDMI@
Q42A 2N7002DW-T/R7_SOT363-6 40NM_HDMI@
VGA_HDMI_SCL (16,23)
R993 4.7K_0402_5% 40NM_HDMI@
Q42B 2N7002DW-T/R7_SOT363-6 40NM_HDMI@
VGA_HDMI_SDA (16,23)

5V PULL UP IN CONNECTER SIDE

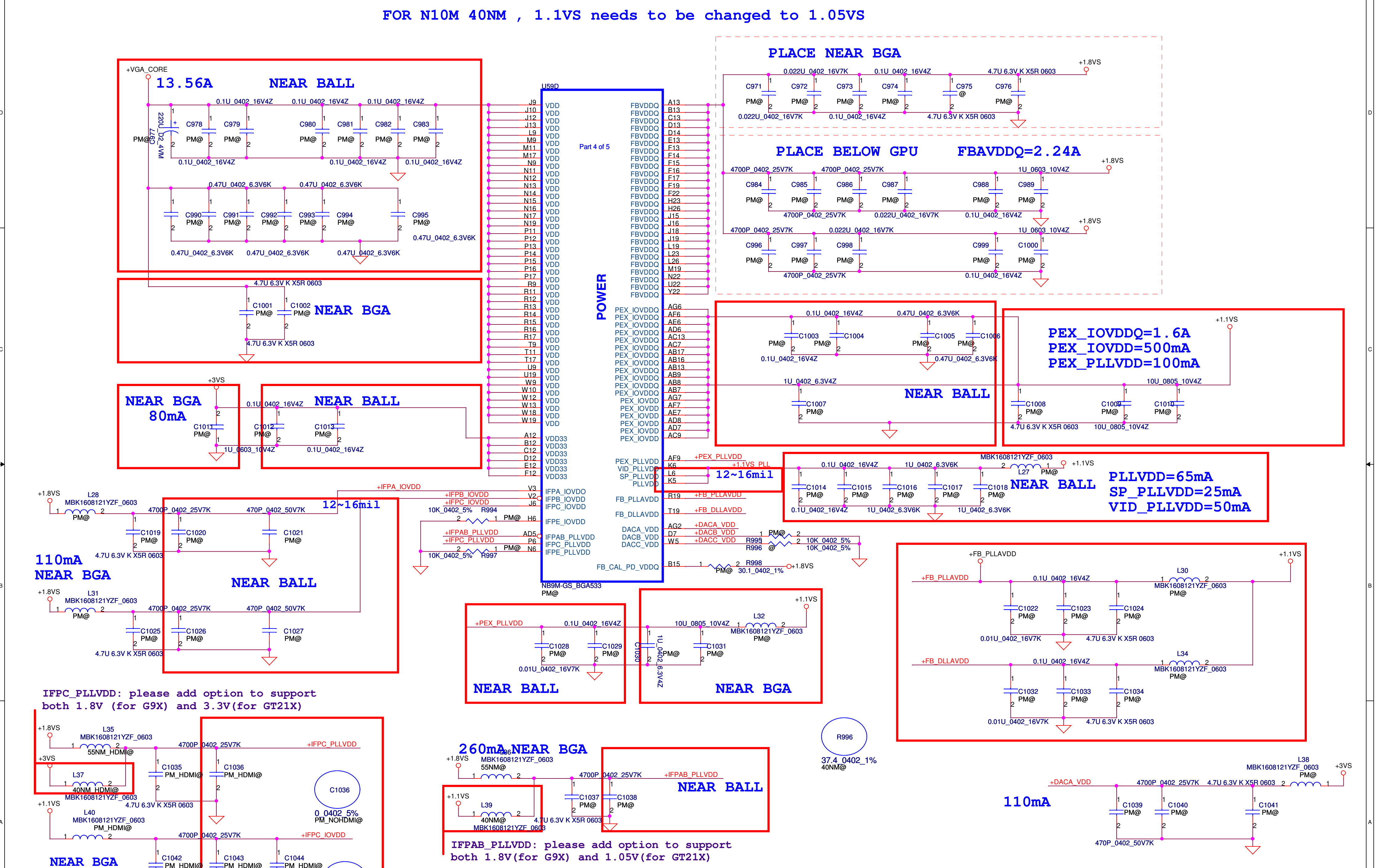
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: N10M Memory

Size	Document Number	Rev
B	KIWA5/6 LA-5081P	0.4

Date: Wednesday, March 18, 2009 Sheet 17 of 53



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

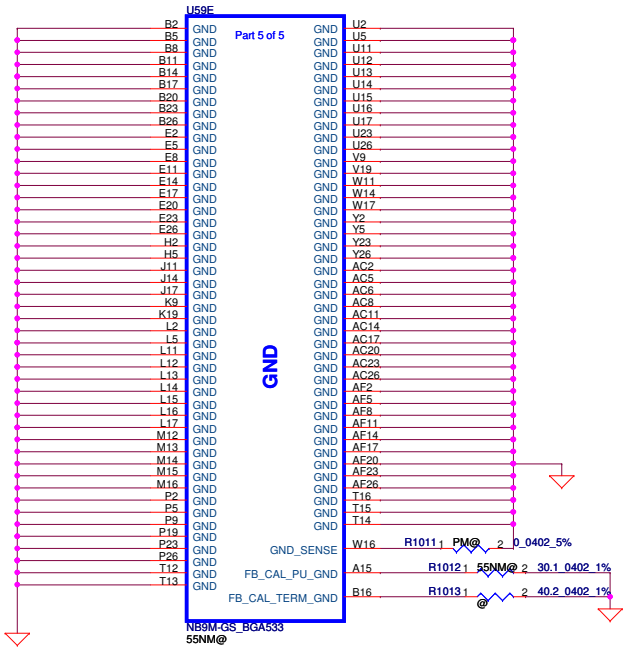
Compal Electronics, Inc.

Title: NB10M Power

Size: Custom | Document Number: KIWA5/6 LA-5081P | Rev: 0.4

Date: Wednesday, March 18, 2009 |

A total of 8 signals are required for GB1 strapping this includes
2 reference signals
6 physical strapping pins
4 logical strapping bits
A total of 24 logical strapping bits are available

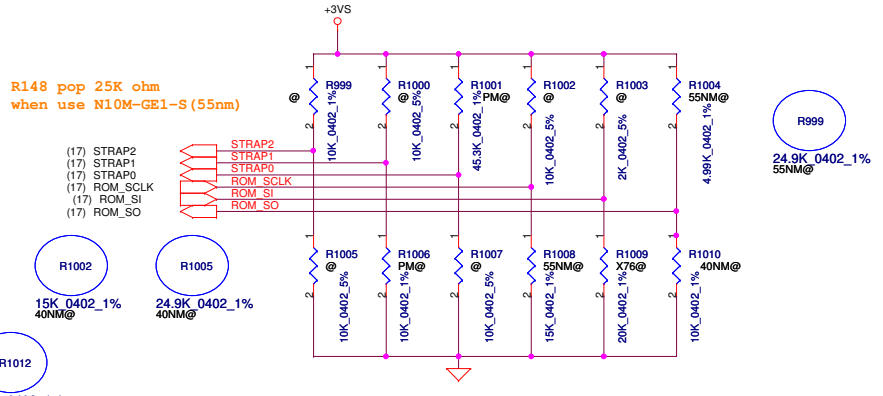


Memory/PKG	FBCAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
DDR2	30.1ohm	30.1ohm	NC
GDDR3	33.2ohm	44.2ohm	40.2ohm

To update for NV PUN-03304-001_V06 (2008/4/01)

U59
NB10M-GS-S
40NM@

R148 pop 25K ohm
when use N10M-GE1-S(55nm)

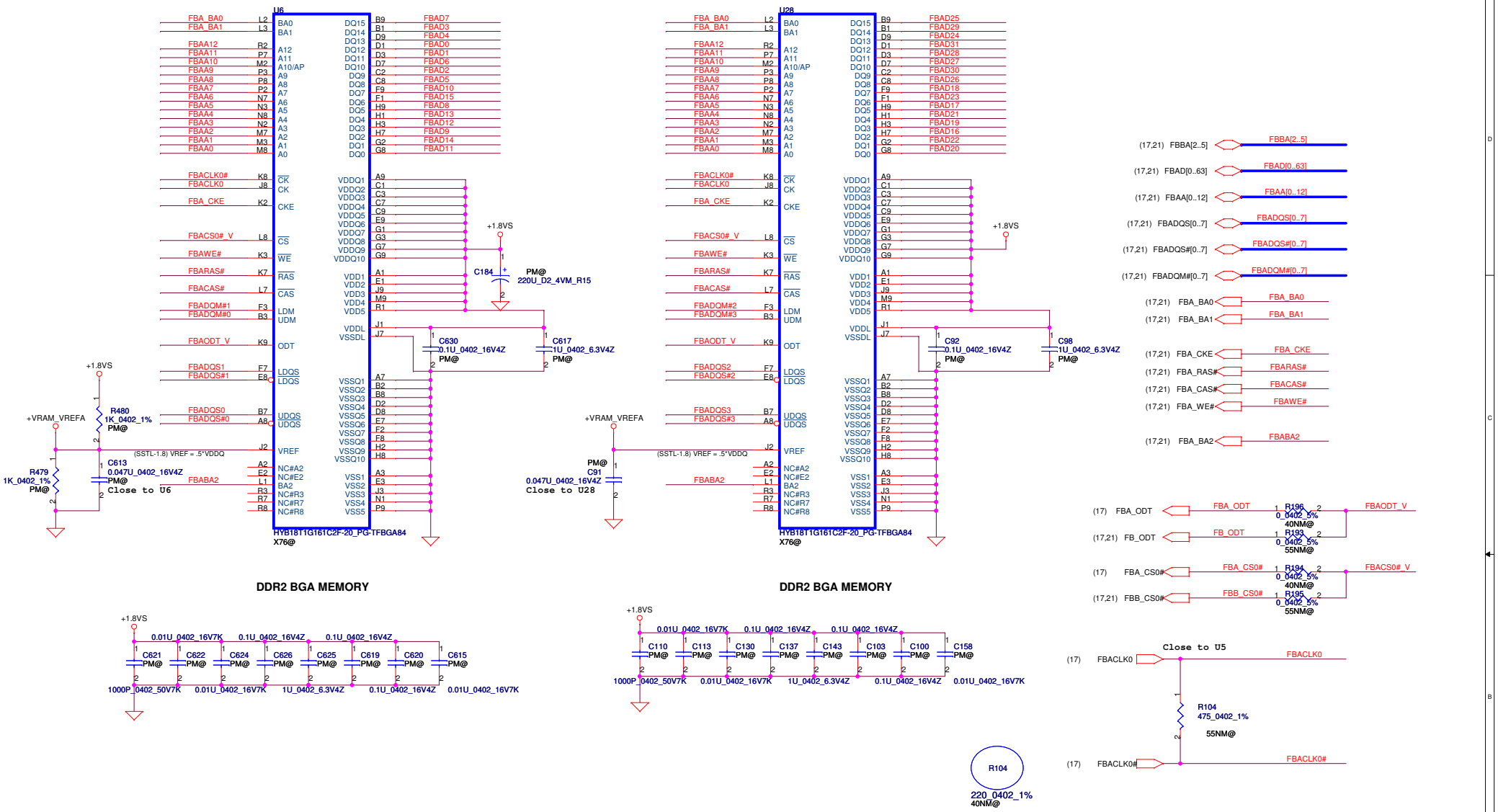


GB1 Family GPU Strap Options X76

GPU	FB Memory (DDR2)		ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N10M-GE1-S (0x6EC) 55nm	Samsung	64Mx16	PU 5K	PD 15K	PD 10K	PU 5K	PD 10K	PU 45K
	Hynix	64Mx16	PU 5K	PD 15K	PD 5K	PU 5K	PD 10K	PU 45K
	Qimonda	64Mx16	PU 5K	PD 15K	PD 15K	PU 5K	PD 10K	PU 45K

GPU	FB Memory (DDR2)		ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N10M-GS (0x6EC) 40nm	Samsung	64Mx16	PD 10K	PD 15K	PD 10K	PU 10K	PD 10K	PU 45K
	Hynix	64Mx16	PD 10K	PD 15K	PD 5K	PU 10K	PD 10K	PU 45K
	Qimonda	64Mx16	PD 10K	PD 15K	PD 15K	PU 10K	PD 10K	PU 45K

Compal Electronics, Inc.
Title: N10M GND & STRAP
Size: B | Document Number: KIWA5/6 LA-5081P | Rev: 0.4
Date: Thursday, March 19, 2009 | Sheet 19 of 53



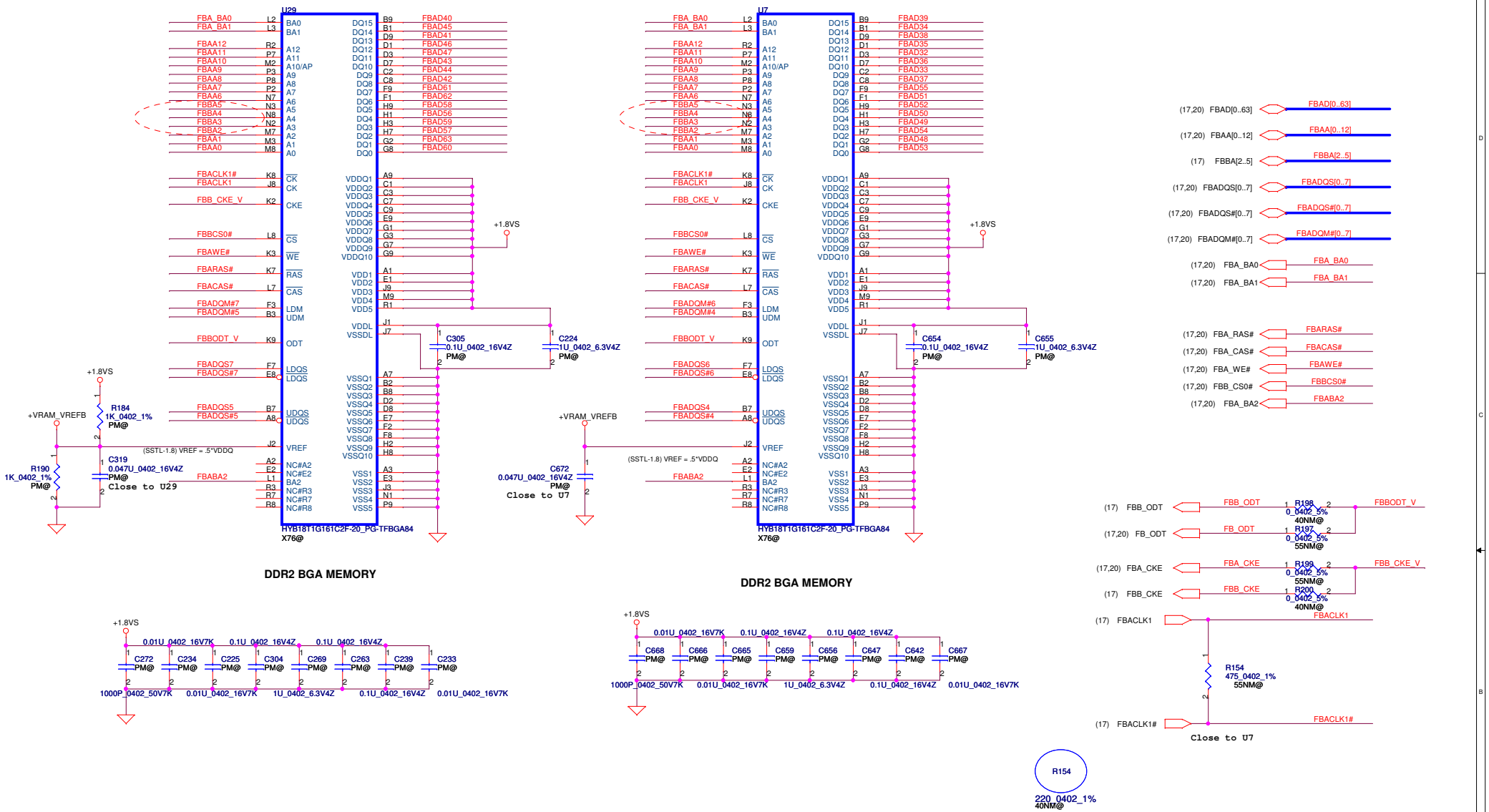
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: VRAM DDRA

Size	Document Number	Rev
Custom	KIWA5/6 LA-5081P	0.4

Date: Wednesday, March 18, 2009 Sheet 20 of 53



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **VRAM DDRB**

Size	Document Number	Rev
Custom	KIWA5/6 LA-5081P	0.4

Date: Wednesday, March 18, 2009 | Sheet 21 of 53

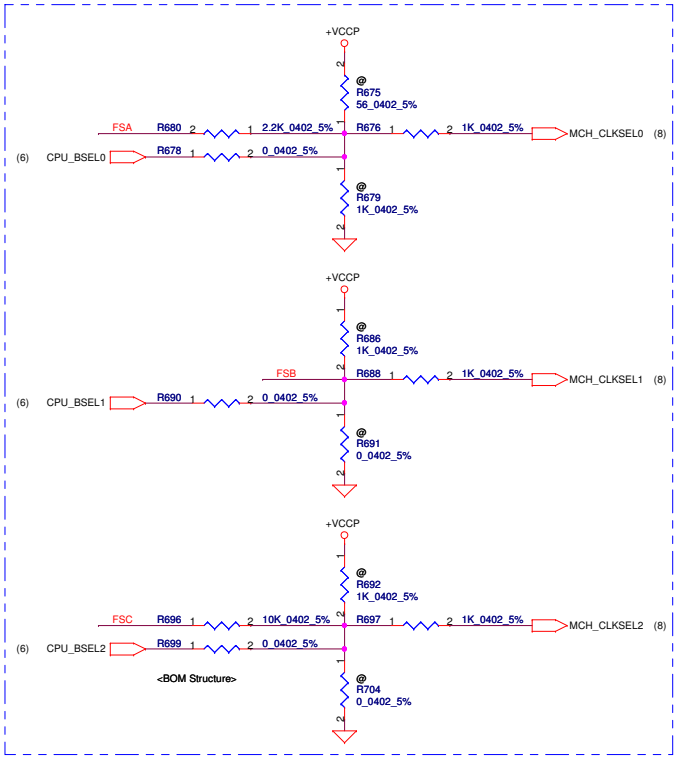
FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					

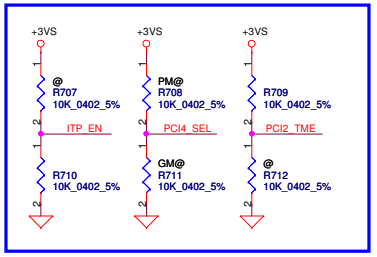
SA000020K00 (Silego : SLG8SP556VTR)

SA000020H00 (ICS : ICS9LPRS387AKLFT)

<BOM Structure>

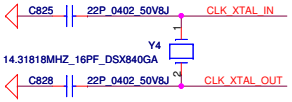
<BOM Structure>



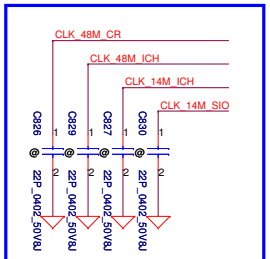


For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#

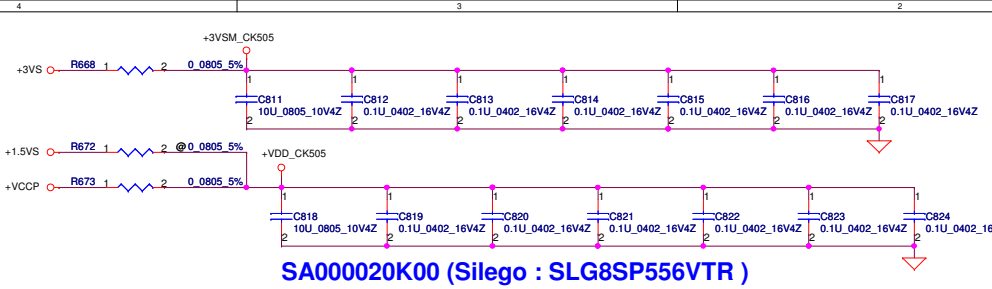
For PCI4_SEL, 0 = Pin24/25 : DOT96 / DOT96#
Pin28/29 : LCDCLK / LCDCLK#
1 = Pin24/25 : SRC_0 / SRC_0#
Pin28/29 : 27M/27M_SS

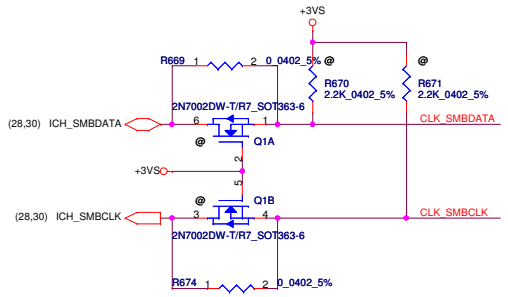


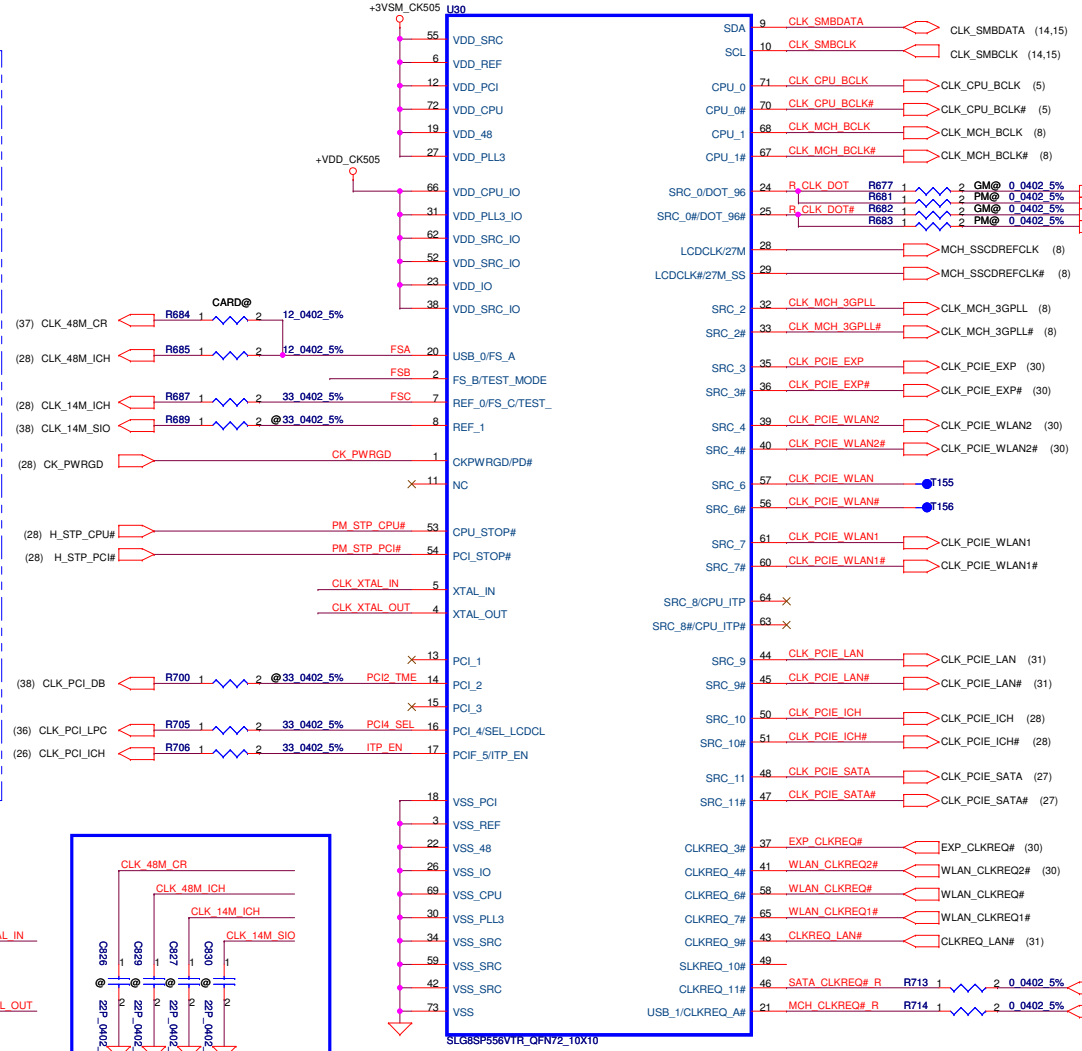
Routing the trace at least 10mil



place CAPs near Resistors of U10
For 3G RF noise .

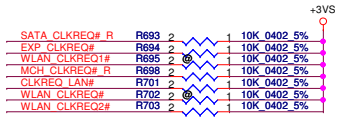






SRC PORT LIST

PORT	DEVICE
SRC0	MCH_DREFCLK
SRC2	MCH_3GPLL
SRC3	PCIE_EXP#
SRC4	
SRC6	PCIE_WLAN
SRC7	PCIE_WLAN1
SRC8	
SRC9	PCIE_LAN
SRC10	PCIE_ICH
SRC11	PCIE_SATA



REQ PORT LIST

PORT	DEVICE
REQ_3#	PCIE_EXP#
REQ_4#	PCIE_WLAN2
REQ_6#	PCIE_WLAN
REQ_7#	PCIE_WLAN1
REQ_9#	PCIE_LAN
REQ_10#	
REQ_11#	PCIE_SATA
REQ_A#	MCH_3GPLL

Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

Compal Electronics, Inc.

Title: Clock Generator CK505

Size: Custom | Document Number: KIWA5/6 LA-5081P | Rev: 0.4

Date: Wednesday, March 18, 2009 | Sheet 22 of 53

10/30 update PS8171 co-lay circuit

P/N:SA00002D700 (8101T)
P/N:SA00001U920 (CH7318C)

For 8171

PIN NUM	8101T	8171
PIN1	GND	ASQ0
PIN3	PC0	PEQ
PIN4	PC1	PIO
PIN7	HPD#	HPDX
PIN10	RE_EN#	CEXT
PIN11	VCC	ASQ1
PIN12	GND	APD
PIN27	GND	EMI0
PIN33	VCC	EMI1
PIN34	DDCBUF_EN	DDCBUF
PIN35	CFG	PRE

For 8171 net name:
EMI0, EMI1
ASQ0, ASQ1
APD

TMDS pull down (500ohm) resistors for ATI M92-S2 XT

NEAR CONNECTOR

U31 PS8101TQFN48G_QFN48_7X7 GM_HDMI@

Reserved for CH7318C

1.2k for CH7318C

place those component near JP? for NV request 0515

KIWB3/B4_LA4551P

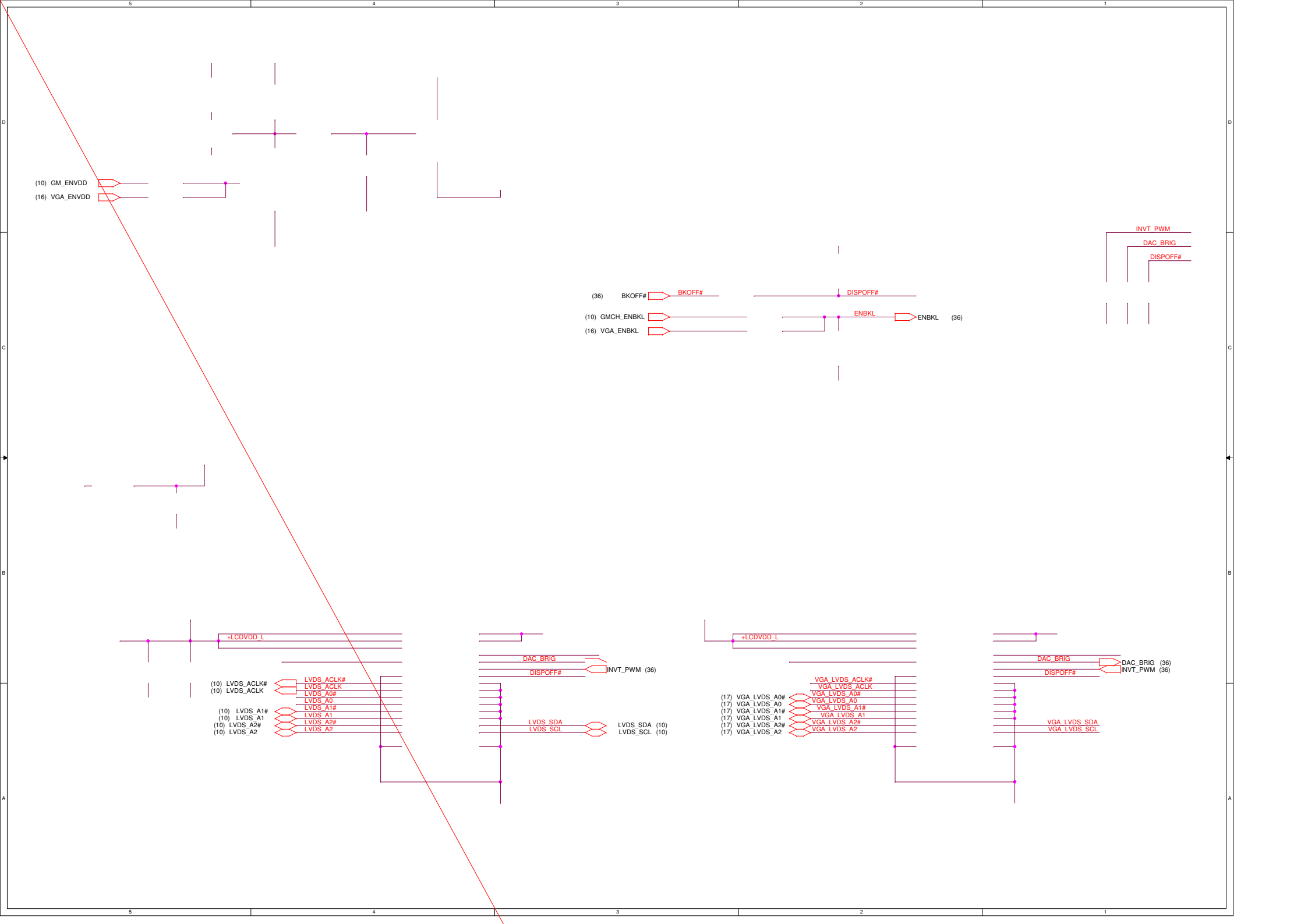
Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

Compal Electronics, Inc.

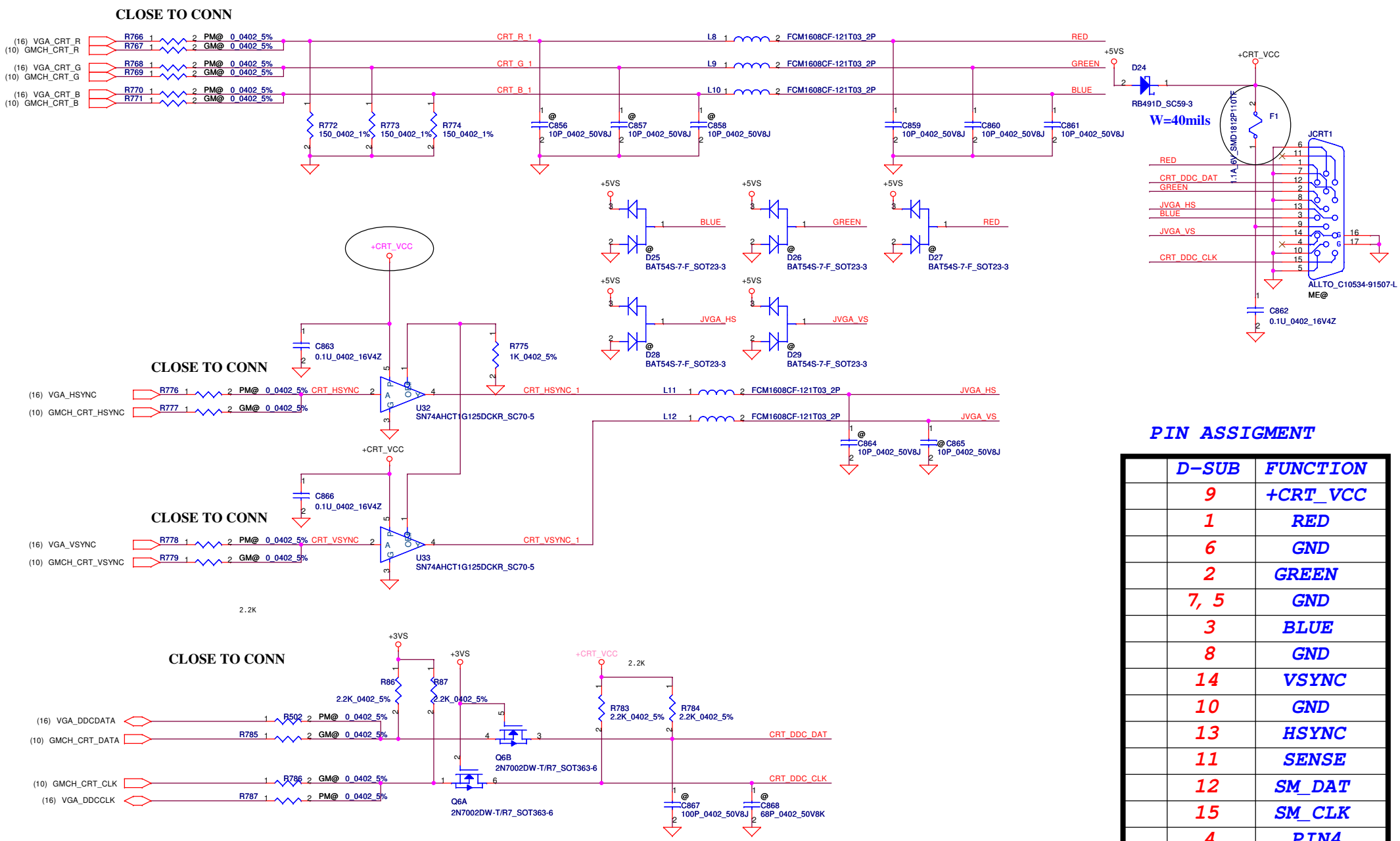
Title: **Level Shiftter_PS8101T**

Size	Document Number	Rev
Custom	KIWAX_LA-5082P	0.4

Date: Wednesday, March 18, 2009 | Sheet 23 of 53


(10) GM_ENVDD
(16) VGA_ENVDD
(36) BKOFF#
BKOFF#
DISPOFF#
(10) GMCH_ENBKL
(16) VGA_ENBKL
ENBKL
ENBKL (36)
INVT_PWM
DAC_BRIG
DISPOFF#
+LCDVDD_L
(10) LVDS_ACLK#
(10) LVDS_ACLK
(10) LVDS_A1#
(10) LVDS_A1
(10) LVDS_A2#
(10) LVDS_A2
LVDS_ACLK#
LVDS_ACLK
LVDS_A0#
LVDS_A0
LVDS_A1#
LVDS_A1
LVDS_A2#
LVDS_A2
DAC_BRIG
DISPOFF#
INVT_PWM (36)
LVDS_SDA
LVDS_SCL
LVDS_SDA (10)
LVDS_SCL (10)
+LCDVDD_L
(17) VGA_LVDS_A0#
(17) VGA_LVDS_A0
(17) VGA_LVDS_A1#
(17) VGA_LVDS_A1
(17) VGA_LVDS_A2#
(17) VGA_LVDS_A2
VGA_LVDS_ACLK#
VGA_LVDS_ACLK
VGA_LVDS_A0#
VGA_LVDS_A0
VGA_LVDS_A1#
VGA_LVDS_A1
VGA_LVDS_A2#
VGA_LVDS_A2
DAC_BRIG
DISPOFF#
DAC_BRIG (36)
INVT_PWM (36)
VGA_LVDS_SDA
VGA_LVDS_SCL

CRT Connector



PIN ASSIGMENT

	D-SUB	FUNCTION
	9	+CRT_VCC
	1	RED
	6	GND
	2	GREEN
	7, 5	GND
	3	BLUE
	8	GND
	14	VSYNC
	10	GND
	13	HSYNC
	11	SENSE
	12	SM_DAT
	15	SM_CLK
	4	PIN4

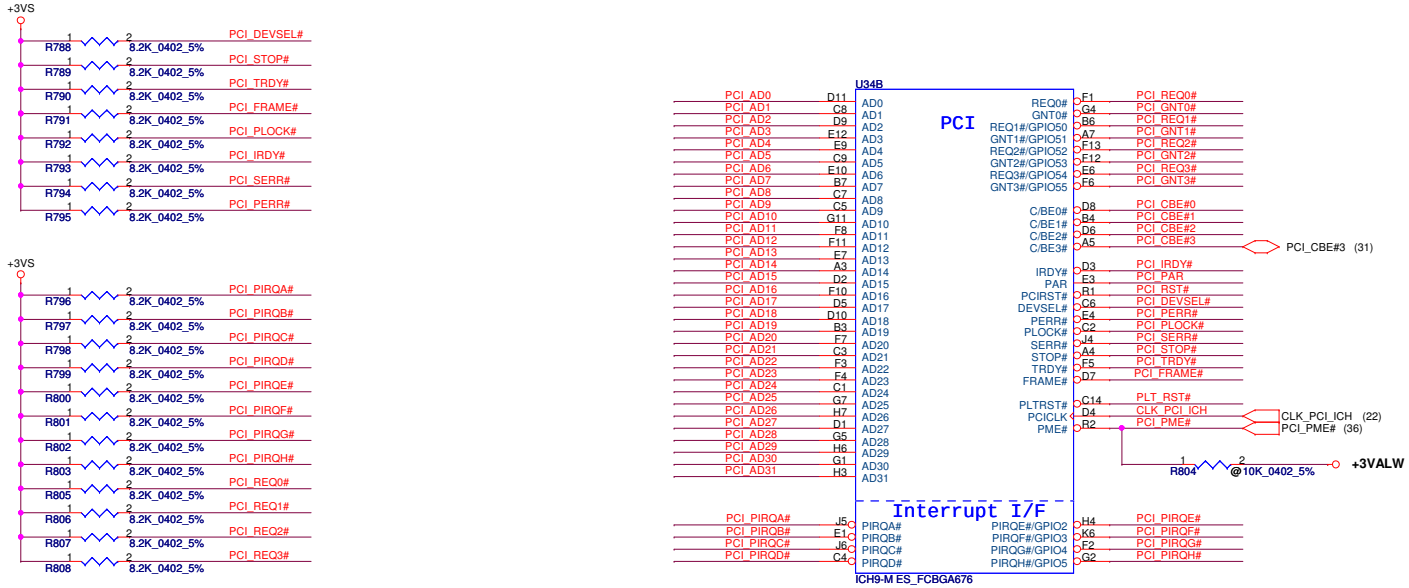
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: CRT & TV-OUT Connector

Size: Custom | Document Number: KIWA5/6 LA-5081P | Rev: 0.4

Date: Wednesday, March 18, 2009 | Sheet 25 of 53

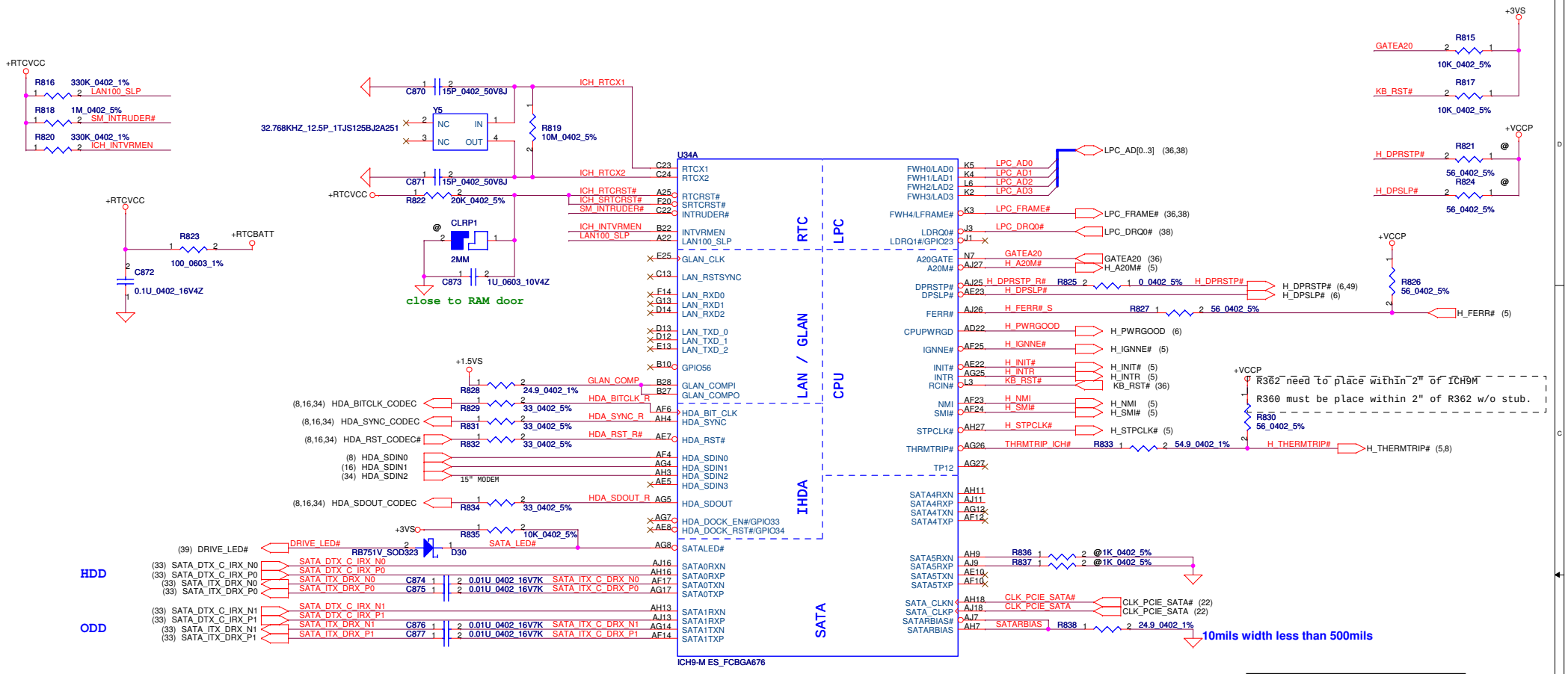


A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Loaction
0	1	SPI
1	0	PCI
1	1	LPC*

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.	
Title	ICH9M(1/4)-PCI
Size	Document Number: KIWA5/6 LA-5081P
Rev	0.4
Date: Wednesday, March 18, 2009	Sheet 26 of 53



SATA PORT LIST	
PORT	DEVICE
0	HDD
1	ODD
4	E-SATA
5	

XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIE port config bit 1

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

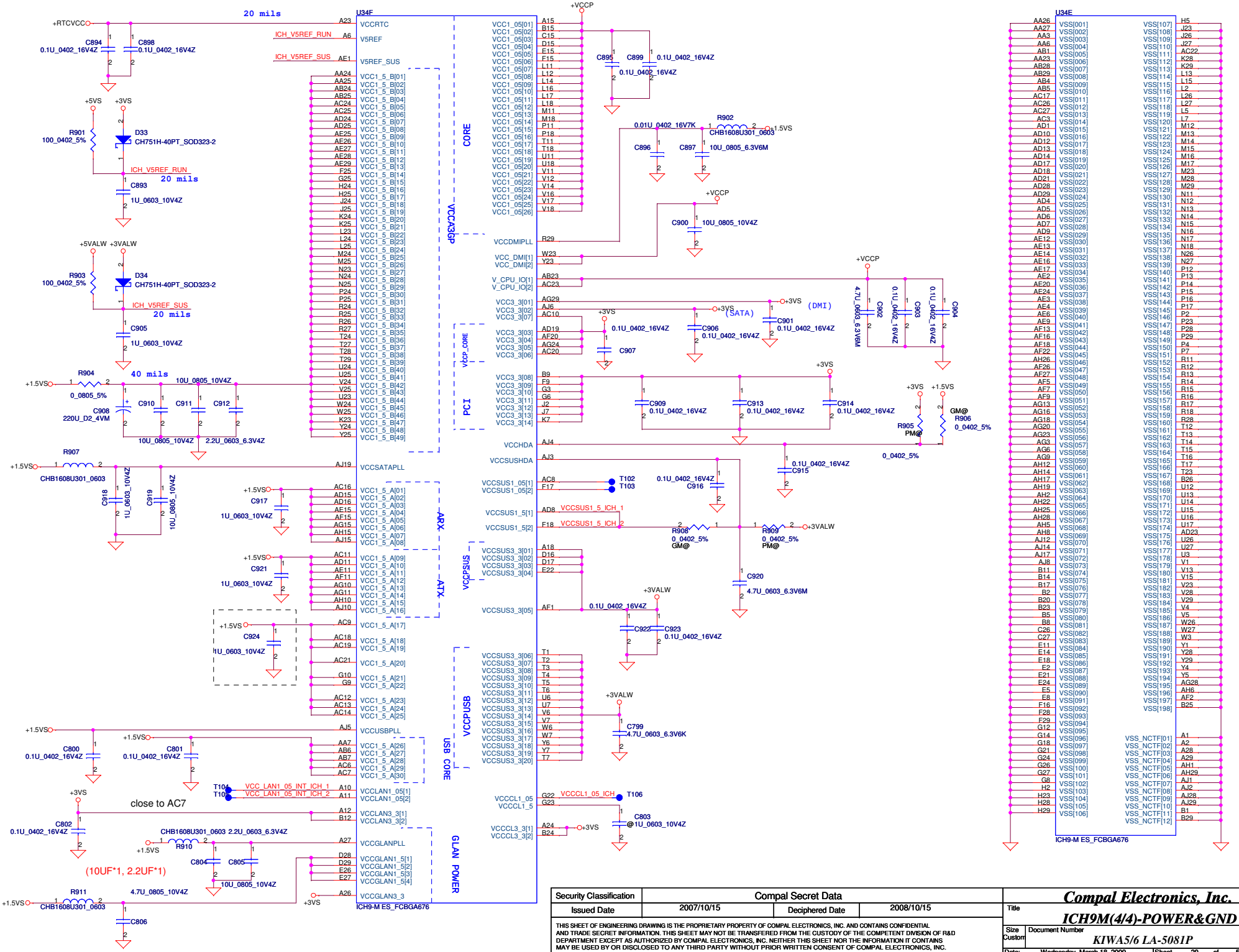
Compal Electronics, Inc.

Title: ICH9M(2/4)-LAN,IDELPC,RTC

Size: Custom | Document Number: KIWA5/6 LA-5081P | Rev: 0.4

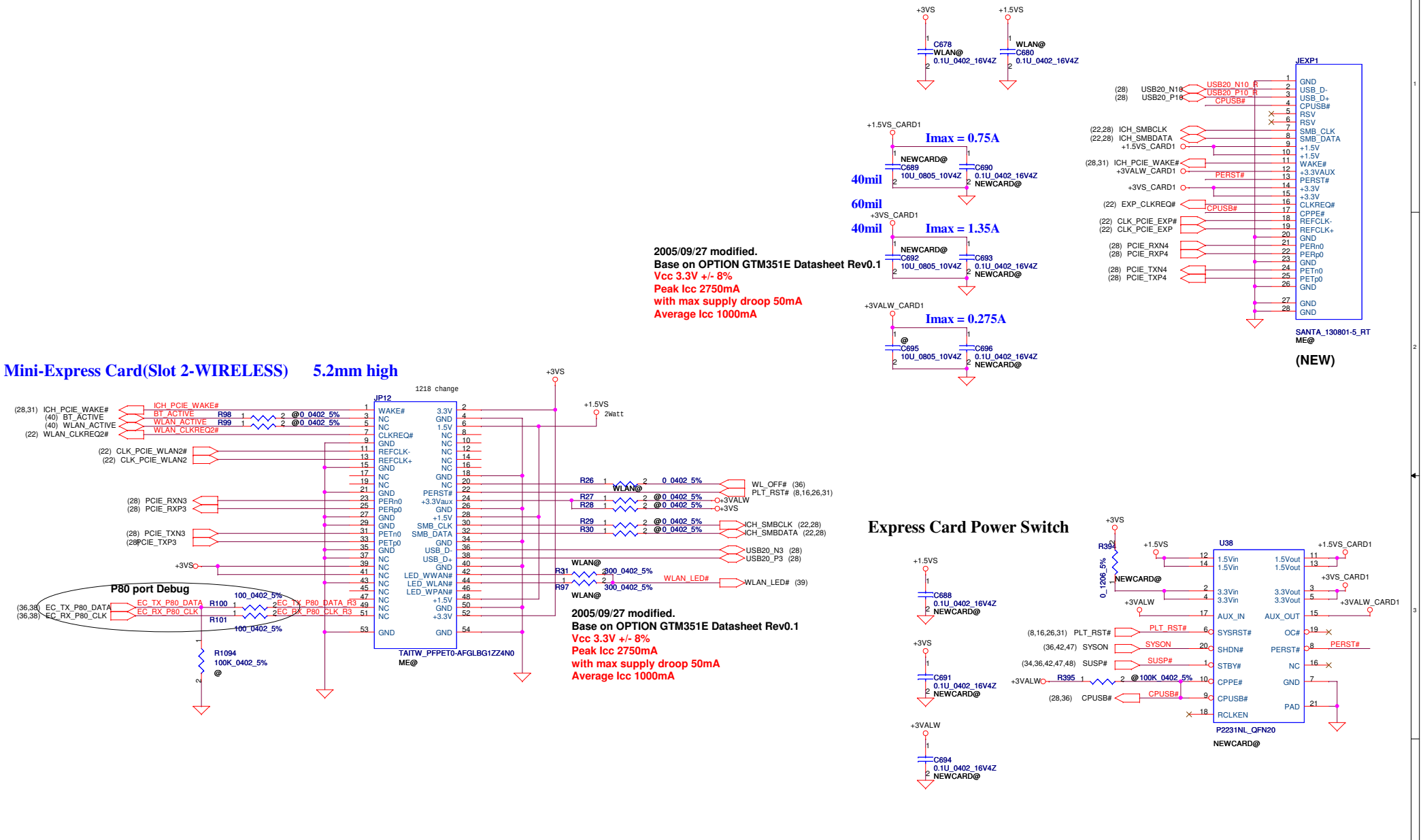
Date: Wednesday, March 18, 2009 | Sheet 27 of 53


SERIRQ
PCI_CLKRUN#
GPIO38
EC_THERM#
OCP#
PM_BMBUSY#
GPIO39
GPIO48
LINKALERT#
CL_RST#
XDP_DBRESET#
ICH_RI#
ICH_PCIE_WAKE#
ICH_LOW_BAT#
LID_OUT#
GPIO7
GPIO13
GPIO17
GPIO20
GPIO22
SB_SPKR
GPIO57
DPRSLPVR
ICH_RSVD
LINKALERT#
ME_EC_CLK1
ME_EC_DATA1
ICH_RI#
XDP_DBRESET#
PM_BMBUSY#
LID_OUT#
H_STP_PCI#
R_STP_CPU#
PCI_CLKRUN#
ICH_PCIE_WAKE#
SERIRQ
EC_THERM#
VRMPWRGD
SST_CTL
OCP#
GPIO7
EC_SMI#
EC_SCI#
GPIO13
GPIO17
GPIO18
GPIO20
GPIO22
GPIO27
GPIO38
GPIO39
GPIO48
GPIO49
GPIO57
SB_SPKR
MCH_ICH_SYNC#
ICH_RSVD
CLK_48M_ICH
CLK_14M_ICH
CLK_14M_ICH
CLK_48M_ICH
ICH_SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
S4_STATE#
ICH_POK
M_PWROK
M_PWROK
DPRSLPVR
ICH_LOW_BAT#
PBTN_OUT#
EC_RSMRST#R
EC_RSMRST#R
CK_PWRGD_R
CK_PWRGD
M_PWROK
CL_VREF1_ICH
CL_RST#
ACIN
GPIO14
WOL_EN



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.			
Title: ICH9M(4/4)-POWER&GND			
Size: Custom	Document Number: KIWA5/6 LA-5081P		Rev: 0.4
Date: Wednesday, March 18, 2009	Sheet 29 of 53		



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.			
Title	Mini-Card/3G/TV /BT		
Size	Document Number	KIWAX_LA-5082P	Rev 0.4
Date: Wednesday, March 18, 2009	Sheet 30 of 53		

Layout Notice : Filter place as close chip as possible.

Layout Notice : Place as close chip as possible.

Layout Notice : 1.2V filter. Place as close chip as possible.

(CLKREQ#) and (ENERGY_DET) are only supported in BCM5787M

Notice : 4.7u 6.3V capactor Thickness 1.25mm

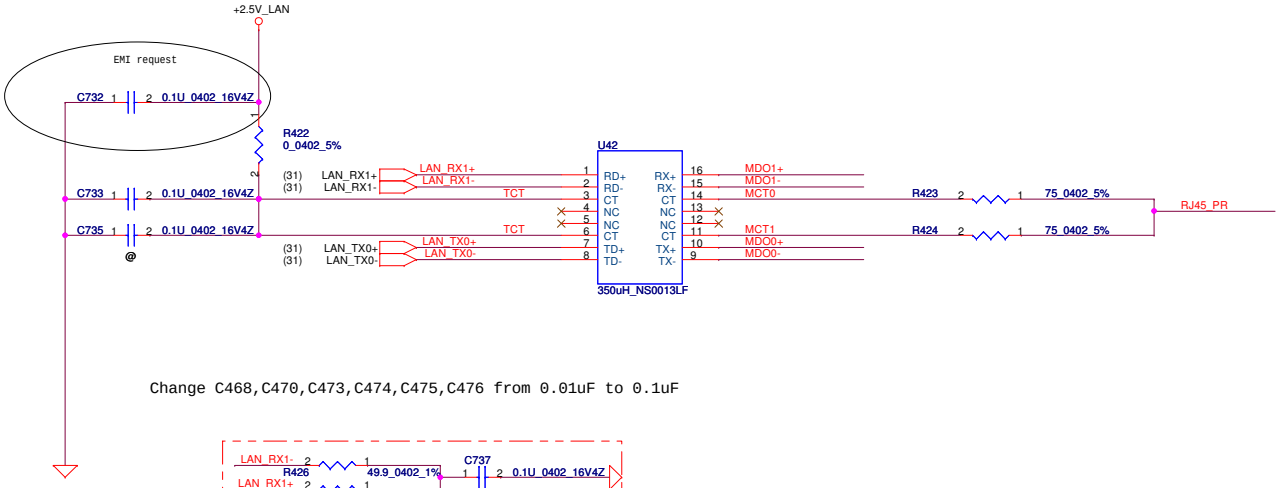
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

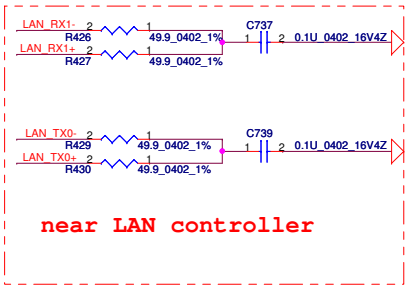
Title: BCM5787MKML

Size: Custom | Document Number: KIWA5/6 LA-5081P | Rev: 0.4

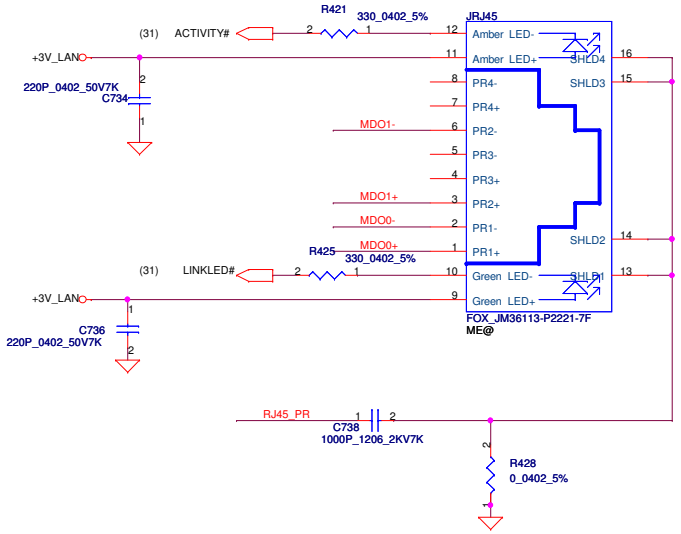
Date: Wednesday, March 18, 2009 | Sheet 31 of 53



Change C468,C470,C473,C474,C475,C476 from 0.01uF to 0.1uF



RJ45 CONN



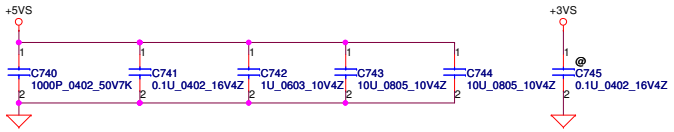
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

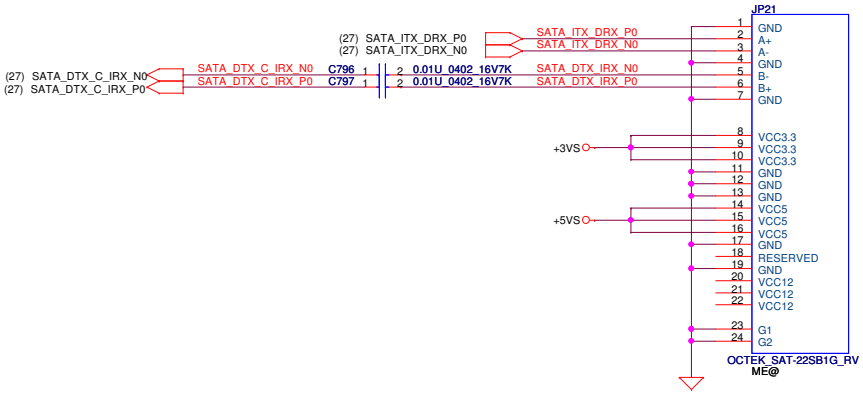
Title: LAN CONTROLLER

Size	Document Number	Rev
Custom	KIWA5/6 LA-5081P	0.4

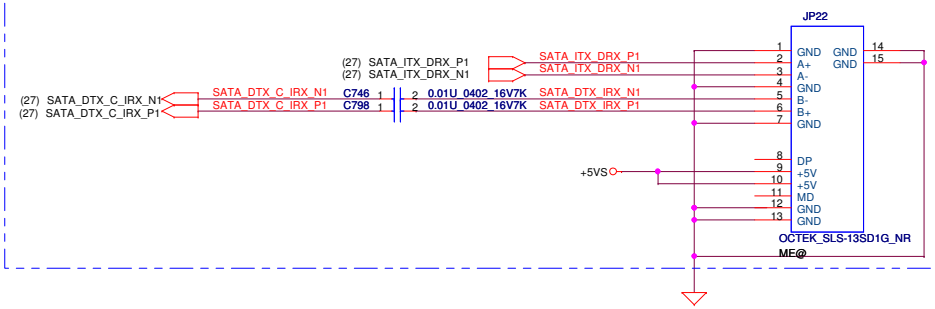
Date: Wednesday, March 18, 2009 | Sheet 32 of 53



SATA HDD Conn.



SATA ODD Conn.



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **HDD & ODD Connector**

Size	Document Number	Rev
B	KIWA5/6 LA-5081P	0.4

Date: Wednesday, March 18, 2009 | Sheet 33 of 53

AUDIO CODEC

0308_Change R294 and R295 from 0 ohm to bead, C363 from 10uF to 680pF, C365 and C368 from 0.1uF to 680p

In order for the modem wake on ring feature to function, the CODEC must be powered by a rail that is not removed when the system is in standby.

For Layout:
Place decoupling caps near the power pins of SmartAMC device.

CX20548
AMOM DAA

11/20 update
PC_BEEP dB control

0216_Change value.

CODEC POWER

(3.33V)
250mW

W=40Mil

2.2kohm for MICL + MICR
4.7kohm for MICL or MICR

external MIC
Internal MIC / Array MIC
Internal WOOFER
Internal SPKR.

11/20 update

port A : 5.11K ohm
port B : 10.0K ohm
port C : 20.0K ohm
port D : 39.2K ohm

DIGITAL ANALOG

Place these C and R around AGND and DGND, then choose the one which is close to Codec to populate

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

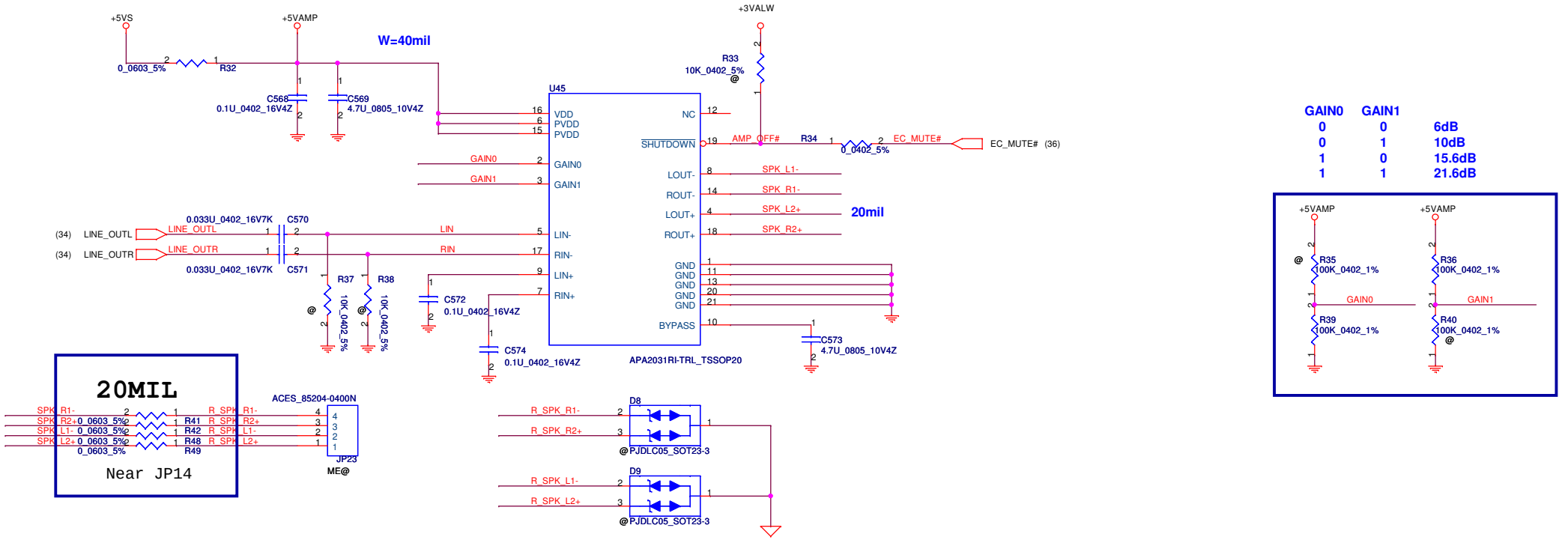
Compal Electronics, Inc.

Title: CX20561-AMOM Codec

Size: Custom | Document Number: KIWA5/6 LA-5081P | Rev: 0.4

Date: Wednesday, March 18, 2009 | Sheet 34 of 53

Speaker Connector

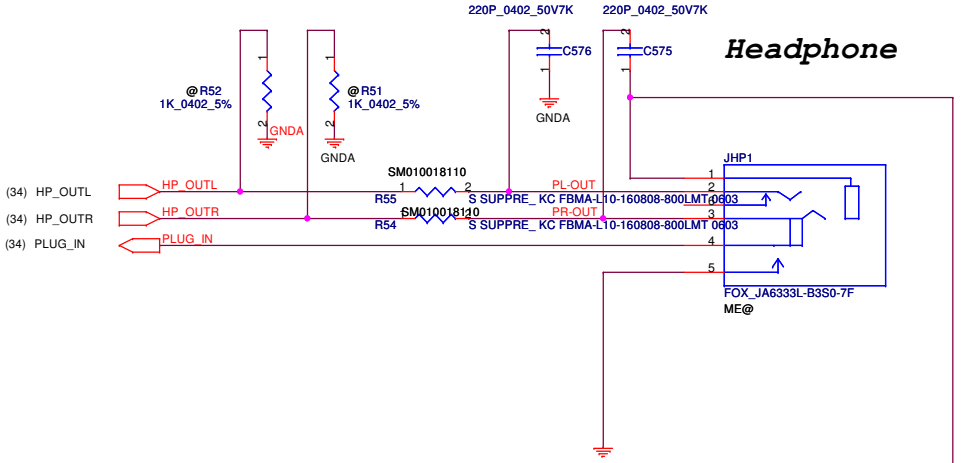


GAIN0	GAIN1	
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

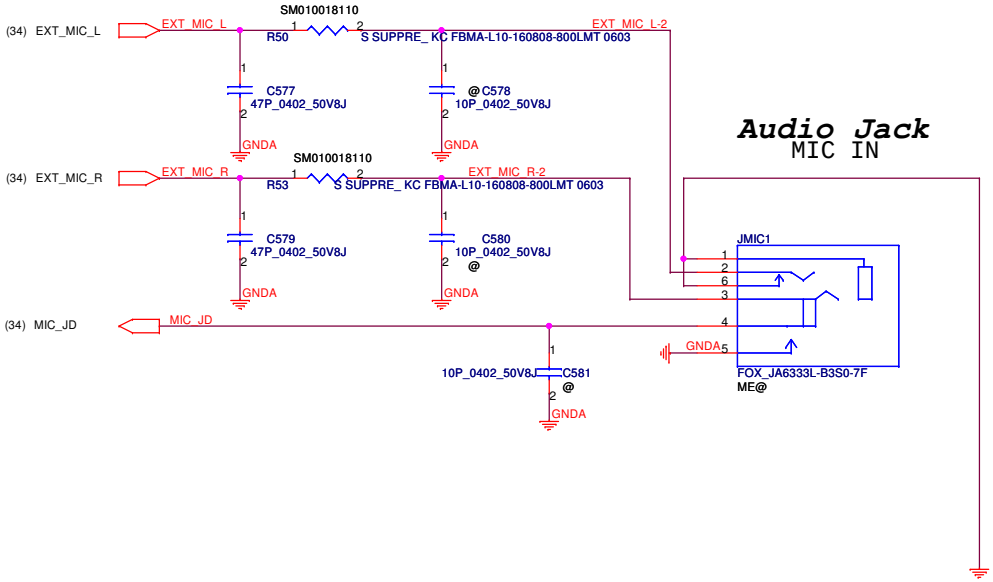
20MIL

Near JP14

Headphone



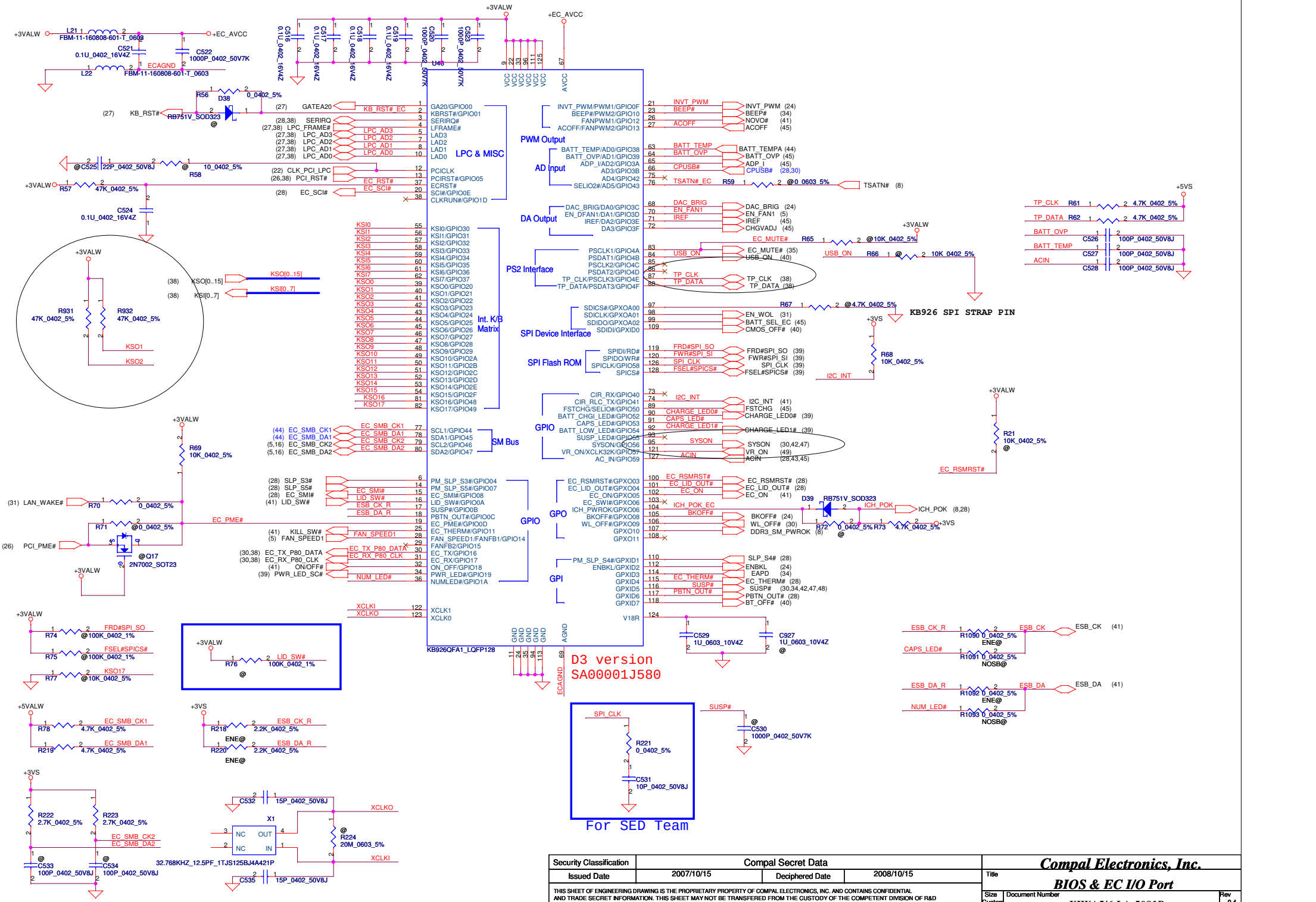
Audio Jack



Audio Jack
MIC IN

Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

Compal Electronics, Inc.			
Title: AMP,Audio speaker CONN			
Size: Custom	Document Number: KIWA5/6 LA-5081P		Rev: 0.4
Date: Wednesday, March 18, 2009	Sheet 35 of 53		



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

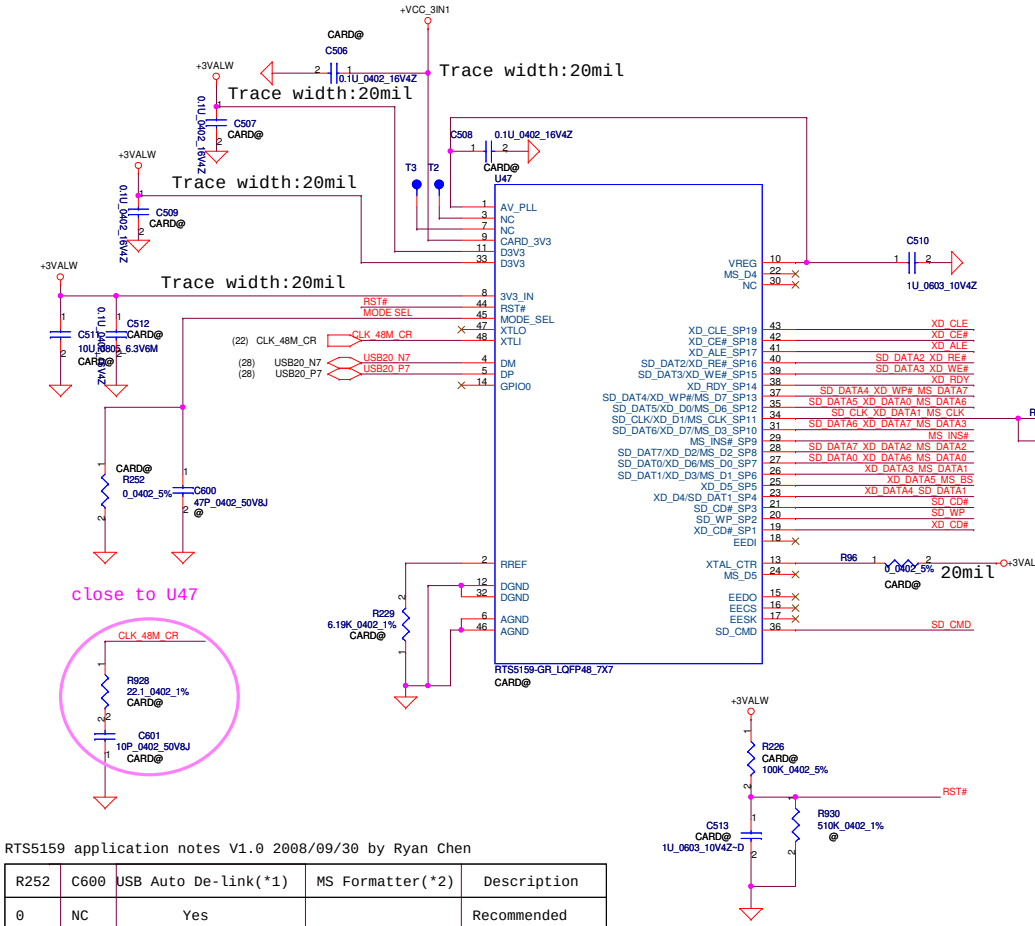
Compal Electronics, Inc.

Title: **BIOS & EC I/O Port**

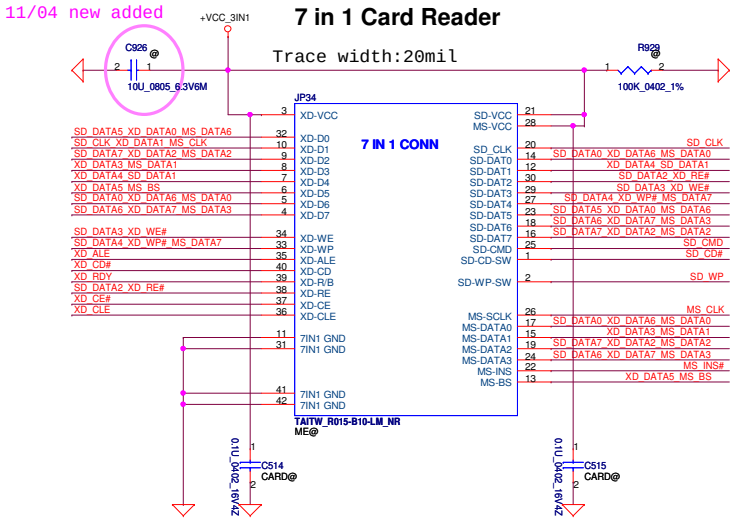
Size	Document Number	Rev
Custom	KIWA5/6 LA-5081P	0.4

Date: Wednesday, March 18, 2009 | Sheet 36 of 53

Card reader(XD/SD/MMC/MS/MS-Pro HD SD)



11/04 new added



RTS5159 application notes V1.0 2008/09/30 by Ryan Chen

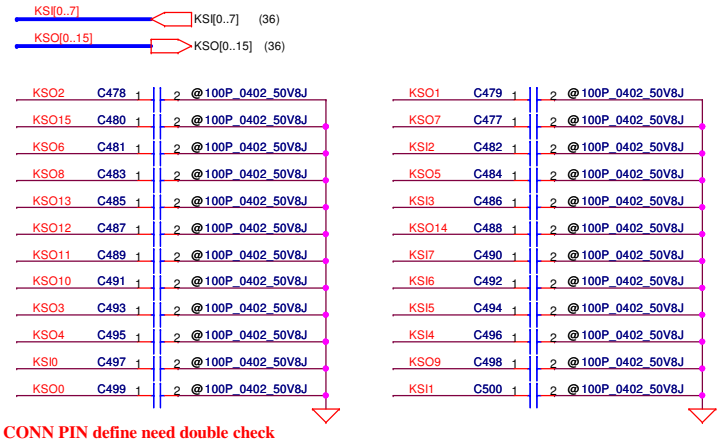
R252	C600	USB Auto De-link(*1)	MS Formatter(*2)	Description
0	NC	Yes		Recommended
NC	47pF	Yes	Yes	
NC	NC			Compatible with RTS5158E
NC	680pF	Yes		LED ON (*3)
10K	180pF			LED ON (*3)
10K	680pF		Yes	

Security Classification	Compal Secret Data		
Issued Date	2008/06/10	Deciphered Date	2008/12/31

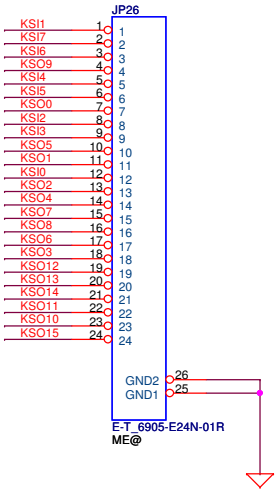
Compal Electronics, Inc.			
Title: USB_CR board			
Size: Custom	Document Number: KIWAX_LA-5082P		Rev: 0.4
Date: Wednesday, March 18, 2009	Sheet 37 of 53		

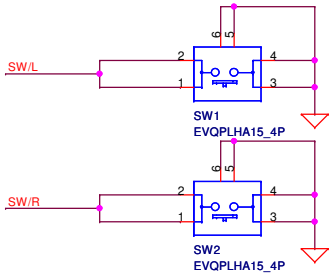
Source:SP01000IE00
2nd source:SP01000IF00
30 pin

INT_KBD Conn.

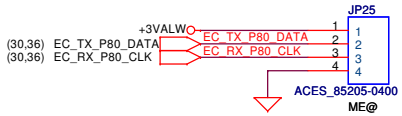


CONN PIN define need double check

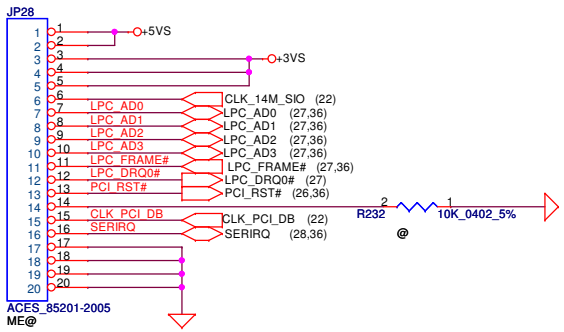


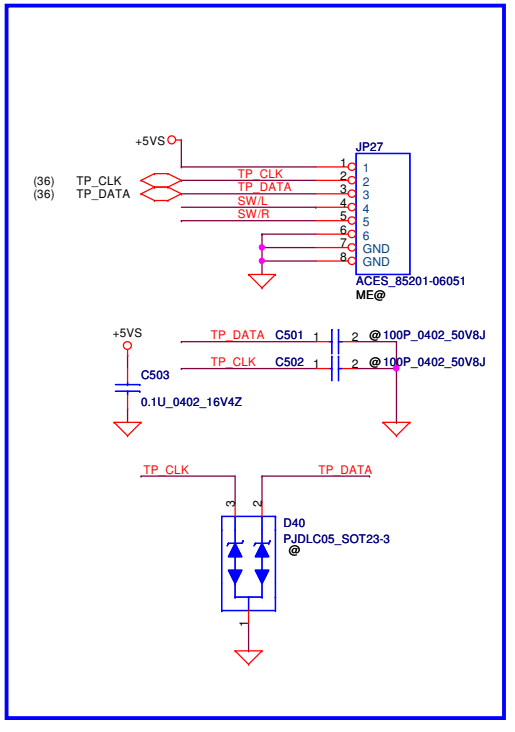


EC DEBUG PORT



FOR LPC SIO DEBUG PORT

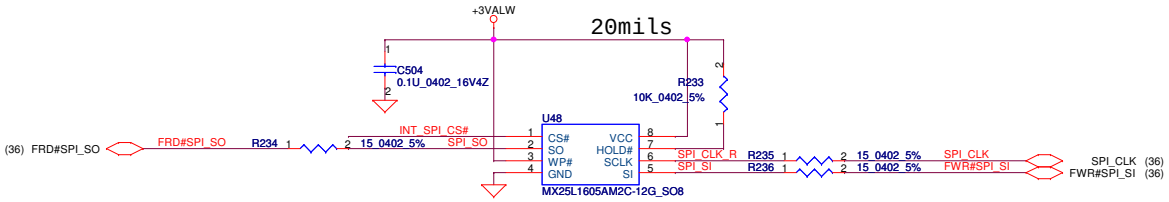


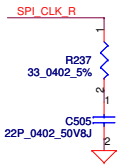


Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.			
Title: KB /SW /LPC Debug Conn.			
Size: B	Document Number: KIWA5/6 LA-5081P		Rev: 0.4
Date: Wednesday, March 18, 2009	Sheet 38 of 53		

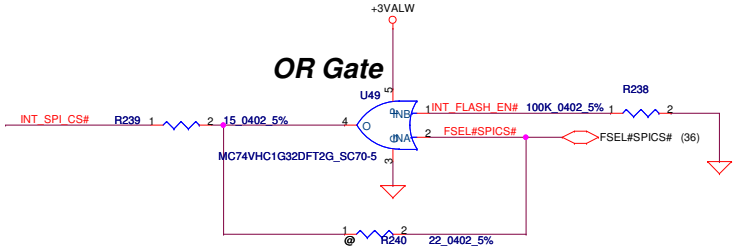
FOR EC 16M SPI ROM

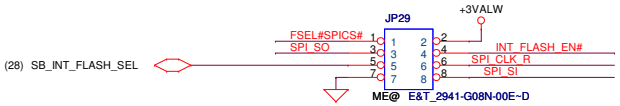




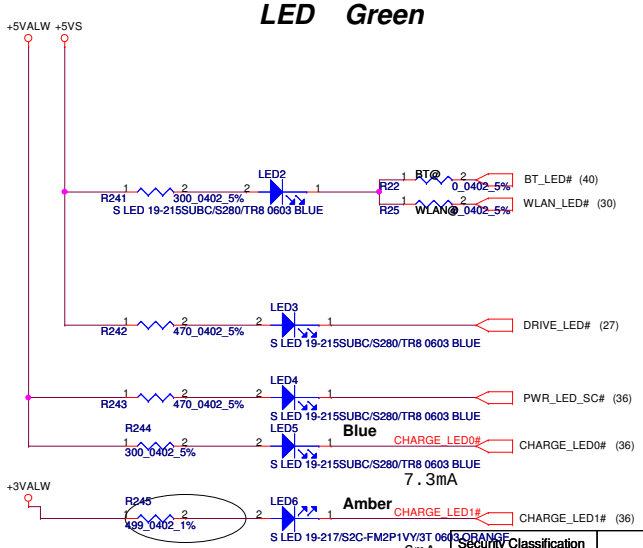
INPUT		OUTPUT
A	B	Y
L	L	L
H	L	H
L	H	H
H	H	H

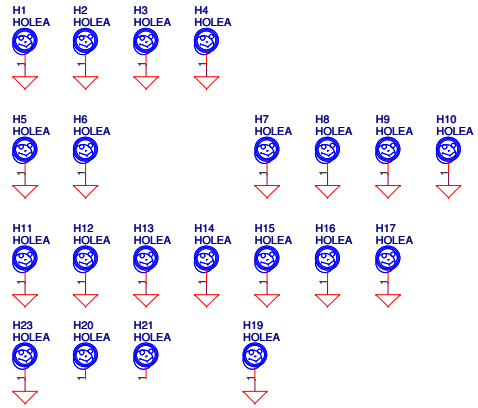
OR Gate





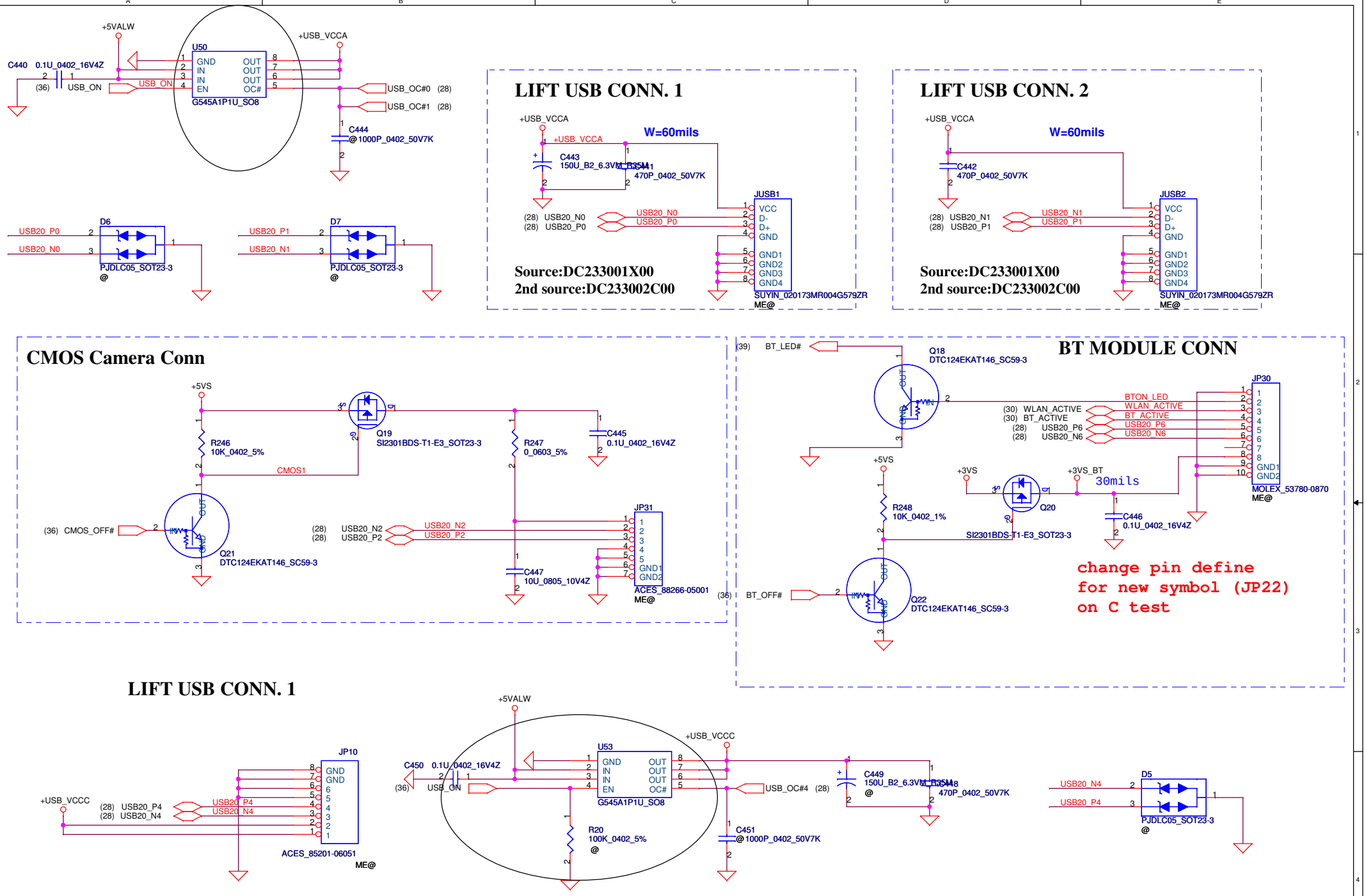
LED Green





Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.			
Title	LED/EC SPI ROM		
Size B	Document Number KIWA5/6 LA-5081P		Rev 0.4
Date: Wednesday, March 18, 2009	Sheet 39 of 53		



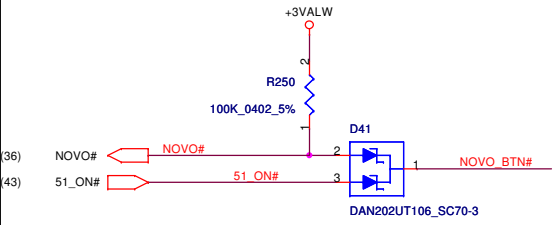
Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

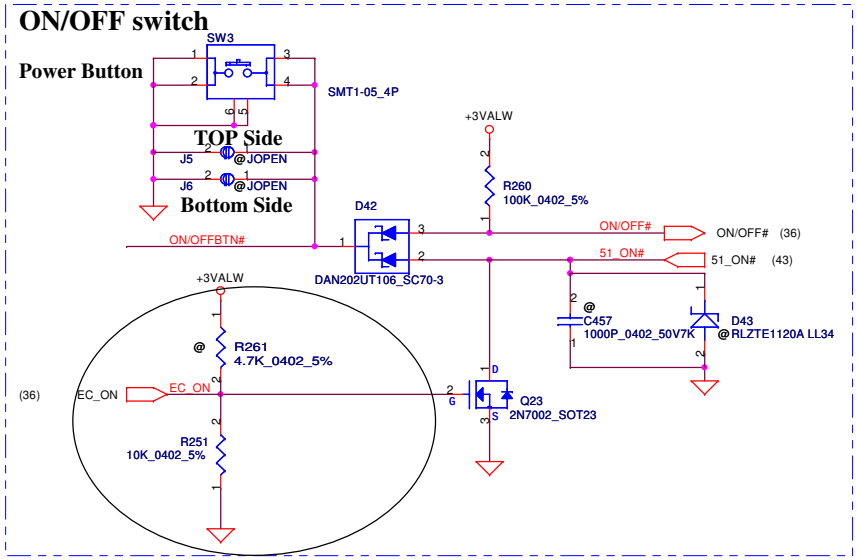
Compal Electronics, Inc.

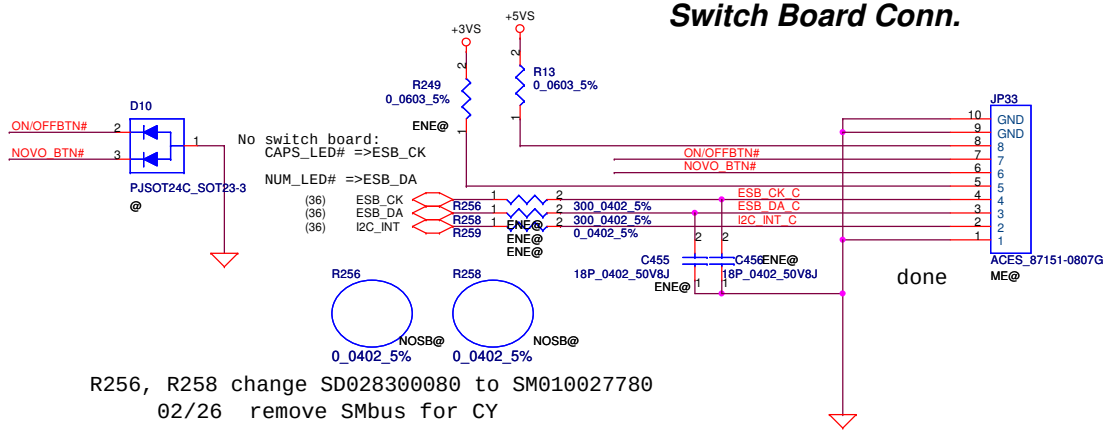
Title: Power OK, Reset and RTC Circuit, TP

Size	Document Number	Rev
Custom	KIWA5/6 LA-5081P	0.4

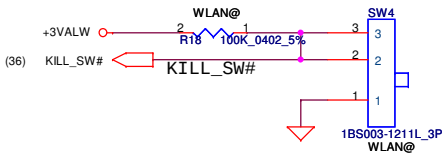
Date: Wednesday, March 18, 2009 Sheet 40 of 53

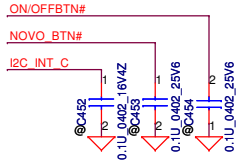




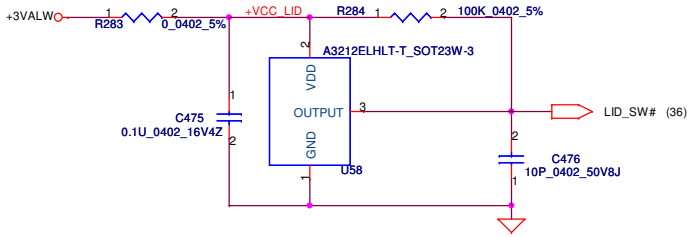


R256, R258 change SD028300080 to SM010027780
02/26 remove SMbus for CY





Lid Switch



Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

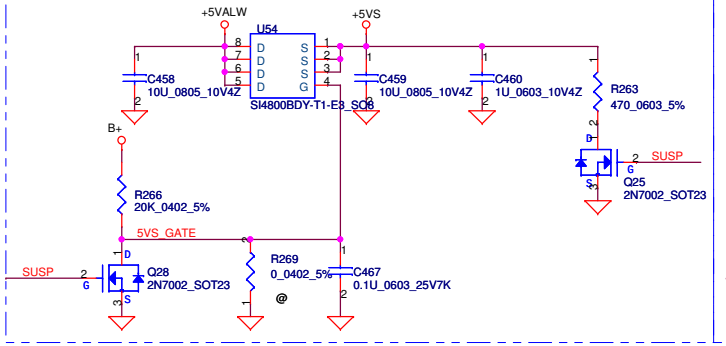
Compal Electronics, Inc.

Title: Audio Jack & SW connector

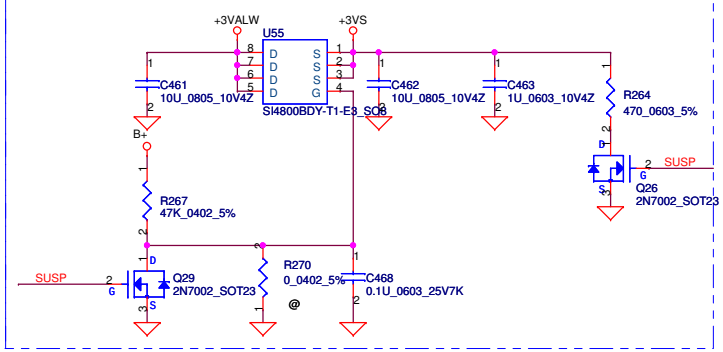
Size	Document Number	Rev
Custom	KIWA5/6 LA-5081P	0.4

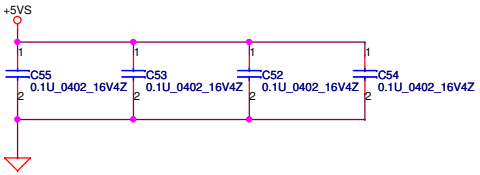
Date: Wednesday, March 18, 2009 Sheet 41 of 53

+5VALW TO +5VS

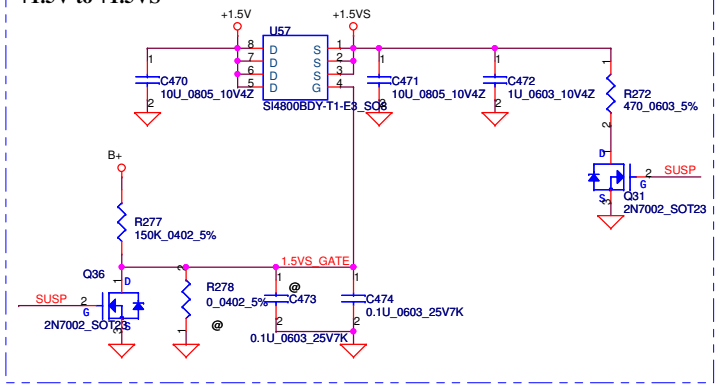


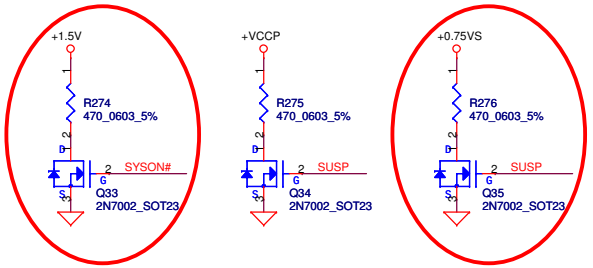
+3VALW TO +3VS

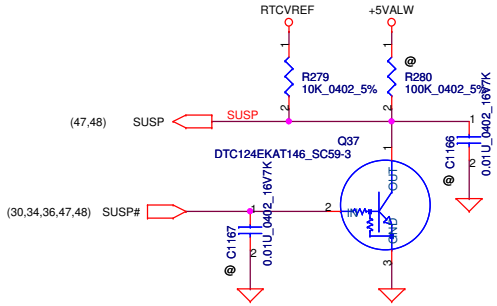


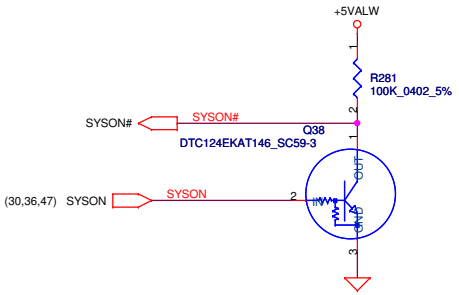


+1.5V to +1.5VS









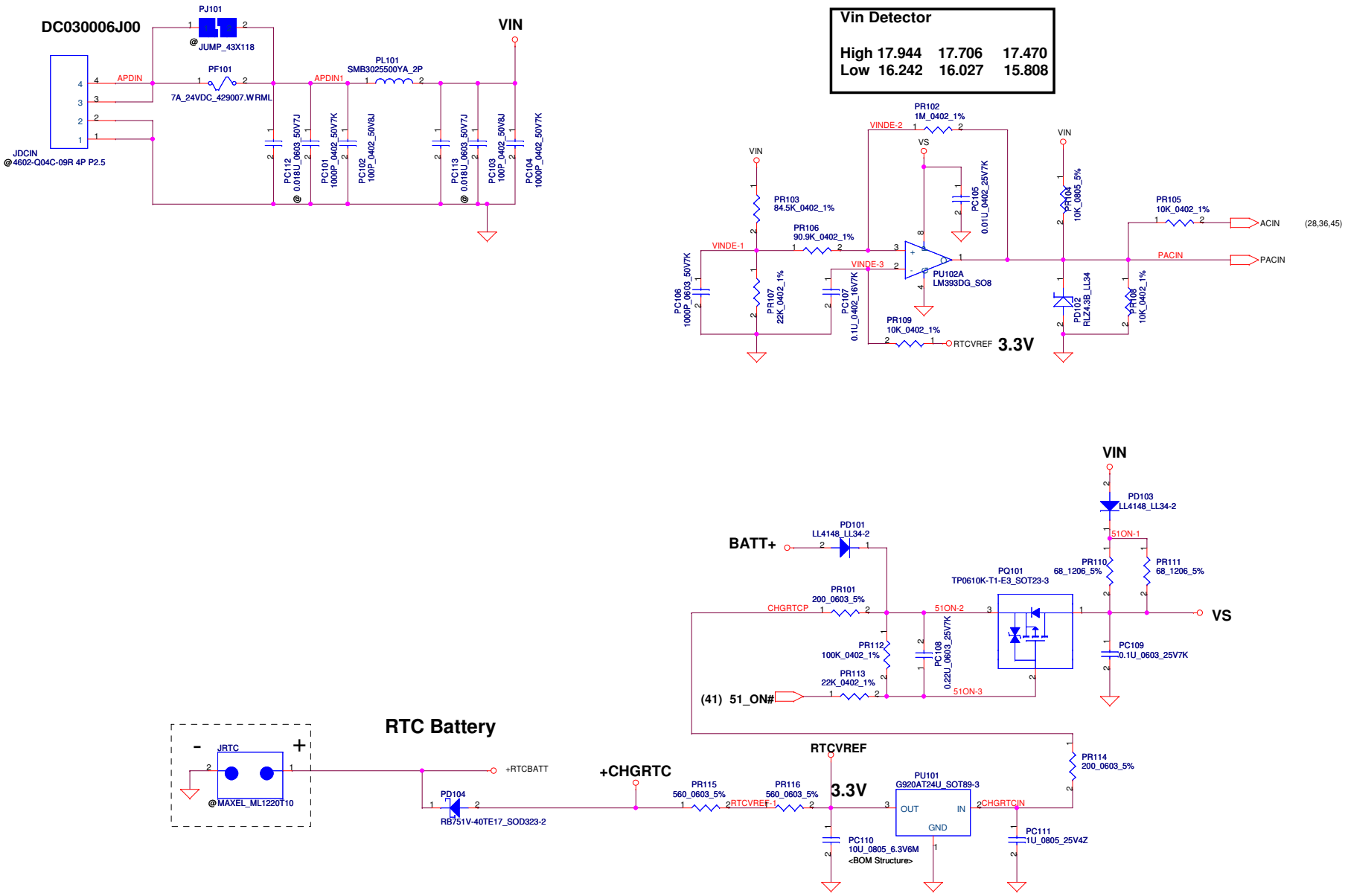
Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
Custom	KIWA5/6 LA-5081P	0.4

Date: Wednesday, March 18, 2009 | Sheet 42 of 53



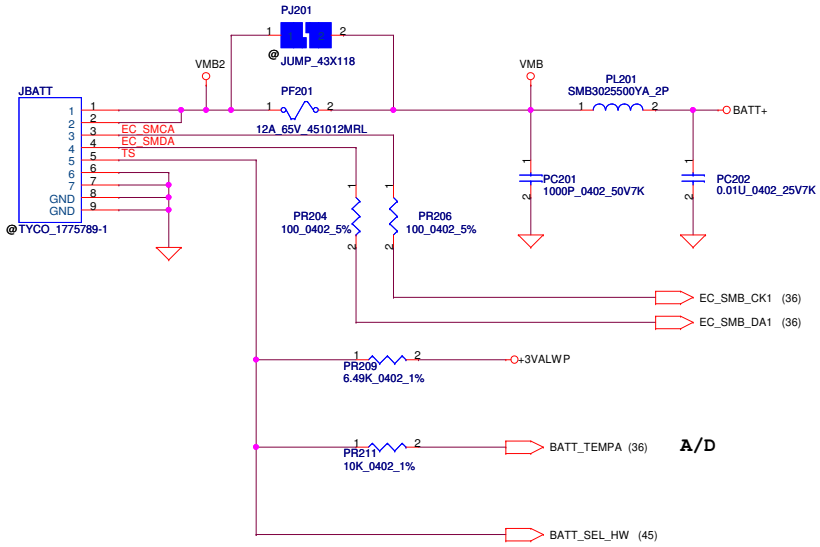
Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

Compal Electronics, Inc.

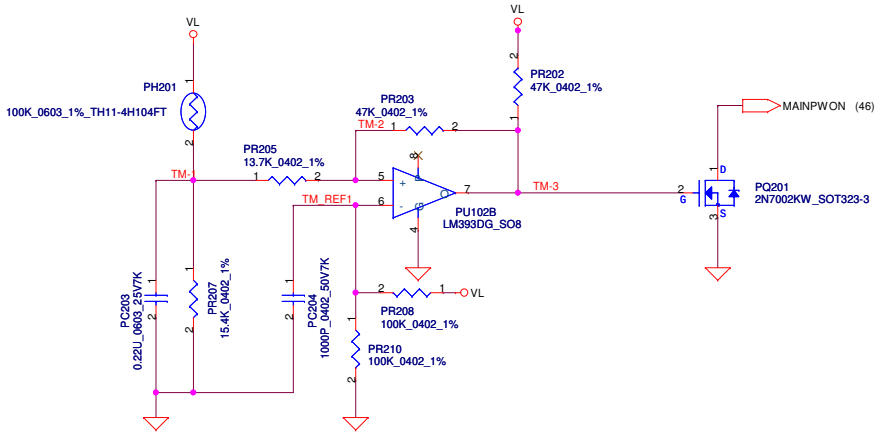
Title: DCIN & DETECTOR

Size	Document Number	Rev
Custom		0.4

Date: Wednesday, March 18, 2009 | Sheet 43 of 53



PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



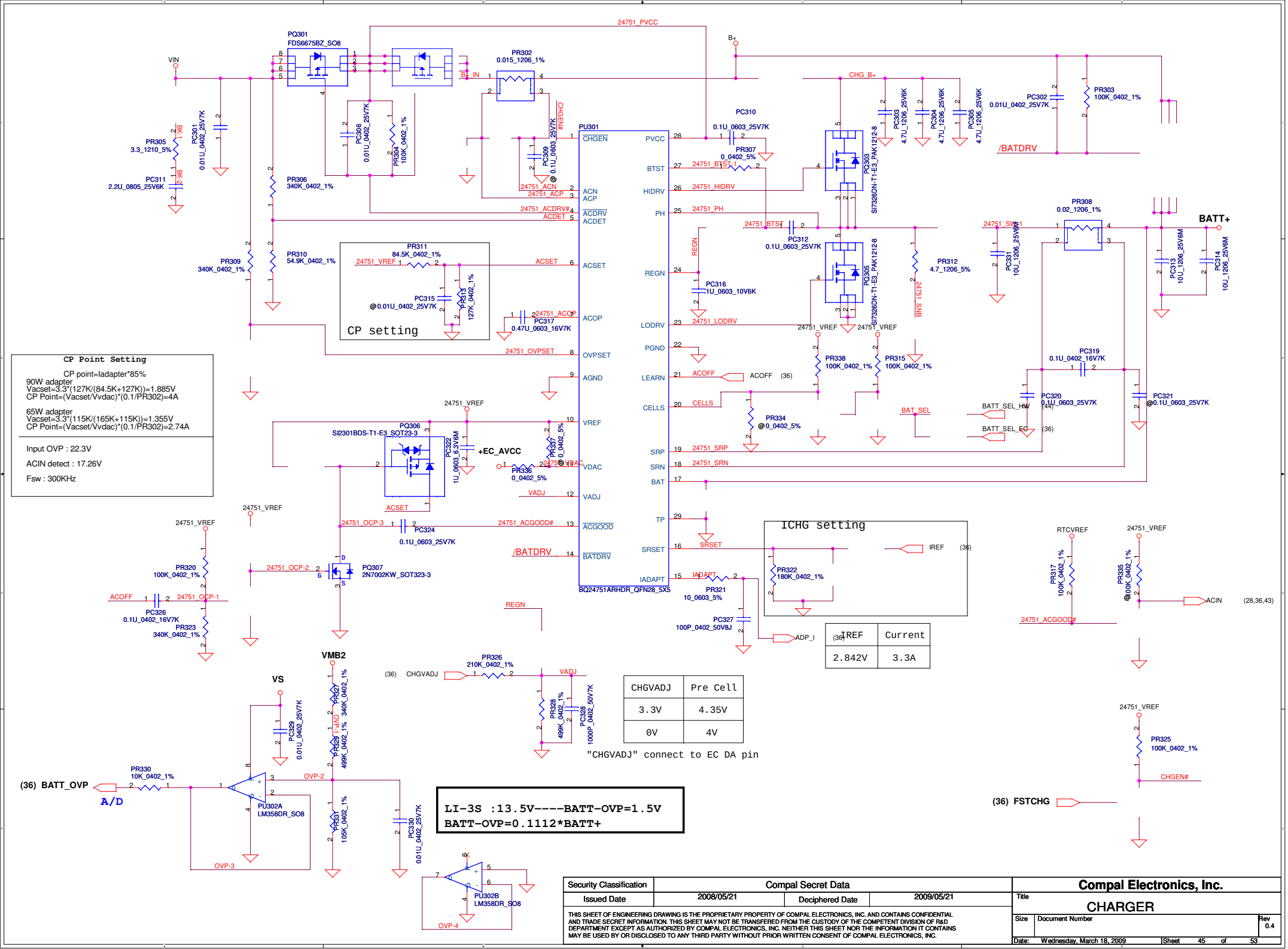
Security Classification	Compal Secret Data		
Issued Date	2007/6/22	Deciphered Date	2008/6/22

Compal Electronics, Inc.

Title: BATTERY CONN / OTP

Size	Document Number	Rev
		0.4

Date: Wednesday, March 18, 2009 | Sheet 44 of 53


CP Point Setting
CP point=ladapter*85%
90W adapter
Vacset=3.3*(127K/(84.5K+127K))=1.885V
CP Point=(Vacset/Vvdac)*(0.1/PR302)=4A
65W adapter
Vacset=3.3*(115K/(165K+115K))=1.355V
CP Point=(Vacset/Vvdac)*(0.1/PR302)=2.74A
Input OVP : 22.3V
ACIN detect : 17.26V
Fsw : 300KHz
CP setting
ICHG setting
IREF (36)
IREF | Current
2.842V | 3.3A
CHGVADJ | Pre Cell
3.3V | 4.35V
0V | 4V
"CHGVADJ" connect to EC DA pin
LI-3S :13.5V----BATT-OVP=1.5V
BATT-OVP=0.1112*BATT+
PU301
BQ24751ARHDR_QFN28_5X5
PQ301 FDS6675BZ_SO8
PQ303 SI7326DN-T1-E3_PAK1212-8
PQ305 SI7326DN-T1-E3_PAK1212-8
PQ306 SI2301BDS-T1-E3_SOT23-3
PQ307 2N7002KW_SOT323-3
PU302A LM358DR_SO8
PU302B LM358DR_SO8
VIN
B+
CHG_B+
BATT+
/BATDRV
ACIN (28,36,43)
(36) BATT_OVP
A/D
(36) FSTCHG
Security Classification | Compal Secret Data
Issued Date | 2008/05/21 | Deciphered Date | 2009/05/21
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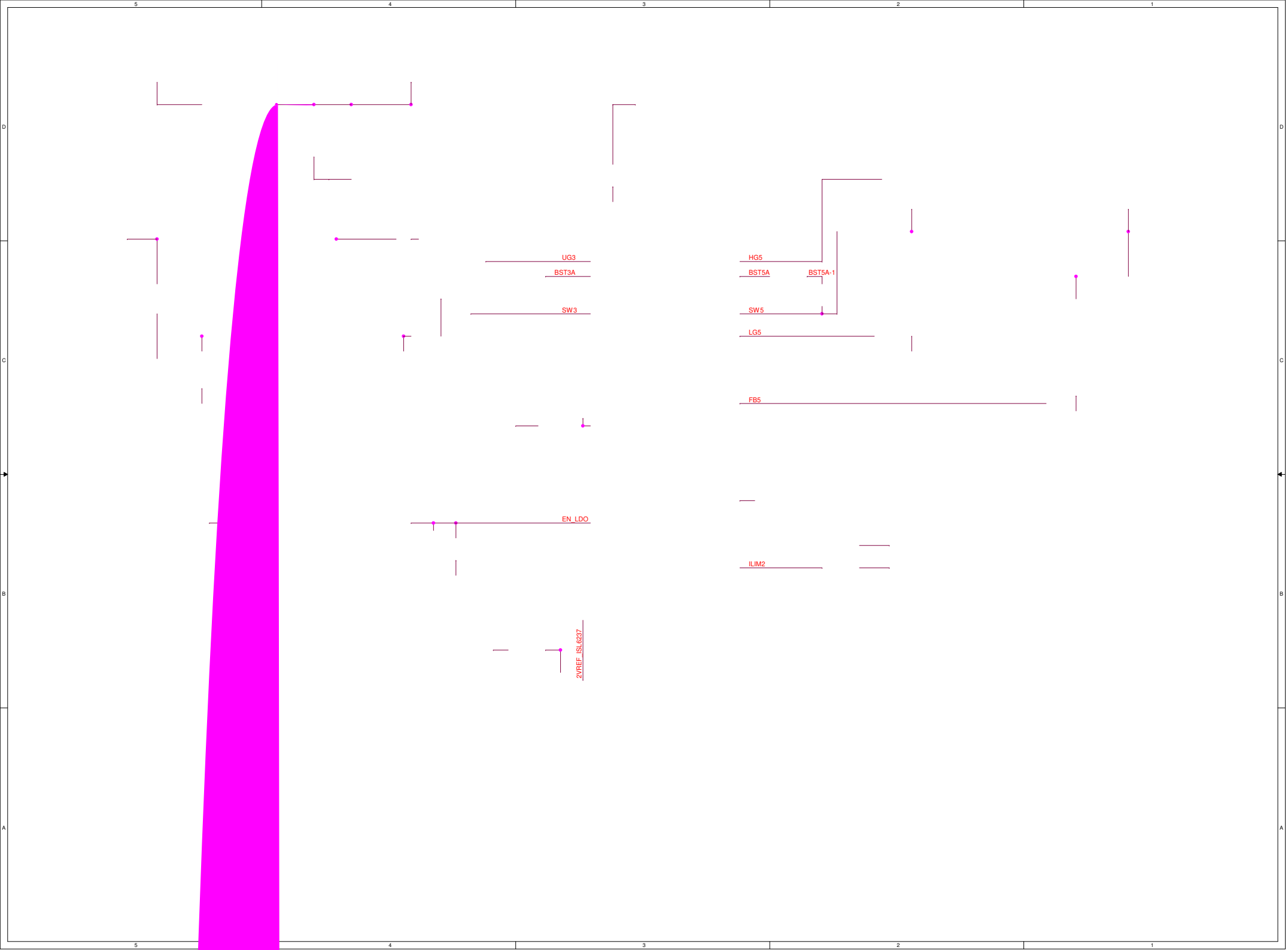
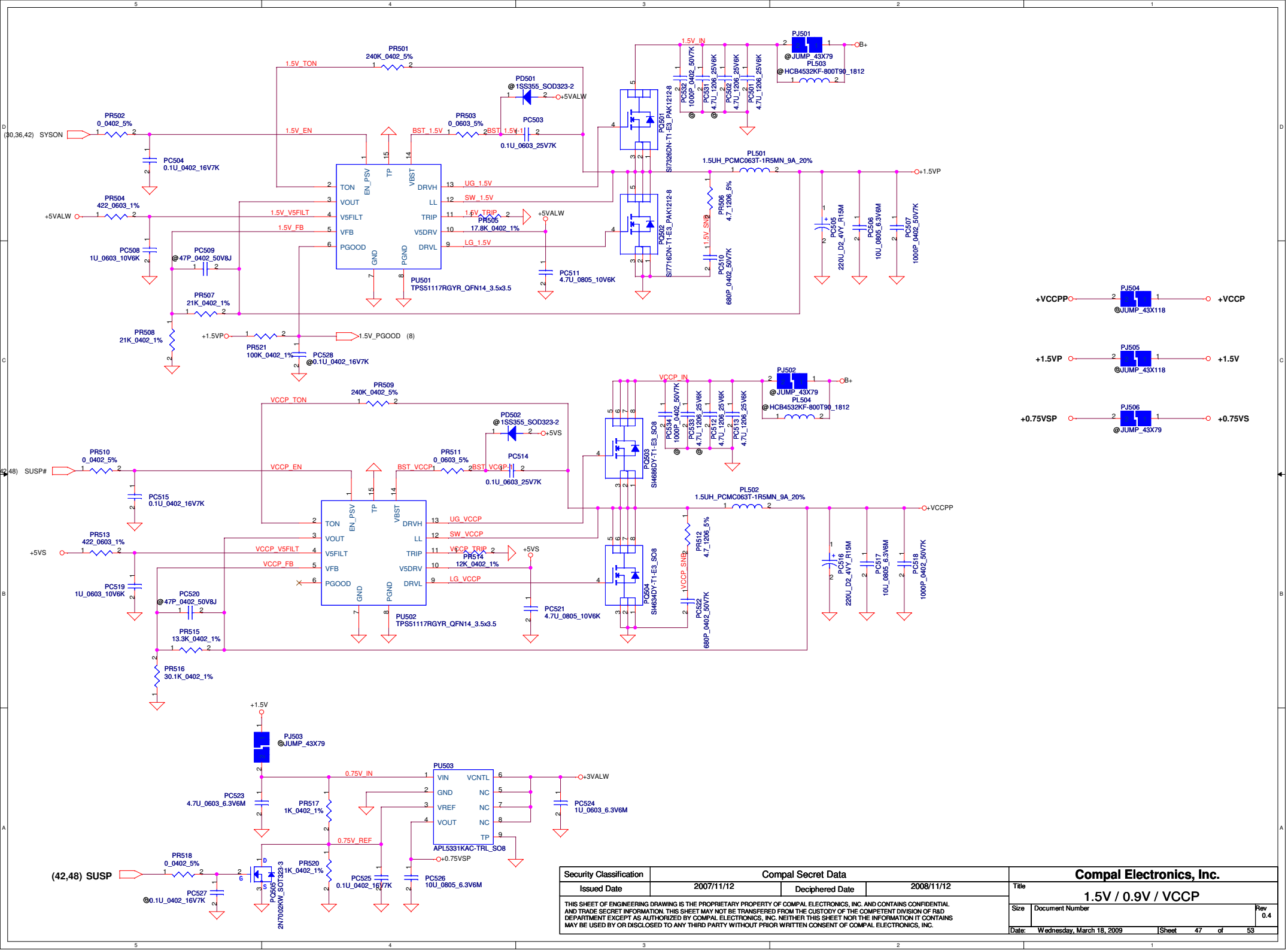
Compal Electronics, Inc.
Title: CHARGER
Size | Document Number | Rev 0.4
Date: Wednesday, March 18, 2009 | Sheet 45 of 53


UG3
BST3A
SW3
EN_LDO
2VREF_ISL6237
HG5
BST5A
BST5A-1
SW5
LG5
FB5
ILIM2



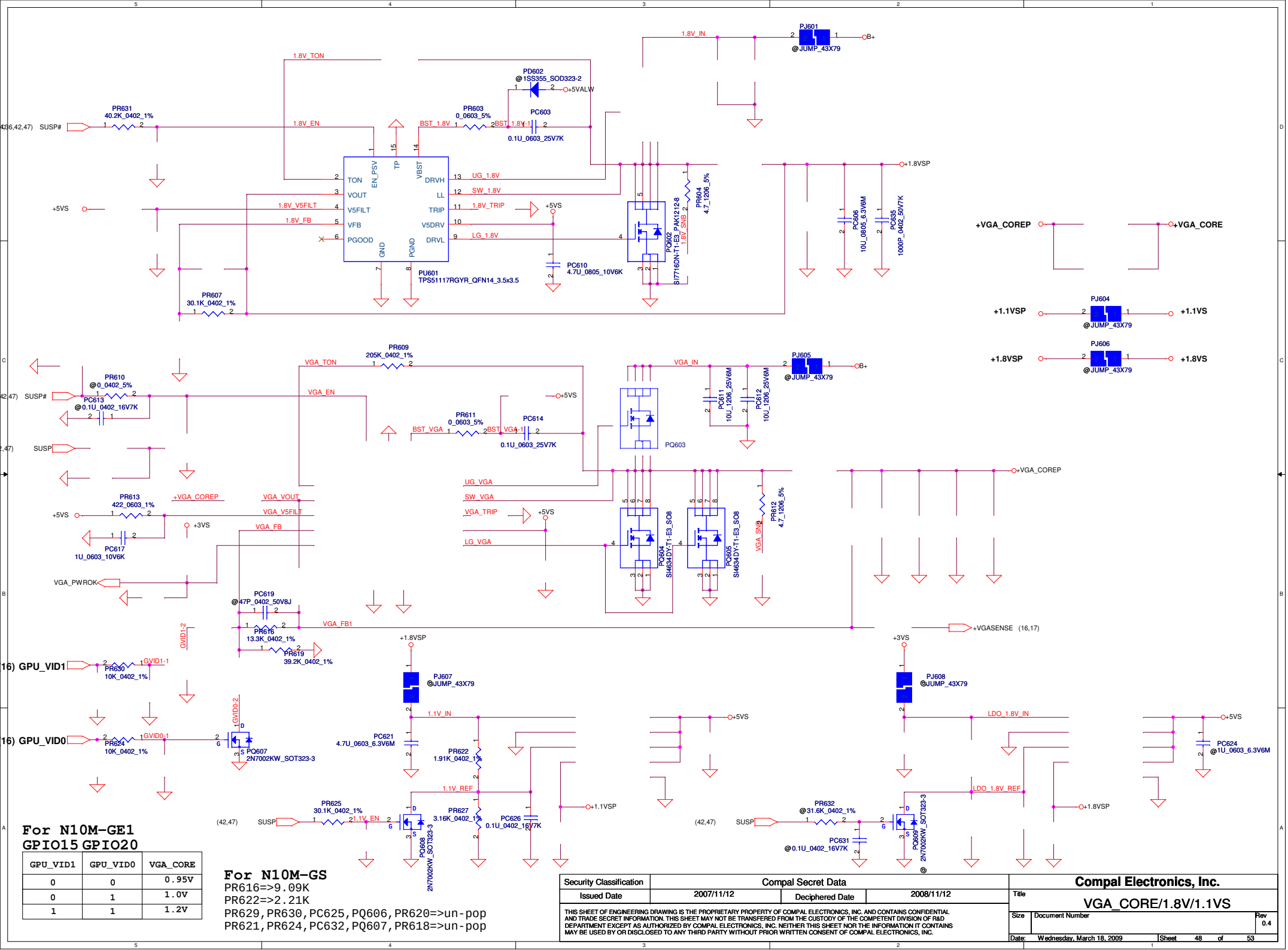
Security Classification	Compal Secret Data		
Issued Date	2007/11/12	Deciphered Date	2008/11/12

Compal Electronics, Inc.

Title: 1.5V / 0.9V / VCCP

Size	Document Number	Rev
		0.4

Date: Wednesday, March 18, 2009 | Sheet 47 of 53



For N10M-GE1
GPIO15 GPIO20

GPU_VID1	GPU_VID0	VGA_CORE
0	0	0.95V
0	1	1.0V
1	1	1.2V

For N10M-GS
PR616=>9.09K
PR622=>2.21K
PR629,PR630,PC625,PQ606,PR620=>un-pop
PR621,PR624,PC632,PQ607,PR618=>un-pop

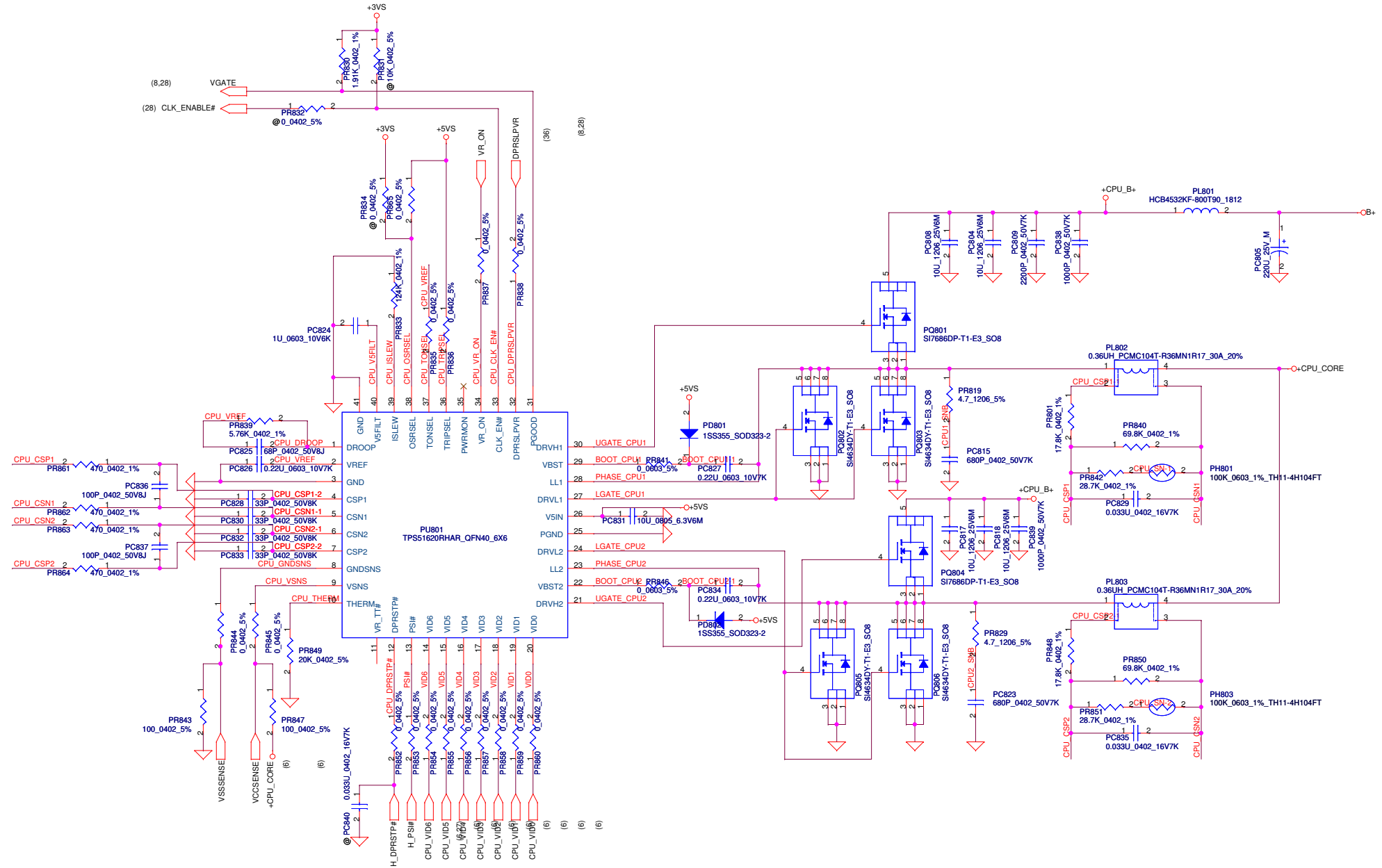
Security Classification	Compal Secret Data		
Issued Date	2007/11/12	Deciphered Date	2008/11/12

Compal Electronics, Inc.

Title: VGA_CORE/1.8V/1.1VS

Size	Document Number	Rev
		0.4

Date: Wednesday, March 18, 2009 | Sheet 48 of 53



Security Classification	Compal Secret Data		
Issued Date	2008/05/21	Deciphered Date	2009/05/21

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Compal Electronics, Inc.

Title: +CPU_CORE

Size	Document Number	Rev
Custom		0.4

Date: Wednesday, March 18, 2009 | Sheet 49 of 53

Version change list (P.I.R. List)

for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		modify battery select circuit			add PQ312 and PR338	2009.01.14	
2		change +1.1VS voltage to +1.05V			change P622 to 2.21K only for N10M-GS(40nm)		
3							
4							
5							
6							
8							
9							
10							
11							
12							
13							
14							
15							
16							
17							
18							
19							
20							
21							

Compal Electronics, Inc.

Title: PIR (PWR)

Size	Document Number	Rev
Custom	KIWAX_LA-5082P	0.4

Date: Wednesday, March 18, 2009 | Sheet 50 of 53

5 4 3 2 1

D

C

B

A

Title

Size DocumenC612 46.9141 m rg 3836 12.g 3836 12.g 3836 12.g 3836 12.g 3836 12.g 383

5 3836 12.g0 3836 12.g8836t12.g0383029Wg3cm 9(7g0 3836 12.g. 12.g 3834)nC61/R13 1023295 46.9141572(e)-257019 l 7184707

5 4 3 2 1

5 3836 12.g0 3836 12.g8836t12.g0383029Wg3cm 9(7g0 3836 12.g. 12.g 3834)nC61/R13 1023295 46.9141572(e)-257019 l 7184707

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	1/15	39	modify H19 hold size, and change the H5、H6 and H19 hold type.	
		42	add 4 CAPs C52, C53, C54 and C55 for EMI.	
		35	change C572 and C574 footprint from 0603 to 0402.	
		34	add R44 for BEEP# test	
2	1/16	30	Remove one Mini-PCIE function! (Connector Side) Remove component is JP18, R363, R364, R367, R369, R371, R373, R375, R377, R378, R379, R380 and R383 Remove 3G function! Remove component is JP14, D12, R6, C6, C7, R7 and D13	
		28	Remove one Mini-PCIE function!(SB side) Remove component is C884 and C885	

Compal Electronics, Inc.		
Title: HW PIR		
Size: B	Document Number: KIWAX_LA-5082P	Rev: 0.4
Date: Wednesday, March 18, 2009	Sheet 52 of 53	

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	3/16	06	add R1089, C1162 and H_DPRSTP#_R	
			add C1163, C1164,and C1165 for EMC request.	
		08	change H_DPRSTP# to H_DPRSTP#_R	
		19	P19 add Bom structure 40nm@ GPU and 55nm@ GPU	
			R999 change to 24.9K	
		23	add R1095 pull high	
		35	swap HP_OUTL and HP_OUTR	
		36	add R1090, R1091, R1092, R1093	
			CAPS_LED#, NUJM_LED#, ESB_CK_R, and ESB_DA_R	
		41	add R256, R258 Bom configuration	
			Remove CY SMBus	
		42	add C1166, C1167 for EMC request.	
2	3/16	28	change PCIE Port1 to Port3	
		30	change PCIE Port1 to Port3	

Compal Electronics, Inc.		
Title: HW PIR		
Size: B	Document Number: KIWAX_LA-5082P	Rev: 0.4
Date: Wednesday, March 18, 2009	Sheet 53 of 53	