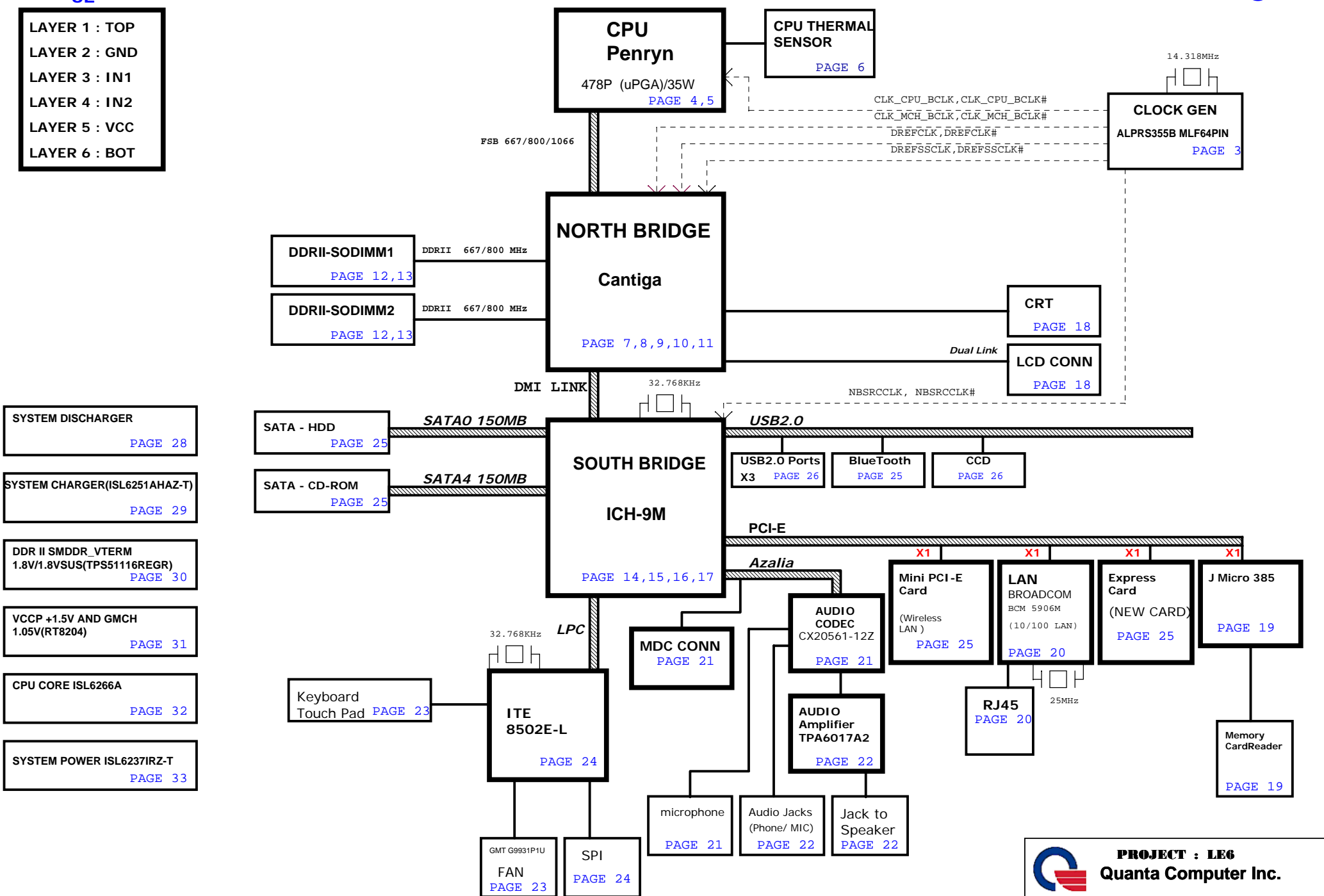


LAYER 1 : TOP
 LAYER 2 : GND
 LAYER 3 : IN1
 LAYER 4 : IN2
 LAYER 5 : VCC
 LAYER 6 : BOT



PROJECT : LE6
Quanta Computer Inc.

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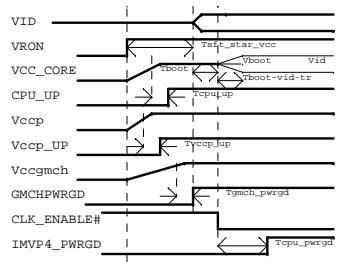
PCB Layers

- Layer 1 TOP
- Layer 2 GND
- Layer 3 IN1
- Layer 4 IN2
- Layer 5 SVCC
- Layer 6 BOTTOM

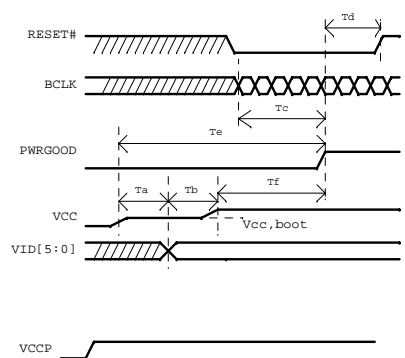
Voltage Rails

Voltage Rails	ON S0-S2	ON S3	ON S4	ON S5	Control signal
VCC_CORE	X				VRON
+1.5V	X				MAINON
+1.05V	X				MAINON
5V_S5/3V_S5/1.5V_S5	X	X	X	X	S5_ON
5VSUS/3VSUS/1.8VSUS	X	X			SUSON
SMDRR_VTERM/+2.5V/+3V/+5V/+12V	X				MAINON
+VCC GFX_CORE/+1.2V GFX_PCIE	X				MAINON
LANVCC	X	X	X	X	LAN_ON
3VPCU	X	X	X	X	VL
5VPCU	X	X	X	X	VL

Power On Sequencing Timing Diagram

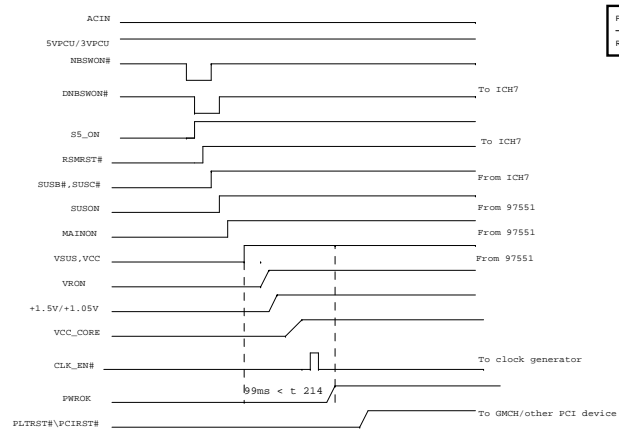


YONAH Power-up Timing Specifications

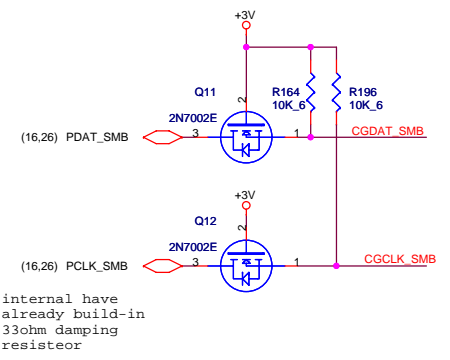
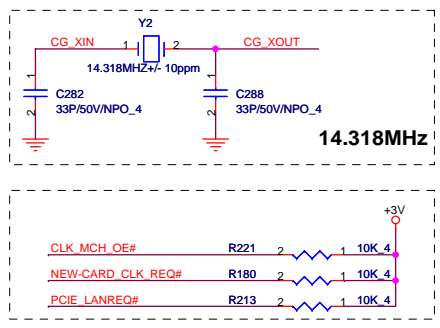
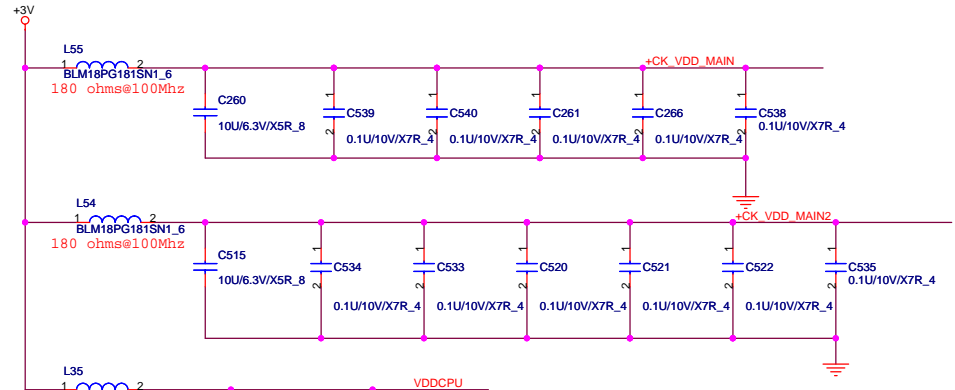


Te=VCC and WCCP assertion to VID[5:0] valid
 Tb=VID[5:0] stable to VCC valid
 Tc=BCLK stable to PWRGOOD assertion
 Td=PWRGOOD to RESET# de-assertion time
 Te=Vcc,boot valid to PWRGOOD assertion time

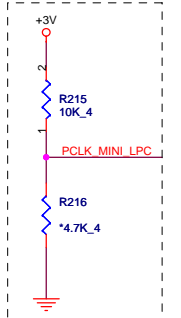
ACIN POWER ON TIMING



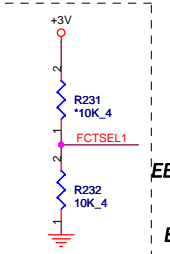
PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
RICHES2	AD25	REQ0# / GNT0#	INT Err#



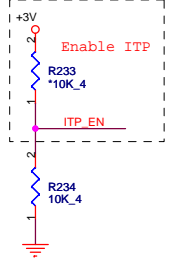
internal have already build-in 33ohm damping resistor



0=overclocking of CPU and SRC Allowed
1 = overclocking of CPU and SRC not Allowed



0=UMA
1 = External VGA



Enable ITP

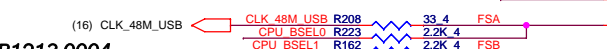
EB1213-0001



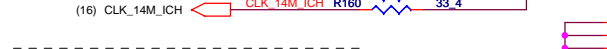
EB1213-0002



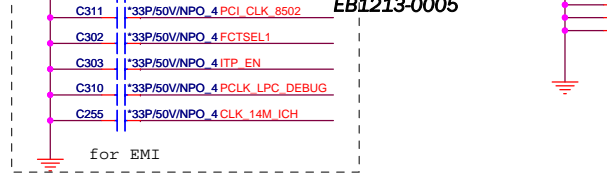
EB1213-0003



EB1213-0004

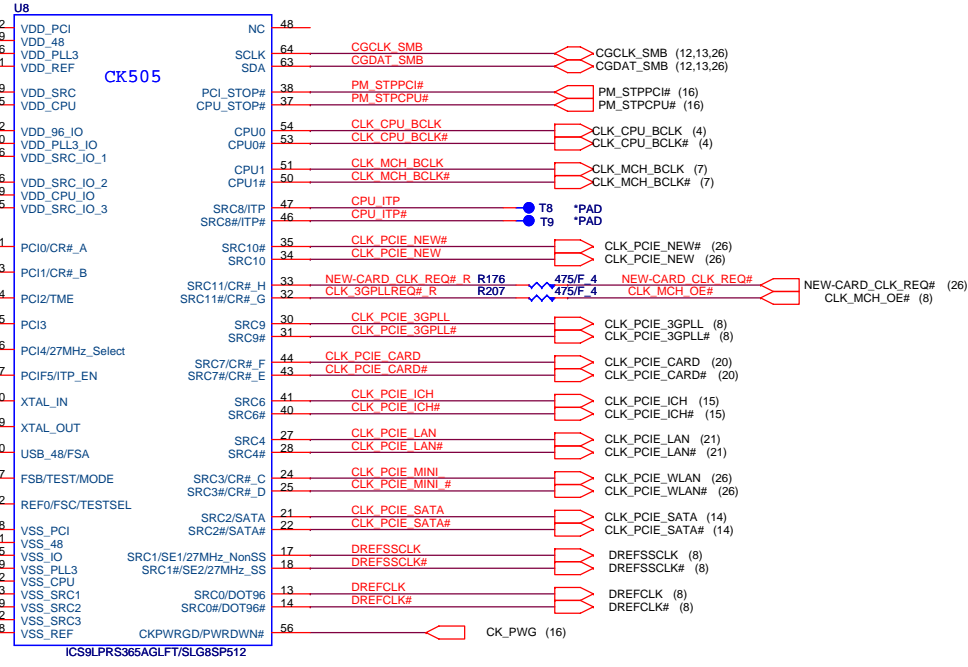


EB1213-0005

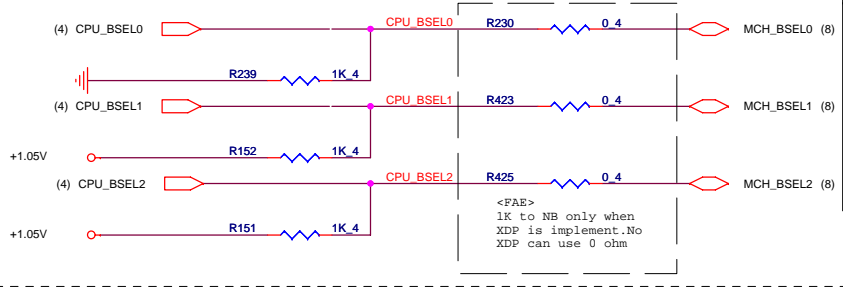


for EMI

CK505



CPU Clock select

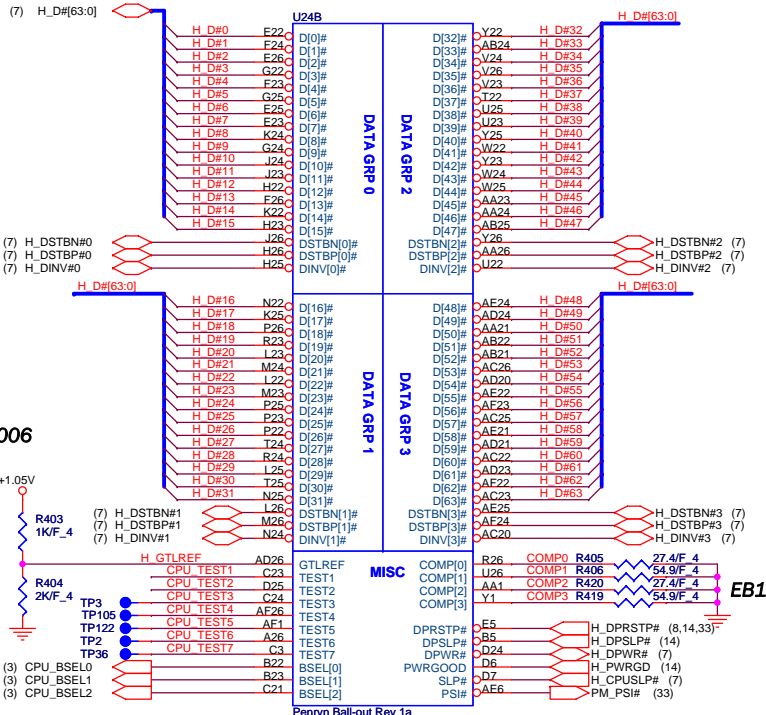
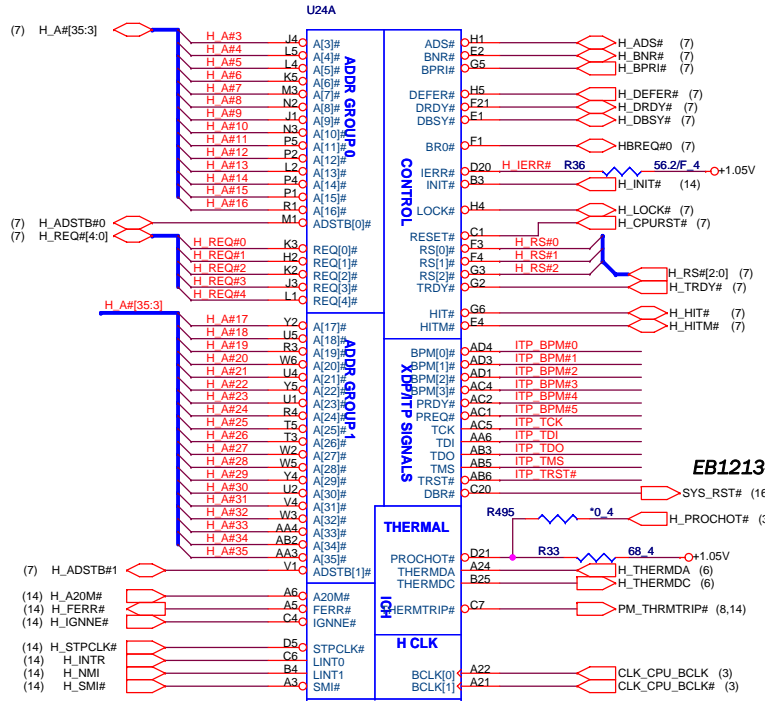


FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	0	0	200	100	33
0	1	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

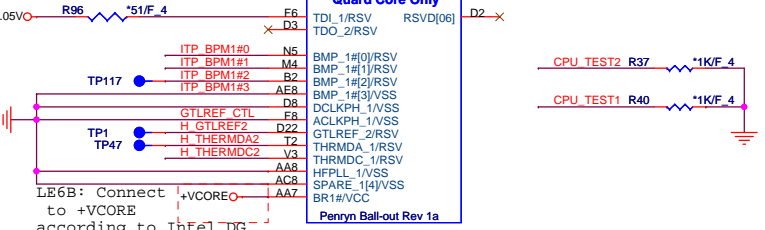
<FAE>
1K to NB only when XDP is implement. No XDP can use 0 ohm

GCLK_SEL = FCTSEL1

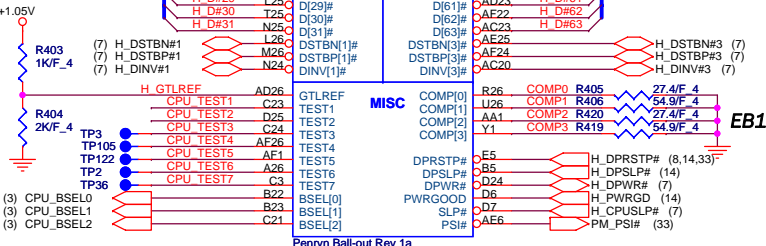
FCTSEL1 (PIN6)	PIN13	PIN14	PIN24	PIN25
0=UMA	DREFCLK	DREFCLK#	SRCT1/LCDT_100	SRCT1/LCDT_100



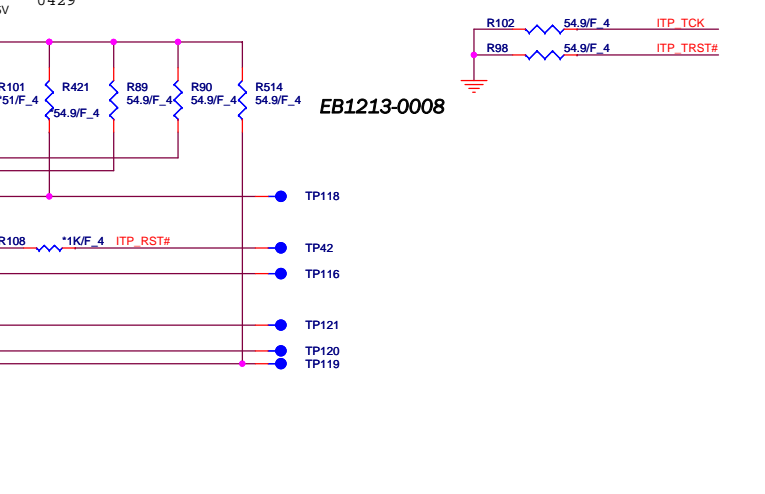
EB1213-0007



EB1213-0006



EB1213-0010

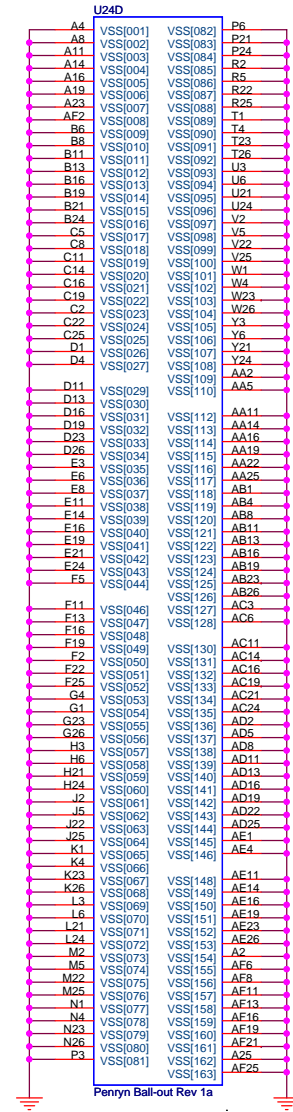
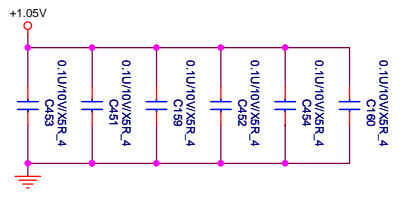
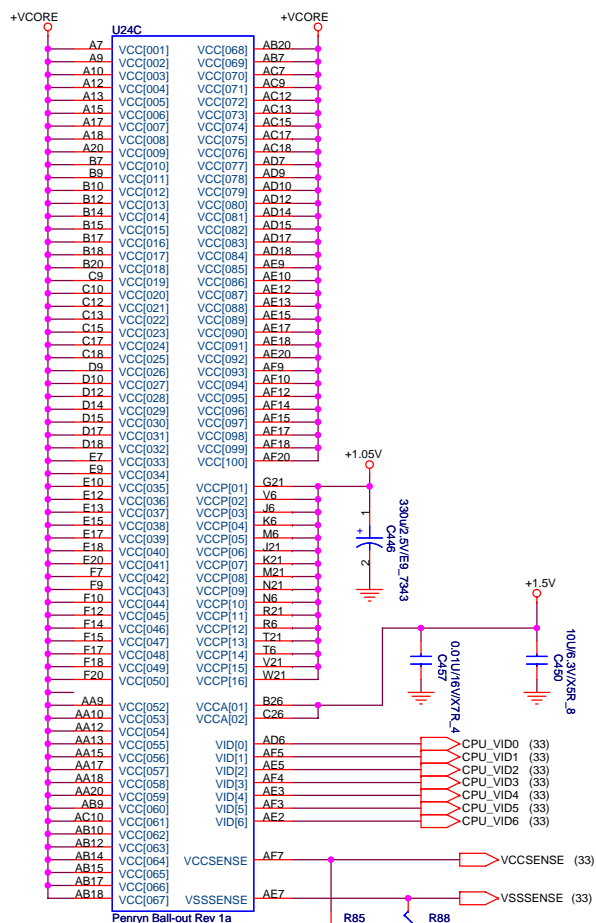
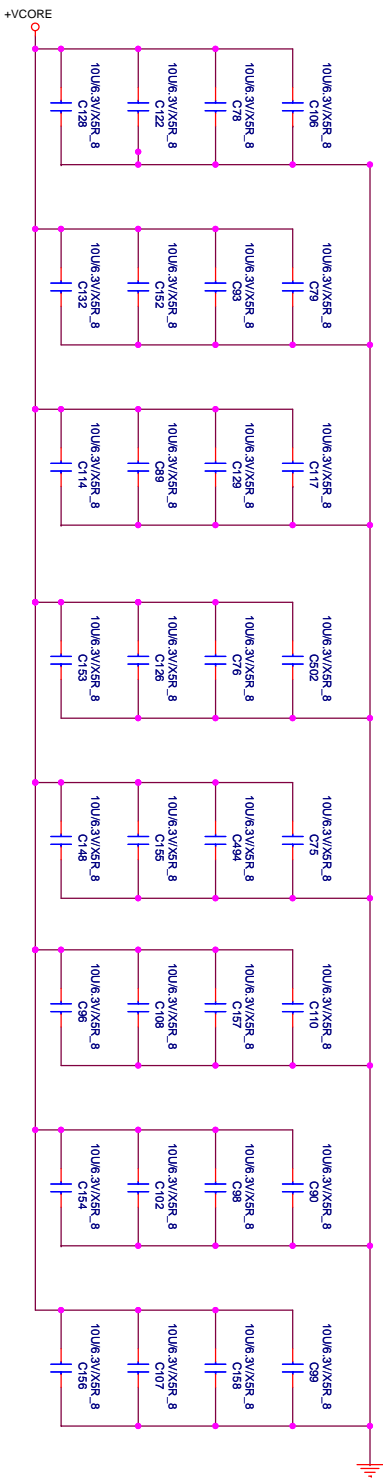


EB1213-0008

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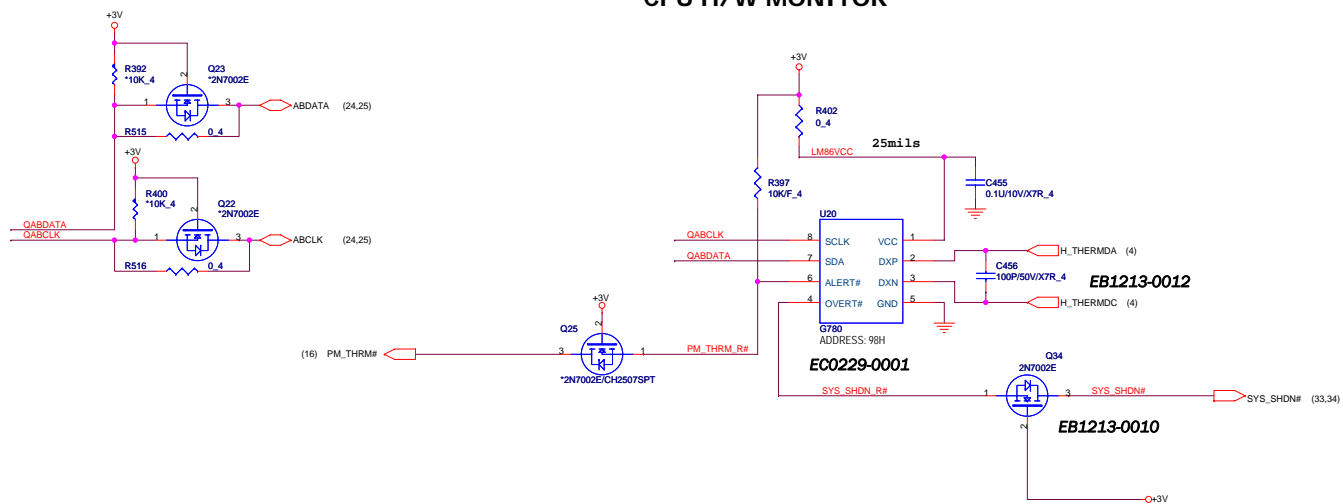
(3,6,8,11,12,13,14,15,16,17,18,20,22,24,25,26,27,29,30,31,32,33,34) +3V
(3,4,7,8,10,11,14,17,29,32,33) +1.05V
(11,14,15,17,26,29,32) +1.5V
(29,33) +VCORE



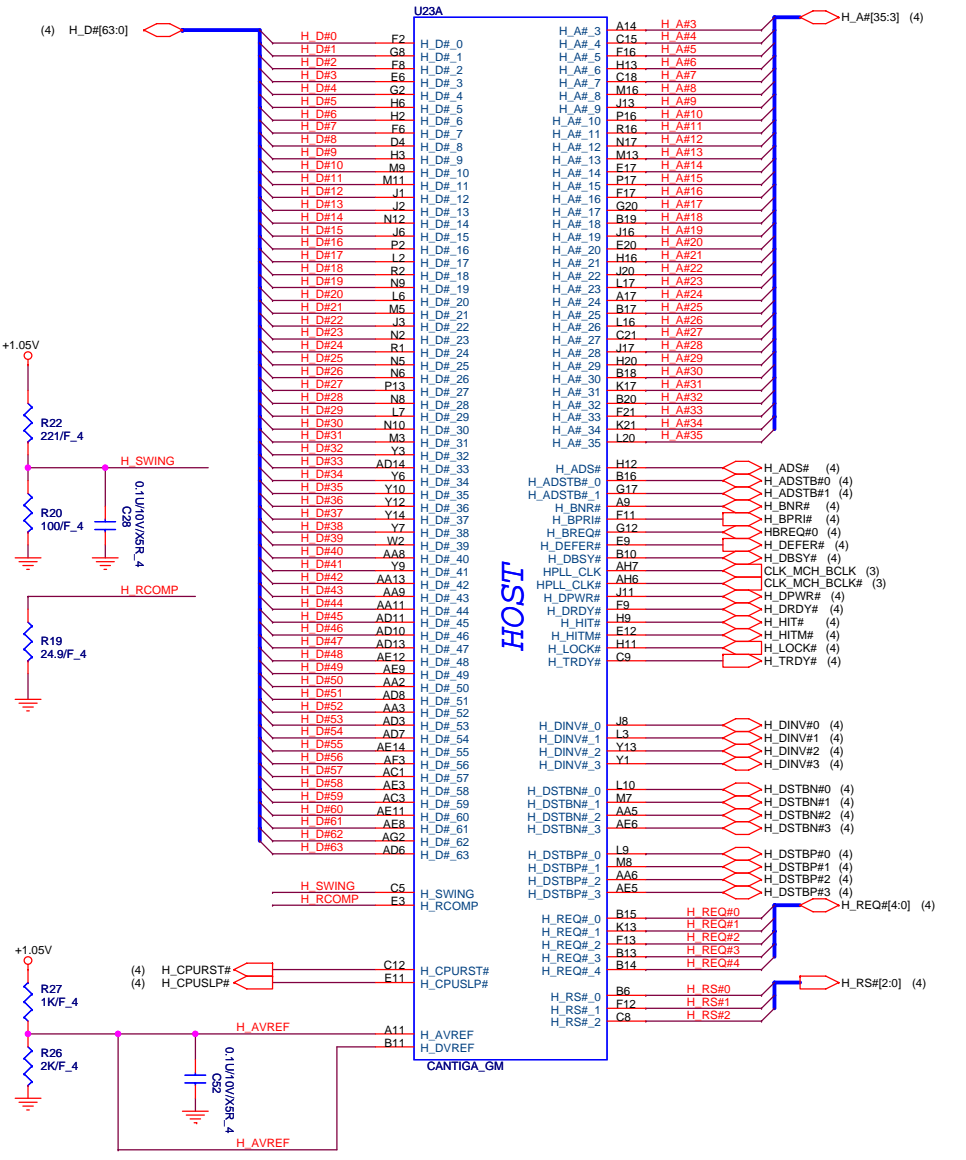
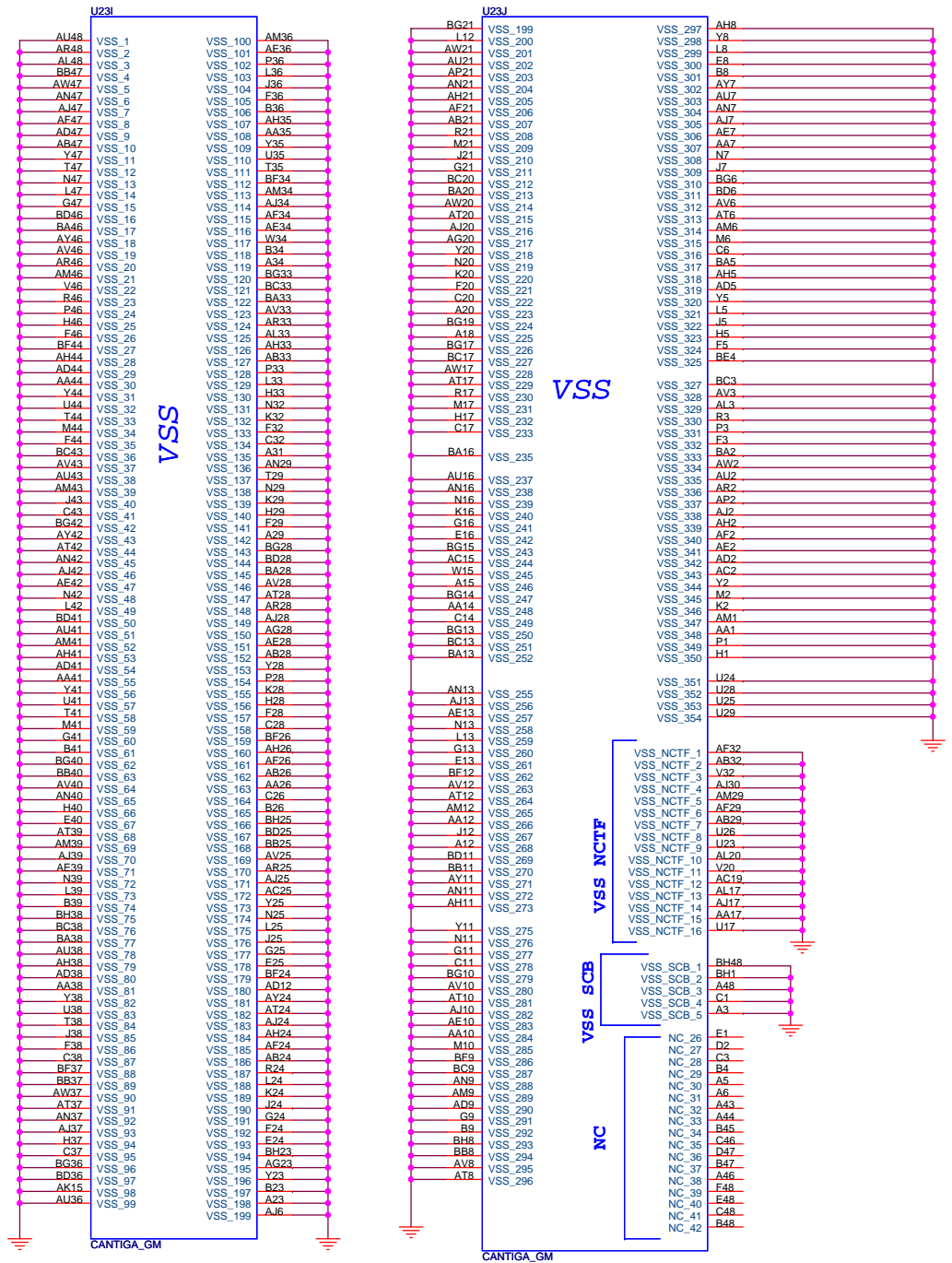
PROJECT : LEG
Quanta Computer Inc.

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CPU H/W MONITOR



EB1213-0011



(3,4,5,8,10,11,14,17,29,32,33) +1.05V

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(3,6,11,12,13,14,15,16,17,18,20,22,24,25,26,27,29,30,31,32,33,34) +V
 (10,11,12,29,31,32) +1.8VSUS
 (3,4,5,7,10,11,14,17,29,32,33) +1.05V
 (11) +1.05V_PEG

MCH_CFG_5 DMi2 selection
 Low: DMi2
 High: DMi4 (Default)
 MCH_CFG_16 FSB Dynamic ODT

Low: Dynamic ODT disabled
 High: Dynamic ODT enabled (Default)
 MCH_CFG_9 PCI Express Graphic Lane

Low: Reverse Lane
 High: Normal operation(Default)
 MCH_CFG_19 DMI Lane Reversal

Low: Normal (Default)
 High: Lane Reserved
 MCH_CFG_6 ITPM Host Interface

Low: ITPM Host Interface enabled
 High: ITPM Host Interface disabled (Default)
 MCH_CFG_7 Intel (R) Management Engine Crypto

Low: Intel (R) Management Engine Crypto
 TLS cipher suite with no confidentiality
 High: Intel (R) Management Engine Crypto
 TLS cipher suite with no confidentiality (Default)

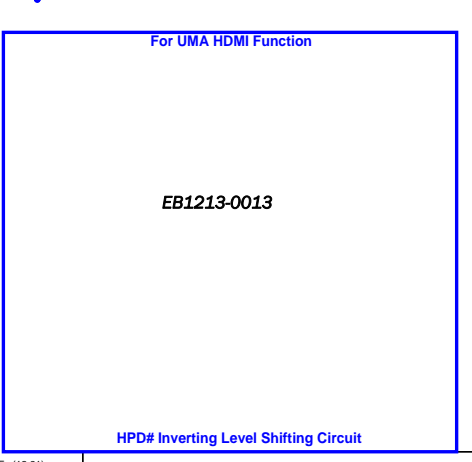
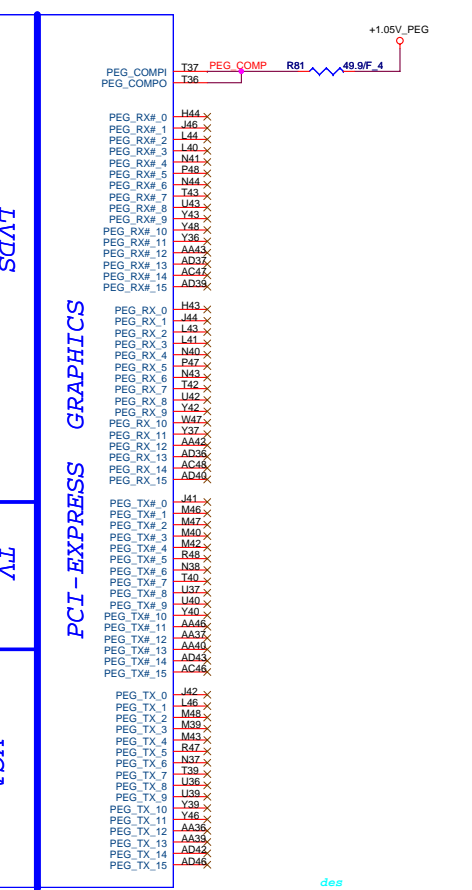
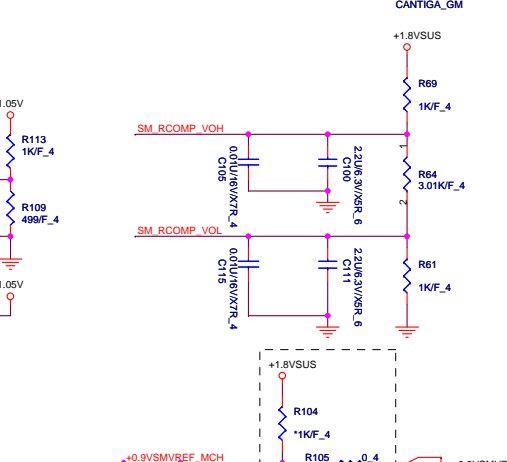
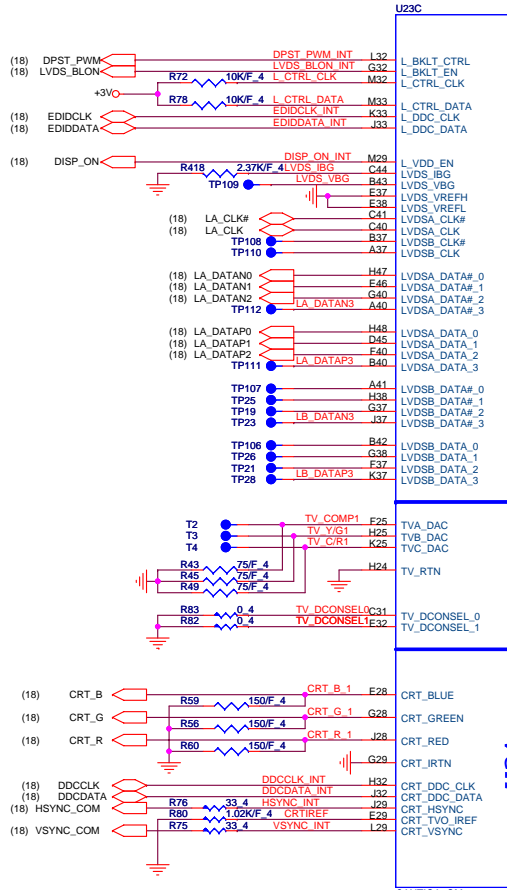
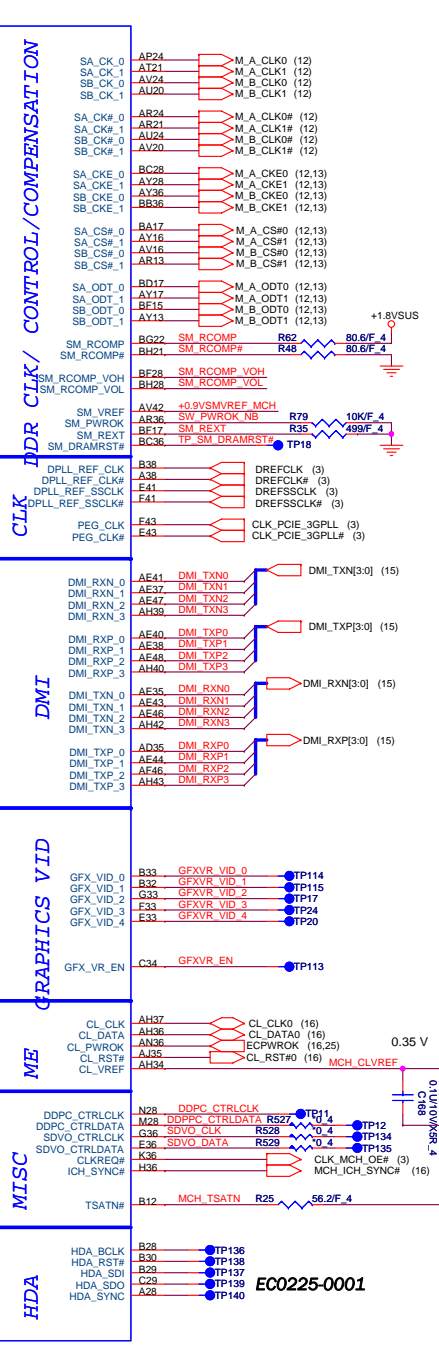
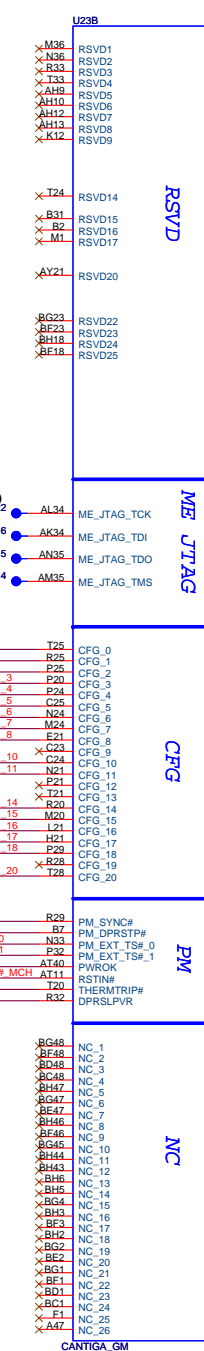
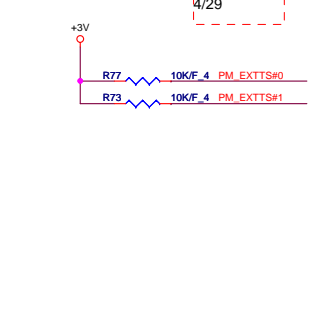
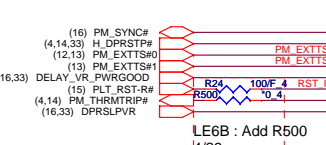
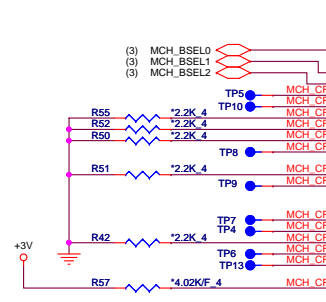
MCH_CFG_10 PCIe Lookback Enable
 Low: Enabled
 High: Disabled (Default)
 MCH_CFG_12/13 XOR/ALLZ/CLOCK Un-gating

MCH_CFG_13 MCH_CFG_12 Configuration

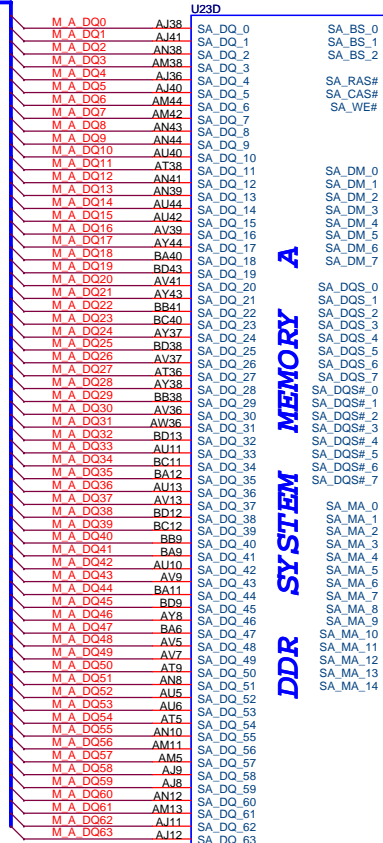
0	0	Reserved
1	0	XOR Mode enabled
0	1	All-Z Mode enabled
1	1	Normal operation (Default)

MCH_CFG_13 MCH_CFG_12 Configuration

0	0	Reserved
1	0	XOR Mode enabled
0	1	All-Z Mode enabled
1	1	Normal operation (Default)

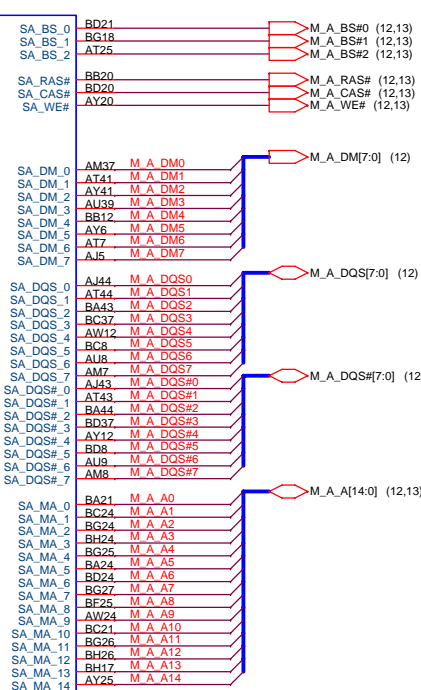


(12) M_A_DQ[63:0]



CANTIGA_GM

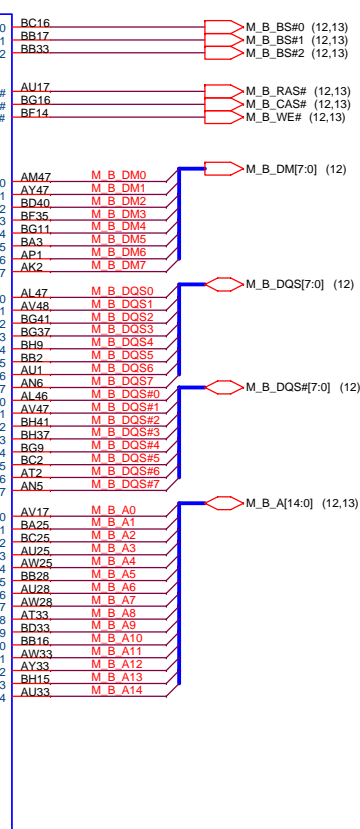
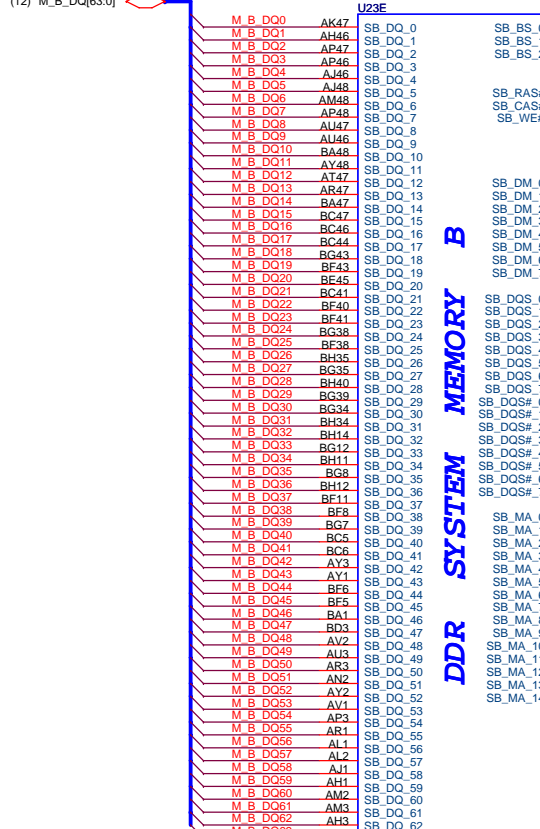
DDR SYSTEM MEMORY A



CANTIGA_GM

DDR SYSTEM MEMORY B

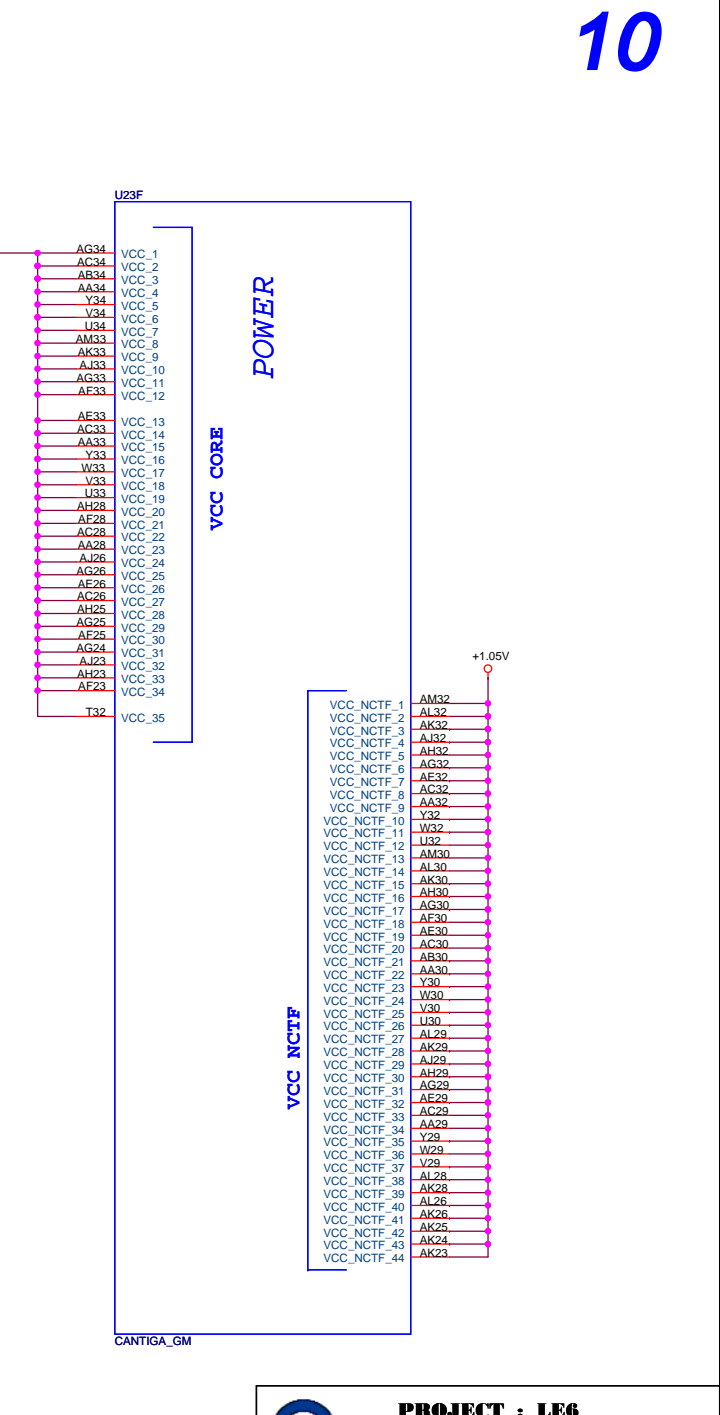
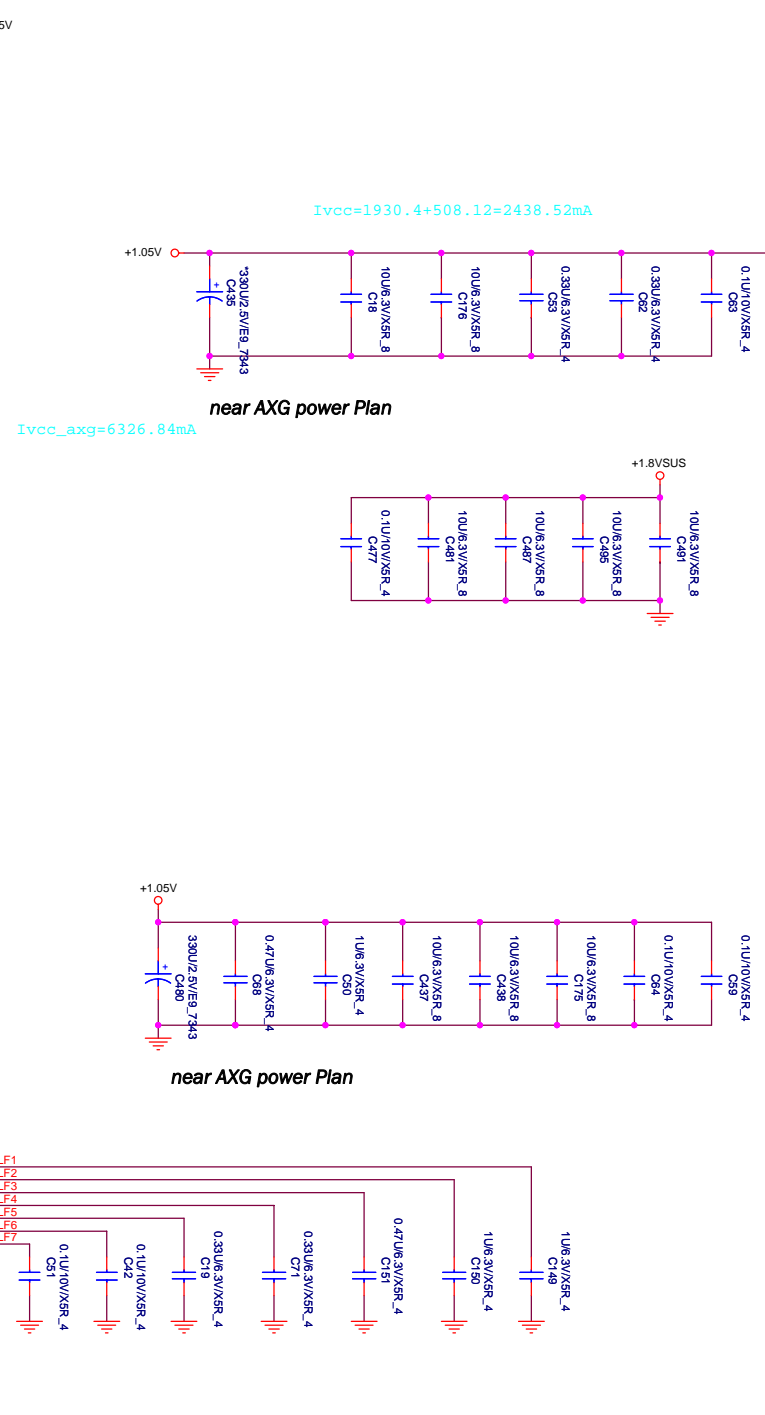
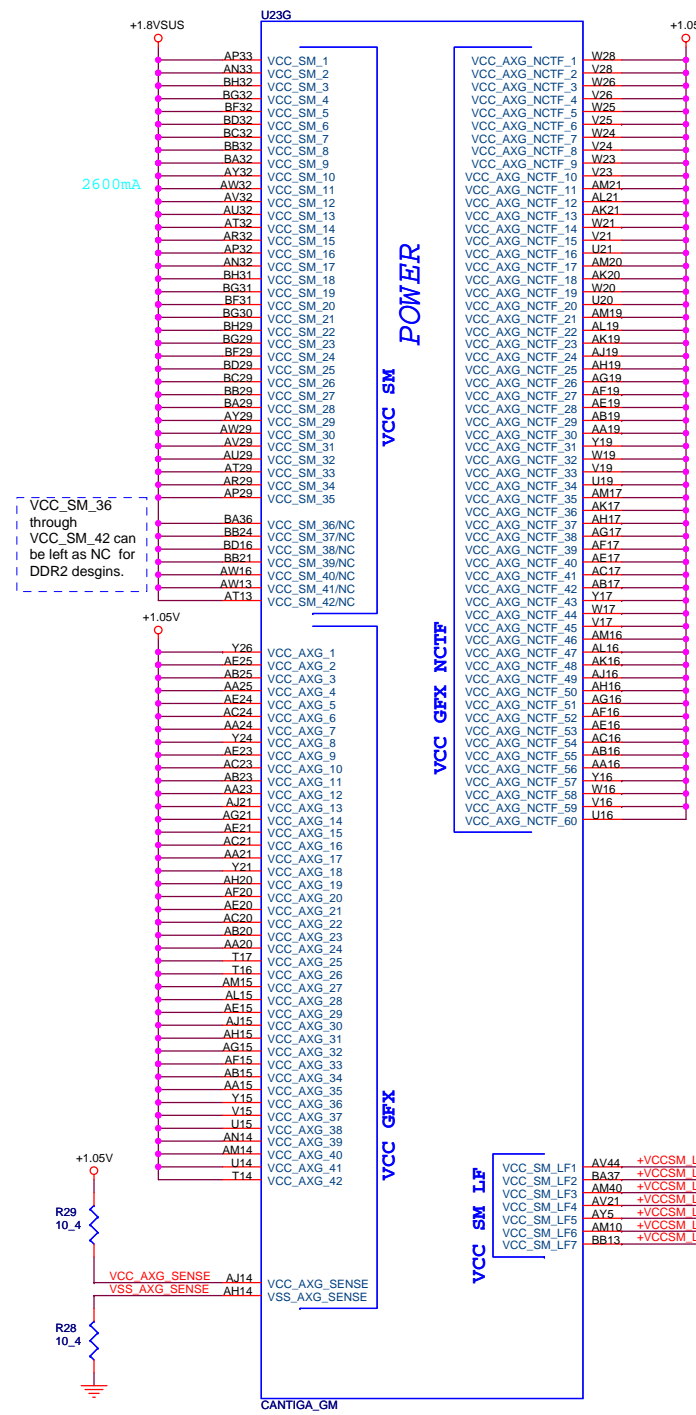
(12) M_B_DQ[63:0]

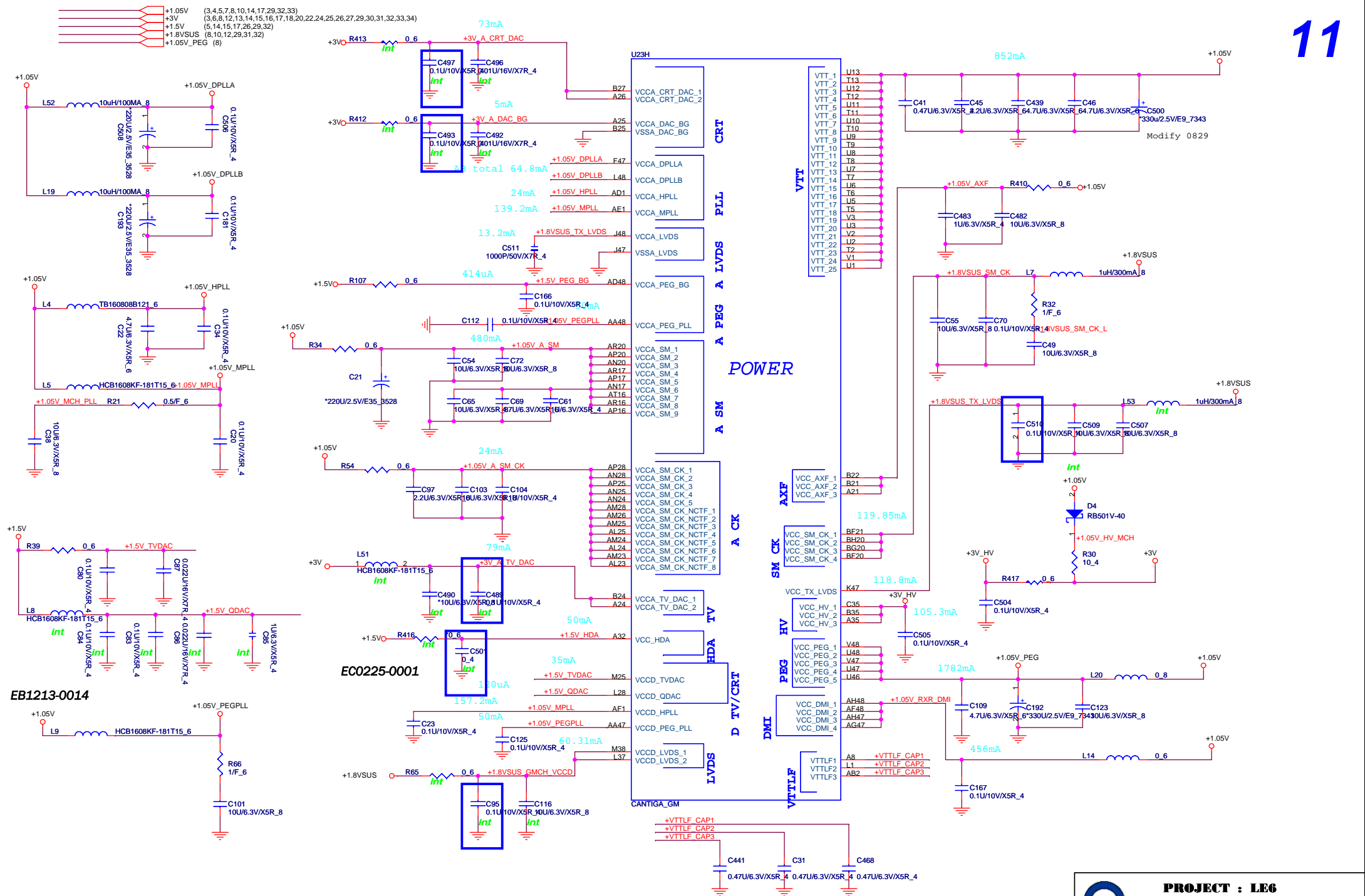


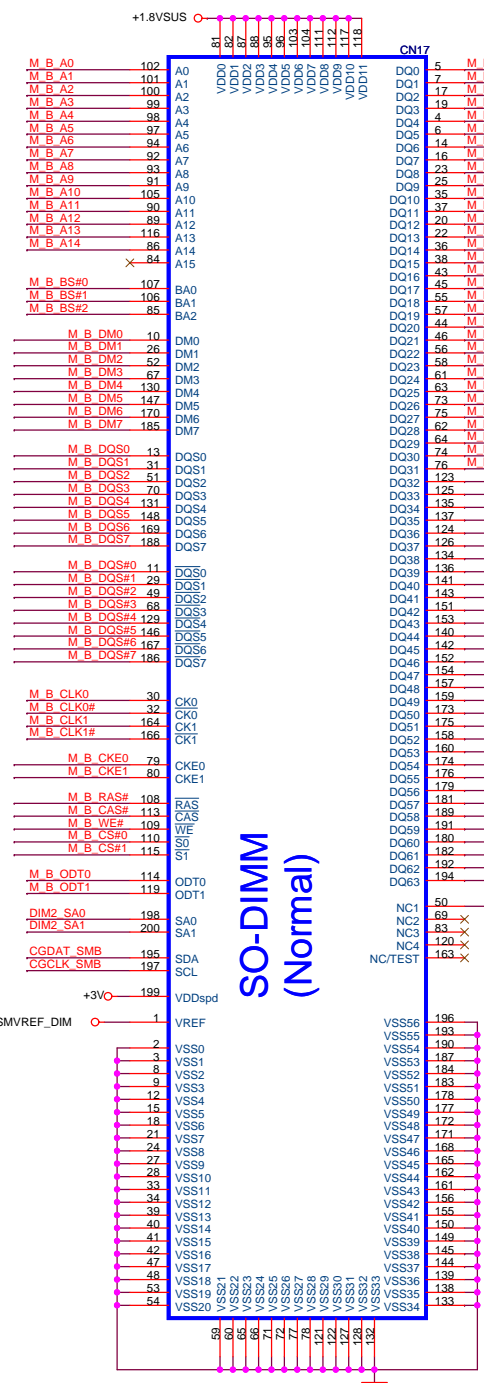
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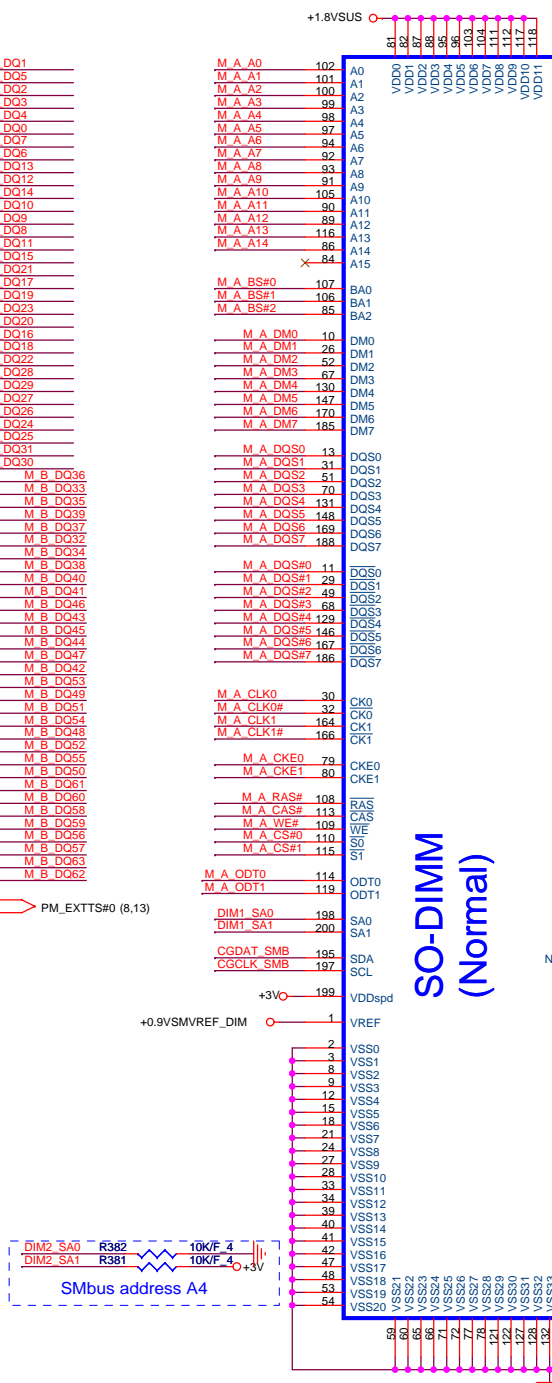






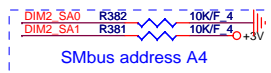
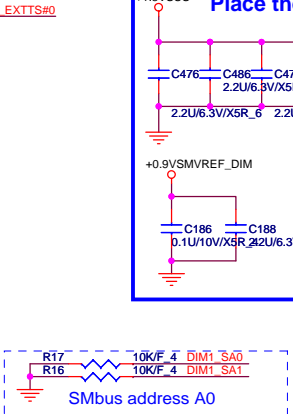
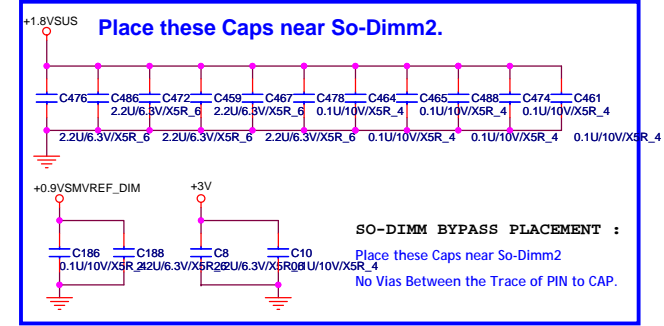
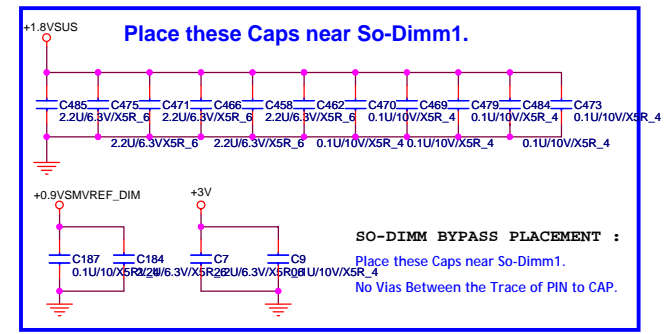
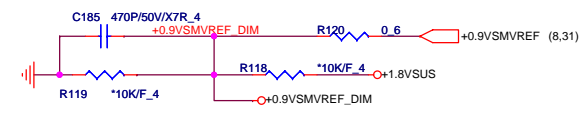
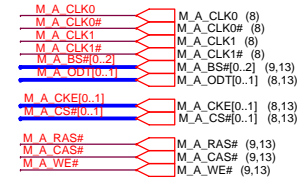
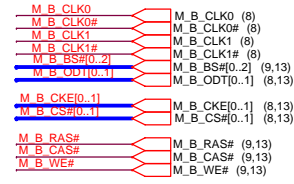
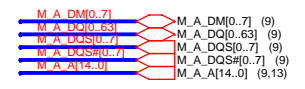
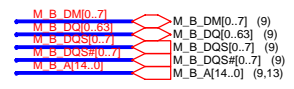
SO-DIMM (Normal)

H 9.2



SO-DIMM (Normal)

H 5.2



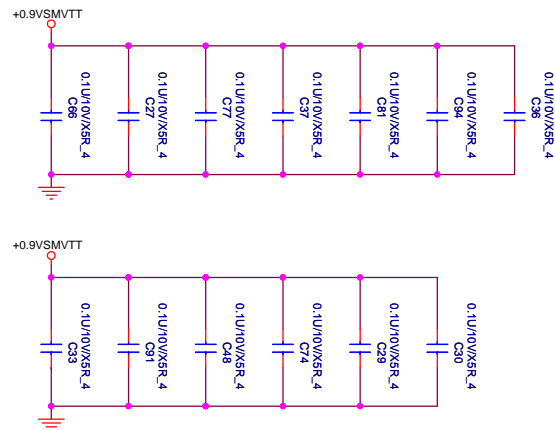
(3,6,8,11,13,14,15,16,17,18,20,22,24,25,26,27,29,30,31,32,33,34) +1.8VSUS +3V

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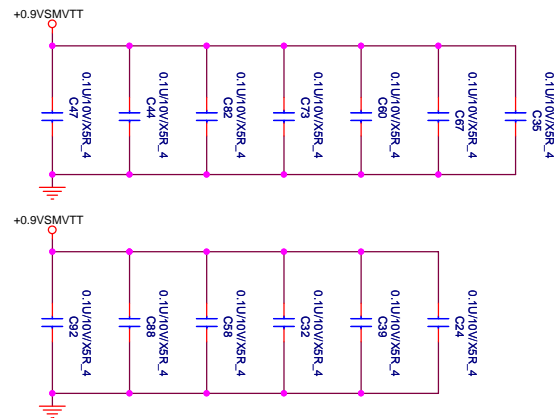
Size: Custom Document Number: **DDR2 DIMM** Rev: 1A
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DDRII DUAL CHANNEL A,B.

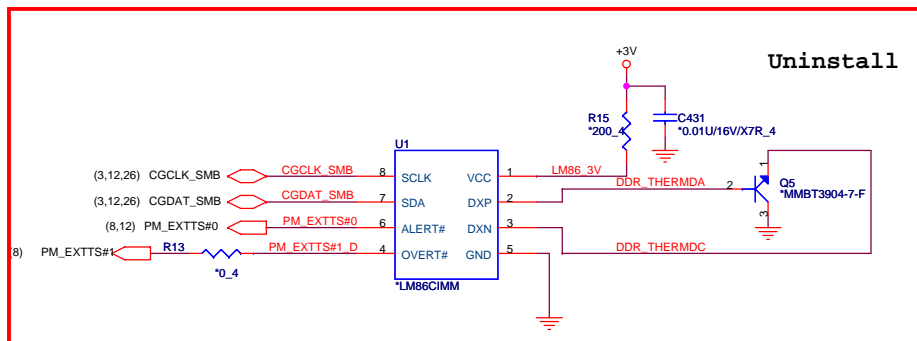
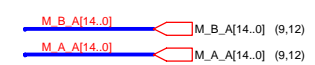
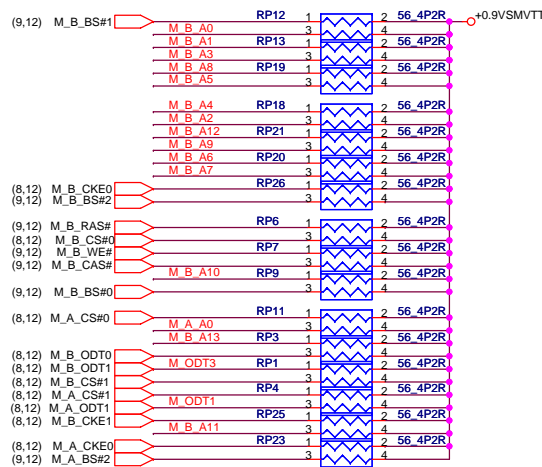
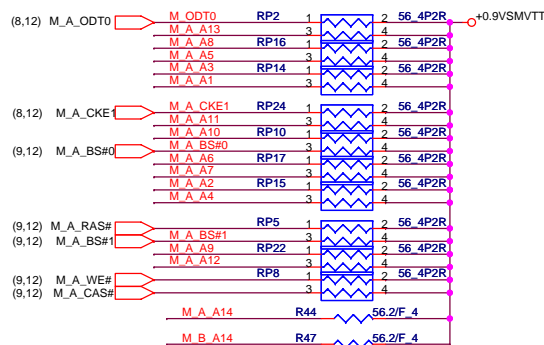
DDRII A CHANNEL

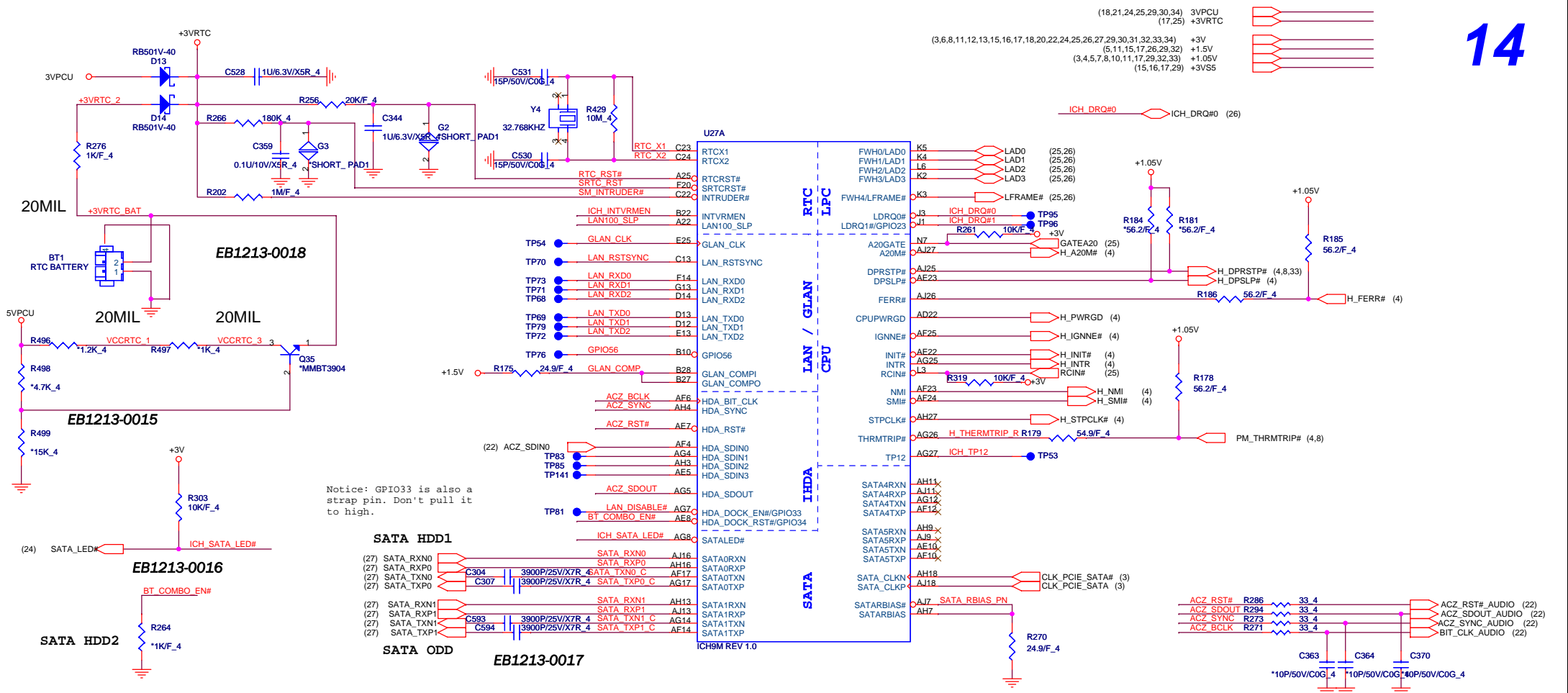


DDRII B CHANNEL



Layout note: Place one cap close to every 2 pullup resistors terminated to SMDR_VTERM





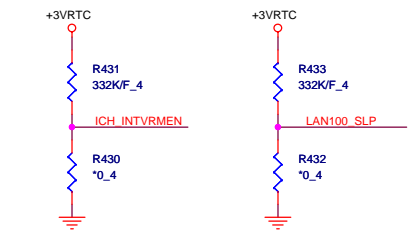
Notice: GPIO33 is also a strap pin. Don't pull it to high.

SB Strap

ICH9-M Internal VR Enable strap
(Internal VR for VccSus1_05, VccSus1_5 and VccCL1_5)

ICH9-M LAN100_SLP Strap
(Internal VR for VccLAN1_05 and VccCL1_05)

INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)
LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)



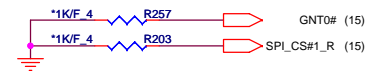
XOR Chain Entrance Strap

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCIe port config bit 1

ICH9 Boot BIOS select

STRAP	PCI_GNT0#	SPL_CS#1
SPI	0	1
PCI	1	0
LPC	1	1

(default)

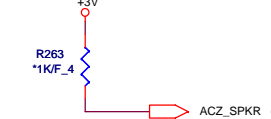


A16 swap override strap

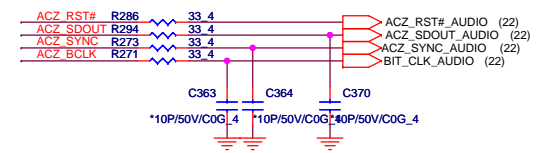
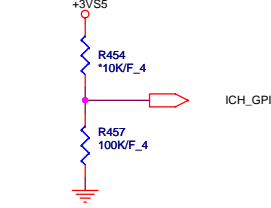
PCI_GNT#3	Low = A16 swap override enabled Hi = Default
-----------	---



No Reboot Strap	
ACZ_SPKR	Low: Default Hi: No reboot



TPM physical presence	
ICH_GPIO57	Low: Default



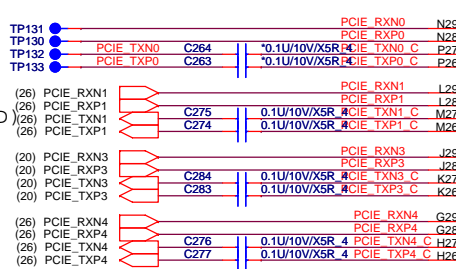
EC0225-0002

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Quanta Computer Inc.

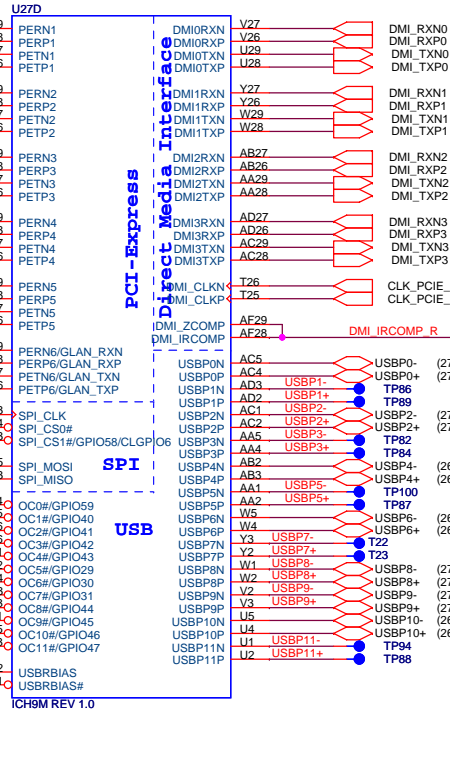
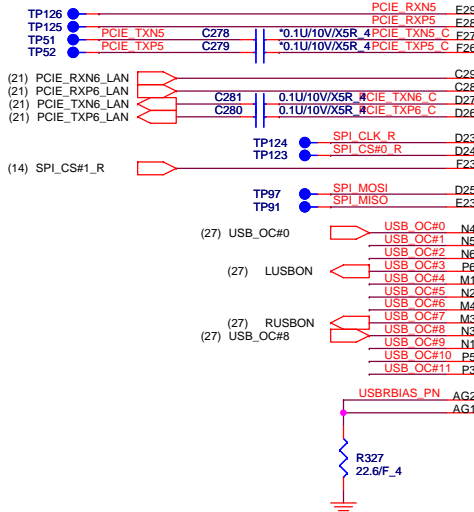
Size	Document Number	Rev
Custom	ICH9M Host 1/4	1A
Date:	Friday, May 02, 2008	Sheet 14 of 34



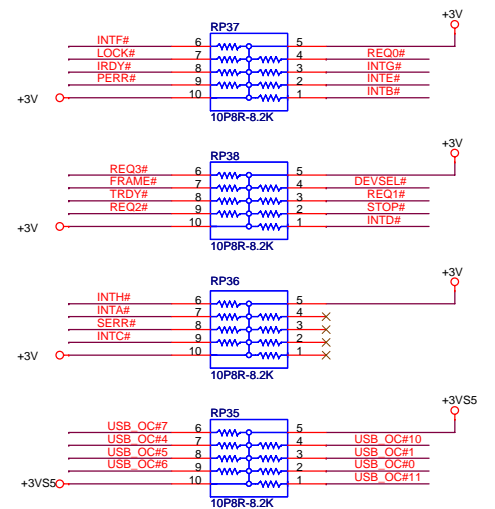
EC0225-0004



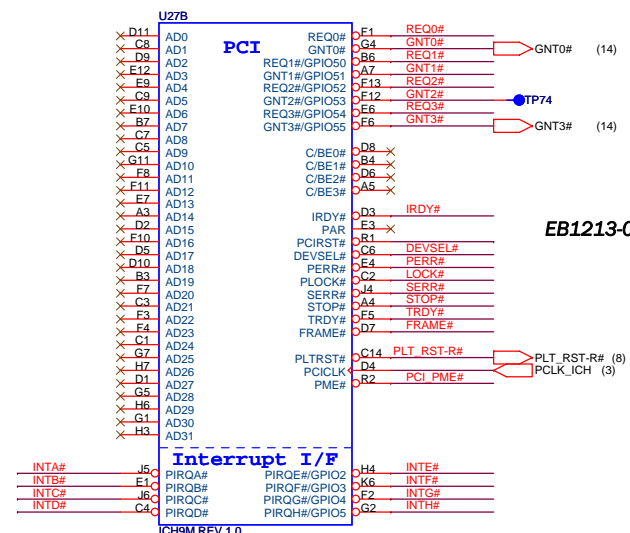
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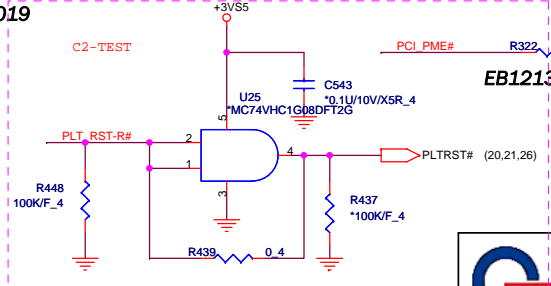
- USB Connector
- CCD Connector
- BLUETOOTH
- NEW CARD
- USB Connector
- USB Connector
- WLAN



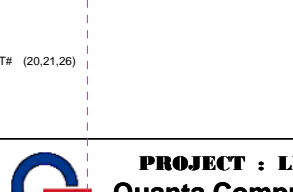
LE6B: Delete HDMI SPI flash IC and relate circuit
 2008-4-24



EB1213-0019

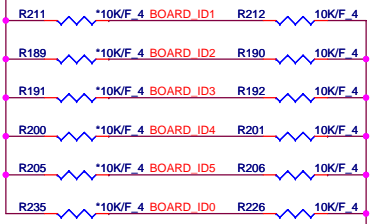
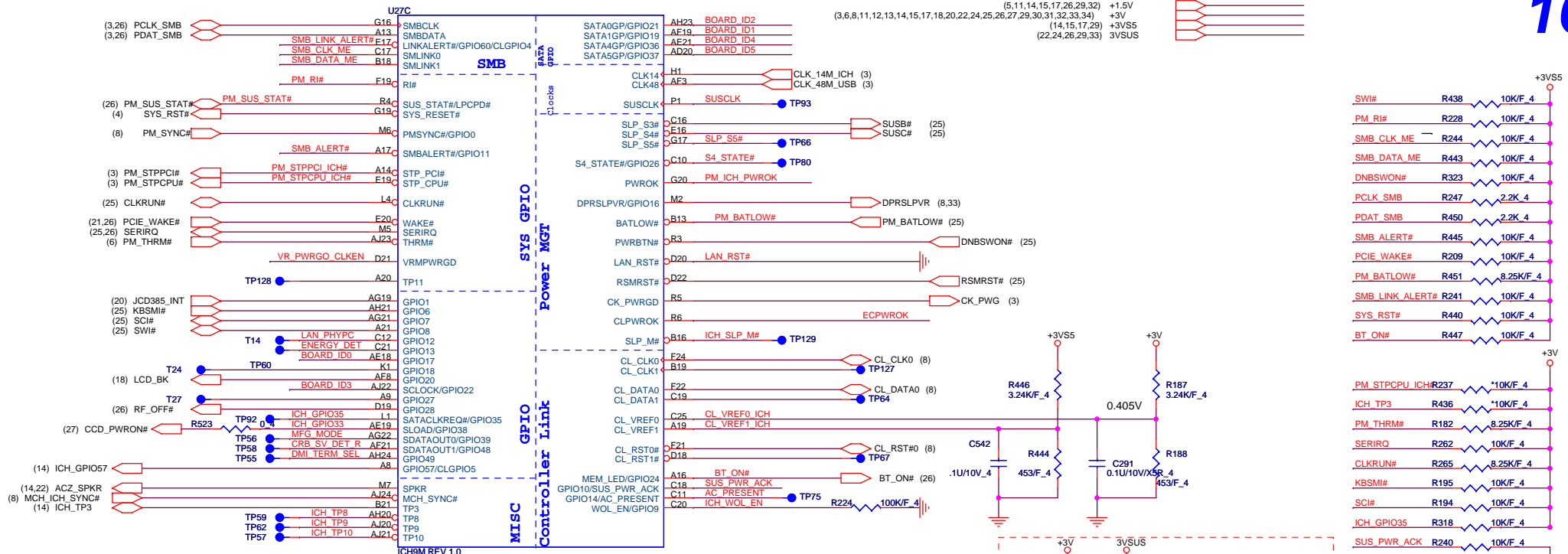


EB1213-0020



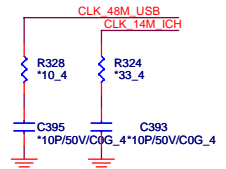
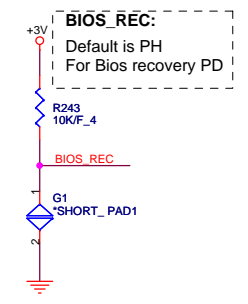
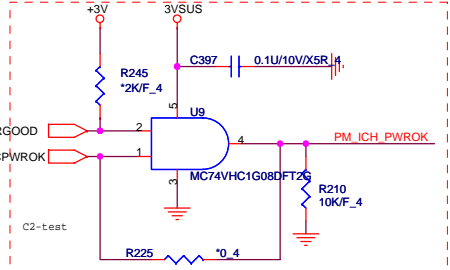
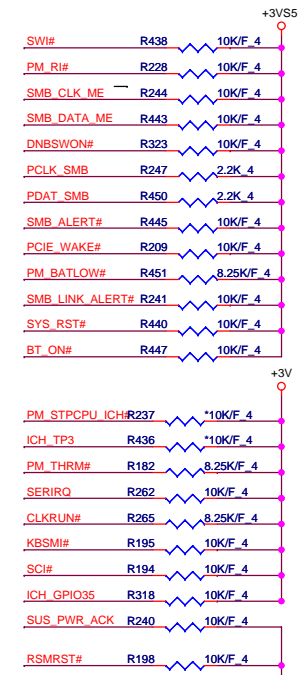
PROJECT : LE6
Quanta Computer Inc.

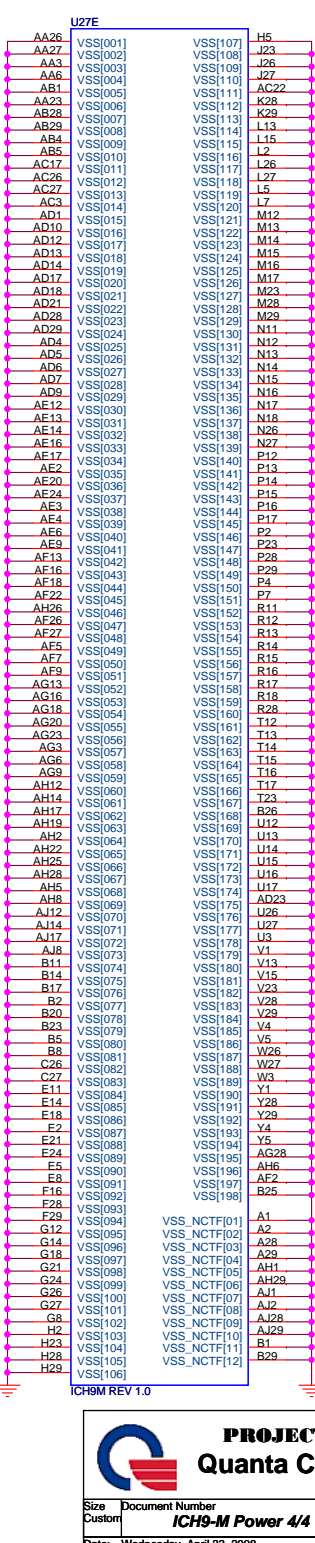
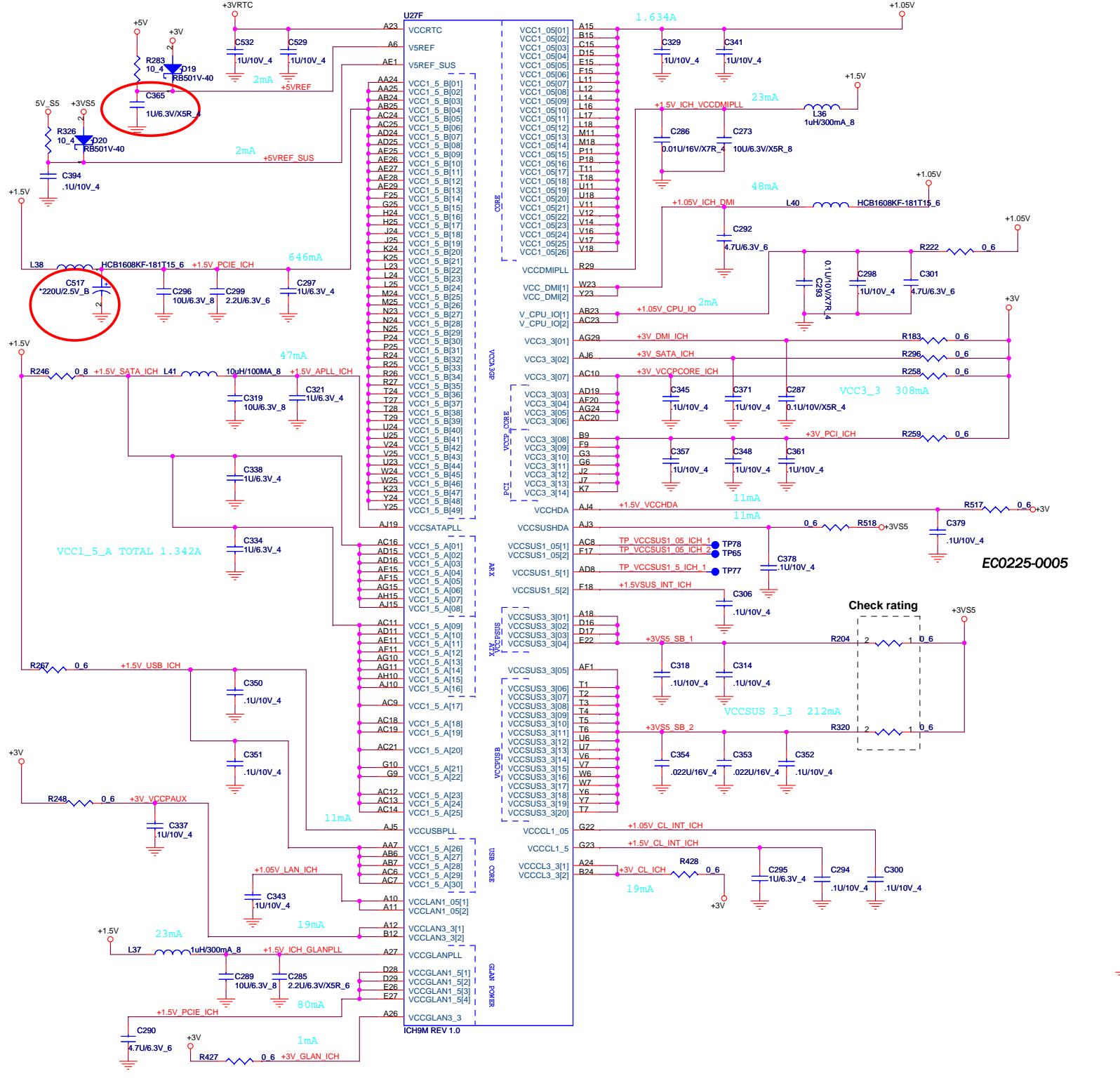
Size: Custom Document Number: ICH9-M PCIE 2/4 Rev: 1A
 Date: Friday, May 02, 2008 Sheet: 15 of 34



BOARD_ID0 GPIO17	BOARD_ID1 GPIO19	BOARD_ID2 GPIO21	BOARD_ID3 GPIO22	BOARD_ID4 GPIO36	BOARD_ID5 GPIO37	
L	L	L	L	L	L	LE6 (GPIO36/GPIO37)
L	L	L	L	H	L	LE7 (GPIO36/GPIO37)

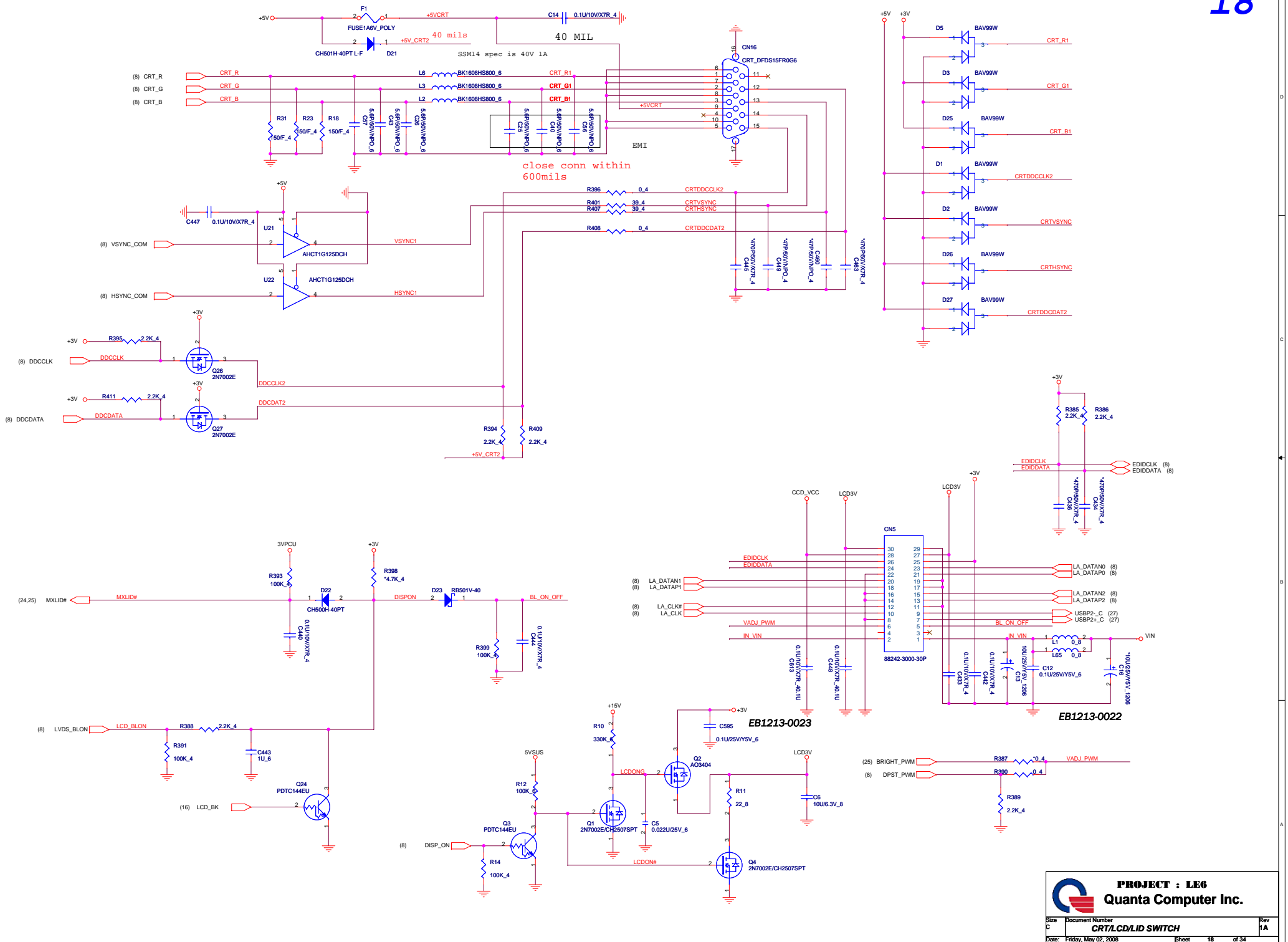
EB1213-0004



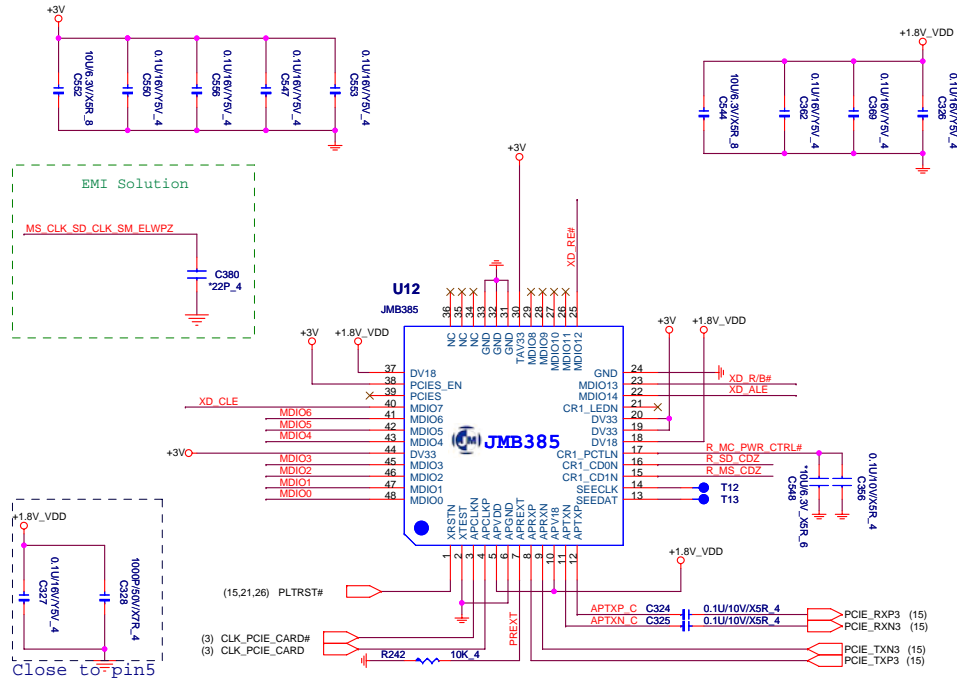


AA26	VSS107	H5
AA27	VSS108	J23
AA3	VSS109	J26
AA6	VSS110	J27
AA1	VSS111	K22
AA23	VSS112	K28
AB28	VSS113	L1
AB29	VSS114	L13
AB5	VSS115	L2
AB4	VSS116	L25
AB6	VSS117	L26
AC17	VSS118	L27
AC26	VSS119	L5
AC27	VSS120	L7
AC3	VSS121	L12
AD10	VSS122	M12
AD12	VSS123	M14
AD13	VSS124	M15
AD14	VSS125	M16
AD17	VSS126	M17
AD18	VSS127	M23
AD21	VSS128	M28
AD28	VSS129	M29
AD9	VSS130	N11
AD5	VSS131	N13
AD6	VSS132	N14
AD7	VSS133	N15
AD9	VSS134	N16
AE12	VSS135	N17
AE13	VSS136	N18
AE14	VSS137	N19
AE16	VSS138	N26
AE17	VSS139	N27
AE2	VSS140	P12
AE20	VSS141	P13
AE24	VSS142	P14
AE3	VSS143	P15
AE4	VSS144	P16
AE6	VSS145	P2
AE9	VSS146	P23
AF13	VSS147	P28
AF16	VSS148	P29
AF18	VSS149	P4
AF22	VSS150	P7
AH26	VSS151	R11
AF26	VSS152	R12
AF27	VSS153	R13
AF5	VSS154	R14
AF7	VSS155	R15
AF9	VSS156	R16
AG13	VSS157	R17
AG16	VSS158	R18
AG18	VSS159	R28
AG20	VSS160	R28
AG23	VSS161	T13
AG3	VSS162	T14
AG6	VSS163	T15
AG9	VSS164	T16
AH12	VSS165	T23
AH14	VSS166	T27
AH17	VSS167	B26
AH19	VSS168	B26
AH22	VSS169	U13
AH25	VSS170	U14
AH28	VSS171	U15
AH5	VSS172	U16
AH8	VSS173	U17
AH12	VSS174	AD23
AH14	VSS175	U26
AH17	VSS176	U27
AH19	VSS177	U3
AJ8	VSS178	U3
B11	VSS179	V1
B14	VSS180	V15
B17	VSS181	V23
B23	VSS182	V28
B2	VSS183	V29
B20	VSS184	V4
B23	VSS185	V5
B5	VSS186	V6
B8	VSS187	W26
C26	VSS188	W27
C27	VSS189	W3
E11	VSS190	Y1
E14	VSS191	Y28
E18	VSS192	Y29
E2	VSS193	Y4
E21	VSS194	Y5
E24	VSS195	AC28
E5	VSS196	AH6
E8	VSS197	AF2
F16	VSS198	B25
F28	VSS199	A1
F29	VSS200	A2
G12	VSS_NCTF[01]	A28
G14	VSS_NCTF[02]	A29
G18	VSS_NCTF[03]	A29
G21	VSS_NCTF[04]	AH1
G24	VSS_NCTF[05]	AH29
G26	VSS_NCTF[06]	AJ1
G27	VSS_NCTF[07]	AJ28
G8	VSS_NCTF[08]	AJ29
H2	VSS_NCTF[09]	AJ28
H23	VSS_NCTF[10]	B1
H28	VSS_NCTF[11]	B29
H29	VSS_NCTF[12]	B29

CRT PORT



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NUMBER SAME AS DISCRETE**



CARDREADER POWER

Memory Card Power Supply

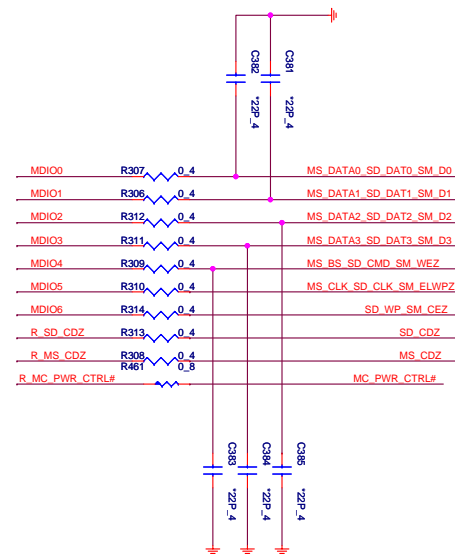
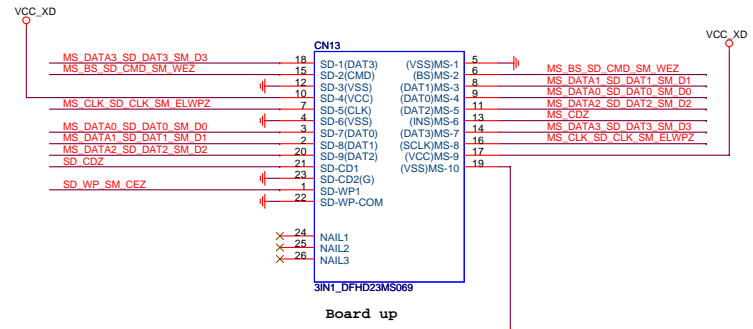
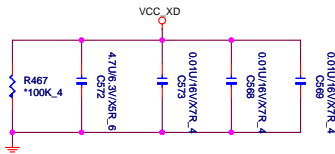
EB1213-0025

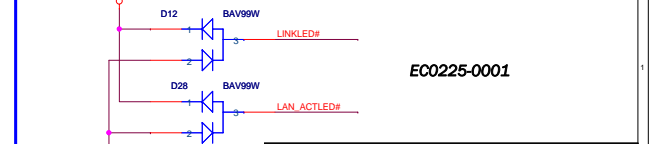
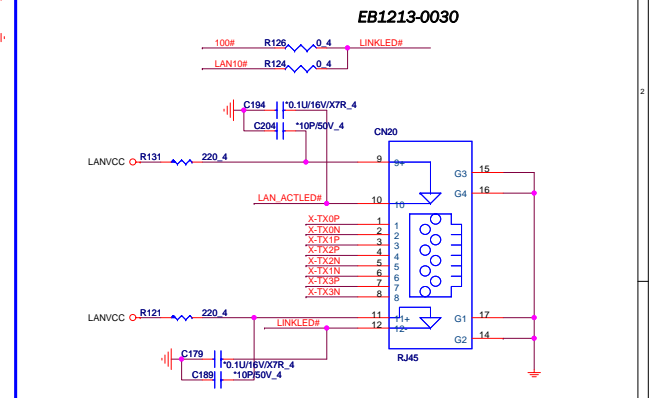
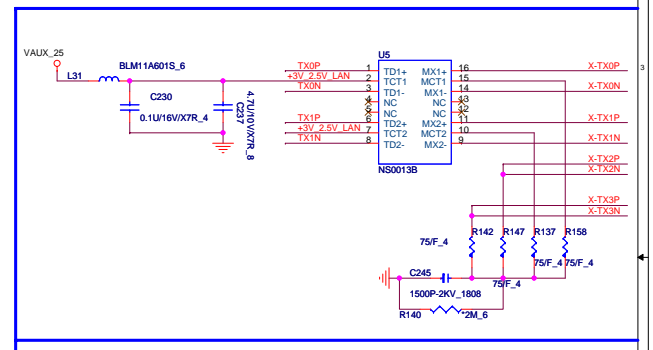
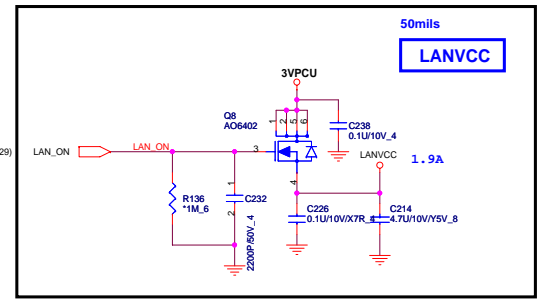
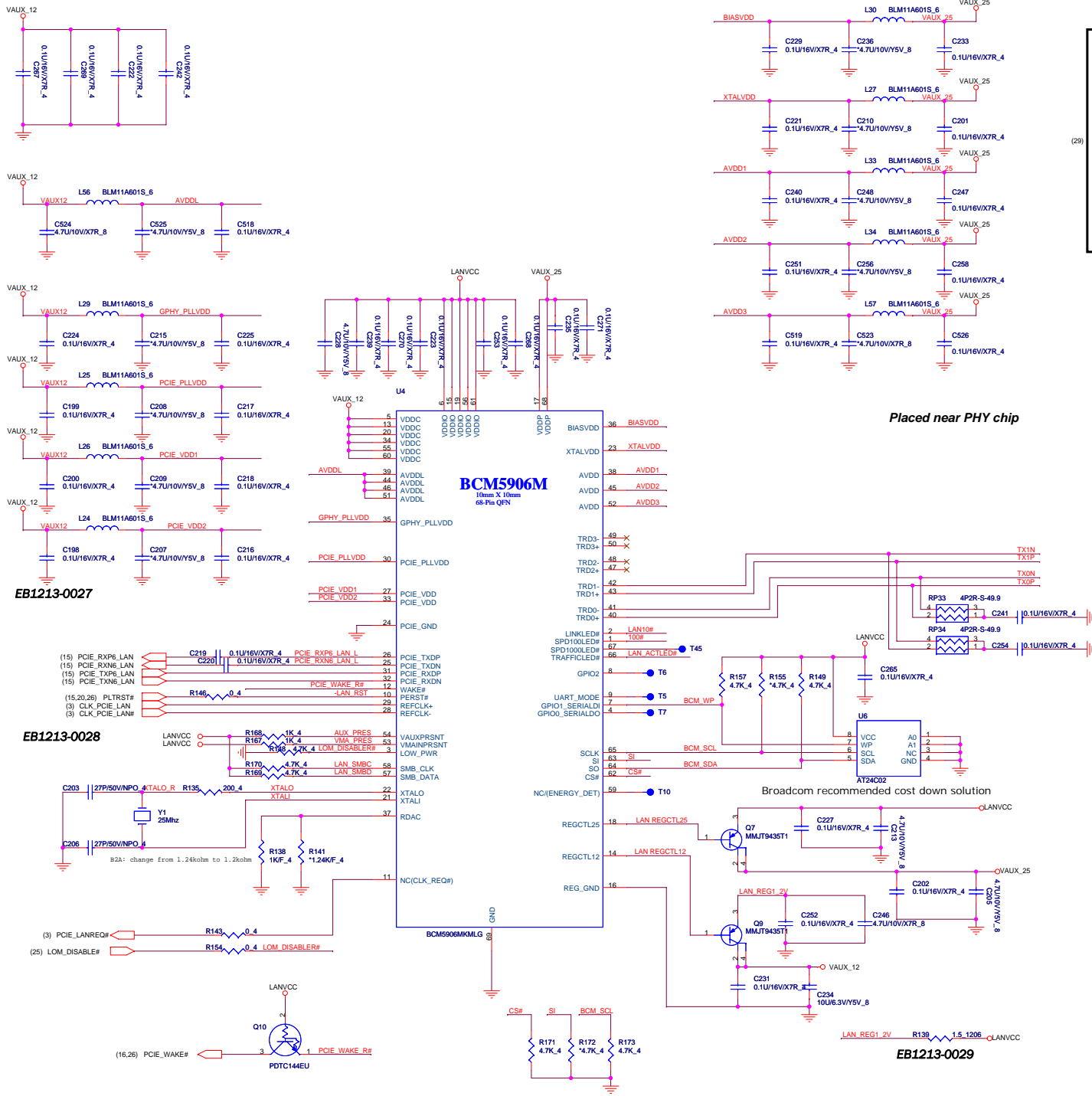


Use 0805 type and over 20 mils trace width on both side

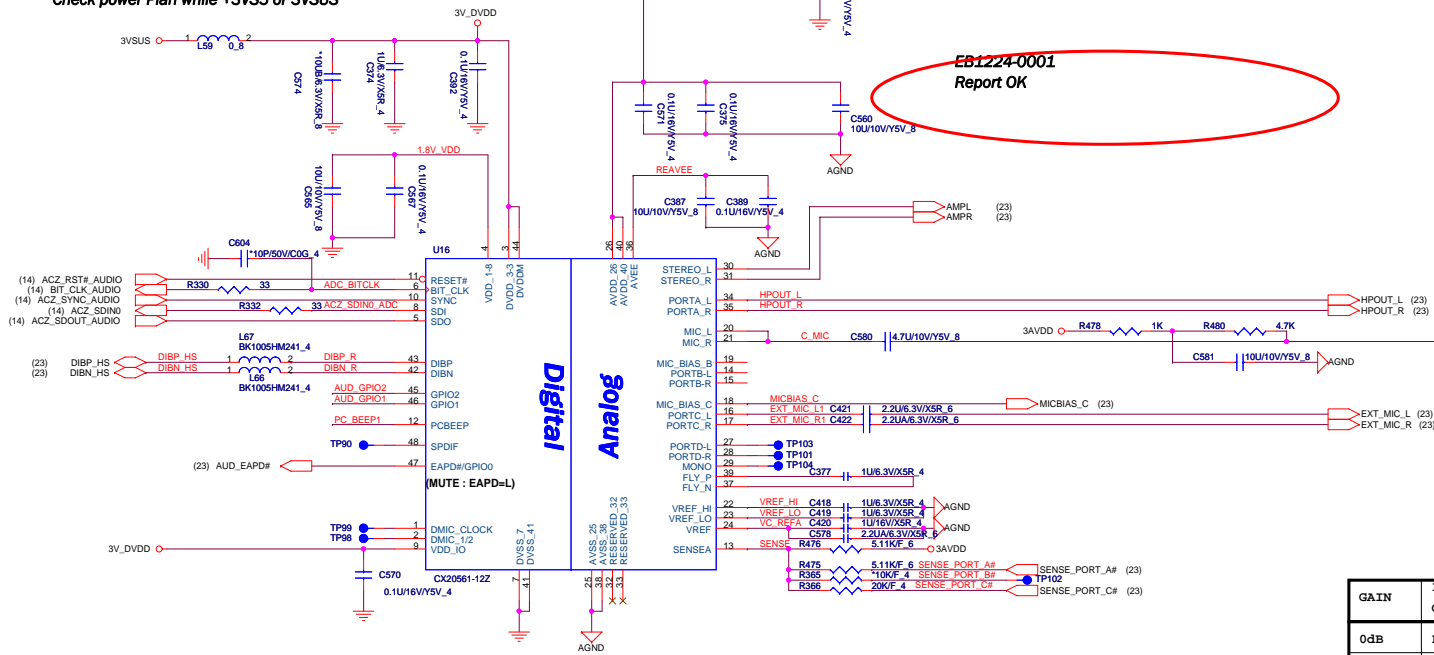
EB1213-0026

DEL some parts for Q32 R469 C577





EB1213-0031
Check power Plan while +3VS5 or 3VSUS



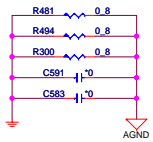
EB1213-0032

Check power Plan while +1.5VS5 or 1.5VSUS

GAIN	10K GPIO RESISTORS	GPIO1	GPIO2
0dB	Populate	Populate	Populate
-6dB	Omit	Omit	Omit
-12dB	Populate	Omit	Omit
-16dB	Omit	Populate	Omit

STEREO	INTERNAL SPEAKERS
PORT-A	EXTERNAL HEAD-PHONE
MIC	INTERNAL MIC
PORT-B	EXTERNAL MIC

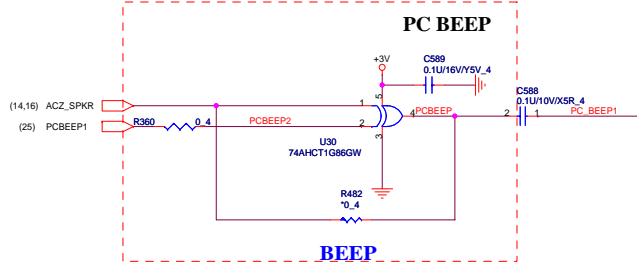
FOR EMI SOLUTION



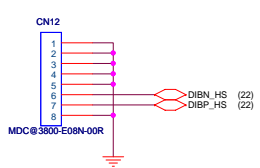
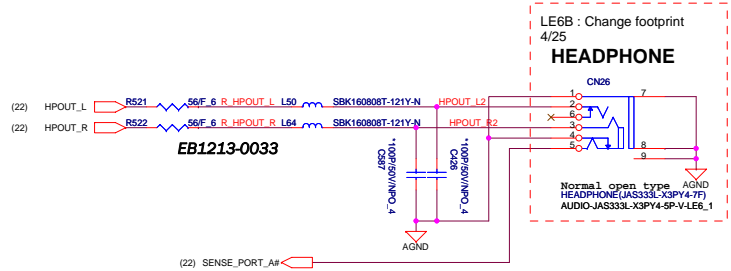
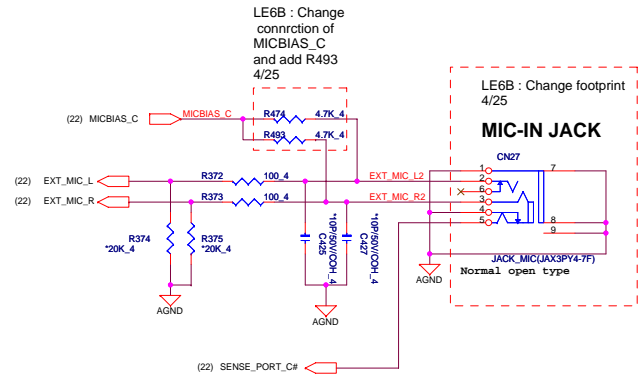
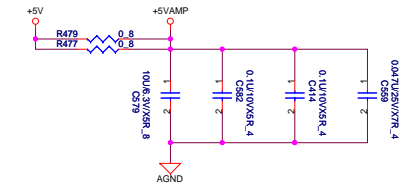
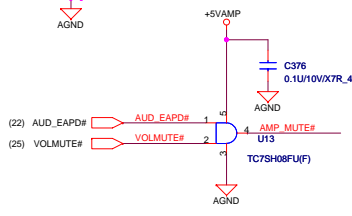
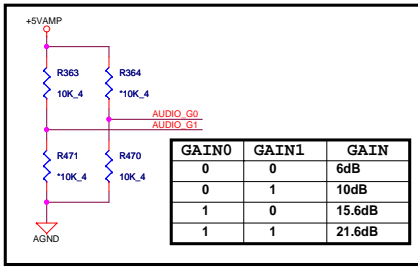
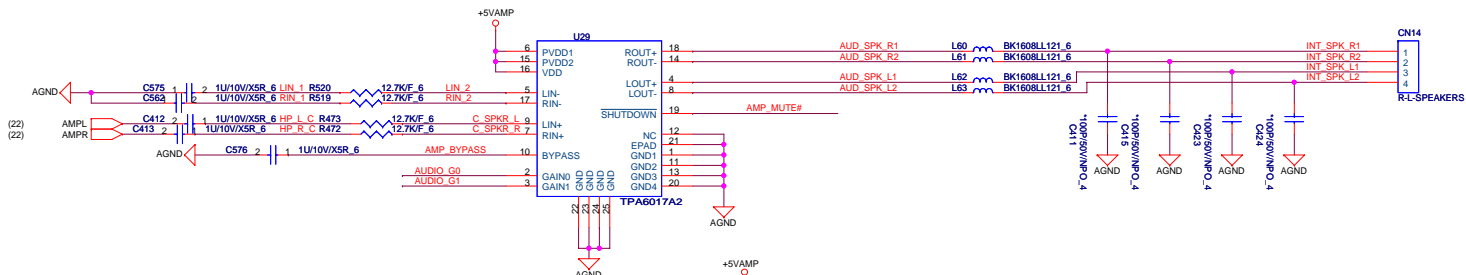
Default gain is -6dB without populating the 10K ohm pull down resistors going to GPIO1 and GPIO2



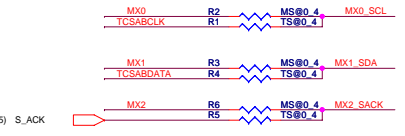
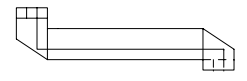
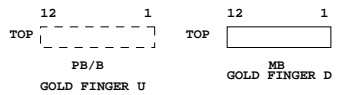
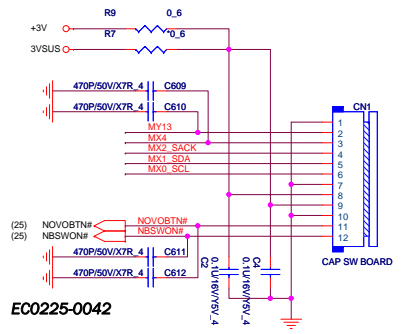
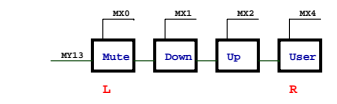
LE6B: Add R360 and change U30 to OR gate base on customer request



INTERNAL SPEAKER AMPLIFIER

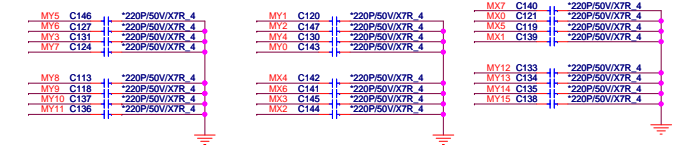
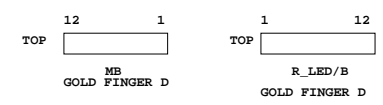
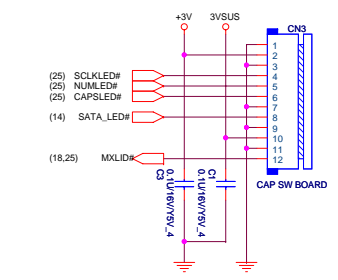
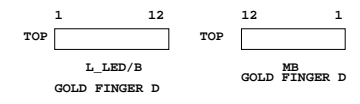
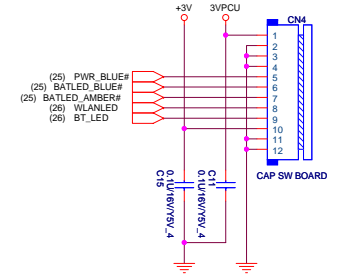
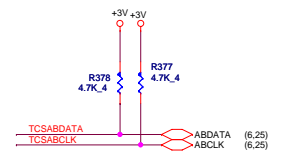


Modem connector

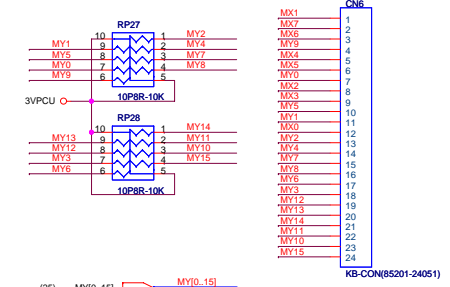


check EC and Vendor for CTS

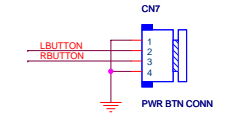
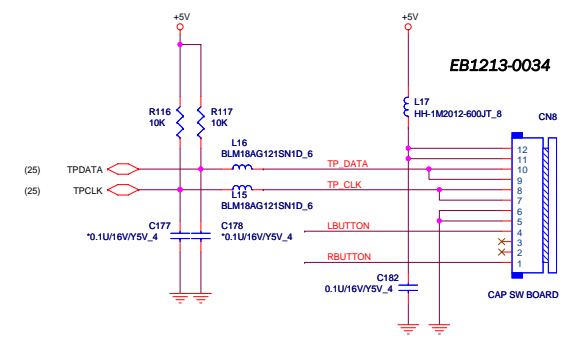
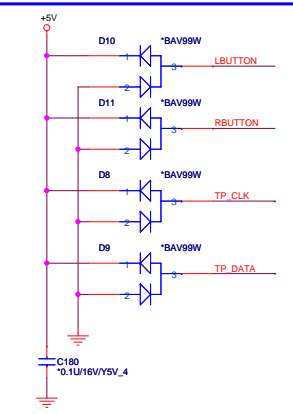
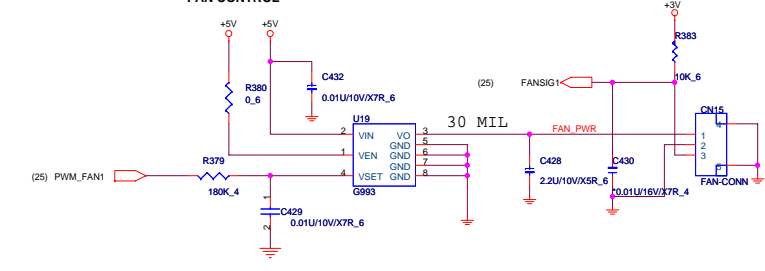
EB1213-0022



KEYBOARD PULL-UP



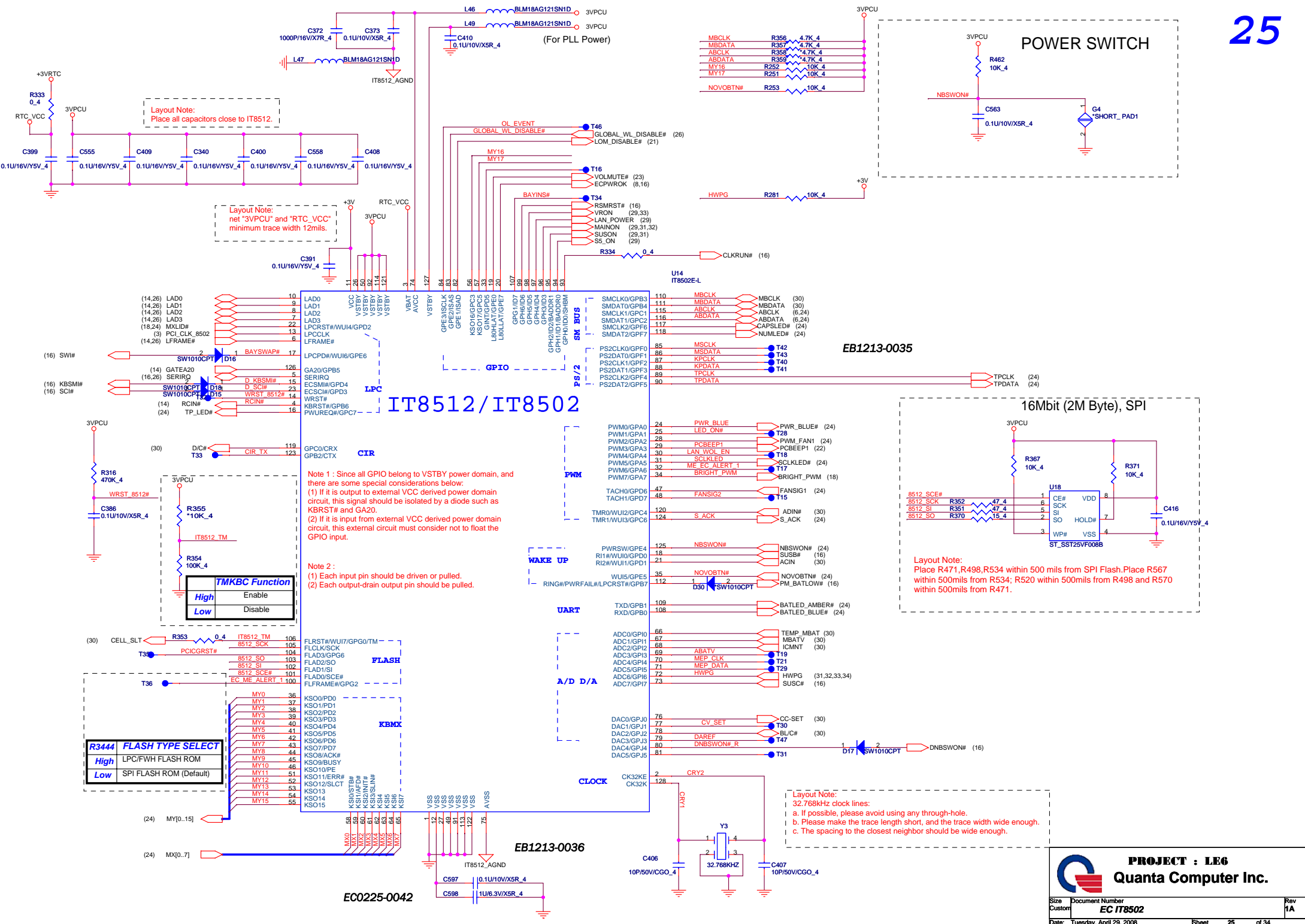
FAN CONTROL



EB1213-0034

PROJECT : LEG
Quanta Computer Inc.

Size C Document Number **KEYBOARD/FAN** Rev 1A
 Date: Tuesday, April 26, 2006 Sheet 24 of 34



Layout Note:
Place all capacitors close to IT8512.

Layout Note:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.

Note 1 : Since all GPIO belong to VSTBY domain, and there are some special considerations below:
 (1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
 (2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.

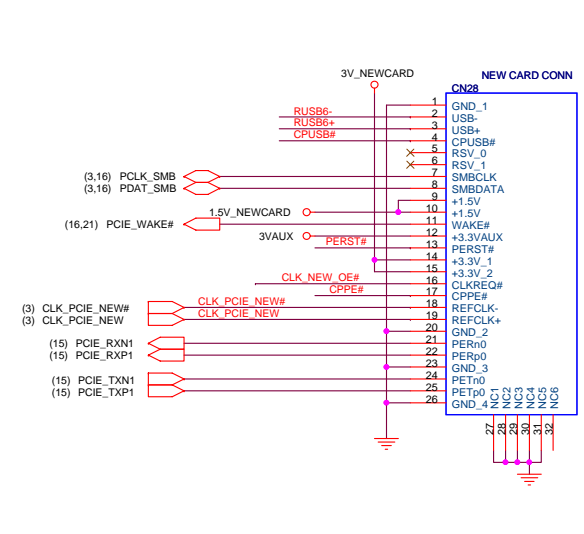
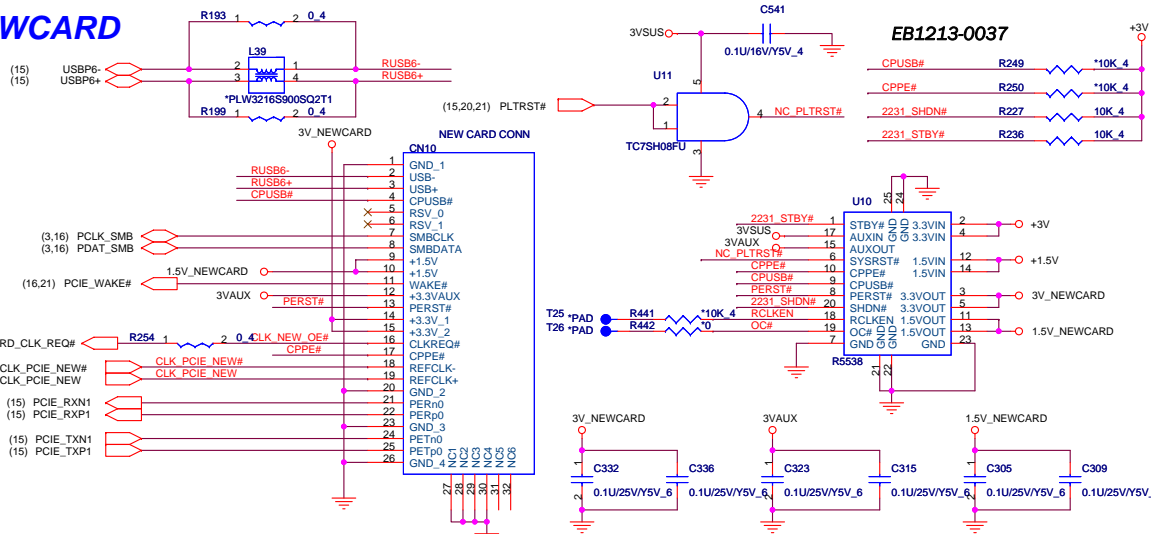
Note 2 :
 (1) Each input pin should be driven or pulled.
 (2) Each output-drain output pin should be pulled.

TMKBC Function	
High	Enable
Low	Disable

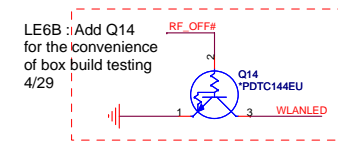
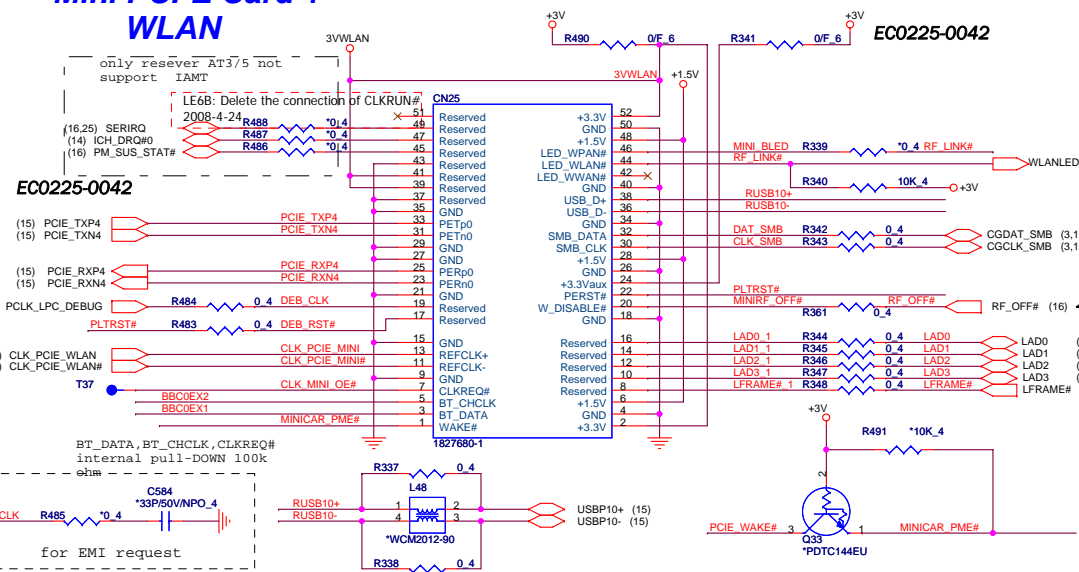
R3444 FLASH TYPE SELECT	
High	LPC/FWH FLASH ROM
Low	SPI FLASH ROM (Default)

Layout Note:
Place R471,R498,R534 within 500 mils from SPI Flash. Place R567 within 500mils from R534; R520 within 500mils from R498 and R570 within 500mils from R471.

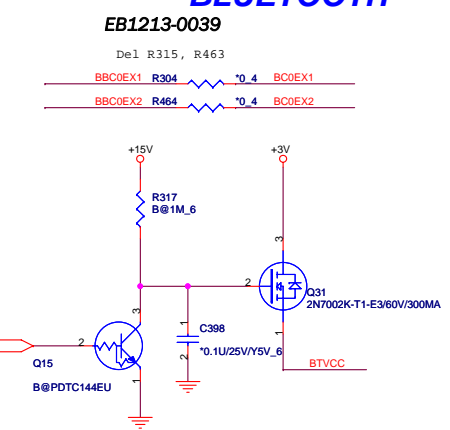
Layout Note:
32.768kHz clock lines:
 a. If possible, please avoid using any through-hole.
 b. Please make the trace length short, and the trace width wide enough.
 c. The spacing to the closest neighbor should be wide enough.



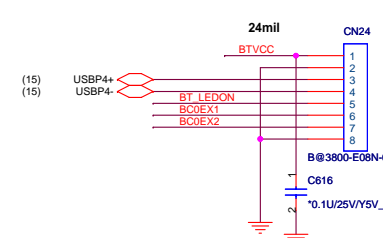
Mini PCI-E Card 1 WLAN



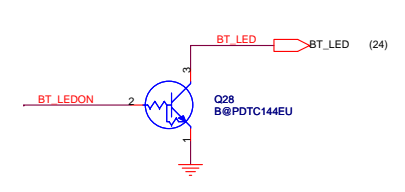
BLUETOOTH



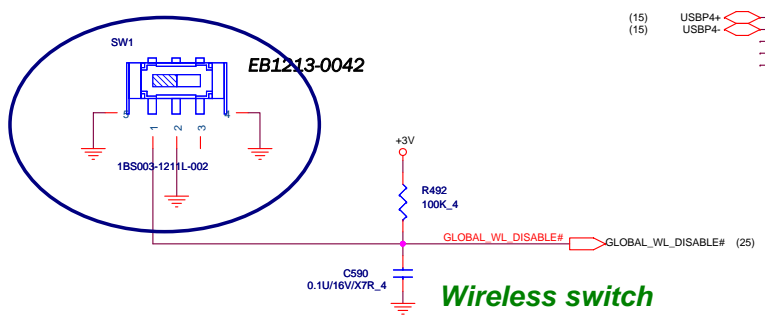
EB1213-0038



EB1213-0041



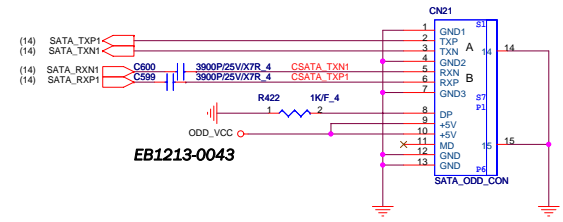
EB1213-0042



Wireless switch

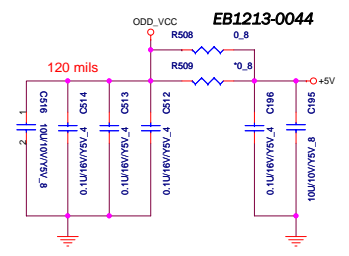
PROJECT : LE6
Quanta Computer Inc.

SATA CD-ROM



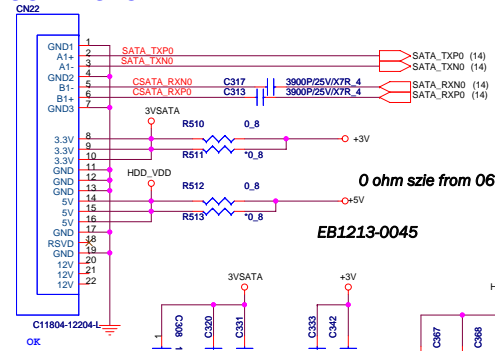
EB1213-0043

0 ohm szle from 0603 to 0805



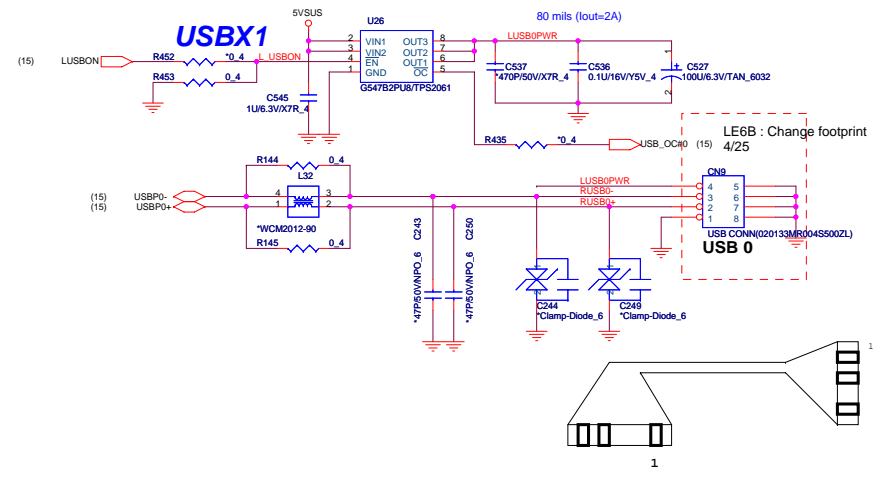
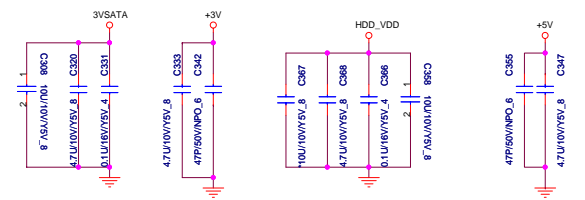
EB1213-0044

SATA_1 CONNECTOR



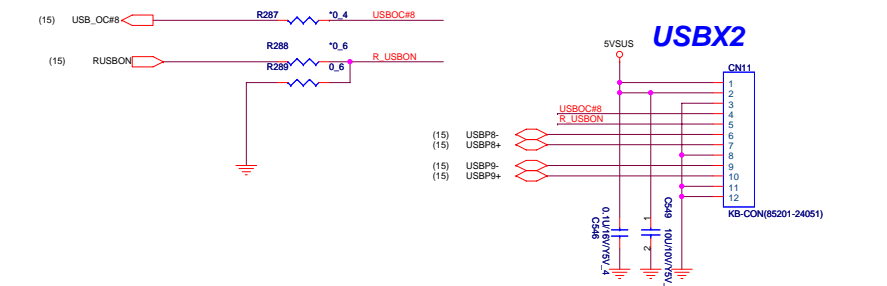
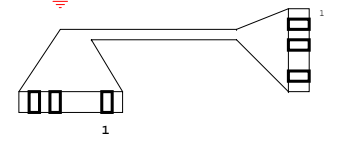
0 ohm szle from 0603 to 0805

EB1213-0045



LE6B : Change footprint 4/25

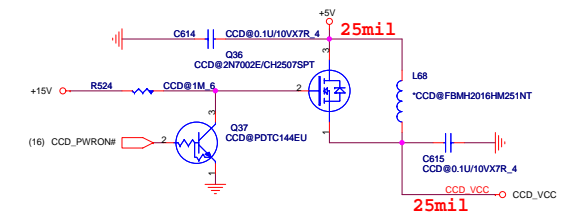
USB CONN(020133MR044S002L)



USBX2

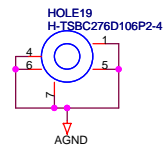
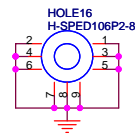
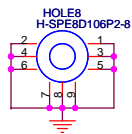
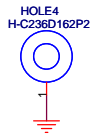
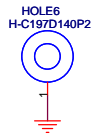
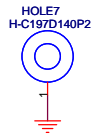
KB-CON(85201-24051)

CCD MODULE

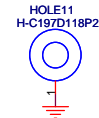
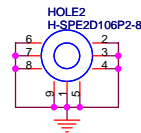
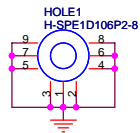
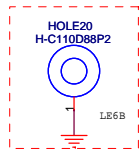
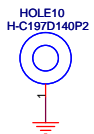
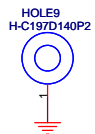


25mil

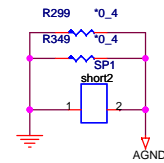
CCD_PWRON#	High	Low
	Disable	Enable



TOP FAN

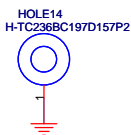
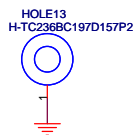


EB1213-0019

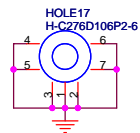
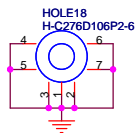


CPU

EB1221-0001



MINI-PCie



RSPKR

RSPKL

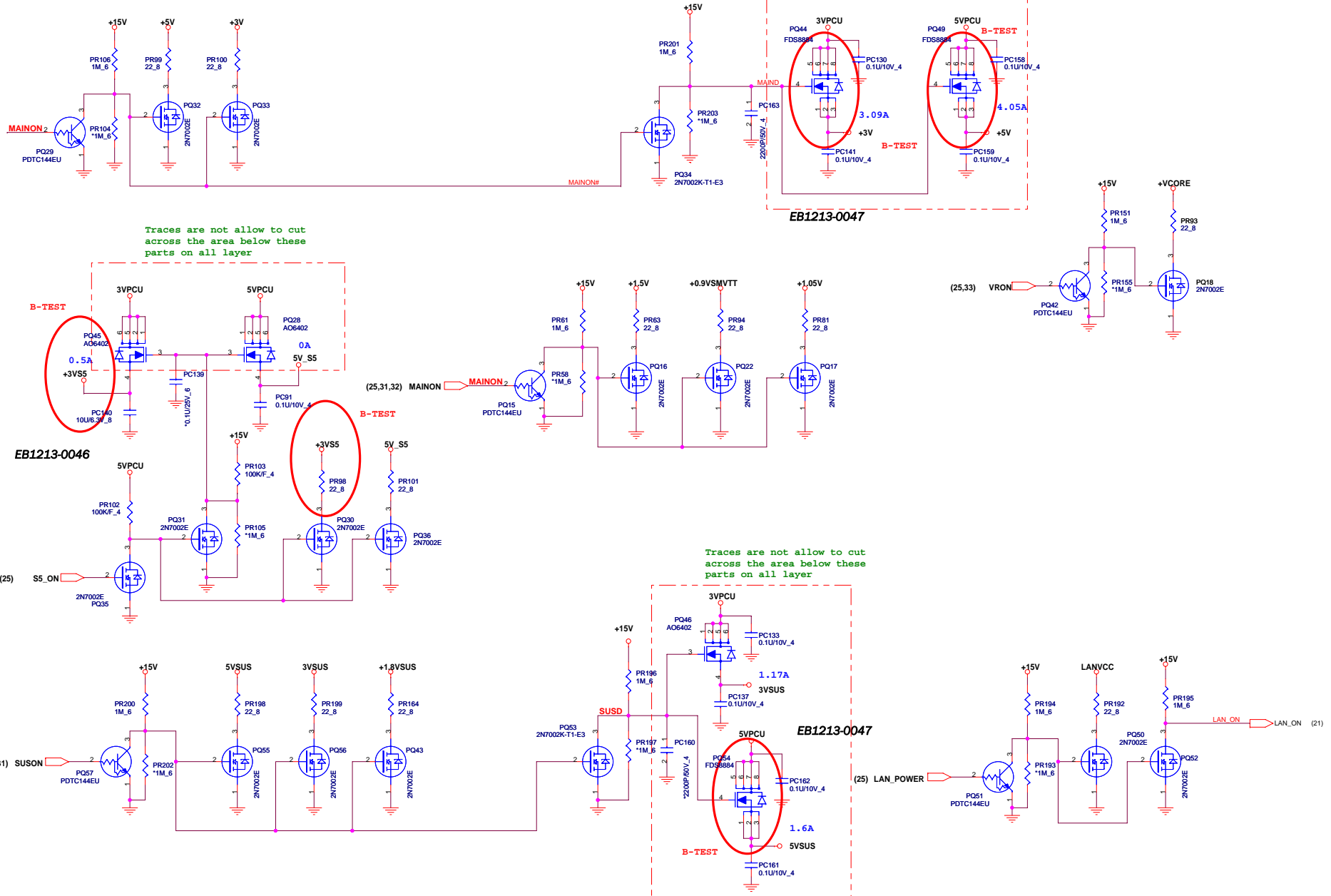
BOT NB

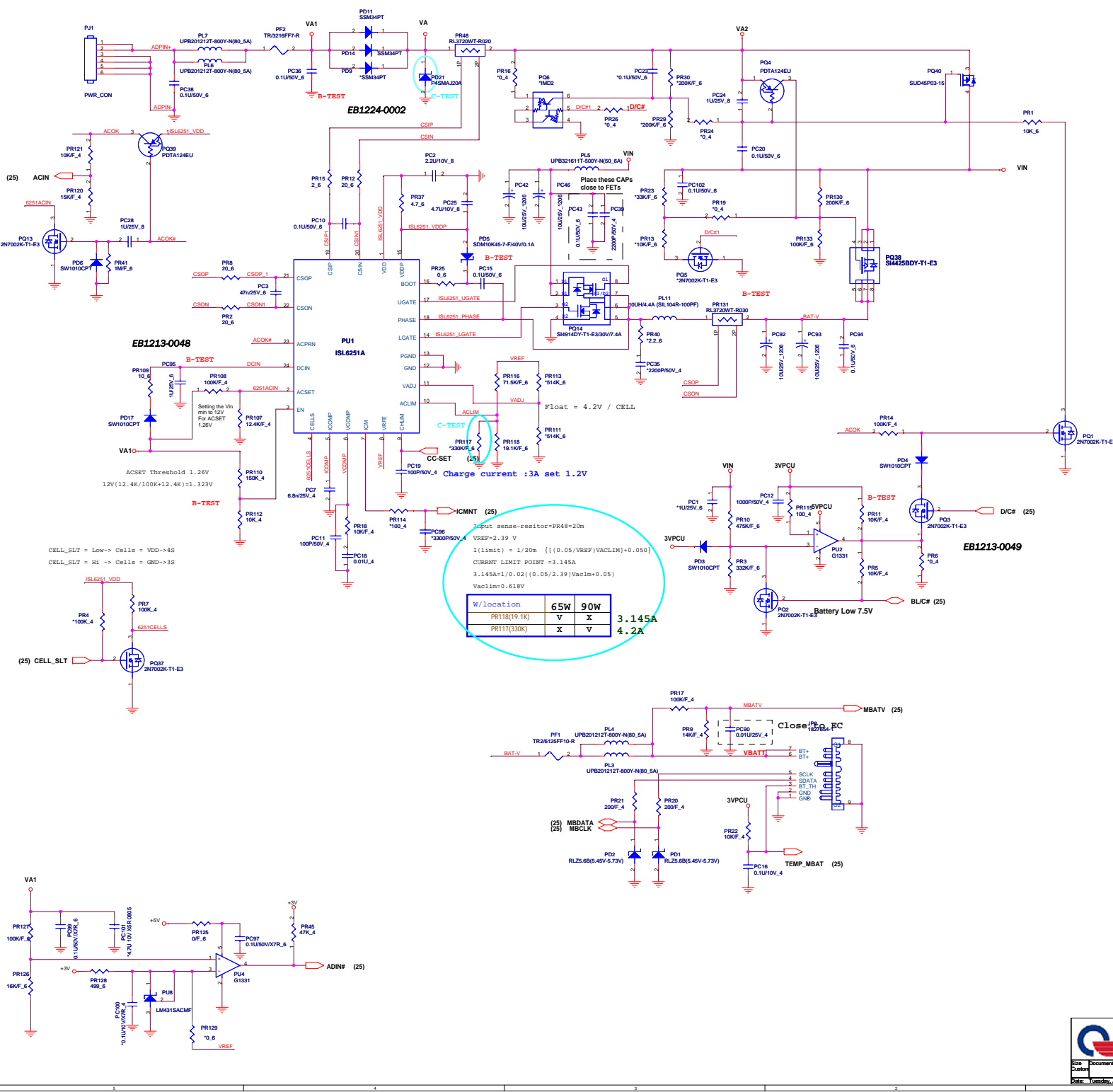
USB
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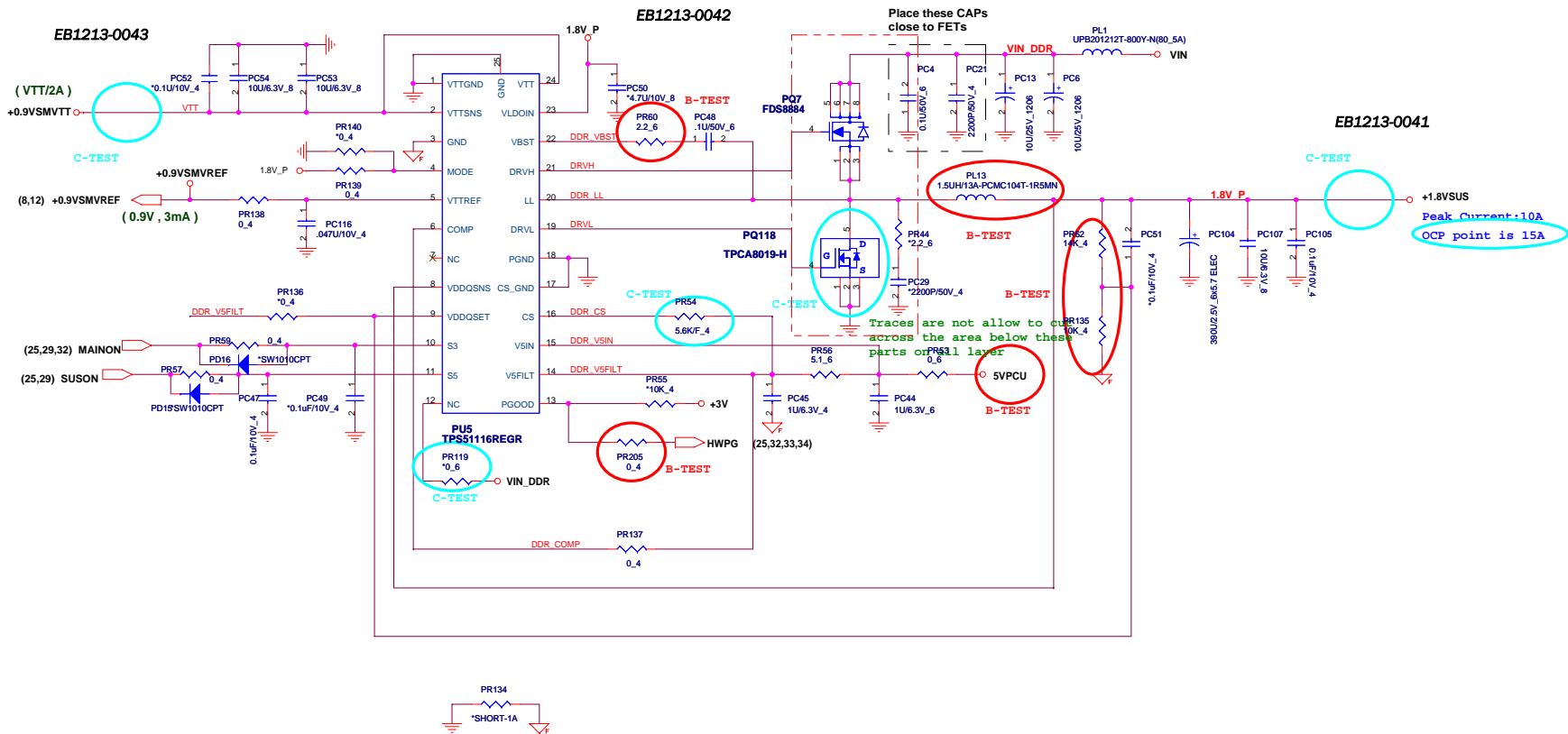
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		Quanta Computer Inc.	
Size Custom	Document Number EMI PAD/SCREW/DEBUG PORT	Date: Friday, May 02, 2008	Rev 1A
		Sheet 28	of 34

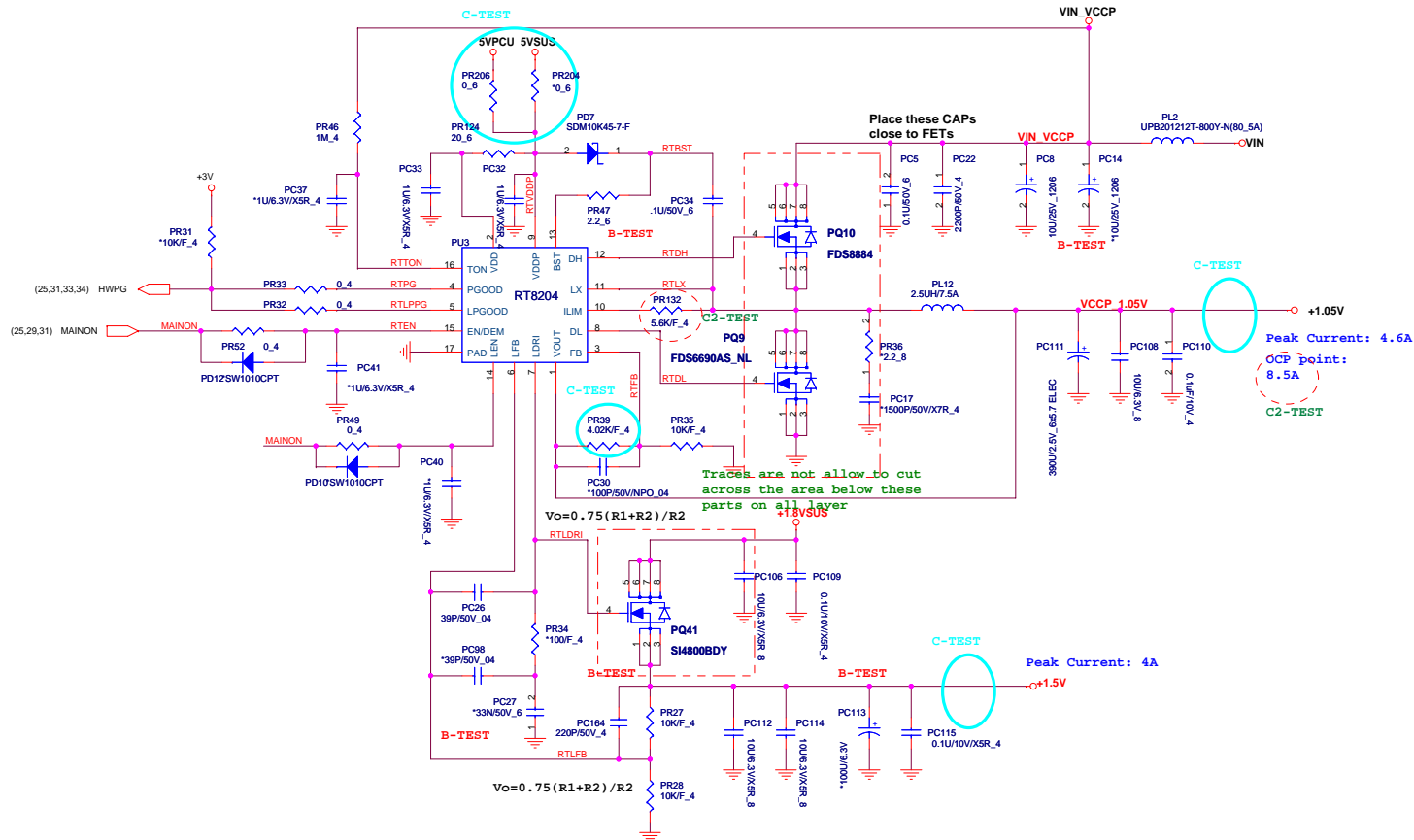
DISCHARGE

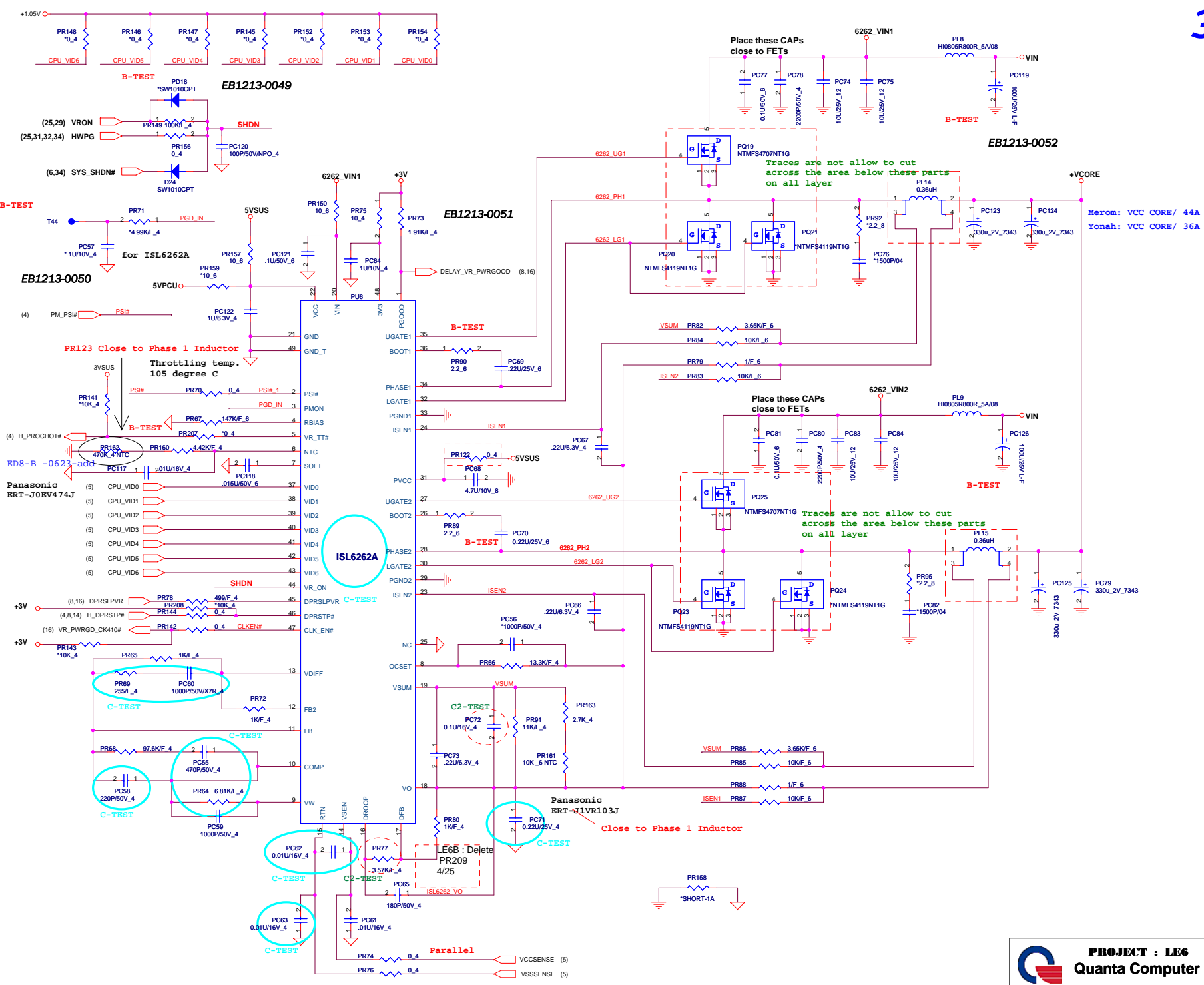
Traces are not allow to cut across the area below these parts on all layer











Merom: VCC_CORE/ 44A
 Yonah: VCC_CORE/ 36A

DC/DC 3VPCU/5VPCU/+15V

Ton:OUT1/OUT2 Switching Frequency
 VCC: 200kHz/300kHz
 OPEN (REF): 400kHz/300kHz
 GND: 400kHz/500kHz

