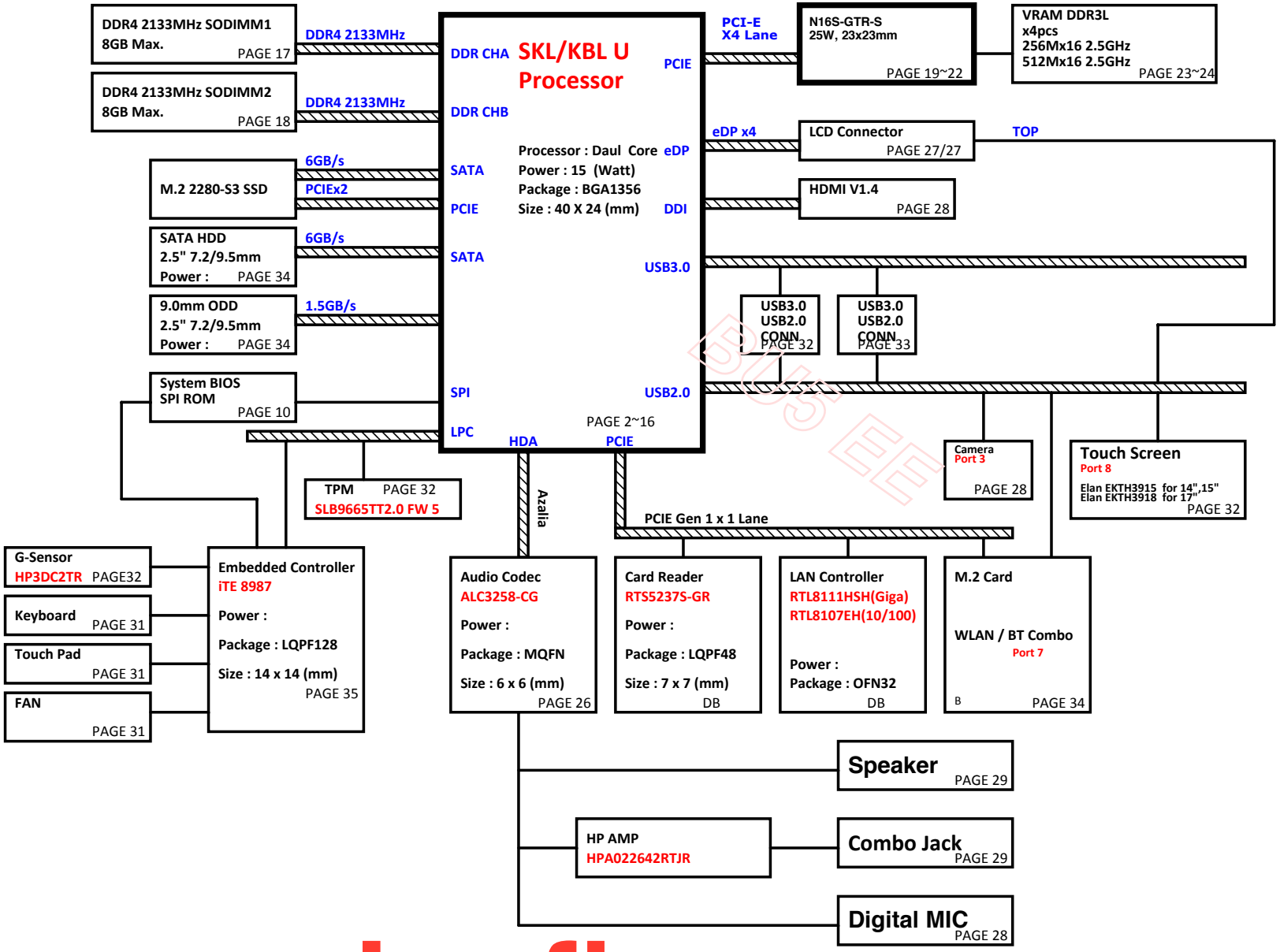
Dessert DIS (15")
Intel SKL/KBL ULT Platform Block Diagram

PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT



BU5

PROJECT : G34A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	1A

Date: Tuesday, January 05, 2016 Sheet 1 of 47

need surport to UHD 3840x2160

02

+3V [4,10,11,12,13,14,15,16,17,18,19,20,21,25,26,27,28,29,30,31,32,33,39,43,44,47]
+1.0V [4,6,16,33,38]
+VCCSTPLL [4,5,6,9,38,39]

HDMI

Need apply PN

U1A SKL_ULT ?

[27] IN_D2# → E55 DDI1_TXN[0]
[27] IN_D2 → F55 DDI1_TXP[0]
[27] IN_D1# → E58 DDI1_TXN[1]
[27] IN_D1 → F58 DDI1_TXP[1]
[27] IN_D0# → F53 DDI1_TXN[2]
[27] IN_D0 → G53 DDI1_TXP[2]
[27] IN_CLK# → F56 DDI1_TXN[3]
[27] IN_CLK → G56 DDI1_TXP[3]

C50 DDI2_TXN[0]
D50 DDI2_TXP[0]
C52 DDI2_TXN[1]
D52 DDI2_TXP[1]
A50 DDI2_TXN[2]
B50 DDI2_TXP[2]
D51 DDI2_TXN[3]
C51 DDI2_TXP[3]

DDI

[27] SDVO_CLK → L13 GPP_E18/DDPB_CTRLCLK
[27] SDVO_DATA → L12 GPP_E19/DDPB_CTRLDATA

TP2 DDPC_CTRLDATA → N7 GPP_E20/DDPC_CTRLCLK
N8 GPP_E21/DDPC_CTRLDATA

TP3 DDPD_CTRLDATA → N11 GPP_E22/DDPD_CTRLCLK
N12 GPP_E23/DDPD_CTRLDATA

+VCCIO → R3 24.9/F_4 EDP_RCOMP → E52 EDP_RCOMP

DISPLAY SIDEBANDS

EDP

EDP_TXN[0] → C47 INT_EDP_TXN0 → INT_EDP_TXN0 [25]
EDP_TXP[0] → C46 INT_EDP_TXP0 → INT_EDP_TXP0 [25]
EDP_TXN[1] → D46 INT_EDP_TXN1 → INT_EDP_TXN1 [25]
EDP_TXP[1] → C45 INT_EDP_TXP1 → INT_EDP_TXP1 [25]
EDP_TXN[2] → A45 INT_EDP_TXN2 → INT_EDP_TXN2 [25]
EDP_TXP[2] → B45 INT_EDP_TXP2 → INT_EDP_TXP2 [25]
EDP_TXN[3] → A47 INT_EDP_TXN3 → INT_EDP_TXN3 [25]
EDP_TXP[3] → B47 INT_EDP_TXP3 → INT_EDP_TXP3 [25]

EDP_AUXN → E45 INT_EDP_AUXN → INT_EDP_AUXN [25]
EDP_AUXP → F45 INT_EDP_AUXP → INT_EDP_AUXP [25]

EDP_DISP_UTIL → B52 EDP_DISP_UTIL → TP1

DDI1_AUXN → G50
DDI1_AUXP → F50
DDI2_AUXN → F48
DDI2_AUXP → F48
DDI3_AUXN → G46
DDI3_AUXP → F46

GPP_E13/DDPB_HPD0 → L9 HDMI_HPD_CON → HDMI_HPD_CON [27]
GPP_E14/DDPC_HPD1 → L7
GPP_E15/DDPD_HPD2 → L5
GPP_E16/DDPE_HPD3 → N9
GPP_E17/EDP_HPD → L10 ULT_EDP_HPD → ULT_EDP_HPD [25]

EDP_BKLTEN → R12 PCH_LVDS_BLON → PCH_LVDS_BLON [25]
EDP_BKLTCTL → R11 PCH_DPST_PWM → PCH_DPST_PWM [25]
EDP_VDDEN → U13 PCH_DISP_ON → PCH_DISP_ON [25]

*SKL_ULT
REV = 1

1 OF 20

?

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

Reserve EDP_HPD opposites circuit!

+3V
R1 *10K/F_4
ULT_EDP_HPD
R2 100K_4

U1D SKL_ULT ?

Need apply PN

[33,39,47] H_PROCHOT# → R4 499/F_4 → CATERR# D63
[33] EC_PECI → EC_PECI A51 PECI
PROCHOT# C55 PROCHOT#
[33] PM_THRMTRIP# → PM_THRMTRIP# C57 THERMTRIP#
A61 SKTOCC#

CPU MISC

[16] XDP_BPM0 → C55 BPM#[0]
[16] XDP_BPM1 → D55 BPM#[1]
B54 BPM#[2]
C56 BPM#[3]

TP113 3D_FW_GPIO_R → A6 GPP_E3/CPU_GP0
TP4 CPU_GP1 → A7 GPP_E7/CPU_GP1
TP5 CPU_GP2 → BA5 GPP_B3/CPU_GP2
TP6 CPU_GP3 → AY5 GPP_B4/CPU_GP3

R8 49.9/F_4 PROC_POPIRCOMP → AT16 PROC_POPIRCOMP
R11 49.9/F_4 PCH_OPI_RCOMP → AU16 PCH_OPIRCOMP
R12 49.9/F_4 EDRAM_OPIO_RCOMP → H66 OPCE_RCOMP
R14 49.9/F_4 EOPIO_RCOMP → H65 OPC_RCOMP

JTAG

PROC_TCK → B61 XDP_TCK0 → XDP_TCK0 [16]
PROC_TDI → D60 XDP_TDI_CPU → XDP_TDI_CPU [16]
PROC_TDO → A61 XDP_TDO_CPU → XDP_TDO_CPU [16]
PROC_TMS → C60 XDP_TMS_CPU → XDP_TMS_CPU [16]
PROC_TRST# → B59 XDP_TRST#_CPU → XDP_TRST#_CPU [2,16]

PCH_JTAG_TCK → B56 JTAG_TCK_PCH → JTAG_TCK_PCH [16]
PCH_JTAG_TDI → D59 JTAG_TDI_PCH → JTAG_TDI_PCH [16]
PCH_JTAG_TDO → A56 JTAG_TDO_PCH → JTAG_TDO_PCH [16]
PCH_JTAG_TMS → C59 JTAG_TMS_PCH → JTAG_TMS_PCH [16]
PCH_TRST# → C61 XDP_TRST#_CPU → XDP_TRST#_CPU [2,16]
JTAGX → A59 JTAGX_PCH → JTAGX_PCH [16]

*SKL_ULT
REV = 1

4 OF 20

+VCCSTPLL
R6 *49.9/F_4 CATERR#

+1.0V
R9 0_4
R10 *51_4 JTAGX_PCH
R13 51_4 JTAG_TMS_PCH
R15 51_4 JTAG_TDI_PCH
R16 51_4 JTAG_TDO_PCH
R18 51_4 JTAG_TCK_PCH
Close to Chipset

Close to EC

+VCCSTPLL
PM_THRMTRIP# R5 1K_4

Processor pull-up (CPU)
TO BE REPLACED WITH 1K OHMS FOR SKL .
470 OHM IS FOR I/P

PLACE NEAR CPU

+1.0V
XDP_TMS_CPU R17 *51_4
XDP_TDI_CPU R19 *51_4
XDP_TDO_CPU R20 *51_4

+1.0V
H_PROCHOT# R21 1K_4
XDP_TCK0 R22 51_4
XDP_TRST#_CPU R23 51_4

BU5

PROJECT : G34A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	02 -- SKYPAKE 1/20(eDP/DDI)	1A
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SkyLake ULT Processor (DDR4)

[17] M_A_DQSN[7:0]
[17] M_A_DQSP[7:0]
[18] M_B_DQSN[7:0]
[18] M_B_DQSP[7:0]
[17] M_A_DQ[63:0]
[18] M_B_DQ[63:0]

+1.2VSUS [6,17,18,36,38,46]

Need apply PN

U1B — SKL_ULT — *SKL_ULT REV = 1 — 2 OF 20

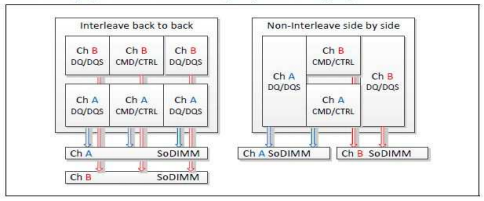
U1C — SKL_ULT — *SKL_ULT REV = 1 — 3 OF 20

NIL-DDR CH - A

NIL-DDR CH - B

20mils width

Interleave (IL) and Non-Interleave (NIL) Modes Mapping



PROJECT : G34A	Quanta Computer Inc.
Size: Custom	Document Number: 03 -- SKYPAKE 3/20(DDR3-A I/F)
Rev: 1A	
Date: Tuesday, January 05, 2016	Sheet 3 of 47

[10,11,12,14,15,16,18] +3V_DEEP_SUS
[2,10,11,12,13,14,15,16,17,18,19,20,21,25,26,27,28,29,30,31,32,33,39,43,44,47] +3V
[10,15,16,25,32,33,35,36,37,38,42,43,46,47] +3VS5
[2,5,6,9,38,39] +VCCSTPLL
[2,6,16,33,38] +1.0V
[13,15,29,30,34,47] +BAT_RTC
[13,15] +3V_RTC_2

U1K SKL_ULT ?

SYSTEM POWER MANAGEMENT

Need apply PN

[33] RSMRST#
EC1 *220P/50V_4
R29 *10K_4 PROCPWRGD
C1 *0.1U/16V_4
[16] SYS_PWROK
[16,33] EC_PWROK
SUSWARN# *0_4 R32
[33] SUSACK#_EC 0_4 R34
[33] SUSWARN#_EC R33 0_4
[28,29,32,33] PCIE_WAKE#
[3,18] DDR_VTT_CNTL

PLTRST# AN10
SYS_RESET# B5
RSMRST# AY17
PROCPWRGD A68
H_VCCST_PWRGD B65
SYS_PWROK B6
PCH_PWROK BA20
DSWROK_EC_R BB20
SUSWARN# AR13
SUSACK# AP11
PCIE_WAKE# BB15
LAN_WAKE# AM15
AW17
DDR_VTT_CNTL AT15

GPP_B13/PLTRST#
SYS_RESET#
RSMRST#
PROCPWRGD
VCCST_PWRGD
SYS_PWROK
PCH_PWROK
DSW_PWROK
GPP_A13/SUSWARN#/SUSPWRDNACK
GPP_A15/SUSACK#
WAKE#
GPD2/LAN_WAKE#
GPD11/LANPHYPC
GPD7/RSVD

*SKL_ULT
REV = 1
11 OF 20
?

GPP_B12/SLP_S0# AT11 PCH_SLP_S0_N
GPD4/SLP_S3# AP15
GPD5/SLP_S4# BA16
GPD10/SLP_S5# AY16
SLP_SUS# AN15 SLP_SUS#_EC
SLP_LAN# AW15
GPD9/SLP_WLAN# BB17 GPD9
GPD6/SLP_A# AN16
GPD3/PWRBTN# BA15 DNBSWON#
GPD1/ACPRESENT AY15 AC_PRESENT_EC
GPD0/BATLOW# AU13 RF_OFF_PCH
GPP_A11/PME# AU11
INTRUDER# AP16 INTRUDER# R
GPP_B11/EXT_PWR_GATE# AM10
GPP_B2/VRALERT# AM11 GPP_B2

PCH_SLP_S0_N [16,33]
SUSB# [16,33]
SUSC# [16,33]
SLP_S5# [16]
SLP_SUS#_EC [33]
TP8
SLP_A# [16]
DNBSWON# [33]
AC_PRESENT_EC [33]
RF_OFF_PCH [32]
TP9

Ra R36 *1M_4 +BAT_RTC
R305 1M_4 +3V_RTC_2
Rb
Modify 0922

Main BAT -->Ra
Coin BAT -->Rb (default)

1005 Change +3V_RTC to +BAT_RTC

PCH Pull-high/low(CLG)

+3V_DEEP_SUS
SUSWARN# R28 *10K_4
SUSACK# R30 10K_4
RF_OFF_PCH R31 10K_4
+3VS5
PCIE_WAKE# R35 1K_4
AC_PRESENT_EC R37 *10K_4
LAN_WAKE# R38 *10K_4
+3V
SYS_RESET# R39 10K_4
RSMRST# R40 10K_4
DSWROK_EC R41 100K/F_4

For DS3 Sequence

For DS3 -->Ra
Non-DS3 -->Rb
RSMRST# R42 Rb *0_4
[33] DSWROK_EC R46 0_4 DSWROK_EC_R
Ra

PLTRST#(CLG)

Check Rise/Fall time less than 100ns

PLTRST# [16,19,28,29,31,32,33]
R52 100K/F_4

System PWR_OK(CLG)

SYS_PWROK R53 0_4 EC_PWROK
R54 10K/F_4

+1.0V R47 1K_4
+VCCSTPLL R48 *1K_4
Ra
[16,33,35,36,37] HWPG D1 1 2 MEK500V-40 H_VCCST_PWRGD_R R50 60.4/F_4 H_VCCST_PWRGD
C3 *10P/50V_4

Ra close to CPU side
H_VCCST_PWRGD trace 0.3" - 1.5"

+1.0V R43 15K/F_4
+5VS5 R44 100K_4
+3VS5 R45 10K_4
HWPG
+1.0V_PWRGD_G2 2
Q1 2N7002K
R49 100K_4
+1.0V_PWRGD_G1 2
Q2 METR3904-G
C2 0.1U/16V_4
R51 100K_4

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PROJECT : G34A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	04 -- SKYPAKE 5/20(Power Manger)	1A
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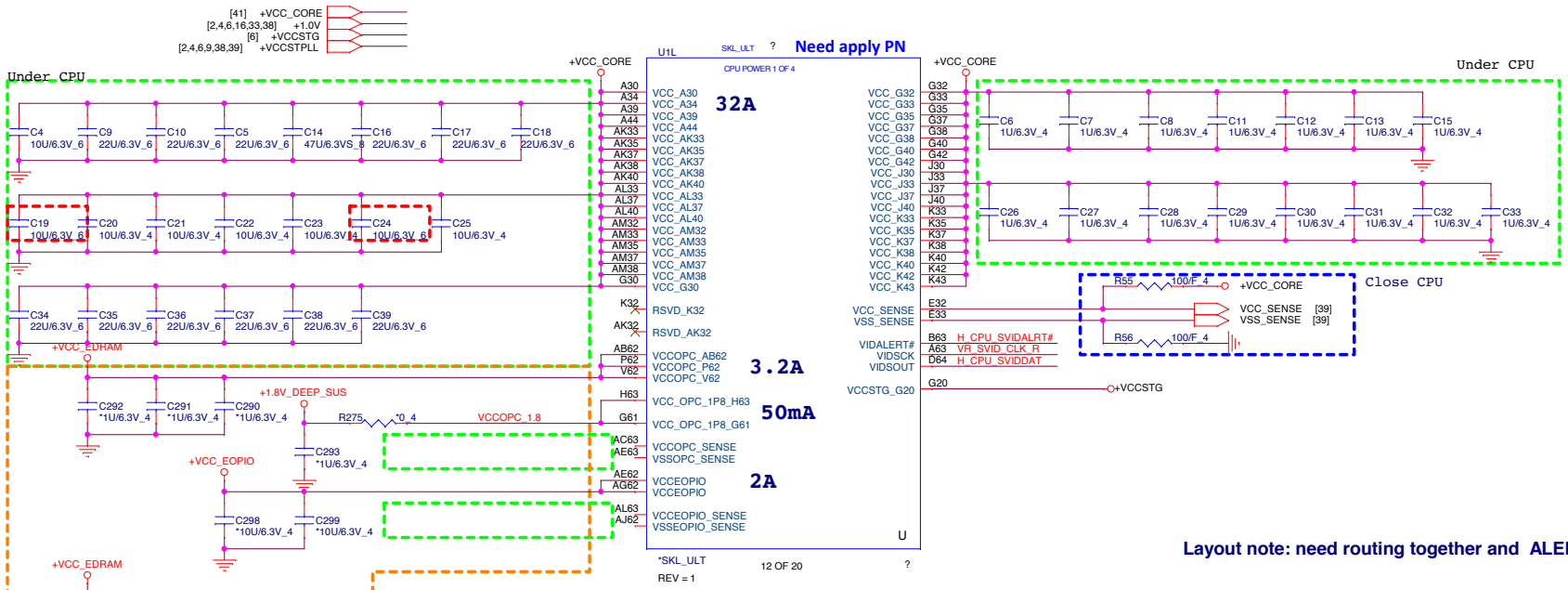

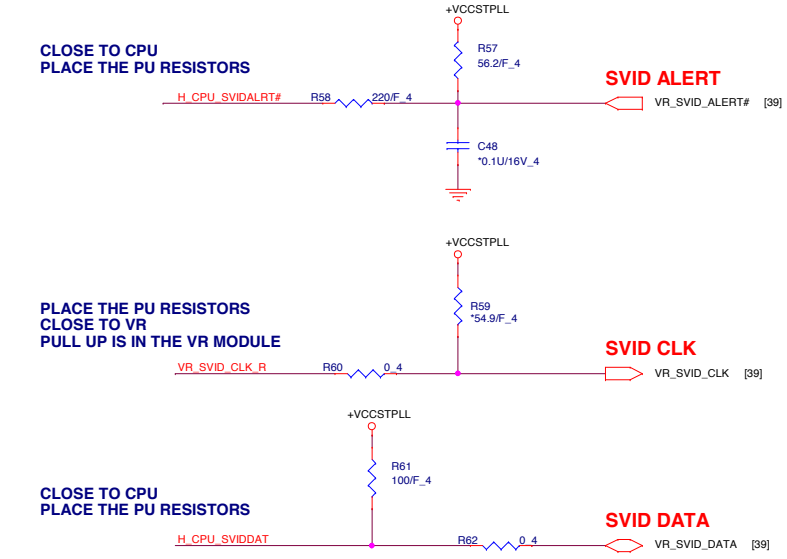

Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
$V_{CC_{GT}}$	Processor Graphics Power Rails	SVID
$V_{CC_{GTX}}$	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
$V_{CC_{SA}}$	System Agent Power Rail	SVID/Fixed (SKU dependent)
$V_{CC_{IO}}$	IO Power Rail	Fixed
$V_{CC_{ST}}$	Sustain Power Rail	Fixed
$V_{CC_{PLL}}$	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
$V_{CC_{OPC}}$	Processor OPC power rail (available only in SKU's with OPC)	Fixed
$V_{CC_{OPC\_1P8}}$	Processor OPC power rail (available only in SKU's with OPC)	Fixed
$V_{CC_{EOPIO}}$	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

BU5

PROJECT : G34A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	05 -- SKYPAKE 6/20 (POWER-1)	1A

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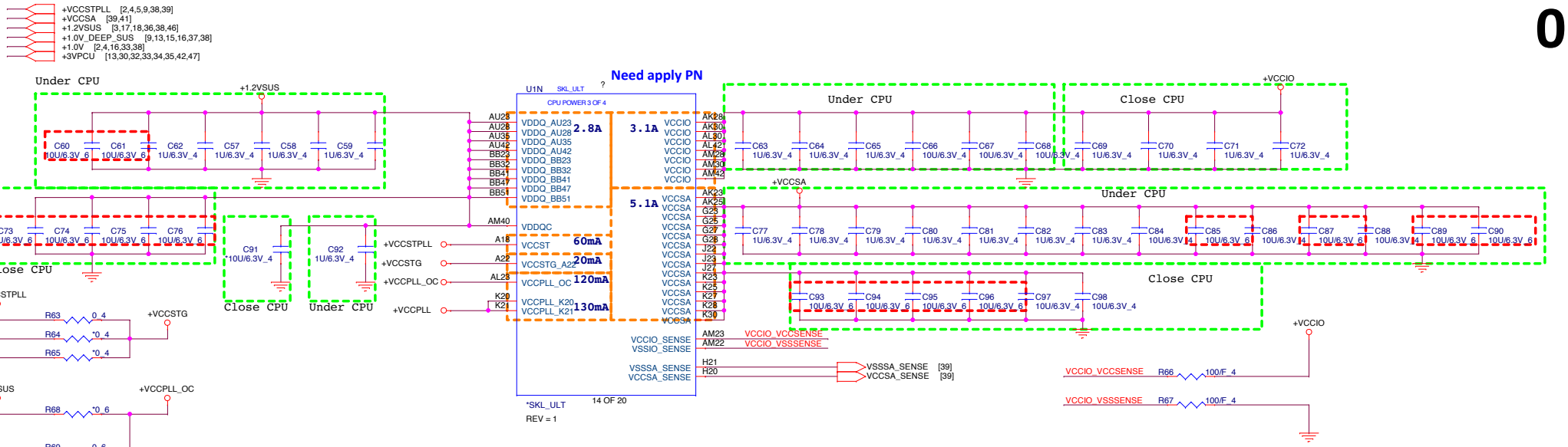
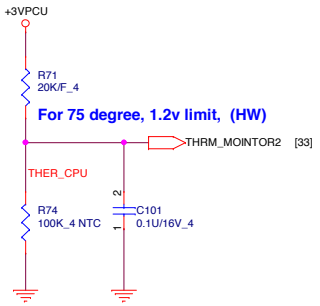
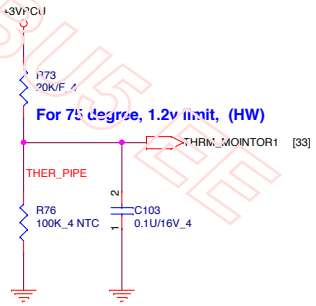


IO Thrm Protect

For CPU USE



For PIPE USE



Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

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PROJECT : G34A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	06 -- SKYPAKE 7/20 (POWER-2)	1A

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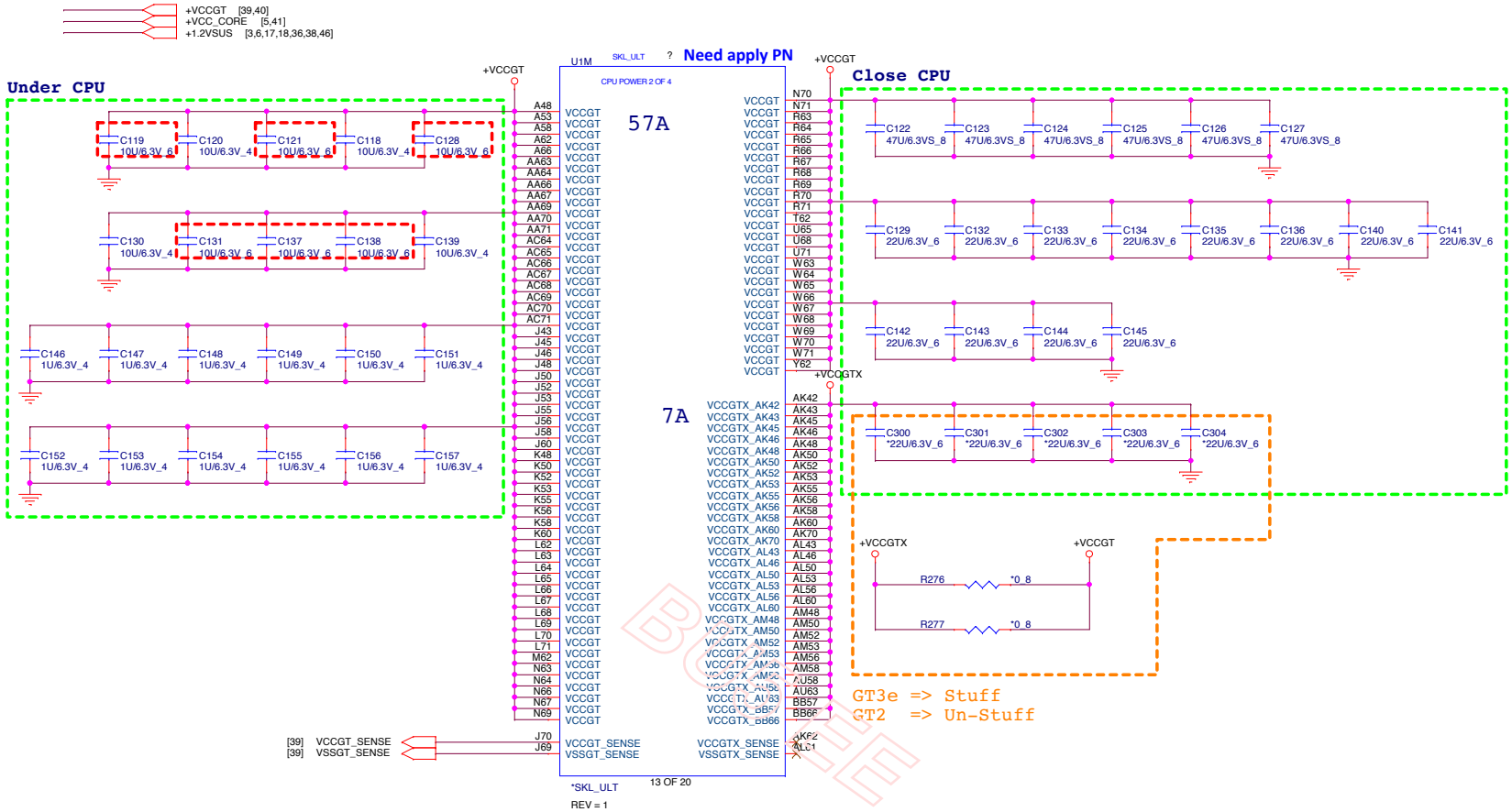
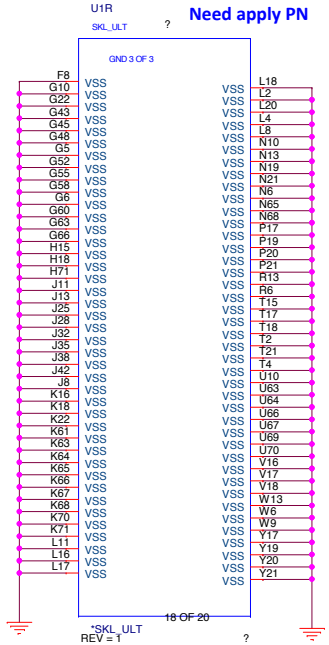


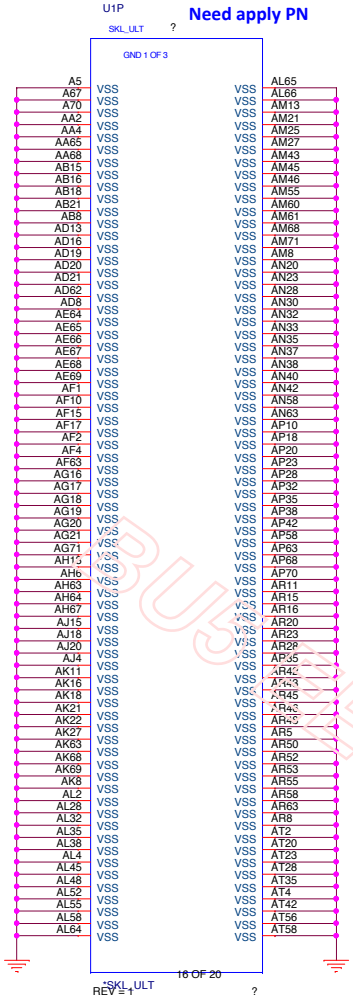
Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

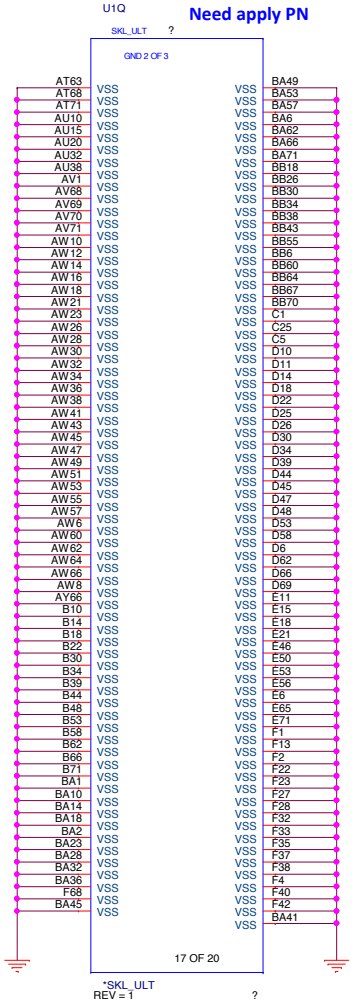
BU5

PROJECT : G34A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	07 -- SKYPAKE 8/20 (POWER-3)	1A
Date: Tuesday, January 05, 2016	Sheet 7 of 47	







BU5	**PROJECT : G34A** Quanta Computer Inc.	
Size: Custom	Document Number: 8 -- SKYPAKE 9/20 (GND-1)	Rev: 1A
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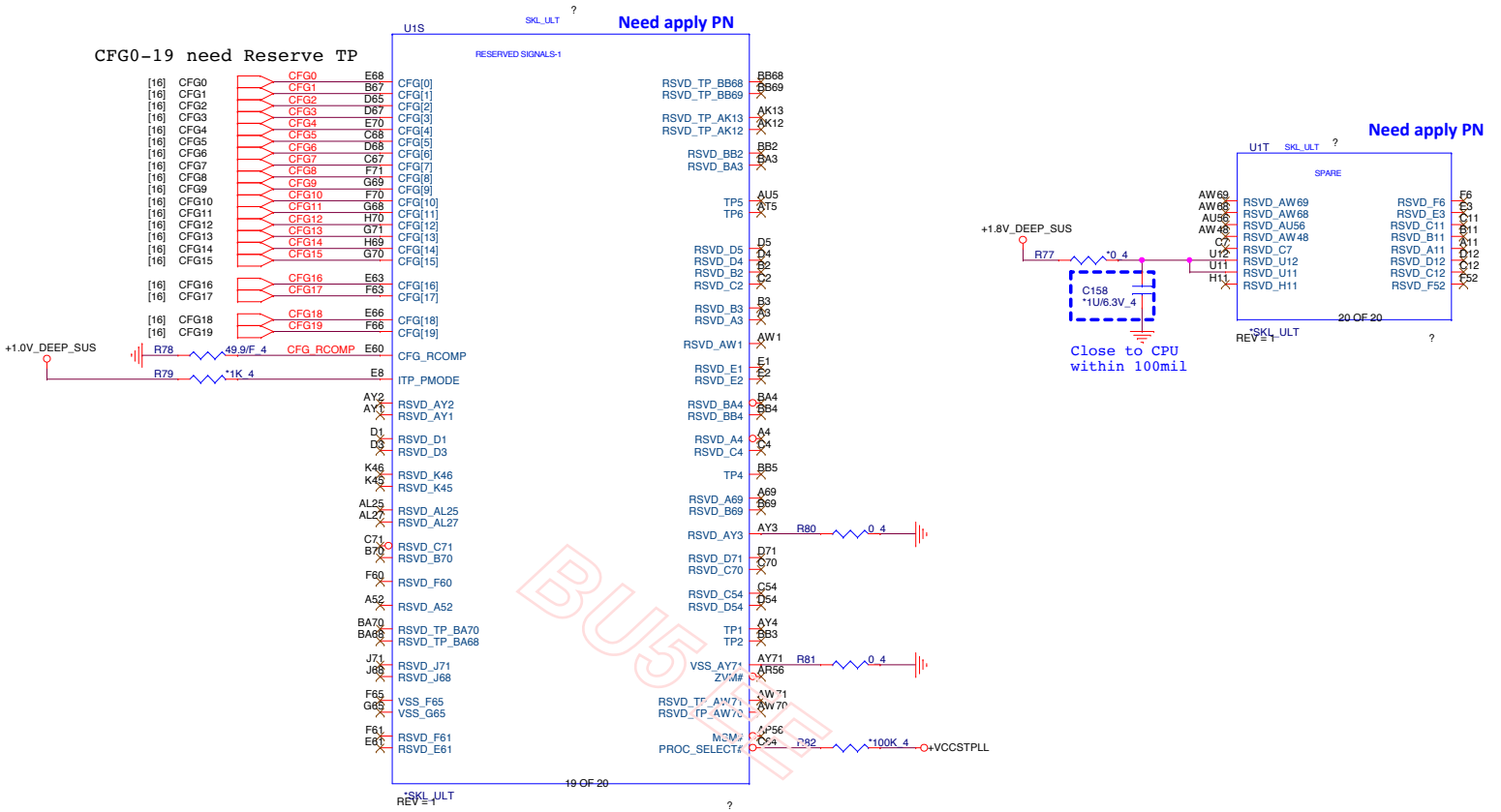

Processor Strapping The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physcial Debug Enable) DFX Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	CFG3 R83 *1K_4
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	CFG4 R84 1K_4

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PROJECT : G34A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	9 -- SKYPAKE 12/20 (RSV-1)	1A

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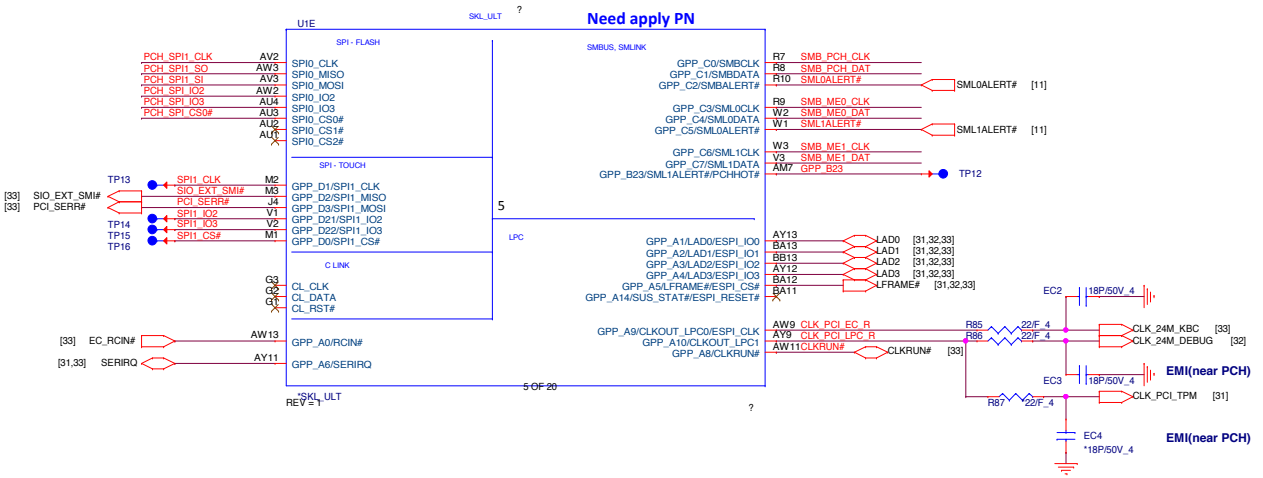
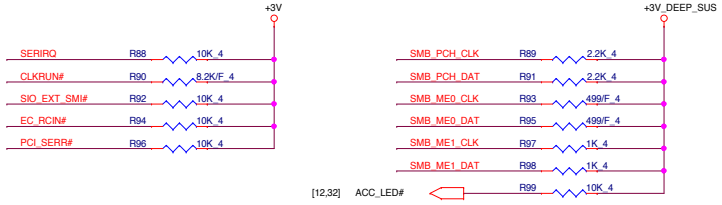
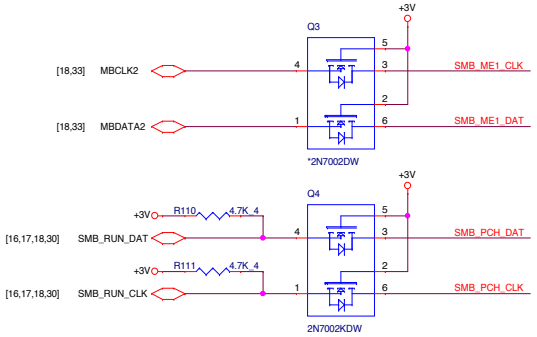
+3V_DEEP_SUS [4,11,12,14,15,16,18]
+3V [2,4,11,12,13,14,15,16,17,18,19,20,21,25,26,27,28,29,30,31,32,33,39,43,44,47]
+5V [25,26,27,30,32,43]
+1.0V [2,4,6,16,33,38]
+3VS5 [4,15,16,25,32,33,35,36,37,38,42,43,46,47]



GPIO Pull UP



SMBus/Pull-up(CLG)



CPU heat pipe local thermal sensor
DDR thermal sensor
EC

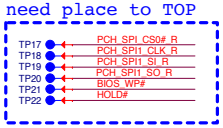
Touch Pad
XDP
DDR4

PCH SPI ROM(CLG)

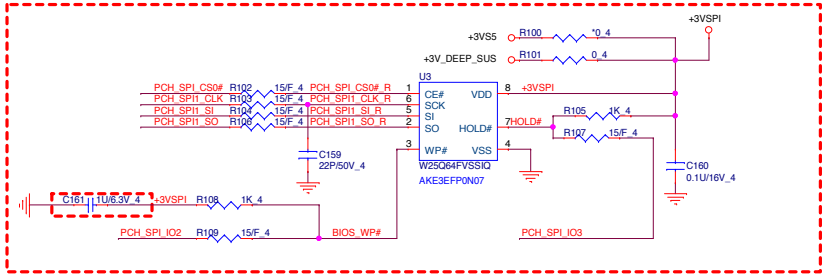
Vender	Size	P/N
EON	8MB	AKE3EZN0Q01 (EN25QH64-104HIP)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)
Socket		DFHS08FS023

[33] PCH_SPI_CS0#_R
[33] PCH_SPI1_CLK_R
[33] PCH_SPI1_SI_R
[33] PCH_SPI1_SO_R
PCH_SPI_CS0#_R
PCH_SPI1_CLK_R
PCH_SPI1_SI_R
PCH_SPI1_SO_R

need place to TOP



PCH SPI ROM(CLG)



1005 Change P/N to DFHS08FS023(Socket)

BU5

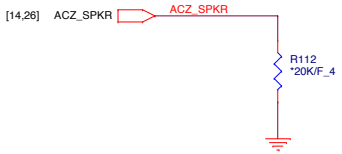
PROJECT : G34A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	10 -- SKYPAKE 14/20(SPI/LPC/SMBUS)	1A

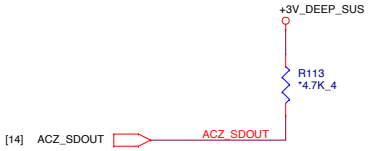
Date: Tuesday, January 05, 2016 Sheet 10 of 47

Functional Strap Definitions

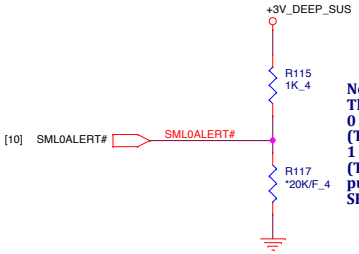
DESIGN NOTE:
WEAK PULL UP RESISTOR PRESENT ON THIS NET



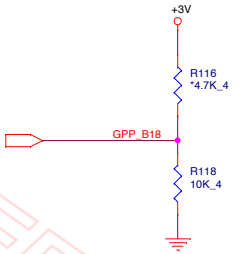
TOP SWAP OVERRIDE
HIGH - TOP SWAP ENABLE
LOW-DISABLED
HIGH: LPC SELECTED FOR SYSTEM FLASH
WEAK INTERNAL PD



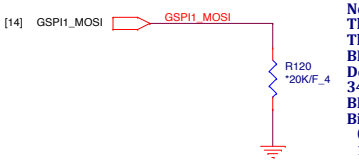
No Boot:
The signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.



No Boot:
The signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.

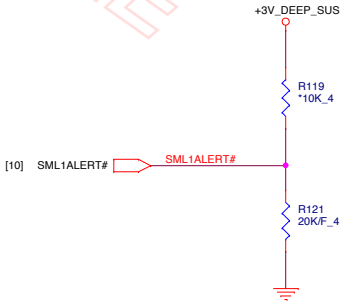


No Boot:
The signal has a weak internal pull-down.
0 = Disable No Reboot mode.
1 = Enable No Reboot mode
(PCH will disable the TCO
Timer system reboot feature).
This function is useful when running ITP/XDP.



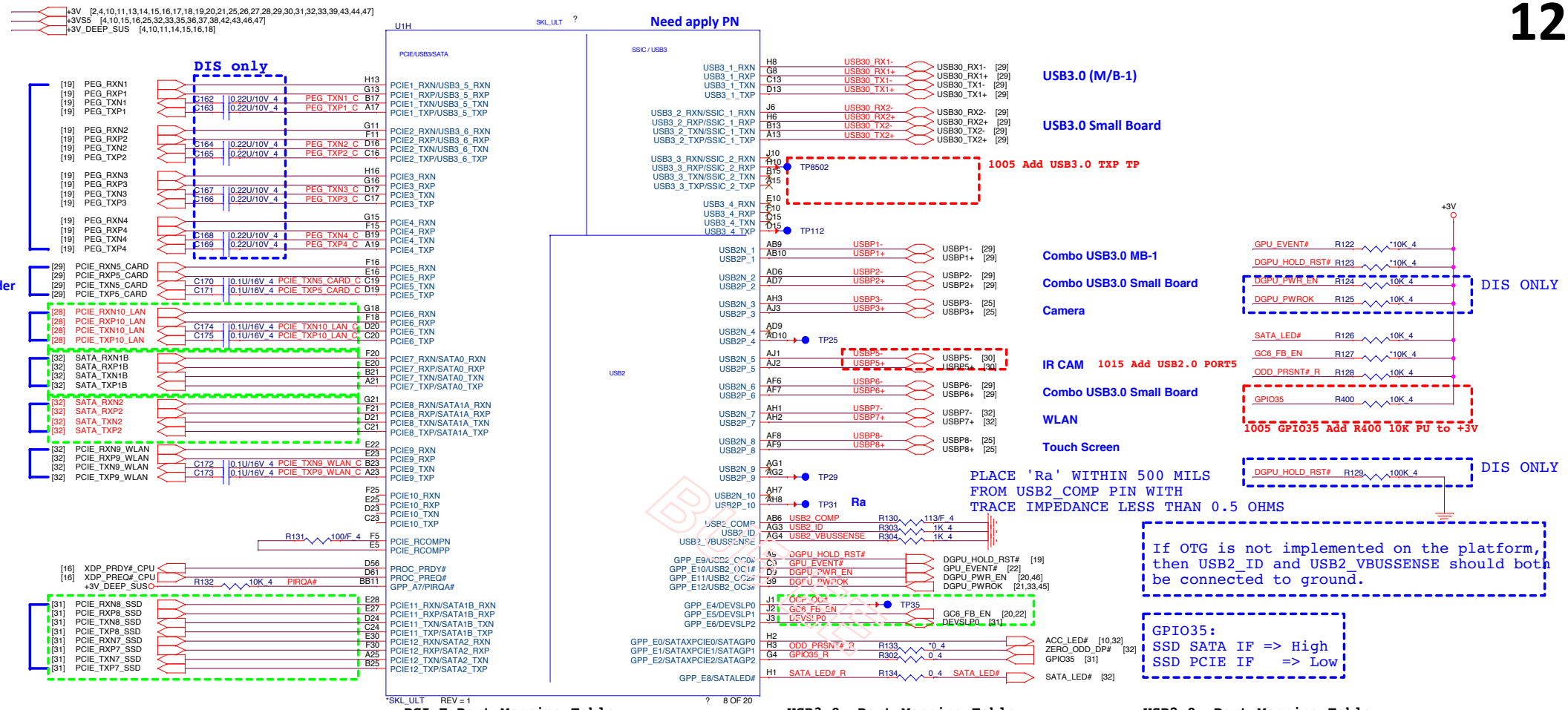
No Boot:
The signal has a weak internal pull-down.
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.

Bit 10	Boot BIOS Destination
0	SPI
1	LPC



No Boot:
The signal has a weak internal pull-down.
0 = LPC Is selected for EC.
1 = eSPI Is selected for EC.

BU5	PROJECT : G34A Quanta Computer Inc.	
Size: Custom	Document Number: 11 -- SKYPAKE 15/20(HDA)	Rev: 1A
Date: Tuesday, January 05, 2016	Sheet 11 of 47	



PCI-E Port Mapping Table

PCI-E Port	Function	CLK RQ Port	Function
Port1	dGPU	Port0	VGA
Port2	dGPU	Port1	CR
Port3	dGPU	Port2	SSD
Port4	dGPU	Port3	WLAN
Port5	CardReader	Port4	LAN
Port6	LAN	Port5	Un-used
Port7	HDD		
Port8	ODD		
Port9	WLAN		
Port10	Un-used		
Port11	SSDx2		
Port12	SSDx2/ SATA2		

USB3.0 Port Mapping Table

USB3.0	Function
PORT-1	USB3.0 MB-1
PORT-2	Cobime USB3.0 Small Board
PORT-3	NC
PORT-4	NC

1005 Change Name from DEVSLP2 to DEVSLP0
DEVSLP0 and GC6_FB_EN SWAP
1005 GPIO35 and ACC_LED# SWAP

USB2.0 Port Mapping Table

USB2.0	Function
PORT-1	Cobime USB3.0 MB-1
PORT-2	Cobime USB3.0 Small Board
PORT-3	Camera
PORT-4	NC
PORT-5	IR CAM
PORT-6	Cobime USB3.0 Small Board
PORT-7	WLAN
PORT-8	Touch Screen
PORT-9	NC
PORT-10	NC

BU5

PROJECT : G34A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	12 -- SKYPAKE 16/20 (PCIE/USB)	1A
Date: Tuesday, January 05, 2016	Sheet 12 of 47	

+3V_RTC_2 [4,15]
+BAT_RTC [4,15,29,30,34,47]
+1.8V_DEEP_SUS [5,9,15,37,47]
+3V [2,4,10,11,12,14,15,16,17,18,19,20,21,25,26,27,28,29,30,31,32,33,39,43,44,47]

VGA
Cardreader
SSD
WLAN
LAN

1005 SWAP CLK RQ Port

U1J SKL_ULT ? Need apply PN

CLOCK SIGNALS

TBT

*SKL_ULT REV = 1

10 OF 20

Install for XDP

RP1 *0_4P2R_4

+1.0V_DEEP_SUS

R135 2.7K/F_4

R137 *60.4/F_4

XCLK_BIASREF

CLK_REQ/Strap Pin(CLG)

+3V

PCIE_CLKREQ_VGA# R136 10K_4
PCIE_CLKREQ_WLAN# R138 10K_4
PCIE_CLKREQ_LAN# R139 10K_4
PCIE_CLKREQ_CR# R140 10K_4
PCIE_CLKREQ_SSD# R141 10K_4
PCIE_CLKREQ5# R142 10K_4

U1I SKL_ULT ? Need apply PN

CSI-2

R143 100/F_4 TP39

1005 Delete TP

R144 200/F_4

9 OF 20

*SKL_ULT REV = 1

RTC Clock 32.768KHz

C177 12P/50V_4 RTC_X1
Y1 32.768KHZ
R147 10M_4
C179 12P/50V_4 RTC_X2

RTC Circuitry(RTC)

30mils

1005 Change +3V_RTC to +BAT_RTC

Main BAT -->Ra
Coin BAT -->Rb (default)

Rb R306 0_4
Ra R307 *0_4

R145 *0_6
R146 20K/F_4
RTC_RST#

RTC Power trace width 20mils.

+3V_RTC_0
R150 1K_4
+3VPCU
+3V_RTC_1
D2 BAT54CW-7-F
C181 1U/6.3V_4
CN1 BAT_CONN DFHS02FS027 BAT-23_2-4_2

C178 1U/6.3V_4
R149 20K/F_4
SRTC_RST#
C182 1U/6.3V_4
R152 *0_6 SRTC_RST#

Q5 2N7002K
EC_RTC_RST [33]
R151 10K_4

External Crystal

The 24 MHz (50 Ohm ESR) XTAL used for Skylake-U needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-U.

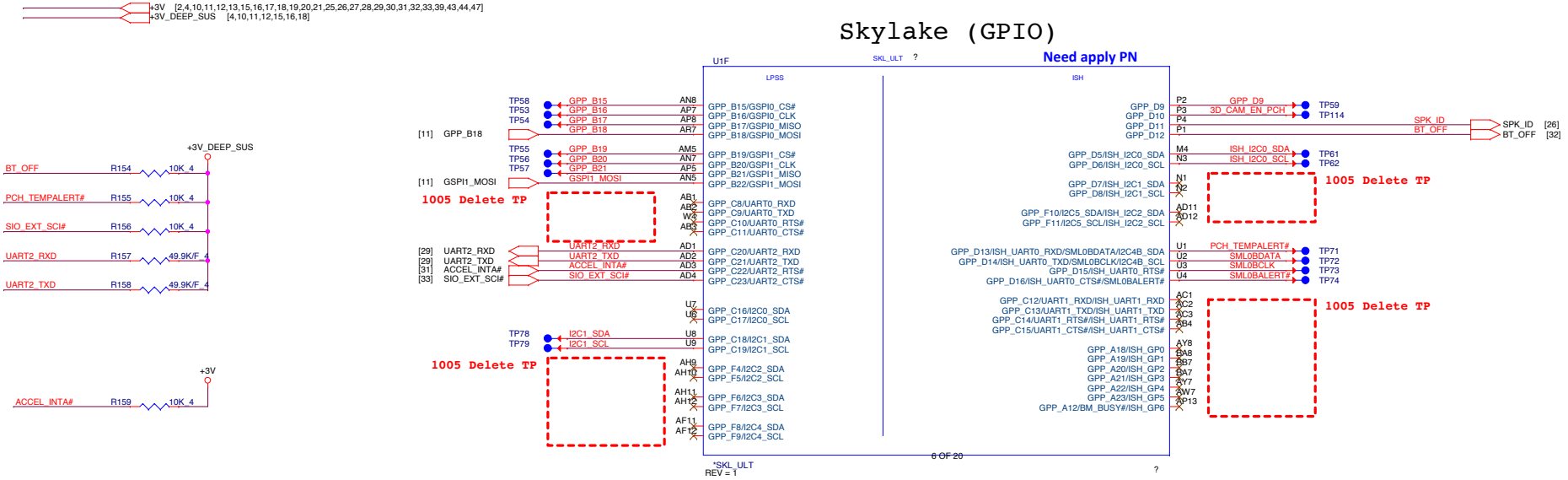
TP51 C176 27P/50V_4
XTAL24_IN
XTAL24_OUT
R148 1M_4
24MHZ +-20PPM Y2
C180 27P/50V_4 TP52

BU5

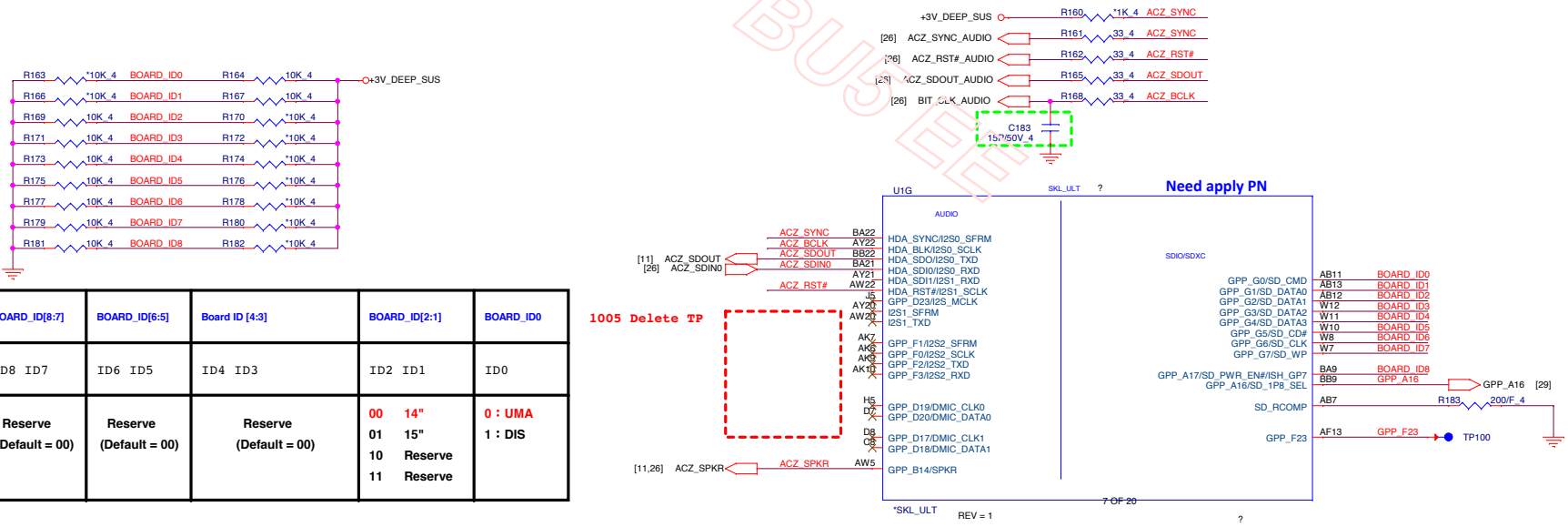
PROJECT : G34A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	13 -- SKYPAKE 17/20 (CLK)	1A
Date: Tuesday, January 05, 2016	Sheet 13 of 47	

Skylake (GPIO)



HDA Bus(CLG)



Skylake U	BOARD_ID[8:7]	BOARD_ID[6:5]	Board ID [4:3]	BOARD_ID[2:1]	BOARD_ID0
Model	ID8 ID7	ID6 ID5	ID4 ID3	ID2 ID1	ID0
Definition	Reserve (Default = 00)	Reserve (Default = 00)	Reserve (Default = 00)	00 14" 01 15" 10 Reserve 11 Reserve	0 : UMA 1 : DIS

BU5

PROJECT : G34A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	14 – SKYPAKE 19/20 (GPIO)	1A
Date: Tuesday, January 05, 2016	Sheet 14 of 47	

[4,10,11,12,14,16,18] +3V_DEEP_SUS
[9,13,16,37,38] +1.0V_DEEP_SUS
[5,9,37,47] +1.8V_DEEP_SUS
[4,13,29,30,34,47] +BAT_RTC
[4,10,16,25,32,33,35,36,37,38,42,43,46,47] +3VS5

U1O SKL_ULT

CPU POWER 4 OF 4

Need apply PN

PCH Internal VRM

Ca and Cb close to CPU less then 100 mils

+VCCPRIM
C184 1U/6.3V_4
AB19 VCCPRIM_1P0
AB20 VCCPRIM_1P0
P18 VCCPRIM_1P0
2.899A

+1.0V_DEEP_SUS
C185 1U/6.3V_4
AF18 VCCPRIM_CORE
AF19 VCCPRIM_CORE
V20 VCCPRIM_CORE
V21 VCCPRIM_CORE
2.57A

+VCCDSW_1.0V
Ca
C187 1U/6.3V_4
AL1 DCPDSW_1P0

+1.0V_DEEP_SUS
R188 0_6
C188 1U/6.3V_4
+VCCMPHYAON_1P0
K17 VCCMPHYAON_1P0
L1 VCCMPHYAON_1P0

+1.0V_DEEP_SUS
C189 1U/6.3V_4
C190 47U/6.3VS_8
N15 VCCMPHYGT_1P0_N15
N16 VCCMPHYGT_1P0_N16
N17 VCCMPHYGT_1P0_N17
P15 VCCMPHYGT_1P0_P15
P16 VCCMPHYGT_1P0_P16
1.714A

+1.0V_DEEP_SUS
R194 0_6
C192 1U/6.3V_4
+VCCAMPHYPLL_1P0
K15 VCCAMPHYPLL_1P0
L15 VCCAMPHYPLL_1P0

+1.0V_DEEP_SUS
R196 0_6
+VCCAPLL_1.0V
V15 VCCAPLL_1P0
0.03A

+1.0V_DEEP_SUS
R199 0_6
+VCCPRIM
AB17 VCCPRIM_1P0_AB17
Y18 VCCPRIM_1P0_Y18

+3VS5
R201 0_4
C193 1U/6.3V_4
AD17 VCCDSW_3P3_AD17
AD18 VCCDSW_3P3_AD18
AJ17 VCCDSW_3P3_AJ17
0.09A

+V3.3DX_1.5DX_ADO
C194 1U/6.3V_4
AJ19 VCCHDA

+3V_DEEP_SUS
R205 0_6
+VCCSPI
AJ16 VCCSPI

+1.0V_DEEP_SUS
R206 0_6
C196 1U/6.3V_4
+VCCSRAM_1.0V
AF20 VCCSRAM_1P0
AF21 VCCSRAM_1P0
T19 VCCSRAM_1P0
T20 VCCSRAM_1P0

+3V_DEEP_SUS
R207 0_6
+VCCPRIM_3.3V
AJ21 VCCPRIM_3P3_AJ21

+1.0V_DEEP_SUS
R208 0_6
+VCCPRIM_1.0V
AK20 VCCPRIM_1P0_AK20

+1.0V_DEEP_SUS
R209 0_6
C197 1U/6.3V_4
+VCCAPLLEBB
N18 VCCAPLLEBB

15 OF 20

*SKL_ULT
REV = 1

VCCPGPPA AK15 +VCCPGPPA
VCCPGPPB AG15 +VCCPGPPB
VCCPGPPC Y16 +VCCPGPPC
VCCPGPPD Y15 +VCCPGPPD
VCCPGPPE T16 +VCCPGPPE
VCCPGPPF AF16 +VCCPGPPF
VCCPGPPG AD15 +VCCPGPPG

C186 1U/6.3V_4
VCCPRIM_3P3_V19 V19 +3V_DEEP_SUS

VCCPRIM_1P0_T1 T1 +VCCPRIM_1.0V_T1
R187 0_6 +1.0V_DEEP_SUS

VCCATS_1P8 AA1 +VCCATS_1.8V
R190 0_6 +1.8V_DEEP_SUS

VCCRTCPRIM_3P3 AK17 +VCCRTCPRIM_3.3V
R192 0_6 +3V_DEEP_SUS

VCCRTC_AK19 AK19 +VCCRTC
VCCRTC_BB14 BB14
Ra R308 *0_4
Rb R309 0_4
+BAT_RTC
+3V_RTC_2
20mils

Main BAT -->Ra
Coin BAT -->Rb (default)

DCPRTC BB10 DCPRTC
Cb C191 0.1U/16V_4
+1.0V_DEEP_SUS
1005 Change +3V_RTC to +BAT_RTC

VCCCLK1 A14 +VCCCLK1
R195 0_6

VCCCLK2 K19 +VCCCLK2
R198 0_6

VCCCLK3 L21 +VCCCLK3
R200 0_6

VCCCLK4 N20 +VCCCLK4
R202 0_6

VCCCLK5 L19 +VCCCLK5
R203 0_6

VCCCLK6 A10 +VCCCLK6
R204 0_6
C195 1U/6.3V_4

GPP_B0/CORE_VID0 AN11 CORE_VID0
GPP_B1/CORE_VID1 AN13 CORE_VID1
TP102
TP103

+3V_DEEP_SUS
+VCCPGPPA R184 0_6
+VCCPGPPB R185 0_6
+VCCPGPPC R186 0_6
+VCCPGPPD R189 0_6
+VCCPGPPE R191 0_6
+VCCPGPPG R193 0_6

+1.8V_DEEP_SUS
+VCCPGPPF R197 0_6

+V3.3DX_1.5DX_ADO
R210 0_4 +3V
+1.0V_DEEP_SUS
C203 *1U/6.3V_4
C204 *22U/6.3V_6

for DS3

+3VS5
R211 100K_4
C205 1U/6.3V_4
U4
5 IN
4 IN
3 ON/OFF
OUT 1
GND 2
AP2821KTR-G1
[33,37,38] SLP_SUS_ON
C210 *10P/50V_4
+3V_DEEP_SUS
C209 0.1U/16V_4

+VCCATS_1.8V
C198 1U/6.3V_4

+VCCRTC
C199 0.1U/16V_4
C200 1U/6.3V_4

+VCCRTCPRIM_3.3V
C201 1U/6.3V_4
C202 0.1U/16V_4

+VCCPGPPB
C206 1U/6.3V_4

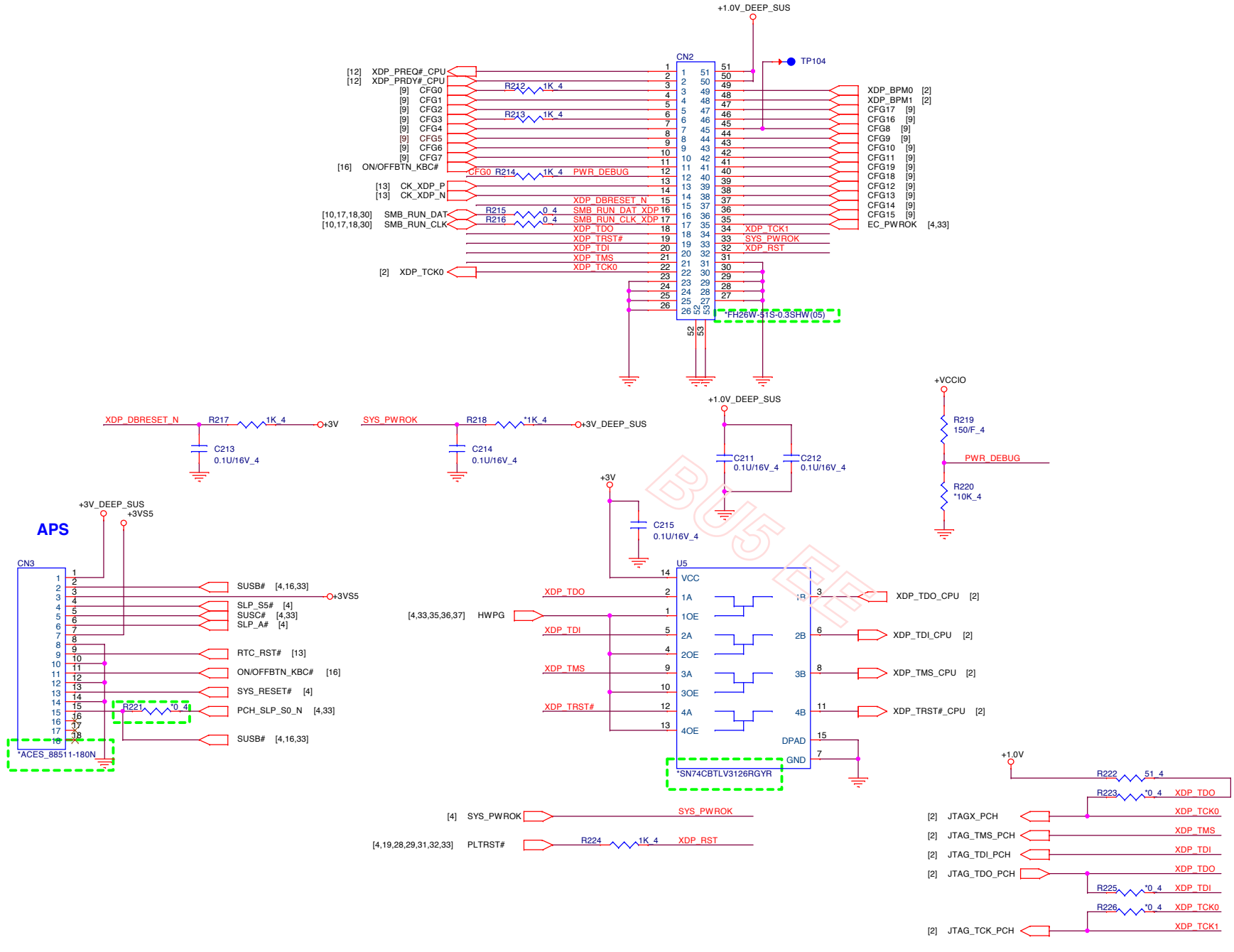
+VCCPGPPC
C207 1U/6.3V_4

+VCCPGPPE
C208 1U/6.3V_4

BU5

PROJECT : G34A
Quanta Computer Inc.

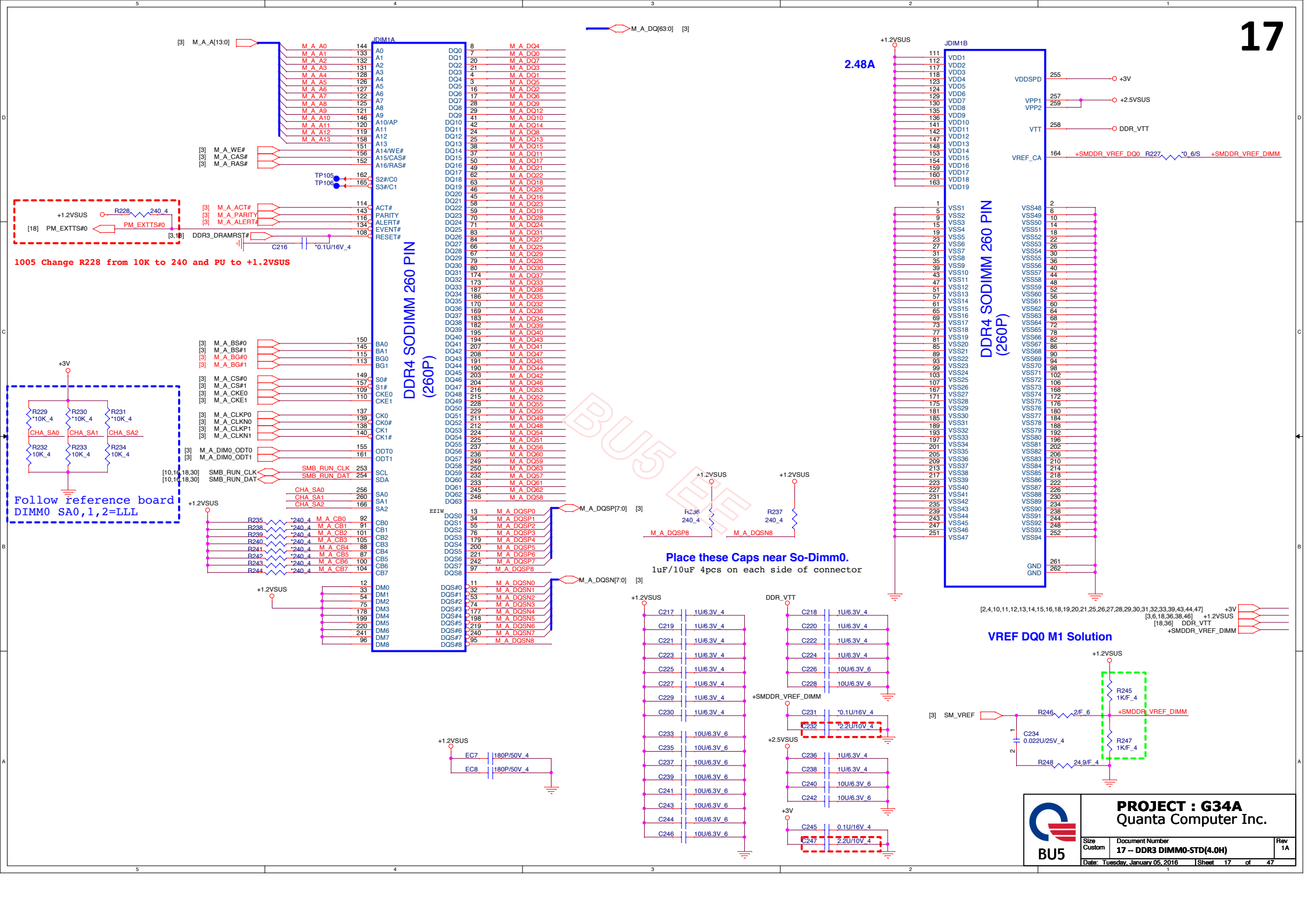
Size	Document Number	Rev
Custom	15 -- SKYPAKE 20/20(PCH POWER)	1A
Date: Tuesday, January 05, 2016	Sheet 15 of 47	

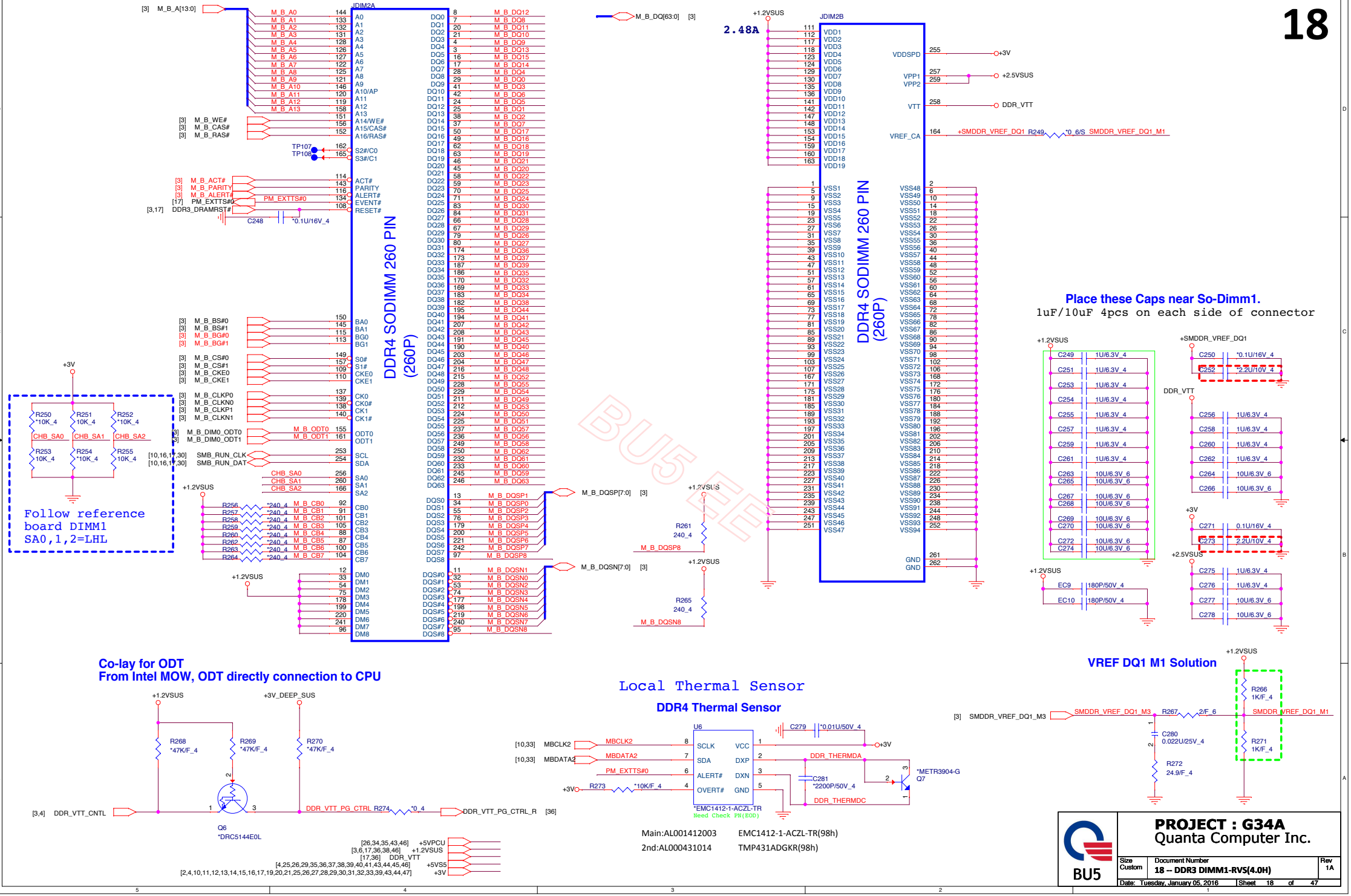


BU5

PROJECT : G34A
Quanta Computer Inc.

Size	Document Number	Rev
	16 -- HSW XDP & APS	1A
Date: Tuesday, January 05, 2016	Sheet 16 of 47	


JDIM1A
DDR4 SODIMM 260 PIN
(260P)
JDIM1B
DDR4 SODIMM 260 PIN
(260P)
2.48A
1005 Change R228 from 10K to 240 and PU to +1.2VSUS
Follow reference board
DIMM0 SA0,1,2=LLL
Place these Caps near So-Dimm0.
1uF/10uF 4pcs on each side of connector
VREF DQ0 M1 Solution
PROJECT : G34A
Quanta Computer Inc.
BU5
Size Custom
Document Number
17 -- DDR3 DIMM0-STD(4.0H)
Rev 1A
Date: Tuesday, January 05, 2016
Sheet 17 of 47



PROJECT : G34A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	18 -- DDR3 DIMM1-RVS(4.0H)	1A
Date: Tuesday, January 05, 2016	Sheet 18 of 47	

BU5

PEX_IOVDD + PEX_IOVDDQ = 1.042A

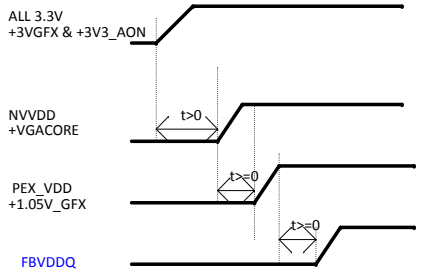
PEX_PLL_HVDD + PEX_SVDD_3V3 = 143mA

PEX_PLLVDD = 130mA

NVDD = 32.22 ~ 26.66 A

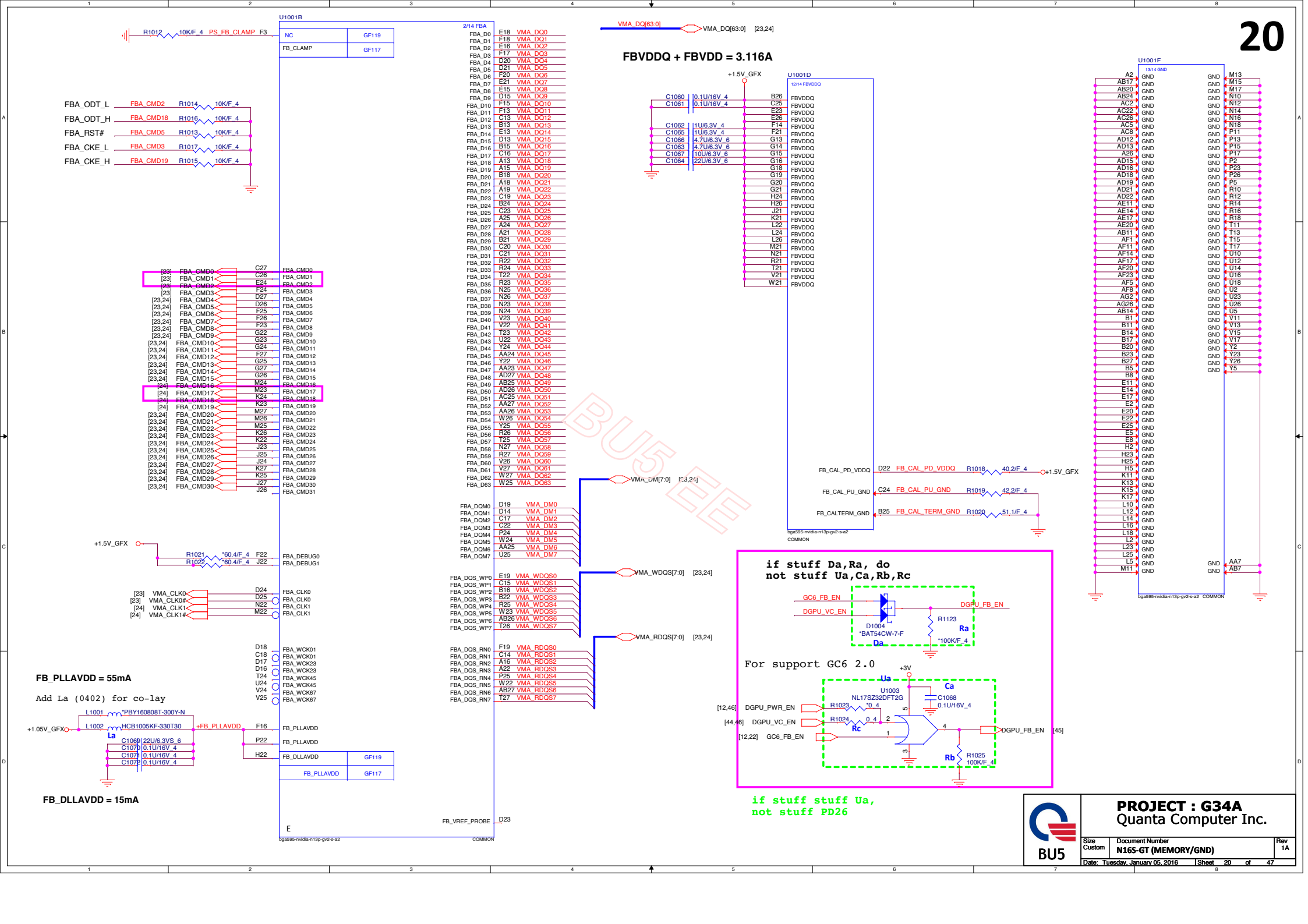
VDD33 = 56mA

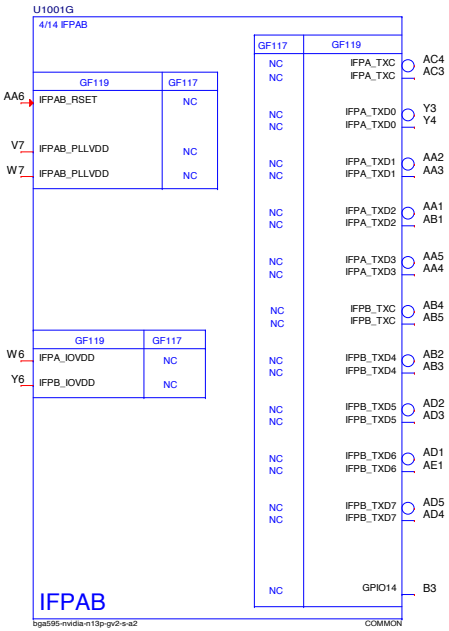
Power up sequence

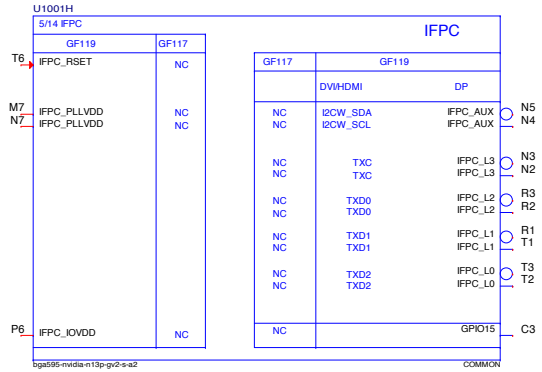


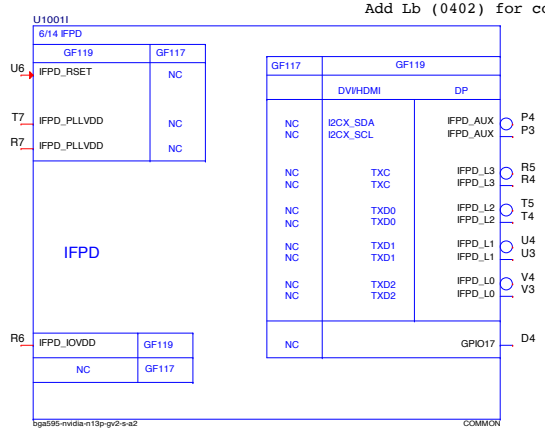
if stuff Da,Db,Ra,Rb, do not stuff Ua,Ub,Ca,Cb,Rc,Rd

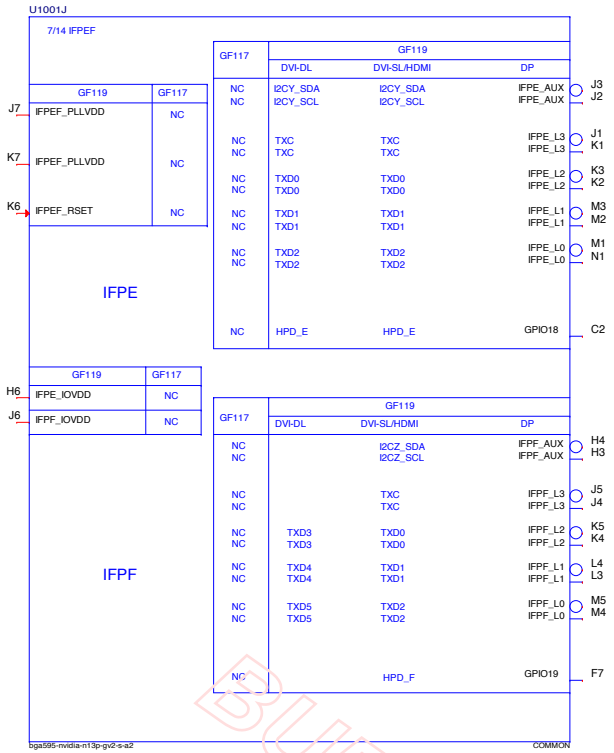
BU5	**PROJECT : G34A** Quanta Computer Inc.	
Size Custom	Document Number **N16S-GT (PCIE I/F) /NVDD**	Rev 1A
Date: Tuesday, January 05, 2016	Sheet 19 of 47	

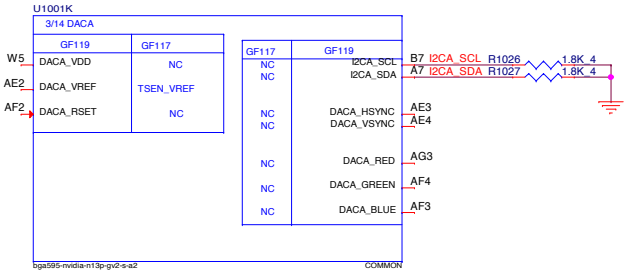

U1001B
2/14 FBA
R1012 10K/F_4 PS_FB_CLAMP F3
NC GF119
FB_CLAMP GF117
FBA_ODT_L FBA_CMD2 R1014 10K/F_4
FBA_ODT_H FBA_CMD18 R1016 10K/F_4
FBA_RST# FBA_CMD5 R1013 10K/F_4
FBA_CKE_L FBA_CMD3 R1017 10K/F_4
FBA_CKE_H FBA_CMD19 R1015 10K/F_4
FBA_CMD0 FBA_CMD1 FBA_CMD2 FBA_CMD3 FBA_CMD4 FBA_CMD5 FBA_CMD6 FBA_CMD7 FBA_CMD8 FBA_CMD9 FBA_CMD10 FBA_CMD11 FBA_CMD12 FBA_CMD13 FBA_CMD14 FBA_CMD15 FBA_CMD16 FBA_CMD17 FBA_CMD18 FBA_CMD19 FBA_CMD20 FBA_CMD21 FBA_CMD22 FBA_CMD23 FBA_CMD24 FBA_CMD25 FBA_CMD26 FBA_CMD27 FBA_CMD28 FBA_CMD29 FBA_CMD30 FBA_CMD31
+1.5V_GFX
R1021 *60.4/F_4 R1022 *60.4/F_4
FBA_DEBUG0 FBA_DEBUG1
VMA_CLK0 VMA_CLK0# VMA_CLK1 VMA_CLK1#
FBA_CLK0 FBA_CLK0 FBA_CLK1 FBA_CLK1
FBA_WCK01 FBA_WCK01 FBA_WCK23 FBA_WCK23 FBA_WCK45 FBA_WCK45 FBA_WCK67 FBA_WCK67
FB_PLLAVDD = 55mA
Add La (0402) for co-lay
L1001 *PBY160808T-300Y-N
L1002 HCB1005KF-330T30
+1.05V_GFX
+FB_PLLAVDD
La
C1069 22U/6.3VS_6
C1070 0.1U/16V_4
C1071 0.1U/16V_4
C1072 0.1U/16V_4
FB_PLLAVDD FB_PLLAVDD
FB_DLLAVDD GF119
FB_PLLAVDD GF117
FB_DLLAVDD = 15mA
FB_VREF_PROBE D23
bga595-nvidia-n13p-gv2-s-a2 COMMON
FBA_D0 FBA_D1 FBA_D2 FBA_D3 FBA_D4 FBA_D5 FBA_D6 FBA_D7 FBA_D8 FBA_D9 FBA_D10 FBA_D11 FBA_D12 FBA_D13 FBA_D14 FBA_D15 FBA_D16 FBA_D17 FBA_D18 FBA_D19 FBA_D20 FBA_D21 FBA_D22 FBA_D23 FBA_D24 FBA_D25 FBA_D26 FBA_D27 FBA_D28 FBA_D29 FBA_D30 FBA_D31 FBA_D32 FBA_D33 FBA_D34 FBA_D35 FBA_D36 FBA_D37 FBA_D38 FBA_D39 FBA_D40 FBA_D41 FBA_D42 FBA_D43 FBA_D44 FBA_D45 FBA_D46 FBA_D47 FBA_D48 FBA_D49 FBA_D50 FBA_D51 FBA_D52 FBA_D53 FBA_D54 FBA_D55 FBA_D56 FBA_D57 FBA_D58 FBA_D59 FBA_D60 FBA_D61 FBA_D62 FBA_D63
VMA_DQ0 VMA_DQ1 VMA_DQ2 VMA_DQ3 VMA_DQ4 VMA_DQ5 VMA_DQ6 VMA_DQ7 VMA_DQ8 VMA_DQ9 VMA_DQ10 VMA_DQ11 VMA_DQ12 VMA_DQ13 VMA_DQ14 VMA_DQ15 VMA_DQ16 VMA_DQ17 VMA_DQ18 VMA_DQ19 VMA_DQ20 VMA_DQ21 VMA_DQ22 VMA_DQ23 VMA_DQ24 VMA_DQ25 VMA_DQ26 VMA_DQ27 VMA_DQ28 VMA_DQ29 VMA_DQ30 VMA_DQ31 VMA_DQ32 VMA_DQ33 VMA_DQ34 VMA_DQ35 VMA_DQ36 VMA_DQ37 VMA_DQ38 VMA_DQ39 VMA_DQ40 VMA_DQ41 VMA_DQ42 VMA_DQ43 VMA_DQ44 VMA_DQ45 VMA_DQ46 VMA_DQ47 VMA_DQ48 VMA_DQ49 VMA_DQ50 VMA_DQ51 VMA_DQ52 VMA_DQ53 VMA_DQ54 VMA_DQ55 VMA_DQ56 VMA_DQ57 VMA_DQ58 VMA_DQ59 VMA_DQ60 VMA_DQ61 VMA_DQ62 VMA_DQ63
VMA_DM0 VMA_DM1 VMA_DM2 VMA_DM3 VMA_DM4 VMA_DM5 VMA_DM6 VMA_DM7
VMA_DM[7:0] [23,24]
VMA_WDQS0 VMA_WDQS1 VMA_WDQS2 VMA_WDQS3 VMA_WDQS4 VMA_WDQS5 VMA_WDQS6 VMA_WDQS7
VMA_WDQS[7:0] [23,24]
VMA_RDQS0 VMA_RDQS1 VMA_RDQS2 VMA_RDQS3 VMA_RDQS4 VMA_RDQS5 VMA_RDQS6 VMA_RDQS7
VMA_RDQS[7:0] [23,24]
VMA_DQ[63:0]
VMA_DQ[63:0] [23,24]
FBVDDQ + FBVDD = 3.116A
U1001D
12/14 FBVDDQ
+1.5V_GFX
C1060 0.1U/16V_4
C1061 0.1U/16V_4
C1062 1U/6.3V_4
C1065 1U/6.3V_4
C1066 4.7U/6.3V_6
C1063 4.7U/6.3V_6
C1067 10U/6.3V_6
C1064 22U/6.3V_6
FBVDDQ
FB_CAL_PD_VDDQ D22 FB_CAL_PD_VDDQ R1018 40.2/F_4 +1.5V_GFX
FB_CAL_PU_GND C24 FB_CAL_PU_GND R1019 42.2/F_4
FB_CALTERM_GND B25 FB_CAL_TERM_GND R1020 51.1/F_4
bga595-nvidia-n13p-gv2-s-a2 COMMON
U1001F
13/14 GND
GND
if stuff Da,Ra, do not stuff Ua,Ca,Rb,Rc
GC6_FB_EN
DGPU_VC_EN
D1004 *BAT54CW-7-F
Da
R1123 Ra *100K/F_4
DGPU_FB_EN
For support GC6 2.0
+3V
Ua
U1003 NL17SZ32DFT2G
Ca C1068 0.1U/16V_4
[12,46] DGPU_PWR_EN R1023 *0_4
[44,46] DGPU_VC_EN R1024 0_4
[12,22] GC6_FB_EN
Rc
Rb R1025 100K/F_4
DGPU_FB_EN [45]
if stuff stuff Ua, not stuff PD26
BU5 EE
PROJECT : G34A
Quanta Computer Inc.
BU5
Size Custom
Document Number N16S-GT (MEMORY/GND)
Rev 1A
Date: Tuesday, January 05, 2016
Sheet 20 of 47

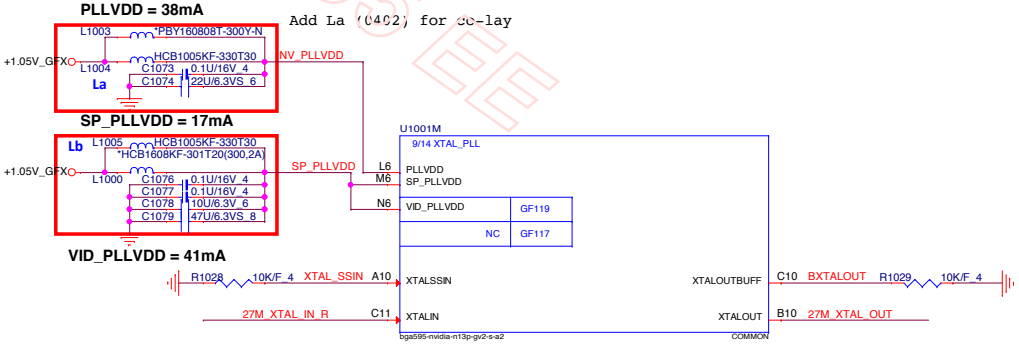


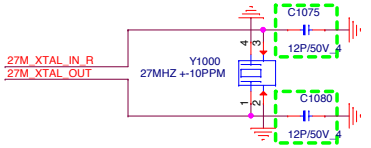


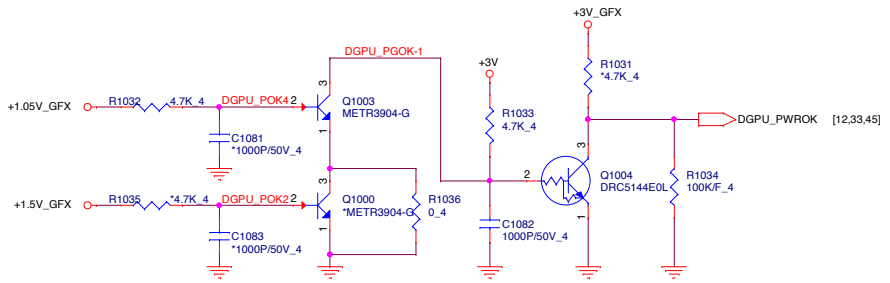












BU5

PROJECT : G34A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N16S-GT (DISPLAY)	1A

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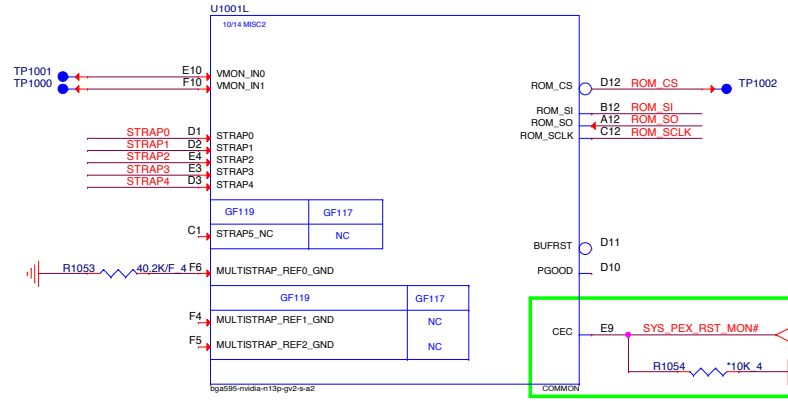
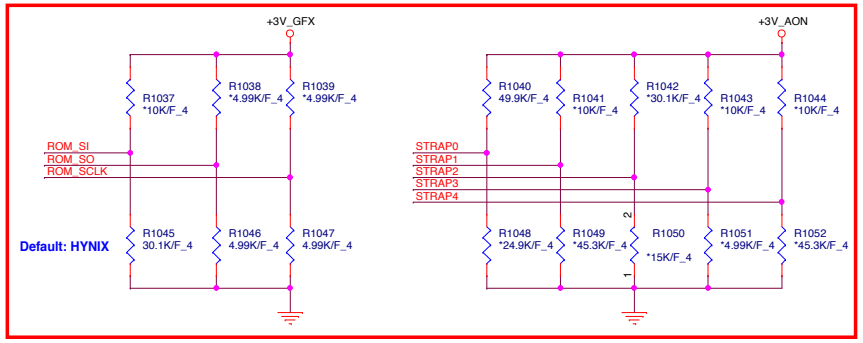
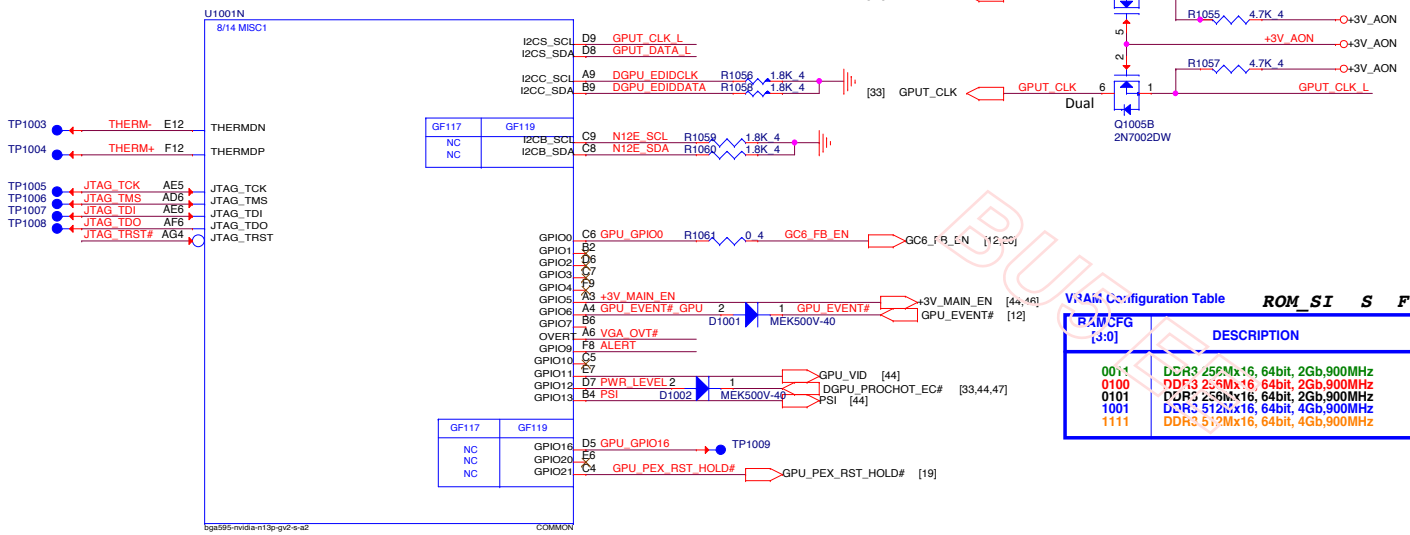




4.99k	CS24992FB26
10k	CS31002FB26
15k	CS31502FB24
20k	CS32002FB29
24.9k	CS32492FB16
30.1k	CS33012FB18
34.8k	CS33482FB06
45.3k	CS34532FB18



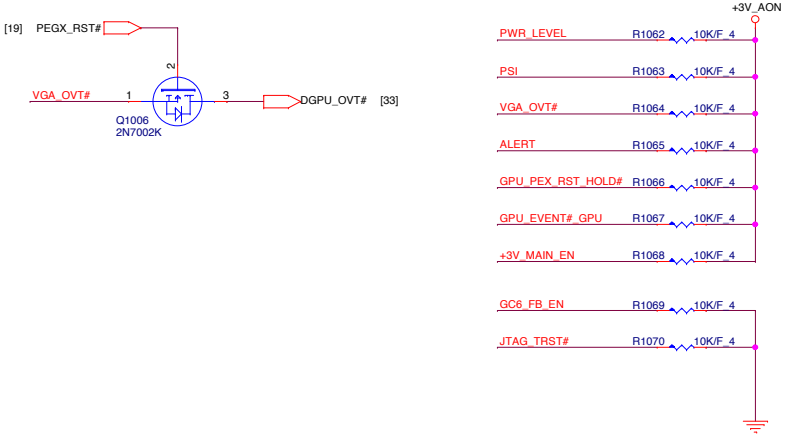


Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

V3A4 Configuration Table

ROM_SI S F

BAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	Straping	TOP B/S	QBC
0011	DDR3 256Mx16, 64bit, 2Gb,900MHz	Micron	MT41J256M16LY-091G:N	0x3	AKD59GSTL01	AKD59GSTL00
0100	DDR3 256Mx16, 64bit, 2Gb,900MHz	SAMSUNG	K4W4G1646E-BC1A	0x4	AKD5PGDT500	AKD5PGDT501
0101	DDR3 256Mx16, 64bit, 2Gb,900MHz	HYNIX	H5TC4G63CFR-NOC	0x5	AKD5PZDTW01	AKD5PZDTW02
1001	DDR3 512Mx16, 64bit, 4Gb,900MHz	Micron	MT41K512M16HA-107G:A	0x9	AKD5QGSTL05	AKD5QGSTL09
1111	DDR3 512Mx16, 64bit, 4Gb,900MHz	HYNIX	H5TC8G63CMR-11C	0xF	AKD5QFDTW00	AKD5QFDTW01

GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor
1	OUT	MEM_VDD_CTL	Memory VDD VID
2	OUT	LCD_BL_PWM	Panel Backlight PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	Reserved	--
6	OUT	FB_CLAMP_TGL_REQ	Active low FB Clamp toggle request
7	OUT	3D VISION	3D VISION LEFT/RIGHT signal
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM VREF_CTL	MEMMORY VREF CONTROL
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding

BU5

PROJECT : G34A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N16S-GT (GPIO/STRAPS)	1A

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Rank0

HYU 256Mx16, H5TC4G63CFR-N0C QBC PN : AKD5PZDTW02---TOP B/S PN : AKD5P2DTW01
MIC 256Mx16, MT41J256M16LY-091G:N QBC PN : AKD59GSTL00---TOP B/S PN : AKD59GSTL01
SAM 256Mx16, K4W4G1646E-BC1A QBC PN : AKD5PGDT501---TOP B/S PN : AKD5PGDT500

U1004

VREFC_VMA1 M8 VREFCA
VREFD_VMA1 H1 VREFDQ

[20,24] FBA_CMD9 N3
[20,24] FBA_CMD11 P7
[20,24] FBA_CMD8 P3
[20,24] FBA_CMD25 N2
[20,24] FBA_CMD10 P8
[20,24] FBA_CMD24 P2
[20,24] FBA_CMD22 R8
[20,24] FBA_CMD7 R2
[20,24] FBA_CMD21 T8
[20,24] FBA_CMD6 R3
[20,24] FBA_CMD29 L7
[20,24] FBA_CMD23 R7
[20,24] FBA_CMD28 N7
[20,24] FBA_CMD20 T3
[20,24] FBA_CMD4 T7
[20,24] FBA_CMD14 M7
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12/BC A13 A14 A15

[20,24] FBA_CMD12 M2
[20,24] FBA_CMD27 N8
[20,24] FBA_CMD26 M3
BA0 BA1 BA2

[20] VMA_CLK0 J7
[20] VMA_CLK0# K7
[20] FBA_CMD3 K9
CK CK CKE

[20] FBA_CMD2 K1
[20] FBA_CMD0 L2
[20,24] FBA_CMD30 J3
[20,24] FBA_CMD15 K3
[20,24] FBA_CMD13 L3
ODT CS RAS CAS WE

[20] VMA_WDQS1 F3
[20] VMA_RDQS1 G3
DQSL DQSL

[20] VMA_DM1 E7
[20] VMA_DM2 D3
DML DMU

[20] VMA_WDQS2 C7
[20] VMA_RDQS2 B7
DQSU DQSU

[20,24] FBA_CMD5 T2
RESET

GND — 243_4 R1072 — FBA_ZQ0 L8 — ZQ

DQL0 E3 DQL1 F7 DQL2 F2 DQL3 F8 DQL4 H3 DQL5 H8 DQL6 G2 DQL7 H7
VMA_DQ11 [20] VMA_DQ14 [20] VMA_DQ8 [20] VMA_DQ13 [20] VMA_DQ10 [20] VMA_DQ12 [20] VMA_DQ9 [20] VMA_DQ15 [20]

DQU0 D7 DQU1 C3 DQU2 C8 DQU3 C2 DQU4 A7 DQU5 A2 DQU6 B8 DQU7 A3
VMA_DQ17 [20] VMA_DQ21 [20] VMA_DQ18 [20] VMA_DQ22 [20] VMA_DQ19 [20] VMA_DQ23 [20] VMA_DQ16 [20] VMA_DQ20 [20]

VDD#B2 B2 VDD#D9 D9 VDD#G7 G7 VDD#K2 K2 VDD#K8 K8 VDD#N1 N1 VDD#N9 N9 VDD#R1 R1 VDD#R9 R9
1.5V_GFX — 4.7U/6.3V_6 C1084 — 0.1U/16V_4 C1085 — 0.1U/16V_4 C1086 — GND

VDDQ#A1 A1 VDDQ#A8 A8 VDDQ#C1 C1 VDDQ#C9 C9 VDDQ#D2 D2 VDDQ#E9 E9 VDDQ#F1 F1 VDDQ#H2 H2 VDDQ#H9 H9
1.5V_GFX — 4.7U/6.3V_6 C1090 — 0.1U/16V_4 C1091 — 0.1U/16V_4 C1092 — GND

VSS#A9 A9 VSS#B3 B3 VSS#E1 E1 VSS#G8 G8 VSS#J2 J2 VSS#J8 J8 VSS#M1 M1 VSS#M9 M9 VSS#P1 P1 VSS#P9 P9 VSS#T1 T1 VSS#T9 T9
GND

VSSQ#B1 B1 VSSQ#B9 B9 VSSQ#D1 D1 VSSQ#D8 D8 VSSQ#E2 E2 VSSQ#E8 E8 VSSQ#F9 F9 VSSQ#G1 G1 VSSQ#G9 G9

[20] FBA_CMD1 — FBA_CMD2 J1 — FBA_CMD1 L1 — FBA_CMD3 J9 — FBA_ZQ2 L9
NC#J1 NC#L1 NC#J9 NC#L9
GND — 243_4 R1124

96-BALL SDRAM DDR3 VRAM _DDR3_HYNIX_256MX16

stuff R1124 for
Hynix 8Gb DDP VRAM

reserve for Hynix 8Gb DDP VRAM

SDDR3_BGA100

	0..31	32..63
CMD0	CS0*	
CMD1	CS1*	
CMD2	ODT	
CMD3	CKE	
CMD16		CS0*
CMD17		CS1*
CMD18		ODT
CMD19		CKE

SNN_FBAO_ODT1	J1	NC/ODT1
SNN_FBAO_CKE1	J9	NC/CKE1
SNN_FBAO_CS1	L1	NC/CS1
SNN_FBAO_ZQ1	L9	NC/ZQ1

162_1% ohm CS11622FB07 RES CHIP 162 1/16W +-1%(0402)
CS11622FB15 RES CHIP 162 1/16W +-1%(0402)

VMA_CLK0 — R1071 162_4 — VMA_CLK0#

+1.5V_GFX — R1073 1.33K/F_4 — VREFC_VMA1 — R1076 1.33K/F_4 — C1096 0.01U/50V_4
+1.5V_GFX — R1074 1.33K/F_4 — VREFD_VMA1 — R1077 1.33K/F_4 — C1097 0.01U/50V_4

+1.5V_GFX — C1103 1U/6.3V_4 — C1106 1U/6.3V_4 — C1108 1U/6.3V_4 — C1111 1U/6.3V_4
+1.5V_GFX — C1104 1U/6.3V_4 — C1107 1U/6.3V_4 — C1109 1U/6.3V_4 — C1112 1U/6.3V_4
+1.5V_GFX — C1098 10U/6.3V_6 — C1099 10U/6.3V_6 — C1100 10U/6.3V_6 — C1101 0.1U/16V_4 — C1102 0.1U/16V_4 — C1105 0.1U/16V_4 — C1110 0.1U/16V_4 — C1113 0.1U/16V_4 — C1114 0.1U/16V_4

U1005

VREFC_VMA1 M8 VREFCA
VREFD_VMA1 H1 VREFDQ

FBA_CMD9 N3
FBA_CMD11 P7
FBA_CMD8 P3
FBA_CMD25 N2
FBA_CMD10 P8
FBA_CMD24 P2
FBA_CMD22 R8
FBA_CMD7 R2
FBA_CMD21 T8
FBA_CMD6 R3
FBA_CMD29 L7
FBA_CMD23 R7
FBA_CMD28 N7
FBA_CMD20 T3
FBA_CMD4 T7
FBA_CMD14 M7
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12/BC A13 A14 A15

FBA_CMD12 M2
FBA_CMD27 N8
FBA_CMD26 M3
BA0 BA1 BA2

VMA_CLK0 J7
VMA_CLK0# K7
FBA_CMD3 K9
CK CK CKE

FBA_CMD2 K1
FBA_CMD0 L2
FBA_CMD30 J3
FBA_CMD15 K3
FBA_CMD13 L3
ODT CS RAS CAS WE

[20] VMA_WDQS0 F3
[20] VMA_RDQS0 G3
DQSL DQSL

[20] VMA_DM0 E7
[20] VMA_DM3 D3
DML DMU

[20] VMA_WDQS3 C7
[20] VMA_RDQS3 B7
DQSU DQSU

FBA_CMD5 T2
RESET

GND — 243_4 R1075 — FBA_ZQ1 L8 — ZQ

DQL0 E3 DQL1 F7 DQL2 F2 DQL3 F8 DQL4 H3 DQL5 G2 DQL6 H7 DQL7
VMA_DQ1 [20] VMA_DQ4 [20] VMA_DQ3 [20] VMA_DQ6 [20] VMA_DQ0 [20] VMA_DQ7 [20] VMA_DQ2 [20] VMA_DQ5 [20]

DQU0 D7 DQU1 C3 DQU2 C8 DQU3 C2 DQU4 A7 DQU5 A2 DQU6 B8 DQU7 A3
VMA_DQ25 [20] VMA_DQ28 [20] VMA_DQ24 [20] VMA_DQ29 [20] VMA_DQ26 [20] VMA_DQ30 [20] VMA_DQ27 [20] VMA_DQ31 [20]

VDD#B2 B2 VDD#D9 D9 VDD#G7 G7 VDD#K2 K2 VDD#K8 K8 VDD#N1 N1 VDD#N9 N9 VDD#R1 R1 VDD#R9 R9
1.5V_GFX — 4.7U/6.3V_6 C1087 — 0.1U/16V_4 C1088 — 0.1U/16V_4 C1089 — GND

VDDQ#A1 A1 VDDQ#A8 A8 VDDQ#C1 C1 VDDQ#C9 C9 VDDQ#D2 D2 VDDQ#E9 E9 VDDQ#F1 F1 VDDQ#H2 H2 VDDQ#H9 H9
1.5V_GFX — 4.7U/6.3V_6 C1093 — 0.1U/16V_4 C1094 — 0.1U/16V_4 C1095 — GND

VSS#A9 A9 VSS#B3 B3 VSS#E1 E1 VSS#G8 G8 VSS#J2 J2 VSS#J8 J8 VSS#M1 M1 VSS#M9 M9 VSS#P1 P1 VSS#P9 P9 VSS#T1 T1 VSS#T9 T9
GND

VSSQ#B1 B1 VSSQ#B9 B9 VSSQ#D1 D1 VSSQ#D8 D8 VSSQ#E2 E2 VSSQ#E8 E8 VSSQ#F9 F9 VSSQ#G1 G1 VSSQ#G9 G9

FBA_CMD2 J1 — FBA_CMD1 L1 — FBA_CMD3 J9 — FBA_ZQ3 L9
NC#J1 NC#L1 NC#J9 NC#L9
GND — 243_4 R1125

96-BALL SDRAM DDR3 VRAM _DDR3_HYNIX_256MX16

stuff R1125 for
Hynix 8Gb DDP VRAM

BU5

PROJECT : G34A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3L - RANK0	1A

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Rank0

HYU 256Mx16, H5TC4G63CFR-NOC QBC PN : AKD5PZDTW02---TOP B/S PN : AKD5PZDTW01
MIC 256Mx16, MT41J256M16LY-091G:N QBC PN : AKD59GSTL00---TOP B/S PN : AKD59GSTL01
SAM 256Mx16, K4W4G1646E-BC1A QBC PN : AKD5PGDT501---TOP B/S PN : AKD5PGDT500

U1006

VREFC_VMA3 M8 VREFCA
VREFD_VMA3 H1 VREFDQ

[20,23] FBA_CMD9 N3 A0
[20,23] FBA_CMD11 P7 A1
[20,23] FBA_CMD8 P3 A2
[20,23] FBA_CMD25 N2 A3
[20,23] FBA_CMD10 P8 A4
[20,23] FBA_CMD24 P2 A5
[20,23] FBA_CMD22 R8 A6
[20,23] FBA_CMD7 R2 A7
[20,23] FBA_CMD21 T8 A8
[20,23] FBA_CMD6 R3 A9
[20,23] FBA_CMD29 L7 A10/AP
[20,23] FBA_CMD23 R7 A11
[20,23] FBA_CMD28 N7 A12/BC
[20,23] FBA_CMD20 T3 A13
[20,23] FBA_CMD4 T7 A14
[20,23] FBA_CMD14 M7 A15

[20,23] FBA_CMD12 M2 BA0
[20,23] FBA_CMD27 N8 BA1
[20,23] FBA_CMD26 M3 BA2

[20] VMA_CLK1 J7 CK
[20] VMA_CLK1# K7 CK
[20] FBA_CMD19 K9 CKE

[20] FBA_CMD18 K1 ODT
[20] FBA_CMD16 L2 CS
[20,23] FBA_CMD30 J3 RAS
[20,23] FBA_CMD15 K3 CAS
[20,23] FBA_CMD13 L3 WE

[20] VMA_WDQS4 F3 DQSL
[20] VMA_RDQS4 G3 DQSL

[20] VMA_DM4 E7 DML
[20] VMA_DM7 D3 DMU

[20] VMA_WDQS7 C7 DQSU
[20] VMA_RDQS7 B7 DQSU

[20,23] FBA_CMD5 T2 RESET

GND — FBA_ZQ4 — L8 ZQ
243_4 R1079

[20] FBA_CMD17 J1 NC#J1
FBA_CMD18 L1 NC#L1
FBA_CMD19 J9 NC#J9
FBA_ZQ6 L9 NC#L9
GND — 243_4 R1126

96-BALL SDRAM DDR3
VRAM _DDR3_HYNIX_256MX16

stuff R1124 for
Hynix 8Gb DDP VRAM

DQL0 E3 … DQL7 H7
VMA_DQ34 … VMA_DQ36 [20]

DQU0 D7 … DQU7 A3
VMA_DQ57 … VMA_DQ60 [20]

VDD#B2 B2 … VDD#R9 R9
1.5V_GFX
4.7U/6.3V_6 C1115
0.1U/16V_4 C1116
0.1U/16V_4 C1117
GND

VDDQ#A1 A1 … VDDQ#H9 H9
1.5V_GFX
4.7U/6.3V_6 C1121
0.1U/16V_4 C1122
0.1U/16V_4 C1123
GND

VSS#A9 A9 … VSS#T9 T9
GND

VSSQ#B1 B1 … VSSQ#G9 G9

162_1% ohm CS11622FB07 RES CHIP 162 1/16W +-1%(0402)
CS11622FB15 RES CHIP 162 1/16W +-1%(0402)

VMA_CLK1 — R1078 162_4 — VMA_CLK1#

+1.5V_GFX
R1081 1.33K/F_4 — VREFC_VMA3 — R1083 1.33K/F_4 — C1127 0.01U/50V_4
+1.5V_GFX
R1082 1.33K/F_4 — VREFD_VMA3 — R1084 1.33K/F_4 — C1128 0.01U/50V_4

+1.5V_GFX
C1134 1U/6.3V_4
C1137 1U/6.3V_4
C1139 1U/6.3V_4
C1142 1U/6.3V_4

+1.5V_GFX
C1135 1U/6.3V_4
C1138 1U/6.3V_4
C1140 1U/6.3V_4
C1143 1U/6.3V_4

+1.5V_GFX
C1129 10U/6.3V_6
C1130 10U/6.3V_6
C1131 10U/6.3V_6
C1132 0.1U/16V_4
C1133 0.1U/16V_4
C1136 0.1U/16V_4
C1141 0.1U/16V_4
C1144 0.1U/16V_4
C1145 0.1U/16V_4

U1007

VREFC_VMA3 M8 VREFCA
VREFD_VMA3 H1 VREFDQ

FBA_CMD9 N3 A0
FBA_CMD11 P7 A1
FBA_CMD8 P3 A2
FBA_CMD25 N2 A3
FBA_CMD10 P8 A4
FBA_CMD24 P2 A5
FBA_CMD22 R8 A6
FBA_CMD7 R2 A7
FBA_CMD21 T8 A8
FBA_CMD6 R3 A9
FBA_CMD29 L7 A10/AP
FBA_CMD23 R7 A11
FBA_CMD28 N7 A12/BC
FBA_CMD20 T3 A13
FBA_CMD4 T7 A14
FBA_CMD14 M7 A15

FBA_CMD12 M2 BA0
FBA_CMD27 N8 BA1
FBA_CMD26 M3 BA2

VMA_CLK1 J7 CK
VMA_CLK1# K7 CK
FBA_CMD19 K9 CKE

FBA_CMD18 K1 ODT
FBA_CMD16 L2 CS
FBA_CMD30 J3 RAS
FBA_CMD15 K3 CAS
FBA_CMD13 L3 WE

[20] VMA_WDQS5 F3 DQSL
[20] VMA_RDQS5 G3 DQSL

[20] VMA_DM5 E7 DML
[20] VMA_DM6 D3 DMU

[20] VMA_WDQS6 C7 DQSU
[20] VMA_RDQS6 B7 DQSU

FBA_CMD5 T2 RESET

GND — FBA_ZQ5 — L8 ZQ
243_4 R1080

FBA_CMD18 J1 NC#J1
FBA_CMD17 L1 NC#L1
FBA_CMD19 J9 NC#J9
FBA_ZQ7 L9 NC#L9
GND — 243_4 R1127

96-BALL SDRAM DDR3
VRAM _DDR3_HYNIX_256MX16

stuff R1124 for
Hynix 8Gb DDP VRAM

DQL0 E3 … DQL7 H7
VMA_DQ41 … VMA_DQ44 [20]

DQU0 D7 … DQU7 A3
VMA_DQ51 … VMA_DQ53 [20]

VDD#B2 B2 … VDD#R9 R9
1.5V_GFX
4.7U/6.3V_6 C1118
0.1U/16V_4 C1119
0.1U/16V_4 C1120
GND

VDDQ#A1 A1 … VDDQ#H9 H9
1.5V_GFX
4.7U/6.3V_6 C1124
0.1U/16V_4 C1125
0.1U/16V_4 C1126
GND

VSS#A9 A9 … VSS#T9 T9
GND

VSSQ#B1 B1 … VSSQ#G9 G9

BU5

PROJECT : G34A
Quanta Computer Inc.

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Custom	DDR3L - RANK0	1A

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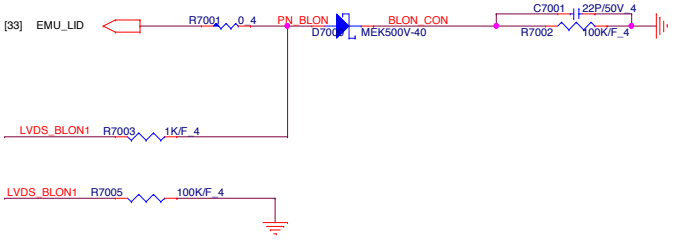
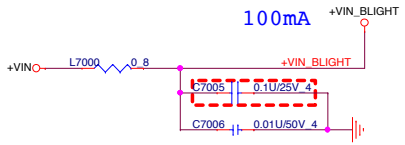
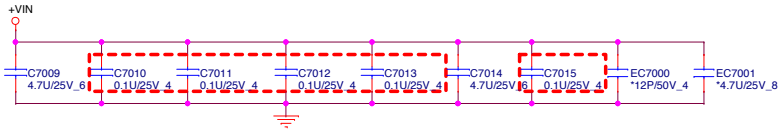
LID Switch

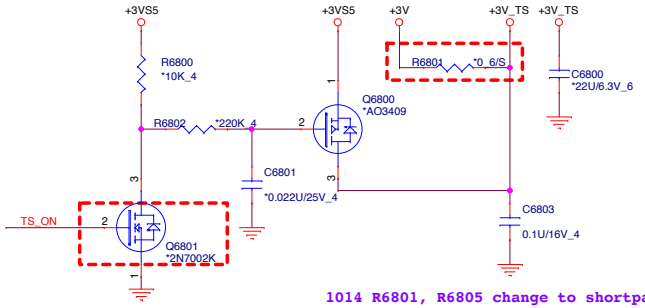




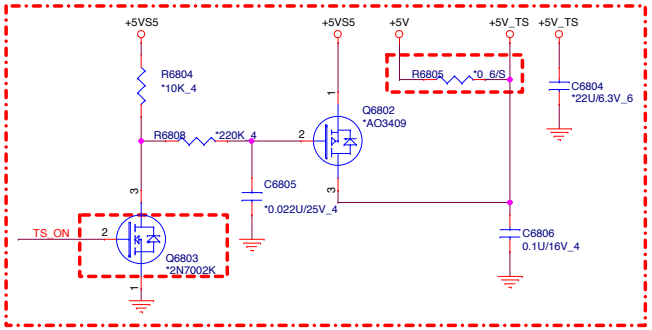
1022 change to CH4104K9B03 0402



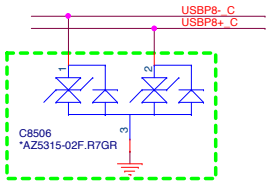
Touch screen



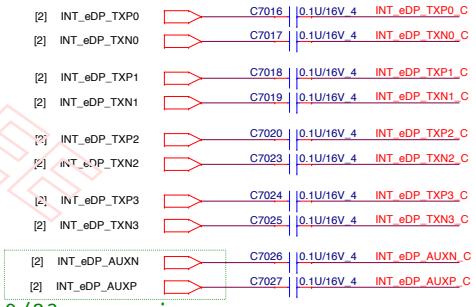
1014 R6801, R6805 change to shortpad



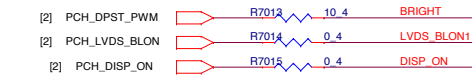
eDP Conn.

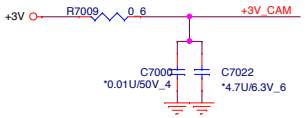


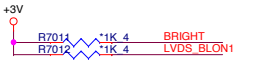
TS USB Interface

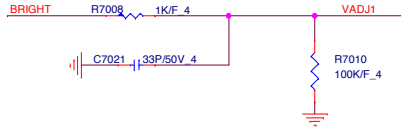


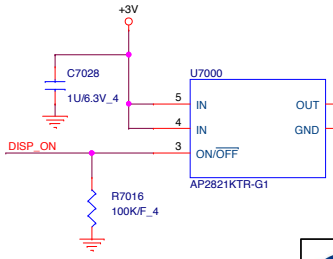
9/23 swap pin

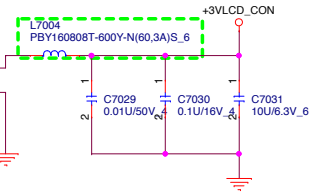


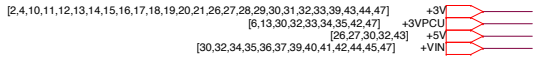












BU5

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Quanta Computer Inc.

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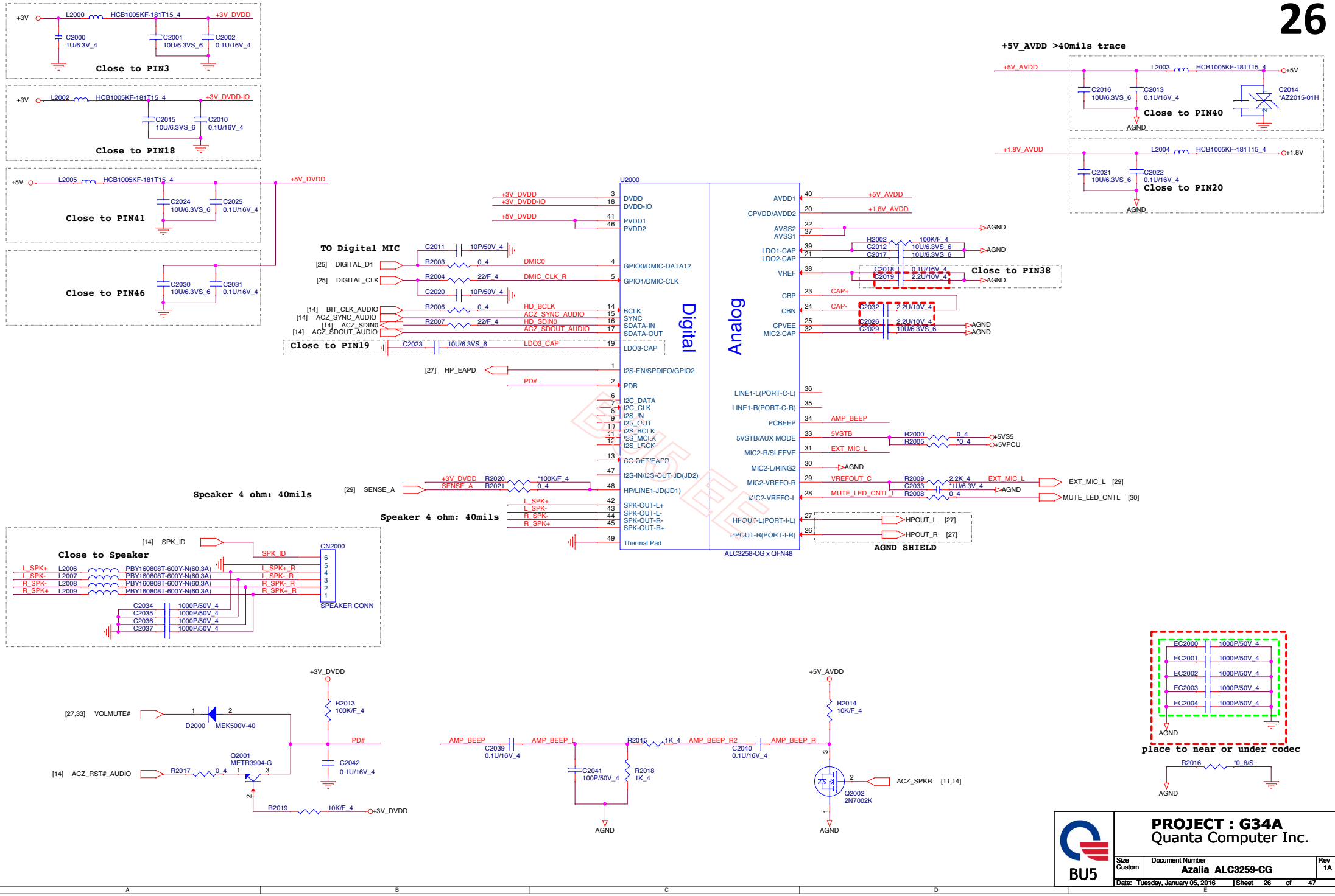

BU5	PROJECT : G34A Quanta Computer Inc.		
	Size: Custom	Document Number: Azalia ALC3259-CG	Rev: 1A
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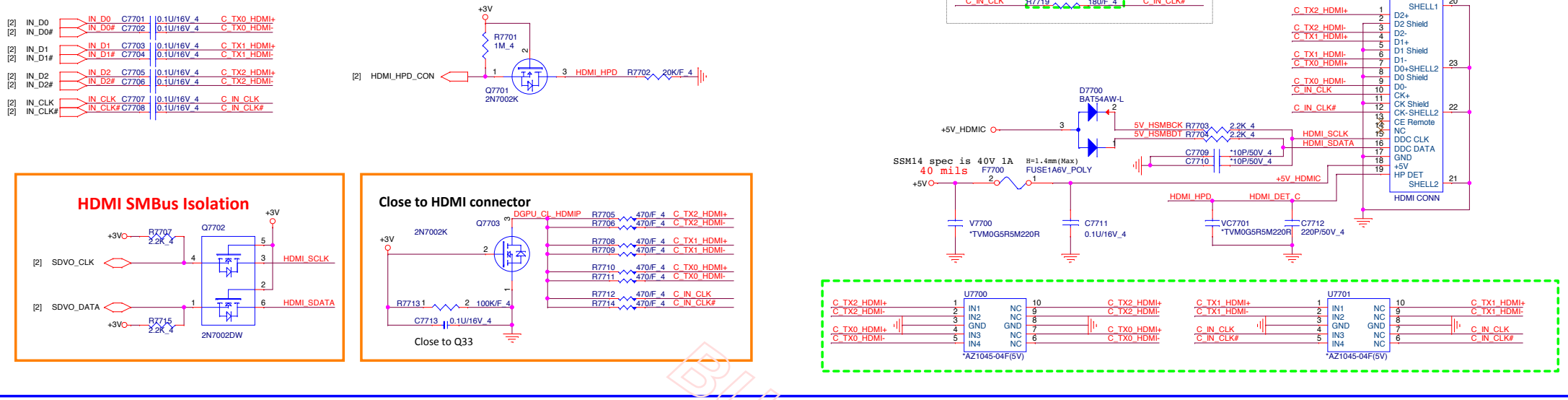
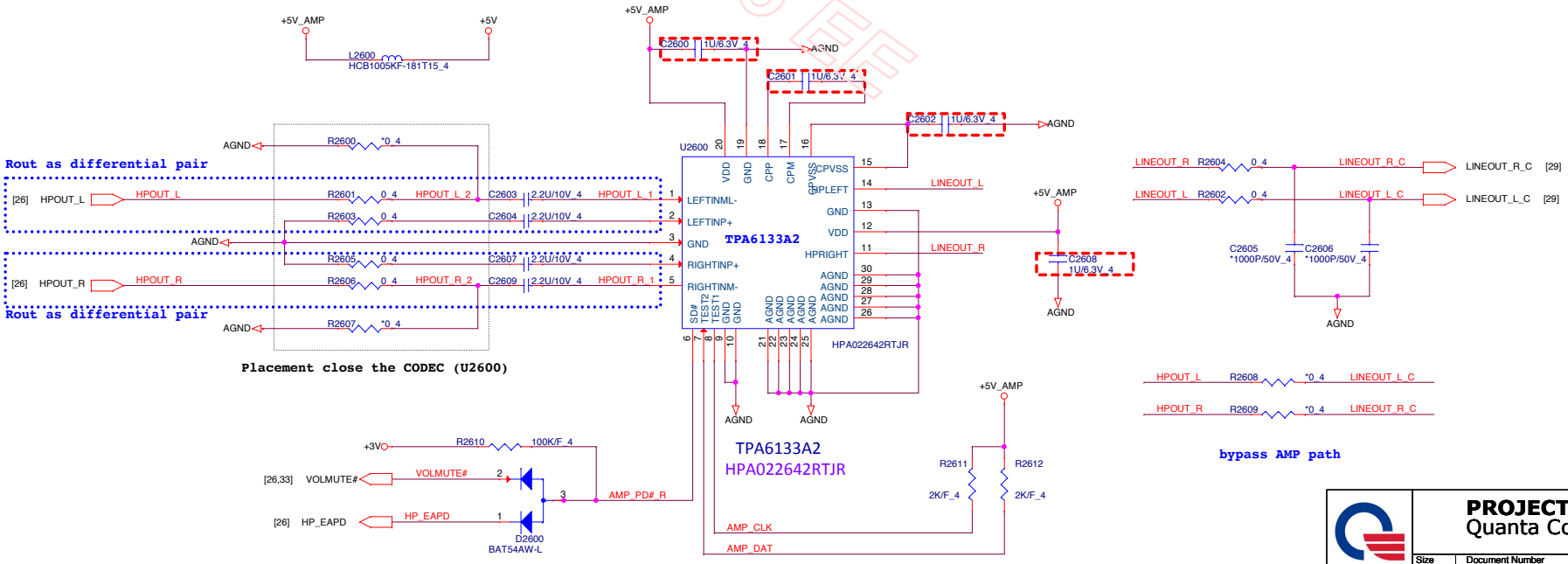
HDMI CONN



Head Phone out



BU5

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Quanta Computer Inc.

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LAN & RJ45

For SWR mode support RTL8111HSH/RTL8107ESH

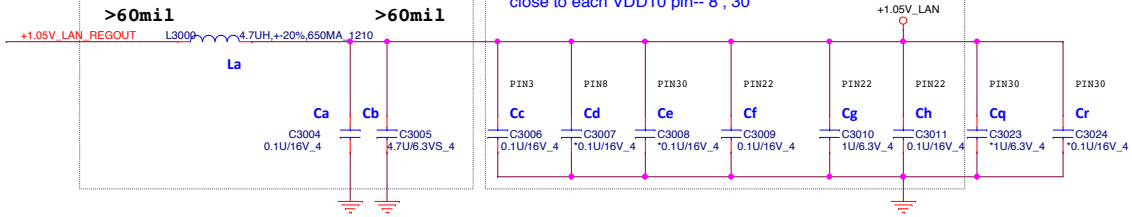
Stuff La, Ca ,Cb

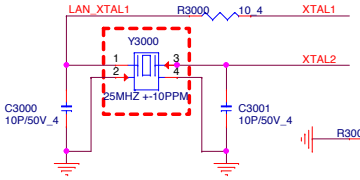
For LDO mode support RTL8166EH

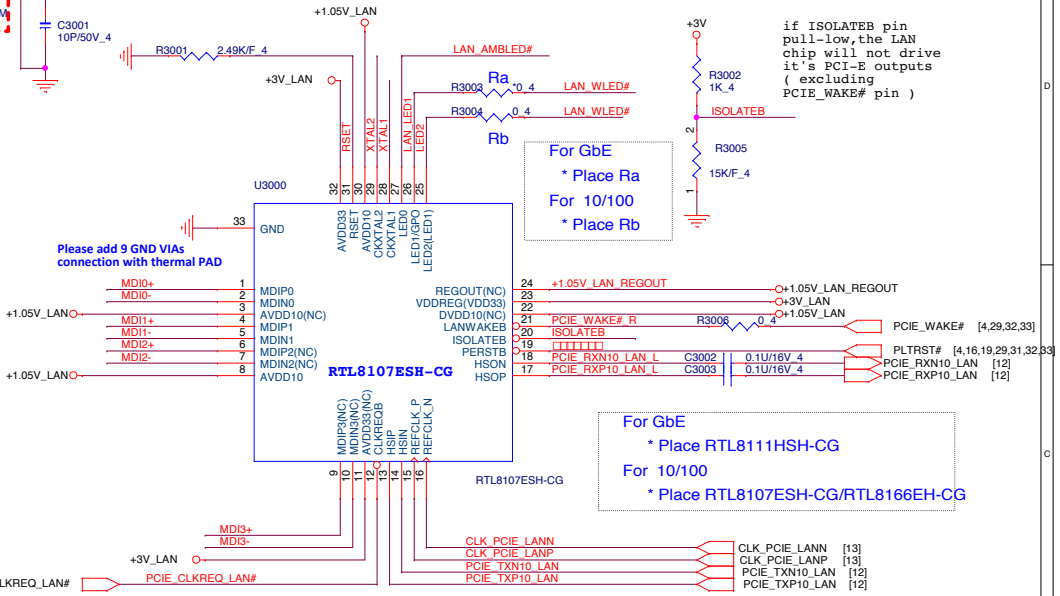
NA : La, Ca, Cb

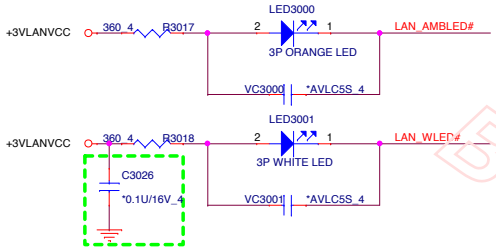
* Place Cc,Cd,Ce,Cf for RTL8111H(S) & RTL8107E(S) close to each VDD10 pin-- 3, 22, 8 , 30
* Place Cg,Ch for RTL8111H(S) & RTL8107E(S) close to each VDD10 pin-- 22(reserved)
* Place Cq,Cr for RTL8166EH close to each VDD10 pin-- 30(reserved)
* Place Ce,Cd for RTL8166EH close to each VDD10 pin-- 8 , 30

Power trace Layout 寬度> 60mil

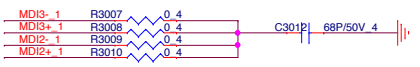




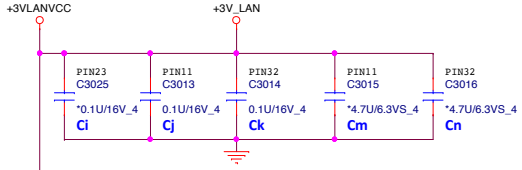


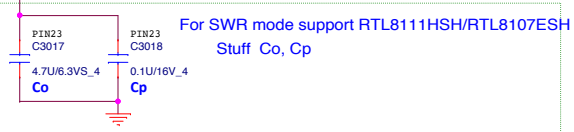


For 10/100 stuff only **Close RJ45**



* Place Ci and Ck, close to each VDD33 pin-- 23, 32 for RTL8166EH
* Place Cj and Ck, close to each VDD33 pin-- 11, 32 for RTL8111H(S) & RTL8107E(S)
* For surge improvement, place Cm and Cn, close to each VDD33 pin-- 11, 32(optional)

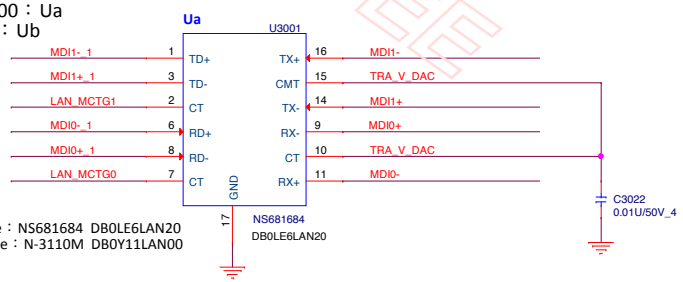




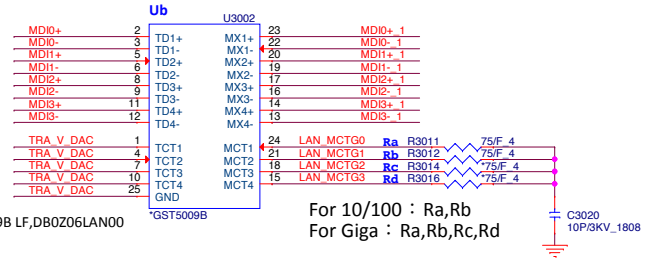
For SWR mode support RTL8111HSH/RTL8107ESH

Stuff Co, Cp

For 10/100：Ua
For Giga：Ub

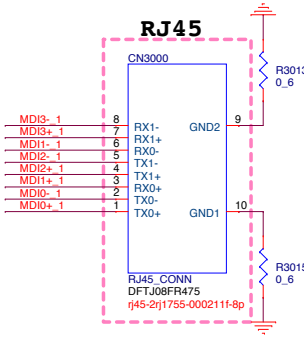


1st source：NS681684 DB0LE6LAN20
2nd source：N-3110M DB0Y11LAN00



For GiGA
BOT:GST5009B LF,DB0Z06LAN00

For 10/100：Ra,Rb
For Giga：Ra,Rb,Rc,Rd



[2,4,10,11,12,13,14,15,16,17,18,19,20,21,25,26,27,29,30,31,32,33,39,43,44,47] +3V
[43] +3VLANVCC

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	Size: Custom	Document Number: LAN RTL8107ESH-CG/RJ45	Rev: 1A
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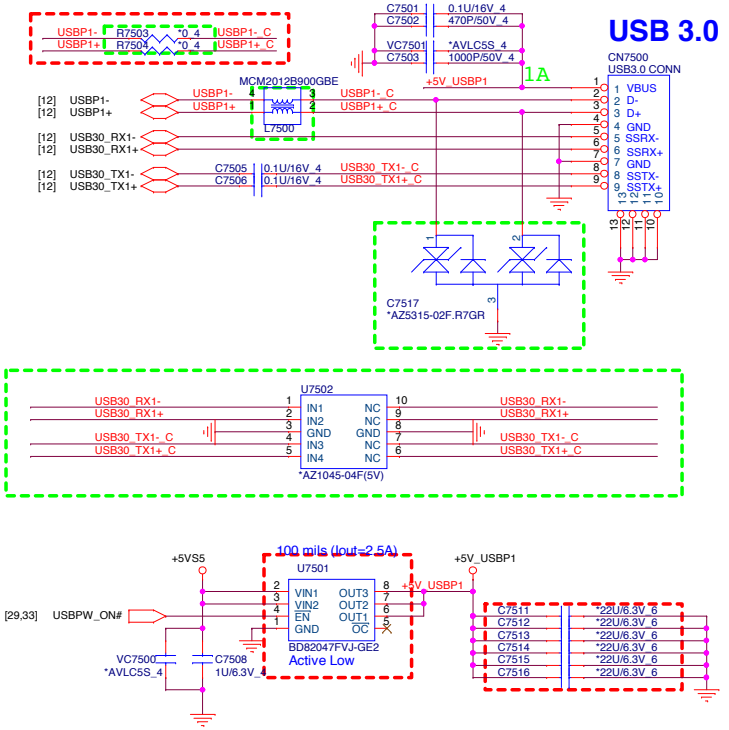
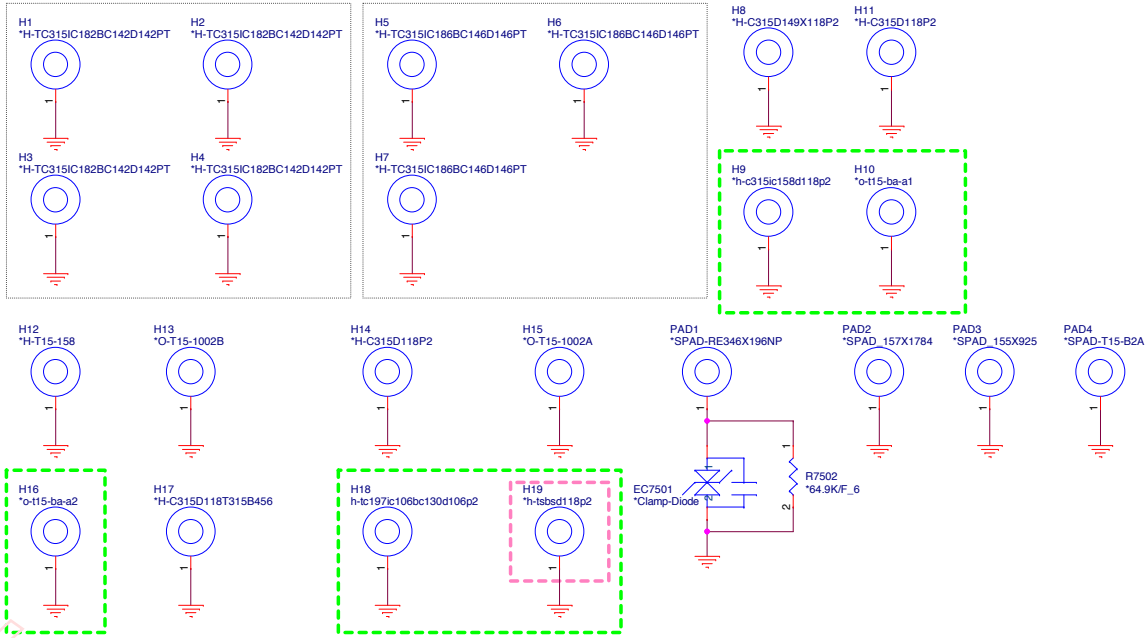
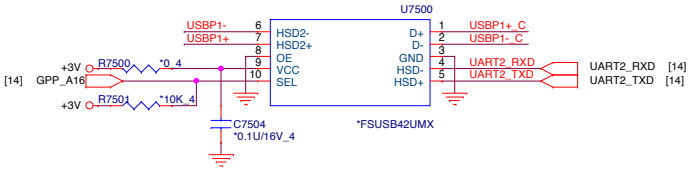
USB 2.0/3.0 Combo



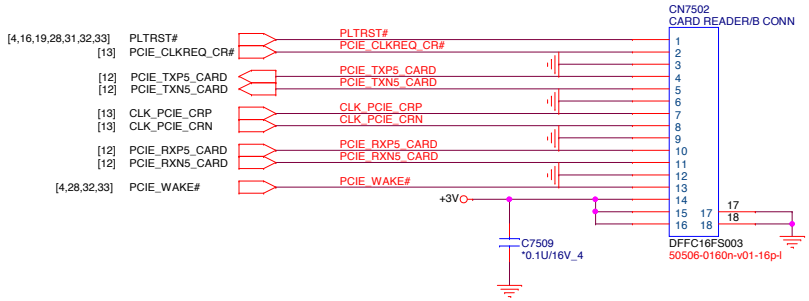
Holes



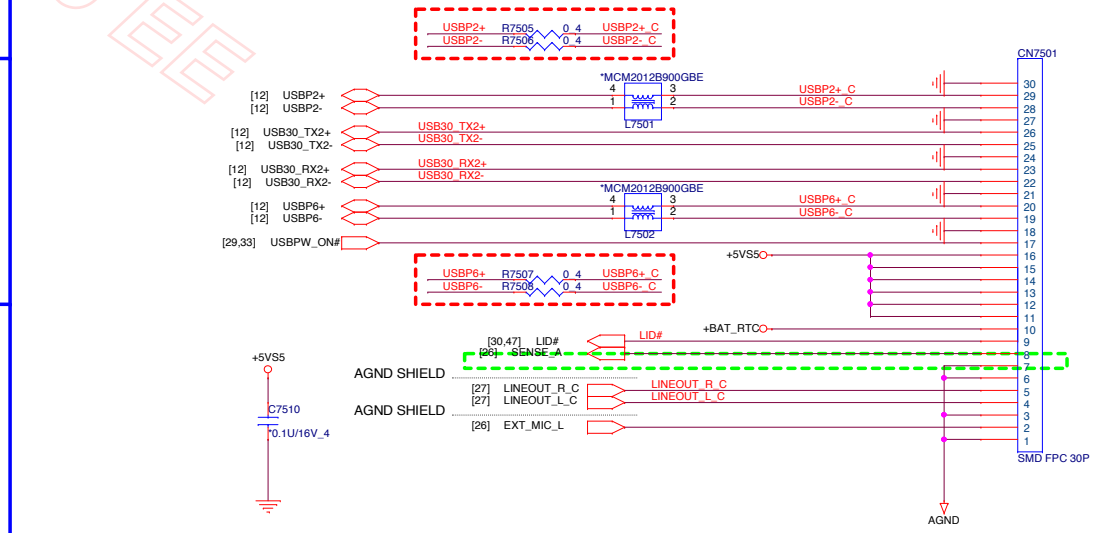
UART for DEBUG



Card Reader Connector



USB Phone Jack Connector



+3VPCU [6,13,30,32,33,34,35,42,47]
+5VS5 [4,25,26,35,36,37,38,39,40,41,43,44,45,46]
+BAT_RTC [4,13,15,30,34,47]
+3V [2,4,10,11,12,13,14,15,16,17,18,19,20,21,25,26,27,28,30,31,32,33,39,43,44,47]

BU5

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Quanta Computer Inc.

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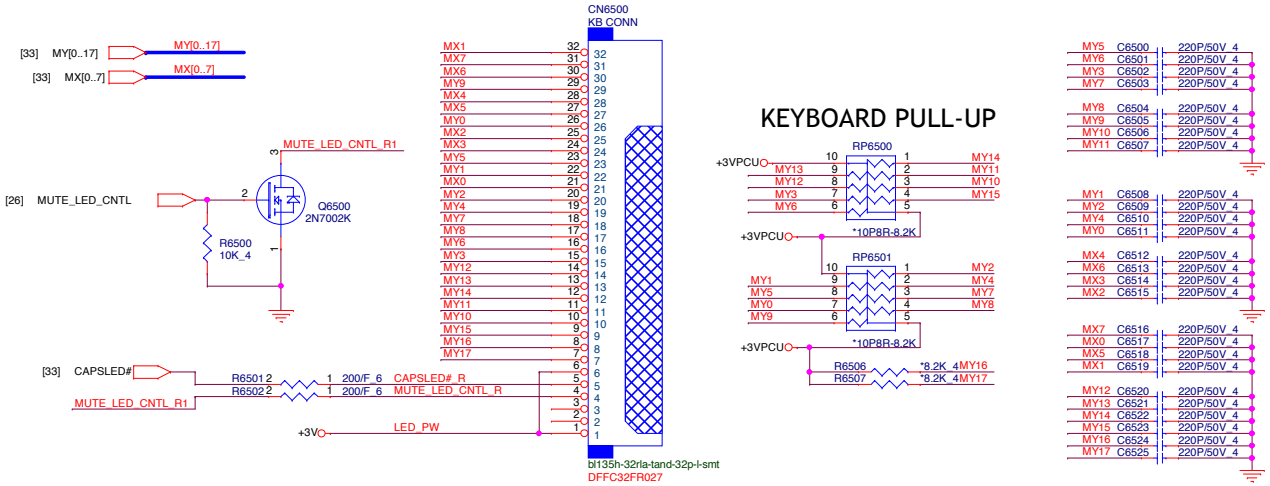
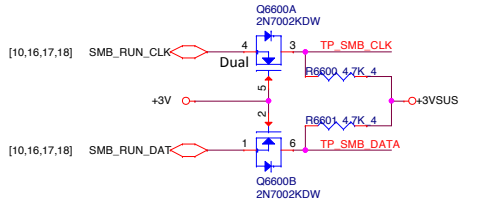
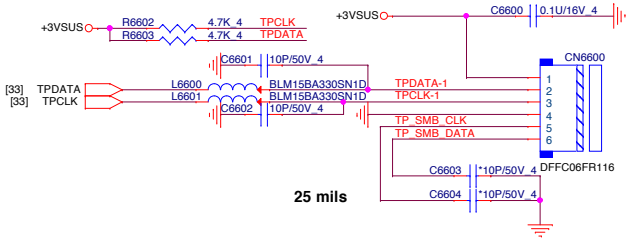
KEYBOARD Con.



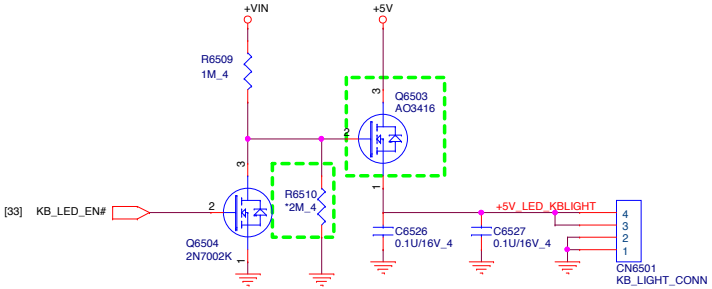
KEYBOARD PULL-UP

Touch Pad Connector

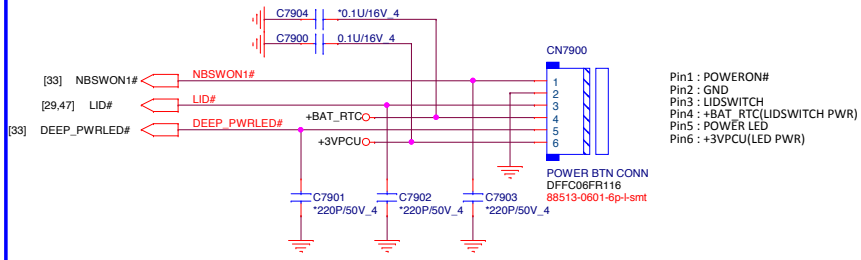




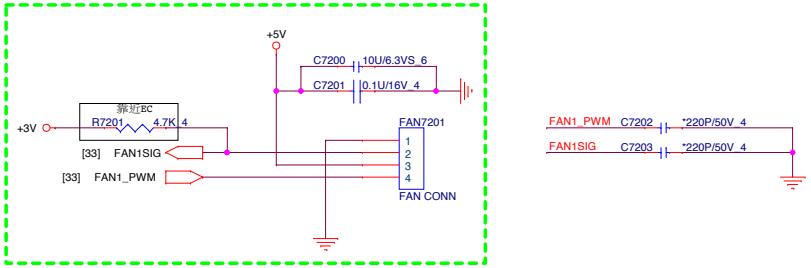
KB LIGHT CONN



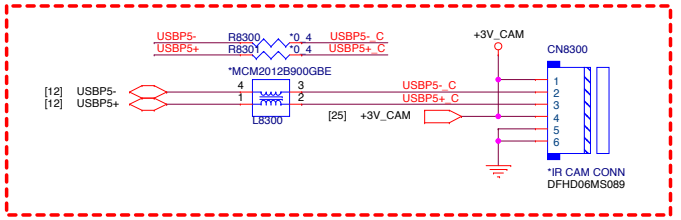
Power Botton Connector



FAN CONN



IR CAM



1015 Add IR CAM circuit

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Quanta Computer Inc.

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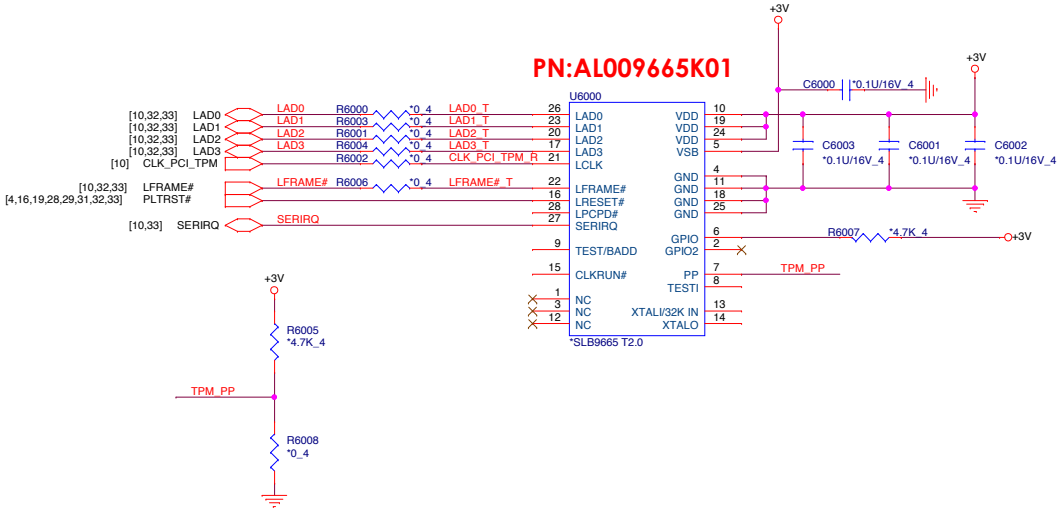
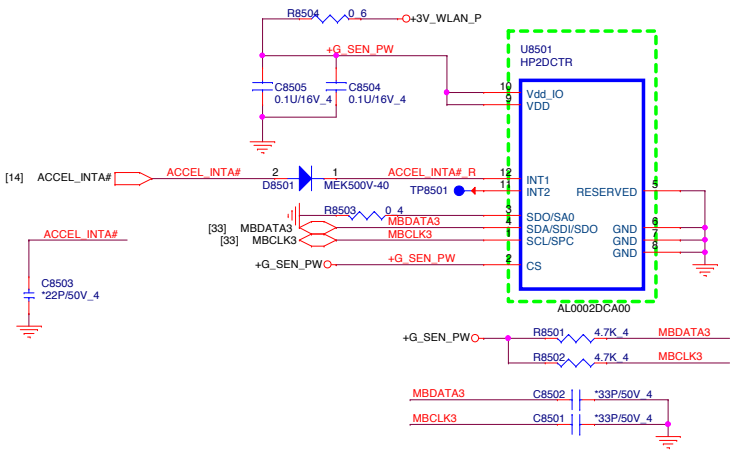
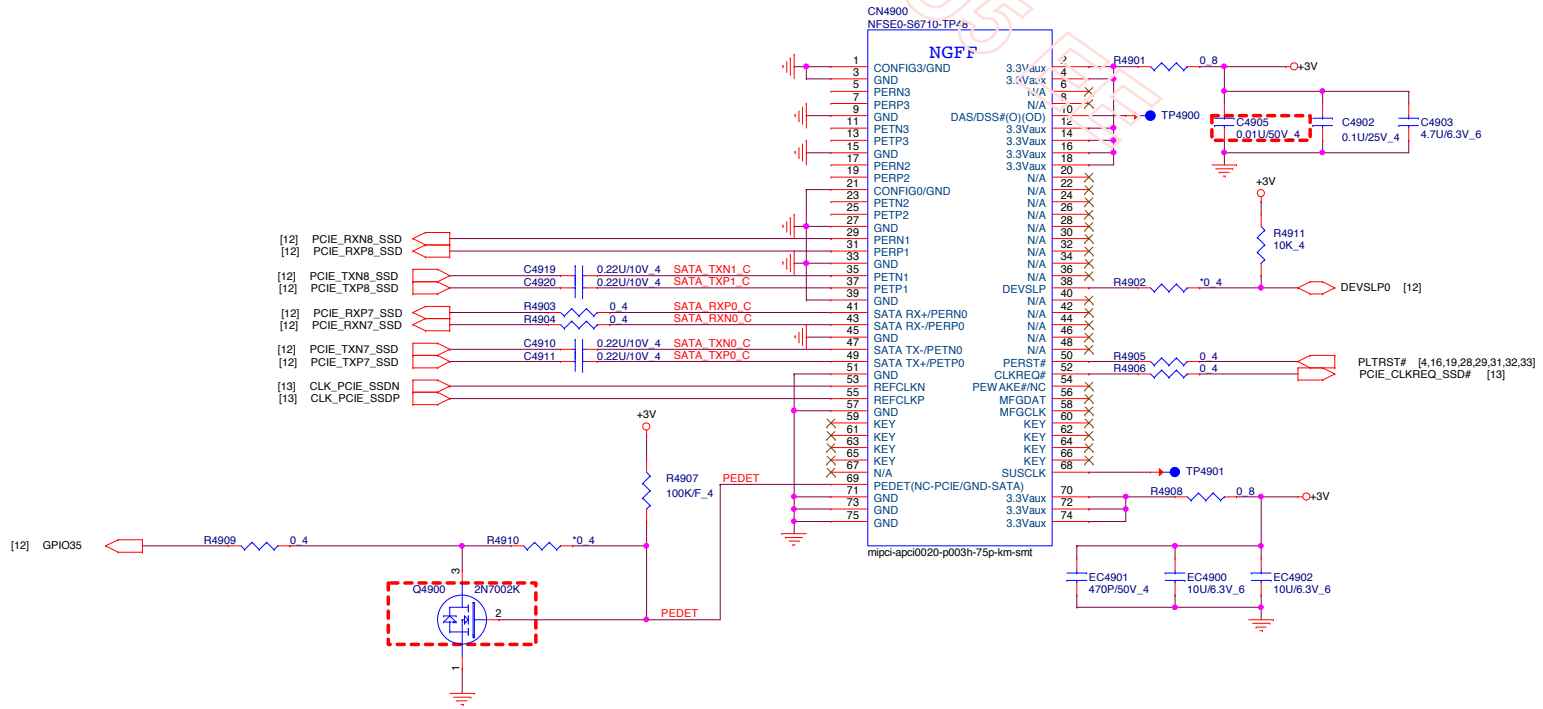
TPM (2.0)



Accelerometer Sensor



SSD



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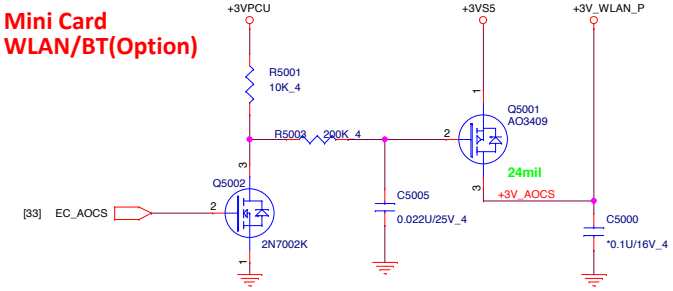
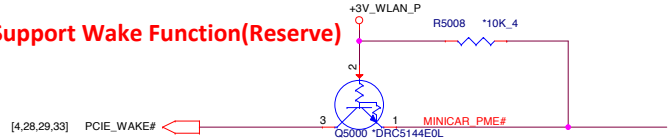
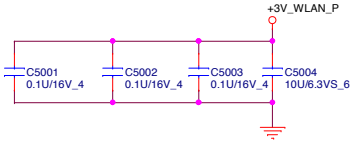
Mini Card WLAN/BT(Option)



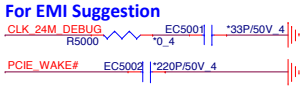
Support Wake Function(Reserve)

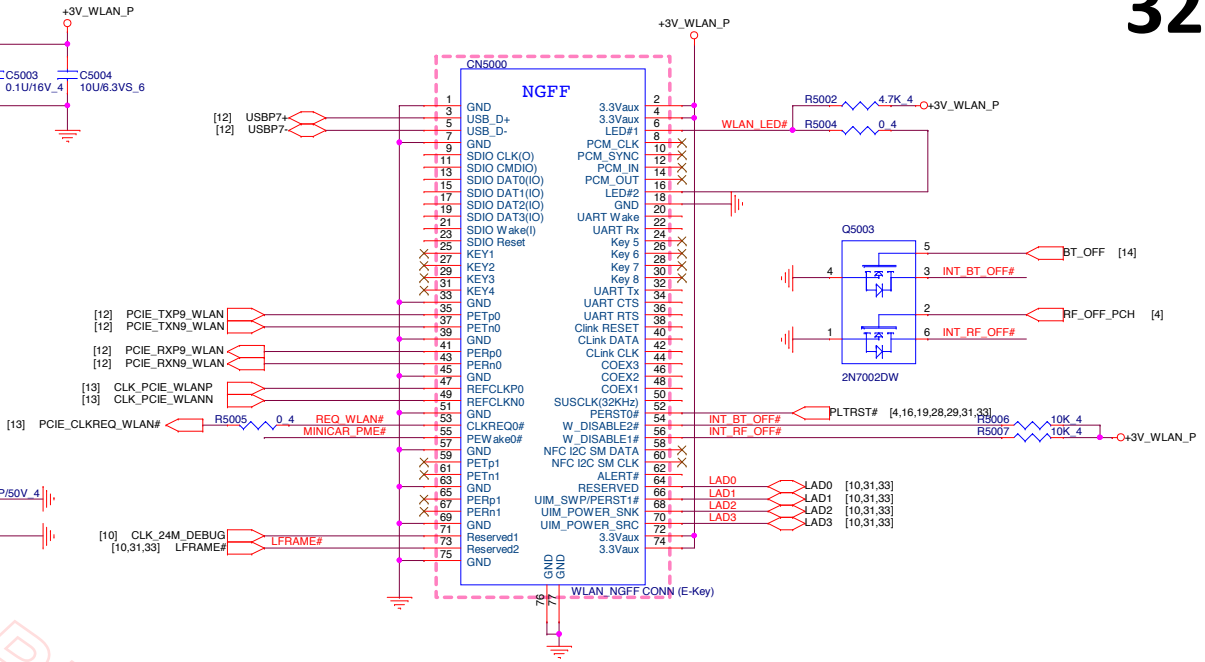


1020 del EC_PCIE_WAKE# circuit

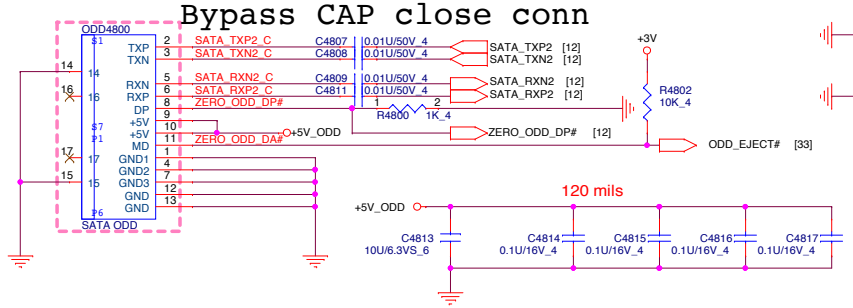


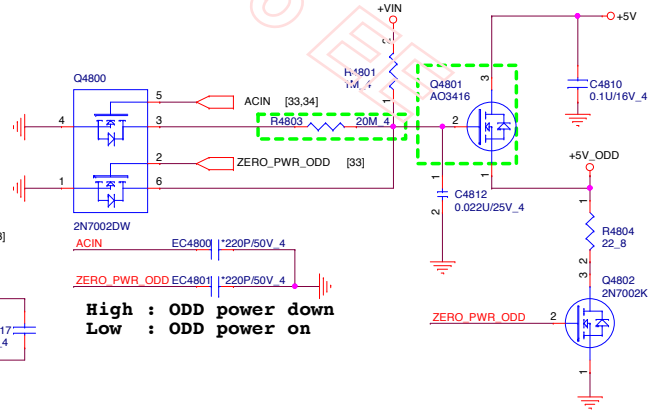
For EMI Suggestion



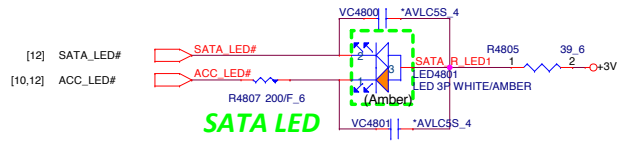


SATA ODD





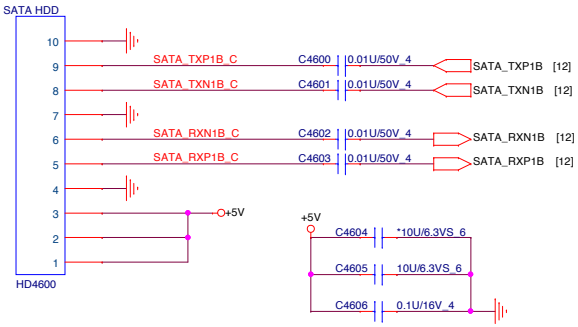
High : ODD power down
Low : ODD power on



SATA LED

[2,4,10,11,12,13,14,15,16,17,18,19,20,21,25,26,27,28,29,30,31,33,39,43,44,47] +3V
[25,26,27,30,43] +5V
[6,13,30,33,34,35,42,47] +3VPCU

HDD



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Quanta Computer Inc.

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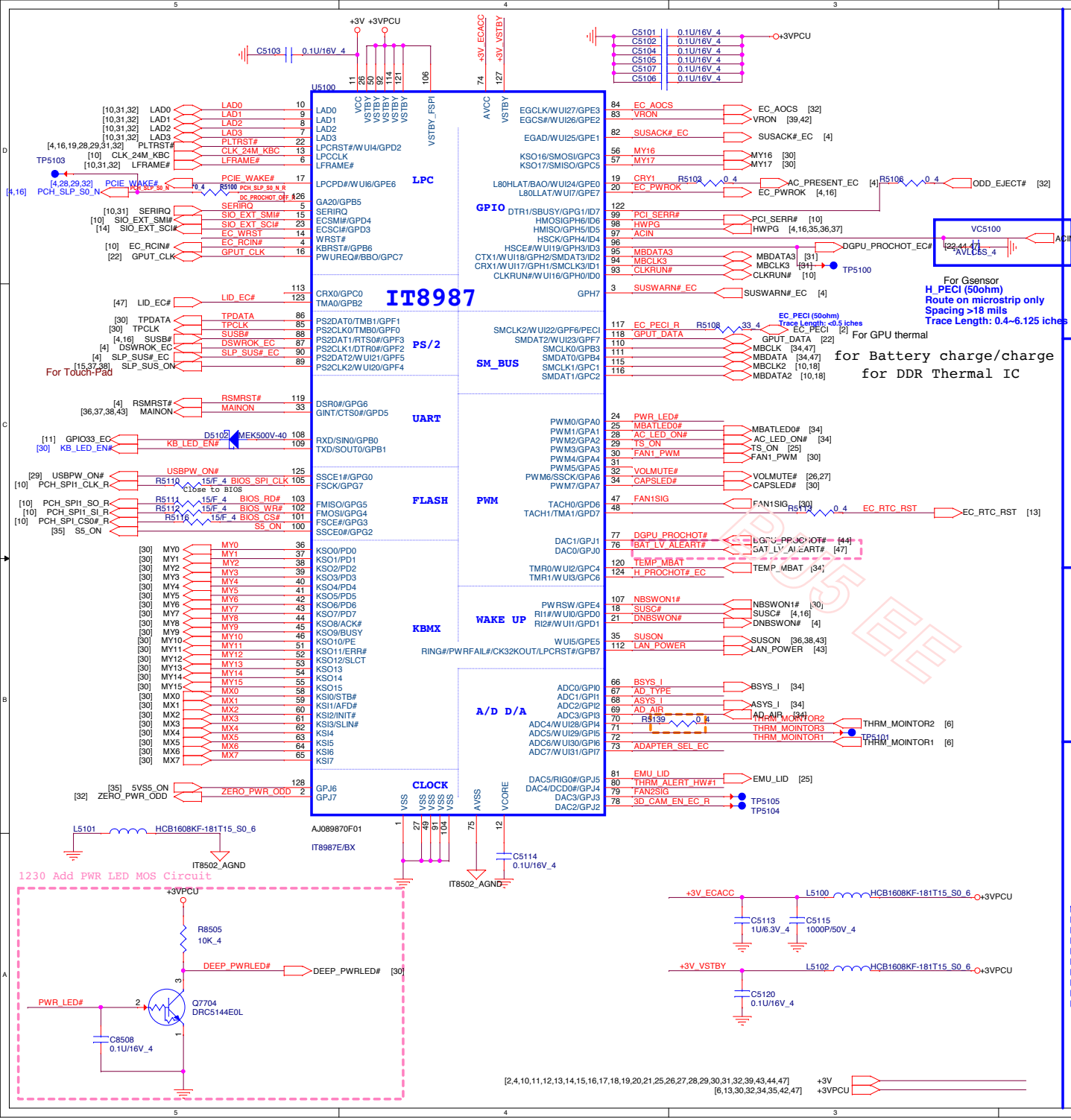
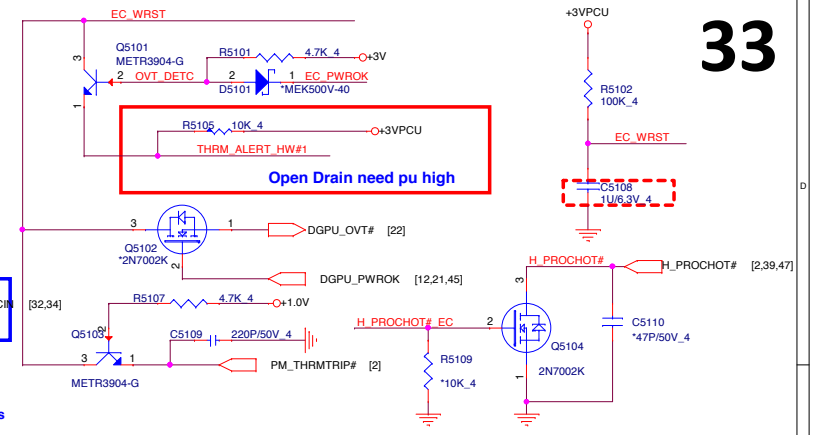




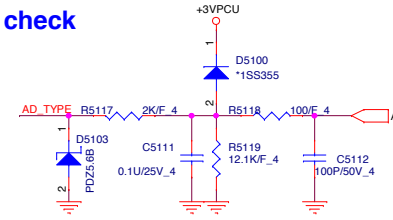
Adapter select for EC

Ra Rb

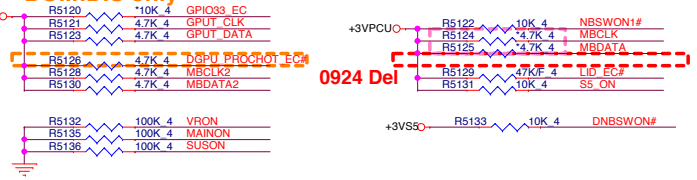
+3VPCU R5114 10K_4 ADAPTER_SEL_EC R5115 2.2K_4

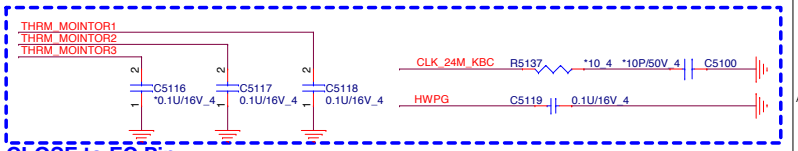
	Ra	Rb	ADAPTER_SEL_EC	BOM
200W	10K(CS31002JB28)	100K (CS41002FB28)	3V	
150W	10K(CS31002JB28)	27.4K(CS32742FB14)	2.42V	
120W	10K(CS31002JB28)	12.1K(CS31212FB28)	1.8V	
90W	10K(CS31002JB28)	6.2K(CS26202FB17)	1.26V	
65W	10K(CS31002JB28)	2.2K(CS22202JB18)	0.59V	DIS
45W	NC	10K(CS31002JB28)	0V	UMA

Adapter Type check



BOM:DIS only





CLOSE to EC Pin

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Quanta Computer Inc.

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Custom	35 -- WLAN/G-Sensor/G-CLK/TS	1A
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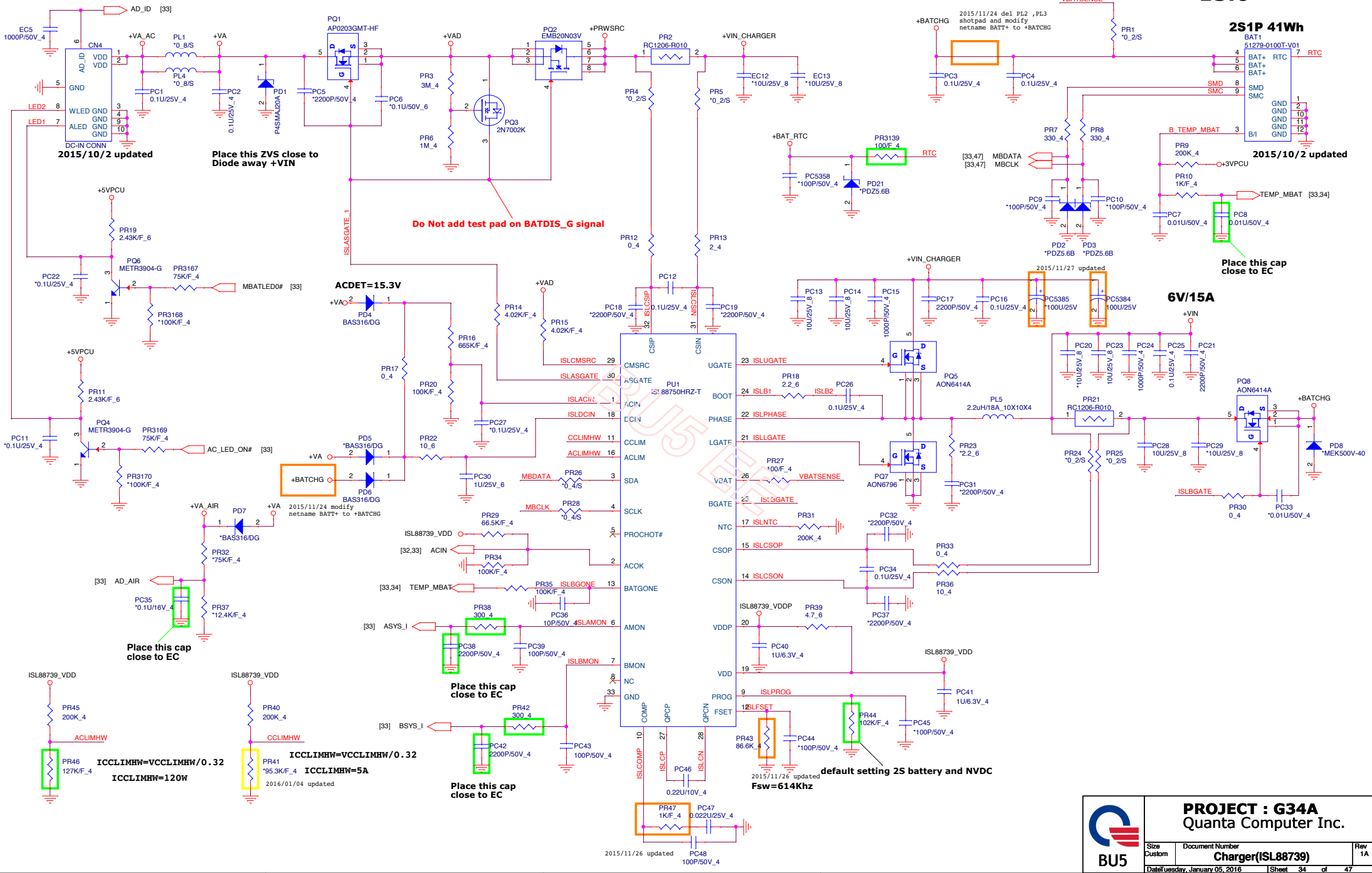
15.6"

DC_JACK 65W

2S1P 41Wh

6V/15A

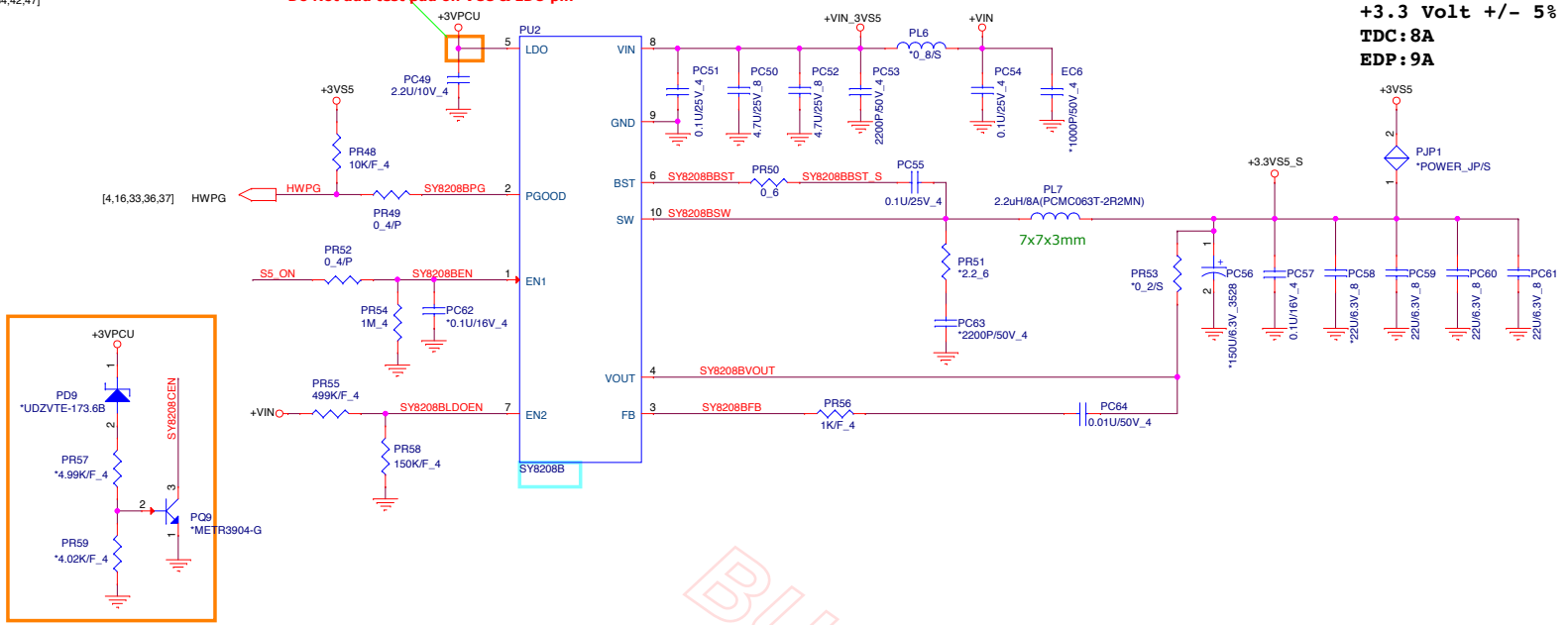


DC/DC +3VS5/+5VS5

+VIN [25,30,32,34,36,37,39,40,41,42,44,45,47]
+3VS5 [4,10,15,16,25,32,33,36,37,38,42,43,46,47]
+5VS5 [4,25,26,29,36,37,38,39,40,41,43,44,45,46]
+3VPCU [6,13,30,32,33,34,42,47]
+5VPCU [26,34,43,46]

Do Not add test pad on VCC & LDO pin

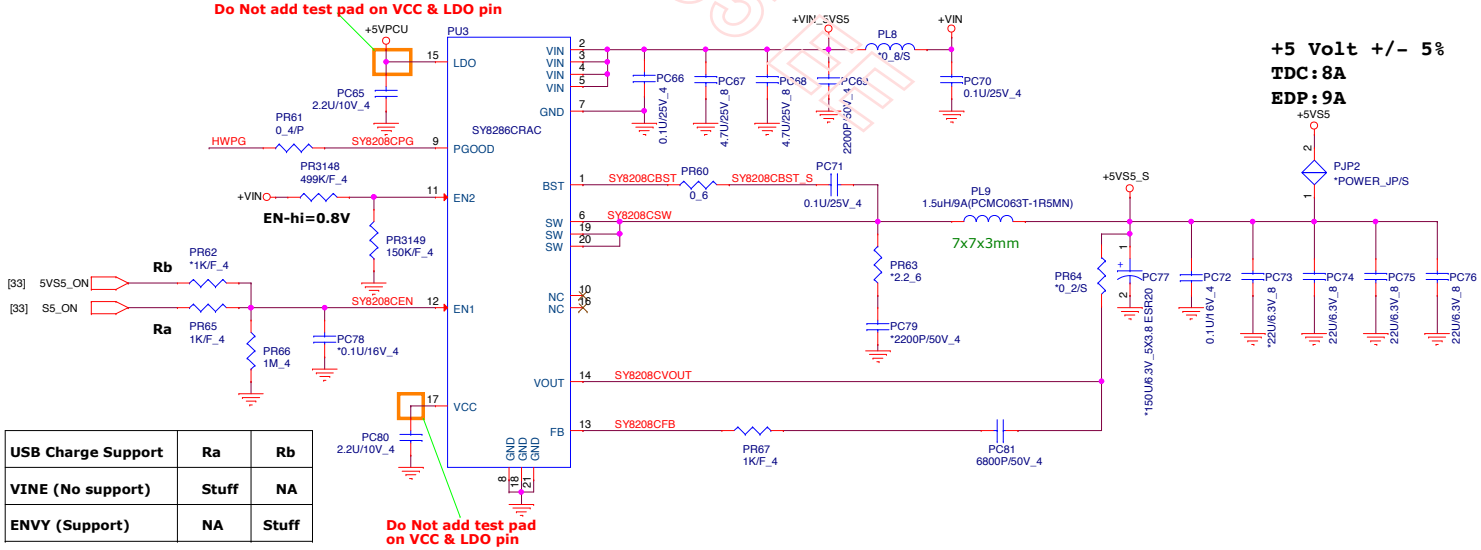
+3.3 Volt +/- 5%
TDC:8A
EDP:9A



2014/12/12 updated

Do Not add test pad on VCC & LDO pin

+5 Volt +/- 5%
TDC:8A
EDP:9A



USB Charge Support	Ra	Rb
VINE (No support)	Stuff	NA
ENVY (Support)	NA	Stuff

Do Not add test pad on VCC & LDO pin

BU5

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Size	Document Number	Rev
Custom	3/5VPCU(RT8243A)	1A
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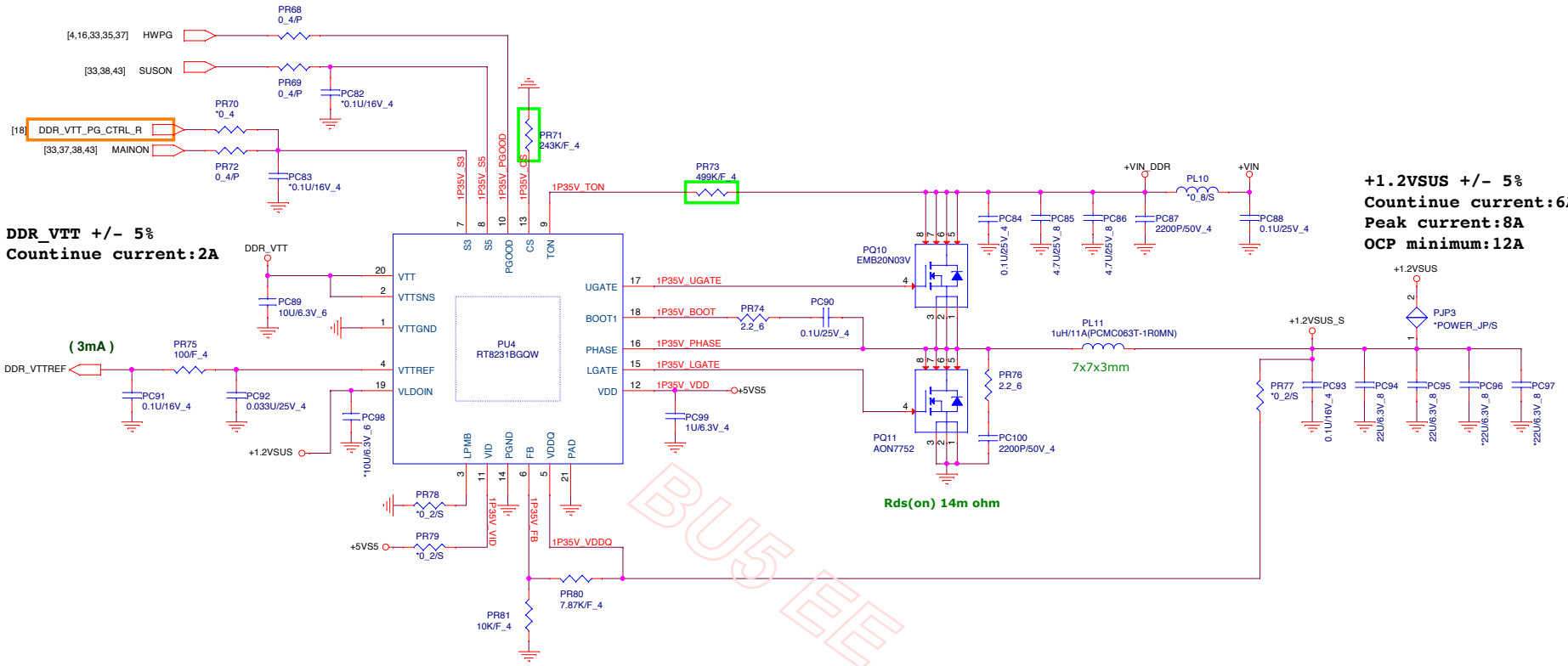
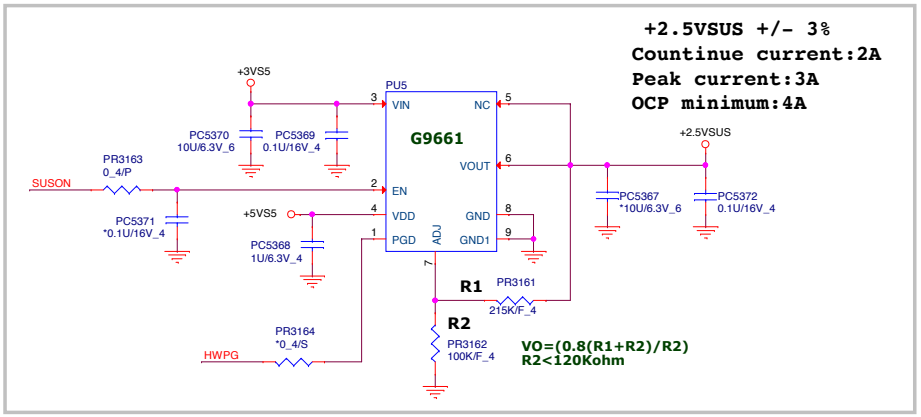
+VIN [25,30,32,34,35,37,39,40,41,42,44,45,47]
+5VS5 [4,25,26,29,35,37,38,39,40,41,43,44,45,46]
+1.2VSUS [3,6,17,18,38,46]
DDR_VTT [17,18]



20151015 updated



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Quanta Computer Inc.

Size	Document Number	Rev
	DDR3 (RT8231B)/1.8VS5	1A

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+VIN [25,30,32,34,35,36,39,40,41,42,44,45,47]
+3VS5 [4,10,15,16,25,32,33,35,36,38,42,43,46,47]
+5VS5 [4,25,26,29,35,36,38,39,40,41,43,44,45,46]
+1.0V_DEEP_SUS [9,13,15,16,38]
+1.8V_DEEP_SUS [5,9,15,47]
+1.8V [26]

(V1.00A+V1.00_MODPHY+VccPRIM_CORE)
+1.0VS5 Volt +/- 5%
Countinue current:6A
Peak current:9A

PU6 AOZ1236QI-03
2015/11/27 updated
2015/10/27 updated
7x7x3mm

20151015 updated
+1.8V_DEEP_SUS +/- 5%
Countinue current:1.0A
Peak current:3A

PU7 G9661
R1
R2
VO=(0.8(R1+R2)/R2)
R2<120Kohm

PQ46 EMB32N03K **0.05A**
PQ47 *2N7002K
PQ48 2N7002K
PQ49 METR3904-G
For 2S PACK

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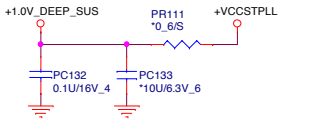
+1.0V [2,4,6,16,33]
+3VS5 [4,10,15,16,25,32,33,35,36,37,42,43,46,47]
+5VS5 [4,25,26,29,35,36,37,39,40,41,43,44,45,46]
+VCCIO [2,6,16]
+1.2VSUS [3,6,17,18,36,46]
+VCCSTPLL [2,4,5,6,9,39]
+1.0V_DEEP_SUS [9,13,15,16,37]
+1.2V_VCCPLL_OC [6]
MAINON [33,36,37,43]

Volume Segment
Vcc_ST: 0.12A
Vcc_PLL: 0.12A

<= 10ms, full load ready
(Vcc_ST+Vcc_PLL)

Imax:0.24A

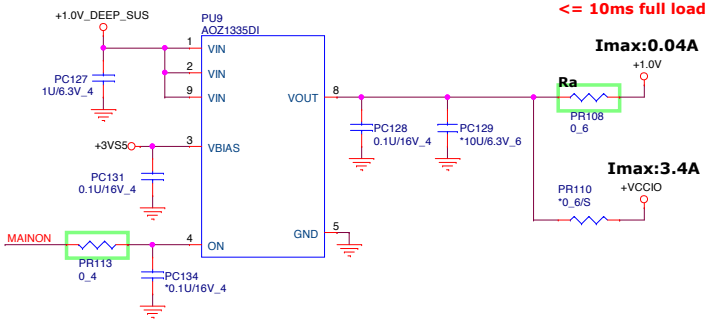


Volume Segment
Vcc_STG: 0.04A
Vcc_IO: 3.4A

<= 10ms full load ready

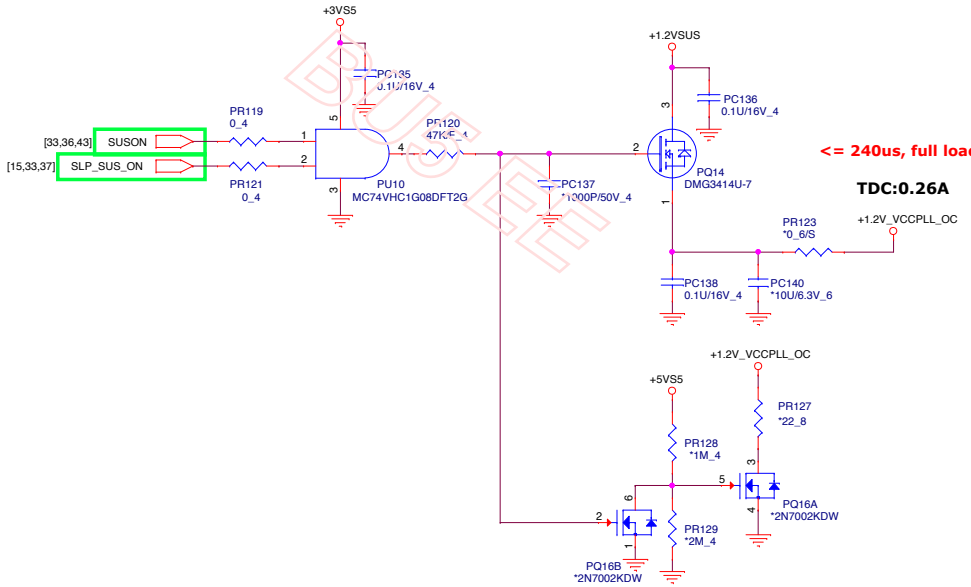
Imax:0.04A

Imax:3.4A



<= 240us, full load ready

TDC:0.26A



PROJECT : G34A
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Size	Document Number	Rev
Custom	+1.0V/+VCCSTPLL	1A
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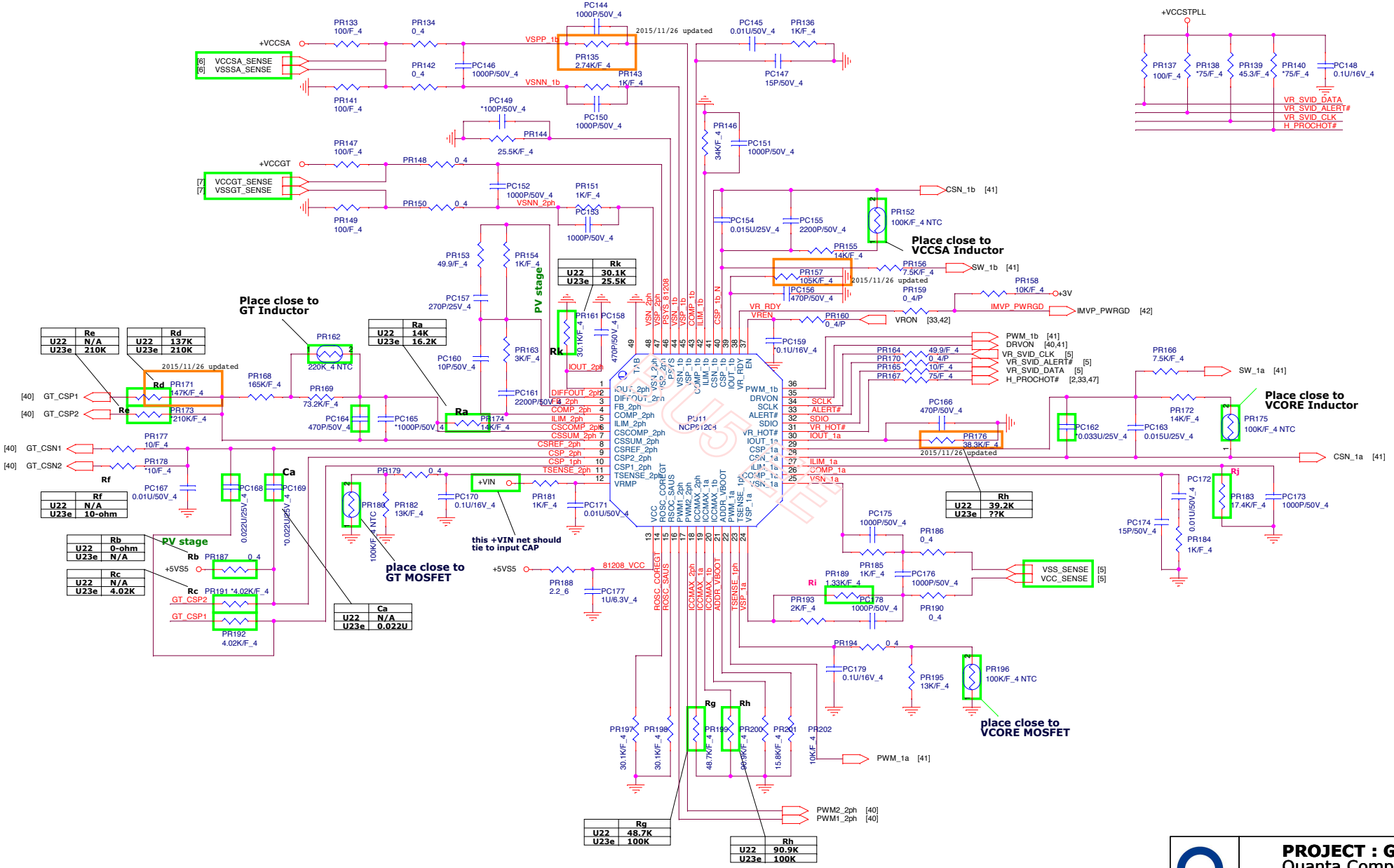
+3V [2,4,10,11,12,13,14,15,16,17,18,19,20,21,25,26,27,28,29,30,31,32,33,43,44,47]
+5V [25,26,27,30,32,43]
+VIN [25,30,32,34,35,36,37,40,41,42,44,45,47]
+5VPCU [26,34,35,43,46]
+VCCSA [6,41]
+VCCGT [7,40]
+VCCSTPLL [2,4,5,6,9,38]



Re	
U22	N/A
U23e	210K

Rd	
U22	137K
U23e	210K

Ra	
U22	14K
U23e	16.2K

Rk	
U22	30.1K
U23e	25.5K

Rf	
U22	N/A
U23e	10-ohm

Rb	
U22	0-ohm
U23e	N/A

Rc	
U22	N/A
U23e	4.02K

Ca	
U22	N/A
U23e	0.022U

Rg	
U22	48.7K
U23e	100K

Rh	
U22	90.9K
U23e	100K

Rh	
U22	39.2K
U23e	??K

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Custom	CPU VR IC (NCP81206)	2A
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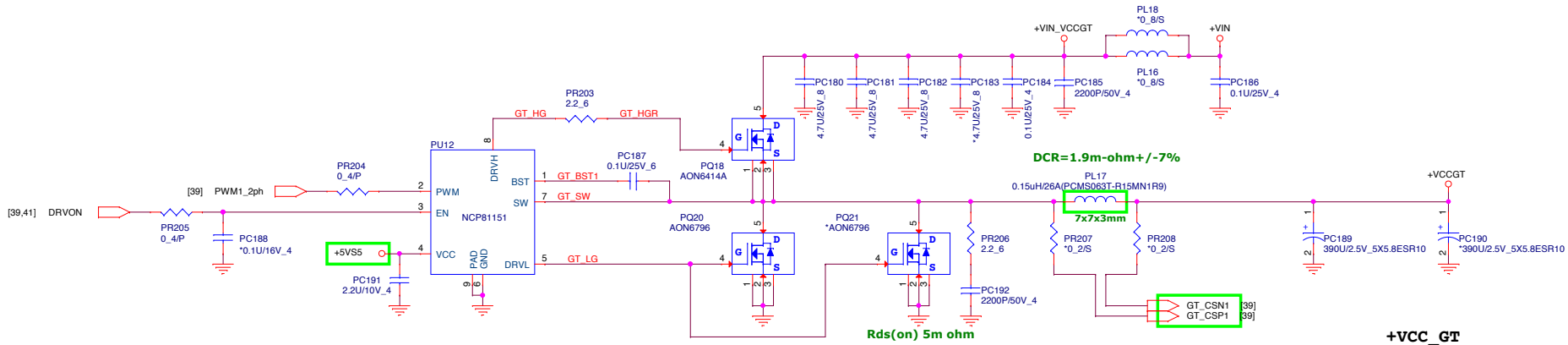
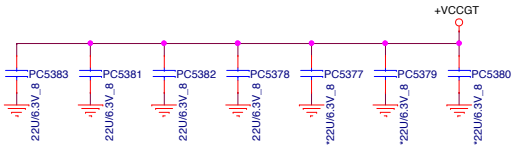
+5V [25,26,27,30,32,43]
+VIN [25,30,32,34,35,36,37,39,41,42,44,45,47]
+5VPCU [26,34,35,43,46]
+VCCGT [7,39]



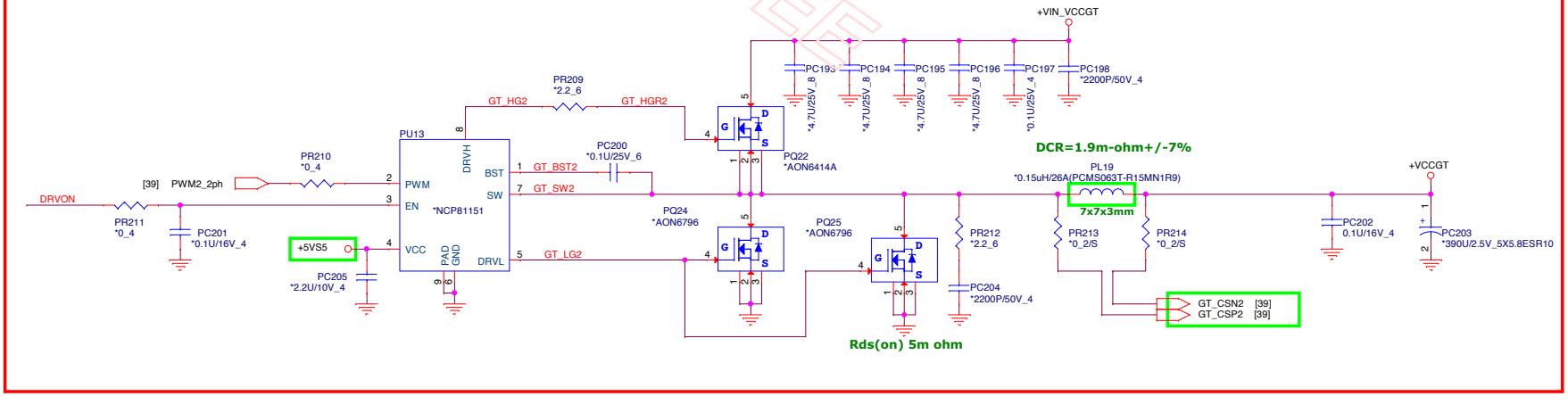


+VCC_GT

U-line 22 (15W)
TDC:18A(22)
Icc max:31A(22)
L/L=3.1mV/A

U-line 23e(28W)
TDC:35A(23e)
Icc max =64A(GT+GTx)
L/L=2mV/A

For U23e --> Add These Components



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Custom	+VCCSA (NCP81253)	2A
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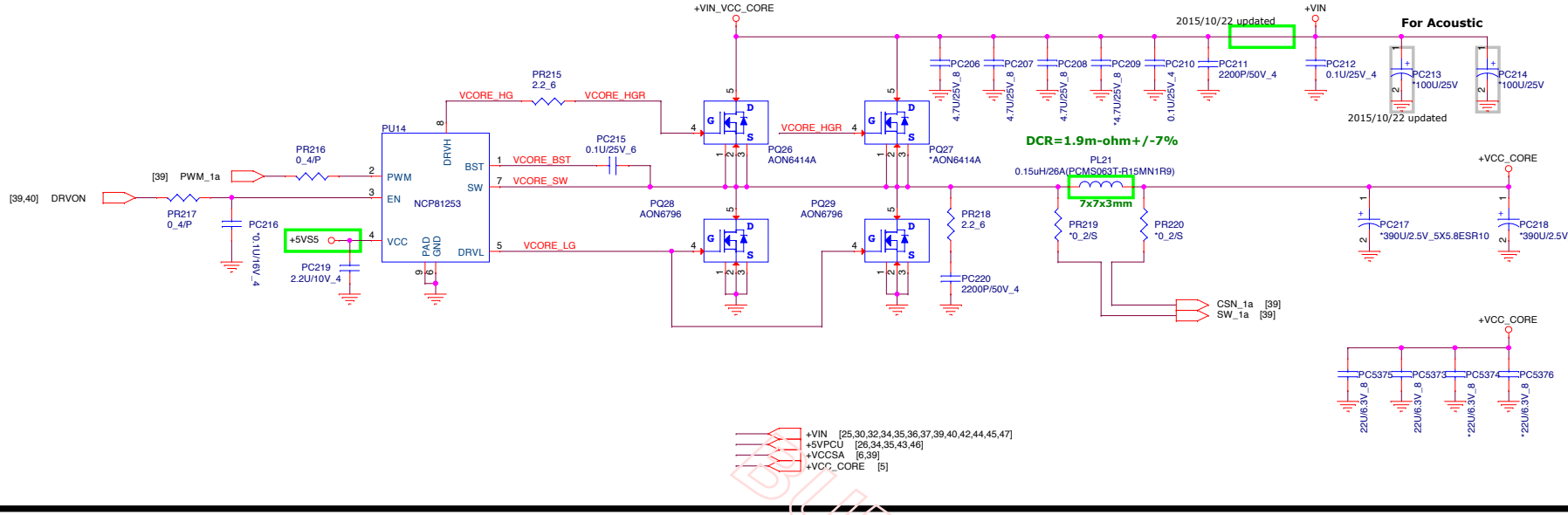
CPU CORE



+VCC_CORE

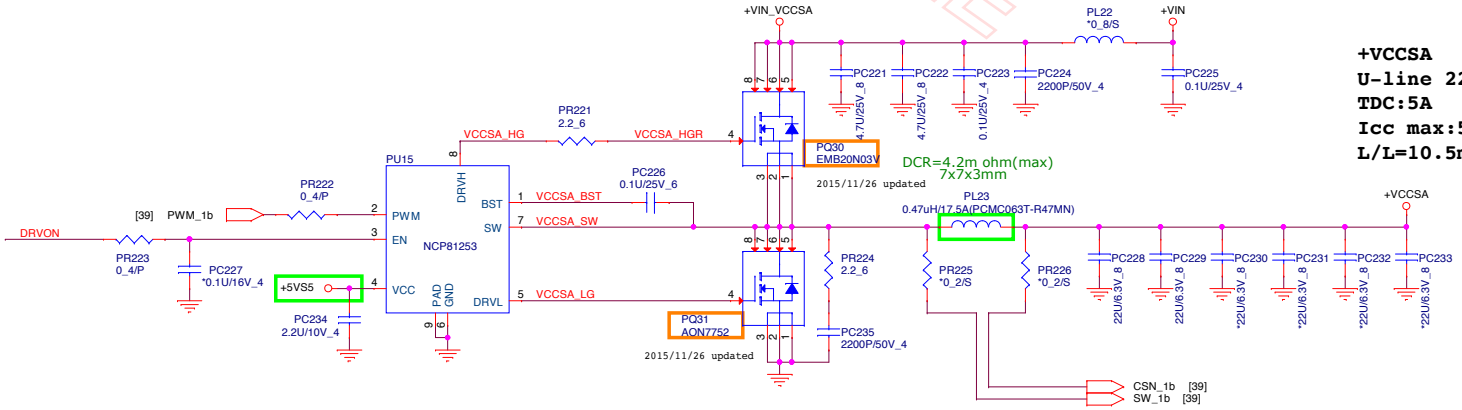
U-line 22(15W)
TDC:21A
Icc max:29A
L/L=2.4mV/A

U-line 23e(28W)
TDC:23A
Icc max:32A
L/L=2.4mV/A

H/W side output CAP list

47U/6.3V_0805 X 9
22U/6.3V_0805 X 1
22U/6.3V_0603 X 13
10U/6.3V_0603 X 1
10U/6.3V_0402 X 15
1U/6.3V_0402 X 15

VCCSA



+VCCSA
U-line 22&23e
TDC:5A
Icc max:5A
L/L=10.5mV/A

BU5	**PROJECT : G34A** Quanta Computer Inc.	
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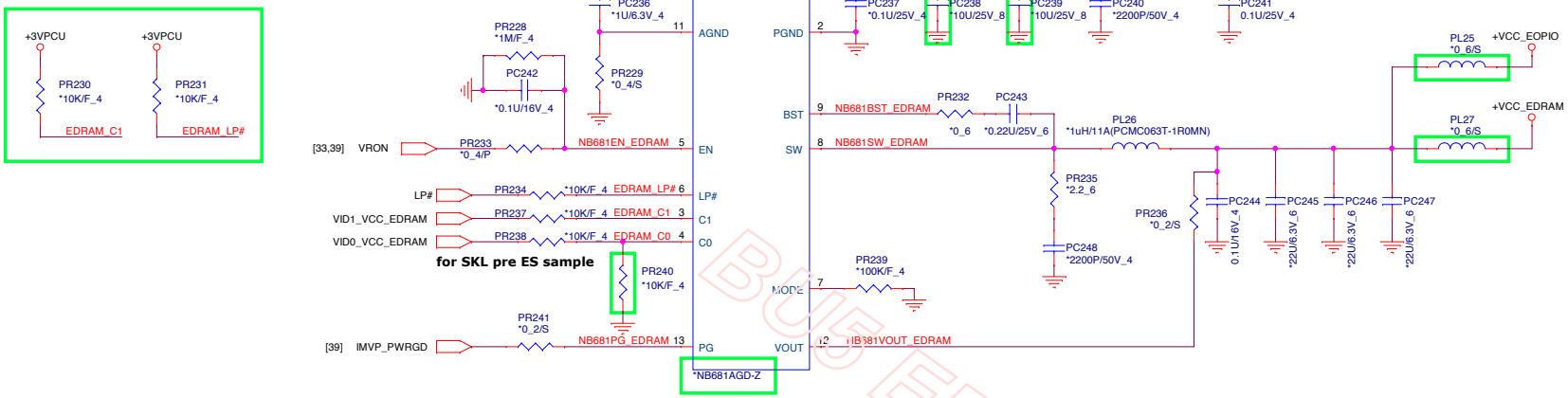
+VIN [25,30,32,34,35,36,37,39,40,41,44,45,47]
+3VPCU [6,13,30,32,33,34,35,47]
+VCC_EOPIO [5]
+VCC_EDRAM [5]

+VCC_EDRAM +/- 5%
Countinue current:4.5A
Peak current:6A



VCC_EDRAM

LP#	C1	C0	Vout
0	X	X	0
1	0	0	0.8
1	0	1	0.95
1	1	0	1.0
1	1	1	1.05

MODE

	VR rail	Resistor
M1	VCCIO	0
M2	PRIMCORE	Float
M3	EDRAM/EOPIO	100K
M4	other	150K

BU5

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Size	Document Number	Rev
Custom	+VCC_EDRAM (NB681)_23E	
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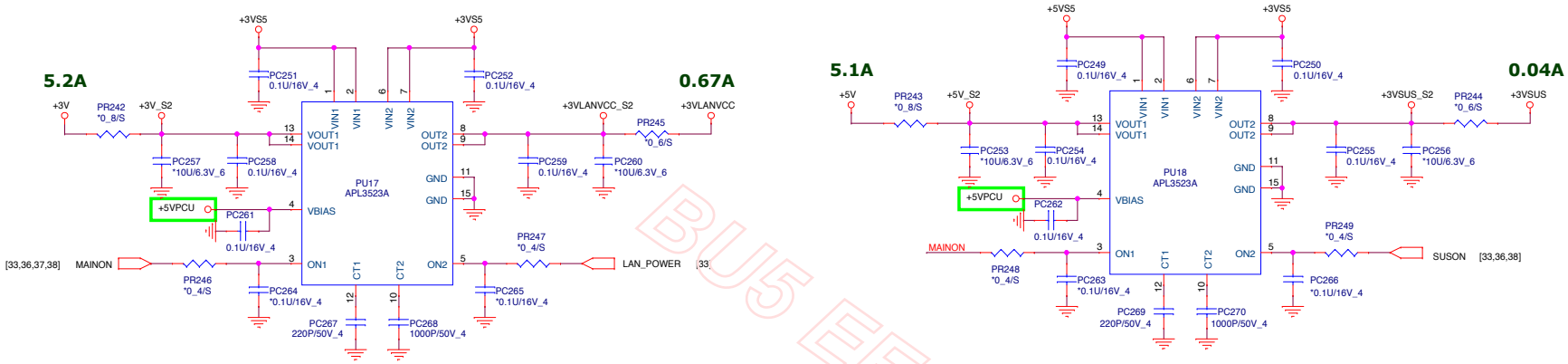
+3V [2,4,10,11,12,13,14,15,16,17,18,19,20,21,25,26,27,28,29,30,31,32,33,39,44,47]
+5V [25,26,27,30,32]
+VIN [25,30,32,34,35,36,37,39,40,41,42,44,45,47]
+3VS5 [4,10,15,16,25,32,33,35,36,37,38,42,46,47]
+5VS5 [4,25,26,29,35,36,37,38,39,40,41,44,45,46]
+3VSUS [30]
+5V_CAM
+3VLANVCC [28]



BU5

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Custom	Dis-charge IC (SLG55448)	1A
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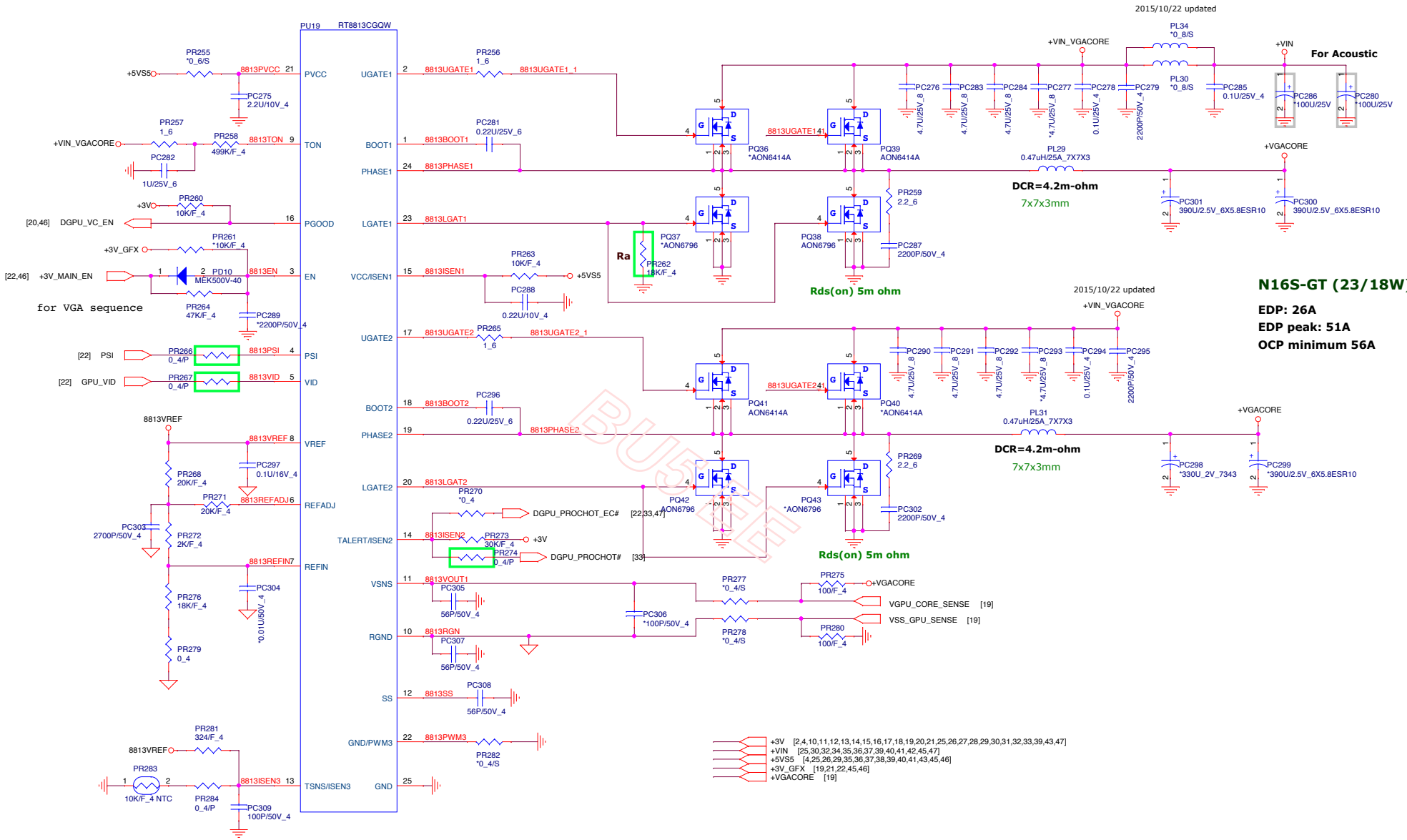
VGA Core



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Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VGACORE (RT8813A)	2A
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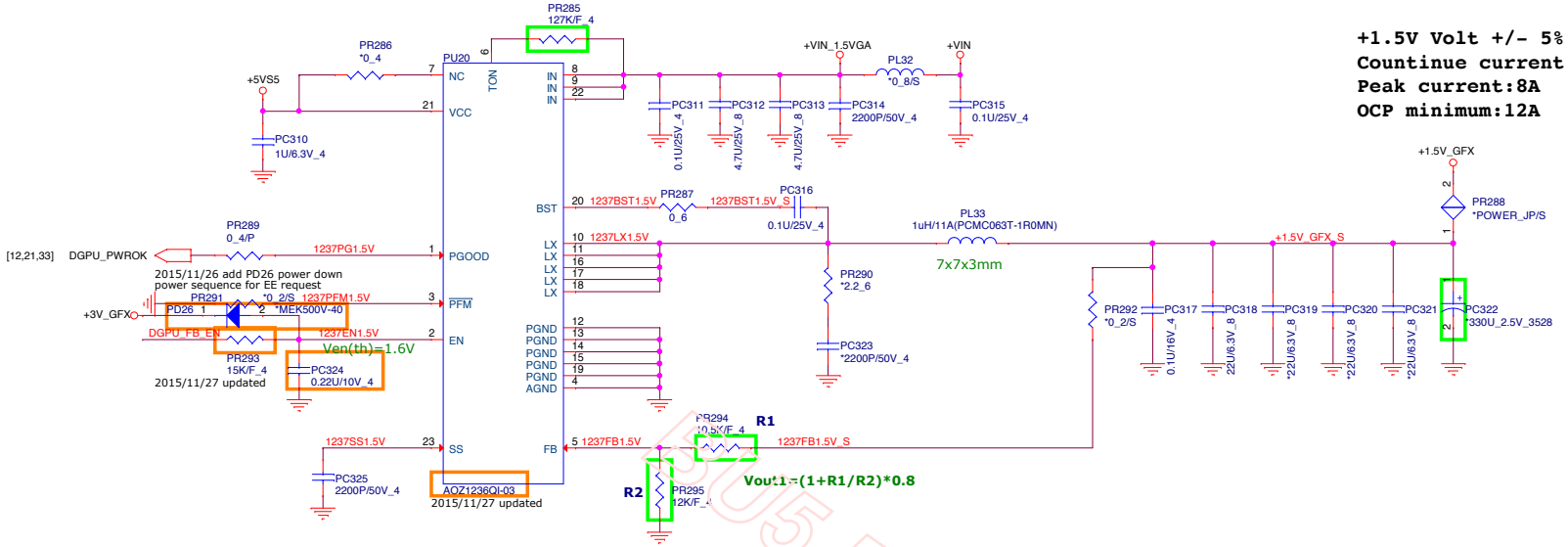
+VIN [25,30,32,34,35,36,37,39,40,41,42,44,47]
+5VS5 [4,25,26,29,35,36,37,38,39,40,41,43,44,46]
+1.5V_GFX [20,21,23,24]

+1.5V Volt +/- 5%
Countinue current:6A
Peak current:8A
OCP minimum:12A



BU5

PROJECT : G34A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.35V_VGA(AOZ1237)	1A
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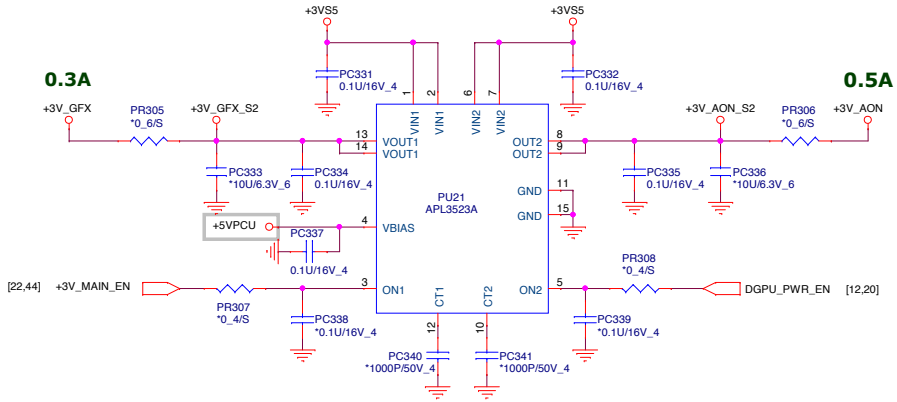
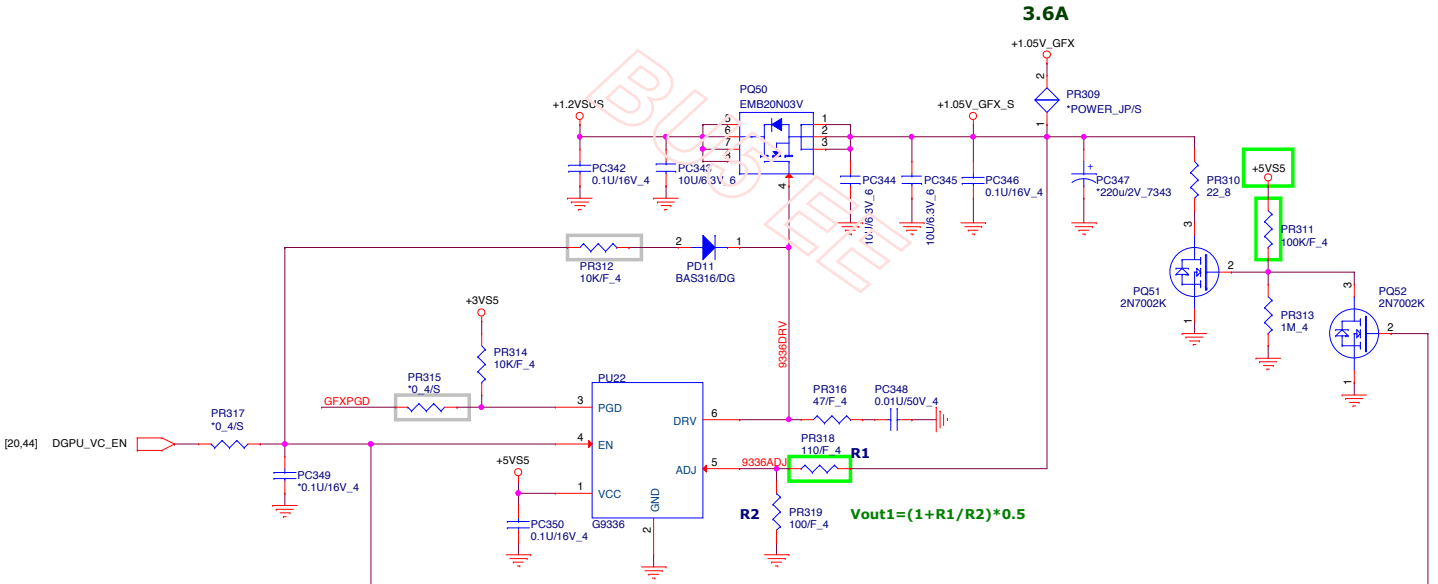
+VIN [25,30,32,34,35,36,37,39,40,41,42,44,45,47]
+3VS5 [4,10,15,16,25,32,33,35,36,37,38,42,43,47]
+5VS5 [4,25,26,29,35,36,37,38,39,40,41,43,44,45]
+3V_GFX [19,21,22,44,45]
+3V_AON [19,22]
+1.2VSUS [3,6,17,18,36,38]
+1.05V_GFX [19,20,21]





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Custom	1.05V_VGA/3V_VGA	1A
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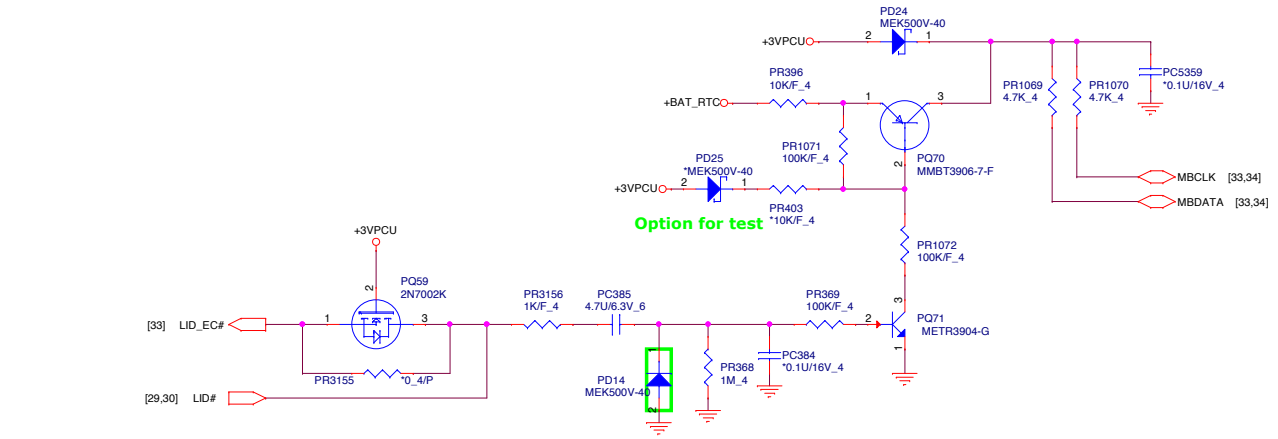

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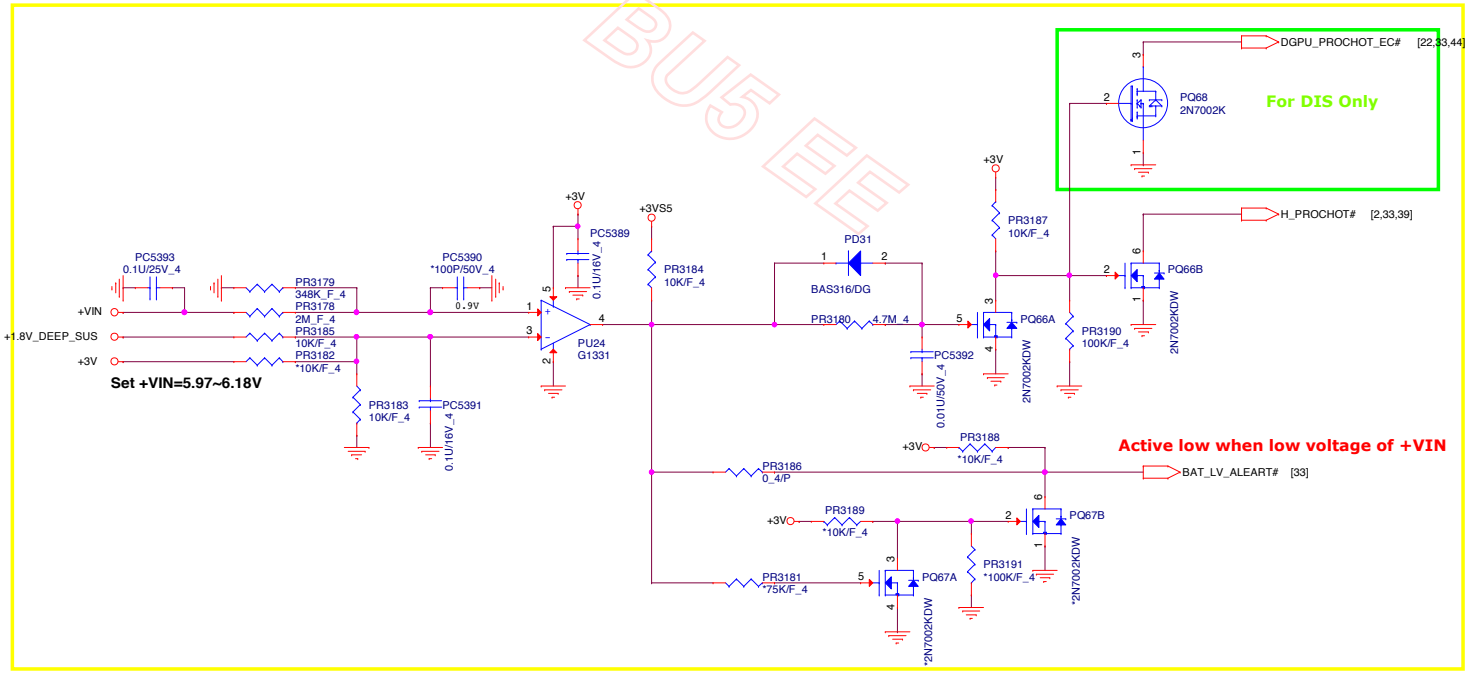

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Size	Document Number	Rev
Custom	LIDS/W for storage mode	1A
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