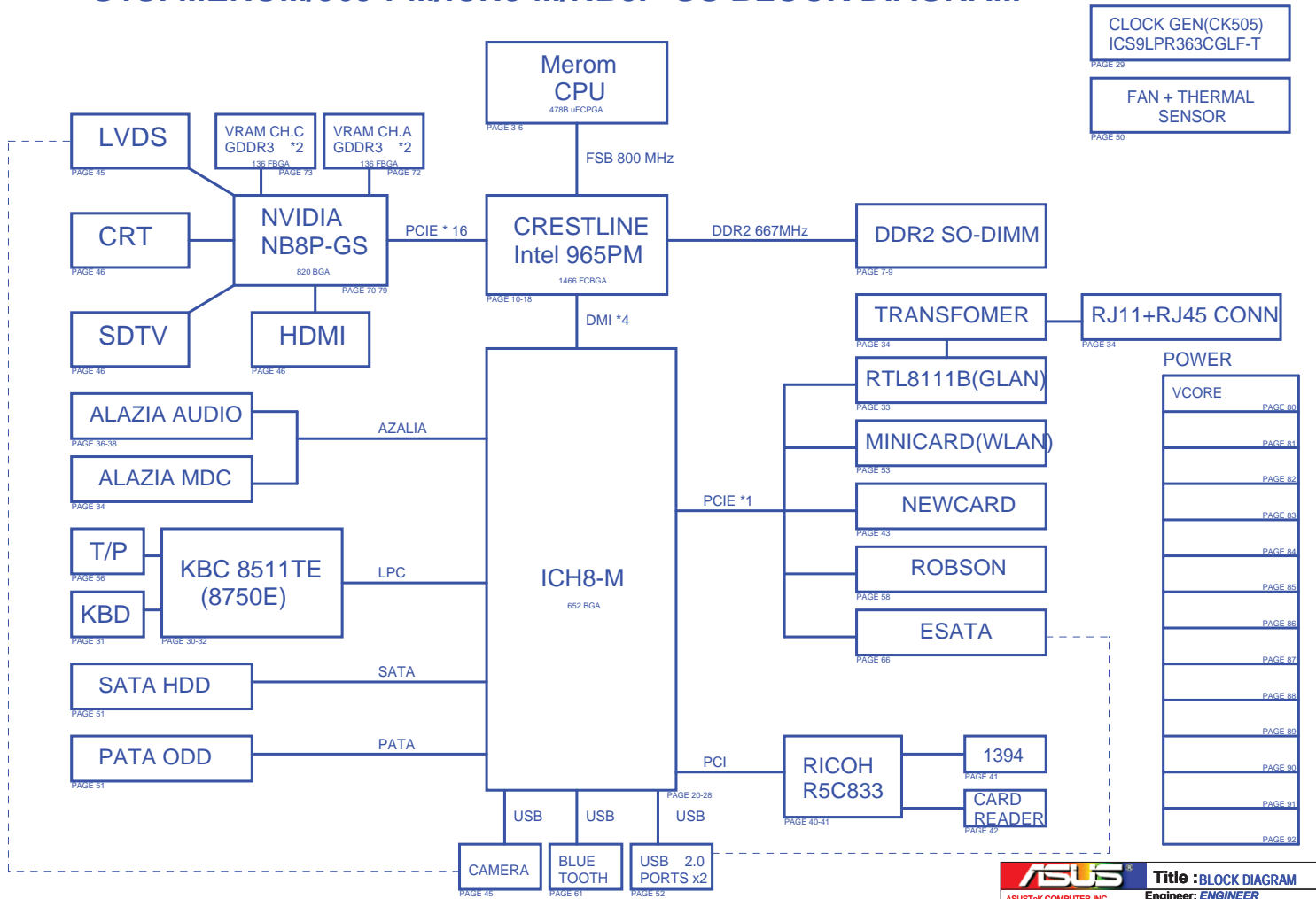
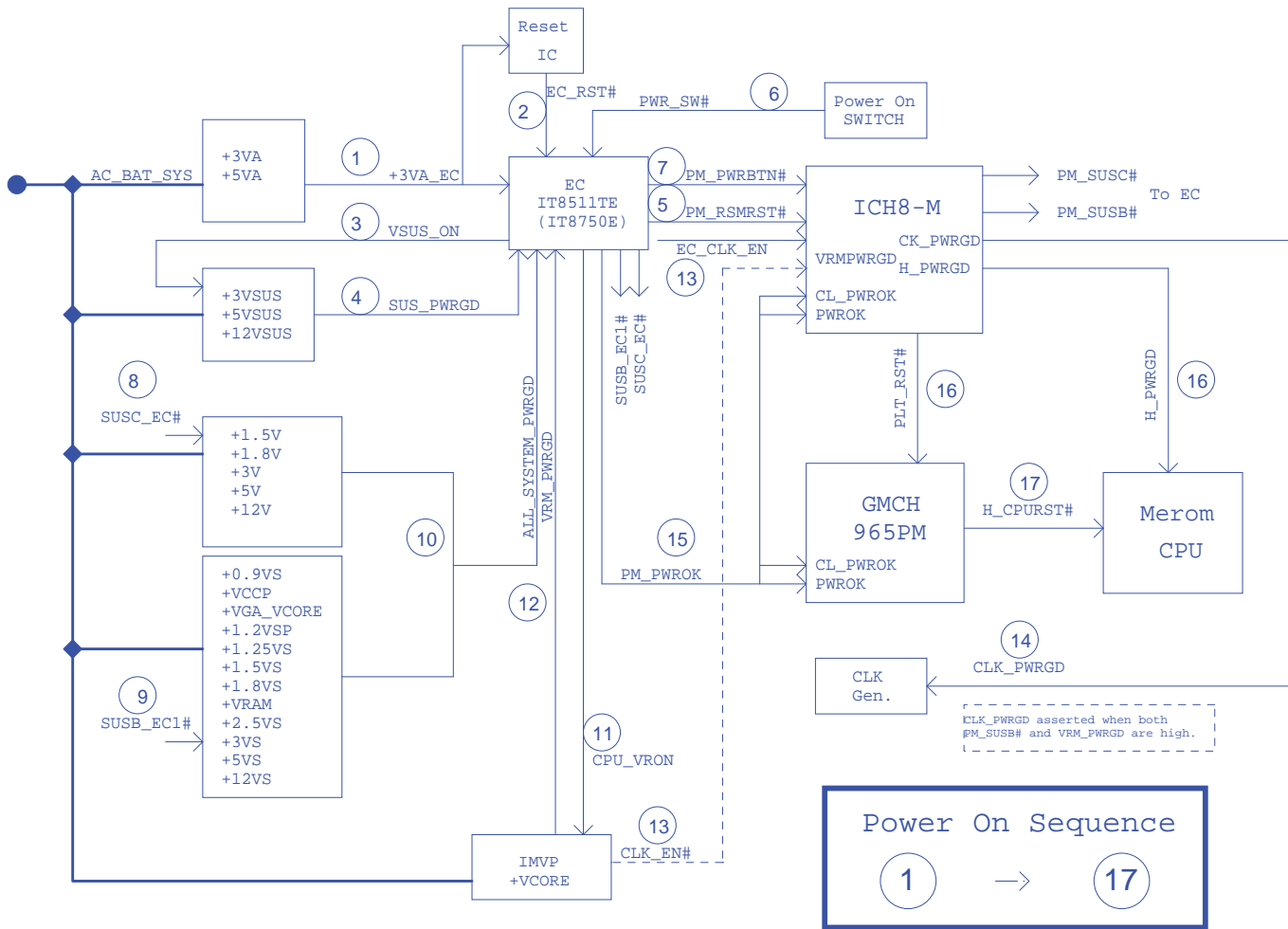
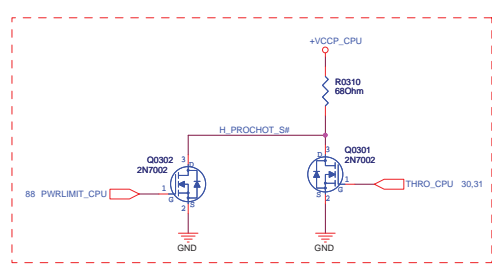
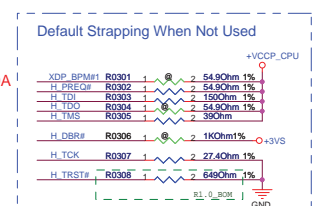
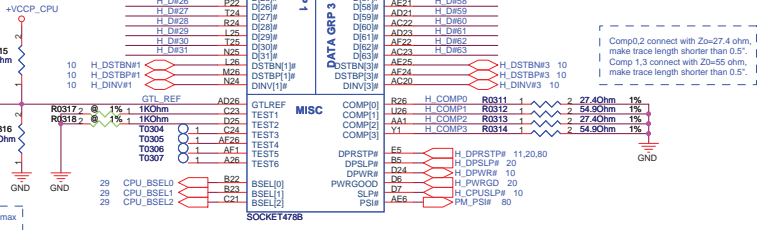
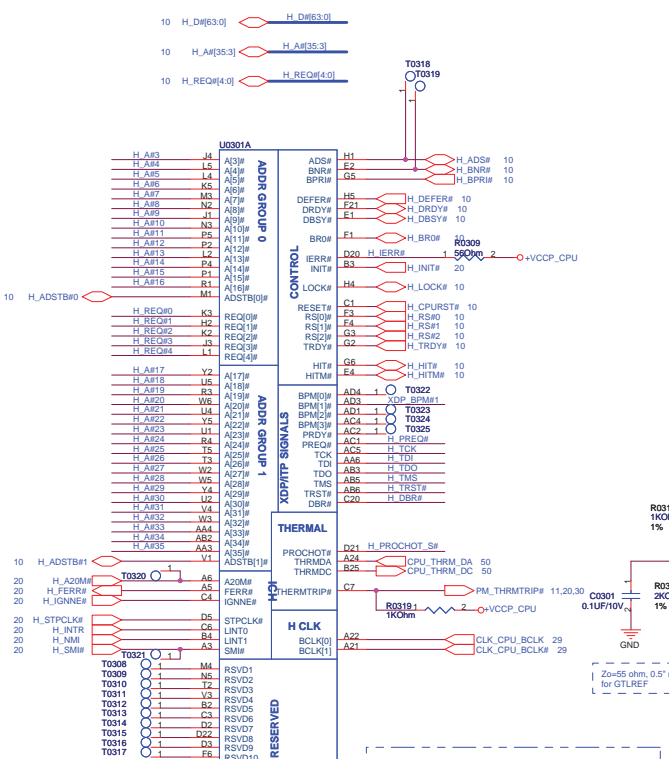


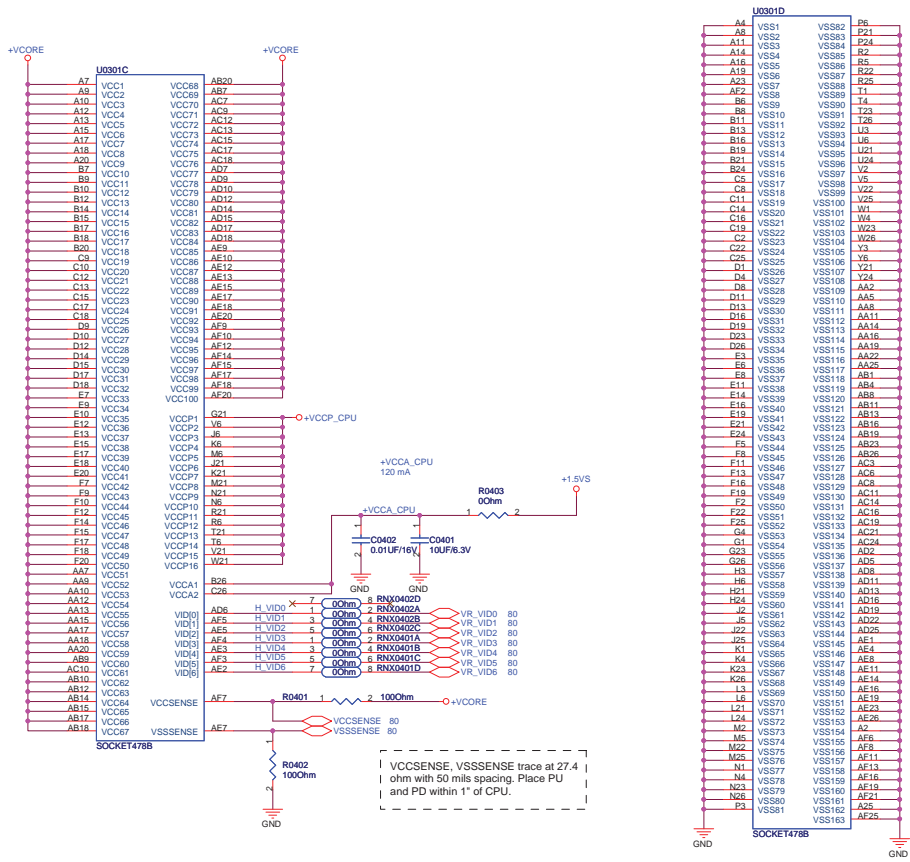
# G1S: MEROM/965-PM/ICH8-M/NB8P-GS BLOCK DIAGRAM

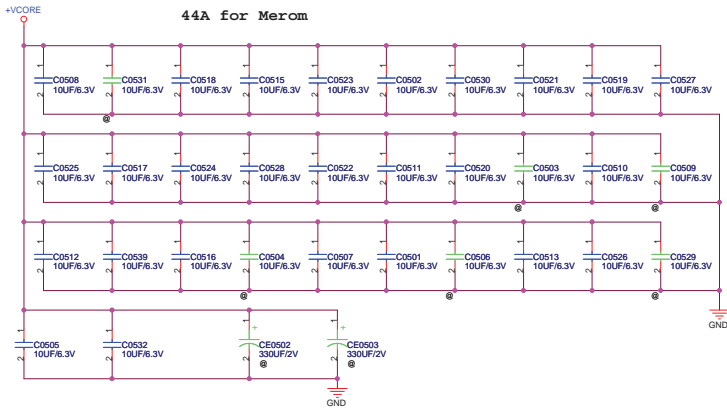




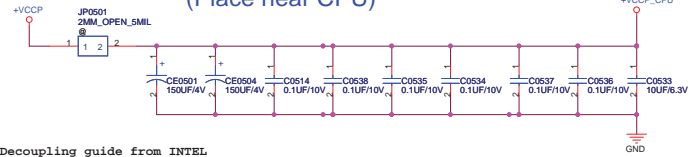


2nd source:12G04600479A





## +VCCP Decoupling Capacitor (Place near CPU)



### Decoupling guide from INTEL

VCCORE 22uF/10V	* 32pcs
330uF/2V	* 6pcs
VCCP 0.1uF	* 6pcs for CPU
150uF	* 1pcs for CPU

5

4

3

2

1

D

D

C


C

B

B

A

A

		<b>Title : EMPTY</b>	
ASUSTeK COMPUTER INC		<b>Engineer: ENGINEER</b>	
Size	Project Name		Rev
A	<b>G1S</b>		1.1
Date: 星期五, 八月 03, 2007		Sheet	6 of 94

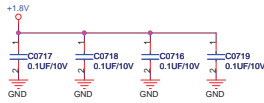
5

4

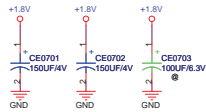
3

2

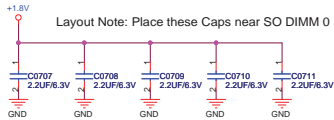
1



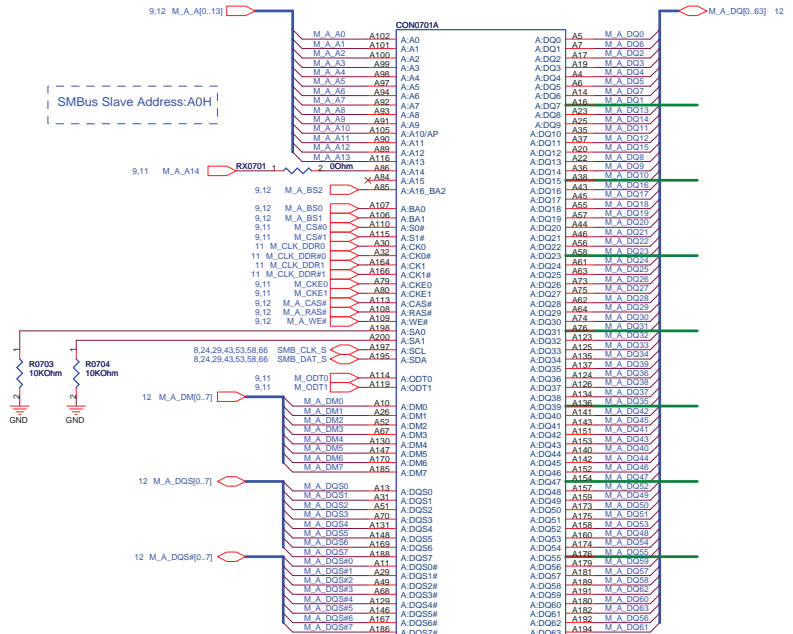
Address reference +1.8V, add four 0.1uF decoupling CAP.



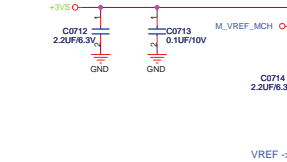
Layout Note: Place these Caps near SO DIMM 0



SO-DIMM 0 is placed further from the GMCH than SO-DIMM 1

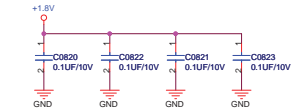


Layout Note: Place these Caps near SO DIMM 0



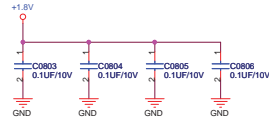
VREF -> 10/10 mils

**ASUS** Title : DDR2 SO-DIMM\_0  
 ASUSTEK COMPUTER INC Engineer: ENGINEER  
 Size Project Name Rev  
 Custom G1S 1,1  
 Date: 2007/03/05 Sheet 7 of 94

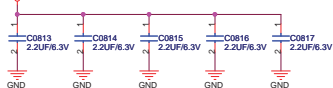


Address reference +1.8V, add four 0.1uF decoupling CAP.

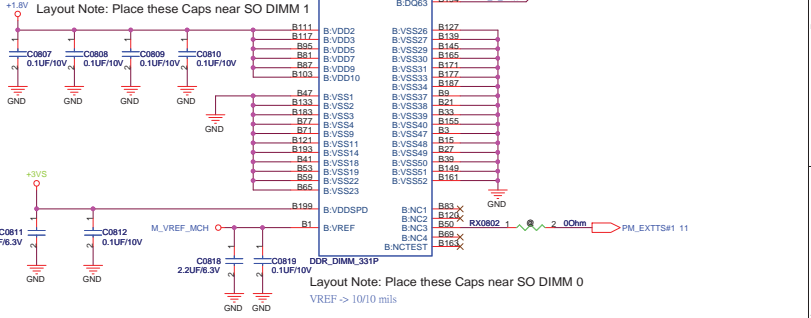
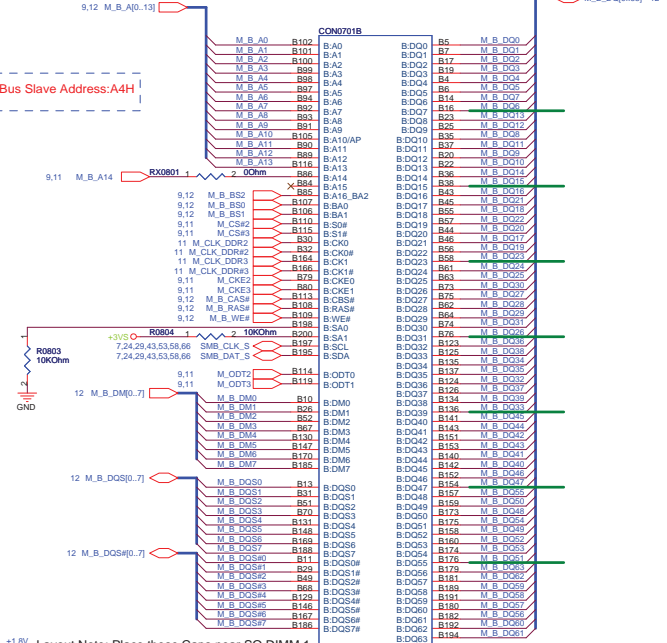
Layout Note: Place these High-Freq decoupling Caps near the GMCH



Layout Note: Place these CAPS near the GMCH



SMBus Slave Address:A4H

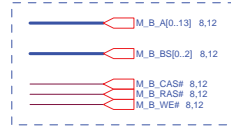
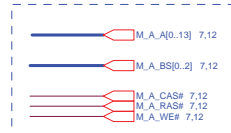
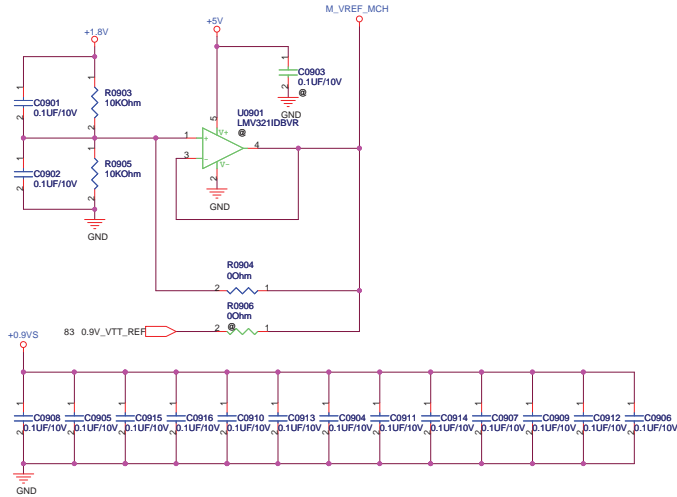


Layout Note: Place these Caps near SO DIMM 0  
VREF > 10/10 mils

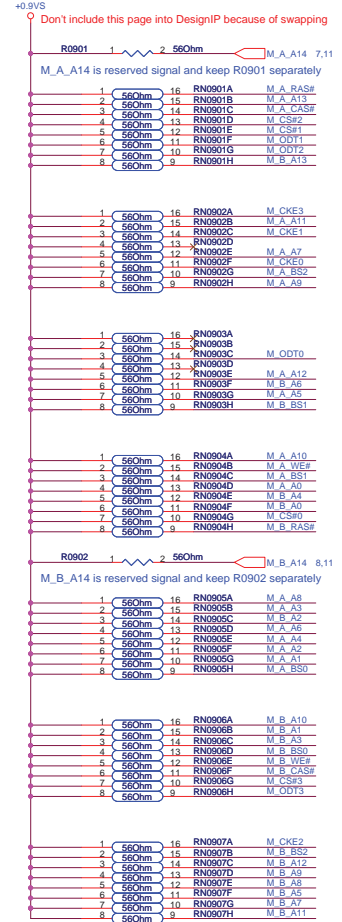
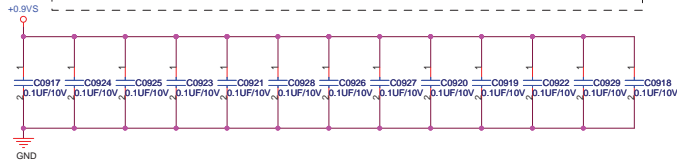


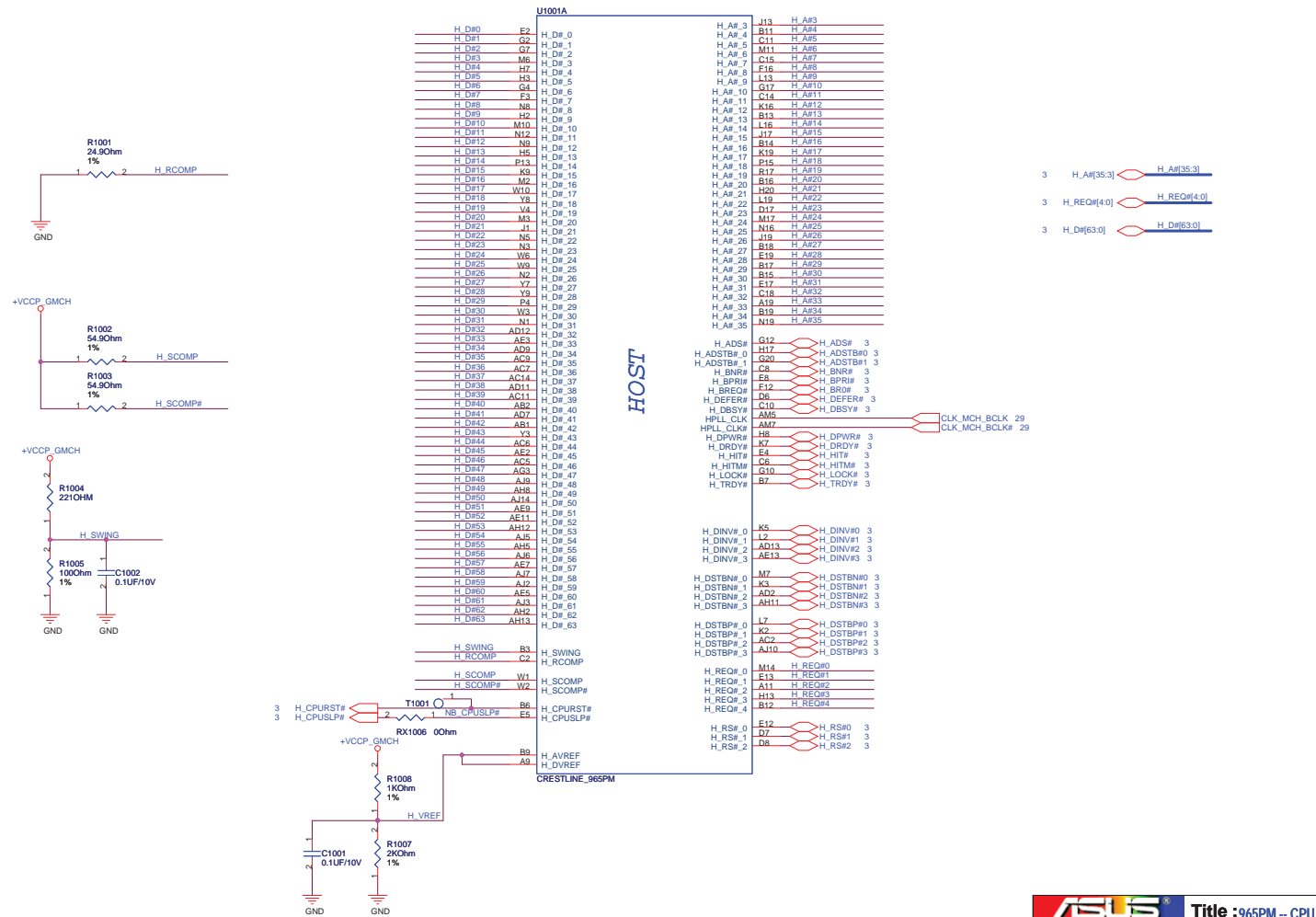
+0.9VS can be controlled to 0.9V or 0.9VS.  
Remind PWR EE to reserve SUSB# and SUCS#

**HAD SWAPED**



Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS

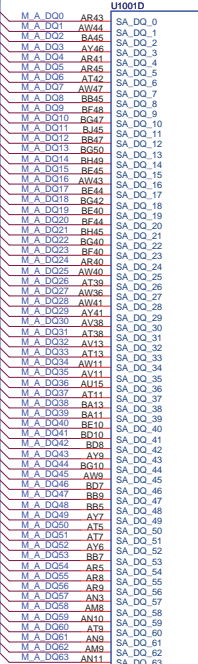




U1001A		HOST	
H_D#0	E0	H_A#3	J13
H_D#1	G2	H_A#4	B11
H_D#2	G7	C111	H_A#5
H_D#3	M6	M11	H_A#6
H_D#4	M7	H_A#7	H_A#7
H_D#5	H3	E16	H_A#8
H_D#6	G4	H_A#9	L13
H_D#7	F3	C17	H_A#9
H_D#8	NS	H_A#10	C14
H_D#9	H2	H_A#11	K16
H_D#10	M10	H_A#12	K16
H_D#11	N12	H_A#13	B13
H_D#12	N3	H_A#14	L16
H_D#13	H5	H_A#15	J17
H_D#14	P13	H_A#16	B14
H_D#15	K9	H_A#17	K19
H_D#16	M2	H_A#18	P15
H_D#17	W10	H_A#19	E17
H_D#18	Y8	H_A#20	B16
H_D#19	VA	H_A#21	P20
H_D#20	M3	H_A#22	L19
H_D#21	J1	H_A#23	D17
H_D#22	NS	H_A#24	M17
H_D#23	N3	H_A#25	N16
H_D#24	W6	H_A#26	J19
H_D#25	WB	H_A#27	B18
H_D#26	N2	H_A#28	E19
H_D#27	Y7	H_A#29	B17
H_D#28	Y9	H_A#30	B15
H_D#29	P4	H_A#31	E17
H_D#30	W3	H_A#32	C18
H_D#31	N1	H_A#33	A19
H_D#32	AD12	H_A#34	B19
H_D#33	AE3	H_A#35	N19
H_D#34	AD9	H_ADS#	G12
H_D#35	AC9	H_ADSTB#	G12
H_D#36	AC7	H_ADSTB#0	A12
H_D#37	AC14	H_ADSTB#1	G20
H_D#38	AD11	H_BNR#	C8
H_D#39	AB2	H_BNR#	E8
H_D#40	AD7	H_BPR#	E12
H_D#41	Y3	H_BPR#	B8
H_D#42	Y3	H_DEFER#	D6
H_D#43	AC6	H_DBSY#	C10
H_D#44	AC5	AM5	AM7
H_D#45	AG3	HPLL_CLK	AM7
H_D#46	A#B	H_DPVR#	J8
H_D#47	A#B	H_DRDY#	K7
H_D#48	A1#4	H_HIT#	E4
H_D#49	AE9	H_HITM#	D8
H_D#50	AE11	H_LOCK#	G10
H_D#51	AH12	H_TRDY#	B7
H_D#52	A#E	H_DIN#0	K5
H_D#53	A#E	H_DIN#1	L2
H_D#54	A#E	H_DIN#2	AD13
H_D#55	A#E	H_DIN#3	AE13
H_D#56	A#E	H_DSTB#0	M7
H_D#57	A#E	H_DSTB#1	K3
H_D#58	A#E	H_DSTB#2	AD2
H_D#59	A#E	H_DSTB#3	AH11
H_D#60	A#E	H_DSTBP#0	L7
H_D#61	A#E	H_DSTBP#1	K2
H_D#62	A#E	H_DSTBP#2	AC2
H_D#63	A#E	H_DSTBP#3	A10

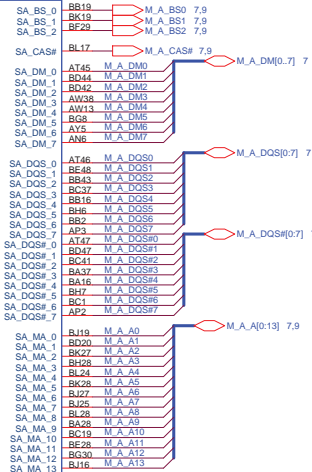


7 M\_A\_DQ[0:63]

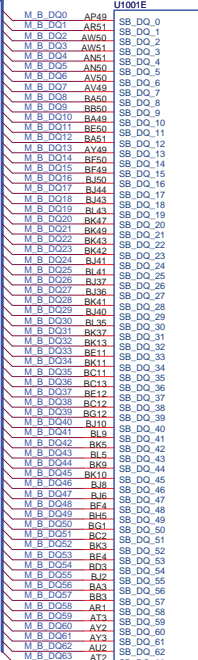


CRESTLINE\_965PM

DDR SYSTEM MEMORY A

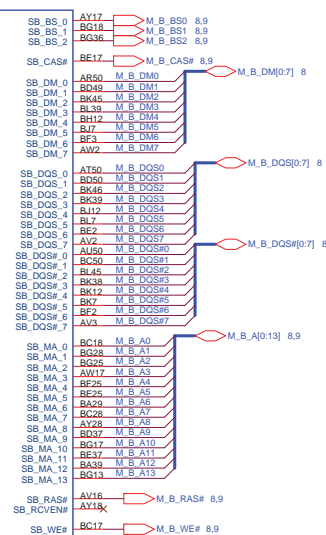


8 M\_B\_DQ[0:63]



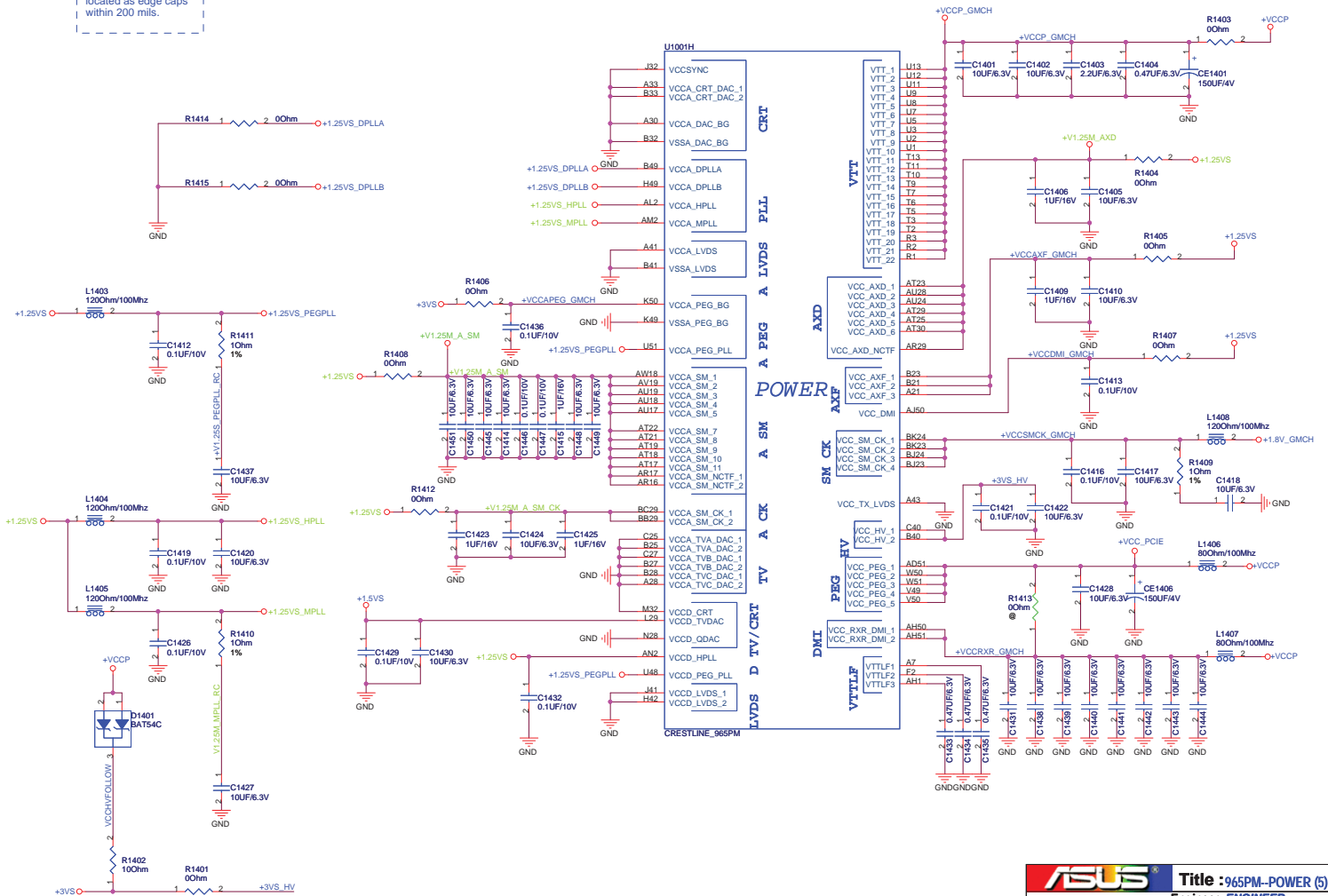
CRESTLINE\_965PM

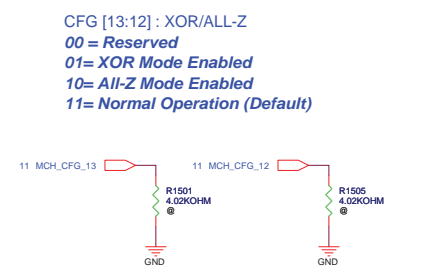
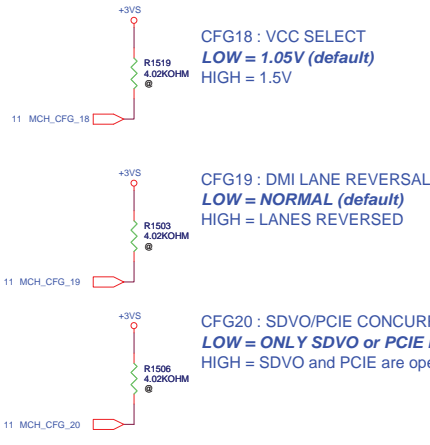
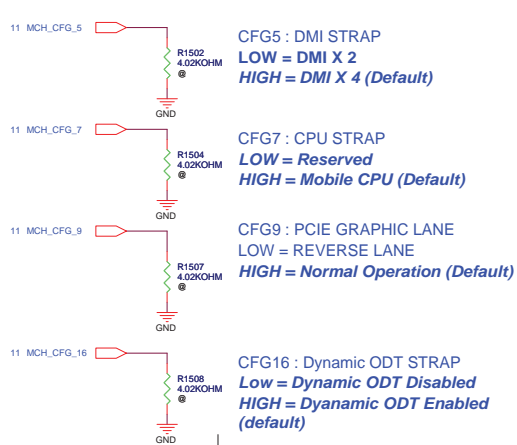
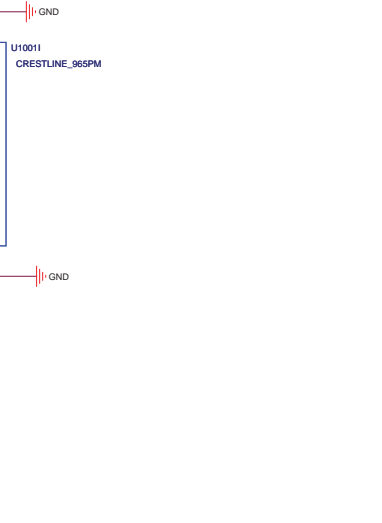
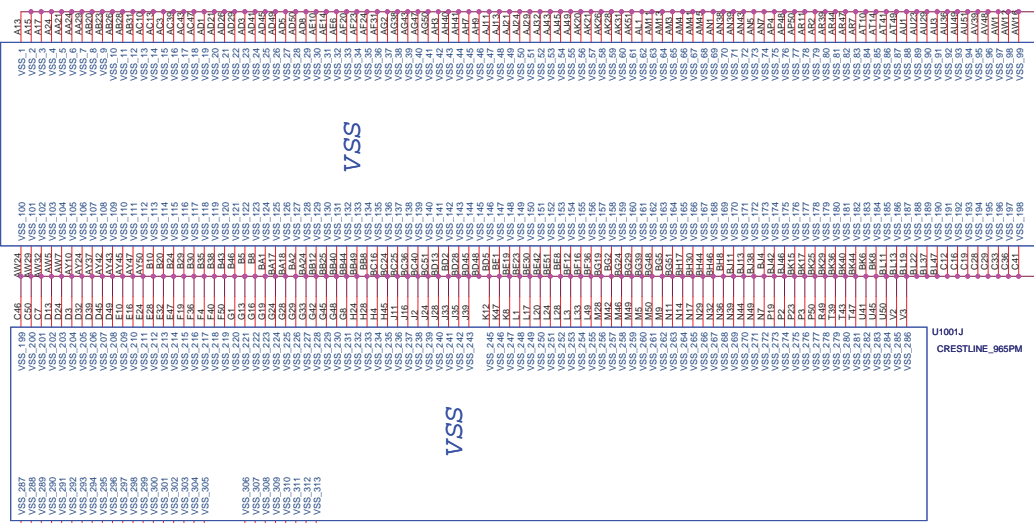
DDR SYSTEM MEMORY B





NOTE: 0.1uF caps in 1.5VS\_XPLL need to be located as edge caps within 200 mils.





5

4

3

2

1

D

D

C


C

B

B

A

A

		<b>Title : EMPTY</b>	
ASUSTeK COMPUTER INC		<b>Engineer: ENGINEER</b>	
Size	Project Name		Rev
A	<b>G1S</b>		1.1
Date: 星期五, 八月 03, 2007		Sheet	16 of 94

5

4

3

2

1



5

4

3

2

1

D

D

C


C

B

B

A

A

		<b>Title : EMPTY</b>	
ASUSTeK COMPUTER INC		<b>Engineer: ENGINEER</b>	
Size	Project Name	Rev	
A	<b>G1S</b>	1.1	
Date: 星期五, 八月 03, 2007		Sheet	17 of 94

5

4

3

2

1

5

4

3

2

1

D

D

C


C

B

B

A

A

		<b>Title : EMPTY</b>	
ASUSTeK COMPUTER INC		<b>Engineer: ENGINEER</b>	
Size	Project Name		Rev
A	<b>G1S</b>		1.1
Date: 星期五, 八月 03, 2007		Sheet	18 of 94

5

4

3

2

1

5

4

3

2

1

D

D

C


C

B

B

A

A

		<b>Title : EMPTY</b>	
ASUSTeK COMPUTER INC		<b>Engineer: ENGINEER</b>	
Size	Project Name	Rev	
A	<b>G1S</b>	1.1	
Date: 星期五, 八月 03, 2007		Sheet	19 of 94

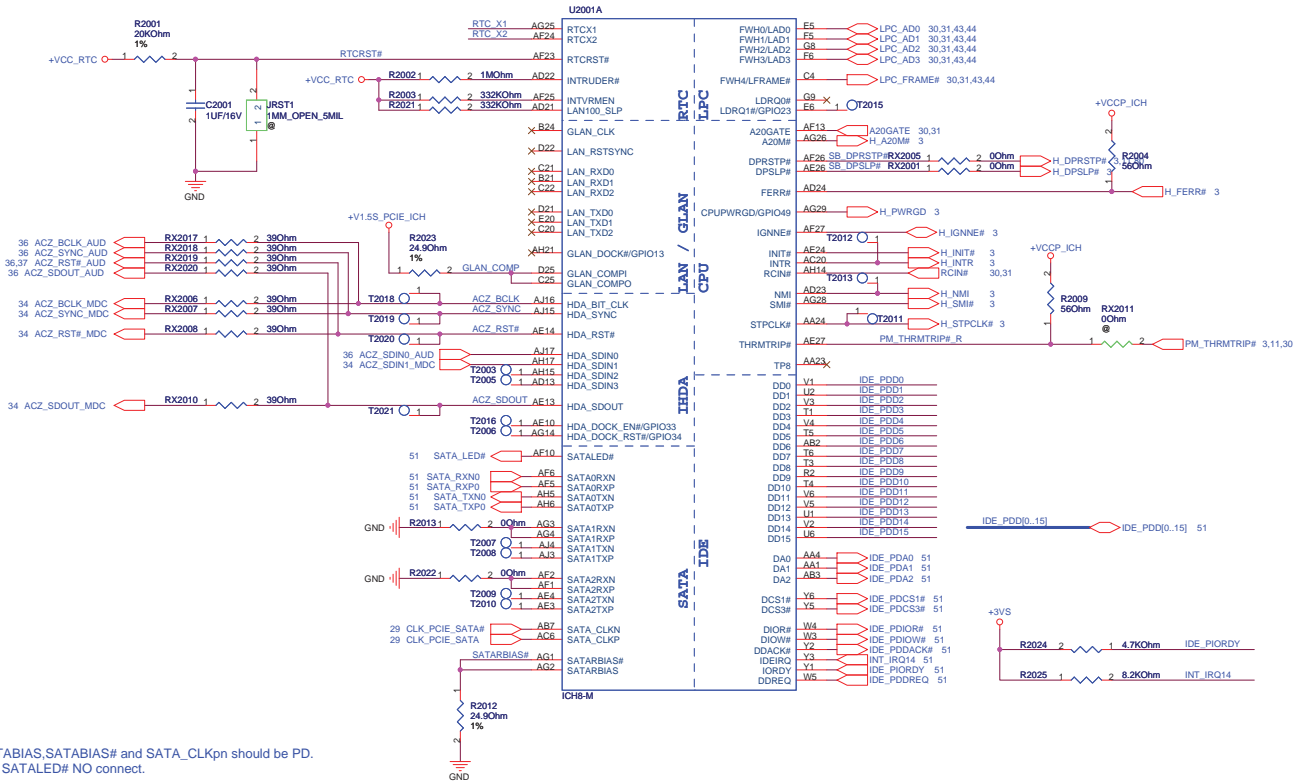
5

4

3

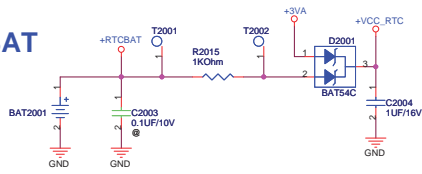
2

1

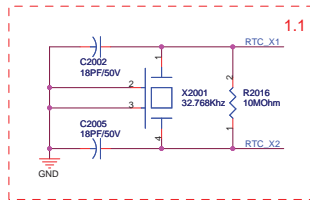


SATA if it non-used,  
 1)SATA[0:3]RXpn SATABIAS# and SATA\_CLKpn should be PD.  
 2)SATA[0:3]TXpn and SATALED# NO connect.

### RTC BAT

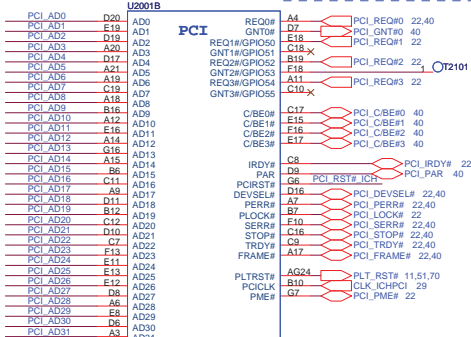
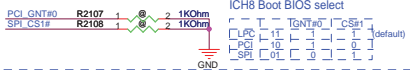


RTC Battery  
 P/N=07G016102032



<b>ASUS</b> <small>ASUSTeK COMPUTER INC</small>		<b>Title :ICH8-M (1)</b>	
Size <small>Project Name</small>		Engineer: <b>ENGINEER</b>	
Custom <b>G1S</b>		Rev 1.1	
Date: 2008.11.03.2007		Sheet 20 of 94	

40 PCI\_AD[0..31] PCI\_AD[0..31]

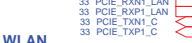


Interrupt I/F



ICH8-M

LAN



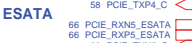
WLAN



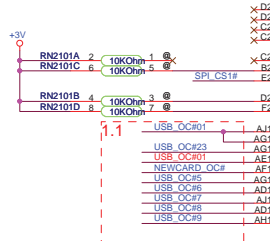
NEWCARD



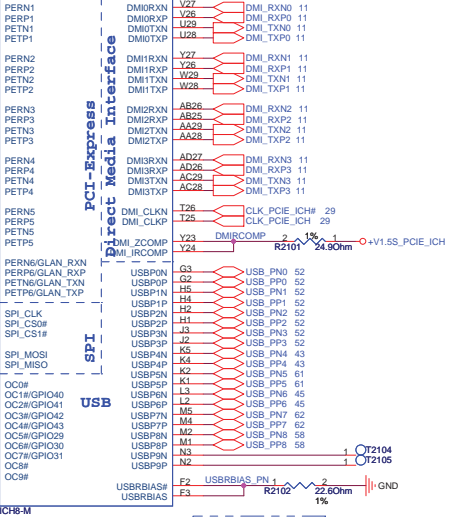
ROBSON



ESATA



U2001D

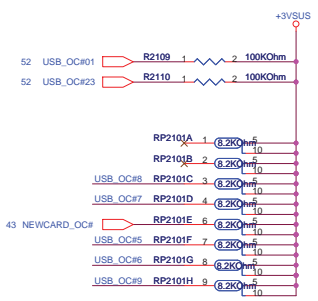
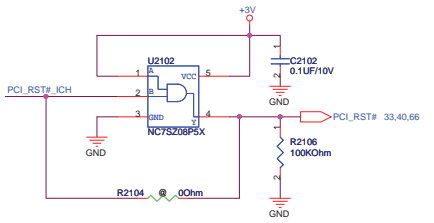
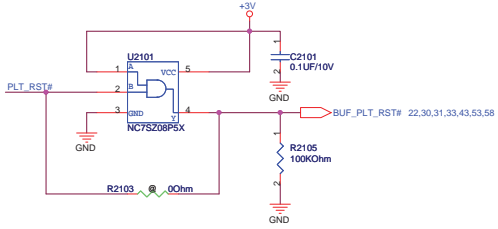


Direct Media Interface

PCI-Express

USB

ICH8-M



Place within 500 mils of ICH

**ASUS** Title : ICH8-M (2)  
 ASUSTek COMPUTER INC Engineer: ENGINEER  
 Size: Project Name  
 Custom: G1S  
 Date: 2007.03.03, 2007 Sheet 21 of 94

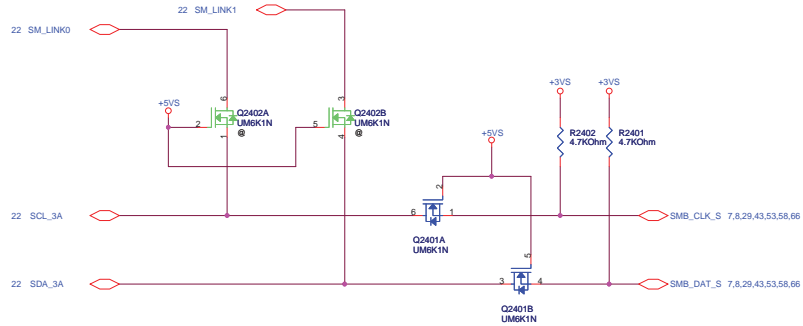




ICH8-M

ICH8-M

Connect SMLINK and SMBUS  
for SMBus 2.0 compliance.





5

4

3

2

1

D

D

C


C

B

B

A

A

		<b>Title : EMPTY</b>	
ASUSTeK COMPUTER INC		<b>Engineer: ENGINEER</b>	
Size	Project Name		Rev
A	<b>G1S</b>		1.1
Date: 星期五, 八月 03, 2007		Sheet	25 of 94

5

4

3

2

1

5

4

3

2

1

D

D

C


C

B

B

A

A

		<b>Title : EMPTY</b>	
ASUSTeK COMPUTER INC		<b>Engineer: ENGINEER</b>	
Size	Project Name	Rev	
A	<b>G1S</b>	1.1	
Date: 星期五, 八月 03, 2007		Sheet	26 of 94

5

4

3

2

1

5

4

3

2

1

D

D

C


C

B

B

A

A

		<b>Title : EMPTY</b>	
ASUSTeK COMPUTER INC		<b>Engineer: ENGINEER</b>	
Size	Project Name	Rev	
A	<b>G1S</b>	1.1	
Date: 星期五, 八月 03, 2007		Sheet	27 of 94

5

4

3

2

1

5

4

3

2

1

D

D

C


C

B

B

A

A

		<b>Title : EMPTY</b>	
ASUSTeK COMPUTER INC		<b>Engineer: ENGINEER</b>	
Size	Project Name		Rev
A	<b>G1S</b>		1.1
Date: 星期五, 八月 03, 2007		Sheet	28 of 94

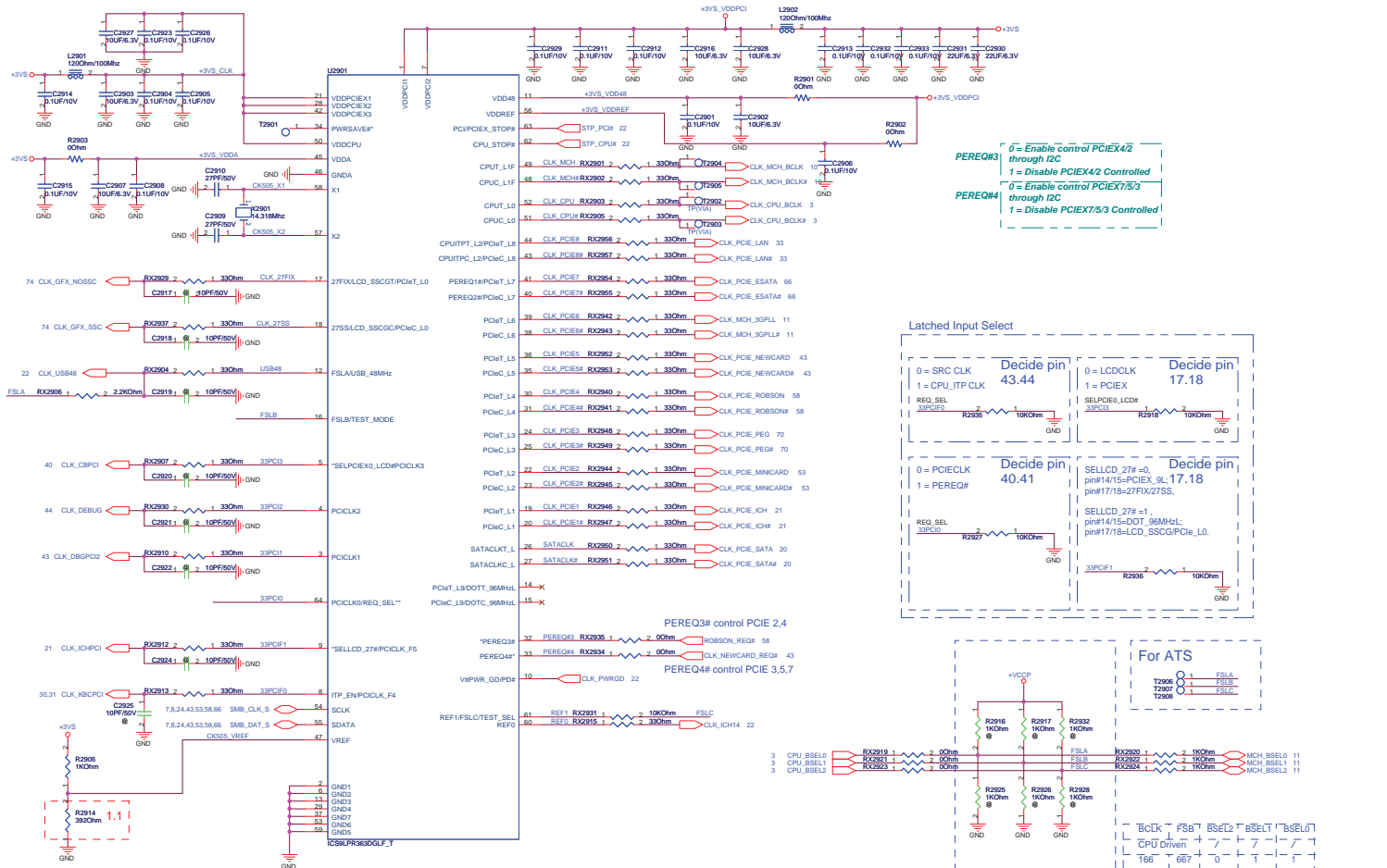
5

4

3

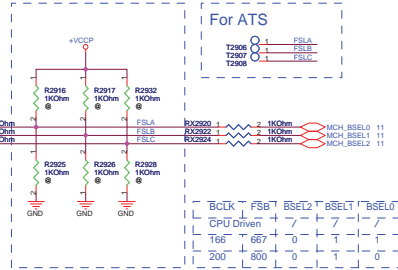
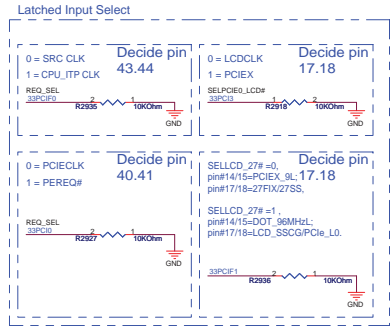
2

1



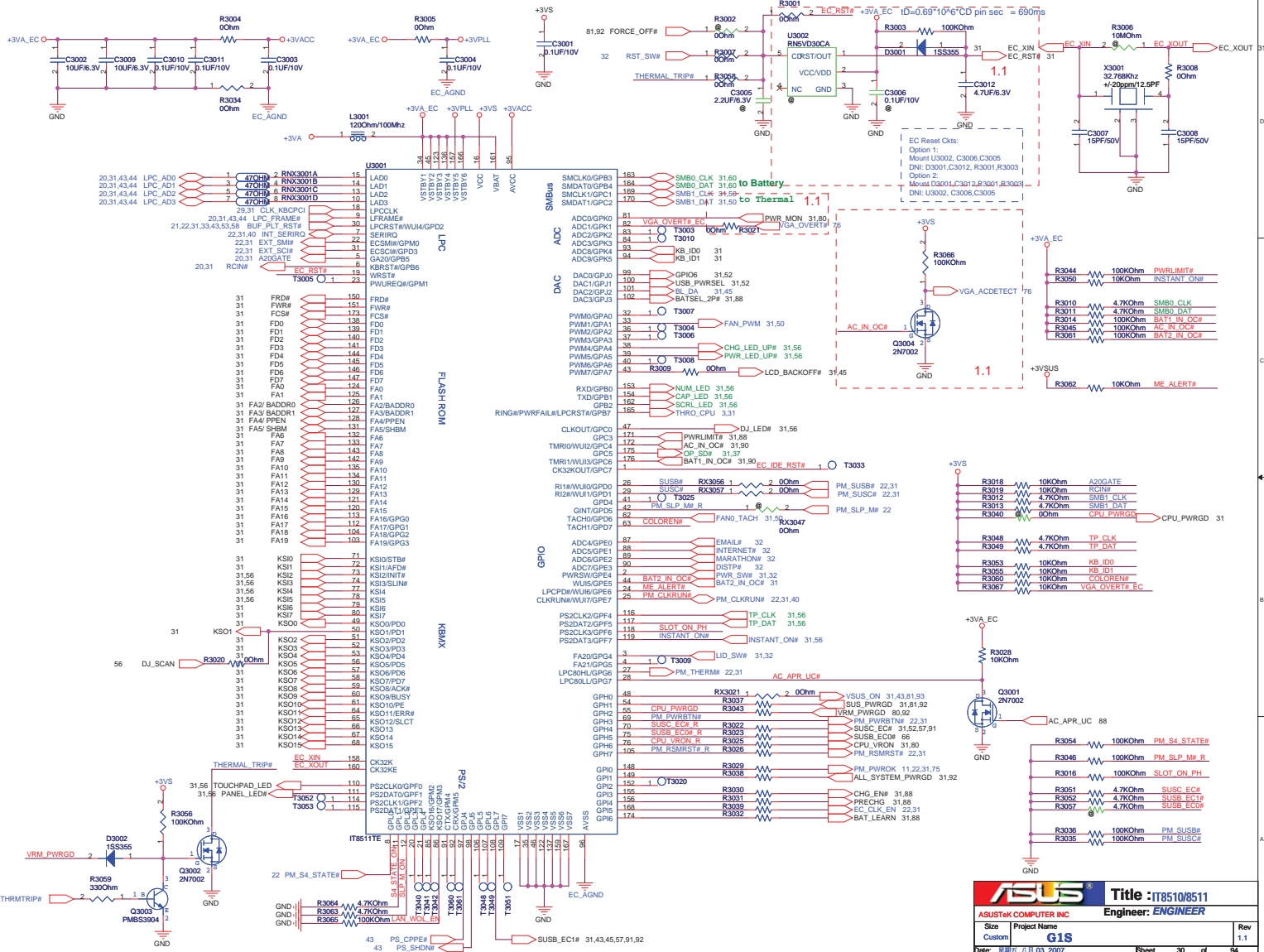
PEREQ#3  
 0 = Enable control PCIeX4/2 through I2C  
 1 = Disable PCIeX4/2 Controlled

PEREQ#4  
 0 = Enable control PCIeT5/3 through I2C  
 1 = Disable PCIeT5/3 Controlled!

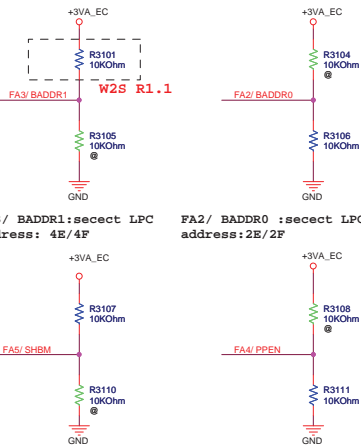


IC59LPR363GLF-T  
 INT-PU, INT-PD-F resistor value is 120K ohm.

SCH: 06G011408011 Ver: C  
 BOM: 06G011408012 Ver: D



10:Determined by EC



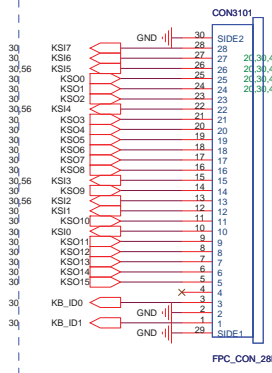
FA3/ BADDR1:select LPC address: 4E/4F

FA2/ BADDR0 :select LPC address: 2E/2F

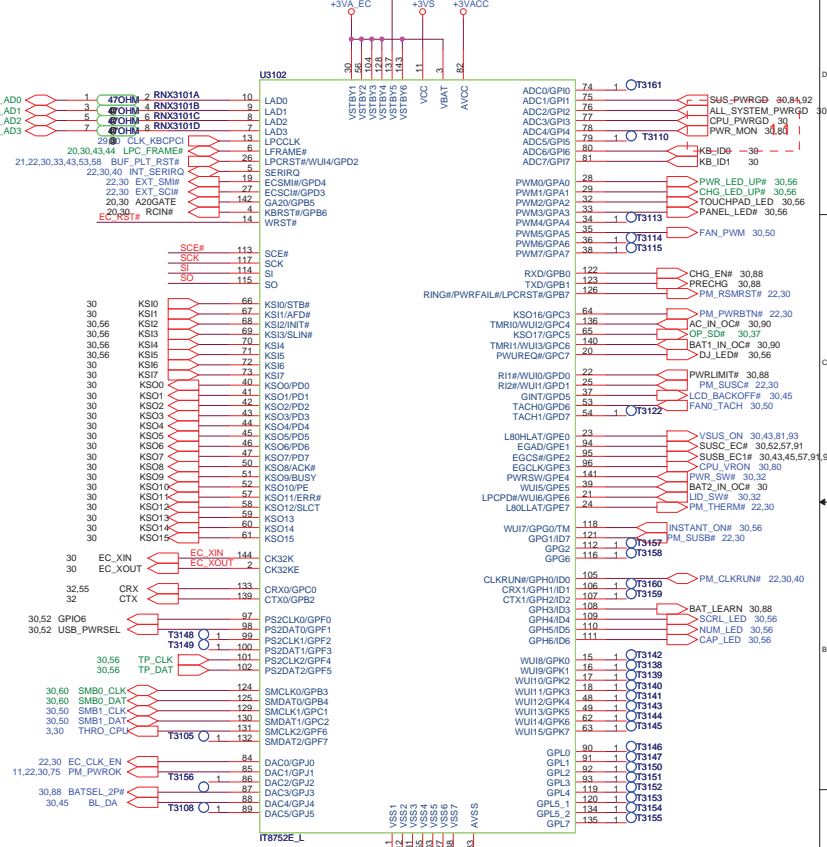
FA5/ SHBM:share BIOS mode enable.

FA4/ PPEN:enable in-system program via parallel port interface. (KBS down)

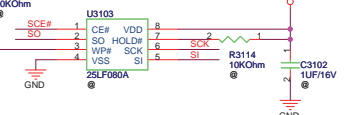
KBD CONN



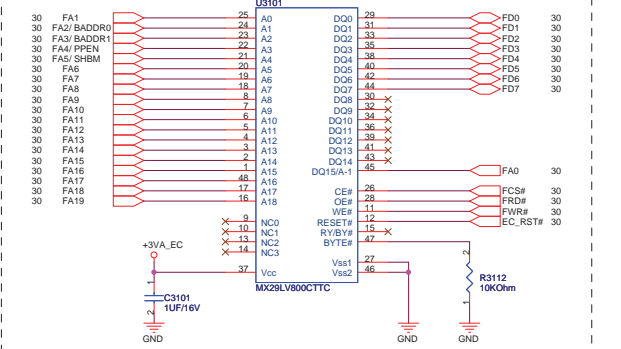
Colay IT8752E



1MB SPI ROM

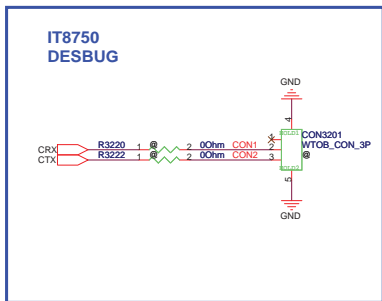
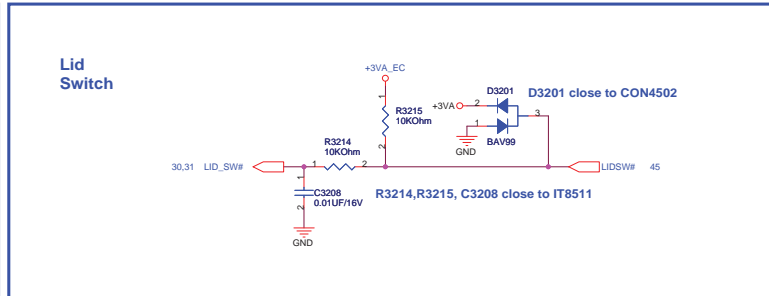
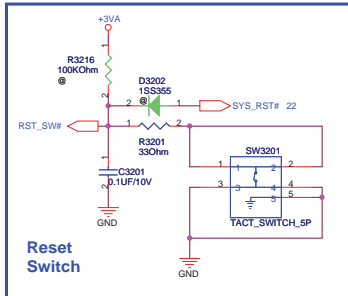
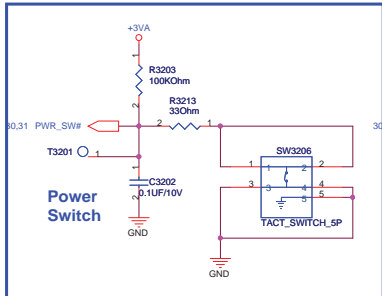
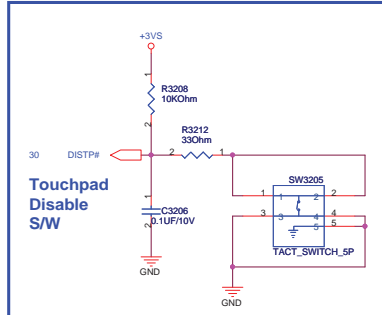
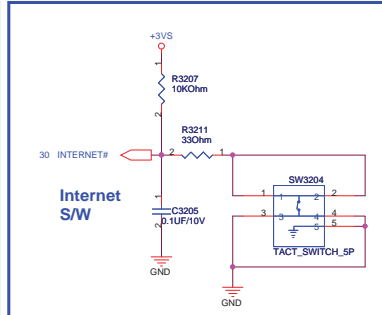
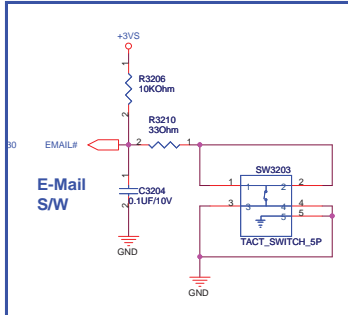
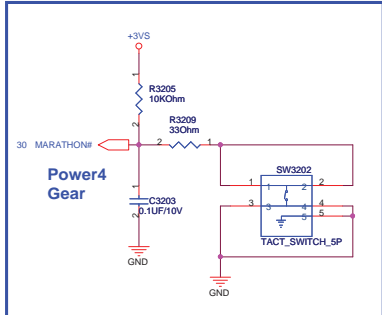


8M TSOP

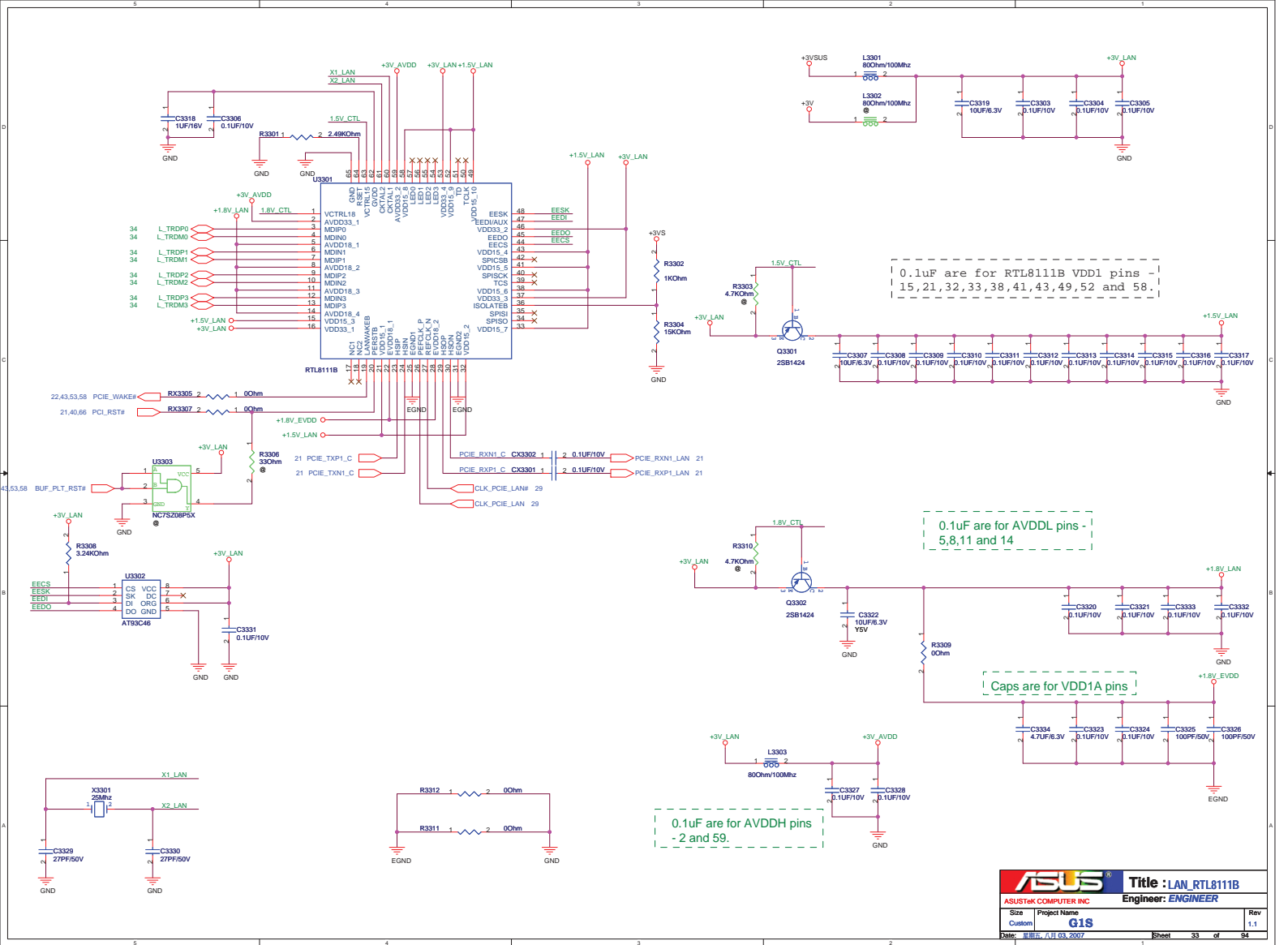


R1.1

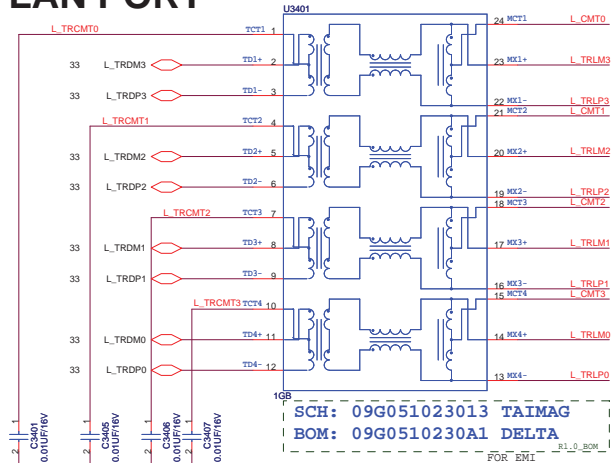
**ASUS** Title :IT8752E  
 ASUSTek COMPUTER INC Engineer: ENGINEER  
 Size: Custom Project Name: G1S  
 Date: 2007.03.03 2007 Sheet 31 of 94



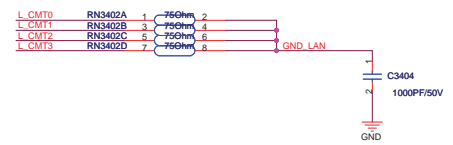




# LAN PORT



L_TRLM2	1	2	RNX3401A	L_TRLM2
L_TRLP2	3	4	RNX3401B	L_TRLP2
L_TRLM0	5	6	RNX3401C	L_TRLM0
L_TRLP0	7	8	RNX3401D	L_TRLP0
L_TRLP1	1	2	RNX3403A	L_TRLP1
L_TRLM1	3	4	RNX3403B	L_TRLM1
L_TRLM3	5	6	RNX3403C	L_TRLM3
L_TRLP3	7	8	RNX3403D	L_TRLP3



# MDC

