Falcon

Dolphin

FUJITSU CONFIDENTIAL

(Turion64 Rev.F/RS485M/SB450)

02版基板

Index

Version History

Version	Date	Description
Rev.01	2006.06.26	02版出図1
Rev.02	2006.06.30	02版出図2 (+Audio board 04版)
Rev.03	2006.07.04	02版出図3
Rev.04	2006.07.04	02版出図4

PCI REQ#/GNT#

REQ#/GNT#	Device
REQ#0	
REQ#1	
REQ#2	
REQ#3	PCIC / IEEE1394
REQ#4	
REQ#5	

PCI INTERRUPT

PCIINT#	Device
INT#0	
INT#1	
INT#2	
INT#3	
INT#4	PCIC(Slot1), PCIC(MS/SD), PCIC(IEEE1394)
INT#5	
INT#6	
INT#7	

PCI BUS NUMBER = #0 *Reserve*

IDSEL	Dev.Number	Device

PCI BUS NUMBER = #8

IDSEL	Dev.Number	Device
AD24	08h	PCIC / IEEE1394 /MSSD
AD25	09h	
AD26	0Ah	
AD27	0Bh	
AD28	0Ch	

SMBus

address	Device
A0h	LCD
A2h	DIMM1
A4h	DIMM2
5Eh	Thermal IC
D2h	PLL
32h	PMU

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Top Page

Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE: VB313AA

DRAW. No.: C1CP302570-X2 CAST

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Sheet 1 / 93

Dolphin

System block diagram

AMD K8 Rev.F
uFCPGA 638pin
P7-13

Thermal Sensor MAX6640 P14

DDR2 1.8V

DDR2 SoDIMM2 P24

DDR2 SoDIMM1 P23

Hyper Transport 800MHz

RS485M
465pin
21.0mm x 21.0mm
P15-20

LVDS → -OUT P51

RGB → CD P49

CRT P50

PCI-E x16 (For VGA) X

PCI-E x1 → nBoard G-LAN(88E8055) P63

PCI-E x1 → lini Card Atheros WirelessLAN) P62

PCI-E x1 → Express Card P61

PCI-E x1 X

A-LINK Express (PCI-E x2)

System DC/DC Module P79-86

Battery Module P87

PLL IDT CV137 P6

IDE0 ATA66/100 → PATA HDD P52

IDE1 ATA66/100 → PATA ODD P53

SB450
P27-33
564pin
31mm x 31mm

PCIC/IEEE1394/MS/SD/XD (OZ711MP1/OZ711SP1) P57-61

AZALIA → MDC MODEM P65

Audio CODEC ALC262 — Audio AMP — Audio JACK

Audio Board P94-99

SATA0 X
SATA1 X
SATA2 X
SATA3 X

LPC 3.3V 33MHz

LPC ROM M50LPW080 P37

BENN ASIC P54,55

TPM P48

LUNA2 PMU/KBC P90,91

KB P70

PAD P56

G-sensor P67

SIO LPC47N217

Sub Board

SERIAL

PARALLEL

USB2.0/1.1

Finger Sensor	USBCN47	USBCN22	USBCN22
USB7 P72	USB6 P66	USB5 P66	USB4 P66

USB2.0/1.1

ExpressCard	USBCN21	BlueTooth	USBCN21
USB3 P66	USB2 P66	USB1 P56	USB0 P66

RTC

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Block Diagram

Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

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DRAW. No.: C1CP302570-X2
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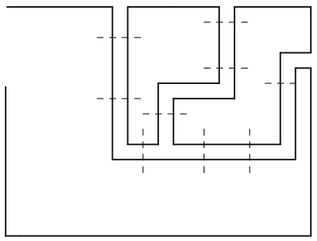
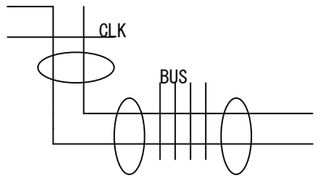
Sheet 2 / 93

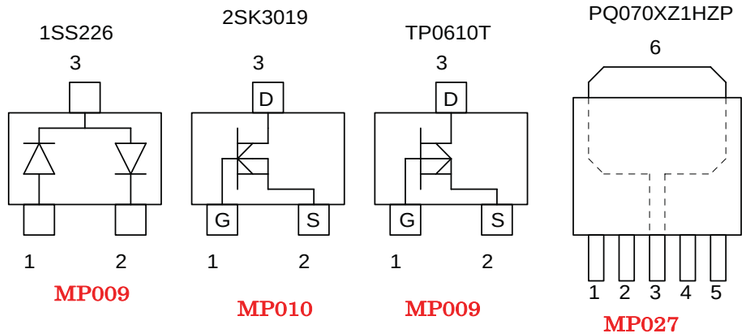
Dolphin

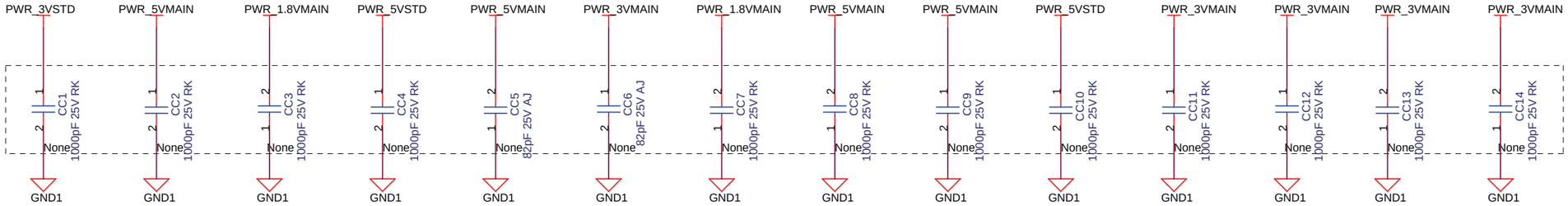
本部品は電波対策用であり、基板外周で電源-GND間に挿入する
ィルタ(スナバ回路)である。
周に均等に配置すること。またそれぞれの間隔は30mm間隔で配置
るように考慮すること。
た、特に電源の種別は便宜上設定しているものである。
、配置する場所により電源を設定すること。
については、適宜増やすこと。

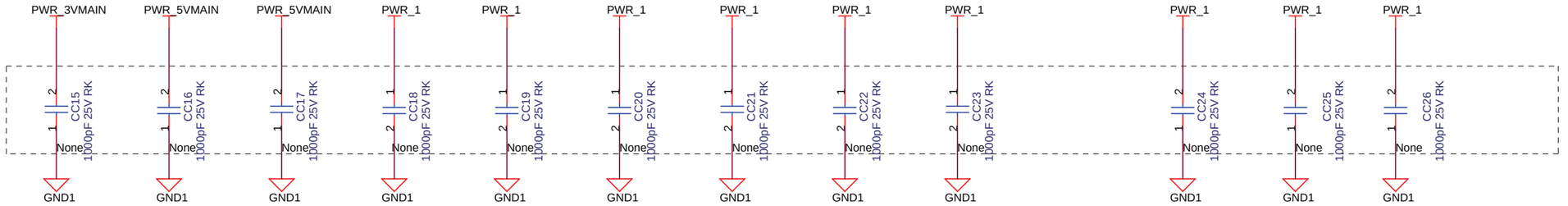


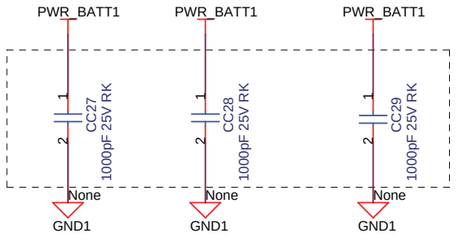


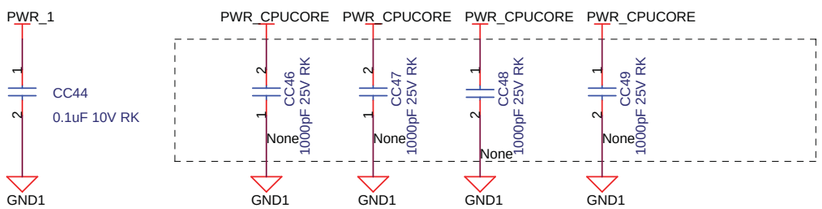
本コンデンサは電源/グランド層に発生するベタプレーン同士を接続する
ためのものである。
そのため、上記のようなベタ構成であれば、ポイントなる個所にコンデンサ
を配置する。
-クロックがベタをまたいで引く場合
-Bus系がベタをまたいで引く場合(数本毎に1個間隔で)
個数については、適宜増やすこと。











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R-C for EMI

Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE **VB313AA**

DRAW. No. C1CP302570-X2 CAST

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Sheet 3 / 93

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CPU_LDT_PWRGD
CPU_LDT_RST#
CPU_LDT_STOP#
CC70 100pF 25V AJ
CC71 100pF 25V AJ
CC72 100pF 25V AJ
GND1

CPU(CN1)の近傍に配置

54,55,76,88 LCDEN
54,69,91 SUSSW#
54,90,92,93 PMU_ACON
54,55,90 PMU_PLLB
29,54,55,57,72 PCI_RST#
54,90,92 PWROK_PMU
4,62,74,76,85,88 DLY_SUSB#
54,90 ASIC_PON
CC51 1000pF 25V RK
CC52 1000pF 25V RK
CC53 1000pF 25V RK
CC54 1000pF 25V RK
CC55 1000pF 25V RK
CC56 1000pF 25V RK
CC57 1000pF 25V RK
CC58 1000pF 25V RK
GND1

BENN(M10)の近傍に配置

62 A_RST#_MINIC
CC50 2200pF 25V RK
GND1

MiniCard(CN18)の近傍に配置

54,90,92 PWROK_PMU
29,91 KBC_A20G
36,5 63,76,91 A_RST#_C
66,7 76,88,91 SUSC#
54,69,91 SUSSW#
CC74 100pF 25V AJ
CC75 100pF 25V AJ
CC77 100pF 25V AJ
CC78 100pF 25V AJ
CC79 100pF 25V AJ
GND1

05/11
CC76削除

LUNA(M67)の近傍に配置

7,48,62,71,74,76 A_RST#_B
9,29,4 54,71,73,74 PWROK_3VMAIN
7,34,48,57,71,91 SERIRQ
CC80 100pF 25V AJ
CC81 100pF 25V AJ
CC82 100pF 25V AJ
GND1

SuperI/O(M40)の近傍に配置

49,74 BL_EEN_INV
49,54 BL_VOL
CC83 1000pF 25V RK
CC84 1000pF 25V RK
GND1

LCD CN(CN7)の近傍に配置

29 SB_PWROK_3VMAIN
9,29,34 SB_THERMTRIP#
27,34,48,57,71,91 SERIRQ
29,34,91 KBC_SCI
29,91 KBC_A20G
29,91 KBC_INIT#
29 SB_RSMRST#
29,34,75 BSRBTN#
29,34 S3_STATE
29,34,54 EXTSMI#
29,34,54 EXTSCI#
29,34,54 RIOUT#
29,34,90 SB_SMBALT#
29,54,55 PMEOUT#
29,34,61,63 PCIE_WAKE#
29,55 PLLB#
29,34,69 SB_LCDCL#
CC87 100pF 25V AJ
CC88 100pF 25V AJ
CC89 100pF 25V AJ
CC90 100pF 25V AJ
CC91 100pF 25V AJ
CC92 100pF 25V AJ
CC94 100pF 25V AJ
CC95 100pF 25V AJ
CC96 100pF 25V AJ
CC97 100pF 25V AJ
CC98 100pF 25V AJ
CC99 100pF 25V AJ
CC100 100pF 25V AJ
CC101 100pF 25V AJ
CC102 100pF 25V AJ
CC104 100pF 25V AJ
CC112 100pF 25V AJ
GND1

SB450(M4)の近傍に配置

57 PCIC_RST#
57,58,75 PCIC_GBRST#
CC85 100pF 25V AJ
CC86 100pF 25V AJ
GND1

PCIC(M12)の近傍に配置

52,53,74 RSTDRV#
CC120 2200pF 25V RK
CC105 2200pF 25V RK
GND1

ODD CN(CN12)の近傍に配置

16,29,36,76 A_RST#
16,76 NB_PWRGD
16,29 LDT_STOP#_NB
CC121 100pF 25V AJ
CC108 100pF 25V AJ
CC109 100pF 25V AJ
GND1

RS485M(M3)の近傍に配置

54,63 LAN_DISABLE#
63 LAN_RST#
CC106 1000pF 25V RK
CC107 1000pF 25V RK
GND1

LAN(M18)の近傍に配置

37,48,62,71,74,76 A_RST#_B
CC110 2200pF 25V RK
GND1

LPC ROM(M9)の近傍に配置

29,54,55 PMEOUT#
29,34,54 RIOUT#
54,62 WAKE_MINIC#
54,55 PME_ILAN#
54,55,57 PME_PCIC#
9,29,48,54,71,73,74 PWROK_3VMAIN
54,75 PWROK_3VSUS
CC168 1000pF 25V RK
CC169 1000pF 25V RK
CC170 1000pF 25V RK
CC171 1000pF 25V RK
CC172 1000pF 25V RK
CC173 1000pF 25V RK
CC174 1000pF 25V RK
GND1

BENN(M10)の近傍に配置

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R-C for ESD

Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE: VB313AA
DRAW. No.: C1CP302570-X2
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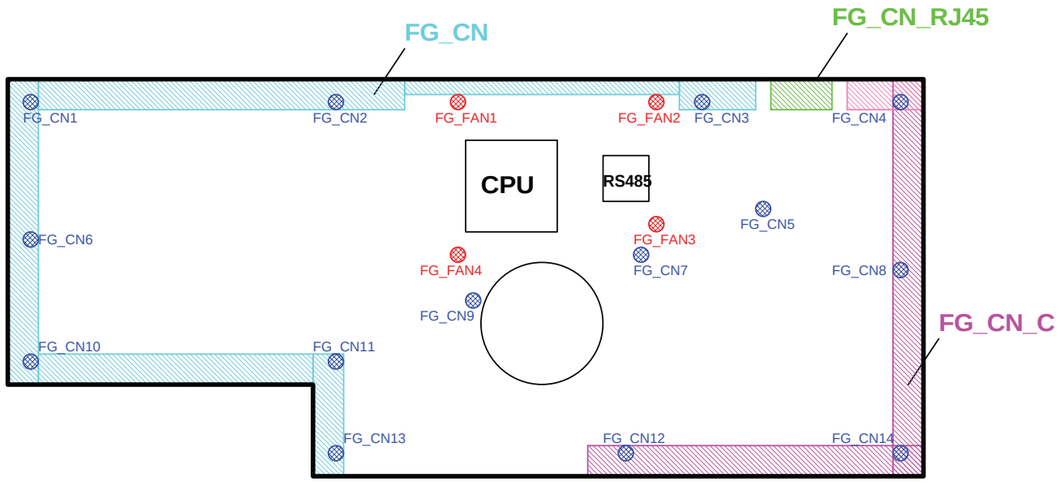
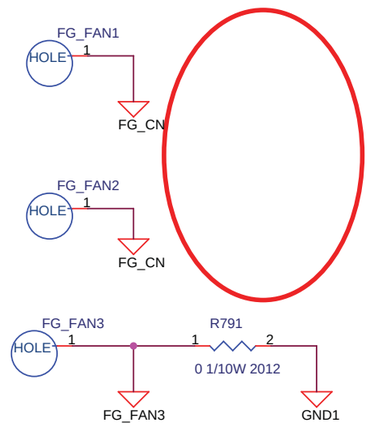
Sheet 4 / 93

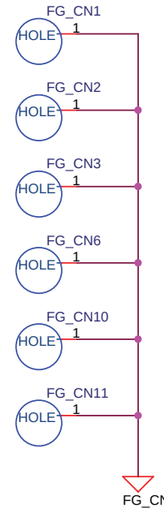
EMC対策

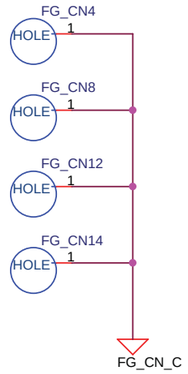
2006.7.4
02版: R721, R1

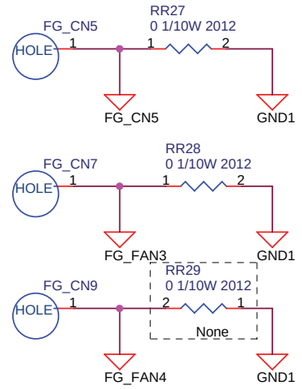
基板外周はFGグランド「FG_CN」,「FG_CN_C」,「FG_CN_RJ45」としてGND1から分離する。



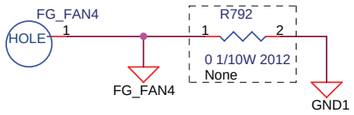


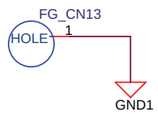






このFG_CNについては、全層で可能な限り接続する。
FG_CNとGND1とは1mmのギャップを取ること。
また、FG_CNについては信号線のGNDガードには使用せず、
その他信号についてもFG_CNから1.5mm以上離して配線すること。
（通す場合は相談すること。信号の種類によって判断する。）





FG-CN

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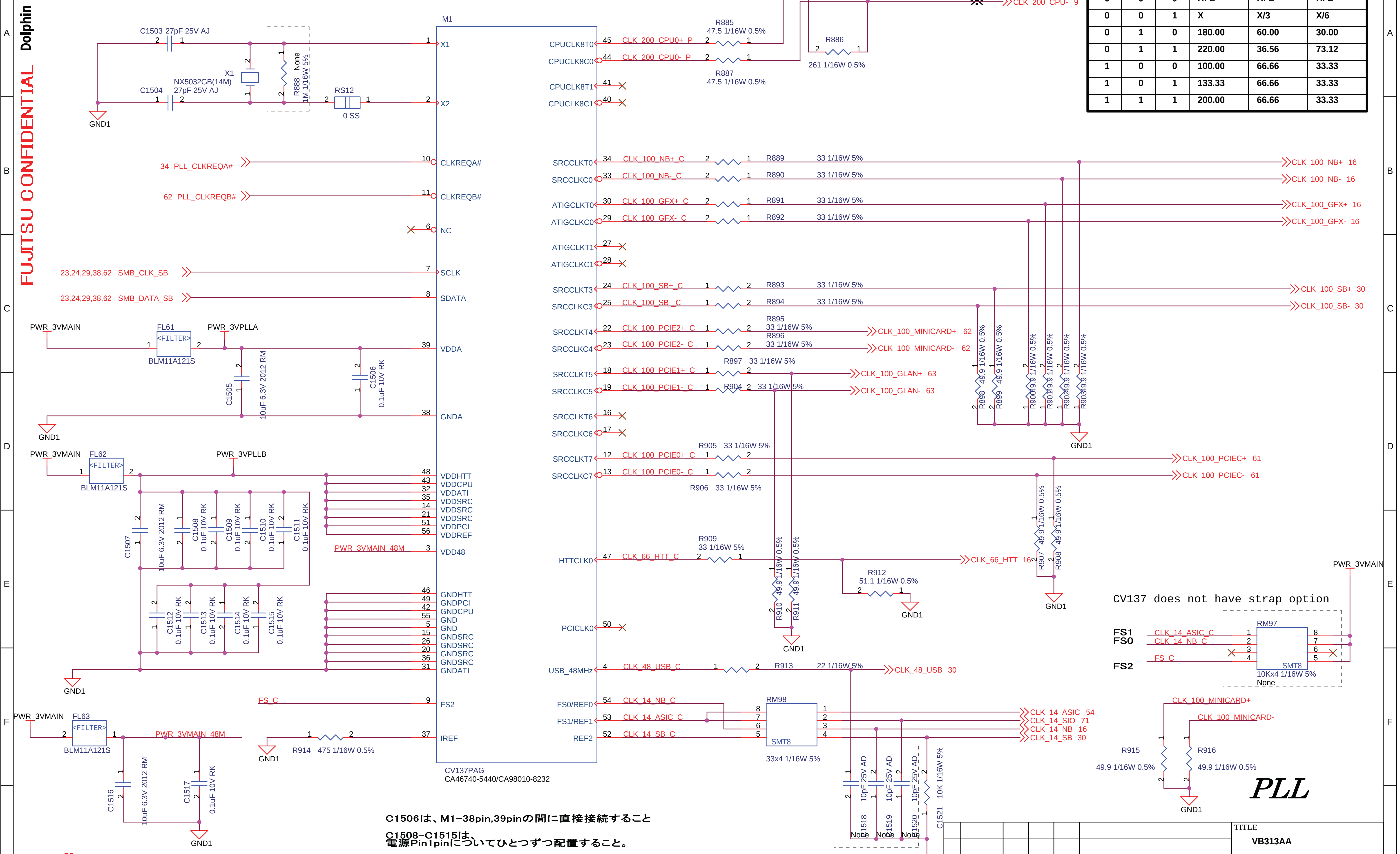
							TITLE	VB313AA
							DRAW. No.	C1CP302570-X2 CAST
Rev.	Date	Design	Check	Appr.	Description		FUJITSU LTD.	Sheet 5 / 93
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	

X1の部品・配線の周辺・上下層はGNDでガードすること。
また、配線は極力短く行い、振動子及び周辺部品の
パッドの下層は配線禁止とする。

http://hobi-elektronika.net

FS2	FS1	FS0	CPU(MHz)	HTT(MHz)	PCI(MHz)
0	0	0	Hi-Z	Hi-Z	Hi-Z
0	0	1	X	X/3	X/6
0	1	0	180.00	60.00	30.00
0	1	1	220.00	36.56	73.12
1	0	0	100.00	66.66	33.33
1	0	1	133.33	66.66	33.33
1	1	1	200.00	66.66	33.33



C1506は、M1−38pin,39pinの間に直接接続すること
C1508−C1515は、
電源Pin1pinについてひとつずつ配置すること。

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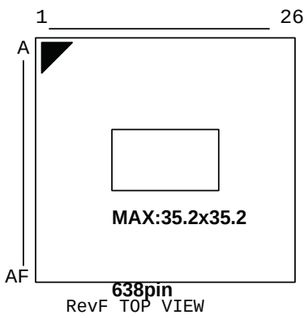
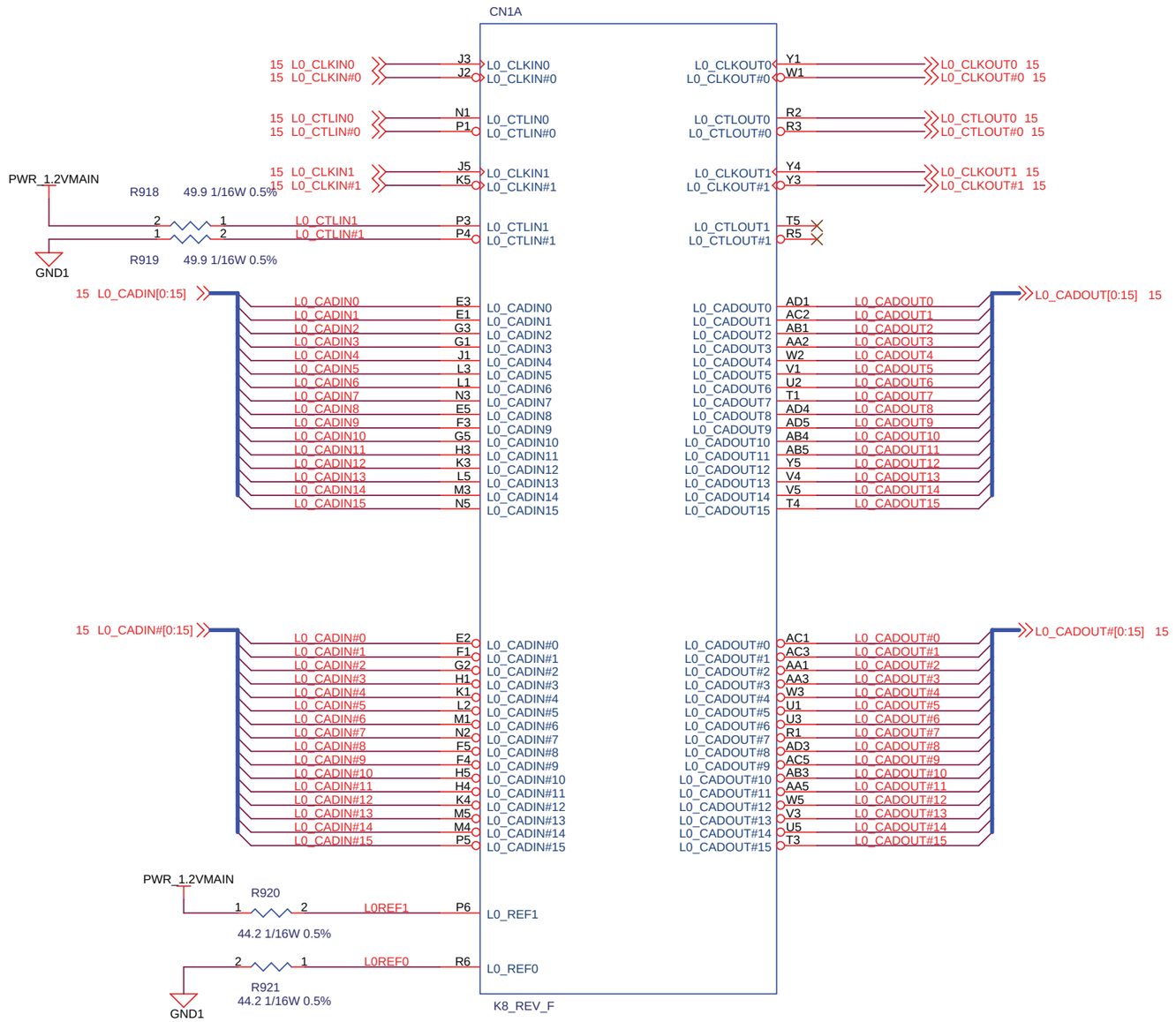
TITLE	VB313AA
DRAW. NO.	C1CP302570-X2
CAST	
Rev. / Date / Design / Check / Appr. / Description	
Design	06/07/04
Design	Mizukami
Check	Urita
Appr.	Hasegawa
	FUJITSU LTD.
Sheet	6 / 93

Dolphin





L0REF0,L0REF1は0.127mmの線幅にて配線し、
他の信号から0.254mm以上離すこと。
R920,R921は25.4mm以内に配置すること。

K8-1

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Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE: **VB313AA**

DRAW. No.: C1CP302570-X2 CAST

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Sheet 7 / 93

23 MEMA_D[0:63]

CN1B

MEMA_D0 G12
MEMA_D1 F12
MEMA_D2 H14
MEMA_D3 G14
MEMA_D4 H11
MEMA_D5 H12
MEMA_D6 C13
MEMA_D7 E13
MEMA_D8 H15
MEMA_D9 E15
MEMA_D10 E17
MEMA_D11 H17
MEMA_D12 E14
MEMA_D13 F14
MEMA_D14 C17
MEMA_D15 G17
MEMA_D16 G18
MEMA_D17 C19
MEMA_D18 D22
MEMA_D19 E20
MEMA_D20 E18
MEMA_D21 F18
MEMA_D22 B22
MEMA_D23 C23
MEMA_D24 F20
MEMA_D25 F22
MEMA_D26 H24
MEMA_D27 J19
MEMA_D28 E21
MEMA_D29 E22
MEMA_D30 H20
MEMA_D31 H22
MEMA_D32 Y24
MEMA_D33 AB24
MEMA_D34 AB22
MEMA_D35 AA21
MEMA_D36 W22
MEMA_D37 W21
MEMA_D38 Y22
MEMA_D39 AA22
MEMA_D40 Y20
MEMA_D41 AA20
MEMA_D42 AA18
MEMA_D43 AB18
MEMA_D44 AB21
MEMA_D45 AD21
MEMA_D46 AD19
MEMA_D47 Y18
MEMA_D48 AD17
MEMA_D49 W16
MEMA_D50 W14
MEMA_D51 Y14
MEMA_D52 Y17
MEMA_D53 AB17
MEMA_D54 AB15
MEMA_D55 AD15
MEMA_D56 AB13
MEMA_D57 AD13
MEMA_D58 Y12
MEMA_D59 W11
MEMA_D60 AB14
MEMA_D61 AA14
MEMA_D62 AB12
MEMA_D63 AA12

MA_DATA0 … MA_DATA63

MA_CKE0 J21 → MEMA_CKE0 23,25
MA_CKE1 J20 → MEMA_CKE1 23,25
MA_ODT0 U19 → MEMA_ODT0 23,25
MA_ODT1 V20 → MEMA_ODT1 23,25
MA_CLK1 E16 → MEMA_CLK1 23
MA_CLK#1 F16 → MEMA_CLK#1 23
MA_CLK2 Y16 → MEMA_CLK2 23
MA_CLK#2 AA16 → MEMA_CLK#2 23

MA_CS#0 T19 → MEMA_CS#0 23,25
MA_CS#1 V22 → MEMA_CS#1 23,25
MA_CS#2 J22 → MEMA_CS#2 23,25
MA_CS#3 V19 → MEMA_CS#3 23,25
MA_RAS# T20 → MEMA_RAS# 23,25
MA_CAS# U20 → MEMA_CAS# 23,25
MA_WE# U21 → MEMA_WE# 23,25
MA_BNK0 T22 → MEMA_BS#0 23,25
MA_BNK1 R20 → MEMA_BS#1 23,25
MA_BNK2 K22 → MEMA_BS#2 23,25

MA_ADD0 R21 MEMA_A0
MA_ADD1 N21 MEMA_A1
MA_ADD2 N22 MEMA_A2
MA_ADD3 M22 MEMA_A3
MA_ADD4 M24 MEMA_A4
MA_ADD5 M20 MEMA_A5
MA_ADD6 M19 MEMA_A6
MA_ADD7 L21 MEMA_A7
MA_ADD8 L22 MEMA_A8
MA_ADD9 L19 MEMA_A9
MA_ADD10 R19 MEMA_A10
MA_ADD11 L20 MEMA_A11
MA_ADD12 K24 MEMA_A12
MA_ADD13 V24 MEMA_A13
MA_ADD14 K20 MEMA_A14
MA_ADD15 K19 MEMA_A15
→ MEMA_A[0:15] 23,25

23 MEMA_DQS0 G13 → MA_DQS0
23 MEMA_DQS#0 H13 → MA_DQS0#
23 MEMA_DQS1 G16 → MA_DQS1
23 MEMA_DQS#1 G15 → MA_DQS1#
23 MEMA_DQS2 C22 → MA_DQS2
23 MEMA_DQS#2 C21 → MA_DQS2#
23 MEMA_DQS3 G22 → MA_DQS3
23 MEMA_DQS#3 G21 → MA_DQS3#
23 MEMA_DQS4 AD23 → MA_DQS4
23 MEMA_DQS#4 AC23 → MA_DQS4#
23 MEMA_DQS5 AB19 → MA_DQS5
23 MEMA_DQS#5 AB20 → MA_DQS5#
23 MEMA_DQS6 Y15 → MA_DQS6
23 MEMA_DQS#6 W15 → MA_DQS6#
23 MEMA_DQS7 W12 → MA_DQS7
23 MEMA_DQS#7 W13 → MA_DQS7#

23 MEMA_DM0 E12 → MA_DM0
23 MEMA_DM1 C15 → MA_DM1
23 MEMA_DM2 E19 → MA_DM2
23 MEMA_DM3 F24 → MA_DM3
23 MEMA_DM4 AC24 → MA_DM4
23 MEMA_DM5 Y19 → MA_DM5
23 MEMA_DM6 AB16 → MA_DM6
23 MEMA_DM7 Y13 → MA_DM7

23,24,85 REF_MEM → W17 MEM_VREF

C1522 0.1uF 10V RK
C1523 100pF 25V RK
GND1

MEM_ZN AE10 R922 39.2 1/16W 0.5% 2 1 PWR_1.8VSUS
MEM_ZP AF10 R923 39.2 1/16W 0.5% 2 1 GND1

K8_REV_F

24 MEMB_D[0:63]

CN1C

MEMB_D0 C11
MEMB_D1 A11
MEMB_D2 A14
MEMB_D3 B14
MEMB_D4 G11
MEMB_D5 E11
MEMB_D6 D12
MEMB_D7 A13
MEMB_D8 A15
MEMB_D9 A16
MEMB_D10 A19
MEMB_D11 A20
MEMB_D12 C14
MEMB_D13 D14
MEMB_D14 C18
MEMB_D15 D18
MEMB_D16 D20
MEMB_D17 A21
MEMB_D18 D24
MEMB_D19 C25
MEMB_D20 B20
MEMB_D21 C20
MEMB_D22 B24
MEMB_D23 C24
MEMB_D24 E23
MEMB_D25 E24
MEMB_D26 G25
MEMB_D27 G26
MEMB_D28 C26
MEMB_D29 D26
MEMB_D30 G23
MEMB_D31 G24
MEMB_D32 AA24
MEMB_D33 AA23
MEMB_D34 AD24
MEMB_D35 AE24
MEMB_D36 AA26
MEMB_D37 AA25
MEMB_D38 AD26
MEMB_D39 AE25
MEMB_D40 AC22
MEMB_D41 AD22
MEMB_D42 AE20
MEMB_D43 AF20
MEMB_D44 AF24
MEMB_D45 AF23
MEMB_D46 AC20
MEMB_D47 AD20
MEMB_D48 AD18
MEMB_D49 AE18
MEMB_D50 AC14
MEMB_D51 AD14
MEMB_D52 AF19
MEMB_D53 AC18
MEMB_D54 AF16
MEMB_D55 AF15
MEMB_D56 AF13
MEMB_D57 AC12
MEMB_D58 AB11
MEMB_D59 Y11
MEMB_D60 AE14
MEMB_D61 AF14
MEMB_D62 AF11
MEMB_D63 AD11

MB_DATA0 … MB_DATA63

MB_CKE0 J23 → MEMB_CKE0 24,25
MB_CKE1 H26 → MEMB_CKE1 24,25
MB_ODT0 W26 → MEMB_ODT0 24,25
MB_ODT1 W23 → MEMB_ODT1 24,25
MB_CLK1 A17 → MEMB_CLK1 24
MB_CLK#1 A18 → MEMB_CLK#1 24
MB_CLK2 AF18 → MEMB_CLK2 24
MB_CLK#2 AF17 → MEMB_CLK#2 24

MB_CS#0 U23 → MEMB_CS#0 24,25
MB_CS#1 W24 → MEMB_CS#1 24,25
MB_CS#2 J24 → MEMB_CS#2 24,25
MB_CS#3 Y26 → MEMB_CS#3 24,25
MB_RAS# U24 → MEMB_RAS# 24,25
MB_CAS# V26 → MEMB_CAS# 24,25
MB_WE# U22 → MEMB_WE# 24,25
MB_BNK0 U26 → MEMB_BS#0 24,25
MB_BNK1 T26 → MEMB_BS#1 24,25
MB_BNK2 K26 → MEMB_BS#2 24,25

MB_ADD0 T24 MEMB_A0
MB_ADD1 P26 MEMB_A1
MB_ADD2 P24 MEMB_A2
MB_ADD3 N26 MEMB_A3
MB_ADD4 N25 MEMB_A4
MB_ADD5 N24 MEMB_A5
MB_ADD6 N23 MEMB_A6
MB_ADD7 L26 MEMB_A7
MB_ADD8 M26 MEMB_A8
MB_ADD9 L24 MEMB_A9
MB_ADD10 U25 MEMB_A10
MB_ADD11 L25 MEMB_A11
MB_ADD12 L23 MEMB_A12
MB_ADD13 W25 MEMB_A13
MB_ADD14 J26 MEMB_A14
MB_ADD15 J25 MEMB_A15
→ MEMB_A[0:15] 24,25

24 MEMB_DQS0 C12 → MB_DQS0
24 MEMB_DQS#0 B12 → MB_DQS0#
24 MEMB_DQS1 D16 → MB_DQS1
24 MEMB_DQS#1 C16 → MB_DQS1#
24 MEMB_DQS2 A24 → MB_DQS2
24 MEMB_DQS#2 A23 → MB_DQS2#
24 MEMB_DQS3 F26 → MB_DQS3
24 MEMB_DQS#3 E26 → MB_DQS3#
24 MEMB_DQS4 AC25 → MB_DQS4
24 MEMB_DQS#4 AC26 → MB_DQS4#
24 MEMB_DQS5 AF21 → MB_DQS5
24 MEMB_DQS#5 AF22 → MB_DQS5#
24 MEMB_DQS6 AE16 → MB_DQS6
24 MEMB_DQS#6 AD16 → MB_DQS6#
24 MEMB_DQS7 AF12 → MB_DQS7
24 MEMB_DQS#7 AE12 → MB_DQS7#

24 MEMB_DM0 A12 → MB_DM0
24 MEMB_DM1 B16 → MB_DM1
24 MEMB_DM2 A22 → MB_DM2
24 MEMB_DM3 E25 → MB_DM3
24 MEMB_DM4 AB26 → MB_DM4
24 MEMB_DM5 AE22 → MB_DM5
24 MEMB_DM6 AC16 → MB_DM6
24 MEMB_DM7 AD12 → MB_DM7

K8_REV_F

MEM_ZN MEM_ZPは0.127mmの線幅にて配線し、
他の信号から0.254mm以上離すこと。
R922,R923は25.4mm以内に配置すること。

K8-2

Rev.	Date	Design	Check	Appr.	Description			
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	

TITLE: VB313AA
DRAW. No.: C1CP302570-X2
CAST
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Sheet 8 / 93

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R924は15.4mm以内に配置すること。
C1524,C1525は25.4mm以内に配置すること。

CN1D

6 CLK_200_CPU+ — C1524 3900pF 25V RK — R924 169 1/16W 1% — C1525 3900pF 25V RK — 6 CLK_200_CPU-

CLK_200_CPU+_C A9 CLKIN
CLK_200_CPU-_C A8 CLKIN#
DBREQ# E10 DBREQ#
VIA8
VIA9 TCK AC9 TCK
VIA11 TMS AA9 TMS
VIA12 TRST# AD9 TRST#
VIA13 TDI AF9 TDI

DBRDY G10 DBRDY — VIA7
TDO AE9 TDO — VIA10

14 CPU_THMDA W8 THERMDA
14,18 THMDC W7 THERMDC

THERMTRIP# AF6 CPU_THERMTRIP#

Q125 DTC143TE
PWR_1.8VSUS
SB_THERMTRIP# 4,29,34

4 CPU_LDT_RST# CPU_LDT_RST# B7 RESET#
4 CPU_LDT_PWRGD CPU_LDT_PWRGD A7 PWROK
4 CPU_LDT_STOP# CPU_LDT_STOP# F10 LDTSTOP#

PROCHOT# AC7 CPU_PROCHOT#

SIC AF4 SIC
SID AF5 SID

VID0 B5 CPU_VID0 79
VID1 C5 CPU_VID1 79
VID2 A4 CPU_VID2 79
VID3 A6 CPU_VID3 79
VID4 C6 CPU_VID4 79
VID5 A5 CPU_VID5 79

CPU_PRESENT# AC6 CPU_PRESENT#

14,34,90 THLTL#
THLTL — Q124A SSM6N15FU — Q124B SSM6N15FU — GND1

PSI# A3 CPU_PSI# 79

R930 80.6 1/16W 0.5%
FBCLKOUT C9 — FBCLKOUT# C8

CPU_TEST25 E9 TEST25
CPU_TEST25# E8 TEST25#
CPU_TEST19 G9 TEST19
CPU_TEST18 H10 TEST18
AA7 TEST13
C2 TEST9

TEST29 FBCLKOUT
TEST29# FBCLKOUT#

VIA15 VIA17 VIA19 VIA20 VIA22 — GND1
CPU_TEST17 D7 TEST17
CPU_TEST16 E7 TEST16
CPU_TEST15 F7 TEST15
CPU_TEST14 C7 TEST14
CPU_TEST12 AC8 TEST12

TEST24 AE7 CPU_TEST24 — VIA14
TEST23 AD7 CPU_TEST23 — VIA16
TEST22 AE8 CPU_TEST22 — VIA18
TEST21 AB8 CPU_TEST21
TEST20 AF7 CPU_TEST20 — VIA21

C3 TEST7
AA6 TEST6
Y6 TEST3
AB6 TEST2

TEST28 J7
TEST28# H8
AF8
TEST27 AE6 CPU_TEST26
TEST26 K8
TEST10 C4
TEST8

H18 RSVD0
R26 RSVD1
N19 RSVD2
P19 RSVD3

RSVD8 R24
RSVD9 R22
RSVD10 R23
RSVD11 AA8
RSVD12 C1
RSVD13 P22
RSVD14 P20

N20 RSVD4
H19 RSVD5
H16 RSVD6
R25 RSVD7

RSVD15 D5
RSVD16 W18
RSVD17 G6
RSVD18 H6
RSVD19 B18
RSVD20 B3

K8_REV_F

ROUTE AS 80ohm DIFEERENTIAL PAIR
PLACE IT CLOSE TO CPU WITHIN 1"

PWR_3VMAIN
THLTL — R925 330 1/16W 5% — 1 2

PWR_1.8VSUS
CPU_VID1 — R926 330 1/16W 5% — 1 2

RM99
CPU_PROCHOT# 8 1
SIC 5 4
SID 6 3
CPU_THERMTRIP# 7 2
SMT8
330x4 1/16W 5%

PWR_1.8VSUS
CPU_PRESENT# — R927 1K 1/16W 5% — 1 2
CPU_TEST25 — R928 510 1/16W 5% — 1 2
CPU_TEST25# — R929 510 1/16W 5% — 1 2
GND1

PWR_1.8VSUS
RM100
CPU_TEST26 4 5
CPU_TEST19 2 7
CPU_TEST18 1 8
CPU_TEST21 3 6
8.1WS
330x4 1/16W 5%
GND1

Revision Guide Errata
Number133適用

M124A
29 LDT_PWRGD 1
4,29,48,54,71,73,74 PWROK_3VMAIN 2
& SN74LVC08APW 1.8VSUS
3 LDT_PWRGD_B — R931 10 1/16W 5% — 2 1 — CPU_LDT_PWRGD 4

M124B
29 LDT_RST# 4
4,29,48,54,71,73,74 PWROK_3VMAIN 5
& SN74LVC08APW 1.8VSUS
6 LDT_RST#_B — R932 10 1/16W 5% — 2 1 — CPU_LDT_RST# 4

M124C
29 LDT_STOP# 9
4,29,48,54,71,73,74 PWROK_3VMAIN 10
& SN74LVC08APW 1.8VSUS
8 LDT_STOP#_B — R933 10 1/16W 5% — 2 1 — CPU_LDT_STOP# 4

M124D
12
13
& SN74LVC08APW 1.8VSUS
11
GND1

PWR_1.8VSUS
C1526 0.1uF 10V RK
M124E SN74LVC08APW
VCC 14
GND 7
1.8VSUS
GND1

K8-3

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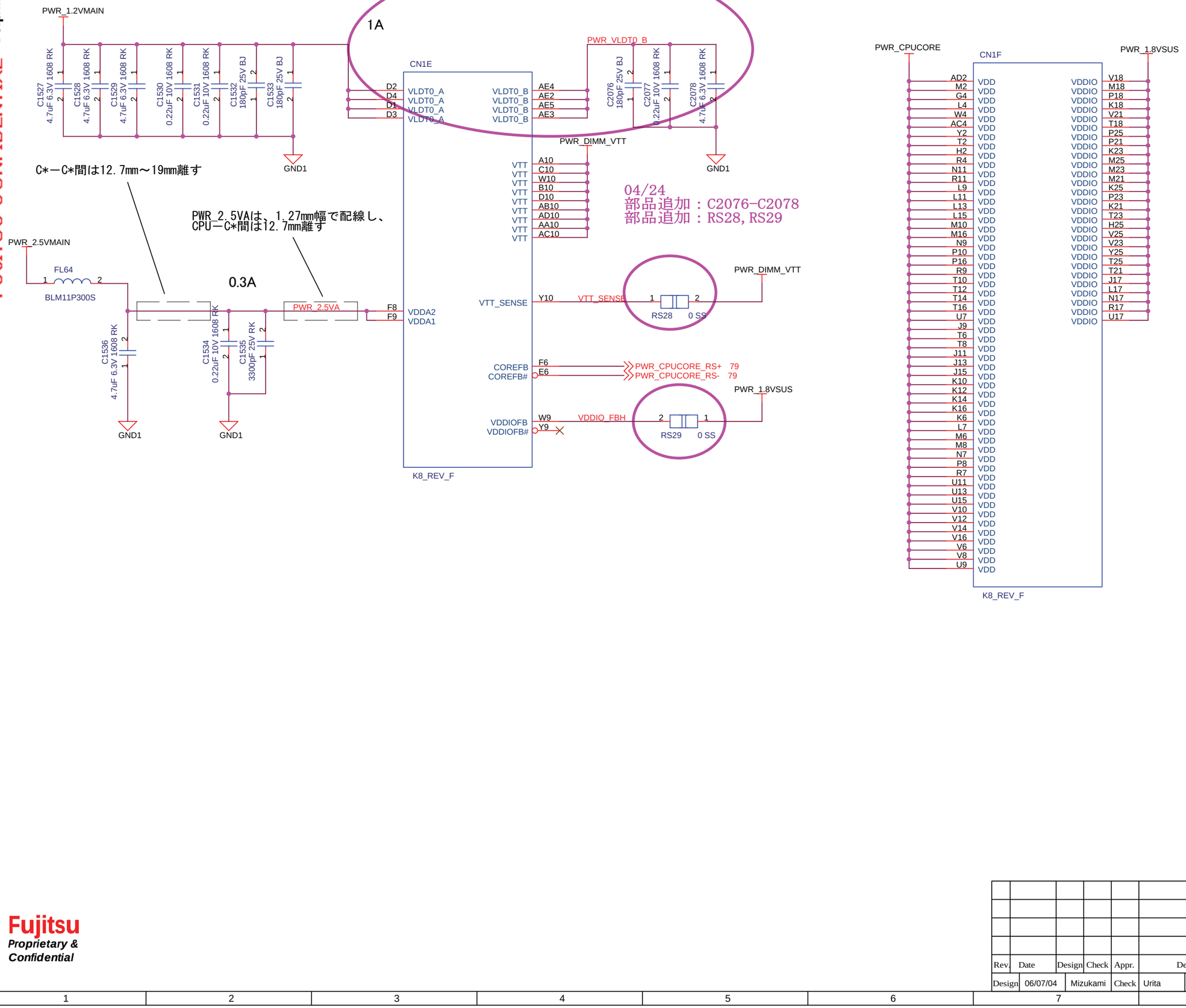
Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE: VB313AA
DRAW. No.: C1CP302570-X2
CAST
FUJITSU LTD.
Sheet 9 / 93



K8-4

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Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE: **VB313AA**

DRAW. No.: C1CP302570-X2 CAST

FUJITSU LTD. Sheet 10 / 93

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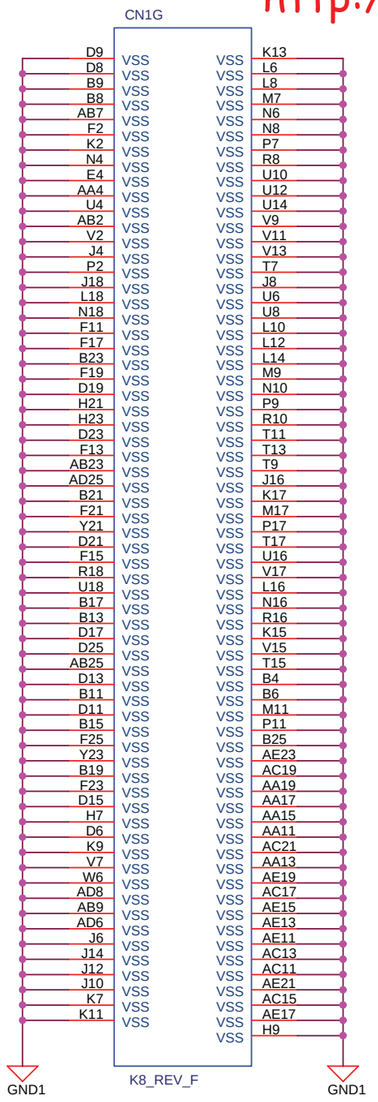

K8-5

Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE: **VB313AA**

DRAW. No.: C1CP302570-X2

CAST

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Sheet 11 / 93

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PWR_CPUCORE

C1537 22uF 6.3V 2012 RM
C1538 22uF 6.3V 2012 RM
C1539 22uF 6.3V 2012 RM
C1540 22uF 6.3V 2012 RM
C1541 22uF 6.3V 2012 RM
C1542 22uF 6.3V 2012 RM
C1543 22uF 6.3V 2012 RM
C1544 22uF 6.3V 2012 RM
C1545 22uF 6.3V 2012 RM
C1546 0.22uF 10V 1608 RK
C1547 0.22uF 10V 1608 RK
C1548 0.01uF 25V RK
C1549 180pF 25V BJ

GND1

PWR_CPUCORE

C1550 22uF 6.3V 2012 RM
C1551 22uF 6.3V 2012 RM
C1552 22uF 6.3V 2012 RM
C1553 22uF 6.3V 2012 RM
C1554 22uF 6.3V 2012 RM
C1555 22uF 6.3V 2012 RM
C1556 22uF 6.3V 2012 RM
C1557 22uF 6.3V 2012 RM
C1558 22uF 6.3V 2012 RM
C1559 22uF 6.3V 2012 RM
C1560 10uF 6.3V 1608 RM
C1561 10uF 6.3V 1608 RM
C1562 22uF 6.3V 2012 RM
C1563 22uF 6.3V 2012 RM
C1564 22uF 6.3V 2012 RM
C1725 10uF 6.3V 1608 RM
C1726 10uF 6.3V 1608 RM

GND1

PWR_1.8VSUS

C2079 220uF 2.5V(NEO/TPE) B21 CAT22-D0E2200M
C1565 22uF 6.3V 2012 RM
C1566 22uF 6.3V 2012 RM
C1567 4.7uF 6.3V 1608 RK
C1568 4.7uF 6.3V 1608 RK
C1569 4.7uF 6.3V 1608 RK
C1570 4.7uF 6.3V 1608 RK
C1571 0.22uF 10V 1608 RK
C1572 0.22uF 10V 1608 RK
C1573 0.22uF 10V 1608 RK
C1574 0.22uF 10V 1608 RK
C1575 0.22uF 10V 1608 RK
C1576 0.22uF 10V 1608 RK
C1577 0.01uF 25V RK
C1578 0.01uF 25V RK
C1579 180pF 25V BJ
C1580 180pF 25V BJ

GND1

PWR_DIMM_VTT

C1581 4.7uF 6.3V 1608 RK
C1582 4.7uF 6.3V 1608 RK
C1583 4.7uF 6.3V 1608 RK
C1584 4.7uF 6.3V 1608 RK
C1585 0.22uF 10V 1608 RK
C1586 0.22uF 10V 1608 RK
C1587 0.22uF 10V 1608 RK
C1588 0.22uF 10V 1608 RK
C1589 1000pF 25V RK
C1590 1000pF 25V RK
C1591 1000pF 25V RK
C1592 1000pF 25V RK
C1593 180pF 25V BJ
C1594 180pF 25V BJ
C1595 180pF 25V BJ
C1596 180pF 25V BJ

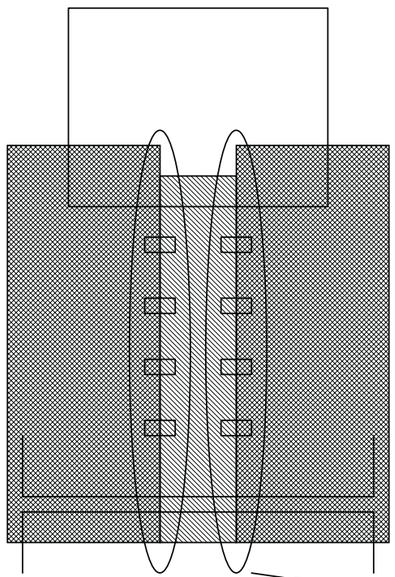
GND1

PWR_1.8VSUS

C1597 0.1uF 10V RK
C1598 0.1uF 10V RK None
C1599 0.1uF 10V RK
C1600 0.1uF 10V RK
C1601 0.1uF 10V RK
C1602 0.1uF 10V RK None
C1603 0.1uF 10V RK
C1604 0.1uF 10V RK None

GND1

K8_CPU



これらのコンデンサC1597～C1604は、図のように
PWR_1.8VSUS,GND1のプレーンの間に
約1インチ間隔で配置すること。

CPU PASS_C

							TITLE	VB313AA
							DRAW. No.	C1CP302570-X2
							CAST	
Rev.	Date	Design	Check	Appr.	Description		FUJITSU LTD.	Sheet 12 / 93
Design	06/07/04	Mizukami	Check	Urita		Appr. Hasegawa		

Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE
VB313AA

DRAW. No.
C1CP302570-X2

CAST

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Sheet 13 / 93

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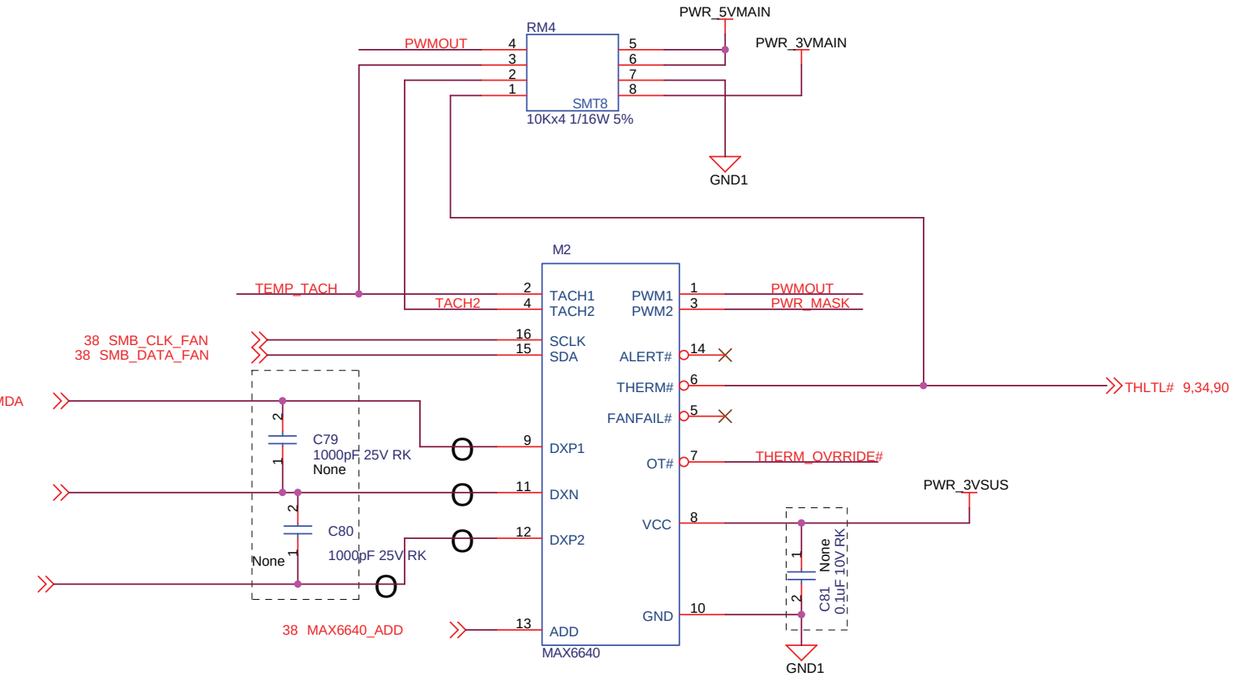


CPU_THMDA,
CPU_THMDCのパターンが最短に
なるよう、M2は、CPUの近傍に
配置すること。

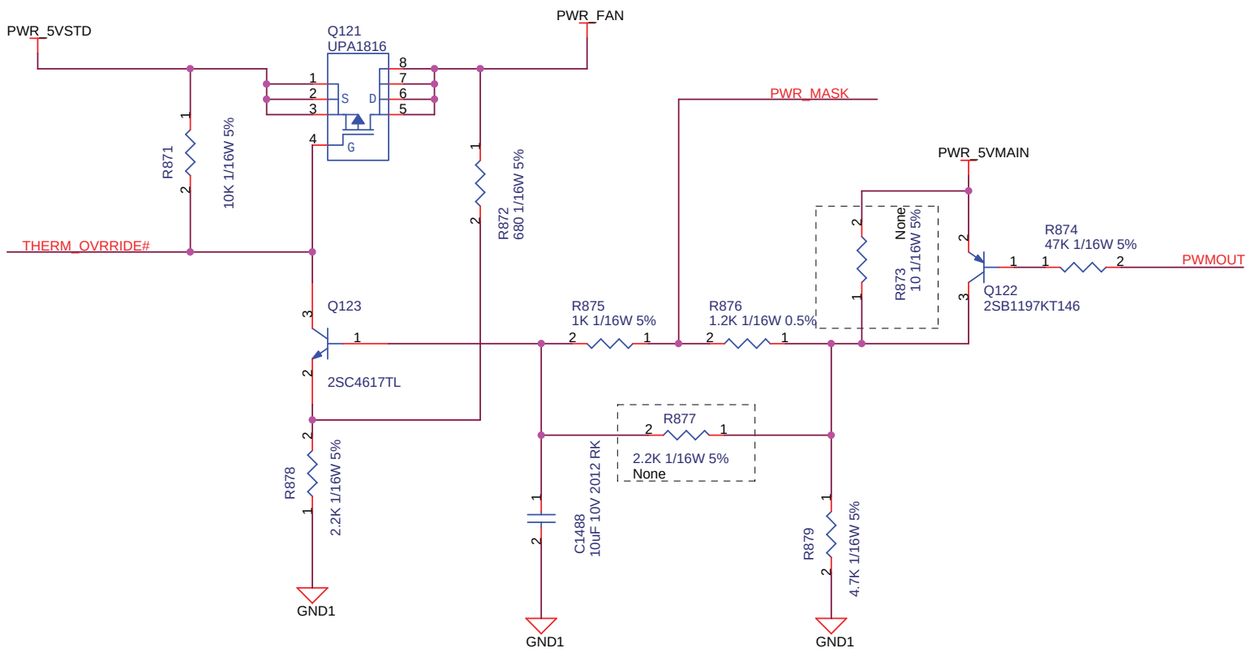
CPU_THMDA, CPU_THMDC,NB_THMDCA両端に入って
いるコンデンサC79,C80(1000pF)は、M2の直近に配置すること。

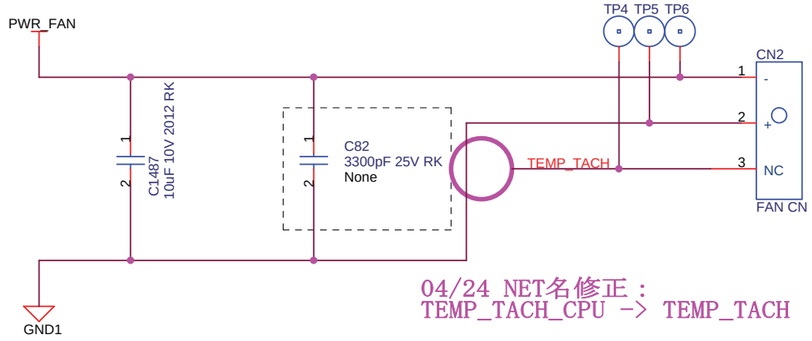
○印の付いた信号線は、GND1で両側をガードすること
(下図参照)

10mil (
10mil (
10mil (
10mil (

MAX6640
SMBAdress:01011110[5E固定]

5.0V 0.3A





04/24 NET名修正：
TEMP_TACH_CPU -> TEMP_TACH

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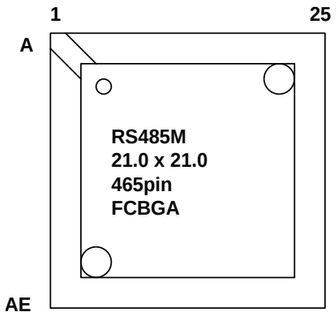
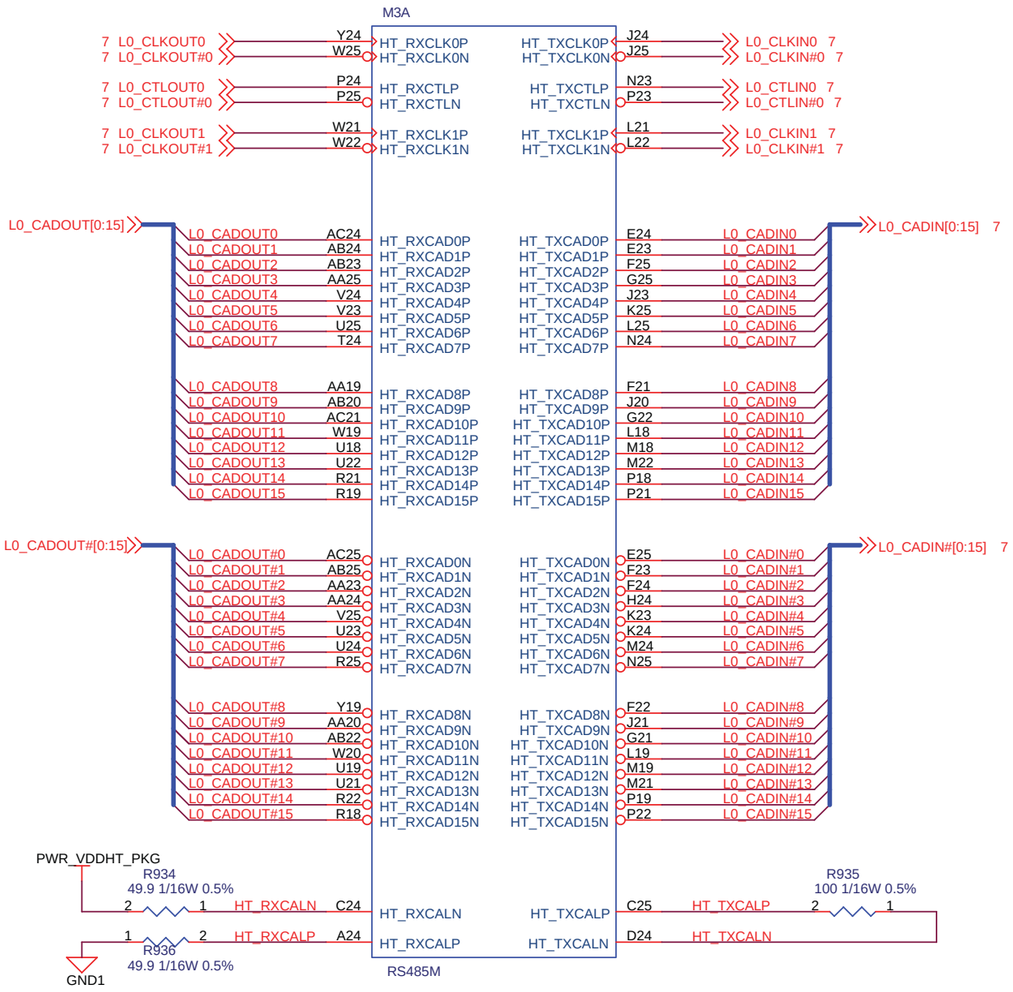
						TITLE	VB313AA
						DRAW. No.	C1CP302570-X2
						CAST	
Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.	Sheet 14 / 93
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa		

Dolphin





RS485-1

						TITLE	VB313AA
						DRAW. No.	C1CP302570-X2
						CAST	
Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.	Sheet 15 / 93
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa		

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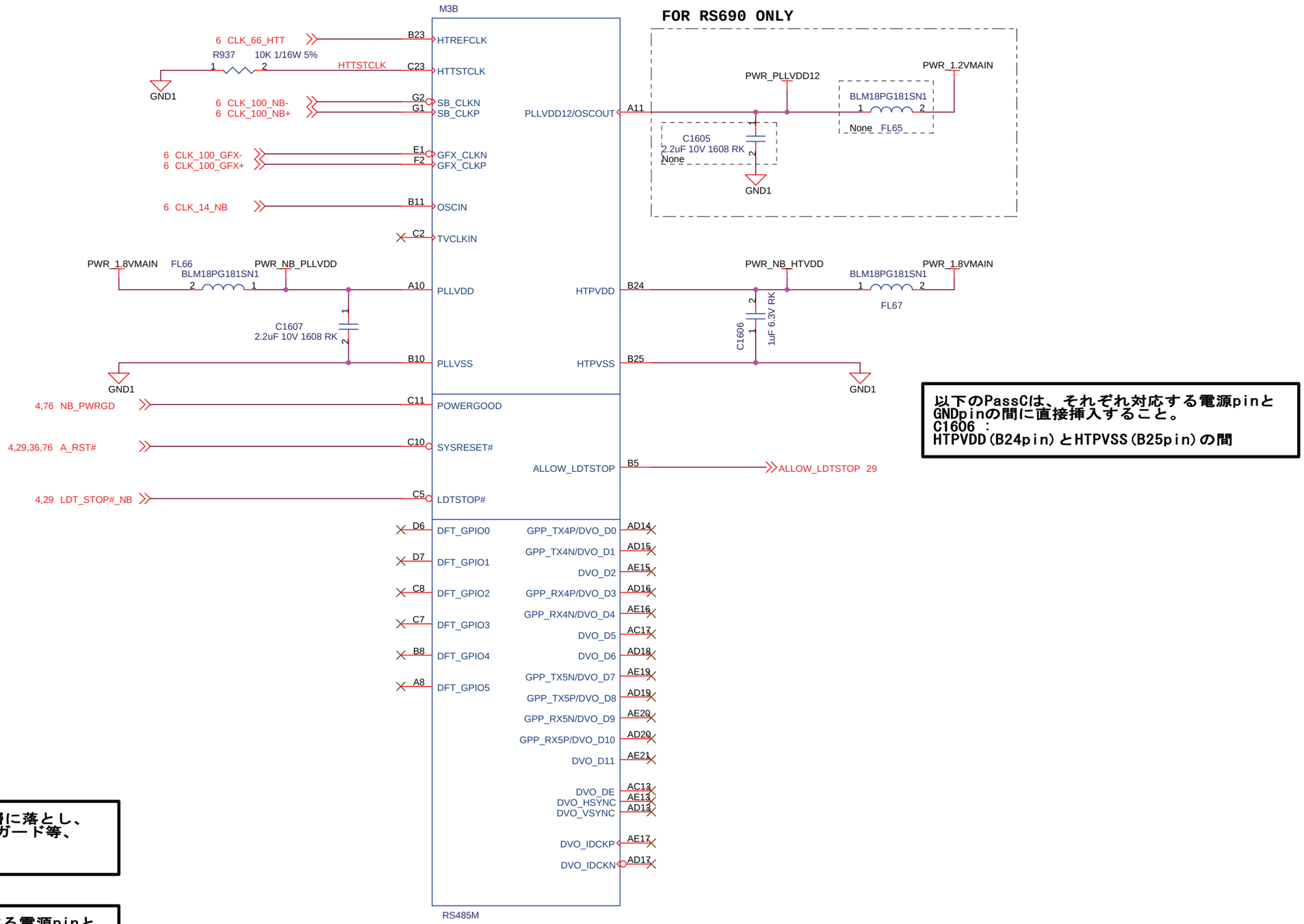

以下のPassCは、それぞれ対応する電源pinとGNDpinの間に直接挿入すること。
C1606 :
HTPVDD(B24pin)とHTPVSS(B25pin)の間

以下のpinのGND VIAは直接GND層に落とし、別のGND pinと共用したり、GNDガード等、他の用途には使用しないこと。
PLLVSS(B10pin)

以下のPassCは、それぞれ対応する電源pinとGNDpinの間に直接挿入すること。
C1607 :
PLLVDD(A10pin)とPLLVSS(B10pin)の間

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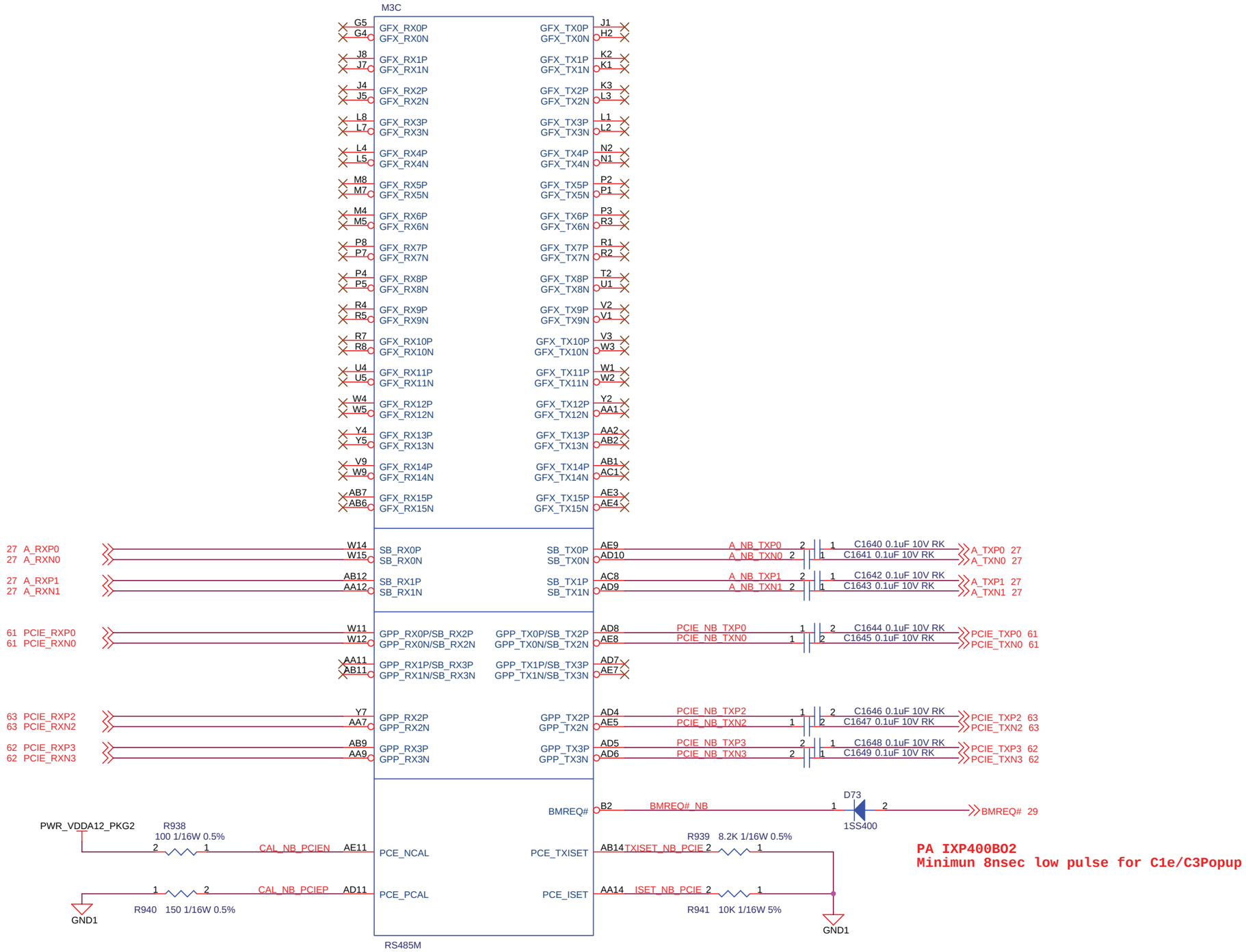
RS485-2

Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE: VB313AA
DRAW. No.: C1CP302570-X2
CAST:
FUJITSU LTD.
Sheet 16 / 93



PA IXP400B02
Minimun 8nsec low pulse for C1e/C3Popup

	RS485	RS690
R938	100ohm 0.5%	2Kohm 1%
R940	150ohm 1%	562ohm 1%

	RS485	RS690
R939	8.2Kohm 0.5%	None
R941	10Kohm 5%	1.47Kohm 5%

CAL_NB_PCIEN, CAL_NB_PCIEP
TXISET_NB_PCIE, ISET_NB_PCIE
は0.254mm以上の幅で配線し、
他の信号から0.254mm以上ギャップを保つこと。
R938, R939, R940, R941
は、M14から12.7mm以内に配置すること

RS485-3

Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE: **VB313AA**

DRAW. No.: C1CP302570-X2 CAST

FUJITSU LTD. Sheet 17 / 93

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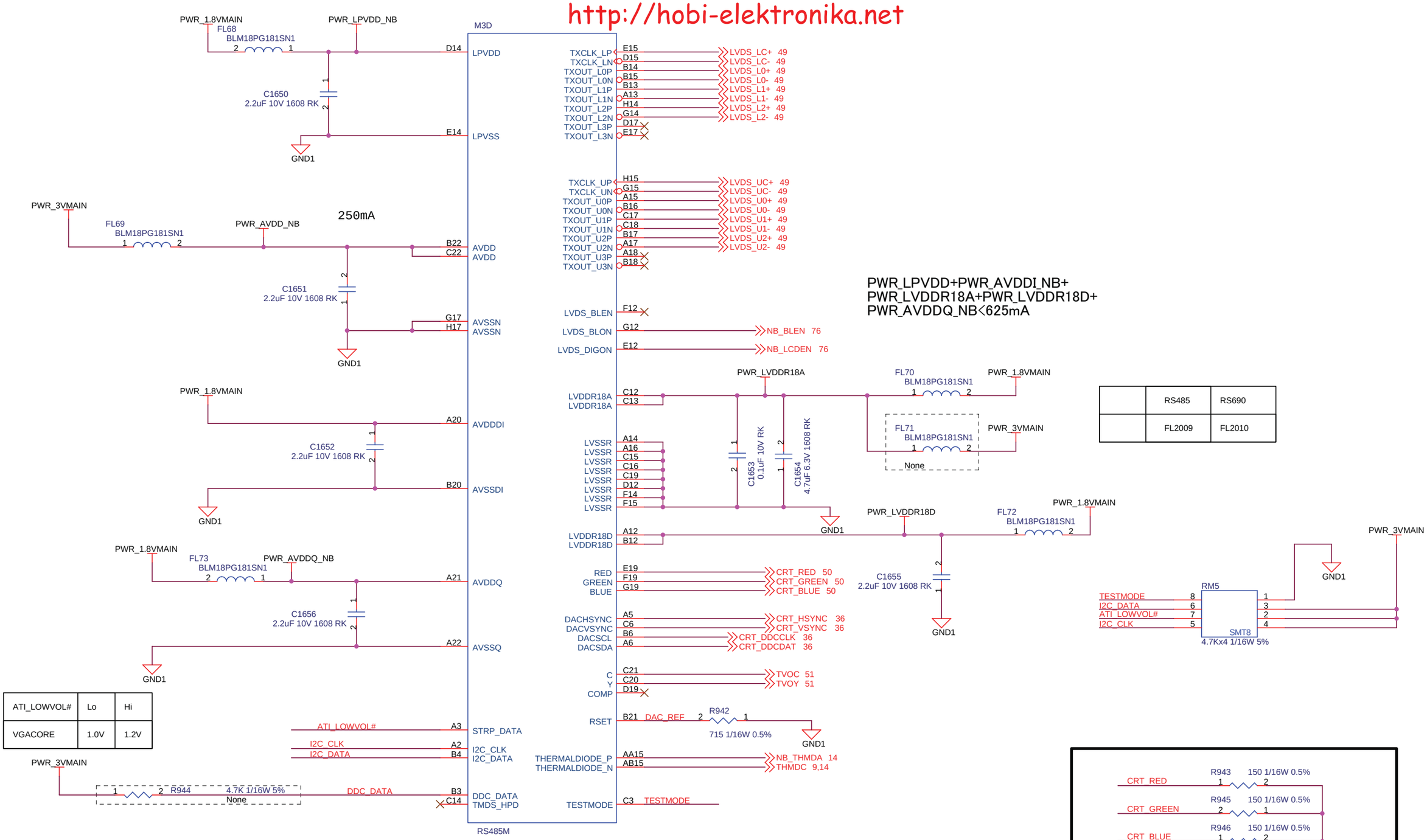

	RS485	RS690
	FL2009	FL2010

ATI_LOWVOL#	Lo	Hi
VGACORE	1.0V	1.2V

R943,R945,R946は、M3(RS485M)の直近に配置すること

以下のpinのGND VIAは直接GND層に落とし、
別のGND pinと共用したり、GNDガード等、
他の用途には使用しないこと。
LPVSS(E14pin)
LVSSR(A14,A16,C15,C16,C19,D12,F14,F15pin)
AVSSN(G17,H17pin)
AVSSDI(B20pin)
AVSSQ(A22pin)

以下のPassCは、それぞれ対応する電源pinと
GNDpinの間に直接挿入すること。
C1650　　：LPVDD(D14pin)とLPVSS(E14pin)の間
C1653, C1654　：LVDDR18A(C12,C13pin)と
　　LVSSR(A14,A16,C15,C16,C19,D12,F14,F15pin)の間
C1651　　：AVDD(B22,C22pin)とAVSSN(G17,H17pin)の間
C1652　　：AVDDI(A20pin)とAVSSDI(B20pin)の間
C1656　　：AVDDQ(A21pin)とAVSSQ(A22pin)の間

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RS485-4

Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE: VB313AA
DRAW. No.: C1CP302570-X2
CAST:
FUJITSU LTD.
Sheet: 18 / 93

Dolphin

PWR_1.2VMAIN

PWR_VGACORE

1.0~1.2V

5.0A

FL74 BLM18SG121TN1 CA53140-5172

FL75 BLM18SG121TN1 CA53140-5172

FL76 BLM18SG121TN1 CA53140-5172

C2075 220uF 2.5V(NEO/TPE) B21 CAT22-D0E2200M

C1657 22uF 6.3V 2012 RM

C1658 1uF 6.3V RK

C1659 1uF 6.3V RK

C1660 1uF 6.3V RK

C1661 1uF 6.3V RK

C1662 1uF 6.3V RK

C1663 1uF 6.3V RK

C1664 1uF 6.3V RK

GND1

M3E

VDD_CORE: A19, A4, A7, A9, B19, B9, C9, D20, D9, G20, H11, J11, J19, L11, L13, L15, L17, M12, M14, N11, N13, N15, P12, P14, P17, R11, R13, R15, U11, U12, U14, U15

0.5A

PWR_1.2VMAIN

VDD_HT: AA17, AB17, AB19, AC18, AC19, AC20, AD21, AD22, AD23, AD24, AE23, AE24, AE25, W17, Y17

C1665 1uF 6.3V RK

C1666 1uF 6.3V RK

C1667 1uF 6.3V RK

C1668 1uF 6.3V RK

GND1

2.25A

PWR_VDDA12

PWR_1.2VMAIN

FL77 BLM18PG181SN1

FL78 BLM18PG181SN1

VDDA12: B1, C1, D1, D2, D3, E2, E3, E6, F4, G7, L9, M9

C1670 1uF 6.3V RK

C1671 1uF 6.3V RK

C1672 1uF 6.3V RK

C1673 1uF 6.3V RK

C1669 220uF 2.5V(NEO/TPE) B21 CAT22-D0E2200M

GND1

PWR_VDDPLL

PWR_1.2VMAIN

VDDPLL/VDDA12: E7, F7

R947 0 1/16W 1608

C1674 4.7uF 6.3V 1608 RK

C1675 1uF 6.3V RK

VSSA: F9, G9

GND1

	RS485	RS690
R2051	0ohm	BLM18PG181SN1

PWR_1.8VMAIN

PWR_VDDDVO

FL79 BLM18PG181SN1

C1676 1uF 6.3V RK

C1677 1uF 6.3V RK

C1678 1uF 6.3V RK

GND1

VDD_DVO: AC12, AD12, AE12

750mA

PWR_VDDA18

PWR_1.8VMAIN

FL80 BLM18PG181SN1

PWR_1.2VMAIN

FL81 BLM18PG181SN1 None

VDDA18: AB3, AB4, AC3, AD2, AE1, AE2, U7, W7

C1680 1uF 6.3V RK

C1681 1uF 6.3V RK

C1682 1uF 6.3V RK

C1683 1uF 6.3V RK

C1684 1uF 6.3V RK

C1685 1uF 6.3V RK

C1679 100uF 6.3V (POSE) B20 CAT22-D0J1000M

GND1

	RS485	RS690
FL80	Mount	
FL81		Mount

PWR_VDDA12_PKG1

C1686 10uF 6.3V 2012 RM

GND1

PWR_VDDA12_PKG2

PWR_VDDA12_PKG1

PWR_VDDHT_PKG

D22 VDD_HT_PKG

M1 VDDA12_PKG1

AC11 VDDA12_PKG2

50mA

PWR_3VMAIN

PWR_VDDR3

FL83 BLM18PG181SN1

C1691 2.2uF 10V 1608 RK

GND1

D11 VDDR3

E11 VDDR3

RS485M

0.2A

PWR_VDD_18

PWR_1.8VMAIN

FL82 BLM18PG181SN1

VDD_18: J14, J15

C1687 1uF 6.3V RK

C1688 1uF 6.3V RK

C1689 1uF 6.3V RK

C1690 1uF 6.3V RK

GND1

RS485-5

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Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

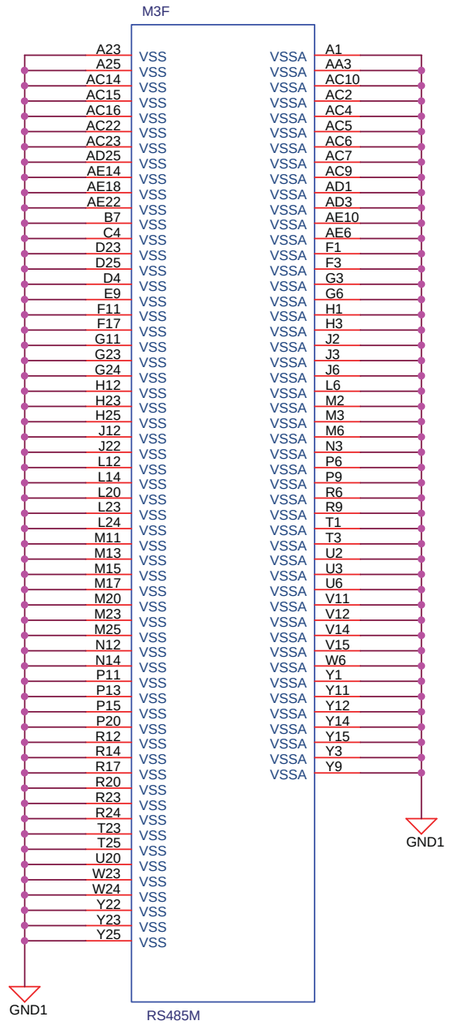
TITLE: VB313AA

DRAW. No.: C1CP302570-X2

CAST

FUJITSU LTD.

Sheet 19 / 93



RS485-6

						TITLE	VB313AA
						DRAW. No.	C1CP302570-X2 CAST
Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.	Sheet 20 / 93
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa		

Dolphin

Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE
VB313AA

DRAW. No.
C1CP302570-X2

CAST

FUJITSU LTD.

Sheet 21 / 93

Dolphin

Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

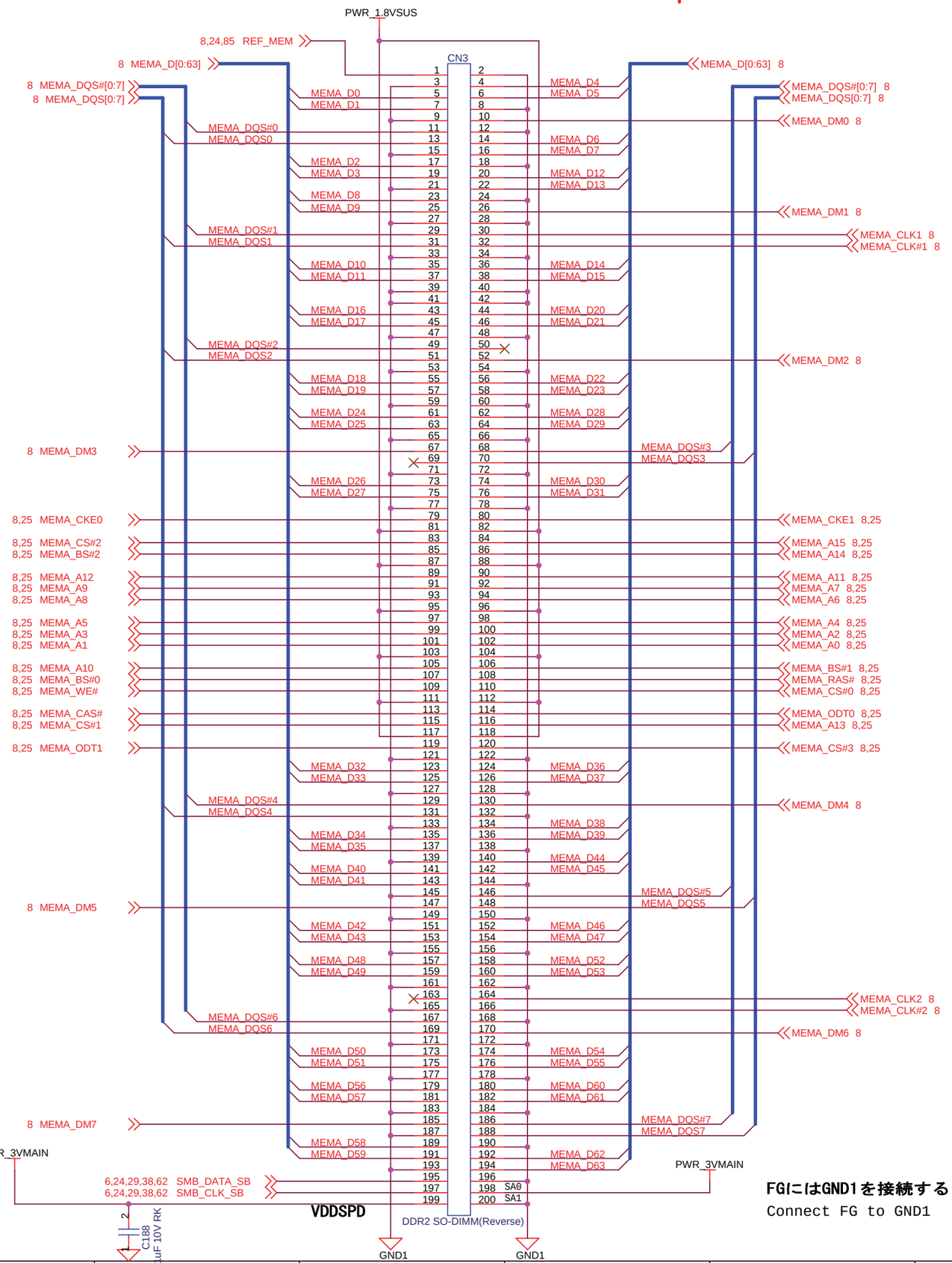
TITLE
VB313AA

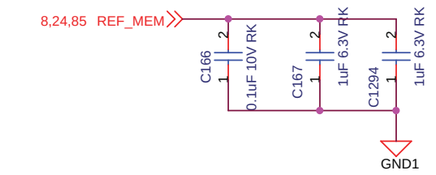
DRAW. No.
C1CP302570-X2

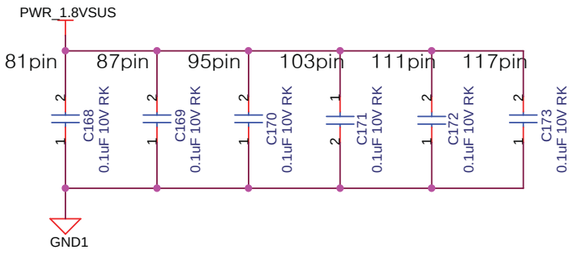
CAST

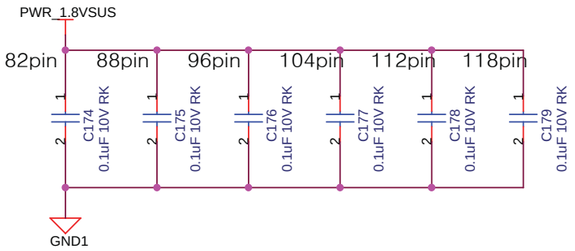
FUJITSU LTD.

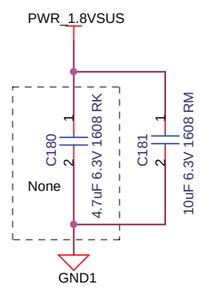
Sheet 22 / 93

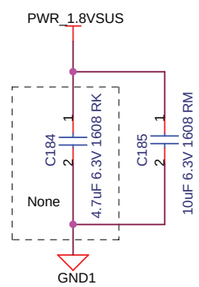












FGにはGND1を接続すること。
Connect FG to GND1

Memory Slot1

						TITLE	VB313AA	
						DRAW. No.	C1CP302570-X2	CAST
Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.		Sheet 23 / 93
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa			

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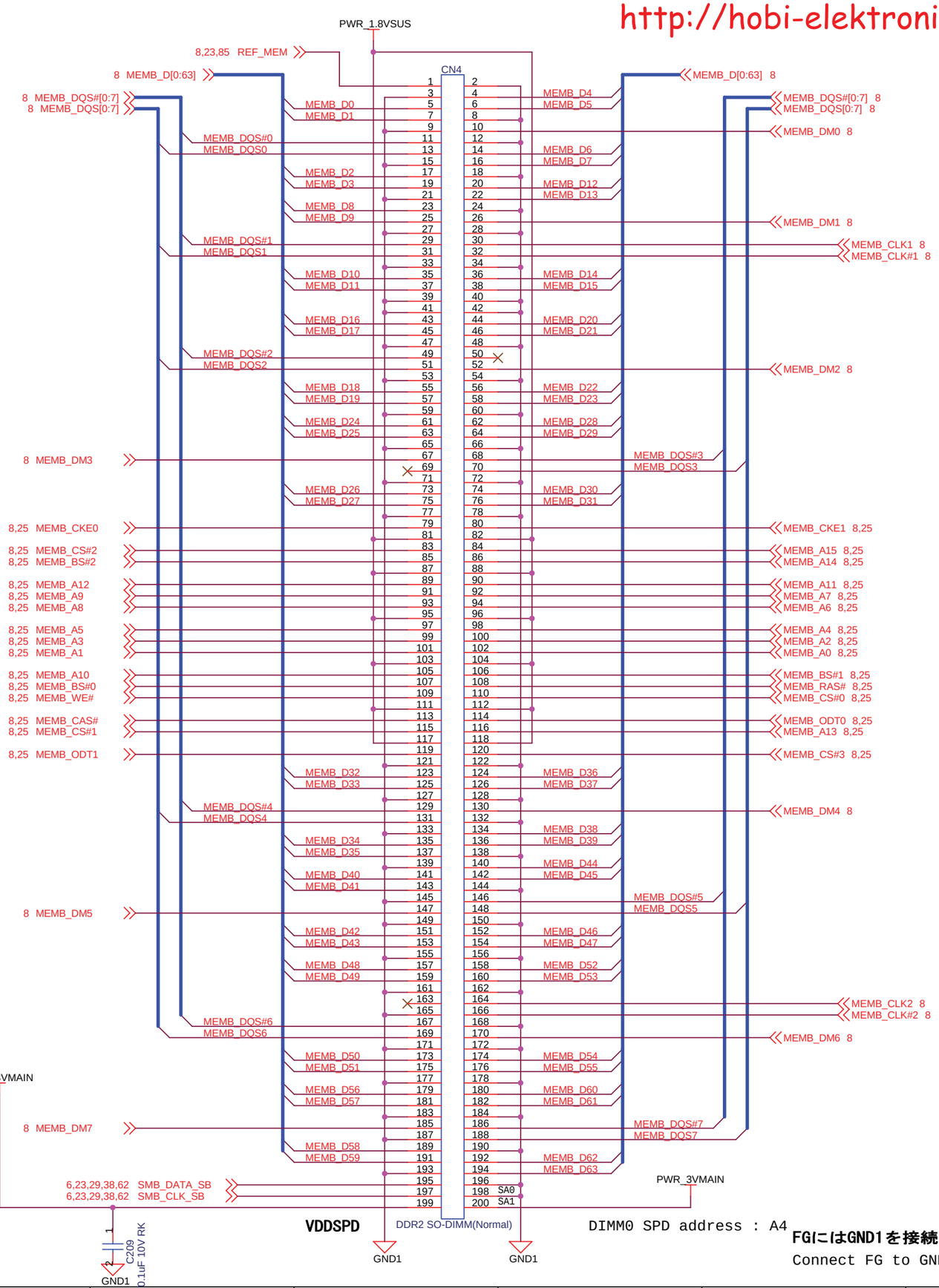
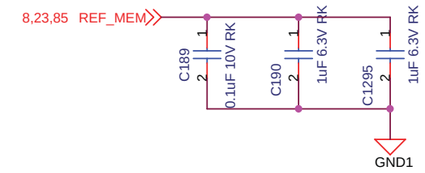
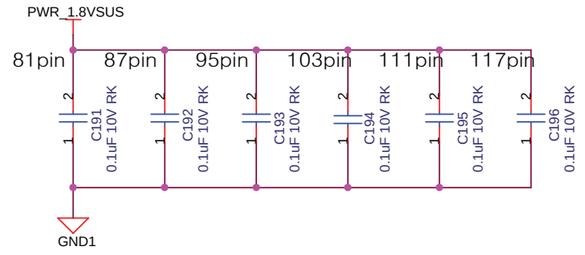
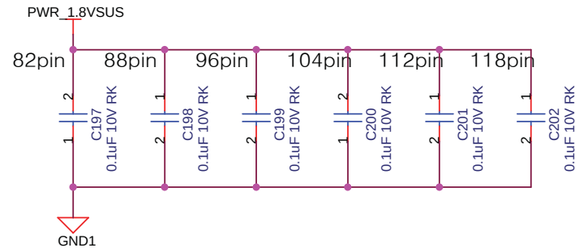


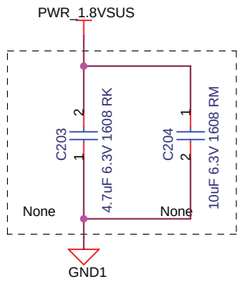
DIMM0 SPD address : A4

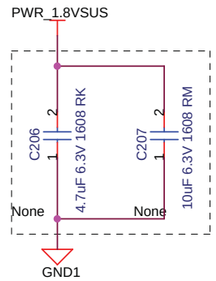
FGにはGND1を接続すること。
Connect FG to GND1











Memory Slot2

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							TITLE	VB313AA
							DRAW. No.	C1CP302570-X2
							CAST	
Rev.	Date	Design	Check	Appr.	Description		FUJITSU LTD.	Sheet 24 / 93
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	

本ページの集合抵抗内でピンスワップ可

8,23 MEMA_A[0:15]

MEMA_A0
MEMA_A1
MEMA_A2
MEMA_A3
MEMA_A4
MEMA_A5
MEMA_A6
MEMA_A7
MEMA_A8
MEMA_A9
MEMA_A10
MEMA_A11
MEMA_A12
MEMA_A13
MEMA_A14
MEMA_A15

8,24 MEMB_A[0:15]

MEMB_A0
MEMB_A1
MEMB_A2
MEMB_A3
MEMB_A4
MEMB_A5
MEMB_A6
MEMB_A7
MEMB_A8
MEMB_A9
MEMB_A10
MEMB_A11
MEMB_A12
MEMB_A13
MEMB_A14
MEMB_A15

PWR_DIMM_VTT
PWR_1.8VSUS

C1692 0.1uF 10V RK
C1693 0.1uF 10V RK
C1694 0.1uF 10V RK
C1695 0.1uF 10V RK
C1696 0.1uF 10V RK
C1697 0.1uF 10V RK
C1698 0.1uF 10V RK
C1699 0.1uF 10V RK
C1700 0.1uF 10V RK
C1701 0.1uF 10V RK
C1702 0.1uF 10V RK
C1703 0.1uF 10V RK
C1704 0.1uF 10V RK
C1705 0.1uF 10V RK
C1706 0.1uF 10V RK
C1707 0.1uF 10V RK
C1718 0.1uF 10V RK
C1719 0.1uF 10V RK
C1720 0.1uF 10V RK
C1721 0.1uF 10V RK
C1722 0.1uF 10V RK
C1723 0.1uF 10V RK
C1724 0.1uF 10V RK

GND1

RM101
MEMA_A8 MEMA_A9 MEMA_A15 MEMA_A4 MEMA_A11 MEMA_A3 MEMA_A5 MEMA_A6
47x8 1/16W 5% r
CAC39-Q1J47R0J

RM103
MEMA_A7 MEMA_A14 MEMA_A12
8,23 MEMA_CKE1
8,23 MEMA_BS#2
8,23 MEMA_CS#2
8,23 MEMA_CKE0
47x8 1/16W 5% r
CAC39-Q1J47R0J

RM105
MEMA_A1 MEMA_A2 MEMA_A0 MEMA_A10
8,23 MEMA_BS#1
8,23 MEMA_BS#0
8,23 MEMA_RAS#
8,23 MEMA_CS#0
47x8 1/16W 5% r
CAC39-Q1J47R0J

RM107
8,23 MEMA_ODT0
8,23 MEMA_CS#3
MEMA_A13
8,23 MEMA_WE#
8,23 MEMA_CAS#
8,23 MEMA_CS#1
8,23 MEMA_ODT1
47x8 1/16W 5% r
CAC39-Q1J47R0J

PWR_DIMM_VTT
PWR_1.8VSUS

C212 0.1uF 10V RK
C213 0.1uF 10V RK
C214 0.1uF 10V RK
C215 0.1uF 10V RK

PWR_DIMM_VTT

C210 10uF 6.3V 1608 RM
C211 10uF 6.3V 1608 RM
C1292 10uF 6.3V 1608 RM
C1293 10uF 6.3V 1608 RM

GND1

PWR_DIMM_VTT
PWR_1.8VSUS

C1708 0.1uF 10V RK
C1709 0.1uF 10V RK
C1714 None 0.1uF 10V RK
C1715 0.1uF 10V RK

PWR_1.8VSUS

C2088 None 22uF 6.3V 2012 RM
C2089 None 22uF 6.3V 2012 RM

GND1

PWR_DIMM_VTT

C2086 None 22uF 6.3V 2012 RM
C2087 None 22uF 6.3V 2012 RM
C1710 10uF 6.3V 1608 RM
C1711 10uF 6.3V 1608 RM
C1712 None 10uF 6.3V 1608 RM
C1713 None 10uF 6.3V 1608 RM

GND1

PWR_DIMM_VTT

CM25 0.1uFx4 16V RM
CM26 0.1uFx4 16V RM None
CM27 0.1uFx4 16V RM
CM28 0.1uFx4 16V RM None
CM29 0.1uFx4 16V RM

RM102
MEMB_A10 MEMB_A13
8,24 MEMB_CAS#
8,24 MEMB_CS#3
8,24 MEMB_CS#0
8,24 MEMB_BS#0
47x8 1/16W 5% r
CAC39-Q1J47R0J

RM123
8,24 MEMB_CS#2
8,24 MEMB_CKE1
MEMB_A15
8,24 MEMB_BS#2
SMT8
47x4 1/16W 5%

RM124
8,24 MEMB_CKE0
MEMB_A8 MEMB_A12 MEMB_A14
SMT8
47x4 1/16W 5%

RM125
MEMB_A1 MEMB_A5
8,24 MEMB_BS#1
8,24 MEMB_RAS#
SMT8
47x4 1/16W 5%

RM126
8,24 MEMB_CS#1
8,24 MEMB_ODT0
8,24 MEMB_WE#
8,24 MEMB_ODT1
SMT8
47x4 1/16W 5%

RM108
MEMB_A2 MEMB_A0 MEMB_A6 MEMB_A4 MEMB_A3 MEMB_A11 MEMB_A7 MEMB_A9
47x8 1/16W 5% r
CAC39-Q1J47R0J

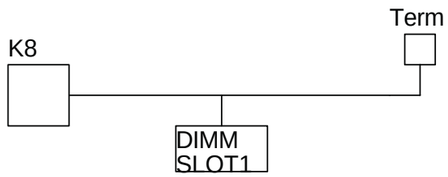
GND1

Memory Termination

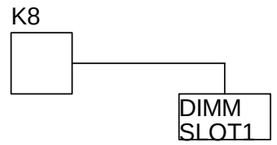
						TITLE	VB313AA
						DRAW. No.	C1CP302570-X2
							CAST
Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.	Sheet 25 / 93
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa		

Channel A

DIMM Address/Command Topology

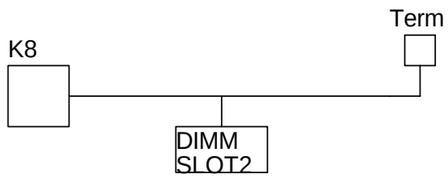


DIMM Data Bus Topology

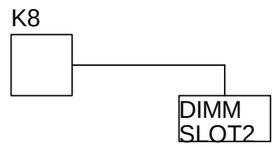


Channel B

DIMM Address/Command Topology



DIMM Data Bus Topology



Topology

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Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE: **VB313AA**

DRAW. No.: C1CP302570-X2 CAST

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Sheet 26 / 93

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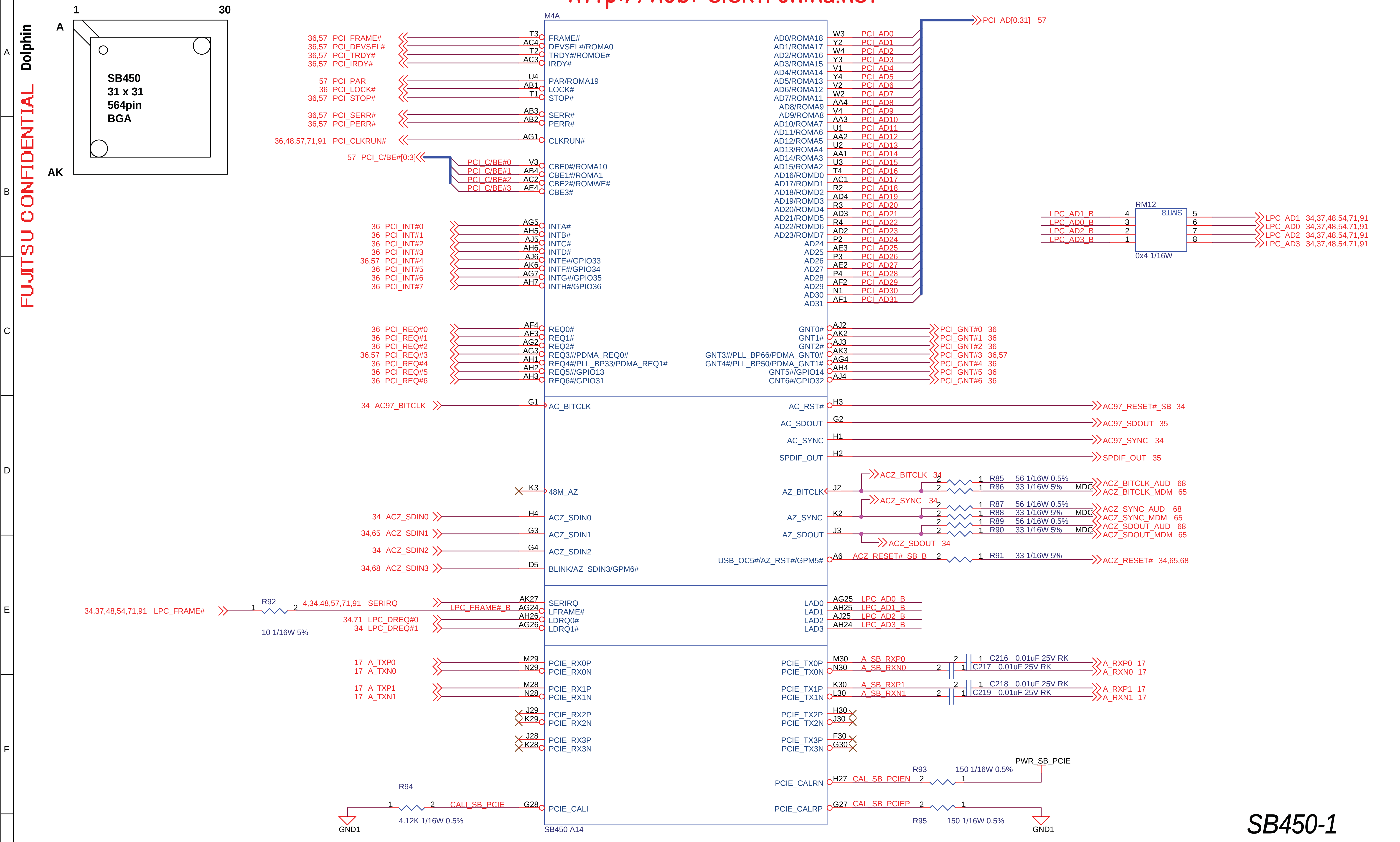

SB450-1

R94はG28pinから12.7mm以内に配置すること。
R93はH27pinから12.7mm以内に配置すること。
R95はG27pinから12.7mm以内に配置すること。

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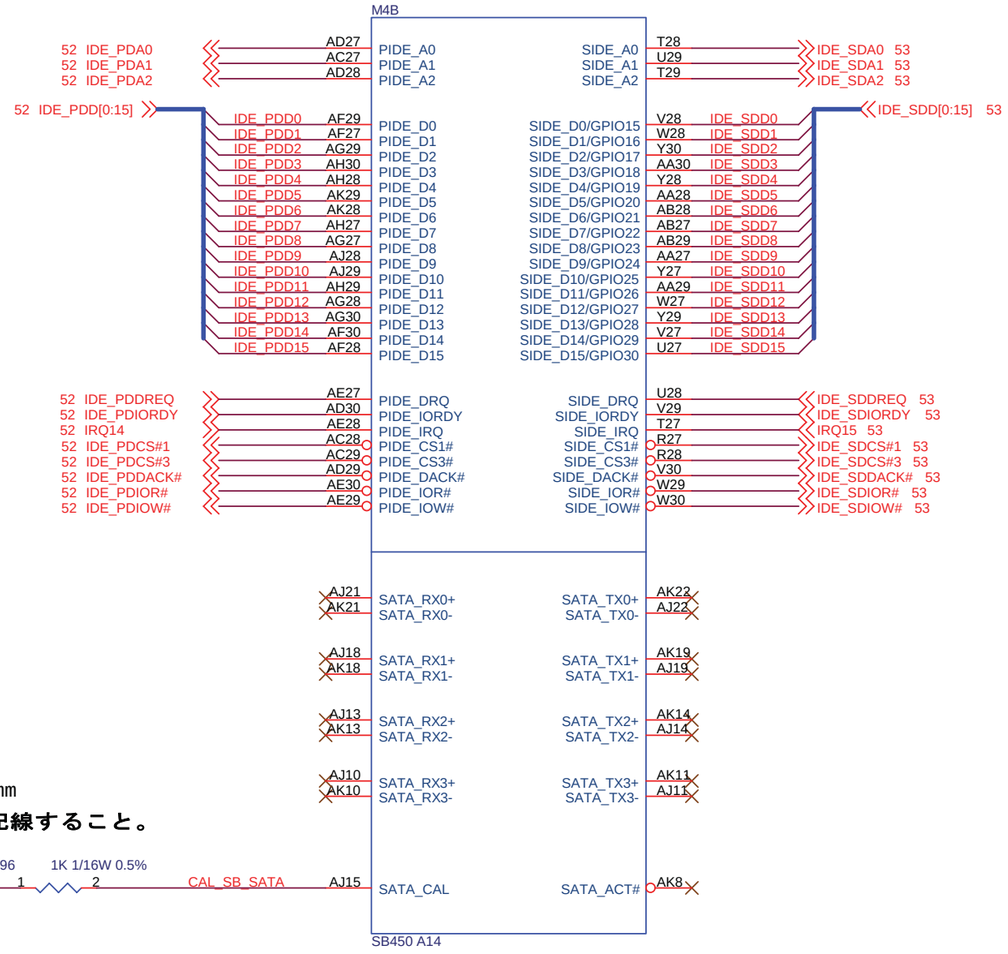
TITLE	VB313AA
DRAW. No.	C1CP302570-X2
CAST	
Design	06/07/04 Mizukami
Check	Urita
Appr.	Hasegawa
FUJITSU LTD.	Sheet 27 / 93



Route CAL_SB_SATA within 12.7mm

CAL_SB_SATAは、12.7mm以内で配線すること。

SB450-2

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Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE: **VB313AA**

DRAW. No.: C1CP302570-X2 CAST

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Sheet 28 / 93

M4C

4,34,75 BSRBTN# B3 PWR_BTN#
35 AUTO_ON# F3 RTC_IRQ#/ACPWR_STRAP
4,34,54 RIOUT# D3 RI#/EXTEVENT0#
34 EXTEVENT1# A25 LPC_SMI#/EXTEVENT1#
4,9,34 SB_THERMTRIP# D6 SMBALERT#/THRMTRIP#/GEVENT2#
4,34,90 SB_SMBALT# C5 LPC_PME#/GEVENT3#
4,54,55 PMEOUT# C4 PCI_PME#/GEVENT4#
4,34 S3_STATE D8 S3_STATE/GEVENT5#
4,34,61,63 PCIE_WAKE# D2 WAKE#/GEVENT8#
34 SYS_RST# D7 SYS_RESET#/GPM7#

4,34,54 EXTSMI# B8 USB_OC0#/GPM0#
4,34,54 EXTSCI# C8 USB_OC1#/GPM1#
4,55 PLLB# C7 USB_OC2#/FANOUT1/LLB#/GPM2#
4,34,69 SB_LCDCL# B7 USB_OC3#/GPM3#
4,34,91 KBC_SCI B6 USB_OC4#/GPM4#

34 GEVENT6# B5 USB_OC6#/GEVENT6#
58,61 CPPE# A5 USB_OC7#/GEVENT7#

LDT_PG/SSMUXSEL/GPIO0 D25 LDT_PWRGD 9
ROM_CS#/GPIO1 B25 NEWCARD_CLKEN# 34
SPKR/GPIO2 C24 SB_SPKR 54
FANOUT0/GPIO3 A27 NEWCARD_RST# 34,58
GPIO4 D24 AGP_STP# 34
GPIO5 D23 AGP_BUSY# 34
GHI#/GPIO6 C25 SB_GPIO6 34
VGATE/GPIO7 C23 VRM_PWRGD 34
DDC1_SDA/GPIO8 C26 SB_GPIO8 34,38
DDC1_SCL/GPIO9 B27 SB_GPIO9 34
TALERT#/TEMP_ALERT#/GPIO10 C6 THLTL#_SB 34
DDC2_SCL/GPIO11 C27 SB_GPIO11 34
DDC2_SDA/GPIO12 D26 SB_GPIO12 34

SCL0/GPOC0# A26 SMB_CLK_SB 6,23,24,38,62
SDA0/GPOC1# B26 SMB_DATA_SB 6,23,24,38,62

PWR_3VMAIN
R948
10K 1/16W 5%
17 BMREQ#
C1716
15pF 25V AJ
GND1

PA IXP400BO2 Minimun 8nsec low pulse

IGNNE# B30
FERR# E28
BMREQ# D27
4,91 KBC_A20G GA20IN AJ26

INTR/LINT0 A28
NMI/LINT1 C28
INIT# B29
SMI# D29
A20M# F28
STPCLK#/ALLOW_LDTSTP E29 ALLOW_LDTSTOP 16
DPSLP_OD#/GPIO37 AK7
SLP#/LDT_STP# E4 LDT_STOP# 9
CPU_STP#/DPSLP_3V# AJ8
DPRSLPVR E27

4 SB_RSMRST#
SB_RSMRST#_B R489 10 1/16W 5%
4 SB_PWROK_3VMAIN
PWROK_3VMAIN_B R850 10 1/16W 5%
4,91 KBC_INIT# AJ27

RSMRST# D1
PWR_GOOD C3
KBRST#

SLP_S5# E3 SLP_S5# 34,74
SLP_S3# B4 SLP_S3# 34,74
CPU_PG C29
LDT_RST# D28 LDT_RST# 9
A_RST# AH8 A_RST# 4,16,36,76
PCIRST# AJ7 PCI_RST# 4,54,55,57,72
SUS_STAT# D4

COMP_SB_USBは、12.7mm以内で配線すること。

R97 11.8K 1/16W 0.5%
COMP_SB_USB C15
GND1

USB_RCOMP
USB_ATEST0 D15
USB_ATEST1 C16
USB_VREFOUT D16

34 SB_TEST0 E2 TEST0
34 SB_TEST1 F2 TEST1

USB_HSDP0+ A20 USB_P0+ 66
USB_HSDM0- B20 USB_P0- 66
USB_HSDP1+ A21 USB_P1+ 56
USB_HSDM1- B21 USB_P1- 56
USB_HSDP2+ A17 USB_P2+ 66
USB_HSDM2- B17 USB_P2- 66
USB_HSDP3+ A18 USB_P3+ 61
USB_HSDM3- B18 USB_P3- 61
USB_HSDP4+ A13 USB_P4+ 66
USB_HSDM4- B13 USB_P4- 66
USB_HSDP5+ A14 USB_P5+ 66
USB_HSDM5- B14 USB_P5- 66
USB_HSDP6+ A10 USB_P6+ 66
USB_HSDM6- B10 USB_P6- 66
USB_HSDP7+ A11 USB_P7+ 56
USB_HSDM7- B11 USB_P7- 56

SB450 A14

PWR_PMU
M5
TC7SZ32AFE
54,74,75 RSMRST#
SB_RSMRST#_B
C228 0.1uF 10V RK
GND1

PWR_3VSTD
M125
NL17SZ08XV5
4,9,48,54,71,73,74 PWROK_3VMAIN
9 LDT_STOP#
LDT_STOP#_C
R949 10 1/16W 5%
LDT_STOP#_NB 4,15
C1717 0.1uF 10V RK
GND1

PWR_3VMAIN
RM109
8.1WS
LDT_RST#
LDT_PWRGD
LDT_STOP#
330x4 1/16W 5%

PWR_3VSTD
M82
TC7SZ32AFE
4,9,48,54,71,73,74 PWROK_3VMAIN
PWROK_3VMAIN_B
C1486 0.1uF 10V RK
GND1

SB450-3

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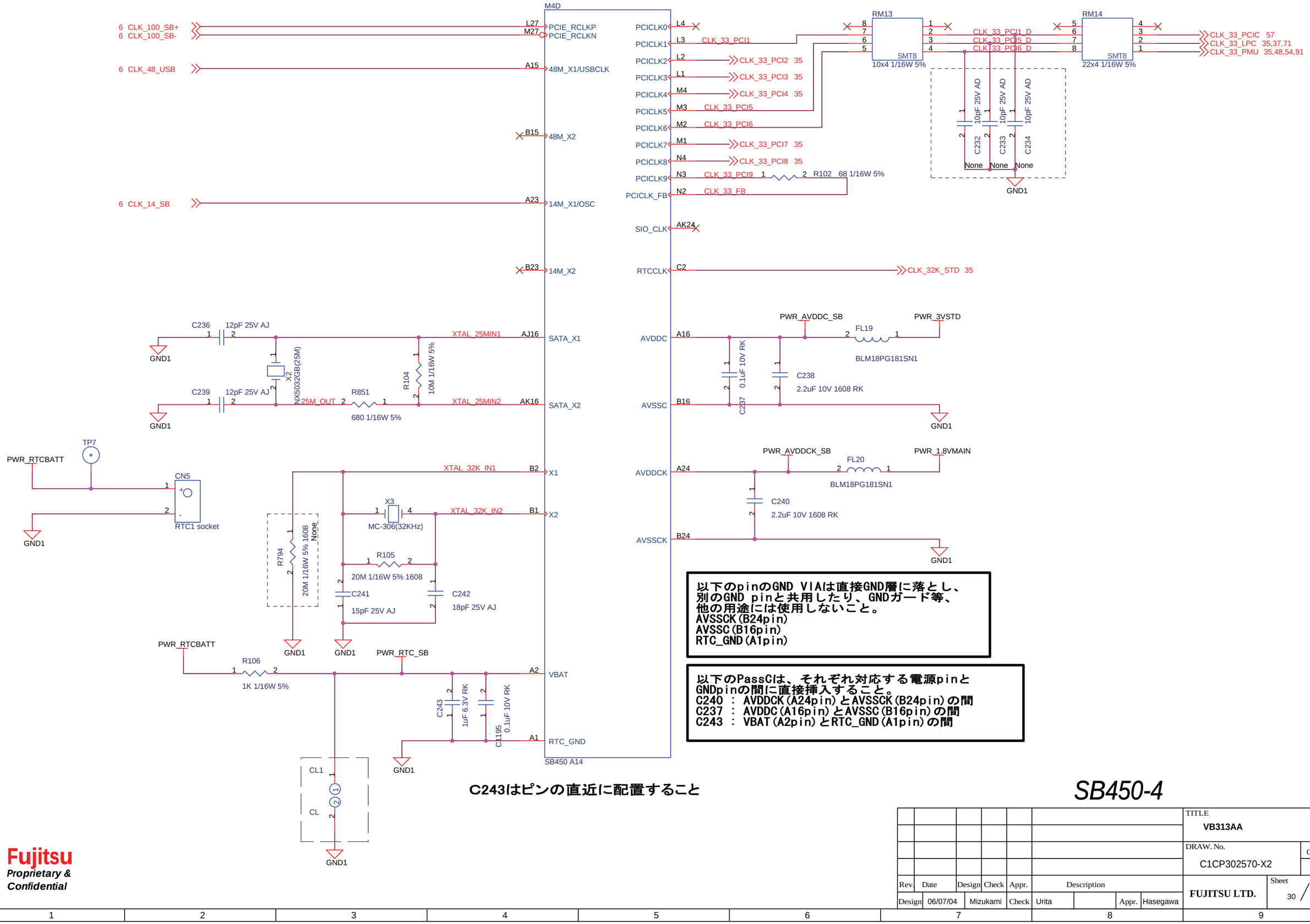
Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE: **VB313AA**
DRAW. No.: C1CP302570-X2
CAST:
FUJITSU LTD.
Sheet 29 / 93

Dolphin



以下のpinのGND VIAは直接GND層に落とし、
別のGND pinと共用したり、GNDガード等、
他の用途には使用しないこと。
AVSSCK(B24pin)
AVSSC(B16pin)
RTC_GND(A1pin)

以下のPassCは、それぞれ対応する電源pinと
GNDpinの間に直接挿入すること。
C240 : AVDDCK(A24pin)とAVSSCK(B24pin)の間
C237 : AVDDC(A16pin)とAVSSC(B16pin)の間
C243 : VBAT(A2pin)とRTC_GND(A1pin)の間

C243はピンの直近に配置すること

SB450-4

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						TITLE	VB313AA
						DRAW. No.	C1CP302570-X2
						CAST	
Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.	Sheet 30 / 93
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa		

VDD+AVDD_CK = MAX 1415mA

PWR_1.8VMAIN

M4E

M12 VDD_1
M13 VDD_2
M18 VDD_3
M19 VDD_4
N12 VDD_5
N13 VDD_6
N18 VDD_7
N19 VDD_8
V12 VDD_9
V13 VDD_10
V18 VDD_11
V19 VDD_12
W12 VDD_13
W13 VDD_14
W18 VDD_15
W19 VDD_16

VDDQ = MAX 300.3mA

PWR_3VMAIN

VDDQ1 A30
VDDQ2 D30
VDDQ3 E24
VDDQ4 E25
VDDQ5 J5
VDDQ6 K1
VDDQ7 K5
VDDQ8 N5
VDDQ9 P5
VDDQ10 R1
VDDQ11 U5
VDDQ12 U26
VDDQ13 U30
VDDQ14 V5
VDDQ15 V26
VDDQ16 Y1
VDDQ17 Y26
VDDQ18 AA5
VDDQ19 AA26
VDDQ20 AB5
VDDQ21 AC30
VDDQ22 AD5
VDDQ23 AD26
VDDQ24 AE1
VDDQ25 AE5
VDDQ26 AE26
VDDQ27 AF6
VDDQ28 AF7
VDDQ29 AF24
VDDQ30 AF25
VDDQ31 AK1
VDDQ32 AK4
VDDQ33 AK26
VDDQ34 AK30

PCIE_VDDR+PCIE_PVDD = MAX 300mA

PWR_1.8VMAIN — FL21 (2–1) — PWR_SB_PCIE
BLM18SG121TN1
CA53140-5172

F26 PCIE_VDDR_1
R29 PCIE_VDDR_2
G26 PCIE_VDDR_3
P26 PCIE_VDDR_4
K26 PCIE_VDDR_5
L26 PCIE_VDDR_6
P28 PCIE_VDDR_7
N26 PCIE_VDDR_8
P27 PCIE_VDDR_9

S5_3.3V = MAX 36.1mA

PWR_3VSTD

A3 S5_3.3V_1
A7 S5_3.3V_2
E6 S5_3.3V_3
E7 S5_3.3V_4
E1 S5_3.3V_5
F5 S5_3.3V_6

AVDD_SATA_1 AG10
AVDD_SATA_2 AG14
AVDD_SATA_3 AH12
AVDD_SATA_4 AG12
AVDD_SATA_5 AG18
AVDD_SATA_6 AG21
AVDD_SATA_7 AH18
AVDD_SATA_8 AG20

PWR_SB_SATA — FL22 (1–2) — PWR_1.8VMAIN
BLM18SG121TN1
CA53140-5172

S5_1.8V + USB_PHY_1.8 = MAX 300mA

PWR_1.8VSTD

E9 S5_1.8V_1
E10 S5_1.8V_2
E20 S5_1.8V_3
E21 S5_1.8V_4

PWR_SB_AVDD — FL23 (2–1) — PWR_3VSTD
BLM18PG181SN1

AVDDRX_0 D20
AVDDRX_1 D17
AVDDRX_2 C14
AVDDRX_3 C11

PWR_1.8VSTD — FL24 (1–2) — PWR_SB_USB_PHY
BLM18PG181SN1

E13 USB_PHY_1.8V_1
E14 USB_PHY_1.8V_2
E16 USB_PHY_1.8V_3
E17 USB_PHY_1.8V_4

AVDDTX_0 C21
AVDDTX_1 C18
AVDDTX_2 D13
AVDDTX_3 D10

PWR_1.8VMAIN — FL26 (1–2) — PWR_SB_SATAXTL
BLM18PG181SN1

AH16 XTLVDD_SATA

PWR_SB_PCIEPVDD — FL25 (1–2) — PWR_1.8VMAIN
BLM18PG181SN1

PCIE_PVDD R30

PWR_1.8VMAIN — FL27 (1–2) — PWR_SB_SATAPLL
BLM18PG181SN1

AH15 PLLVDD_SATA

CPU_PWR = MAX 4.5mA

PWR_1.2VMAIN

CPU_PWR C30

PWR_5VMAIN
C244 0.1uF 10V RK
C245 1uF 6.3V RK
GND1

V5_VREF AG6

V5_VREF = MAX 0.35mA

SB450 A14

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SB450-5

Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE: VB313AA
DRAW. No.: C1CP302570-X2
CAST
FUJITSU LTD.
Sheet 31 / 93

FUJITSU CONFIDENTIAL Dolphin

M4F

A4	VSS_1	PCIE_VSS_1	H28
A8	VSS_2	PCIE_VSS_2	F29
A29	VSS_3	PCIE_VSS_3	H29
B28	VSS_4	PCIE_VSS_4	H26
C1	VSS_5	PCIE_VSS_5	F27
E5	VSS_6	PCIE_VSS_6	G29
E8	VSS_7	PCIE_VSS_7	L29
E11	VSS_8	PCIE_VSS_8	J26
E12	VSS_9	PCIE_VSS_9	L28
E15	VSS_10	PCIE_VSS_10	J27
E18	VSS_11	PCIE_VSS_11	N27
E19	VSS_12	PCIE_VSS_12	M26
E22	VSS_13	PCIE_VSS_13	K27
E23	VSS_14	PCIE_VSS_14	P29
E26	VSS_15	PCIE_VSS_15	P30
E30	VSS_16		
F1	VSS_17		
F4	VSS_18		
G5	VSS_19	AVSS_USB_1	A9
H5	VSS_20	AVSS_USB_2	A12
J1	VSS_21	AVSS_USB_3	A19
J4	VSS_22	AVSS_USB_4	A22
K4	VSS_23	AVSS_USB_5	B9
L5	VSS_24	AVSS_USB_6	B12
M5	VSS_25	AVSS_USB_7	B19
P1	VSS_26	AVSS_USB_8	B22
R5	VSS_27	AVSS_USB_9	C9
R26	VSS_28	AVSS_USB_10	C10
T5	VSS_29	AVSS_USB_11	C12
T26	VSS_30	AVSS_USB_12	C13
T30	VSS_31	AVSS_USB_13	C17
W1	VSS_32	AVSS_USB_14	C19
W5	VSS_33	AVSS_USB_15	C20
W26	VSS_34	AVSS_USB_16	C22
Y5	VSS_35	AVSS_USB_17	D9
AB26	VSS_36	AVSS_USB_18	D11
AB30	VSS_37	AVSS_USB_19	D12
AC5	VSS_38	AVSS_USB_20	D14
AC26	VSS_39	AVSS_USB_21	D18
AD1	VSS_40	AVSS_USB_22	D19
AF5	VSS_41	AVSS_USB_23	D21
AF8	VSS_42	AVSS_USB_24	D22
AF23	VSS_43		
AF26	VSS_44		
AG8	VSS_45		
AJ1	VSS_46		
AJ24	VSS_47		
AJ30	VSS_48	AVSS_SATA_1	AG9
AK5	VSS_49	AVSS_SATA_2	AF10
AK25	VSS_50	AVSS_SATA_3	AF11
M14	VSS_51	AVSS_SATA_4	AF12
M15	VSS_52	AVSS_SATA_5	AF13
M16	VSS_53	AVSS_SATA_6	AF14
M17	VSS_54	AVSS_SATA_7	AF15
N14	VSS_55	AVSS_SATA_8	AF16
N15	VSS_56	AVSS_SATA_9	AF17
N16	VSS_57	AVSS_SATA_10	AF18
N17	VSS_58	AVSS_SATA_11	AF19
P12	VSS_59	AVSS_SATA_12	AF20
P13	VSS_60	AVSS_SATA_13	AF21
P14	VSS_61	AVSS_SATA_14	AF22
P15	VSS_62	AVSS_SATA_15	AH9
P16	VSS_63	AVSS_SATA_16	AG11
P17	VSS_64	AVSS_SATA_17	AG15
P18	VSS_65	AVSS_SATA_18	AG17
P19	VSS_66	AVSS_SATA_19	AG19
R12	VSS_67	AVSS_SATA_20	AG22
R13	VSS_68	AVSS_SATA_21	AG23
R14	VSS_69	AVSS_SATA_22	AF9
R15	VSS_70	AVSS_SATA23	AH17
R16	VSS_71	AVSS_SATA24	AH23
R17	VSS_72	AVSS_SATA25	AH13
R18	VSS_73	AVSS_SATA26	AH20
R19	VSS_74	AVSS_SATA27	AK9
T12	VSS_75	AVSS_SATA28	AJ12
T13	VSS_76	AVSS_SATA29	AK17
T14	VSS_77	AVSS_SATA30	AK23
T15	VSS_78	AVSS_SATA31	AH10
T16	VSS_79	AVSS_SATA32	AJ23
T17	VSS_80	AVSS_SATA33	AG13
T18	VSS_81	AVSS_SATA34	AH22
T19	VSS_82	AVSS_SATA35	AK12
U12	VSS_83	AVSS_SATA36	AH11
U13	VSS_84	AVSS_SATA37	AJ17
U14	VSS_85	AVSS_SATA38	AH14
U15	VSS_86	AVSS_SATA39	AH19
U16	VSS_87	AVSS_SATA40	AJ20
U17	VSS_88	AVSS_SATA41	AH21
U18	VSS_89	AVSS_SATA42	AJ9
U19	VSS_90	AVSS_SATA43	AG16
V14	VSS_91	AVSS_SATA44	AK15
V15	VSS_92	AVSS_SATA45	AK20
V16	VSS_93		
V17	VSS_94		
W14	VSS_95		
W15	VSS_96		
W16	VSS_97		
W17	VSS_98		

GND1

SB450 A14

GND1

SB450-6

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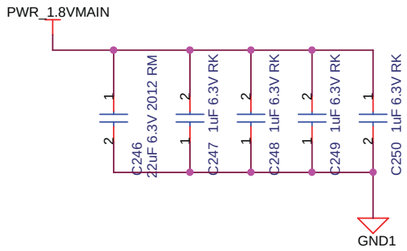
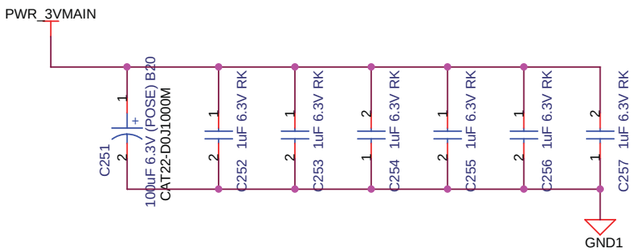
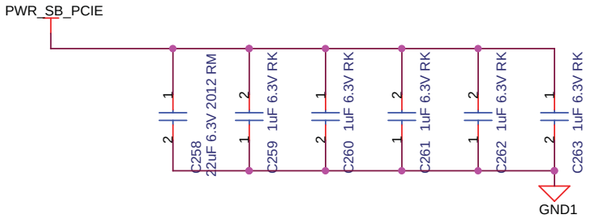
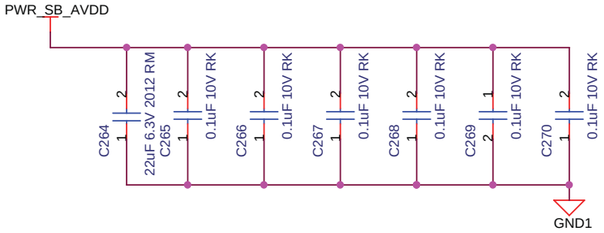
						TITLE	VB313AA	
						DRAW. No.	C1CP302570-X2	CAST
Rev.	Date	Design	Check	Appr.	Description			
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	FUJITSU LTD.
						Sheet	32 / 93	

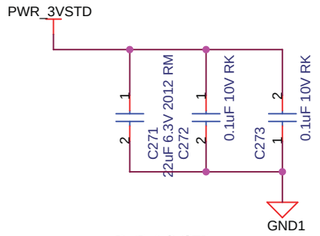
Dolphin

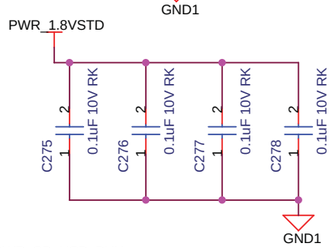


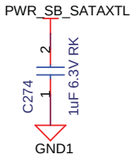


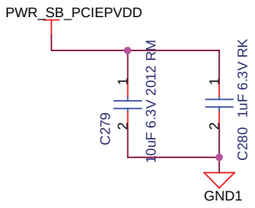


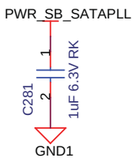


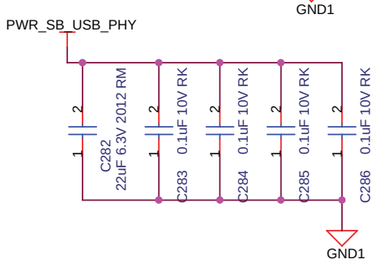


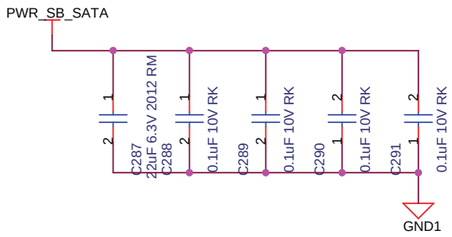












これらのパスコンはSB450近傍、可能な限りピンの直近に配置願います

SB450-7

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Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE: **VB313AA**

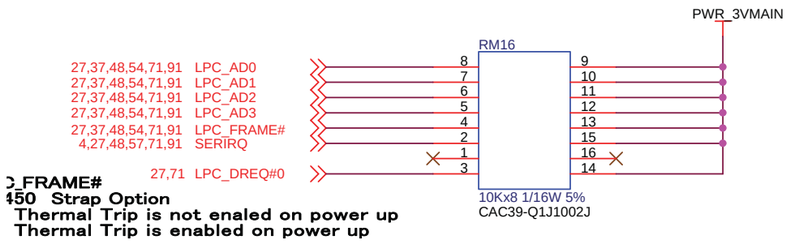
DRAW. No.: C1CP302570-X2

CAST

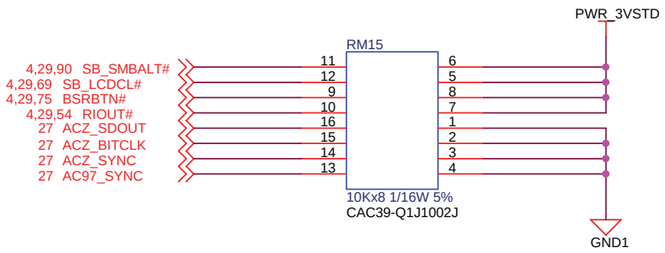
FUJITSU LTD.

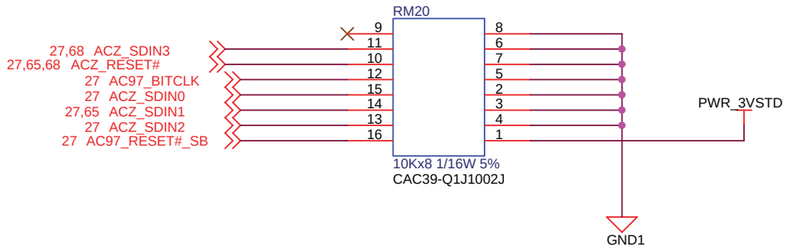
Sheet 33 / 93

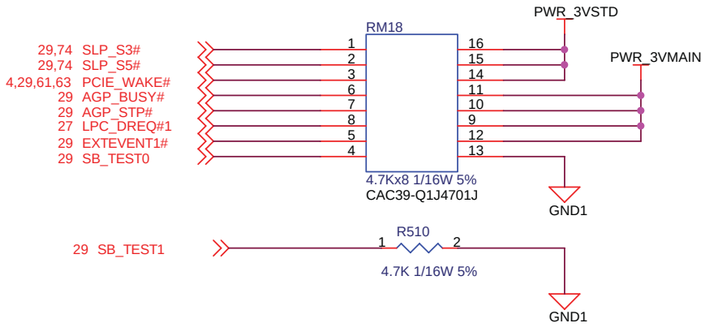
Dolphin

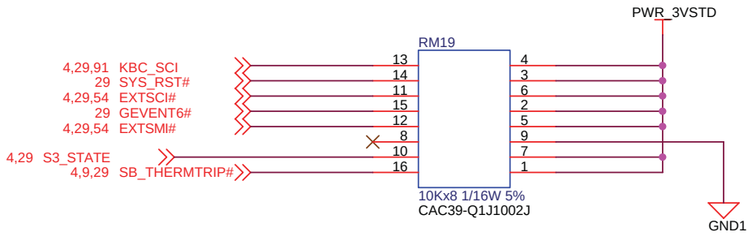


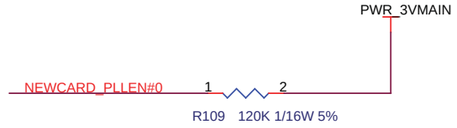
C_FRAME#
450 Strap Option
Thermal Trip is not enaled on power up
Thermal Trip is enabled on power up

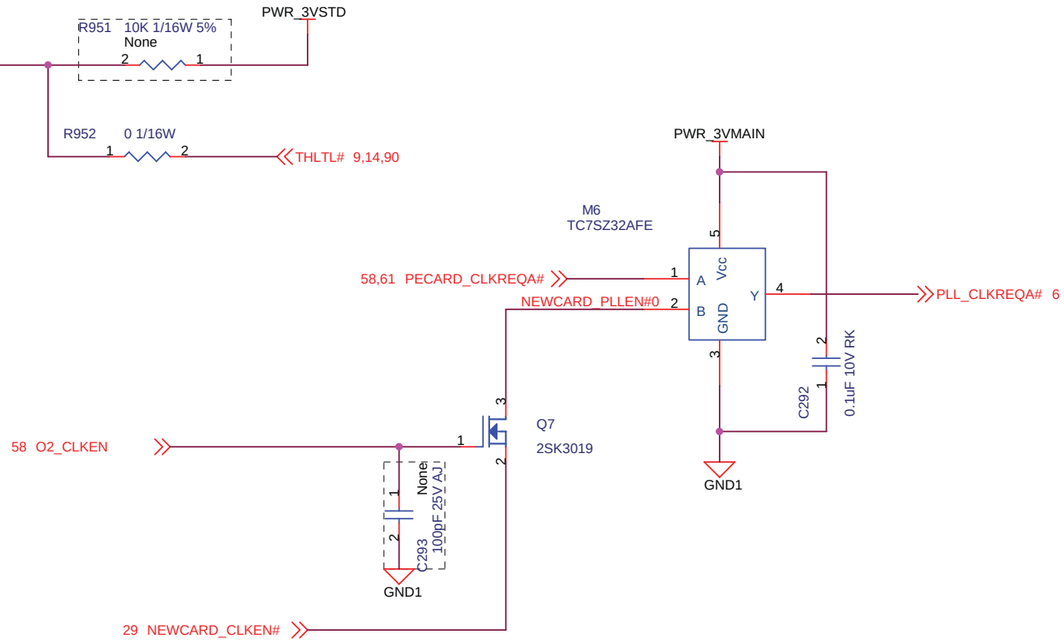


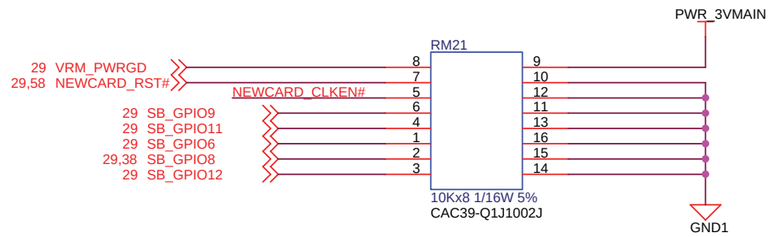












04/28
部品削除：R494, R495, R787, R788

SB450
Pull Up/Down

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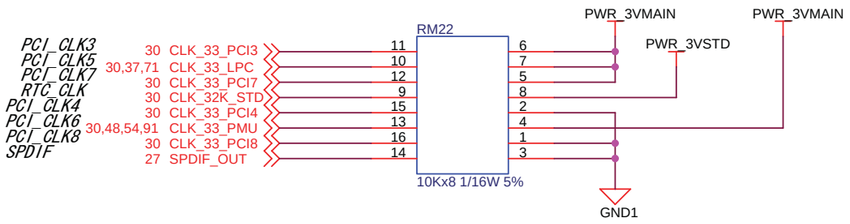
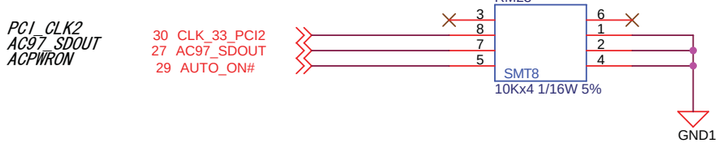
Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE: VB313AA
DRAW. No.: C1CP302570-X2
CAST:
FUJITSU LTD.
Sheet: 34 / 93





Pin Name	Description	Post-Beira Setting
ACPWRON	Active Manual Power On. 0 : Automatic Power On 1 : Manual Power On	**0**
AC97SDOUT	Enable/Disable addional straps for Debugging. 0 : Use Hardcoded defaults for Debug straps 1 : Enable additional Debug Strap	**0**
SPDIF	Select Speed for Super I/O. 0 : SIO Speed is 48MHz 1 : SIO Speed is 24MHz	**0**
PCICLK7 **PCICLK8**	**ROM Type Select** **PCICLK7** 1 1 0 0 **PCICLK8** 0 1 0 1 **ROM Type** LPC ROM (256K) / BIOS ROM (X-bus) / FWH / LPC ROM (512K/1M)	**1** **0**
PCICLK6	Define Type of CPU 0 : Intel Processors 1 : AMD K8 Processors	**1**
PCICLK5	14MHz Clock Pad Select 0 : Ctystal Pad 1 : Clock Input Buffer	**1**
PCICLK4	Bypsdd USB PLL 0 : use external 48MHz 1 : use internal USB PLL for 48MHz	**0**
PCICLK3	USB PHY Powerdown 0 : Enable 1 : Disable	**1**
PCICLK2	48MHz Clock Pad Select 0 : Clock Input Buffer 1 : Ctystal Pad	**0**
RTC_CLK	RTC Select 0 : External RTC 1 : Internal RTC	**1**
LFRAME#	Thermal Trip Strap 0 : Thermal Trip is not enabled on power up 1 : Thermal Trip is enabled on power up (default)	**1**

Pin Name	Description	
IDEPDack	Generate Short Reset 0 : Use Short Reset 1 : Use Long Reset (default)	
PCI_AD31 **PCI_AD30**	PLL Charge Pump control Bit	
PCI_AD29 **PCI_AD28**	PLL VCO control bits	
PCI_AD27	Bypass PCI PLL 0 : Use internal IDE PLL. Generated PCI CLK 1 : Bypass internal PCI PLL	
PCI_AD26	Bypass ACPI BCLK 0 : Use internal ACPI_BCLK 1 : Bypass ACPI_BCLK	
PCI_AD25	Bypass IDE Clock 0 : Use Internal IDE CLK 1 : Bypass Internal IDE CLK	
PCI_AD24	Bit_core strap from I2ROM enable 0 : Use default Value 1 : getting the value from I2C EPROM	
PCI_AD23	Reserved	

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Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE: **VB313AA**

DRAW. No.: C1CP302570-X2

CAST

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Sheet 35 / 93

FUJITSU CONFIDENTIAL Dolphin

M7A SN74HCT32APW PWR5VMAIN
M7B SN74HCT32APW PWR5VMAIN
M7C SN74HCT32APW PWR5VMAIN
M7D SN74HCT32APW PWR5VMAIN

18 CRT_HSYNC
18 CRT_VSYNC

RM25 SMT8 33x4 1/16W 5%
CRT_Q_HSYNC 50
CRT_Q_VSYNC 50

GND1

多連部品RM29については
配線しやすいようにピンスワップ可能。

PWR_5VMAIN

M7E SN74HCT32APW PWR5VMAIN
C294 0.1uF 10V RK

GND1

PWR_3VMAIN

R795 4.7K 1/16W 5%
R796 4.7K 1/16W 5%

PWR_5VMAIN

D3 1SS420

R1225 6.8K 1/16W 5%
R1226 6.8K 1/16W 5%

4,58,63,76,91 A_RST#_C
18 CRT_DDCCLK
CRT_Q_DDCCLK 50
Q94 2N7002LT1G

4,58,63,76,91 A_RST#_C
18 CRT_DDCDAT
CRT_Q_DDCDAT 50
Q95 2N7002LT1G

PWR_3VMAIN

RM24 8.2Kx8 1/16W 5%
27,48,57,71,91 PCI_CLKRUN#
27,57 PCI_SERR#
27,57 PCI_IRDY#
27,57 PCI_DEVSEL#
27,57 PCI_PERR#
27,57 PCI_STOP#
27,57 PCI_TRDY#

RM127 SMT8 8.2kx4 1/16W 5%
27,57 PCI_INT#4
27,57 PCI_FRAME#
27,57 PCI_REQ#3
27,57 PCI_GNT#3

RM128 SMT8 8.2kx4 1/16W 5%
27 PCI_INT#5
27 PCI_INT#2
27 PCI_GNT#6
27 PCI_GNT#2

RM129 SMT8 8.2kx4 1/16W 5%
27 PCI_GNT#1
27 PCI_GNT#0
27 PCI_REQ#5
27 PCI_REQ#4

R1221 8.2K 1/16W 0.5%
27 PCI_LOCK#

R1222 8.2K 1/16W 0.5%
27 PCI_REQ#2

RM130 SMT8 8.2kx4 1/16W 5%
27 PCI_REQ#0
27 PCI_REQ#1
27 PCI_REQ#6

RM28 8.2Kx8 1/16W 5%
27 PCI_GNT#5
27 PCI_GNT#4
27 PCI_INT#3
27 PCI_INT#0
27 PCI_INT#6
27 PCI_INT#7
27 PCI_INT#1
4,16,29,76 A_RST#

GND1

上記多連部品(8.2Kx4)については
配線しやすいようにピンスワップ可能。

Pullup for AGP,PCI,LPC

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TITLE: VB313AA
DRAW. No.: C1CP302570-X2
CAST
FUJITSU LTD.
Sheet 36 / 93

Dolphin

PWR_3VMAIN

RM30
10Kx8 1/16W 5%

ROM_TBL#
ROM_WP#

Socket for LPC ROM.

※LPC ROMはソケットを実装可能なパターンにすること。

M9

30,35,71 CLK_33_LPC → CLK
54 ROM_TBL# → TBL#
54 ROM_WP# → WP#
INIT#
4,48,62,71,74,76 A_RST#_B → RST#
GPI0
GPI1
GPI2
GPI3
GPI4
IC

FWH0/LAD0 → LPC_AD0 27,34,48,54,71,91
FWH1/LAD1 → LPC_AD1 27,34,48,54,71,91
FWH2/LAD2 → LPC_AD2 27,34,48,54,71,91
FWH3/LAD3 → LPC_AD3 27,34,48,54,71,91
FWH4/LFRAME# → LPC_FRAME# 27,34,48,54,71,91
ID2
ID3
ID1/RFU0
ID0/RFU1
RFU2
RFU3
RFU4
RFU5

M050FLW040 2pin has internal Pull-down

PWR_3VMAIN
VCC
VPP
C296
0.1uF 10V RK

PWR_3VMAIN
R114
10 1/16W 5%
None

NC0
NC1
NC2
NC4
VSS0
VSS1

M50FLW040A

GND1

STM : 9pin PWR_3VMAIN
SST : 30pin
PWR_3VMAIN

PWR_3VMAIN
PWR_5VMAIN

27,34,48,54,71,91 LPC_AD0
27,34,48,54,71,91 LPC_AD1
27,34,48,54,71,91 LPC_AD2
27,34,48,54,71,91 LPC_AD3
27,34,48,54,71,91 LPC_FRAME#
30,35,71 CLK_33_LPC
4,48,62,71,74,76 A_RST#_B

CN6
PORT80
None
Debug

GND1

LPC ROM

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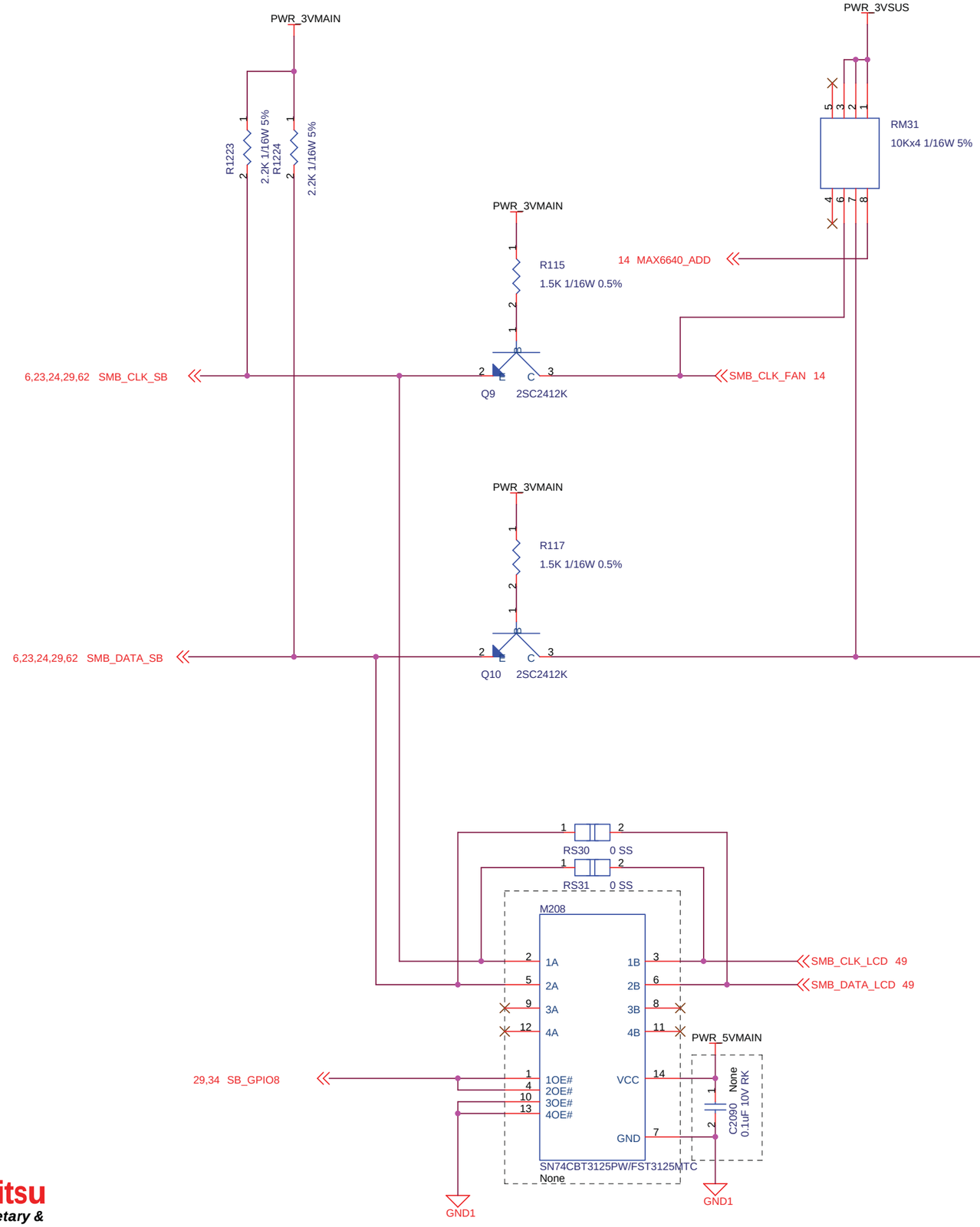
TITLE: VB313AA
DRAW. No.: C1CP302570-X2
CAST
FUJITSU LTD.
Sheet 37 / 93

Dolphin



Device	Hex	Address
MAX6640	5Eh	0101 111x b
MEM slot0	A2h	1010 001x b
MEM slot1	A4h	1010 010x b
PMU	32h	0011 001x b
LCD(SPWG)	A0h	1010 000x b

BUS	Device	address
	DIMM1	A2h
	DIMM2	A4h
	MAX6640	5Eh
	LCD	A0h
PLL	PLL	D2h
PMU	PMU	32h

SMBus

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TITLE: **VB313AA**

DRAW. No.: C1CP302570-X2 CAST

FUJITSU LTD.

Sheet 38 / 93

Reserve

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Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE: **VB313AA**

DRAW. No.: C1CP302570-X2

CAST

FUJITSU LTD.

Sheet 39 / 93

Reserve

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Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE: **VB313AA**

DRAW. No.: C1CP302570-X2 CAST

FUJITSU LTD.

Sheet 40 / 93

Dolphin

Reserve

Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE: **VB313AA**

DRAW. No.: C1CP302570-X2

CAST:

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Sheet 41 / 93

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Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE: **VB313AA**

DRAW. No.: C1CP302570-X2

CAST:

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Sheet 42 / 93

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Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE
VB313AA

DRAW. No.
C1CP302570-X2

CAST

FUJITSU LTD.

Sheet 43 / 93

Dolphin

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Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE
VB313AA

DRAW. No.
C1CP302570-X2

CAST

FUJITSU LTD.

Sheet 44 / 93

Dolphin

Reserve

Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE: **VB313AA**

DRAW. No.: C1CP302570-X2

CAST

FUJITSU LTD.

Sheet 45 / 93

Dolphin

Reserve

Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE: **VB313AA**

DRAW. No.: C1CP302570-X2

CAST

FUJITSU LTD.

Sheet 46 / 93

Dolphin

Rev.	Date	Design	Check	Appr.	Description

Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa

TITLE
VB313AA

DRAW. No.
C1CP302570-X2

CAST

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Sheet 47 / 93

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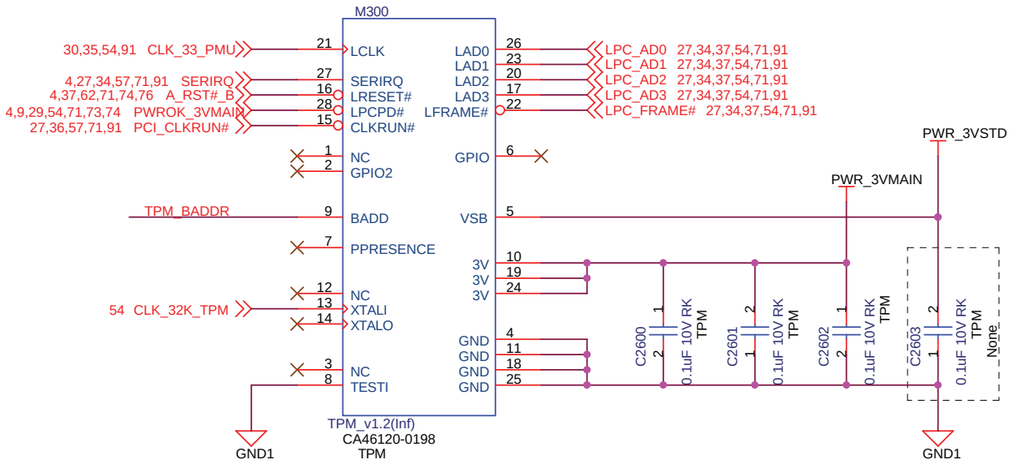
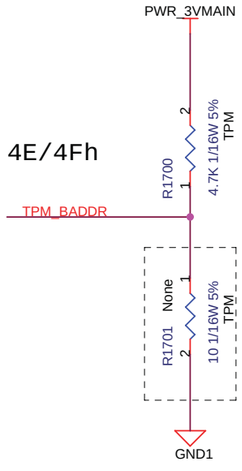
TPM Configuration

	High	Low
TPM_BADDR	4E/4Fh	2E/2Fh





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TPM

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DRAW. No.: C1CP302570-X2 CAST

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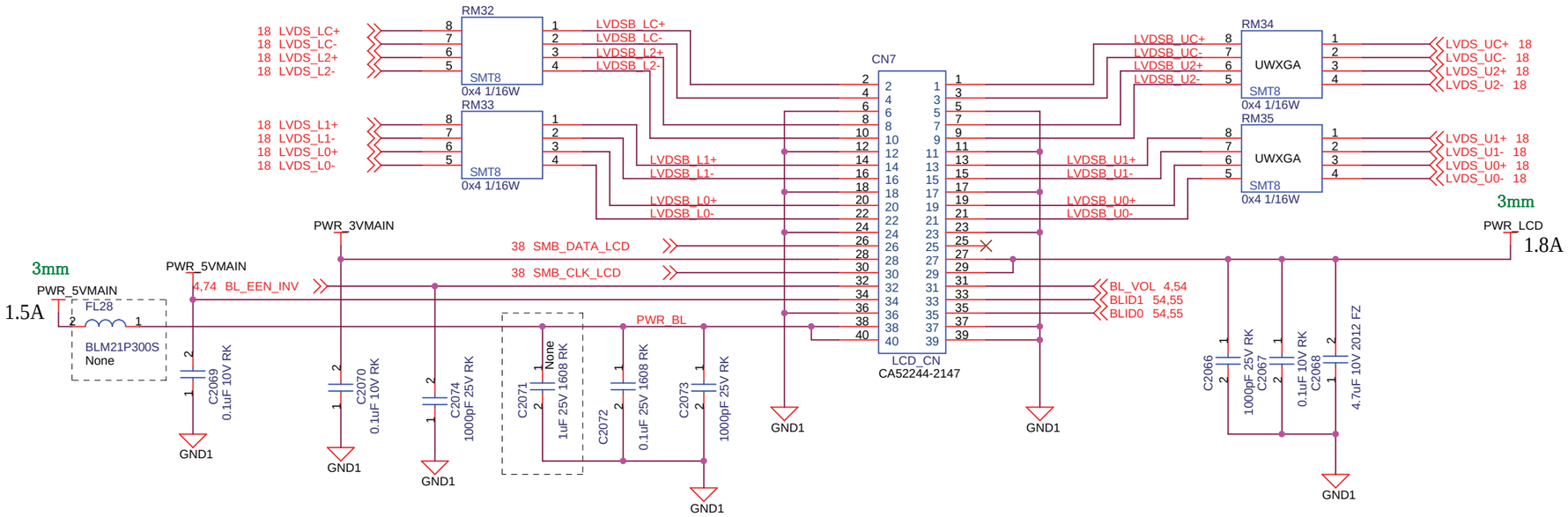
Sheet 48 / 93

Dolphin



各LVDSのパターンから上記部品までの距離（スタブ）はできるだけ短くすること。
Stab of LVDS is shortest.

LVDxxの設計条件
−原則として等長配線する(各線長の誤差は15mm以下)
−LVDSC+,−とLVDS0+,−とLVDS1+,−とLVDS2+,−の間はGNDでｶﾞｰﾄﾞする
−各線のｲﾝﾋﾟｰﾀﾞﾝｽを100Ωにする
−ビヤ打ちは最小限(3回以下)とし、各信号等長でﾋﾟｱ打ちをすること

LCD CN

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Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE: VB313AA
DRAW. No.: C1CP302570-X2
CAST:
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Sheet 49 / 93

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これらのコンデンサは可能な限りCN8直近に配置し、
GNDパターンは引き回さず、VIAでGND層に落とすこと。

これらのESD対策コンデンサは
可能な限りDiodeの直近に配置すること

R119,120,121はCN7近傍に配置

本ページに記載されている部品は
CRTコネクタの近くに配置すること。

CRT

CRT connector

Rev.	Date	Design	Check	Appr.	Description		
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa

TITLE: VB313AA
DRAW. No.: C1CP302570-X2
CAST
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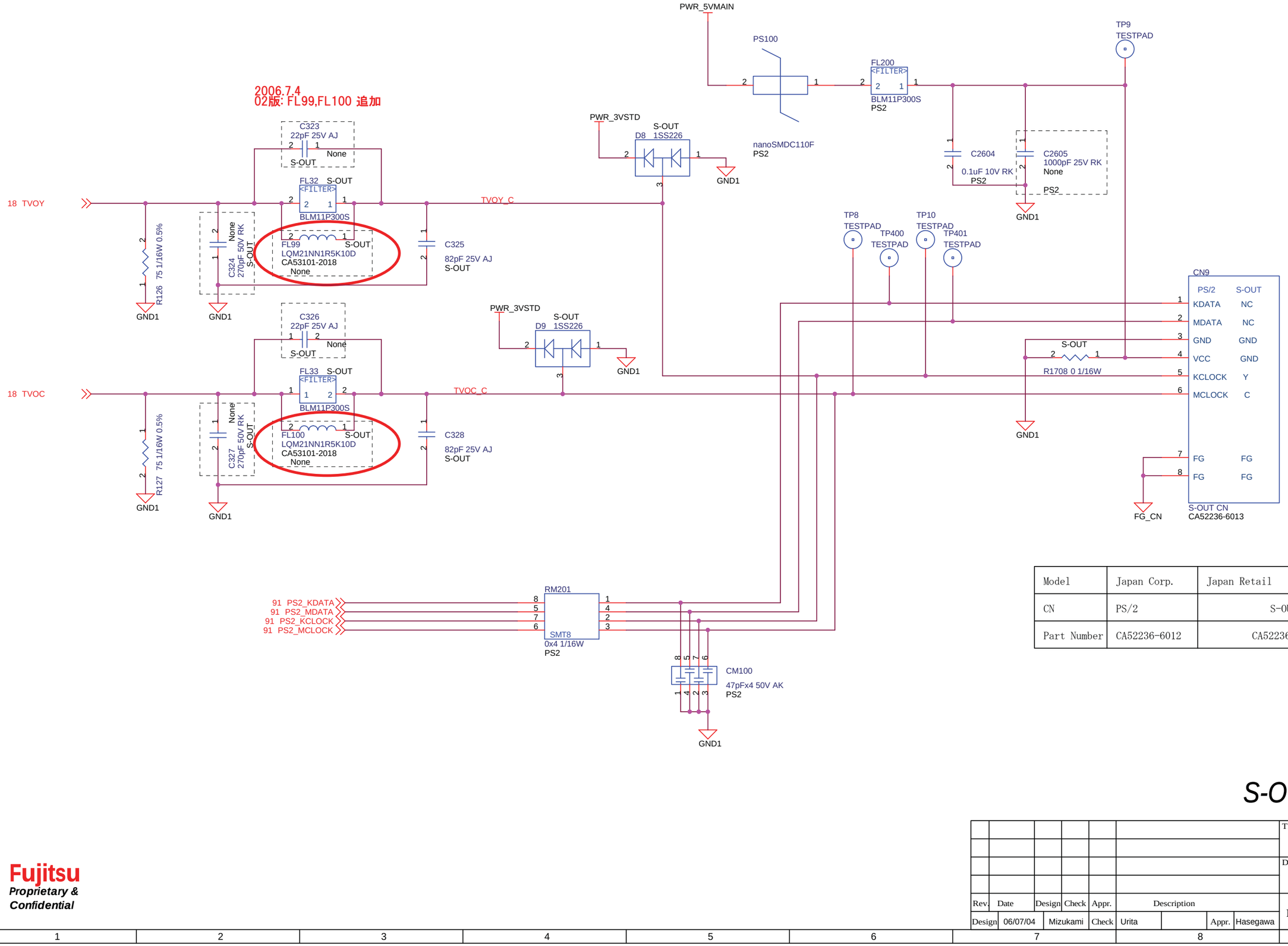
Sheet 50 / 93

FUJITSU CONFIDENTIAL Dolphin

2006.7.4
02版: FL99,FL100 追加



Model	Japan Corp.	Japan Retail Oversea
CN	PS/2	S-OUT
Part Number	CA52236-6012	CA52236-6013

S-OUT/PS2

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Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE: VB313AA
DRAW. No.: C1CP302570-X2
CAST
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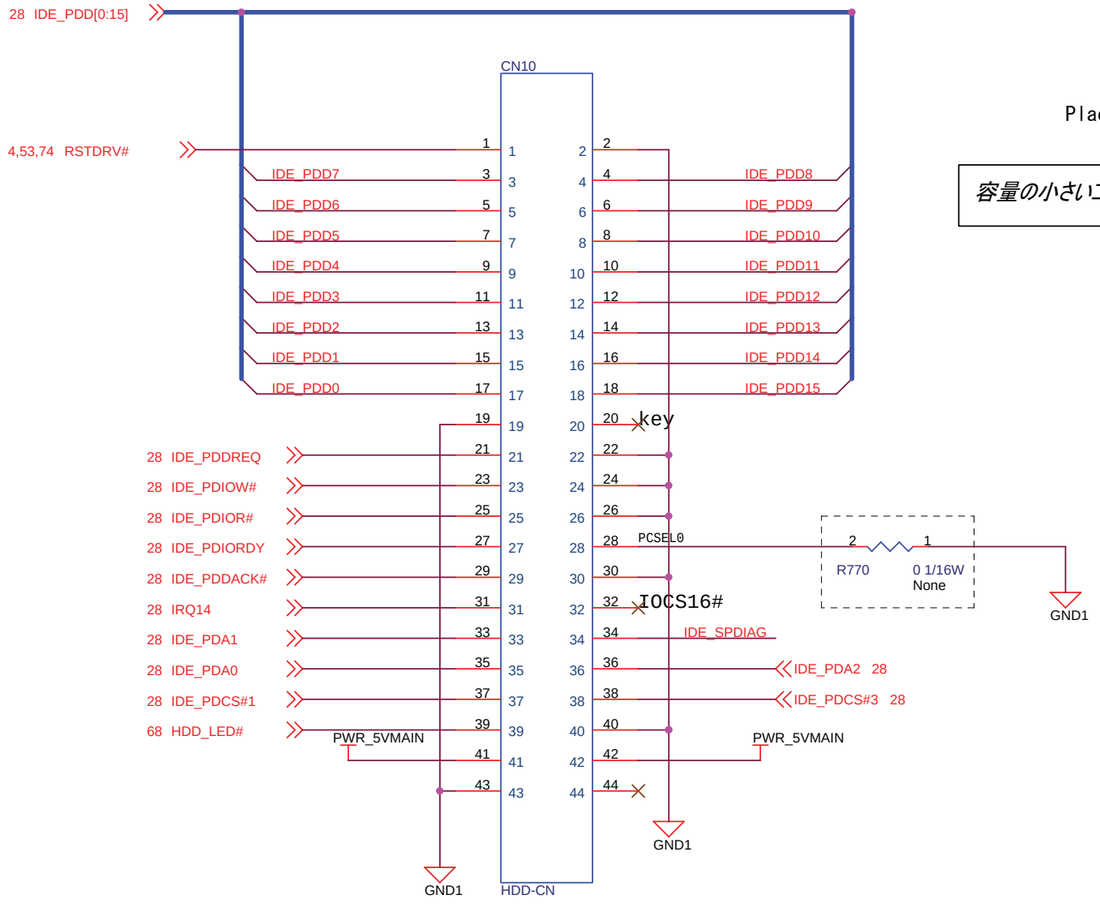
Sheet 51 / 93

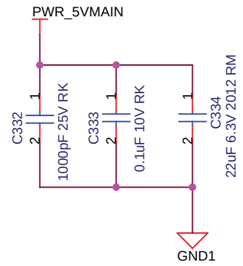
TOP view
KB side

S1 HDD CN S15

Max:2A

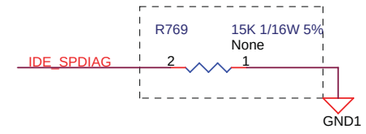
Supply enough current volume.
Need tie to GND1 fully.





Place the capacitors near power pin of HDD CN

容量の小さいコンデンサを優先的にHDD-CNの電源PINの近くに配置すること。



1st HDD CN

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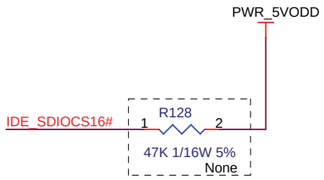
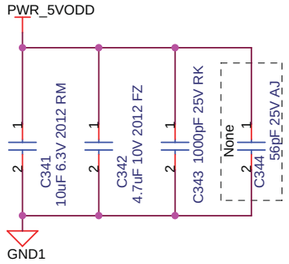
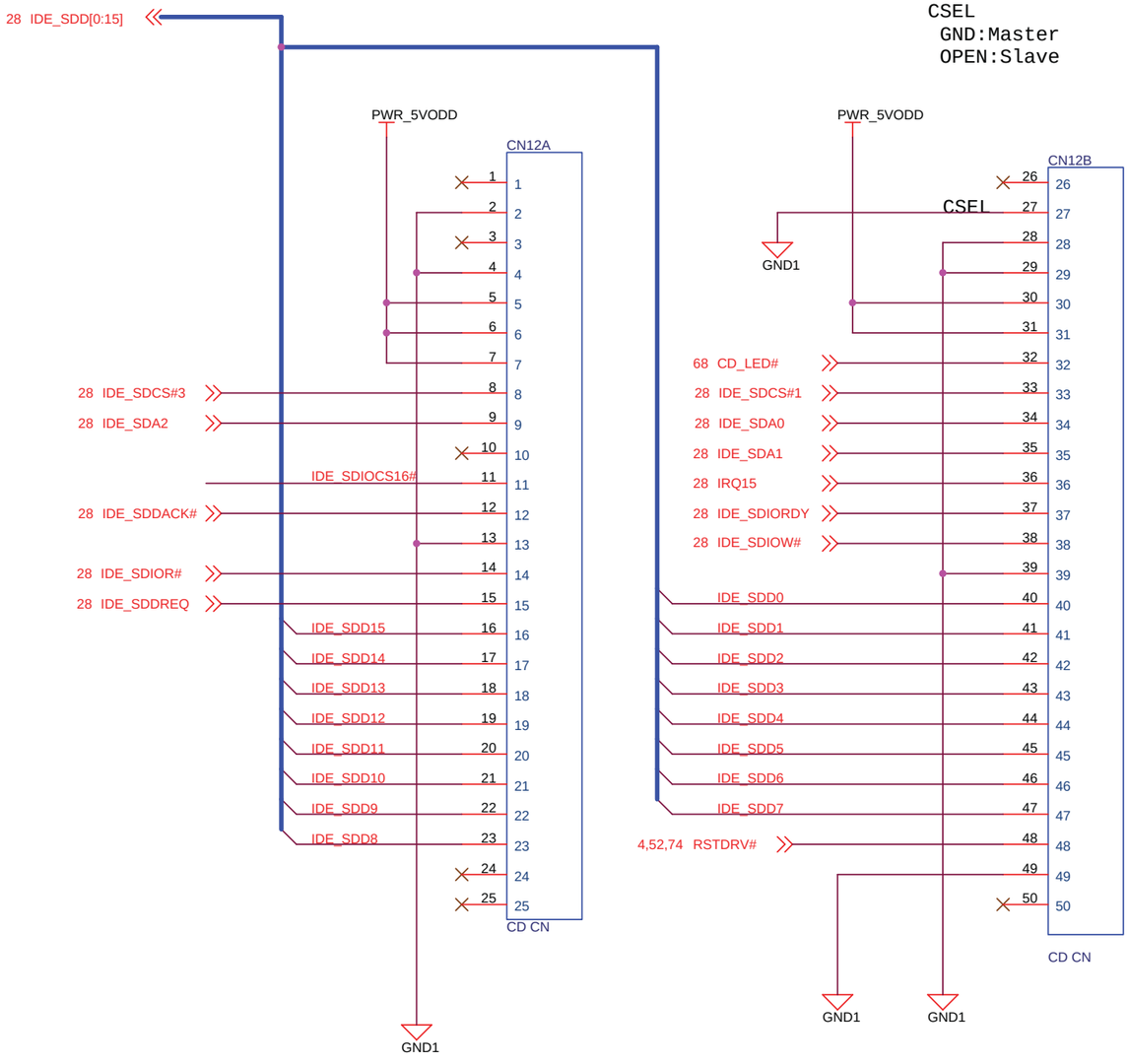
								TITLE	VB313AA
								DRAW. No.	C1CP302570-X2
								CAST	
Rev.	Date	Design	Check	Appr.	Description			FUJITSU LTD.	Sheet 52 / 93
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa		





本コンデンサは、CN12の
電源の近傍に配置のこと。

CSEL
GND:Master
OPEN:Slave



ODD-CN

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TITLE: **VB313AA**

DRAW. No.: C1CP302570-X2 CAST

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Sheet 53 / 93

Dolphin

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PWR_3VSTD

R1709
10K 1/16W 5%
TPM

M10A

30,35,48,91 CLK_33_PMU — 55 PCICLK(D)
6 CLK_14_ASIC — 87 CLK14M(D)
55 CLK_32K_ASIC — 21 CLK32IN
CLK32OD 96 → CLK_32K_TPM 48
CLK32XO 127

27,34,37,48,71,91 LPC_AD0 — 50 LAD0
27,34,37,48,71,91 LPC_AD1 — 51 LAD1
27,34,37,48,71,91 LPC_AD2 — 52 LAD2
27,34,37,48,71,91 LPC_AD3 — 53 LAD3
27,34,37,48,71,91 LPC_FRAME# — 48 LFRAME#

GID0 119
GID1 120
GID2 121
GID3 122
GID4 123
GID5 124 → SYS_ID0 55
GID6 125 → SYS_ID1 55
GID7 126 → SYS_ID2 55

91 PMU_PARST# — 41 PARST#
91 PMU_PE# — 42 PE#
91 PMU_PRM# — 45 PRM#
91 PMU_SMI — 46 PMUSMII

PD0 114
PD1 115
PD2 116
PD3 117

55 BENN_3VMAIN — 18 BAYLMP0#/3VMAIN
19 BAYLMP1#/LONGDLY

55 BENN_3VSUS — 20 HDLMP#/3VSUS
55 BENN_3VSTD — 64 PCMLMP0/3VSTD
65 PCMLMP1/1VOK#
55 BENN_NOLMP — 16 NOLMP

29 SB_SPKR — 110 SPK1
57 SPKPCM — 107 SPK2
SPKOUT 109 → DG_GSPKOUT 68

55 FDD_ATCH#A — 1 FDATCH#
FMODE#(OD) 112

RIOUT#(OD) 88 → RIOUT# 4,29,34

EXTSCI#(OD) 74 → EXTSCI# 4,29,34
EXTSMI#(OD) 71 → EXTSMI# 4,29,34

pull-up@p.36

pull-up@p.49

Net Name change

WAKEOUT#(OD) 92 → PMEOUT# 4,29,55

GND1

(Wireless LAN)
(Marvel LAN)

4,62 WAKE_MINIC# — 93 WAKEA#
4,55 PME_ILAN# — 94 WAKEB#
4,55,57 PME_PCIC# — 95 WAKEC#

(RS232C)

55 RI_RS232# — 89 RI1#
55 RI2# — 90 RI2#
55 RI3# — 91 RI3#

PWR_PMU

VCC: 3V1 17, 3V2 49, 81, 3V3 113, 3V4 43, 3V5 75, 3V6

GND: VSS 2, VSS1 12, VSS2 22, VSS3 34, VSS4 44, VSS5 54, VSS6 66, VSS7 76, VSS8 86, VSS9 98, VSS10 108, VSS11 118

C345 0.1uF 10V RK
C346 0.1uF 10V RK
C347 0.1uF 10V RK
C348 0.1uF 10V RK

GND1

68,74 WLAN_SW — 69 ESMIBE2
91 HTKYSMI — 70 ESMIBE4

BENN 1/2
BENN

M10B

4,55,90 PMU_PLLB — 40 PLLB(ESMIBE9)
4,90,92,93 PMU_ACON — 15 ACON(ESMIBE5)

4,69,91 SUSSW# — 32 SUSSW#

4,75 PWROK_3VSUS — 37 SUSOK(I/O)
4,90,92 PWROK_PMU — 36 PMUVCCOK

4,9,29,48,71,73,74 PWROK_3VMAIN — 14 MAINOK(I/O)
4,62,74,76,85,88 DLY_SUSB# — 67 SUSB#

55,76 BL_EN — 13 LCDEN
4,55,76,88 LCDEN — 61 BLEN
69,90 LCDCL# — 39 LCDCL#(ESMIBE6)

PWR_PMU → 35 ACTIN#/SUSC#

4,29,55,57,72 PCI_RST# — 31 PCIRST#

55 CRISIS — 3 GPIO0(D)
70 KSHIP_ID0 — 4 GPIO1(D)
70 KSHIP_ID1 — 5 GPIO2(D)
70 KSHIP_ID2 — 6 GPIO3(D)
CRLBOOT

55 GPIO4 — 7 GPIO4(D)
55 BLUE_EXIST — 8 GPIO5(D)
9 GPIO6(D)
55,56 FR_EXIST# — 10 GPIO7(D)

55,63 ILAN_RST# — 77 G3STDIO0
55,88 LAN_PON — 78 G3STDIO1
62,74 MINIC_ON — 79 G3STDIO2
4,63 LAN_DISABLE# — 80 G3STDIO3
56 BT_ON — 82 G3STDIO4
83 G3STDIO5
84 G3STDIO6

PWR_PMU → 4,90 ASIC_PON — 85 PON
111 EPSONTEST
128 TEST#

GND1

BENN 2/2
BENN

DLYSUSC# 11
STDOK 63 → RSMRST# 29,74,75
PWRON 38 → POWERON 74,83
BSRBTN# 68 → ANN_BSRBTN# 75
DLYSUSB# 47
BAY1ON 72
BAY2ON 73
EBLENO(OD) 62 → BL_EEN 55,74,91
PWM BLO 97 → BL_VOL 4,49

PWR_PMU

VGARST# 33 → VGA_RST# 57

G3PIO0(D) 23
G3PIO1(D) 24
G3PIO2(D) 25 → EXIST_MS# 55
G3PIO3(D) 26
G3PIO4(D) 27 → EXIST_SOUT# 55
G3PIO5(D) 28
G3PIO6(D) 29 → ROM_WP# 37
G3PIO7(D) 30 → ROM_TBL# 37

G3PIO8(D) 99 → G3PIO8 55
G3PIO9(D) 100 → G3PIO9 55

G3PIO10/BAY1ATCH1# 101 → G3PIO10 55
G3PIO11/BAY1ATCH2# 102 → G3PIO11 55
G3PIO12/BAY2ATCH1# 103 → G3PIO12 55
G3PIO13/BAY2ATCH2# 104 → G3PIO13 55
G3PIO14(D) 105 → SW_MODE0 55
G3PIO15(D) 106 → SW_MODE1 55
G3PIO16(D) 56 → HPON_GPIO 68
G3PIO17(D) 57 → BLID0 49,55
G3PIO18(D) 58 → BLID1 49,55
G3PIO19(D) 59 → EXIST_3G 55
G3PIO20(D) 60 → G3PIO20 55

BENN

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TITLE: VB313AA
DRAW. No.: C1CP302570-X2
CAST:
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Sheet: 54 / 93

本ページ内の集合抵抗については、
同じ容量のものについては部品間PINSWAP可

PCI_RST# 4,29,54,57,72
PWR_3VMAIN
PWR_3VSUS
RM38
54 FDD_ATCH#A
49,54 BLID0
49,54 BLID1
54 G3PIO13
54 G3PIO12
54 G3PIO10
54 G3PIO11
10Kx8 1/16W 5%
CAC39-Q1J1002J
GND1
GND1

PWR_3VSTD
PWR_3VSUS
RM36
4,54 PME_ILAN#
54 RI2#
SMT8
10Kx4 1/16W 5%
4,54,90 PMU_PLLB
M11C
SN74LV05ADGV
PLLB# 4,29
4,54,76,88 LCDEN
M11D
SN74LV05ADGV
LCDEN# 88

PWR_3VMAIN
54,74,91 BL_EEN
R145
10K 1/16W 5%
PWR_3VMAIN
54 GPIO4
R1018 None
1K 1/16W 5%

PWR_3VMAIN
SW_MODE1 SW_MODE0 NO_MS/SD NO_SOUT BT
R136 R137 R138 R139 R146
10K 1/16W 5%
1K 1/16W 5% None
BLUE_EXIST 54
EXIST_SOUT# 54
EXIST_MS# 54
SW_MODE0 54
SW_MODE1 54

PWR_3VSUS
PWR_3VMAIN
PWR_3VSTD
RM39
54,76 BL_EN
54,88 LAN_PON
54 RI3#
4,54,57 PME_PCIC#
4,29,54 PMEOUT#
10Kx8 1/16W 5%
CAC39-Q1J1002J
GND1
73 RI_RS232
M11F
SN74LV05ADGV
RI_RS232# 54

PWR_3VMAIN
54 G3PIO8
R141 10K 1/16W 5% None
54 G3PIO9
R142 10K 1/16W 5% None
R148 G-SENSOR
54 EXIST_3G
10K 1/16W 5%
R150 None
54 G3PIO20
10K 1/16W 5%

SW_MODE[1:0]
00 : 4ボタン(店頭/FCS)
[Appli], [Appli], [VolumeDown], [VolumeUp]
01 :4ボタンモデル(FKL/FPC)
[Appli], [Appli], [Aplpli], [Appli]
10 : クラサバモデル
(T.B.D)
11 : 6ボタンモデル(仕向け先は未定。06秋冬はなし)
[Internet], [Mail], [A], [B], [VolumeDown], [VolumeUp]

※本IC/CAPの外周、及びその直下層はGND1とする。
2個以上の貫通VIAでGND層へと接続すること。

PWR_3VSTD
R1019
10K 1/16W 5%
None
54,63 ILAN_RST#
R143
10K 1/16W 5%
GND1

PWR_3VMAIN
R144
1K 1/16W 5%
BL1
BL
54 CRISIS
R147
100K 1/16W 5%
GND1

PWR_3VMAIN
PWR_3VSUS
PWR_PMU
RM40
54,56 FR_EXIST#
54 BENN_3VSUS
54 BENN_NOLMP
54 BENN_3VMAIN
SMT8
10Kx4 1/16W 5%

PWR_3VSTD
R152
54 BENN_3VSTD
10K 1/16W 5%

PWR_PMU
M88
VDD
VIO
OUT
GND
C1501 0.01uF 25V RK None
GND1
SG-3030JF(32KHz)
CAN17-32K768/0
None
CLK_32K_OSC

PWR_PMU
M87
VCC
SPEED
GND
E.C.
CLK
C1502 0.1uF 10V RK
GND1
MAX7377AXRD+
CBM48-32K768/0
GND1
R1703 0 1/16W None
RS200 0 SS
RS201 0 SS
CLK_32K_ASIC 54
CLK_32K_PMU 90

※本IC/CAPの外周、及びその直下層はGND1とする。
2個以上の貫通VIAでGND層へと接続すること。

PWR_3VMAIN
R149 10K 1/16W 5%
SYS_ID0
SYS_ID0 54
R151 10K 1/16W 5%
SYS_ID1
SYS_ID1 54
R1437 10K 1/16W 5%
SYS_ID2
SYS_ID2 54

SYS_ID[2:0]
000 : 国内店頭
001 : 海外
010 : クラサバ
011 – 111 : Reserve

本ページ内の集合抵抗については、
特に指定の無い限りBENNの近傍に配置すること。

Pullup/down
for BENN

Fujitsu
Proprietary &
Confidential

						TITLE	VB313AA	
						DRAW. No.	C1CP302570-X2	CAST
Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.	Sheet	55 / 93
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa			

FUJITSU CONFIDENTIAL Dolphin

TP19 PS2_PCLOCK
TP20 PS2_PDATA
TP21 FR_EXIST#
TP22 USB_P7+
TP23 USB_P7-
TP24 PWR_5VMAIN
TP26 GND1

CN14
1
2
3 PS2_PCLOCK 91
4 PS2_PDATA 91
5 PWR_5VMAIN
6
7
8
9 USB_P7+ 29
10 USB_P7- 29
11 FR_EXIST# 54,55
12
13
14
GLIDE/FINGER CN
FINGER
GND1

PWR_5VMAIN
FINGER
FINGER
C355 2 1 1uF 10V 1608 FZ
C356 2 1 1000pF 25V RK
None
GND1

2mm
0.6A
PWR_3VSTD

3mm
3.3V/0.6A
PWR_3VBT

Q174
SI2305DS-T1-E3
BT

R1207 1 2 470K 1/16W 5% BT
C2056 1 2 0.01uF 25V RK BT
R1208 2 1 47K 1/16W 5% BT
Q175 2SK3019 BT
54 BT_ON

Target 20ms

PWR_3VBT
C2057 2 1 0.1uF 10V RK BT
C2058 1 2 4700pF 25V RK BT
M129
1 VDD
3 CD
2 GND
4 OUT
BT_RESET#
R3112Q271C-TR-FA
BT
td(s)=4.485xC(uF)
GND1

CN49
GND1
1
2
3
4
5
6
7
PIO5 BT_RESET#
8
PIO3 9
10
11
PIO7 12
PIO2 13
BT_CHCLK_CN_C PIO1 14
15
16
BT_DATA_CN_C PIO0 17
18
19
PWR_3VBT 20
Bluetooth CN
BT
CA52300-3419

62 BT_CHCLK_CN
62 BT_DATA_CN
None R1723 0 1/16W
R1724 0 1/16W None
29 USB_P1+
29 USB_P1-
R1209 47K 1/16W 5%
R1210 47K 1/16W 5%
None None
GND1
C2062 BT 0.1uF 10V RK
GND1

TP274 PWR_3VBT
TP404 USB_P1-
TP405 USB_P1+
TP406 BT_RESET#
TP407 BT_CHCLK_CN
TP408 BT_DATA_CN

PWR_3VBT
C2059 BT 2 1 4.7uF 6.3V 1608 RK None
C2060 BT 2 1 0.1uF 10V RK
C2061 BT 2 1 1000pF 25V RK None
R1211 BT 2 1 100K 1/16W 5%
GND1

2006.6.29
02版：RS202,RS203削除
R1718,R1719削除

2006.6.26
02版：USB_P1+とUSB_P1-入れ替え

2006.6.26
02版：
CN49のピンアサインを逆に変更

FINGER_CN

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Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE: VB313AA
DRAW. No.: C1CP302570-X2
CAST
FUJITSU LTD.
Sheet 56 / 93

FUJITSU CONFIDENTIAL
Dolphin

4,29,54,55,72 PCI_RST#
R852 10 1/16W 5%
PCIC_RST#
54 VGA_RST#
R853 10 1/16W 5% None

RM41 10Kx4 1/16W 5%
PWR_3VSUS

M12A

30 CLK_33_PCIC
58 VCCD1#
4 PCIC_RST#
4,58,75 PCIC_GBRST#
27 PCI_AD[0:31]
27 PCI_C/BE#[0:3]
27 PCI_AD24
60 SD_DET#
60 ODR_WP
60 MS_DET#
60 XD_DET#

L4 PCI_CLK
R16 VCCD1#/SCLK
K7 RST#
R13 NC(GLOBAL_RST#)

PCI_AD0 T11 AD0
PCI_AD1 N10 AD1
PCI_AD2 P10 AD2
PCI_AD3 T10 AD3
PCI_AD4 R10 AD4
PCI_AD5 T9 AD5
PCI_AD6 R9 AD6
PCI_AD7 N9 AD7
PCI_AD8 R8 AD8
PCI_AD9 P8 AD9
PCI_AD10 N8 AD10
PCI_AD11 R7 AD11
PCI_AD12 N7 AD12
PCI_AD13 T6 AD13
PCI_AD14 R6 AD14
PCI_AD15 T5 AD15
PCI_AD16 M5 AD16
PCI_AD17 M4 AD17
PCI_AD18 L7 AD18
PCI_AD19 L6 AD19
PCI_AD20 K6 AD20
PCI_AD21 K5 AD21
PCI_AD22 J4 AD22
PCI_AD23 J5 AD23
PCI_AD24 H5 AD24
PCI_AD25 H6 AD25
PCI_AD26 H7 AD26
PCI_AD27 G4 AD27
PCI_AD28 G5 AD28
PCI_AD29 G7 AD29
PCI_AD30 F4 AD30
PCI_AD31 F5 AD31

PCI_C/BE#0 T8 C/BE0#
PCI_C/BE#1 T4 C/BE1#
PCI_C/BE#2 M6 C/BE2#
PCI_C/BE#3 H4 C/BE3#

R155 100 1/16W 0.5%
PCIC_IDSEL
J7 IDSEL
27,36 PCI_FRAME# M7 FRAME#
27,36 PCI_IRDY# N4 IRDY#
27,36 PCI_GNT#3 E4 GNT#

T7 SD_CD#(ODR_CD#)
MS_DATA0_OZ T12 MF1/ODR_DATA0
MS_DATA1_OZ R11 ODR_DATA1
MS_DATA2_OZ N14 ODR_DATA2
MS_DATA3_OZ K16 ODR_DATA3
N12 MF2/ODR_WP
P13 MF4/MS_CD#

XD_R/B#_OZ C5 SC_CLK/XD_R/B#
U5 SC_CD#/XD_CD#
XD_DATA4_OZ C7 SC_C4/XD_D4
XD_DATA5_OZ C15 SC_IO/XD_D5
XD_DATA6_OZ C9 SC_RST/XD_D6
XD_DATA7_OZ C13 SC_C8/XD_D7

OZ711MP1

PWR_3VSUS
R156 22K 1/16W 5% None

T16 VCCD0#/SDATA
T15 VPPD0/SLATCH/ODR_3V#
VCCD0# 58
MS/XD_ON# 60

R12 SPKR_OUT#
SPKPCM 54

P14 ODR_LEDON
H8 SKTA_LEDON

N11 MF0
PCI_INT#4 27,36

T13 MF3
SERIRQ 4,27,34,48,71,91

P11 RI_OUT#/PME#
PME_PCIC# 4,54,55

R14 MF6/CLKRUN#
P4 DEVSEL#
N6 TRDY#
R5 PAR
P6 PERR#
R4 SERR#
P5 STOP#
D4 REQ#
PCI_CLKRUN# 27,36,48,71,91
PCI_DEVSEL# 27,36
PCI_TRDY# 27,36
PCI_PAR 27
PCI_PERR# 27,36
PCI_SERR# 27,36
PCI_STOP# 27,36
PCI_REQ#3 27,36

R15 VPPD1/ODR_CLK
T14 MF5/ODR_CMD_BS/XD_ALE
MS_CLK_OZ
MS_BS_OZ

G15 CORE_VCC
J6 CORE_VCC
L14 CORE_VCC
P12 CORE_VCC
E7 CORE_VCC
F11 CORE_VCC
N5 CORE_VCC
K4 PCI_VCC
P9 PCI_VCC

PWR_3VSUS
C366 None 4.7uF 6.3V 1608 RK
GND1
PWR_PCIVCC

PWR_3VMAIN
AWS200
AW Short (R1608)

C11 SC_VCC/XD_VCC

U7 SC_3V#/XD_WE#
U9 SC_5V#/XD_WPO
U11 XD_RE#/ODR_3V#
XD_WE#_OZ
XD_WP 60
XD_RE# 60

C367 0.1uF 25V 1608 RK
C368 0.1uF 10V RK
PWR_3VSUS
GND1

E9 GND
F13 GND
G6 GND
J15 GND
L5 GND
P7 GND
GND1

★にはGNDガードを入れること

Power Control Mode is set by BIOS

下記コンデンサは各電源PINの直近に配置すること。

PWR_3VSUS
P12 C357 0.1uF 10V RK None GND1
E7 C358 0.1uF 10V RK None GND1
F11 C359 0.1uF 10V RK GND1
N5 C360 0.1uF 10V RK GND1
L14 C361 0.1uF 10V RK GND1
J6 C362 0.1uF 10V RK GND1
G15 C363 0.1uF 10V RK GND1

PWR_PCIVCC
K4 C364 0.1uF 10V RK None GND1
P9 C365 0.1uF 10V RK None GND1

2006.6.26
02版: AWS200追加
PWR_PCIVCCの浮きを修正

RM42 8SMT8 MP1/MC1 22x4 1/16W 5%
SD_DATA3 60
SD_DATA2 60
SD_DATA1 60
SD_DATA0 60

RM43 8SMT8 22x4 1/16W 5%
MS_DATA0_OZ
MS_DATA1_OZ
MS_DATA2_OZ
MS_DATA3_OZ
MS_DATA0 60
MS_DATA1 60
MS_DATA2 60
MS_DATA3 60

RM44 22x8 1/16W 5% CAC39-Q1J22R0J
XD_DATA4_OZ
XD_DATA5_OZ
XD_DATA6_OZ
XD_DATA7_OZ
XD_R/B#_OZ
XD_WE#_OZ
MS_BS_OZ
XD_DATA4 60
XD_DATA5 60
XD_DATA6 60
XD_DATA7 60
XD_R/B# 60
XD_WE# 60
MS_BS 59,60

MS_CLK_OZ
R157 10 1/16W 5%
MS_CLK 59,60
C369 None 1000pF 25V RK
GND1

♪はGND1で両端をガードすること

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PCIC-1

Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE: VB313AA
DRAW. No.: C1CP302570-X2
CAST
FUJITSU LTD.
Sheet 57 / 93

3.3VPEC Max 1.3A

3.3VPEC Max 1.3A
1.5VPEC Max 650mA
3.3VPECAUX Max 275mA

M12B

61 JDA[0:15]

JDA0 F7 D0/CAD27
JDA1 E6 D1/CAD29
JDA2 D5 D2/RFU
JDA3 P16 D3/CAD0
JDA4 N15 D4/CAD1
JDA5 M13 D5/CAD3
JDA6 M15 D6/CAD5
JDA7 L13 D7/CAD7
JDA8 D6 D8/CAD28
JDA9 F6 D9/CAD30
JDA10 E5 D10/CAD31
JDA11 N13 D11/CAD2
JDA12 N16 D12/CAD4
JDA13 M14 D13/CAD6
JDA14 M16 D14/RFU
JDA15 L15 D15/CAD8

61 JBVD1A F8 BVD1/RI#/CSTSCHG
61 JBVD2A E8 BVD2/SPKR#/CAUDIO

R159 470K 1/16W 5% None
GND1

61 JCD1A# P15 CD1#/CCD1#
61 JCD2A# D7 CD2#/CCD2#

61 JINPACKA# E11 INPACK#/CREQ#
61 JBSYA# G9 RDY/IREQ#/CINT#
61 JWAITA# D8 WAIT#/CSERR#
61 JWPA G8 WP/IOIS16#/CCLKRUN#

61 JVS1A# F9 VS1/CVS1
61 JVS2A# G12 VS2/CVS2

A0/CAD26 D9 JAA0
A1/CAD25 G10 JAA1
A2/CAD24 F10 JAA2
A3/CAD23 D11 JAA3
A4/CAD22 G11 JAA4
A5/CAD21 D12 JAA5
A6/CAD20 F12 JAA6
A7/CAD18 E13 JAA7
A8/CC/BE1# H14 JAA8
A9/CAD14 H16 JAA9
A10/CAD9 K15 JAA10
A11/CAD12 J14 JAA11
A12/CC/BE2# D14 JAA12
A13/CPAR G16 JAA13
A14/CPERR# F16 JAA14
A15/CIRDY# D15 JAA15
A16/CCLK E15
A17/CAD16 H15 JAA17
A18/RFU H13 JAA18
A19/CBLOCK# G14 JAA19
A20/CSTOP# F15 JAA20
A21/CDEVSEL# E16 JAA21
A22/CTRDY# D16 JAA22
A23/CFRAME# E14 JAA23
A24/CAD17 G13 JAA24
A25/CAD19 D13 JAA25

JAA16_D

CE1#/CC/BE0# L16 JCE1A# 61
CE2#/CAD10 K14 JCE2A# 61

IORD#/CAD13 J16 JIORDA# 61
IOWR#/CAD15 J13 JIOWRA# 61
OE#/CAD11 K13 JOEA# 61
REG#/CC/BE3# E10 JREGA# 61
RESET/CRST# E12 JRSTA 61
WE#/CGNT# F14 JWEA# 61

JAA[0:25] 61

本抵抗はIC近傍に配置

JAA16

R158 22 1/16W 5%
C373 None 22pF 25V AJ
GND1

JAA16はCardBus時に
クロック信号になるので
GND1にてガードをすること。

OZ711MP1

PWR_PCMVCC0
SKT_VCC D10
C377 0.1uF 10V RK
C376 None 2.2uF 10V 1608 RK
GND1 GND1

PWR_PCMVCC0
R165 43K 1/16W 5% None
61 JWPA

RM46 SMT8 10Kx4 1/16W 5% None
61 JCE2A#
61 JCE1A#

PWR_3VSTD PWR_1.5VMAIN
C370 None 1uF 10V 1608 FZ
C371 1uF 10V 1608 FZ
C372 1uF 10V 1608 FZ
GND1

M13

12 1.5VIN1
14 1.5VIN2
2 3.3VIN1
4 3.3VIN2
17 AUXIN

1.5VOUT1 11
1.5VOUT2 13
3.3VOUT1 3
3.3VOUT2 5
AUXOUT 15

PWR_1.5VPEC PWR_3.3VPECAUX
PWR_3.3VPEC
D10 RB521-S30 None

29,61 CPPE# → 10 CPPE#(PU)
61 CPUSB# → CPUSB# → 9 CPUSB#(PU)
PWR_3VMAIN → 1 STBY#(PU)
PERST# 8 → PECARD_RST# 61
RCLKEN(OD) 18 → O2_CLKEN 34
20 SHDN#(PU)
OC#(OD) 19
SYSRST#(PU) 6
NC 16
GND 7 → GND1
PU: IntPU to AUXIN

OZ27C10-B1
CA46710-0077

PWR_3VSTD
M72 NL17SZ08XV5
4,36,63,76,91 A_RST#_C
29,34 NEWCARD_RST#
C1196 0.1uF 10V RK
GND1

PWR_3VSTD
C374 1uF 10V 1608 FZ
C375 0.1uF 10V RK
GND1 GND1
1.5A

PWR_5VSTD
1.5A
C378 1uF 10V 1608 FZ
C379 0.1uF 10V RK
GND1 GND1

M14
3 3.3V
4 3.3V
5 5V
6 5V
9 12V
VCC 11
VCC 12
VCC 13
VPP 10
1 VCC5#
2 VCC3#
14 VPP_VCC
15 VPP_PGM
16 SHDN#
7 GND
OC# 8

57 VCCD0#
57 VCCD1#
4,57,75 PCIC_GBRST#

OZ2211SN-C1
CA46710-0020
GND1

PWR_3VSTD
RM121 SMT8 100Kx4 1/16W 5%
CPUSB#
CPPE#
34,61 PECARD_CLKREQA#
34 O2_CLKEN
PWR_3.3VPEC
PWR_3VMAIN
R163 100K 1/16W 5% None GND1

PWR_PCMVCC0
1.0A
PWR_PCMVPP0
R164 0 1/16W 1608 None

PCIC-2

注 In case of using cardbus card, JAA16 are clock signal, these clock need have GND1 guard.

Place this clock dumping register near PCIC.

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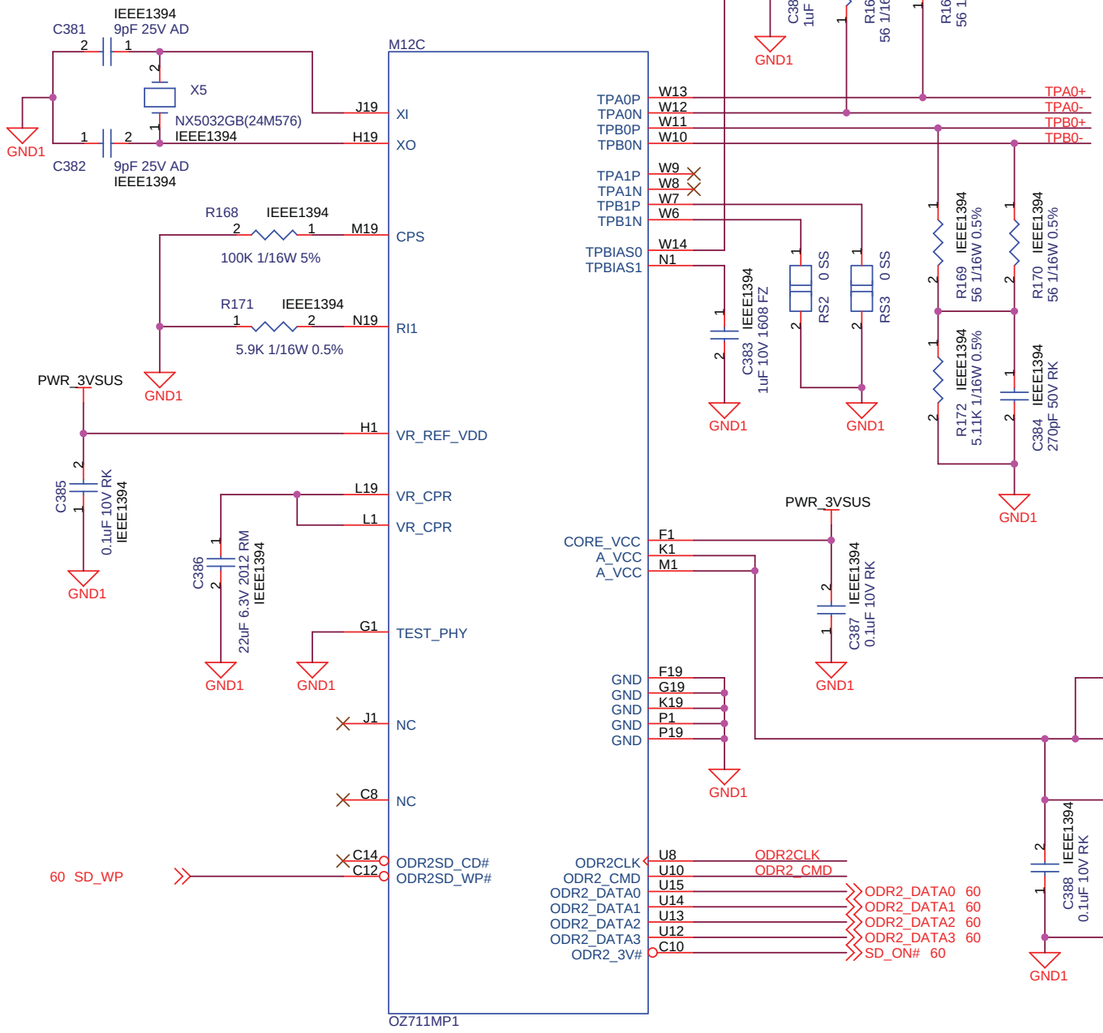
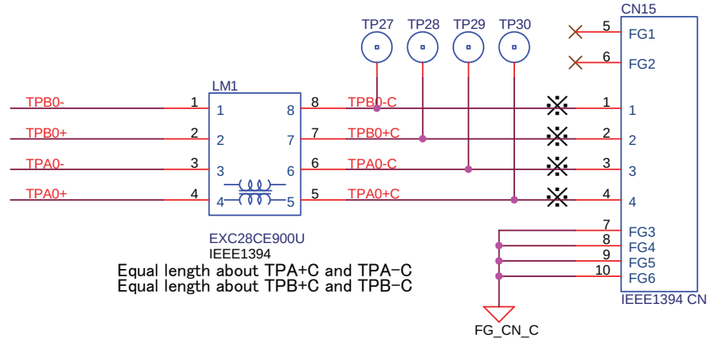
Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE: VB313AA
DRAW. No.: C1CP302570-X2
CAST:
FUJITSU LTD.
Sheet 58 / 93

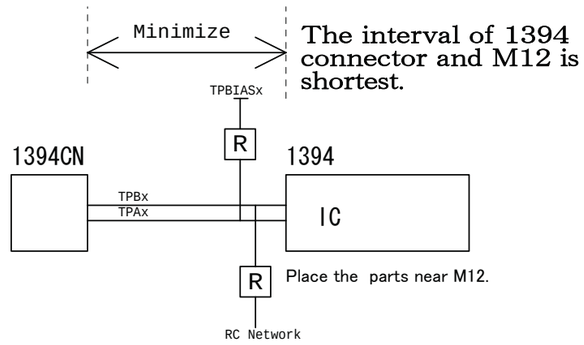
Dolphin

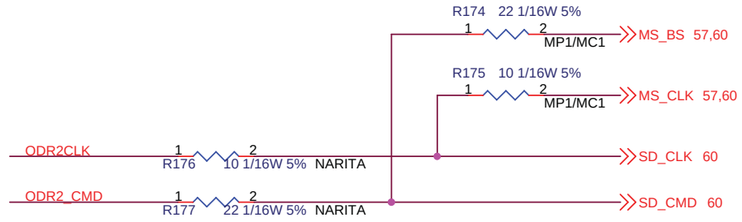


Place Testpad for IEEE1394 without stab.



Equal length about TPA+C and TPA-C
Equal length about TPB+C and TPB-C





IEEE1394 CN

Fujitsu
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						TITLE	VB313AA
						DRAW. No.	C1CP302570-X2
						CAST	
Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.	Sheet 59 / 93
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa		

Dolphin

57 MS_DATA3
57 MS_DATA2
57 MS_DATA1
57 MS_DATA0

PWR_3VSUS
R180 470K 1/16W 5%
None MS_DET#

PWR_MS

CN16

57 XD_DATA7
57 XD_DATA6
57 XD_DATA5
57 XD_DATA4

57 XD_WP
57 XD_WE#
57,59 MS_BS
57,59 MS_CLK
57 MS_DET#
57 XD_RE#
57 XD_R/B#
57 XD_DET#

43	VCC2		
38	VCC1		
37	D7		
36	D6		
35	D5		
34	D4		
33	D3		
32	D2		
31	D1		
30	D0		
29	GND2		
28	WP#		
27	WE#		
26	ALE		
25	CLE		
24	CE#		
23	RE#		
22	R/B#		
10	CD for xD		
21	GND		

xD

43	39	
38	40	
37	41	
36	8	SD
35	7	
34	6	
33	5	
32	4	
31	11	MS
30	12	SD
29	13	MS
28	14	
27	15	SD
26	16	MS
25	17	
24	18	SD
23	19	MS
22	20	
10	3	SD
21	2	MS
	1	
	9	SD
		MS
		SD

42

SD/MS/xD(Yamaichi)

C392 1uF 10V 1608 FZ

GND
42
GND1

PWR_3VSUS
R181 100K 1/16W 5%
None SD_DET#

PWR_MS
R182 100K 1/16W 5%
None SD_CMD

PWR_MS

39	WP SW	
40	COMMON	
41	CD SW	
8	DAT1	DAT1
7	DAT0	DAT0
6	VSS2	
11	VSS	
5	CLK	* SD_CLK 59
12	BS	* MS_BS 57,59
13	DATA1	
4	VDD	
14	SDIO/DATA0	
15	DATA2	
3	VSS1	
16	INS	MS_DET# 57
17	DATA3	
2	CMD	SD_CMD 59
18	SCLK	* MS_CLK 57,59
19	VCC	
1	CD/DAT3	DAT3
20	VSS	
9	DAT2	DAT2

C393 1uF 10V 1608 FZ
C394 1uF 10V 1608 FZ

GND1

R178 10 1/16W 5% MP1/MC1
R179 10 1/16W 5% NARITA

ODR_WP 57
SD_WP 59
SD_DET# 57

M15

DAT0	2	1A	1B 3 SD_DATA0 57
DAT3	5	2A	2B 6 SD_DATA3 57
DAT1	9	3A	3B 8 SD_DATA1 57
DAT2	12	4A	4B 11 SD_DATA2 57
	1	1OE#	VCC 14
	4	2OE#	
	10	3OE#	
	13	4OE#	GND 7

SN74CBT3125PW/FST3125MTC
MP1/MC1

PWR_5VSTD
C391 0.1uF 10V RK
GND1

59 ODR2_DATA0
59 ODR2_DATA1
59 ODR2_DATA2
59 ODR2_DATA3

RM47
8 SMT8

4	5	DAT0
3	6	DAT1
2	7	DAT2
1	8	DAT3

NARITA
22x4 1/16W 5%

0.5A

PWR_3VSTD

Q11
SI2305DS-T1-E3

R183 470K 1/16W 5%
C395 0.1uF 10V RK

R185 47K 1/16W 5%

D11
57 MS/XD_ON#
1SS400

D12
59 SD_ON#
1SS400
NARITA

PS2
nanoSMDC110F
1510P102

TP36

C396 1uF 10V 1608 FZ
R184 150K 1/16W 5% None

GND1

3.3V 0.5A

PWR_MS

MS/SD/XD

Fujitsu
Proprietary & Confidential

Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE: **VB313AA**

DRAW. No.: C1CP302570-X2

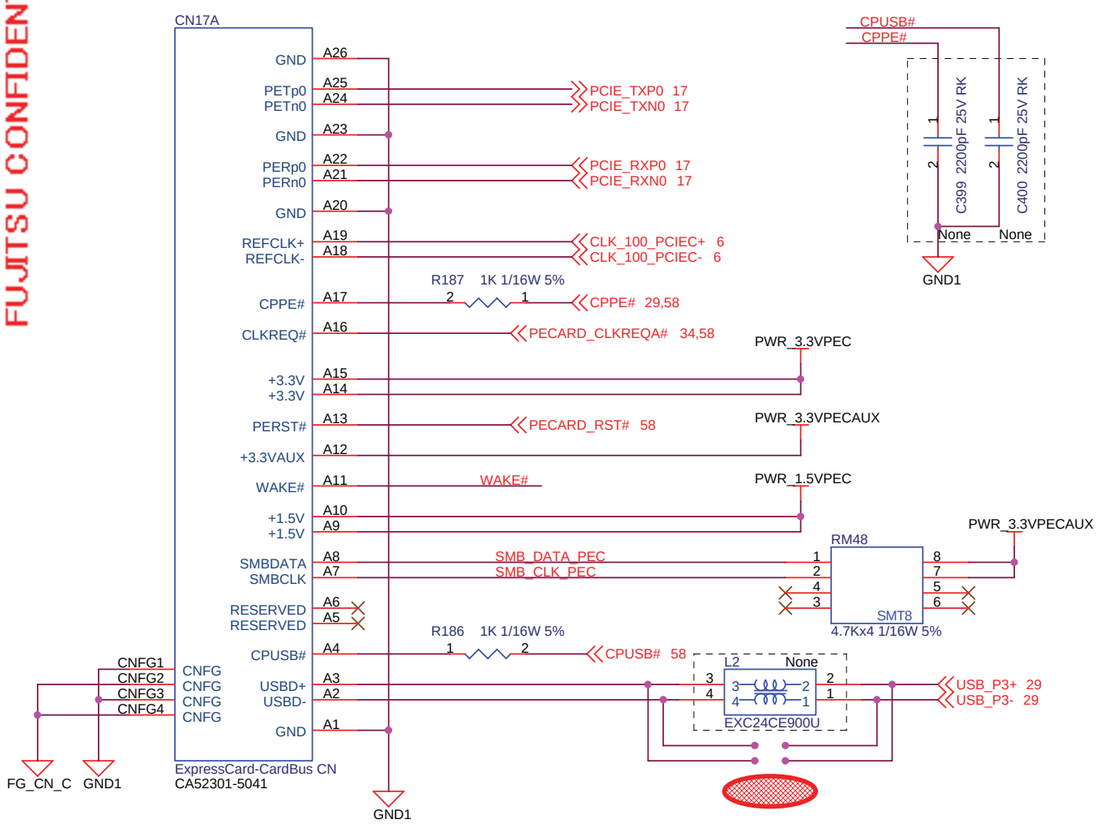
CAST

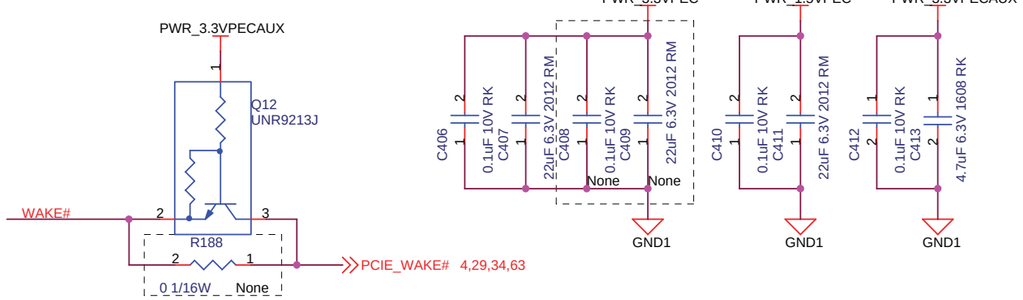
FUJITSU LTD.

Sheet 60 / 93

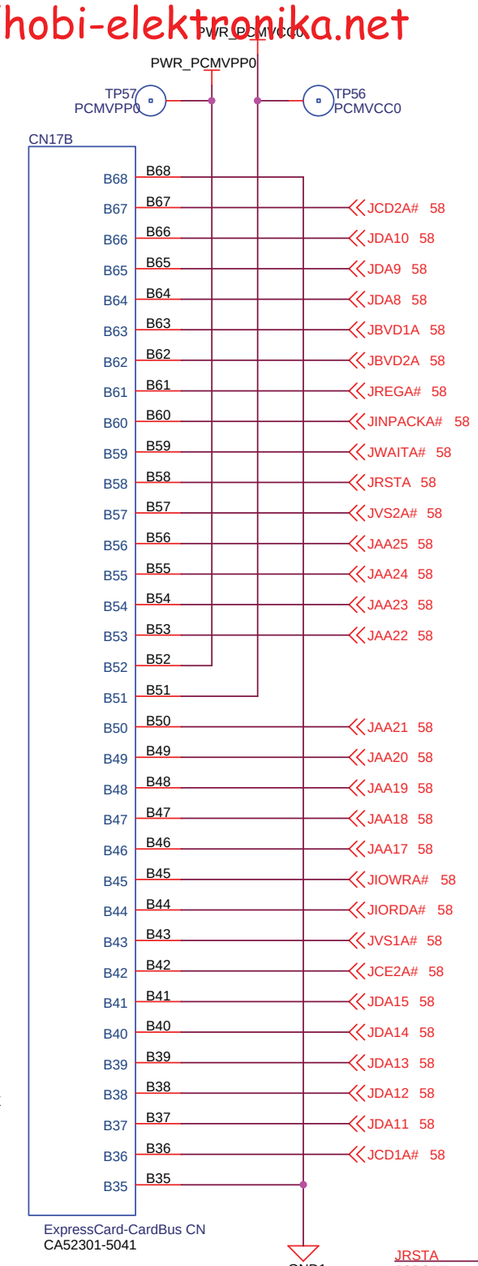
Dolphin

SLOT #1

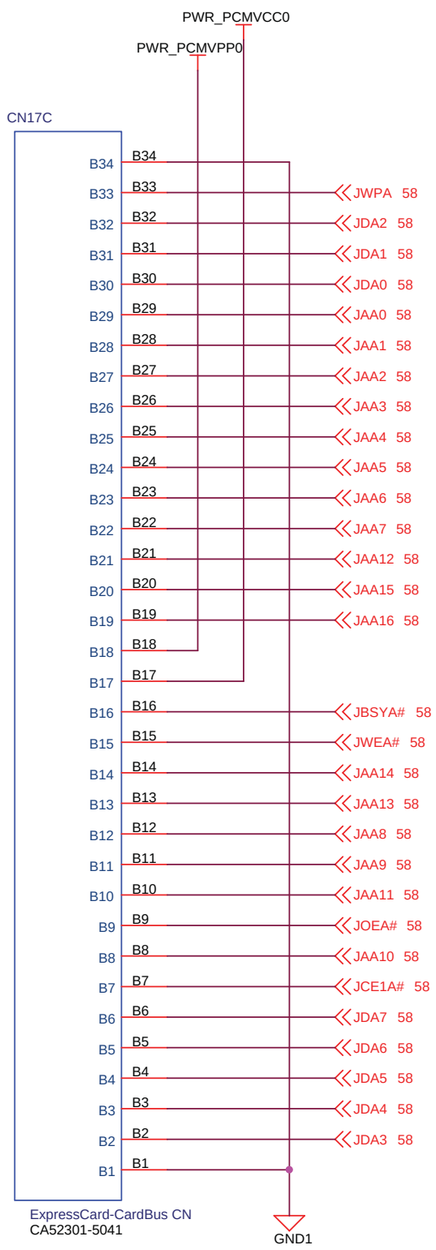




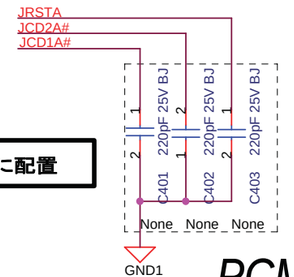
05/11
部品変更
Q12 ： DTC144EE(CA47001-0312) -->
DTC144EETL(CA471005016)

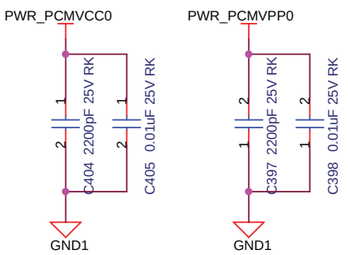


SLOT #0



出来る限りSlotのPinそばに配置





PCMCIA SLOT

FGはGND1に接続してください。

A・Bスロットとも JCE1x#, JCE2x#, JOEx#, JWEx#は、データバスとの平行配線とならないように配線すること。

Express Card SLOT
PCMCIA SLOT
PCB

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Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE: VB313AA
DRAW. No.: C1CP302570-X2
CAST:
FUJITSU LTD.
Sheet 61 / 93

FUJITSU CONFIDENTIAL Dolphin

2mm MAX(Peak) 1A

PWR_3VMAIN
R189 2 1 10K 1/16W 5% None
PWR_3VMINIC_AUX
R190 2 1 10K 1/16W 5%

FL203 2 1 BLM18PG181SN1 180ohm 1500mA
PWR_3VMAIN

2mm PWR_1.5VMAIN MAX(Peak) 500mA
1mm PWR_3VMINIC_AUX MAX(Peak) 330mA

CN18

4,54 WAKE_MINIC#	1	WAKE#	3.3V 2
56 BT_DATA_CN	3	Reserved**	VSS 4
56 BT_CHCLK_CN	5	Reserved**	1.5V 6
6 PLL_CLKREQB#	7	CLKREQ#	UIM_PWR 8
	9	VSS	UIM_DATA 10
6 CLK_100_MINICARD-	11	REFCLK-	UIM_CLK 12
6 CLK_100_MINICARD+	13	REFCLK+	UIM_RESET 14
	15	VSS	UIM_VPP 16
		Mechanical Key	
	17	Reserved***	VSS 18
	19	Reserved***	W_DISABLE# 20
	21	VSS	PERST# 22
17 PCIE_RXN3	23	PERn0	3.3Vaux 24
17 PCIE_RXP3	25	PERp0	VSS 26
	27	VSS	1.5V 28
	29	VSS	SMB_CLK 30
17 PCIE_TXN3	31	PETn0	SMB_DATA 32
17 PCIE_TXP3	33	PETp0	VSS 34
	35	VSS	USB_D- 36
	37	Reserved*	USB_D+ 38
	39	Reserved*	VSS 40
	41	Reserved*	LED_WWAN# 42
	43	Reserved*	LED_WLAN# 44
	45	Reserved*	LED_WPAN# 46
	47	Reserved*	1.5V 48
	49	Reserved*	VSS 50
	51	Reserved*	3.3V 52

*: 2nd PCI Express
**: Wireless Control
***: UIM Interface

PCI Express Mini Card CN
MINIC

GND1 GND1

WLAN_RFON 74
RS7 2 1 0 SS
A_RST#_B 4,37,48,71,74,76
A_RST#_MINIC 4
SMB_CLK_SB 6,23,24,29,38
SMB_DATA_SB 6,23,24,29,38

上記コイルはCNのPIN近くに配置すること。

FL204 2 1 BLM18PG181SN1 180ohm 1500mA
PWR_3VMAIN

2006.6.13
02版：FL203,FL204追加
CN18の各ピン直近に配置すること

これらのコンデンサはCN18の各電源PINの近くに配置すること。

PWR_3VMAIN
C414 MINIC 1uF 10V 1608 RK
None
C415 MINIC 0.1uF 10V RK
C416 MINIC 0.1uF 10V RK
C417 MINIC 0.1uF 10V RK
C418 MINIC 0.1uF 10V RK
GND1

PWR_3VMINIC_AUX
C419 MINIC 1uF 10V 1608 RK
None
C420 MINIC 0.1uF 10V RK
C421 MINIC 0.1uF 10V RK
GND1

PWR_1.5VMAIN
C422 MINIC 1uF 10V 1608 RK
None
C423 MINIC 0.1uF 10V RK
C424 MINIC 0.1uF 10V RK
C425 MINIC 0.1uF 10V RK
C426 MINIC 0.1uF 10V RK
C427 MINIC 0.1uF 10V RK
GND1

CN42
1 NC
2 NC
3 NC
4 NC
5 NC
6 NC
Mini Card Spacer
GND1

3.3V/0.3A 1mm
1.2mm
0.3A
PWR_3VSTD
PWR_3VMINIC_AUX
None R193 MINIC 0 1/16W
MINIC R195 470K 1/16W 5%
MINIC C428 0.01uF 50V 1608 RK
Q13 SI2305DS-T1-E3 MINIC
R196 47K 1/16W 5% MINIC
54,74 MINIC_ON
Q302A SSM6N15FU MINIC
GND1
4,54,74,76,85,88 DLY_SUSB#
Q302B SSM6N15FU MINIC
GND1

PWR_3VMAIN
PWR_3VMINIC_AUX
R192 None MINIC 0 1/16W
PWR_3VSUS
R194 None MINIC 0 1/16W

MiniCard CN

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Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE: VB313AA
DRAW. No.: C1CP302570-X2
CAST
FUJITSU LTD.
Sheet 62 / 93

FUJITSU CONFIDENTIAL

Dolphin

OnBoard LAN(Marvell)

M18 88E805X

Xtal: XTALI, XTALO

PCI Express: TX_P, TX_N, RX_P, RX_N, REFCLKP, REFCLKN, WAKEn, PERSTn/TSTPT

Media Dependent Interface(PHY): MDIP[0]/MDIN[0], MDIP[1]/MDIN[1], MDIP[2]/MDIN[2], MDIP[3]/MDIN[3]

EEPROM: VPD_CLK, VPD_DATA, SPI_DO, SPI_DI, SPI_CLK, SPI_CS

Analog(PHY): RSET, LOM_DISABLEn, VMAIN_AVLBL, VAUX_AVLBL, SWITCH_VCC, SWITCH_VAUX, CTRL18, CTRL12

TEST: TESTMODE

LED: LED_ACTn, LED_LINK10/100n, LED_LINK1000n, LED_LINKn

POWER: AVDDH(3.3V), AVDD_1, AVDD_2, AVDD_3, AVDD_4, VDDO_TTL_1, VDDO_TTL_2, VDDO_TTL_3, VDDO_TTL_4, VDD_1, VDD_2, VDD_3, VDD_4, VDD_5, VDD_6, VDD_7, VDD_8, VSS

NC: NC_1, NC_2, NC_3, NC_4, NC_5, NC_6, NC_7, NC_8, NC_9, NC_10

X13 K30-3C0(25M) CAN27-25M00000 None

X6 NX5032GB(25M) GLAN CAP80-25M00000

M17 M24C16-WDW6P GLAN

M20 NL17SZ08XV5

RM49 SMT8 10Kx4 1/16W 5% None

Q15 2SA1900QT100

Q16 2SA1900QT100

2SA1900 (B, C, E)

FL39 BLM18BD601SN1

FL40 BLM18BD601SN1

						TITLE	VB313AA
						DRAW. No.	C1CP302570-X2
							CAST
Rev.	Date	Design	Check	Appr.	Description		
Design	06/07/04	Mizukami	Check	Urita		FUJITSU LTD.	Sheet 63 / 93
				Appr.	Hasegawa		

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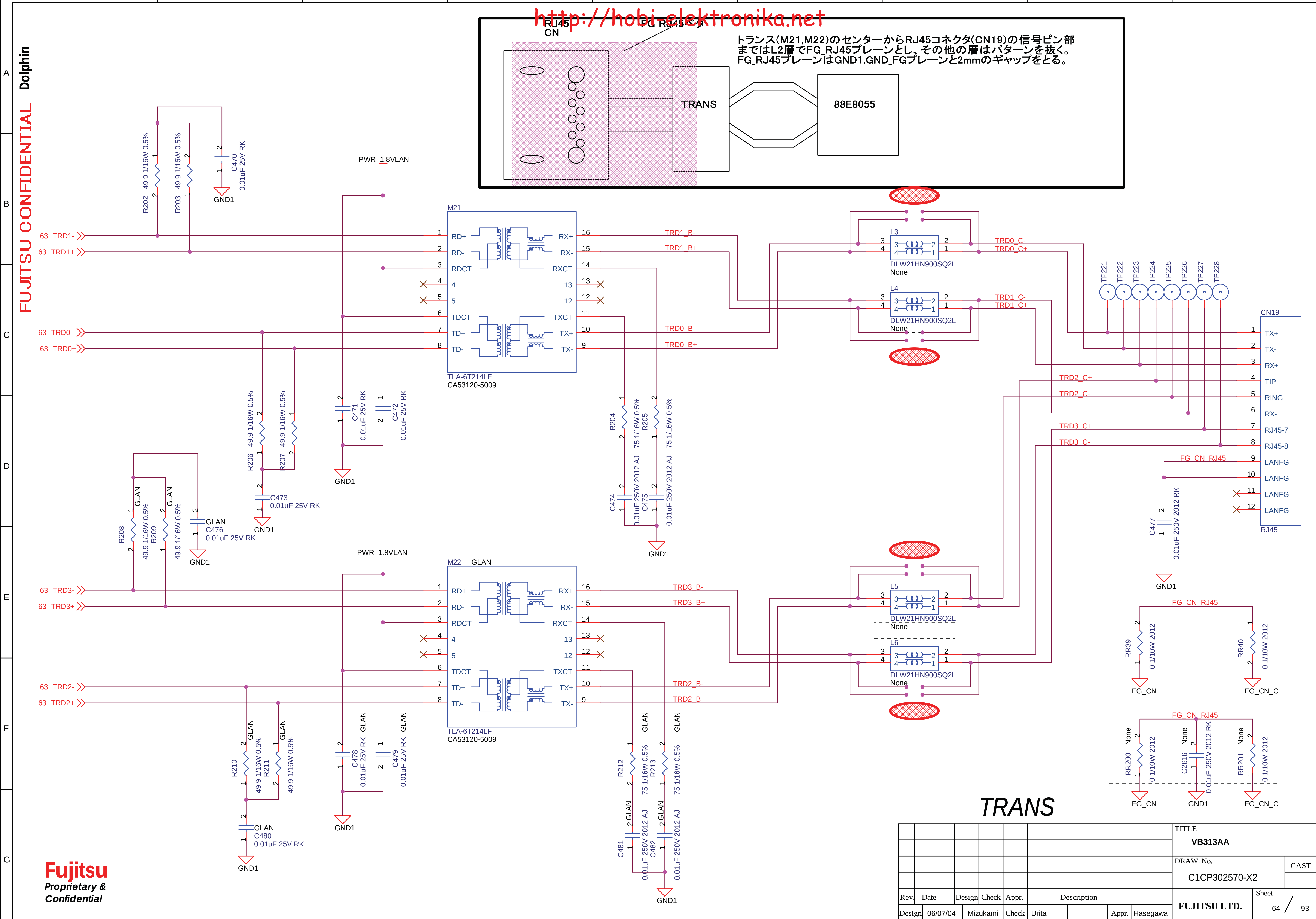

http://hobi-elektronika.net
Dolphin
FUJITSU CONFIDENTIAL
RJ45 CN
FG_RJ45
TRANS
88E8055
トランス(M21,M22)のセンターからRJ45コネクタ(CN19)の信号ピン部
まではL2層でFG_RJ45プレーンとし、その他の層はパターンを抜く。
FG_RJ45プレーンはGND1,GND_FGプレーンと2mmのギャップをとる。
63 TRD1-
63 TRD1+
63 TRD0-
63 TRD0+
63 TRD3-
63 TRD3+
63 TRD2-
63 TRD2+
R202 49.9 1/16W 0.5%
R203 49.9 1/16W 0.5%
C470 0.01uF 25V RK
GND1
PWR_1.8VLAN
M21
RD+
RD-
RDCT
TDCT
TD+
TD-
RX+
RX-
RXCT
TXCT
TX+
TX-
TLA-6T214LF
CA53120-5009
TRD1_B-
TRD1_B+
TRD0_B-
TRD0_B+
C471 0.01uF 25V RK
C472 0.01uF 25V RK
R206 49.9 1/16W 0.5%
R207 49.9 1/16W 0.5%
C473 0.01uF 25V RK
R204 75 1/16W 0.5%
R205 75 1/16W 0.5%
C474 0.01uF 250V 2012 AJ
C475 0.01uF 250V 2012 AJ
L3
L4
L5
L6
DLW21HN900SQ2L
None
TRD0_C-
TRD0_C+
TRD1_C-
TRD1_C+
TRD2_C+
TRD2_C-
TRD3_C+
TRD3_C-
TP221
TP222
TP223
TP224
TP225
TP226
TP227
TP228
CN19
TX+
TX-
RX+
TIP
RING
RX-
RJ45-7
RJ45-8
LANFG
RJ45
FG_CN_RJ45
C477 0.01uF 250V 2012 RK
R208 49.9 1/16W 0.5%
R209 49.9 1/16W 0.5%
GLAN
C476 0.01uF 25V RK
M22 GLAN
TRD3_B-
TRD3_B+
TRD2_B-
TRD2_B+
R210 49.9 1/16W 0.5%
R211 49.9 1/16W 0.5%
C480 0.01uF 25V RK
C478 0.01uF 25V RK
C479 0.01uF 25V RK
R212 75 1/16W 0.5%
R213 75 1/16W 0.5%
C481 0.01uF 250V 2012 AJ
C482 0.01uF 250V 2012 AJ
RR39 0 1/10W 2012
RR40 0 1/10W 2012
FG_CN
FG_CN_C
RR200 0 1/10W 2012
C2616 0.01uF 250V 2012 RK
RR201 0 1/10W 2012
TRANS
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Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE: VB313AA

DRAW. No.: C1CP302570-X2

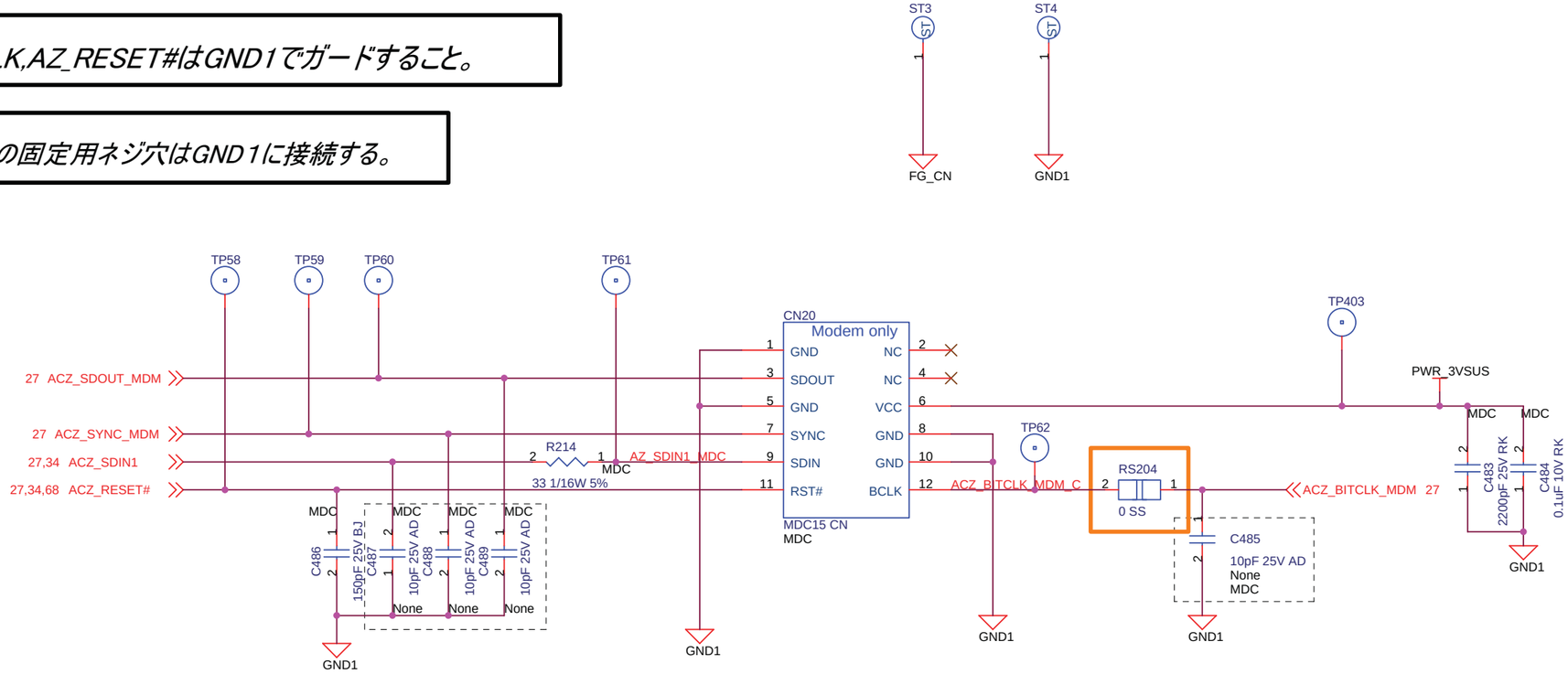
CAST

FUJITSU LTD.

Sheet 64 / 93

AZ_BITCLK,AZ_RESET#はGND1でガードすること。

モジュールの固定用ネジ穴はGND1に接続する。



2006.6.26
02版：RS204追加

MDC Modem

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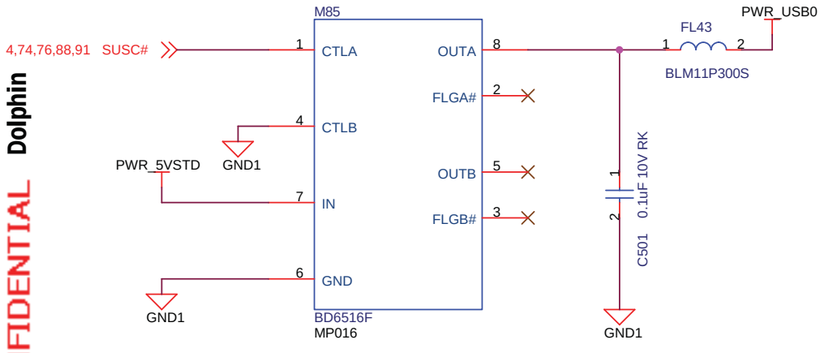
Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

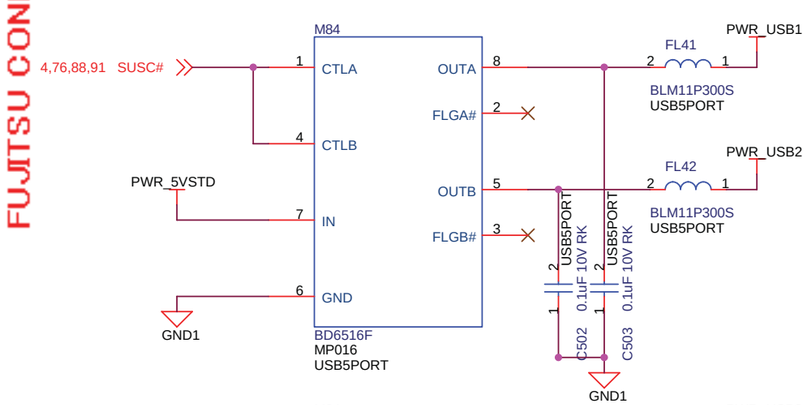
TITLE: **VB313AA**

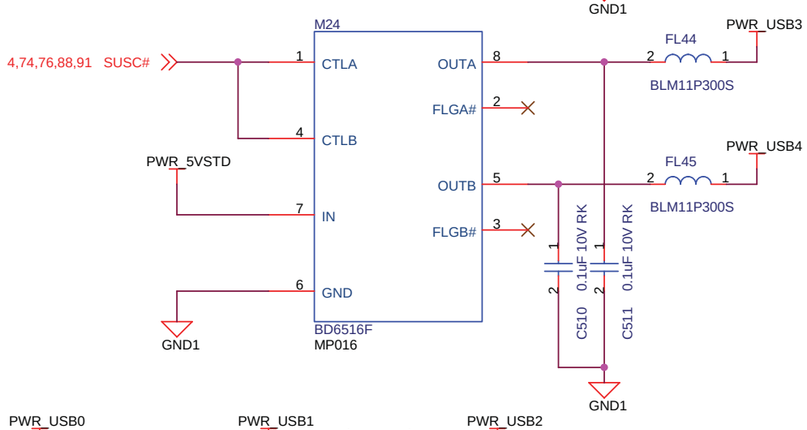
DRAW. No.: C1CP302570-X2 CAST

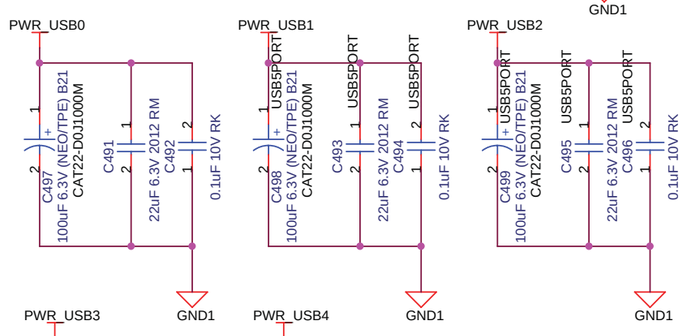
FUJITSU LTD.

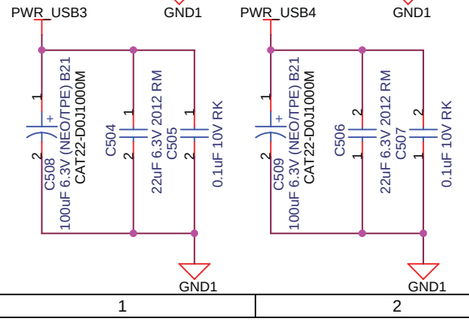
Sheet 65 / 93

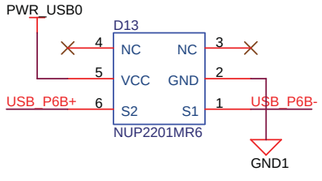


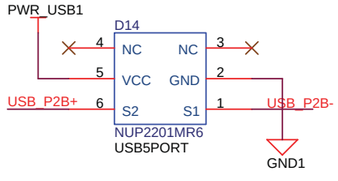


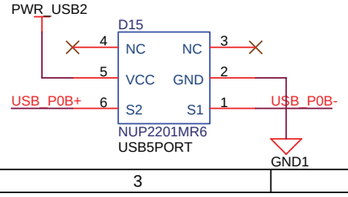


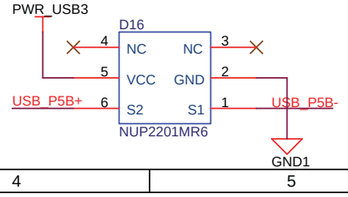


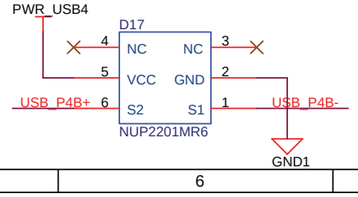


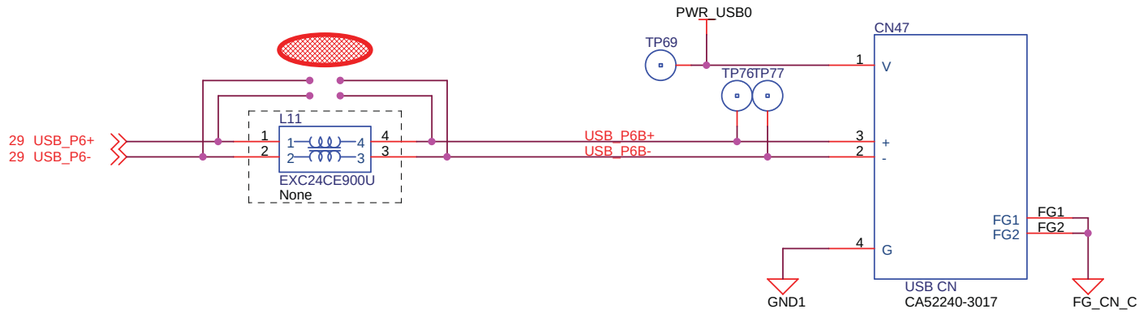


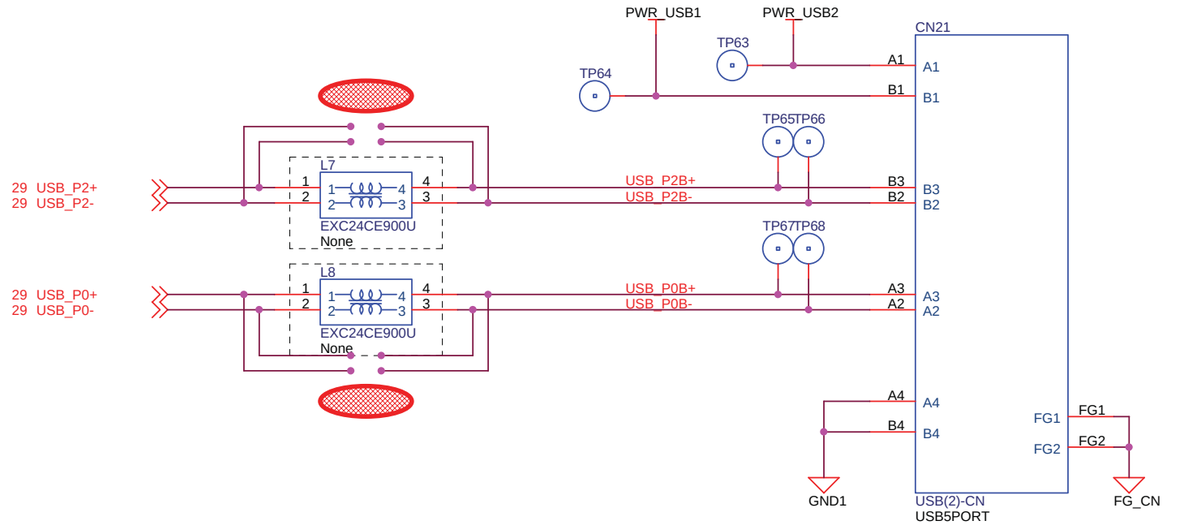


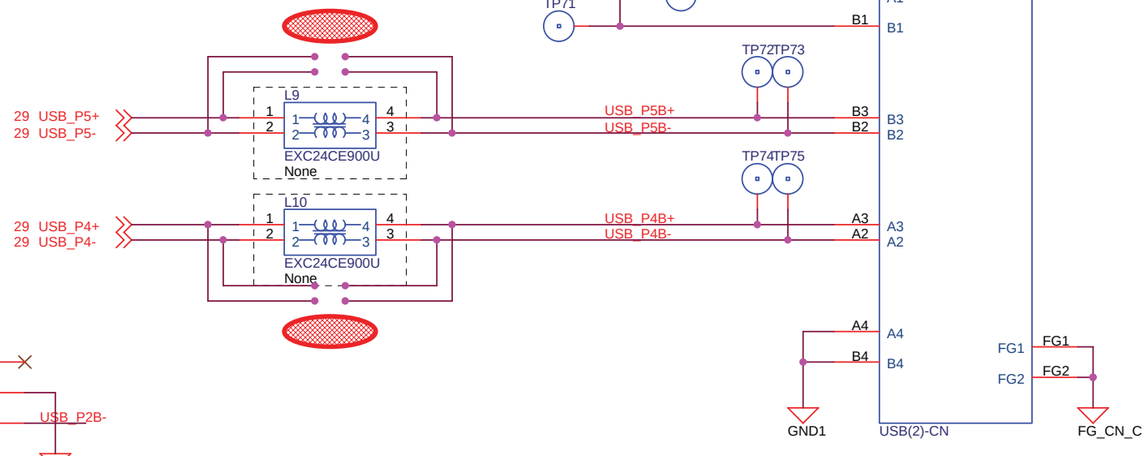




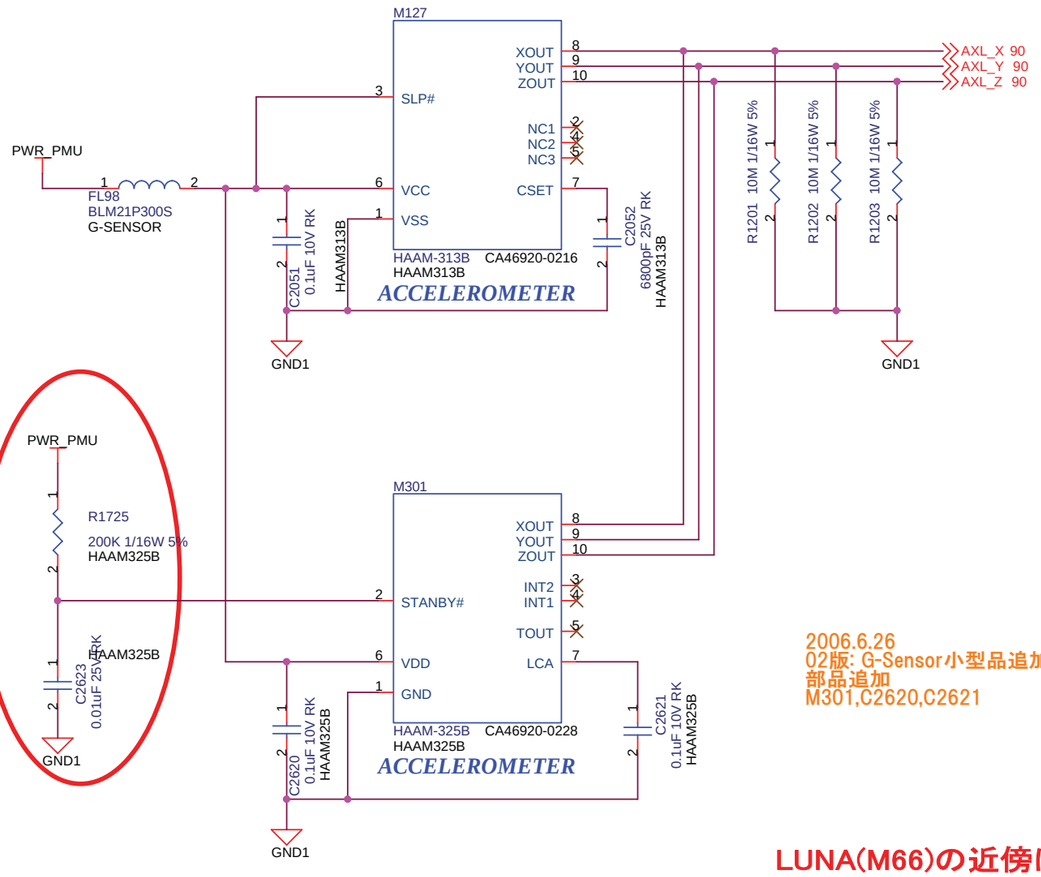








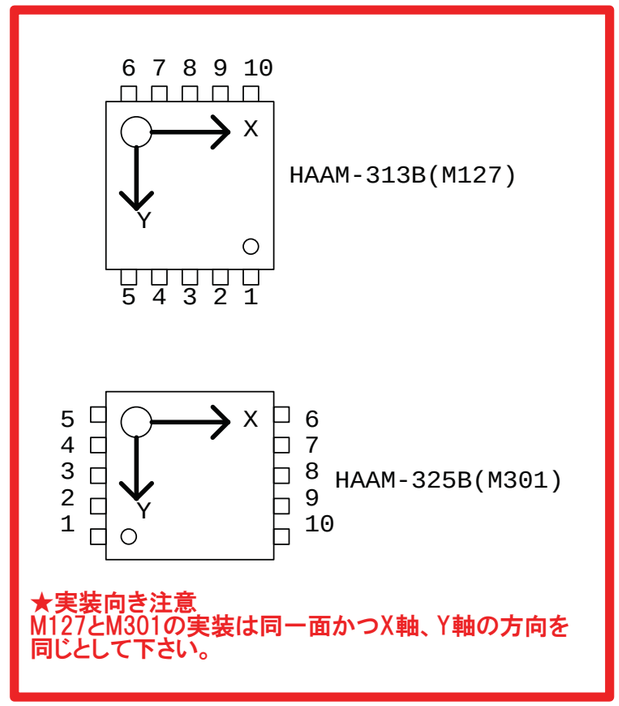
						TITLE	VB313AA
						DRAW. No.	C1CP302570-X2
						CAST	
Rev.	Date	Design	Check	Appr.	Description		
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa
						FUJITSU LTD.	Sheet 66 / 93



2006.7.4
02版: R1725、C2623追加

2006.6.26
02版: G-Sensor小型品追加
部品追加
M301,C2620,C2621

LUNA(M66)の近傍に配置



★実装向き注意
M127とM301の実装は同一面かつX軸、Y軸の方向を同じとして下さい。

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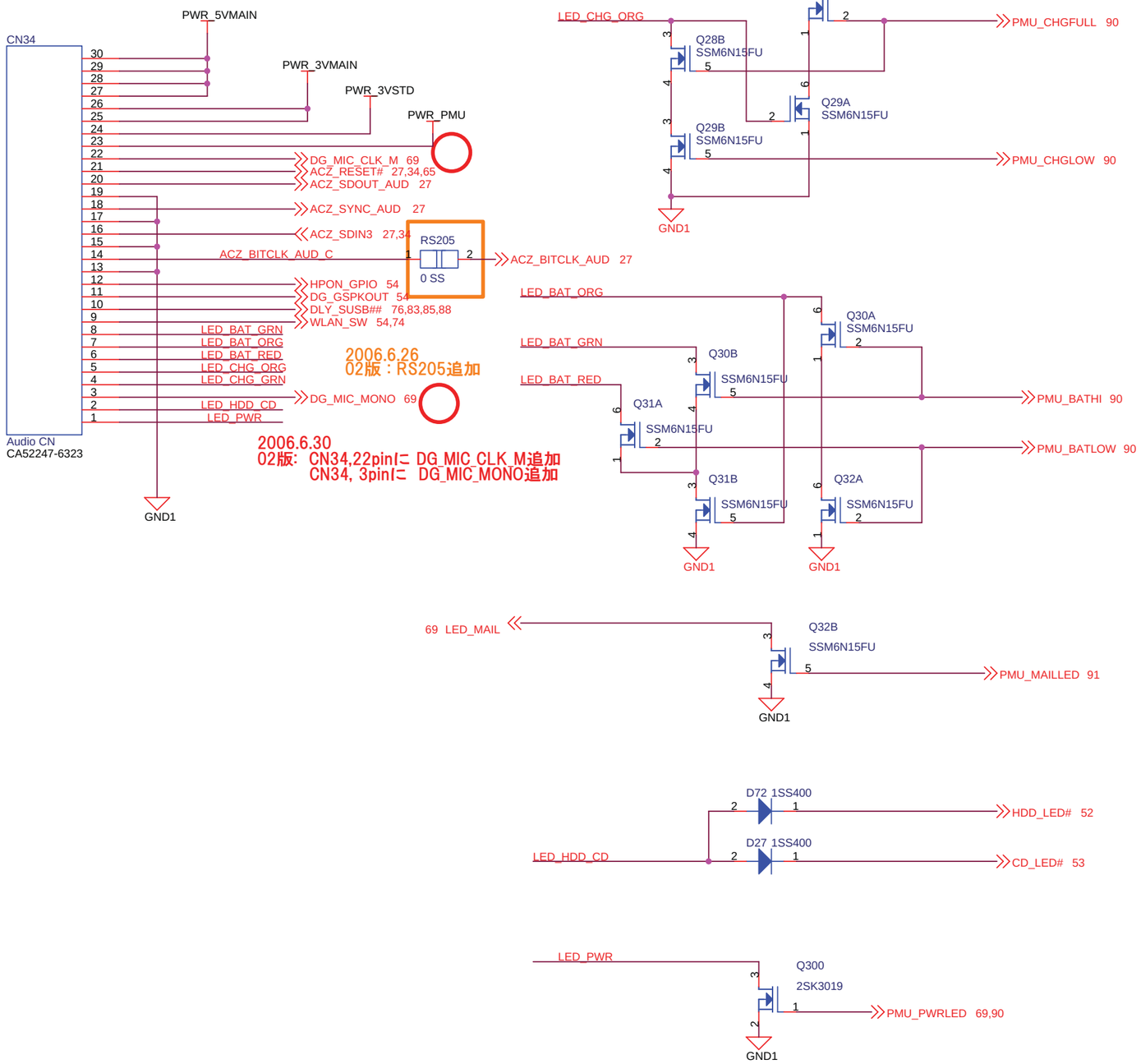
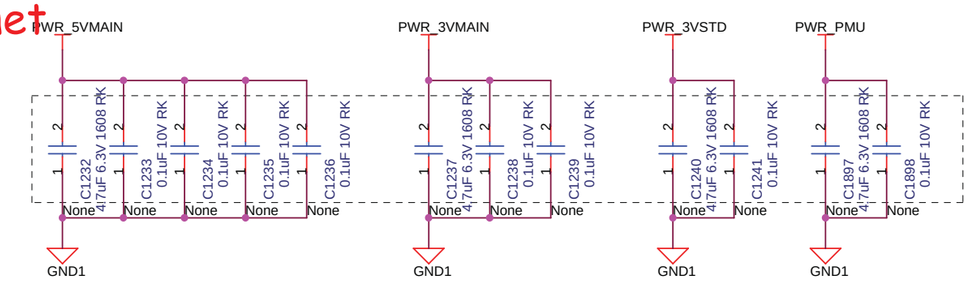
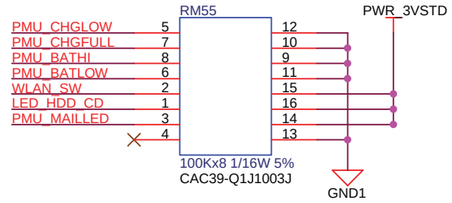
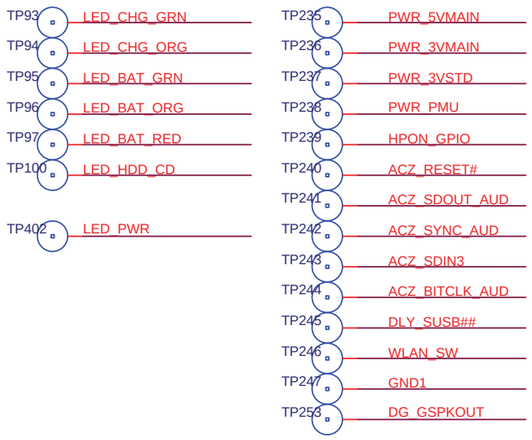
						TITLE	VB313AA
						DRAW. No.	C1CP302570-X2
						CAST	
Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.	Sheet 67 / 93
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa		

FUJITSU CONFIDENTIAL Dolphin









Audio/Statsu CN

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Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE: **VB313AA**
DRAW. No.: C1CP302570-X2
CAST:
FUJITSU LTD.
Sheet 68 / 93

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FUJITSU CONFIDENTIAL Dolphin

PWR_5VMAIN

D103 Num GREEN SML-412MWT86S(GREEN) — R1204 680 1/16W 5% — LED_NUM — Q303 2SK3019 — TP443 — PMU_NUM_LED 90

D104 Caps GREEN SML-412MWT86S(GREEN) — R1205 680 1/16W 5% — LED_CAPS — Q35A SSM6N15FU — TP444 — PMU_CAPS_LED 90

D105 Scr GREEN SML-412MWT86S(GREEN) — R1206 680 1/16W 5% — LED_SCR — Q35B SSM6N15FU — TP445 — PMU_SCR_LED 90

GND1

PWR_5VSTD

D97 GREEN SML311BBT(LED-BLUE) None — R661 150 1/16W 0.5% None — LED_PWR2 — Q304 2SK3019 — TP446 — PMU_PWRLED 68,90

GND1

2006.6.26
02版:
LEDにTP追加。TP443,TP444,TP445,TP446
(Fennecと配置の共通化をお願い致します)

PWR_3VSTD

RM119 SMT8 100Kx4 1/16W 5%
PMU_CAPS_LED
PMU_SCR_LED
PMU_NUM_LED

TP102 LED_NUM
TP103 LED_CAPS
TP104 LED_SCR
TP105 LED_PWR2

2006.6.26
02版: 電源ボタンにTP追加
(Fennecと配置の共通化をお願い致します)

TP442

SW1 SW

Q176 2SK3019

R302 1K 1/16W 5%

PWR_PMU

R301 100K 1/16W 5%

C701 0.1uF 10V RK

GND1

SUSSW# 4,54,91

2006.6.26
02版: 電源ボタン変更
CA49001-5370 --> CA49001-5119

PWR_PMU

R303 100K 1/16W 5%

R304 1K 1/16W 5%

LCDCL_SW# 2

C702 0.1uF 10V RK

GND1

LCDCL# 54,90

M49E SN74LV14APW PMU

M11A SN74LV05ADGV PMU OD

SB_LCDCL# 4,29,34

LCDCL 90

PWR_3VSTD

RM200 SMT8 100Kx4 1/16W 5%

LED_PLAYER
PMU_APPMODE

ROW#0 SW_Mode
ROW#1 SW_Appli-A
ROW#2 SW_Appli-B
ROW#3 SW_Internet
ROW#4 SW_Mail
ROW#5 SW_Vol_Down
ROW#6 Unused
ROW#7 SW_Vol_up

CN28 Button CN CA52300-3419

PWR_3VMAIN PWR_PMU PWR_5VMAIN PWR_5VSTD

C2622 0.1uF 10V RK None
C2617 0.1uF 10V RK None
C2618 0.1uF 10V RK None
C2619 0.1uF 10V RK None

OPE_ROW#0
OPE_ROW#1
OPE_ROW#2
OPE_ROW#3
OPE_ROW#4
OPE_ROW#5
OPE_SCANX#
OPE_SCANY#

LED_MAIL 68

LCDCL_SW#
LED_APPLI
LED_PLAYER

R1718 0 1/16W
R1719 0 1/16W

DG_MIC_CLK_M 68

DG_MIC_MONO 68

GND1

2006.6.30
02版: R1718-1721,C2622追加

2006.7.04
R1720,R1721をMainボードからAudioボードへ移動

OPE_ROW#1 — R1704 0 1/16W APPLIx4
OPE_ROW#2 — R1705 0 1/16W APPLIx4
OPE_ROW#5 — R1706 0 1/16W APPLIx2
OPE_ROW#7 — R1707 0 1/16W APPLIx2

OPE_ROW#0
OPE_ROW#3
OPE_ROW#4
OPE_ROW#6

CM13 100pFx4 50V BK None
CM14 100pFx4 50V BK None

GND1

RM53 1Kx8 1/16W 5% CAC39-Q1J1001J

ROW#0
ROW#1
ROW#2
ROW#3
ROW#4
ROW#5
ROW#6
ROW#7

ROW#[0:7] 70,91

RM54 SMT8 1Kx4 1/16W 5%

OPE_SCANX#
OPE_SCANY#

SCANX# 91
SCANY# 91

LED_APPLI
LED_PLAYER

Q301A SSM6N15FU
Q301B SSM6N15FU

GND1

PMU_APPMODE 90

TP81 OPE_ROW#0
TP82 OPE_ROW#1
TP83 OPE_ROW#2
TP84 OPE_ROW#3
TP85 OPE_ROW#4
TP86 OPE_ROW#5
TP88 OPE_ROW#6
TP89 OPE_ROW#7

TP409 LED_APPLI
TP410 LED_PLAYER
TP90 OPE_SCANX#
TP91 OPE_SCANY#
TP87 LCDCL_SW#
TP108 GND1
TP101 LED_MAIL

[Button CN]

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Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE: VB313AA
DRAW. No.: C1CP302570-X2
CAST
FUJITSU LTD.
Sheet 69 / 93

Dolphin

	SHIPID		
	ID0	ID1	ID2
OYA	0	0	0
UK	0	0	1
US	0	1	0
JP	0	1	1

0 CLM#0
2 CLM#1
4 CLM#2
6 CLM#3
8 CLM#4
0 CLM#5
2 CLM#6
4 CLM#7
TP126 CLM#8
TP128 CLM#9

TP111 CLM#10
TP113 CLM#11
TP115 CLM#12
TP117 CLM#13
TP119 CLM#14
TP252 CLM#15
TP123 ROW#0
TP125 ROW#1
TP127 ROW#2
TP129 ROW#3
TP130 ROW#4
TP131 ROW#5
TP132 ROW#6
TP133 ROW#7
TP134 KSHIP_ID0
TP135 KSHIP_ID1
TP136 KSHIP_ID2

TP109
PWR_5VMAIN
R305 1K 1/16W 5%

CN29
ID0 30 KSHIP_ID0 54
ID1 29 KSHIP_ID1 54
ID2 28 KSHIP_ID2 54
ID-C 27 KB_ID
NC 26
NC 25
NC 24 CLM#15
UP0 23 CLM#0
UP1 22 CLM#1
UP2 21 CLM#2
UP3 20 CLM#3
UP4 19 CLM#4
UP5 18 CLM#5
UP6 17 CLM#6
LOW0 16 ROW#0
LOW1 15 ROW#1
LOW2 14 ROW#2
LOW3 13 ROW#3
LOW4 12 ROW#4
LOW5 11 ROW#5
LOW6 10 ROW#6
LOW7 9 ROW#7
UP7 8 CLM#7
UP8 7 CLM#8
UP9 6 CLM#9
UP10 5 CLM#10
UP11 4 CLM#11
UP12 3 CLM#12
UP13 2 CLM#13
UP14 1 CLM#14
INTE K/B

CLM#[0:15] 91
ROW#[0:7] 69,91

69,91 ROW#3
69,91 ROW#2
69,91 ROW#1
69,91 ROW#0
CM16
100pFx4 50V BK
GND1

69,91 ROW#4
69,91 ROW#6
69,91 ROW#5
69,91 ROW#7
CM17
100pFx4 50V BK
GND1

91 CLM#0
91 CLM#1
91 CLM#2
91 CLM#3
CM101
100pFx4 50V BK
GND1

91 CLM#4
91 CLM#5
91 CLM#6
91 CLM#7
CM102
100pFx4 50V BK
GND1

91 CLM#8
91 CLM#9
91 CLM#10
91 CLM#11
CM103
100pFx4 50V BK
GND1

91 CLM#12
91 CLM#13
91 CLM#14
91 CLM#15
CM104
100pFx4 50V BK
GND1

KB/Pointing-CN

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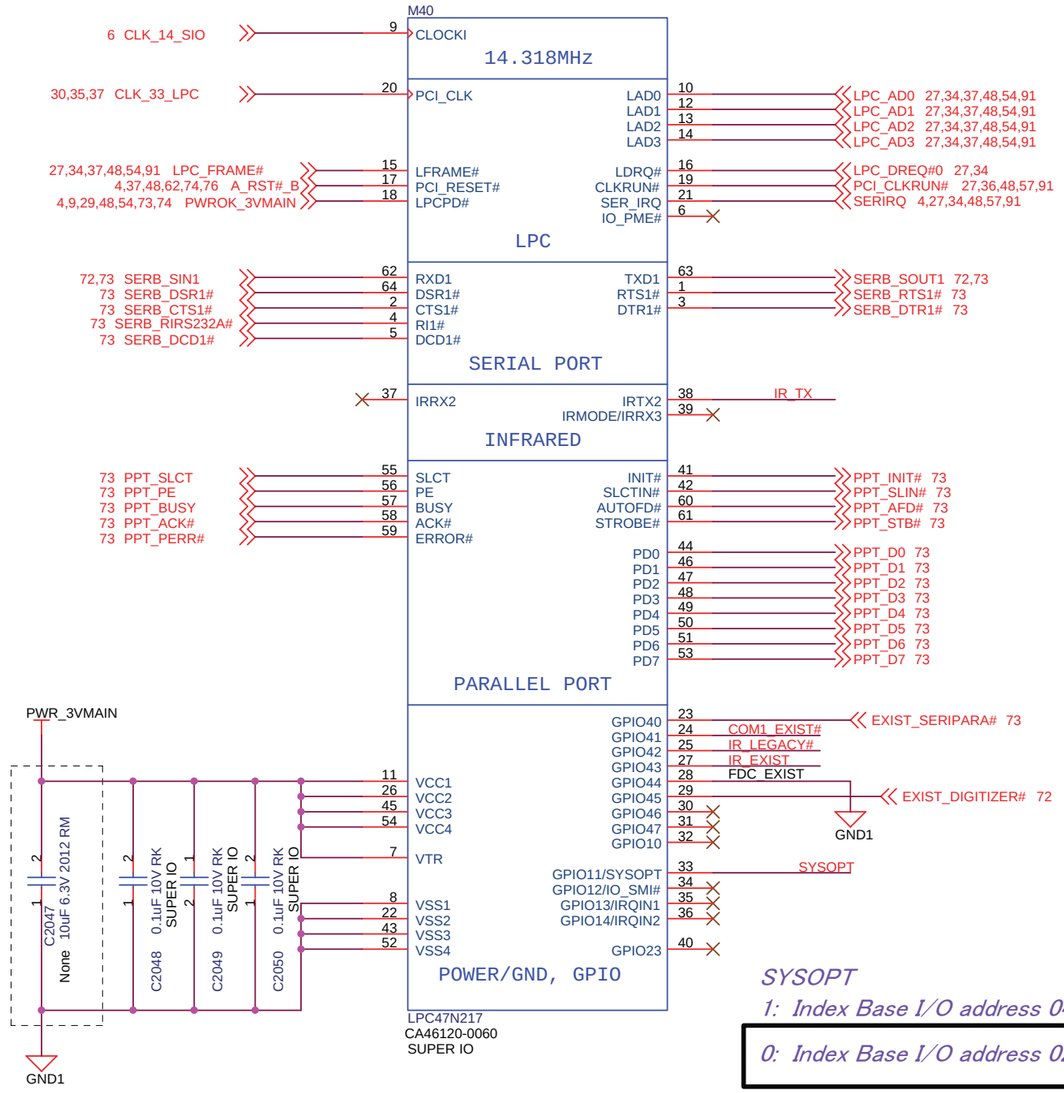
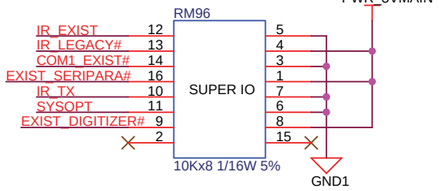
Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE: **VB313AA**
DRAW. No.: C1CP302570-X2
CAST:
FUJITSU LTD.
Sheet 70 / 93





SYSOPT

1: Index Base I/O address 04Eh

0: Index Base I/O address 02Eh

本ページの抵抗・コンデンサはKONA付近に配置すること。

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Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

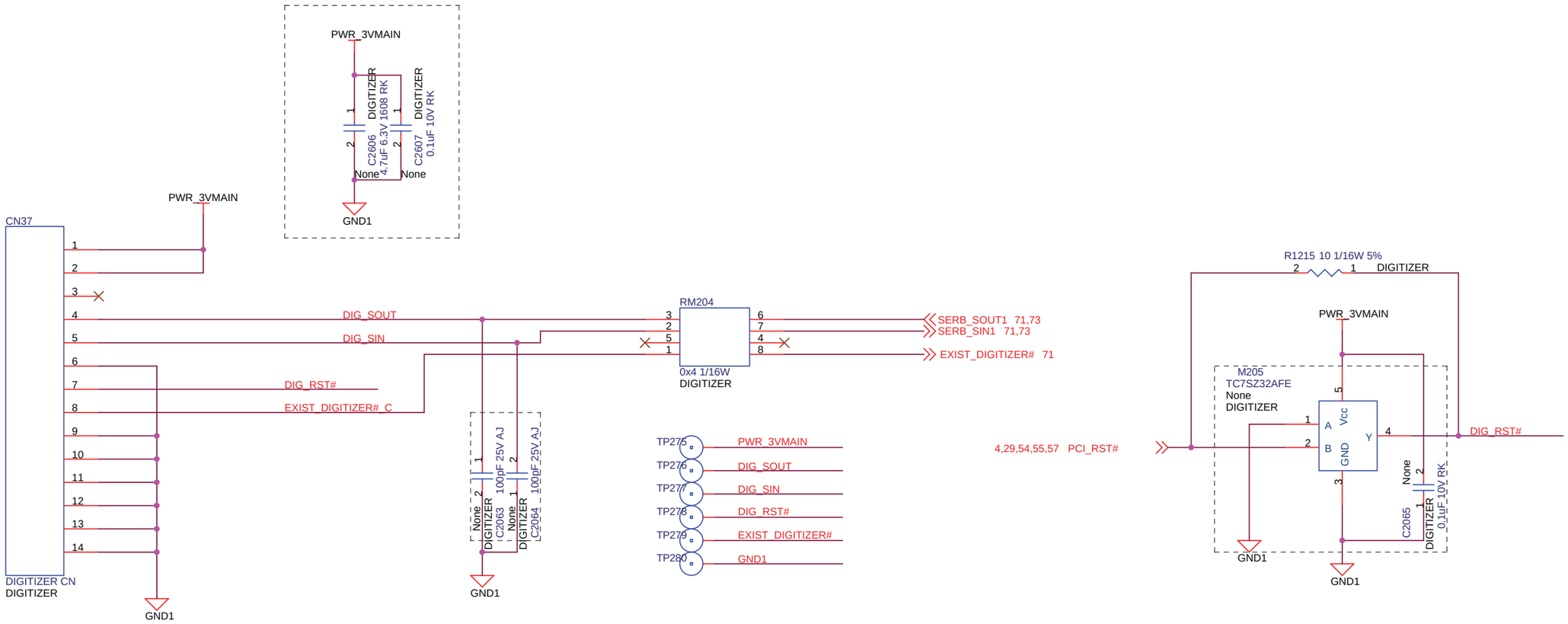
TITLE: **VB313AA**

DRAW. No.: C1CP302570-X2 CAST

FUJITSU LTD.

Sheet 71 / 93

Dolphin



DIGITIZER CN

Fujitsu
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Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE: **VB313AA**

DRAW. No.: C1CP302570-X2

CAST

FUJITSU LTD.

Sheet 72 / 93

Dolphin

TP413 PWROK_3VMAIN
TP414 PPT_STB#
TP415 PPT_D0
TP416 PPT_D1
TP417 PPT_D2
TP418 PPT_D3
TP419 PPT_D4
TP420 PPT_D5
TP421 PPT_D6
TP422 PPT_D7
TP423 PPT_BUSY
TP424 PPT_PE
TP425 PPT_ACK#
TP426 PPT_SLCT
TP427 PPT_AFD#
TP428 PPT_PERR#
TP429 PPT_INIT#
TP430 PPT_SLIN#
TP431 SERB_RTS1#_C
TP432 SERB_DTR1#_C
TP433 SERB_SOUT1_C
TP434 SERB_CTS1#_C
TP435 SERB_RIRS232A#_C
TP436 SERB_SIN1_C
TP437 SERB_DCD1#_C
TP438 SERB_DSR1#_C
TP439 EXIST_SERIPARA#_C
TP440 RI_RS232
TP441 PWR_3VSUS

CN32
SERI/PARA CN
Undecided
SERI/PARA

PWR_3VSUS
PWROK_3VMAIN 4,9,29,48,54,71,74
PPT_STB# 71
PPT_D0 71
PPT_D1 71
PPT_D2 71
PPT_D3 71
PPT_D4 71
PPT_D5 71
PPT_D6 71
PPT_D7 71
PPT_BUSY 71
PPT_PE 71
PPT_ACK# 71
PPT_SLCT 71
PPT_AFD# 71
PPT_PERR# 71
PPT_INIT# 71
PPT_SLIN# 71
SERB_RTS1#_C
SERB_DTR1#_C
SERB_SOUT1_C
SERB_CTS1#_C
SERB_RIRS232A#_C
SERB_SIN1_C
SERB_DCD1#_C
SERB_DSR1#_C
RI_RS232 55
GND1

RM203
10x8 1/16W 5%
SERI/PARA
SERB_RTS1# 71
SERB_DTR1# 71
SERB_SOUT1 71,72
SERB_CTS1# 71
SERB_RIRS232A# 71
SERB_SIN1 71,72
SERB_DCD1# 71
SERB_DSR1# 71

EXIST_SERIPARA#_C
R1711
0 1/16W
SERI/PARA
EXIST_SERIPARA# 71

PWR_5VMAIN
D35
1SS420
SUPER IO

RM61
4.7Kx8 1/16W 5%
SUPER IO
PPT_BUSY
PPT_D7
PPT_D6
PPT_D2
PPT_AFD#
PPT_D1
PPT_D3
PPT_STB#

RM62
4.7Kx8 1/16W 5%
SUPER IO
PPT_ACK#
PPT_D0
PPT_D5
PPT_D4
PPT_PERR#
PPT_INIT#
PPT_PE
PPT_SLIN#

R310
4.7K 1/16W 5%
SUPER IO
PPT_SLCT

PWR_3VMAIN
RM59
10Kx8 1/16W 5%
CAC39-Q1J1002J
SERB_DSR1#
SERB_DCD1#
SERB_SIN1
SERB_RIRS232A#
SERB_CTS1#
RI_RS232
GND1

PWR_3VSUS
C2608 7uF 6.3V 1608 RK
C2609 0.1uF 10V RK
SUPER IO
None
None
GND1

04/28
部品追加：C2608, C2609

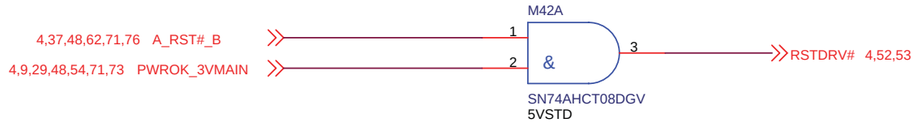
本ページの部品は、I/O-CNの近くに配置すること

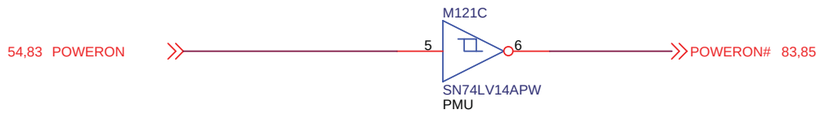
PARALLEL/SERIAL CN

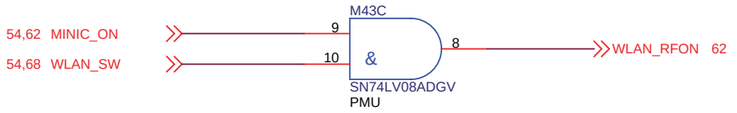
Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

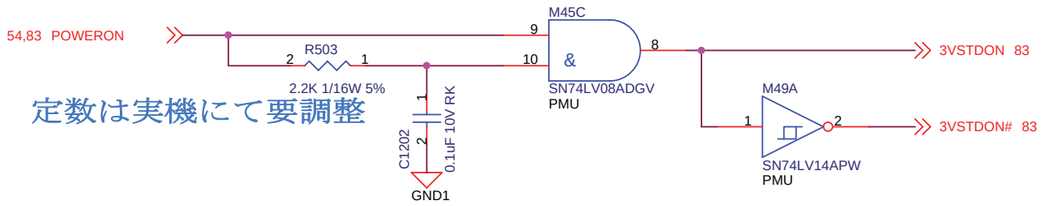
TITLE: VB313AA
DRAW. No.: C1CP302570-X2
CAST
FUJITSU LTD.
Sheet 73 / 93

Dolphin

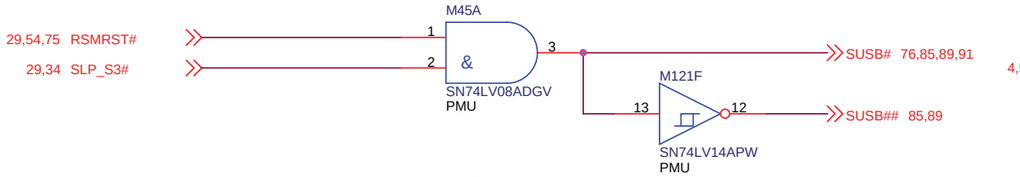


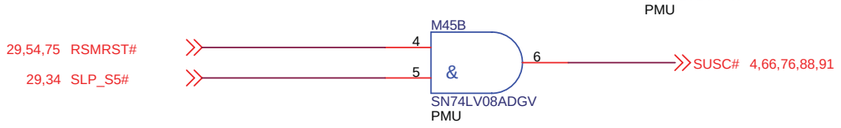


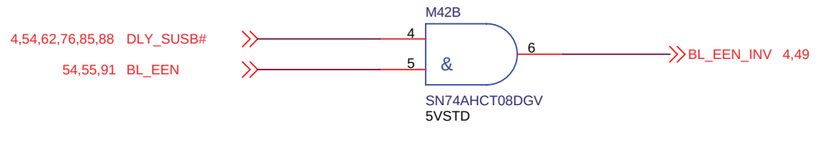




定数は実機にて要調整







A:71page
B:79page
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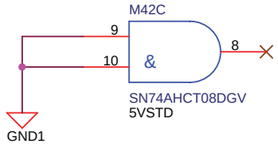
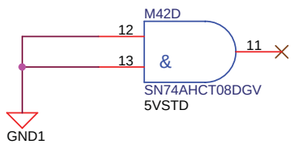
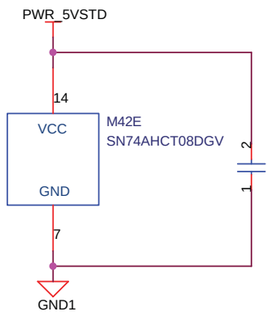
D:49page
E:79page
F:49page
G:78page

SLP_S3, SLP_S5#に3VSTDでPull-Upがあるためマスク回路追加







A:78page
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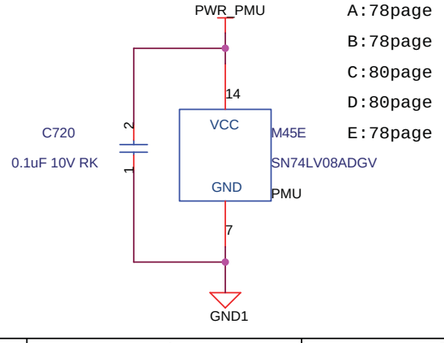
C:78page(Reserve)
D:78page(Reserve)
E:78page

SN74AHCT08
VCC : 4.5V - 5.5V
VIH : 2.00V
VIL : 0.80V
VI : 0V - 5.5V



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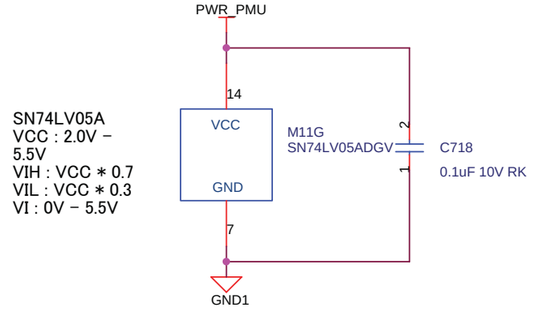

SN74LV05A
VCC : 2.0V ~ 5.5V
VIH : VCC * 0.7
VIL : VCC * 0.3
VI : 0V ~ 5.5V

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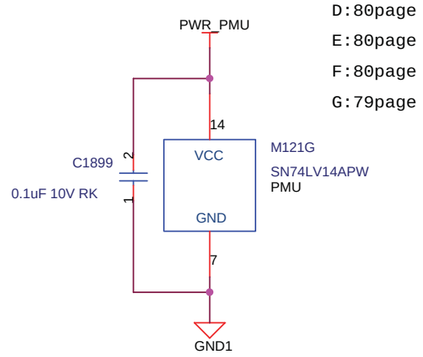
Logic

						TITLE	VB313AA
						DRAW. No.	C1CP302570-X2
						CAST	
Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.	Sheet 74 / 93
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa		

Dolphin

PWR_3VSUS to BENN_SUSOK
Default 50ms



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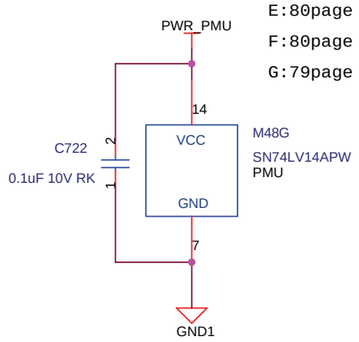

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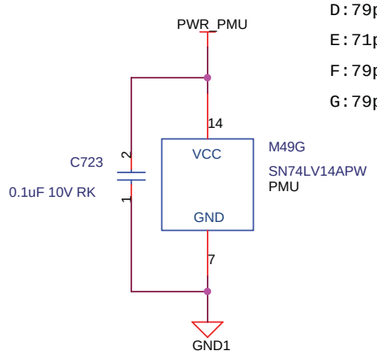

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D:79page
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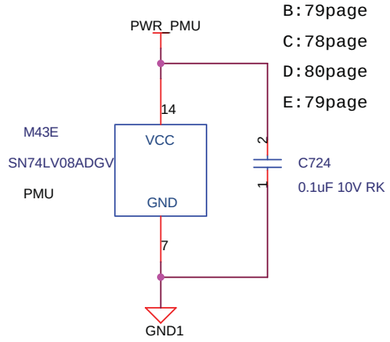
G:79page

PWR_3VMAIN to BENN_MAINOK
Default 170ms



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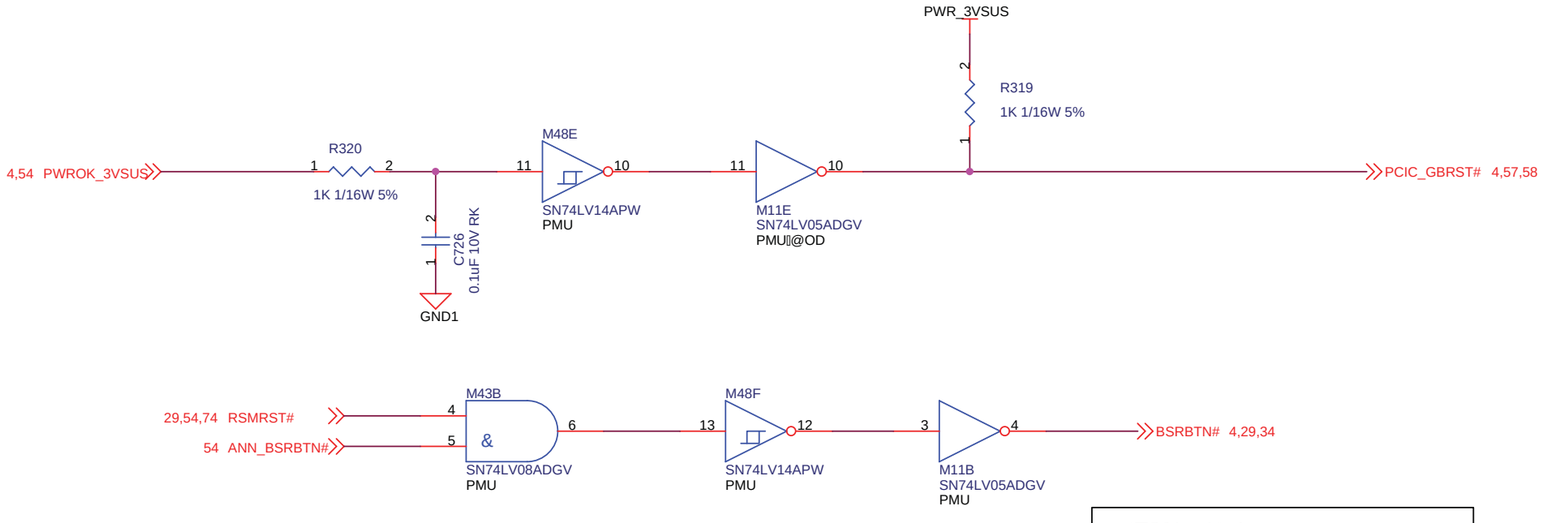

遅延ターゲット
BD5327G:
Tplh(s) = 0.69(TYP)x9(MΩ)x CT(F)

RESET IC

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Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

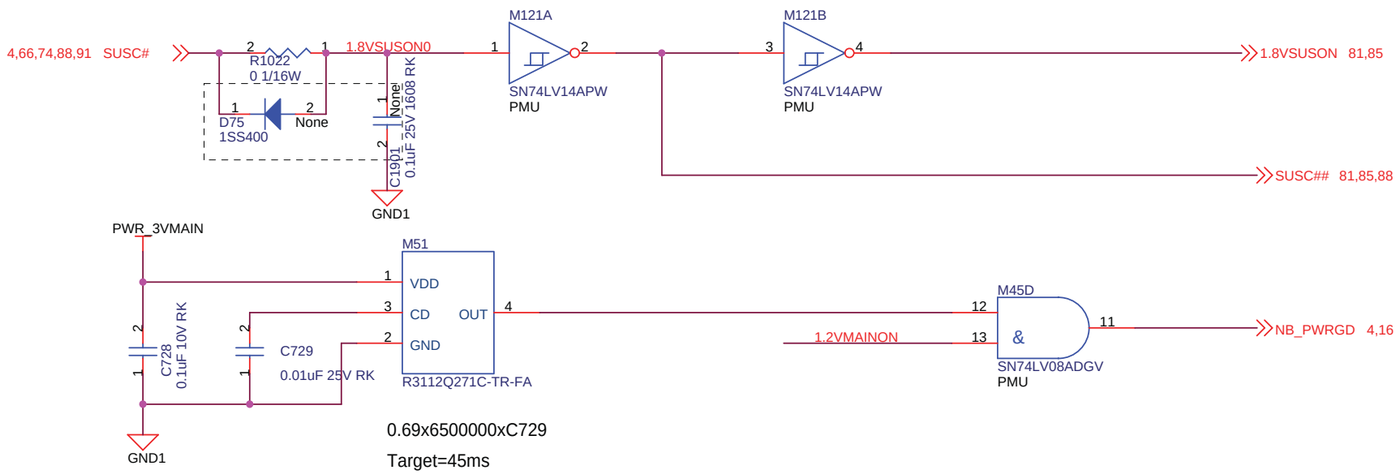
TITLE: **VB313AA**

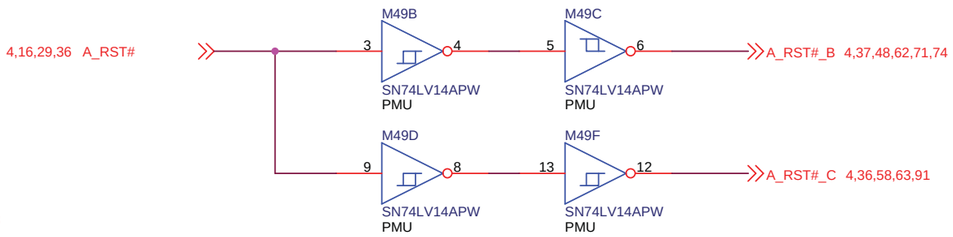
DRAW. No.: C1CP302570-X2

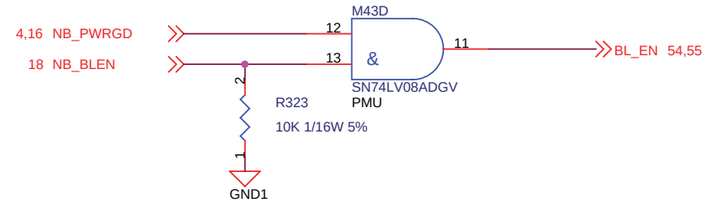
CAST

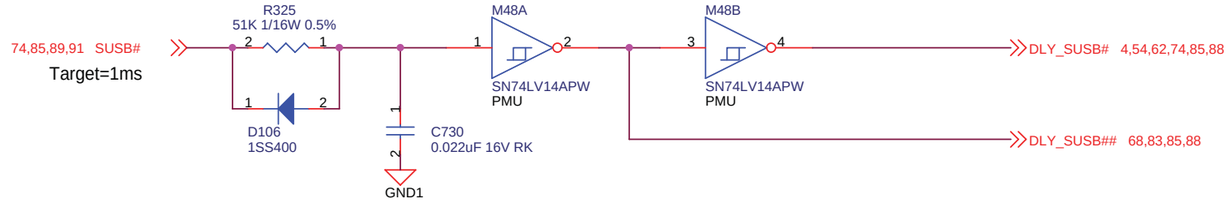
FUJITSU LTD.

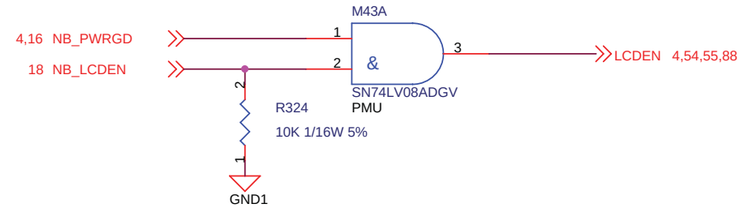
Sheet 75 / 93

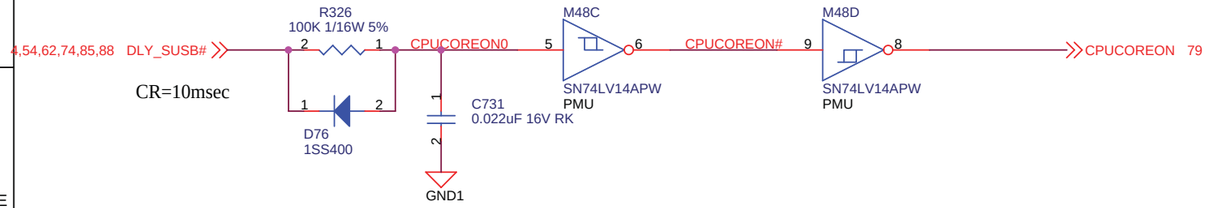


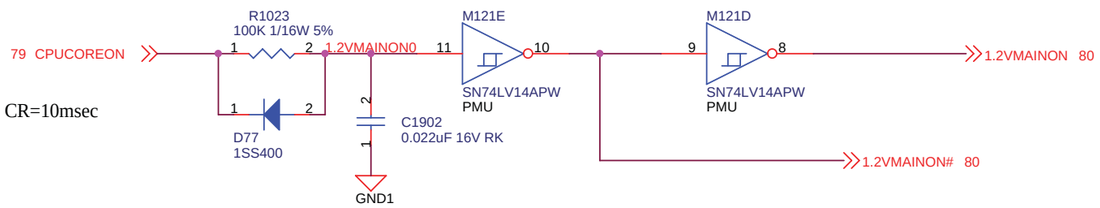












SEQUENCE

Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE: **VB313AA**

DRAW. No.: C1CP302570-X2 CAST

FUJITSU LTD.

Sheet 76 / 93

Dolphin

Falcon Power Supply

Caution

Features

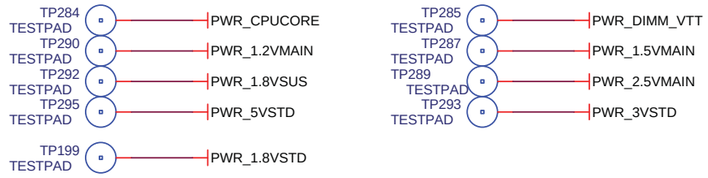
1/ Voltage Regulator for AMD K8 Rev.F Processor
2/ ATI RS480M Chipset
3/ DDR2 Memory
4/ Internal VGA (PowerPlay is not supported)
5/ Normal Speed Charger
6/ 19V AC Adaptor
7/ A circuit reducing a rush current from AC adaptor
8/ Internal Battery with 4 or 3 Seirial cells and Digital Interface

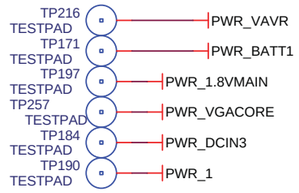
Power Contents

Voltage Regulator Spec.

DDC	CPUCore	TBD	35Atyp/peak
	1.2VMain	1.200V +/-5% (1.140V-1.260V)	6Atyp / 8Apeak
	1.8VSus	1.800V +/-5% (1.710V-1.890V)	6Atyp / 8Apeak
	3VStd	3.300V +/-5% (3.135V-3.465V)	6Atyp / 8Apeak
	5VStd	5.000V +/-4% (4.800V-5.200V)	6Atyp / 8Apeak
Charger	CV 3-serial 12.60V +/-1.2% (12.45V-12.75V)		CC 1.33A
	CV 4-serial 16.80V +/-1.2% (16.60V-17.00V)		CC 1.33A
LDO	DimmVtt	0.900V +/-100mV (0.800-1.000V)	+-0.25Atyp / +-1Apeak
	1.5VMain	1.500V +/-5% (1.425V-1.575V)	1A
	1.8VStd	1.800V +/-5% (1.710V-1.890V)	0.3A
	2.5VMain	2.500V +/-5% (2.375V-2.625V)	40mA
	VAVR	3.300V +/-2% (3.234V-3.366V)	30mA

TestPad (for SFJ)





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Power/ TopPage

Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE: **VB313AA**

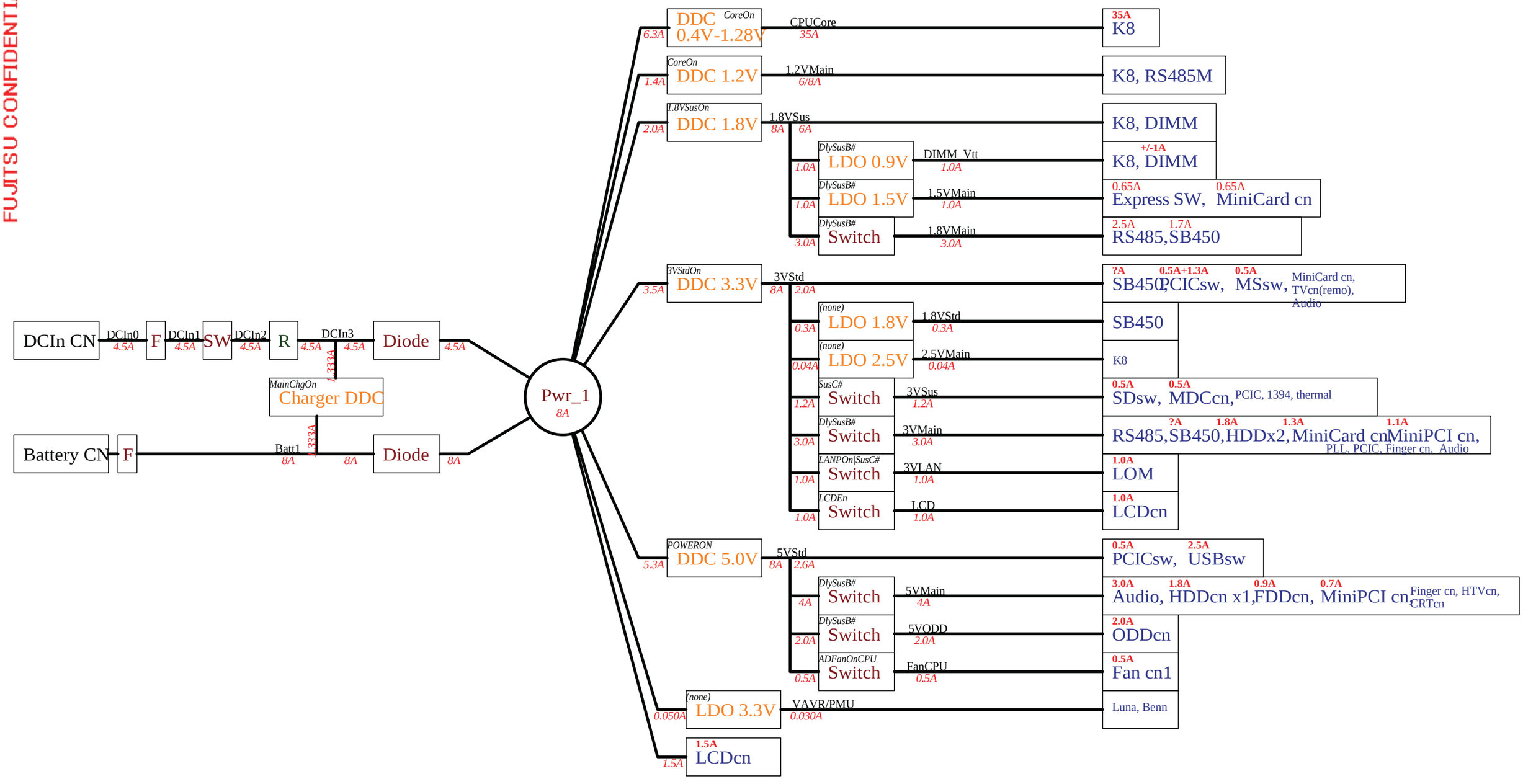
DRAW. No.: C1CP302570-X2 CAST

FUJITSU LTD.

Sheet 77 / 93

Dolphin

Power Delivery



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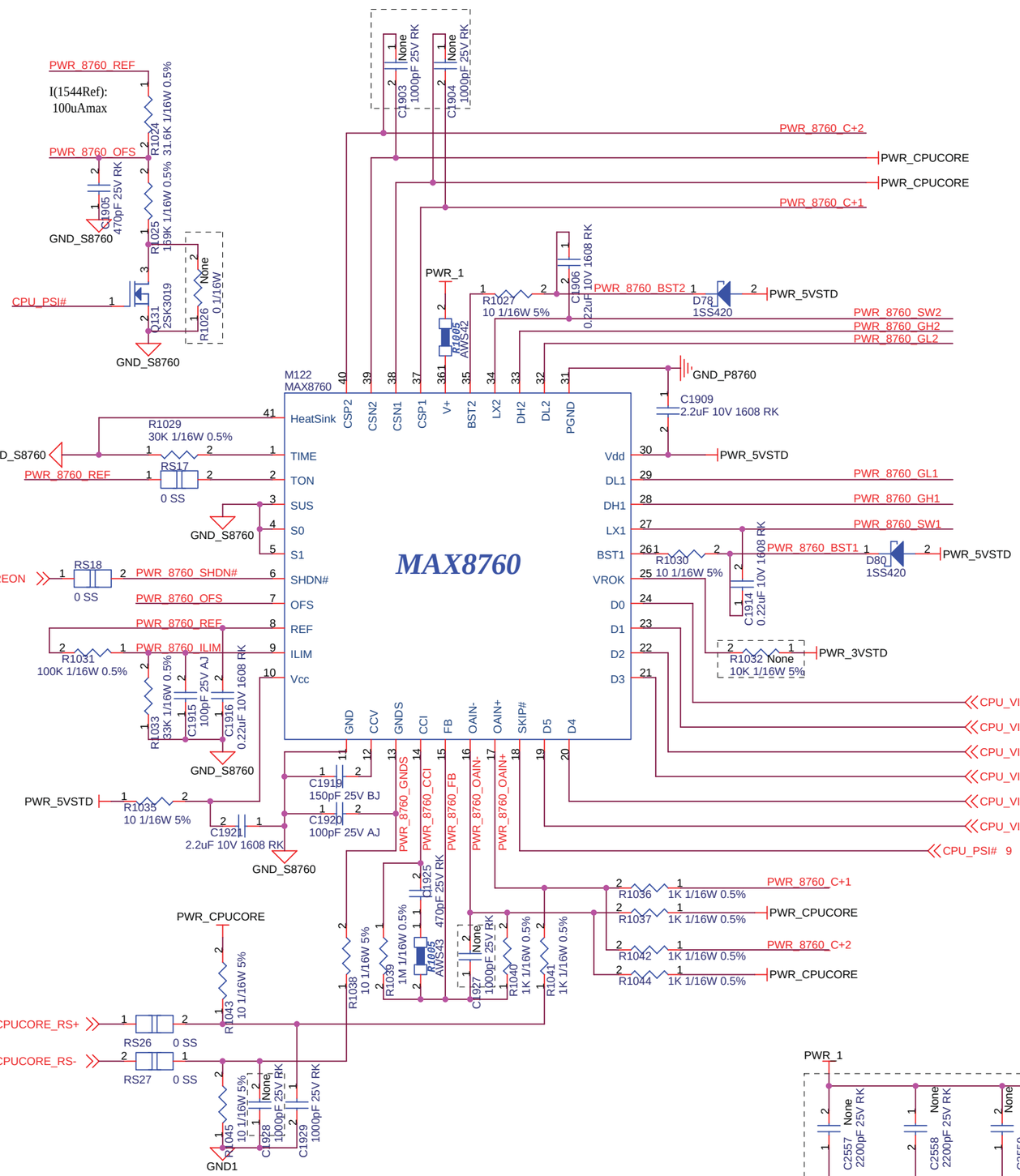
Power/ Delivery

0.1A以下はフォント小で、電流表示なし

						TITLE	VB313AA
						DRAW. No.	C1CP302570-X2
						CAST	
Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.	Sheet 78 / 93
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa		

Dolphin



0.400V-1.288V/35A typ,peak

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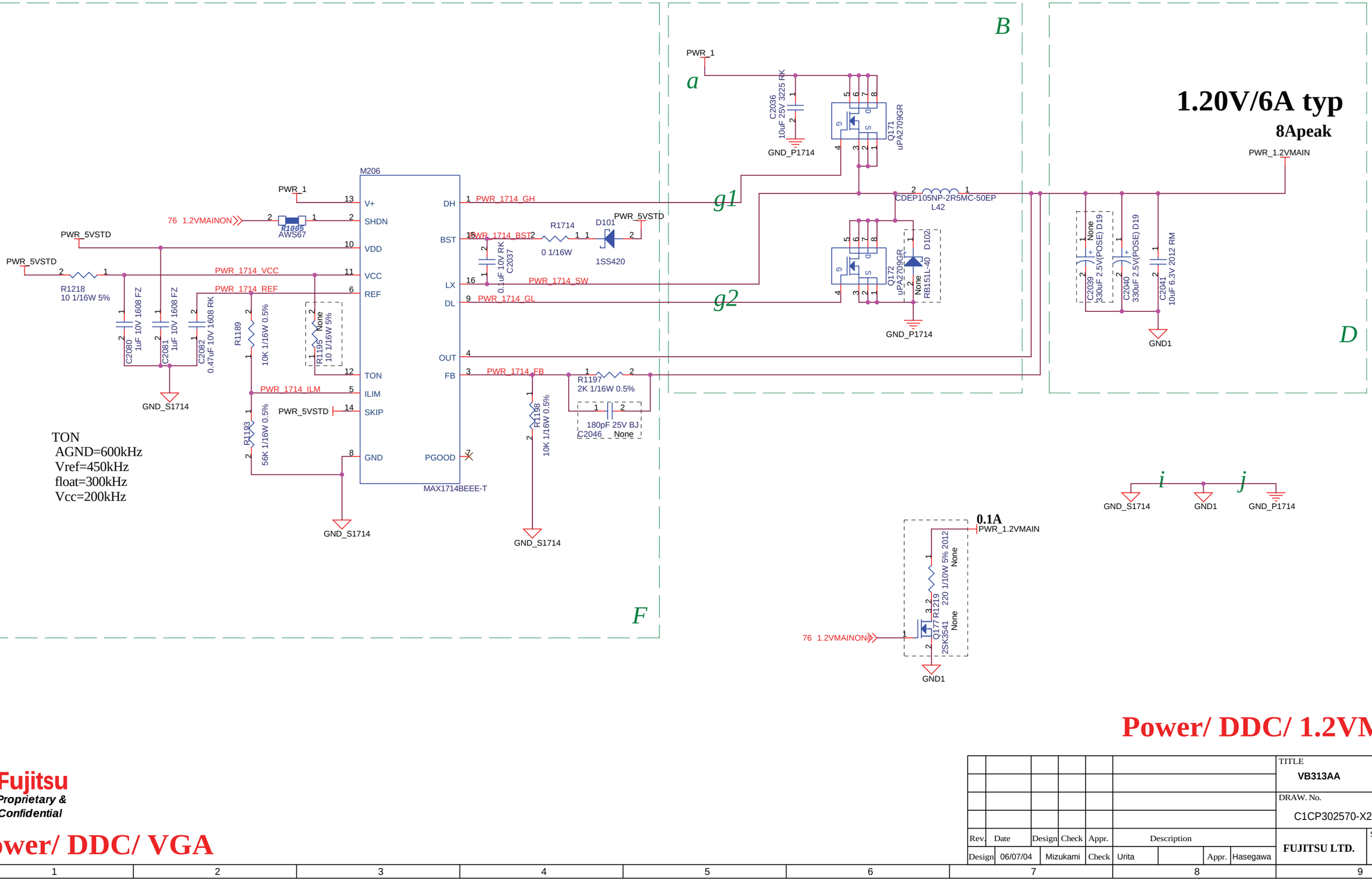
Power/ DDC/ CPUCore

TITLE	VB313AA						
DRAW. No.	C1CP302570-X2					CAST	
Rev.	Date	Design	Check	Appr.	Description	Sheet	79 / 93
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa	FUJITSU LTD.	

Dolphin

1.20V/6A typ

8Apeak



Power/ DDC/ 1.2VMAIN

Power/ DDC/ VGA

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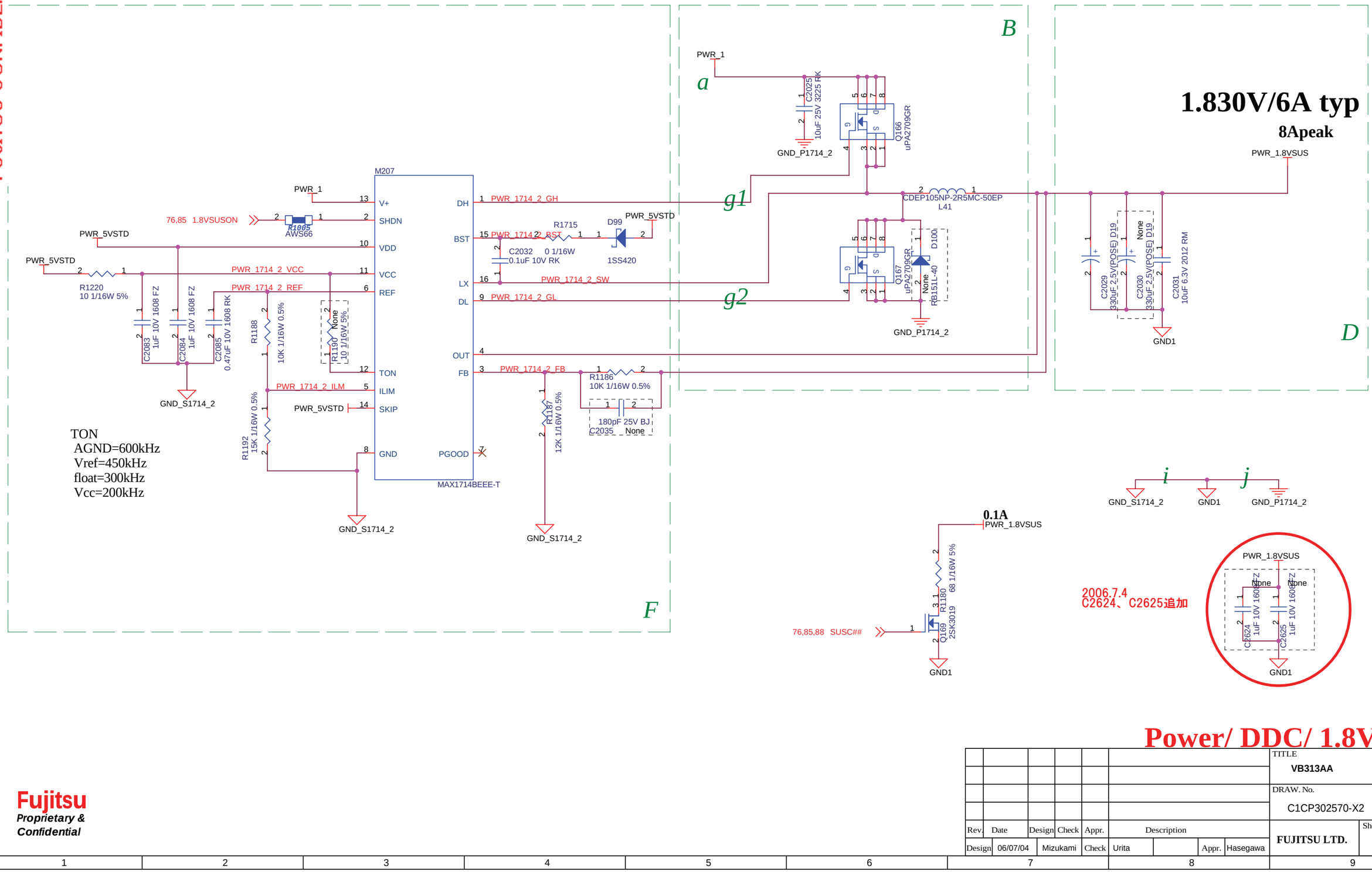
						TITLE	VB313AA	
						DRAW. No.	C1CP302570-X2	CAST
Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.		Sheet 80 / 93
Design	06/07/04	Mizukami	Check	Urita			Appr. Hasegawa	

Dolphin



Power/ DDC/ 1.8VSus

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						TITLE	VB313AA
						DRAW. No.	C1CP302570-X2
						CAST	
Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.	Sheet 81 / 93
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa		

Dolphin

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Power/ DDC/ 1.2V,1.8V

Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE: **VB313AA**

DRAW. No.: C1CP302570-X2

CAST

FUJITSU LTD.

Sheet 82 / 93

Frequency Select: FSEL(3pin)
VCC=500kHz
REF=300kHz
GND=200kHz
I Limit: ILIM(4,5pin)
VCC=75mV
or
V(ILIM)/10 V
(50mV-200mV)

Under/Over Voltage Protection:
OVP#(15pin)/UVP#(11pin)
H=disable
L=enable

MAX1533

MAX1533A
CA46710-0076

5.025V/6A typ
8Apeak

3.324V/6A typ
8Apeak

JISC5202により、
定格電圧の2.5倍、
5秒以内であればOK

Fujitsu
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Power/ DDC/ 3.3V,5V

						TITLE	VB313AA
						DRAW. No.	C1CP302570-X2
						CAST	
Rev.	Date	Design	Check	Appr.	Description		
Design	06/07/04	Mizukami	Check	Urita		FUJITSU LTD.	Sheet 83 / 93
				Appr.	Hasegawa		

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Dolphin

8A PWR_DCIN2 — Rs1 R392 15m 1W 1% — 8A PWR_DCIN3

h1 h1

R1005 AWS23 / R1005 AWS24

C807 None 0.1uF 25V 1608 RK

C808 None 0.1uF 25V 1608 RK

GND_S8724

PWR_8724_CSSN 26 CSSN

PWR_8724_CSSP 27 CSSP

PWR_DCIN3

D53 1SS420

R394 91K 1/16W 0.5%

R395 12K 1/16W 0.5%

C810 1000pF 25V RK None

C811 1uF 25V 1608 RK

GND_S8724 GND_P8724

PWR_8724_DCIN 1 DCIN

PWR_8724_ACIN 10 ACIN

PWR_8724_REFIN 12 REFIN

90 PMU_VB1 — R1005 AWS25 — PWR_8724_ICTL 13 ICTL

PWR_8724_VCTL 15 VCTL

V(ICHG)=Iout x Rs2 x G(ICHG) x R(ICHG)
[G(ICHG)=3uAtyp]
V(IINP)=Iinp x Rs2 x G(IINP) x R(IINP)
[G(IINP)=3uAtyp]

R396 20K 1/16W 0.5%

R398 12K 1/16W 0.5%

GND_S8724

PWR_8724_ICHG 9 ICHG

PWR_8724_IINP 28 IINP

90 PMU_MAINCHG — R1005 AWS26 — PWR_8724_SHDN 8 SHDN

PWR_8724_CCV 7 CCV

PWR_8724_CCI 6 CCI

PWR_8724_CCS 5 CCS

PWR_8724_REF4 4 REF

V(REF)=4.096V

R407 10K 1/16W 0.5%

PWR_8724_CLS 3 CLS

V(CLS)=3.263V

R410 39K 1/16W 0.5%

ACOK# 11

GND 14

GND_S8724

MAX8724
CA46710-0050

M58

V(CELLS):
GND= 2cells
Float= 3cells
RefIn= 4cells

CELLS 17

PWR_8724_CELLS

Q60 RVE002P03

PWR_8724_REFIN

R393 470K 1/16W 5%

PWR_PMU

Q61 2SK3019

PMU_SERIAL4/3# 90

GND_S8724

DHI 25 PWR_8724_GH

DLO 21 PWR_8724_GL

g1 g2

V(LDO)=5.4V

LDO 2

PWR_8724_LDO

C809 1uF 10V 1608 RK

GND_S8724

BST 24 PWR_8724_BST

R1716 0 1/16W

D55 RB520S-30

PWR_8724_DP

C813 0.47uF 10V 1608 RK

LX 23 PWR_8724_SW1

DLOV 22 PWR_8724_DP

R399 33 1/16W 5%

PWR_8724_LDO

C814 1uF 10V 1608 RK

PGND 20

CSIP 19 PWR_8724_CSIP — R1005 AWS27

CSIN 18 PWR_8724_CSIN — R1005 AWS28

BATT 16

C818 None 0.1uF 25V 1608 RK

C819 None 0.1uF 25V 1608 RK

GND_S8724

FG 29 GND_S8724

a

1.2A PWR_DCIN3

PWR_8724_IN

D54 RB053L-30FA

C812 10uF 25V 3225 RK

Q62 SP8K3TB

GND_P8724

L36 CDRH8D43HP-100NC

PWR_8724_ILR

D56 RB151L-40

GND_P8724

B

8.4V-16.8V/1.3A

R397 27m 1W 1% KOA-SL1

Rs2

PWR_BATT1

C815 10uF 25V 3225 RK

C816 10uF 25V 3225 RK

C817 10uF 25V 3225 RK None

R400 10K 1/16W 5% None

GND1

C

h2 h2

PWR_PMU

R412 13K 1/16W 0.5%

PWR_8724_IINP

R413 20K 1/16W 0.5%

C825 1000pF 25V RK

C826 0.01uF 25V RK

M59 NJU7141F(TE1)

VDD IN- IN+ OUT VSS

R411 100K 1/16W 5%

PMU_CHGMASK 90

C824 0.1uF 10V RK

GND1

R414 1M 1/16W 0.5%

F

Conventional Parameter
20K(side_Ref4) / 39K

PWR_PMU

PWR_8724_REF4

R403 13K 1/16W 0.5% None

R404 20K 1/16W 0.5%

PWR_8724_REFIN

V(RefIn)=2.728V

R408 39K 1/16W 0.5%

GND_S8724

Conventional Parameter
56K(side_PMU) / 39K

PWR_8724_REFIN

PWR_PMU

R405 10K 1/16W 0.5% None

R406 56K 1/16W 0.5%

PWR_8724_VCTL

V(VCTL)=1.364V

R409 39K 1/16W 0.5%

GND_S8724

Iinp_max=<4.21A @80W AC Adaptor

Iinp_max={ V(CLS)/V(REF) }_max x 0.078/Rs1_min

Vout= CELLS x { 4V + 0.4xV(VCTL)/V(RefIn) }
Vout= CELLS x 4.2V
-> 0.4VxV(VCTL)/V(RefIn) =0.2V
-> V(VCTL)/V(RefIn) =0.5

Iout= V(ICTL)/V(RefIn) x 0.075/Rs2
VB1=0.984V @Iout=1A (Luna Spec.)
Rs=0.027
-> V(ICTL)/Iout=0.984
-> ideal V(RefIn)=0.984 x 0.075 x 0.027=2.733V
real V(RefIn)=2.728V
-> real / ideal =0.998

C820 0.022uF 16V RK

C821 0.01uF 25V RK

C822 1000pF 25V RK

C823 1uF 10V 1608 RK

R401 470K 1/16W 5%

R402 4.7K 1/16W 0.5%

↑64Wアダプタ設定

2006. 05. 31
ACアダプタ80W化に伴う変更
R398: 12k -> 10K
R407: 12k -> 10K
R410: 20k -> 39K

i j

GND_S8724 GND1 GND_P8724

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Power/ DDC/ Charger

Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE: VB313AA

DRAW. No.: C1CP302570-X2 CAST

FUJITSU LTD.

Sheet 84 / 93

FUJITSU CONFIDENTIAL Dolphin

5V/30mA
PWR_1533_LDO5

M60
BH33FB1WHFV
CA46530-1272
STBY
GND
VIN
N.C.
VOUT
C827 0.1uF 10V RK
C828 10uF 6.3V 2012 RM
R1005 AWS33
R1005 AWS31

3.3V/30mA
3.3V/5mA
PWR_VAVR
3.3V/30mA
PWR_PMU
GND1
GNDA

LUNA(M66)の近傍に配置

76,81 1.8VSUSON
R1005 AWS29
PWR_3534_EN
PWR_1.8VSUS
PWR_5VSTD
R415 22 1/16W 5%
PWR_3534_VCC
8,23,24 REF_MEM
R1005 AWS32
PWR_3534_REF

M61 BD3534FVM
BD3534FVM
CA46530-1750
VDDQ
VCC
EN
VREF
VTT IN
VTTS
VTT
GND
C831 10uF 6.3V 2012 RM
C832 0.1uF 10V RK
C833 0.1uF 10V RK
C830 10uF 6.3V 2012 RM
C829 220uF 2.5V(NEO/TPE) B21 CAT22-D0E2200M

1.8V/1.0A
PWR_1.8VSUS
0.9V +/-1A
0.25Acontinuous
PWR_DIMM_VTT
R859 68 1/16W 5% None
Q119 2SK3019 None
76,81,88 SUSC##
GND1

3.3V/0.3A
PWR_3VSTD
Must Keep Cool !
1.8V/0.3A
PWR_1.8VSTD

M75
R1173S001B
CA46530-1800
VDD
GND
CE
VOUT
GND
ADJ
C1964 10uF 6.3V 2012 RM
C1965 10uF 6.3V 2012 RM
C1963 100uF 6.3V (NEO/TPE) B21 CAT22-D0J1000M
R1005 AWS55
R1101 24K 1/16W 0.5%
R1102 30K 1/16W 0.5%
R1100 220 1/16W 5% None
Q152 2SK3019 None
GND1

74,83 POWERON#

UVP 1.14Vtyp
0.93Vmin, 1.36Vmax
M63 BD3504FVM
BD3504FVM
NRCS
GND
EN
VCC
VD
G
VS
VFB
R417 15K 1/16W 0.5%
R419 10K 1/16W 0.5%
PWR_3504_G
R421 5.1K 1/16W 0.5%
R426 3.9K 1/16W 0.5%
C840 0.1uF 10V RK
C841 0.033uF 16V RK
4,54,62,74,76,88 DLY_SUSB#
PWR_5VSTD
Q64 RTW060N03
C835 10uF 6.3V 2012 RM
R423 220 1/16W 5%
C842 0.022uF 16V RK
C837 100uF 6.3V (NEO/TPE) B21 CAT22-D0J1000M
R424 220 1/16W 5%
Q65 2SK3019
GND1

1.8V/1.0A
PWR_1.8VSUS
1.5V/1.0A
PWR_1.5VMAIN
2006.7.4
02版: Q64のFootPrint変更：MP078 -> MP158
68,76,83,88 DLY_SUSB##

0.5mm
3.3V/0.04A
PWR_3VSTD
CA46530-2082
M123 R1114D251B
Vdd
CE
GND
GND
Vout
NC
C1966 0.1uF 10V RK
C1967 1uF 10V 1608 RK
C1968 10uF 6.3V 2012 RM
R1103 220 1/16W 5% None
Q153 2SK3019 None
74,76,89,91 SUSB#
74,89 SUSB##
GND1

0.5mm
2.5V/0.04A
PWR_2.5VMAIN

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Power/ LDO

Rev.	Date	Design	Check	Appr.	Description		
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa

TITLE: VB313AA
DRAW. No.: C1CP302570-X2
CAST
FUJITSU LTD.
Sheet 85 / 93

Dolphin

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Power/ LDO2

Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE: **VB313AA**

DRAW. No.: C1CP302570-X2 CAST

FUJITSU LTD.

ゴミ信号線削除

FUJITSU CONFIDENTIAL

Dolphin

CN35
DC-IN CN

TP411 TESTPAD
TP187 TESTPAD
TP412 TESTPAD
TP189 TESTPAD

PWR_DCIN_CN+ 4.5A
PWR_DCIN_CN- 4.5A

CA53140-5170
FL201
BLM18SG260TN1
FL59
FBMJ4516HM560
CA53140-5140
None
FL60
FBMJ4516HM560
CA53140-5140
None
FL202
BLM18SG260TN1
CA53140-5170

C849 0.01uF 25V RK
C850 1000pF 25V RK
C851 1000pF 25V RK
C852 0.01uF 25V RK
C854 0.01uF 25V RK
C855 0.01uF 25V RK

PWR_DCIN0 4.5A
4.5mm
GND1

05/11
TP411, TP412追加

2006.5.16
FL201,FL202追加

F1
10A 60V(P129)
PWR_DCIN1 4.5A

R430 100K 1/16W 5%
R431 100K 1/16W 5%
C853 0.1uF 25V 1608 RK
Q67
uPA2719GR
CA47100-6362
PWR_DCIN2
C848 47uF 25V(AL) WM

6mm
18-21V/4.5A

8mm
8.4-16.8V/8A

CN36
BAT CN
CA52300-3001

F2
15A 60V(P129)
PWR_BATT1
PWR_BATT1_CN
PMU_VSENSE1_CN
PMU_BT1TEMP/IN#_CN
PWR_BT1ROM_CN
PMU_BT1CLK_CN
PMU_BT1DAT_CN
PMU_SCONT1#_CN

R1005 AWS34
R1005 AWS35
R432 10 1/16W 5%
R433 100 1/16W 0.5%
R434 100 1/16W 0.5%
R1005 AWS36

C856 0.1uF 25V 1608 RK
C857 0.22uF 25V 1608 FZ
C858 0.1uF 25V 1608 RK
C859 220pF 50V RK
D62 RB521S-30
D63 1SS420
D64 RB521S-30
PWR_1533_LDO5
D66 1SS226
D67 1SS226
R435 100K 1/16W 5% D61 1SS400
Q69 2SK3019
PWR_PMU
PMU_SCONT1 93

C2613 220pF 50V RK
C2614 220pF 50V RK
C2615 220pF 50V RK
部品追加 C2613-2615

PMU_VSENSE1 93
PMU_BT1IN#0 90
PWR_BT1ROM
0.3mm
PMU_BT1CLK 90
PMU_BT1DAT 90

B

6mm
18V-21V/4.5A
PWR_DCIN3
D58 RB053L-30FA
D59 RB053L-30FA

8mm
8.4-21V/8A
PWR_1

8mm
8.4-16.8V/8A
PWR_BATT1
D60 RB053L-30FA
Q68
uPA2719GR
CA47100-6362
D65 1SS420
PWR_DCIN3
R436 100K 1/16W 5%
GND1

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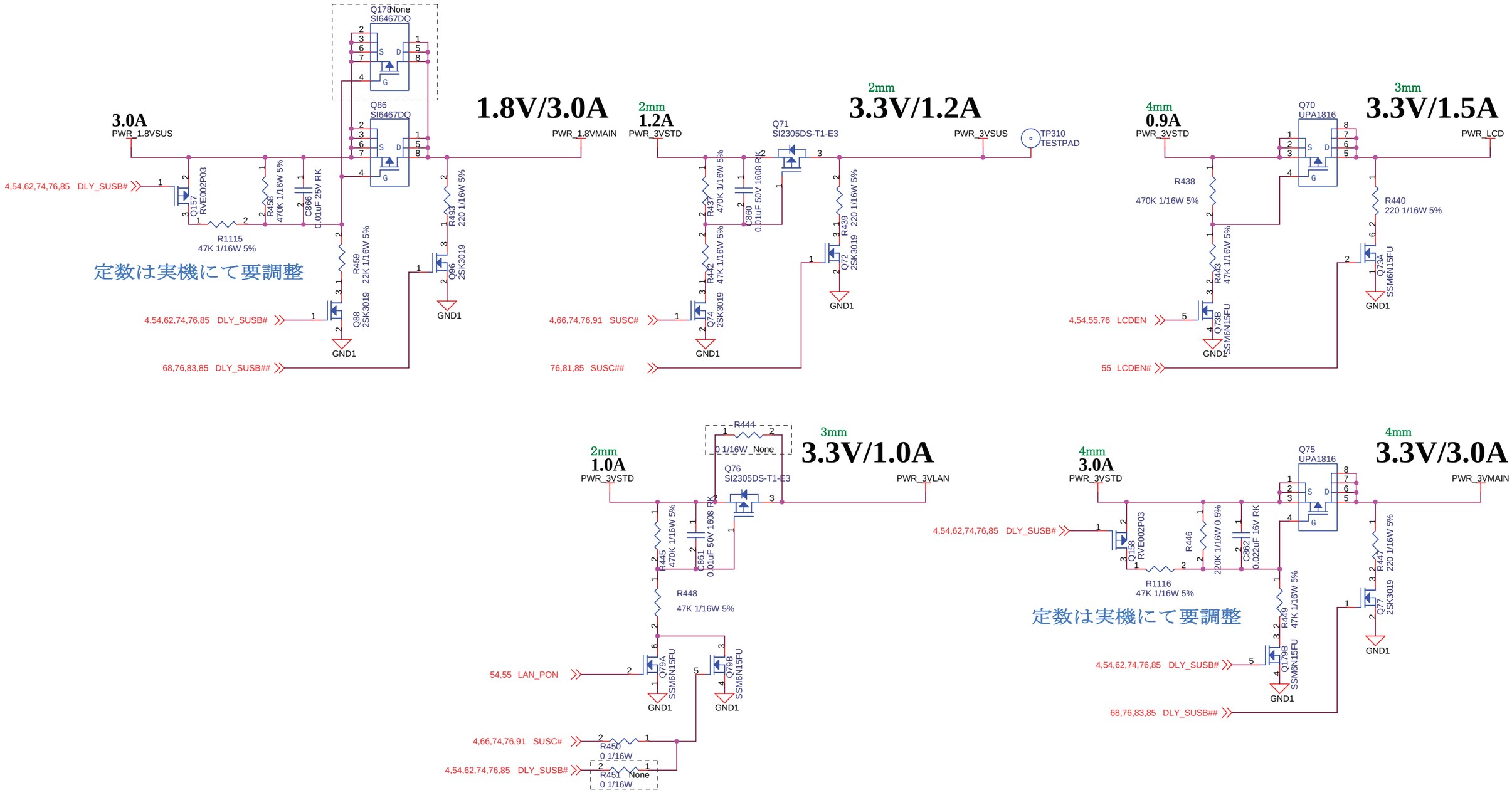
Power/ Node/ DCIn, Battery CN

Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE: VB313AA
DRAW. No.: C1CP302570-X2
CAST:
FUJITSU LTD.
Sheet 87 / 93

FUJITSU CONFIDENTIAL Dolphin



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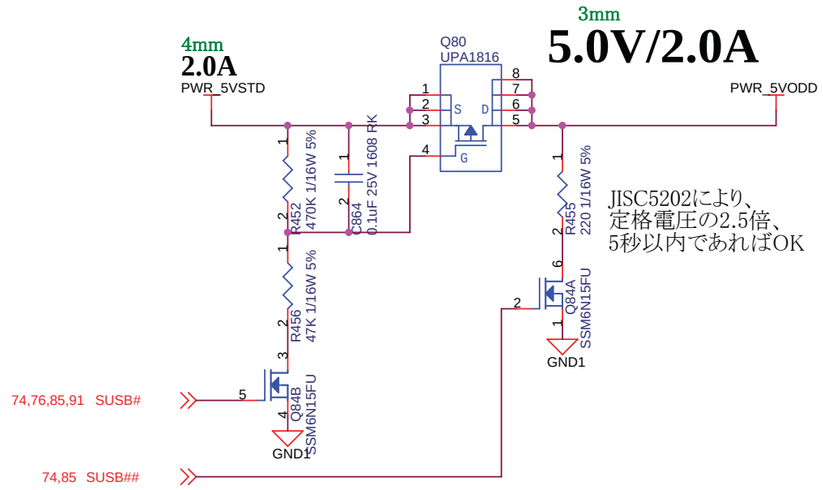
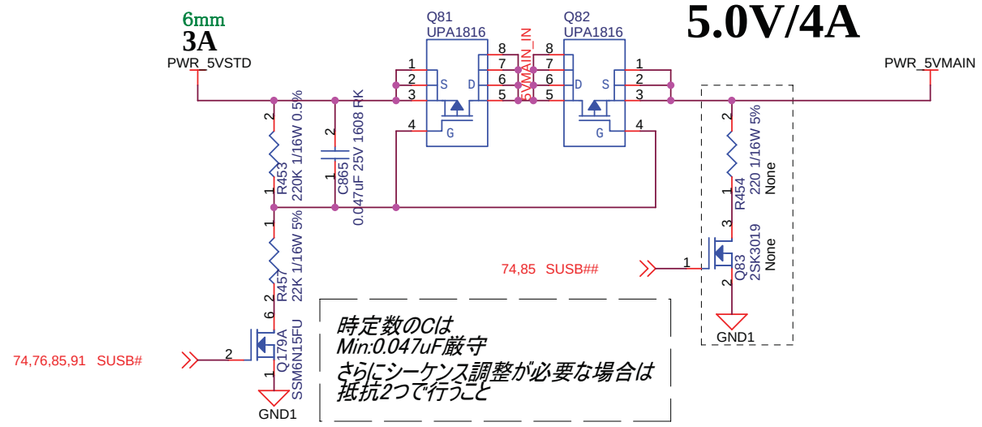
Power/ Node/ Switch1

Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE: VB313AA
DRAW. No.: C1CP302570-X2
CAST:
FUJITSU LTD.
Sheet 88 / 93

FUJITSU CONFIDENTIAL Dolphin





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Power/ Node/ Swicth2

Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

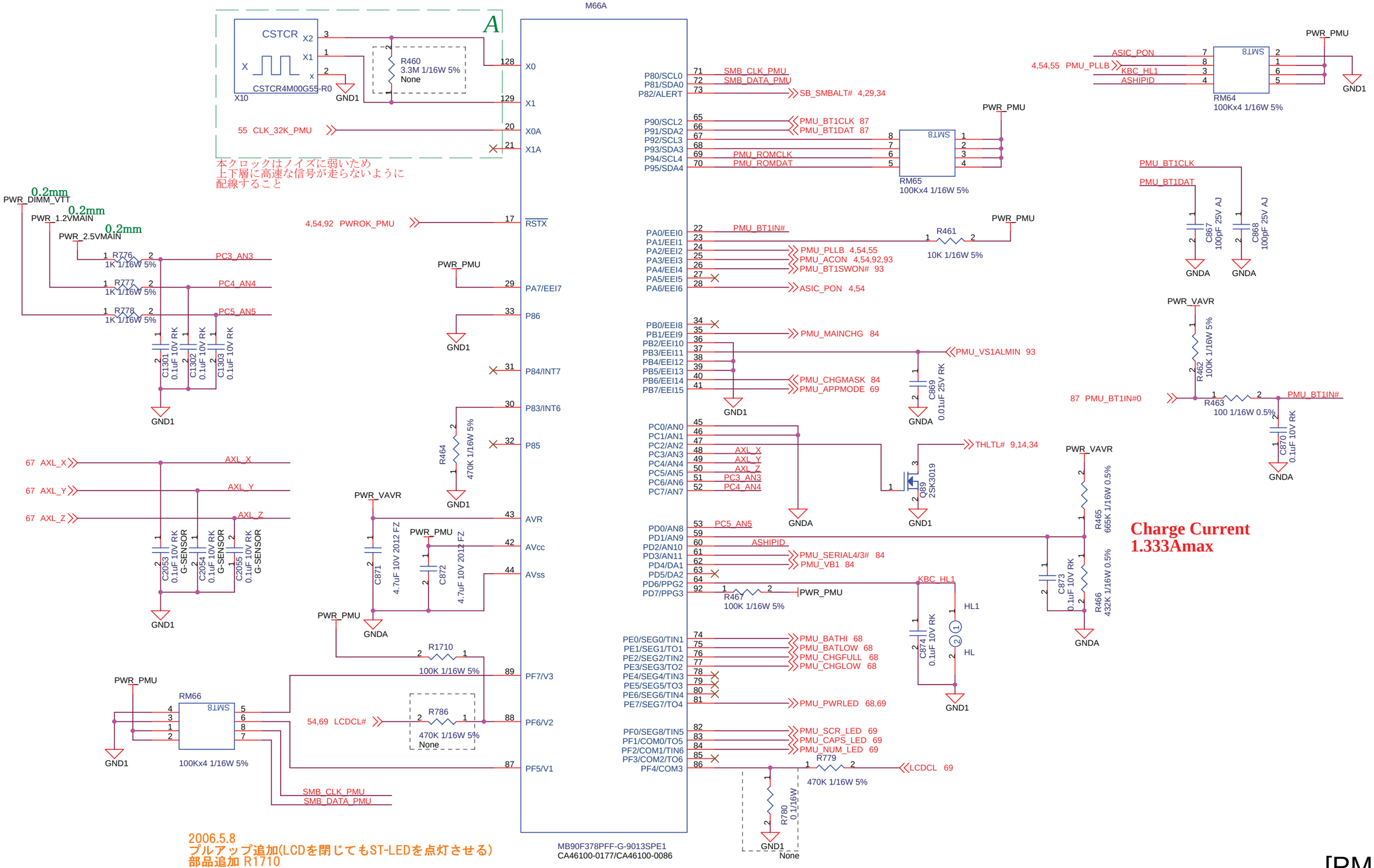
TITLE: VB313AA

DRAW. No.: C1CP302570-X2 CAST

FUJITSU LTD.

Sheet 89 / 93

FUJITSU CONFIDENTIAL Dolphin



Charge Current
1.333Amax

2006.5.8
プルアップ追加(LCDを閉じてもST-LEDを点灯させる)
部品追加 R1710

[PMU]

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Power/ PMU/ LUNA1

						TITLE	VB313AA
						DRAW. No.	C1CP302570-X2
						CAST	
Rev.	Date	Design	Check	Appr.	Description	FUJITSU LTD.	Sheet 90 / 93
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa		

本ページで追加したVIAはTPとして使用する。
シルクを入れること。

VIA1 TESTPAD — LPC_FRAME#
VIA2 TESTPAD — CLK_33_PMU
VIA3 TESTPAD — LPC_AD0
VIA4 TESTPAD — LPC_AD1
VIA5 TESTPAD — LPC_AD2
VIA6 TESTPAD — LPC_AD3

M66B

4,29 KBC_A20G
27,34,37,48,54,71 LPC_FRAME#
4,36,58,63,76 A_RST#_C
30,35,48,54 CLK_33_PMU
27,34,37,48,54,71 LPC_AD0
27,34,37,48,54,71 LPC_AD1
27,34,37,48,54,71 LPC_AD2
27,34,37,48,54,71 LPC_AD3

9 P50/GA20
10 P51/LFRAME#
11 P52/LRESET#
12 P53/LCK
13 P54/LAD0
14 P55/LAD1
15 P56/LAD2
16 P57/LAD3

4,27,34,48,57,71 SERIRQ
27,36,48,57,71 PCI_CLKRUN#
51 PS2_KCLOCK
51 PS2_KDATA
51 PS2_MCLOCK
51 PS2_MDATA
56 PS2_PCLOCK
56 PS2_PDATA

8 P47/SERIRQ
7 P46/CLKRUN#
1 P40/PSCK1
2 P41/PSDA1
3 P42/PSCK2
4 P43/PSDA2
5 P44/PSCK3
6 P45/PSDA3

WakeUp

P00 109 ROW#0
P01 110 ROW#1
P02 111 ROW#2
P03 112 ROW#3
P04 113 ROW#4
P05 114 ROW#5
P06 115 ROW#6
P07 116 ROW#7
ROW#[0:7] 69,70

P10 117 PMU_CLM#0
P11 118 PMU_CLM#1
P12 119 PMU_CLM#2
P13 120 PMU_CLM#3
P14 121 PMU_CLM#4
P15 122 PMU_CLM#5
P16 123 PMU_CLM#6
P17 124 CLM#7
P20 125 CLM#8
P21 130 CLM#9
P22 131 CLM#10
P23 132 CLM#11
P24 133 CLM#12
P25 134 CLM#13
P26 135 CLM#14
P27 136 CLM#15
CLM#[0:15] 70

M67
SN74CBT3384APW
CA46400-2061

PMU_CLM#5 1 1OE#
PMU_CLM#0 3 1A1
PMU_CLM#1 4 1A2
PMU_CLM#2 7 1A3
PMU_CLM#3 8 1A4
PMU_CLM#4 11 1A5
PMU_CLM#6 13 2OE#
PMU_CLM#0 14 2A1
PMU_CLM#1 17 2A2
PMU_CLM#2 18 2A3
PMU_CLM#3 21 2A4
PMU_CLM#4 22 2A5
VCC 24 PWR_PMU
1B1 2 CLM#0
1B2 5 CLM#1
1B3 6 CLM#2
1B4 9 CLM#3
1B5 10 CLM#4
2B1 15 CLM#5
2B2 16 CLM#6
2B3 19
2B4 20
2B5 23 SCANY# 69
GND 12 GND1

PWR_PMU
C875 0.1uF 10V RK
GND1

PWR_PMU
R468 100K 1/16W 5% None
69 SCANX#
54,55,74 BL_EEN
R469 180K 1/16W 5%
C876 100pF 25V AJ
GND1

74,76,85,89 SUSB#
4,66,74,76,88 SUSC#
4,54,69 SUSSW#
68 PMU_MAILLED

93 P60/INT0
94 P61/INT1
95 P62/INT2
96 P63/INT3
97 P64/INT4
98 P65/INT5
99 P66/UCK1
100 P67/UO1

Latch

P30 137 PMU_D0
P31 138 PMU_D1
P32 139 PMU_D2
P33 140 PMU_D3
P34 141
P35 142 PMU_SMI 54
P36 143 PMU_PRM# 54
P37 144 PMU_PARST# 54
PMU_PE# 54

RM67
PMU_D0 8
PMU_D1 7
PMU_D2 6
PMU_D3 5
3 14
2 15
1 16
13
4
9 10
11
12
100Kx8 1/16W 5%
CAC39-Q1J1003J

PWR_PMU

PWR_PMU
C877 0.1uF 10V RK
C878 0.1uF 10V RK
C879 0.1uF 10V RK
C880 0.1uF 10V RK
GND1

RM69
SMT8
10Kx4 1/16W 5%
4 5 PMU_SL
3 6 58 MD0
2 7 57 MD1
1 8 56 MD2

18 54 90 126 Vcc1 Vcc2 Vcc3 Vcc4
19 55 91 127 Vss1 Vss2 Vss3 Vss4

P70/UI1 101 PMU_SL
P71/UCK2 102 PMU_BT1ID 93
P72/UO2 103
P73/UI2 104
P74/UCK3 105 HTKYSMI 54
P75/UO3 106 KBC_SCI 4,29,34
P76/UI3 107 KBC_INIT# 4,29
P77/PPG1 108

R470 100K 1/16W 5%
GND1

PWR_5VMAIN
PWR_3VMAIN
RM68
12 11 10 9 15 16 14 13
5 6 7 8 2 1 3 4
PS2_MDATA
PS2_MCLOCK
PS2_KDATA
PS2_KCLOCK
KBC_INIT#
KBC_A20G
PS2_PDATA
PS2_PCLOCK
10Kx8 1/16W 5%
CAC39-Q1J1002J

MB90F378PFF-G-9013SPE1
CA46100-0177/CA46100-0086

本ページの抵抗・コンデンサはM38867付近に配置すること。
パスコンについてはM38867の電源ピンに対して均等になるように配置分散し、
電源ピンまでのリード長を最大限短くなるようレイアウトすること。

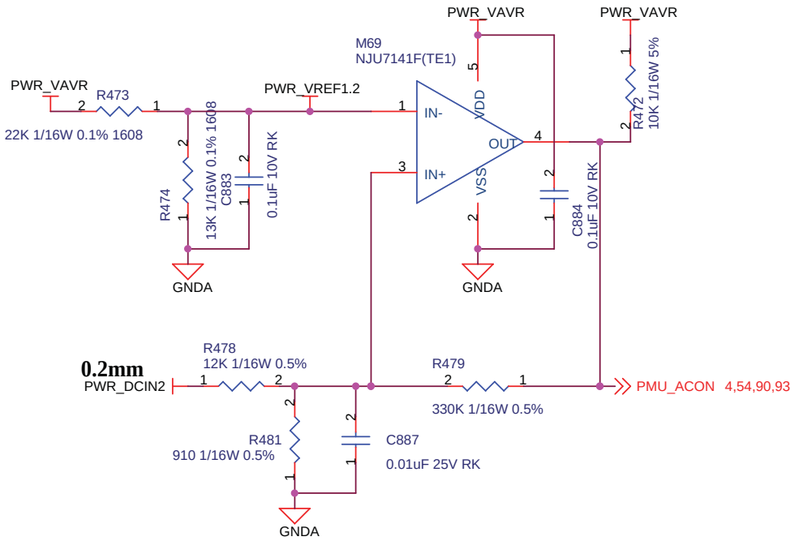
[KBC]

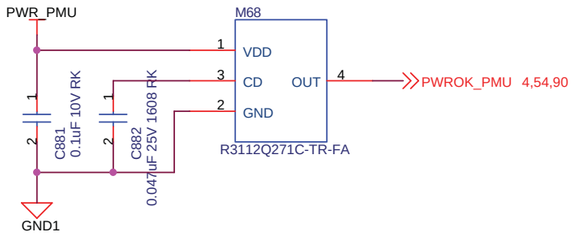
Fujitsu
Proprietary & Confidential

Power/PMU/LUNA2

Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE: VB313AA
DRAW. No.: C1CP302570-X2
CAST:
FUJITSU LTD.
Sheet 91 / 93





Target 200ms

遅延ターゲット
R3112N271C-TR:
Tplh(s) = 0.69(TYP)x6.5(MΩ)x CT(F)

A

LUNA近傍に配置

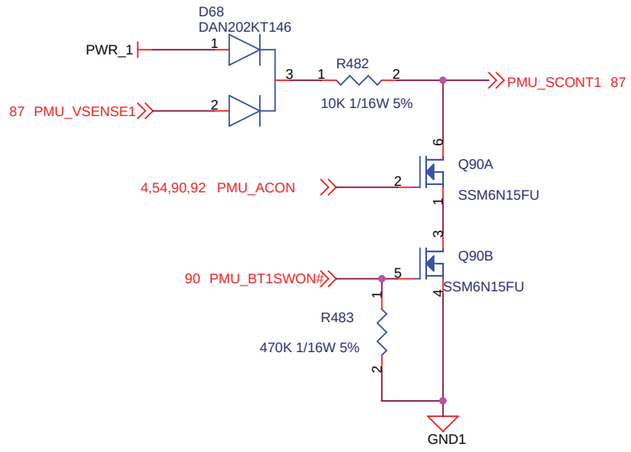
Fujitsu
Proprietary & Confidential

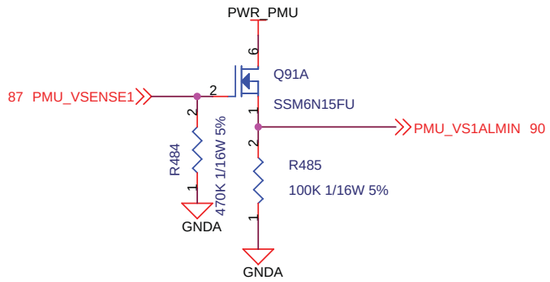
Power/ PMU/ Etc0 (Common)

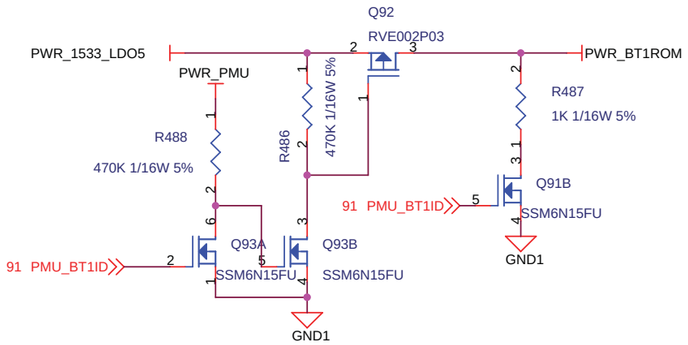
Rev.	Date	Design	Check	Appr.	Description
Design	06/07/04	Mizukami	Check	Urita	Appr. Hasegawa

TITLE: **VB313AA**
DRAW. No.: C1CP302570-X2
CAST
FUJITSU LTD.
Sheet 92 / 93

Dolphin







B

Luna近傍に配置

Fujitsu
Proprietary &
Confidential

Power/ PMU/ Etc1 (Battery1)

							TITLE	VB313AA
							DRAW. No.	C1CP302570-X2 CAST
Rev.	Date	Design	Check	Appr.	Description		FUJITSU LTD.	Sheet 93 / 93
Design	06/07/04	Mizukami	Check	Urita		Appr.	Hasegawa	