GILIA Main Board Rev.03

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Revision History

Rev	Date	Description

Index - Power Block

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87	Power / Blank
88	Power / DDC / VGACORE
89	Power / DDC / VGAMEM
90	Power / LDO / VGA
91	Power / Blank

System Resorce Assign

PCI BUS NUMBER = #0

IDSEL	Dev.ID	Device
AD16	00h	GMCH(HOST/DRAM BRIDGE)
AD17	01h	GMCH(AGP BRIDGE)
AD18	02h	Unused
---	---	---
	1Dh	ICH7-M (USB2.0/USB1.1)
	1Eh	ICH7-M(Hub I/F to PCI Bridge)
	1Fh	ICH7-M(LPC,IDE,SMbus,ACZ)

PCI BUS NUMBER = #2

IDSEL	Dev.ID	Device
AD17	08h	Reserved for ICH7 (Internal LAN)
AD18	09h	On Board LAN
AD19	0Ah	PCIC
AD20	0Ch	On Board LAN
AD21	0Dh	MiniPCI
AD22	0Eh	IEEE1394
AD23	0Fh	---

PCI INTERRUPT

PCIINT#	Device
INT#0	PCIC
INT#1	IEEE1394 (TI)
INT#2 -7	Unused

PCI REQ#/GNT#

REQ#/GNT#	Device
REQ#0	PCIC
REQ#1	IEEE1394 (TI)
REQ#2	Unused
REQ#3	Unused
REQ#4	Unused
REQ#5	Unused

USB

Port#	JP-Retail	WW-Retail	JP-Corp.	WW-Corp.
USB0	System #0	<==	<==	<==
USB1	System #1	<==	<==	<==
USB2	System #2	<==	<==	<==
USB3	(Rsv)	(Rsv)	P-R	<==
USB4	ExpressCard	<==	<==	<==
USB5	BAY	<==	<==	MiniCard2
USB6	Fingerprint	<==	<==	<==
USB7	(Rsv)	(Rsv)	Felica	Bluetooth

SMBus

SMBCNT[2:0]	Device
0,0,0	DIMM SLOT-0/1
0,0,1	PMU
0,1,0	PLL
0,1,1	Thermal,SPWG, MiniCard 0/1

PCI Experss

Port#	Device
PCIE1	On Board LAN
PCIE2	ExpressCard
PCIE3	MiniCard1
PCIE4	MiniCard2/BAY

Please refer to the difinition table attached to the Nile system for part difinition of each system configrations.

実装される部品はモデルによっては回路図と異なるため、必ず添付の実装差分表を確認すること。

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REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	2006.01.26	DESIGN	Seki	CHECK Yamada APPR Miura

TITLE GILIA Main Board Rev.03
DRAW. NO. C1CP272450-X3 CUST.
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[BLOCK DIAGRAM]

CPR2

DVI CN

CRT CN

CPU

Yonah-2M
uFCPGA 478pin
P7 - 10

Thermal

FAN Controller
MAX6640 P49

Host166MHz/133MHz
SRC 100MHz
DREF 96MHz
ICH 48MHz
PCI 33MHz
Ref 14MHz

CK410M PLL
9LPR311AKLF
P5

CRT CN P56

RGB SW
PI5V330S P50

FSB 1.05V 667MHz

Analog RGB

LCD CN P58

LVDS XGA/SXGA+

MCH
945PM/GM
FCBGA 1257pin
Calistoga PM
P11 - 18

DDR2 1.8V 667MHz

DIMM Slot 1
P19

DDR2 1.8V 667MHz

DIMM Slot 2
P20

S-OUT P61

TMDS

PCIE x16

HDCP Key
CH9901 P50

External VGA
GammaChrome
ULP MPM-64
P64 - 67

DMI x4

DVI Transmtter
CH7312 P50

SDVO

ICH
82801GBM/GHM
BGA 652pin
ICH7M
Base SKU

PCI-E x1 1.5V

G-LAN
88E8055 P63

PCI-E x1 1.5V

ExpressCard P35

PC Card P35

BAY Board

PCI-E x1 1.5V

Mini Card Slot1
W-LAN P45

BAY Board

SD/MS/xD Slot
P33

PCI-E x1 1.5V

BAY TV(PCIE)

Cardbus

SmartCard Slot
P33

BAY Board

SATA HDD

SATA

Bridge
88SA8040

PATA HDD

IDE

ODD

PCI 3.3V 33MHz

PCIC
OZ711MP1
OZ711MS1
P31-P32

BAY TV

IEEE1394 CN P61

Audio OUT P59

USB CN 0

USB:0

USB CN 1

USB:1

Azalia

Audio AMP
LM4817 P39

Speaker P59

USB CN 2

USB:2

MDC 1.5 P53

Audio Codec
ALC262 P38

Audio OUT(PR)

USB:3

USB HUB(CPR2)
uPD720114

USB Board

CPR2

Audio IN(PR)

LPC 3.3V 33MHz

USB:4

ExpressCard P35

Super I/O
LPC47N217 P42

ASIC
BENN P46

KBC/PMU
LUNA2 P82-83

TPM V1.2(Main/Sub)
SLB9635TT1.2 P36

USB:5

Fingerprint Sensor
AES2501A

FPS Board

Audio IN P59

CPR2

BAY Board

USB:6

BAY TV/FDD

RS232C Drv.
P42

Serial Port

ST-LCD P62

USB:7

Bluetooth P52

Parrarell Port

Keyboard P60

Appl/Sec Button P62

Mini Card Slot2
UMTS P45

IR port

PS/2 CN

FlatPoint

StickPoint

FeliCa

USB Board

CPR2

BAY Board

SPI

Sim Slot

USB Board

BIOS ROM
M25P80 P29

BIOS ROM
M25P80 P29

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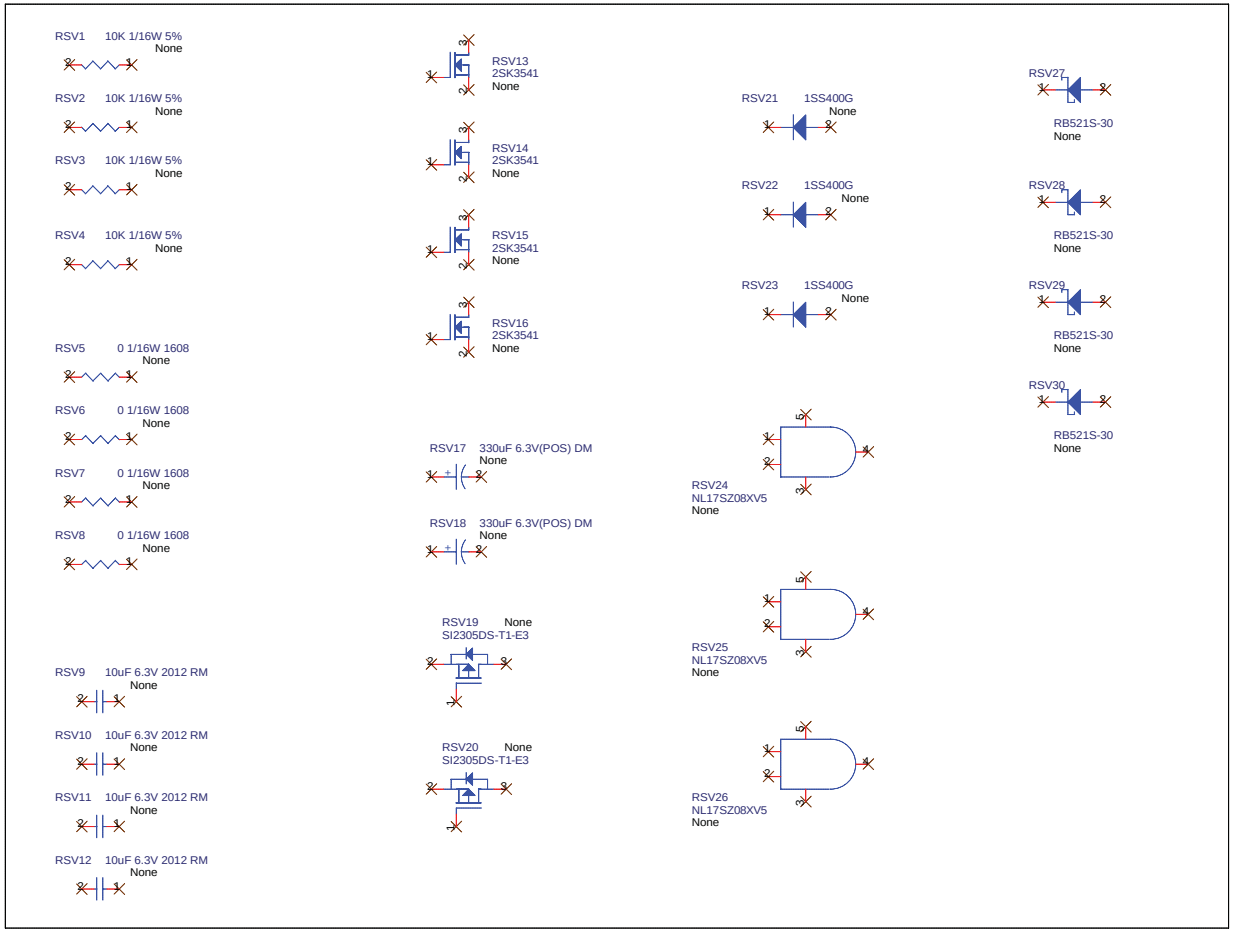
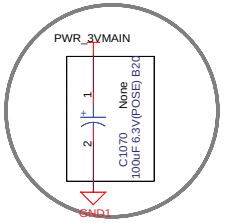


$V01L10
Added parts



$V01L11
Added part

[Reserved parts]

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$V02L01
Added parts(DemitasNX Resuslt)

[EMI]

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FSB	FSA	Function
0	0	Reserved
0	1	133MHz Host CLK
1	0	200MHz Host CLK
1	1	166MHz Host CLK

PLL_FSAについては、分岐するまでの配線幅を2倍にすること

#プラットフォーム回路図よりネット名変更

#TV-BAY挿入によるCLK_REQ検討

#DPST時は不要なのでUMAモデル未実装？

$V03L03 Changed part to pad

$V01L13 Changed part RM1

$V02L01 Changed connection

$V01L13 Changed parts

$V03L04 Changed part

Option pin	target	Low	High
SEL_LCDCLK#/PCICLK4	58pin	LCDCLK	SRC0
SEL_27MHz/PCICLK3	57pin	DOT96	27MHz

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[PLL-1]

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※このページの部品はPLL近傍に配置すること

※のパターンのライン・インピーダンスは55Ωで引くこと。(4mil幅)
また、各対のクロックライン同士の間隔(CPUCLK0,CPUCLK0#間など3対)は信号線間インピーダンス100Ωで引くこと。(9mil幅)

$V01L13
Changed parts
Dumping Resistor: 33ohm -> 0ohm

5 CLK_166_CPU0+_C → R21 0 1/16W → CLK_166_CPU0+ 7
5 CLK_166_CPU0-_C → R22 0 1/16W → CLK_166_CPU0- 7
5 CLK_166_CPU1+_C → R24 0 1/16W → CLK_166_CPU1+ 11
5 CLK_166_CPU1-_C → R25 0 1/16W → CLK_166_CPU1- 11

※

R28 None 49.9 1/16W 1%
R29 None 49.9 1/16W 1%
R30 None 49.9 1/16W 1%
R31 None 49.9 1/16W 1%
GND1

5 CLK_96+_27 → R20 0 1/16W No EXTVGA → CLK_96_DREF+ 12
5 CLK_96-_27 → R23 0 1/16W No EXTVGA → CLK_96_DREF- 12

R26 None 49.9 1/16W 1%
R27 None 49.9 1/16W 1%
GND1

5 CLK_100_SSC+ → R32 0 1/16W → CLK_DREFSSC+ 12
5 CLK_100_SSC- → R33 0 1/16W → CLK_DREFSSC- 12
5 CLK_100_SRC1+ → EXTVGA R34 0 1/16W → CLK_100_EXTVGA+ 64
5 CLK_100_SRC1- → EXTVGA R35 0 1/16W → CLK_100_EXTVGA- 64

5 CLK_100_SRC2+ → R36 0 1/16W → CLK_100_3GPLL+ 12
5 CLK_100_SRC2- → R37 0 1/16W → CLK_100_3GPLL- 12
5 CLK_100_SRC3+ → R38 0 1/16W → CLK_100_SATA+ 22
5 CLK_100_SRC3- → R39 0 1/16W → CLK_100_SATA- 22

5 CLK_100_SRC4+ → R40 0 1/16W → CLK_100_ICH+ 23
5 CLK_100_SRC4- → R41 0 1/16W → CLK_100_ICH- 23
5 CLK_100_SRC5+ → R42 0 1/16W → CLK_100_PELAN+ 43,63
5 CLK_100_SRC5- → R43 0 1/16W → CLK_100_PELAN- 43,63

5 CLK_100_SRC6+ → R44 0 1/16W → CLK_100_MINICARD0+ 45
5 CLK_100_SRC6- → R45 0 1/16W → CLK_100_MINICARD0- 45
5 CLK_100_SRC7+ → R46 0 1/16W → CLK_100_EXCARD+ 35
5 CLK_100_SRC7- → R47 0 1/16W → CLK_100_EXCARD- 35

$V01L08
Changed connection

$V01L13
Mount -> Reserve

5 CLK_100_SRC8+ → R48 0 1/16W 1 2 MINIC_2nd None → CLK_100_MINICARD1+ 45
5 CLK_100_SRC8- → R49 0 1/16W 1 2 MINIC_2nd None → CLK_100_MINICARD1- 45

R740 0 1/16W 1 2 TV-PCIE → CLK_100_PCIETV+ 51
R741 0 1/16W 1 2 TV-PCIE → CLK_100_PCIETV- 51

※分岐によるスタブは最短とすること。

$V01L02
Added parts

R50 None 49.9 1/16W 1%
R51 None 49.9 1/16W 1%
R52 None 49.9 1/16W 1%
R53 None 49.9 1/16W 1%
R54 None 49.9 1/16W 1%
R55 None 49.9 1/16W 1%
R56 None 49.9 1/16W 1%
R57 None 49.9 1/16W 1%
R58 None 49.9 1/16W 1%
R59 None 49.9 1/16W 1%
R60 None 49.9 1/16W 1%
R61 None 49.9 1/16W 1%
R62 None 49.9 1/16W 1%
R63 None 49.9 1/16W 1%
R64 None 49.9 1/16W 1%
R65 None 49.9 1/16W 1%
R66 None 49.9 1/16W 1%
R67 None 49.9 1/16W 1%
R742 None 49.9 1/16W 1%
R743 None 49.9 1/16W 1%
GND1

$V01L02
Added parts

[PLL-2]

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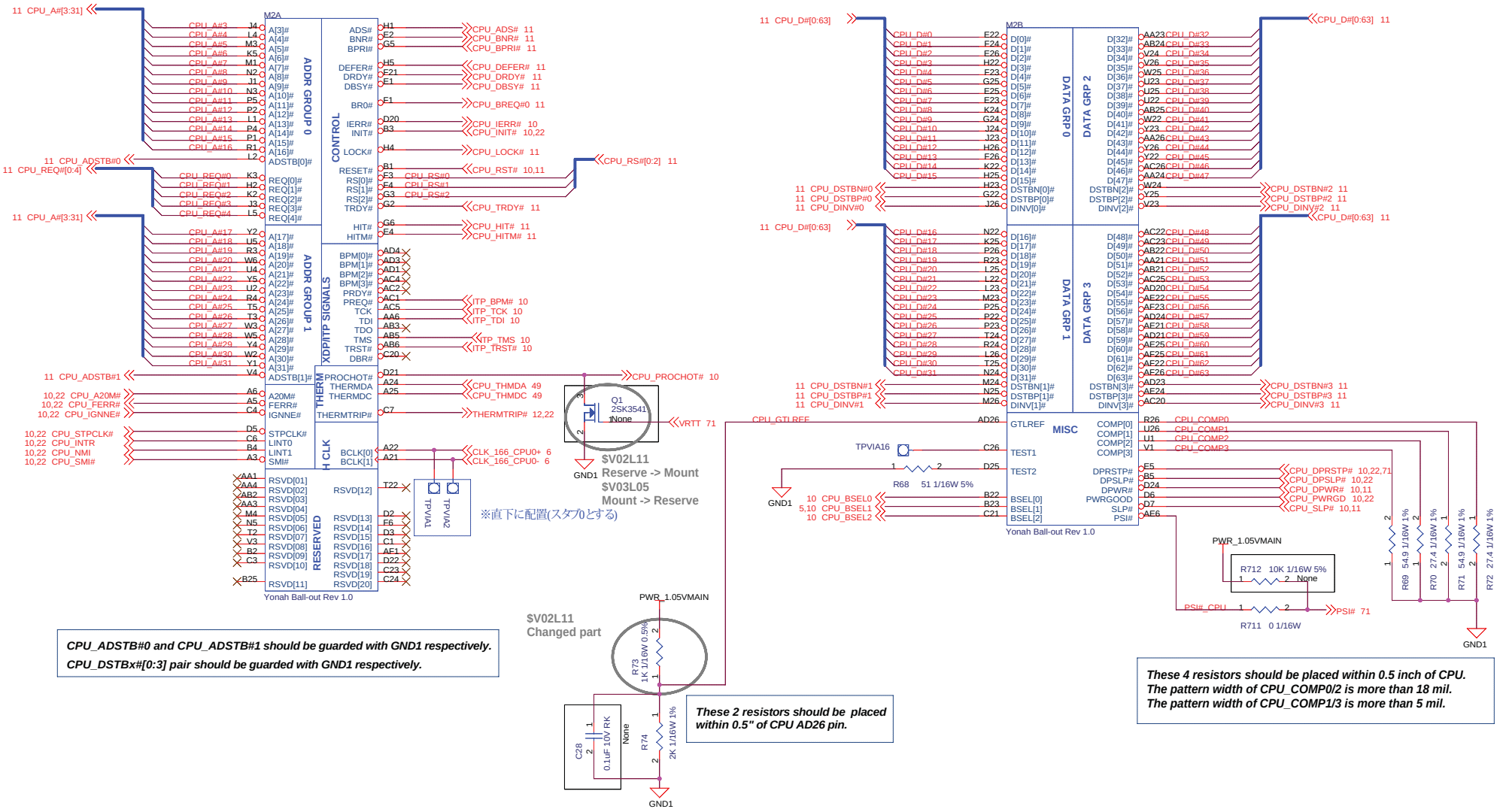

CPU_ADSTB#0 and CPU_ADSTB#1 should be guarded with GND1 respectively.
CPU_DSTBx#[0:3] pair should be guarded with GND1 respectively.

These 2 resistors should be placed within 0.5" of CPU AD26 pin.

These 4 resistors should be placed within 0.5 inch of CPU.
The pattern width of CPU_COMP0/2 is more than 18 mil.
The pattern width of CPU_COMP1/3 is more than 5 mil.

[CPU-1]

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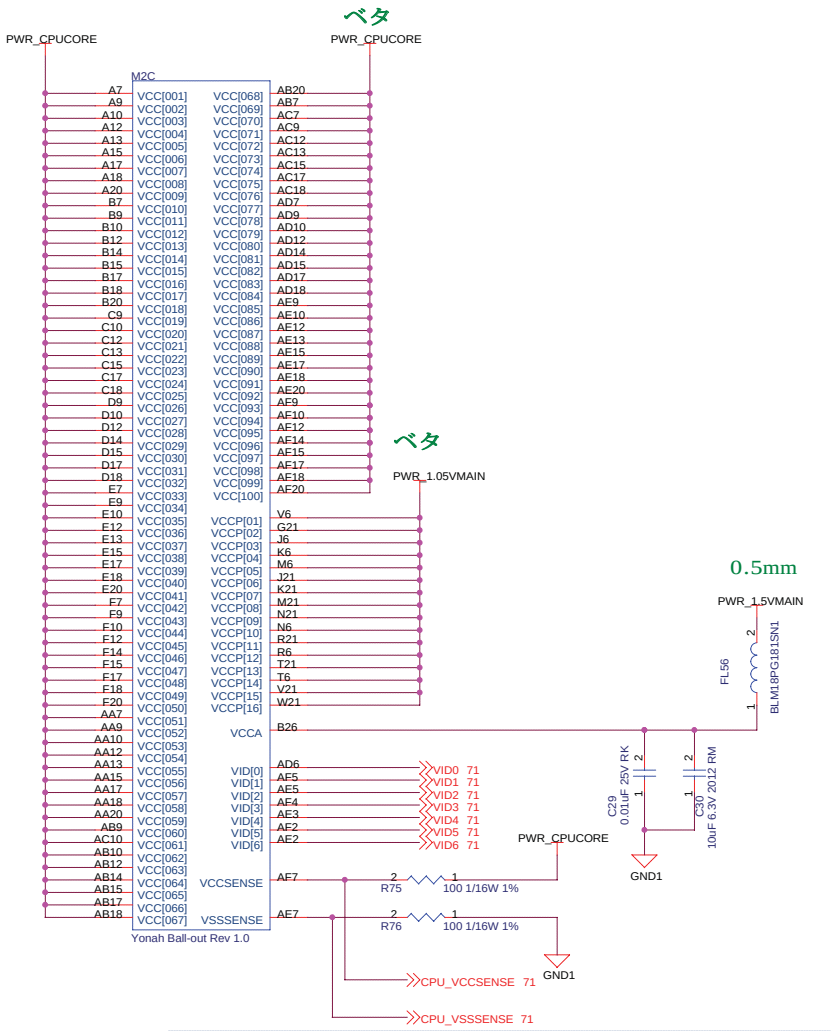
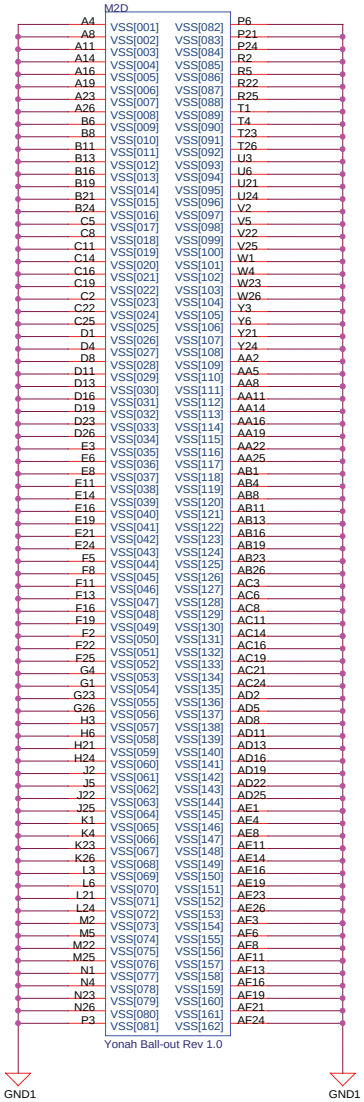


VCCSENSE, VSSSENSEは線幅0.2mmでかつ平行に配線すること。



IMVP-6

VID6	VID5	VID4	VID3	VID2	VID1	VID0	V
0	0	0	0	0	0	0	15000
0	0	0	0	0	0	1	14875
0	0	0	0	0	1	0	14750
0	0	0	0	0	1	1	14625
0	0	0	0	1	0	0	14500
0	0	0	0	1	0	1	14375
0	0	0	0	1	1	0	14250
0	0	0	0	1	1	1	14125
0	0	0	1	0	0	0	14000
0	0	0	1	0	0	1	13875
0	0	0	1	0	1	0	13750
0	0	0	1	0	1	1	13625
0	0	0	1	1	0	0	13500
0	0	0	1	1	0	1	13375
0	0	0	1	1	1	0	13250
0	0	0	1	1	1	1	13125
0	0	1	0	0	0	0	13000
0	0	1	0	0	0	1	12875
0	0	1	0	0	1	0	12750
0	0	1	0	0	1	1	12625
0	0	1	0	1	0	0	12500
0	0	1	0	1	0	1	12375
0	0	1	0	1	1	0	12250
0	0	1	0	1	1	1	12125
0	0	1	1	0	0	0	12000
0	0	1	1	0	0	1	11875
0	0	1	1	0	1	0	11750
0	0	1	1	0	1	1	11625
0	0	1	1	1	0	0	11500
0	0	1	1	1	0	1	11375
0	0	1	1	1	1	0	11250
0	0	1	1	1	1	1	11125
0	1	0	0	0	0	0	11000
0	1	0	0	0	0	1	10875
0	1	0	0	0	1	0	10750
0	1	0	0	0	1	1	10625
0	1	0	0	1	0	0	10500
0	1	0	0	1	0	1	10375
0	1	0	0	1	1	0	10250
0	1	0	0	1	1	1	10125
0	1	0	1	0	0	0	10000
0	1	0	1	0	0	1	09875
0	1	0	1	0	1	0	09750
0	1	0	1	0	1	1	09625
0	1	0	1	1	0	0	09500
0	1	0	1	1	0	1	09375
0	1	0	1	1	1	0	09250
0	1	0	1	1	1	1	09125
0	1	1	0	0	0	0	09000
0	1	1	0	0	0	1	08875
0	1	1	0	0	1	0	08750
0	1	1	0	0	1	1	08625
0	1	1	0	1	0	0	08500
0	1	1	0	1	0	1	08375
0	1	1	0	1	1	0	08250
0	1	1	0	1	1	1	08125
0	1	1	1	0	0	0	08000
0	1	1	1	0	0	1	07875
0	1	1	1	0	1	0	07750
0	1	1	1	0	1	1	07625
0	1	1	1	1	0	0	07500
0	1	1	1	1	0	1	07375
0	1	1	1	1	1	0	07250
0	1	1	1	1	1	1	07125
1	0	0	0	0	0	0	07000
1	0	0	0	0	0	1	06875
1	0	0	0	0	1	0	06750
1	0	0	0	0	1	1	06625
1	0	0	0	1	0	0	06500
1	0	0	0	1	0	1	06375
1	0	0	0	1	1	0	06250
1	0	0	0	1	1	1	06125
1	0	0	1	0	0	0	06000
1	0	0	1	0	0	1	05875
1	0	0	1	0	1	0	05750
1	0	0	1	0	1	1	05625
1	0	0	1	1	0	0	05500
1	0	0	1	1	0	1	05375
1	0	0	1	1	1	0	05250
1	0	0	1	1	1	1	05125
1	0	1	0	0	0	0	05000
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	1	00000

[CPU-2 Power/GND]

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TITLE GILIA Main Board Rev.03
DRAW. NO. C1CP272450-X3 CUST.
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$V02L08
Changed connection

CPU
Yonah

PWR_CPUCORE

C31 22uF 6.3V 2012 RM
C32 22uF 6.3V 2012 RM
C33 22uF 6.3V 2012 RM
C34 22uF 6.3V 2012 RM
C35 22uF 6.3V 2012 RM
C36 22uF 6.3V 2012 RM
C37 22uF 6.3V 2012 RM
C968 0.1uF 10V RK
C969 0.1uF 10V RK
C970 0.1uF 10V RK
C971 0.1uF 10V RK

C42 22uF 6.3V 2012 RM
C43 22uF 6.3V 2012 RM
C44 22uF 6.3V 2012 RM
C45 22uF 6.3V 2012 RM
C46 22uF 6.3V 2012 RM
C47 22uF 6.3V 2012 RM
C48 22uF 6.3V 2012 RM
C972 0.1uF 10V RK
C973 0.1uF 10V RK
C974 0.1uF 10V RK
C975 0.1uF 10V RK

C52 22uF 6.3V 2012 RM
C53 22uF 6.3V 2012 RM
C54 22uF 6.3V 2012 RM
C55 22uF 6.3V 2012 RM
C56 22uF 6.3V 2012 RM
C57 22uF 6.3V 2012 RM
C58 22uF 6.3V 2012 RM
C976 0.1uF 10V RK
C977 0.1uF 10V RK
C978 0.1uF 10V RK
C979 0.1uF 10V RK

C62 22uF 6.3V 2012 RM
C63 22uF 6.3V 2012 RM
C64 22uF 6.3V 2012 RM
C65 22uF 6.3V 2012 RM
C66 22uF 6.3V 2012 RM
C67 22uF 6.3V 2012 RM
C68 22uF 6.3V 2012 RM
C980 0.1uF 10V RK
C981 0.1uF 10V RK
C982 0.1uF 10V RK
C983 0.1uF 10V RK

GND1

PWR_1.05VMAIN

C73 0.1uF 10V RK
C74 0.1uF 10V RK
C75 0.1uF 10V RK
C76 0.1uF 10V RK
C77 0.1uF 10V RK
C78 0.1uF 10V RK
C984 10uF 6.3V 2012 RM
C985 10uF 6.3V 2012 RM

GND1

上記のコンデンサはCPUの各電源ピンの近傍に配置すること。

CPU Socket

7x 10uF + 3x 0.1uF
7x 10uF + 3x 0.1uF
7x 10uF + 3x 0.1uF
7x 10uF + 3x 0.1uF

Secondary Side

CORE電源のコンデンサについて配置が困難な場合は、
場所、数について要相談。

※下記の抵抗/コンデンサの組については、
CPU直下L1層のPWR_CPUCOREのプレーンの
4隅に配置すること

PWR_CPUCORE
PWR_CPUCORE
PWR_CPUCORE
PWR_CPUCORE

C79 None 0.1uF 10V RK
C80 None 0.1uF 10V RK
C81 None 0.1uF 10V RK
C82 None 0.1uF 10V RK
R707 None 10 1/16W 5%
R708 None 10 1/16W 5%
R709 None 10 1/16W 5%
R710 None 10 1/16W 5%

GND1
GND1
GND1
GND1

[CPU3 CAP]

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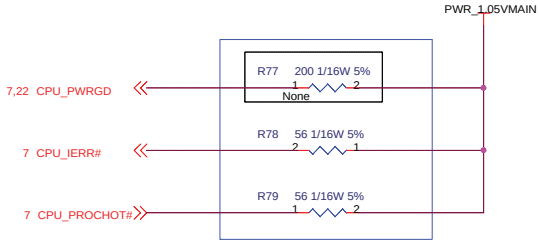
REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	2006.01.26	Seki	Yamada	Miura	

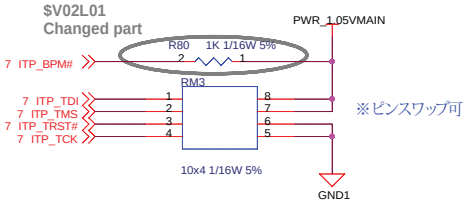
TITLE GILIA Main Board Rev.03
DRAW. NO. C1CP272450-X3
CUST.
FUJITSU LTD.
SHEET 9 / 91



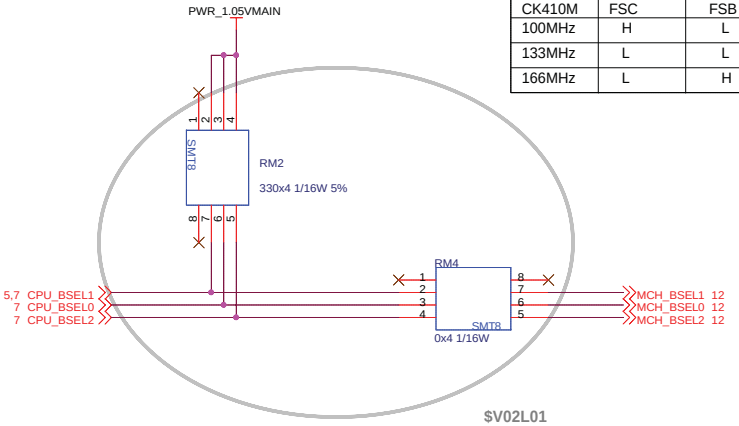
※CPUコネクタの 近くに置くこと

FSB Frequency	BSEL 2	BSEL 1	BSEL 0
533MHz	L	L	H
667MHz	L	H	H

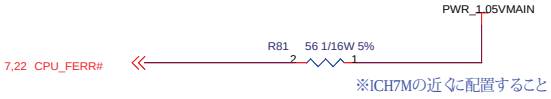
CPU CK410M	BSEL2 FSC	BSEL1 FSB	BSEL0 FSA
100MHz	H	L	H
133MHz	L	L	H
166MHz	L	H	H



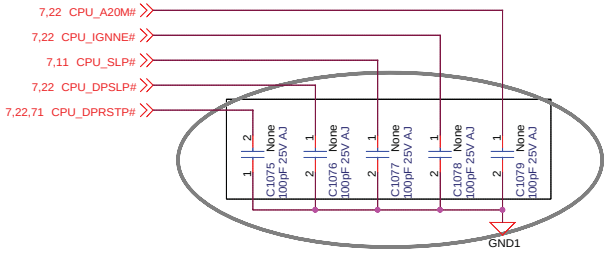
※ピンスワップ可



$V02L01
Changed parts

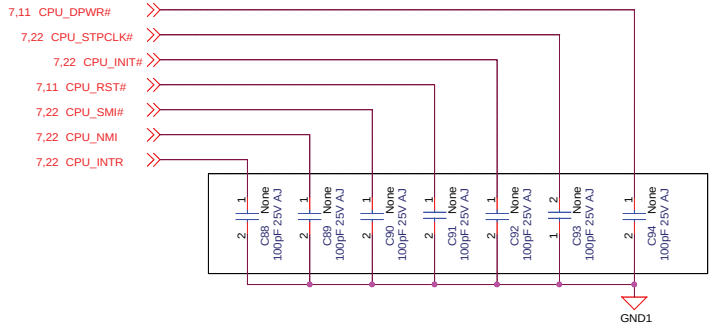


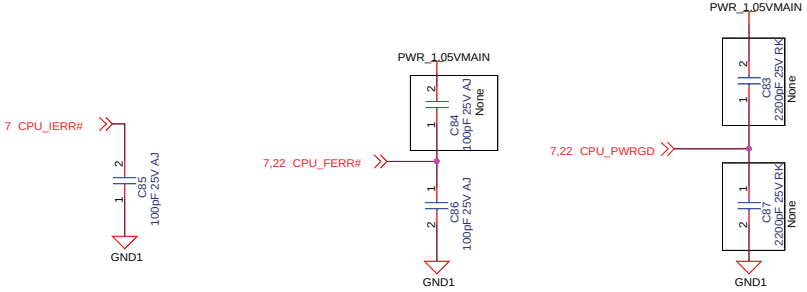
※ICH7Mの近くに配置すること



$V02L01
Added parts

※CPUの端子直近に配置すること





[CPU-4 Pull-up/Pull-down]

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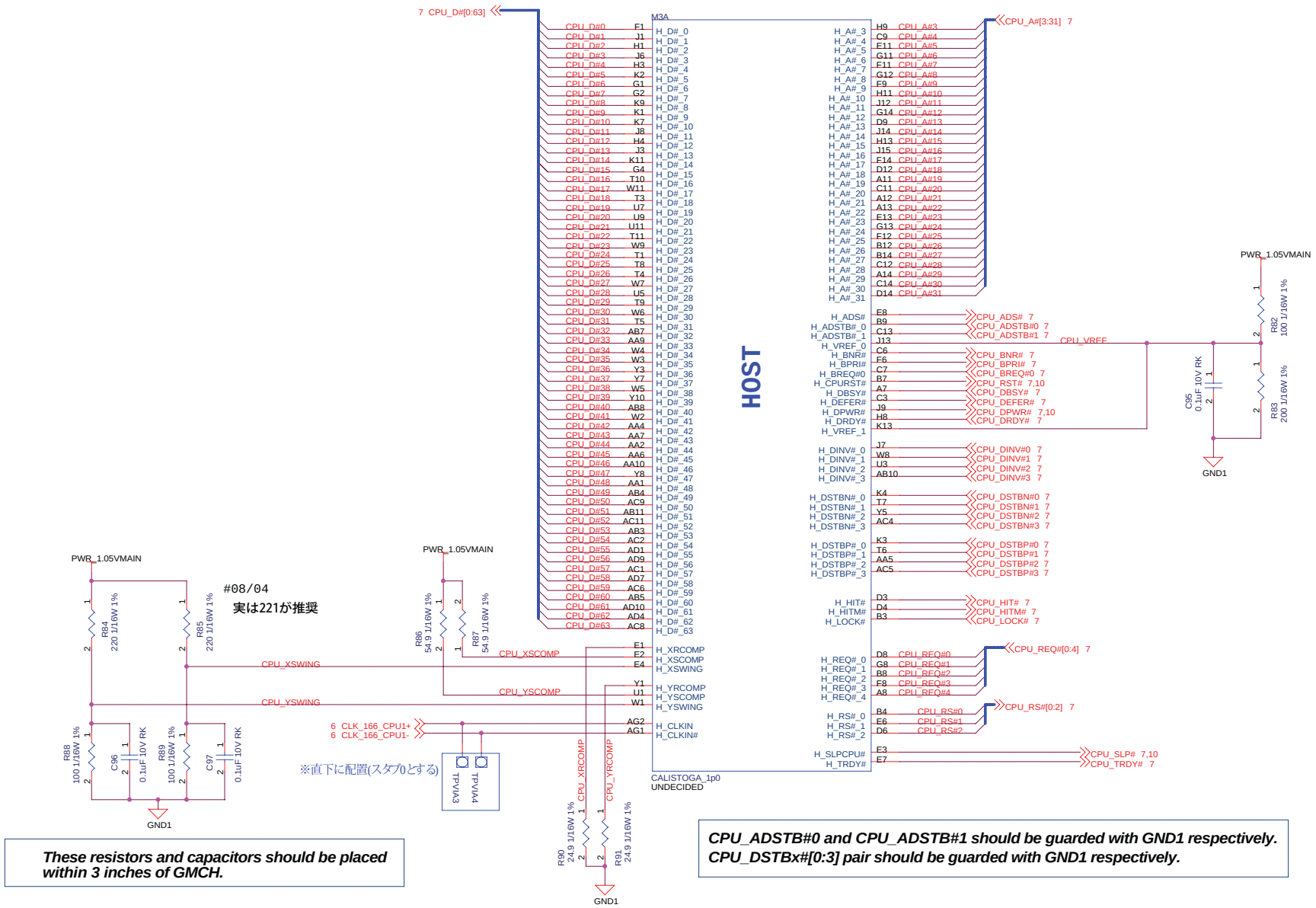
REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE 2006.01.26	DESIGN Seki	CHECK Yamada	APPR Miura	

TITLE GILIA Main Board Rev.03
DRAW. NO. C1CP272450-X3 CUST.
FUJITSU LTD. SHEET 10 / 91



These resistors and capacitors should be placed within 3 inches of GMCH.

CPU_ADSTB#0 and CPU_ADSTB#1 should be guarded with GND1 respectively.
CPU_DSTBx#[0:3] pair should be guarded with GND1 respectively.

[GMCH-1]

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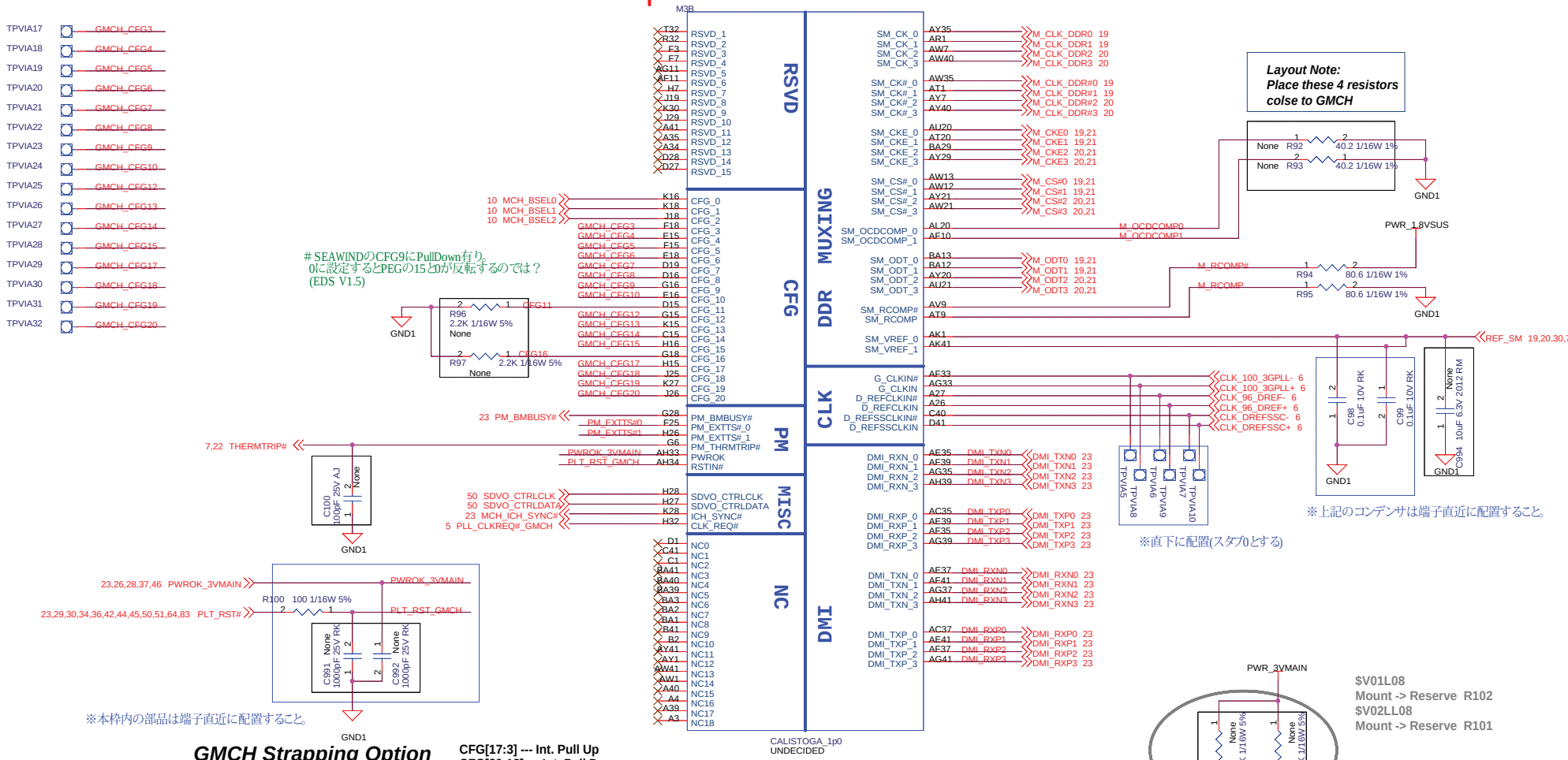
REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	2006.01.26	Seki	Yamada	Miura	

TITLE GILIA Main Board Rev.03
DRAW. NO. C1CP272450-X3 CUST.
FUJITSU LTD. SHEET 11 / 91



GMCH Strapping Option

CFG[17:3] --- Int. Pull Up
CFG[20:18] --- Int. Pull Down

PIN	Function
CFG5 (DMI x2 Select)	Low = DMI x 2 High = DMI x 4 (Default)
CFG6 (Calistoga Select)	Low = Reserved High = Calistoga (Default)
CFG7 (CPU Strap)	Low = Reserved High = Mobile CPU (Default)
CFG9 (PCI-E Lane Reversal)	Low = Reverse Lanes High = Normal operation (Default)
CFG11 (FSB x4 Select)	Low = FSB x 4 High = FSB x 8 (Default)
CFG16 (FSB Dynamic ODT)	Low = Dynamic ODT Disabled High = Dynamic ODT Enabled (Default)
CFG18 (VCC Select)	Low = 1.05V (Default) High = 1.5V
CFG19 (DMI Lane Reversal)	Low = Normal (Default) High = Reverse Lanes
CFG20 (SDVO/PCIe concurrent)	Low = Only SDVO or PCI-E x1 Operational (Default) High = SDVO and PCIE x1 are Operating simultaneously

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[GMCH-2]

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	2006.01.26	Seki	Yamada	Miura	

TITLE GILIA Main Board Rev.03
DRAW. NO. C1CP272450-X3 CUST.
FUJITSU LTD. SHEET 12 / 91

Layout Note:
Place these resistors colse to GMCH

37 GM_BL_VOL
46 GM_BLEN

R103 100K 1/16W 5% None
R104 100K 1/16W 0.5%
本当は1%でもよい

PWR_3VMAIN
RM5
10Kx4 1/16W 5%

37 GM_LCDON
R107 4.7K 1/16W 5%
R106 1.2K 1/16W 0.5%

$V03L05
Changed part

M3C

LVDS
L_BKLTCTL
L_BKLTEN
L_CLKCTLA
L_CLKCTLB
L_DDC_CLK
L_DDC_DATA
L_IBG
L_VBG
L_VDDEN
L_VREFH
L_VREFL
LA_CLK#
LA_CLK
LB_CLK#
LB_CLK
LA_DATA#_0
LA_DATA#_1
LA_DATA#_2
LA_DATA_0
LA_DATA_1
LA_DATA_2
LB_DATA#_0
LB_DATA#_1
LB_DATA#_2
LB_DATA_0
LB_DATA_1
LB_DATA_2

55 LVDS_LC-_GMCH
55 LVDS_LC+_GMCH
55 LVDS_UC-_GMCH
55 LVDS_UC+_GMCH
55 LVDS_L0-_GMCH
55 LVDS_L1-_GMCH
55 LVDS_L2-_GMCH
55 LVDS_L0+_GMCH
55 LVDS_L1+_GMCH
55 LVDS_L2+_GMCH
55 LVDS_U0-_GMCH
55 LVDS_U1-_GMCH
55 LVDS_U2-_GMCH
55 LVDS_U0+_GMCH
55 LVDS_U1+_GMCH
55 LVDS_U2+_GMCH

TV_CVBS_GMCH
TV_S_Y_GMCH
TV_S_C_GMCH
R108 75 1/16W 1% S-OUT(GMCH)#
R109 150 1/16W 1%
R110 150 1/16W 1%

$V01L07
Changed part

TV
TV_DACA_OUT
TV_DACB_OUT
TV_DACC_OUT
TV_IREF
TV_IRTNA
TV_IRTNB
TV_IRTNC
R111 4.99k 1/16W 0.5%

VGA
CRT_BLUE
CRT_BLUE#
CRT_GREEN
CRT_GREEN#
CRT_RED
CRT_RED#
CRT_DDC_CLK
CRT_DDC_DATA
CRT_HSYNC
CRT_IREF
CRT_VSYNC
54 CRT_BLUE_GMCH
54 CRT_GREEN_GMCH
54 CRT_RED_GMCH
R113 150 1/16W 1%
R114 150 1/16W 1%
R115 150 1/16W 1%

$V01L07
Mount -> Reserve

37 CRT_DDCCLK_GMCH
37 CRT_DDCDAT_GMCH
37 CRT_HSYNC_GMCH
37 CRT_VSYNC_GMCH
R117 255 1/16W 1%

CALISTOGA_1p0
UNDECIDED

PCI-EXPRESS GRAPHICS
EXP_A_COMPI
EXP_A_COMPO
R105 24.9 1/16W 1%
PWR_1.5V_PCIE

EXP_A_RXN_0 ... EXP_A_RXN_15
PEG_RXN0 64 ... PEG_RXN15 64
EXP_A_RXP_0 ... EXP_A_RXP_15
PEG_RXP0 64 ... PEG_RXP15 64

EXP_A_TXN_0 ... EXP_A_TXN_15
EXP_A_TXN0 ... EXP_A_TXN15
EXP_A_TXP_0 ... EXP_A_TXP_15
EXP_A_TXP0 ... EXP_A_TXP15

C117 0.1uF 10V RK SDVO
C118 0.1uF 10V RK SDVO
C119 0.1uF 10V RK SDVO
C121 0.1uF 10V RK SDVO
SDVOB_RED# 50
SDVOB_GREEN# 50
SDVOB_BLUE# 50
SDVOB_CLK- 50

C127 0.1uF 10V RK SDVO
C129 0.1uF 10V RK SDVO
C130 0.1uF 10V RK SDVO
C132 0.1uF 10V RK SDVO
SDVOB_RED 50
SDVOB_GREEN 50
SDVOB_BLUE 50
SDVOB_CLK+ 50

EXP_A_TXN0 C101 ... EXP_A_TXN15 C140
0.1uF 10V RK EXTVGA
PEG_TXN0 64 ... PEG_TXN15 64
EXP_A_TXP0 C102 ... EXP_A_TXP15 C139
PEG_TXP0 64 ... PEG_TXP15 64

[GMCH-3 GFX]

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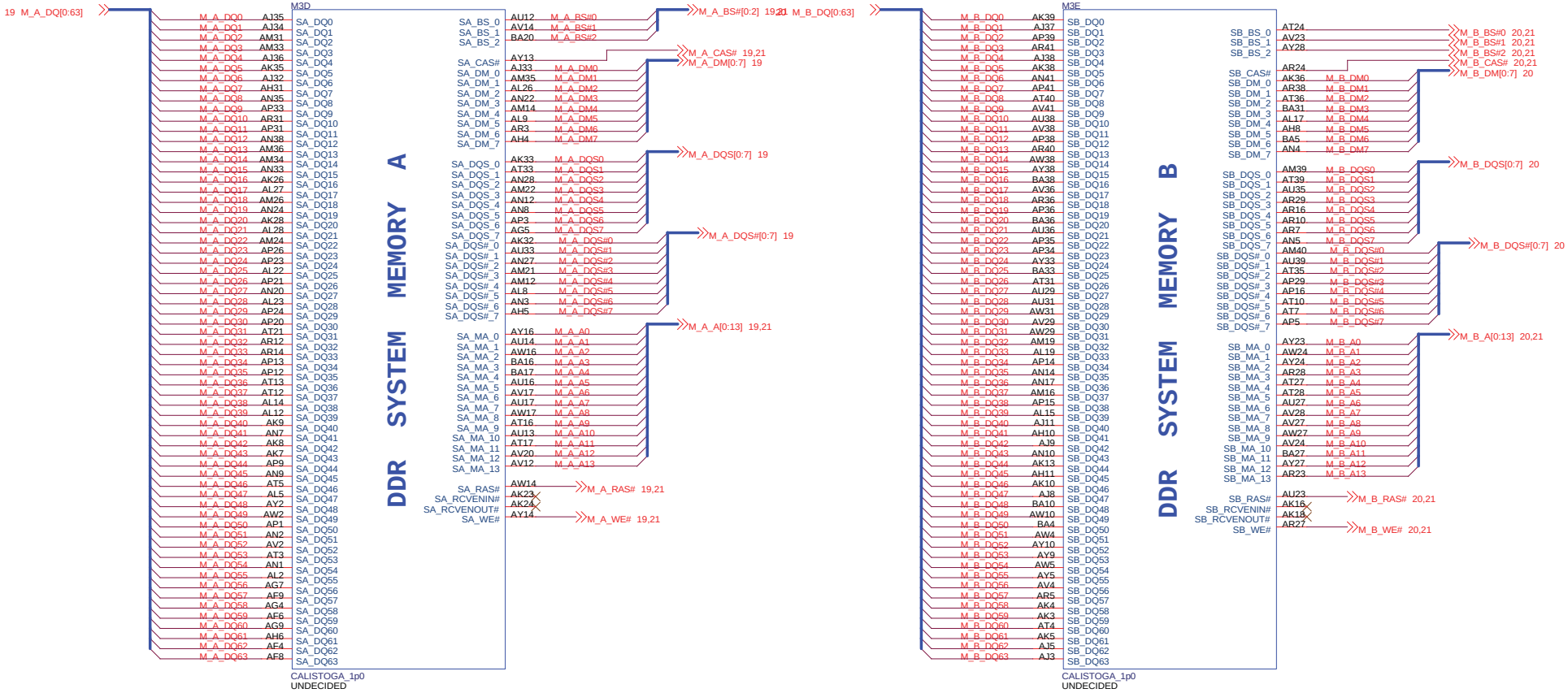
REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	2006.01.26	Seki	Yamada	Miura	

TITLE: GILIA Main Board Rev.03
DRAW. NO.: C1CP272450-X3
CUST.:
FUJITSU LTD.
SHEET 13 / 91



[GMCH-4 DDR2]

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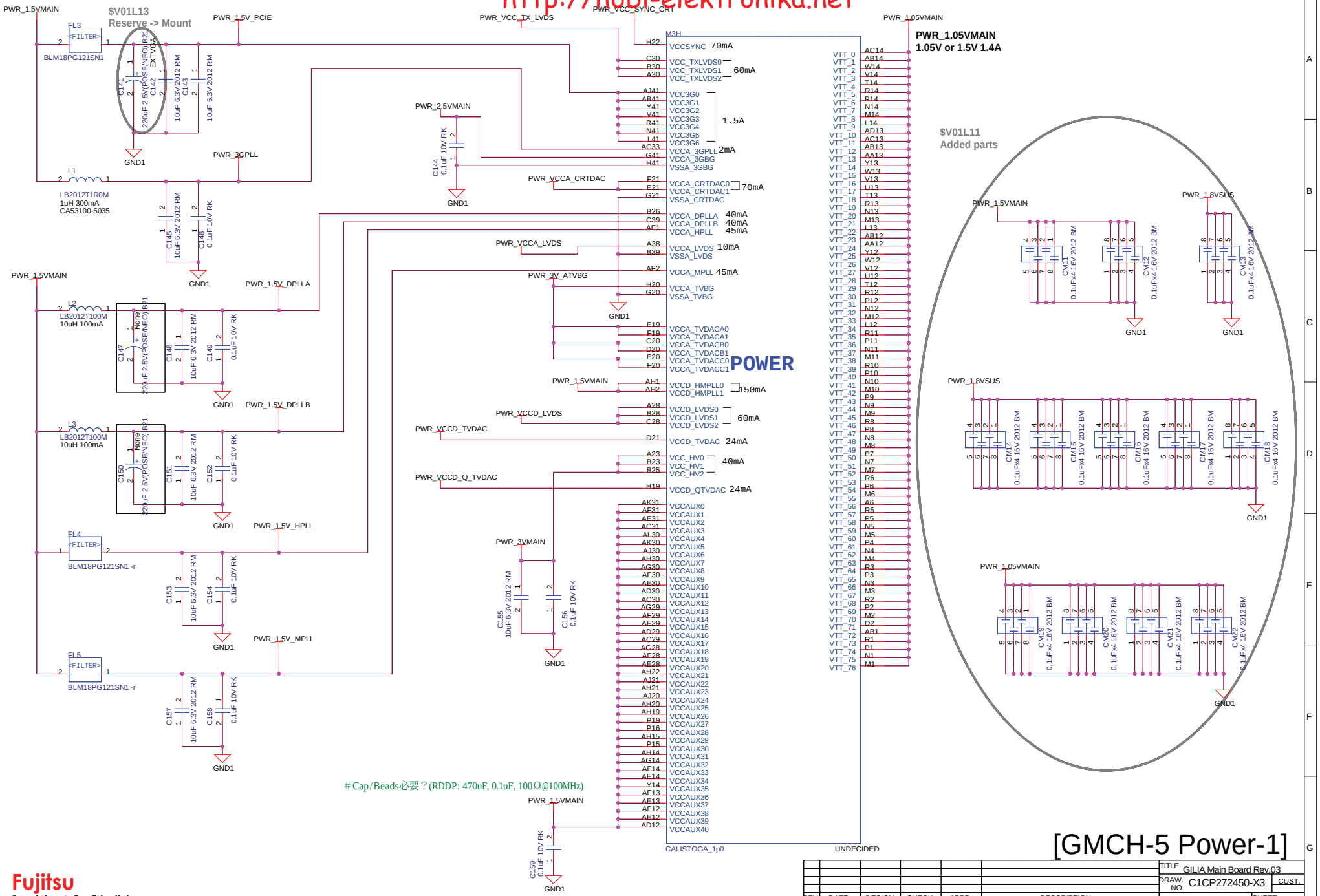
REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE 2006.01.26	DESIGN Seki	CHECK Yamada	APPR. Miura	

TITLE GILIA Main Board Rev.03
DRAW. NO. C1CP272450-X3 CUST.
FUJITSU LTD. SHEET 14 / 91



[GMCH-5 Power-1]

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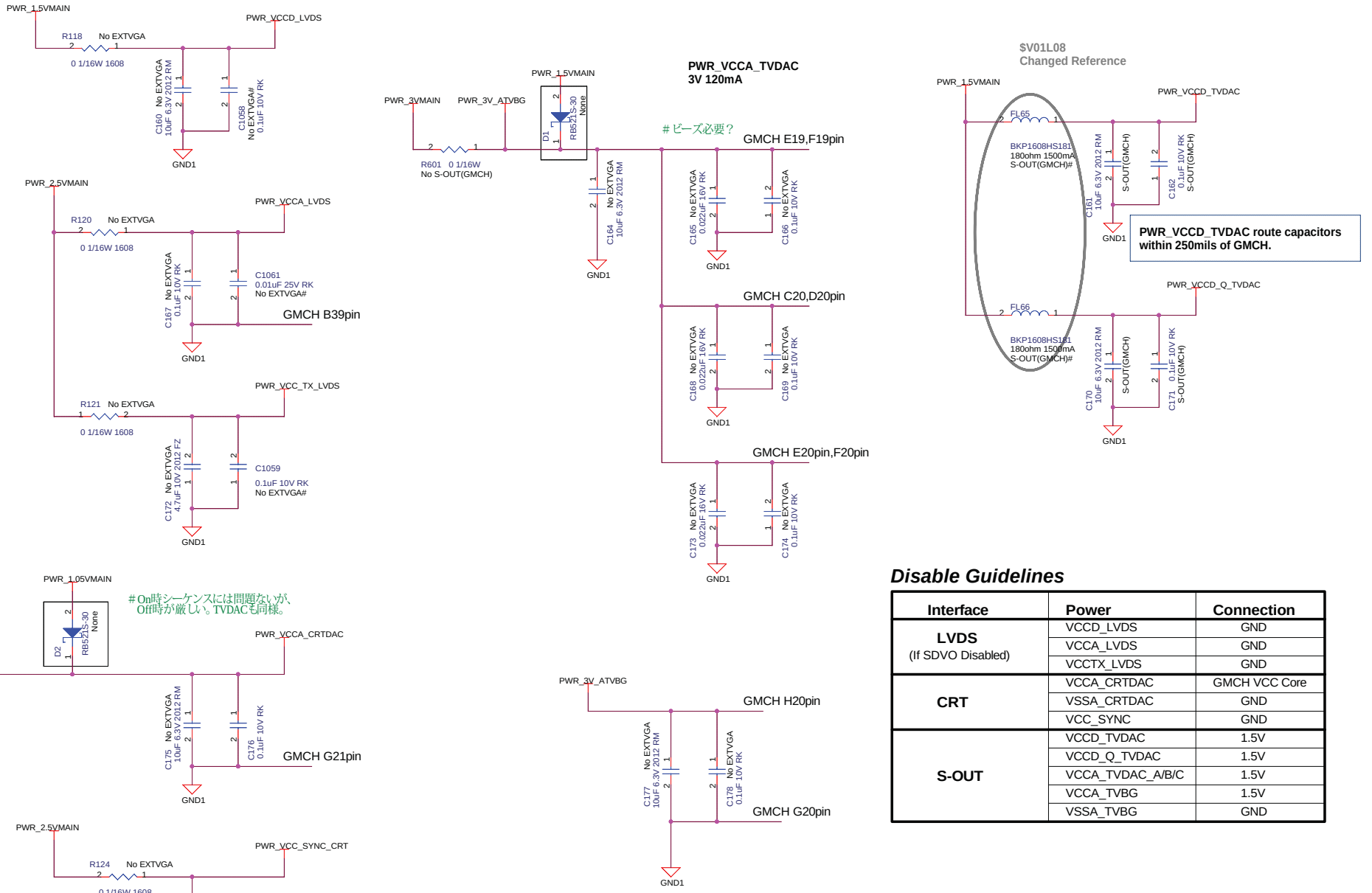
REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION		
	DATE	2006.01.26	DESIGN	Seki	CHECK	Yamada	APPR.	Miura

TITLE GILIA Main Board Rev.03
DRAW. NO. C1CP272450-X3 CUST.
FUJITSU LTD. SHEET 15 / 91



Disable Guidelines

Interface	Power	Connection
LVDS (If SDVO Disabled)	VCCD_LVDS	GND
	VCCA_LVDS	GND
	VCCTX_LVDS	GND
CRT	VCCA_CRTDAC	GMCH VCC Core
	VSSA_CRTDAC	GND
	VCC_SYNC	GND
S-OUT	VCCD_TVDAC	1.5V
	VCCD_Q_TVDAC	1.5V
	VCCA_TVDAC_A/B/C	1.5V
	VCCA_TVBG	1.5V
	VSSA_TVBG	GND

[GMCH-6 Power-2]

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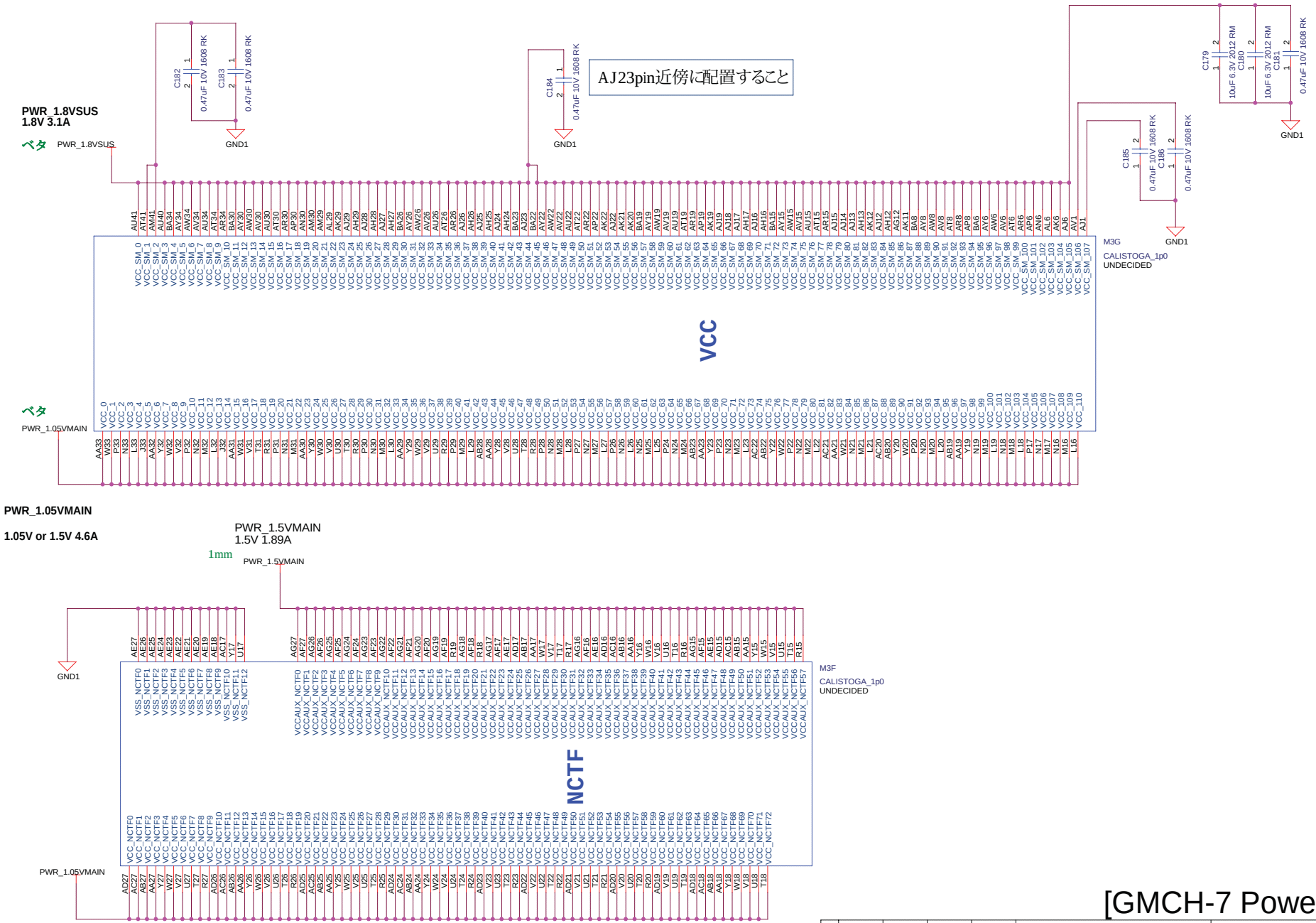
	DATE 2006.01.26	DESIGN Seki	CHECK Yamada	APPR. Miura	

TITLE GILIA Main Board Rev.03
DRAW. NO. C1CP272450-X3 CUST.
FUJITSU LTD. SHEET 16 / 91



[GMCH-7 Power-3]

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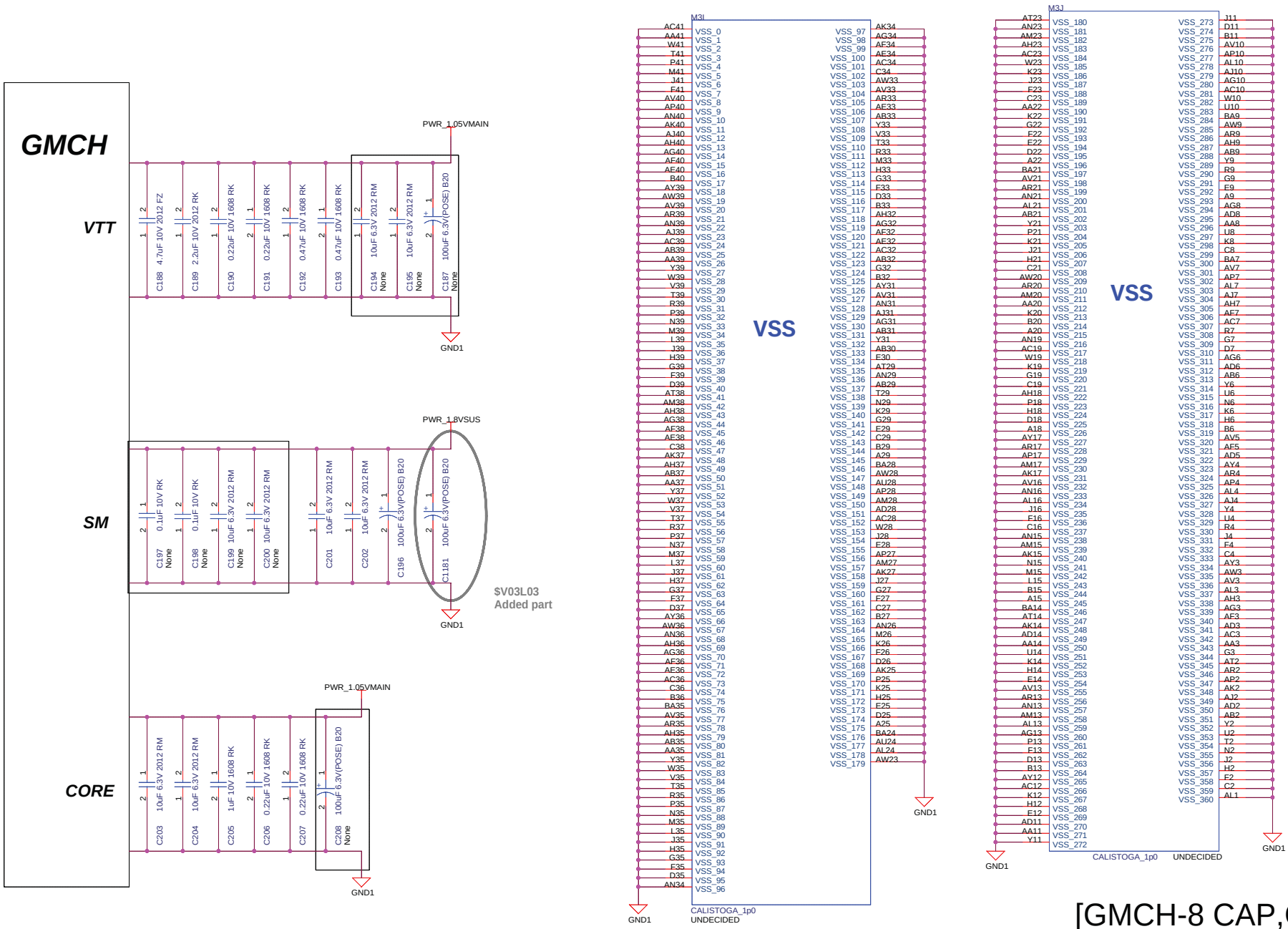
REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE 2006.01.26	DESIGN Seki	CHECK Yamada	APPR. Miura	

TITLE: GILIA Main Board Rev.03
DRAW. NO.: C1CP272450-X3
CUST.:
FUJITSU LTD.
SHEET 17 / 91



[GMCH-8 CAP,GND]

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REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE 2006.01.26	DESIGN Seki	CHECK Yamada	APPR. Miura	

TITLE GILIA Main Board Rev.03
DRAW. NO. C1CP272450-X3 CUST.
FUJITSU LTD. SHEET 18 / 91

ベタ PWR_1.8VSUS

※本項記載のコンデンサについては、DIMM Slotと同一の面に配置すること。

コンデンサ配置見直し予定
スナバ、EMI用CAP追加予定
バネ追加？

12,20,30,76 REF_SM
C209 0.1uF 10V RK
C210 1uF 10V 1608 RK
GND1

PWR_1.8VSUS
82pin C211 0.1uF 10V RK
88pin C212 0.1uF 10V RK
96pin C213 0.1uF 10V RK
104pin C214 0.1uF 10V RK
112pin C215 0.1uF 10V RK
118pin C216 0.1uF 10V RK
GND1

PWR_1.8VSUS
81pin C217 0.1uF 10V RK
87pin C218 0.1uF 10V RK
95pin C219 0.1uF 10V RK
113pin C220 0.1uF 10V RK
103pin C221 0.1uF 10V RK
117pin C222 0.1uF 10V RK
GND1

Bottom View
Slot1(A) Slot2(B)

PWR_1.8VSUS
C224 1uF 10V 1608 RK
C225 1uF 10V 1608 RK
C226 1uF 10V 1608 RK
C227 1uF 10V 1608 RK
C228 1uF 10V 1608 RK
C229 1uF 10V 1608 RK
C230 10uF 10V 2012 RK
C231 4.7uF 10V 2012 FZ None
GND1

$V03L04
Changed part/Reserve -> Mount
C230

CN1
DDR2 CN(RSV)
CA49500-1043

14 M_A_DQ[0:63]
M_A_DQS#[0:7] 14
M_A_DQS[0:7] 14
M_A_DM[0:7] 14
12,20,30,76 REF_SM
M_CLK_DDR0 12
M_CLK_DDR#0 12
DIMM_THRMSD 12,20
M_CLK_DDR1 12
M_CLK_DDR#1 12
12,21 M_CKE0
M_CKE1 12,21
14,21 M_A_BS#2
14,21 M_A_A12
14,21 M_A_A9
14,21 M_A_A8
14,21 M_A_A5
14,21 M_A_A3
14,21 M_A_A1
14,21 M_A_A10
14,21 M_A_BS#0
14,21 M_A_WE#
14,21 M_A_CAS#
12,21 M_CS#1
12,21 M_ODT1
M_A_BS#1 14,21
M_A_RAS# 14,21
M_CS#0 12,21
M_ODT0 12,21
M_A_A13 14,21
M_A_A11 14,21
M_A_A7 14,21
M_A_A6 14,21
M_A_A4 14,21
M_A_A2 14,21
M_A_A0 14,21
M_A_DM0
M_A_DM1 14
M_A_DM2 14
M_A_DM3 14
M_A_DM4 14
M_A_DM5 14
M_A_DM6 14
M_A_DM7 14
M_A_DQS0
M_A_DQS1
M_A_DQS2
M_A_DQS3
M_A_DQS4
M_A_DQS5
M_A_DQS6
M_A_DQS7
20,28,30 SMB_DATA_DIMM
20,28,30 SMB_CLK_DIMM
VDDSPD1
SA0
SA1
PWR_3VMAIN
C232 0.1uF 10V RK
GND1

※FG端子については、それぞれ2個以上のVIAを設けて
端子直近でGND1へと接続すること。

DIMM0 SPD address : A0

[DDR2 DIMM Slot-1]

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REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	2006.01.26	Seki	Yamada	Miura	

TITLE GILIA Main Board Rev.03
DRAW. NO. C1CP272450-X3
CUST.
FUJITSU LTD.
SHEET 19 / 91

ベタ PWR_1.8VSUS

12,19,30,76 REF_SM

14 M_B_DQ[63:0]

14 M_B_DQS#[7:0]

14 M_B_DQS[7:0]

CN2

M_B_DQ[63:0] 14

M_B_DQS#[7:0] 14

M_B_DQS[7:0] 14

M_B_DM2 14

M_B_DM[7:0] 14

M_B_DM0

M_CLK_DDR3 12

M_CLK_DDR#3 12

DIMM_THRMSD 12,19

M_B_DM3 14

14 M_B_DM1

M_B_DQS#1

M_B_DQS1

12,21 M_CKE2

M_CKE3 12,21

14,21 M_B_BS#2

14,21 M_B_A12

14,21 M_B_A9

14,21 M_B_A8

14,21 M_B_A5

14,21 M_B_A3

14,21 M_B_A1

M_B_A11 14,21

M_B_A7 14,21

M_B_A6 14,21

M_B_A4 14,21

M_B_A2 14,21

M_B_A0 14,21

14,21 M_B_A10

14,21 M_B_BS#0

14,21 M_B_WE#

M_B_BS#1 14,21

M_B_RAS# 14,21

M_CS#2 12,21

14,21 M_B_CAS#

12,21 M_CS#3

M_ODT2 12,21

M_B_A13 14,21

12,21 M_ODT3

M_B_DM4 14

$V01L04
Changed connection

14 M_B_DM5

M_B_DQS#5

M_B_DQS5

M_CLK_DDR2 12

M_CLK_DDR#2 12

M_B_DM6 14

14 M_B_DM7

M_B_DQS#7

M_B_DQS7

19,28,30 SMB_DATA_DIMM

19,28,30 SMB_CLK_DIMM

PWR_3VMAIN

VDDSPD0

SA0

SA1

R714 1K 1/16W 5%

DIMM1 SPD address : A4

C256 0.1uF 10V RK

DDR2 CN(STD)
CA49500-1042

GND1

Bottom View

Slot1(A) Slot2(B)

※本項記載のコンデンサについては、DIMM Slotと同一の面に配置すること。

コンデンサ配置見直し予定
スナバ、EMI用CAP追加予定
バネ追加？

12,19,30,76 REF_SM

C233 0.1uF 10V RK

C234 1uF 10V 1608 FZ

PWR_1.8VSUS

81pin C235 0.1uF 10V RK

87pin C236 0.1uF 10V RK

95pin C237 0.1uF 10V RK

113pin C238 0.1uF 10V RK

103pin C239 0.1uF 10V RK

117pin C240 0.1uF 10V RK

82pin C241 0.1uF 10V RK

88pin C242 0.1uF 10V RK

96pin C243 0.1uF 10V RK

104pin C244 0.1uF 10V RK

112pin C245 0.1uF 10V RK

118pin C246 0.1uF 10V RK

C248 1uF 10V 1608 RK

C249 1uF 10V 1608 RK

C250 1uF 10V 1608 RK

C251 1uF 10V 1608 RK

C252 1uF 10V 1608 RK

C253 1uF 10V 1608 RK

C254 None 4.7uF 10V 2012 FZ

C255 10uF 10V 2012 RK

$V03L04
Changed part/Reserve -> Mount
C255

※FG端子については、それぞれ2個以上のVIAを設けて
端子直近でGND1へと接続すること。

[DDR2 DIMM Slot-2]

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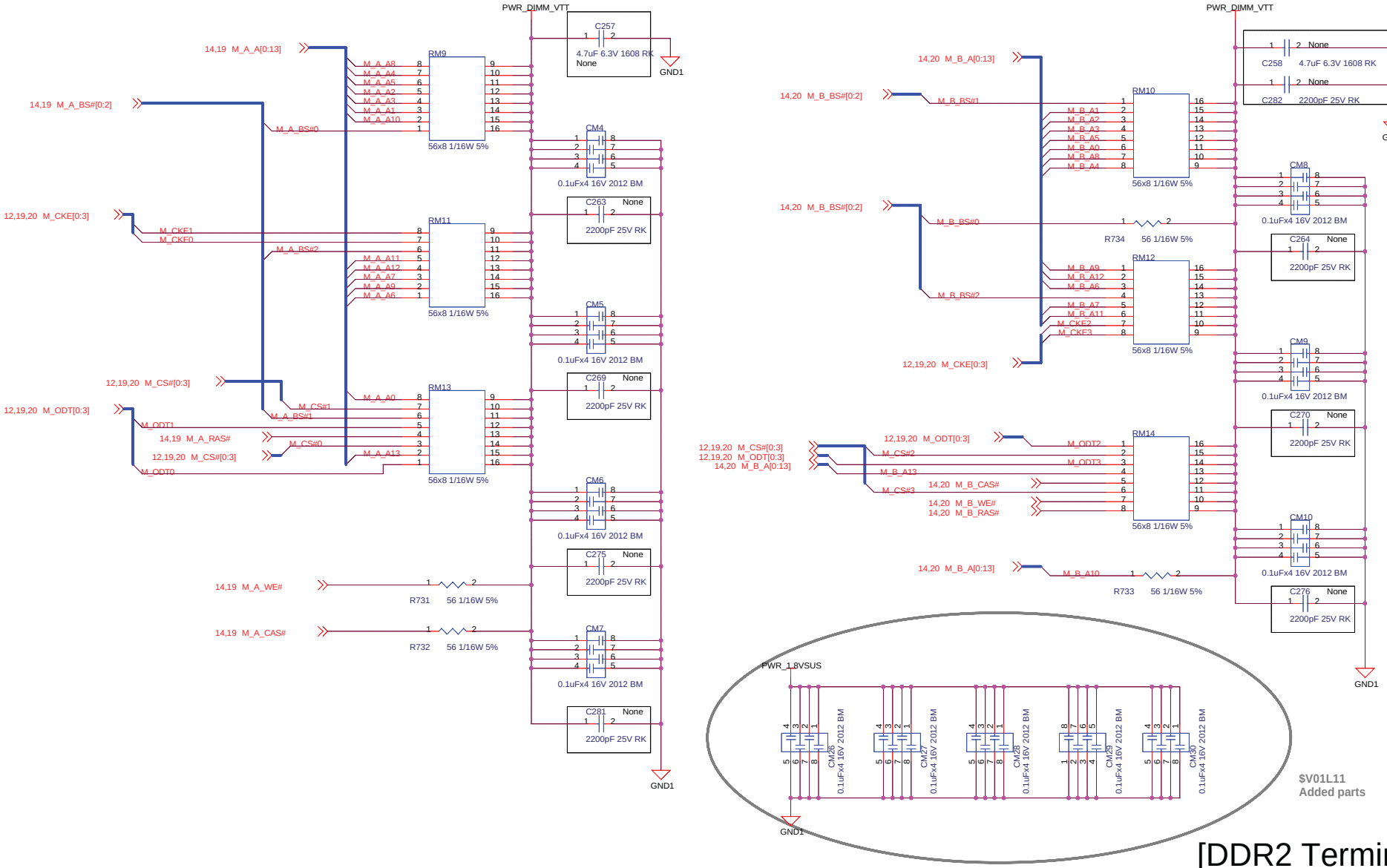
REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	2006.01.26	Seki	Yamada	Miura	

TITLE GILIA Main Board Rev.03
DRAW. NO. C1CP272450-X3 CUST.
FUJITSU LTD. SHEET 20 / 91

※本項の部品については、ピンスワップ可能である。
配線を最優先とし、適宜ピンスワップを行うこと。
また集合抵抗を個別抵抗へと分解してもよい。



[DDR2 Termination]

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REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	2006.01.26	Seki	Yamada	Miura	

TITLE: GILIA Main Board Rev.03
DRAW. NO.: C1CP272450-X3
CUST.:
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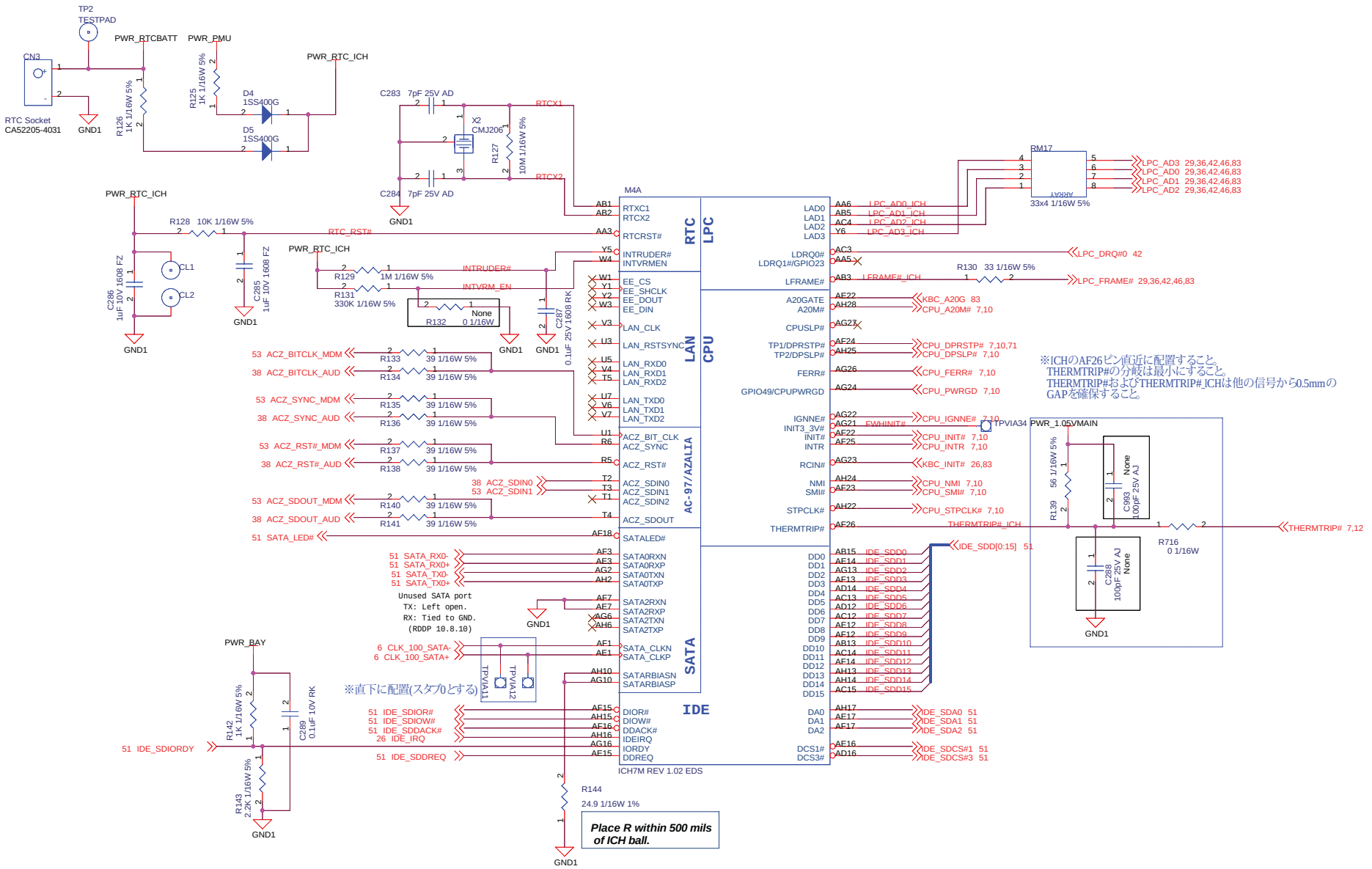

[ICH7M-1]

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	2006.01.26	Seki	Yamada	Miura	

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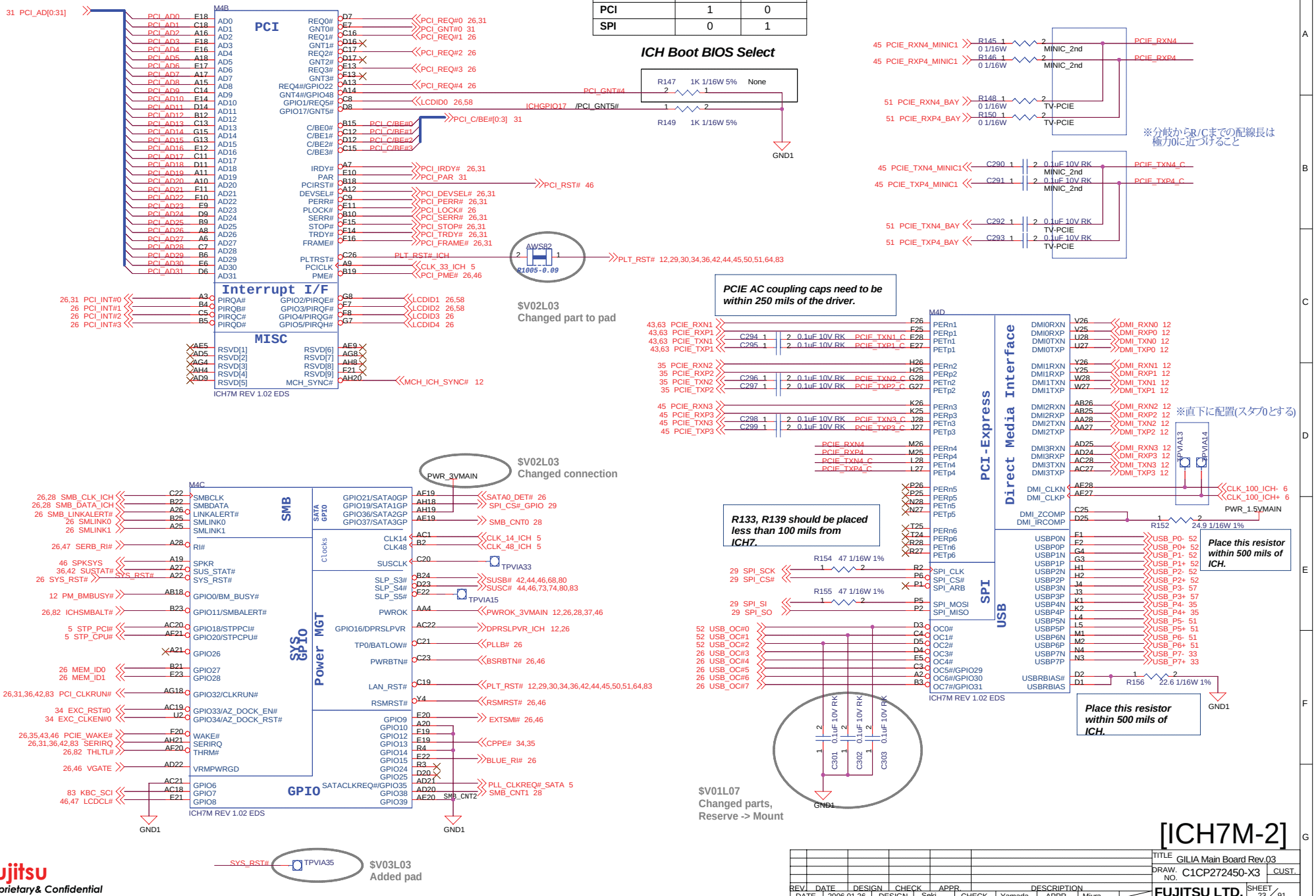
	LCNOPIO17	CHGA1048
LPC (Default)	1	1
PCI	1	0
SPI	0	1

ICH Boot BIOS Select



[ICH7M-2]

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	DATE	2006.01.26	DESIGN	Seki	CHECK Yamada APPR Miura

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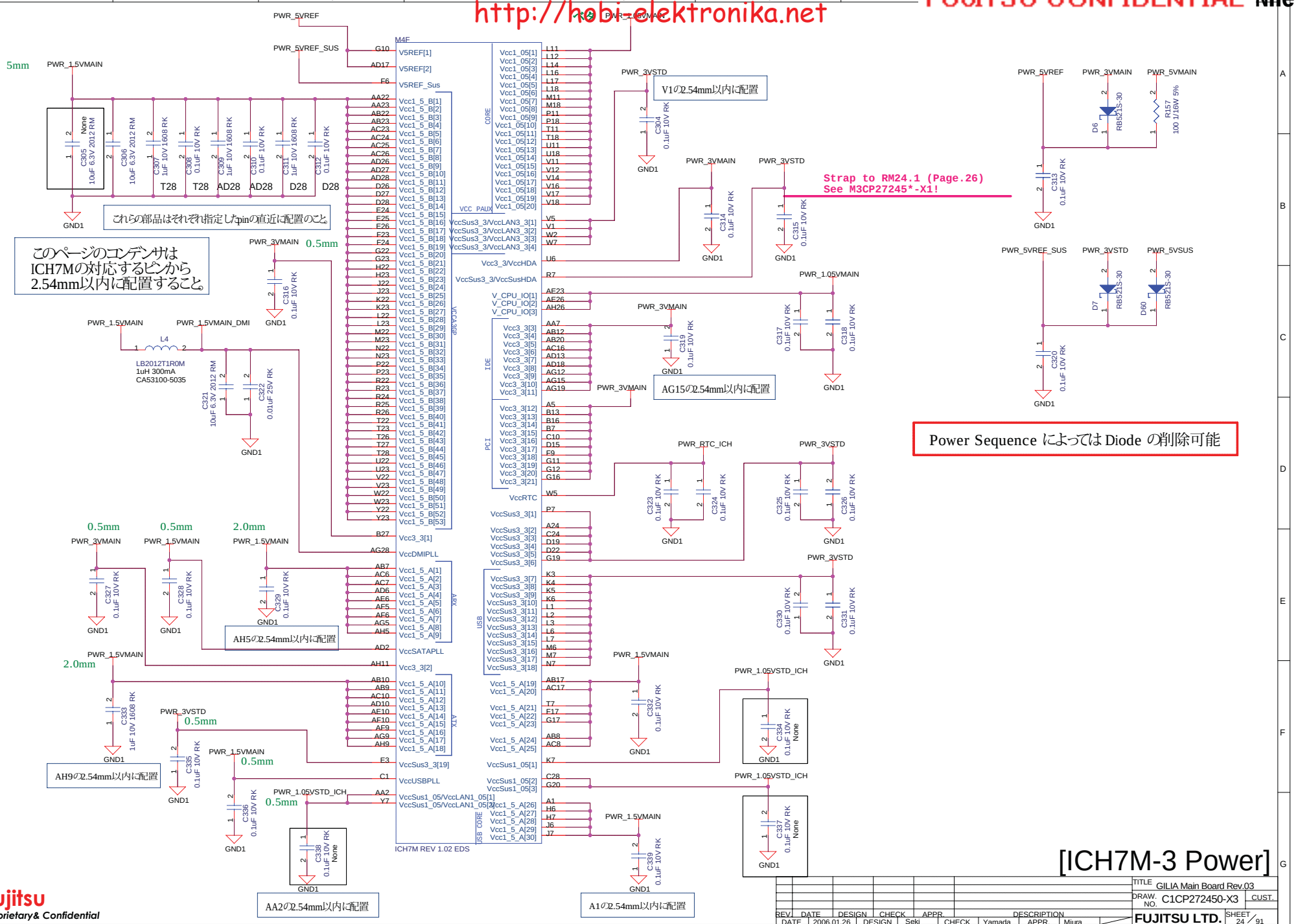

[ICH7M-3 Power]

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	2006.01.26	Seki	Yamada	Miura	

TITLE: GILIA Main Board Rev.03
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CUST.:
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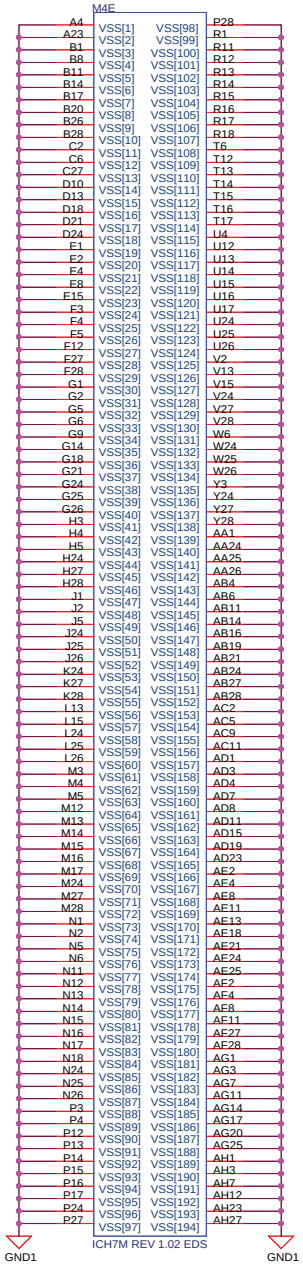
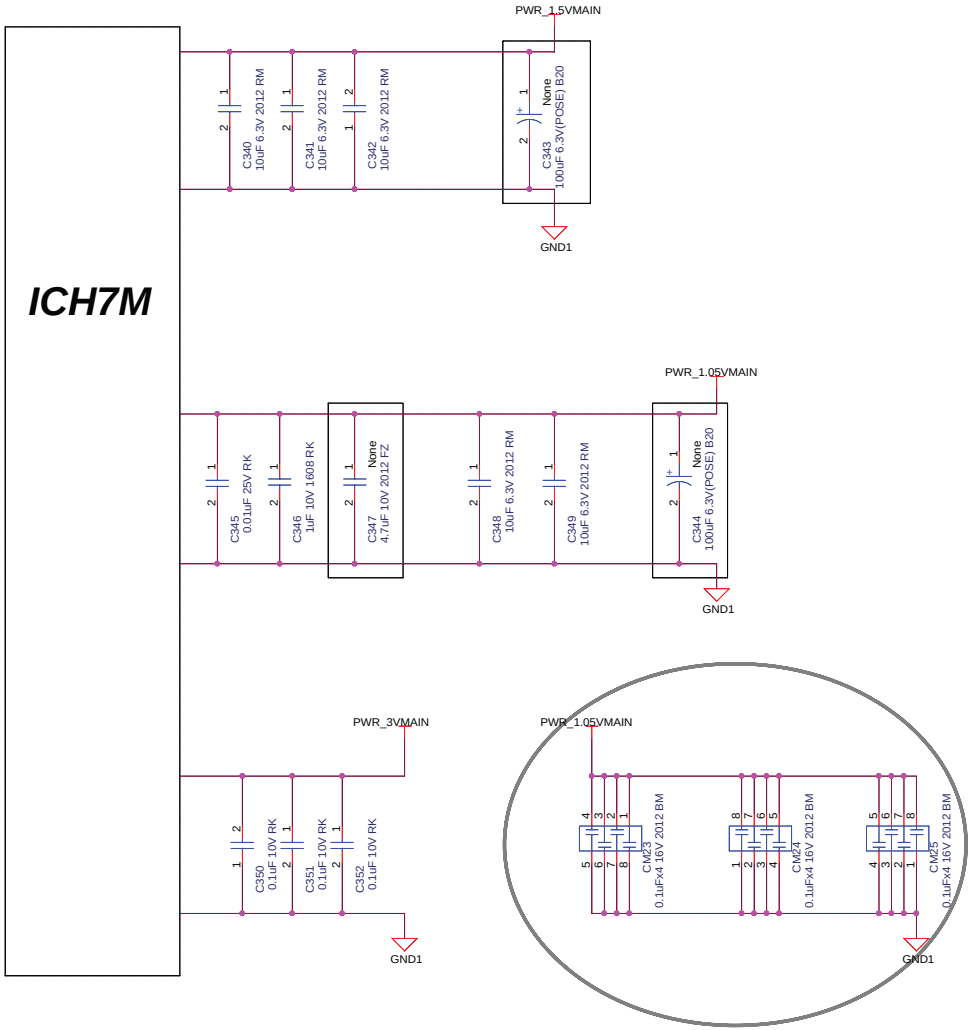
SHEET 24 / 91





$V01L11
Added parts

[ICH7M-4 GND/CAP]

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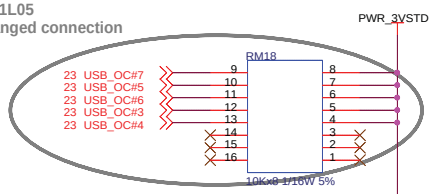
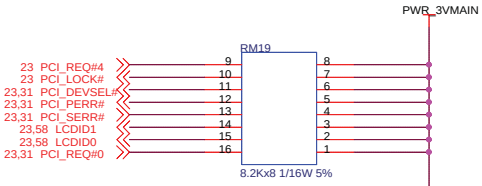
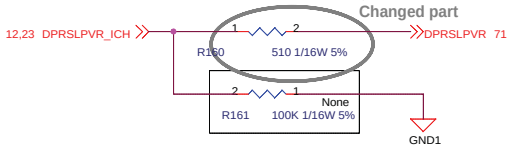
配線を最優先とし、適宜ピンスワップを行うこと。
集合抵抗を個別抵抗へと分解する必要がある場合は設計者に連絡すること。

$V01L05
Changed connection

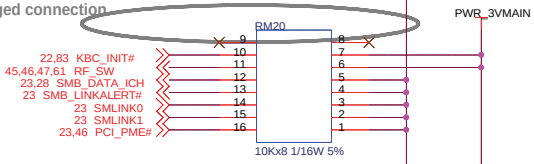


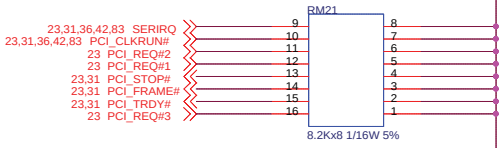


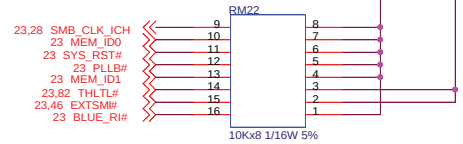
$V01L08
Changed part

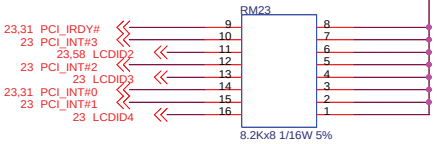


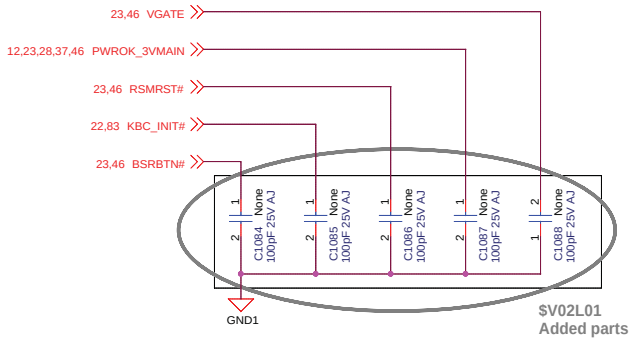
$V01L08
Changed connection







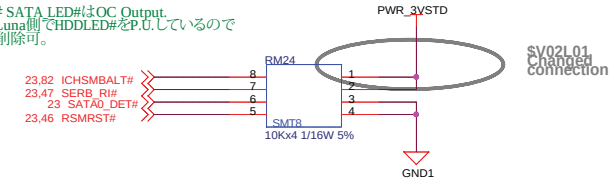




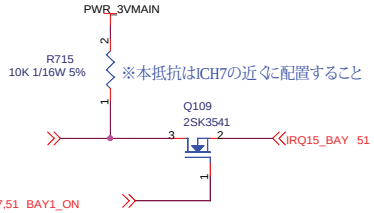
$V02L01
Added parts

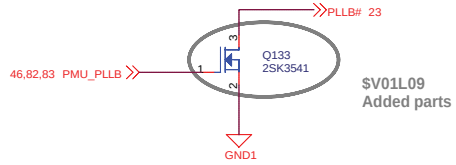
※ICH7の端子直近に配置すること

SATA_LED#はOC Output.
Luna側でHDDLED#をP.U.しているので
削除可。



$V02L01
Changed connection





$V01L09
Added parts

[ICH7M-5 P.U./P.D.]

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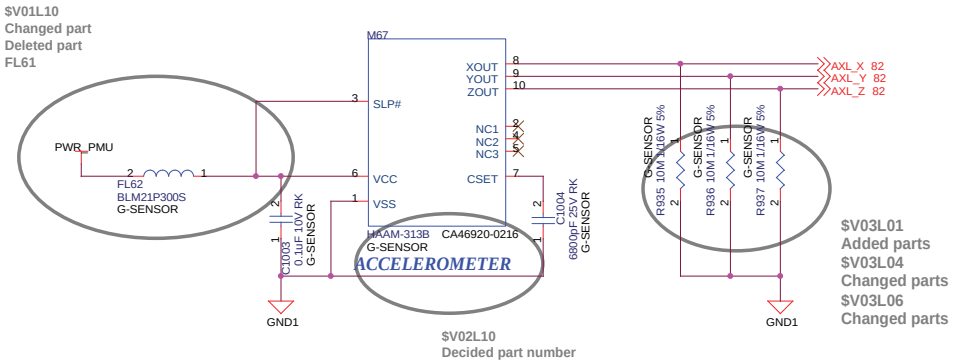
TITLE GILIA Main Board Rev.03
DRAW. NO. C1CP272450-X3 CUST.
FUJITSU LTD. SHEET 26 / 91

$V01L02
Added parts



[G-Sensor]

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	DATE 2006.01.26	DESIGN Seki	CHECK Yamada	APPR Miura	

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DRAW. NO. C1CP272450-X3 CUST.
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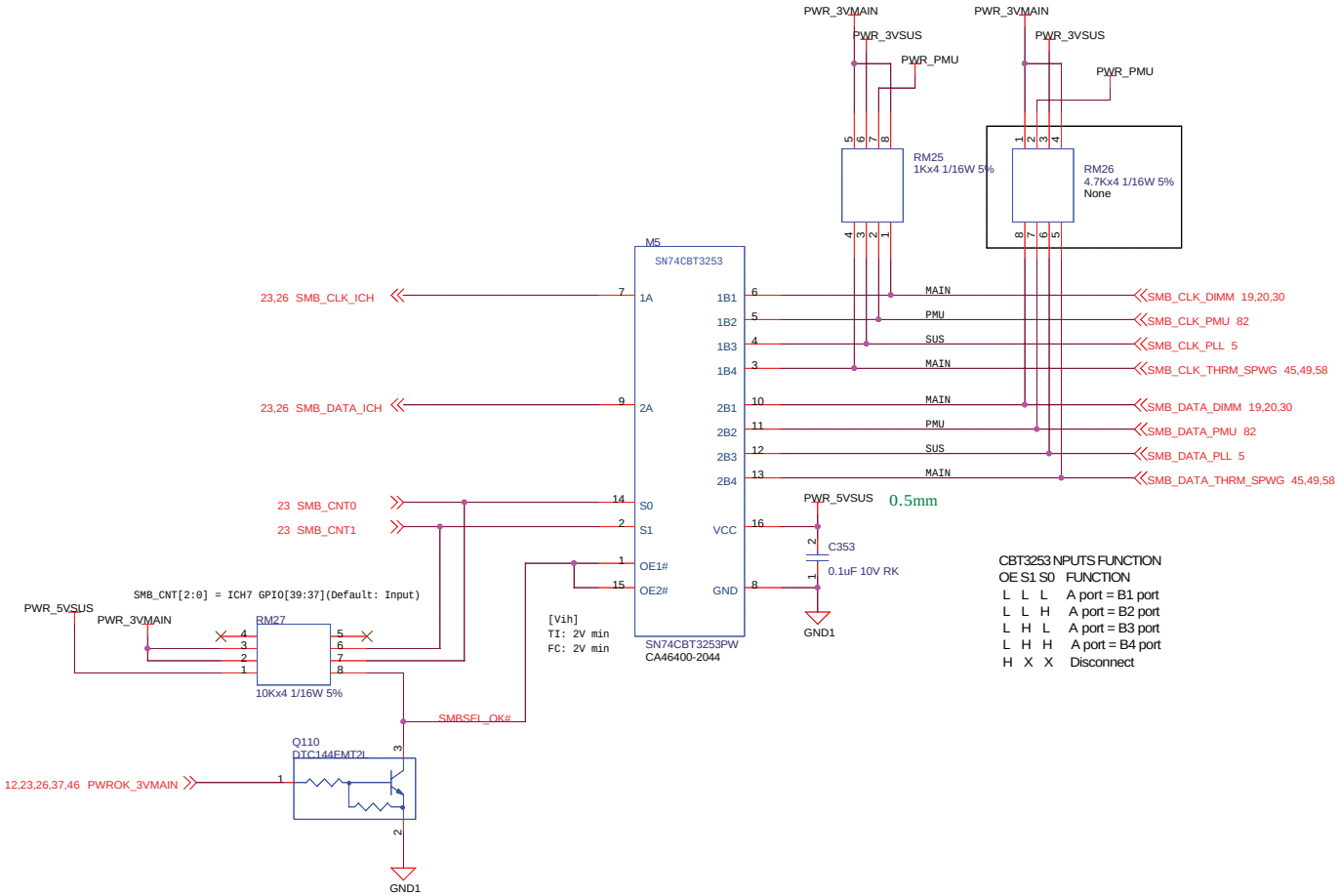

CBT3253 NPUTS FUNCTION

OE	S1	S0	FUNCTION
L	L	L	A port = B1 port
L	L	H	A port = B2 port
L	H	L	A port = B3 port
L	H	H	A port = B4 port
H	X	X	Disconnect

BUS	Device	Address
DIMM	DIMM0	A0h
	DIMM1	A4h
PMU	PMU	32h
PLL	PLL	D2h
THERMAL _LCD	THERMAL	5Ch
	LCD	A0h

Device	Hex	Address
ADT7473	5Ch	0101 110x b
MEM slot0	A0h	1010 000x b
MEM slot1	A4h	1010 010x b
PMU	32h	0011 001x b
LCD(SPWG)	A0h	1010 000x b

[SMBus]

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TITLE GILIA Main Board Rev.03
DRAW. NO. C1CP272450-X3 CUST.
FUJITSU LTD. SHEET 28 / 91

$V01L08
Changed
part

0.5mm
PWR_3VMAIN

M6
VDD
WP#
HOLD#
SI
SO
CE#
SCK
VSS

R163 4.7K 1/16W 5%
R164 4.7K 1/16W 5%
R162 47 1/16W 1%

SPI_SI 23
SPI_SO 23
SPI_CE#0
SPI_SCK 23
17.86M

M25P80-VMP6G
CA46206-2331
GND1

0.5mm
PWR_3VMAIN

M7
SPI_WP#1
SPI_HOLD#1
SPI_CE#1
R166 47 1/16W 1%
SPIx2

$V03L05
Changed part

M25P80-VMP6G
CA46206-2333 SPIx2
GND1

Layout Note:
R135, R136 should be placed less than 100 mils from the serial flash device.

SPI_CS#_GPIO	Description
High	1st SPI is available.
Low	2nd SPI is available.

PWR_3VMAIN

RM28
10Kx4 1/16W 5%
SPIx2

SPI_WP#1
SPI_HOLD#1
SPI_CS#_GPIO#
23 SPI_CS#_GPIO
SPI_CS#_GPIO

Q3
2SK3541
SPIx2

R165
1K 1/16W 5%
SPIx2

TP3
TP4

GND1

評価用(TPショート時2nd ROMアクセス固定)

SPI_CS#_GPIO
23 SPI_CS#

Q4A
EM6K1T2R
SPIx2

SPI_CE#0

R167 0 1/16W
No SPIx2

SPI_CS#_GPIO#

Q4B
EM6K1T2R
SPIx2

SPI_CE#1

$V02L01
Added parts

0.5mm
PWR_3VMAIN

0.5mm
PWR_5VMAIN

22,36,42,46,83 LPC_AD0
22,36,42,46,83 LPC_AD1
22,36,42,46,83 LPC_AD2
22,36,42,46,83 LPC_AD3
22,36,42,46,83 LPC_FRAME#
5,46 CLK_33_ASIC
12,23,30,34,36,42,44,45,50,51,64,83 PLT_RST#

R824 10 1/16W 5% None
R825 10 1/16W 5% None
R826 10 1/16W 5% None
R827 10 1/16W 5% None
R828 10 1/16W 5% None
R829 10 1/16W 5% None
R830 10 1/16W 5% None

LPC_AD0_DBG
LPC_AD1_DBG
LPC_AD2_DBG
LPC_AD3_DBG
LPC_FRAME#_DBG
CLK_33_ASIC_DBG
PLT_RST#_DBG

CN4
PORT80
None

GND1

※R824～R829は、M33(BENN)の端子直近に配置すること。
R830は、M16(TPM)の端子直近に配置すること。

PWR_3VMAIN

RM29
SMT8
10Kx4 1/16W 5%

23 SPI_SI
23 SPI_SO
SPI_CE#1
SPI_CE#0

Layout Note:
RM28 should be placed close to ICH7M.

[BIOS]

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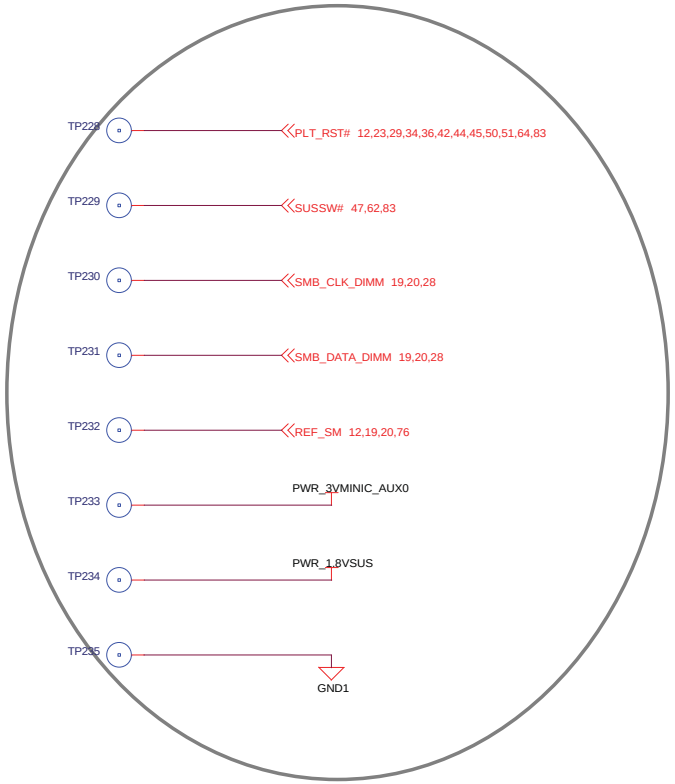
※個別に位置指定します。



$V02L03
Added pads

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	DATE 2006.01.26	DESIGN Seki	CHECK Yamada	APPR Miura	

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※JAA16はCardBus時クロック信号になるので、GND1にてガードを行うこと。

$V02L03
Changed part to pad

$V01L10
Added parts
Changed connection

※上記のコンデンサはPCICの電源ピン近くに配置すること。

※上記の抵抗/コンデンサはPCICの近くに配置すること。

※上記のコンデンサはPCICの電源ピン近くに配置すること。

[PCIC-1]

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION		
	DATE	2006.01.26	DESIGN	Seki	CHECK	Yamada	APPR.	Miura

TITLE: GILIA Main Board Rev.03
DRAW. NO.: C1CP272450-X3
CUST.
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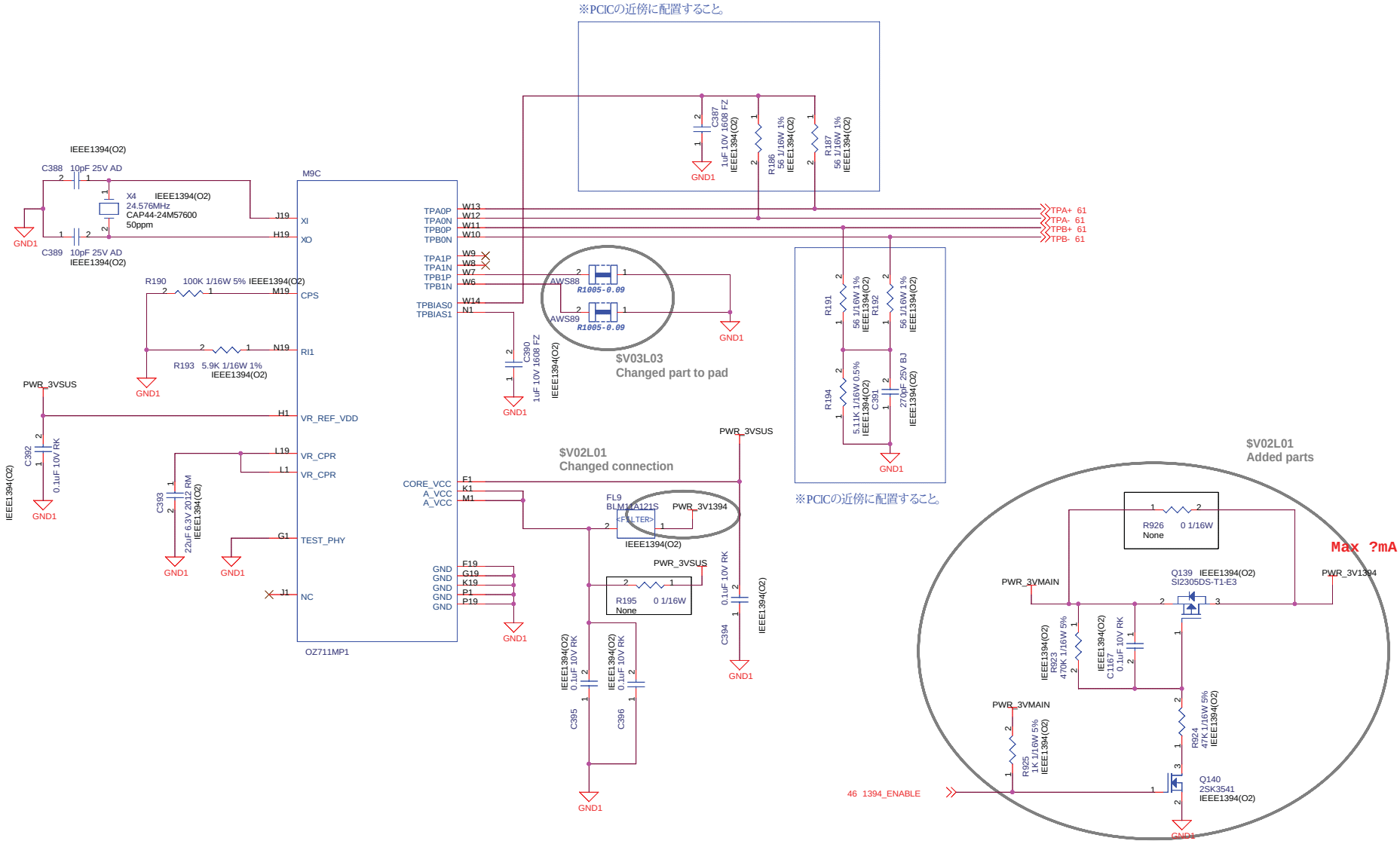

[PCIC-2]

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	DATE 2006.01.26	DESIGN Seki	CHECK Yamada	APPR. Miura	

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DRAW. NO. C1CP272450-X3 CUST.
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[SD/MS/xD Slot]

$V01L05
Changed connection CN5

$V01L10
Changed connection

$V01L10
Added part

$V01L08
Changed connection

$V01L10
Changed connection

$V01L09
Added pads

$V02L05
Added pad

$V01L05
Deleted part M11,M12,Q6,R202,R203,C400.C402

$V01L06
Changed part

$V01L05
Deleted part C398

＃SCR時Pull-up不要

※分岐/TPのスタブは最小とすること。

※RM33,RM34はピンスワップ可能

＃SYSID1はSmartCardSlotの有無判別用bitとする。
SDMS_EXIST#がLowの場合、SD,MS,xDをEnableするが、
SDMS_EXIST#とSYSID1が両方Lowの場合は、
BIOSはPCICのxDのFunctionをDisableし、SRCのFunctionをEnableする。

※上記の<1A-B>～<4A-B>の組み合わせはスワップ可能

USB/SD/MS Board CN
SD/FeliCa

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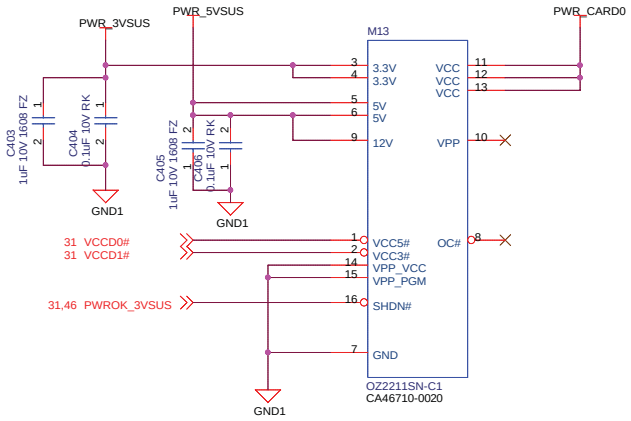

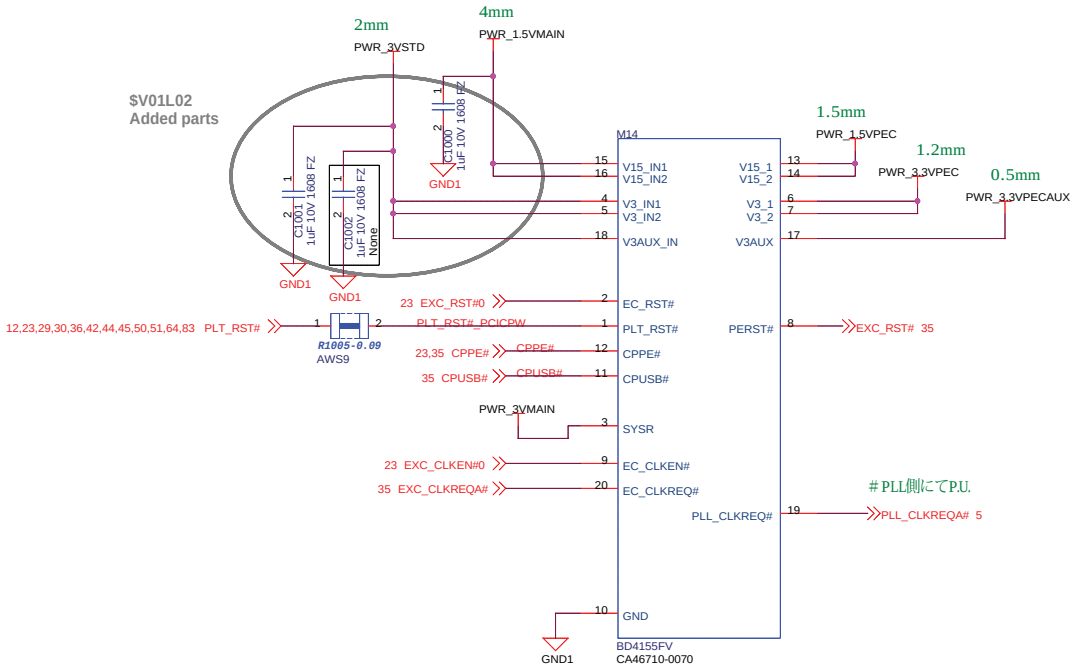

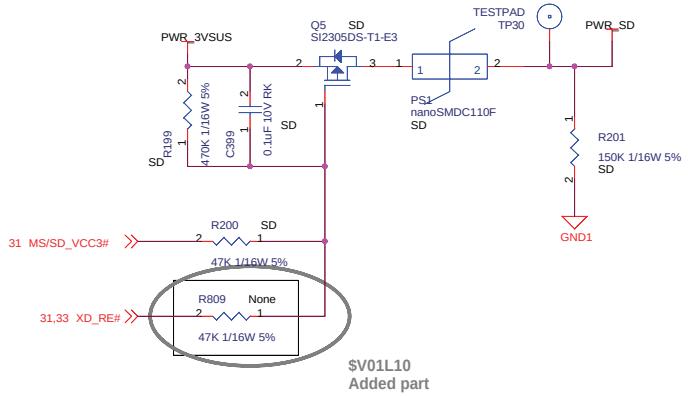

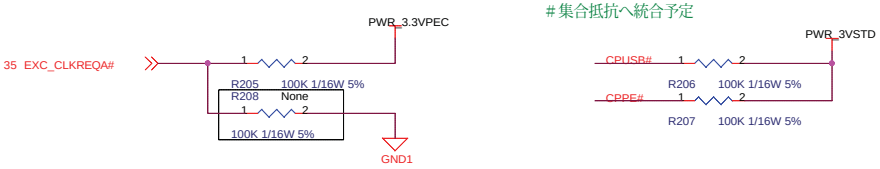

[PCMCIA Power]

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	DATE 2006.01.26	DESIGN Seki	CHECK Yamada	APPR. Miura	

TITLE GILIA Main Board Rev.03
DRAW. NO. C1CP272450-X3 CUST.
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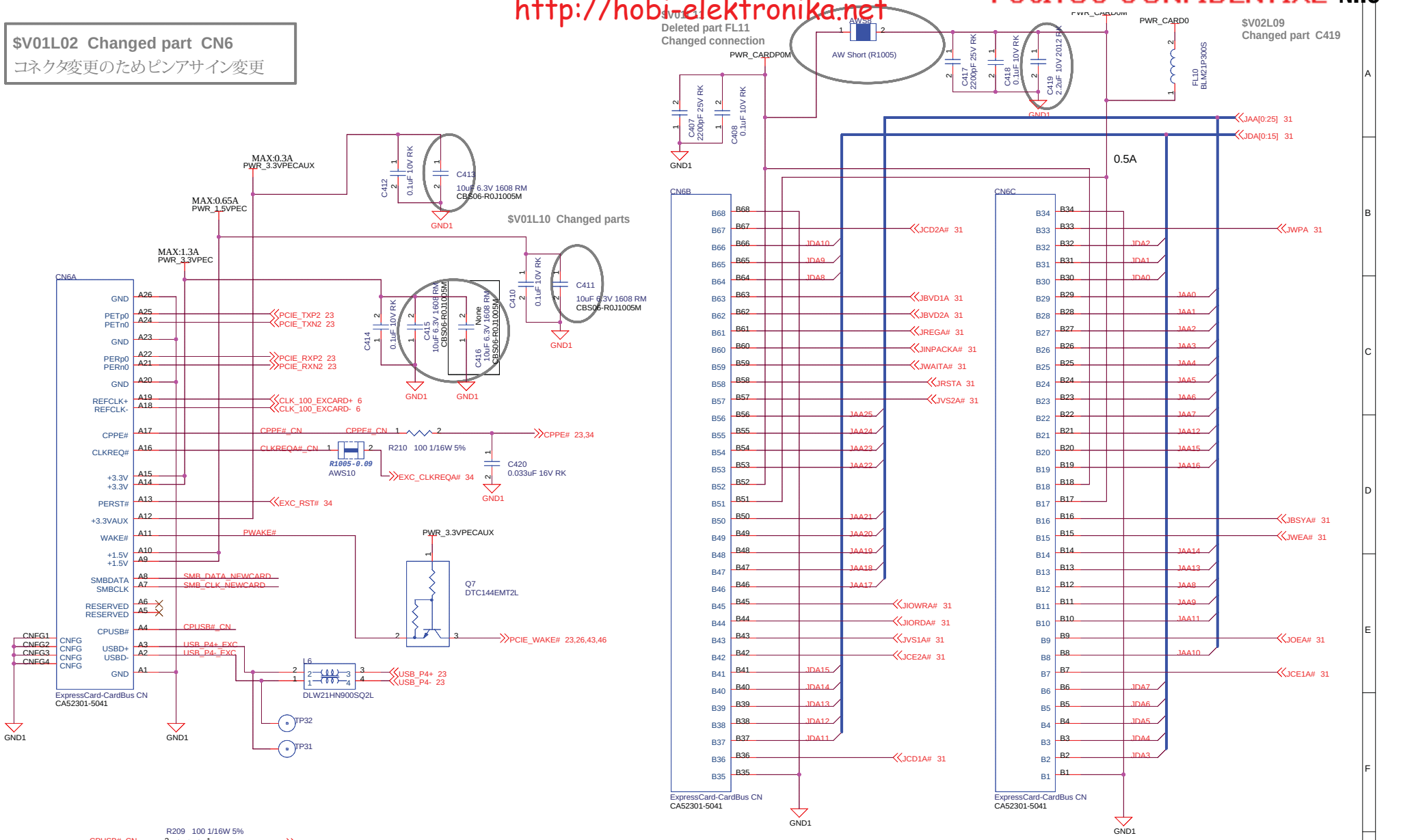
$V01L02 Changed part CN6
コネクタ変更のためピンアサイン変更

$V01L11
Deleted part FL11
Changed connection

$V02L09
Changed part C419

$V01L10 Changed parts



※JCE1x#, JCE2x#, JOEx#, JWEx#は、
データバスとの平行配線とならないように配線すること。

※FGはGND1に接続すること。

SLOT#2:ExpressCard
SLOT#1:CardBus

[PCMCIA-Connector]

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	DATE	2006.01.26	DESIGN	Seki	CHECK	Yamada	APPR.	Miura

TITLE: GILIA Main Board Rev.03
DRAW. NO.: C1CP272450-X3
CUST.:
FUJITSU LTD.
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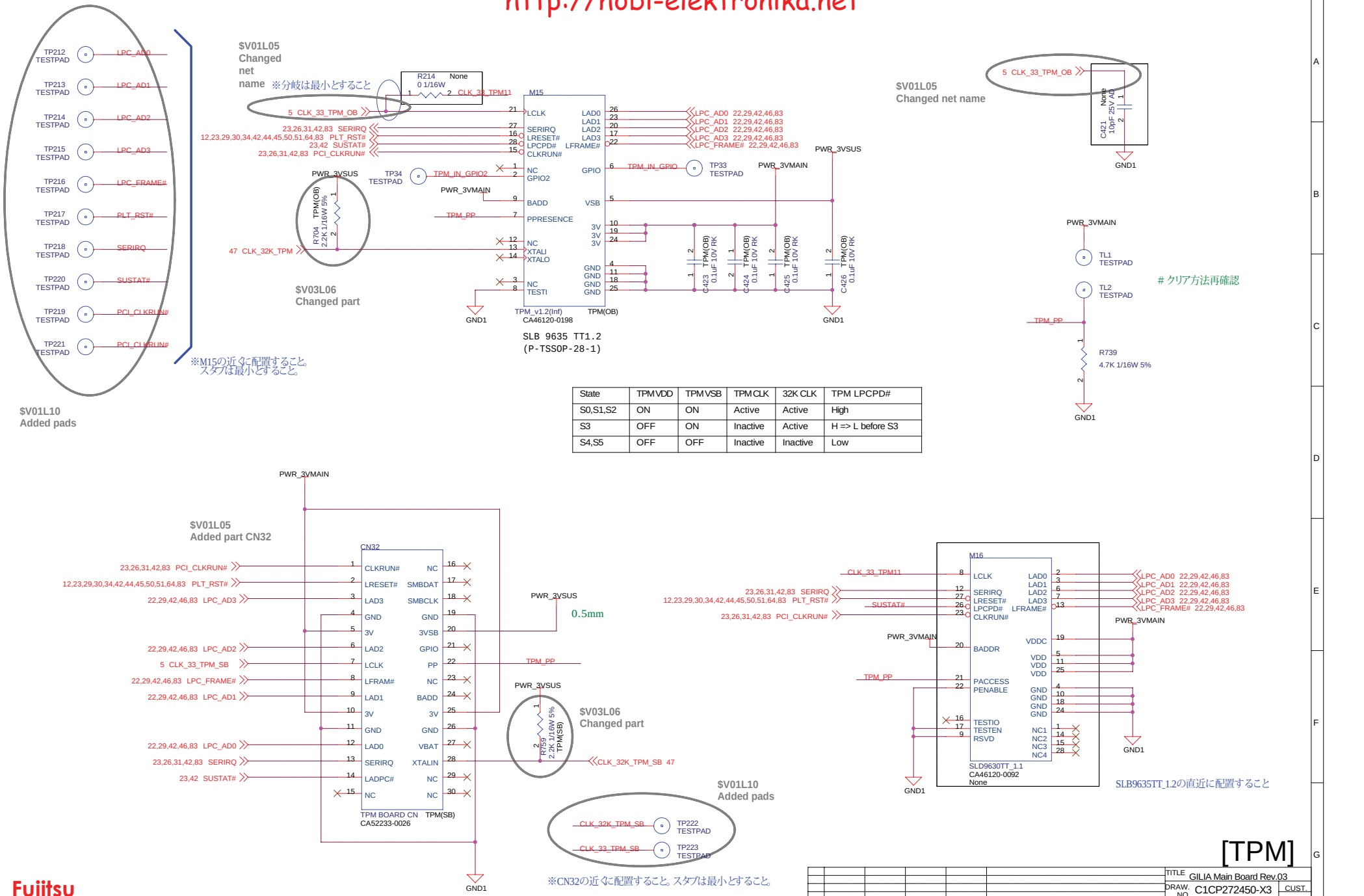

State	TPM VDD	TPM VSB	TPM CLK	32K CLK	TPM LPCPD#
S0,S1,S2	ON	ON	Active	Active	High
S3	OFF	ON	Inactive	Active	H => L before S3
S4,S5	OFF	OFF	Inactive	Inactive	Low

[TPM]

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TITLE GILIA Main Board Rev.03
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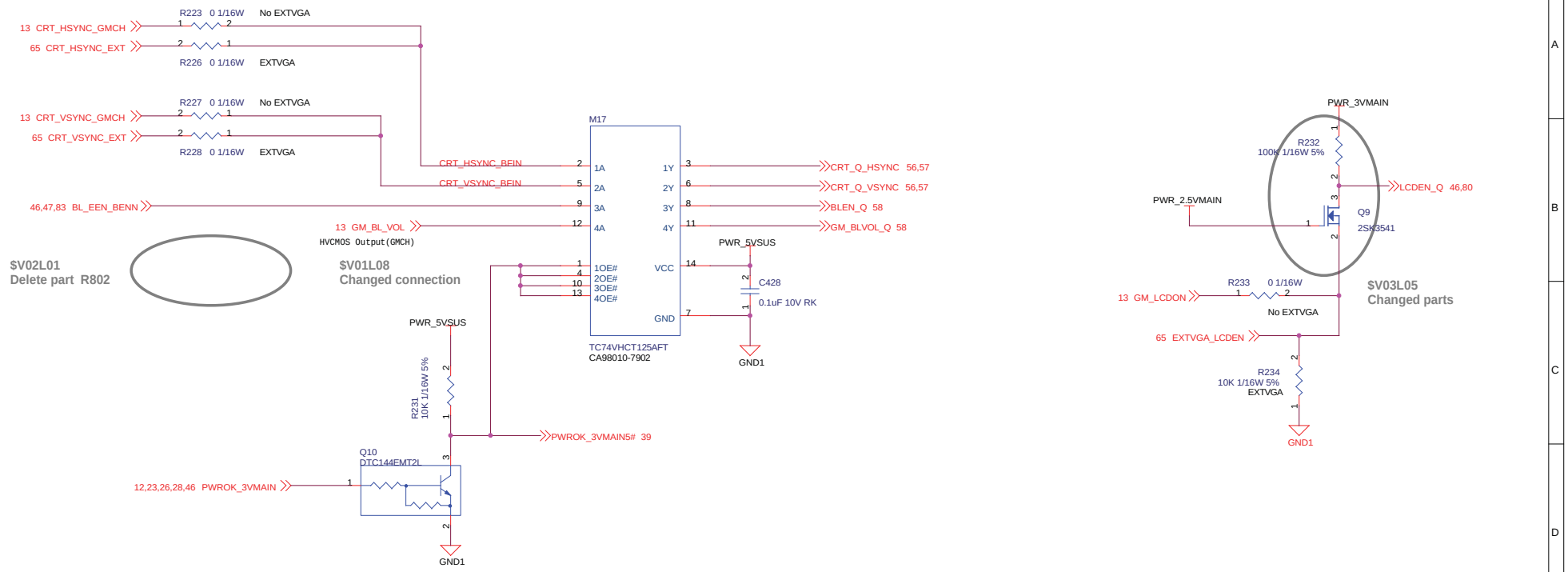

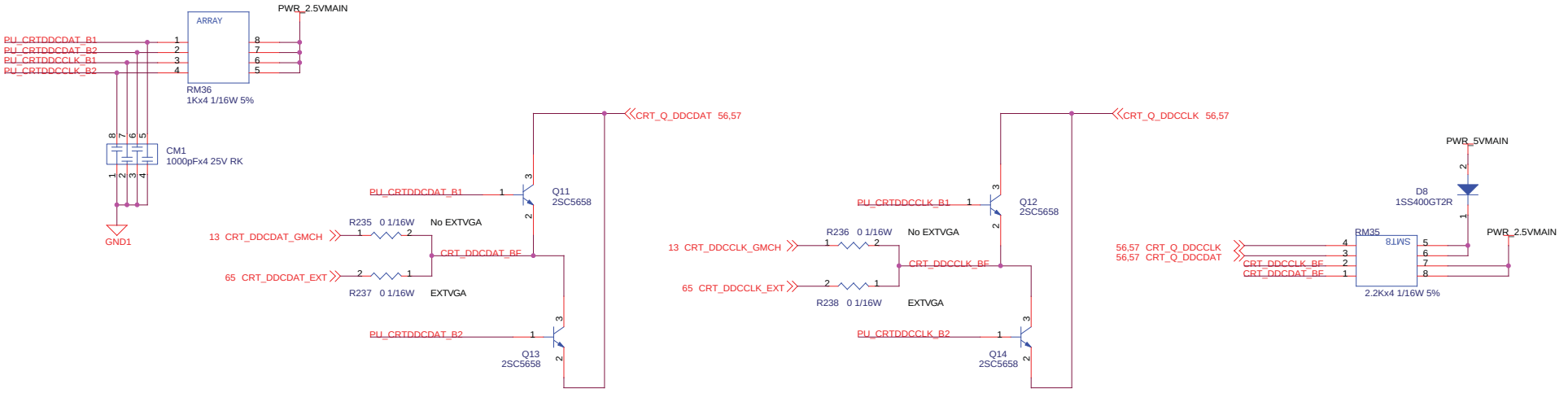

#CRT Portに保護ダイオードを実装しないため、
FETを使用するとESD破壊の危険がある。
そのため、従来どおりNPN-Trを使用する。

[Buffer/LV Shift]

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TITLE: GILIA Main Board Rev.03
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※回路図中の *印はAnalogLineのため、0.25mm以上の幅で配線し、可能な限りGNDAUDでガード(上下層を含む)すること。

[Audio CODEC]

5.0V 200mA

3.3V 200mA

$V02L11 Changed part

$V02L04 Added parts

$V02L01 Added parts C1071,C1072,C1073

$V01L3 Changed part

$V02L10 Added parts Changed connection

$V02L10 Added parts

P.R Out

Main Out

SP Out

Int. Mic

Main In

P.R In

for PR Audio Out

for Mainboard Audio Out

#ALコンNG(高さ条件)

for Internal Speaker TV Tuner

#未使用モデルは入力固定不要?

※C439,C440,C1071はM22の近くに配置すること

※C1170, C1171はM18の直近に配置すること。

※Codec近くにて接続すること

※0.5mm幅にて配線

M18 ALC262 CA46120-1164

M74 NJM2741F3 CA46500-0210

FL12 BLM18PG181SN1

$V02L01
Deleted parts M19 and others

$V01L15
Changed parts

$V02L08
Reserve -> Mount

$V01L15
Changed parts

$V02L11
Changed parts

$V02L08
Changed part

$V02L03
Changed connection
$V02L04
Changed connection

$V02L03
Addded pad

$V03L01
Deleted parts D9,D11
Added parts D78,D79,D80

$V02L03
Changed connection
$V02L04
Changed connection

＃部品種削減のため高精度品使用

＃評価用

[Audio AMP]

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	2006.01.26	Seki	Yamada	Miura	

TITLE GILIA Main Board Rev.03
DRAW. NO. C1CP272450-X3
CUST.
FUJITSU LTD.
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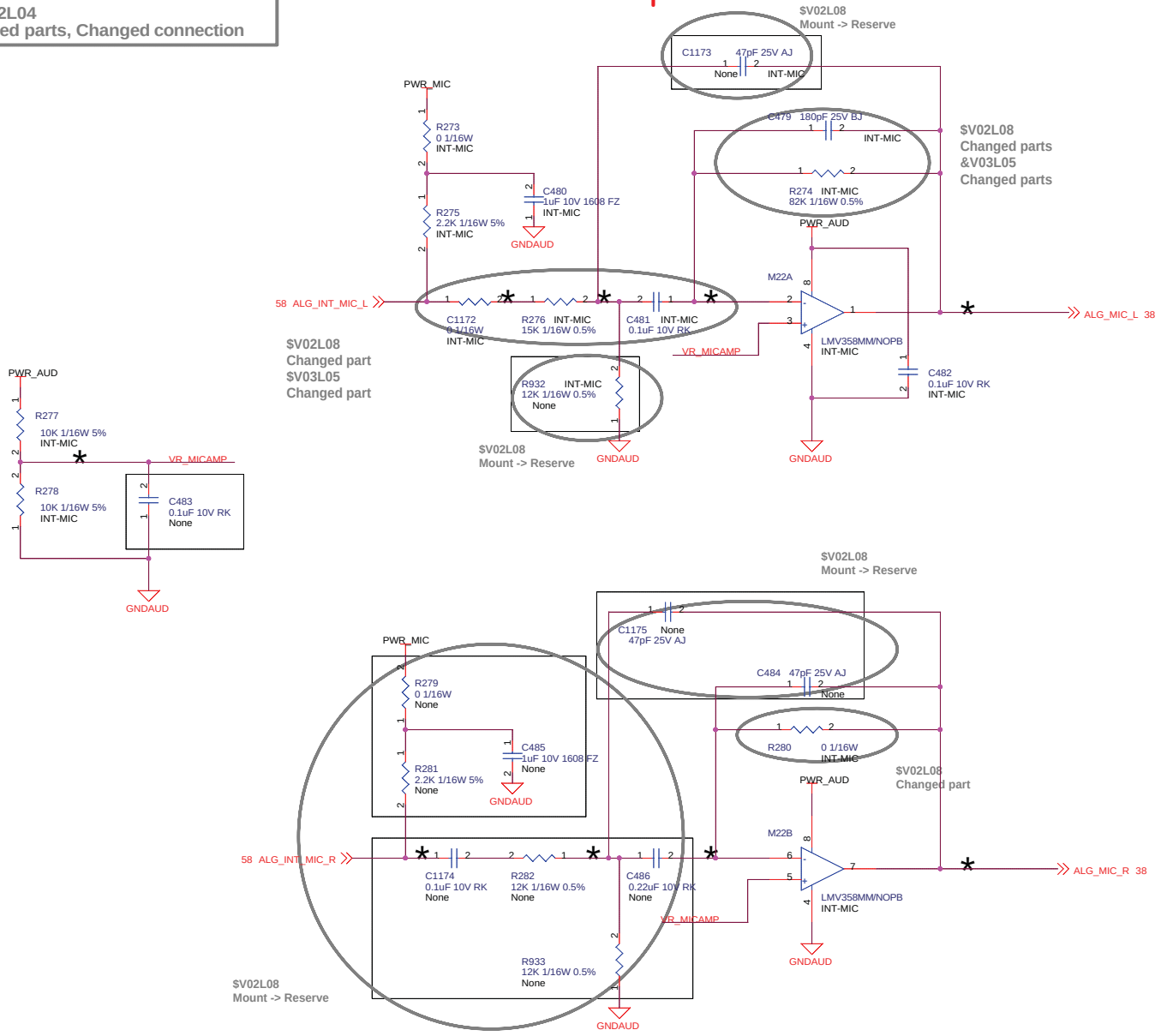
$V02L04
Added parts, Changed connection



[Audio Int-Mic]

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	DATE	2006.01.26	DESIGN	Seki	CHECK Yamada APPR Miura

TITLE GILIA Main Board Rev.03
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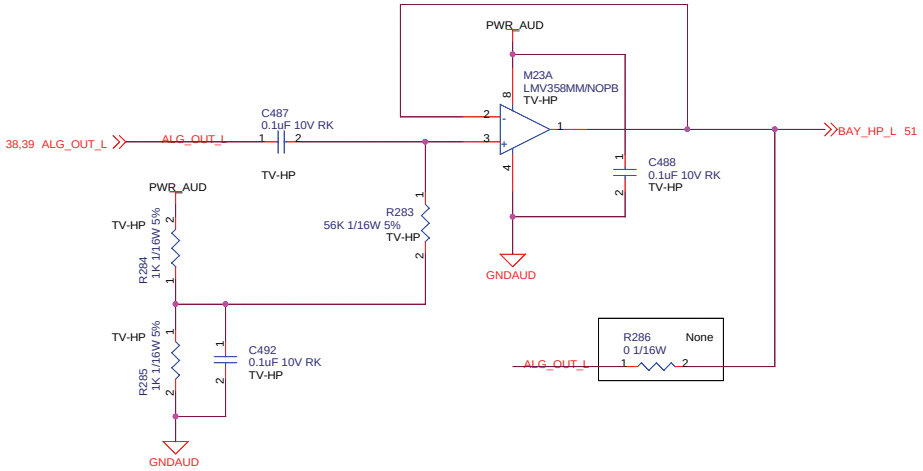
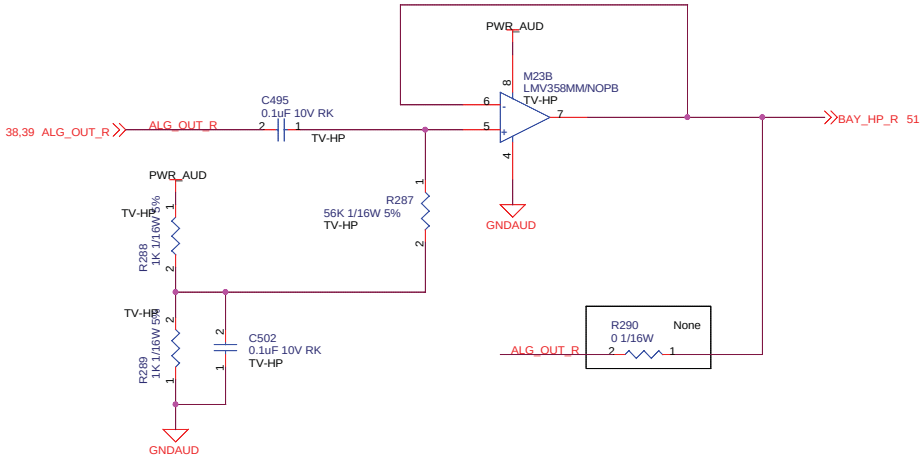
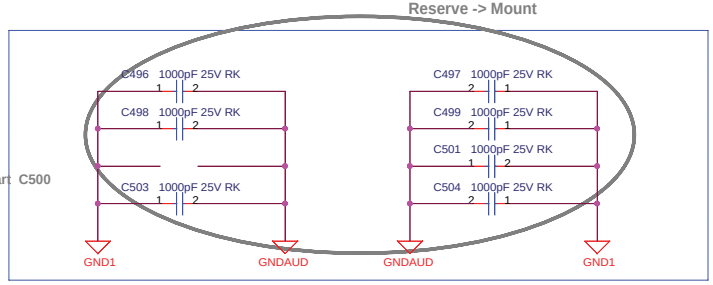
FUJITSU LTD. SHEET 40 / 91





$V03L04
Reserve -> Mount

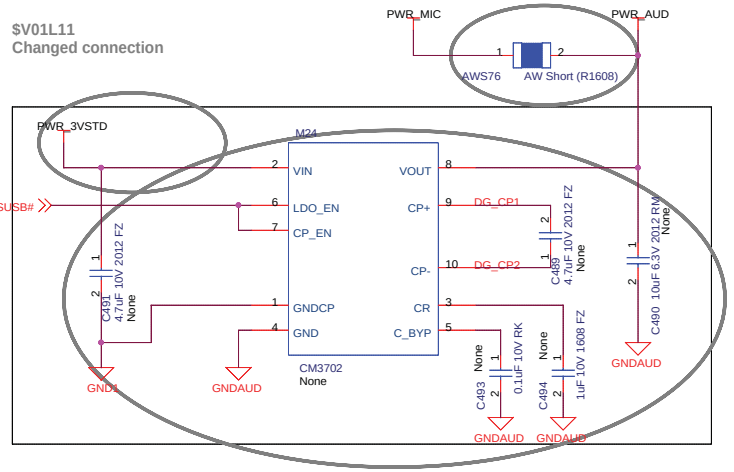


$V01L10
Deleted part C500

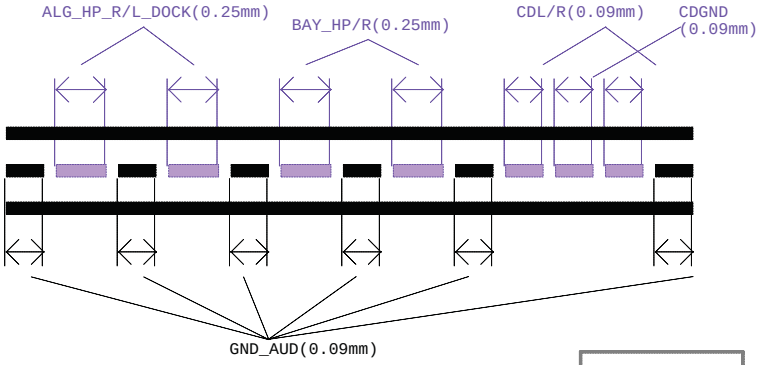
※上記のコンデンサは、GND1とGNDAUDの分割をまたぐように配置すること。

$V01L06
Added Pad

$V01L11
Changed connection



$V01L06
Mount -> Reserve



$V02L08
Changed drawing.

[Audio etc]

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REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE 2006.01.26	DESIGN Seki	CHECK Yamada	APPR Miura	

TITLE GILIA Main Board Rev.03
DRAW. NO. C1CP272450-X3
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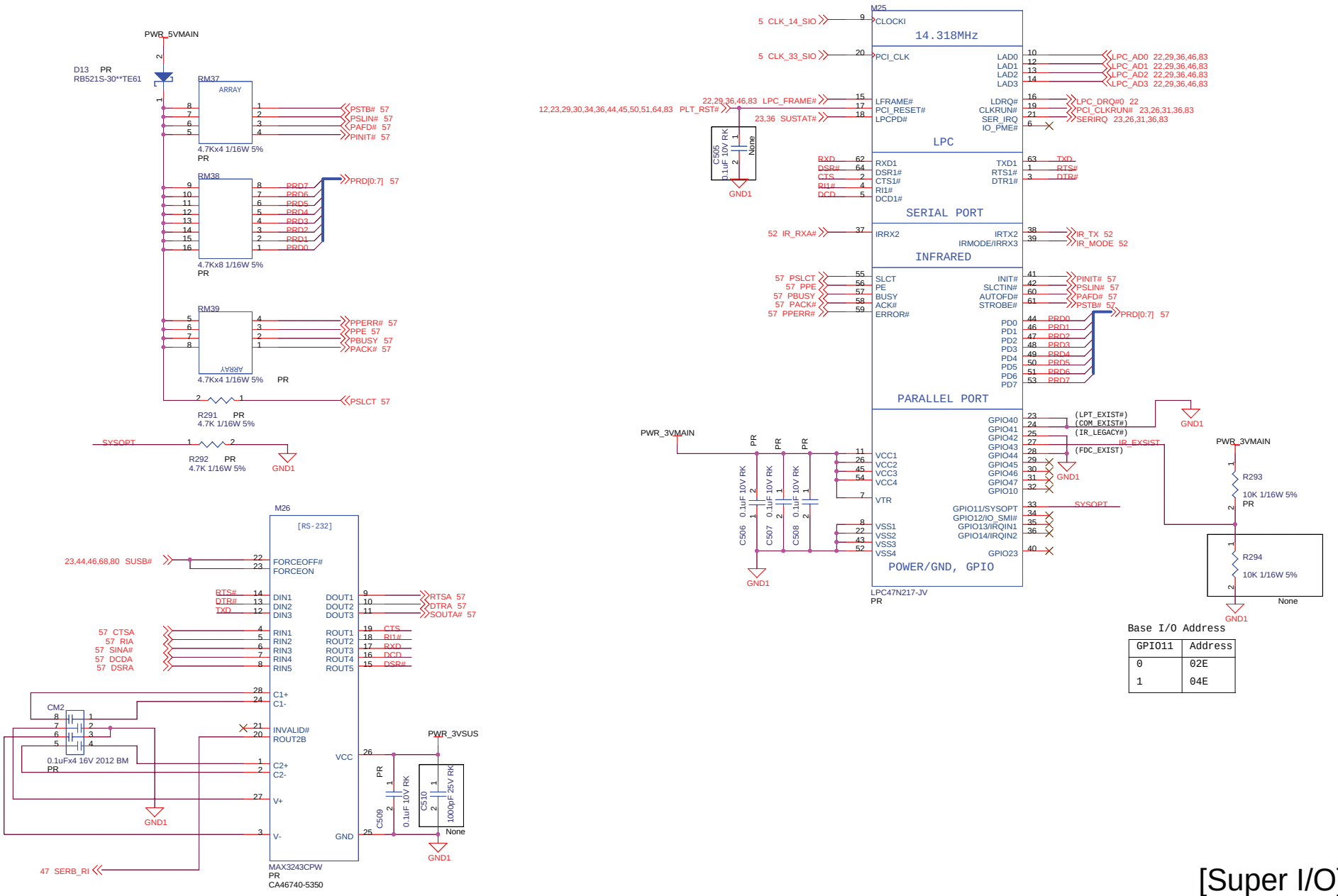

Base I/O Address

GPIO11	Address
0	02E
1	04E

[Super I/O]

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TITLE GILIA Main Board Rev.03
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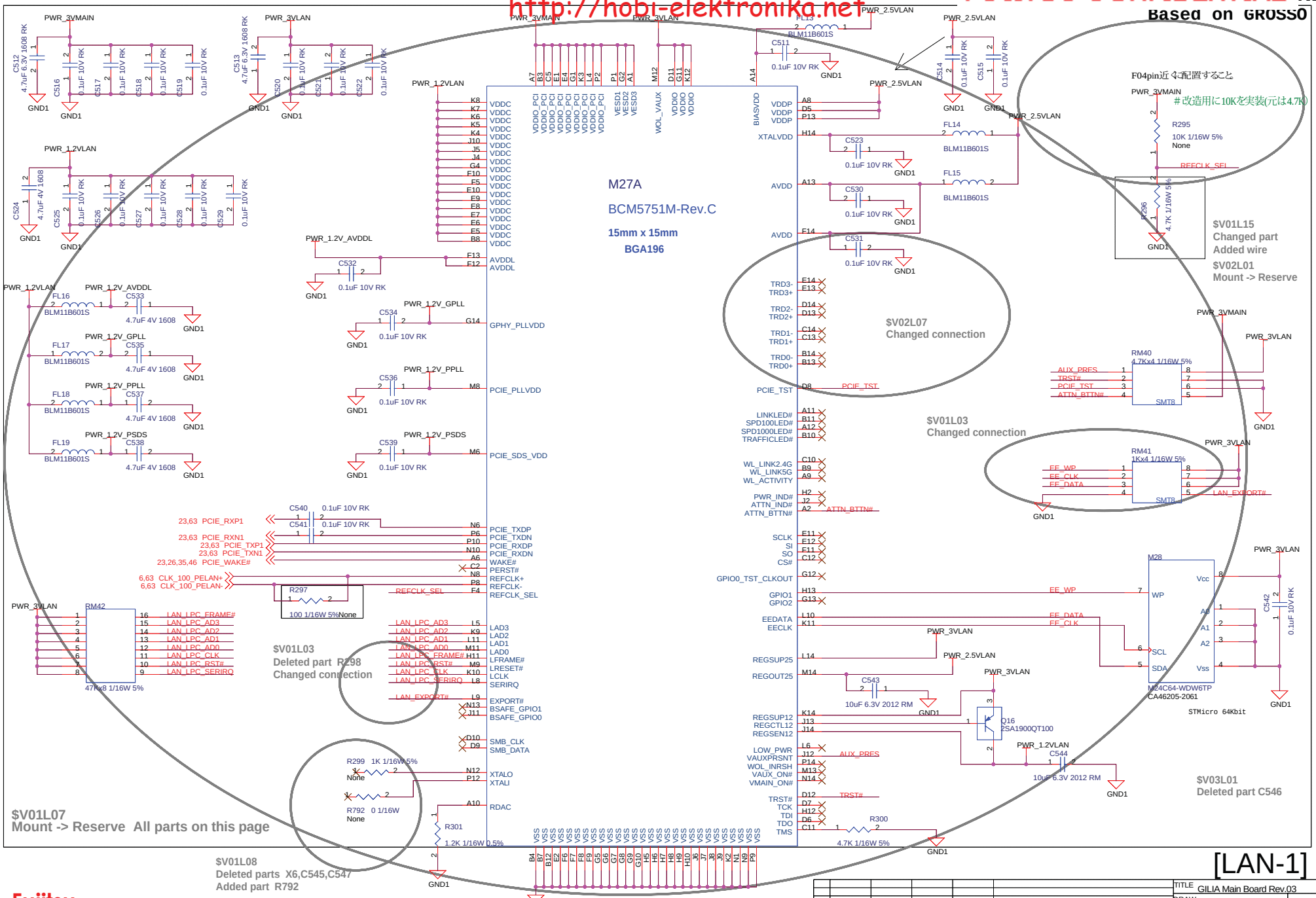
FUJITSU LTD. SHEET 42 / 91



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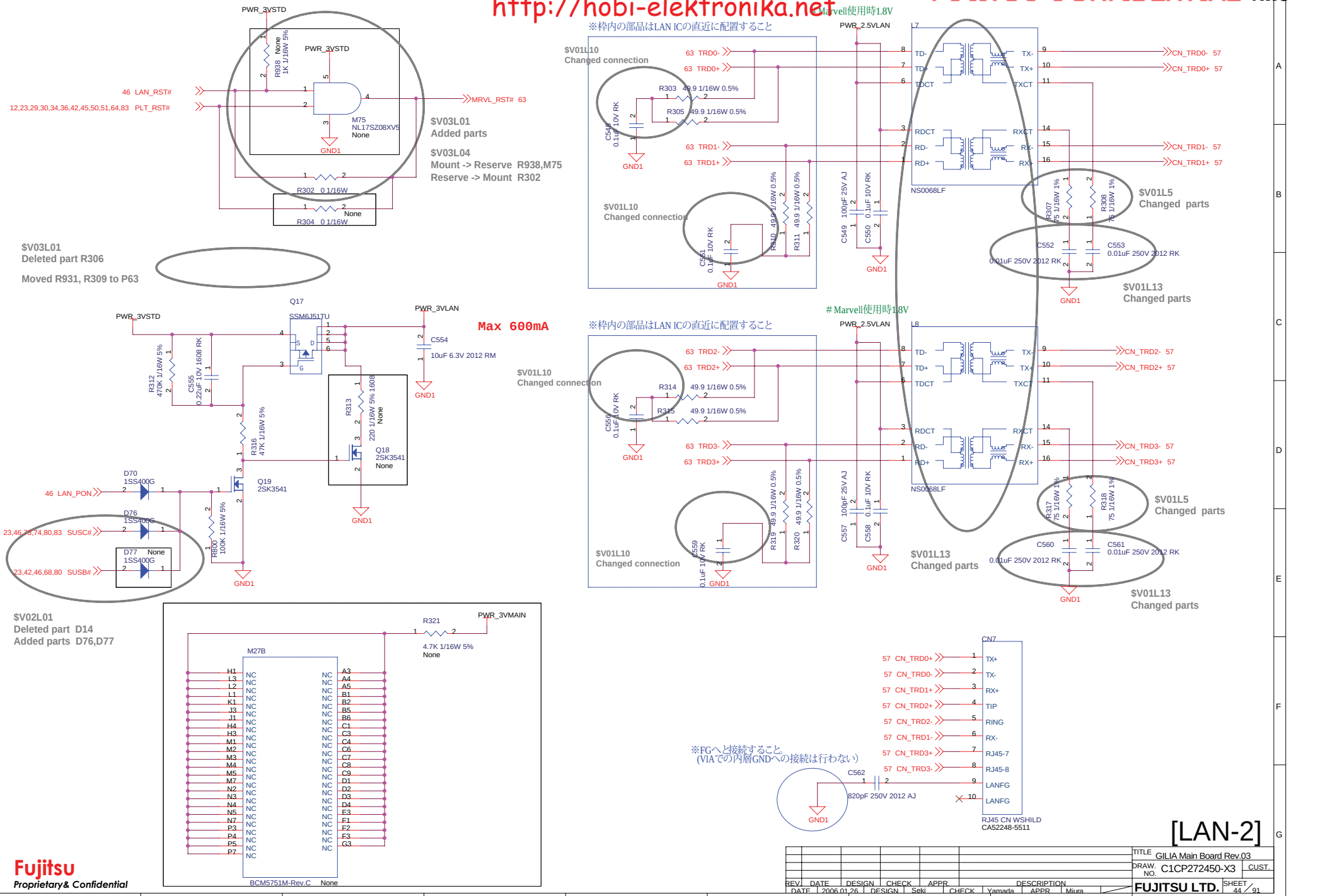
[LAN-1]

TITLE	GILIA Main Board Rev.03		
DRAW. NO.	C1CP272450-X3	CUST.	
FUJITSU LTD.		SHEET	43 / 91

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
DATE	2006.01.26	DESIGN	Seki	CHECK	Yamada
APPR.	Miura				



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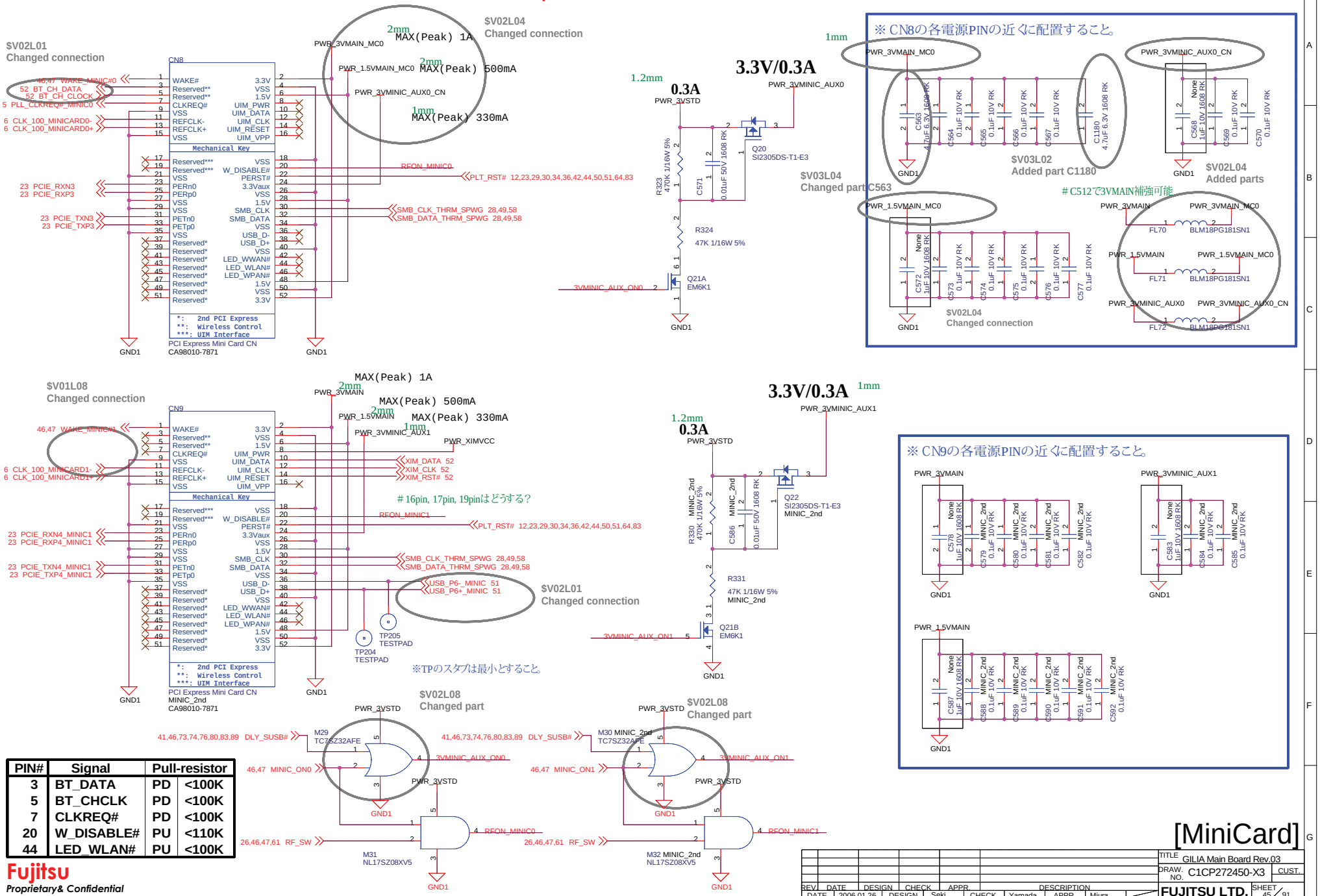
[LAN-2]

REV.	DATE	DESIGN	CHECK	APPR.	DESCRIPTION		
	DATE	2006.01.26	DESIGN	Seki	CHECK	Yamada	APPR. Miura

TITLE GILIA Main Board Rev.03
DRAW. NO. C1CP272450-X3 CUST.
FUJITSU LTD. SHEET 44 / 91



PIN#	Signal	Pull-resistor	
3	BT_DATA	PD	<100K
5	BT_CHCLK	PD	<100K
7	CLKREQ#	PD	<100K
20	W_DISABLE#	PU	<110K
44	LED_WLAN#	PU	<100K

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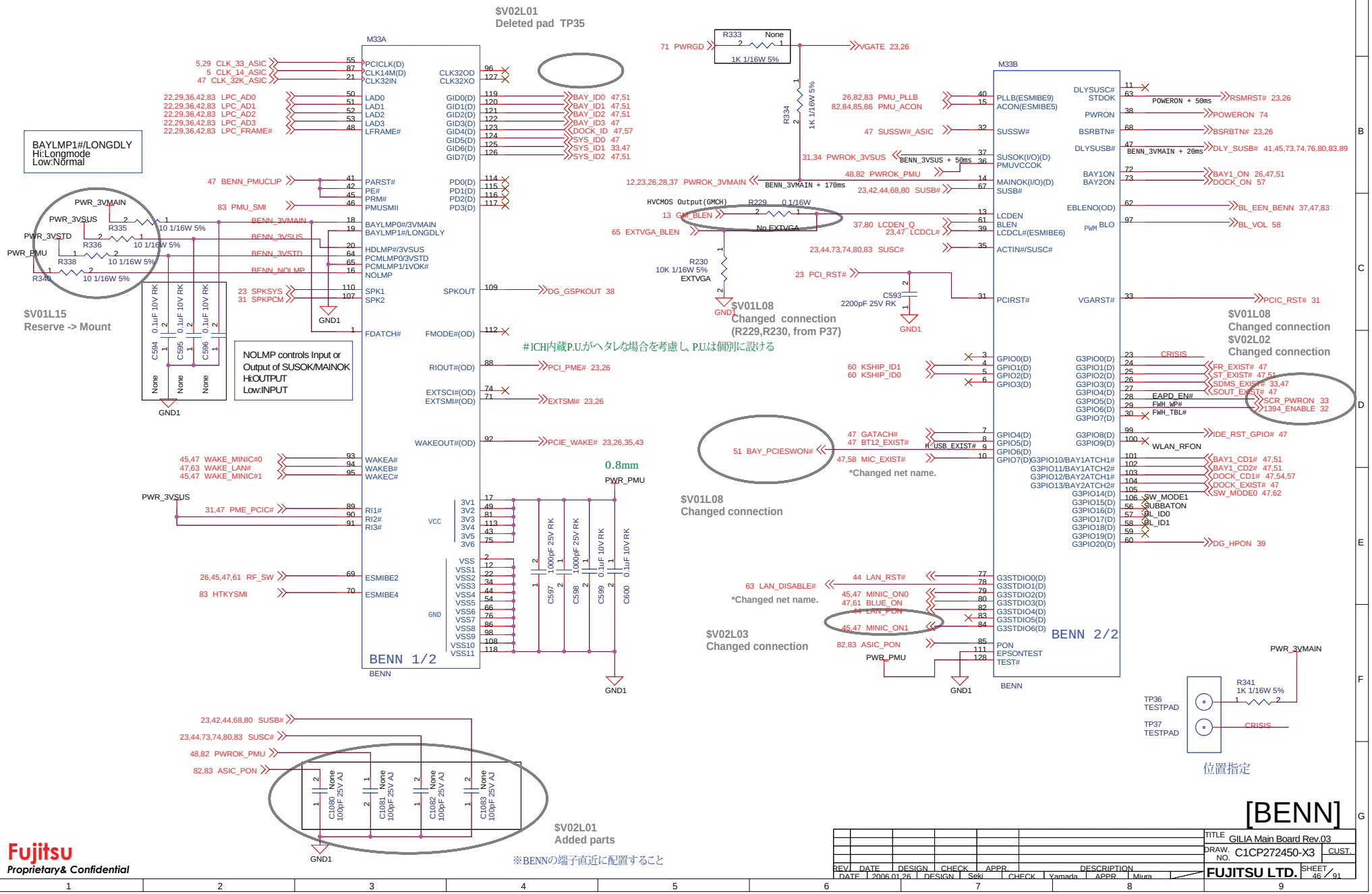
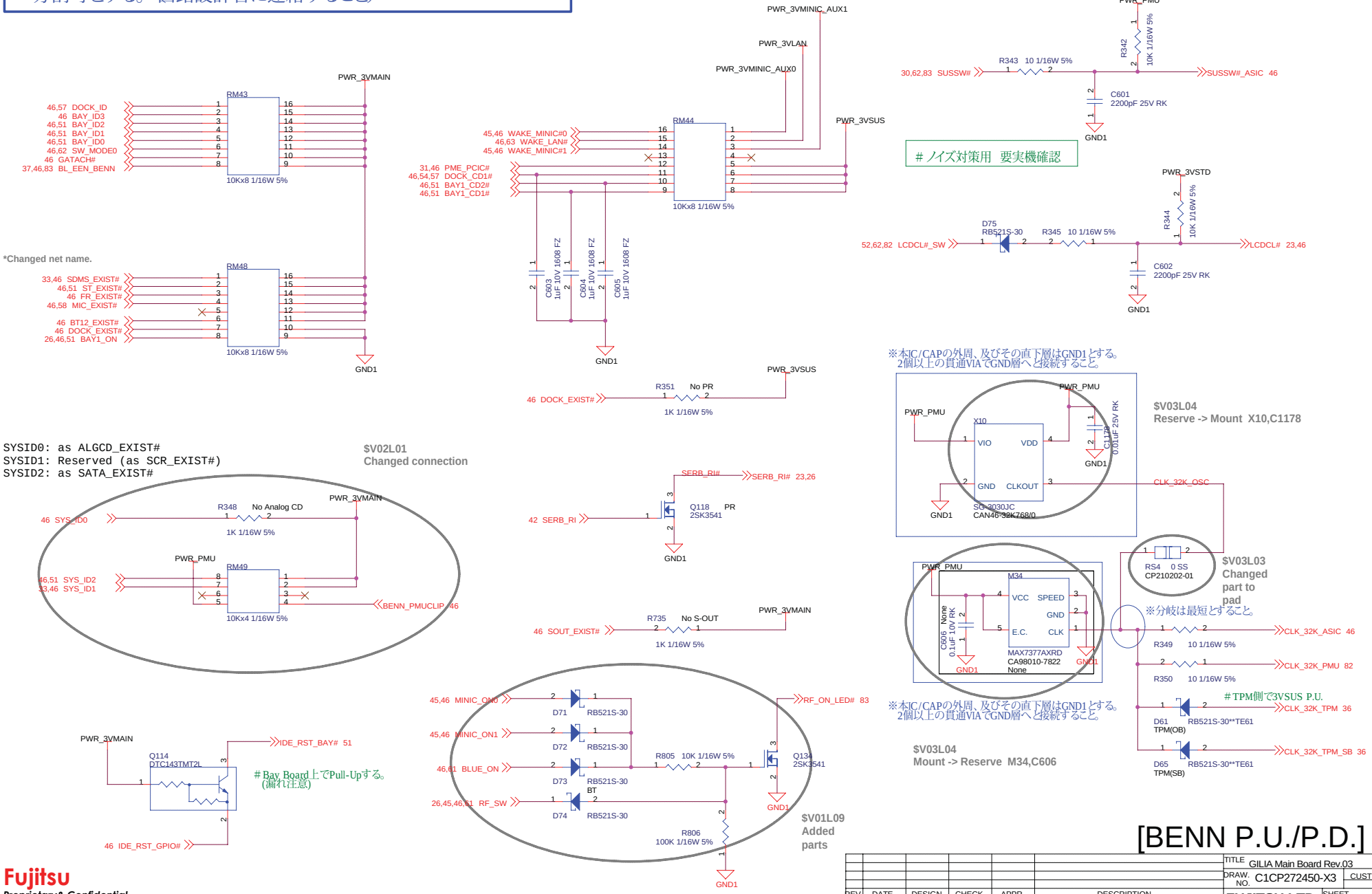
	2006.01.26	Seki	Yamada	Miura	

TITLE: GILIA Main Board Rev.03
DRAW. NO.: C1CP272450-X3
CUST.
FUJITSU LTD.
SHEET 45 / 91



※本項の部品は指示のない限りBENNの近くに配置すること。
集合抵抗を個別の抵抗に分割することで配線が有利になる場合、
分割可とする。(回路設計者に連絡すること)



SYSID0: as ALGCD_EXIST#
SYSID1: Reserved (as SCR_EXIST#)
SYSID2: as SATA_EXIST#

[BENN P.U./P.D.]

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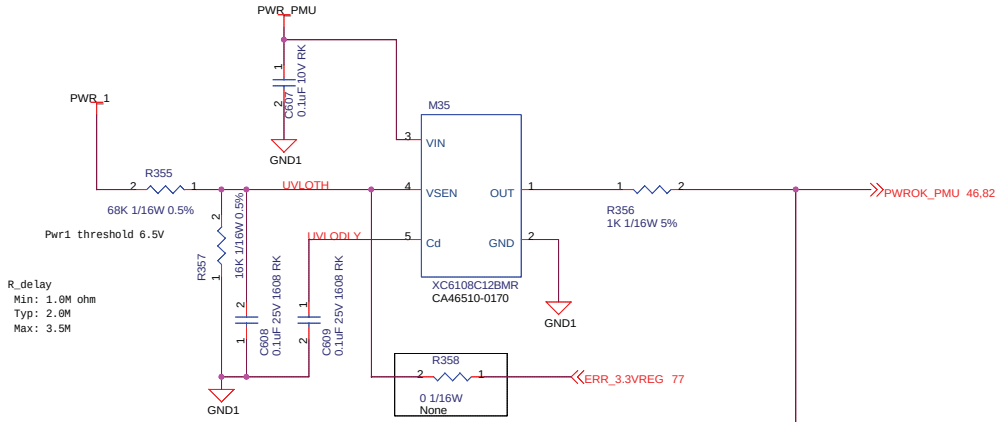
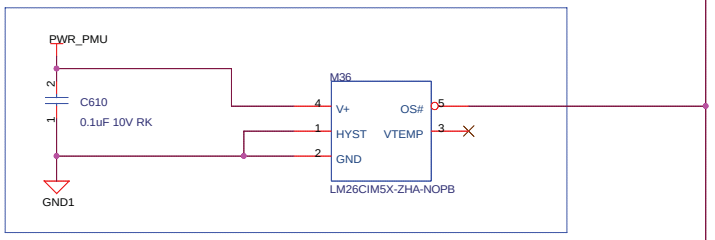
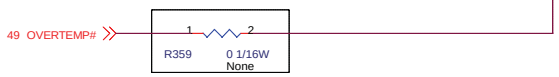
REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	2006.01.26	Seki	Yamada	Miura	

TITLE: GILIA Main Board Rev.03
DRAW. NO.: C1CP272450-X3
CUST.
FUJITSU LTD.
SHEET 47 / 91



※CPU-DDCの直近に配置すること





[Reset]

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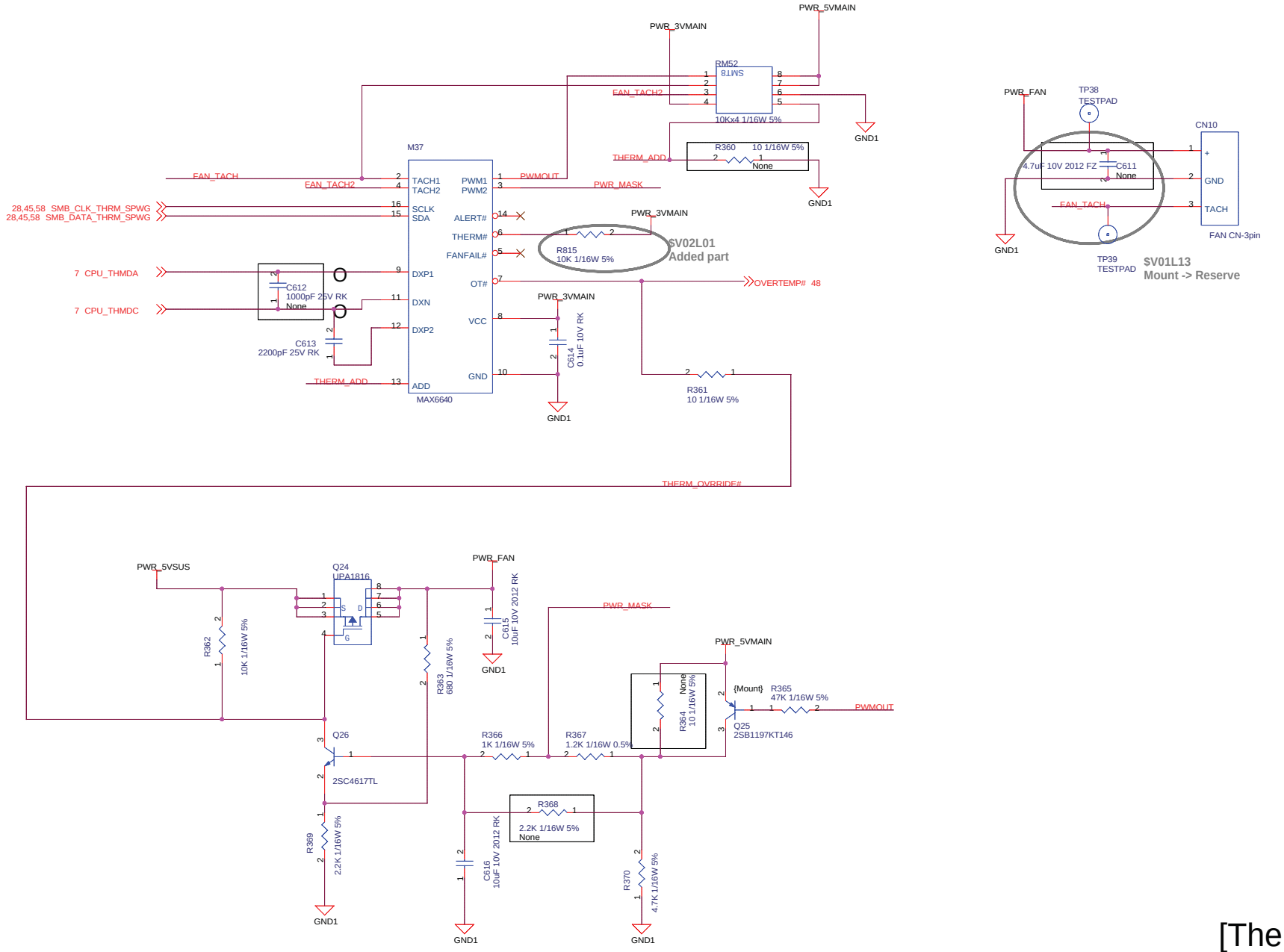
REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	2006.01.26	Seki	Yamada	Miura	

TITLE GILIA Main Board Rev.03
DRAW. NO. C1CP272450-X3 CUST.
FUJITSU LTD. SHEET 48 / 91



[Thermal]

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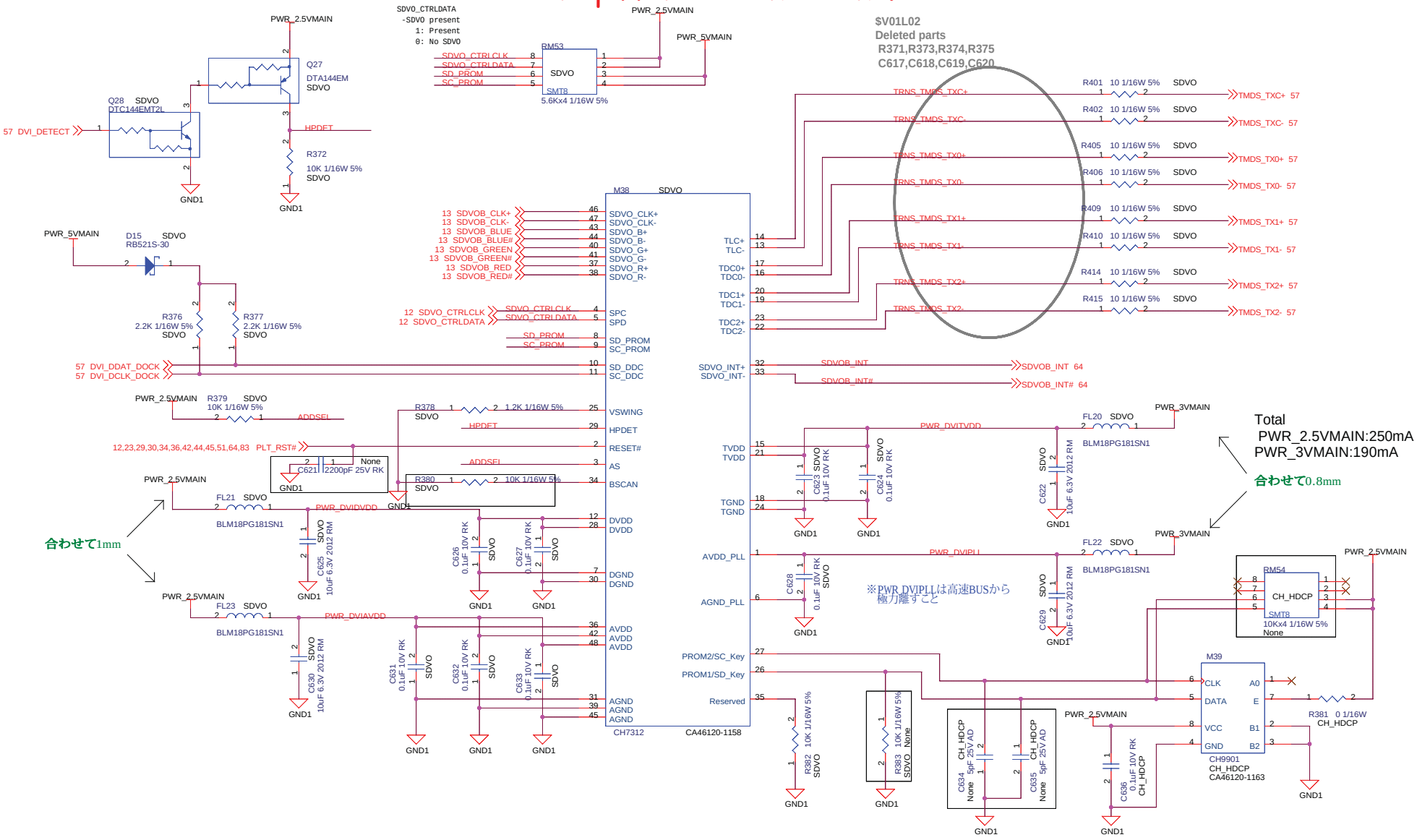
	DATE	2006.01.26	DESIGN	Seki	CHECK Yamada APPR Miura

TITLE GILIA Main Board Rev.03
DRAW. NO. C1CP272450-X3 CUST.
FUJITSU LTD. SHEET 49 / 91



	CH7307	CH7312
Pin 26	BSCAN (PD)	SD_Key
Pin 27	Reserved (NC)	SC_Key
Pin 34	Reserved (NC)	BSCAN (PD)
Pin 35	Reserved (NC)	Reserved (PD)

[DVI Tranmitter]

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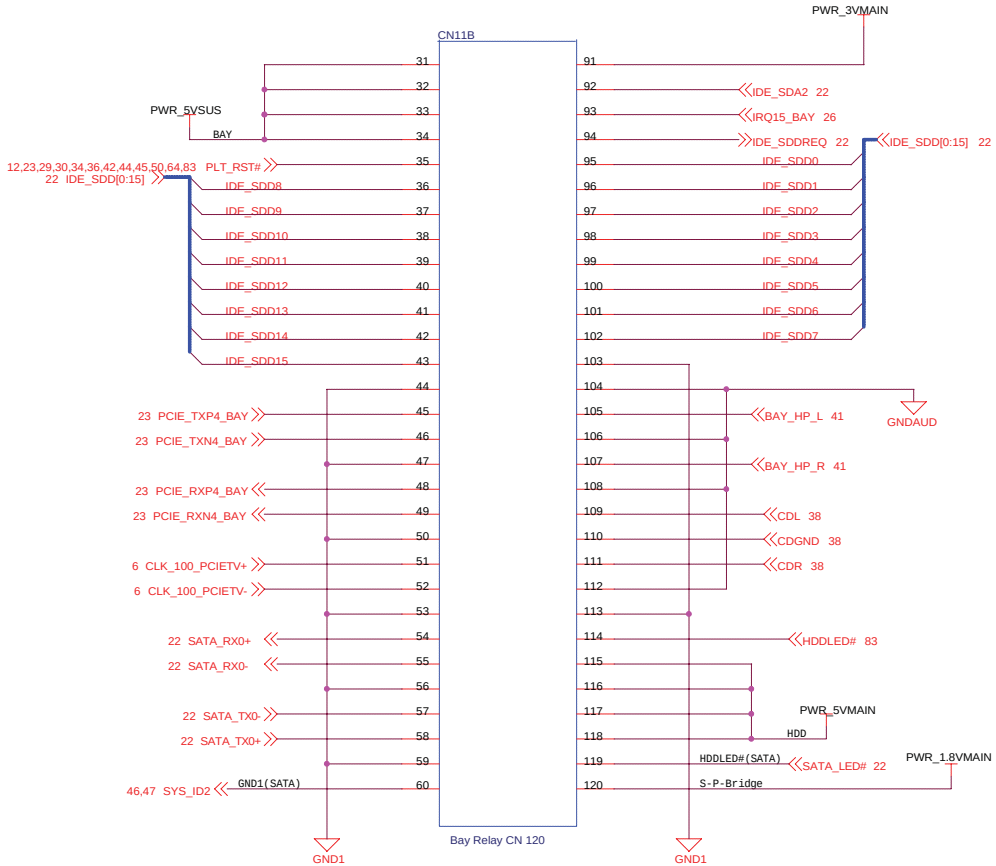
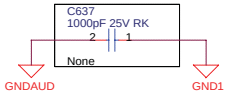
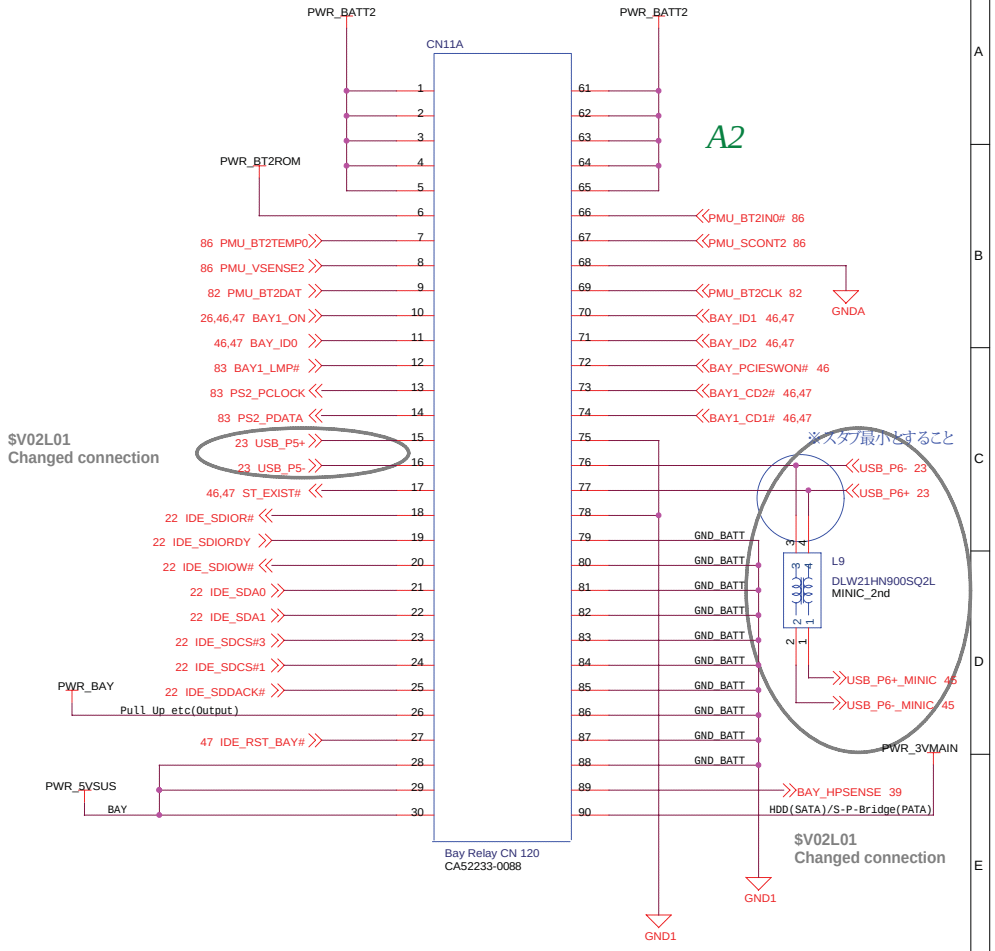
FUJITSU LTD. SHEET 50 / 91

$V01L02
Changed connection CN11
$V01L05
Changed connection CN11



AC/DC 0.3A/pin





$V02L01
Changed connection

※スタブ最小とすること

$V02L01
Changed connection

[CN - BAY Board]

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	DATE 2006.01.26	DESIGN Seki	CHECK Yamada	APPR Miura	

TITLE GILIA Main Board Rev.03
DRAW. NO. C1CP272450-X3 CUST.
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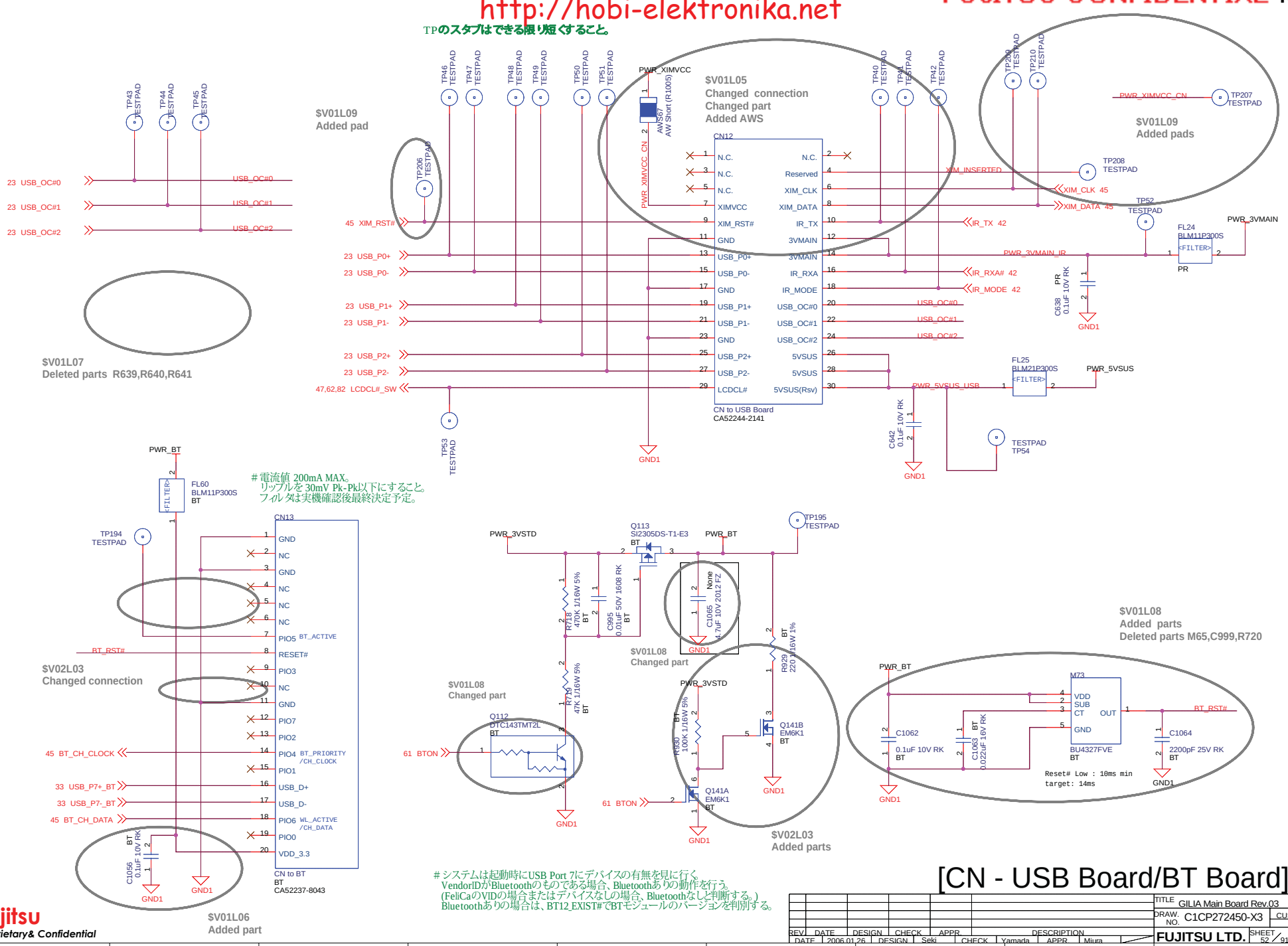
TPのスタブはできる限り短くすること。

[CN - USB Board/BT Board]



＃電流値 200mA MAX。
リップルを 30mV Pk-Pk以下にすること。
フィルタは実機確認後最終決定予定。

＃システムは起動時にUSB Port 7にデバイスの有無を見に行く。
VendorIDがBluetoothのものである場合、Bluetoothありの動作を行う。
(FeliCaのVIDの場合またはデバイスなしの場合、Bluetoothなしと判断する。)
Bluetoothありの場合は、BT12_EXIST#でBTモジュールのバージョンを判別する。

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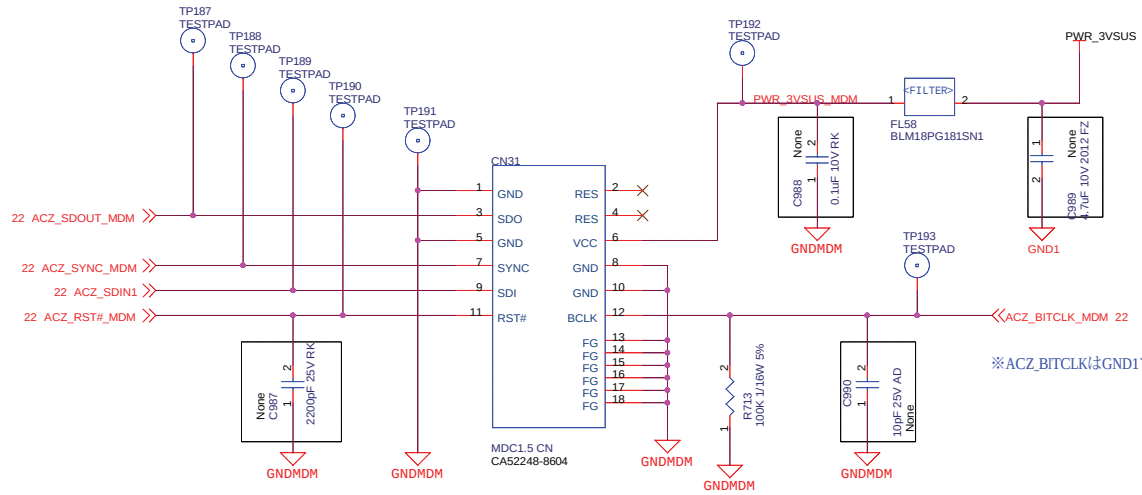
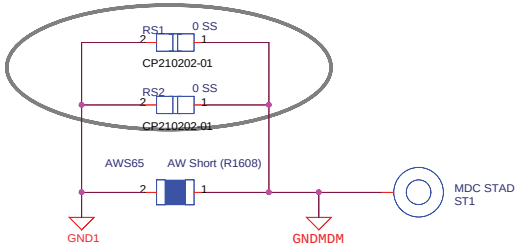
TITLE: GILIA Main Board Rev.03
DRAW. NO.: C1CP272450-X3
CUST.:
FUJITSU LTD.
SHEET 52 / 91



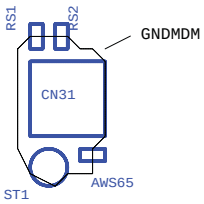
※ACZ_BITCLKはGND1でガードすること。

$V02L01
Added pads.

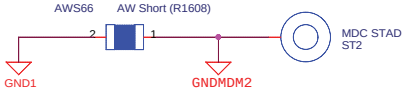
$V02L10
Changed parts



※RS1,RS2の配置は下の図参照。



※RSxxは、はんだショート用パッドのため、パッド間のパターン接続はしないこと。
(1pin - 2pin間をアートワークで接続しないこと。)



※ST1,ST2は内層でGND1へと接続しないこと。

[MDC]

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	DATE 2006.01.26	DESIGN Seki	CHECK Yamada	APPR Miura	

TITLE GILIA Main Board Rev.03
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[VGA Switch]

＃各RGB配線について、スタブが最小となるように配線すること。

65 CRT_RED_EXTVGA
R384 0 1/16W EXTVGA
13 CRT_RED_GMCH
R385 0 1/16W No EXTVGA
R386 0 1/16W CRT(JC)/CRT(JR)
R388 0 1/16W CRT(JC)

65 CRT_GREEN_EXTVGA
R390 0 1/16W EXTVGA
13 CRT_GREEN_GMCH
R391 0 1/16W No EXTVGA
R392 0 1/16W CRT(JC)/CRT(JR)
R394 0 1/16W CRT(JC)

65 CRT_BLUE_EXTVGA
R395 0 1/16W EXTVGA
13 CRT_BLUE_GMCH
R396 0 1/16W No EXTVGA
R397 0 1/16W CRT(JC)/CRT(JR)
R399 0 1/16W CRT(JC)

M66
CRT_RED_SW → DA
CRT_GREEN_SW → DB
CRT_BLUE_SW → DC
DD
IN
EN#
S1A → CRT_RED_PR 57
S2A → CRT_RED_MAIN 56
S1B → CRT_GREEN_PR 57
S2B → CRT_GREEN_MAIN 56
S1C → CRT_BLUE_PR 57
S2C → CRT_BLUE_MAIN 56
S1D
S2D
VCC
GND
PI5V330S CRT(WW)
CA98010-7674

$V01L08
Changed connection

$V01L11
Changed connection

46,47,57 DOCK_CD1#
0: S1x Enable
1: S2x Enable
R814 470K 1/16W 5% CRT(WW)
C643 0.1uF 10V RK CRT(WW)
C996 None 4.7uF 6.3V 1608 RK CRT(WW)
PWR_3VSTD
GND1

“dŒ¹,ð•Afpf^•[f“,ï“s•‡,ÅSTD,É•Ï•X•B
DOCK_CD1#,ï3VSUS P.U.

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TITLE GILIA Main Board Rev.03
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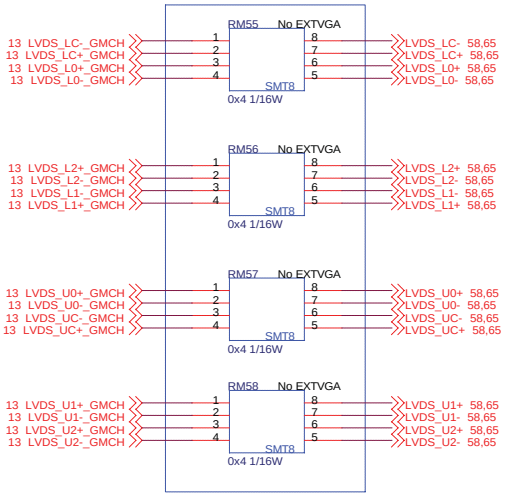
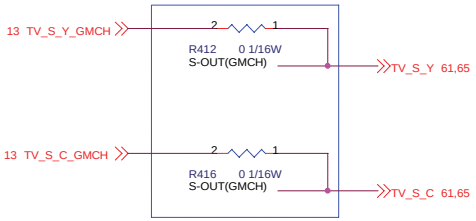
FUJITSU LTD.
SHEET 54 / 91

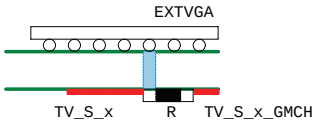
※下記の抵抗は外部VGAの端子直近に配置すること。
分岐から抵抗までの配線長は極力0に近づけること



※下記の抵抗は外部VGAの端子直近に配置すること。
分岐から抵抗までの配線長は極力0に近づけること



＃配線イメージ



[VGA Jumper]

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REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	2006.01.26	Seki	Yamada	Miura	

TITLE GILIA Main Board Rev.03
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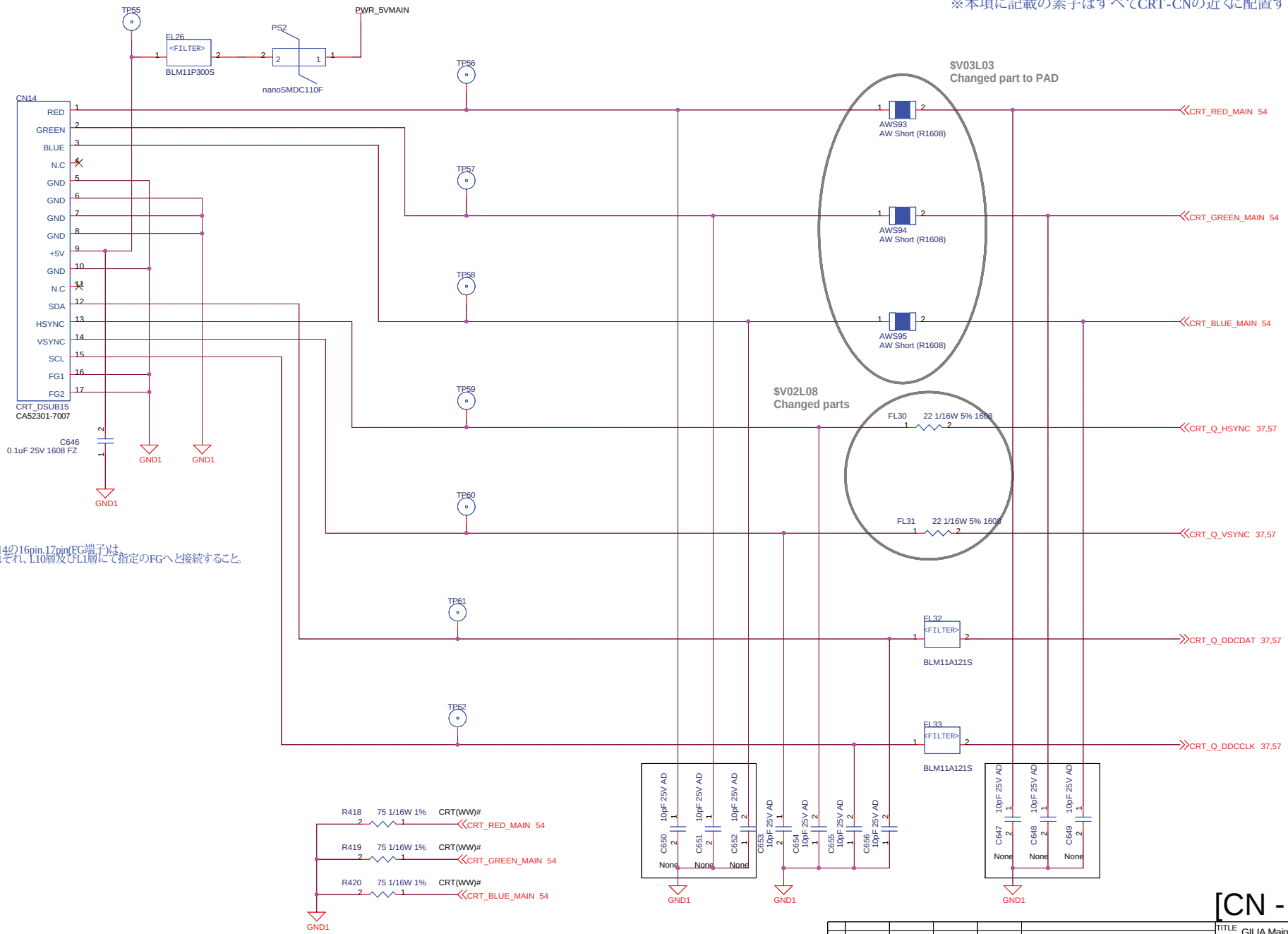
FUJITSU LTD. SHEET 55 / 91

※本項に記載の素子はすべてCRT-CNの近くに配置すること



※CN14の16pin,17pin(FG端子)は、
それぞれ、L10層及びL1層にて指定のFGへと接続すること。

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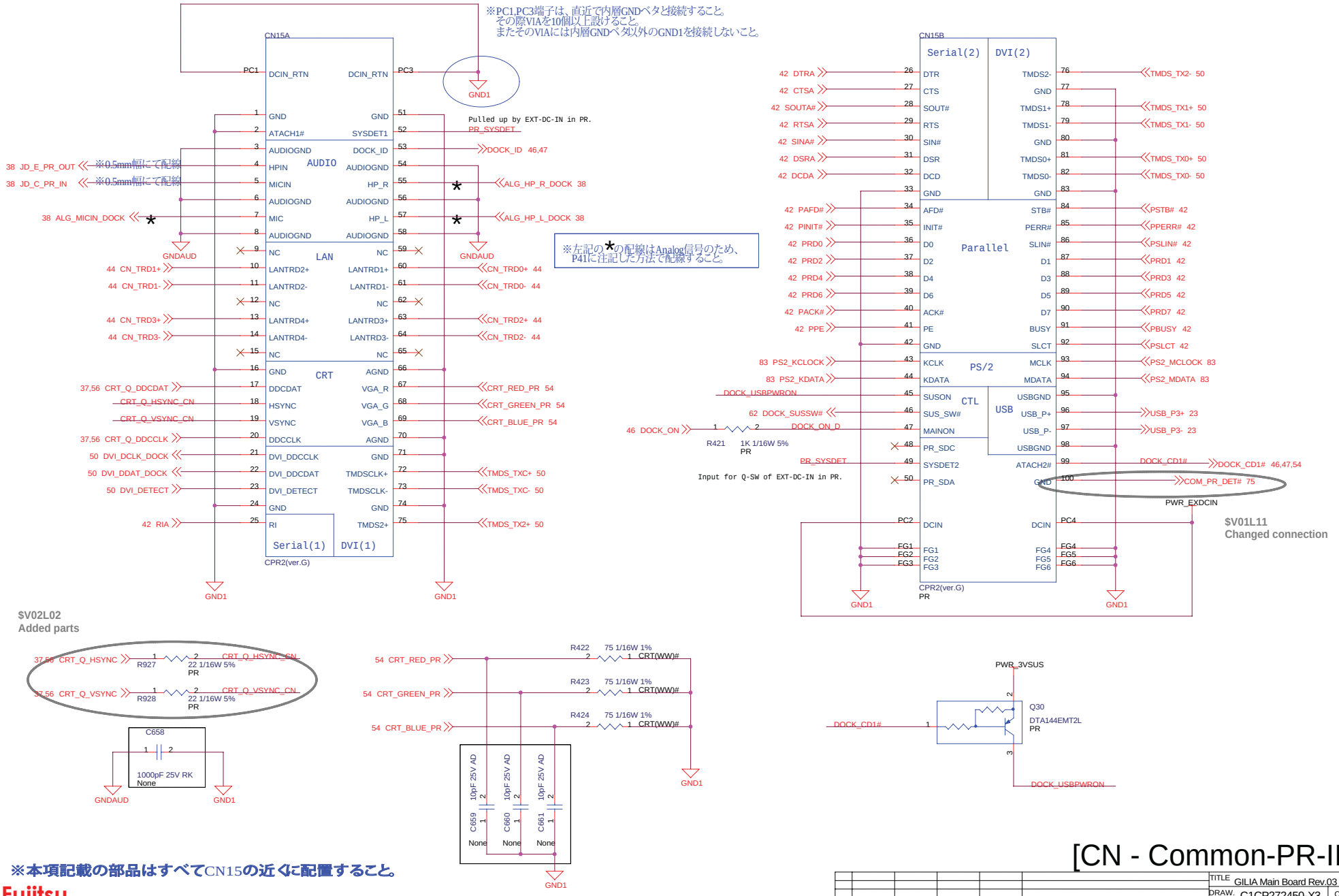
[CN - CRT]

REV	DATE	DESIGN	CHECK	APPR	DESCRIPTION
	2006.01.26	Seki	Yamada	Miura	

TITLE GILIA Main Board Rev.03
DRAW. NO. C1CP272450-X3 CUST.
FUJITSU LTD. SHEET 56 / 91



※回路図中の * 印はAnalogLineのため、0.25mm以上の幅で配線し、
可能な限りGNDAUDでガード(上下層を含む)すること。
ガード配線が難しい場合は、他のデジタル信号に対し0.25mm以上のGAPを設けること。
AnalogLineとAnalogGNDの隣接はかまわない。

$V02L01
Added parts

※FL67, FL68, FL69はCN16の直近に配置すること。

$V01L07
Changed part F3

$V02L01
Changed connection

＃PRのUSB、ここまでもってくる？

＃LCDID3,4はGILIAではHigh固定とする。

＃電圧効果注意！パターン/VIA必ず確認！

※43pin, 45pinは表層で他のGND1パターンへと接続しないこと。

$V01L07
Changed part F2
$V01L08
Changed connection(Changed each place of F2 and F5)

$V01L08
Changed connection

[CN - LCD]

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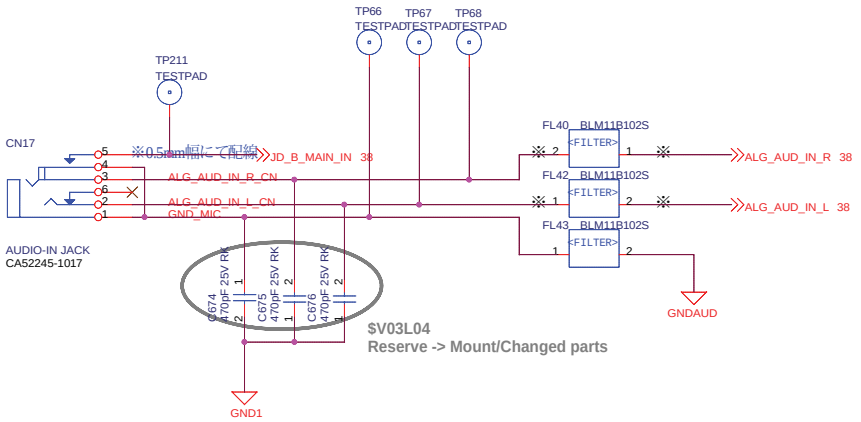
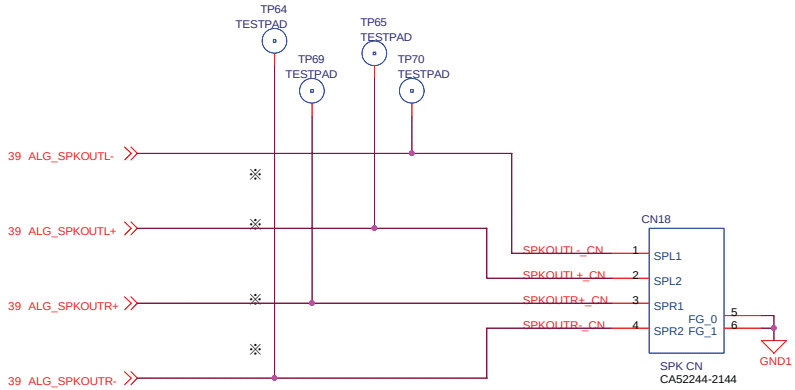
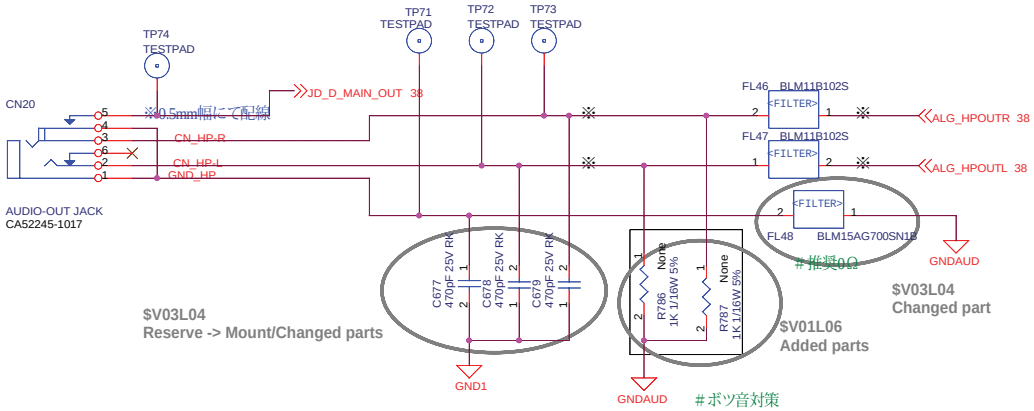
	2006.01.26	Seki	Yamada	Miura	

TITLE GILIA Main Board Rev.03
DRAW. NO. C1CP272450-X3 CUST.
FUJITSU LTD. SHEET 58 / 91

＃MIC CNは削除。LCD-CNにアサイン







本ページ中に記載されているフィルタ(FLxx)はそれぞれ接続されているコネクタの近くに配置し、フィルターコネクタ間の配線は非常に短く配線すること。
The filters in this page (refered with FLxx) have to be placed near each connector connecting to respective filters. The traces between connector and filter have to be short as much as possible.

本項中※印のついたパターンは、GND_AUDでガードし、その上下はGND_AUDのベタパターンで覆うこと。また、Mxの下の基板面およびその下の層には、ディジタル系の信号線を配線しないこと。
The traces marked with ※ have to be guarded both side and both adjacent layer with AUDIOGND. Underneath Mx on surface layer and in one more internal layer don't allow digital traces to be run.

[CN - Audio]

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE 2006.01.26	DESIGN Seki	CHECK Yamada	APPR. Miura	

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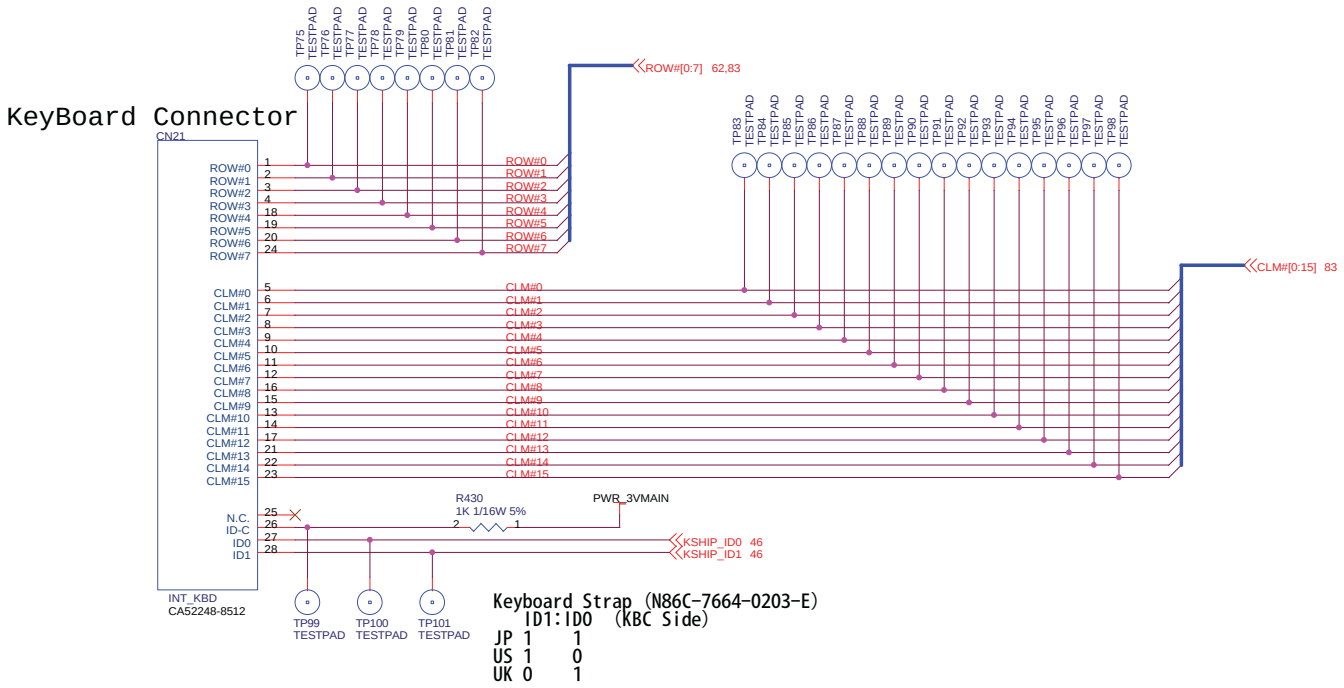

$V01L05
Deleted parts CN22,CN23

[CN - Keyboard]

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REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	2006.01.26	Seki	Yamada	Miura	

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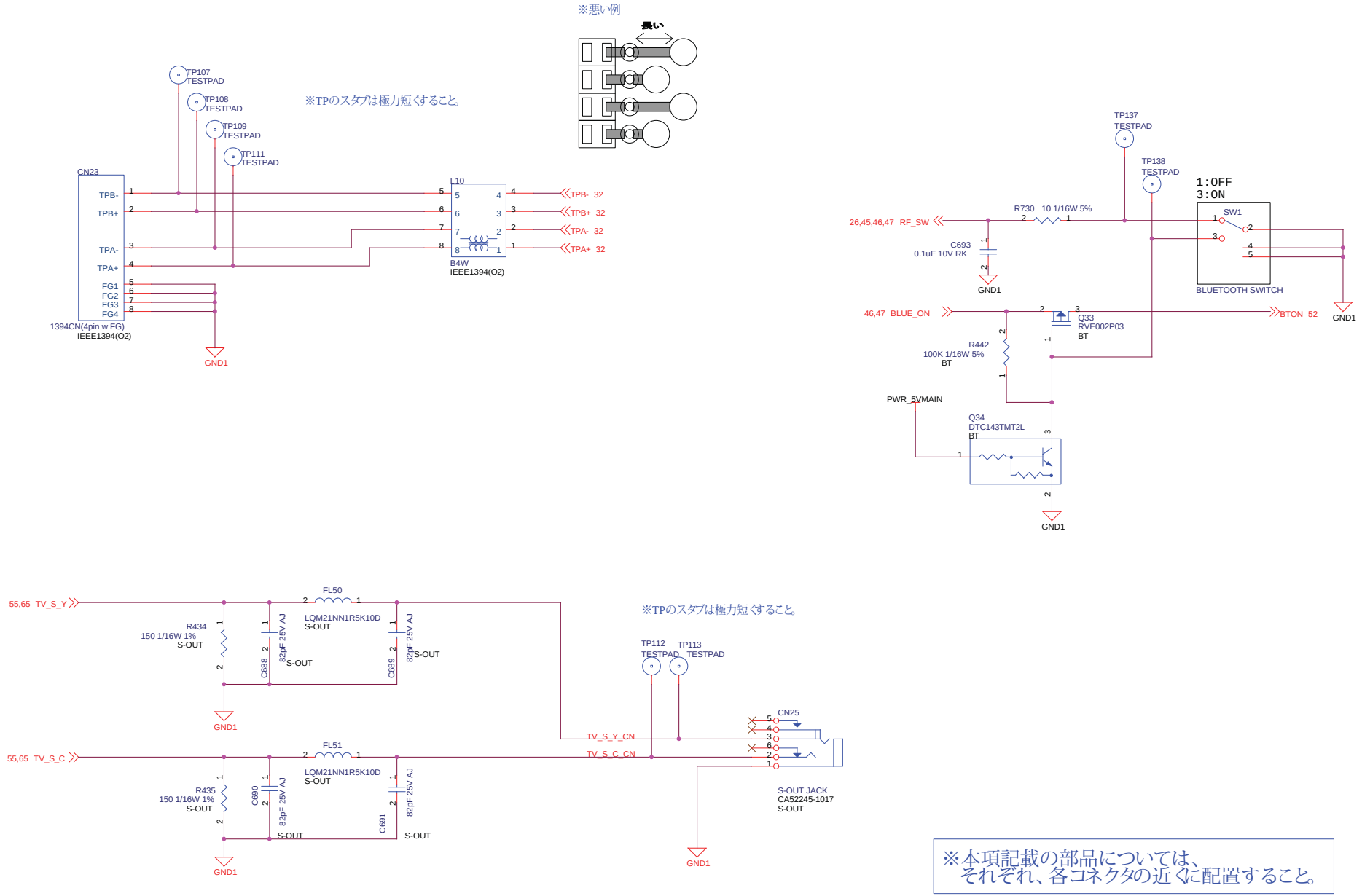

[CN - 1394/S-out/RF-SW]

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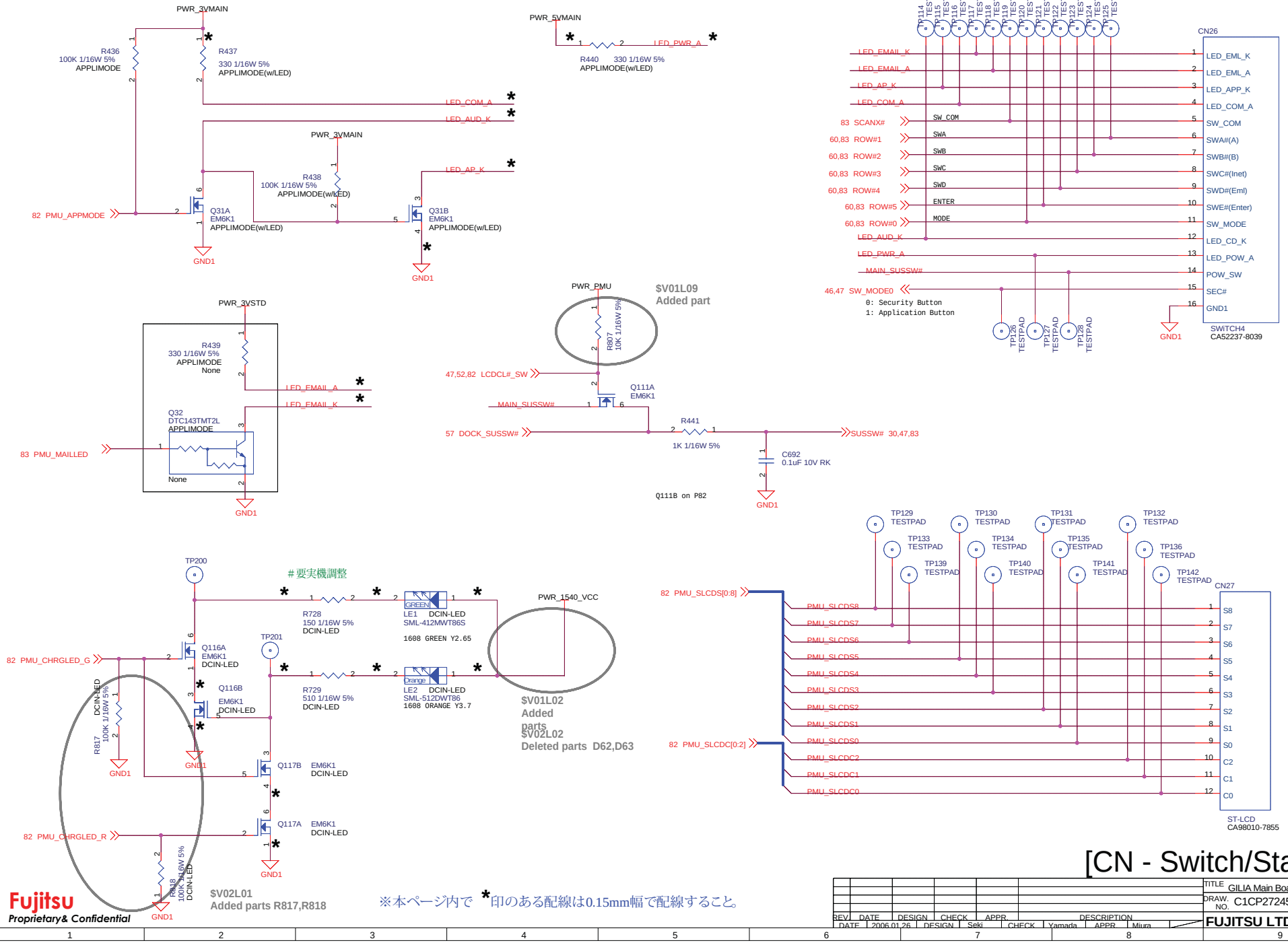

[CN - Switch/Status]

※本ページ内で *印のある配線は0.15mm幅で配線すること。

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REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE 2006.01.26	DESIGN Seki	CHECK Yamada	APPR Miura	

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$V02L03
Changed connections
Changed part to pad
$V02L11
Changed parts

$V02L01
Changed connection

$V02L05
Deleted part R797
Changed connection

$V02L03
Changed parts to pads
$V02L05
Changed connection

$V02L08
Changed part

$V03L01
Changed part

$V02L08
Changed part

$V03L01
Changed part

$V02L03
Changed part to pad

$V02L04
Added part
$V02L11
Reserve -> Mount

Moved R931 and R309 from P44

$V02L10
Decided part number

※部品下メタルパット(65pin)は4隅にそれぞれVIAを設けてGND1に接続すること。

$V02L11
Changed part

[LAN-3(Marvel)]

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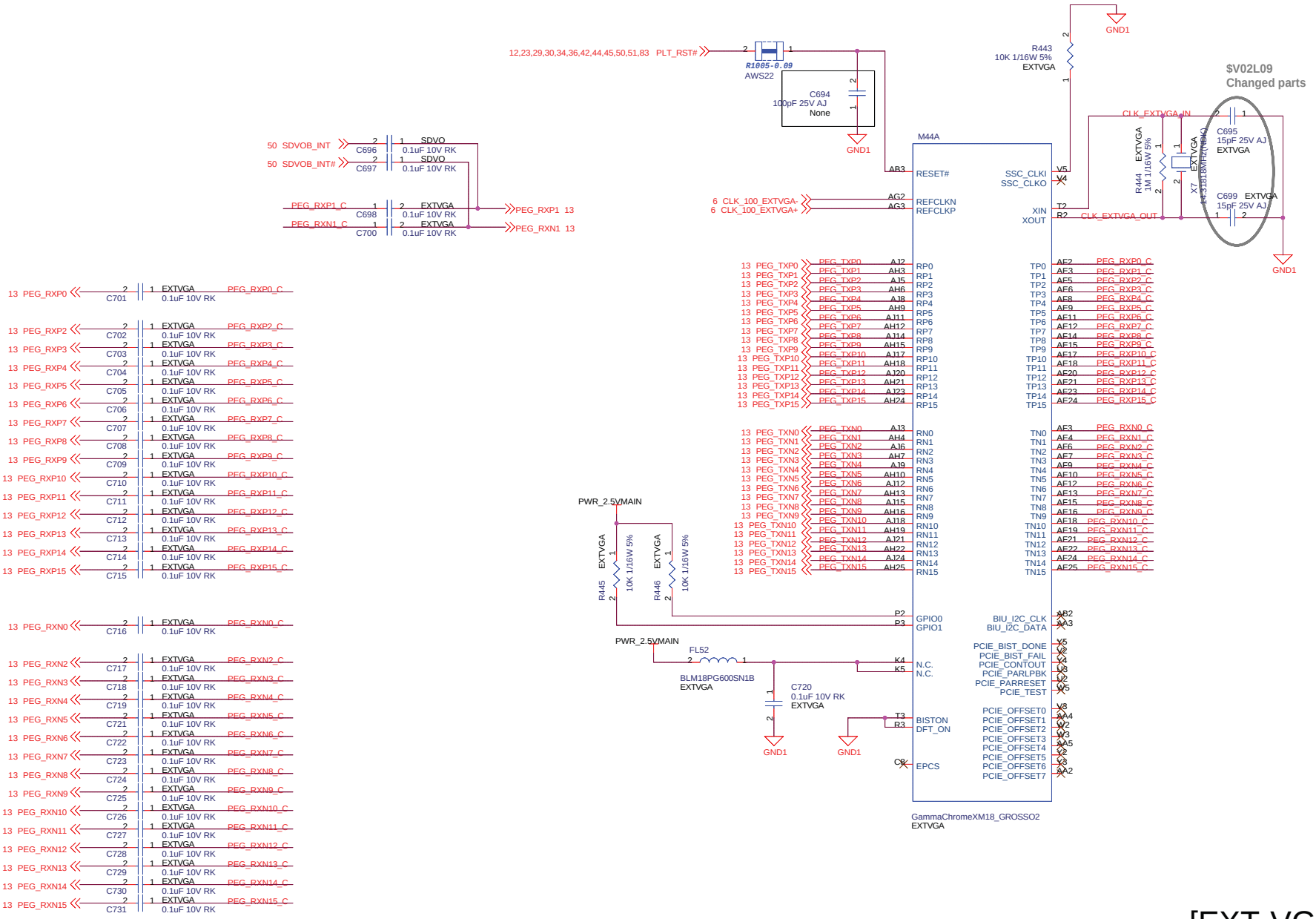
FUJITSU LTD.	SHEET	63 / 91

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	2006.01.26	DESIGN	Seki	CHECK Yamada APPR Miura



[EXT-VGA-1]

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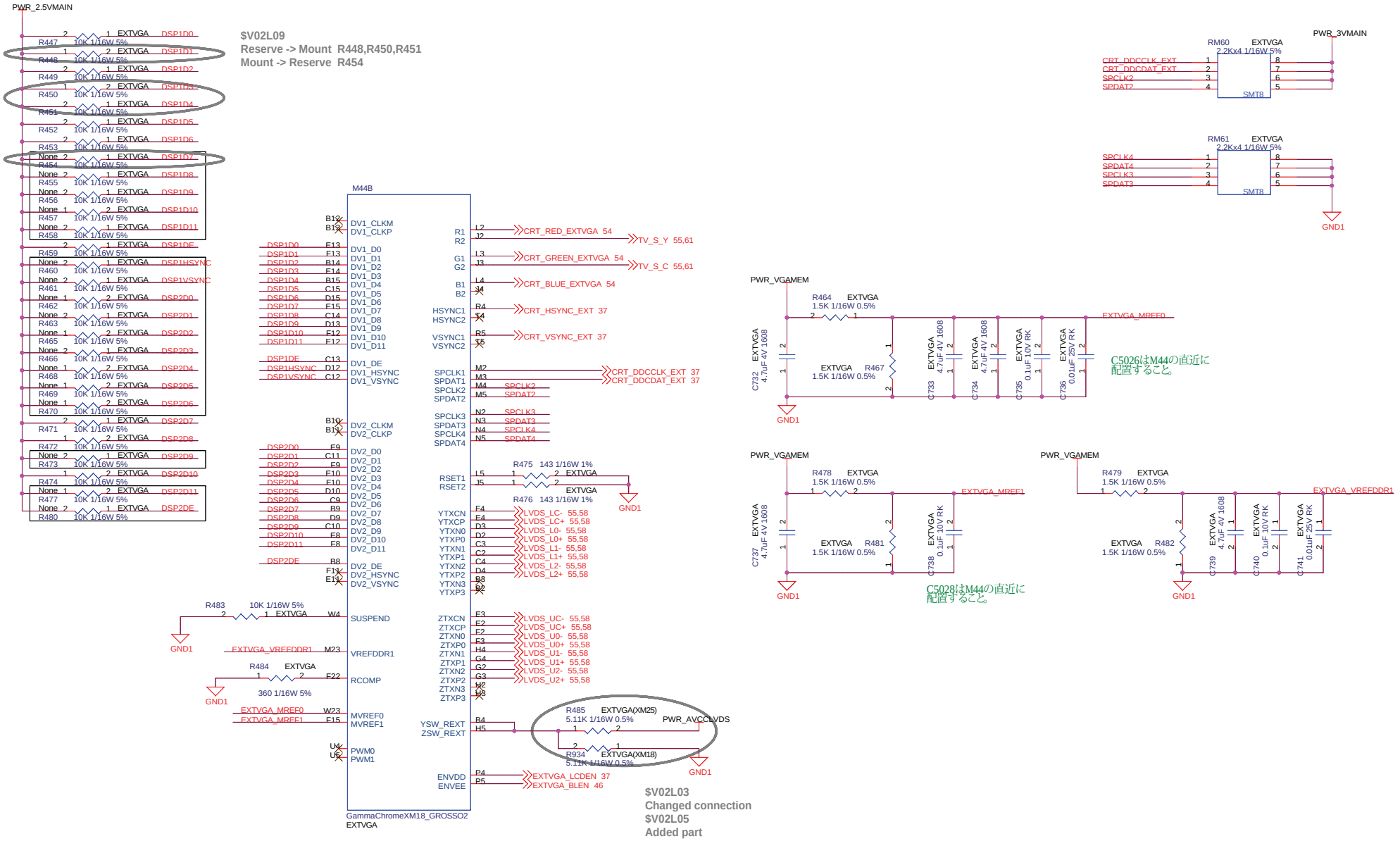
TITLE	GILIA Main Board Rev.03		
DRAW. NO.	C1CP272450-X3	CUST.	
FUJITSU LTD.		SHEET	64 / 91

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	2006.01.26	Seki	Yamada	Miura	



[EXT-VGA-2]

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REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION		
	DATE	2006.01.26	DESIGN	Seki	CHECK	Yamada	APPR. Miura

TITLE GILIA Main Board Rev.03
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$V01L10 Changed parts

PWR_VGACORE: DDC
PWR_VGAMEM: DDC
PWR_VGA1.0V: LDO
PWR_VGA1.4V: LDO

$V01L10 Changed part

$V01L10 Changed part

No description about M9/P9 pin on reference schematics.

M44C

GammaChromeXM18_GROSSO2 EXTVGA

[EXT-VGA-3]

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	2006.01.26	Seki	Yamada	Miura	

TITLE GILIA Main Board Rev.03
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CUST.
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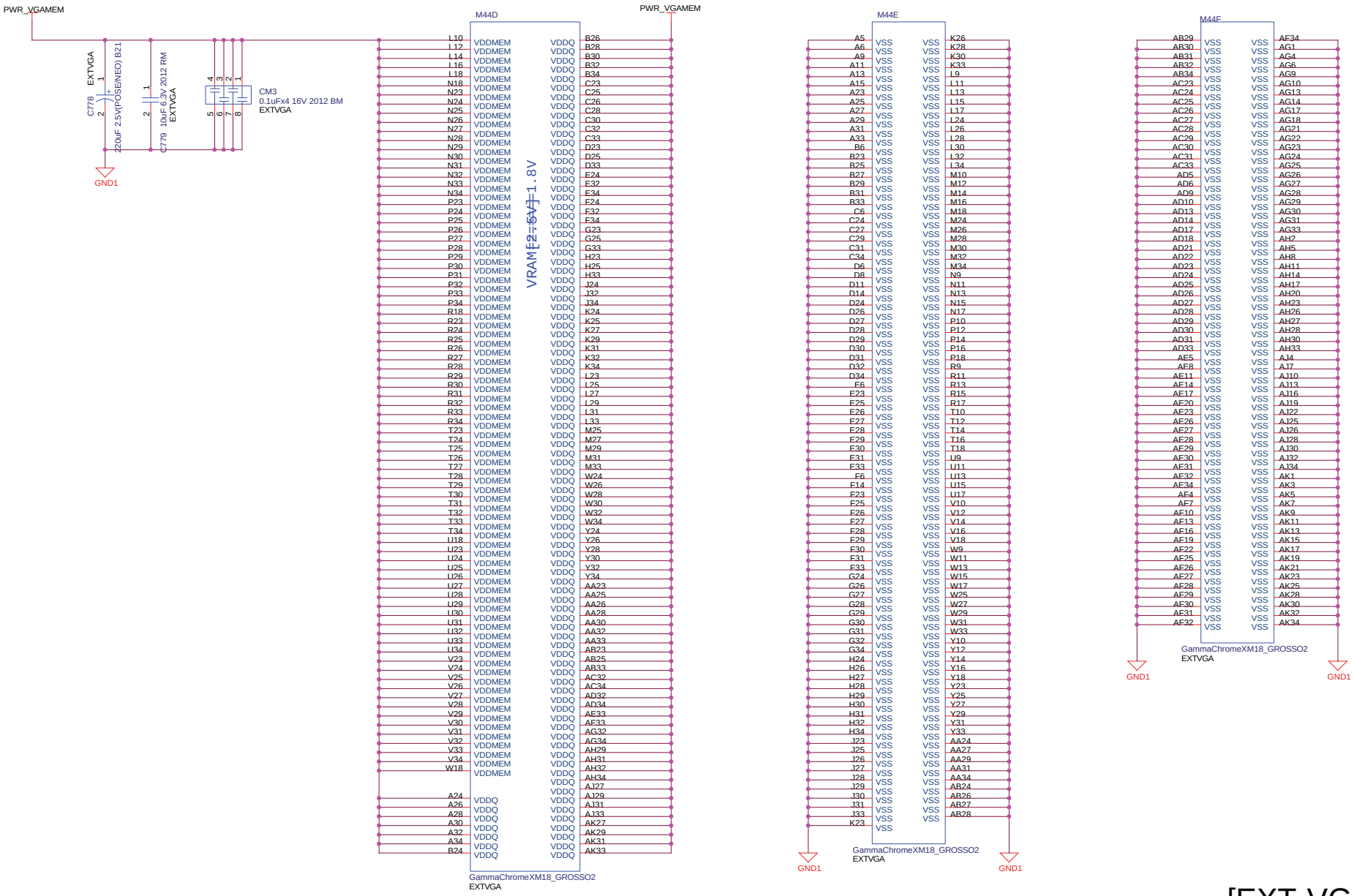

[EXT-VGA-4]

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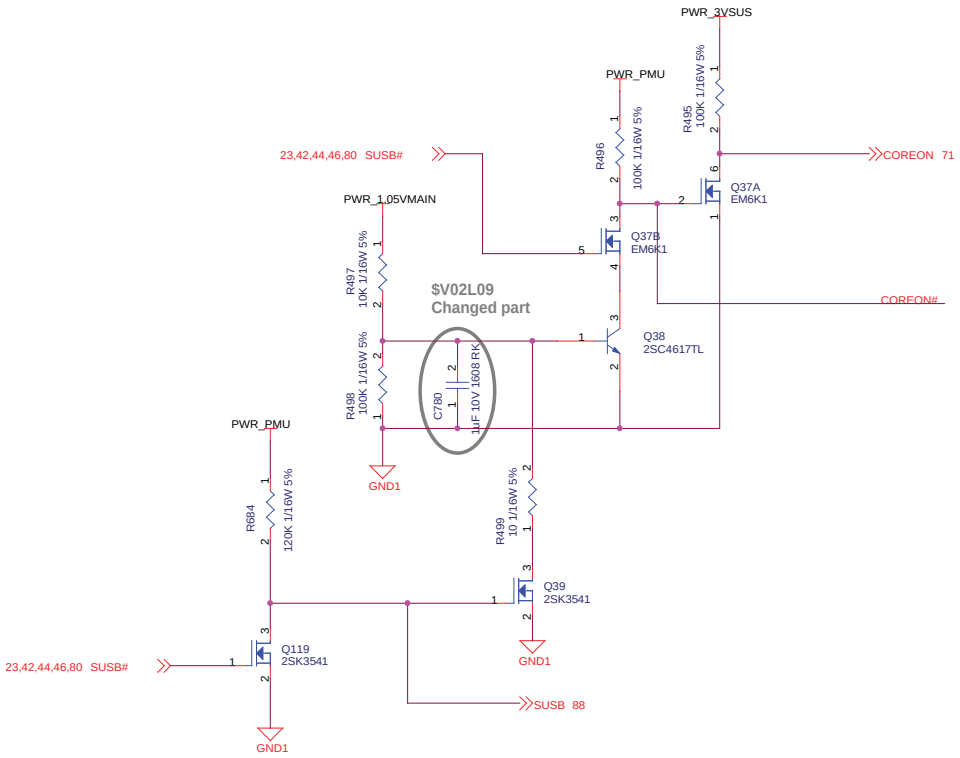
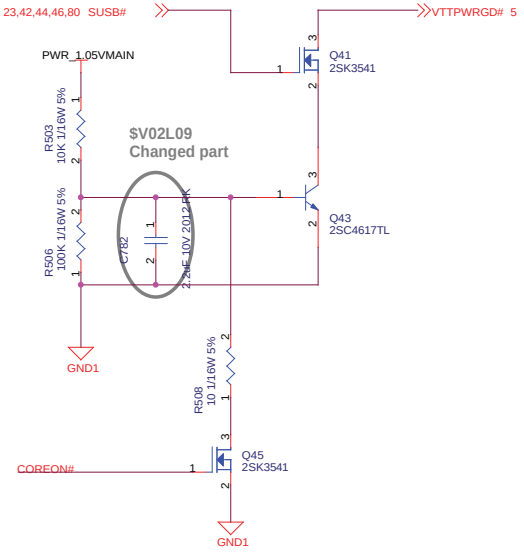
REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION	TITLE	GILIA Main Board Rev.03
	2006.01.26	Seki		Yamada	Miura	DRAW. NO.	C1CP272450-X3 CUST.
						FUJITSU LTD.	SHEET 67 / 91

＃見直し予定





POWER_SEQUENCE/DISCHARGE

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	2006.01.26	Seki	Yamada	Miura	

TITLE GILIA Main Board Rev.03
DRAW. NO. C1CP272450-X3 CUST.
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Gilia Power Supply

Temporary

Caution

See "design guide for power circuit" Keep design rule.

Features

1/ Voltage Regulator for Mobile Yonah Processor (IMVP6)
2/ Calistoga Chipset (CoreVoltage=1.05V only)
3/ DDR2 533MHzSODIMM(Vddq=1.8V only)
4/ Internal VGA or ExVGA:S3 Gamma Chrome
5/ Quick Charging Power Supply (Target: 2.5hours)
6/ 19V AC Adaptor
7/ A circuit reducing a rush current from AC adaptor
8/ Internal Battery with 3 Seirial cells and Digital Interface
9/ Bay Battery with 3 Seirial cells and Analog Interface
10/ Common PortReplicator 2 support

Power Contents

	Contents	Page#		Contents	Page#
	TopPage	69	Node	DCIn,Battery	78
	Delivery	70		PWR_1	79
DDC	CPUCore1	71		Switch1	80
	CPUCore2	72	PMU	LUNA1 (PMU part)	82
	1.05V/1.8V	73		LUNA2 (KBC part)	83
	3.3V/5V	74		Etc0 (Common)	84
	Charger	75		Etc1 (Battery1)	85
LDO	System	76		Etc2 (Battery2)	86
	PMU	77	VGA	VGACore	88
				VGAMem	89
				VGA	90

Voltage Regulator Spec.

DDC	CPUCore	TBD	33Atyp / 44Apeak
	1.05VMain	1.050V +/-5% (0.998V-1.102V)	5Atyp / 6Apeak
	1.8VSus	1.800V +/-5% (1.710V-1.890V)	6Atyp / 8Apeak
	3.3VStd	3.300V +/-5% (3.135V-3.465V)	6Atyp / 8Apeak
	5VSus	5.000V +/-5% (4.750V-5.250V)	6Atyp / 8Apeak
Charger	CV 3-serial 12.60V +/-1.2% (12.45V-12.75V)		CC 3.0A
LDO	DimmVtt	0.900V +/-100mV (0.800-1.000V)	+-0.25Atyp / +-1Apeak
	1.5VMain	1.500V +/-5% (1.425V-1.575V)	2.3A
	2.5VMain	2.500V +/-5% (2.375V-2.625V)	0.5A
	3VATVBG	3.300V +/-5% (3.135V-3.465V)	0.10A
	PMU	3.300V +/-2% (3.234V-3.366V)	30mA

Power/ TopPage

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	2006.01.26	Seki	Yamada	Miura	

TITLE: GILIA Main Board Rev.03
DRAW. NO.: C1CP272450-X3 CUST.
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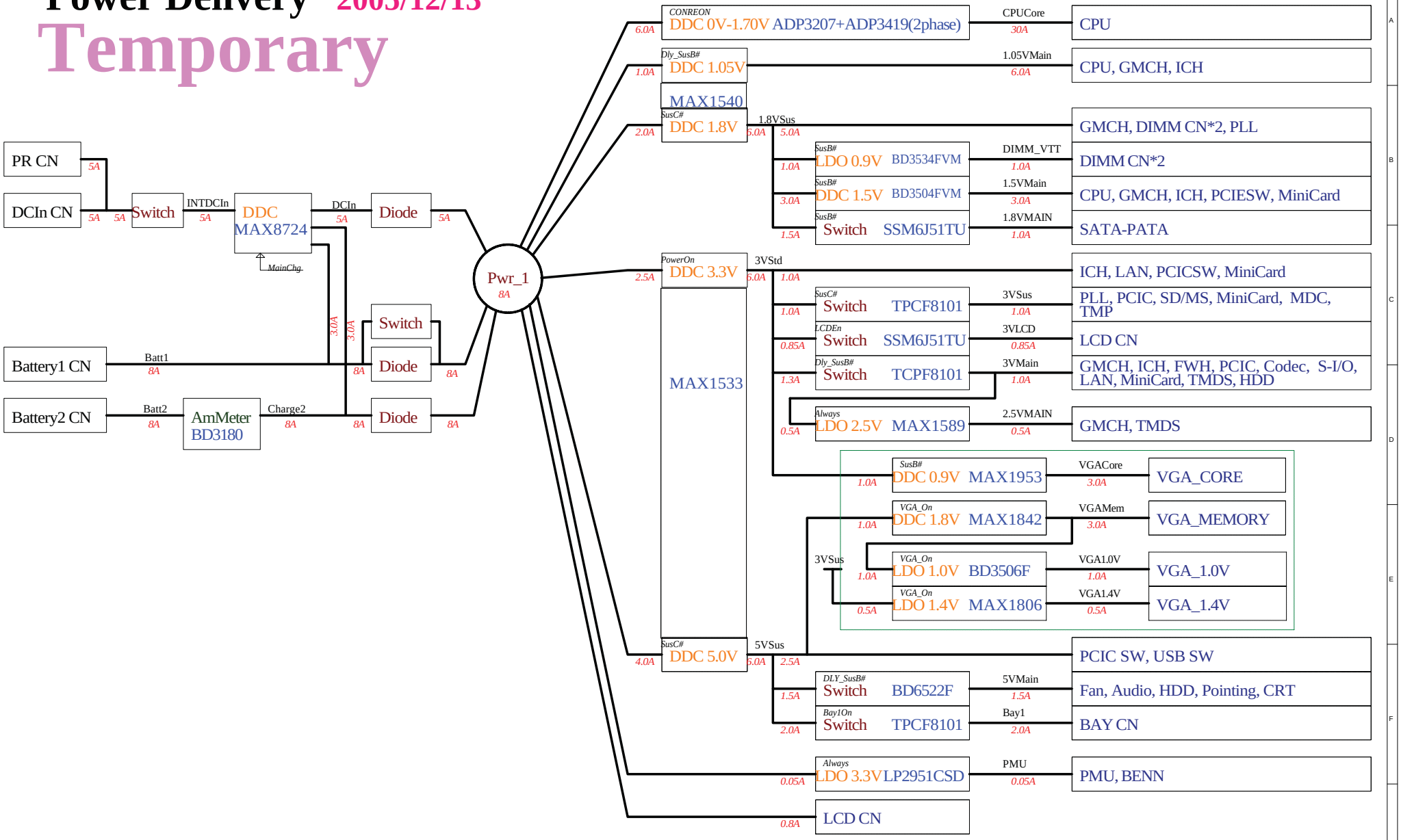
DDC ; DC to DC Convertor

Power Delivery 2005/12/13

Temporary



Power/ Delivery

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
DATE	2006.01.26	DESIGN	Seki	CHECK	Yamada
				APPR.	Miura

TITLE: GILIA Main Board Rev.03
DRAW. NO.: C1CP272450-X3
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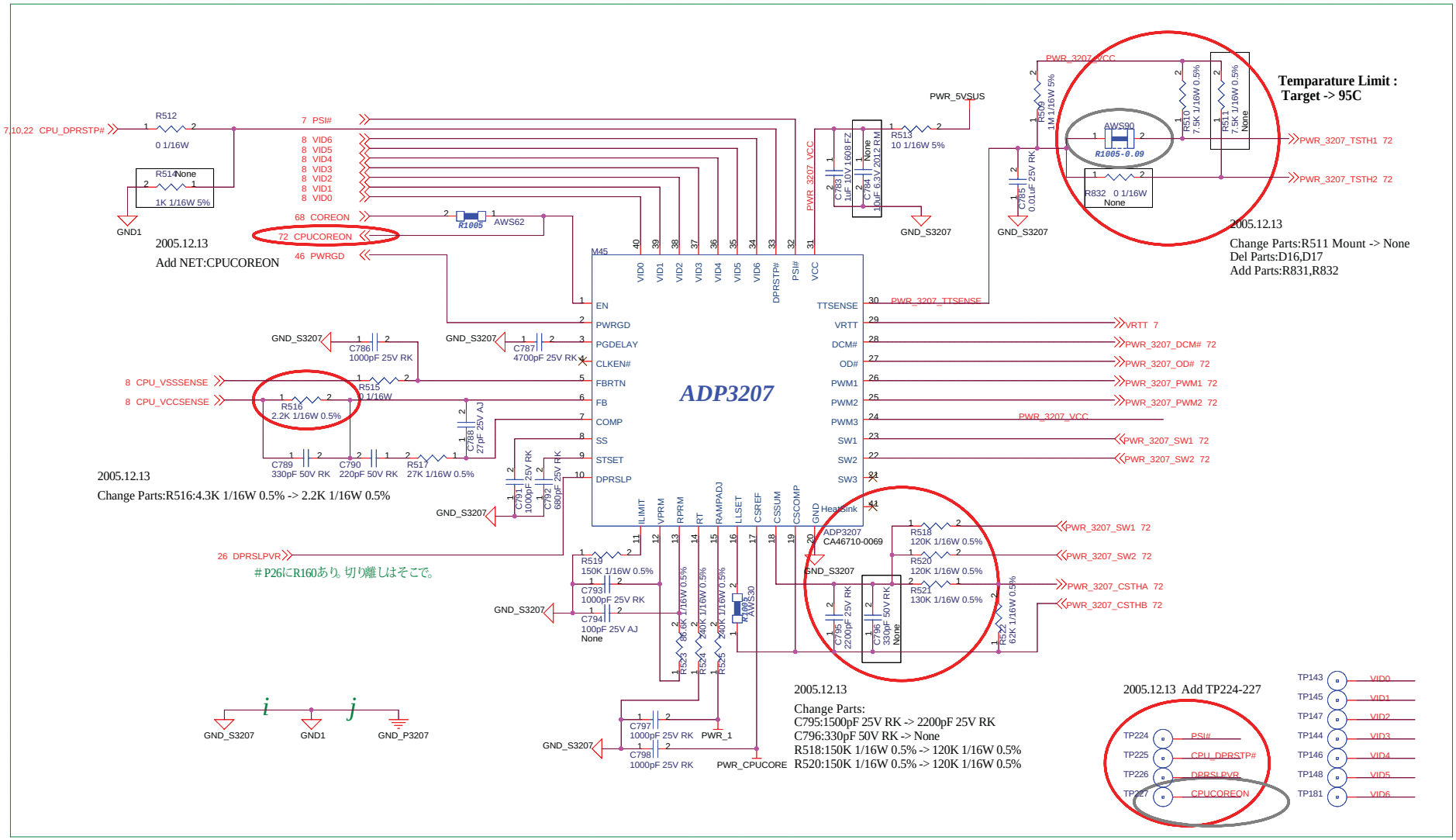
SHEET 70 / 91

$V03L03
Changed part to pad

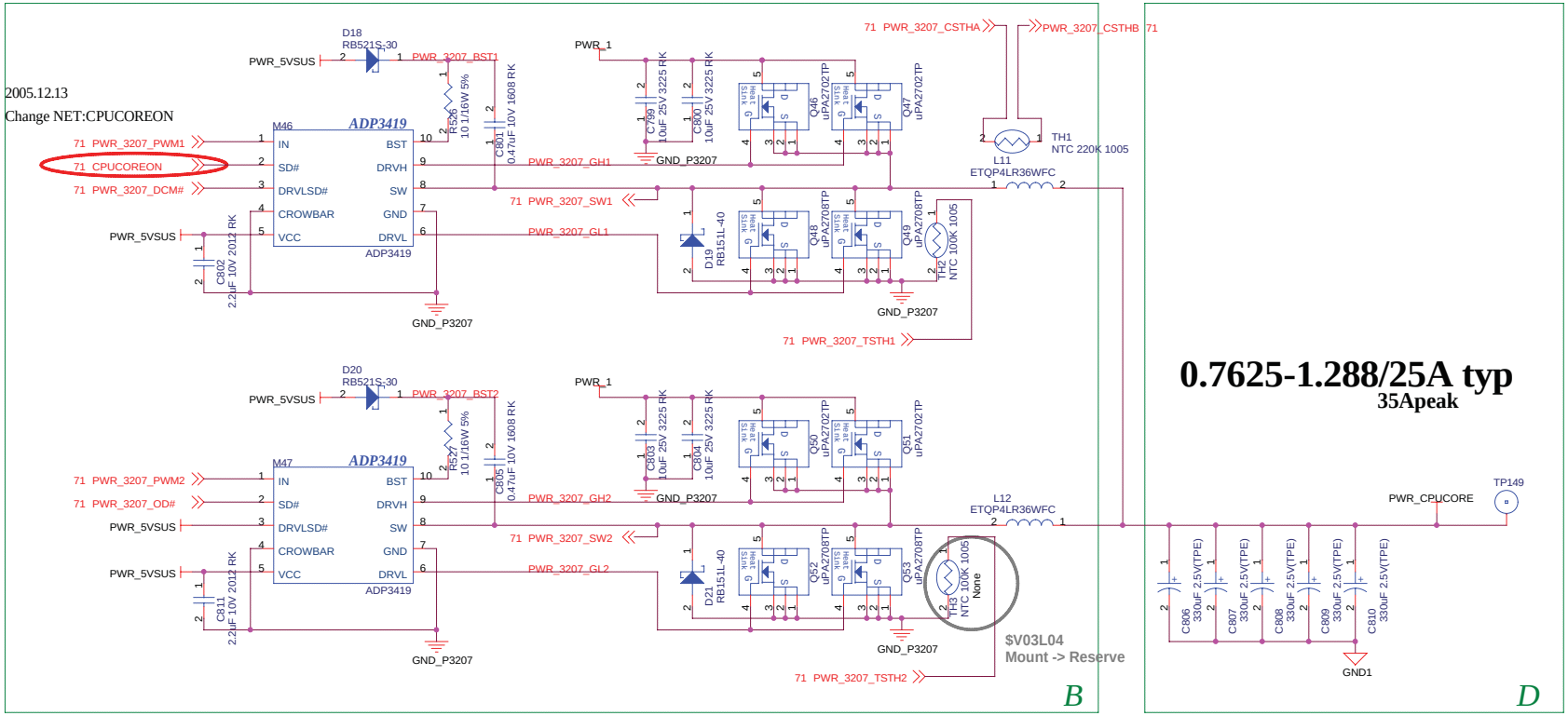


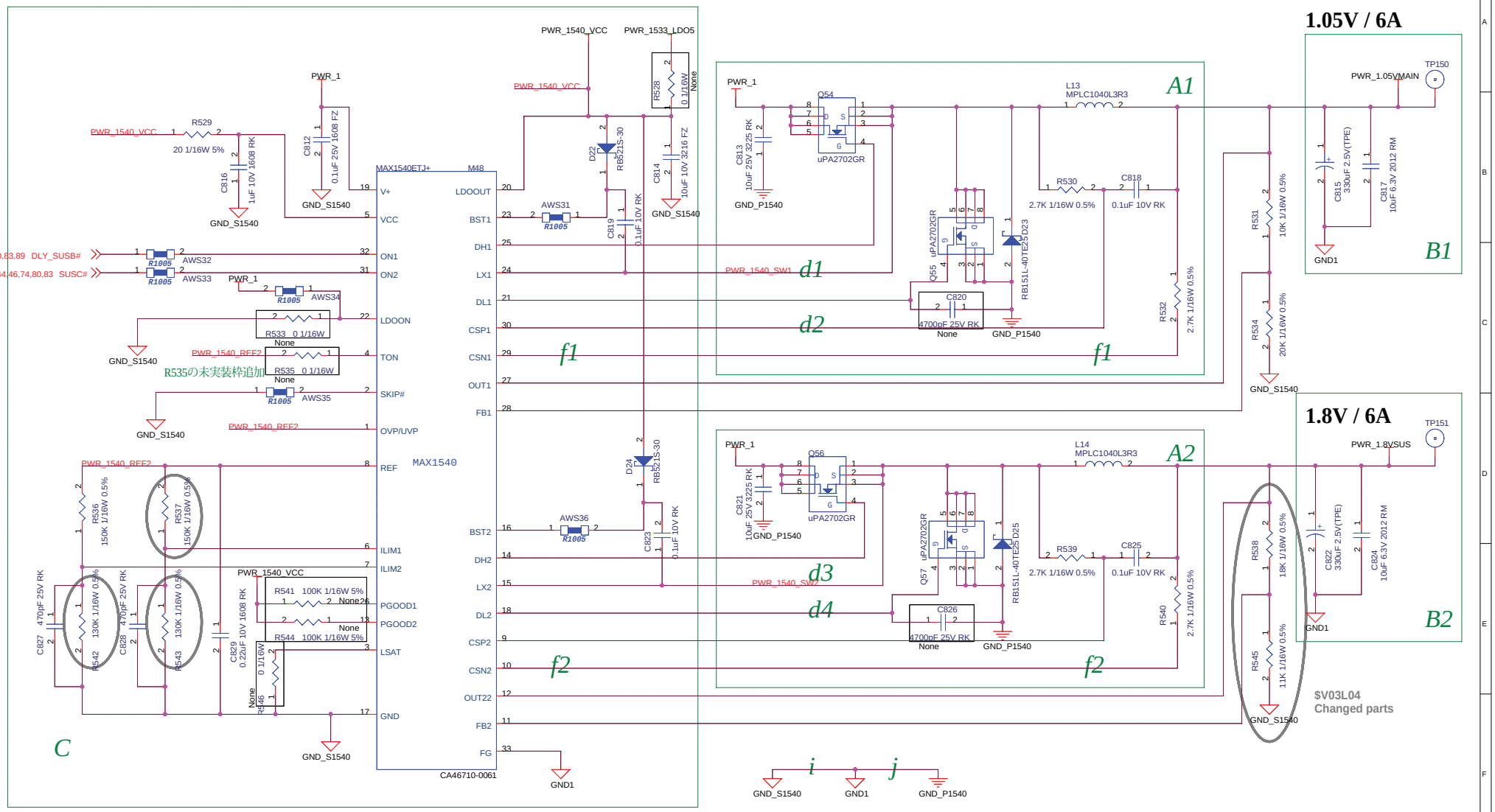
$V01L13
Changed parts

Power/ DDC/ CPUCore 1

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	2006.01.26	Seki	Yamada	Miura	

TITLE GILIA Main Board Rev.03
DRAW. NO. C1CP272450-X3 CUST.
FUJITSU LTD. SHEET 71 / 91





Power/ DDC/ 1.05VMain, 1.8VSus

REV.	DATE	DESIGN	CHECK	APPR.	DESCRIPTION		
DATE	2006.01.26	DESIGN	Seki	CHECK	Yamada	APPR.	Miura

TITLE: GILIA Main Board Rev.03
DRAW. NO.: C1CP272450-X3
CUST.
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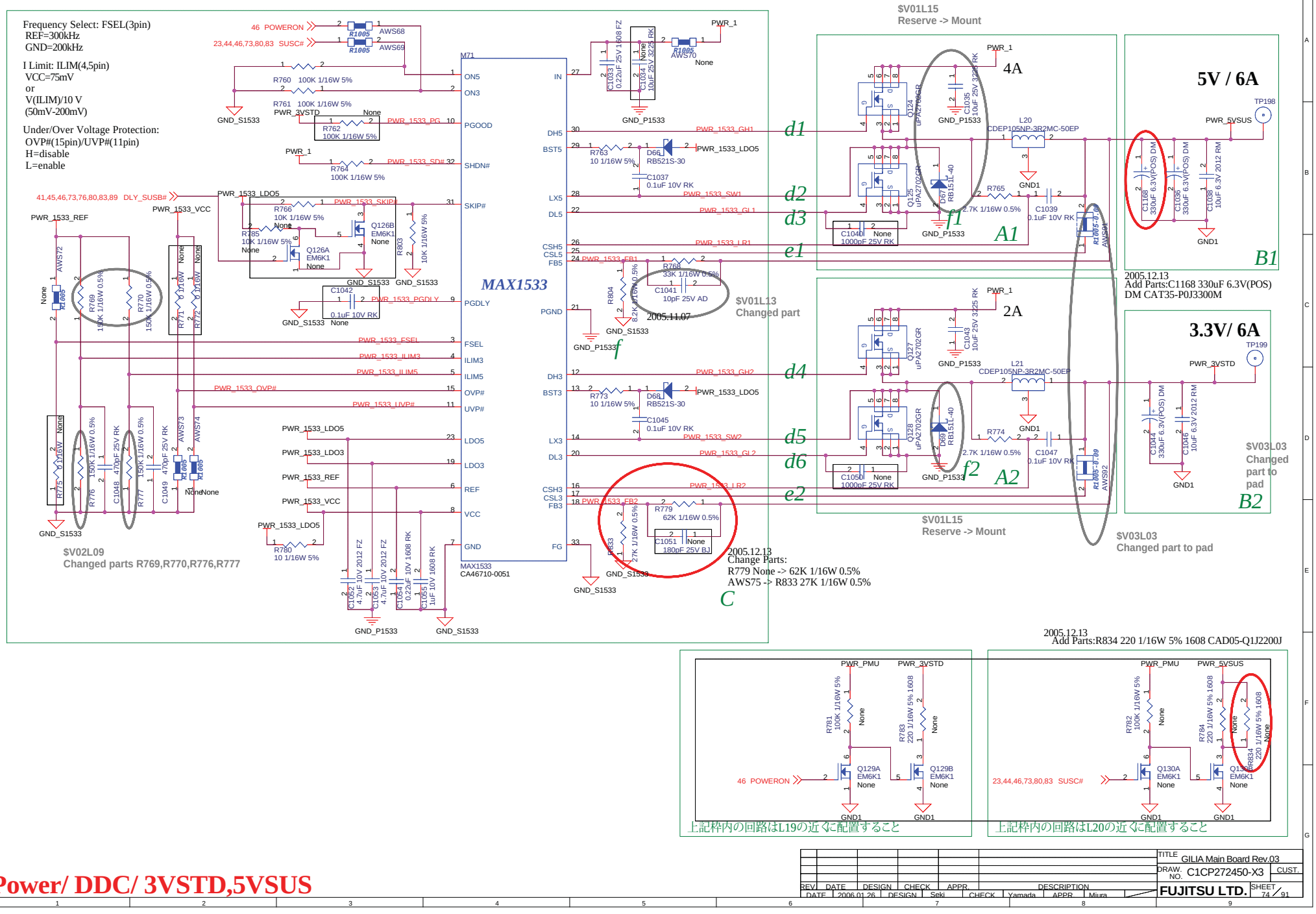
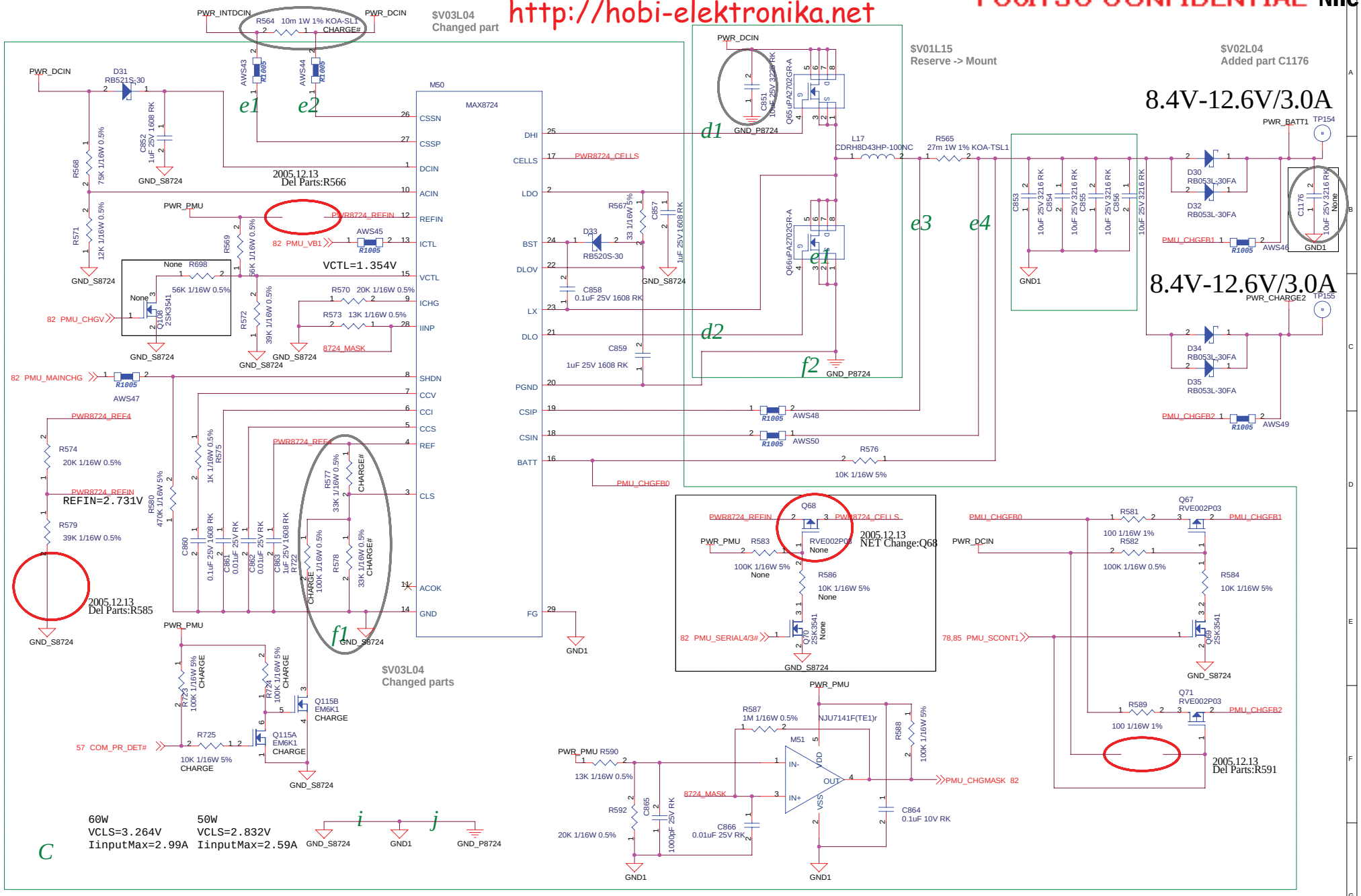
SHEET 73 / 91



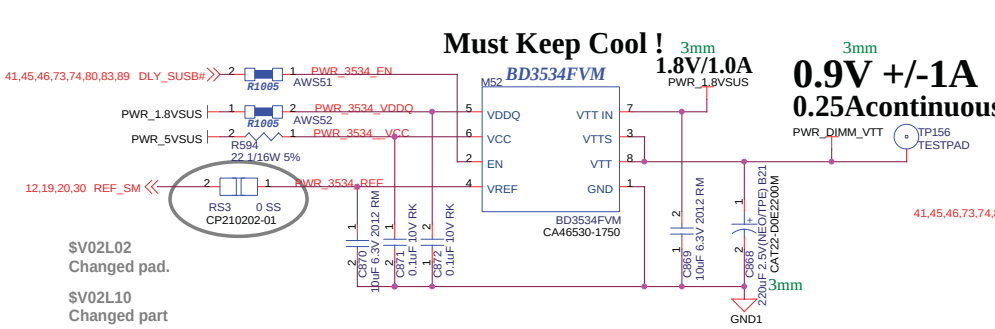
Power/ DDC/ 3VSTD,5VSUS

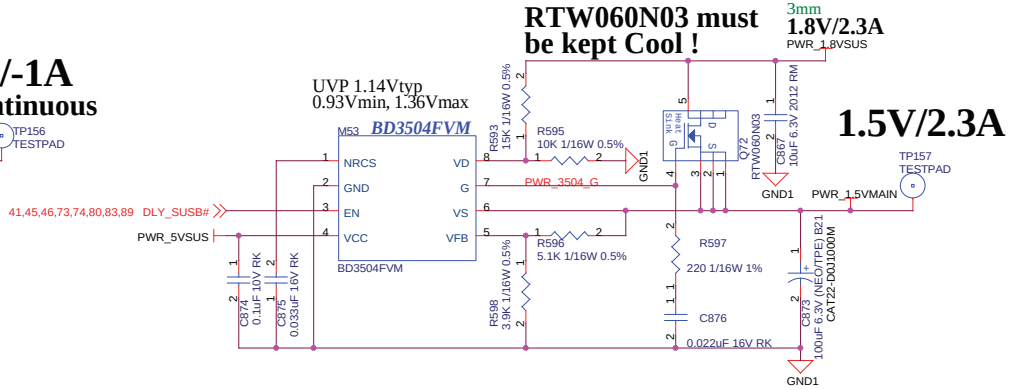
REV.	DATE	DESIGN	CHECK	APPR.	DESCRIPTION	TITLE	GILIA Main Board Rev.03
DATE	2006.01.26	DESIGN	Seki	CHECK	Yamada	DRAW. NO.	C1CP272450-X3
				APPR.	Miura	CUST.	
						FUJITSU LTD.	SHEET 74 / 91

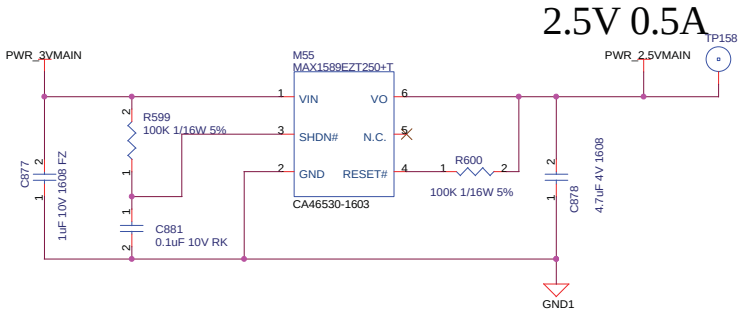


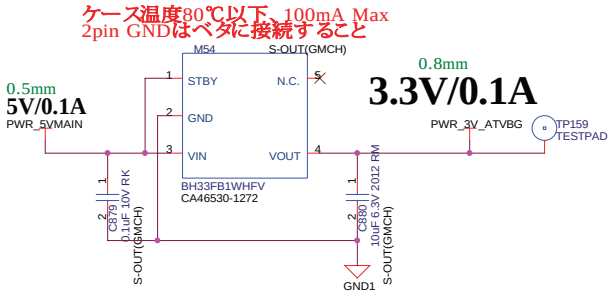
REV.	DATE	DESIGN	CHECK	APPR.	DESCRIPTION	
	DATE	2006.01.26	DESIGN	Seki	CHECK	Yamada	APPR.	Miura

TITLE GILIA Main Board Rev.03
DRAW. NO. C1CP272450-X3 CUST.
FUJITSU LTD. SHEET 75 / 91









＃TVDAC電源ショート=> P16

Power/ LDO/ SYS

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	2006.01.26	DESIGN	Seki	CHECK Yamada APPR. Miura

TITLE GILIA Main Board Rev.03
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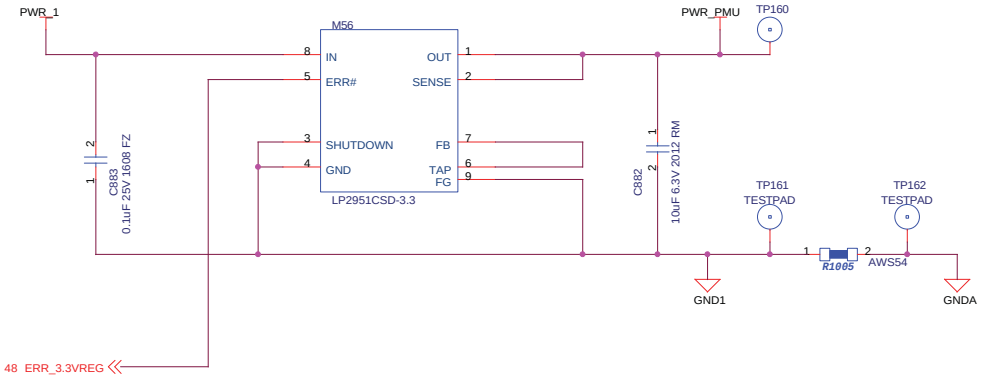
3.3V 50mA



Power/ LDO/ PMU

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
DATE	2006.01.26	DESIGN	Seki	CHECK	Yamada
				APPR.	Miura

TITLE: GILIA Main Board Rev.03
DRAW. NO.: C1CP272450-X3
CUST.:
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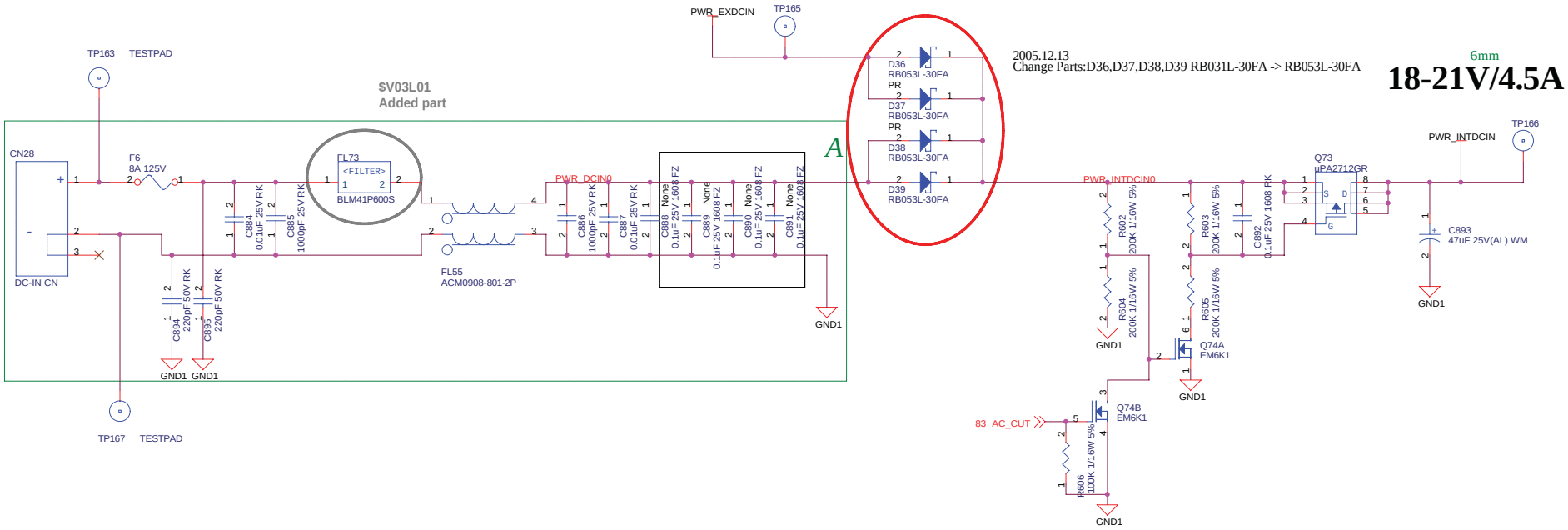

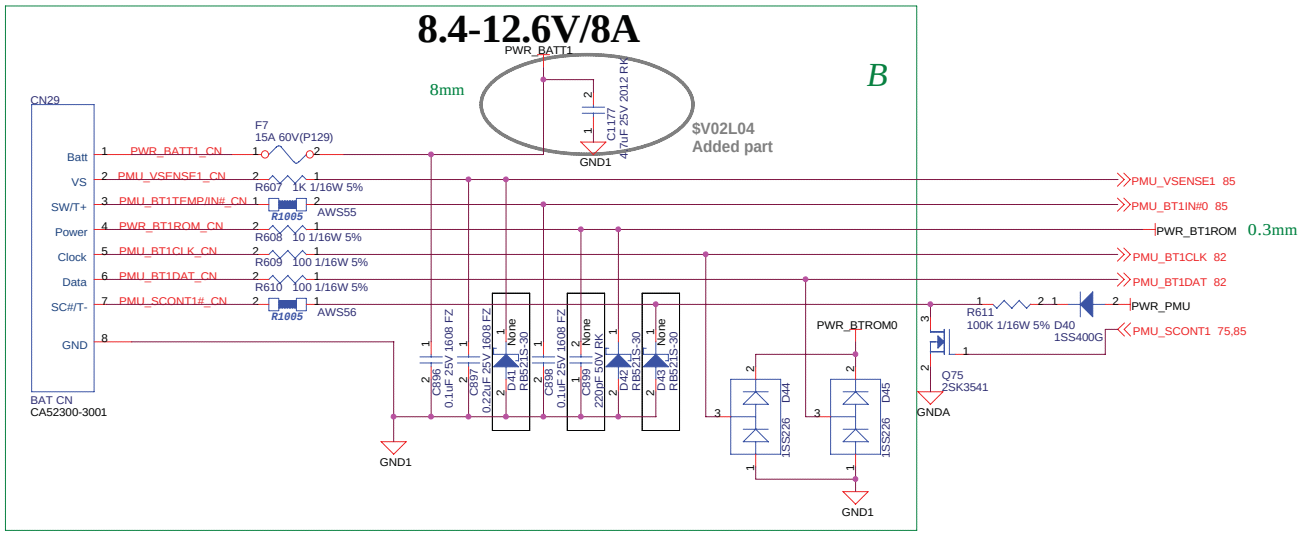

Power/ Node/ DCIn, Battery CN

REV.	DATE	DESIGN	CHECK	APPR.	DESCRIPTION		
	DATE	2006.01.26	DESIGN	Seki	CHECK	Yamada	APPR. Miura

TITLE GILIA Main Board Rev.03
DRAW. NO. C1CP272450-X3 CUST.
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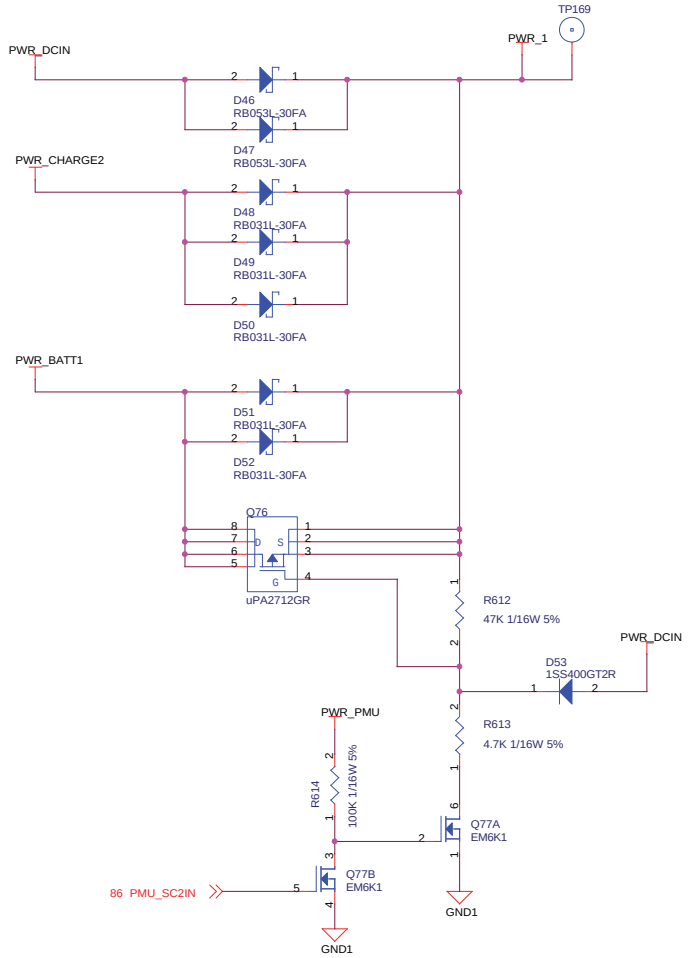

Power/ Node/ PWR_1

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	2006.01.26	Seki	Yamada	Miura	

TITLE GILIA Main Board Rev.03
DRAW. NO. C1CP272450-X3 CUST.
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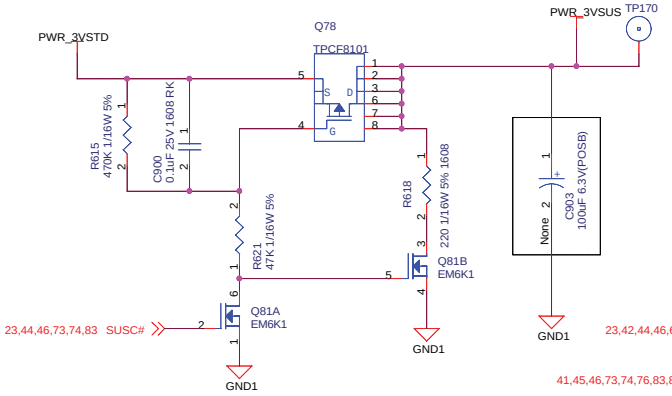
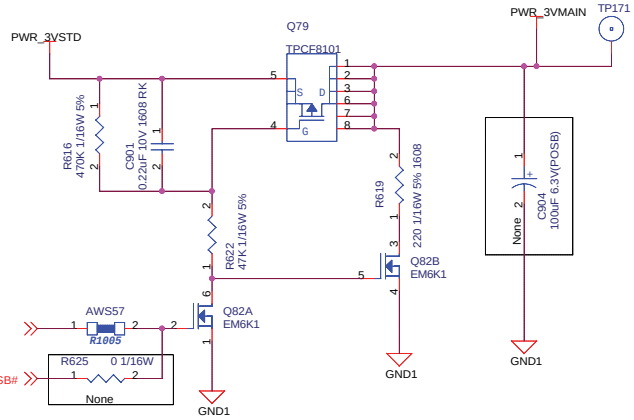
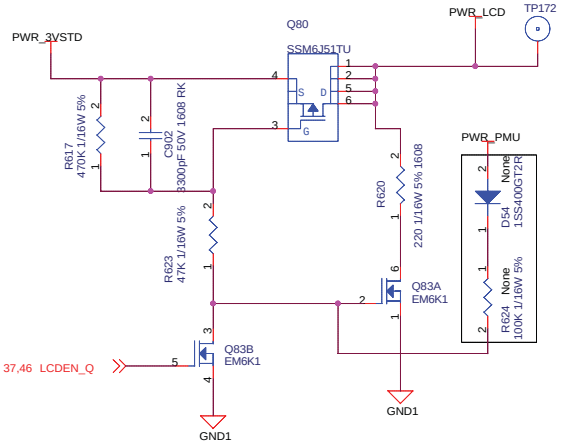
3.3V 2.0A



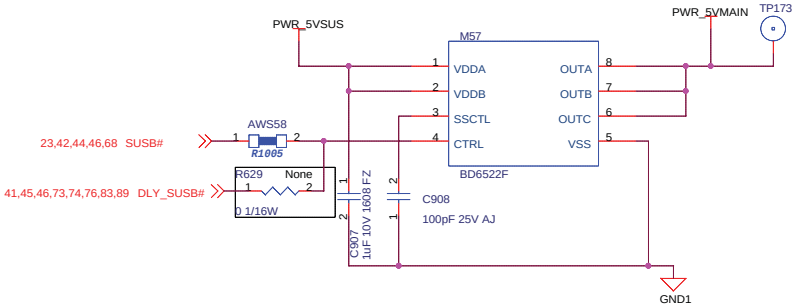
3.3V 2.0A



3.3V 1.0A



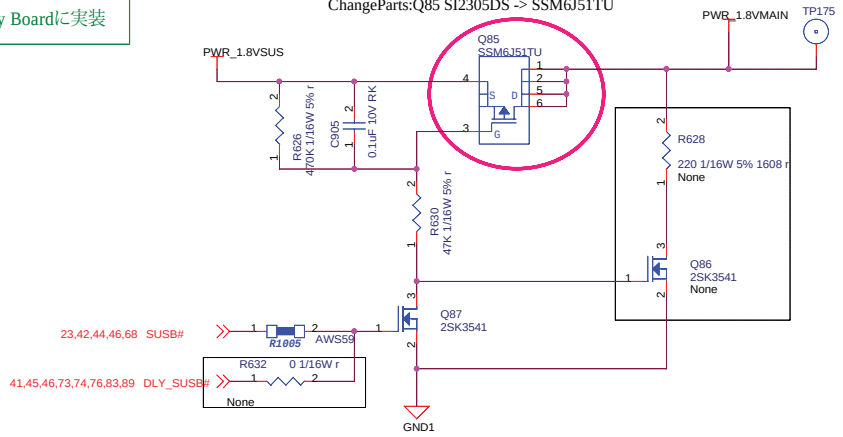
5.0V 2.0A

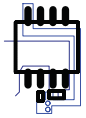


PWR_BAY SW => Bay Boardに実装

2005.10.14
ChangeParts:Q85 SI2305DS -> SSM6J51TU

1.8V 0.5A





※M57の5pinは、GNDベタには接続しないこと。
C907,C908との1点アースとする。
(左図参照)

Power/ Node/ Switch1

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	2006.01.26	Seki	Yamada	Miura	

TITLE: GILIA Main Board Rev.03
DRAW. NO.: C1CP272450-X3
CUST.:
FUJITSU LTD.
SHEET 80 / 91

Power/ Blank

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
DATE	2006.01.26	DESIGN	Seki	CHECK	Yamada
				APPR.	Miura

TITLE GILIA Main Board Rev.03

DRAW. NO. C1CP272450-X3 CUST.

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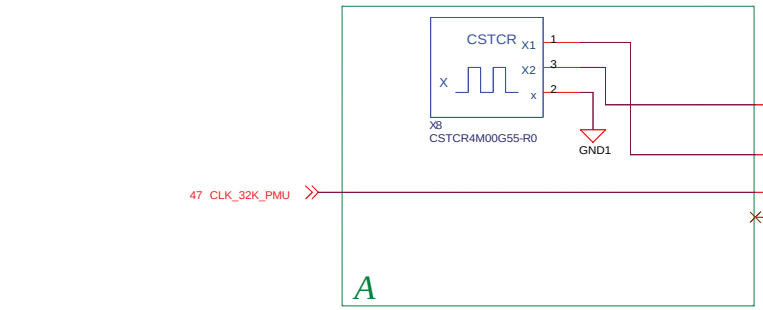
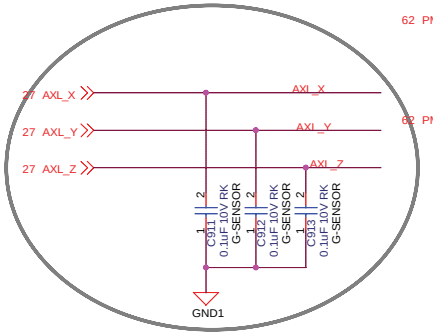
本クロックはノイズに弱いため
上下層に高速な信号が走らないように
配線すること





$V01L02
Deleted parts R636,R637,R638
Changed connection

＃G-SENSOR未実装時はGND1に接続。

2005.09.16
ChangeParts:R639 ->10K 1/16W 0.5%
R640 ->100K 1/16W 0.5%

$V03L04
Changed part R639

Power/ PMU/ LUNA1

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	2006.01.26	Seki	Yamada	Miura	

TITLE GILIA Main Board Rev.03
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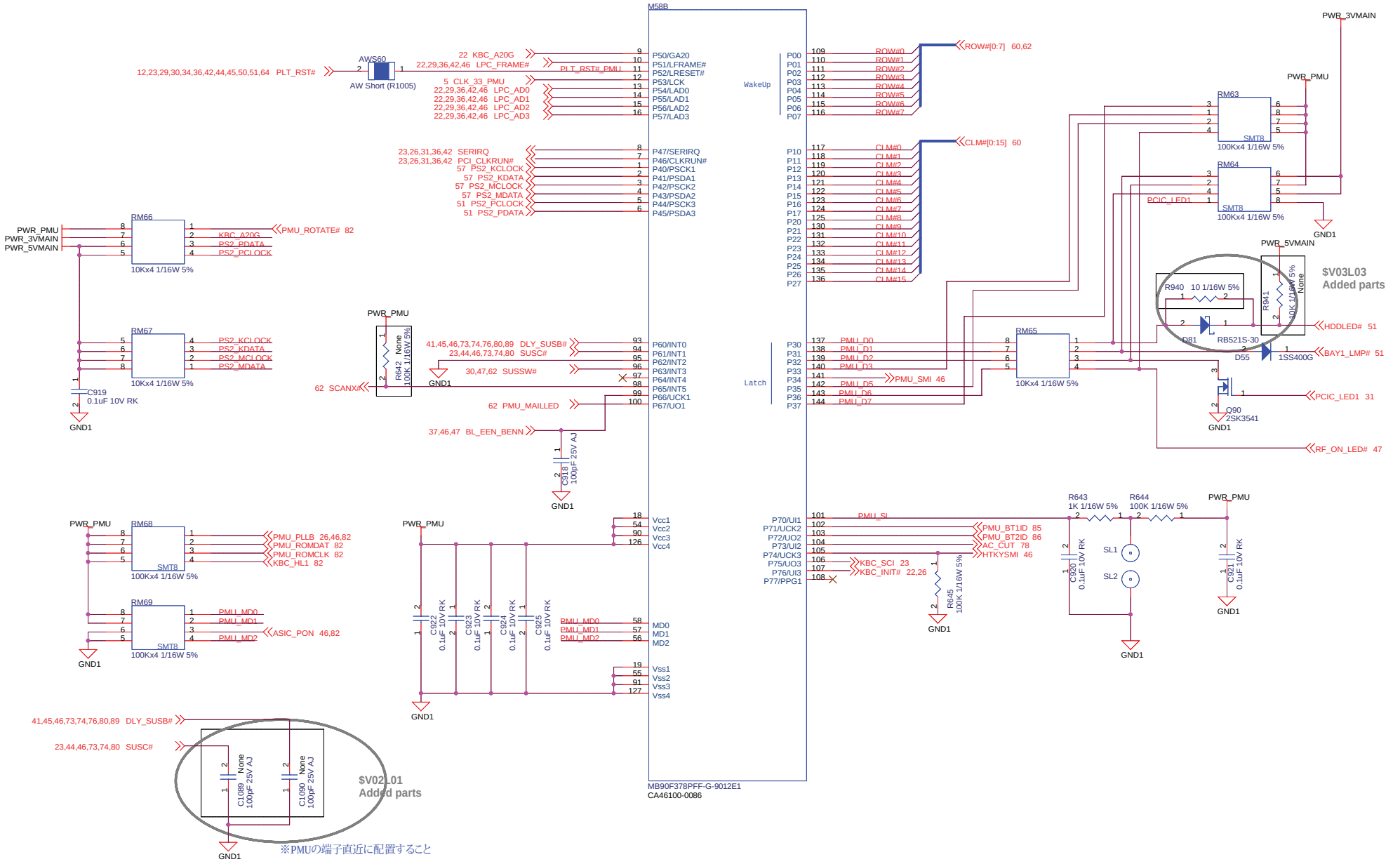

Power/PMU/LUNA2

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	2006.01.26	Seki	Yamada	Miura	

TITLE: GILIA Main Board Rev.03
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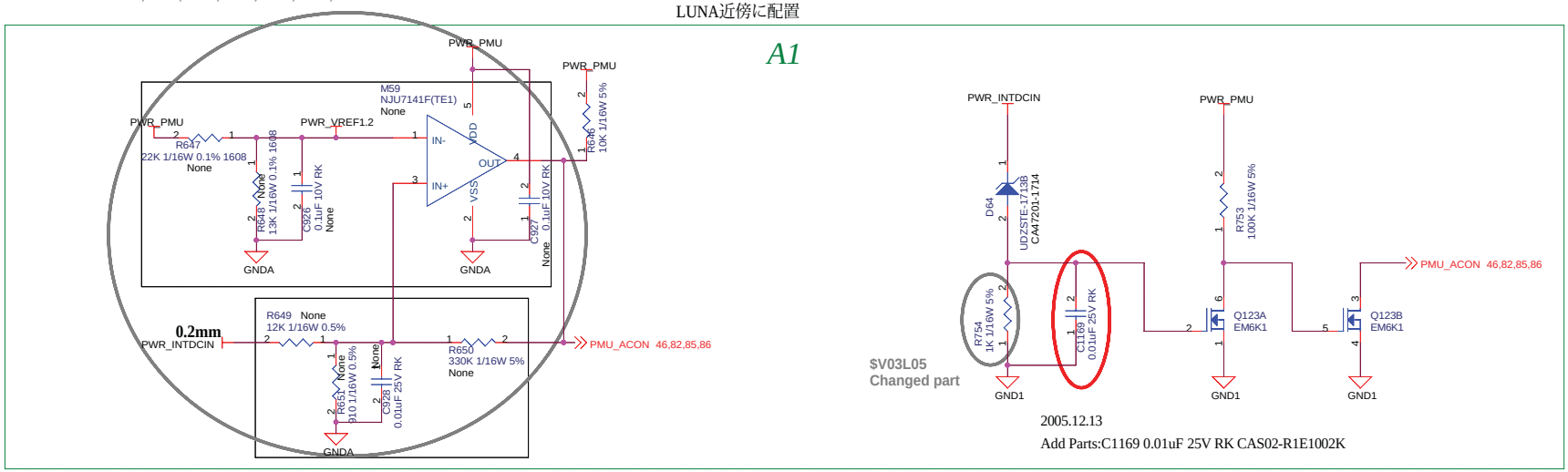
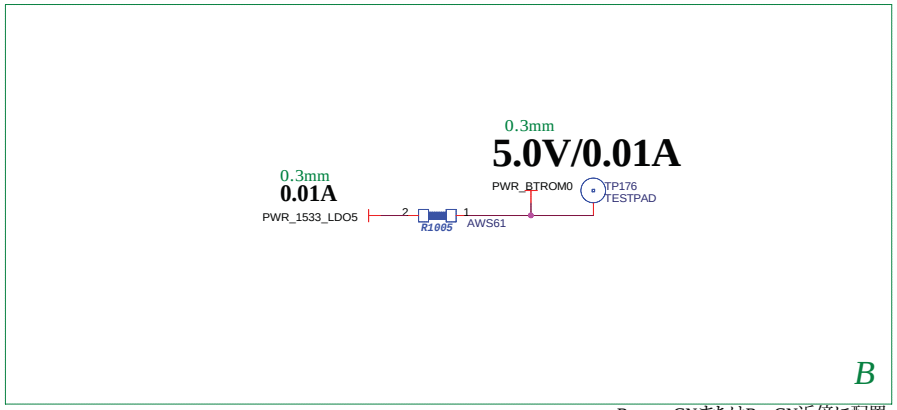
$V03L04
Mount -> Reserve R647,R648,R649,R651,C926,C927,C928

LUNA近傍に配置





BatteryCNまたはBayCN近傍に配置

Power/ PMU/ Etc0 (Common)

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE 2006.01.26	DESIGN Seki	CHECK Yamada	APPR. Miura	

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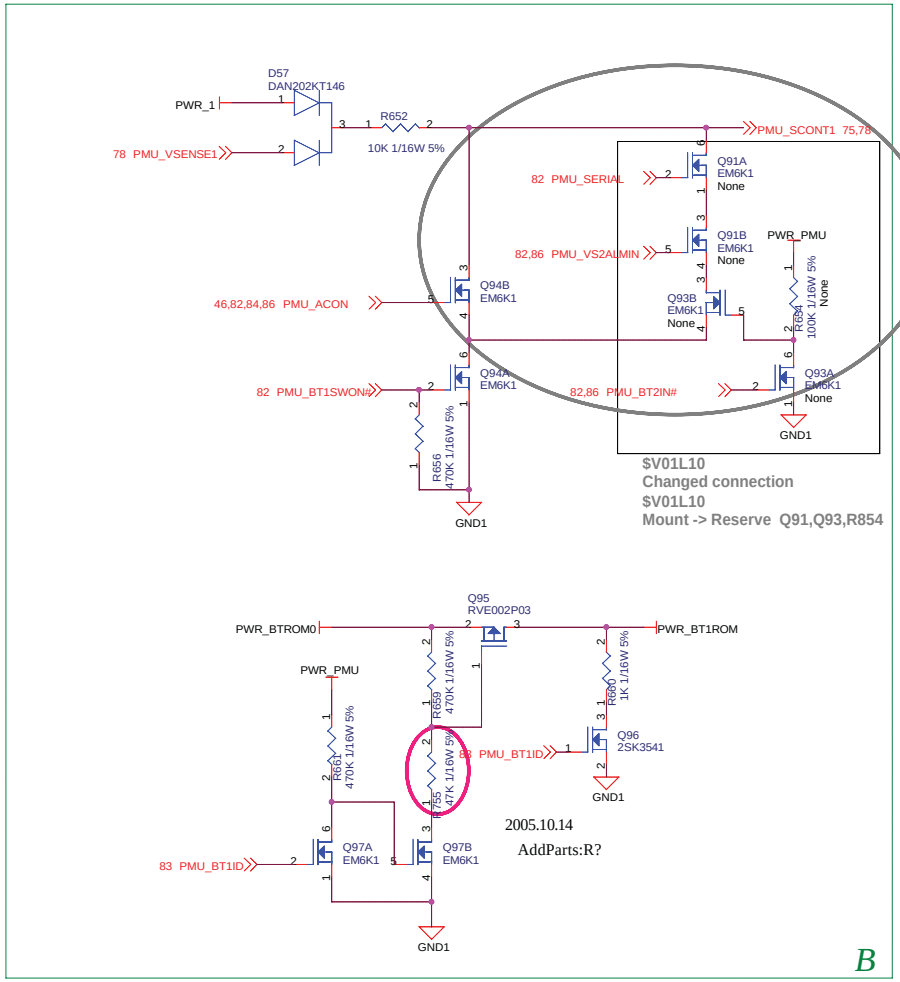
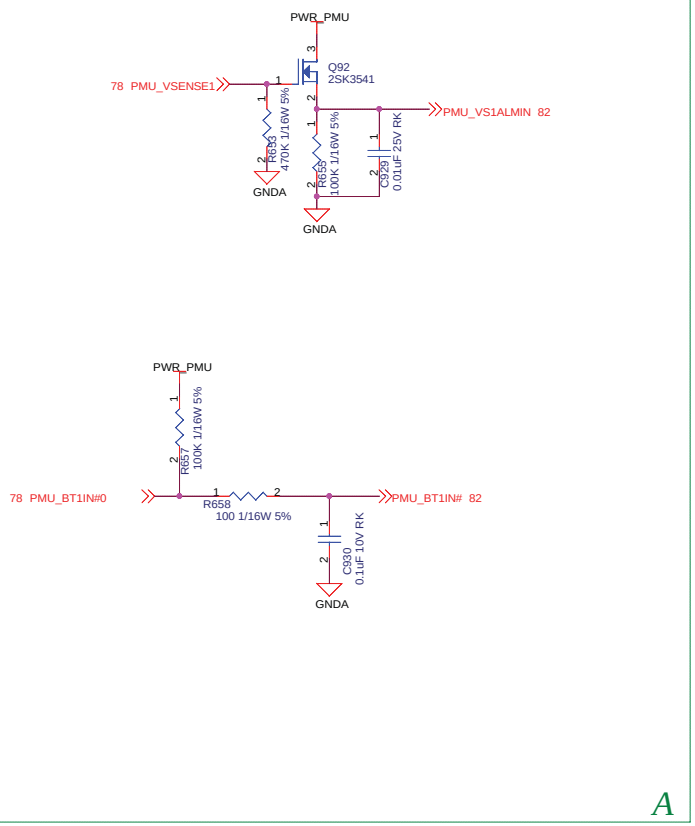


BatteryCNまたはBayCN近傍に配置



LUNA近傍に配置

Power/ PMU/ Etc1 (Battery1)

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	2006.01.26	Seki	Yamada	Miura	

TITLE: GILIA Main Board Rev.03
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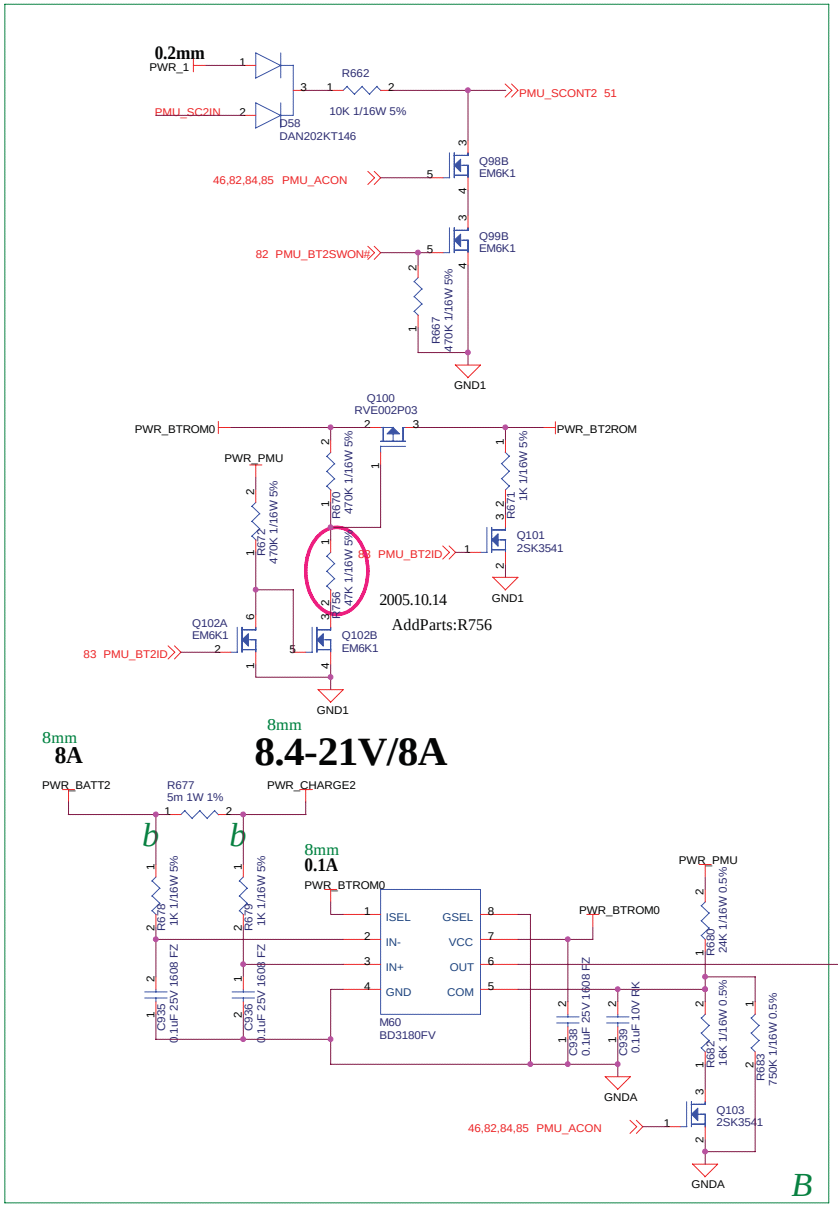
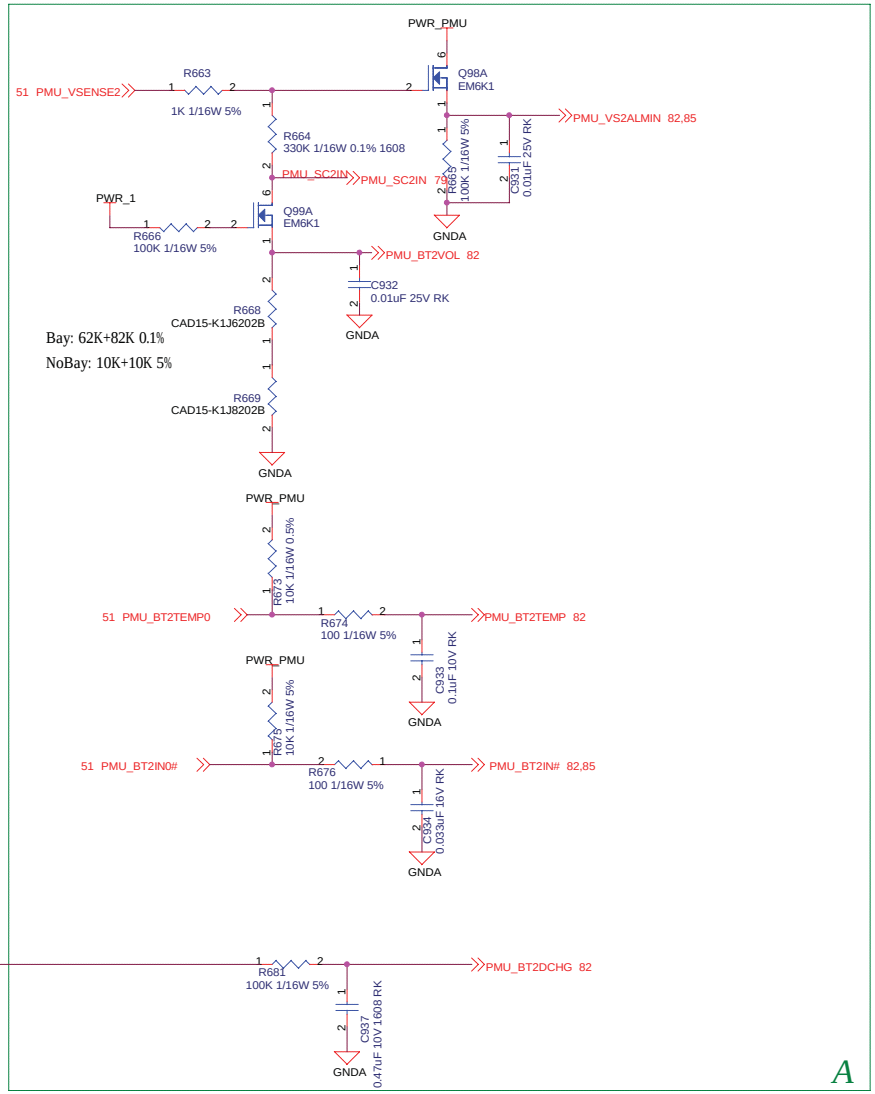


BatteryCNまたはBayCN近傍に配置



LUNA近傍に配置

Power/ PMU/ Etc2 (Battery2)

REV.	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	2006.01.26	DESIGN	Seki	CHECK Yamada APPR Miura

TITLE GILIA Main Board Rev.03
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Power/ Blank

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
DATE	2006.01.26	DESIGN	Seki	CHECK	Yamada
APPR.	Miura				

TITLE GILIA Main Board Rev.03

DRAW. NO. C1CP272450-X3 CUST.

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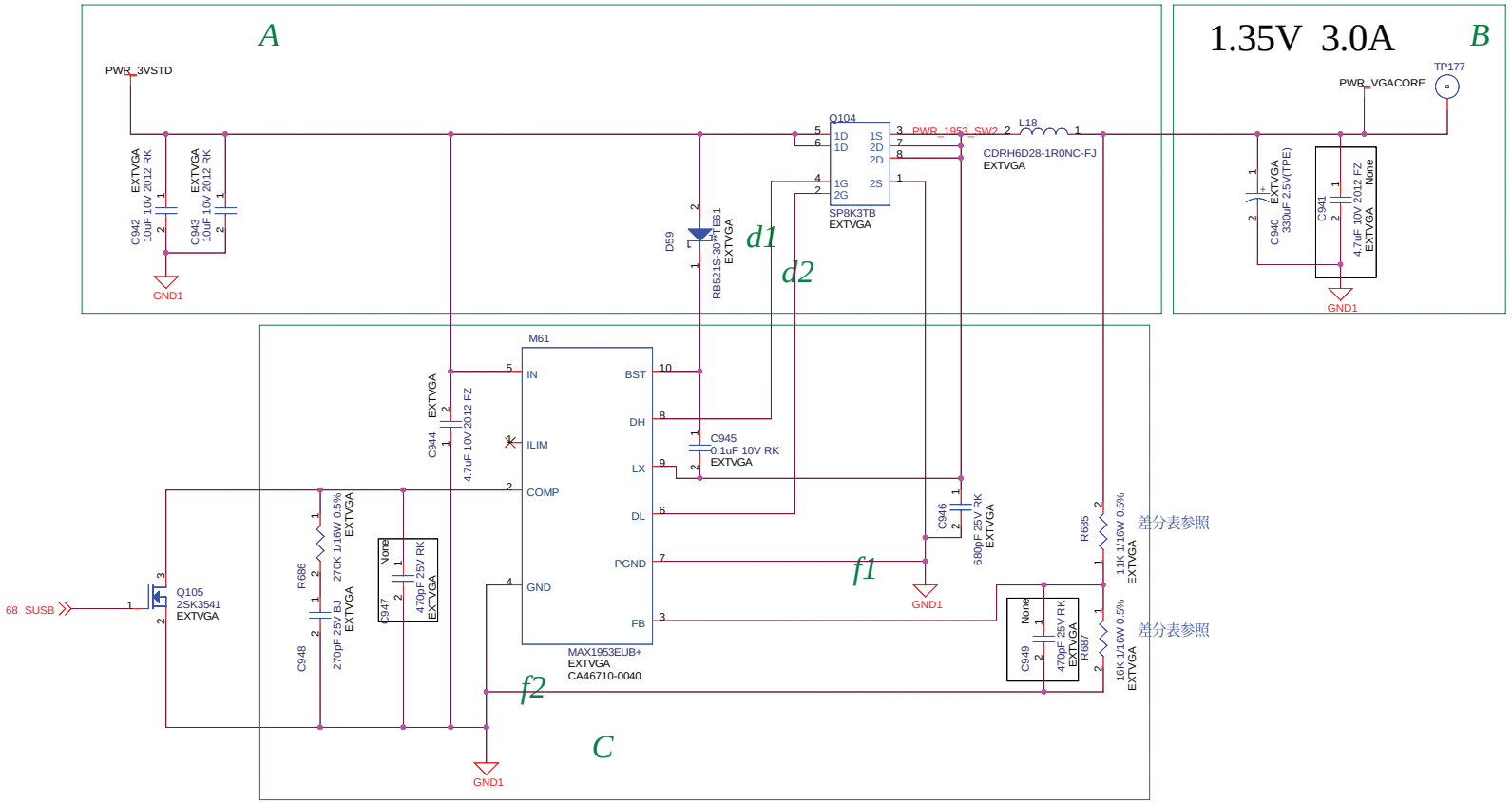

Power/ DDC/ VGACORE

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	2006.01.26	Seki	Yamada	Miura	

TITLE: GILIA Main Board Rev.03
DRAW. NO.: C1CP272450-X3
CUST.
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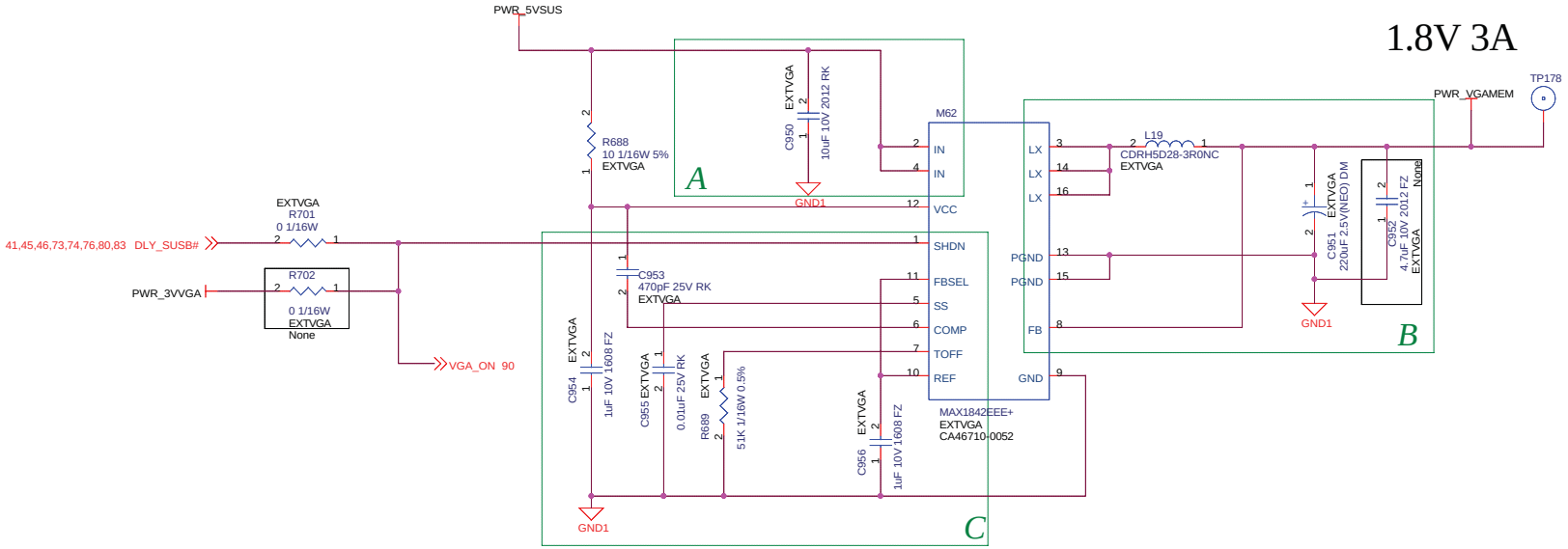

Power/ DDC/ VGAMEM

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	2006.01.26	Seki	Yamada	Miura	

TITLE: GILIA Main Board Rev.03
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$V01L07
Added parts, Changed connection

$V01L11
Changed connection

3.3V 0.30A

1.2V 0.30A

2005.10.14
AddParts:M?,R?,R?,C?,C?

PWR_PMU
PWR_3VSTD
PWR_VGA1.0V
R789 100K 1/16W 5% EXTVGA
R790 100K 1/16W 5% EXTVGA
R788 3.3K 1/16W 5% EXTVGA
Q131 2SC5658 EXTVGA
Q132 2SK3541 EXTVGA
C1057 1uF 10V 1608 RK EXTVGA
GND1

M70
MAX1806EUA08+ EXTVGA
IN, OUT, POK, SHDN#, SET, HeatSink, GND
C1030 0.1uF 10V RK EXTVGA
R757 10K 1/16W 0.5% EXTVGA
R758 20K 1/16W 0.5% EXTVGA
C1031 10uF 6.3V 2012 RM EXTVGA
PWR_VGA1.4V
TP180

1.0V 0.8A

PWR_PMU
PWR_VGAMEM
PWR_5VSUS
89 VGA_ON
R690 100K 1/16W 5% EXTVGA
R691 100K 1/16W 5% EXTVGA
R694 10K 1/16W 5% EXTVGA
R695 100K 1/16W 5% EXTVGA
Q106A EM6K1 EXTVGA
Q106B EM6K1 EXTVGA
Q107 2SC4617TL EXTVGA
C962 1uF 10V 1608 FZ EXTVGA
GND1

M63 BD3506F EXTVGA
VIN, VCC, EN, NRCS, VO1, VO2, VFB, GND
C959 10uF 6.3V 2012 RM EXTVGA
C960 10uF 10V 3216 FZ EXTVGA
C961 0.01uF 25V RK EXTVGA
C957 1000pF 25V RK EXTVGA
VFB=0.650
Vset=1.04V
R692 1.2K 1/16W 0.5% EXTVGA
R693 2.0K 1/16W 0.5% EXTVGA
C958 330uF 2.5V(TPE) EXTVGA
PWR_VGA1.0V
TP179
GND1

f1
f1

2005.10.14
DeleteParts:M64,R696,R697,C963,C964,C965,C966,C967

Power/ LDO/ VGA

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
	DATE	2006.01.26	DESIGN	Seki	CHECK Yamada APPR Miura

TITLE GILIA Main Board Rev.03
DRAW. NO. C1CP272450-X3 CUST.
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Power/ Blank

REV	DATE	DESIGN	CHECK	APPR.	DESCRIPTION
DATE	2006.01.26	DESIGN	Seki	CHECK	Yamada
APPR	Miura				

TITLE GILIA Main Board Rev.03

DRAW. NO. C1CP272450-X3 CUST.

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