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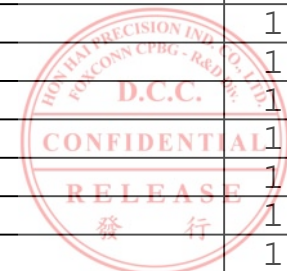
Project Code & Schematics Subject: MS20 MP Main Board

PCB P/N: 1P-0064100-8011 (FUBAI)
1P-1064506-8011 (HANSTAR)

P. Leader	Check by	Design by
紀博文	楊卓川	楊卓川
FOXCONN		
HON HAI Precision Ind. Co., Ltd. CPBG - R&D Division		
Index Page		
Rev. A1	Document Number: MS20-1-01 MainBoard (MS1-10)	Rev. C10
Date: 2006/04/10		

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29	TVIN and OUT/Semi-PnP#	1.00	2006/04/10	69	DDR2 Power(+1_8V/+0_9V)	1.00	2006/04/10
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FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

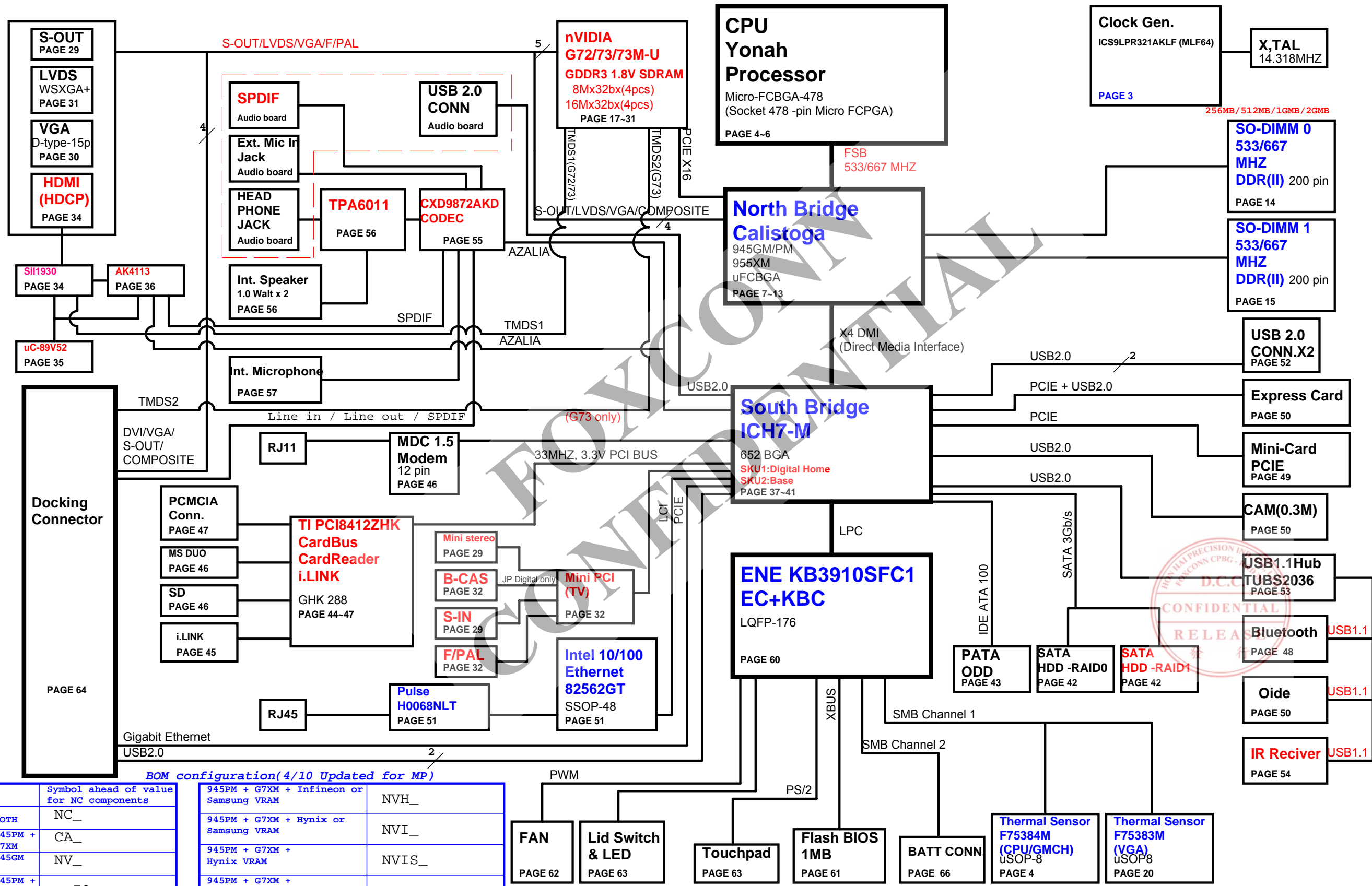
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MS20(CALISTOGA PM/GM+Gfx Block Diagram)

Red texts:
New modified



BOM configuration(4/10 Updated for MP)

Symbol ahead of value for NC components		
BOTH	NC_	NVH_
945PM + G7XM	CA_	NVI_
945GM	NV_	NVIS_
945PM + G72M	NV73_	NVHS_
945PM + G73M	NV72_	NV16M_, NV73U_
945PM + G72M or G73M-U	NV73Only_	NV8M_, NV7273_
		*JP Digital TV Tuner SKU & No Tuner SKU not stick
		JDTVNC_

NC_10P_50V_E_N	2	1	CLK_CB48	
NC_10P_50V_E_N	2	1	CLK_USB48	
NC_10P_50V_E_N	2	1	CLK_KBCPCI	
NC_10P_50V_E_N	2	1	PCLK_CB	
NC_10P_50V_E_N	2	1	PCLK_MINI	
NC_10P_50V_E_N	2	1	CLK_ICHPCI	
NC_10P_50V_E_N	2	1	CLK_ICH14	
NC_10P_50V_E_N	2	1	PCLK_JIG	
NC_10P_50V_E_N	2	1	C92	0402

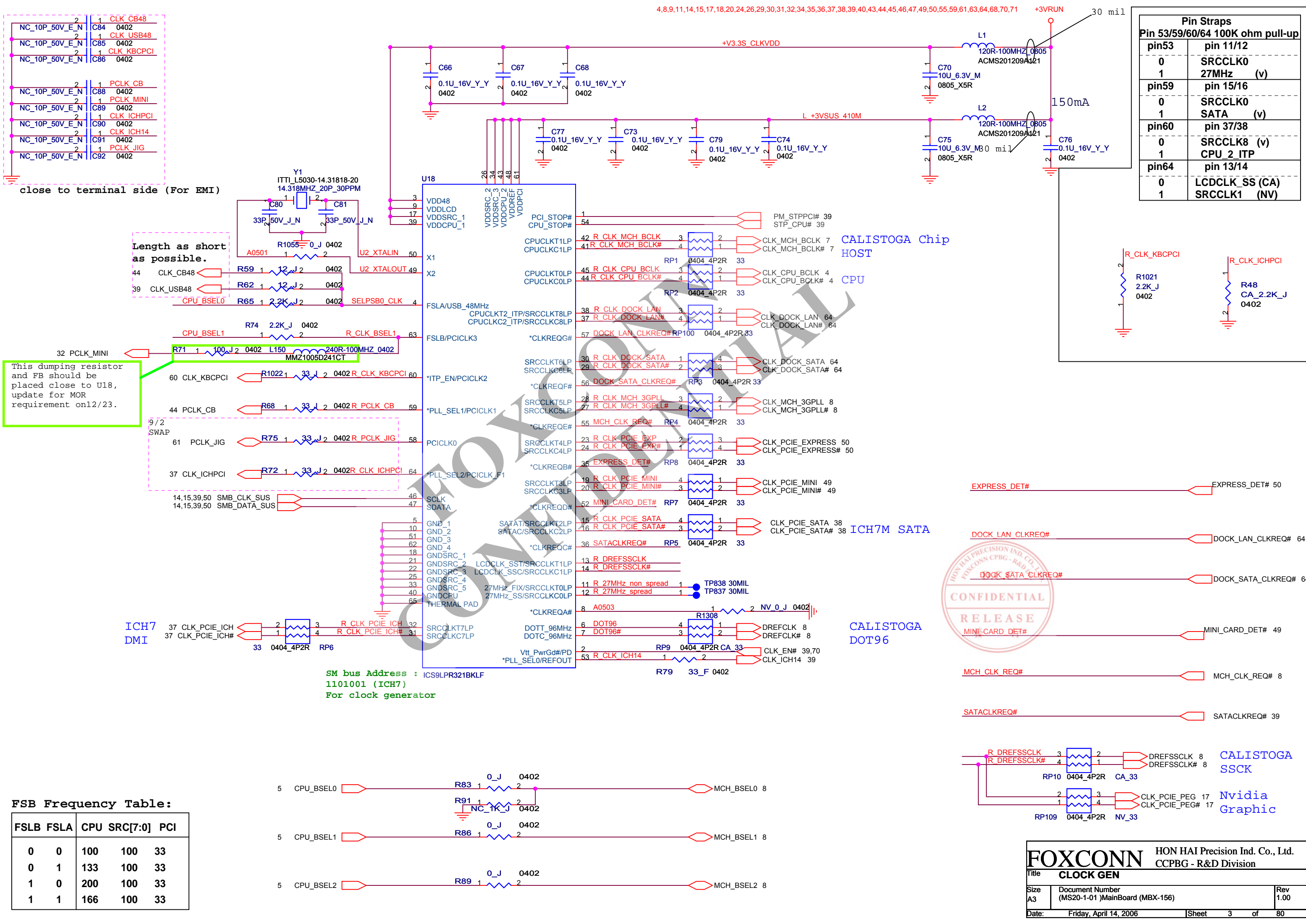
close to terminal side (For EMI)

Length as short as possible.

This dumping resistor and FB should be placed close to U18, update for MOR requirement on12/23.

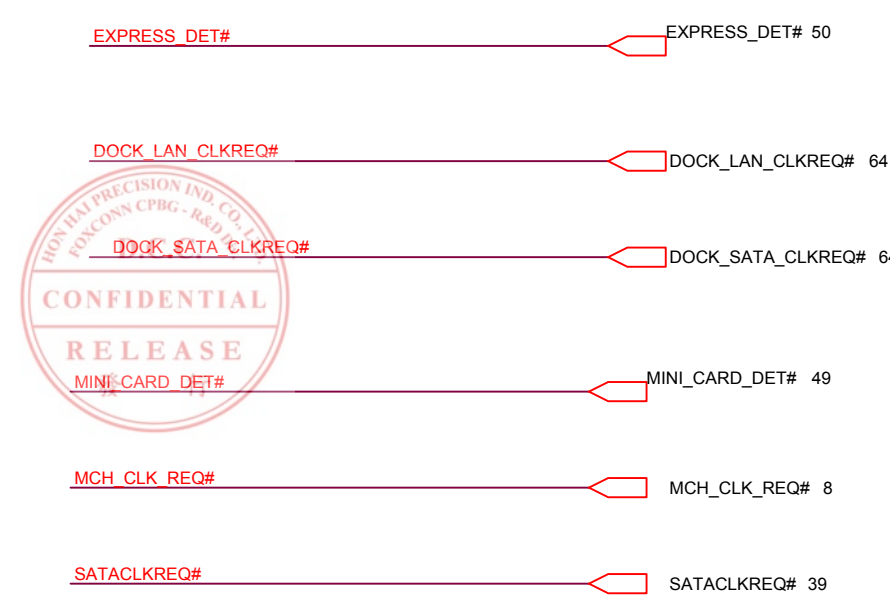
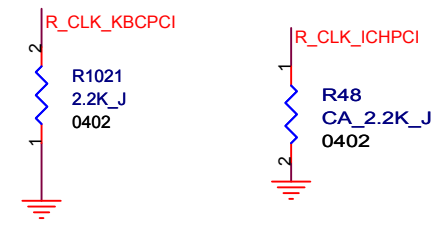
FSB Frequency Table:

FSLB	FSLA	CPU SRC[7:0]	PCI
0	0	100	100 33
0	1	133	100 33
1	0	200	100 33
1	1	166	100 33

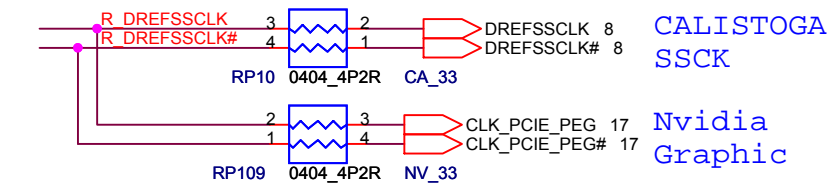
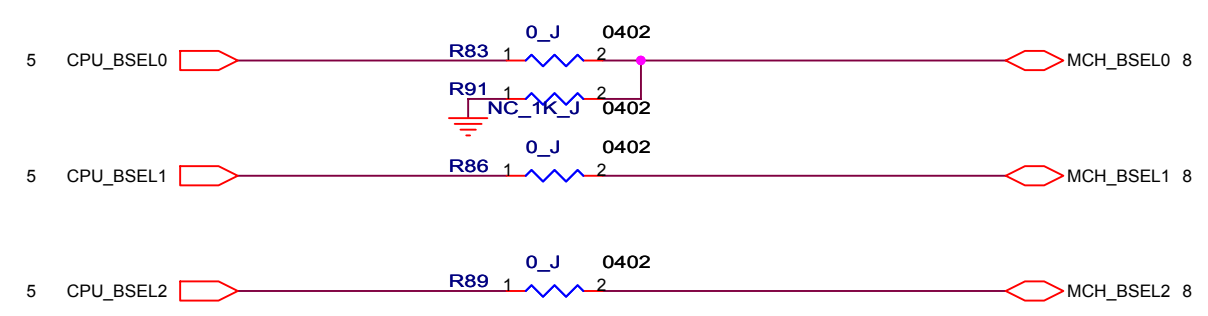


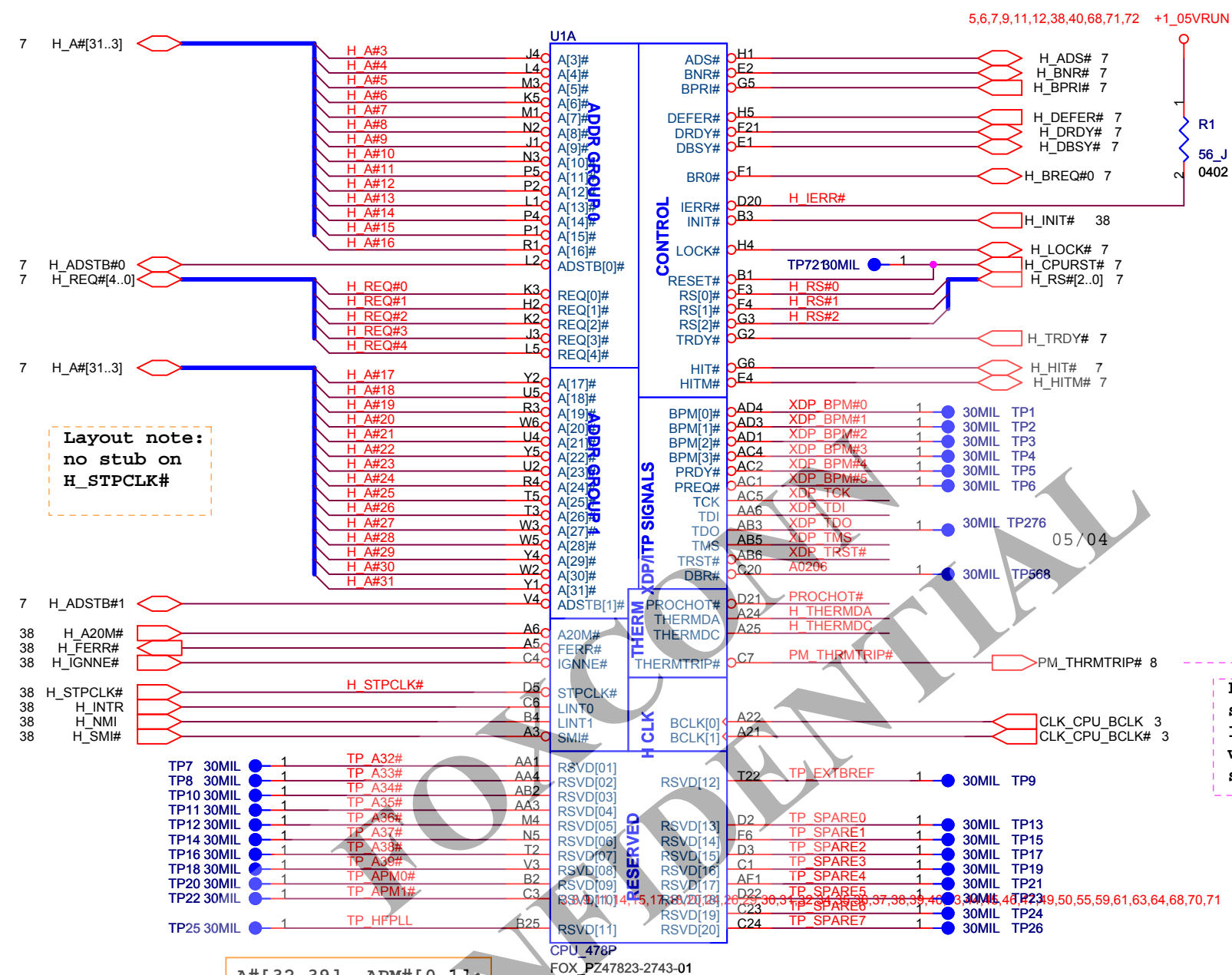
Pin Straps
Pin 53/59/60/64 100K ohm pull-up

pin53	pin 11/12
0	SRCCLK0
1	27MHz (v)
pin59	pin 15/16
0	SRCCLK0
1	SATA (v)
pin60	pin 37/38
0	SRCCLK8 (v)
1	CPU_2_ITP
pin64	pin 13/14
0	LCDCLK_SS (CA)
1	SRCCLK1 (NV)



SM bus Address : ICS9LPR321BKLF
1101001 (ICH7)
For clock generator

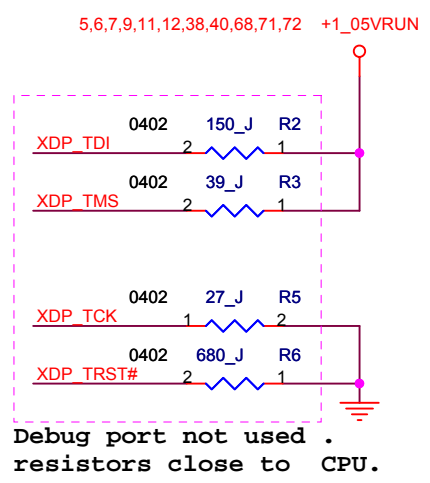




Layout note:
no stub on
H_STPCLK#

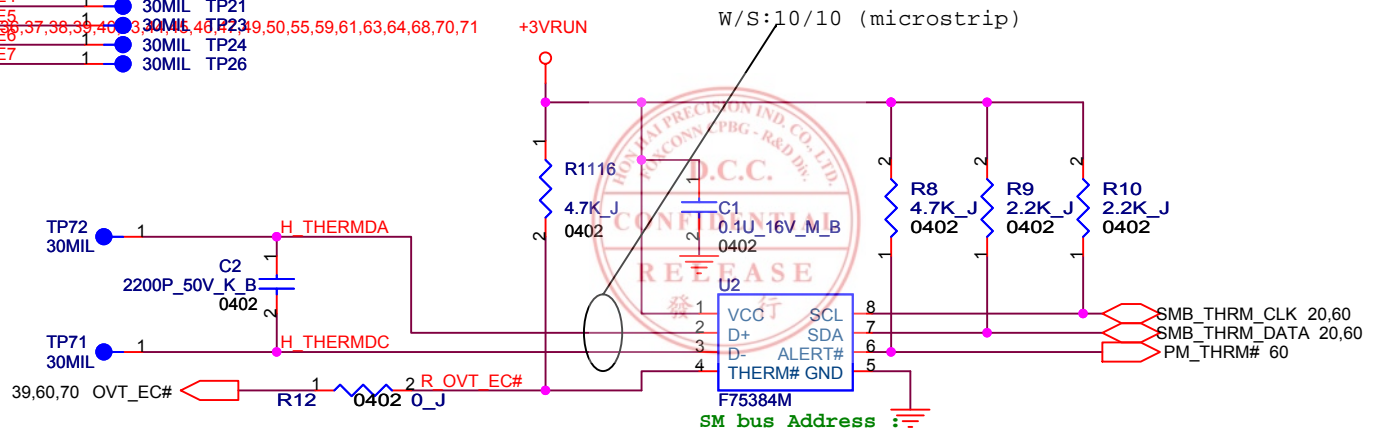
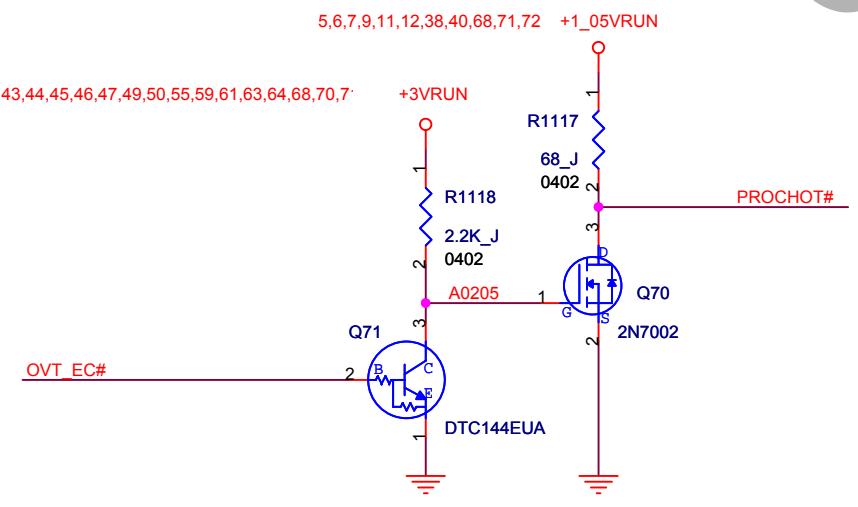
A#[32-39], APM#[0-1]:
Leave escape routing
on for future
functionality

ICH7M's GPIO12: VIL----> -0.5V ~ 0.8V
VIH----> 2.0V ~ 3.3+0.5V
YONAH's PROCHOT#: VIL----> -0.1V ~ 0.3*VCCP
VIH----> 0.7*VCCP ~ VCCP+0.1

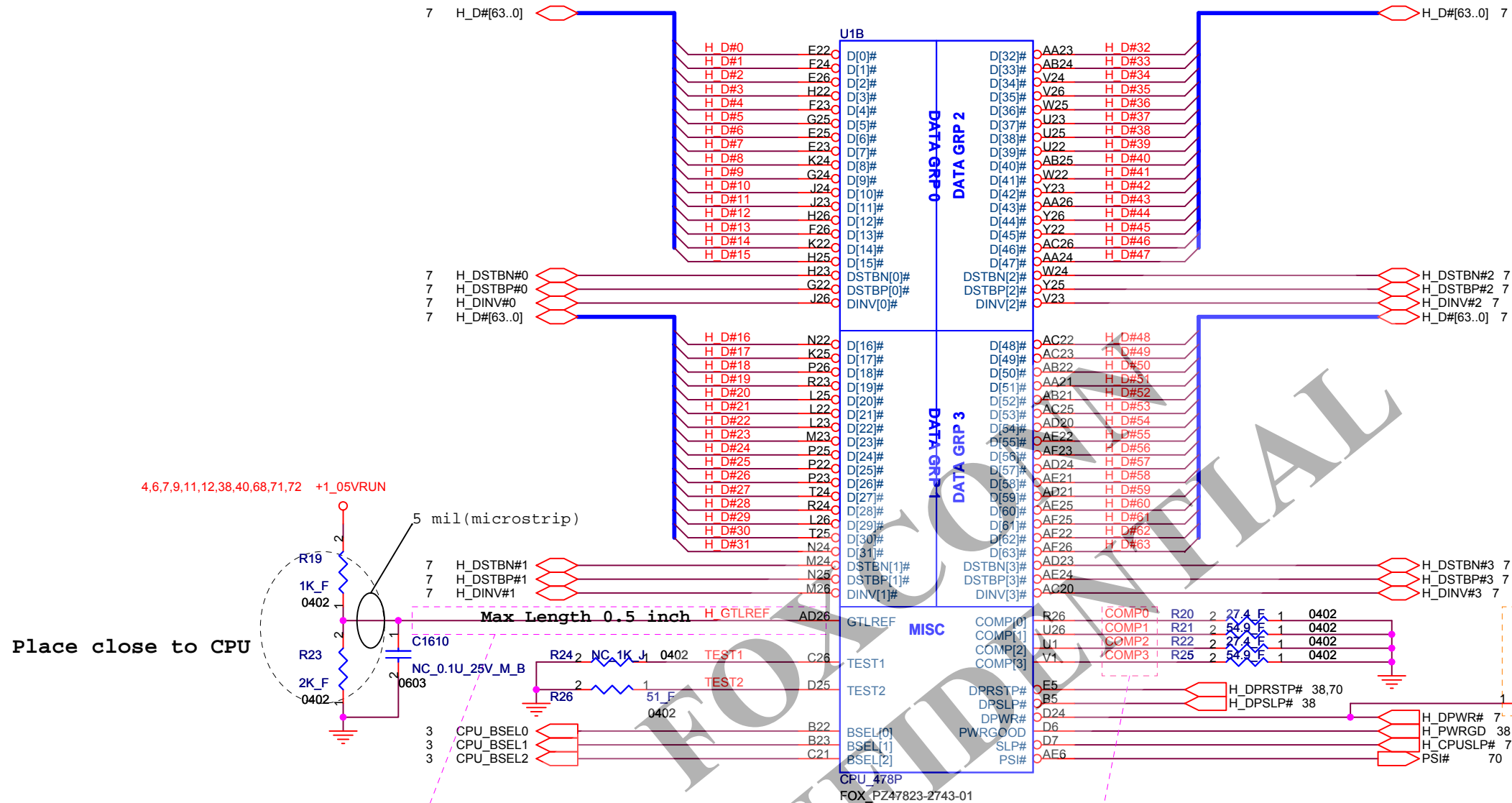


Debug port not used .
resistors close to CPU.

PM_THRMTRIP#
should connect to
ICH7-M and GMCH
without T-ing (No
stub)



Place Thermal-Sensor near
CPU & GMCH.



4,6,7,9,11,12,38,40,68,71,72 +1_05VRUN

5 mil (microstrip)

Max Length 0.5 inch H_GTLREF

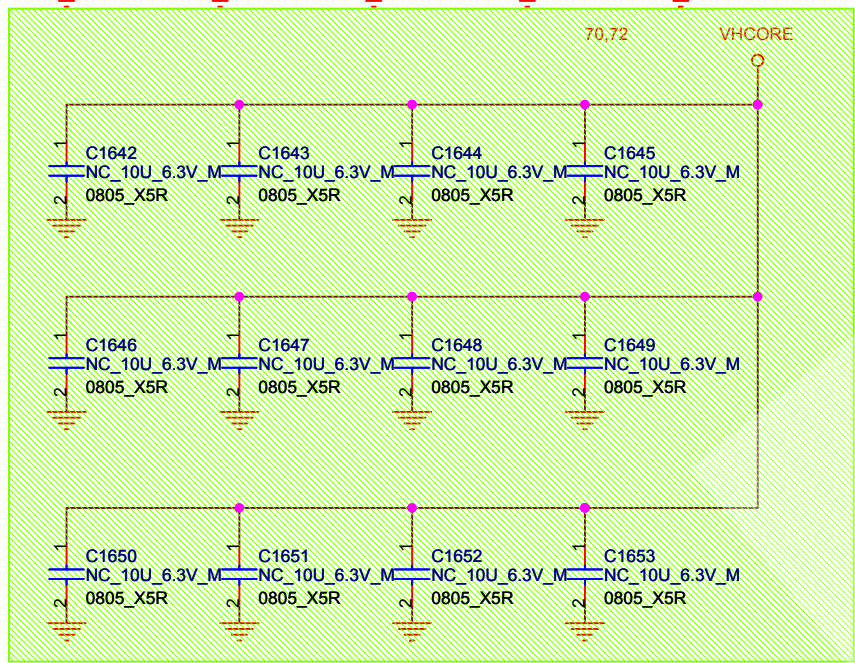
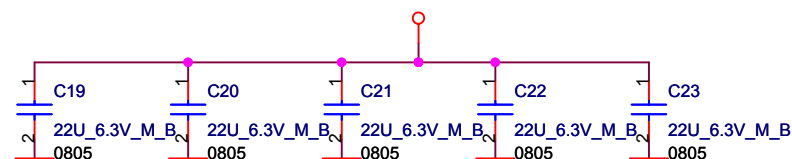
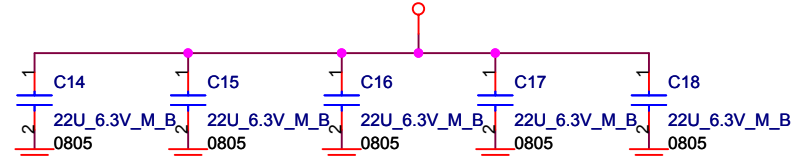
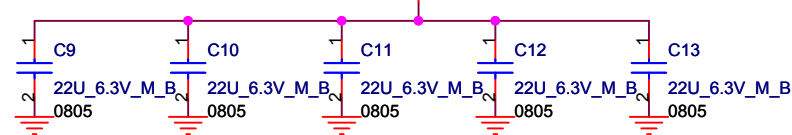
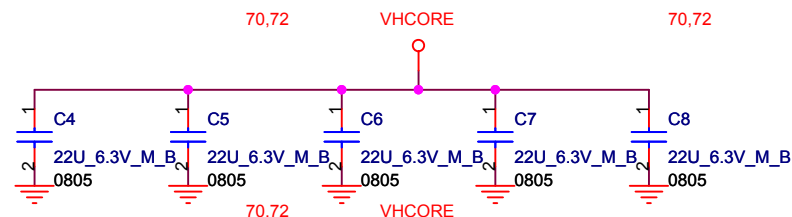
Place close to CPU

Layout Note:
Zo=55 ohm, 0.5" max for GTLREF

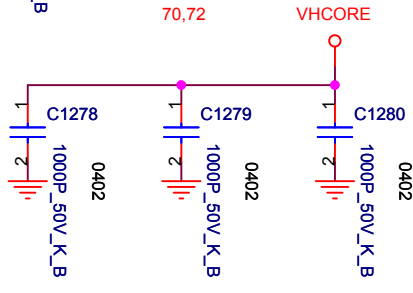
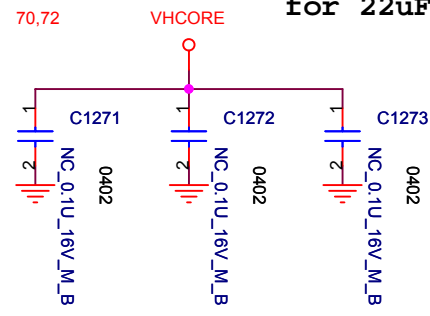
Layout Note:
Comp0,2 connect with Zo=27.4 ohm, make trace length shorter than 0.5".
Comp1,3 connect with Zo=55 ohm, make trace length shorter than 0.5".

Layout:
Connect test point with no stub



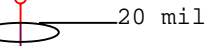
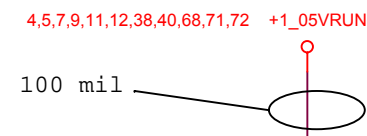
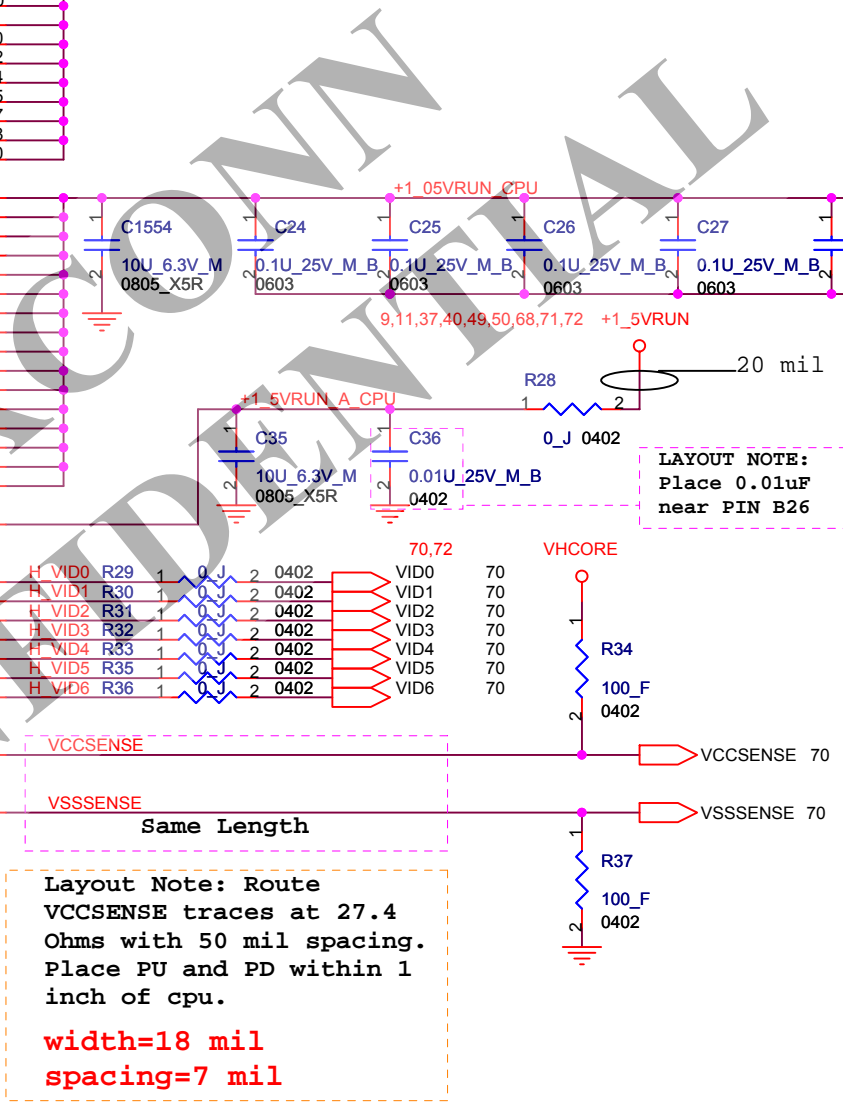


022706: Backup 10uF capacitors for 22uF shortage.



U1C		U1D	
A7	VCC[001]	AB20	VSS[001]
A9	VCC[002]	AB7	VSS[002]
A10	VCC[003]	AC7	VSS[003]
A12	VCC[004]	AC9	VSS[004]
A13	VCC[005]	AC12	VSS[005]
A15	VCC[006]	AC13	VSS[006]
A17	VCC[007]	AC15	VSS[007]
A18	VCC[008]	AC17	VSS[008]
A20	VCC[009]	AC18	VSS[009]
B7	VCC[010]	AD7	VSS[010]
B9	VCC[011]	AD9	VSS[011]
B10	VCC[012]	AD10	VSS[012]
B12	VCC[013]	AD12	VSS[013]
B14	VCC[014]	AD14	VSS[014]
B15	VCC[015]	AD15	VSS[015]
B17	VCC[016]	AD17	VSS[016]
B18	VCC[017]	AD18	VSS[017]
B20	VCC[018]	AE9	VSS[018]
C9	VCC[019]	AE10	VSS[019]
C10	VCC[020]	AE12	VSS[020]
C12	VCC[021]	AE13	VSS[021]
C13	VCC[022]	AE15	VSS[022]
C15	VCC[023]	AE17	VSS[023]
C17	VCC[024]	AE18	VSS[024]
C18	VCC[025]	AE20	VSS[025]
D9	VCC[026]	AF9	VSS[026]
D10	VCC[027]	AF10	VSS[027]
D12	VCC[028]	AF12	VSS[028]
D14	VCC[029]	AF14	VSS[029]
D15	VCC[030]	AF15	VSS[030]
D17	VCC[031]	AF17	VSS[031]
D18	VCC[032]	AF18	VSS[032]
E7	VCC[033]	AF20	VSS[033]
E9	VCC[034]		
E10	VCC[035]	V6	VSS[035]
E12	VCC[036]	G21	VSS[036]
E13	VCC[037]	J6	VSS[037]
E15	VCC[038]	K6	VSS[038]
E17	VCC[039]	M6	VSS[039]
E18	VCC[040]	J21	VSS[040]
E20	VCC[041]	K21	VSS[041]
F7	VCC[042]	M21	VSS[042]
F9	VCC[043]	N21	VSS[043]
F10	VCC[044]	N6	VSS[044]
F12	VCC[045]	R21	VSS[045]
F14	VCC[046]	R6	VSS[046]
F15	VCC[047]	T21	VSS[047]
F17	VCC[048]	T6	VSS[048]
F18	VCC[049]	V21	VSS[049]
F20	VCC[050]	W21	VSS[050]
AA7	VCC[051]		
AA9	VCC[052]	VCCA	VSS[052]
AA10	VCC[053]		
AA12	VCC[054]		
AA13	VCC[055]	AD6	VSS[054]
AA15	VCC[056]	AE5	VSS[055]
AA17	VCC[057]	AE5	VSS[056]
AA18	VCC[058]	AE4	VSS[057]
AA20	VCC[059]	AE3	VSS[058]
AB9	VCC[060]	AE2	VSS[059]
AC10	VCC[061]	AE2	VSS[060]
AB10	VCC[062]		
AB12	VCC[063]		
AB14	VCC[064]		
AB15	VCC[065]		
AB17	VCC[066]		
AB18	VCC[067]		
		VID[0]	VSS[061]
		VID[1]	VSS[062]
		VID[2]	VSS[063]
		VID[3]	VSS[064]
		VID[4]	VSS[065]
		VID[5]	VSS[066]
		VID[6]	VSS[067]

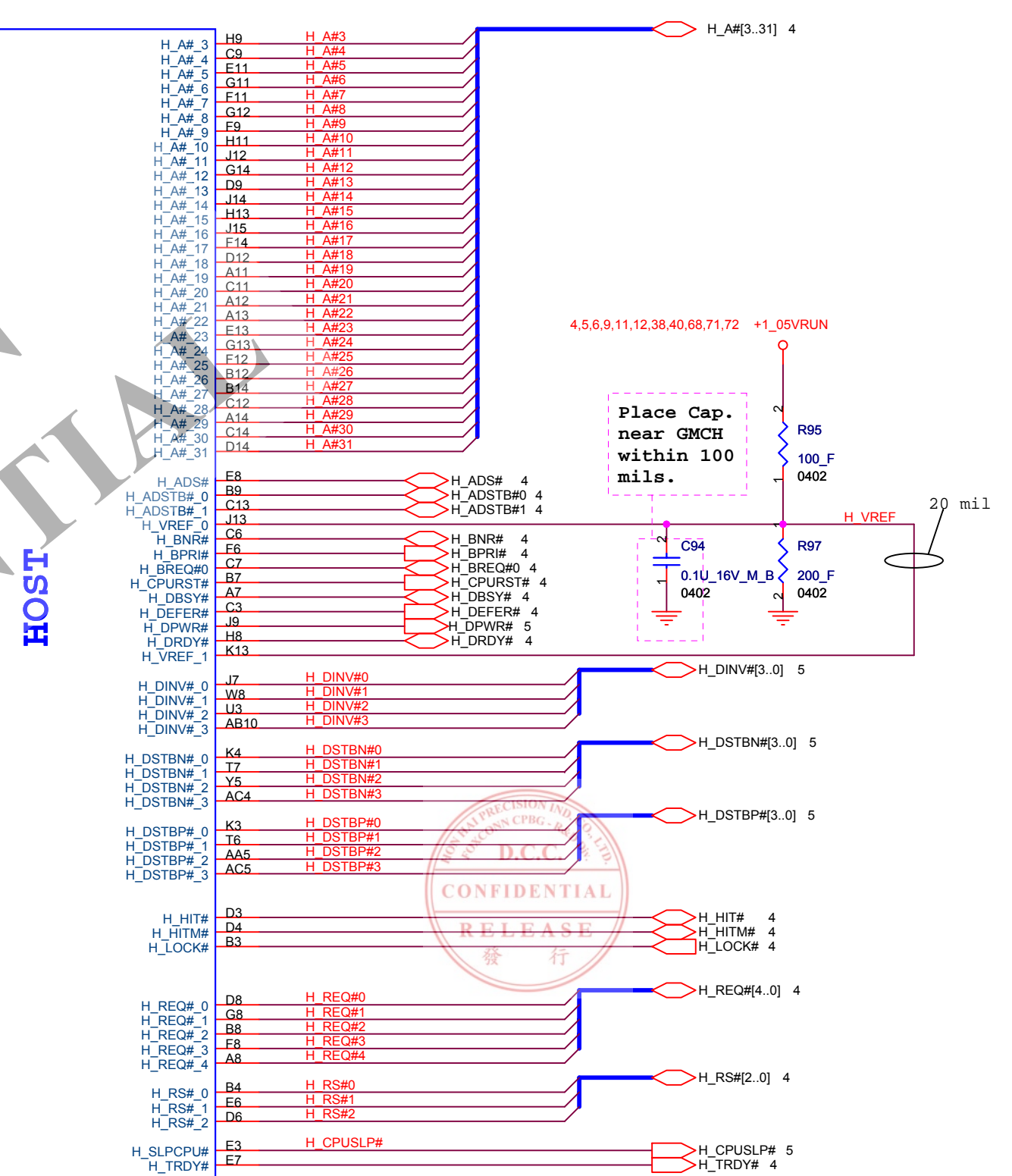
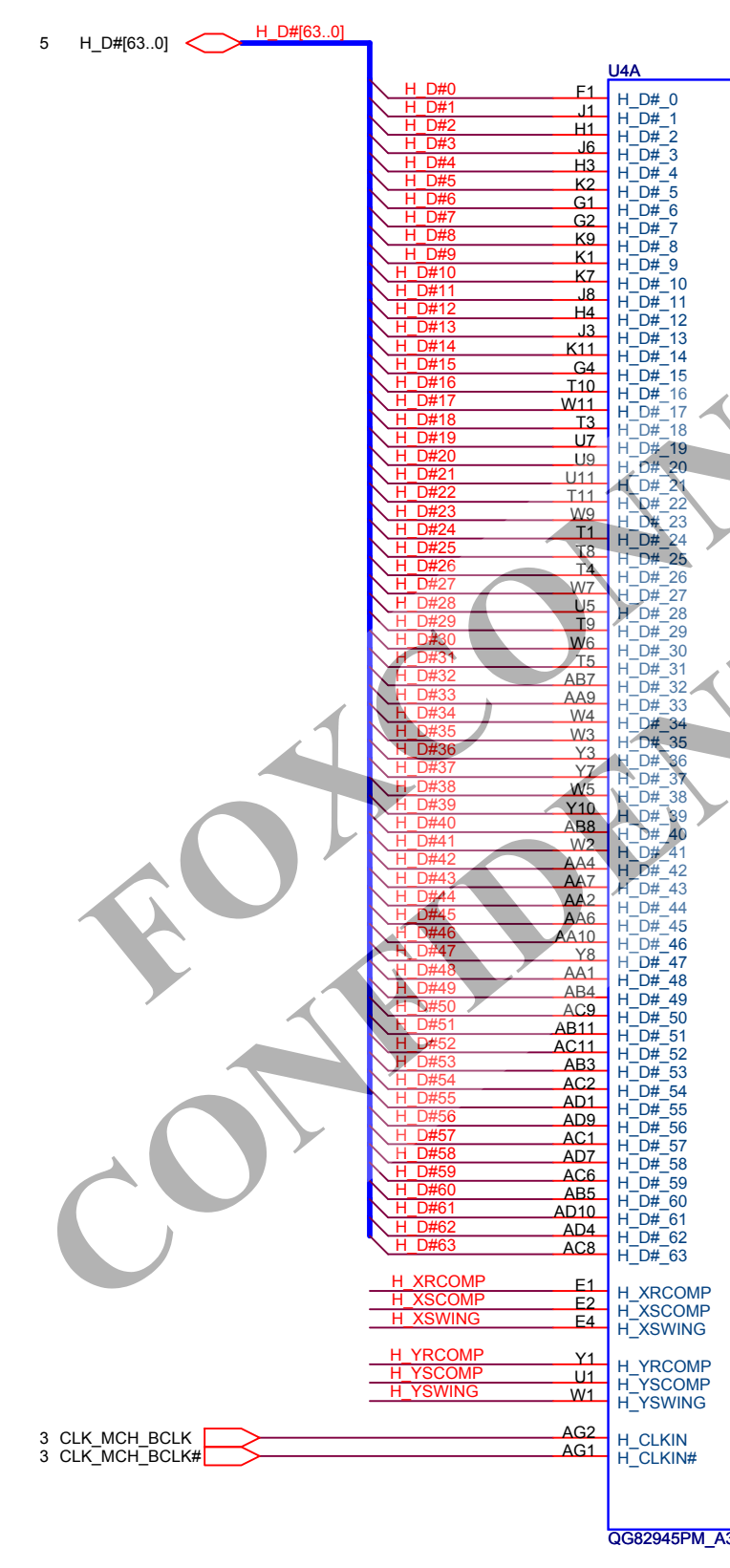
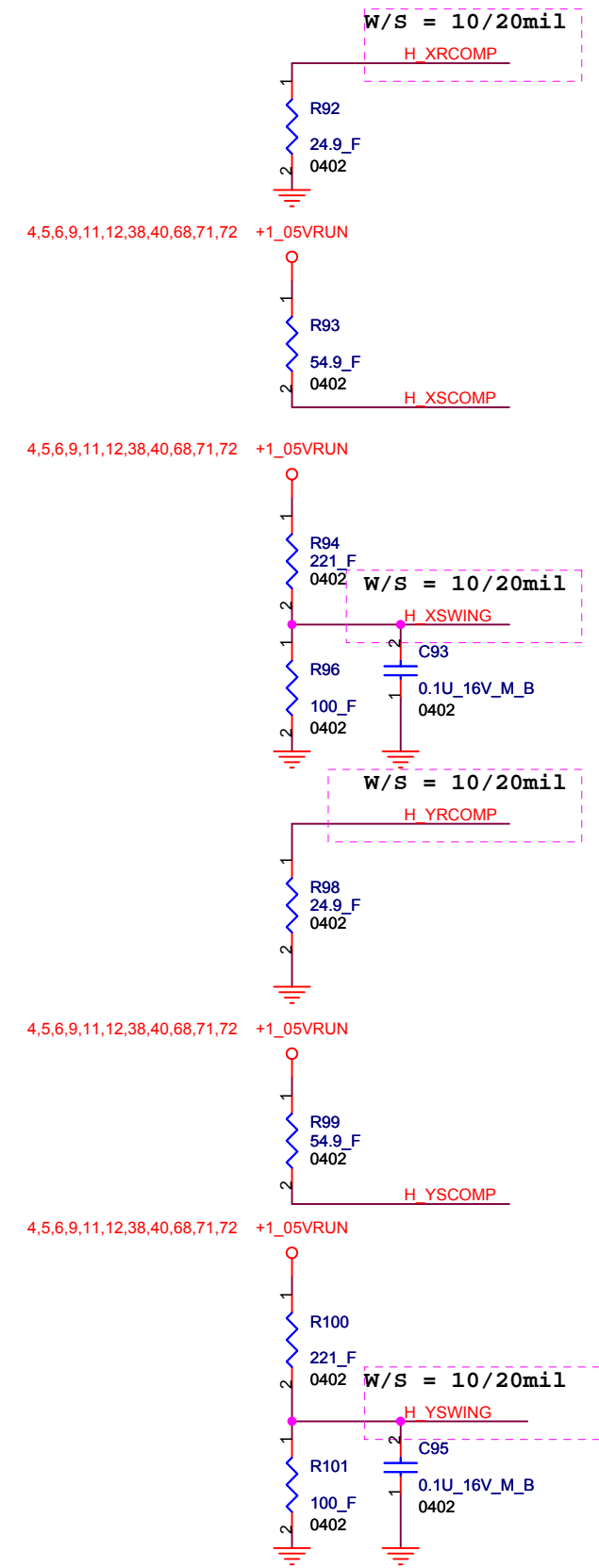
CPU_VCCA---->120mA
 CPU_VCCP---->2.5A
 CPU_VCC---->44A



LAYOUT NOTE:
Place 0.01uF near PIN B26

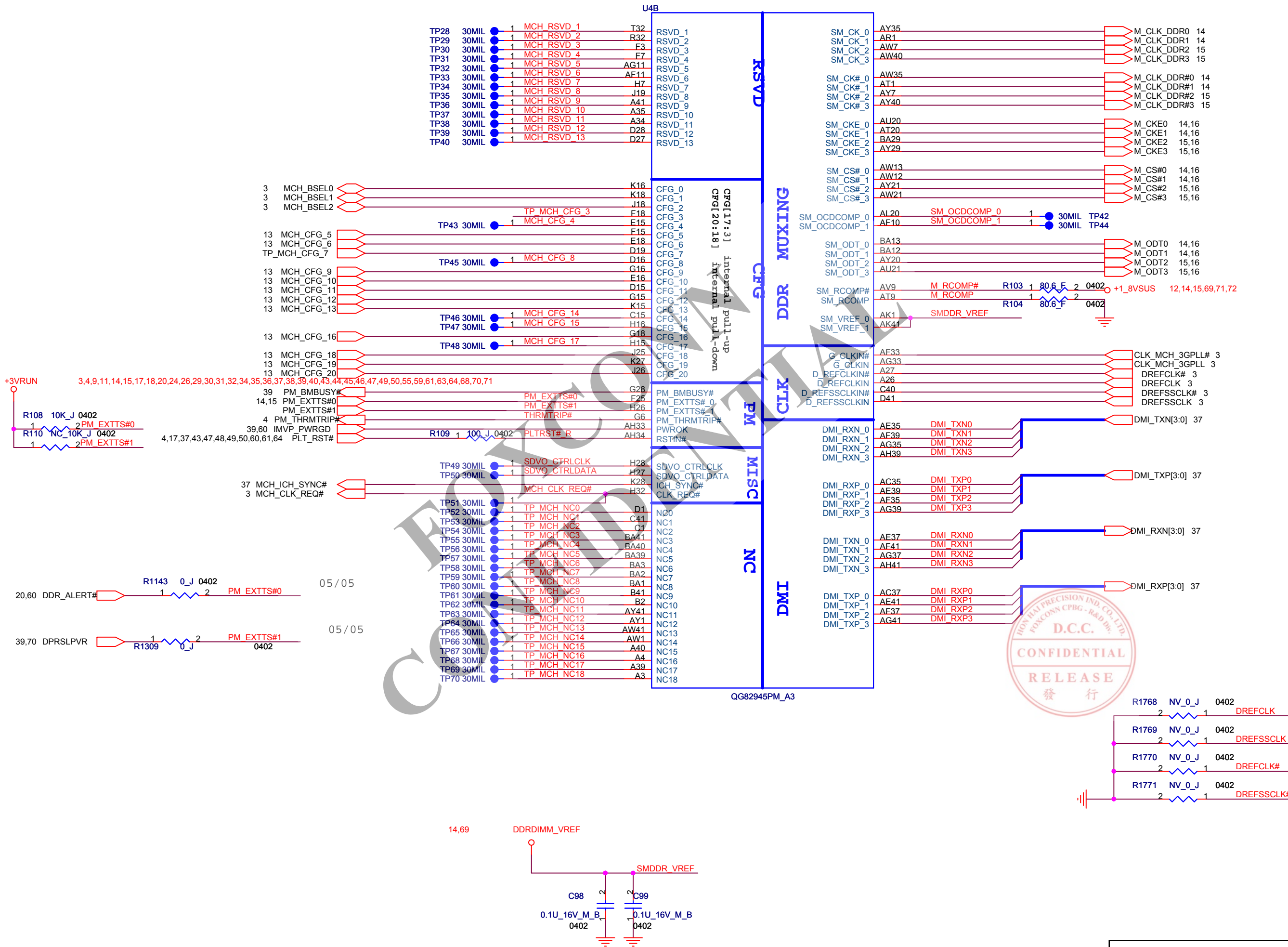


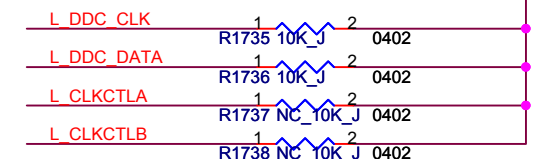
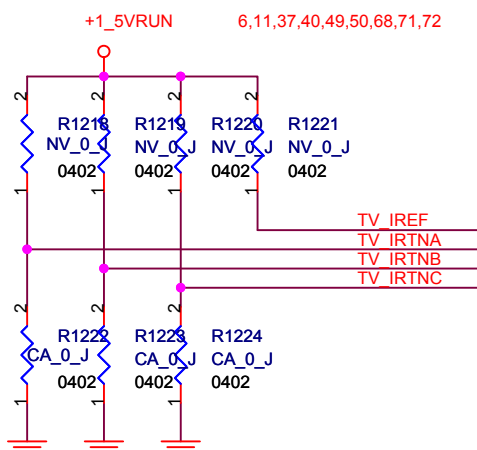
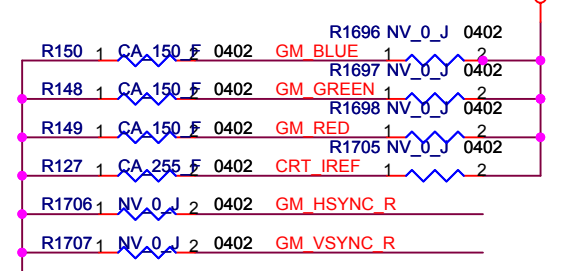
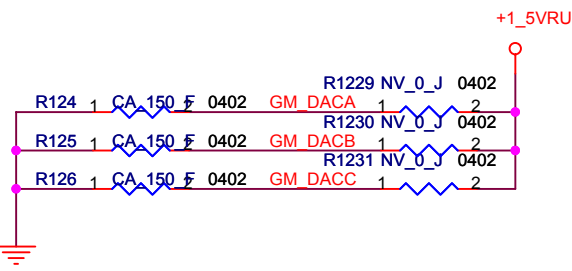
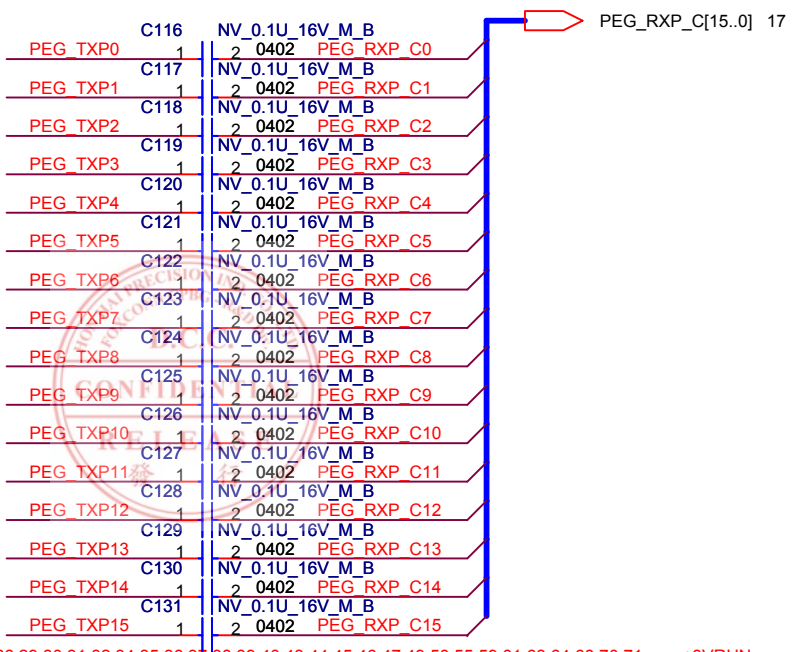
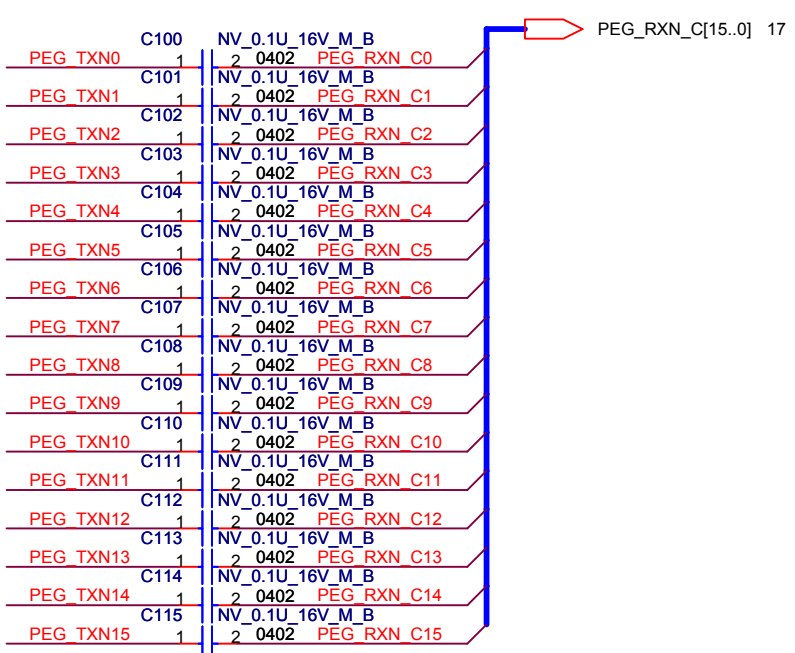
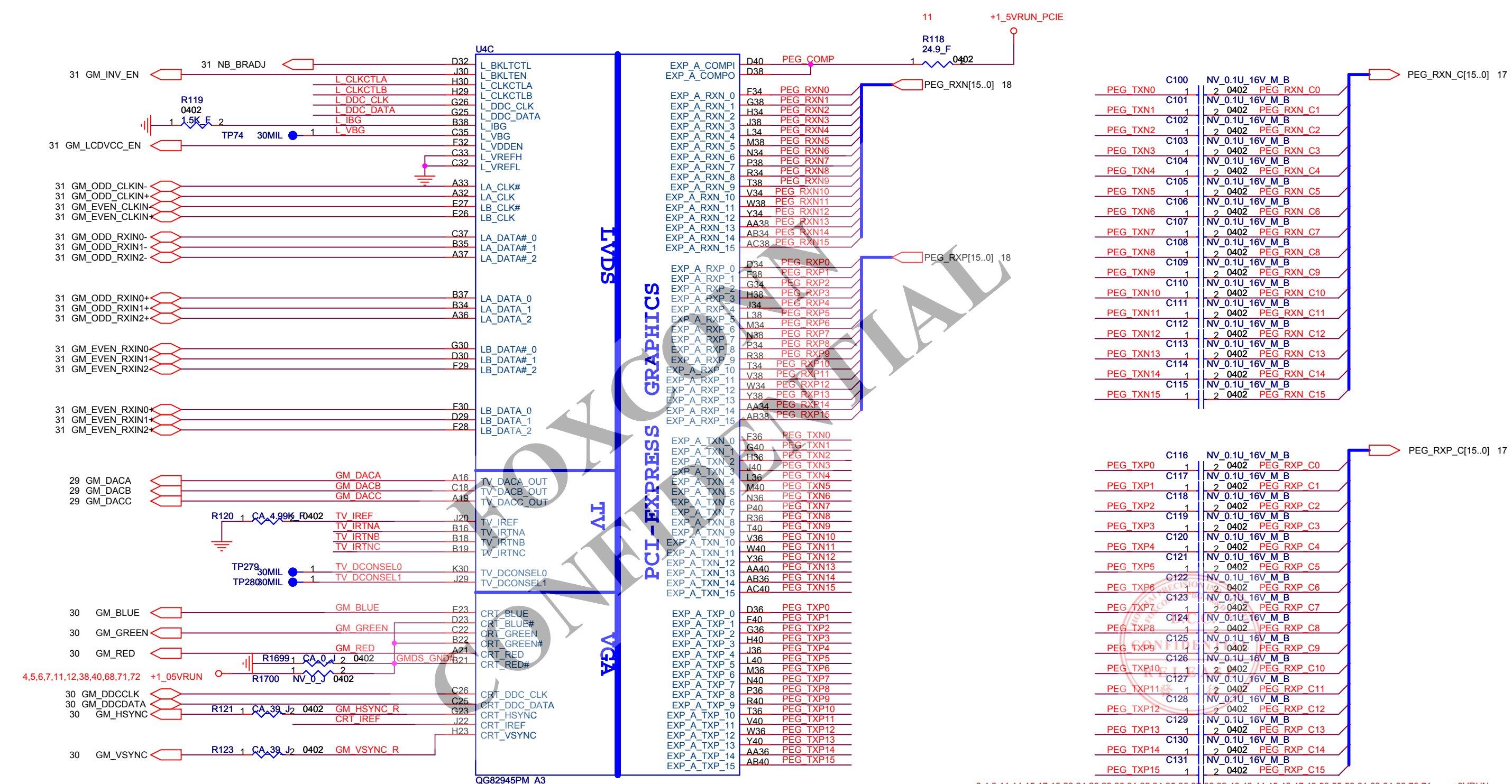
U1D		P6	
A4	VSS[001]	VSS[082]	P21
A8	VSS[002]	VSS[083]	P24
A11	VSS[003]	VSS[084]	R2
A14	VSS[004]	VSS[085]	R5
A16	VSS[005]	VSS[086]	R22
A19	VSS[006]	VSS[087]	R25
A23	VSS[007]	VSS[088]	T1
A26	VSS[008]	VSS[089]	T4
B6	VSS[009]	VSS[090]	T23
B8	VSS[010]	VSS[091]	T26
B11	VSS[011]	VSS[092]	U3
B13	VSS[012]	VSS[093]	U6
B16	VSS[013]	VSS[094]	U21
B19	VSS[014]	VSS[095]	U24
B21	VSS[015]	VSS[096]	V2
B24	VSS[016]	VSS[097]	V5
C5	VSS[017]	VSS[098]	V22
C8	VSS[018]	VSS[099]	V25
C11	VSS[019]	VSS[100]	W1
C14	VSS[020]	VSS[101]	W4
C16	VSS[021]	VSS[102]	W23
C19	VSS[022]	VSS[103]	W26
C22	VSS[023]	VSS[104]	Y3
C25	VSS[024]	VSS[105]	Y6
D1	VSS[025]	VSS[106]	Y21
D4	VSS[026]	VSS[107]	Y24
D8	VSS[027]	VSS[108]	AA2
D11	VSS[028]	VSS[109]	AA5
D13	VSS[029]	VSS[110]	AA8
D16	VSS[030]	VSS[111]	AA11
D19	VSS[031]	VSS[112]	AA14
D23	VSS[032]	VSS[113]	AA16
D26	VSS[033]	VSS[114]	AA19
E3	VSS[034]	VSS[115]	AA22
E6	VSS[035]	VSS[116]	AA25
E8	VSS[036]	VSS[117]	AB1
E11	VSS[037]	VSS[118]	AB4
E14	VSS[038]	VSS[119]	AB8
E19	VSS[039]	VSS[120]	AB11
E19	VSS[040]	VSS[121]	AB13
E21	VSS[041]	VSS[122]	AB16
E24	VSS[042]	VSS[123]	AB19
F5	VSS[043]	VSS[124]	AB23
F8	VSS[044]	VSS[125]	AB26
F11	VSS[045]	VSS[126]	AC3
F13	VSS[046]	VSS[127]	AC6
F16	VSS[047]	VSS[128]	AC8
F19	VSS[048]	VSS[129]	AC11
F2	VSS[049]	VSS[130]	AC14
F2	VSS[050]	VSS[131]	AC16
F22	VSS[051]	VSS[132]	AC19
F25	VSS[052]	VSS[133]	AC21
G4	VSS[053]	VSS[134]	AC24
G1	VSS[054]	VSS[135]	AD2
G23	VSS[055]	VSS[136]	AD5
G26	VSS[056]	VSS[137]	AD8
H3	VSS[057]	VSS[138]	AD11
H6	VSS[058]	VSS[139]	AD13
H21	VSS[059]	VSS[140]	AD16
H24	VSS[060]	VSS[141]	AD19
J2	VSS[061]	VSS[142]	AD22
J5	VSS[062]	VSS[143]	AD25
J22	VSS[063]	VSS[144]	AE1
J25	VSS[064]	VSS[145]	AE4
K1	VSS[065]	VSS[146]	AE8
K4	VSS[066]	VSS[147]	AE11
K23	VSS[067]	VSS[148]	AE14
K26	VSS[068]	VSS[149]	AE16
L3	VSS[069]	VSS[150]	AE19
L6	VSS[070]	VSS[151]	AE23
L21	VSS[071]	VSS[152]	AE26
L24	VSS[072]	VSS[153]	AE3
M2	VSS[073]	VSS[154]	AE6
M5	VSS[074]	VSS[155]	AE8
M22	VSS[075]	VSS[156]	AE11
M25	VSS[076]	VSS[157]	AE13
N1	VSS[077]	VSS[158]	AE16
N4	VSS[078]	VSS[159]	AE19
N23	VSS[079]	VSS[160]	AE21
N26	VSS[080]	VSS[161]	AE24
P3	VSS[081]	VSS[162]	

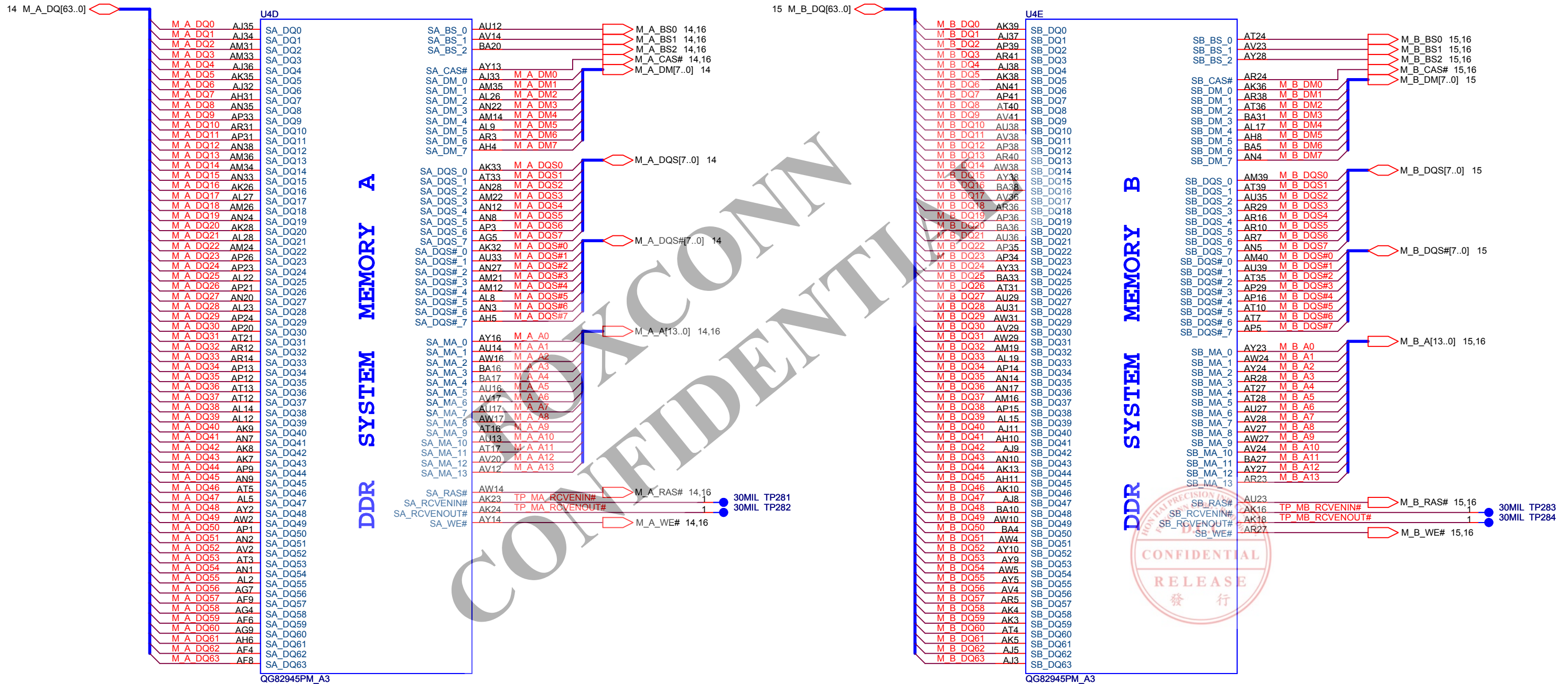


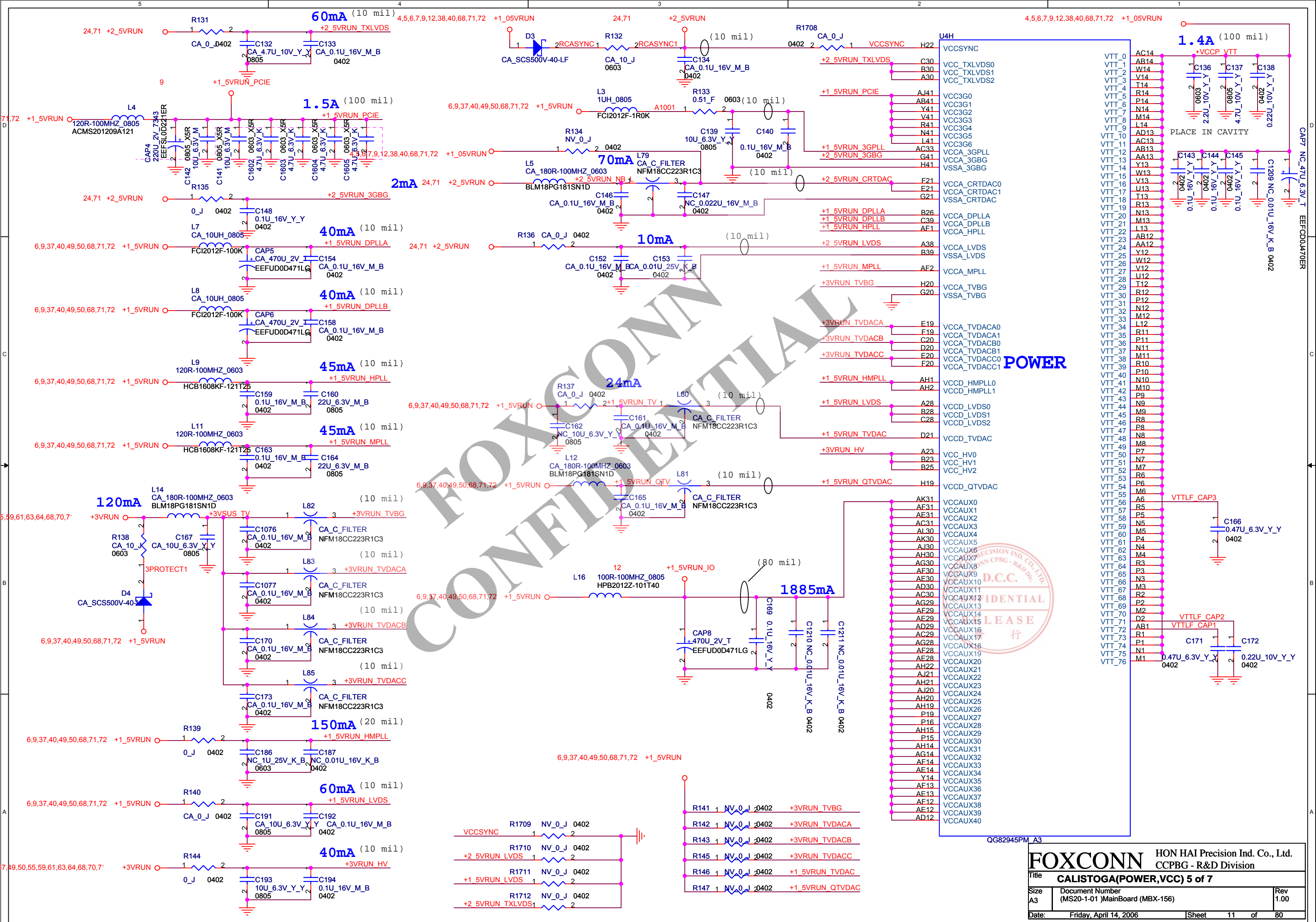
CONFIDENTIAL









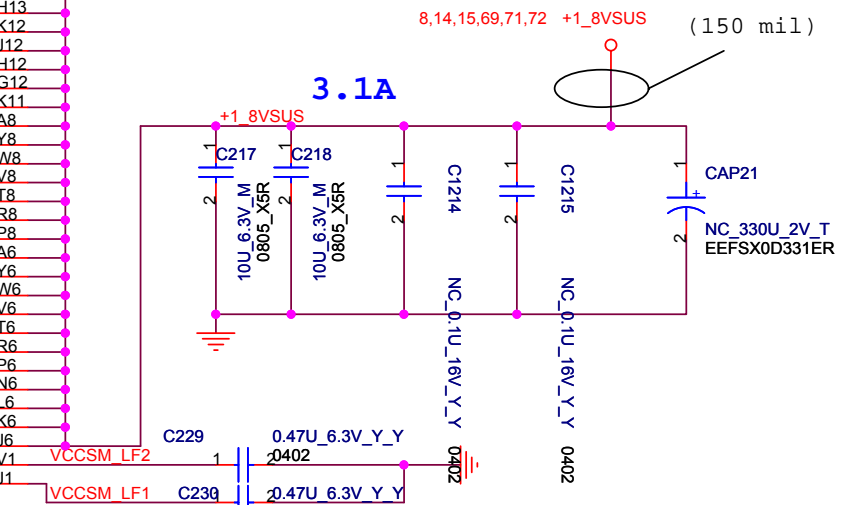
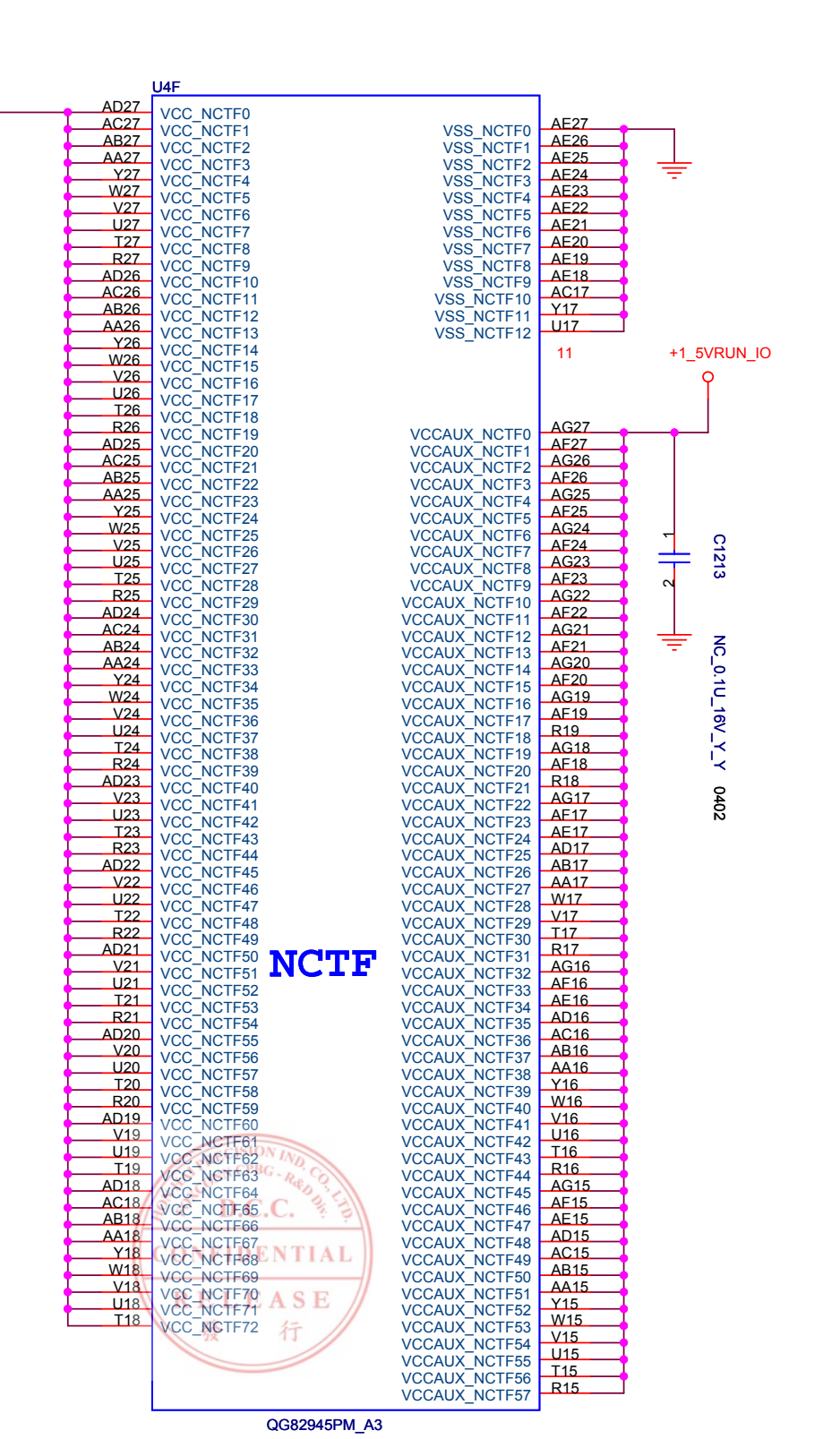
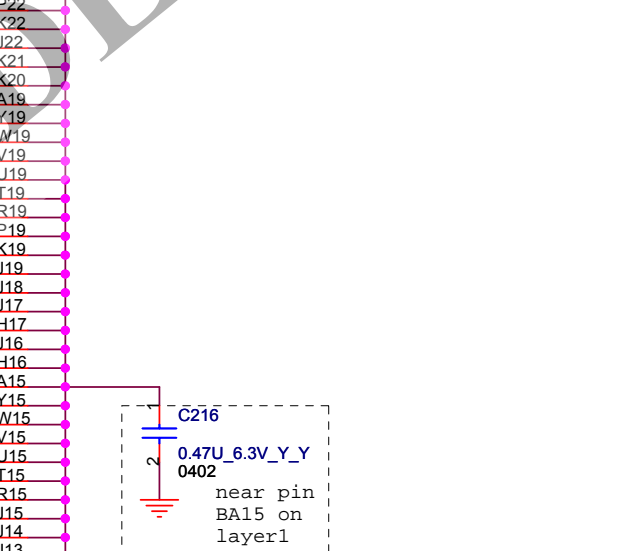
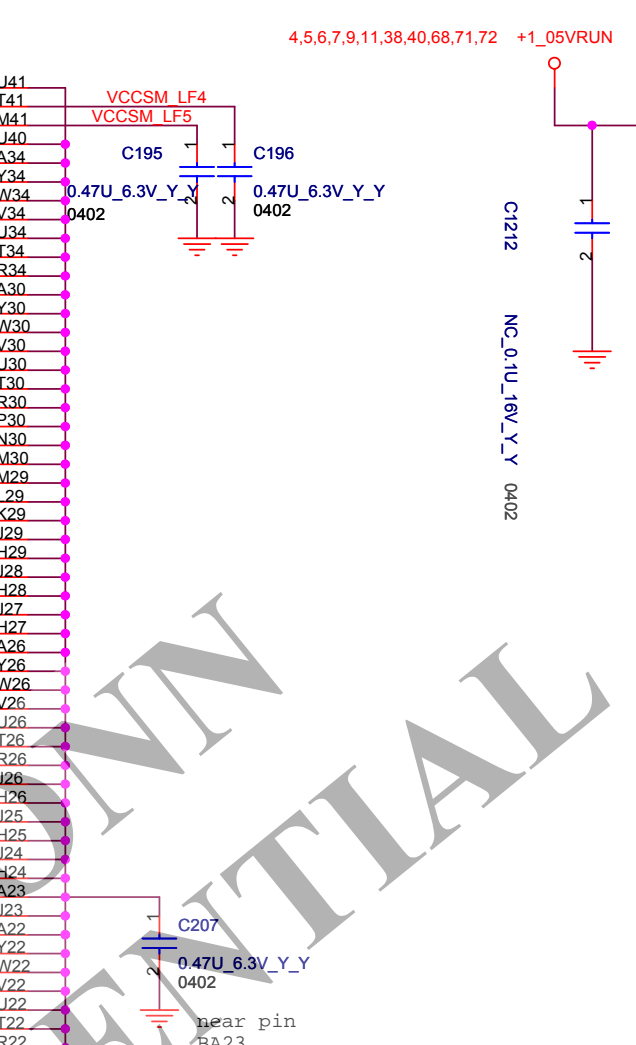
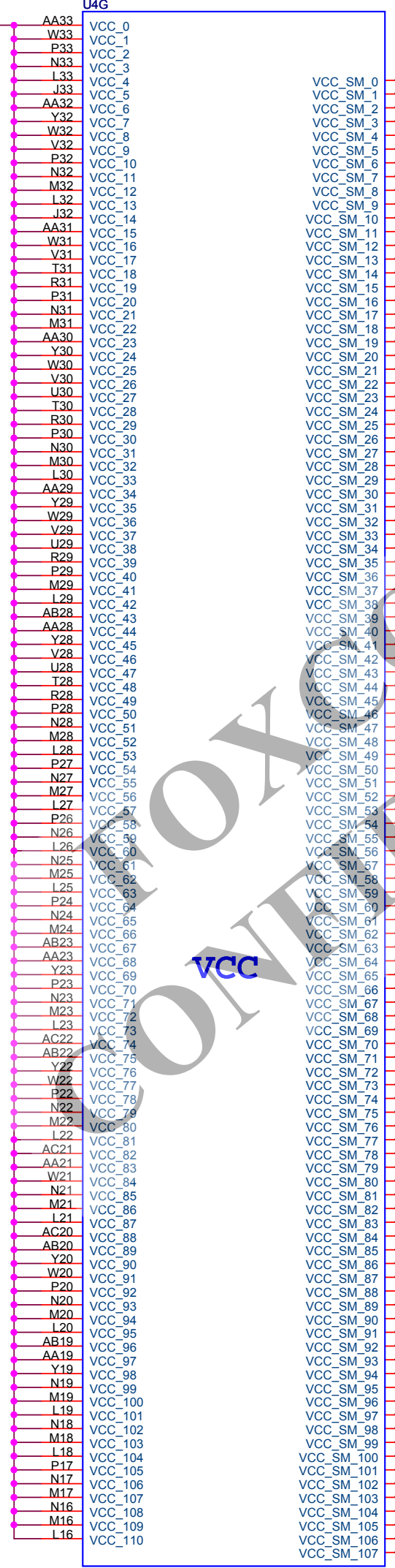
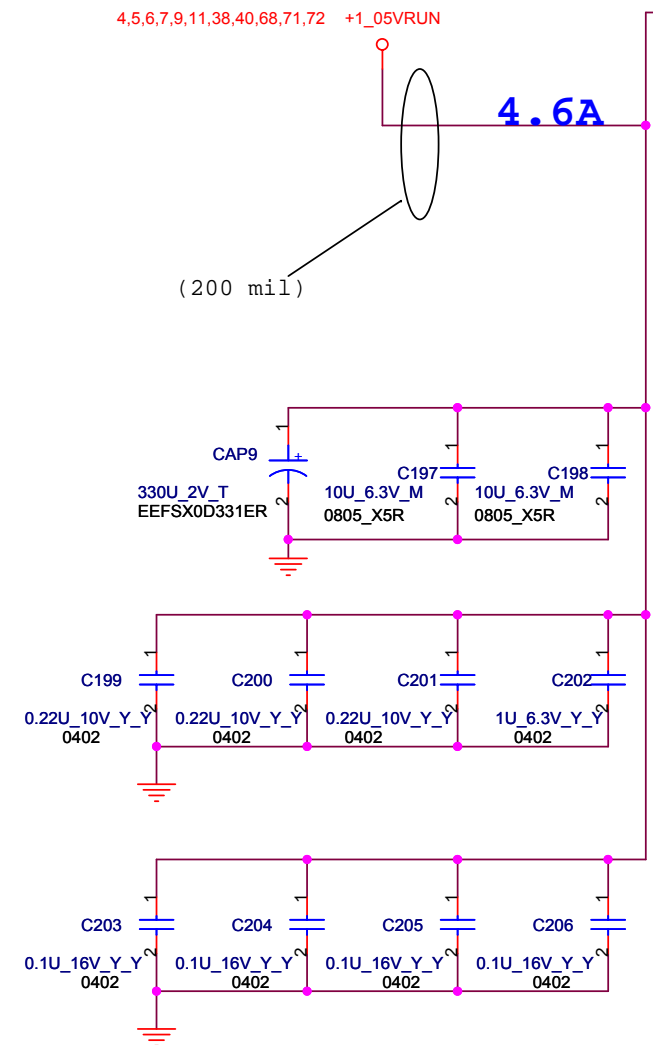


POWER

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: **CALISTOGA(POWER,VCC) 5 of 7**

Size A3	Document Number (MS20-1-01)MainBoard (MBX-156)	Rev 1.00
Date: Friday, April 14, 2006	Sheet 11	of 80





MCH_CFG_5	Low = DMIx2 High = DMIx4
-----------	-----------------------------

MCH_CFG_18 (VCC_CORE Select)	Low = 1.05V(default) High = 1.5V
---------------------------------	-------------------------------------



MCH_CFG_6	Low = Moby Dick High = Calistoga DDR2 select (default high)
-----------	---

MCH_CFG_19 (DMI LANE REVERSAL)	Low = Normal(default) High = LANES REVERSED
-----------------------------------	--



MCH_CFG_7 (CPU Strap)	Low = RSVD High = Mobile Yonah processor
--------------------------	---

MCH_CFG_20 (PCIe Backward Interoperability mode)	Low = Only SDVO or PCIE x1 is operational (defaults) High = SDVO and PCIE x1 are operating simultaneously via the PEG port
---	---



MCH_CFG_9 (PCIe Graphics Lane)	Low = Reverse Lane High = Normal operation
-----------------------------------	---

For layout convenience



MCH_CFG_10 (HOST PLL VCC SELECT)	Low = RESERVED High = MOBILITY
-------------------------------------	-----------------------------------

Layout Noe:
Location of all MCH_CFG strap resistors needs to be close to trace to minimize stub



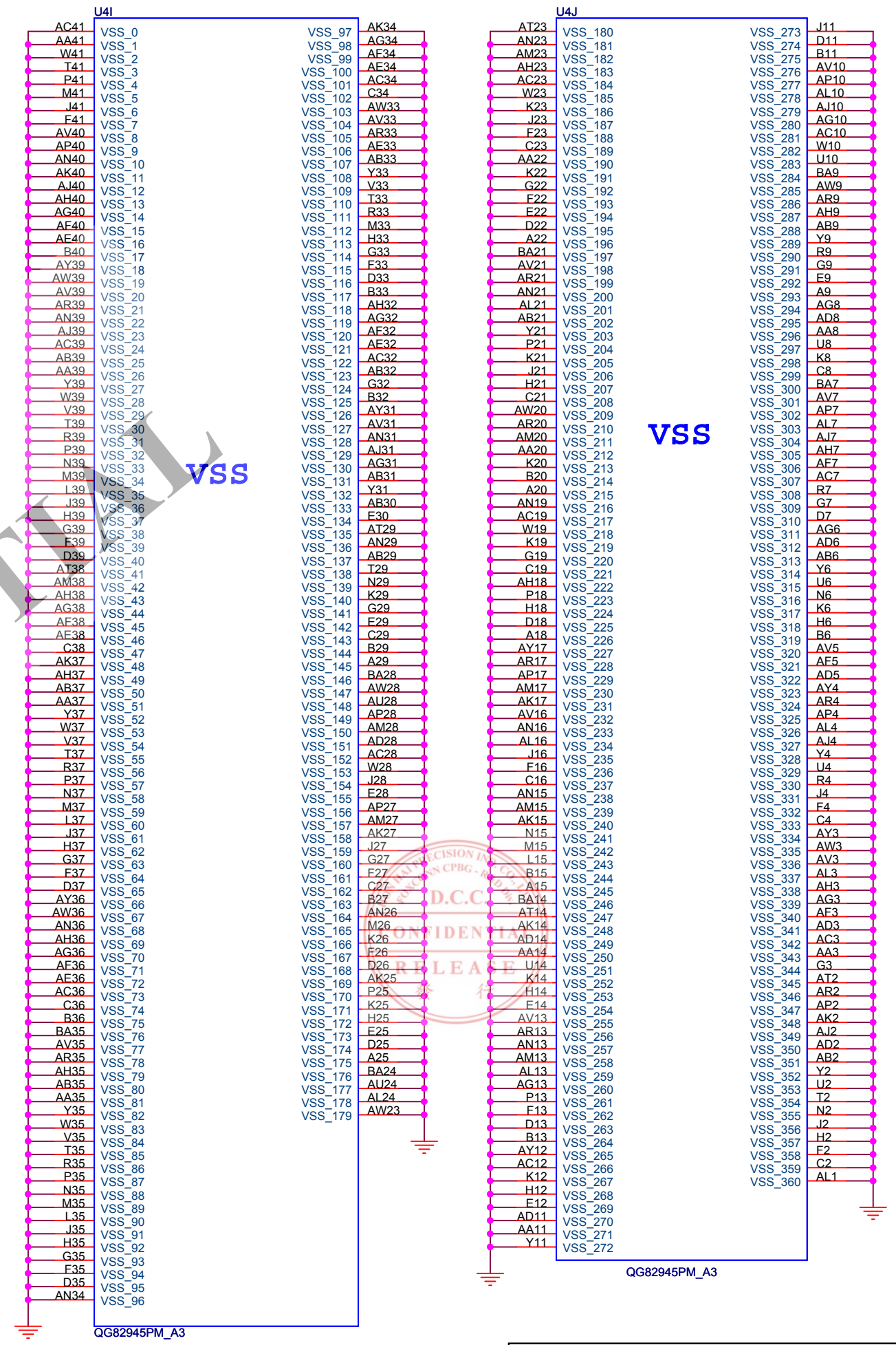
MCH_CFG_11 (PSB 4x CLK ENABLE)	Low = Calistoga High = Reserved
-----------------------------------	------------------------------------



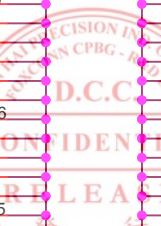
MCH_CFG_[13:12] (XOR/ALLZ)	00=Partial Clock Gating Disable 01=XOR Mode Enable 10=All-Z Mode Enable 11=Normal Operation(Default)
-------------------------------	---



MCH_CFG_16 (FSB Dynamic ODT)	Low = Dynamic ODT Disabled High = Dynamic ODT Enable
---------------------------------	---



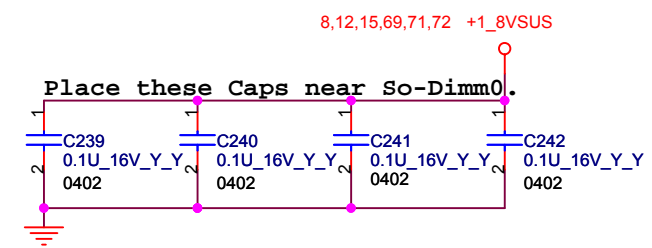
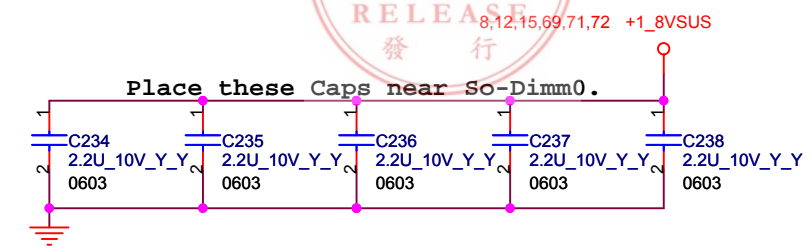
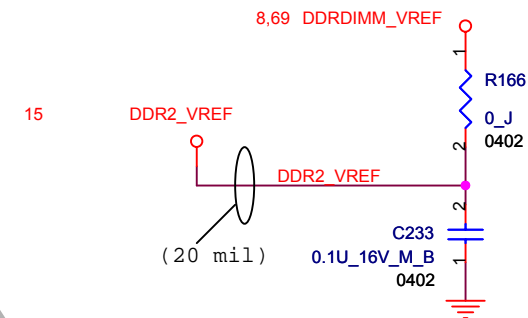
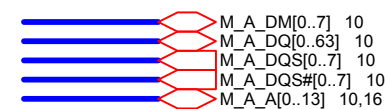
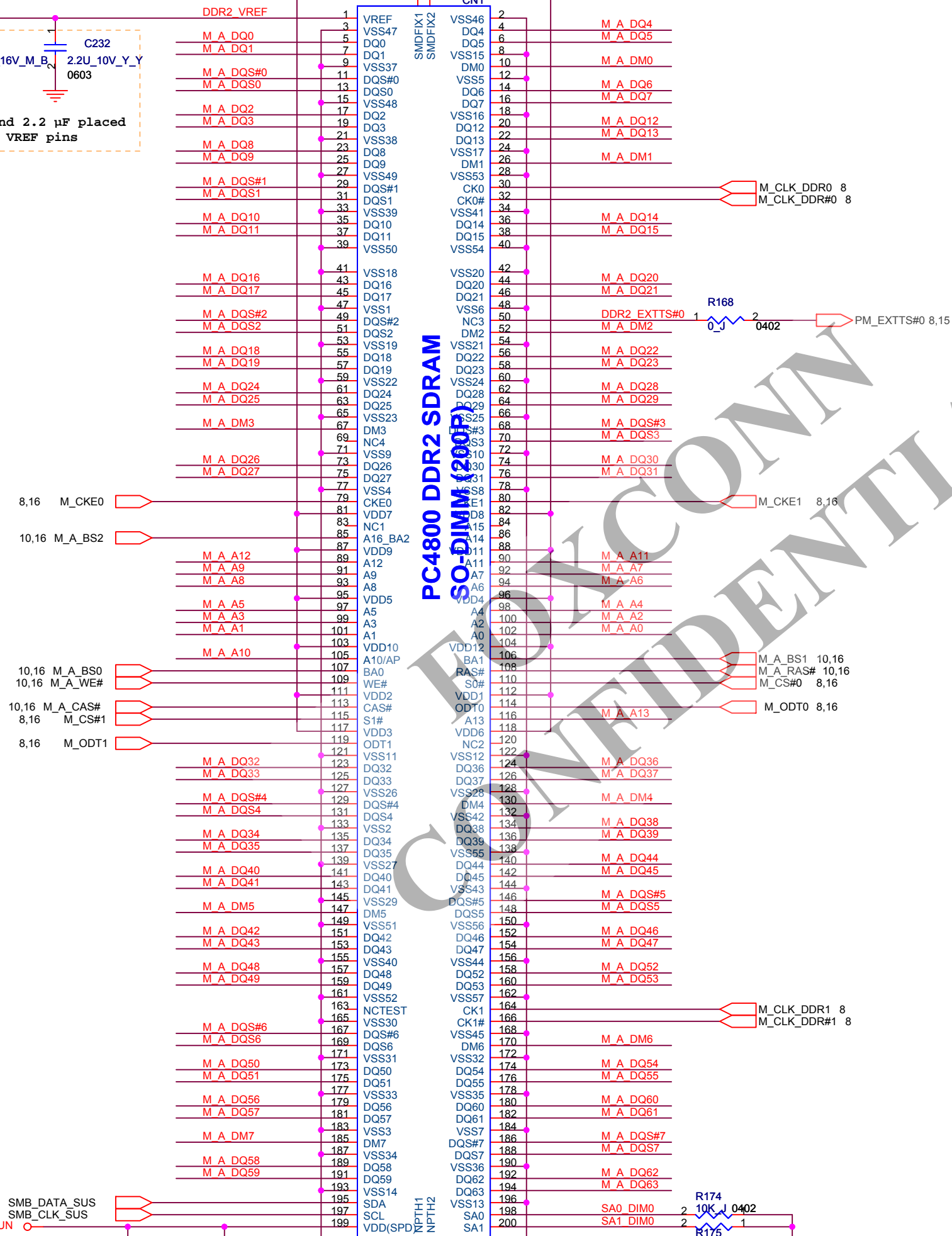
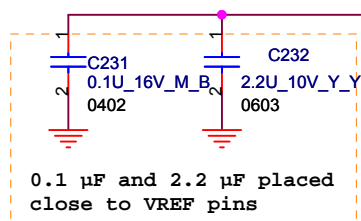
CONFIDENTIAL



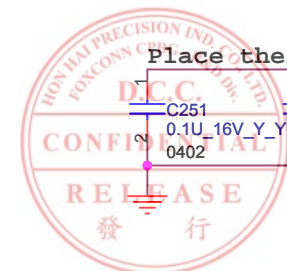
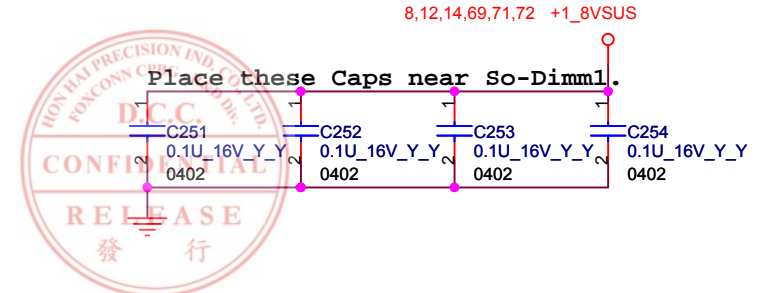
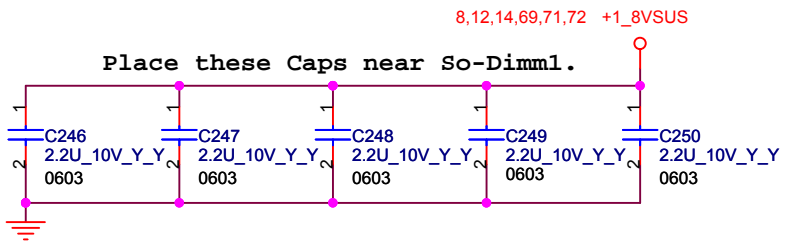
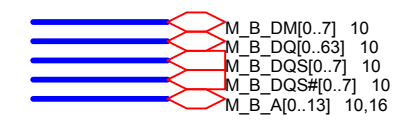
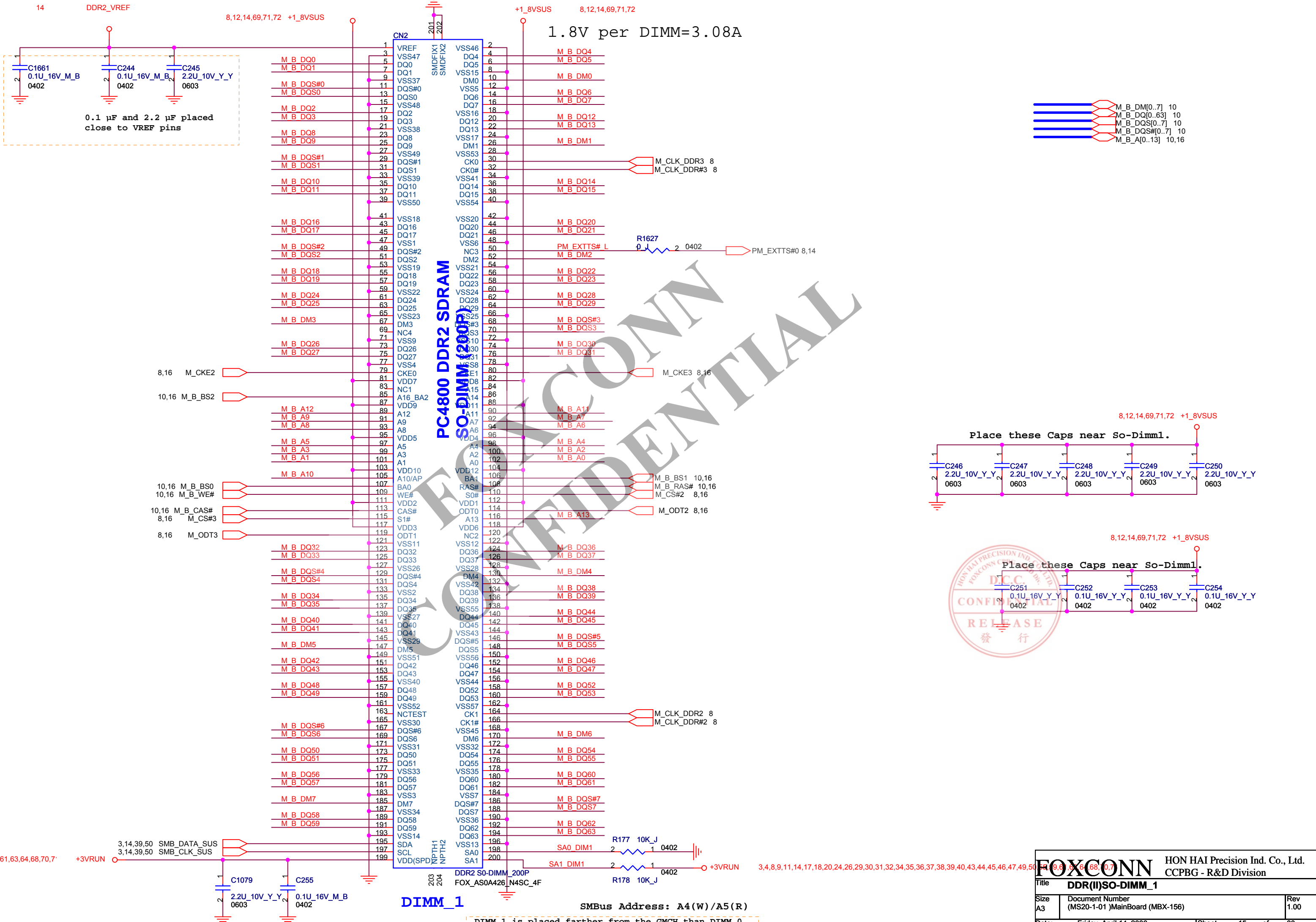
8,12,15,69,71,72 +1_8VSUS

+1_8VSUS 8,12,15,69,71,72

1.8V per DIMM=3.08A



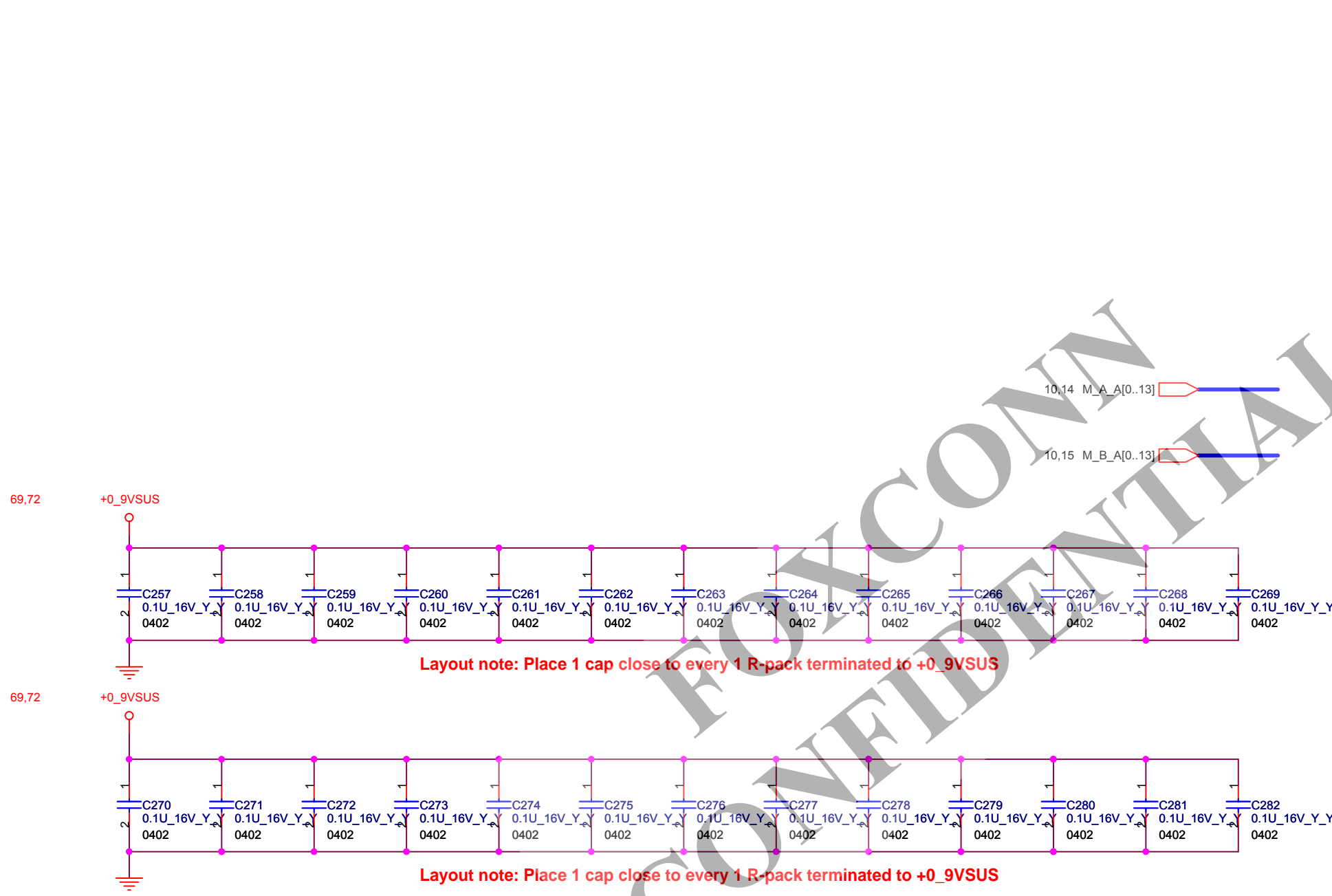
FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R & D Division		
Title DDR(I)SO-DIMM_0		
Size A3	Document Number (MS20-1-01) MainBoard (MBX-156)	Rev 1.00
Date: Friday, April 14, 2006	Sheet 14	of 80



FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	DDR(II)SO-DIMM_1	
Size	Document Number	Rev
A3	(MS20-1-01) MainBoard (MBX-156)	1.00
Date:	Friday, April 14, 2006	Sheet 15 of 80

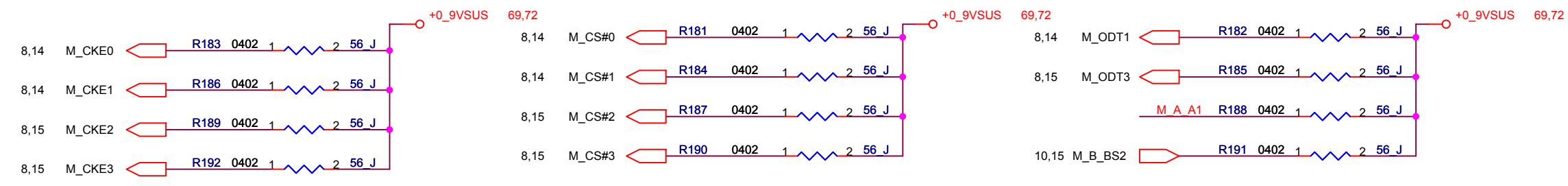
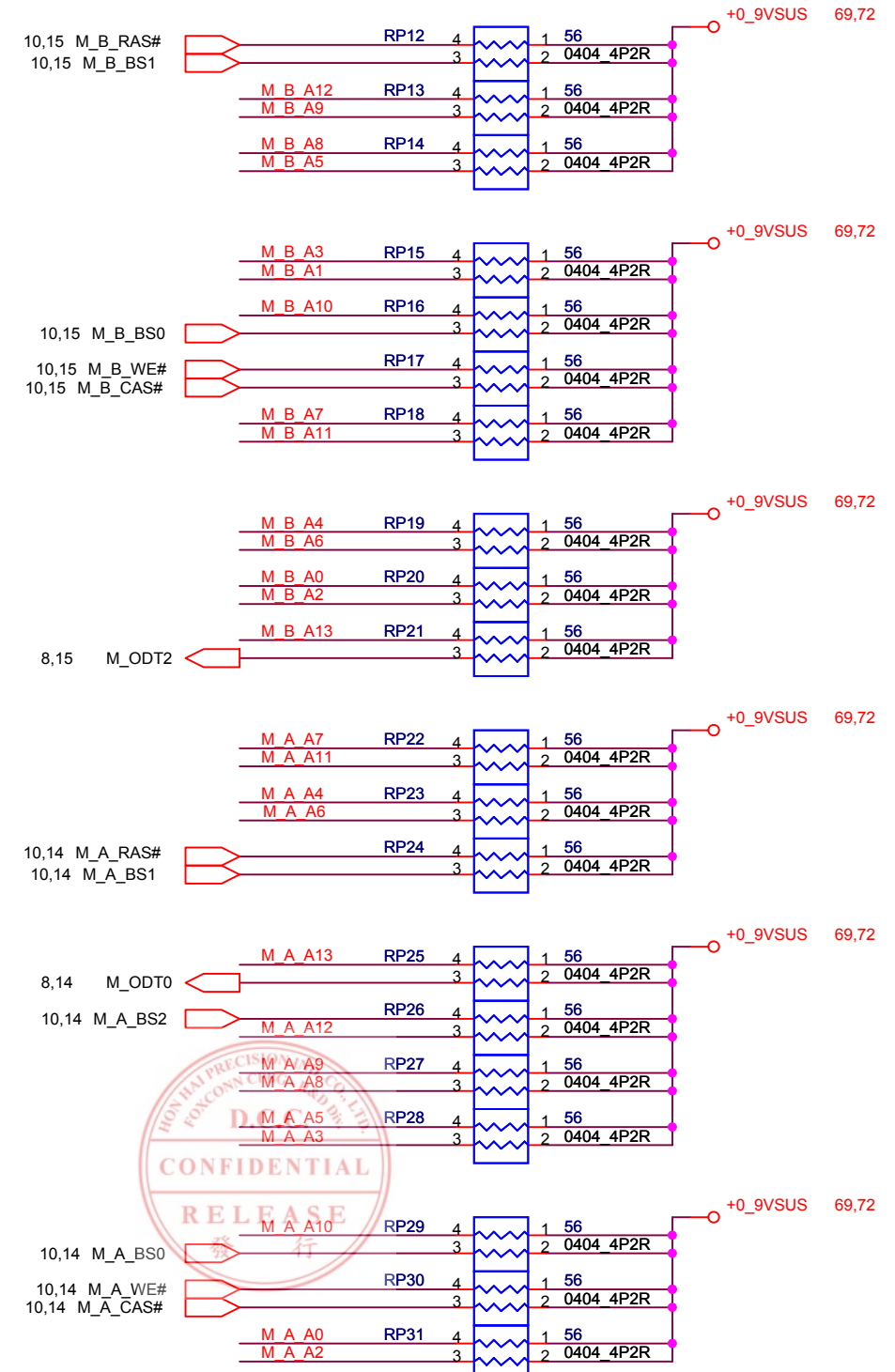
DIMM_1 SMBus Address: A4(W)/A5(R)

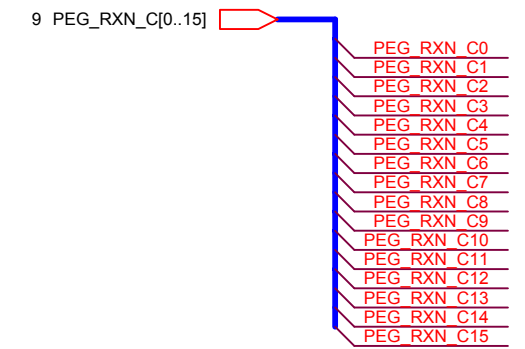
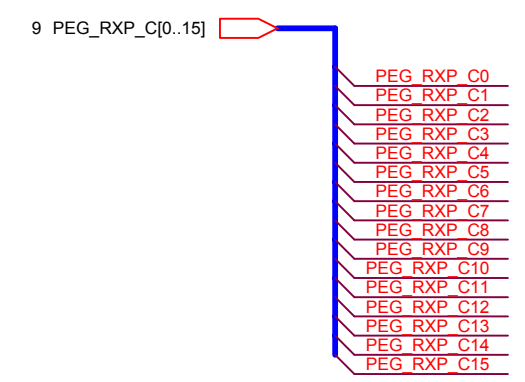
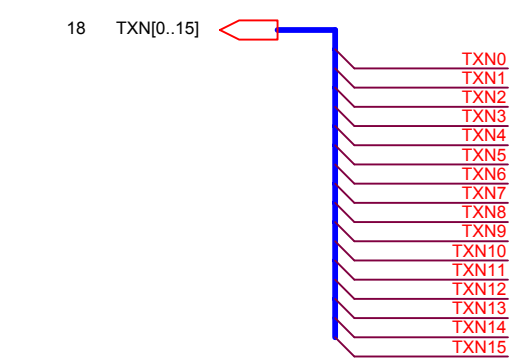
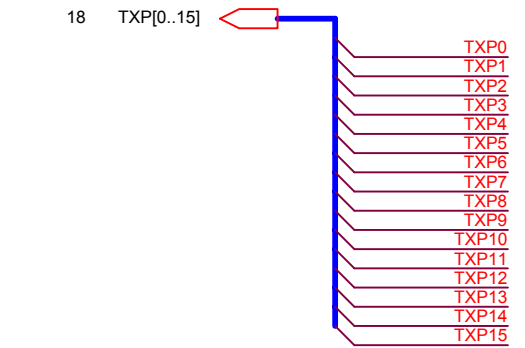
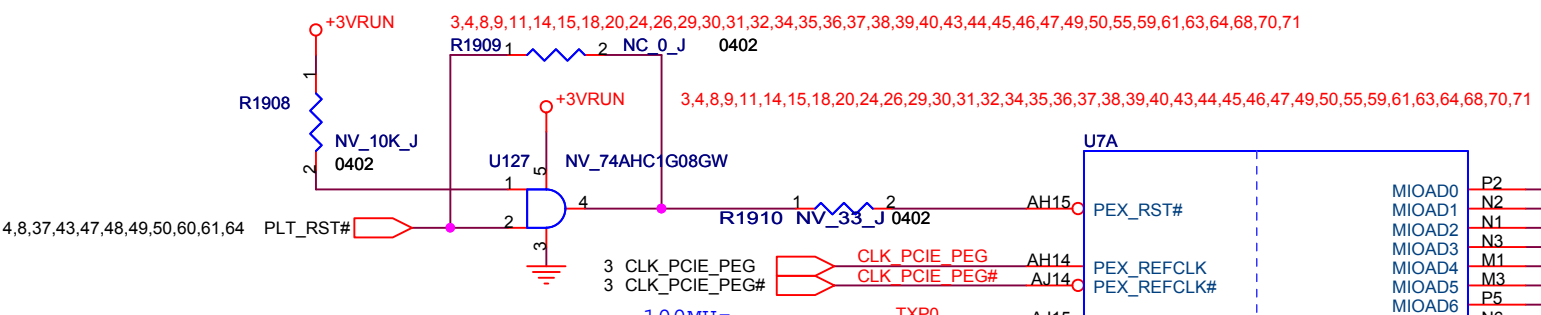
DIMM_1 is placed farther from the GMCH than DIMM_0



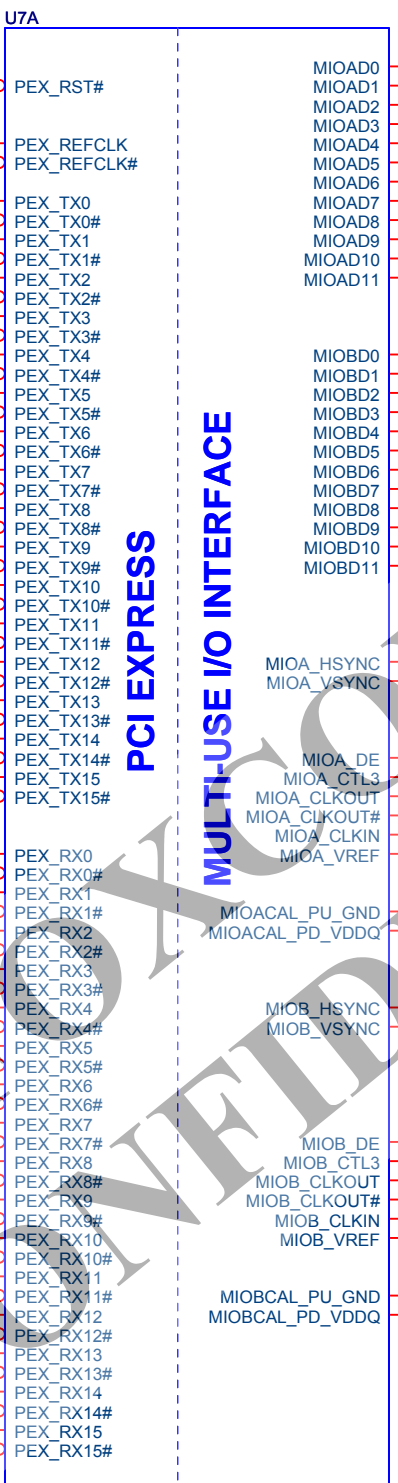
10,14 M_A_A[0..13]

10,15 M_B_A[0..13]



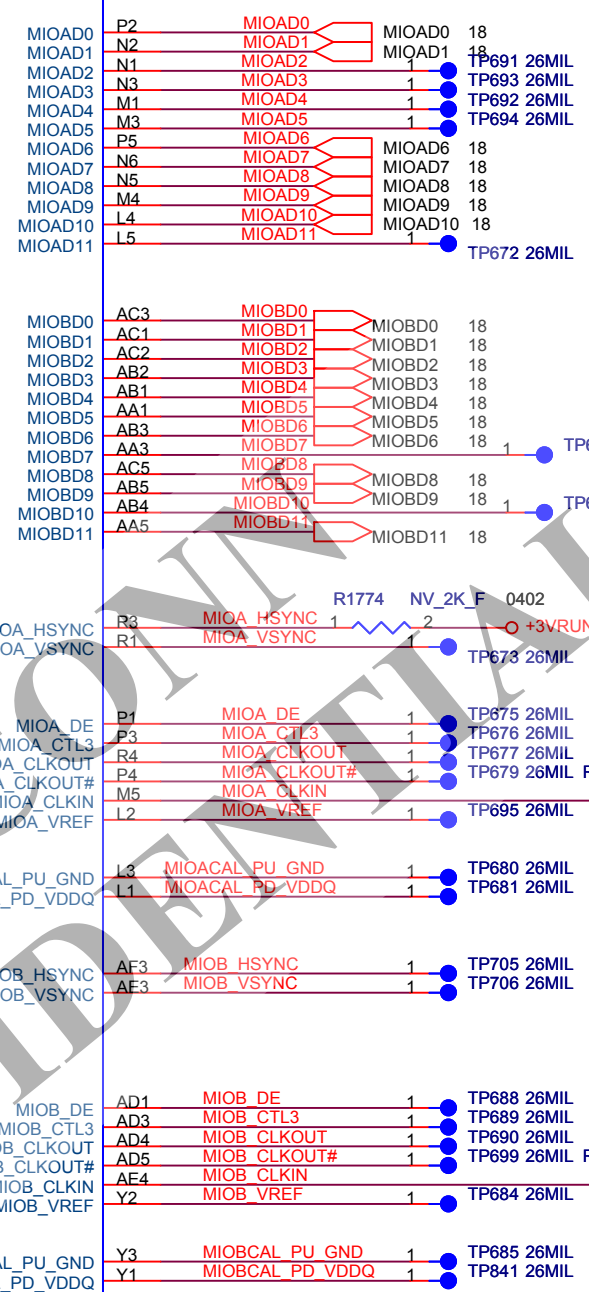


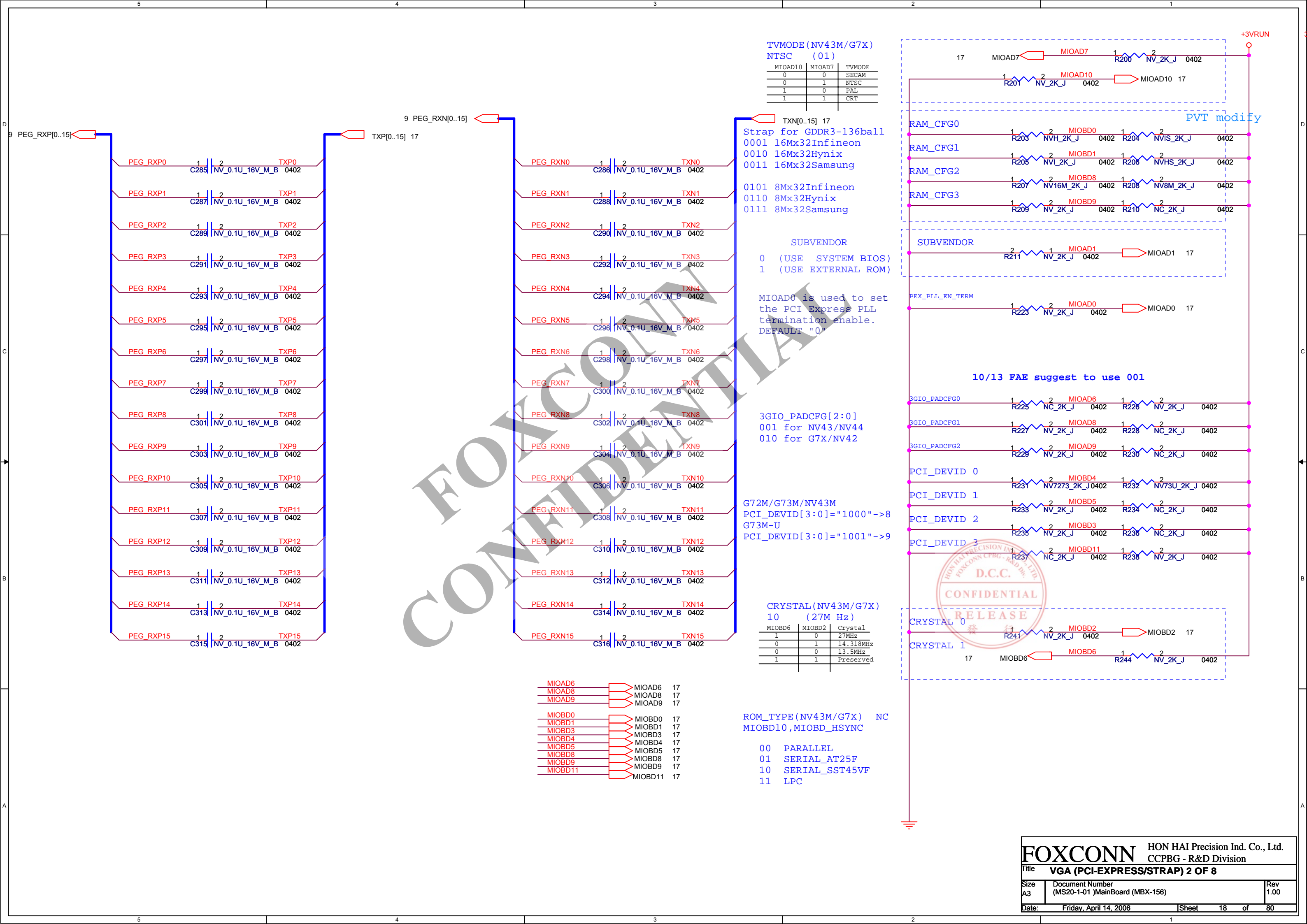
- TXP0 AH15
- TXP1 AK15
- TXP2 AH16
- TXP3 AG16
- TXP4 AG17
- TXP5 AH17
- TXP6 AG18
- TXP7 AH18
- TXP8 AK18
- TXP9 AJ18
- TXP10 AH19
- TXP11 AG20
- TXP12 AH20
- TXP13 AG21
- TXP14 AH21
- TXP15 AK21
- TXN0 AH15
- TXN1 AK15
- TXN2 AH16
- TXN3 AG16
- TXN4 AG17
- TXN5 AH17
- TXN6 AG18
- TXN7 AH18
- TXN8 AK18
- TXN9 AJ18
- TXN10 AH19
- TXN11 AG20
- TXN12 AH20
- TXN13 AG21
- TXN14 AH21
- TXN15 AK21
- PEG_RXP_C0 AK13
- PEG_RXP_C1 AK14
- PEG_RXP_C2 AM14
- PEG_RXP_C3 AM15
- PEG_RXP_C4 AL15
- PEG_RXP_C5 AK16
- PEG_RXP_C6 AK17
- PEG_RXP_C7 AL17
- PEG_RXP_C8 AL18
- PEG_RXP_C9 AM18
- PEG_RXP_C10 AM19
- PEG_RXP_C11 AK19
- PEG_RXP_C12 AK20
- PEG_RXP_C13 AL20
- PEG_RXP_C14 AL21
- PEG_RXP_C15 AM21
- PEG_RXN_C0 AM15
- PEG_RXN_C1 AM16
- PEG_RXN_C2 AK16
- PEG_RXN_C3 AK17
- PEG_RXN_C4 AL17
- PEG_RXN_C5 AL18
- PEG_RXN_C6 AM18
- PEG_RXN_C7 AM19
- PEG_RXN_C8 AK19
- PEG_RXN_C9 AK20
- PEG_RXN_C10 AL20
- PEG_RXN_C11 AL21
- PEG_RXN_C12 AK21
- PEG_RXN_C13 AL22
- PEG_RXN_C14 AM22
- PEG_RXN_C15 AL23



NV_GF-GO6600-N-AX (G73M)

MULTI-USE I/O INTERFACE





TVMODE (NV43M/G7X)
NTSC (01)

MIOAD10	MIOAD7	TVMODE
0	0	SECAM
0	1	NTSC
1	0	PAL
1	1	CRT

TXN[0..15] 17
Strap for GDDR3-136ball
0001 16Mx32Infineon
0010 16Mx32Hynix
0011 16Mx32Samsung

0101 8Mx32Infineon
0110 8Mx32Hynix
0111 8Mx32Samsung

SUBVENDOR
0 (USE SYSTEM BIOS)
1 (USE EXTERNAL ROM)

MIOAD0 is used to set the PCI Express PLL termination enable.
DEFAULT "0"

3GIO_PADCFG[2:0]
001 for NV43/NV44
010 for G7X/NV42

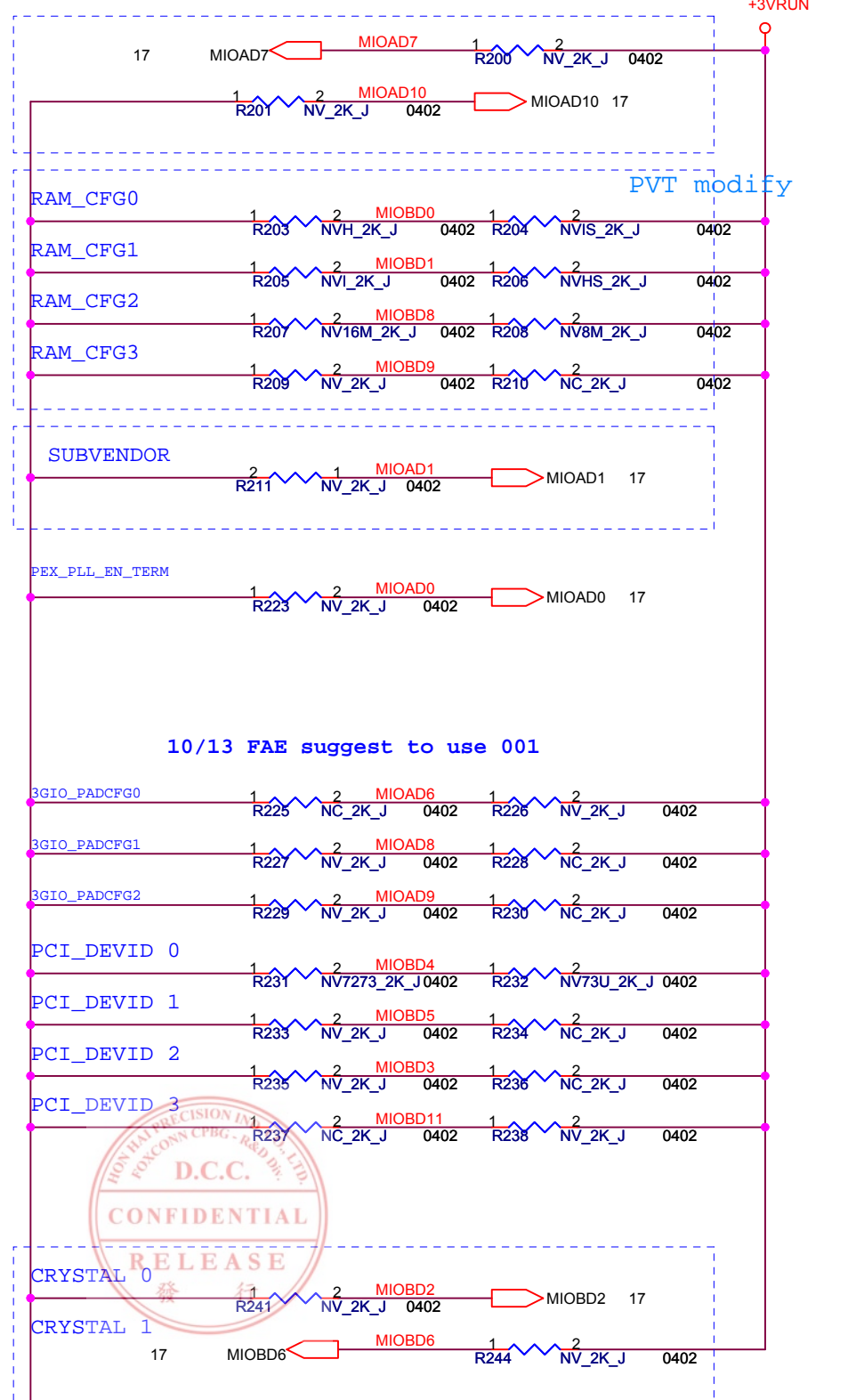
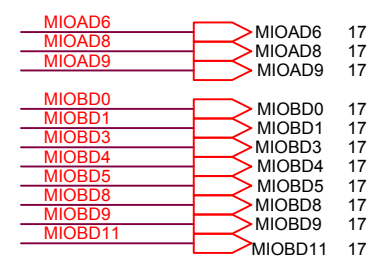
G72M/G73M/NV43M
PCI_DEVID[3:0]="1000"-->8
G73M-U
PCI_DEVID[3:0]="1001"-->9

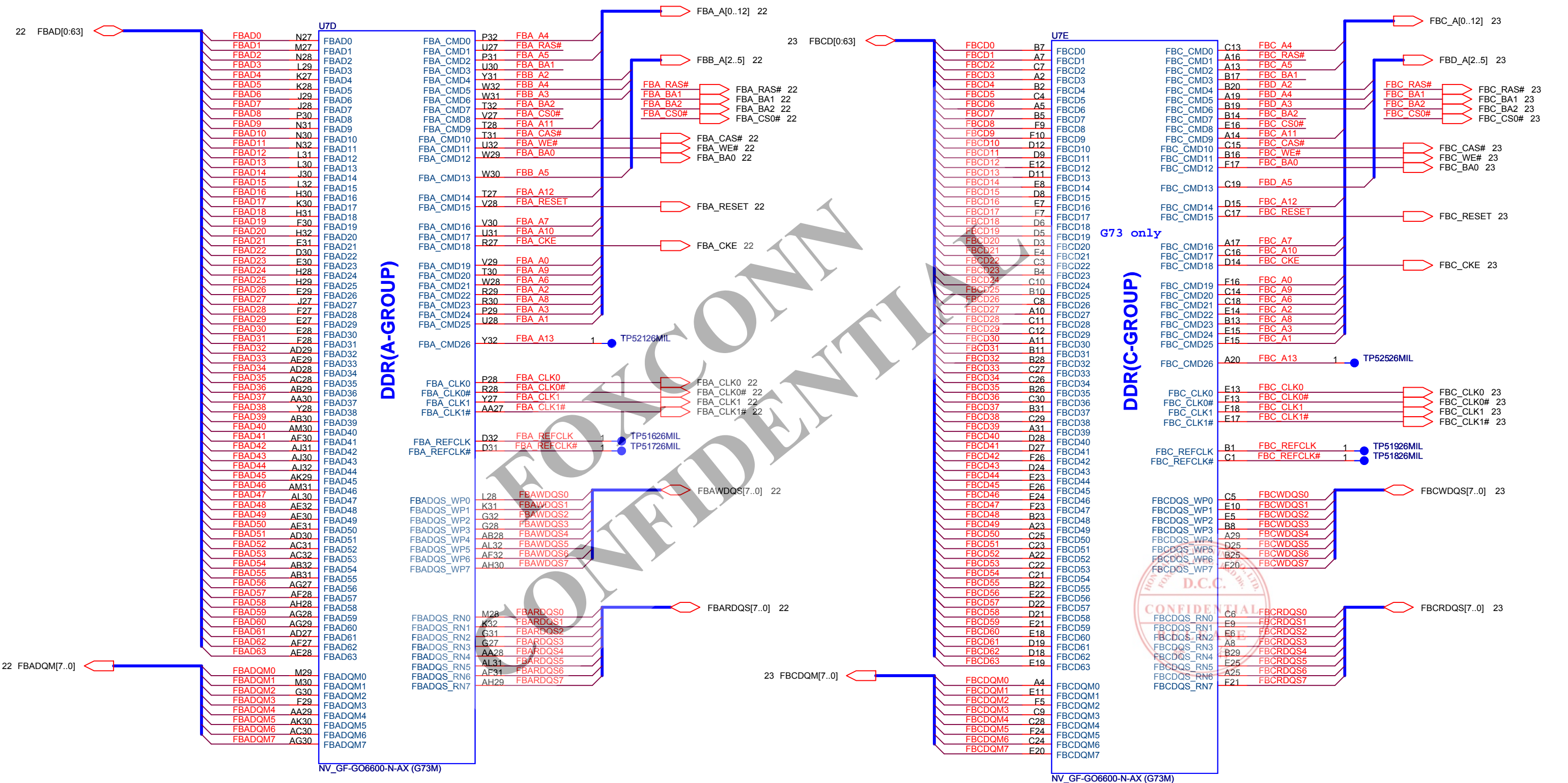
CRYSTAL (NV43M/G7X)
10 (27M Hz)

MIOBD6	MIOBD2	Crystal
1	0	27MHz
0	1	14.318MHz
0	0	13.5MHz
1	1	Preserved

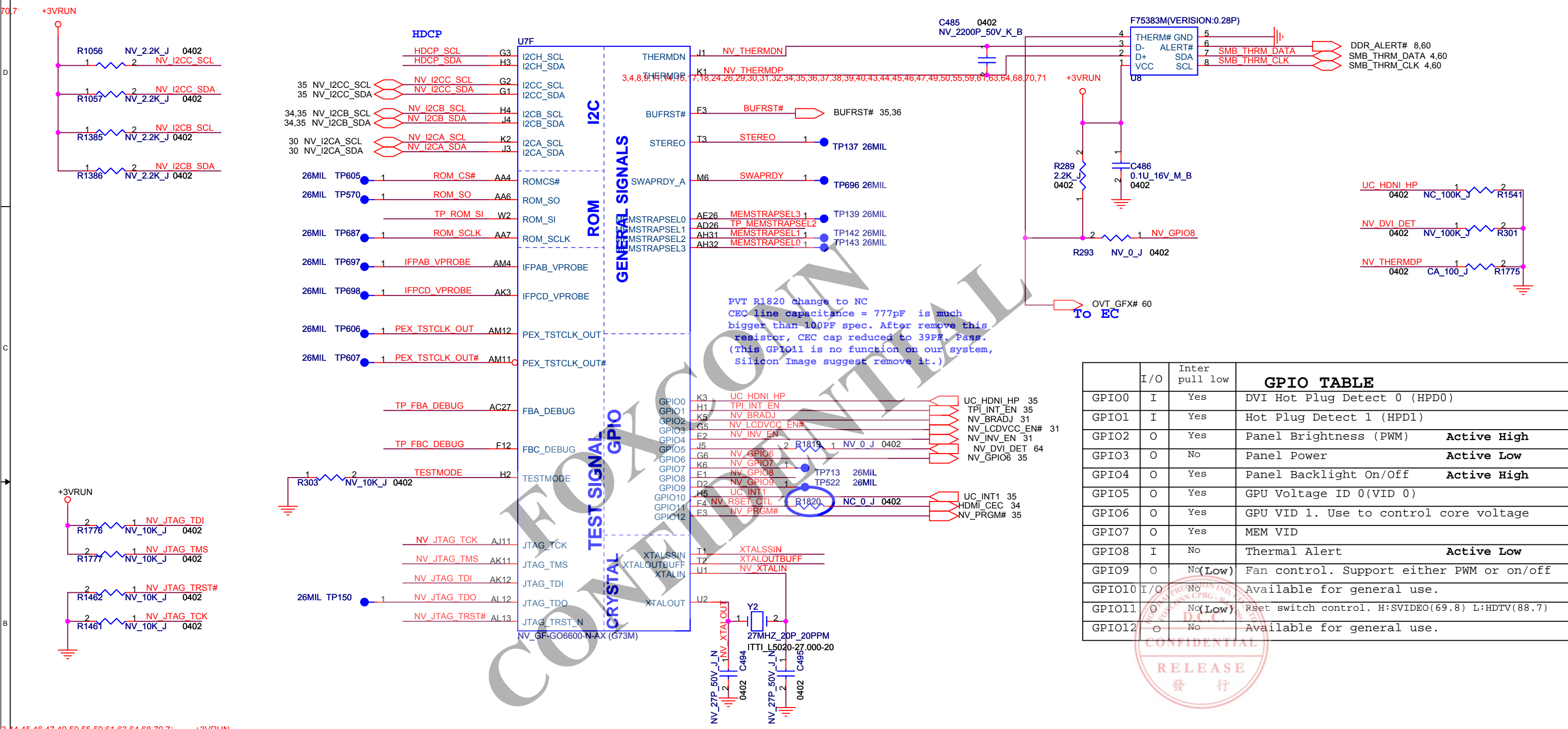
ROM_TYPE (NV43M/G7X) NC
MIOBD10, MIOBD_HSYNC

00 PARALLEL
01 SERIAL_AT25F
10 SERIAL_SST45VF
11 LPC





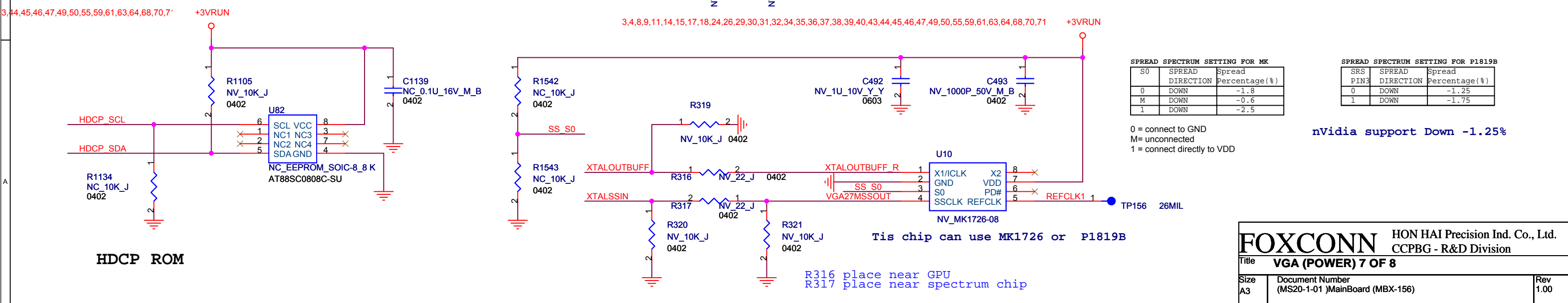
SM bus Address :
1001100(EC)
For F75383M



PVT R1820 change to NC
CEC line capacitance = 777pF is much
bigger than 100PF spec. After remove this
resistor, CEC cap reduced to 39PF. Pass.
(This GPIO11 is no function on our system,
Silicon Image suggest remove it.)

OVT_GFX# 60
To EC

	I/O	Inter pull low	GPIO TABLE
GPIO0	I	Yes	DVI Hot Plug Detect 0 (HPD0)
GPIO1	I	Yes	Hot Plug Detect 1 (HPD1)
GPIO2	O	Yes	Panel Brightness (PWM) Active High
GPIO3	O	No	Panel Power Active Low
GPIO4	O	Yes	Panel Backlight On/Off Active High
GPIO5	O	Yes	GPU Voltage ID 0(VID 0)
GPIO6	O	Yes	GPU VID 1. Use to control core voltage
GPIO7	O	Yes	MEM VID
GPIO8	I	No	Thermal Alert Active Low
GPIO9	O	No(Low)	Fan control. Support either PWM or on/off
GPIO10	I/O	No	Available for general use.
GPIO11	O	No(Low)	Rset switch control. H:SVIDEO(69.8) L:HDTV(88.7)
GPIO12	O	No	Available for general use.



SPREAD SPECTRUM SETTING FOR MK

S0	SPREAD DIRECTION	Spread Percentage(%)
0	DOWN	-1.8
M	DOWN	-0.6
1	DOWN	-2.5

SPREAD SPECTRUM SETTING FOR P1819B

SRS PIN3	SPREAD DIRECTION	Spread Percentage(%)
0	DOWN	-1.25
1	DOWN	-1.75

0 = connect to GND
M = unconnected
1 = connect directly to VDD

nVidia support Down -1.25%

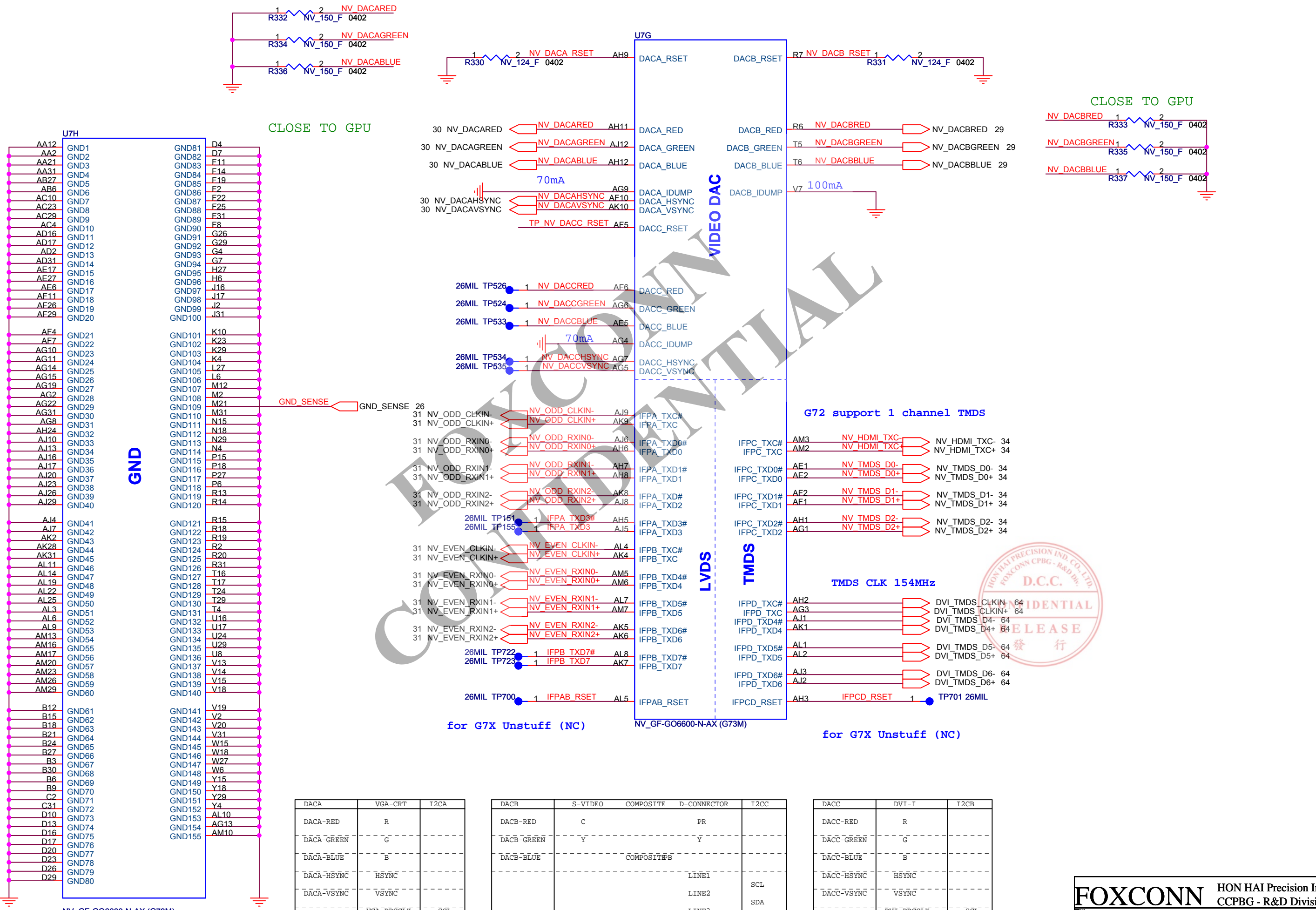
Tis chip can use MK1726 or P1819B

R316 place near GPU
R317 place near spectrum chip

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title **VGA (POWER) 7 OF 8**

Size A3	Document Number (MS20-1-01)MainBoard (MBX-156)	Rev 1.00
Date: Friday, April 14, 2006	Sheet 20 of 80	



DACA	VGA-CRT	I2CA
DACA-RED	R	
DACA-GREEN	G	
DACA-BLUE	B	
DACA-HSYNC	HSYNC	
DACA-VSYNC	VSYNC	
	VGA-DDCLK	SCL
	VGA-DDCDA	SDA

DACB	S-VIDEO	COMPOSITE	D-CONNECTOR	I2CC
DACB-RED	C		PR	
DACB-GREEN	Y		Y	
DACB-BLUE		COMPOSITE		
			LINE1	SCL
			LINE2	SDA
			LINE3	

DACC	DVI-I	I2CB
DACC-RED	R	
DACC-GREEN	G	
DACC-BLUE	B	
DACC-HSYNC	HSYNC	
DACC-VSYNC	VSYNC	
	DVI-DDCLK	SCL
	DVI-DDCDA	SDA

CONFIDENTIAL

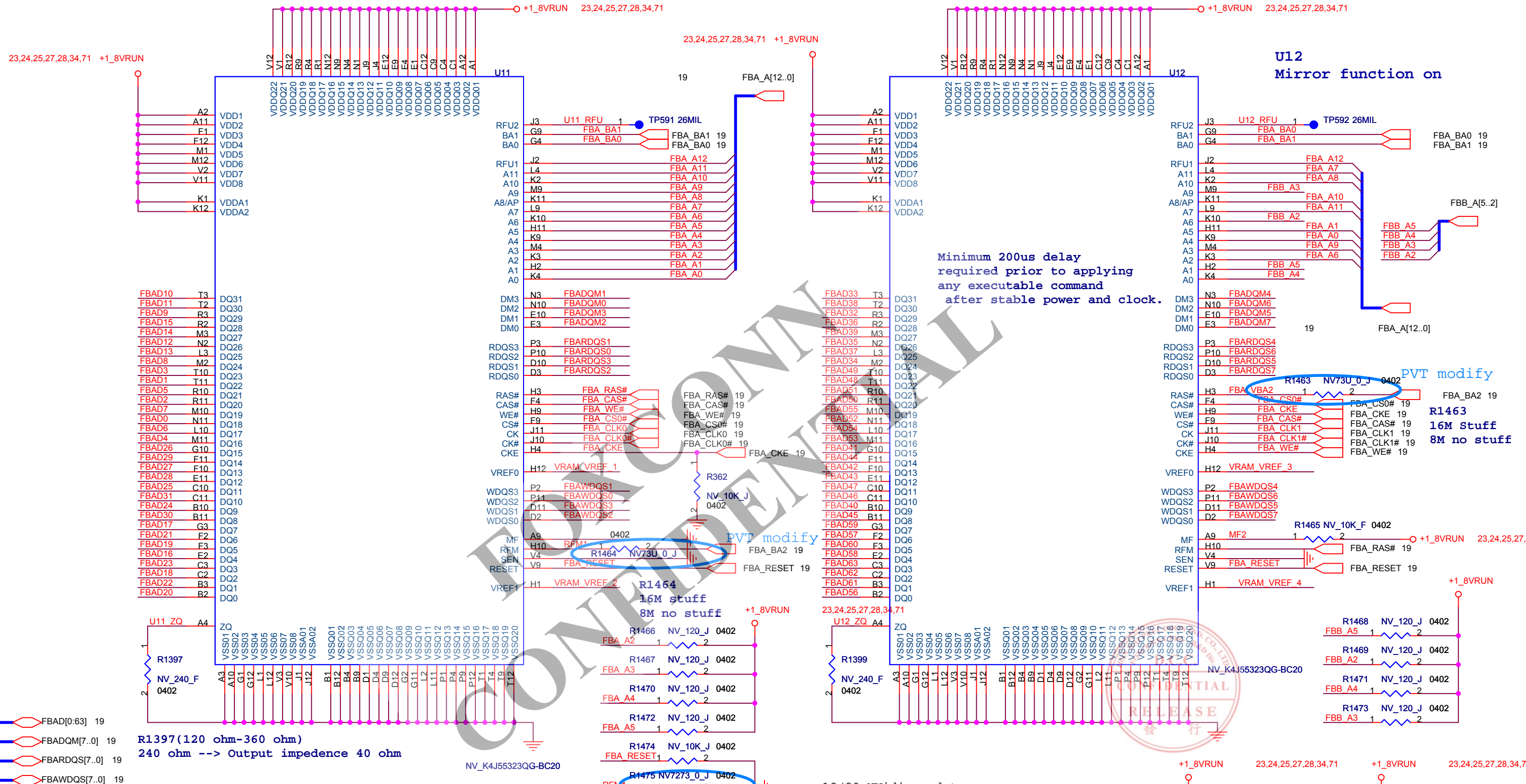
HON HAI Precision Ind. Co., Ltd.
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FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: **VGA (POWER) 8 OF 8**

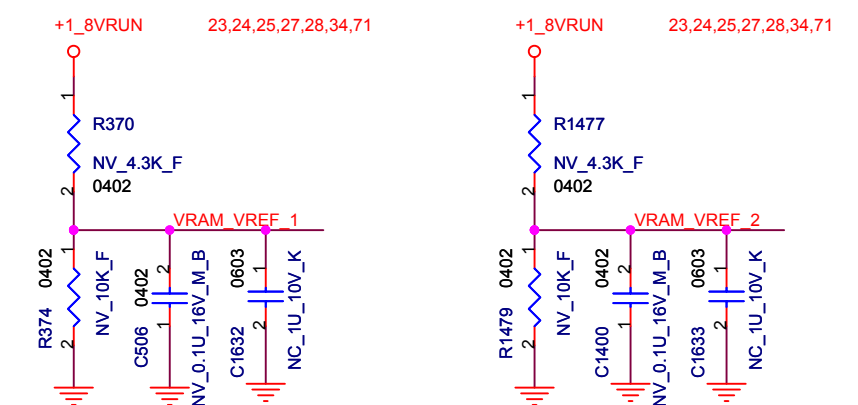
Size: A3	Document Number: (MS20-1-01) MainBoard (MBX-156)	Rev: 1.00
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Date: Friday, April 14, 2006 | Sheet 21 of 80



R1397(120 ohm-360 ohm)
 240 ohm --> Output impedance 40 ohm

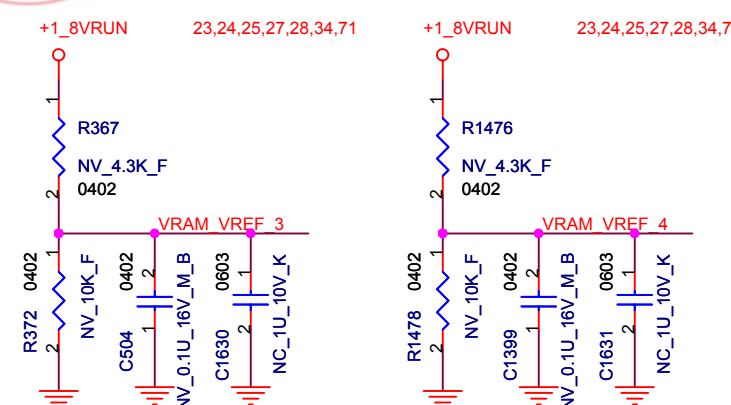
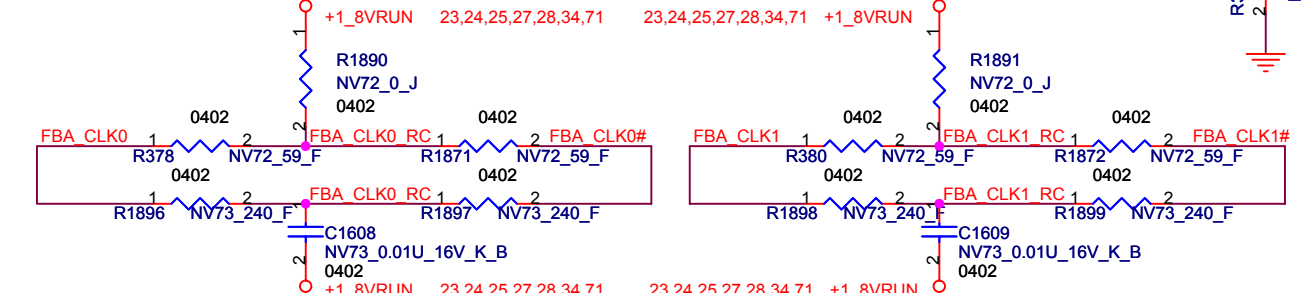
VRAM_VREF is 70%FBVDDQ for GDDR3 1.26V

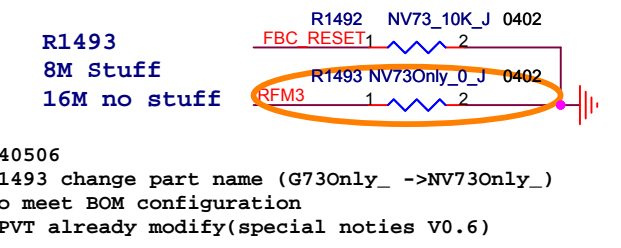
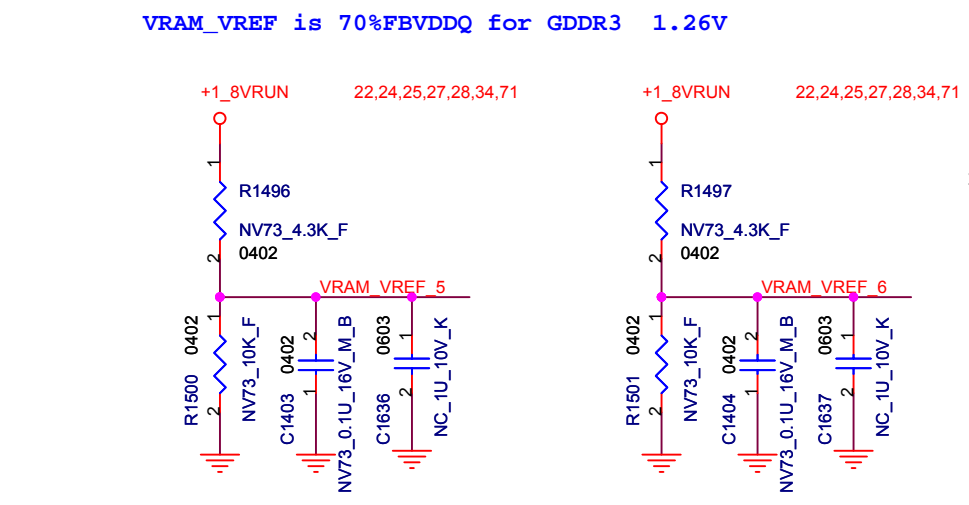
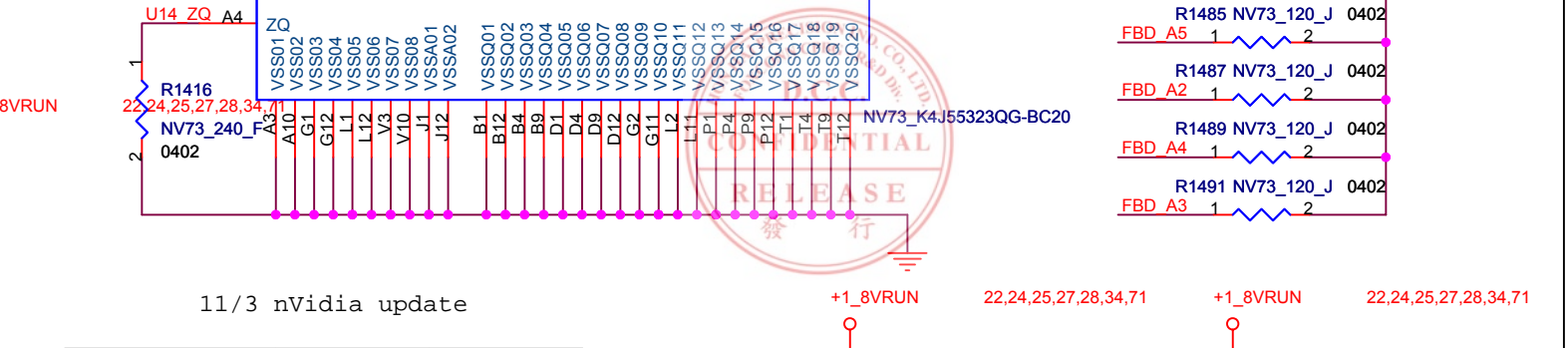
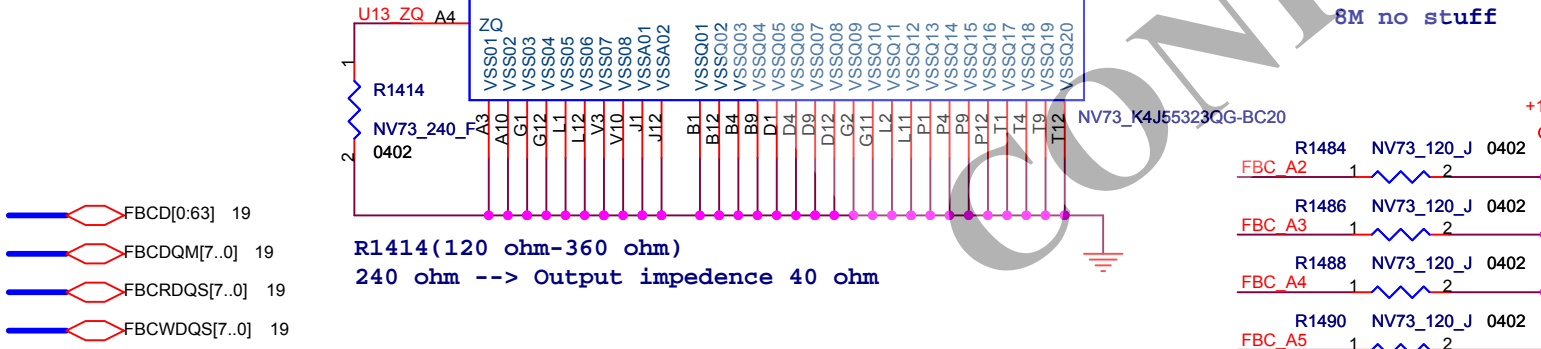
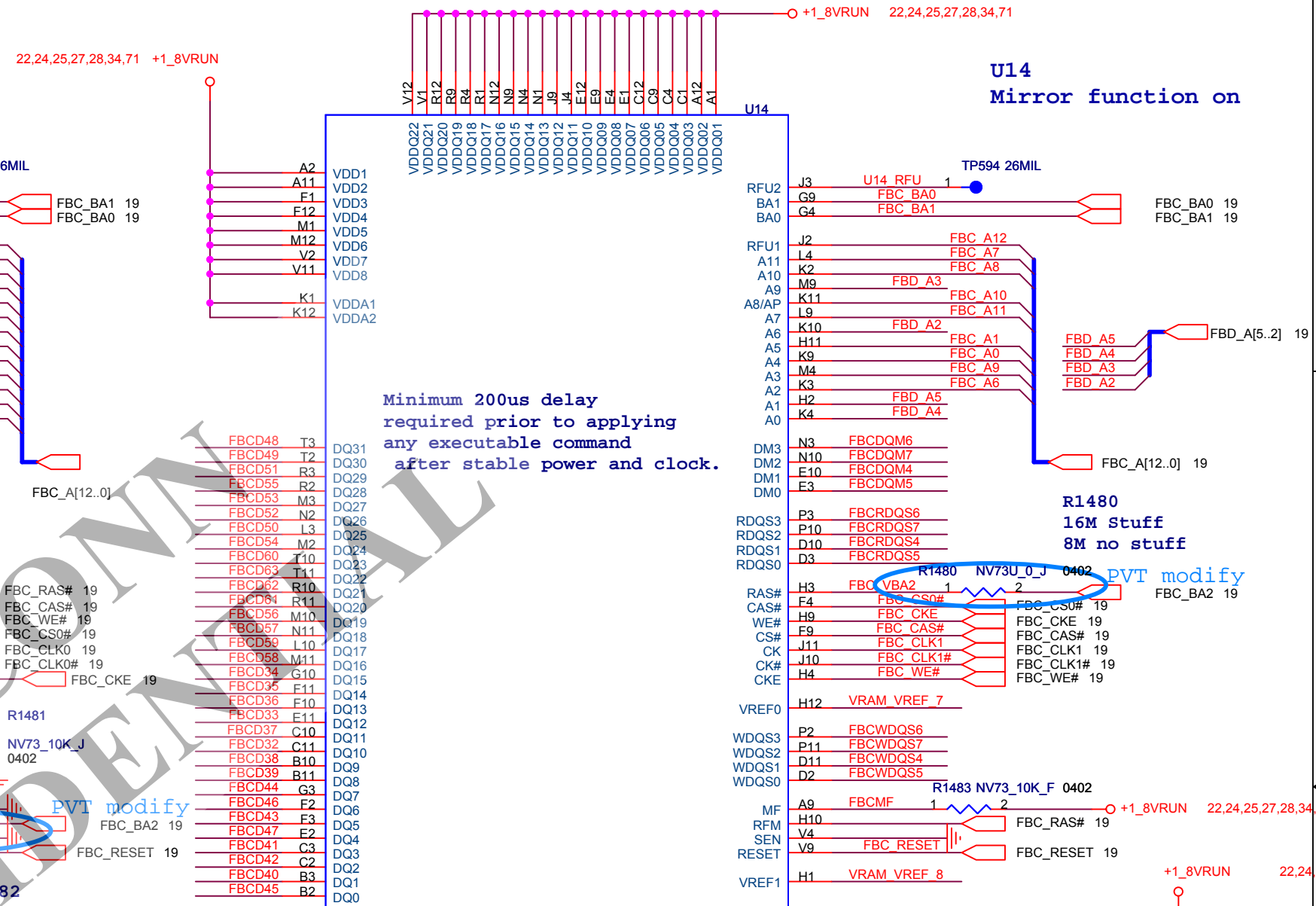
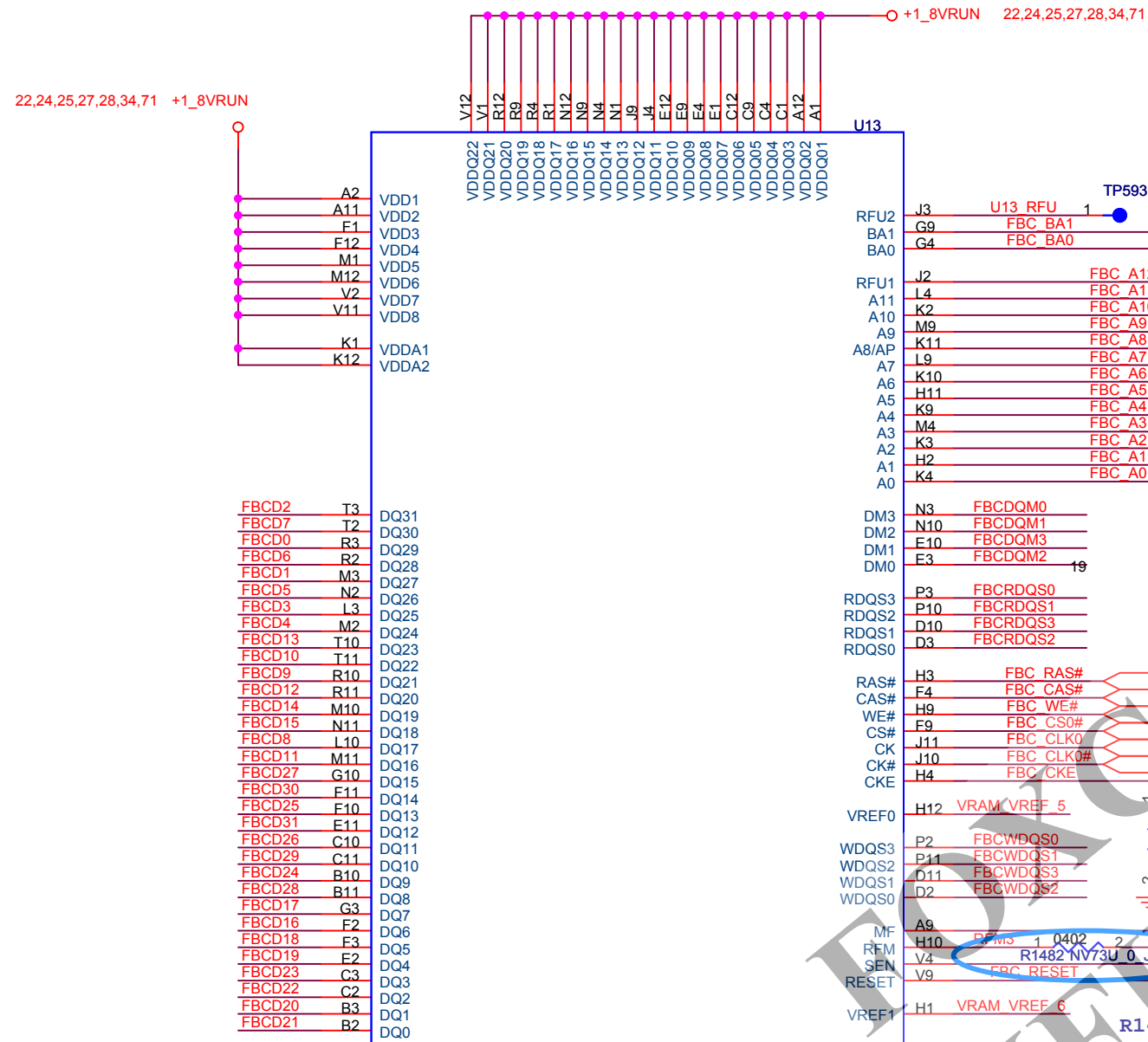


PVT modify R1475
 8M Stuff
 16M no stuff

FAE suggestion on 10/26
 Close to VRAM

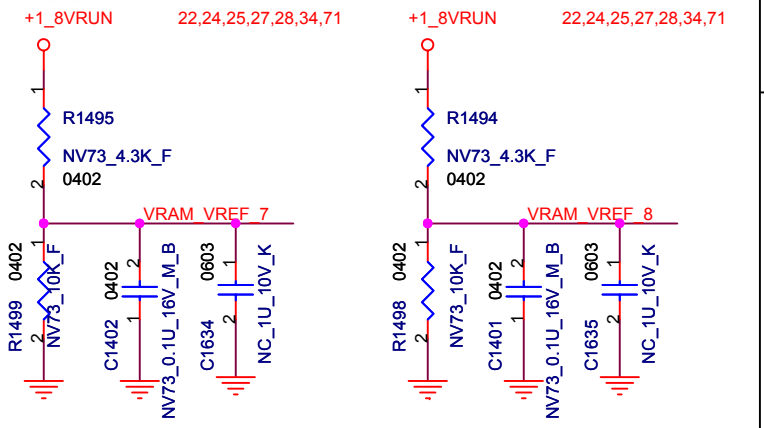
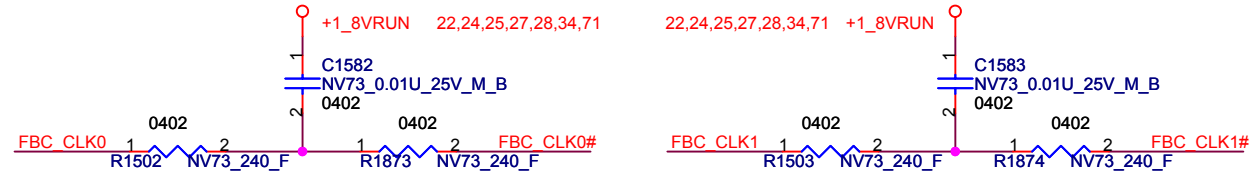
	DDR3 (G72M)	DDR3 (G73M)
R378,R380 R1871,R1872	60 ohm	240 ohm
R,C 1890 R,C 1891	0 ohm	0.01uF

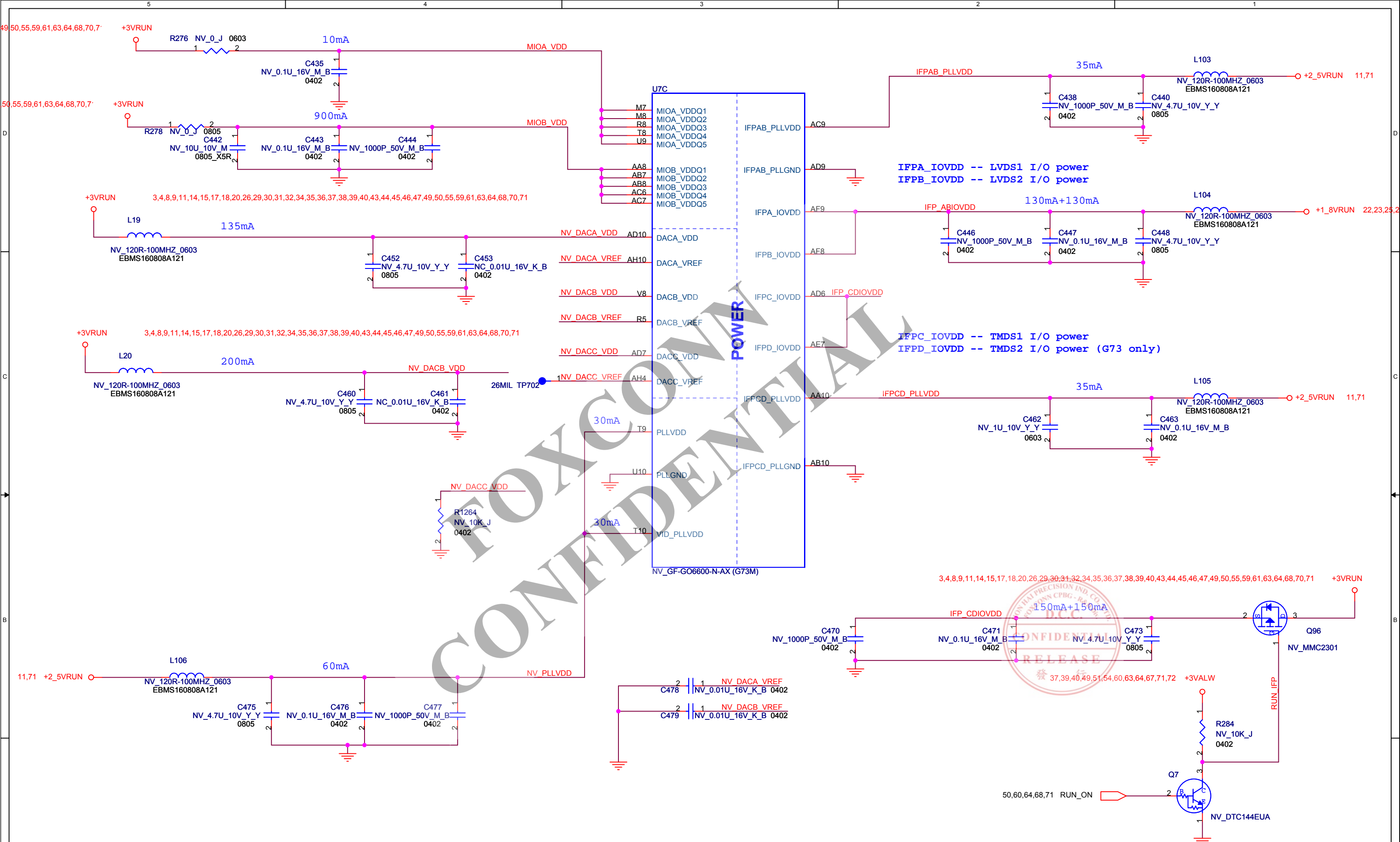




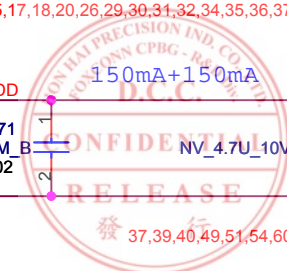
11/3 nVidia update

	DDR3 (G72M)	DDR3 (G73M)
R1502, R1873	40 ohm	240 ohm
R1503, R1874	40 ohm	240 ohm
C1582, C1583	0 ohm	0.01uF



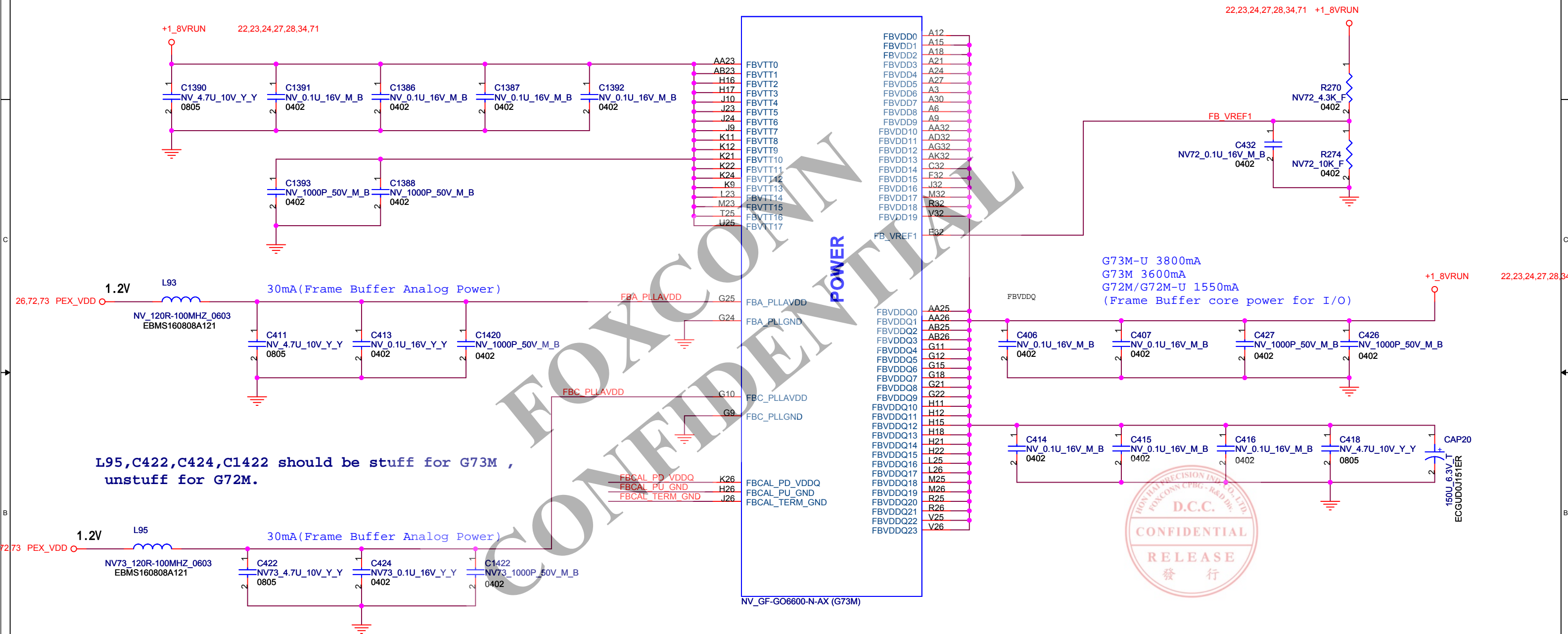


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For GDDR3 FBVTT require decoupling capacitor,FBVDD don't require them.

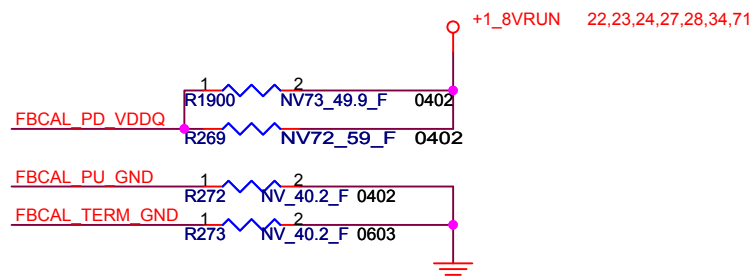
U71



L95,C422,C424,C1422 should be stuff for G73M , unstuff for G72M.

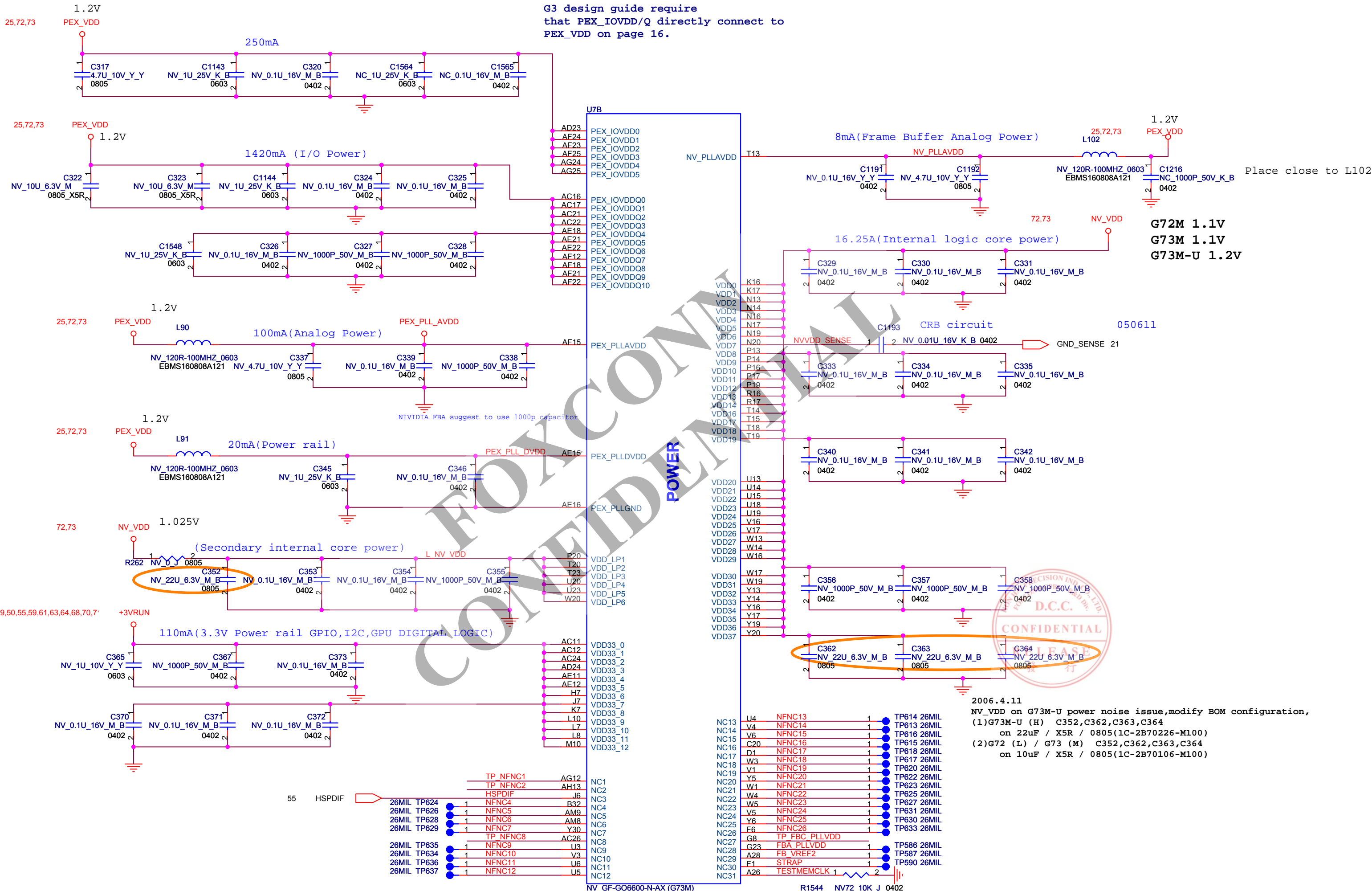


11/3 nVidia update

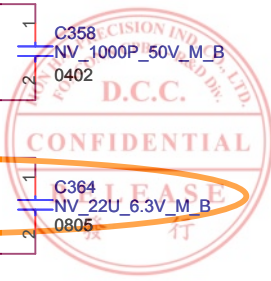


	DDR1	DDR3 (G72M)	DDR3 (G73M)
FBCAL_PD_VDDQ	40 ohm	60 ohm	50 ohm
FBCAL_PU_GND	30 ohm	40 ohm	40 ohm
FBCAL_TERM_GND	NC	40 ohm	40 ohm

G3 design guide require that PEX_IOVDD/Q directly connect to PEX_VDD on page 16.



Place close to L102
G72M 1.1V
G73M 1.1V
G73M-U 1.2V



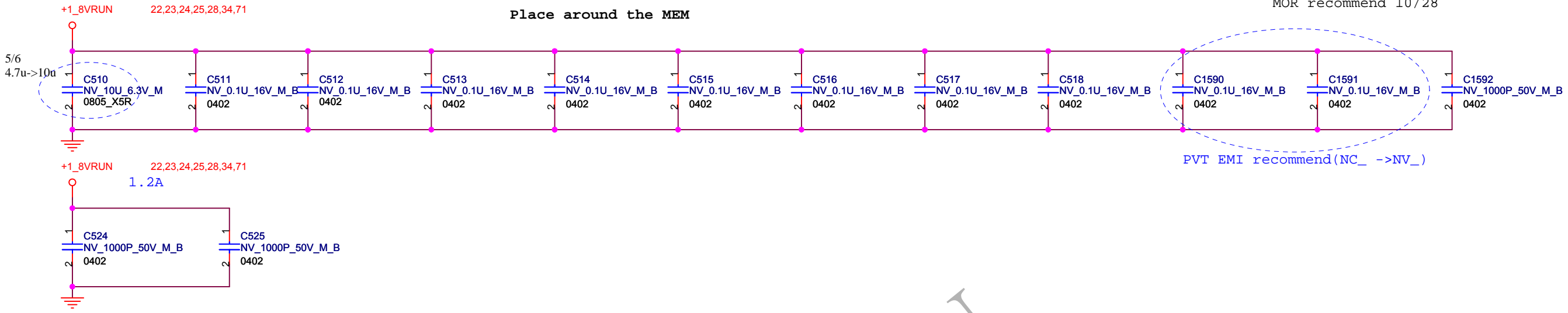
2006.4.11
 NV_VDD on G73M-U power noise issue, modify BOM configuration,
 (1)G73M-U (H) C352, C362, C363, C364
 on 22uF / X5R / 0805(1C-2B70226-M100)
 (2)G72 (L) / G73 (M) C352, C362, C363, C364
 on 10uF / X5R / 0805(1C-2B70106-M100)

G73M Pin A26-NC
G72M Pin A26 need stuff R305 10K

Decoupling for Tright MEMORY

Place around the MEM

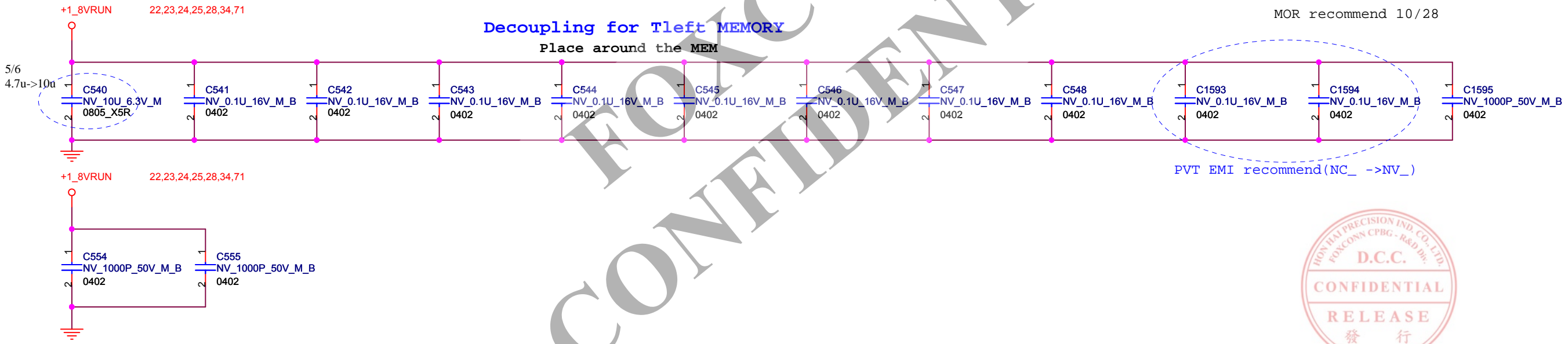
MOR recommend 10/28



Decoupling for Tleft MEMORY

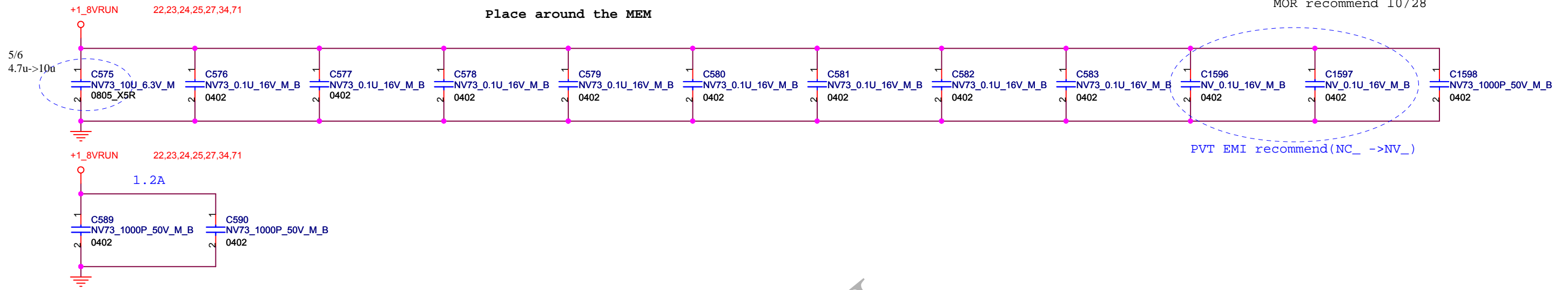
Place around the MEM

MOR recommend 10/28



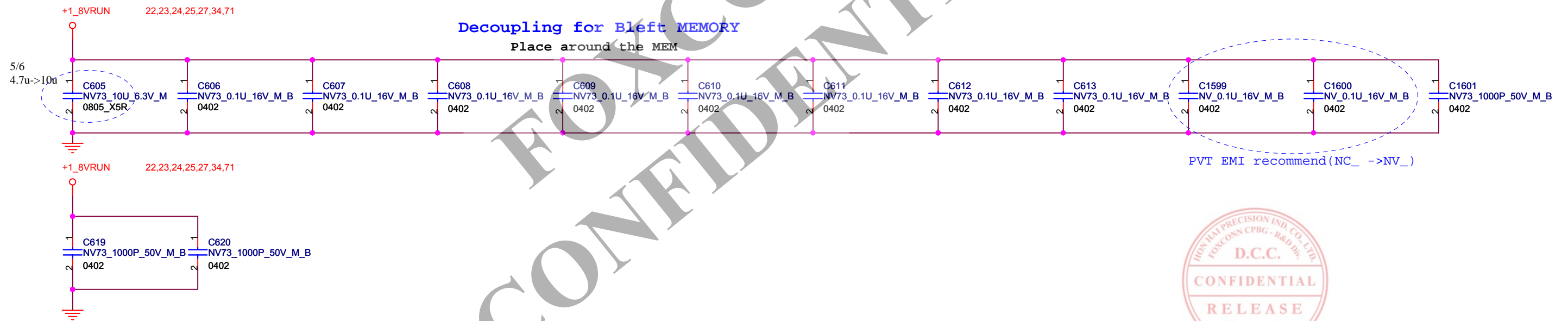
Decoupling for Bright MEMORY

MOR recommend 10/28



Decoupling for Bleft MEMORY

Place around the MEM

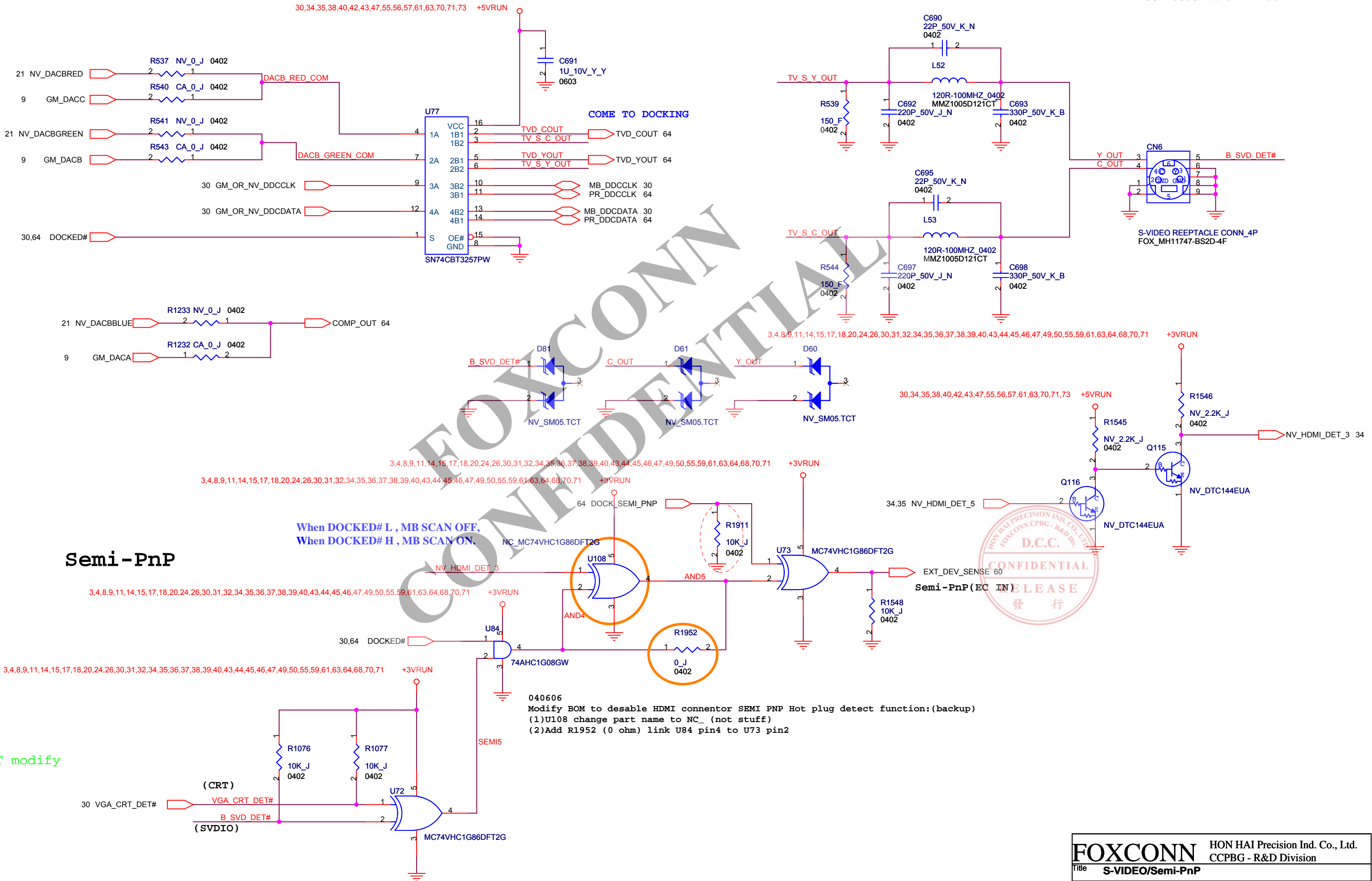


S-VIDEO ANALOG SWITCH

S-VIDEO

H : S-VIDEO&CVBS
L : PORT REPLICATOR

These component close to S-Video connector within 700 mil

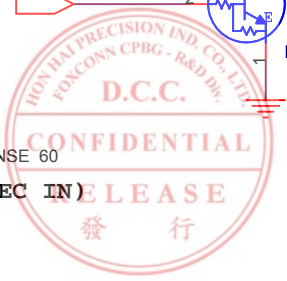


Semi-PnP

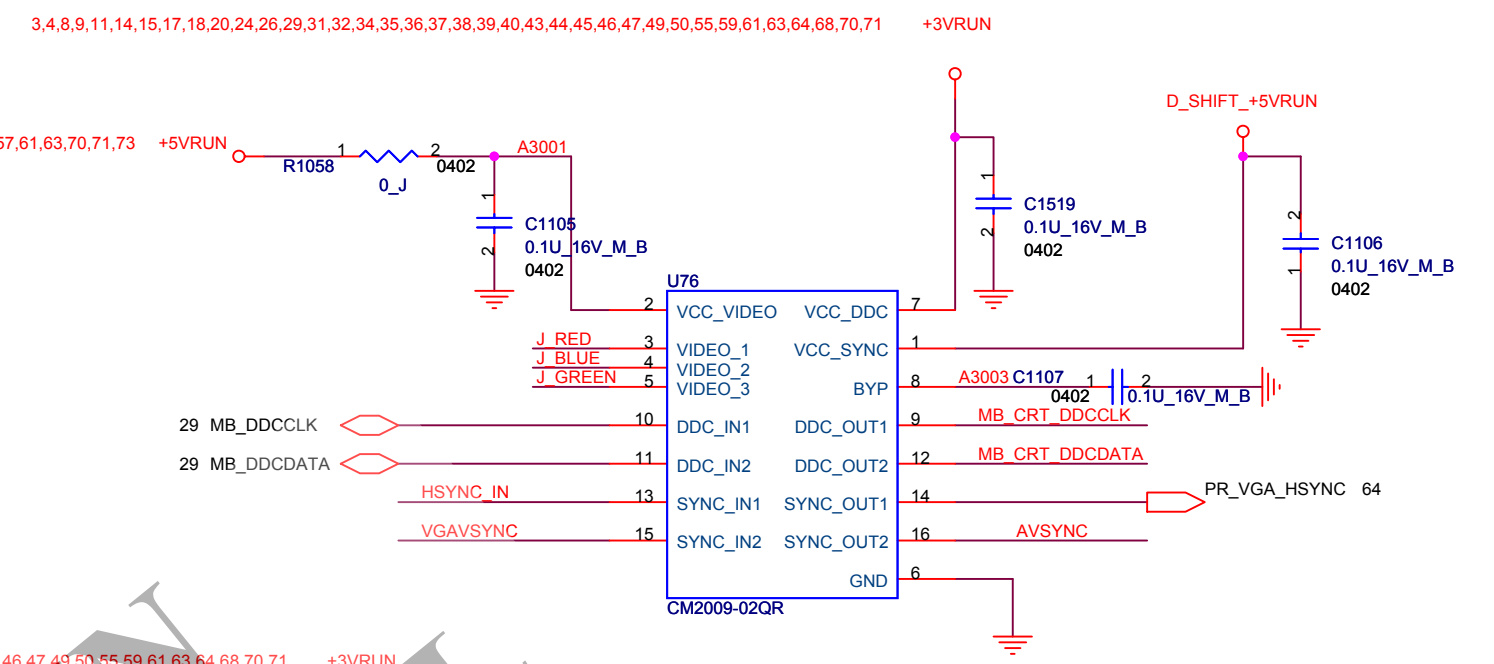
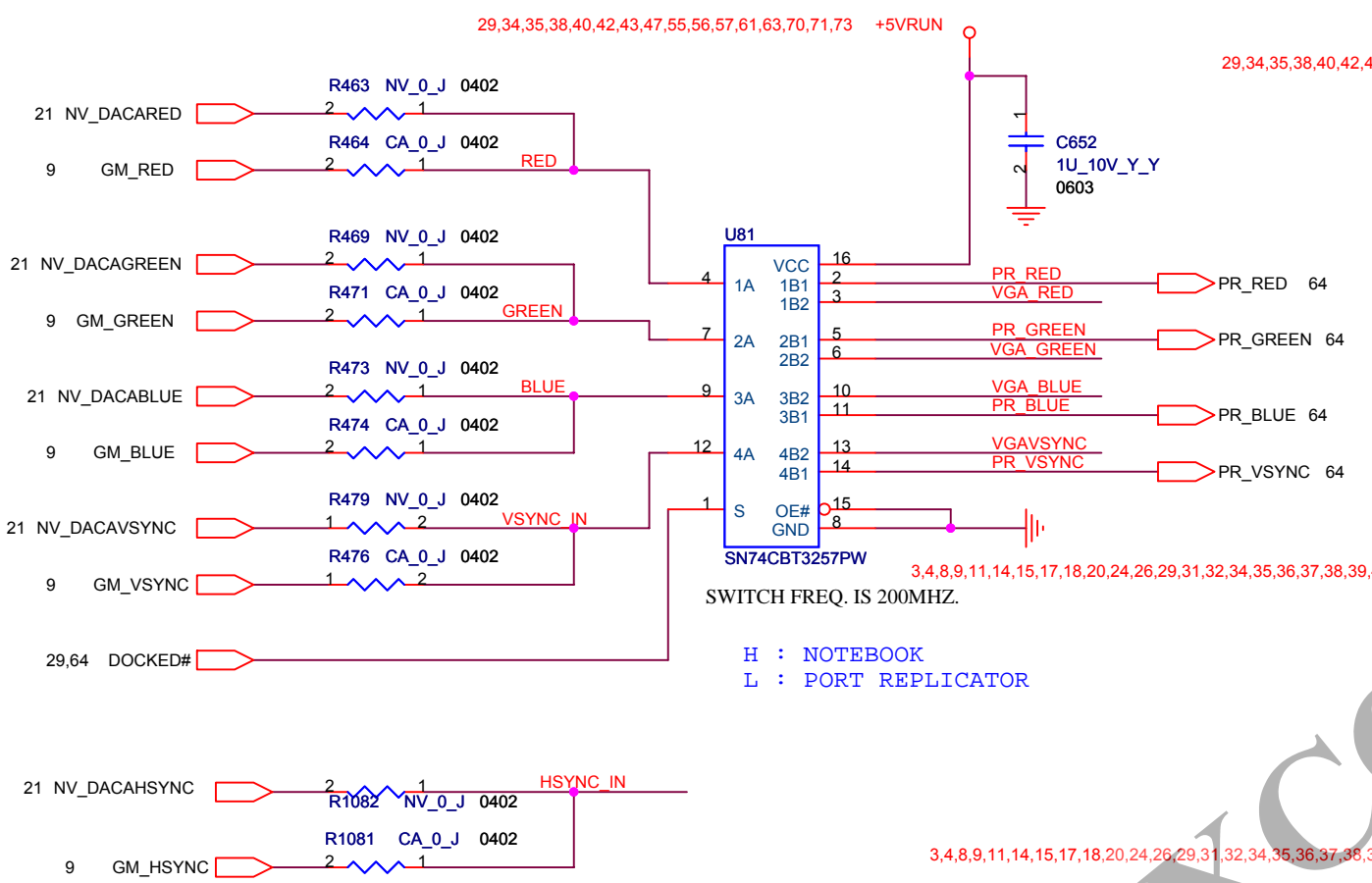
When DOCKED# L, MB SCAN OFF,
When DOCKED# H, MB SCAN ON.

040606
Modify BOM to disable HDMI connector SEMI PNP Hot plug detect function:(backup)
(1)U108 change part name to NC_ (not stuff)
(2)Add R1952 (0 ohm) link U84 pin4 to U73 pin2

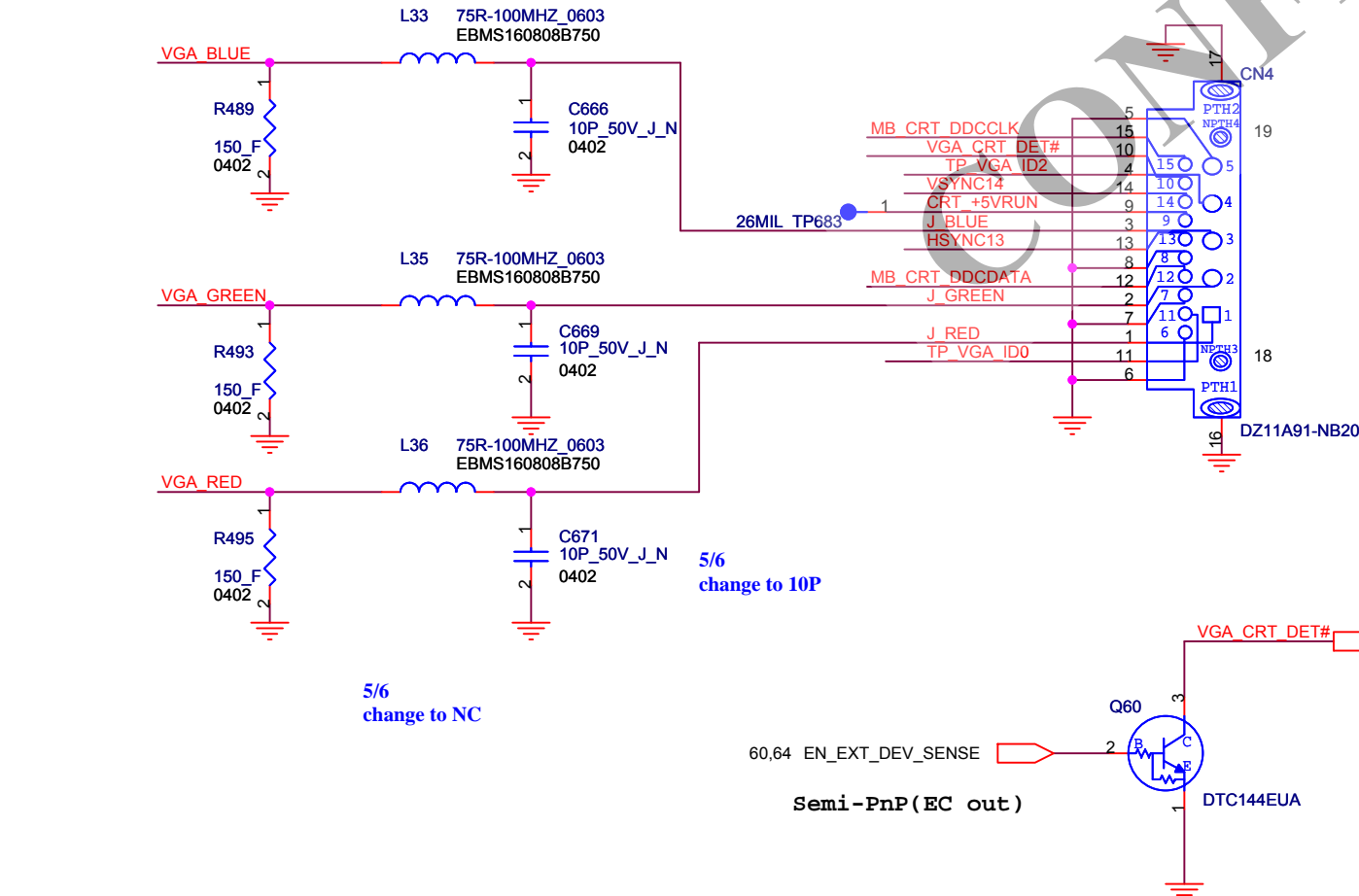
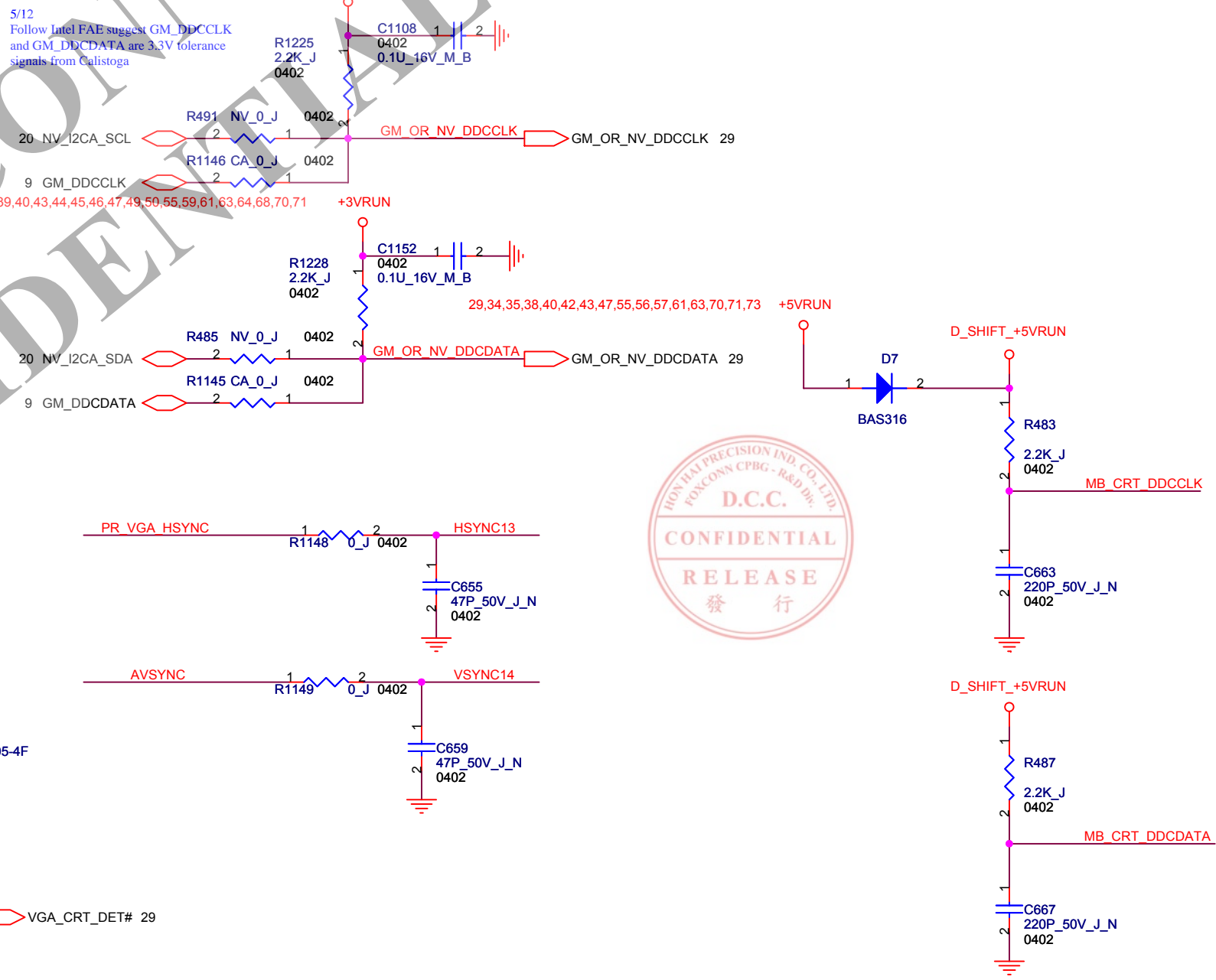
DVT modify



CRT ANALOG SWITCH



CRT CONNECTOR

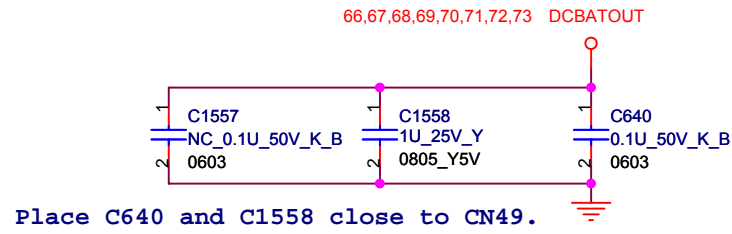
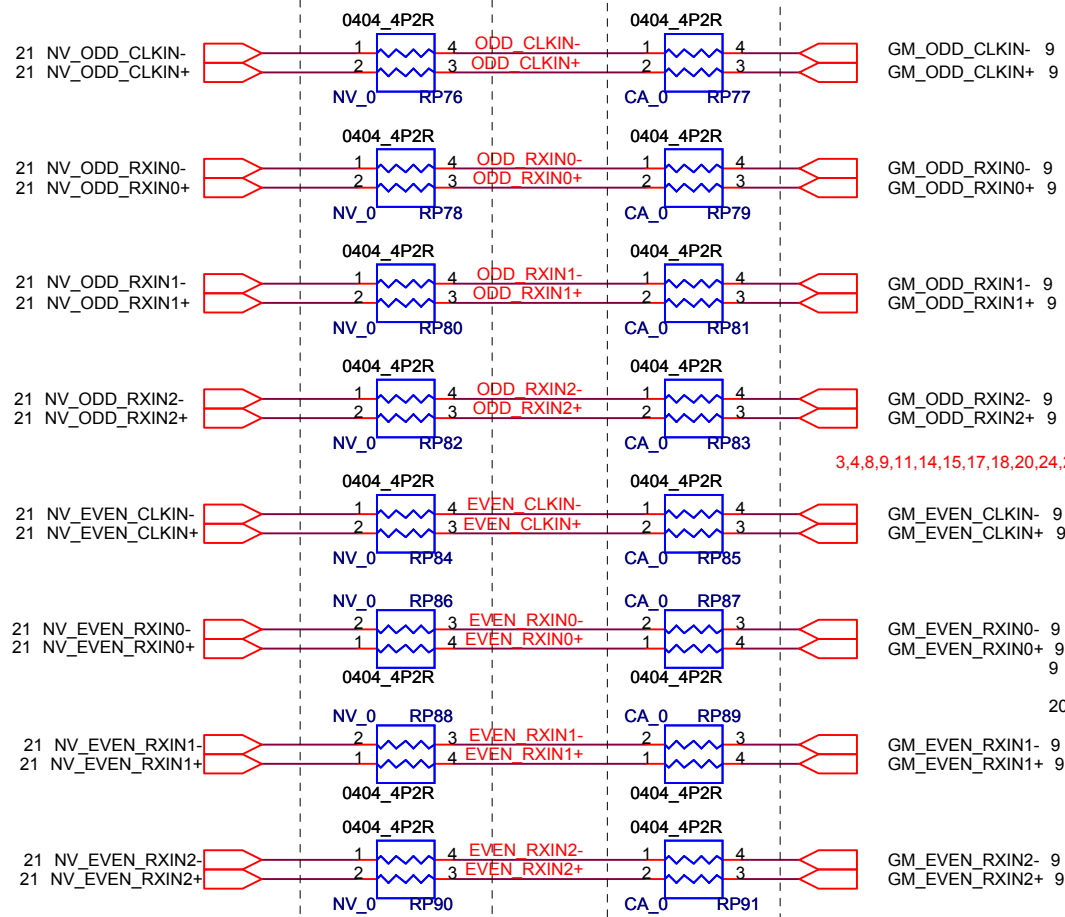


FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	CRT	
Size	Document Number (MS20-1-01)MainBoard (MBX-156)	Rev 1.00
Date:	Friday, April 14, 2006	Sheet 30 of 80

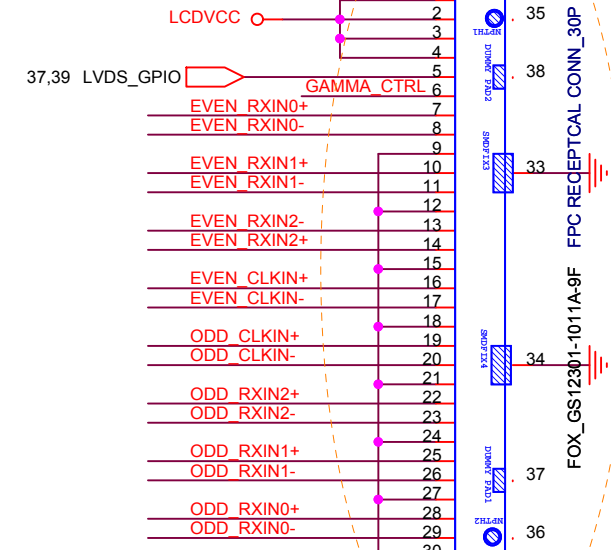
LVDS

Group1

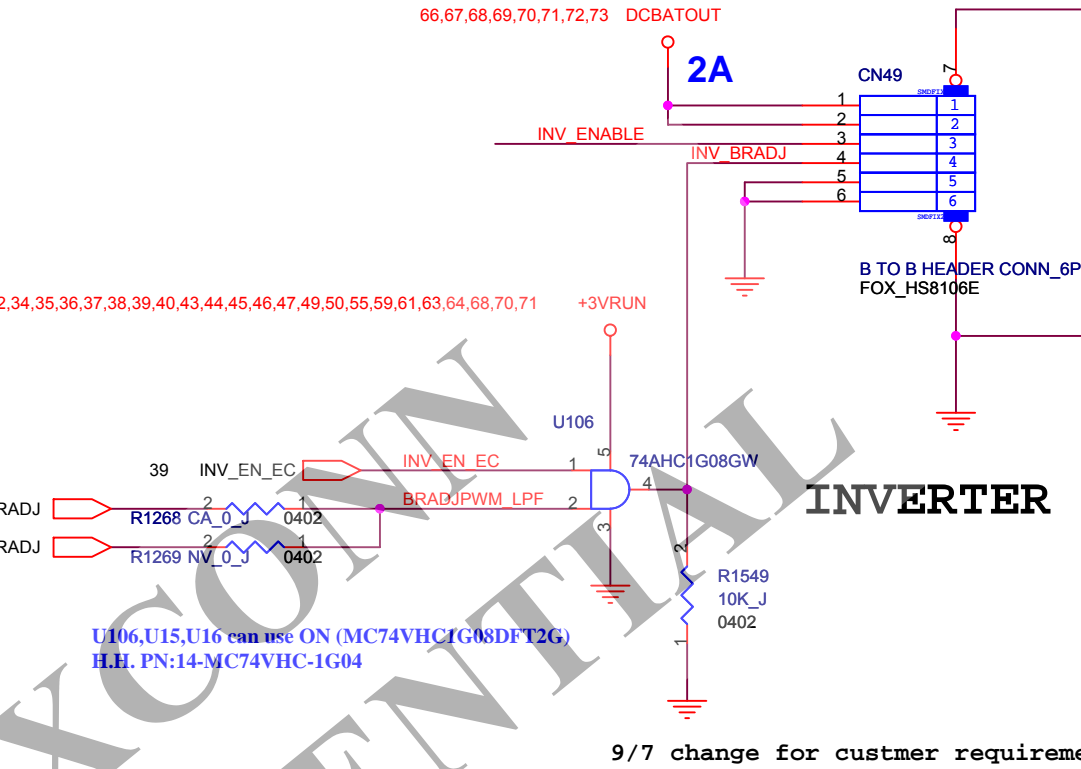
Group2



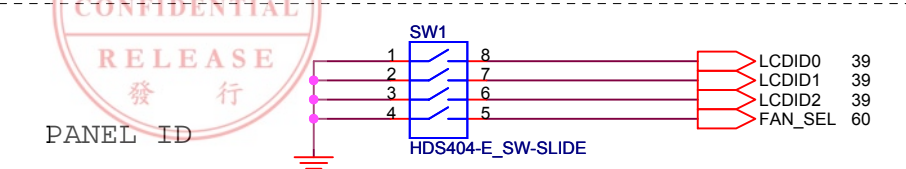
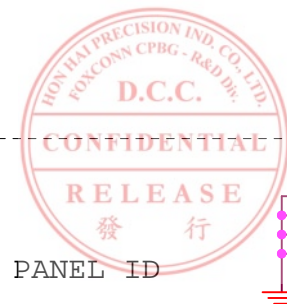
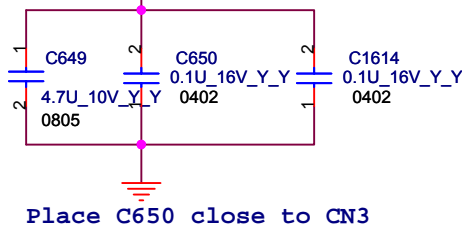
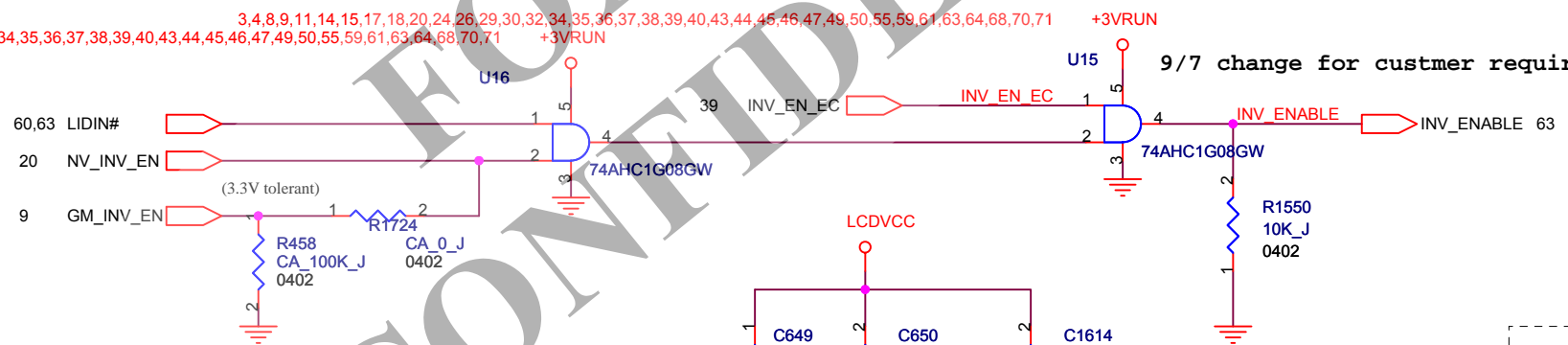
LVDS CONNECTOR



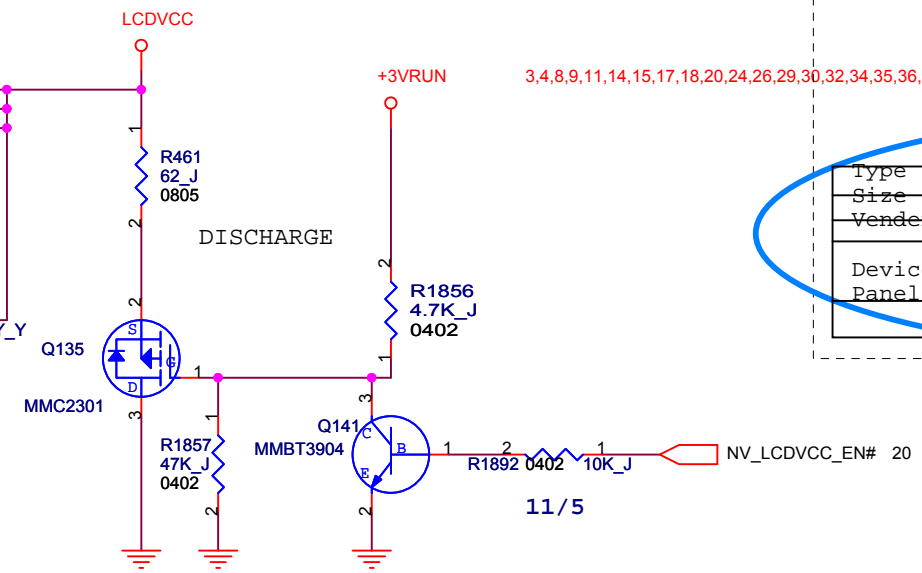
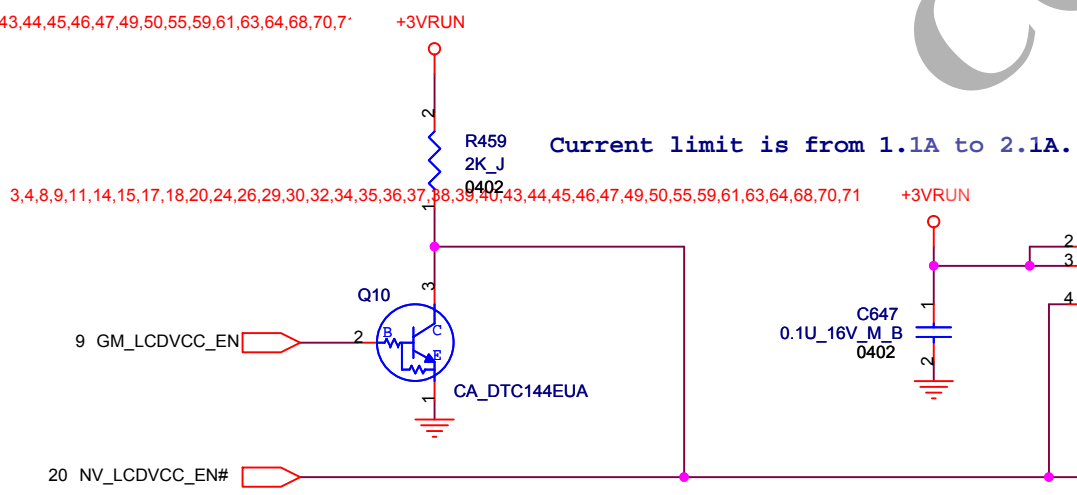
2006.3.13
CN3 update OrCAN symbol



INVERTER CONNECTOR

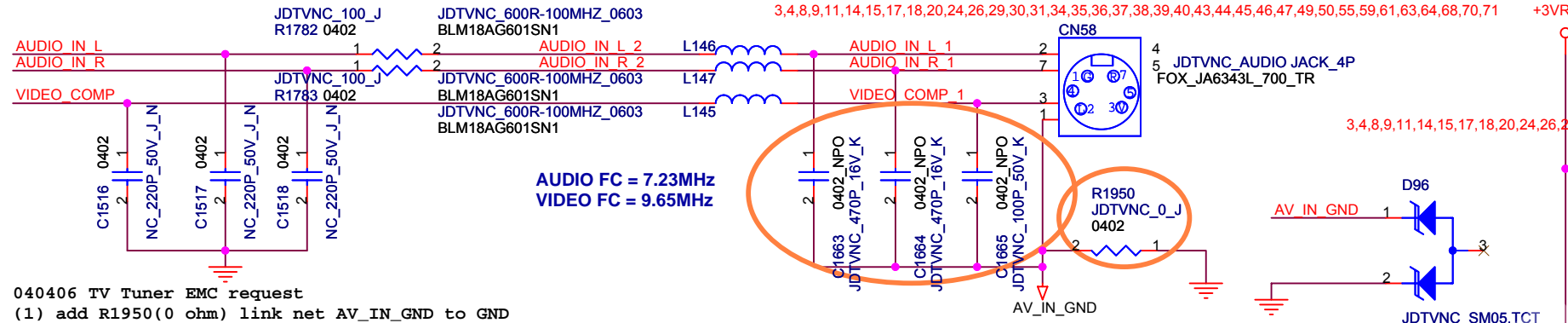


FAN_SEL:
 H: Foxconn FAN
 L: MOR cooling unit



Type	WXGA+	WXGA	WUXGA
Size	17" wide	17" wide	17" wide
Vendor	LG-PHILIPS	LG-PHILIPS	SHARP
Device Name	LP171WP7-TLA1	LP171WX2-A4R3	LQ170M1LA04
Panel ID Check[3...0]	0001	0010	0100

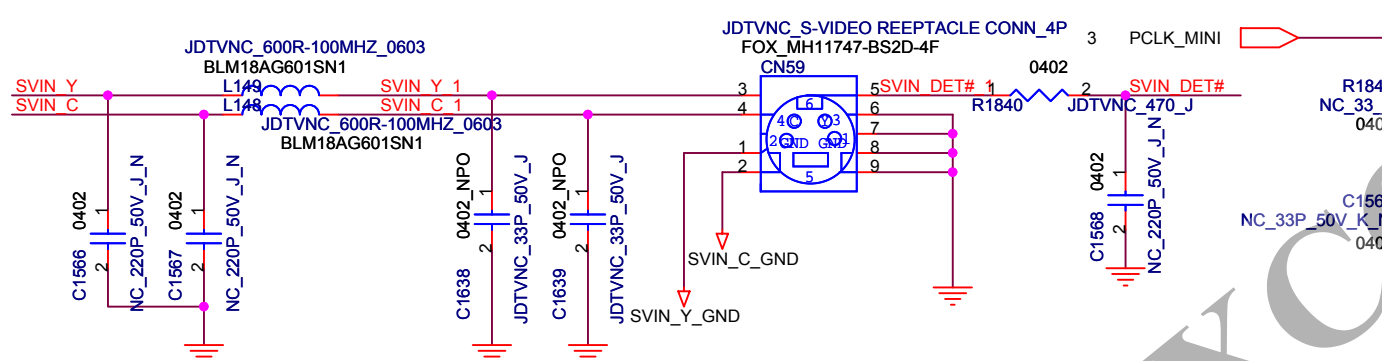
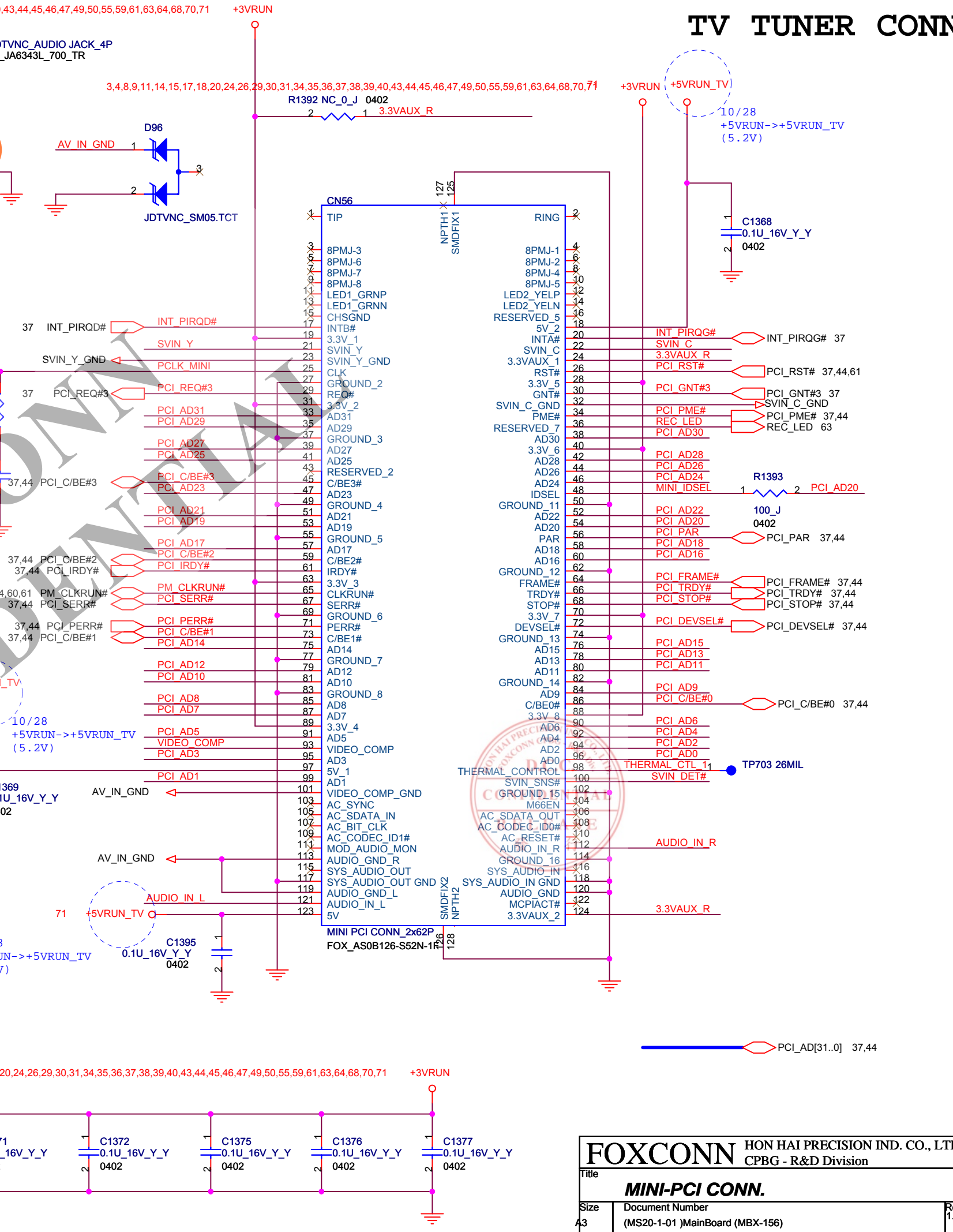
Special mini stereo jack



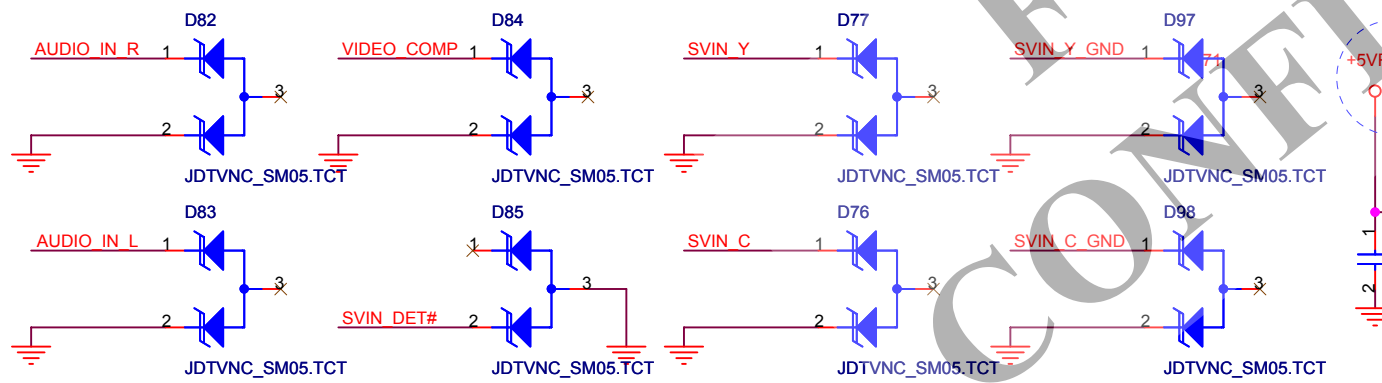
- 040406 TV Tuner EMC request
- (1) add R1950(0 ohm) link net AV_IN_GND to GND
 - (2) add C1663(470pF) link net AUDIO_IN_L_1 to AV_IN_GND
 - (3) add C1664(470pF) link net AUDIO_IN_R_1 to AV_IN_GND
 - (4) add C1665(100pF) link net VIDEO_COMP_1 to AV_IN_GND

- 040406 Modify BOM roul
- (1) Mini PCI socket circuit group change part name from TV_ to normal.
 - (2) Special mini stereo jack and S-VIDEO in group change part name from TV_ to JDTVNC_ (JP digital tuner sku & No tuner SKU NOT stuff)

TV TUNER CONN

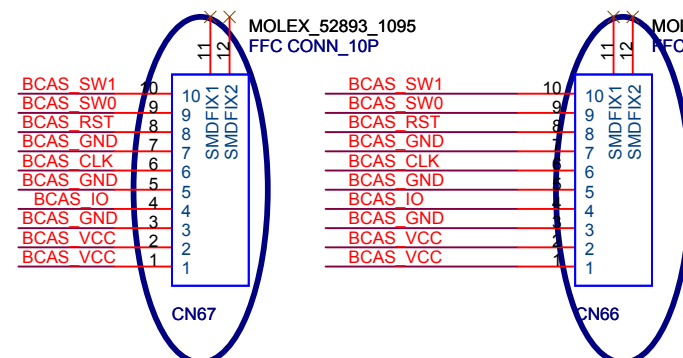


S-VIDEO IN



B-CAS connector (Close to TV Tuner)

FFC CONNECT TO TV TUNER BOARD (FOR JP DIGITAL)



030306: Change S/N from 1N-0010000-M0X0 to 1N-0010000-MWG0.
 031006: change part name from NV73_ ->TV_

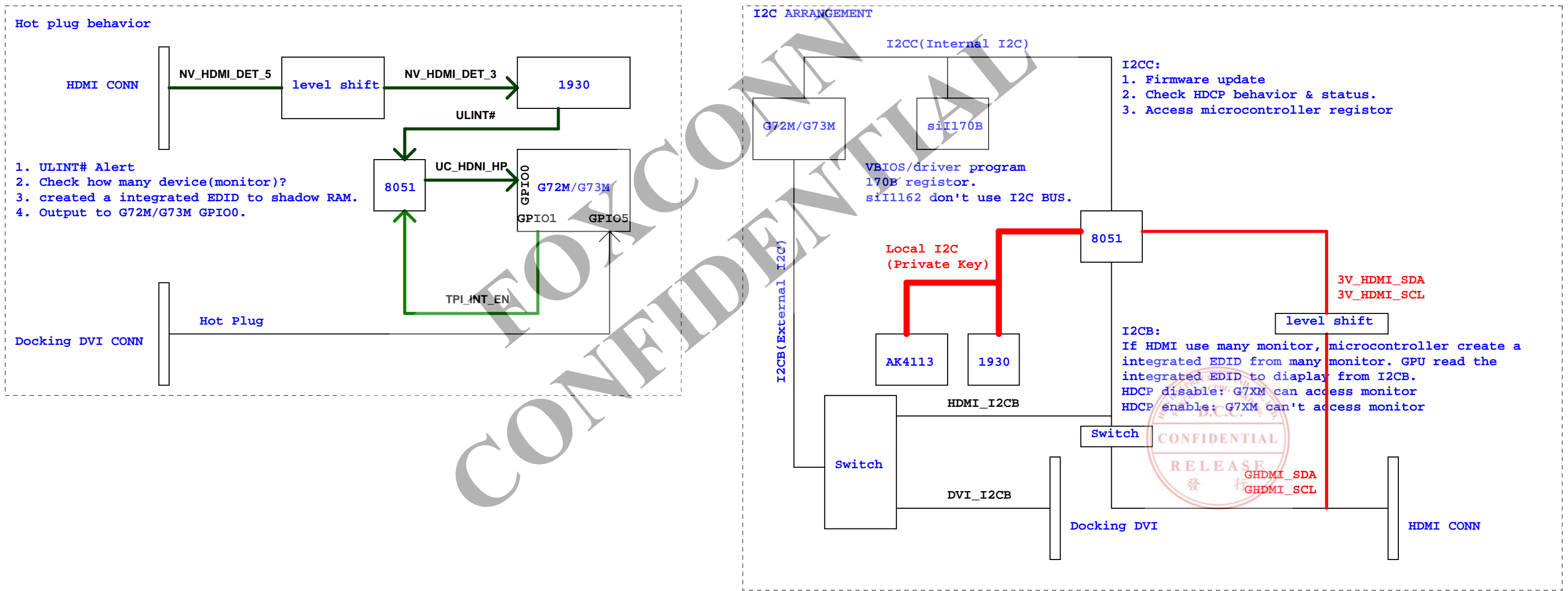
FOXCONN HON HAI PRECISION IND. CO., LTD.
 CPBG - R&D Division

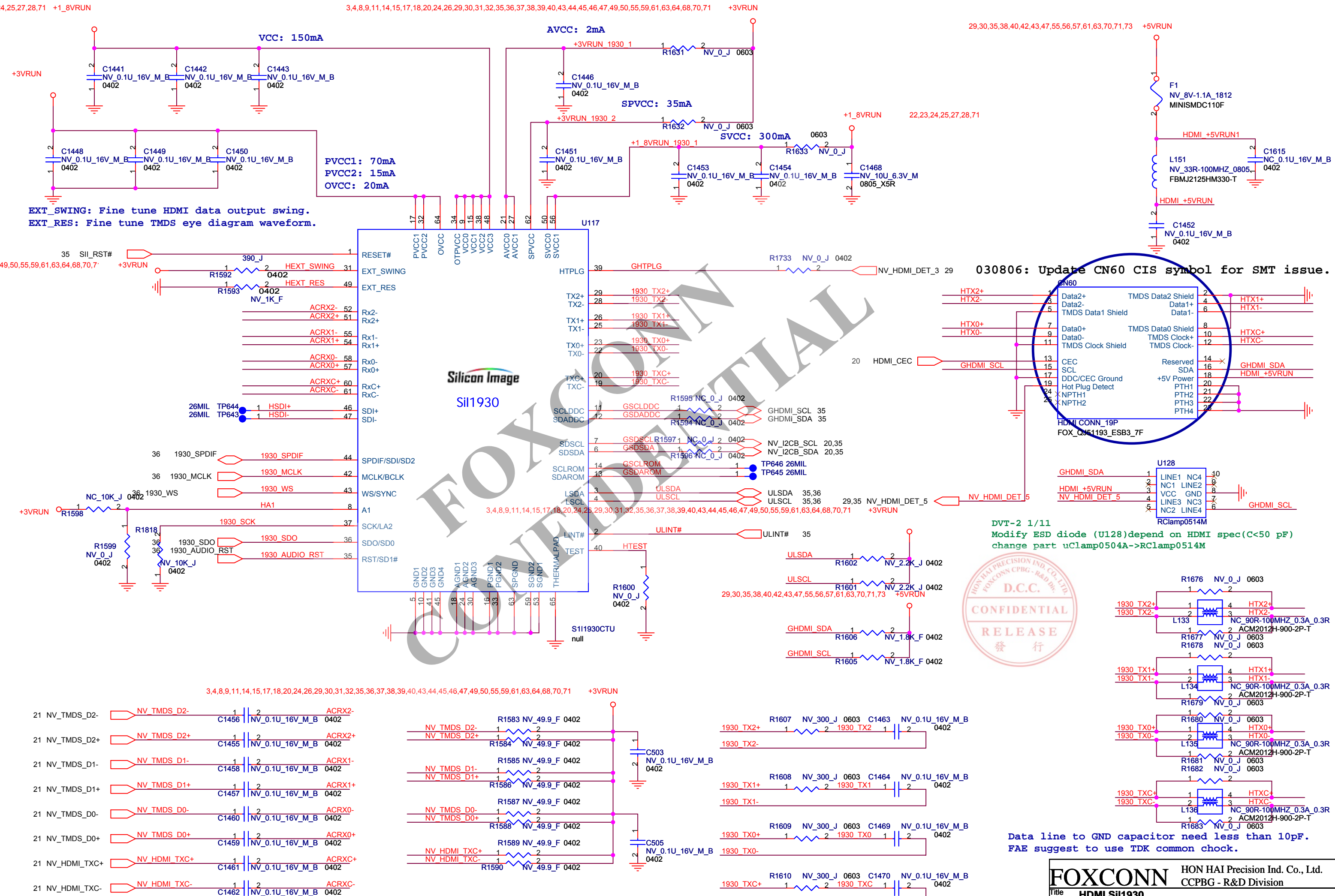
Title: **MINI-PCI CONN.**

Size: 43 Document Number: (MS20-1-01) MainBoard (MBX-156) Rev 1.00

Date: Friday, April 14, 2006 Sheet 32 of 80

Hot plug behavior & I2C ARRANGEMENT block diagram





030806: Update CN60 CIS symbol for SMT issue.

DVT-2 1/11
 Modify ESD diode (U128) depend on HDMI spec (C<50 pF)
 change part uClamp0504A->RClamp0514M

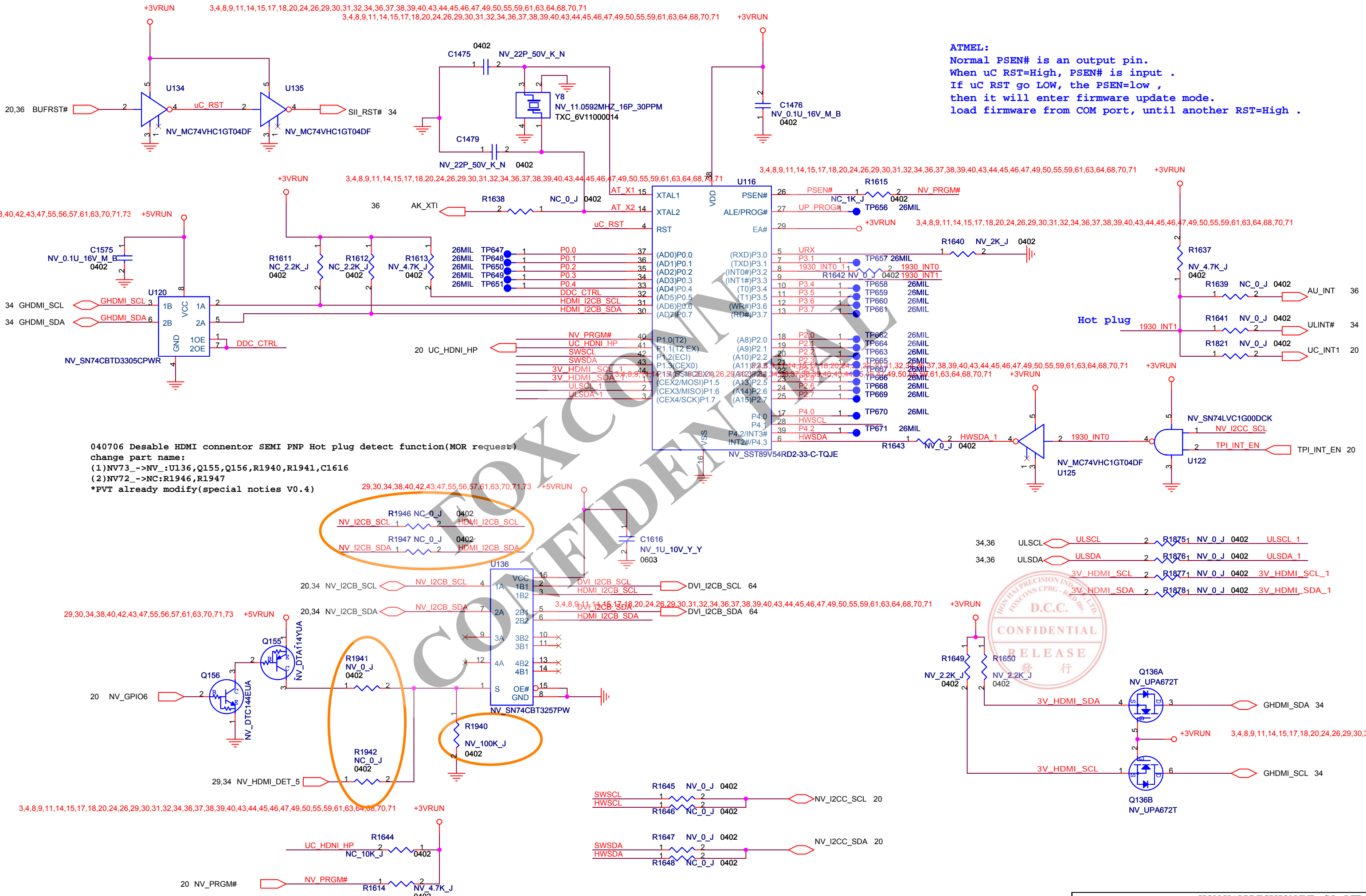


Data line to GND capacitor need less than 10pF.
 FAE suggest to use TDK common chock.

6/16 -> package 0402(300R)->0603(300R)
 For special layout.

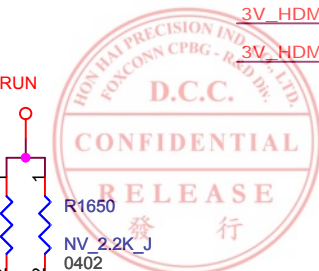
FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	HDMI Sii1930
Size	Document Number
A3	(MS20-101) MainBoard (MBX-156)
Date:	Rev
Friday, April 14, 2006	1.00
Sheet	of
34	80

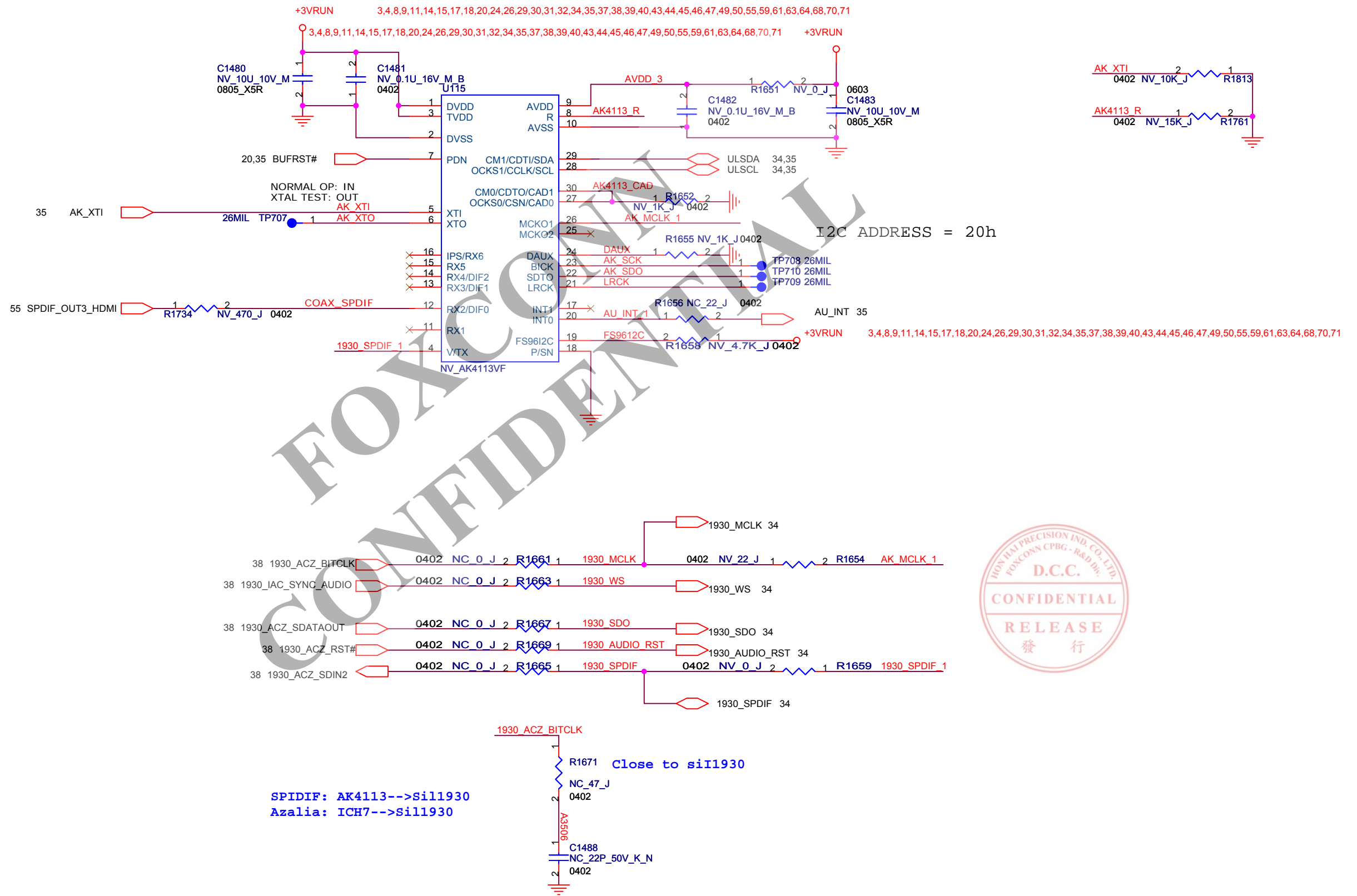
Close to sii1930



ATMEL:
 Normal PSEN# is an output pin.
 When uC RST=High, PSEN# is input .
 If uC RST go LOW, the PSEN=low ,
 then it will enter firmware update mode.
 load firmware from COM port, until another RST=High .

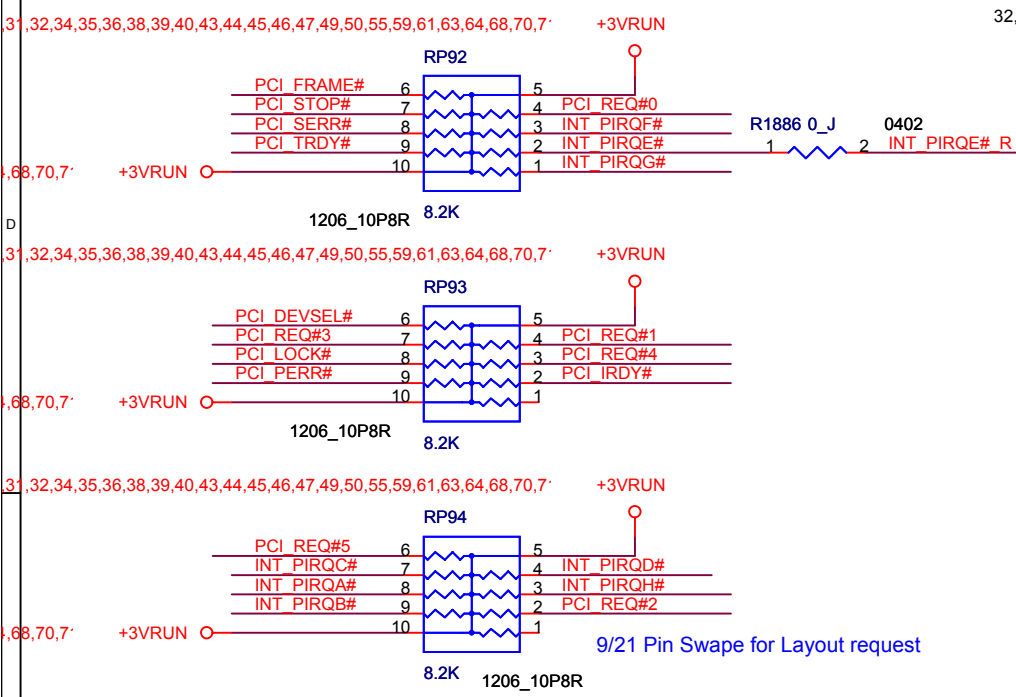
040706 Desable HDMI connentor SEMI PNP Hot plug detect function(MOR request)
 change part name:
 (1)NV73_ ->NV_:U136,Q155,Q156,R1940,R1941,C1616
 (2)NV72_ ->NC:R1946,R1947
 *PVT already modify(special noties V0.4)





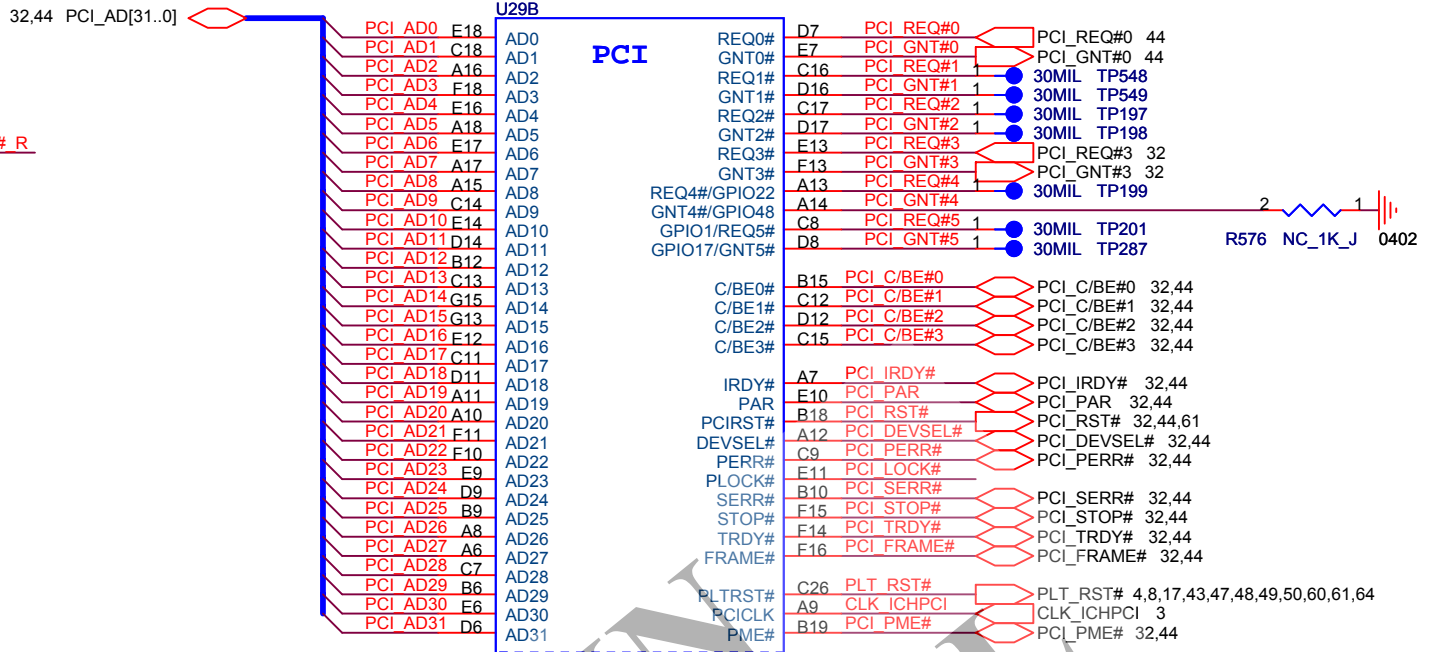
(2006/4/10)Hot plug behavior & I2C ARRANGEMENT block diagram move to page 33

FOXCONN HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title MINI-PCI CONN.		
Size A3	Document Number (MS20-1-01)MainBoard (MBX-156)	Rev 1.00
Date: Friday, April 14, 2006	Sheet 36	of 80



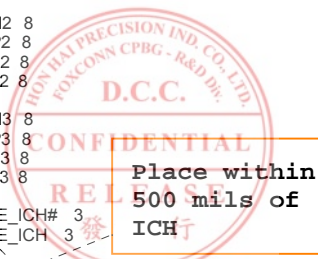
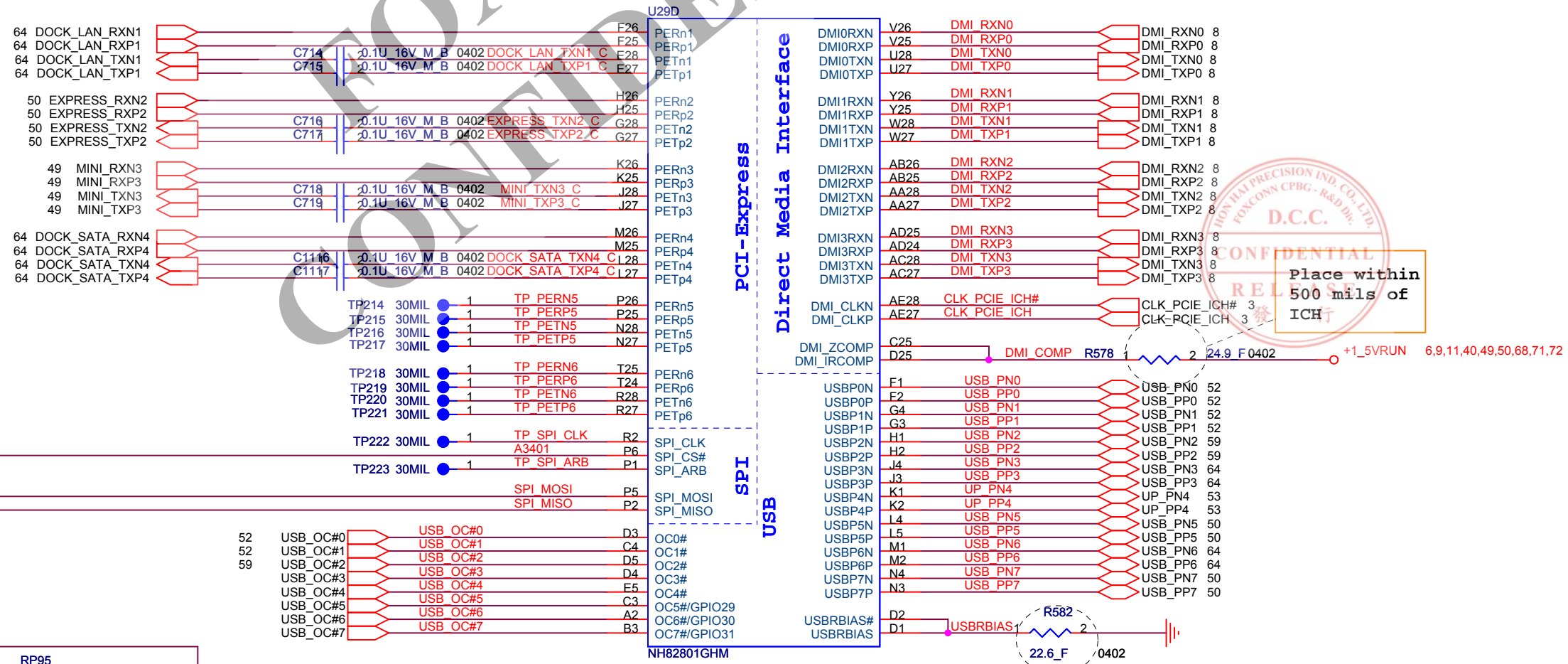
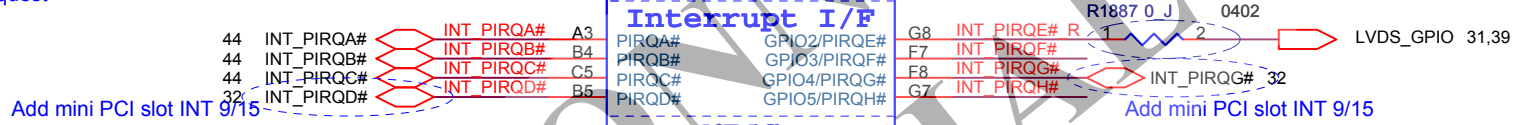
PCI Pullups

9/21 Pin Swape for Layout request

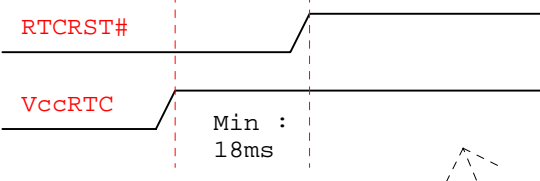


Strap for Boot-BIOS

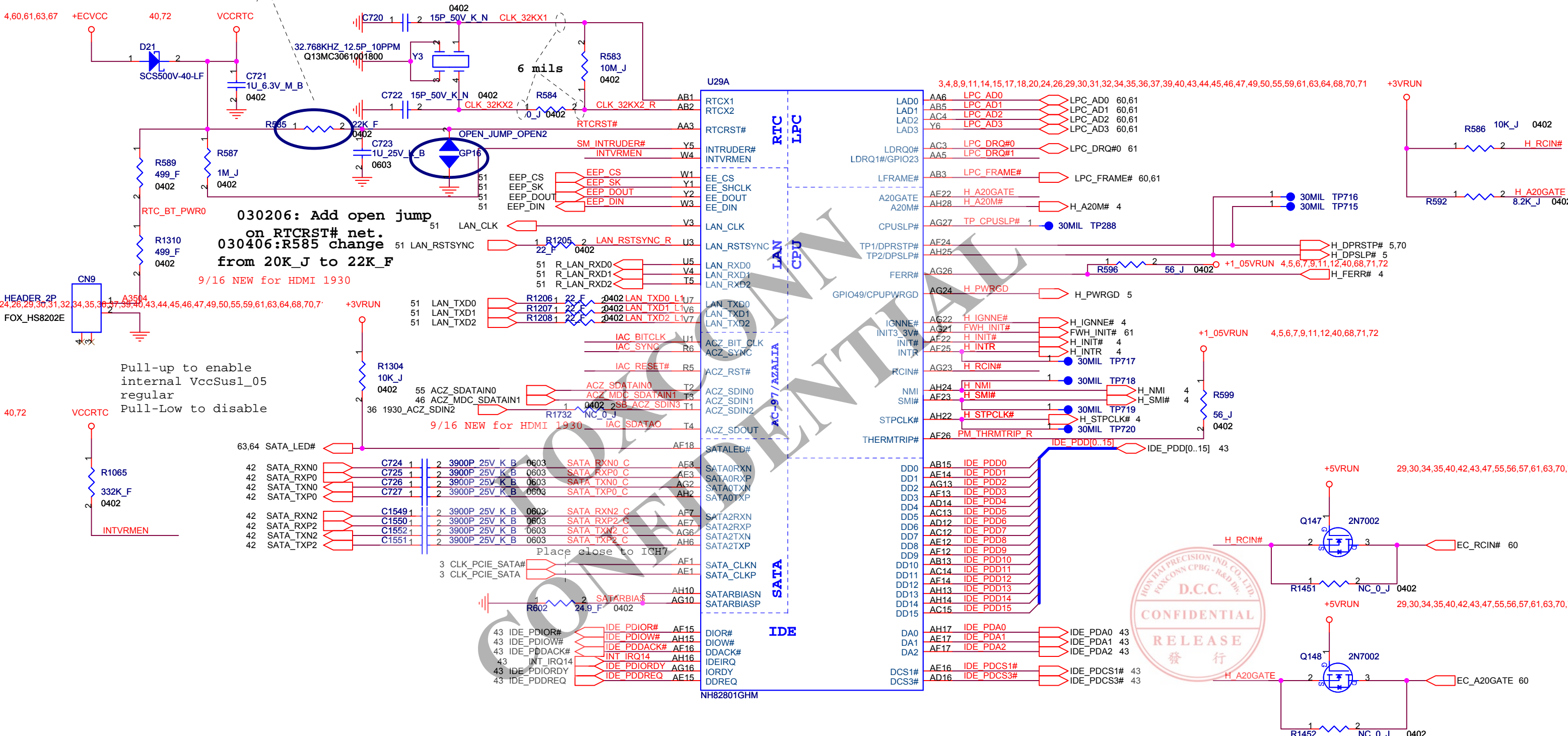
	GNT5#	GNT4#
LPC(Default)	Hi	Hi
PCI	Hi	LOW



Place within 500 mils of ICH and don't routing next to high speed signals

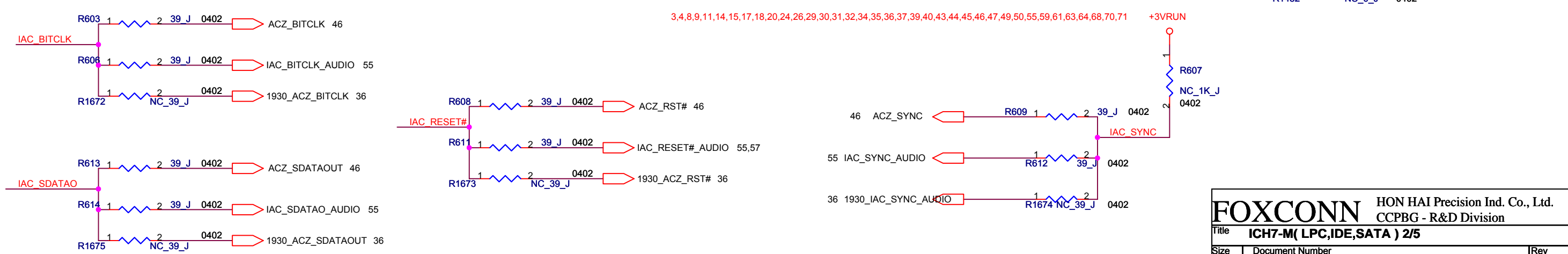


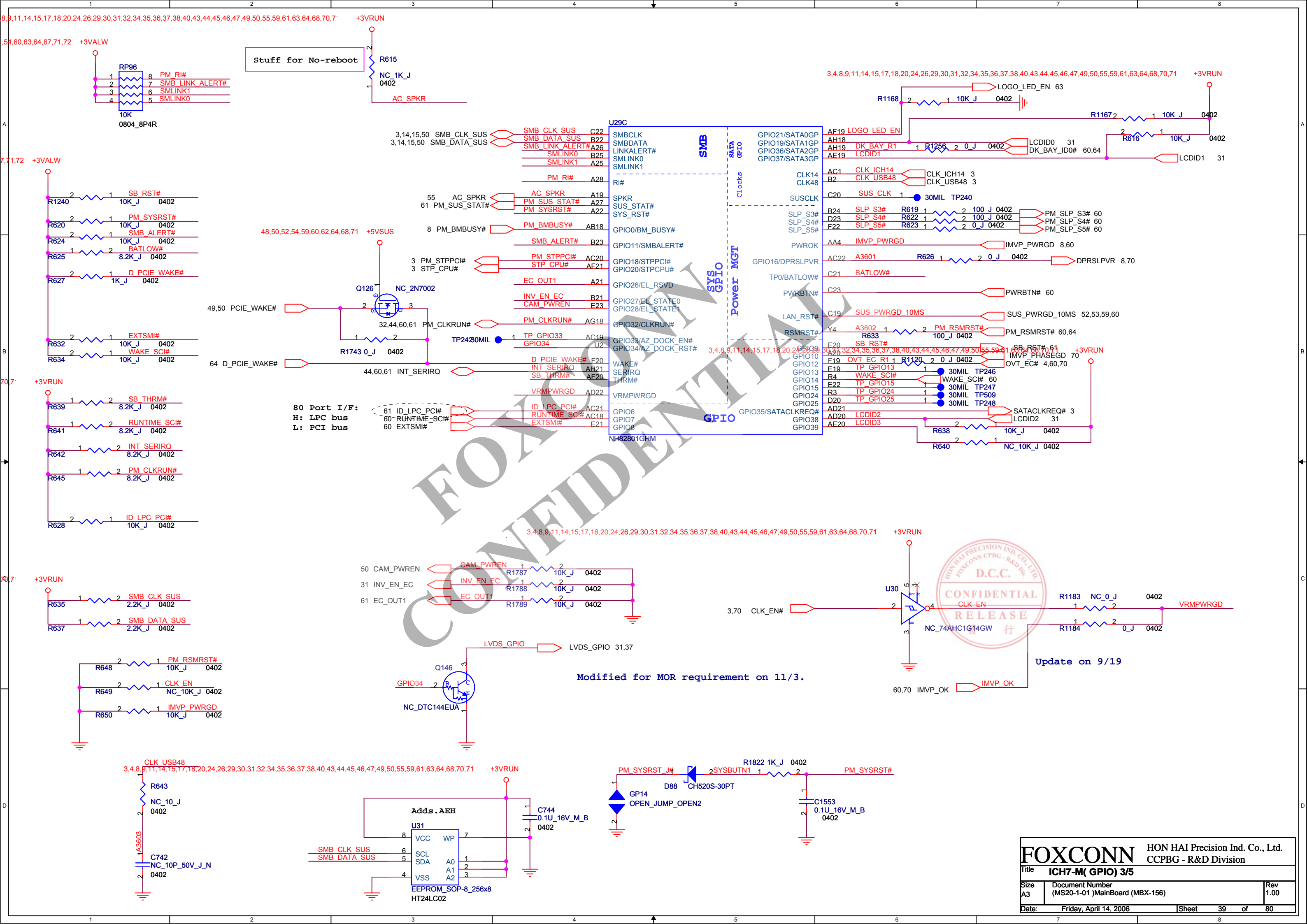
The traces inside this block should be wider.
No digital signals routed under XTAL

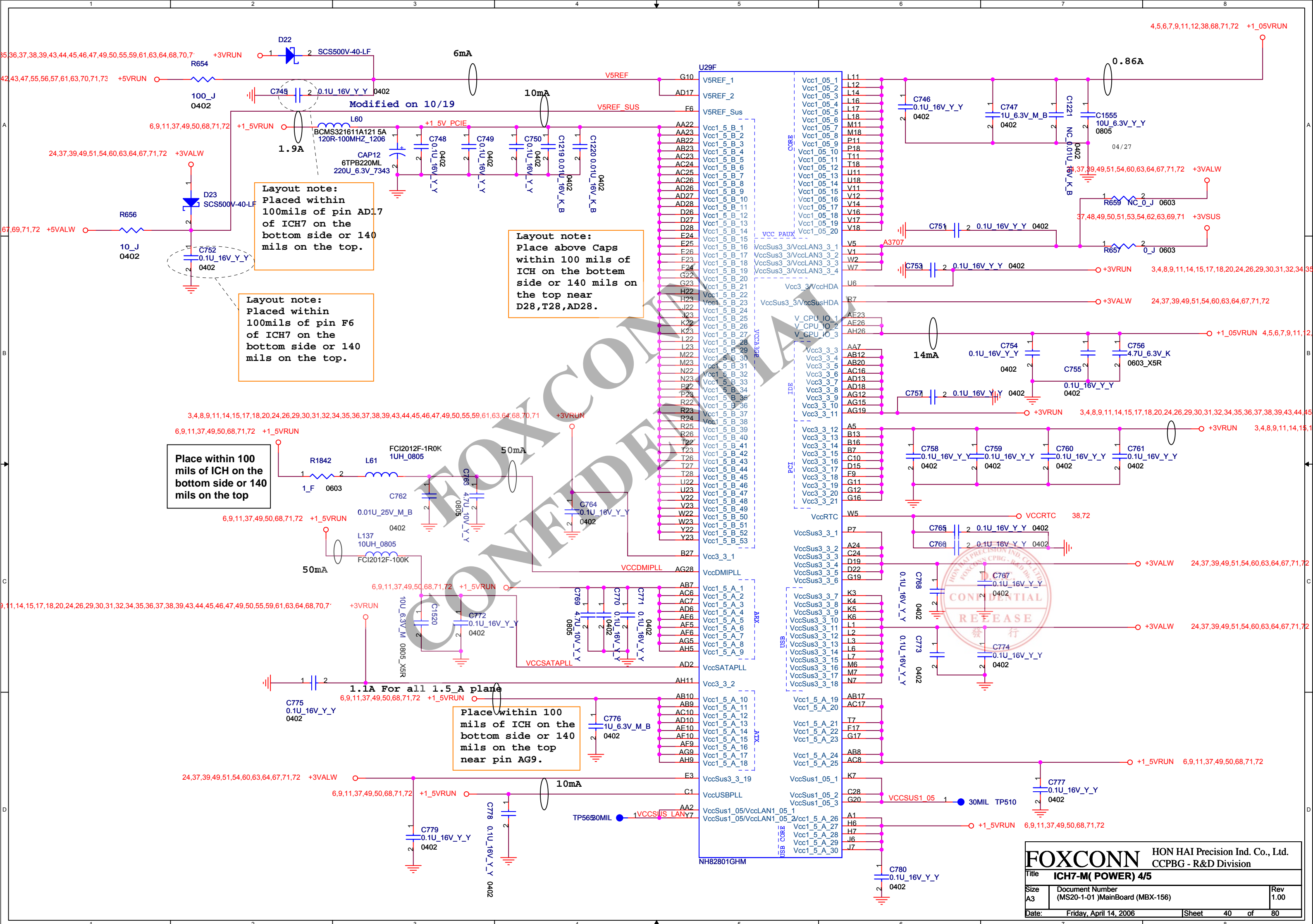


030206: Add open jump on RTCRST# net.
030406: R585 change from 20K_J to 22K_F
9/16 NEW for HDMI 1930

Pull-up to enable internal VccSus1_05 regular
Pull-Low to disable







Layout note:
Placed within 100mils of pin AD17 of ICH7 on the bottom side or 140 mils on the top.

Layout note:
Placed within 100mils of pin F6 of ICH7 on the bottom side or 140 mils on the top.

Layout note:
Place above Caps within 100 mils of ICH on the bottom side or 140 mils on the top near D28, T28, AD28.

Place within 100 mils of ICH on the bottom side or 140 mils on the top

Place within 100 mils of ICH on the bottom side or 140 mils on the top near pin AG9.

U29E

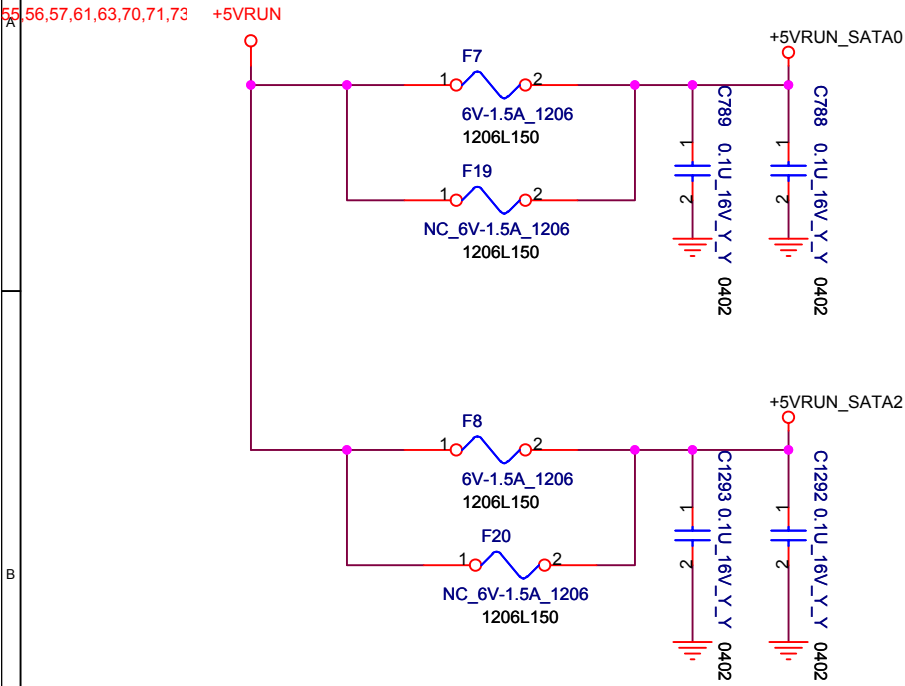
A4	VSS_1	VSS_98	P28
A23	VSS_2	VSS_99	R1
B1	VSS_3	VSS_100	R11
B8	VSS_4	VSS_101	R12
B11	VSS_5	VSS_102	R13
B14	VSS_6	VSS_103	R14
B17	VSS_7	VSS_104	R15
B20	VSS_8	VSS_105	R16
B26	VSS_9	VSS_106	R17
B28	VSS_10	VSS_107	R18
C2	VSS_11	VSS_108	T6
C6	VSS_12	VSS_109	T12
C27	VSS_13	VSS_110	T13
D10	VSS_14	VSS_111	T14
D13	VSS_15	VSS_112	T15
D18	VSS_16	VSS_113	T16
D21	VSS_17	VSS_114	T17
D24	VSS_18	VSS_115	U4
E1	VSS_19	VSS_116	U12
E2	VSS_20	VSS_117	U13
E4	VSS_21	VSS_118	U14
E8	VSS_22	VSS_119	U15
E15	VSS_23	VSS_120	U16
F3	VSS_24	VSS_121	U17
F4	VSS_25	VSS_122	U24
F5	VSS_26	VSS_123	U25
F12	VSS_27	VSS_124	U26
F27	VSS_28	VSS_125	V2
F28	VSS_29	VSS_126	V13
G1	VSS_30	VSS_127	V15
G2	VSS_31	VSS_128	V24
G5	VSS_32	VSS_129	V27
G6	VSS_33	VSS_130	V28
G9	VSS_34	VSS_131	W6
G14	VSS_35	VSS_132	W24
G18	VSS_36	VSS_133	W25
G21	VSS_37	VSS_134	W26
G24	VSS_38	VSS_135	Y3
G25	VSS_39	VSS_136	Y24
G26	VSS_40	VSS_137	Y27
H3	VSS_41	VSS_138	Y28
H4	VSS_42	VSS_139	AA1
H5	VSS_43	VSS_140	AA24
H24	VSS_44	VSS_141	AA25
H27	VSS_45	VSS_142	AA26
H28	VSS_46	VSS_143	AB4
J1	VSS_47	VSS_144	AB6
J2	VSS_48	VSS_145	AB11
J5	VSS_49	VSS_146	AB14
J24	VSS_50	VSS_147	AB16
J25	VSS_51	VSS_148	AB19
J26	VSS_52	VSS_149	AB21
K24	VSS_53	VSS_150	AB24
K27	VSS_54	VSS_151	AB27
K28	VSS_55	VSS_152	AB28
L13	VSS_56	VSS_153	AC2
L15	VSS_57	VSS_154	AC5
L24	VSS_58	VSS_155	AC9
L25	VSS_59	VSS_156	AC11
L26	VSS_60	VSS_157	AD1
M3	VSS_61	VSS_158	AD3
M4	VSS_62	VSS_159	AD4
M5	VSS_63	VSS_160	AD7
M12	VSS_64	VSS_161	AD8
M13	VSS_65	VSS_162	AD11
M14	VSS_66	VSS_163	AD15
M15	VSS_67	VSS_164	AD19
M16	VSS_68	VSS_165	AD23
M17	VSS_69	VSS_166	AE2
M24	VSS_70	VSS_167	AE4
M27	VSS_71	VSS_168	AE8
M28	VSS_72	VSS_169	AE11
N1	VSS_73	VSS_170	AE13
N2	VSS_74	VSS_171	AE18
N5	VSS_75	VSS_172	AE21
N6	VSS_76	VSS_173	AE24
N11	VSS_77	VSS_174	AE25
N12	VSS_78	VSS_175	AF2
N13	VSS_79	VSS_176	AF4
N14	VSS_80	VSS_177	AF8
N15	VSS_81	VSS_178	AF11
N16	VSS_82	VSS_179	AF27
N17	VSS_83	VSS_180	AF28
N18	VSS_84	VSS_181	AG1
N24	VSS_85	VSS_182	AG3
N25	VSS_86	VSS_183	AG7
N26	VSS_87	VSS_184	AG11
P3	VSS_88	VSS_185	AG14
P4	VSS_89	VSS_186	AG17
P12	VSS_90	VSS_187	AG20
P13	VSS_91	VSS_188	AG25
P14	VSS_92	VSS_189	AH1
P15	VSS_93	VSS_190	AH3
P16	VSS_94	VSS_191	AH7
P17	VSS_95	VSS_192	AH12
P24	VSS_96	VSS_193	AH23
P27	VSS_97	VSS_194	AH27

NH82801GHM

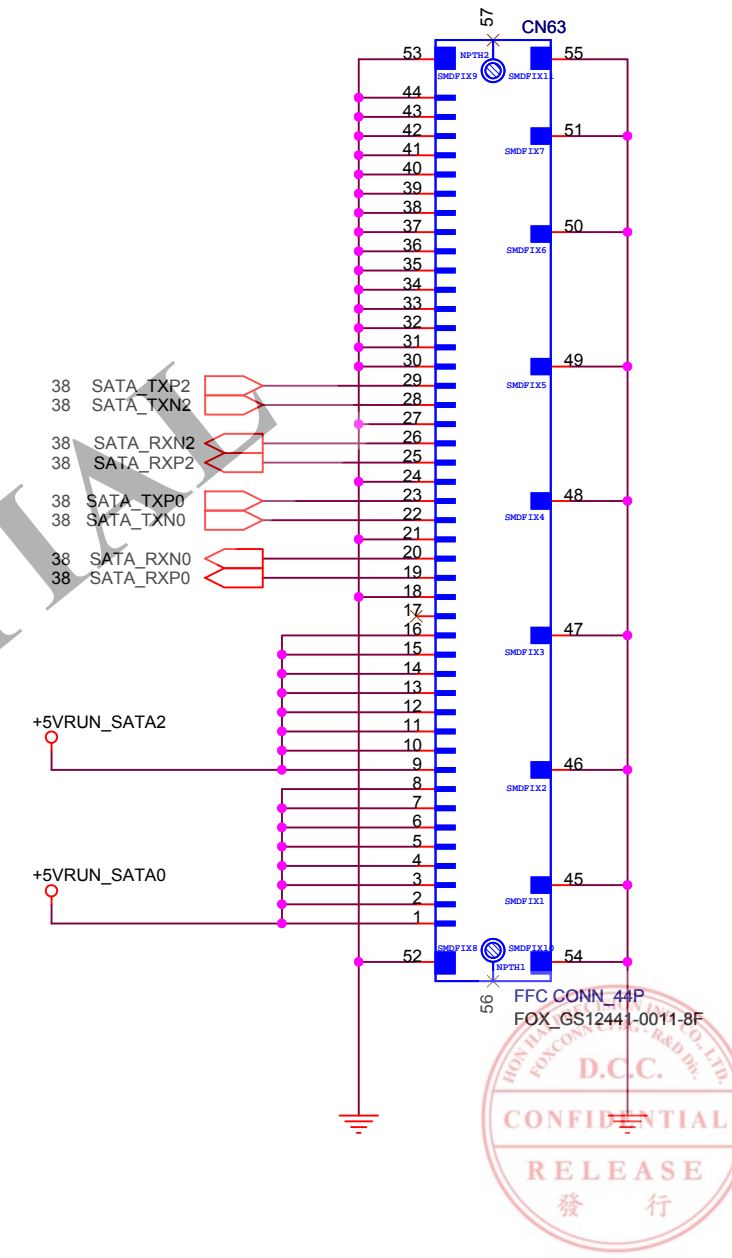
CONFIDENTIAL



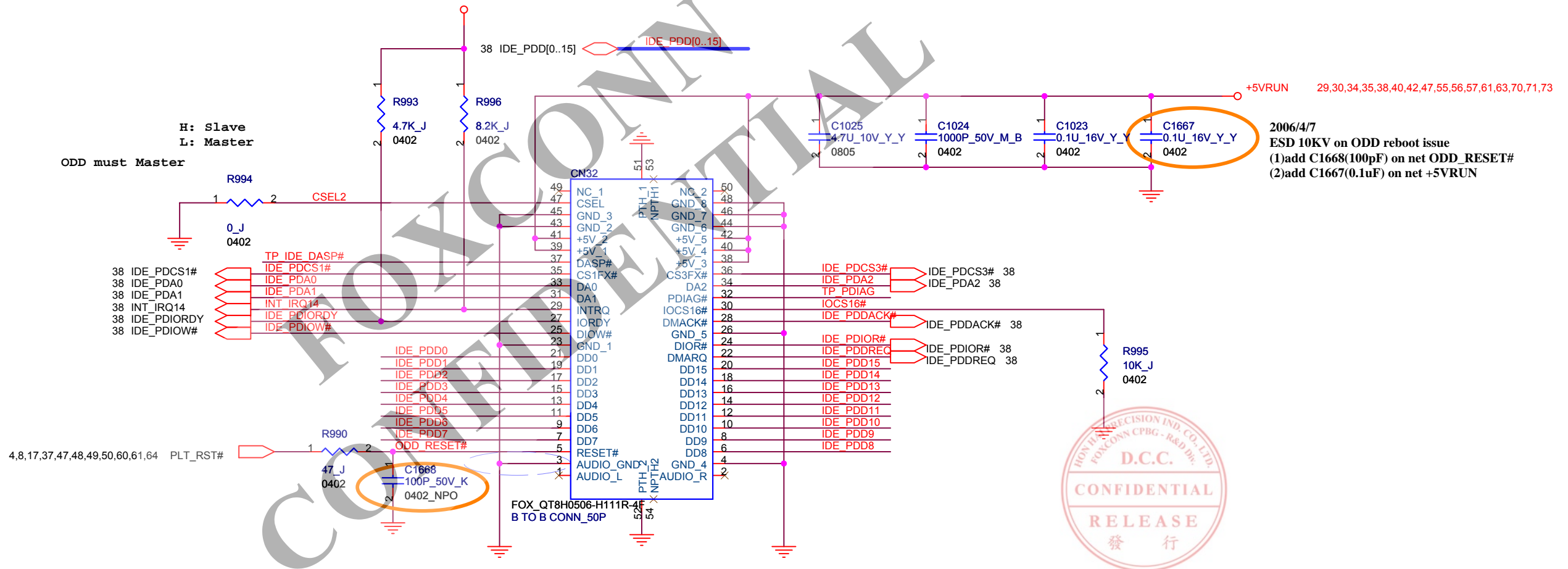
FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
Title ICH7-M (GND) 5/5		
Size A3	Document Number (MS20-1-01) MainBoard (MBX-156)	Rev 1.00
Date:	Friday, April 14, 2006	Sheet 41 of 80



FOXC
 CONFIDENTIAL



3,4,8,9,11,14,15,17,18,20,24,26,29,30,31,32,34,35,36,37,38,39,40,44,45,46,47,49,50,55,59,61,63,64,68,70,71 +3VRUN

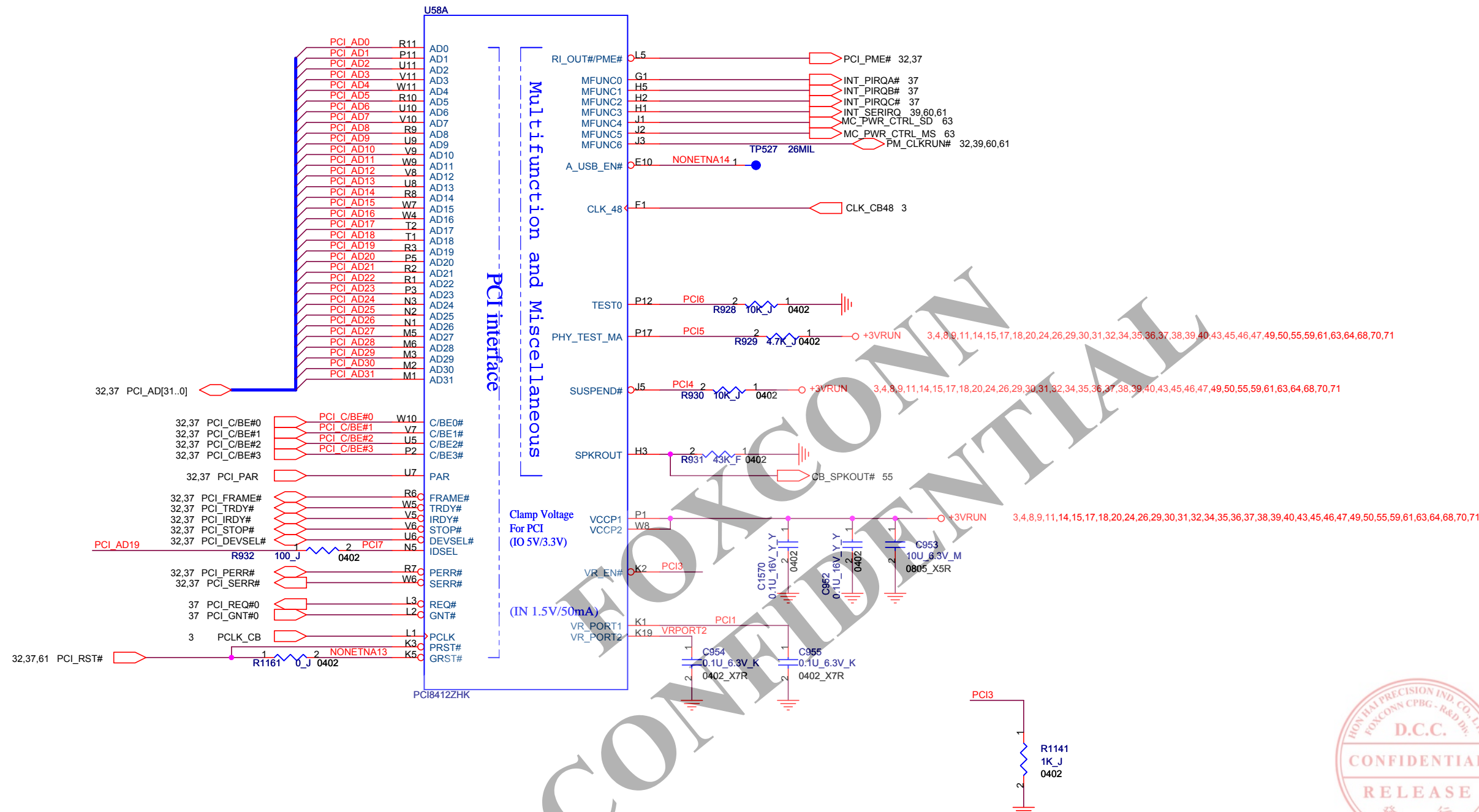


H: Slave
L: Master
ODD must Master

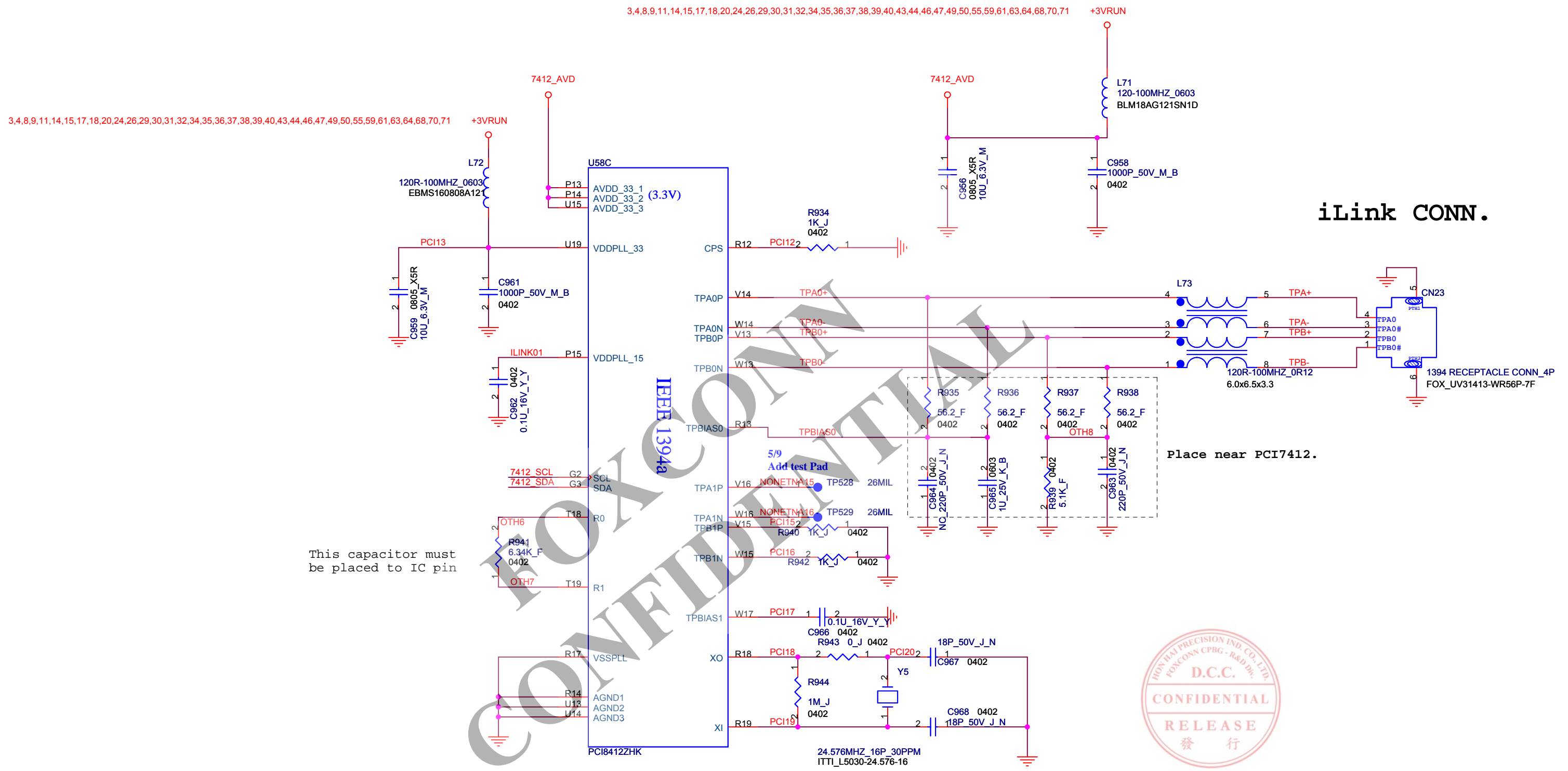
2006/4/7
ESD 10KV on ODD reboot issue
(1)add C1668(100pF) on net ODD_RESET#
(2)add C1667(0.1uF) on net +5VRUN

2005/4/17
Follow Adoi san suggest ODD: Master/HDD:Slave

CD-ROM CONN



FOXCONN		HON HAI Precision Ind. Co., Ltd.
Title PCI (PCI BUS)		CCPBG - R&D Division
Size	Document Number	Rev
Custom	(MS20-1-01) MainBoard (MBX-156)	1.00
Date:	Friday, April 14, 2006	Sheet 44 of 80

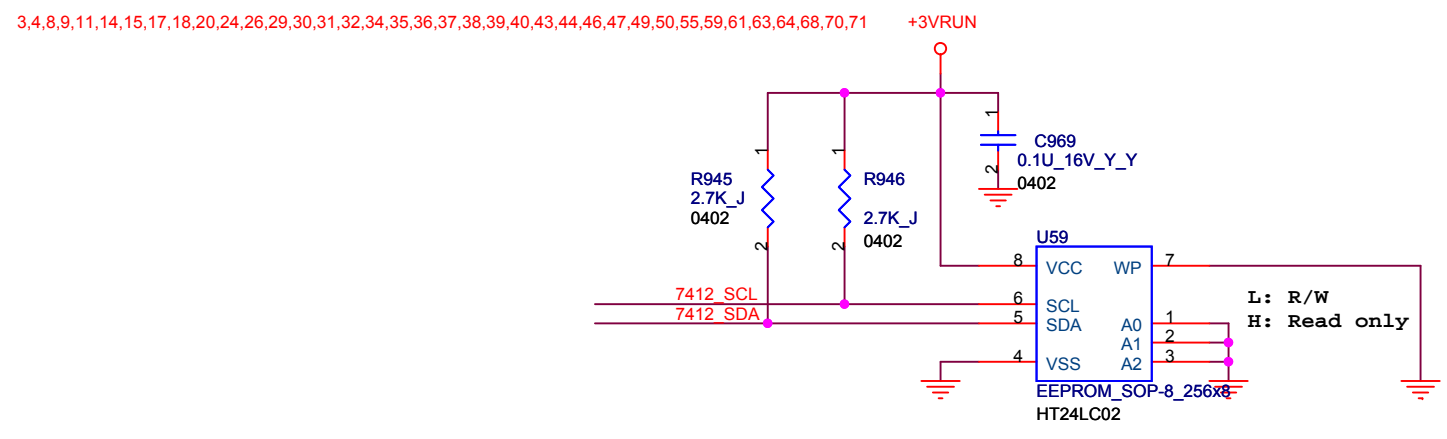


iLink CONN.

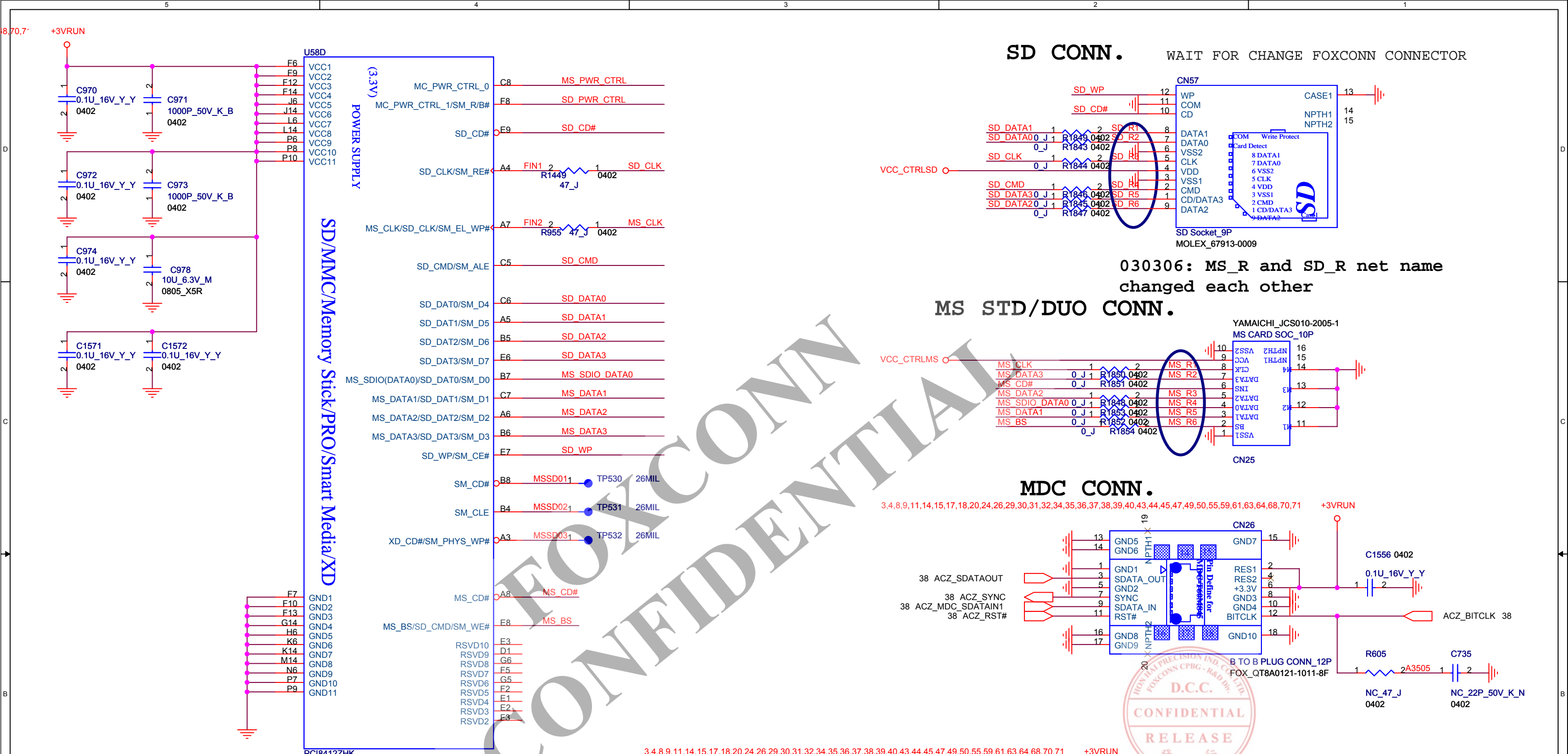
Place near PCI7412.



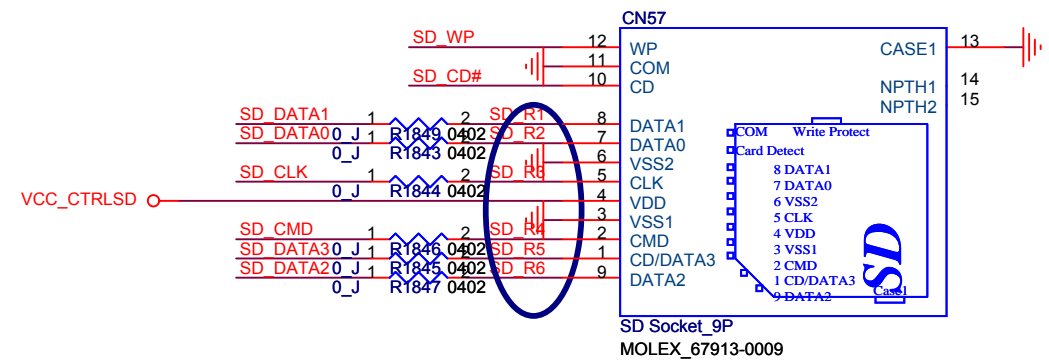
This capacitor must be placed to IC pin



FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title PCI (iLINK)	
Size A3	Document Number (MS20-1-01) MainBoard (MBX-156)
Date: Friday, April 14, 2006	Rev 1.00
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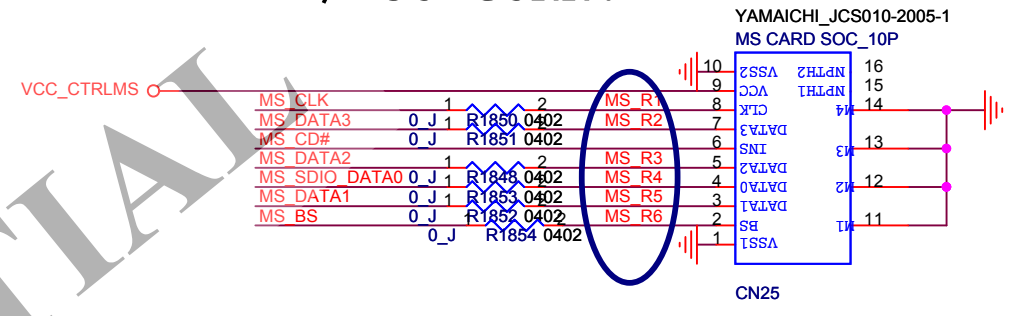


SD CONN. WAIT FOR CHANGE FOXCONN CONNECTOR

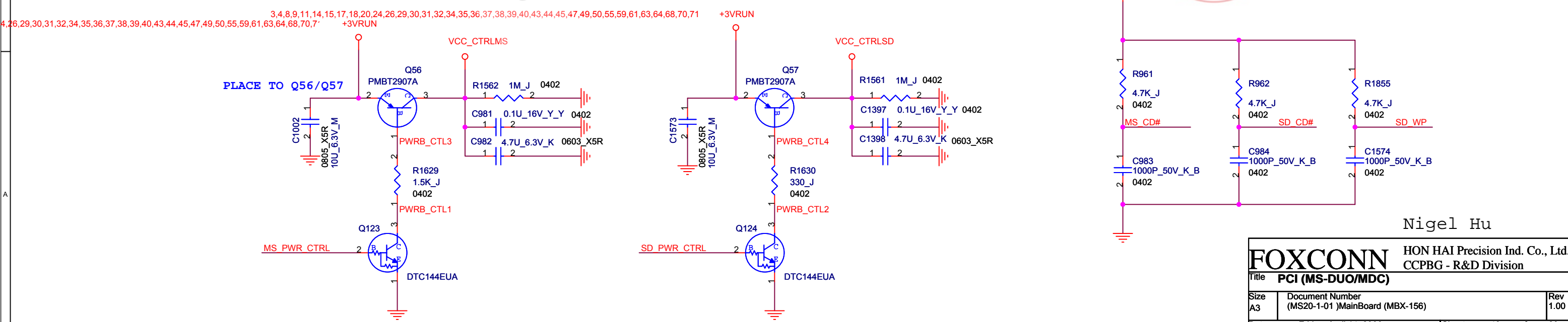
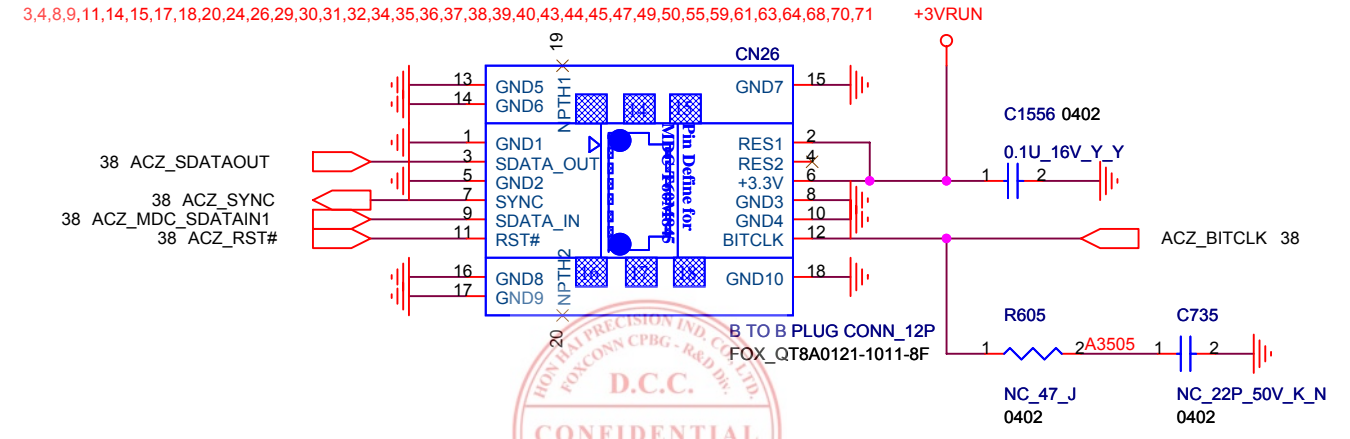


030306: MS_R and SD_R net name changed each other

MS STD/DUO CONN.



MDC CONN.



Nigel Hu

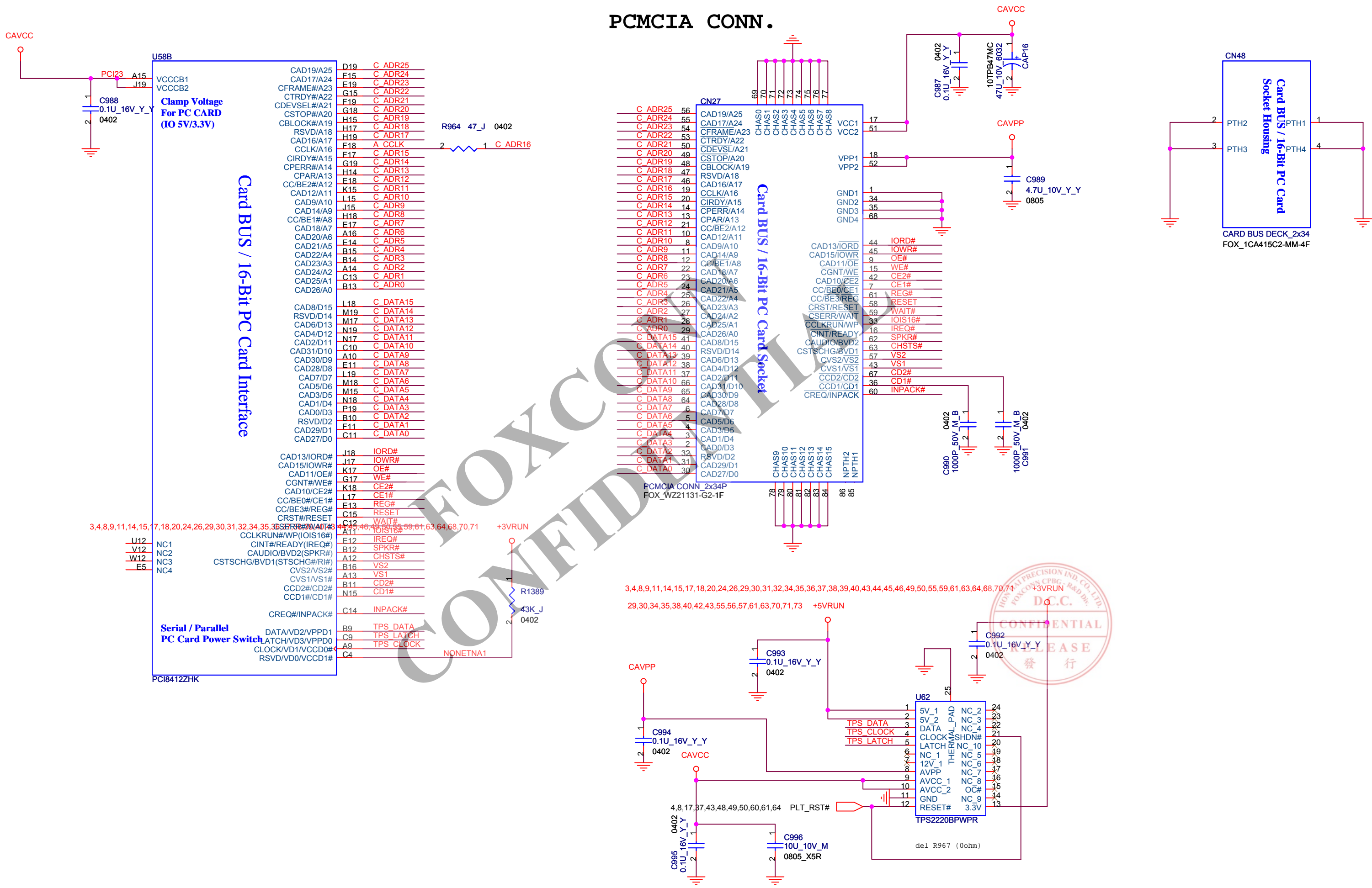
FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

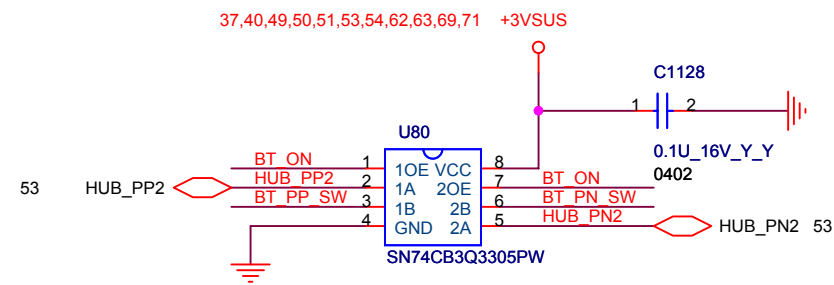
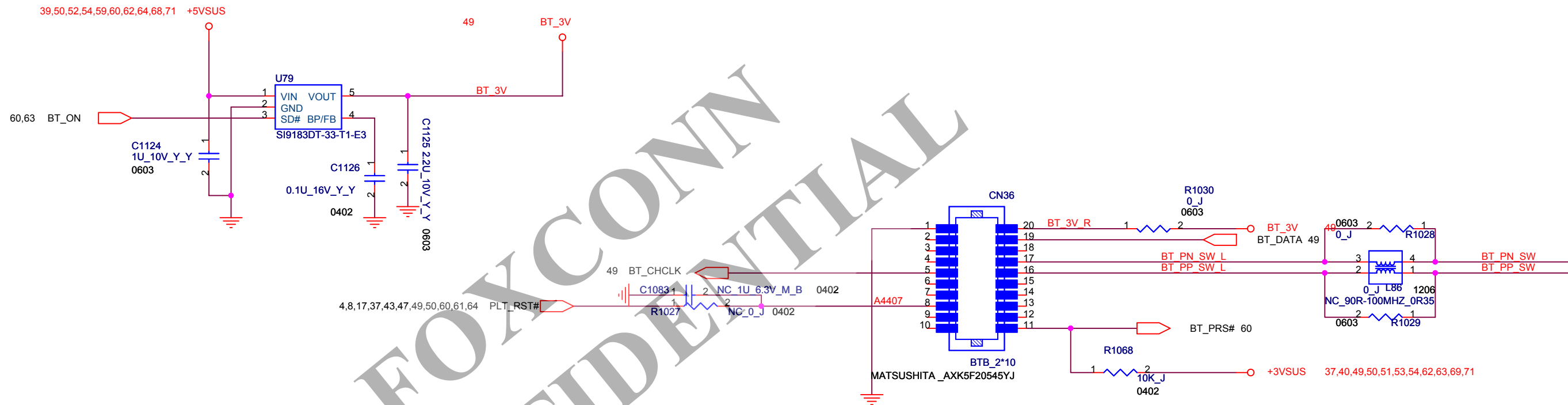
Title **PCI (MS-DUO/MDC)**

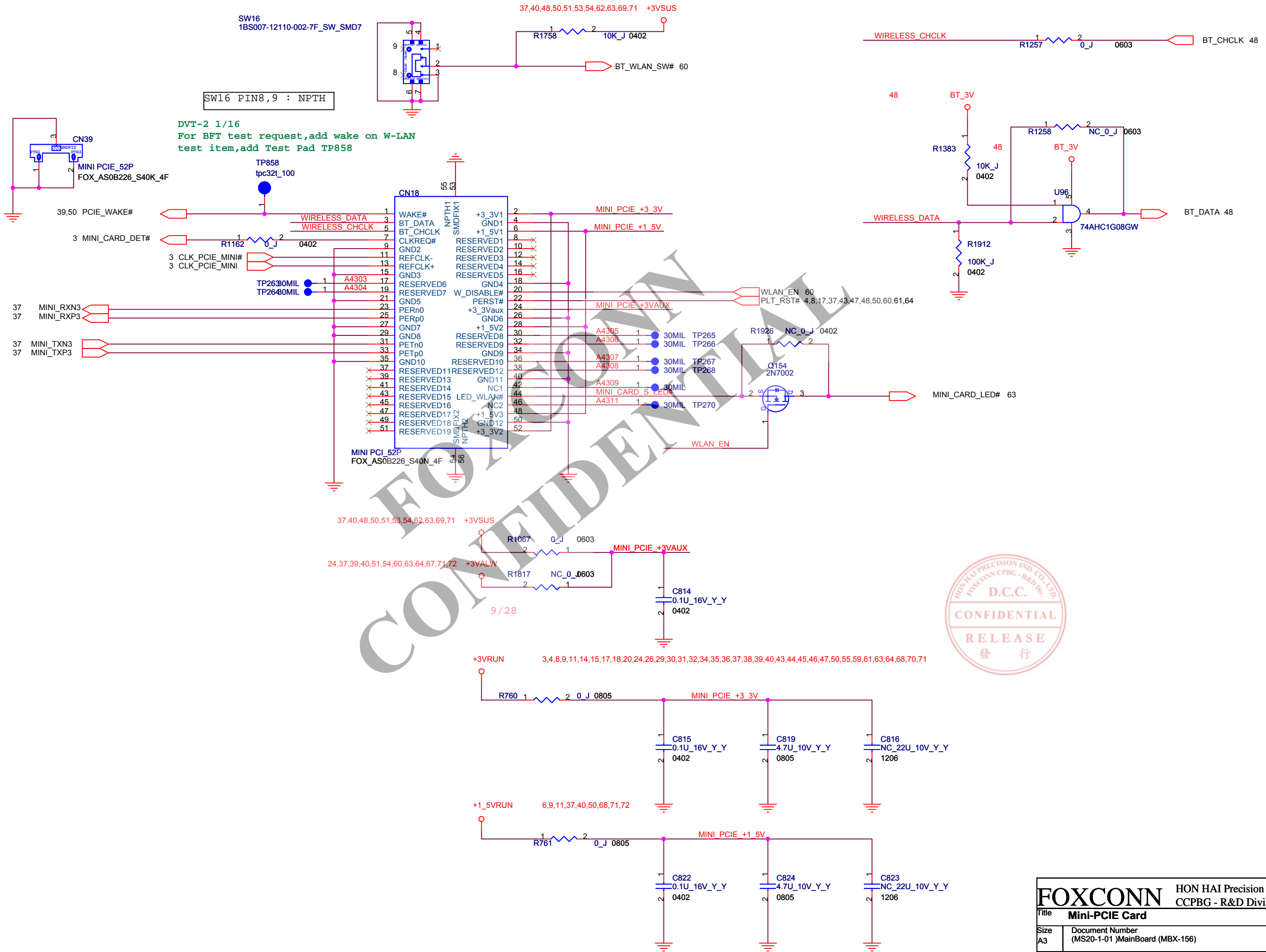
Size A3	Document Number (MS20-1-01) MainBoard (MBX-156)	Rev 1.00
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Date: Friday, April 14, 2006 | Sheet 46 of 80

PCMCIA CONN.

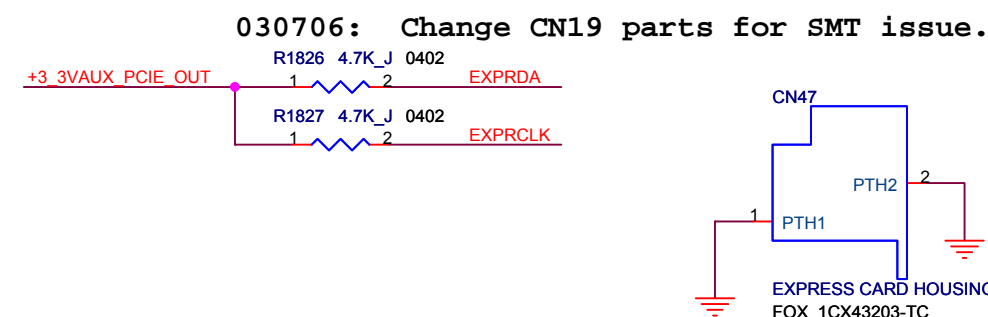
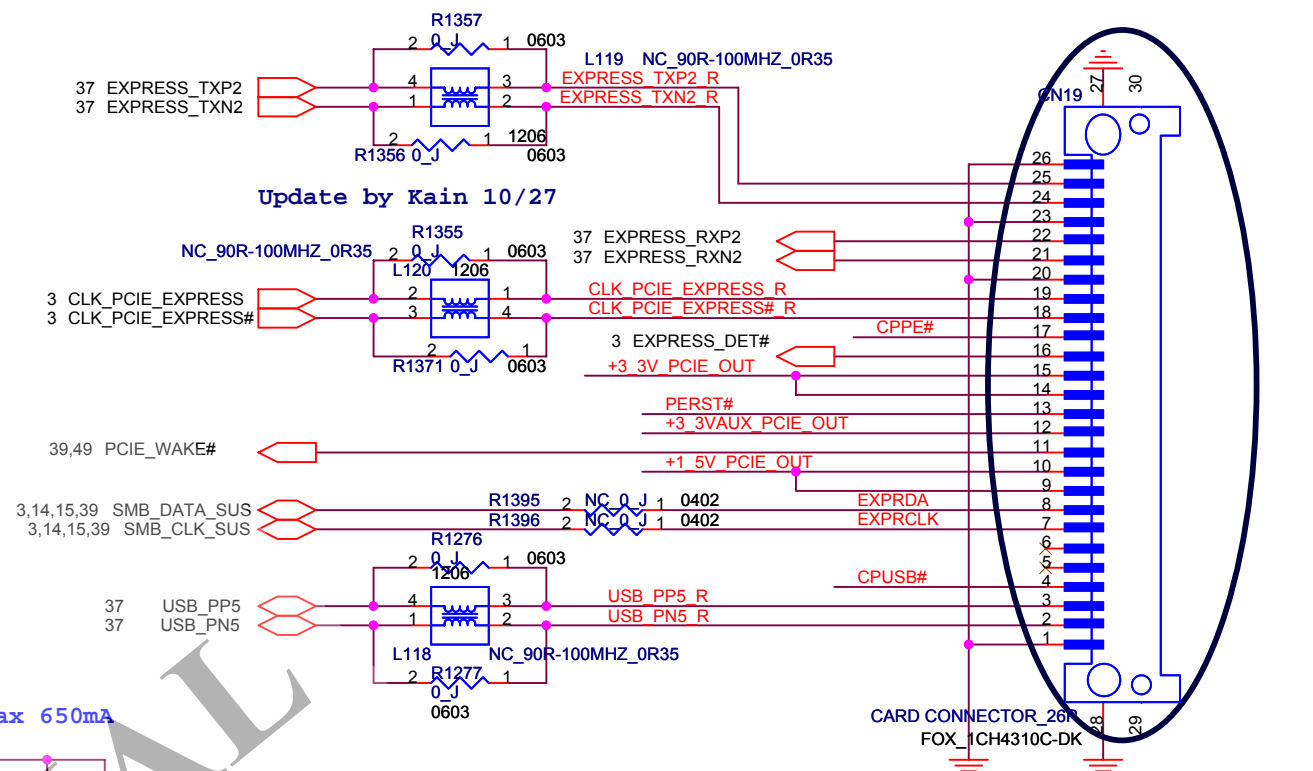
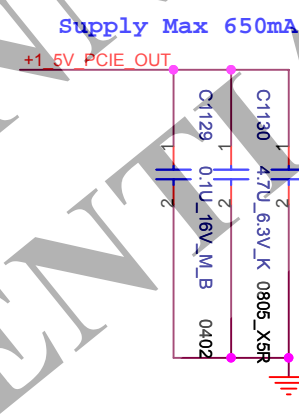
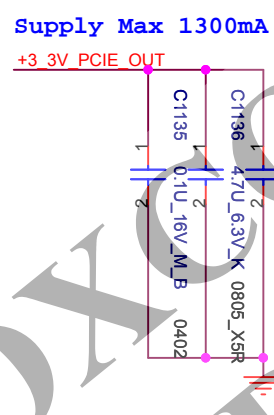
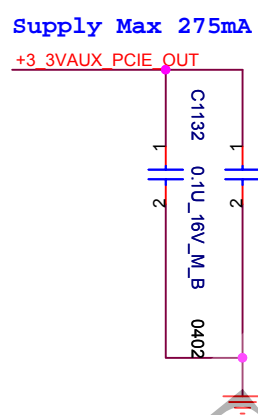
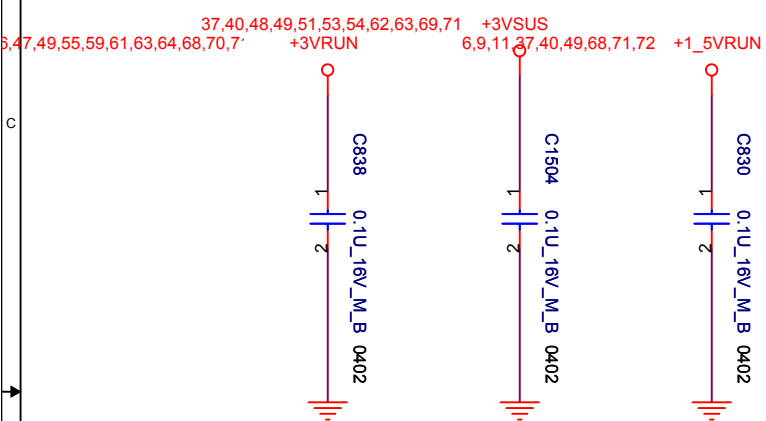
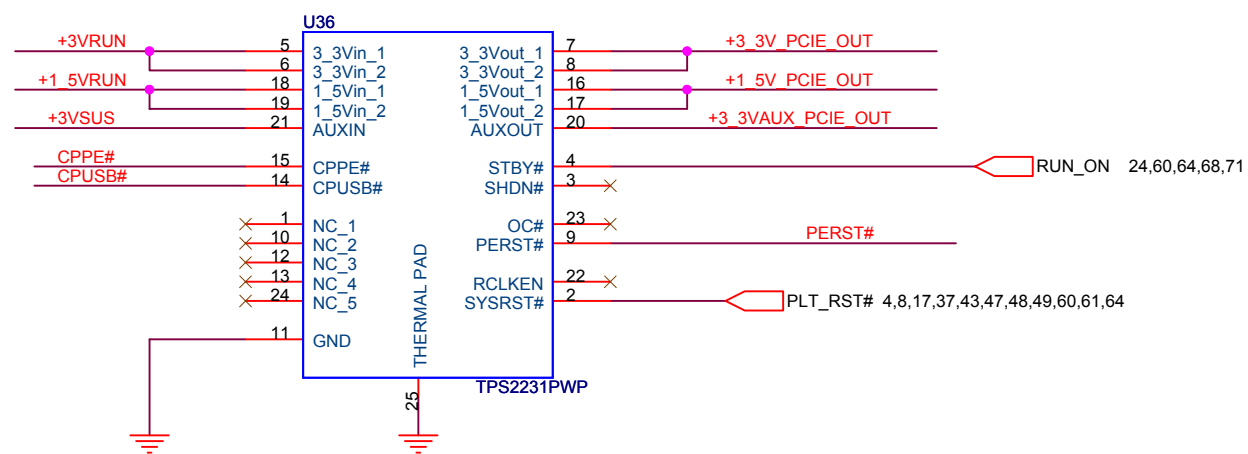






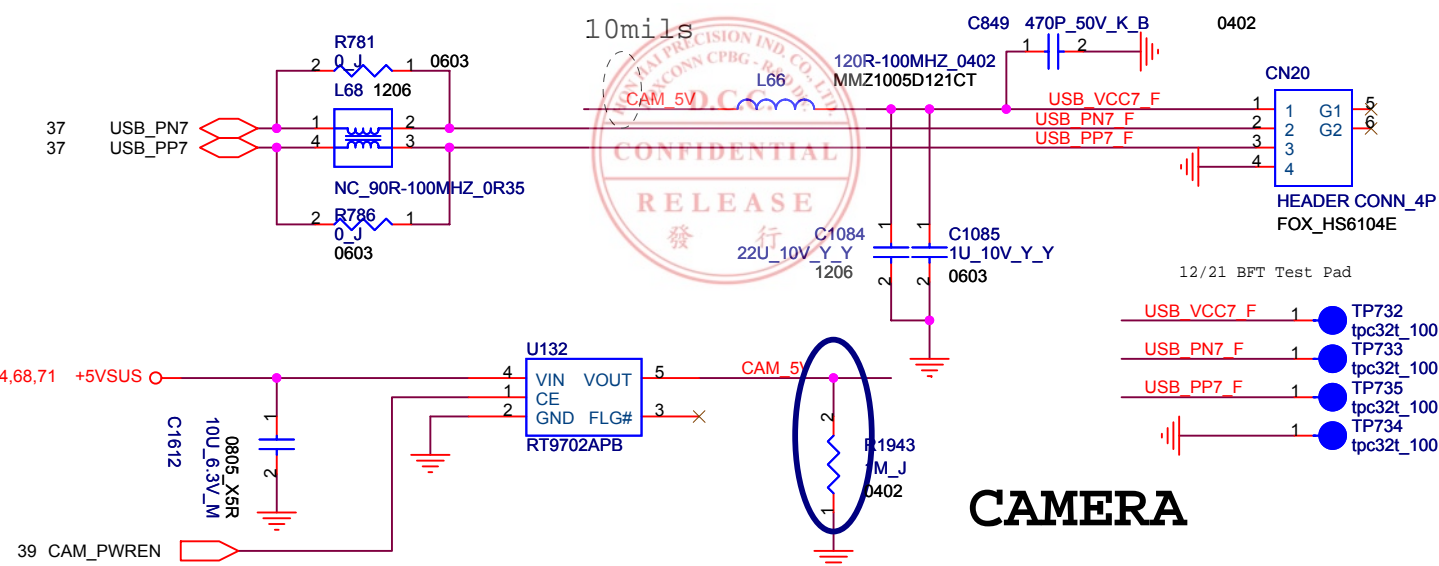
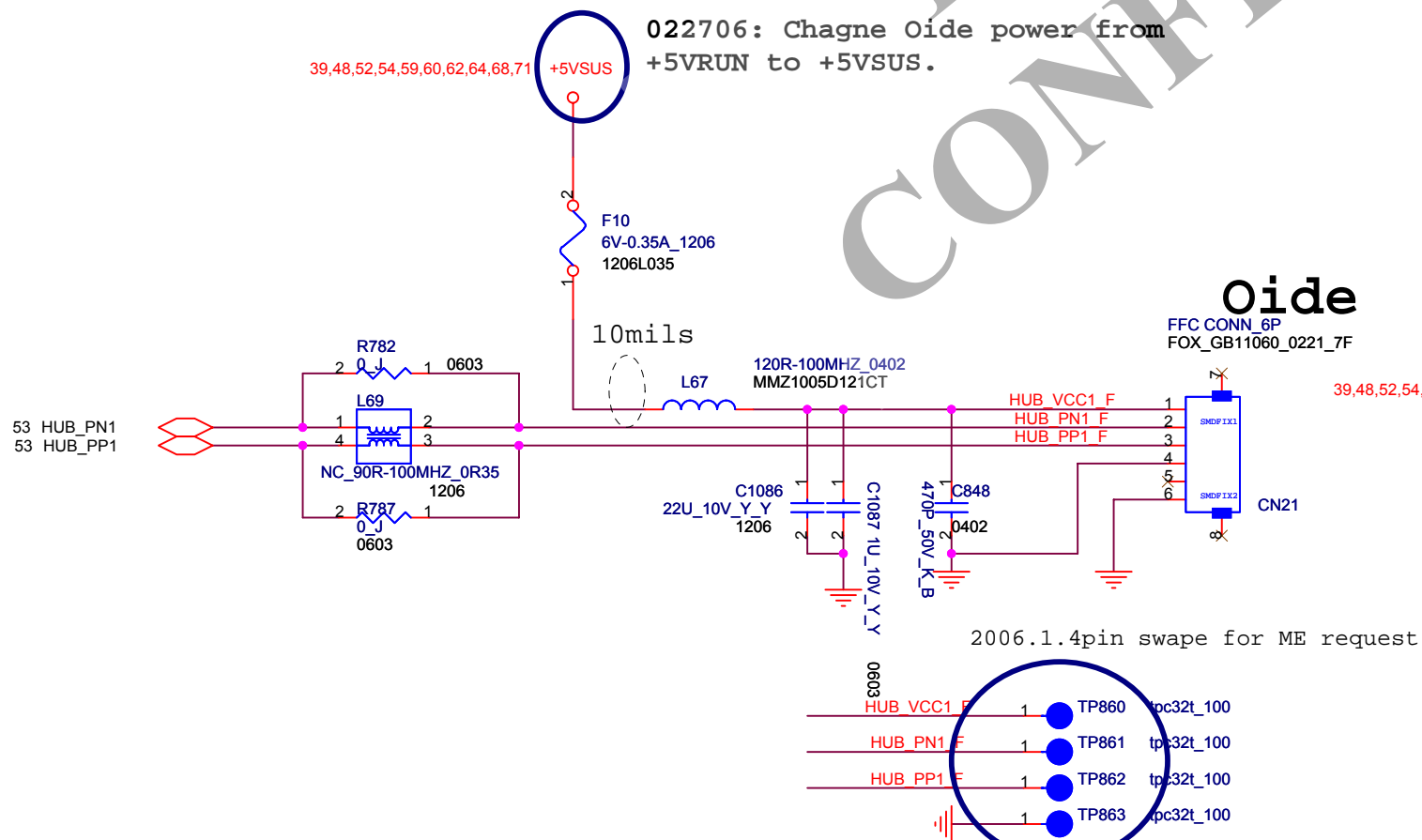
FOXCONN HON HAI Precision Ind. Co., Ltd.	
CCPBG - R&D Division	
Title	Mini-PCIE Card
Size	Document Number (MS20-1-01) MainBoard (MBX-156)
Rev	1.00
Date:	Friday, April 14, 2006
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VOLTAGE INPUTS ⁽¹⁾			LOGIC INPUTS			VOLTAGE OUTPUTS ⁽²⁾			MODE ⁽³⁾
AUXIN	3.3VIN	1.5VIN	SRDN	STBY	CP ⁽⁴⁾	AUXOUT	3.3VOUT	1.5VOUT	
Off	x	x	x	x	x	Off	Off	Off	OFF
On	x	x	0	x	x	GND	GND	GND	Shutdown
On	x	x	1	x	1	GND	GND	GND	No Card
On	On	On	1	0	0	On	Off	Off	Standby
On	On	On	1	1	0	On	On	On	Card Inserted

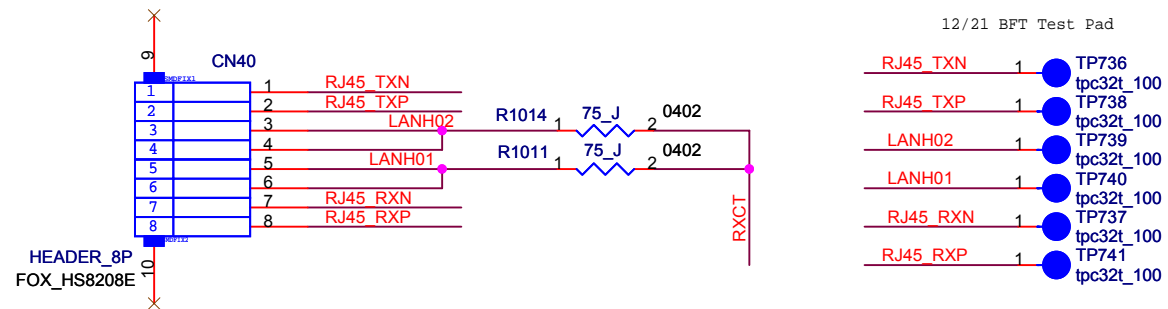


030706: Change CN19 parts for SMT issue.

022706: Change Oide power from +5VRUN to +5VSUS.

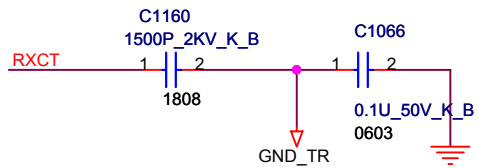
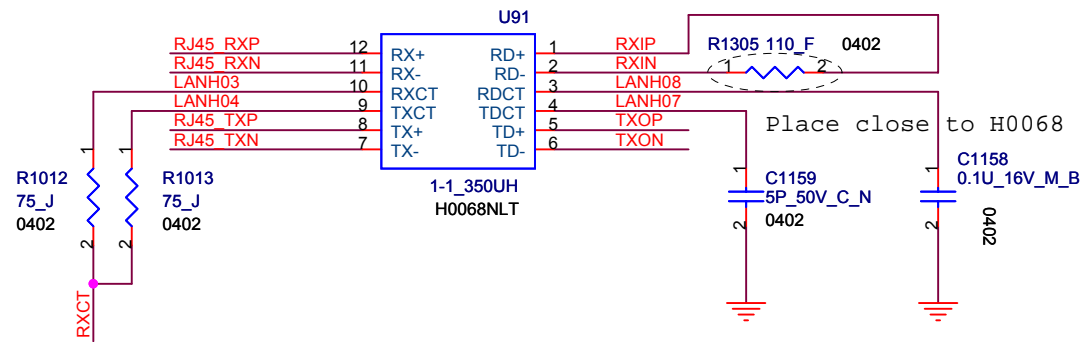
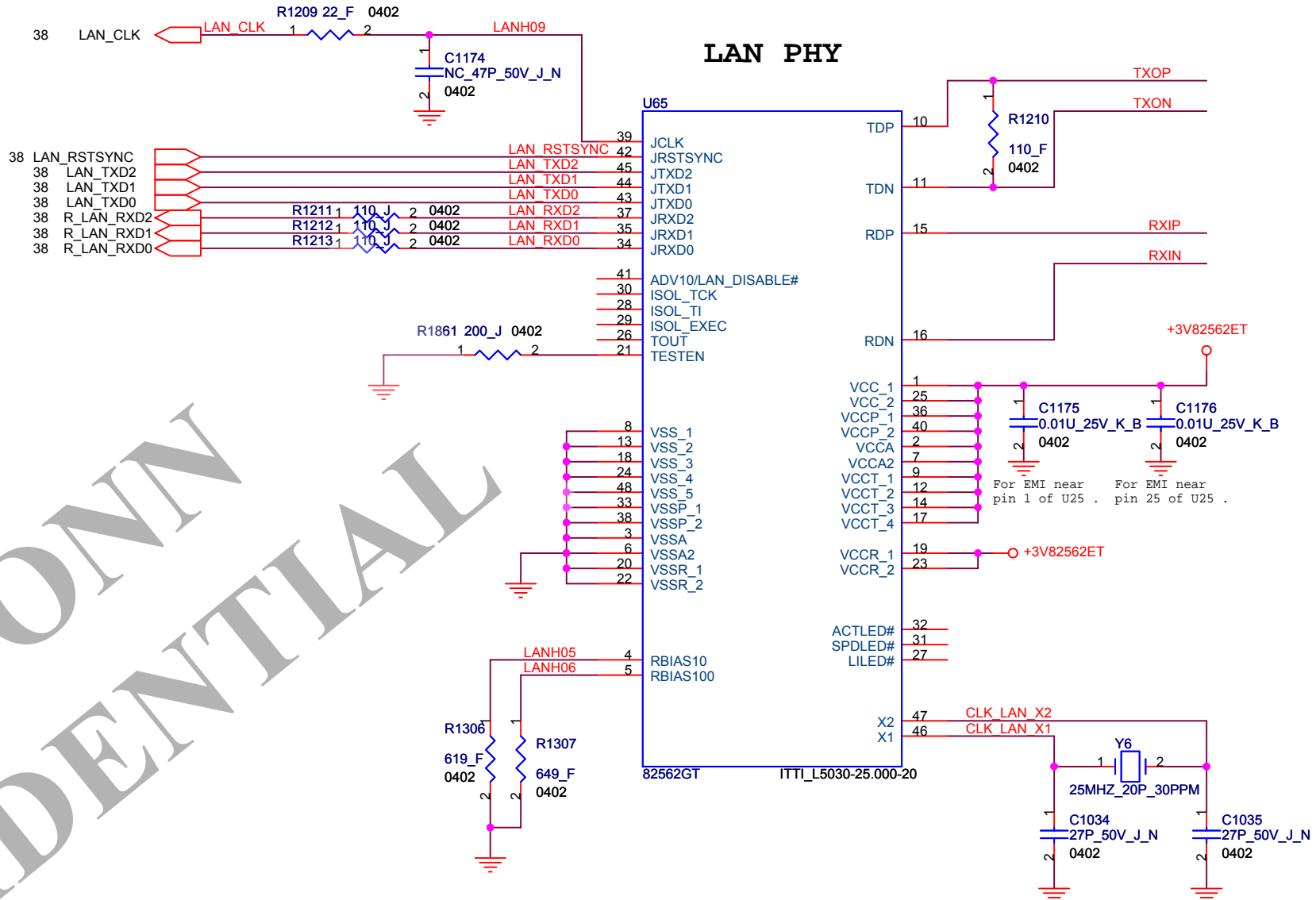


022706: Add discharge resistor for camera.

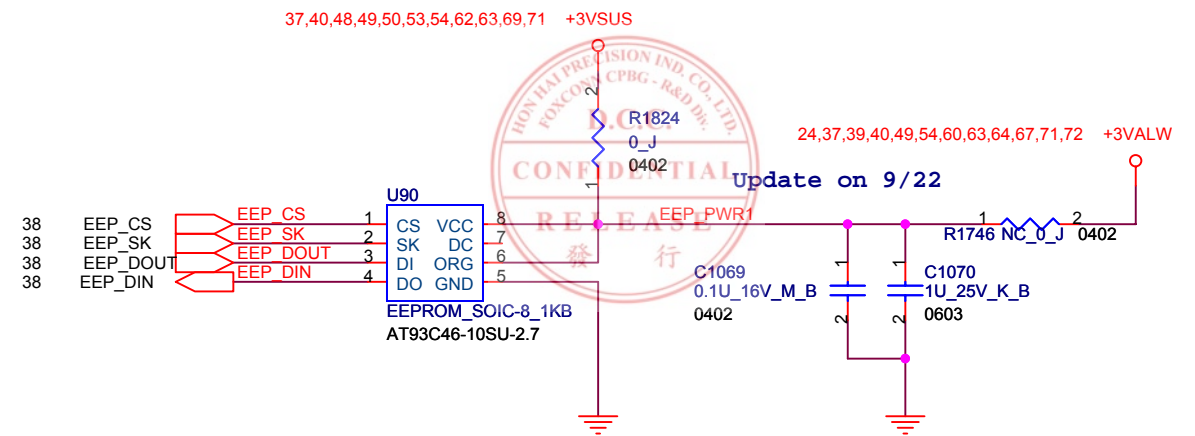
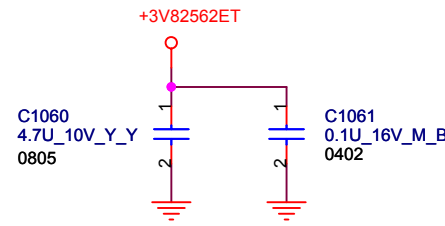
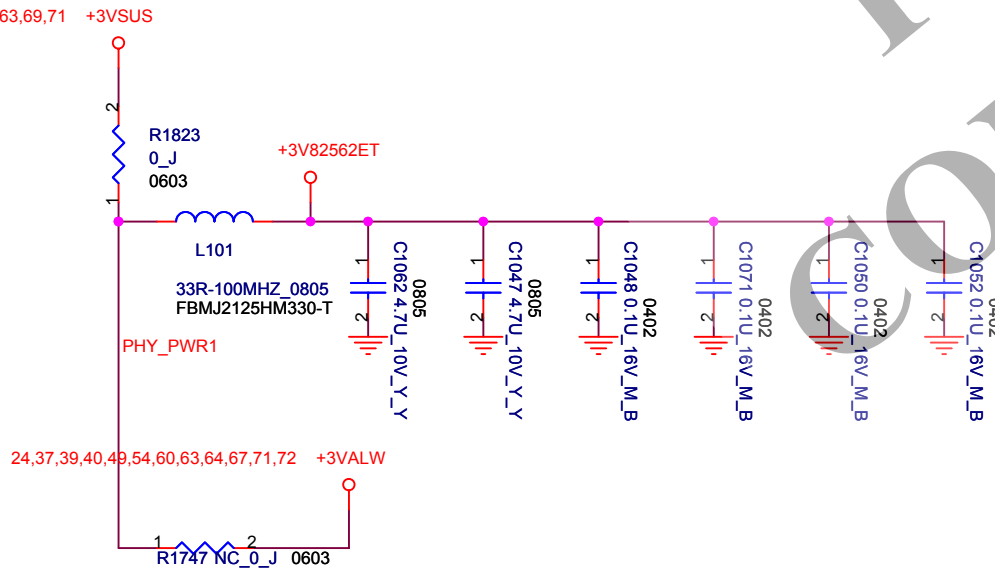


12/21 BPT Test Pad

RJ45 TXN	1	TP736
RJ45 TXP	1	tpc32t_100
LANH02	1	tpc32t_100
LANH01	1	TP739
RJ45 RXN	1	TP740
RJ45 RXP	1	tpc32t_100
RJ45 RXN	1	TP737
RJ45 RXP	1	tpc32t_100
RJ45 RXN	1	TP741
RJ45 RXP	1	tpc32t_100

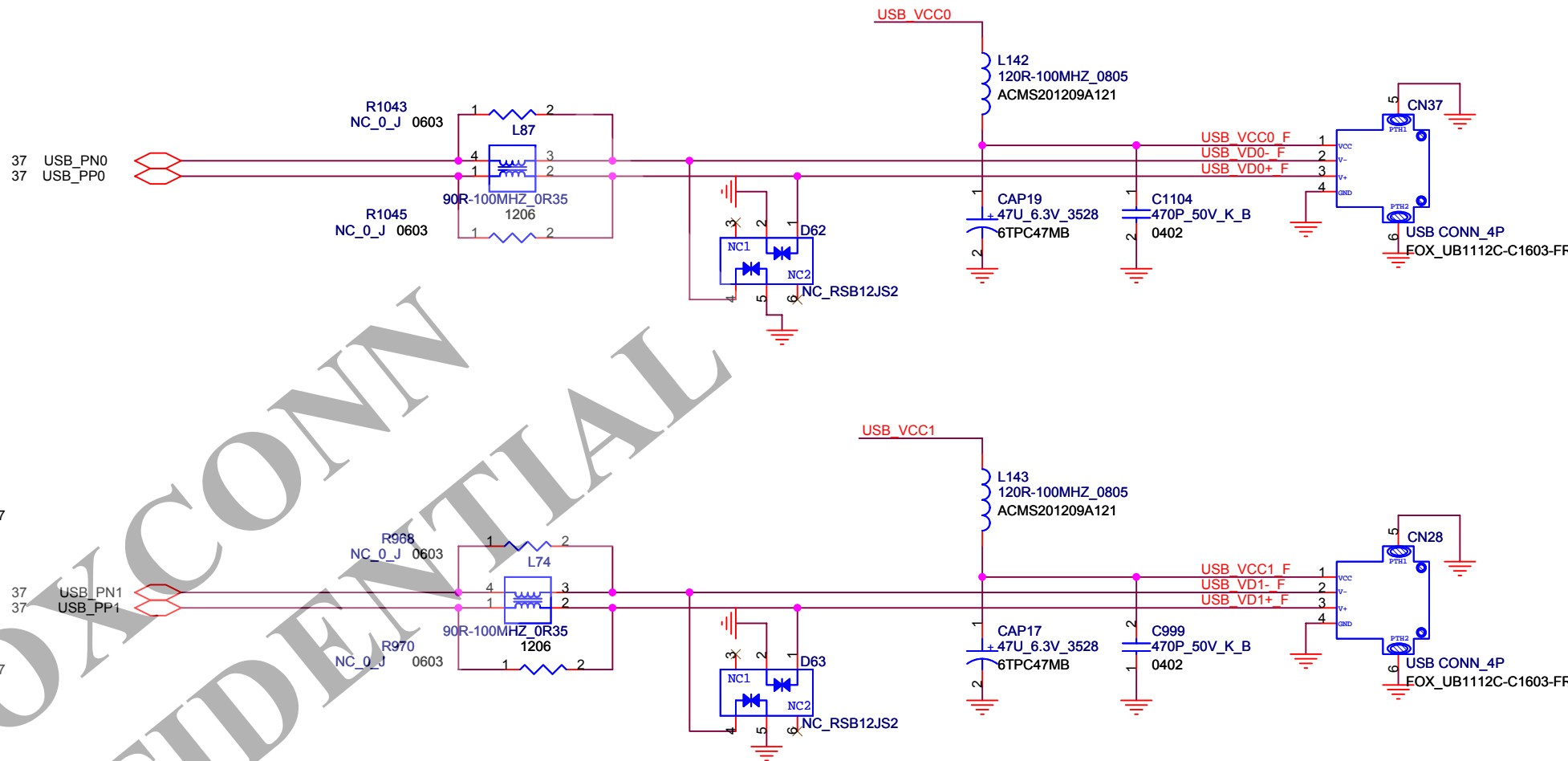
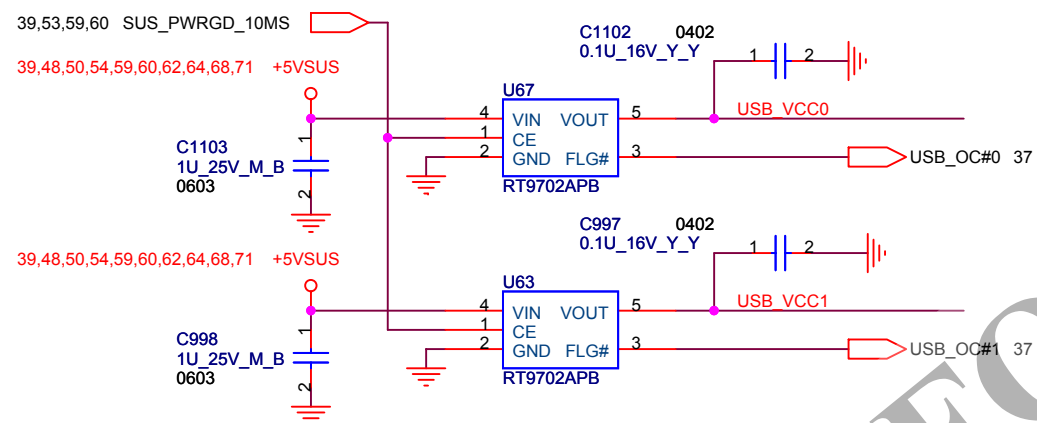


FOXCONN CONFIDENTIAL



Default for S3 waking up event ,
backup for S4 waking up event

USB CONN X 2

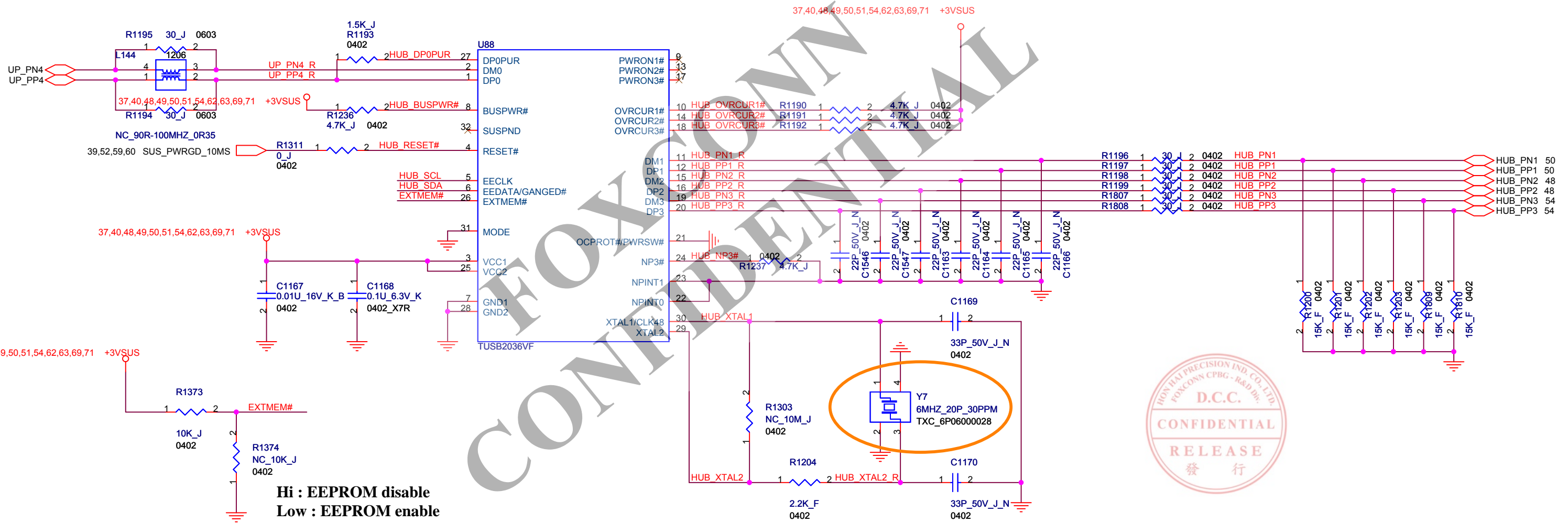


FOXCONN CONFIDENTIAL



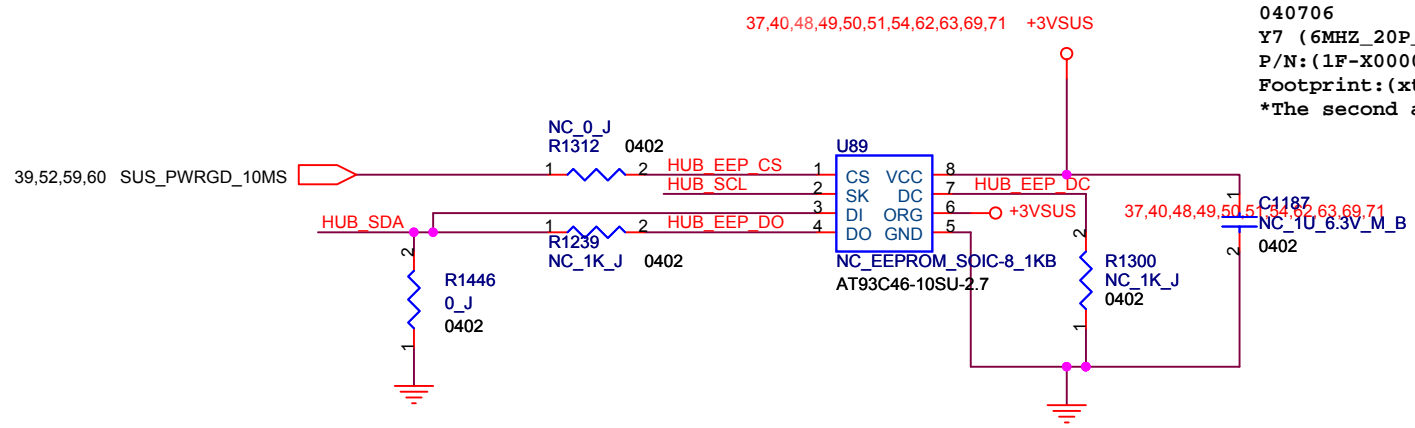
FOXCONN HON HAI Precision Ind. Co., Ltd.		
CCPBG - R&D Division		
Title USB2.0/DOCKING CONN.		
Size A3	Document Number (MS20-1-01) MainBoard (MBX-156)	Rev 1.00
Date: Friday, April 14, 2006	Sheet 52	of 80

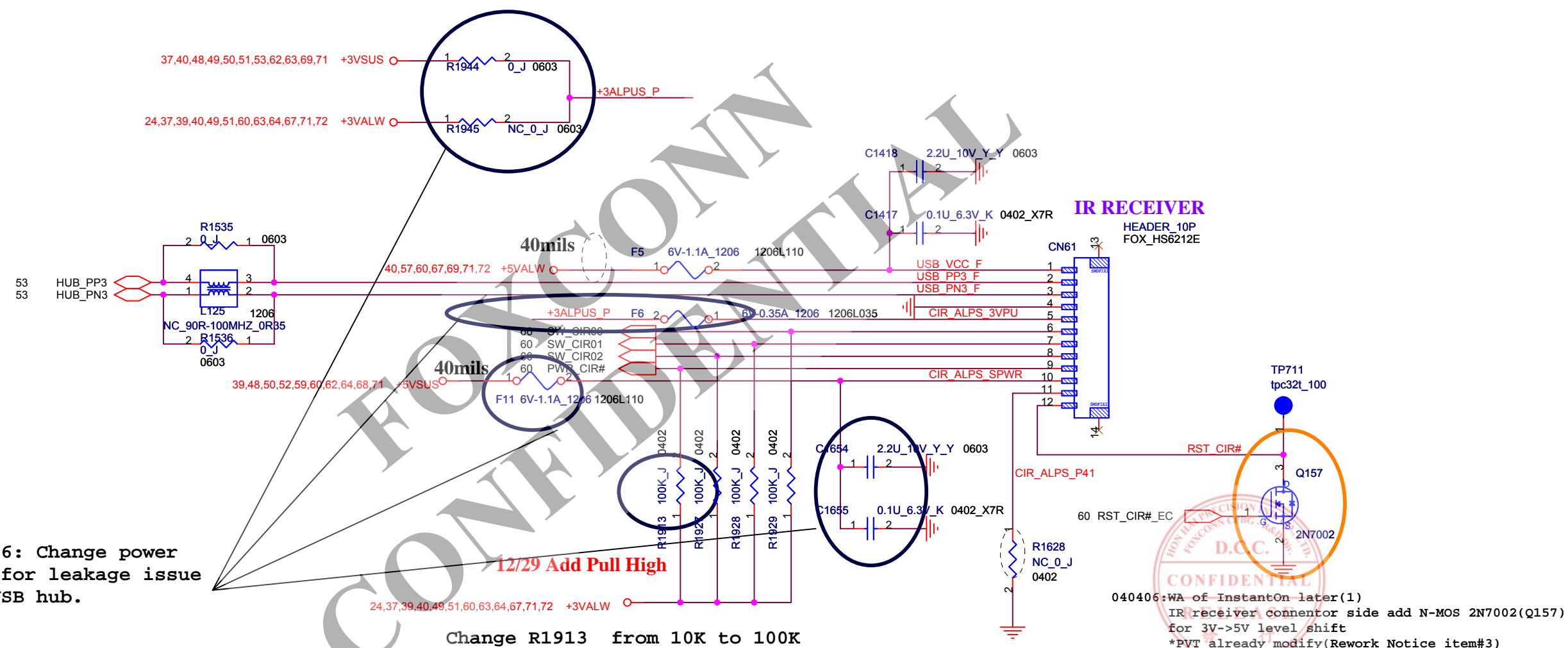
Application design in datasheet 27 ohm;
but 30ohm is also in range of USB Spec.



Hi : EEPROM disable
Low : EEPROM enable

040706
Y7 (6MHZ_20P_30PPM)change part number from secondsource to main source(buyer request)
P/N: (1F-X00006M-3001(AKER) ->1F-X00006M-3002(TXE)
Footprint:(xtal_4p_244_284x205 -> xtal_4p_232_276x197)
*The second already verify on DVT & PVT





030106: Change power plan for leakage issue of USB hub.

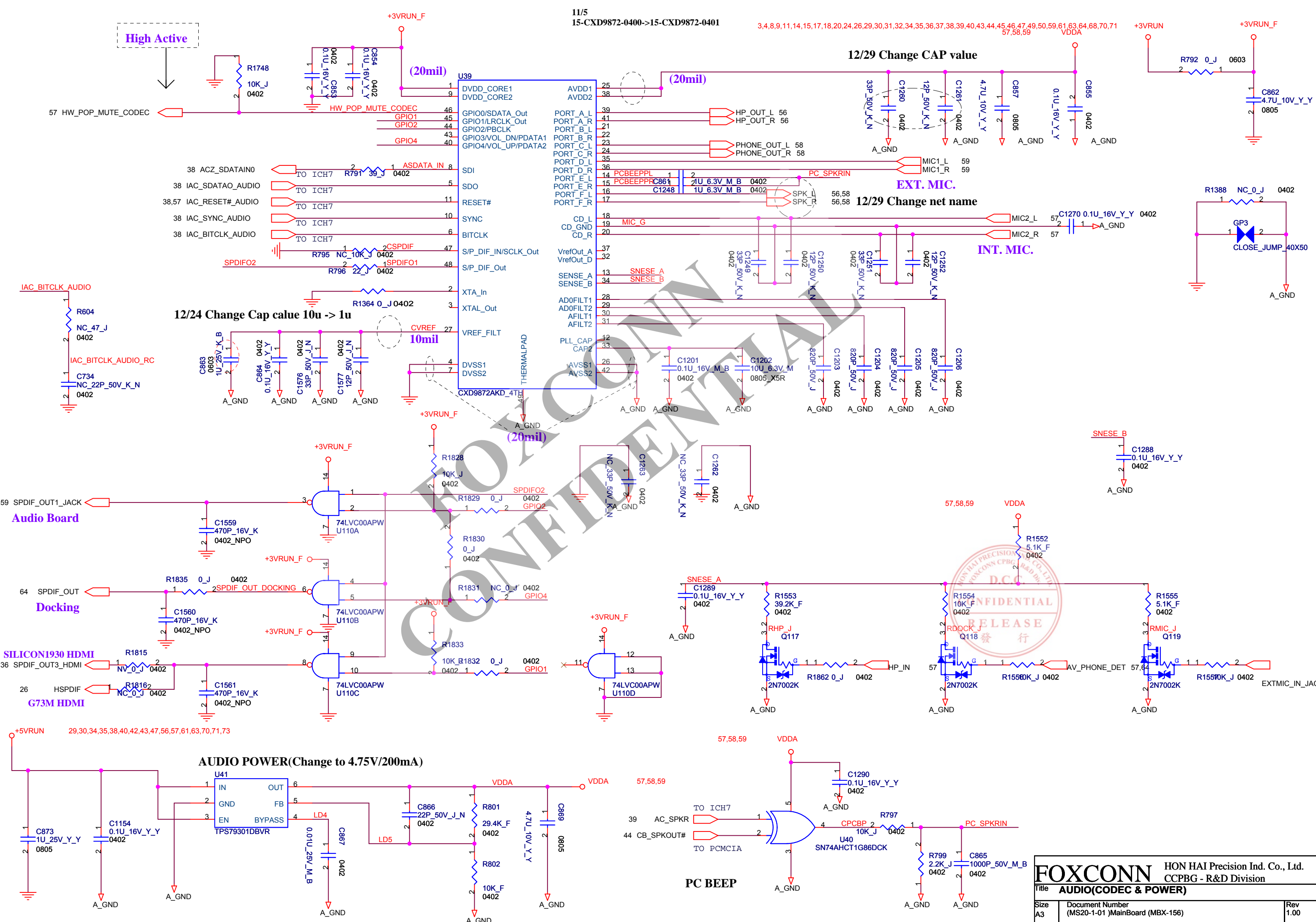
Change R1913 from 10K to 100K

12/29 Add Pull High

040406: WA of InstantOn later(1)
 IR receiver connentor side add N-MOS 2N7002(Q157) for 3V->5V level shift
 *PVT already modify(Rework Notice item#3)

- USB_VCC_F 1 TP847 tpc32t_100
- USB_PP3_F 1 TP848 tpc32t_100
- USB_PN3_F 1 TP849 tpc32t_100
- CIR_ALPS_3VPU 1 TP850 tpc32t_100
- SW_CIR00 1 TP851 tpc32t_100
- SW_CIR01 1 TP852 tpc32t_100
- SW_CIR02 1 TP853 tpc32t_100
- PWR_CIR# 1 TP854 tpc32t_100
- CIR_ALPS_SPWR 1 TP855 tpc32t_100
- CIR_ALPS_P41 1 TP856 tpc32t_100

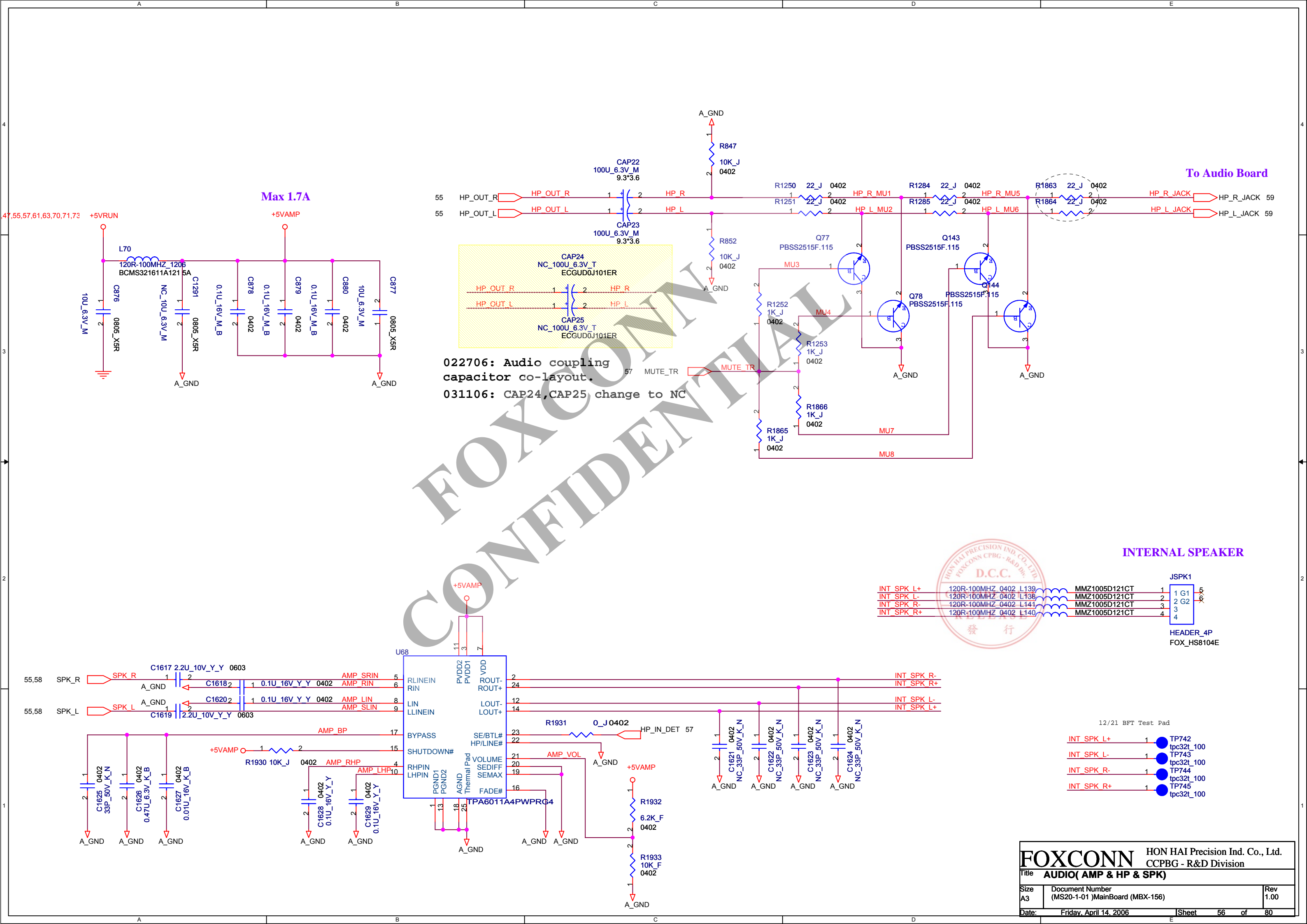
High Active



FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: **AUDIO(CODEC & POWER)**

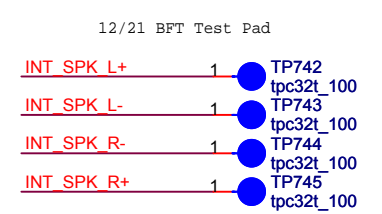
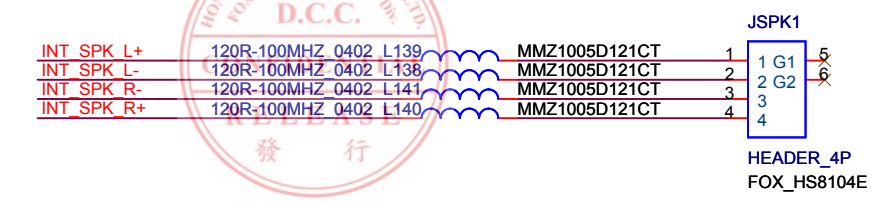
Size: A3	Document Number: (MS20-1-01) MainBoard (MBX-156)	Rev: 1.00
Date: Friday, April 14, 2006	Sheet: 55	of 80



Max 1.7A

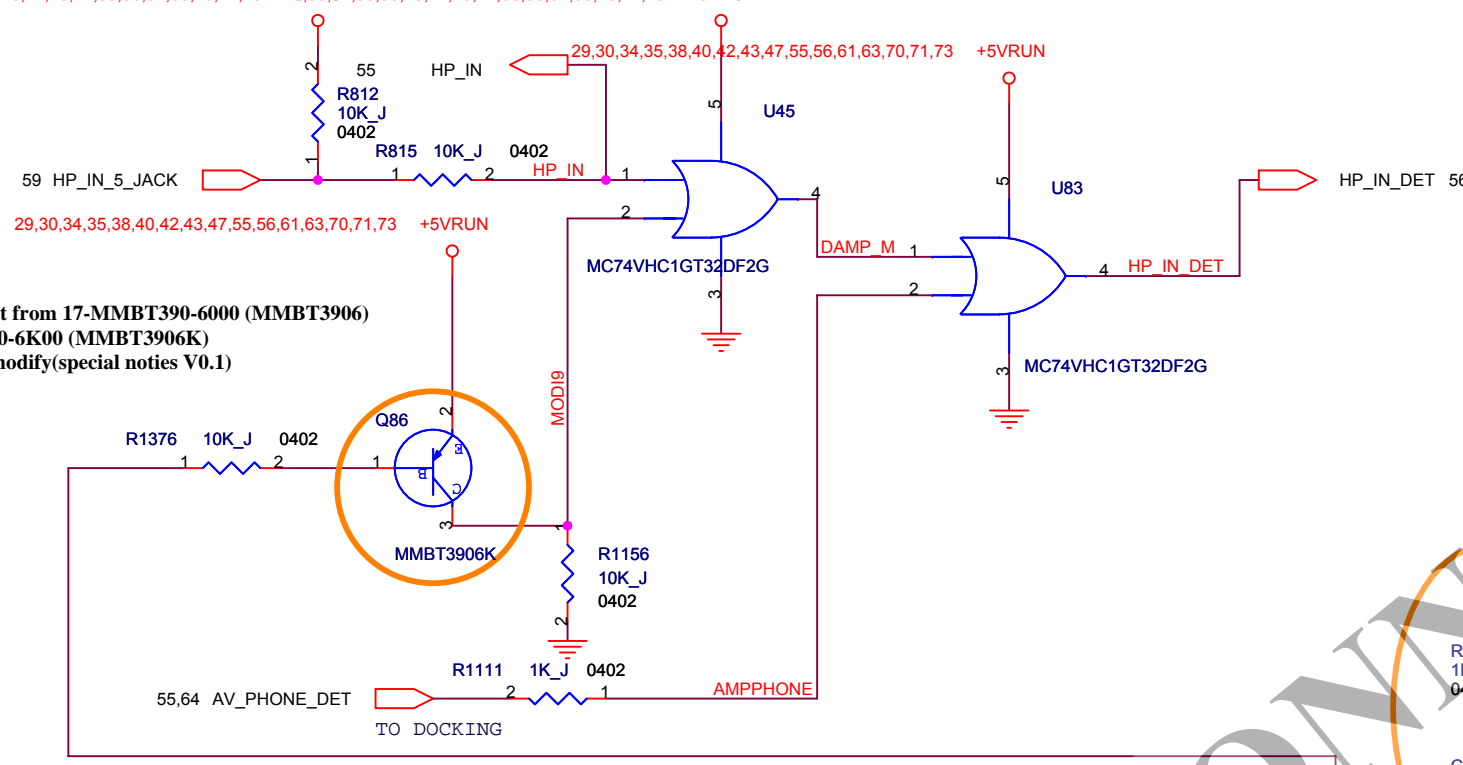
022706: Audio coupling capacitor co-layout.
 031106: CAP24, CAP25 change to NC

INTERNAL SPEAKER

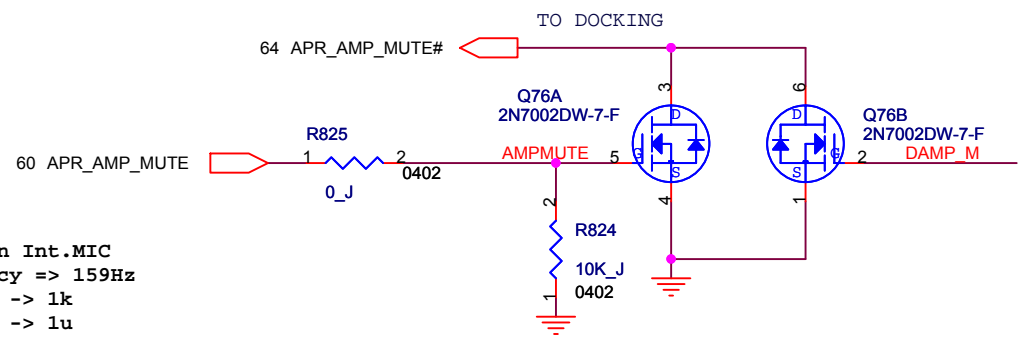


29,30,34,35,38,40,42,43,47,55,56,61,63,70,71,73 +5VRUN

040506
Q86 change part from 17-MMBT390-6000 (MMBT3906)
to 17-MMBT390-6K00 (MMBT3906K)
*PVT already modify(special noties V0.1)

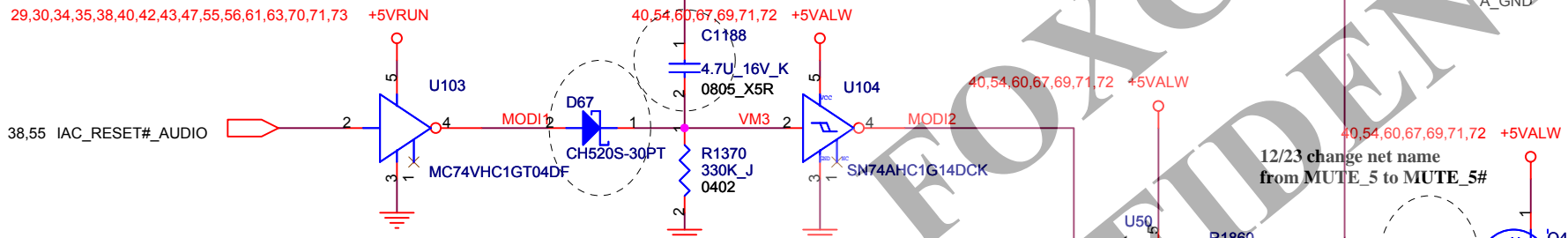


040606 FAN Noise on Int.MIC
(1)Cut-off frequency => 159Hz
R1319 : 2.2k -> 1k
C1232 : 2.2u -> 1u
(2)Cut-off frequency =>7.2kHz
R1318: 22k -> 10k
C1230: 220p -> 2200p
*MOR Nishio-san suggest 3/31



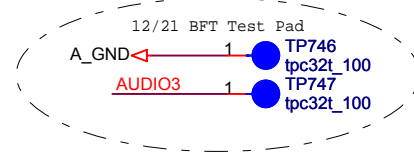
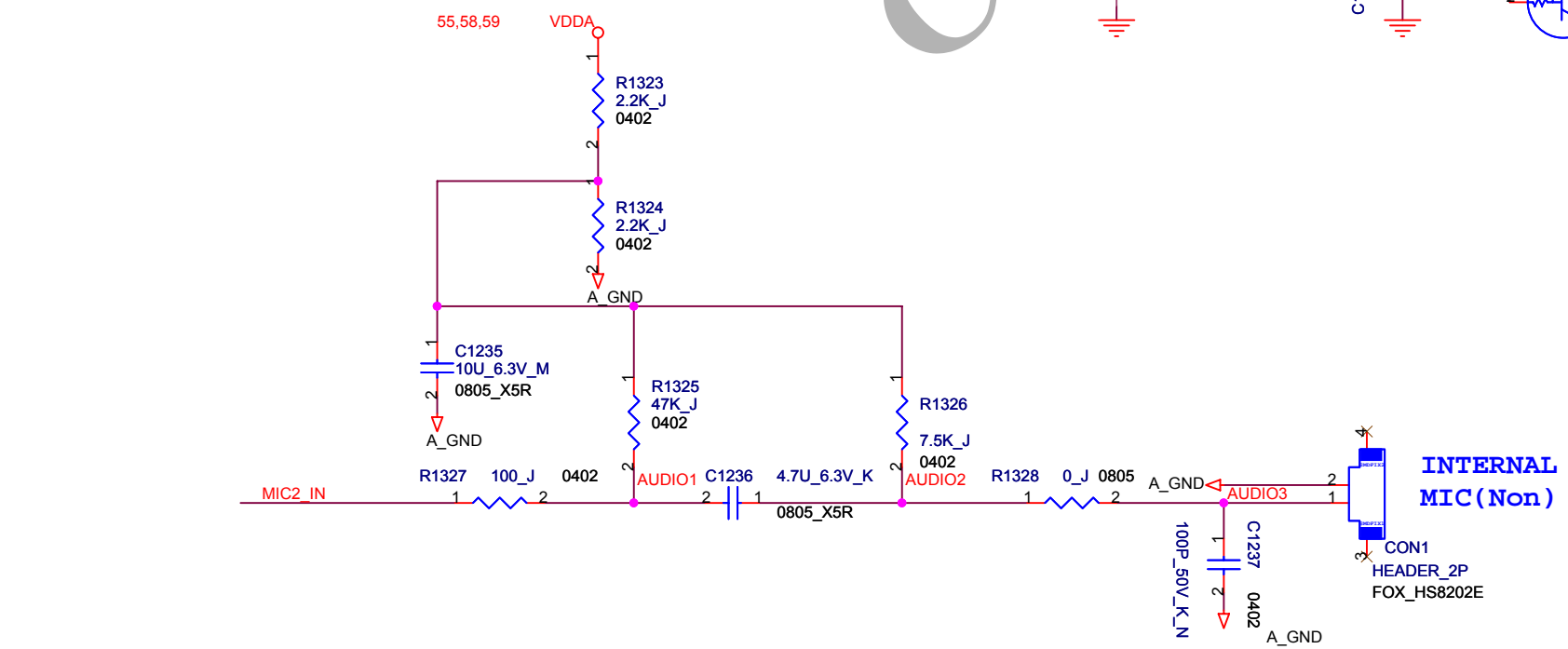
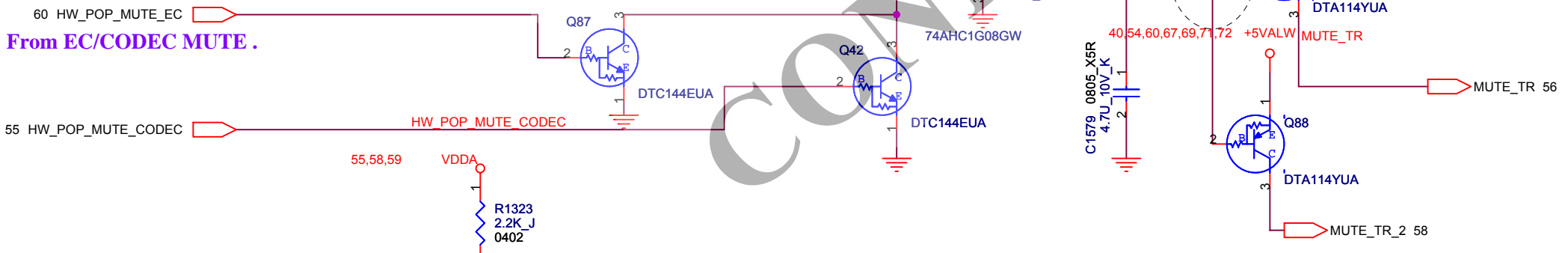
12/24 change part
from 16-ASKS020-3S00 to 16-CH520S3-0P00

12/5 modify capacitor value



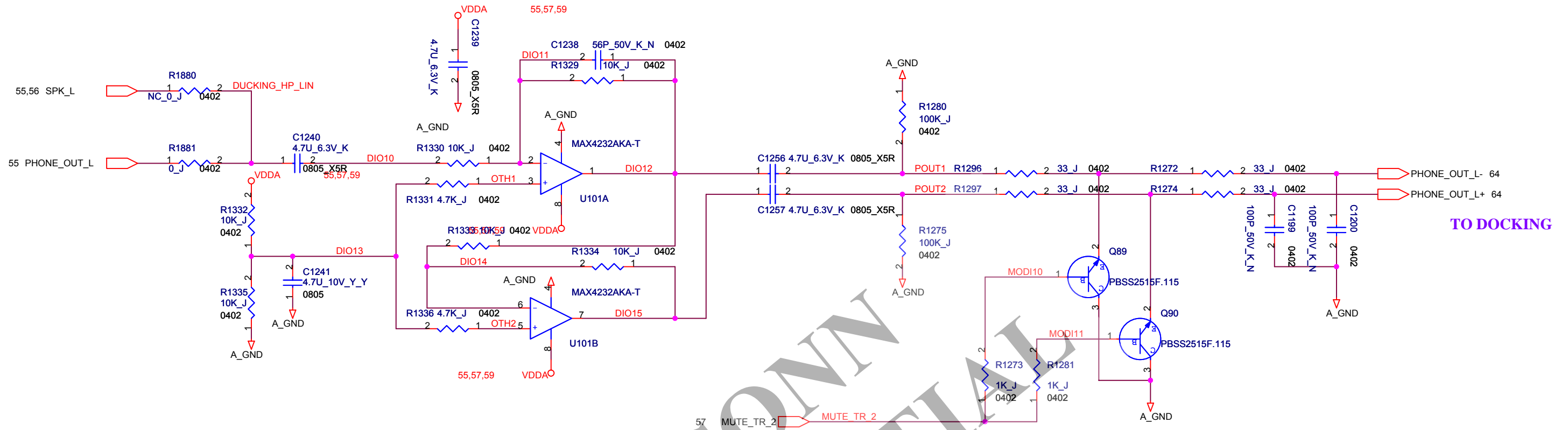
Delay 100-200 ms

12/23 change net name
from MUTE_5 to MUTE_5#

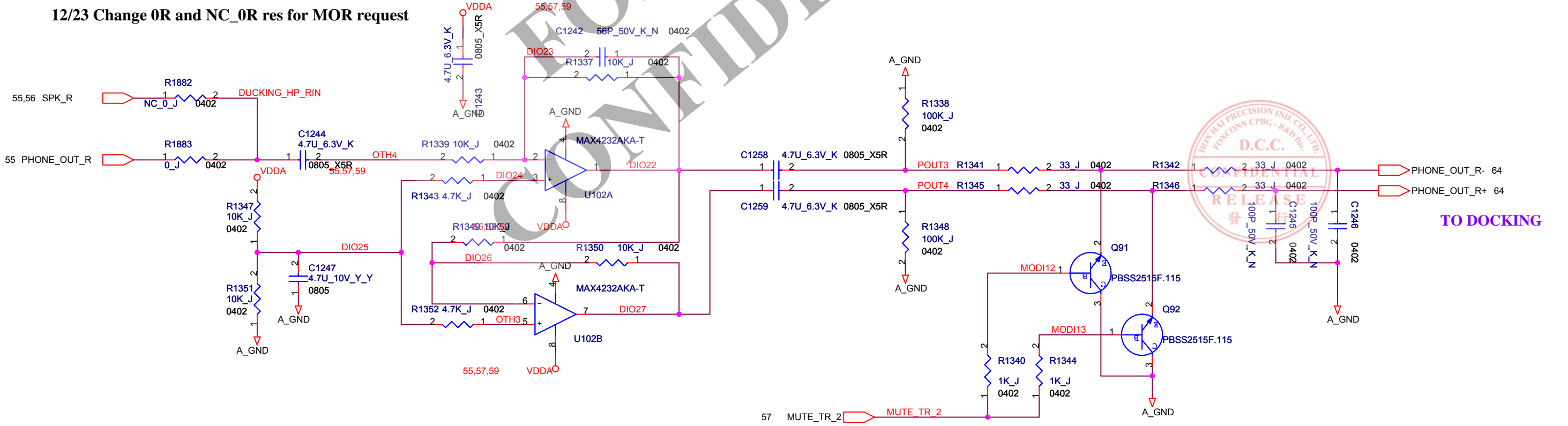


FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title AUDIO (MUTE & INTMIC)		
Size A3	Document Number (MS20-1-01)MainBoard (MBX-156)	Rev 1.00
Date: Friday, April 14, 2006	Sheet 57	of 80

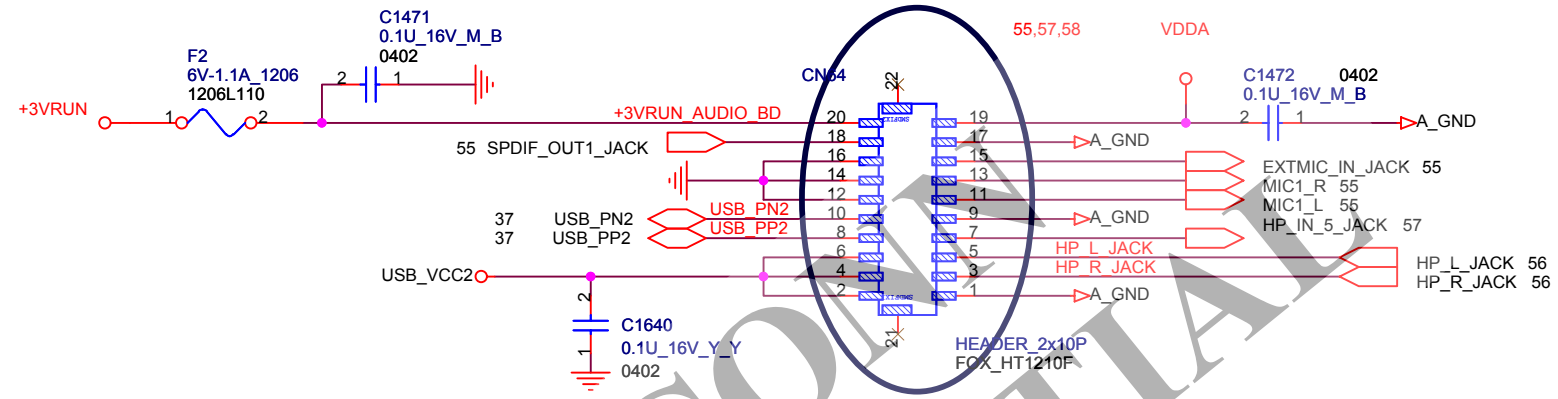
PHONE OUT



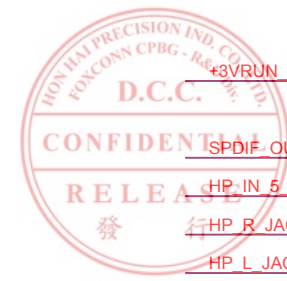
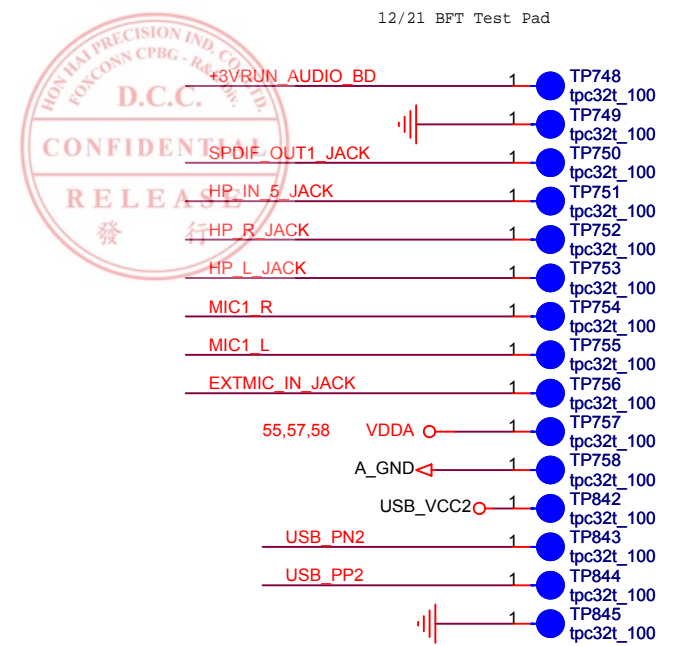
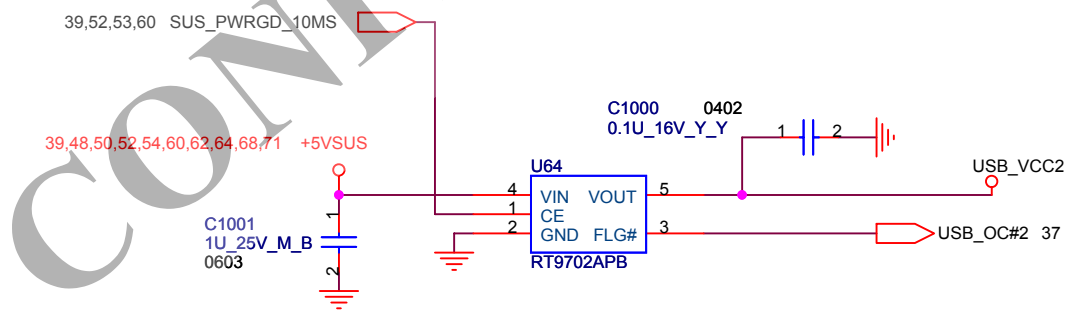
12/23 Change 0R and NC_0R res for MOR request

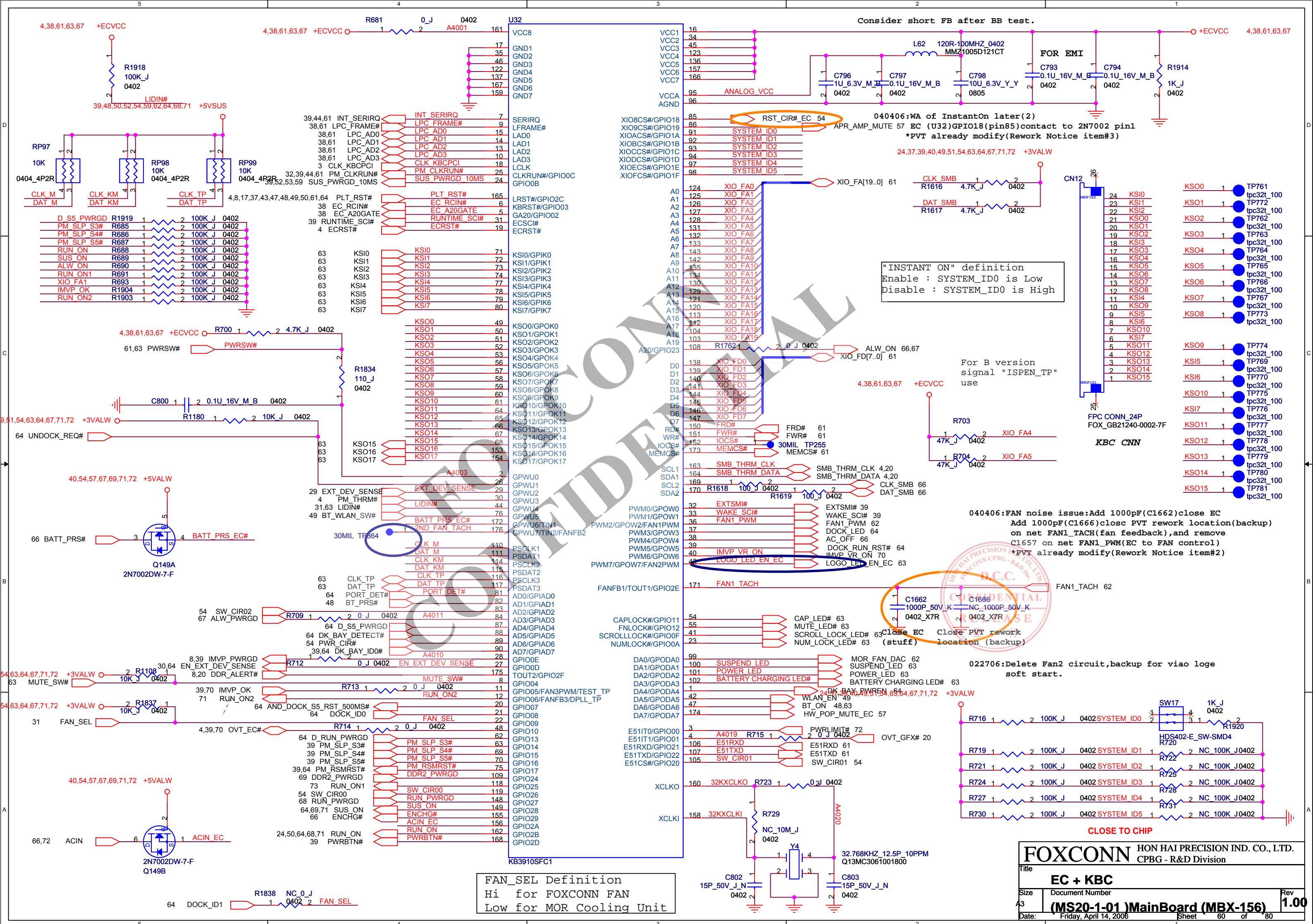


21,24,26,29,30,31,32,34,35,36,37,38,39,40,43,44,45,46,47,49,50,55,61,63,64,68,70,71



030706: Change CN64 PIN16 from +3VSUS to GND
 and change PIN6 from USB_PP2 to USB_VCC2.
 Shift Pin 6&8 to Pin 8&10.
 Delet F9 and C1641.





FAN_SEL Definition
 Hi for FOXCONN FAN
 Low for MOR Cooling Unit

"INSTANT ON" definition
 Enable : SYSTEM_ID0 is Low
 Disable : SYSTEM_ID0 is High

040406:FAN noise issue:Add 1000pF(C1662)close EC
 Add 1000pF(C1666)close PVT rework location(backup)
 on net FAN1_TACH(fan feedback),and remove
 C1657 on net FAN1_PWM(EC to FAN control)
 *PVT already modify(Rework Notice item#2)

022706:Delete Fan2 circuit,backup for viao loge
 soft start.

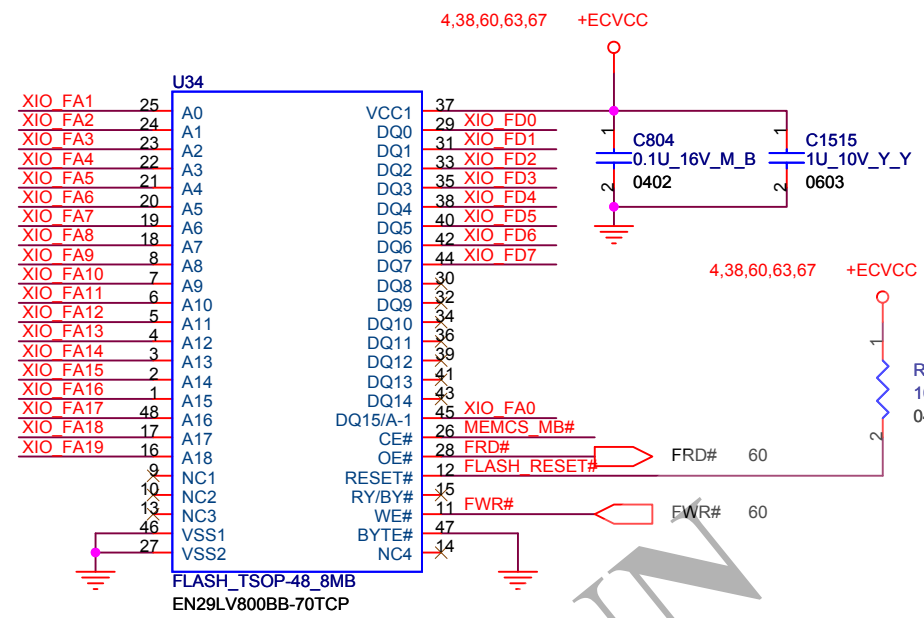
FOXCONN HON HAI PRECISION IND. CO., LTD.
 CPBG - R&D Division

Title: **EC + KBC**

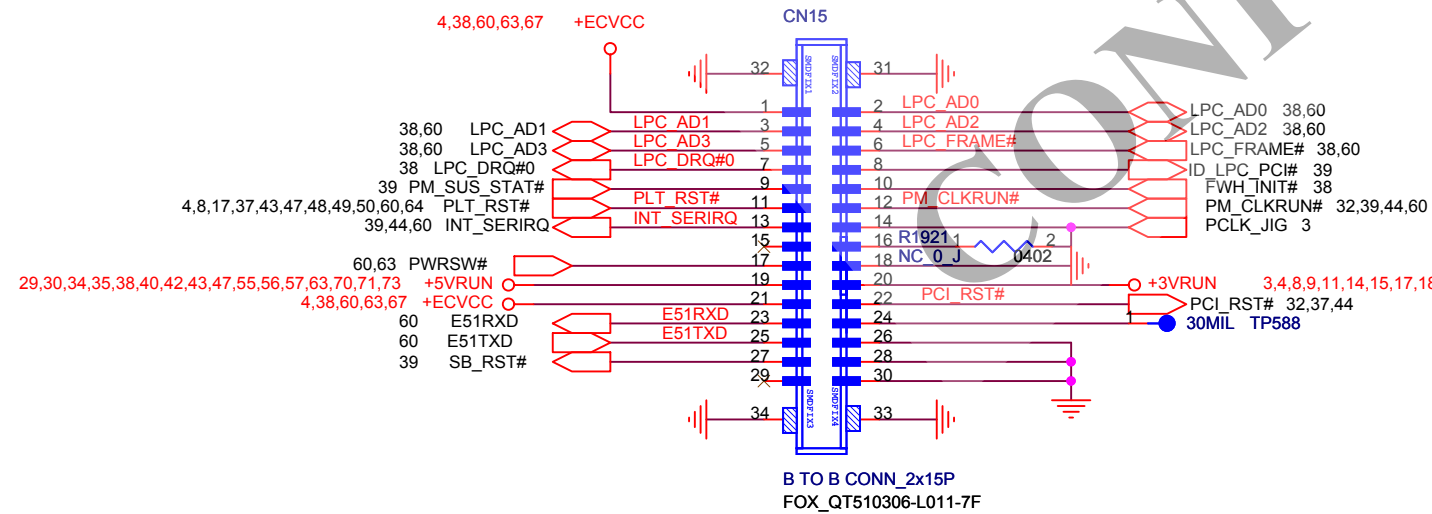
Size: 43 Document Number: **(MS20-1-01) MainBoard (MBX-156)** Rev: 1.00

Date: Friday, April 14, 2006 Sheet: 60 of 80

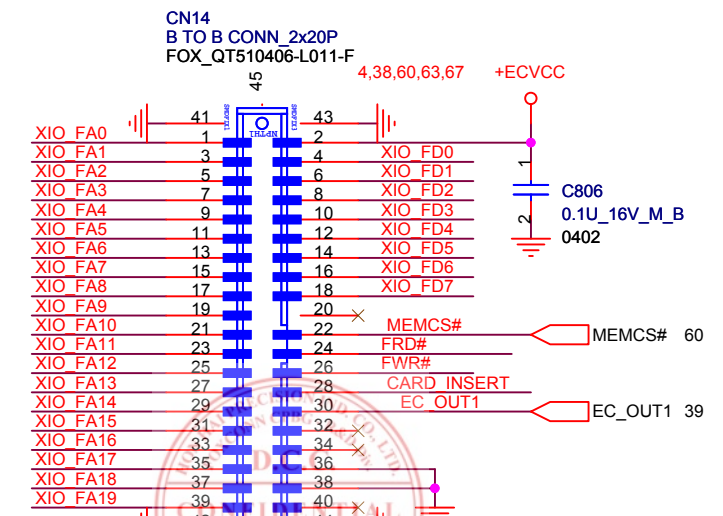
60 XIO_FA[19..0]
60 XIO_FD[7..0]



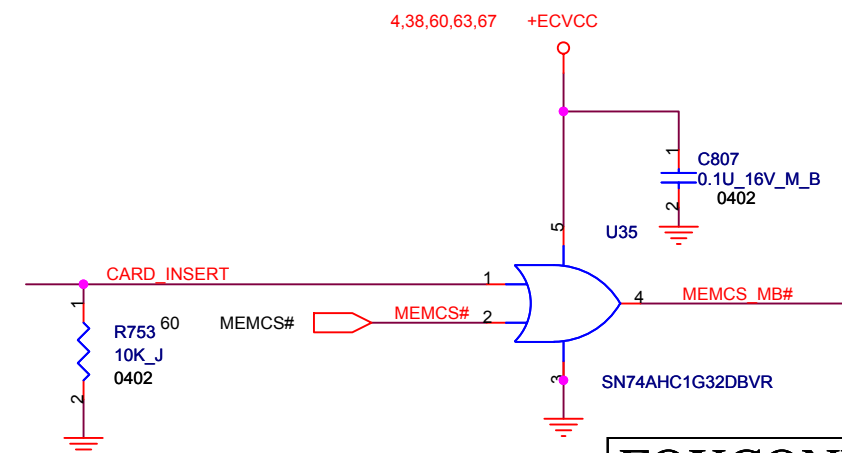
FLASH BIOS



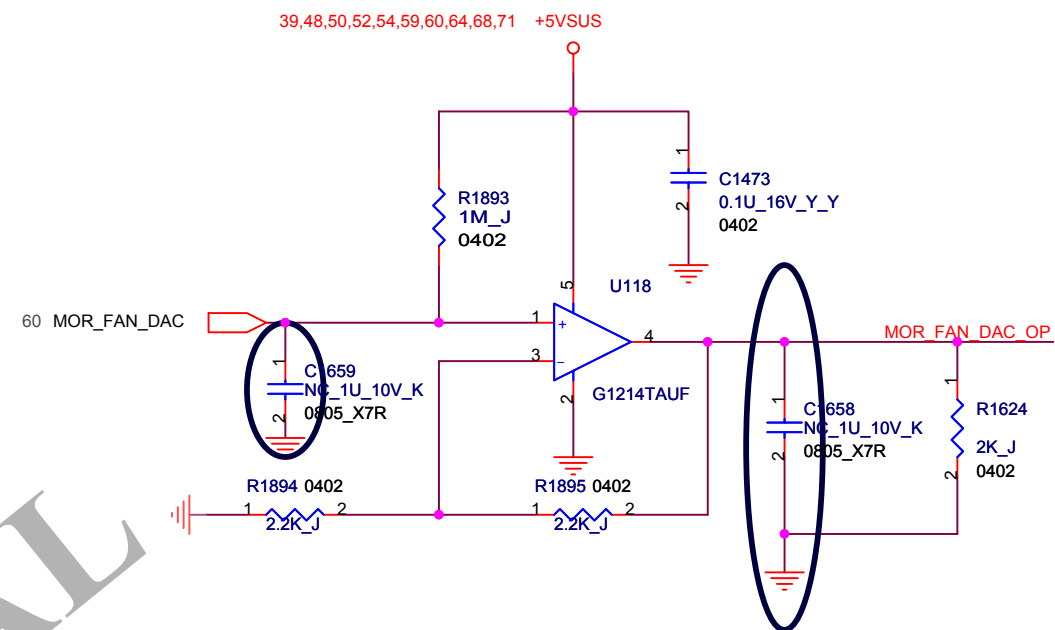
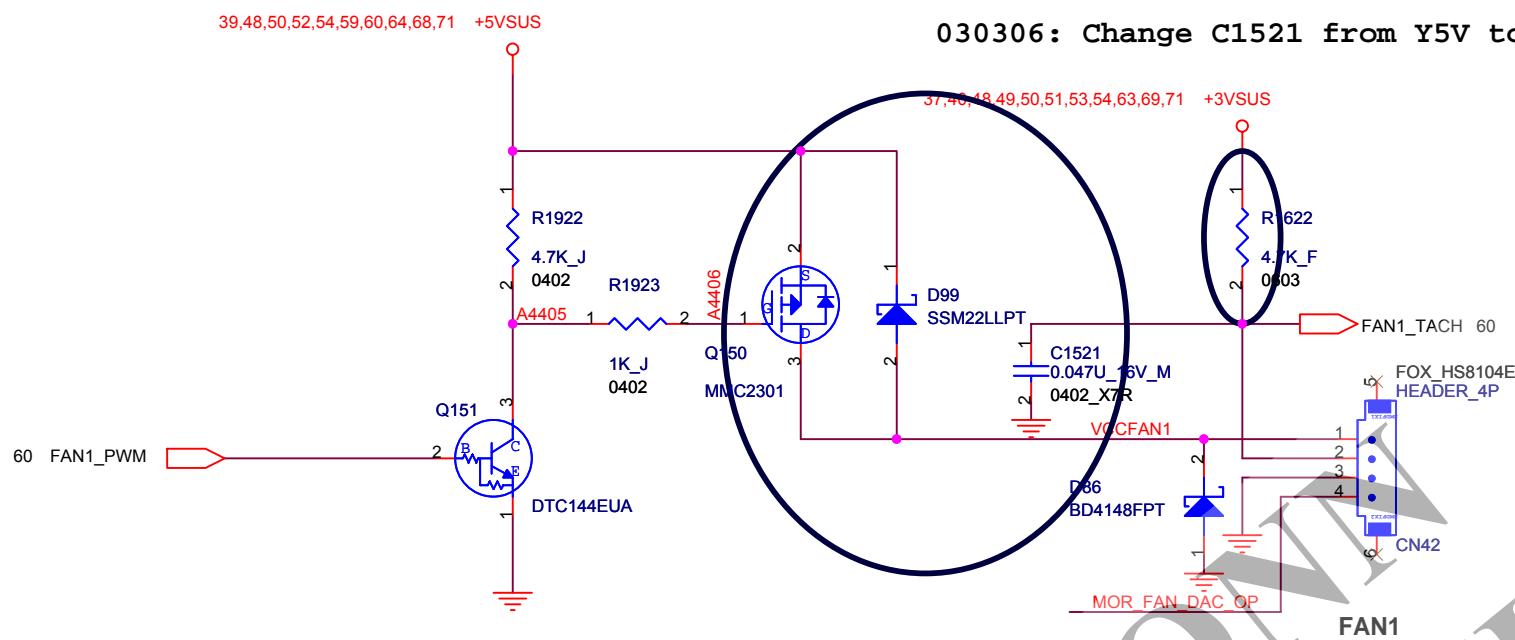
JIG-120



X-BUS



022706: Add doide for inverse current and change pull-high resistor from 10K to 4.7K.



022706: Add capacitor for cooling unit.
031106: C1658 change to NC

- VCCFAN1 1 TP782 tpc32t_100
- FAN1_TACH 1 TP783 tpc32t_100
- MOR_FAN_DAC_OP 1 TP784 tpc32t_100
- MOR_FAN_DAC_OP 1 TP785 tpc32t_100
- TP788 tpc32t_100

030506: Backup Test Pad.

FAN(FAN1+MOR FAN)

CONFIDENTIAL



030306: Delet FAN2 circuit.

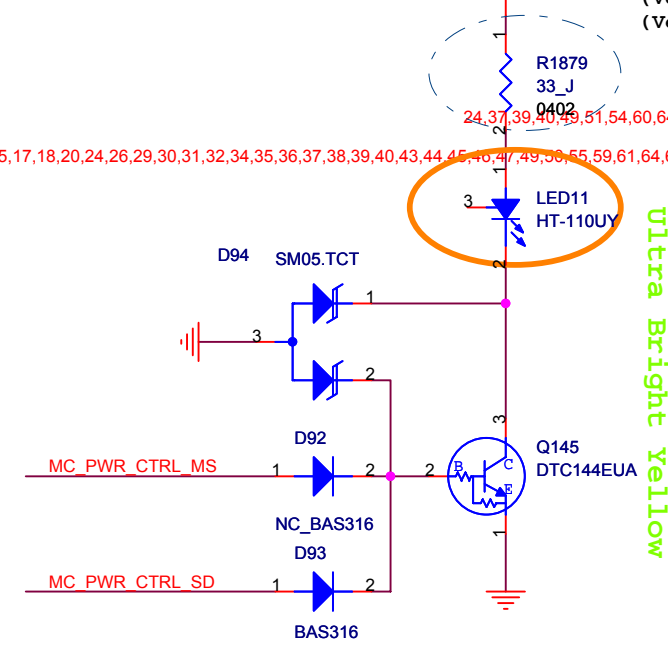
24,37,39,40,49,51,54,60,64,67,71,72 +3VALW

040506 Modify SD LED brightness
LED11 change part from 16-HT110Y0-0000
(Vendor P/N : HT-110Y) to 16-HT110UY-0000.
(Vendor P/N : HT-110UY)

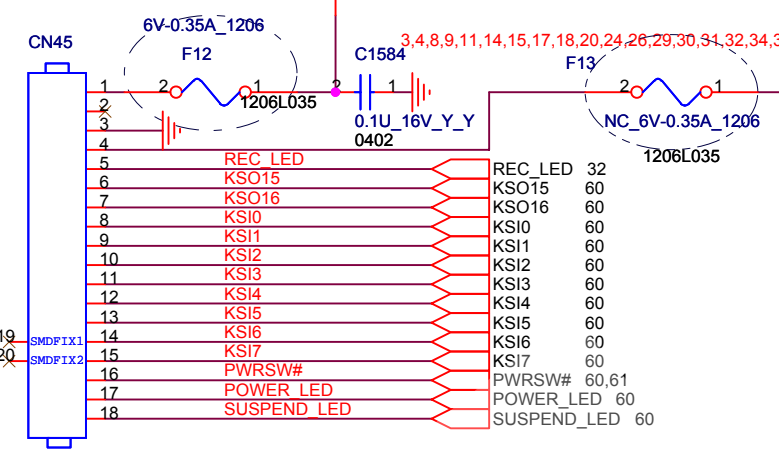
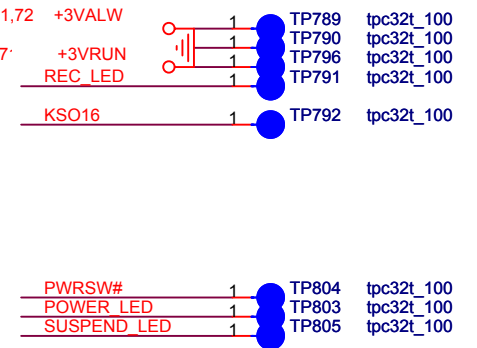
3,4,8,9,11,14,15,17,18,20,24,26,29,30,31,32,34,35,36,37,38,39,40,43,44,45,46,47,49,50,55,59,61,64,68,70,71
24,37,39,40,49,51,54,60,64,67,71,72 +3VALW

+3VRUN

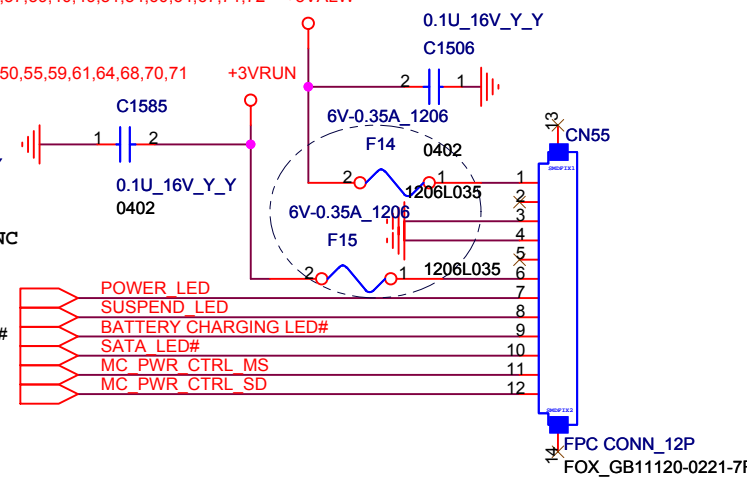
24,37,39,40,49,51,54,60,64,67,71,72 +3VALW



SD LED



FPC BOTTOM CONN_18P 060301: Add 6 fulse for short issue.

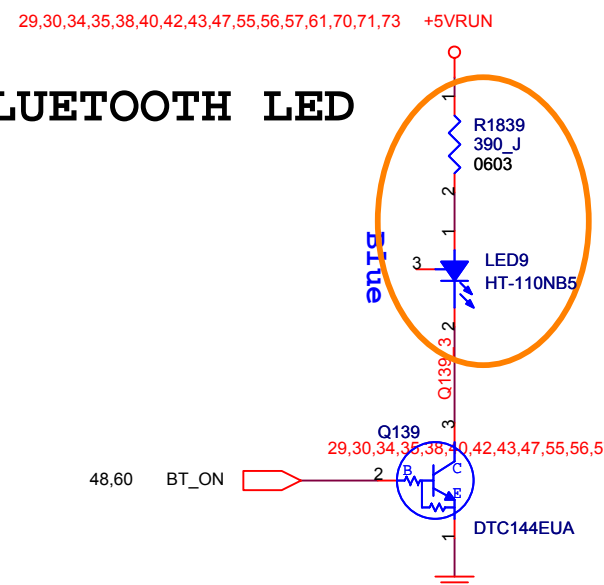


FPC CONN_12P FOX_GB11120-0221-7F

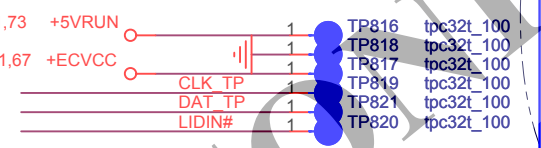
To Power Button Board Connector

To LED Board Connector

BLUETOOTH LED



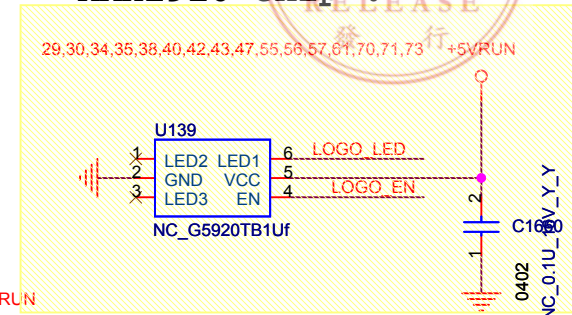
040506 Modify Bluetooth LED brightness
(1) LED9 change part from 16-HT110NB-0000
(Vendor P/N : HT-110NB) to 16-HT110NB-5000.
(Vendor P/N : HT-110NB5) (The same with MS10)
(2) R1839 change part from 1R-0000201-J200
(200ohm,5%,0402) to 1R-0000391-J300.
(390 ohm,5%,0603) (The same with MS10)



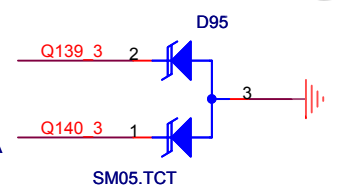
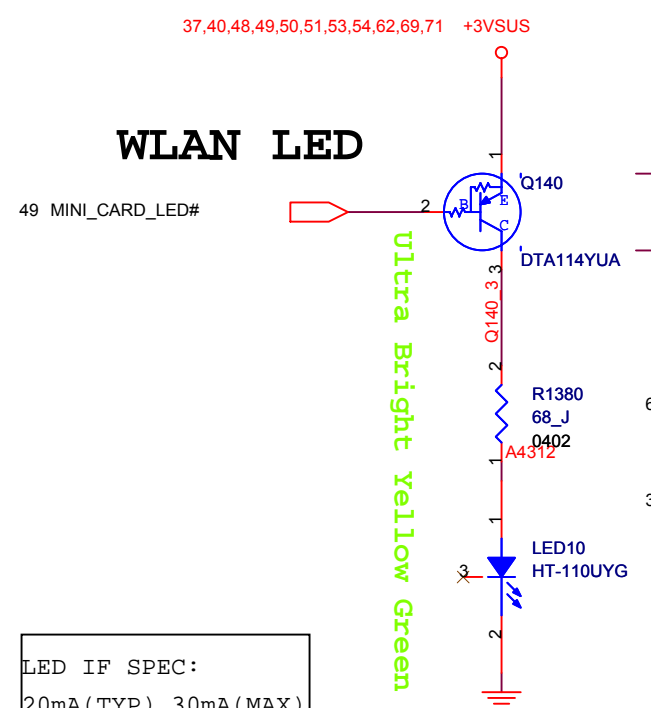
030306: Change S/N from 1N-0010000-M0X0 to 1N-0010000-MWG0.

To Touch Pad Board Connector

030306: Backup for MAX1916 chip



WLAN LED



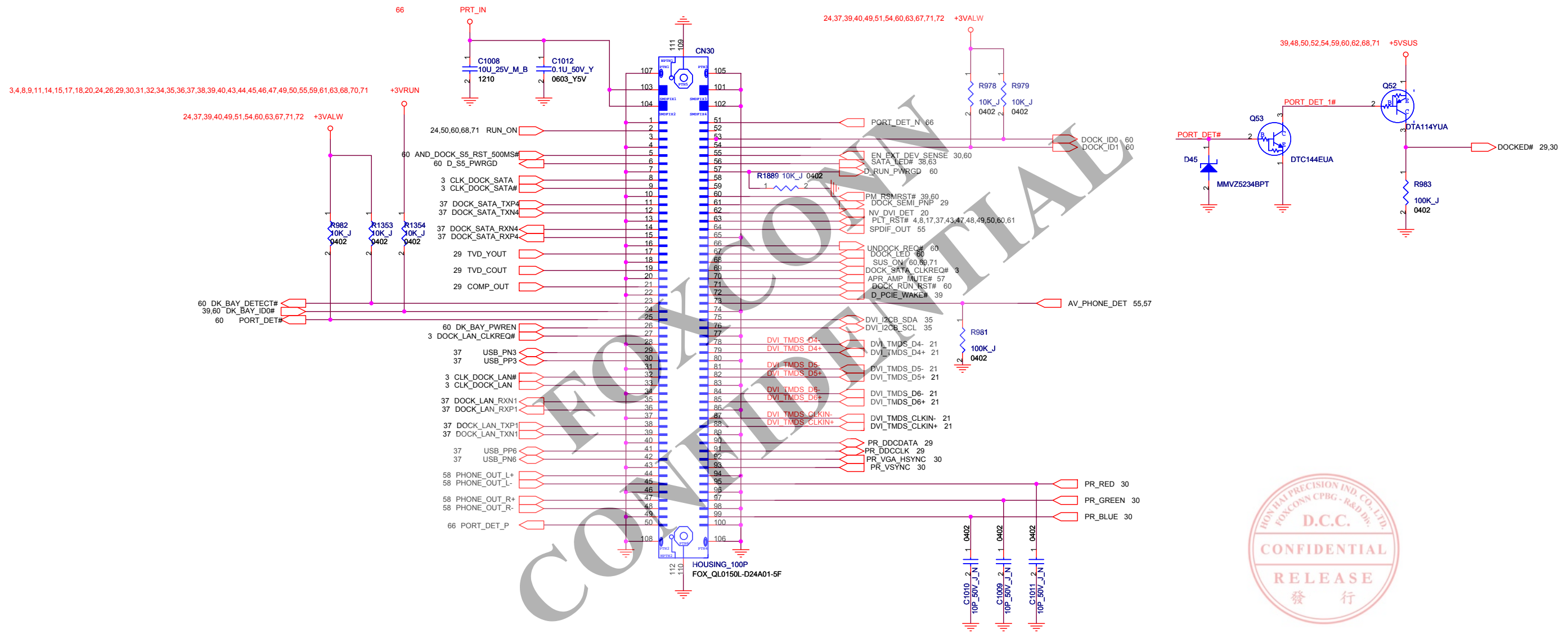
030906: Add two 0ohm resistors for Viao loge soft start issue.

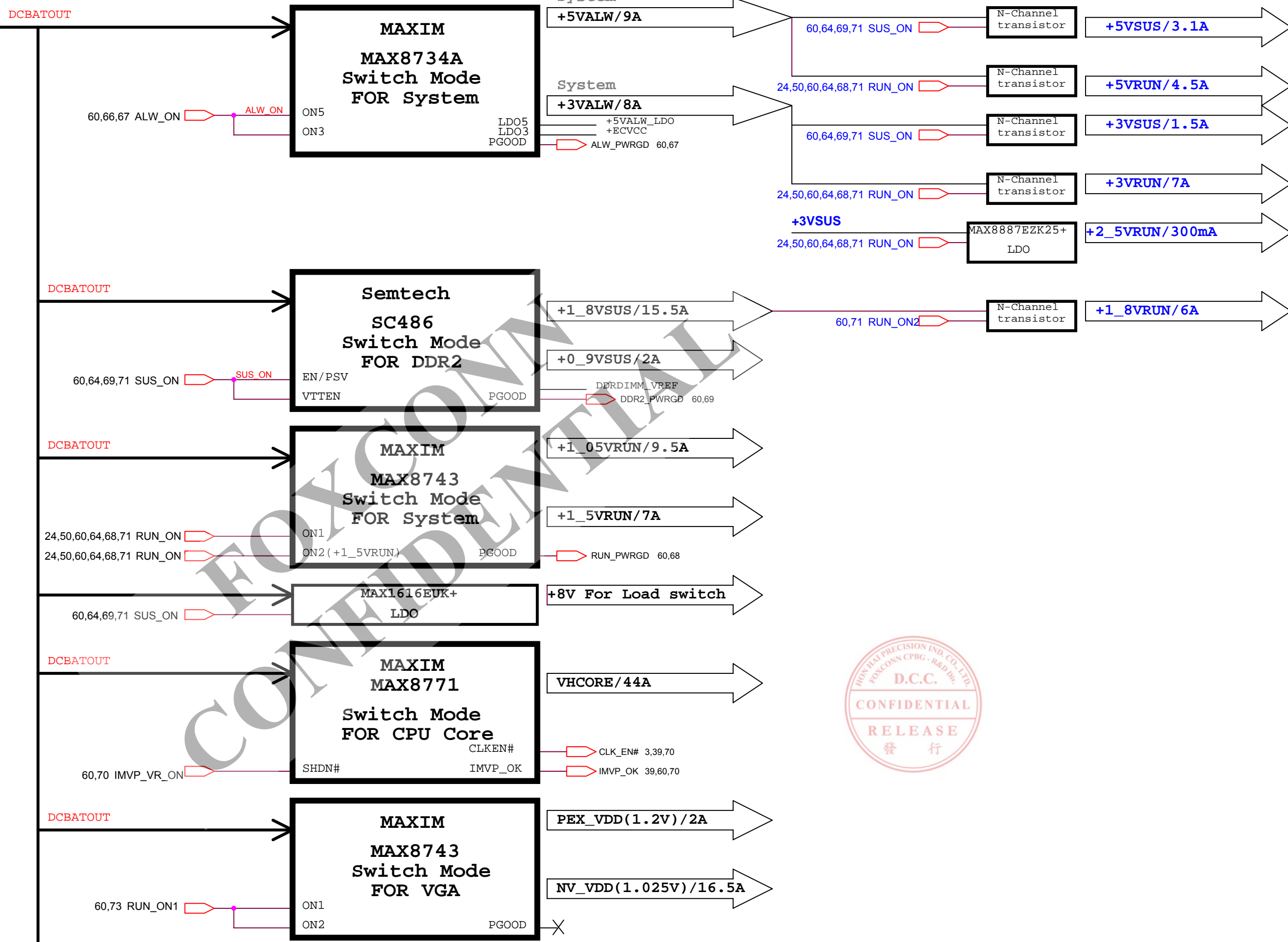
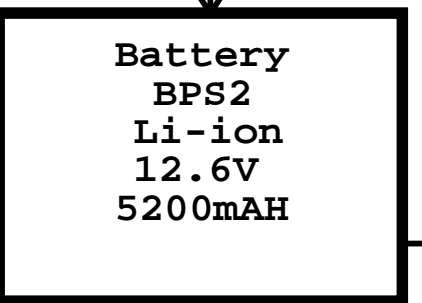
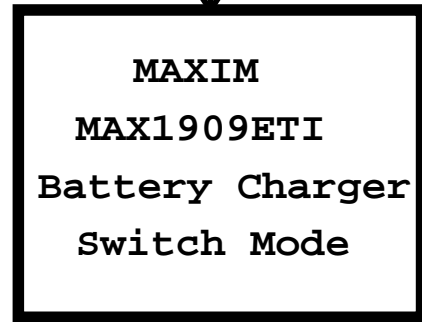
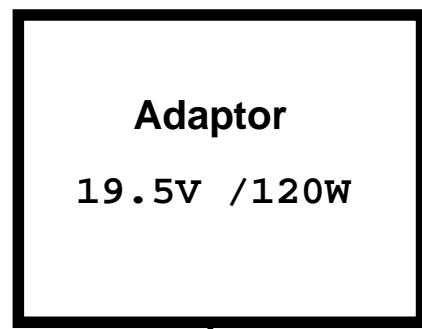
SONY LOGO LED

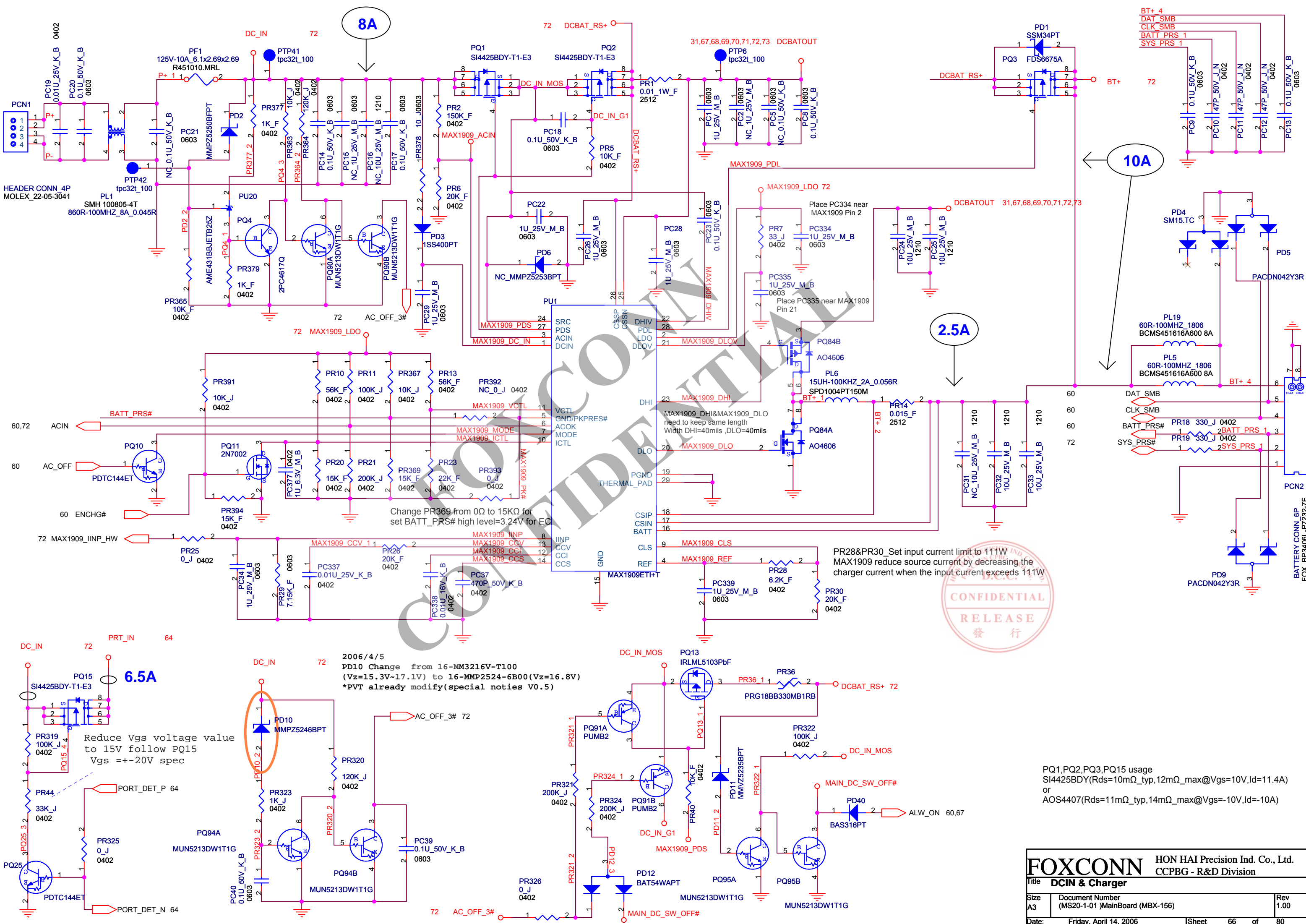
To AV Function Board Connector

LED IF SPEC:
20mA (TYP) , 30mA (MAX)

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
Title: POWER BD + HOT KEY BD + T/P&LED BD + LOGO LED
Size: 43
Date: Friday, April 14, 2006
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Rev: 1.00







8A

10A

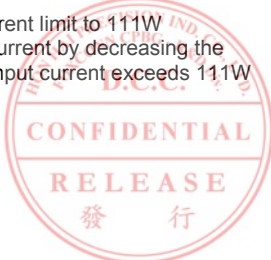
2.5A

6.5A

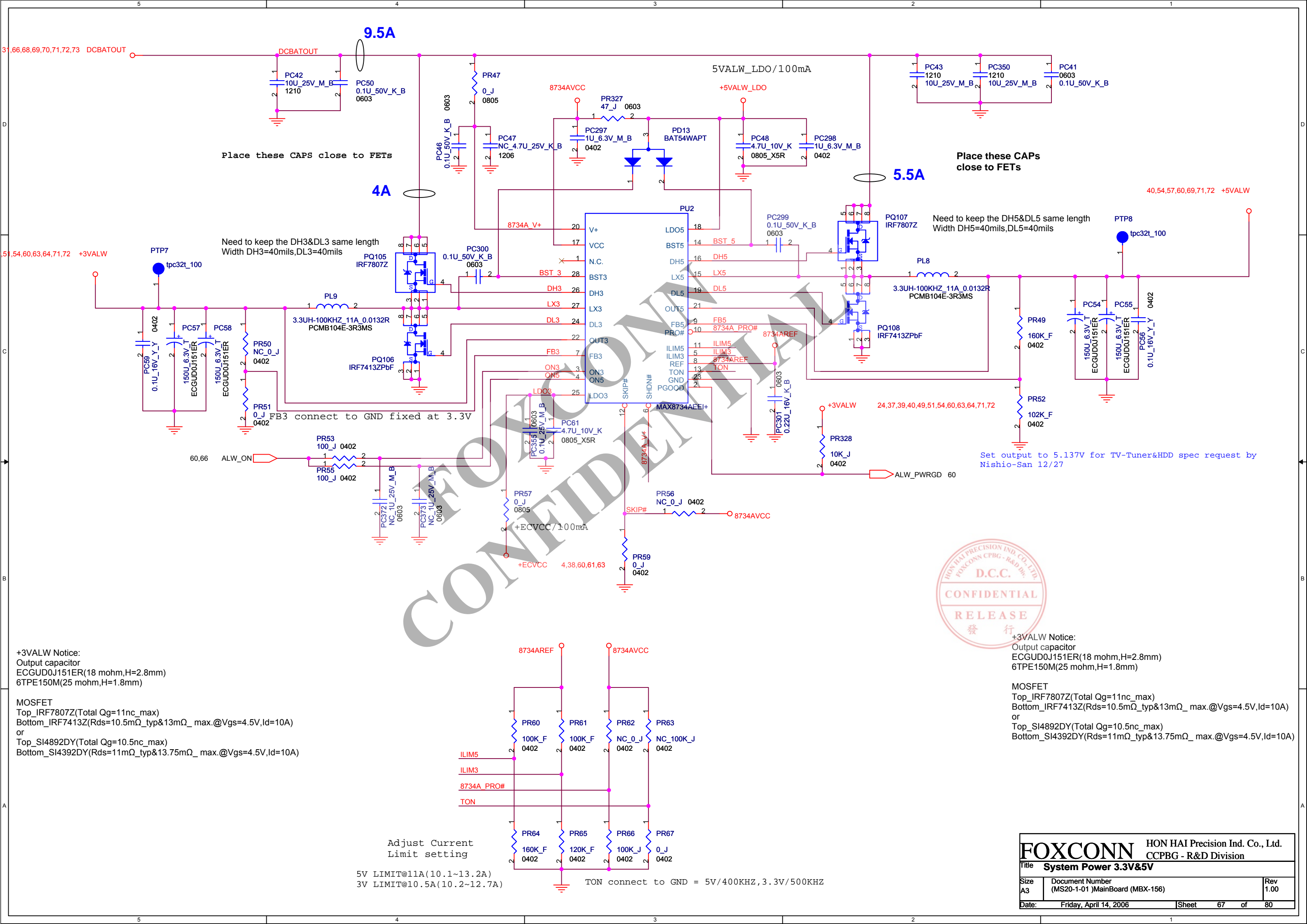
2006/4/5
 PD10 Change from 16-MM3216V-T100 (Vz=15.3V~17.1V) to 16-MMP2524-6B00 (Vz=16.8V)
 *PVT already modify (special notices V0.5)

Reduce Vgs voltage value to 15V follow PQ15
 Vgs = +-20V spec

PR28&PR30_Set input current limit to 111W
 MAX1909 reduce source current by decreasing the charger current when the input current exceeds 111W



PQ1,PQ2,PQ3,PQ15 usage
 SI4425BDY (Rds=10mQ_typ, 12mQ_max@Vgs=10V, Id=11.4A)
 or
 AOS4407 (Rds=11mQ_typ, 14mQ_max@Vgs=-10V, Id=-10A)



Place these CAPS close to FETs

Place these CAPS close to FETs

Need to keep the DH3&DL3 same length
Width DH3=40mils,DL3=40mils

Need to keep the DH5&DL5 same length
Width DH5=40mils,DL5=40mils

+3VALW Notice:
Output capacitor
ECGUD0J151ER(18 mohm,H=2.8mm)
6TPE150M(25 mohm,H=1.8mm)

MOSFET
Top_IRF7807Z(Total Qg=11nc_max)
Bottom_IRF7413Z(Rds=10.5mΩ_typ&13mΩ_max.@Vgs=4.5V,Id=10A)
or
Top_SI4892DY(Total Qg=10.5nc_max)
Bottom_SI4392DY(Rds=11mΩ_typ&13.75mΩ_max.@Vgs=4.5V,Id=10A)

+3VALW Notice:
Output capacitor
ECGUD0J151ER(18 mohm,H=2.8mm)
6TPE150M(25 mohm,H=1.8mm)

MOSFET
Top_IRF7807Z(Total Qg=11nc_max)
Bottom_IRF7413Z(Rds=10.5mΩ_typ&13mΩ_max.@Vgs=4.5V,Id=10A)
or
Top_SI4892DY(Total Qg=10.5nc_max)
Bottom_SI4392DY(Rds=11mΩ_typ&13.75mΩ_max.@Vgs=4.5V,Id=10A)

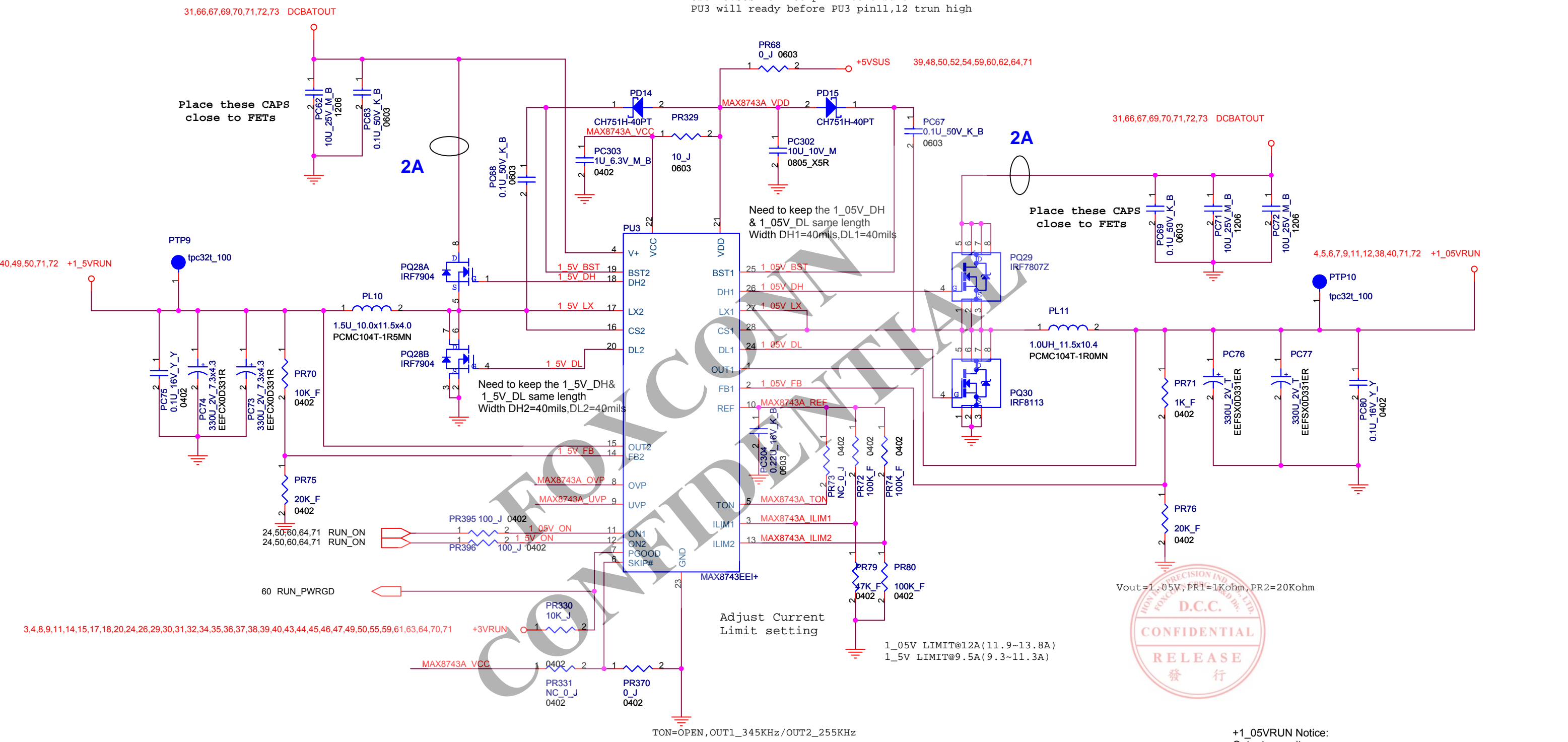
Adjust Current Limit setting
5V LIMIT@11A(10.1~13.2A)
3V LIMIT@10.5A(10.2~12.7A)

TON connect to GND = 5V/400KHZ, 3.3V/500KHZ



FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title System Power 3.3V&5V		
Size A3	Document Number (MS20-1-01) MainBoard (MBX-156)	Rev 1.00
Date: Friday, April 14, 2006	Sheet 67	of 80

Use +5VSUS for PU3 pin21 to ensure
PU3 will ready before PU3 pin11,12 trun high

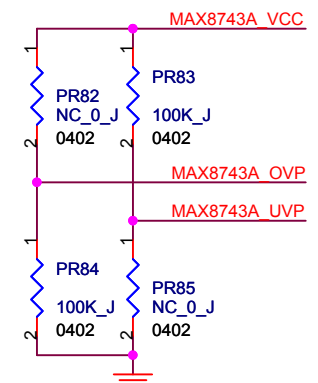


+1_5VRUN Notice:
Output capacitor
EEFCX0D331R(ESR=15 mohm,H=1.9mm,Arms=2.7A)
2R5TPE330MF(ESR=15 mohm,H=1.8mm,Arms=3.1A)

MOSFET(Top+Bottom)
IRF7904(Low side Rds=10.5mΩ_typ,13mΩ_max@Vgs=4.5V,Id=8.9A)

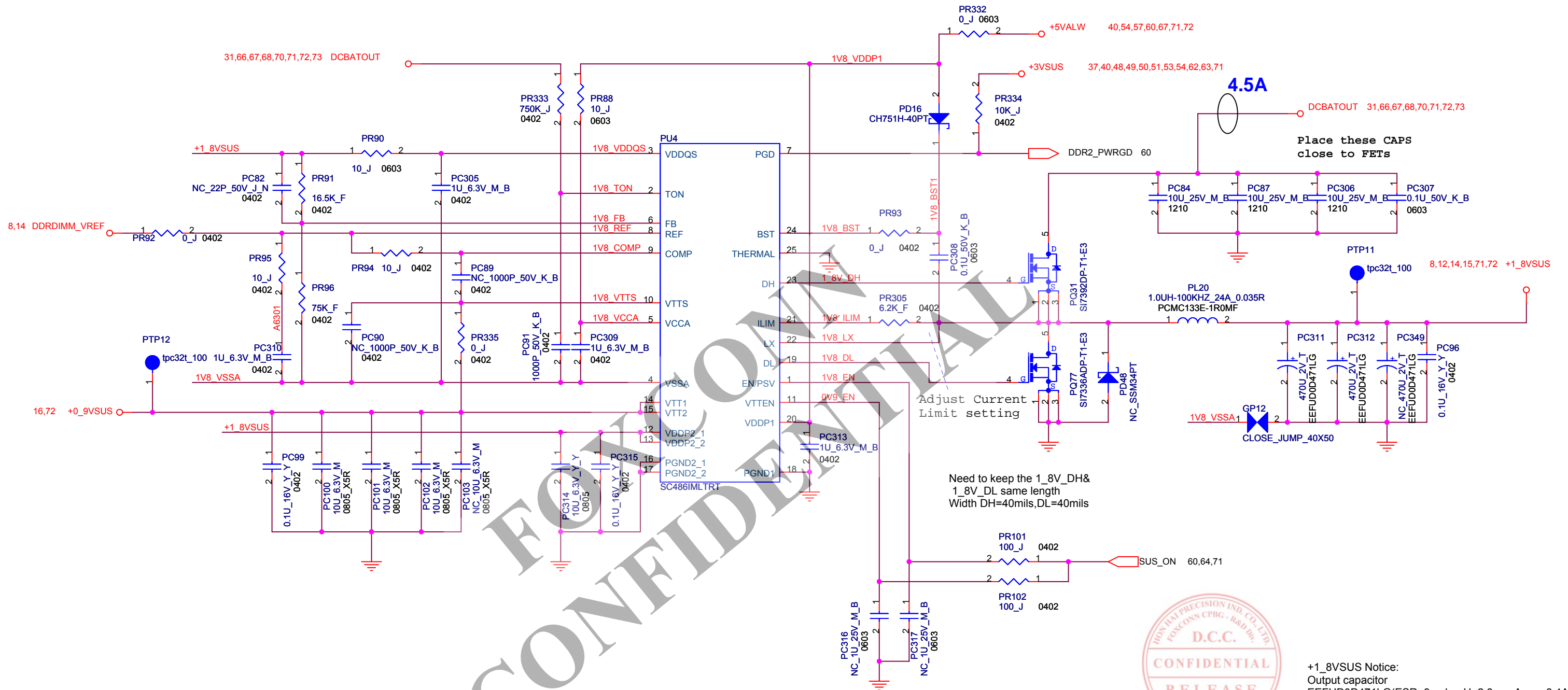
+1_05VRUN Notice:
Output capacitor usage
EEFSX0D331ER(ESR=9mohm,H=1.9mm,Arms=3.0A)
2R5TPE330M9(ESR=9mohm,H=1.8mm,Arms=3.9A)

MOSFET
Top_IRF7807Z(Total Qg=11.5nc_max)
Bottom_IRF8113(Rds=5.8mΩ_typ,6.8mΩ_max@Vgs=4.5V,Id=13.8A)
or
Top_SI4892DY(Total Qg=10nc_max)
Bottom_SI4856ADY(Rds=6.3mΩ_typ,7.6mΩ_max@Vgs=4.5V,Id=14A)



Vout=1.05V, PR1=1Kohm, PR2=20Kohm

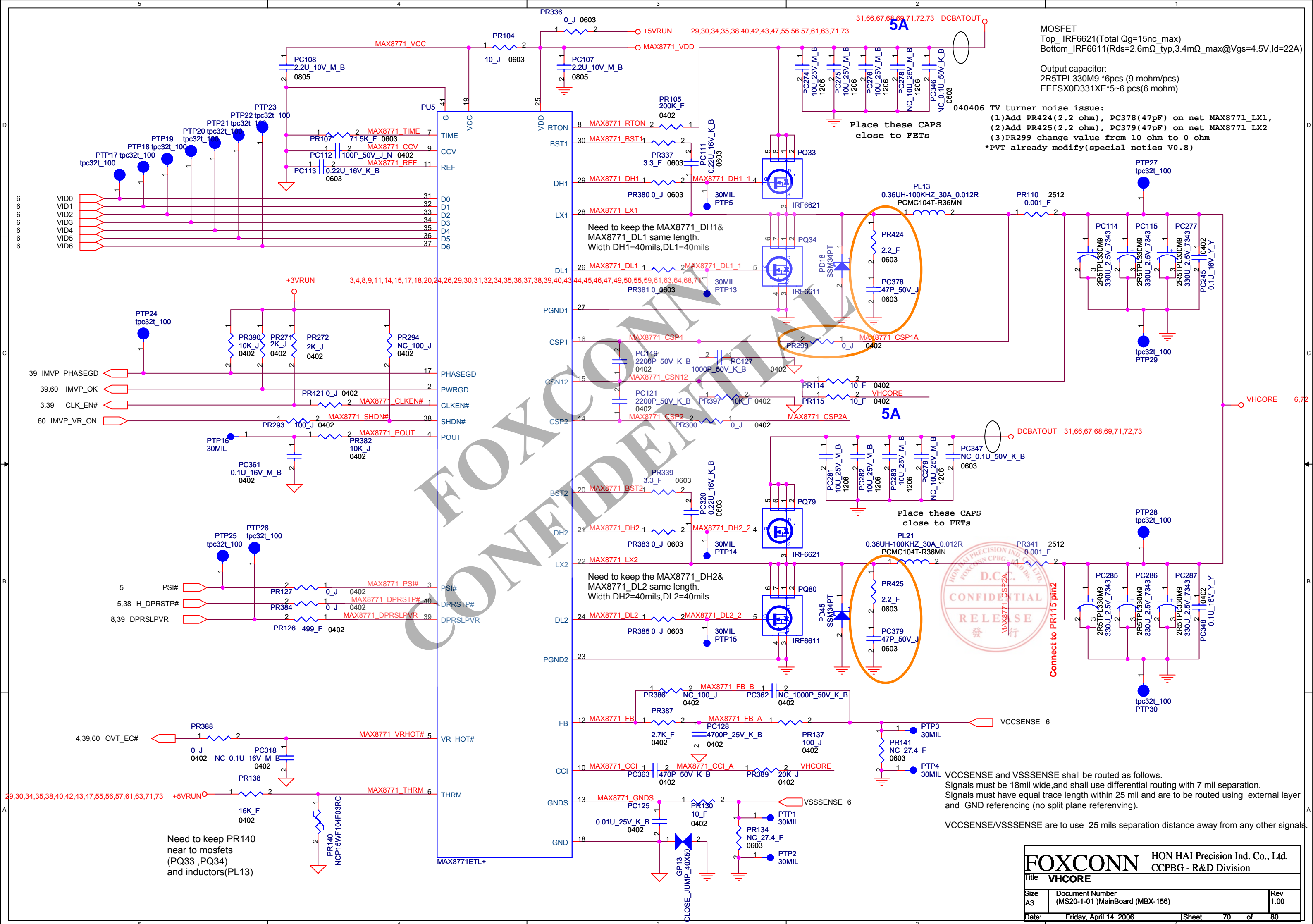
CONFIDENTIAL
D.C.C.
RELEASE



+1_8VSUS Notice:
 Output capacitor
 EEFUD0D471LG (ESR=9mohm, H=2.8mm, Arms=3.4A)
 2R5TPE470M9 (ESR=9mohm, H=1.8mm, Arms=3.9A)

MOSFET
 Top_Si7392DP (Total Qg=15nc_max)
 Bottom_Si7336ADP (Rds=3.1mΩ_typ, 4.0mΩ_max@19A)
 or
 Top_NTMFS4707N (Total Qg=15nc_max)
 Bottom_NTMFS4119N (Rds=3.1mΩ_typ, 4.8mΩ_max@25A)

1_8V LIMIT@20A(19.2~24A)



MOSFET
 Top_IRF6621(Total Qg=15nc_max)
 Bottom_IRF6611(Rds=2.6mΩ_typ,3.4mΩ_max@Vgs=4.5V,Id=22A)

Output capacitor:
 2R5TPL330M9 *6pcs (9 mohm/pcs)
 EEFSX0D331XE*5-6 pcs(6 mohm)

040406 TV turner noise issue:
 (1)Add PR424(2.2 ohm), PC378(47pF) on net MAX8771_LX1,
 (2)Add PR425(2.2 ohm), PC379(47pF) on net MAX8771_LX2
 (3)PR299 change value from 10 ohm to 0 ohm
 *PVT already modify(special notices V0.8)

Place these CAPS close to FETs

Need to keep the MAX8771_DH1& MAX8771_DL1 same length. Width DH1=40mils,DL1=40mils

Need to keep the MAX8771_DH2& MAX8771_DL2 same length. Width DH2=40mils,DL2=40mils

Need to keep PR140 near to mosfets (PQ33 ,PQ34) and inductors(PL13)

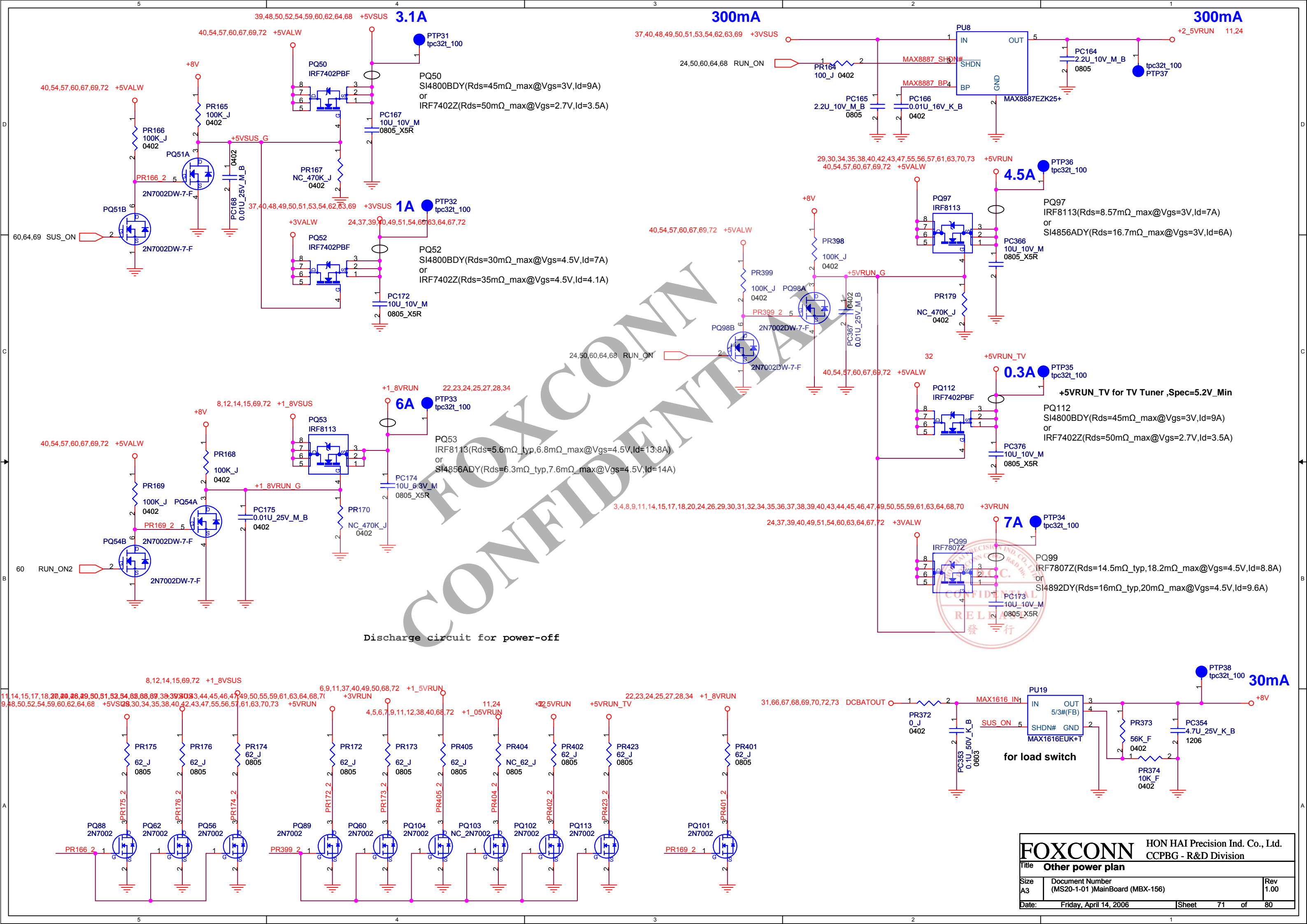


Connect to PR115 pin2

VCCSENSE and VSSSENSE shall be routed as follows.
 Signals must be 18mil wide, and shall use differential routing with 7 mil separation.
 Signals must have equal trace length within 25 mil and are to be routed using external layer and GND referencing (no split plane referencing).

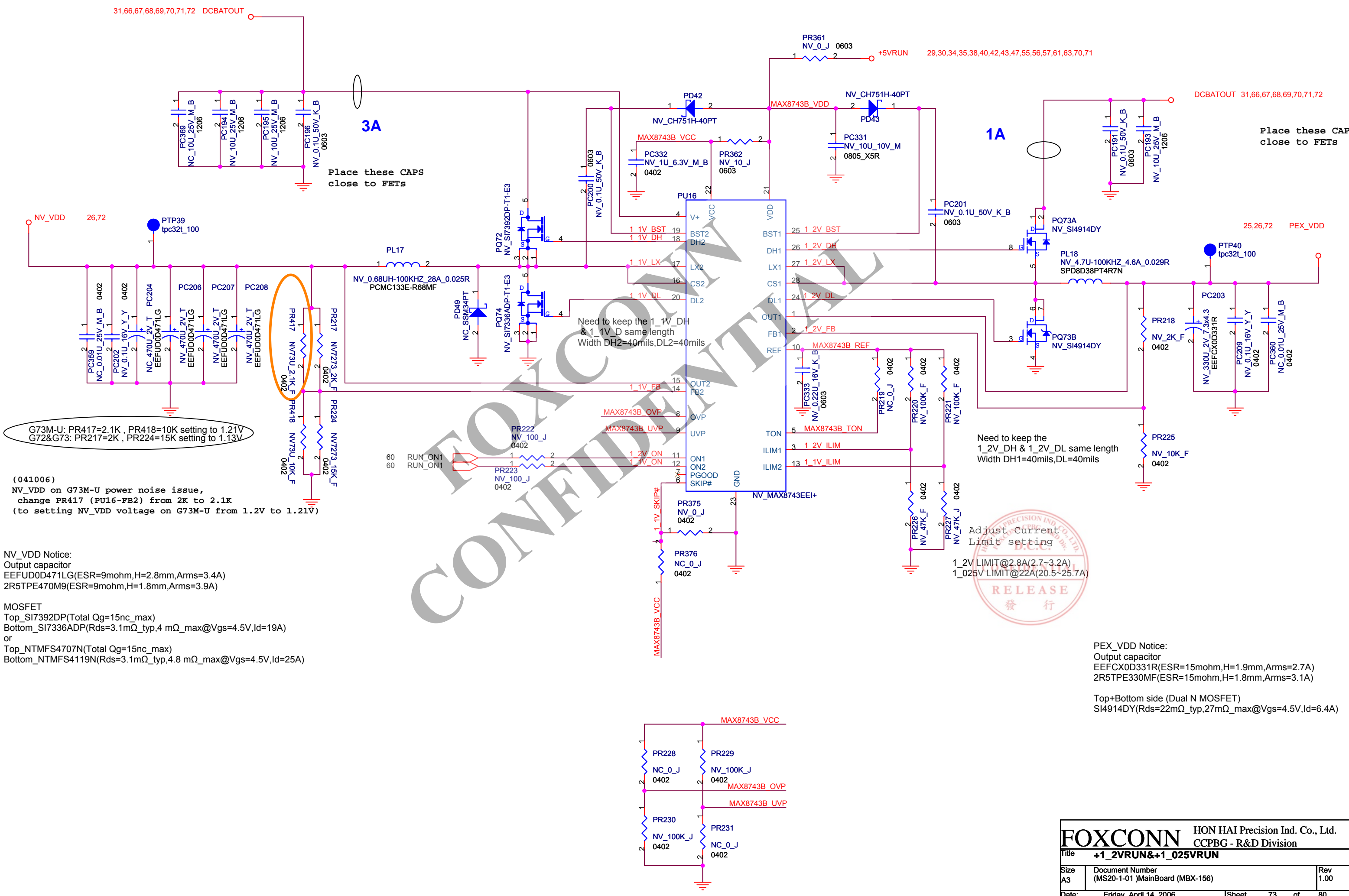
VCCSENSE/VSSSENSE are to use 25 mils separation distance away from any other signals.

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title VHCORE		CCPBG - R&D Division	
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Date: Friday, April 14, 2006	Sheet 70	of 80	



Discharge circuit for power-off

FOXCONN HON HAI Precision Ind. Co., Ltd.	
CCPBG - R&D Division	
Title Other power plan	
Size A3	Document Number (MS20-1-01) MainBoard (MBX-156)
Date: Friday, April 14, 2006	Rev 1.00
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Place these CAPS close to FETs

Place these CAPS close to FETs

Need to keep the 1_1V_DH & 1_1V_D same length
Width DH2=40mils, DL2=40mils

Need to keep the 1_2V_DH & 1_2V_DL same length
Width DH1=40mils, DL=40mils

G73M-U: PR417=2.1K, PR418=10K setting to 1.21V
G72&G73: PR217=2K, PR224=15K setting to 1.13V

(041006)
NV_VDD on G73M-U power noise issue,
change PR417 (PU16-FB2) from 2K to 2.1K
(to setting NV_VDD voltage on G73M-U from 1.2V to 1.21V)

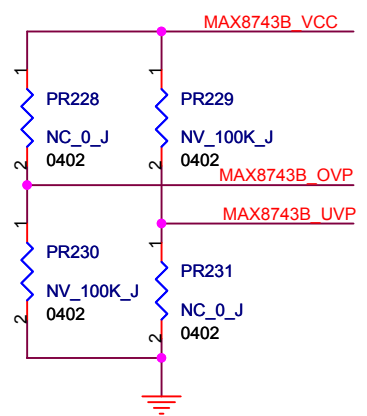
NV_VDD Notice:
Output capacitor
EEFUD0D471LG(ESR=9mohm,H=2.8mm,Arms=3.4A)
2R5TPE470M9(ESR=9mohm,H=1.8mm,Arms=3.9A)

MOSFET
Top_S17392DP(Total Qg=15nc_max)
Bottom_S17336ADP(Rds=3.1mΩ_typ,4 mΩ_max@Vgs=4.5V,Id=19A)
or
Top_NTMFS4707N(Total Qg=15nc_max)
Bottom_NTMFS4119N(Rds=3.1mΩ_typ,4.8 mΩ_max@Vgs=4.5V,Id=25A)

Adjust Current Limit setting
1_2V LIMIT@2.8A(2.7~3.2A)
1_025V LIMIT@22A(20.5~25.7A)

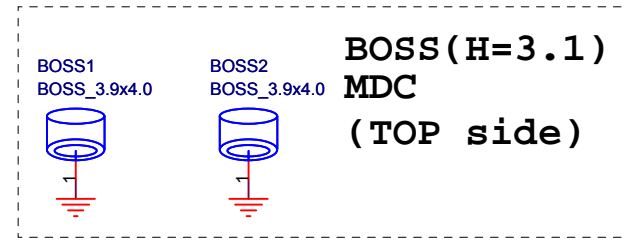
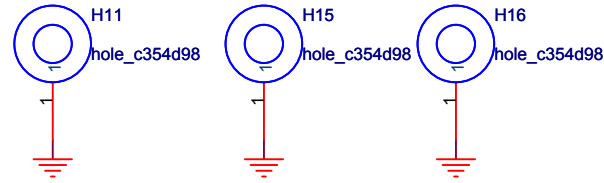
PEX_VDD Notice:
Output capacitor
EEFCX0D331R(ESR=15mohm,H=1.9mm,Arms=2.7A)
2R5TPE330MF(ESR=15mohm,H=1.8mm,Arms=3.1A)

Top+Bottom side (Dual N MOSFET)
SI4914DY(Rds=22mΩ_typ,27mΩ_max@Vgs=4.5V,Id=6.4A)



HOLE

Type 1



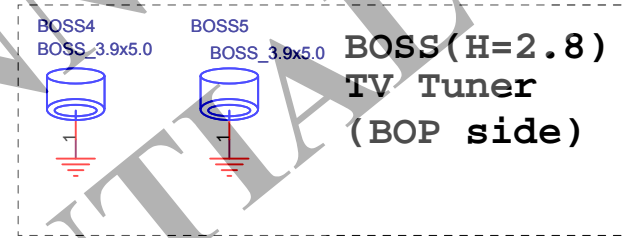
Type 2

10/24
Remove Screw Hole H2
P/N 1X-HOLE000-0108
because the Hole overlay
with CN32 and layout will
modify component screw shipe

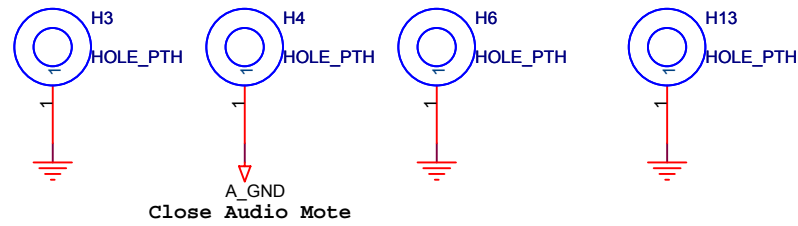


Type 3

10/24
Remove Screw Hole H1
P/N 1X-HOLE000-0110
because the Hole overlay
with CN32 and layout will
modify component screw shipe

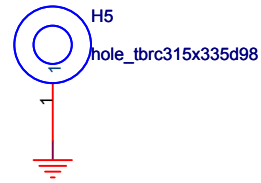


Type 4

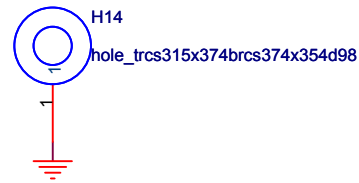


Type NPTH Guide (spherical) HOLD

Type 5



Type 6

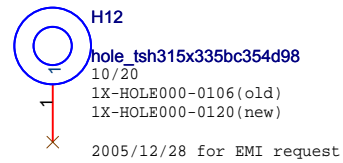


Type NPTH Guide (oval-shaped) HOLD

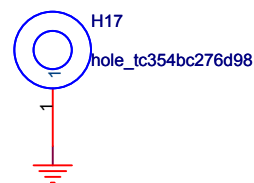
Type 7



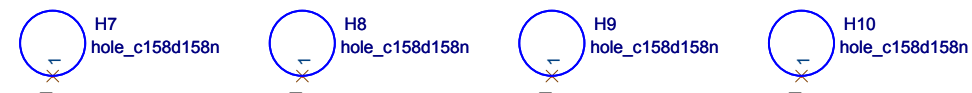
Type 8



Type 9



Type CPU



FOXCONN CONFIDENTIAL



FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title HOLE & BOSS			
Size A3	Document Number (MS20-1-01) MainBoard (MBX-156)		Rev 1.00
Date:	Friday, April 14, 2006	Sheet	74 of 80

(2005/09/19)

- 1.Update the NB and CPU circuit base on intel new design guide revision 1.5
- 2.Changed the wake event from S3 to S4 for lan .
- 3.Modified the MS current resistor from 1K to 1.5K to meet customer specification.
- 4.Express card power plane changed.
- 5.SB some power changed .
- 6.Modify HDMI circuit
- 7.Back Part value "NV"
- 8.Replease LVDS of 945GM interface

(2005/09/21)

- 1.Oide power plane change from 5VSUS to 5VRUN on page 48.
- 2.C1131 was connected to net "+1_5V_PCIE_OUT" on page 48.
- 3.Change R1672~R1675 from stuff to no sutff on page 34.
- 4.Add one series 0ohm resistor to net "1930_ACZ_SDIN2" on page 34.
- 5.Add pull-up resistor to LDDC_CLK/DATA and L_CLKCTLA/CLKCTLB according to intel design guide on page 9.
- 6.ODD/SATA HDD change power plan from SUS to RUN
- 7.CN19/CN47/CN26 updata CIS Library
- 8.CN26 MDC modem Pin 2-Pin 6 short
- 9.CN12 KB connentor change type updata CIS library

(2005/09/22)

- 1.CN48 change from P/N:1N-1080000-0000 to P/N:1N-1068000-0000
- 2.page 72 add battery in current limit protection
- 3.page 66 modified battery input circuit.
- 4.page 46 Modify 2nd FAN circuit
- 5.page 55 Modify CIR interface
- 6.page 54 Modify Audio Board interface
- 7.Delete R772/R774/R1096 and Q35 on page 48.
- 8.Backup express card and Wlan wake event signal leakage circuit and change net name "D_PCIE_WAKE#" on page 35 and 44.
- 9.Default for wake S3,backup for wake S4 circuit on page 36 and 61.
- 10.USB power change from +5valw to +5vsus on page 45.
- 11.Modify the resistors for CRT and TV disable on page 9.
- 12.Update CN29 for new symbol on page 45.
- 13.Modify EC pin out
- 14.Modify Mini PCIE power plan from SUS to RUN
- 15.Modify HDMI circuit
- 16.Change Y8 package to 5mm*7mm(H=1.2)
- 17.GPIO require from EC to SB Waiting S/W assign SB GPIO

(2005/09/23)

- 1.Change R162 from stuff to no stuff on page 13 .
- 2.Change R1354 pull-up power from +3VSUS to +3VRUN on page 44.
3. Pull " +1_5VRUN_DPLLA" and "+1_5VRUN_DPLLA" up to +1_5VRUN for high type and change CAP5/6 to CA on page 11.
- 4.Pull LVDS clock up to +1_5RUN and down to GND for high type base on design version 1.5 on page 8.
- 5.Add one inductance and one capacitor for SATSPLL power filter on page 36.
- 6.Add Function RUN_ON & AND_DOCK_S5_RST_100MS# & D_S5_PWRGD on page 44.
- 7.Detele HDCP_SCL & HDCP_SDA on page 44
- 8.Change MC_PWR_CTRL_MS# to MC_PWR_CTRL_MS; Change MC_PWR_CTRL_SD# to MC_PWR_CTRL_SD on page 56
- 9.Delete R925,R926 on page 56

(2005/09/27)

- 1.Delete R1739~1741 on page 9
- 2.Move three GPIO signals from EC to SB on page 35.
- 3.Change L4 and C142 value on page 11.
- 4.Add two 0ohm resistor for backup S4 wake event on page 61.
- 5.Modify Docking DVI chip from sii170B to sii1162
- 6.Modify FAN circuit
- 7.Change CAP to FB on Audio internal speaker connector
- 8.Page 53 USB HUB 2.0->1.1

(2005/09/30)

- 1.PR407 change 0.012 ohm into 0.01 ohm
- 2.PQ3 change FDS6675A into SI4425BDY
- 3.PF1 change 8A into 10A
- 4.PD11 change MMVZ5231BPT into MMVZ5235BPT
- 5.PCN2 change package
- 6.De1 PQ75,Change PQ72,PQ74 to POWERPAK package
- 7.Add PC374,PC375
- 8.Modify GFX/HDMI circuit,review bypass and reciver RES.
- 9.Modify Docking pin out(Alex chen)

(2005/10/03)

- 1.Modify VRAM DDR3 Address pin swape(Alex chen)

(2005/10/04)

- 1.Schematic page swape
- 2.Modify Audio circuit
- 3.Modify VGA circuit
- 4.Modify SATA/PATA circuit
- 5.Modify SB SATA interface add SATA AC Coupling cap

(2005/10/06)

- 1.Modify Power circuit
- 2.Modify Audio circuit
- 3.Modify VGA circuit
- 4.Modify Mini PCIE Circuit
- 5.Delect R27,R130,R1772,R1773 and add the circuit for reboot.
- 6.Delect SM_VREF buffer circuit ,because the DDRDIMM_VREF can meet specification on page8.

(2005/10/07)

- 1.Modify CIR circuit ,change polyswitch
- 2.Modify GFX VRAM pin swape
- 3.Modify docking circuit
- 4.Add c? beside MDC Power on page 46
- 5.Detele R963 on page 47
- 6.Detele R1093,R1095,R1097; Detele C840,C834,C832,C1134 By on page 50
- 7.Change R1307 form 649 to 620 on page 51
- 8.Update DVI_TMDS* Net Name on page64

(2005/10/11)

- 1.Detele C836; ADD two 4.7K pull-up resistors to SMBUS on page 50
- 2.Change R110 from stuff to NC according to intel WW 41 document on page 8.
- 3.Modify VGA circuit
- 4.HDMI RP122,RP123,RP124,RP125 pin1-pin4 & pin2-pin3 pin swape.
- 5.Modify Power circuit

(2005/10/13)

- 1.Detele C836; ADD two 4.7K pull-up resistors to SMBUS on page 50
- 2.Change R110 from stuff to NC according to intel WW 41 document on page 8.
- 3.Modify VGA circuit
- 4.Modify Power circuit
- 5.Modify I/O Board connentor
- 6.Updata OrCAD symbol CN1,CN2,CN14,CN18,CN25,CPU,NB,Codec
- 7.Add Screw ,Boss,Power sequency page

(2005/10/19)

- 1.Change panel ID for Allen requirement on page39 .
- 2.Add 0.1u capacitance beside Vcpl1&Vcpl2 on page 44
- 3.Change C954,C955 form 1u to 0.1u ; chang R931 form 10k to 43k on page 44
- 4.Add 2 capacitance of 0.1u beside +3VRUN on page 46
- 5.Change R1630 form 1.5k to 1k on 10/17 on page 46
- 6.change D62,D63 place on page 52
- 7.Add ten resistances on SD and MS signals according to MOR requirement.
- 8.Changed cap19/17 value from 150uF to 47uF according to MOR requirement on page52.
- 9.Add one 10uF capacitor and pull up SD_WP on page46.
- 10.Aadded R? 1R-000010X-F300 (1ohm 1%, 0603, 1/10W) according to latest checklist on page 40.
- 11.MIDIFY POWER CIRCUIT
- 12.MODIFY VGA circuit
- 13.MODIFY EC circuit
- 14.MODIFY SATA/ODD circuit

(2005/10/20)

- 1.Page43 PATA CD-ROM: CN32 Pin3(Audio_GND) connect to GND.
- 2.Page49 Mini-PCIE Card:only support S3 Wake On WLAN, so change Mini_PCIE_+3VAUX Default to +3VSUS (R1067 NC=>ON)(R1817 ON=>NC)

(2005/10/20)

- 1.Change the value of R91 to 1K and let PR126 no stuff.
- 2.Update connector pin connection according to Steve's comment.
- 3.Modify EC/Daughter Board connentor Circuit

(2005/10/24)

- 1.U126 pin27 Add 33pF and 12pF capacitor for RF frequency countermeasure.The small capacitance capacitor is put on close to 27 pin.
- 2.Delete L112.
- 3.A_GND GNDD connection through L(NC) at one point. Make this circuit on M/B. (This circuit is moved from Audio daughter board.)
- 4.U41 pin1 Change to following circuit.
- 5.U68 pin 1/pin 27 Add 1 kohm buffer resistance on IN_L. Add 1 kohm buffer resistance on IN_R.
- 6.Q112 It is necessary to check there is no chance not to be ON because of an internal resistance of Digital Tr(Q112) in the case of emitter follower.
- 7.U68 CP_GND do not have any connection to GND in schematics. There is no problem to connect A_GND.
- 8.Change the connection GNDD to A_GND.(C1291)
- 9.U50 Add the following RC filter(R:0 ohm,C:4.7uF) circuit between U50 4pin and MUTE_5
- 10.Modify VGA circuit

(2005/10/26)

- 1.Modify Power circuit
- 2.Delete TP682,TP684,TP619,TP621
- 3.Audio add E-CAP

(2005/10/27)

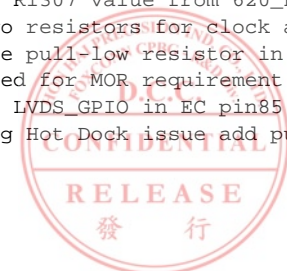
- 1.change PCI7412 to PCI8412
- 2.Connentor Pin swap CN21,for FFC pin1 to pin1,
- 3.Common chock pin swap L68, L120 for layout request
- 4.Modify Power circuit
- 5.Modify GFX circuit

(2005/11/01)

- 1.Modify GFX circuit (include ESD diode)
- 2.Modify Power circuit
- 3.Delete TP41,TP557
- 4.SATA CN63 Pin15.16.17.18.19.20 +3VRUN_SATA*->NC
- 5.SATA Delete Componment F9 & F10 & C791 & C792 & C1295 & C1296
- 6.Add SD LED
- 7.SPDIIF Add R1835 (MOR request) for matching the impedance

(2005/11/01)

- 1.Change C141 value from 0.1uF to 10uF on page 11.
- 2.Change R1307 value from 620_F to 649_F on page 51.
- 3.Add two resistors for clock amplitude tune on page 3.
- 4.Add one pull-low resistor in D_RUN_PWRGD on page64.
- 5.Modified for MOR requirement on page37 and page 39.
- 6.Delete LVDS_GPIO in EC pin85 and then make EC pin85 as Test Point.
- 7.Ducking Hot_Dock issue add pull down 10K(R1889) on D_RUN_PWRGD



(2005/11/27)

- 1.MUTE_SW#(R1108) change from pull +ECVCC to pull +3VALW
- 2.CN42(FAN1)Pin swap
- 3.MOR COOLING UNIT,Add for 0V,1V,1.9V,5V control,solving 5V ringback
- 4.SD/MS LED(LED11) revise for too dark issue
- 5.BLUETOOTH LED(LED9) revise for too dark issue
- 6.SONY LOGO LED(U126)change from +3VRUN to +5VRUN,& change from AHC(CMOS) to AHCT(TTL)

(2005/12/08)

- 1.(U18)Change the connection for clock amplitude issue.(Add C1606,C1607,swape R1884,R1885 with L1,L2)
- 2.(U11)Update VDDR3 CLK terminal for G73(Add C1608,R1896,R1897) =>Omit by 12/21 item#9
- 3.(U12)Update VDDR3 CLK terminal for G73(Add C1609,R1898,R1899)
- 4.(VDDR3) RFMI(R1464),FBA_VBA2(R1463) change to NC
- 5.(EC)BATT_PRS# add circuit controlled by +3VALW(Add Q147,R1905)
- 6.(EC)PWRSW# (R700)pull up from +ECVCC to +3VALW
- 7.(EC)(Pull Down for EC strap issue)(Add RUN_ON2 R1903,IMVP_OK R1904)
- 8.(EC)Swap MUTE_SW# with IMVP_OK (pin8<->pin11)for EC strap(TEST_TP) issue
- 9.(EC)MUTE_SW# pull up(R1108) change from +ECVCC to +3VALW
- 10.(EC)Swap OVT_EC# with RUN_ON2(R713<->R714)for EC strap(DPLL_TP) issue
- 11.(EC)Change BIOS(U32->U34->CN14) net name SIO_FA[0..19] & SIO_FD[0..7]to XIO_FA[0..19] & XIO_FD[0..7]
- 12.(EC)XIO_FA4(R703) & XIO_FA5(R704)pull res change from 470K to 47K based on MS10 PVT revise
- 13.(EC) pin39 change from DOCK_RUN_RST to DOCK_RUN_RST#
- 14.(EC)PU CIR_ALPS_SW1 for EC strap(ISP_TP)(Add R1906)
- 15.(EC)pin156 ACIN Control by +3VALW(addQ148,R1907)
- 16.(GFX)FBCAL_PD_VDDQ add pull res (add R1900)
- 17.(GFX)reverse INV_EN_EC to conctect NONETNA2(add NC R1901)
- 18.(Audio)MUTE_5 add 10K RES to Q112(add R1902)
- 19.(GFX)PLT_RST# to GFX add a AND circuit(Add R1908,R1909,R1910,U127)
- 20.(HDMI)Del BUFIRST# to microcontroller reverse gate(Del U124)
- 21.(Audio)modify capacitor value C1118 to 4.7u
- 22.(Thermal sanner)change part U8 (15-F75383M-0000->15-F75383M-1000)
- 23.(S-VIDEO ANALOG SWITCH)U77 change part U77 SN74CBT3257PW(NEW) <-> TS5A23157DGS(OLD)
- 24.(S-VIDEO ANALOG SWITCH)change through U77:PR_DDCCLK,PR_DDCDATA,MB_DDCCLK,MB_DDCDATA,GM_OR_NV_DDCCLK,GM_OR_NV_DDCDATA.
- 25.(SEMI-PNP)Modify SEMI-PNP circuit
- 26.(CRT)Modify CRT circuit:
- 27.(HDMI)U123 pin44 pull up res R1690 NC_10K_J <- NV72_10K_J
- 28.(HDMI)Modify Y8 circuit.
- 29.(PCMCIA)U62 pin12 connent to PLT_RST#
- 28.(Audio)Change part Q77,Q78,Q89,Q90,Q91,Q92,Q143,Q144(17-2SC5376-0000->17-PBSS251-5F00)
- 29.(SD)power control circuit R1630 (1K->330R)
- 30.(HDMI)U116 change part (SST89V54RD2-33-C-TQ <- NV_SST89V52RD2-33-C)
- 31.(Audio)Q112 change part (MMBT3906 <- 2SC5376)

(2005/12/15)

- 1.(POWER)Page 66---Change PR44 from 13K_J to 33K_J, Change PQ3 from SI4425BDY-T1-E3 to FDS6675A, Change PD1 from SSM34APT to SSM34PT.
- 2.(POWER)Page 67---Change PC350 from NC to 10U_25V_M_B, Change PR67 from NC to 0_J, Change PR63 from NC to 100K_J, change PR64 from 120K_F to 160K_F, change PR65 from 147K_F to 120K_F,Change from PJ29 to PR57 0_J, Delete PJ2&PJ4 and short, Delete PJ1&PJ3 and short, Delete PR414, Add PR422 1K_J.
- 3.(POWER)Page 68---Change PR79 from 56K_F to 47K_F, Delete PJ5&PJ6 and short, Delete PJ7&PJ8 and short.
- 4.(POWER)Page 69---Change PR305 from 8.2K_F to 6.2K_F, Delete PJ11 and short, Delete PJ9,PJ11&PJ37 and short.
- 5.(POWER)Page 70---Delete "Reserve for improve CLK_EN# wrong timing" circuit, Change PC276 & PC283 from NC to 10U_25V_M_B, Change PD18 & PD45 from SKS30-04AT-G to SSM34PT.Del PQ111,PR422
- 6.(POWER)Page 71---Change PQ104 from NC to 2N7002,Change PR404 from 62_J to NC, Change PQ50&PQ97 from IRF7807Z to IRF7402PBF, Delete PJ41 and short, Delete PJ28 and short,Delete PJ40 and short.
- 7.(POWER)Page 72---Change Power Limit circuit.(Add PR366,Del PQ109,PC188,PC189,PR207,PR208,PR212,PR213,PU14, change part:PQ110 NPN->N-MOS
- 8.(POWER)Page 73---Change PR227 from 56K_F to 47K_F, Change PR417 from 560_F to 2K_F, Change PR418 from 22K_F to 10K_F, Delete PJ32,PJ33&PJ35 and short, Delete PJ34 and short.
- 9.(CKG) Del C1606,C1607,R1884 and R1885 on page 3.
- 10.(CPU) Add 0.1uF capacitor(C1610) for GTLREF on page 5.
- 11.(Docking)Change Net From DK_BAY_PWEN to DK_BAY_PWREN
- 12.(Docking)Change Net From DK_BAY_ID# to DK_BAY_ID0#
- 13.(Docking)Change Net From AND_DOCK_S5_RST_100MS# to AND_DOCK_S5_RST_500MS#
- 14.(Docking)Change Net From DK_BAY_ID# to DK_BAY_ID0#
- 15.(GFX)Modify BOM configuration for G73M-U(BLOCK DIAGRAM).
- 16.(GFX)Modify PCI_DEVID[3:0]="1001"->9 for G73M-U.
- 17.(GFX)Add pull down 10K ohm resistor to DOCK_SEMI_PNP.(R1911)
- 18.(GFX)Update the panel ID Spec.
- 19.(GFX)Change the reset signal to PCI_RST for U116 and U117(Nvidia suggestion).
- 20.(EC)Add DIP SW17(HDS401-E) for Instant ON selection.Delete R717,R716 change from CA_100K_J to 100K_J
- 21.(EC)Change CIR_ALPS_SW0 to SW_CIR00 for the same as IR module net name
- 22.(EC)Change CIR_ALPS_SW1 to SW_CIR01 for the same as IR module net name
- 23.(EC)Change CIR_ALPS_SW2 to SW_CIR02 for the same as IR module net name
- 24.(EC) Change CIR_ALPS_WAKE# to PWR_CIR# for the same as IR module net name
- 25.(EC)Change LIDIN# power source from +3VALW to +ECVCC due to SW/Kenny request
- 26.(EC)PWRSW# Pull High change from +3VALW to +ECVCC
- 27.(EC)Add KSO15 and redefine CN45 Pin4 ~ Pin6 for SW/Kenny Request
- 28.(CIR)Change EC to CIR connentor CN61 net name
- 29.(CIR)Add PWR_CIR# pull up RES R1913
- 30.(GFX)U8 modify
- 31.(EC)System ID pull up power source change from +ECVCC->+3VALW
- 32.(Audio)CVREF bypass CAP change from C863(10U)->(1U)
- 33.(Mini PCIE)WIRELESS Add R1912 pull up RES.
- 34.(EC) Add +ECVCC discharge RES (R1914)
- 35.(Touch Pad)LIDIN# pull up from +3VALW ->+ECVCC
- 36.(EC)Q147,Q148 change part from P-MOS->NPN
- 37.(SB) LVDSGPIO R1887 change to NC

(2005/12/21)

- 1.(EC)12/20,40 Revise SW17 from HDS401-E to HDS402-E_SW-SMD4 cause the vendor has stopped producing HDS401-E.
- 2.(EC)12/21,43 Revise C802/C803 from 10pf to 15pf due to Steve's SI test report.
- 3.(POWER)Page 67---Del PR422
- 4.(POWER)Page 69---Change PD19 to PD48
- 5.(POWER)Page 72---Change PU22A to PU15A, Change PU22B to PU15B
- 6.(POWER)Other----Add 32ml test point for BFT test
- 7.(MDC)MDC connentor change to P/N: IN-0012000-F0X0 ,BOSS1/BOSS2 P/N:1M-1A40M20-3100) the same with MS10
- 8.(CARD BUS)CARD BUS control change PCI7412 to 8412
- 9.(SB)RP95 pin swape for Layout request

(2005/12/30)

- 1.(GFX)Modify Si1162 power net SILL162_PVCC.
- 2.(GFX)Add FBA_CLK0_RC and FBA_CLK1_RC net name.
- 3.(GFX)Modify R378,R380,R1871,R1872 from 40ohm to 60ohm for Nvidia suggestion.
- 4.(GFX)Remove Si1162 and other parts to cancel G72M DVI Function.
- 5.(GFX)Add two Inverter gate to prevent the glitch from Silicon 1930.
- 6.(GFX)Update the reset signal of HDMI UCODEC,HDMI Microcontroller and HDMI Silicon 1930.
- 7.(GFX)Remove C432,R270,R274 on G73M SKU.
- 8.(GFX)Add TP682, TP678 test point because MIOBD7 and MIOBD10 unused.
- 9.(GFX)Modify HW strap for Infineon VRAM and update the BOM configuration in block diagram page.
- 10.(GFX)Change ESD diode D78,D79,D80 to meet the HDMI Spec.
- 11.(GFX)Delete the page 33(DVO-TMDS Si1162) for layout space.
- 12.(GFX)Add 1 switch to divide DVI DDC from HDMI DDC.
- 13.(GFX)12/27 Remove R195,R196,R1729,R1730 and C284 for G72M DVI funtion missing.
- 14.(GFX)Change R1592 from 360 ohm to 390 ohm for SiIcon Image suggestion.
- 15.(GFX)Modify the INV_EN_EC to control INV_BRADJ for the Nvidia glitch issue on MS10.
- 16.(POWER)Page 71---Change PQ52,PQ112 from IRF7807Z to IRF7402PBF,Change PQ97 from IRF7402PBF to IRF7807Z.
- 17.(POWER)Page 72---Change PD52,PR420,PC374,PQ110 to NC.
- 18.(POWER)Page 67---Change PR49 from 160K to 187K, Change PR52 from 100K to 120K.
- 19.(ICH7)12/23 Change U30 and R1183 to NC and change R1184 to stuff on page 39.
- 20.(ICH7)12/23 Add two 2N7002 for leakage on page 38
- 21.(camera)Add 10uF capacitor for camera power,and add modify OCP circuit (add u133,del Q79,Q80)on page 50.
- 22.(CKG)12/23 change dumping resistor from 33 ohm to 100ohm and add FB between dumping resistor and clock generator for MOR requirement on page 3.
- 23.(CKG)12/28 Del 27MHZ circuit for Nvidia on page 3.
- 24.(USB)12/28 Change USB connectors to white type on page 52.
- 25.(EC)12/22,45 : Revise net name from FAN1_PWM to 2ND_FAN_PWM for error correction.
- 26.(EC)12/22,46 : Remove R1915 for moving pull high R from connector(CN68) side to EC side
- 27.(EC)12/22,47 : Add pull +ECVCC high R for moving from connector(CN68) side to EC side
- 28.(EC)12/23,48 : Revise H_RCIN# to EC_RCIN# and H_A20GATE to EC_A20GATE for matching leakage-proof circuit in P32
- 29.(EC)12/23,49 : Revise 2ND_FAN component to NC due to Ted request 12/22. (R1920-R1923,R1767,C1615,C1616,C1618,Q150,D87,CN65)
- 30.(EC)12/23,50 : Revise net name from FAN2_DAC to MOR_FAN_DAC due to Ted request 12/22.
- 31.(EC)12/23,51 : Revise net name from FAN2_DAC_OP to MOR_FAN_DAC_OP due to Ted request 12/22.
- 32.(EC)12/23,52 : Add 0 ohm(NC) for improving clock skew of PCLK_JIG.
- 32.(EC)12/23,53 : Revise R693,R1904,1903 from 10K to 100K for improving driving ability
- 33.(EC)12/23,54 : Add 1k ohm for avoiding EC directly short to GND.
- 34.(EC)12/26,55 : Change CN62 from HS8202E to HS8102E due to Mechanical 12/23 outline file
- 35.(EC)12/26,56 : Due to leakage of original circuit we revise 12/23 BATT_PRS# controlled by ALW power well circuit.
- 36.(EC)12/26,57 : Due to leakage of original circuit we revise 12/23 ACIN controlled by ALW power well circuit.
- 37.(EC)12/27,58 : D_S5_PWRGD add pull down 100k ohm due to Hibino San request(12/26 mail).
- 38.(EC)12/28,59 : Delete R1540 due to too dark issue
- 39.(EC)12/28,60 : Add PWRSW# test point due to BFT request.
- 40.(EC)12/28,61 : Change LED11 from HT-110UYG to HT-110UY due to error color correction.
- 41.(EC)12/28,64 : Change BT LED power source from +3VRUN to +5VRUN and R1839 from 68 ohm to 82 ohm due to too dark issue.
- 42.(EC)12/28,65 : Add ESD protector of SD LED due to Jacky Su/EMI request on 12/28.
- 43.(EC)12/28,66 : Add ESD protector of BlueTooth LED and WLAN LED due to Jacky Su/EMI request on 12/28.
- 45.(Ducking) Page64 CN30 pin 75,pin76 change net name NV_I2CB_SDA->DVI_I2CB_SDA NV_I2CB_SCL->DVI_I2CB_SCL
- 46.(GFX)Modify the INV_EN_EC to control INV_BRADJ for the Nvidia glitch issue on MS10.
- 47.(GFX)EMI suggestion:mount Cap.C1592,C1595,C1598,C1601.
- 48.(GFX)EMI suggestion:add cap.0.1uF on LCDVCC near CN3.Mount C1558 near CN49.
- 49.(GFX)EMI suggestion:add EMI bead on HDMI +5VSUS before C1452,and near CN60.reserve cap.0.1uF on +5VRUN near F1.
- 50.(GFX)EMI suggestion:add ESD Diode for AV_IN_GND.
- 51.(W-LAN)Page 49.Change R1912 from 1M to 100k ohm(Nishio San Request)
- 52.(W-LAN)Add FET on MINI_CARD_LED# between CN18 pin 44(P.49) and Q140 2pin(P.63) and control FET by using WLAN_EN that Wireless Off Control signal from EC .(Nishio San Request worry about only SW Driver control.)
- 53.(W-LAN)Prepare big Capacitor pad 22uF(1206) pad for MINI_PCIE +3_3V and MINI_PCIE +1_5V for each. Because .1in is bigger than .11abg from point of view of power consumption.
- 54.(SD)change SD socket to 67913-0009(easy repaiy issue)
- 55.(LAN).XTAL Y6 Load CapC1034,C1035 change 22pF->27pF

(2005/12/31)

- 1.(POWER)Page 67---Change PR49 from 187K to 160K, Change PR52 from 120K to 102K.
- 2.(POWER)Page 72---Change PC368 from NC to 2.2U_10V_M_B
- 3.(EC)12/30,67 : Change R1920 from NC_1K to 1K due to error correction.
- 4.(EC)12/30,68 : Change TP785 net name from FAN2_DAC_OP to MOR_FAN_DAC_OP due to error correction.
- 5.(EC)12/30,69 : Swap CN68 for change T/P FFC from bending to no bending.
- 6.(EC)12/31,70 : Add constant current circuit MAX1916 due to MOR request.
- 7.(GFX)EMI suggestion:Add 33pF Cap to SVIN_Y_1 and SVIN_C_1.
- 8.(GFX)EMI suggestion:Change C1516,C1517,C1518,C1566,C1567,C1568 from 0.1uF to 220pF.
- 9.(GFX)EMI suggestion:add ESD Diode for SVIN_Y_GND and SVIN_C_GND.
- 10.(GFX).Add 1uF capacitor(NC) to VRAM_VREF for VRAM Max Load Drop.
- 11.(GFX).Add two resistor to LVDS CONN pin6 for Gamma control.
- 12.(Audio) Modify CN64 pin definf
- 13.(Audio)Change audio amp from MAXIN to TI
- 14.(USB)Delete EXT USB connentor (MB CN29),and move USB signal to CN64.

(2006/01/03)

- 1.(GFX)page 17.Add MIOB_CLKIN (R1939)10K ohm to GND
- 2.(GFX)page 35.Add NV_HDMI_DET_5 (R1940)100K ohm to GND
- 3.(EC)page 63.Add PWRSW# (TP846) Test Pad on BOT side
- 4.(ESD)page 63.Change Part D94,D95 from PACDN042Y3R to SM05.TCT
- 5.(ICH7) page 37 INT_PIRQE#_R conctect to GND(R1887) NC->OR
- 6.(GFX) page 25 (+1_8VRUN) CAP20 change 47uF to 150 uF

(2006/01/04)

- 1.(Oide)page 50.CN21.pin swape for ME request

(2006/01/20)

- 1.(Power)page 70.PR138 change from 13K to 16K due to 青建德 revise on 1/20.

(2006/01/21)

- 1.(ICH)page 37.Change R1886 from NC to 0 ohm due to control Gamma function.
- 2.(OIDE)page 50.Change F10 from 1206L150 to 1206L035 due to short current protect.

(2006/1/12)DVT-2

- 1.(GFX) For some HDMI device no support detect pin function issue, (1)Page 20 NV_GPIO6 del TP610,add off page port. (2)Page 35 Add backup circuit,NV_GPIO6(level shift) to switch(U136 pin1)Add part:Q156,Q155,R1942,(NC)R1941
- 2.(GFX)Page 35 HDMI 12c double pull up issue change R1611,R1612 NV->NC, because page 20,R1385,R1386 still pull up.
- 3.(Audio Conn)Page 59.For Audio Board USB2.0 HUB request, (1)CN64 pin 16 change GND to +3VSUS. (2)add FUSE(F9),and bypass CAP(C1641)
- 4.(CIR) Page 54 For BFM request,add CIR test pad (TP847-TP856)
- 5.(GFX) Page 34 Modify ESD diode (U128)depend on HDMI spec(<C50 pF) change part uClamp0504A->RClamp0514M (Modify Layout & BOM)
- 6.(SATA) Page 42 Modify SATA connentor pin define,pin swape and add power pin to meet 7200RPM HDD current(MAX 5.2A/2 HDD)
- 7.(SATA) Page 38 SATA signal Eye test Fail issue,change C724-C727,C1549-C1512 from P/N:1C-2B20392-K000(0402)->P/N:1C-2B30392-K001(0603) the same with MS10

(2006/1/16)DVT-2

- 1.(FAN-2) Page 62 Modify second FAN2 short with FAN1 issue
- 2.(FAN-2) Page 62 FAN2 component cost down Q152,Q153,R1924,R1925 change to NC
- 3.(SD LED) Page 63 LED11 change part HARVATEK_HT_110UY ->HARVATEK_HT_110Y

(2006/1/18)DVT-2

- 1.(ICH7)Page37 For support LVDS_GPIO function,ICH7 INT_PIRQE#_R pull up RES.R1886 change OR->NC
- 2.(FAN-1) Page62 Modify fan speed feedback function,stuff C1521
- 3.(W-LAN) Page49 For BFT test request,add wake on W-LAN test item,add Test Pad TP858
- 4.(Audio) Page55 for Audio jack ESD issue,change Q117,Q118,Q119 form 17-2N70020-0000 ->17-2N7002K-0000
- 5.(Oide) Page50 For I/O current protect request,Add F10, (This part only for placement,Wait to change part of I hold=0.35A,I trip=0.7A)



(2006/2/27)

1. Add doide for fan inverse current on page 62
2. Add capacitor 1uF for cooling unit on page 62.
3. Add capacitor 1000pF for fan noise on page 62 and should place colse to EC pin.
4. Chagne Oide power from +5VRUN to +5VSUS on page 50.
5. Audio coupling capacitor co-layout on page 56.
6. Backup 10uF capacitors for 22uF shortage on page 6.
7. Add discharge resistor for camera on page 50.
8. Change power plan for leakage issue of USB hub and change the fulse specification on page 54 , CN61 pin10 trace shold place same as pin1.
9. Add 6 fulse for FFC short issue on page 63.
- 10.Chagne CAP5 to "CA"
- 11.Add 2.2uf and 0.luF capacitor for SMK power and add optional select for Alps pull-high power.

(2006/3/3)

- 1.(VIDEO)Modify the HW strap of VRAM for PVT
- 2.(VIDEO)Modify R1463,R1464,R1475,R1480,R1482,R1493 for 16Mx32 and 8Mx32 VRAM configuration
- 3.(VIDEO)U136 change switch control from NV_HDMI_DET_5 to NV_GPIO6
- 4.(VIDEO)Add two 0 ohm resistors to avoid the switch for NV_I2CB because G72M only support HDMI
- 5.Change codec CIS symbol to four plus.
6. Add open jump on RTCRST# net on page 38.
7. Delet fan2 circuit and change the pull-high resistor of fan_tach from 10K to 4.7K.
8. Back up logo led circuit for GMT solution on page 63.
9. MS_R and SD_R net name changed each other on page46.
- 10.Change connector S/N from 1N-0010000-MOX0 to 1N-0010000-MWG0 for S/N wrong on page32.
- 11.Change CN68 S/N from 1N-0010000-MOX0 to 1N-0010000-MWG0 for S/N wrong on page63.
- 12.Change the resistor (R1839) of bluetooth to 200ohm for too light issue on page 63.
- 13.Change the resistor (R1879) of SD card to 33 ohm for too dark issue on page 63.

(2006/3/9)

1. Change C1521 from Y5V to X7R on page 62
2. R585 change from 20K_J to 22K_F
3. Boss4 and Boss5 change to "NV73_" on page 74.
4. Add one test point on signal "2ND_FAN_TACH" on page 60.
5. Add 4 test points on CN21 connector for TE test on page50.
6. Change net name from "EN_EXT_DEV_SENSE#" to "EN_EXT_DEV_SENSE" on page 30,60 and 64.
7. Delet R1906 on page 60 for CIR double pull-high issue.
8. Change R1913 from 10K to 100K on page 54.
9. Change CN19 parts for SMT issue on page50.
- 10.Change CN64 PIN16 from +3VSUS to GND and change PIN6 from USB_PP2 to USB_VCC2, Shift Pin 6&8 to Pin 8&10, Delet P9 and C1641 on page59.
- 11.Backup fusle for HDD voltage drop issue on page42.
- 12.Update U117 CIS symbol on page 34.
- 13.Update CN60 CIS symbol for SMT issue on page34
- 14.Add two 0ohm resistors for Viao loge soft start issue on page 63 and page60.
- 15.(Power)Page 69-----Change PR91 from 15.8K_F to 16.5K_F.
- 16.(Power)Page 70-----Change PR299/PR114/PR115 to 10 ohm, Change PR300 to 0 ohm, Change PC127 from NC to 1000P_50V_K_B, Change PC126 to PR397 10K ohm. Change PR387 to 2.7K ohm.
- 17.(Power)Page72----Change PC326&PC327 from 0.1U_16V_Y_Y to 0.1U_16V_M (X5R)
- 18.(Power)Page71----Change PQ97 from IRF7807Z to IRF8113.
- 19.(Video)Page 20,R1820change to NC,because The MS20 CEC line capacitance = 777pF is much bigger than 100PF spec. After remove this resistor, CEC cap reduced to 39PF. Pass.(This GPIO11 is no function on our system, Silicon Image suggest remove it.)
- 20.(Video)Page 74-BOSS4,BOSS5 change part name from NV73_->TV_
- 21.(Video)Page 32 change part name from NV73_->TV_
- 22.(Video)Page 32 CN67,change PCB Footprint to co-layout "molex" & "Foxconn"part
- 23.page 63 CN68 change PCB Footprint to co-layout "molex" & "Foxconn"part
- 24.page 15 add C1661 (0.luF) close CN2 pin1 (DDR2_VREF) for voltage level noise debug.

(2006/3/11)

1. Page 62 C1658 change to NC
2. Page 56 CAP24,CAP25 change to NC
3. Page 70 PR397 change part 10K(5%) to 10K(1%)
- 4.(VIDEO)Page 35 R1940 change part name NV_100K_J to NV73_100K_J
- 5.(VIDEO) page 27,Page 28 PVT EMI recommend(NC_ ->NV_):C1590,C1591,C1593,C1594,C1596,C1597,C1599,C1600

(2006/3/13)

"Not neet to modiy BOM and Layout "

- 1.change title block ver "1.0" to "0.40"
- 2.page 34.HDMI circuit, change net name(1)HDMI_+5VSUS->HDMI_+5VRUN (2)HDMI_+5VSUS1->HDMI_+5VRUN1

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Title History(PVT)		
Size A3	Document Number (MS20-1-01)MainBoard (MBX-156)	Rev 1.00
Date: Friday, April 14, 2006	Sheet 77	of 80

(2006/4/5)

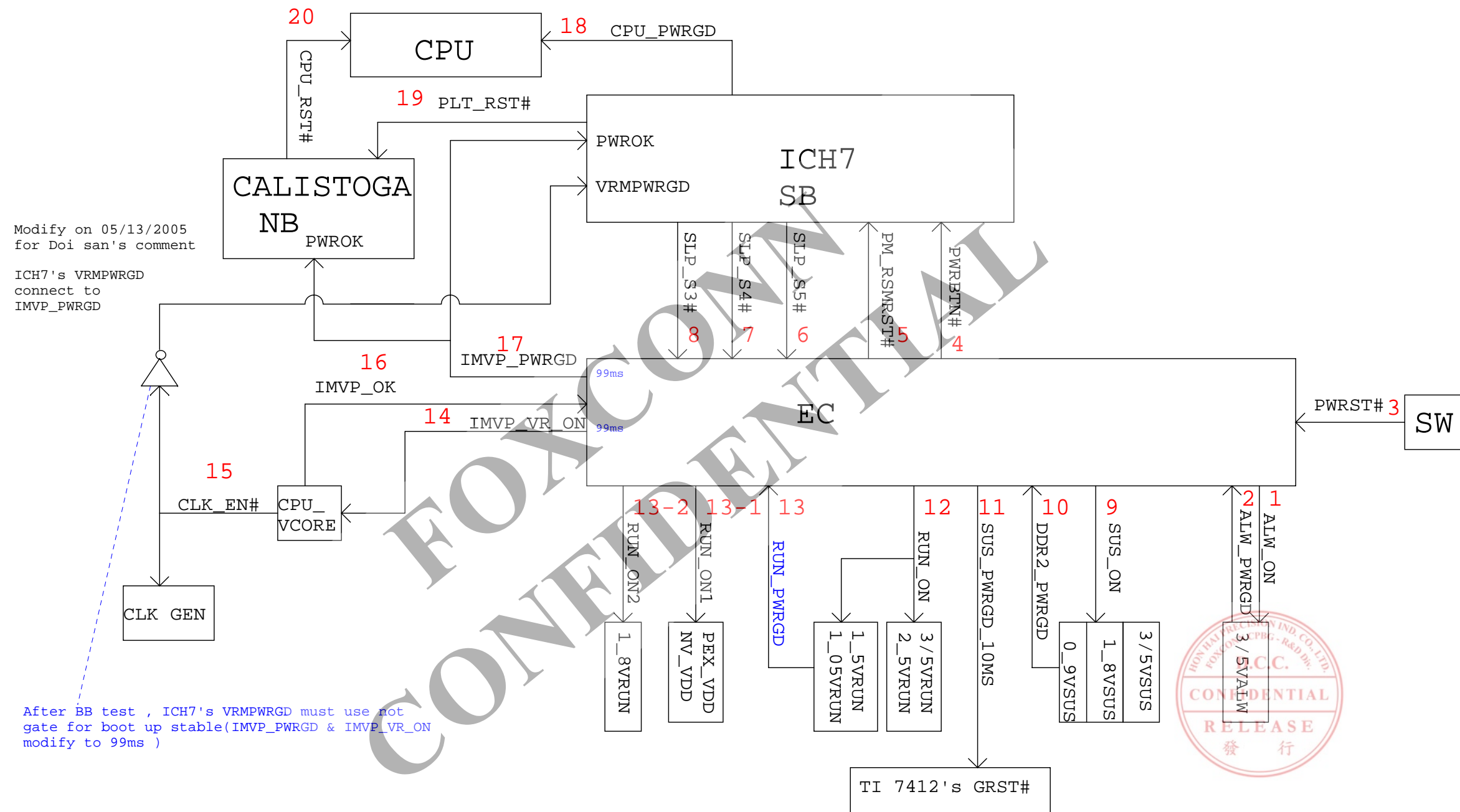
- 1.(page60)FAN noise issue:Add 1000pF(C1662)close EC Add 1000pF(C1666)close PVT rework location(backup only) on net FAN1_TACH(fan feedback),and remove C1657 on net FAN1_PWM(EC to FAN control)
*PVT already modify(Rework Notice item#2)
- 2.(page 70)TV turner noise issue:
(1)Add PR424(2.2 ohm), PC378(47pF) on net MAX8771_LX1,
(2)Add PR425(2.2 ohm), PC379(47pF) on net MAX8771_LX2
(3)PR299 change value from 10 ohm to 0 ohm
*PVT already modify(special noties V0.8)
- 3.(page54)WA of InstantOn later(1)
IR receiver connentor side add N-MOS 2N7002(Q157) for 3V->5V level shift
*PVT already modify(Rework Notice item#3)
- 4.(page60)WA of InstantOn later(2)
EC (U32)GPIO18(pin85)contact to 2N7002 pin1
*PVT already modify(Rework Notice item#3)
- 5.(page29)Modify BOM to desable HDMI connentor SEMI PNP Hot plug detect function:(backup)
(1)U108 change part name to NC_ (not stuff)
(2)Add R1952 (0 ohm) link U84 pin4 to U73 pin2
- 6.(page32)TV module modify BOM roul
(1)Mini PCI socket circuit group change part neam from TV_ to normal.
(2)Special mini stereo jack and S-VIDEO in group change part name from TV_ to JDTVNC_
(JP digital tuner sku NOT stuff)
- 7.(page32)TV Tuner EMC request
(1) add R1950(0 ohm) link net AV_IN_GND to GND
(2) add C1663(470pF) link net AUDIO_IN_L_1 to AV_IN_GND
(3) add C1664(470pF) link net AUDIO_IN_R_1 to AV_IN_GND
(4) add C1665(100pF) link net VIDEO_COMP_1 to AV_IN_GND
- 8.(page66)PD10 Change from 16-MM3216V-T100(Vz=15.3V~17.1V) to 16-MMP2524-6B00(Vz=16.8V)
*PVT already modify(special noties V0.5)
- 9.(page35)Desable HDMI connentor SEMI PNP Hot plug detect function(MOR request)
change part name:
(1)NV73_->NV_:U136,Q155,Q156,R1940,R1941,C1616
(2)NV72_->NC:R1946,R1947
*PVT already modify(special noties V0.4)
- 10.R1493 change part name (G73Only_ ->NV73Only_) to meet BOM configuration
*PVT already modify(special noties V0.6)
- 11.(page57)Q86 change part from 17-MMBT390-6000 (MMBT3906) to 17-MMBT390-6K00 (MMBT3906K)
*PVT already modify(special noties V0.1)
- 12.Modify Bluetooth LED brightness
(1)LED9 change part from 16-HT110NB-0000(Vendor P/N : HT_110NB) to 16-HT110NB-5000.(Vendor P/N : HT-110NB5)
(The same with MS10)
(2)R1839 change part from 1R-0000201-J200 (200ohm,5%,0402) to 1R-0000391-J300.(390 ohm,5%,0603)
(The same with MS10)
- 13.Modify SD LED brightness
LED11 change part from 16-HT110Y0-0000(Vendor P/N : HT_110Y)to 16-HT110UY-0000.(Vendor P/N : HT-110UY)
- 14.(page7~page13) updata U4(NB) part to meet KCL
change from 12-0K58000-A300(945 PM ,QK5800,Version A3) to 12-0G82945-A301(945 PM ,QG82945PM (SL8Z4),Version A3)
- 15.(page37~page41) updata U29(SB) part to meet KCL
change from 12-0K17000-B000(82801GHM1,QK1700,Version B0) to 12-NH82801-0000(NH82801GHM,(SL8YR),Version B0)
- 16.FAN Noise on Int.MIC
(1)Cut-off frequency => 159Hz
R1319 : 2.2k -> 1k
C1232 : 2.2u -> 1u
(2)Cut-off frequency =>7.2kHz
R1318: 22k -> 10k
C1230: 220p -> 2200p
*MOR Nishio-san suggest 3/31
- 17.(page63)Power Button Board Connector back up power plan bypass cap C1507 change to NC
(modify BOM change part name NC_)
- 18.Y7 (6MHZ_20P_30PPM)change part number from secondsource to main source(buyer request)
P/N:(1F-X00006M-3001(AKER) ->1F-X00006M-3002(TXE)
Footprint:(xtal_4p_244_284x205 -> xtal_4p_232_276x197)
*The second already verify on DVT & PVT
- 19.(page43)ESD 10KV on ODD reboot issue
(1)add C1668(100pF) on net ODD_RESET#
(2)add C1667(0.1uF) on net +5VRUN
- 20.(page73)NV_VDD on G73M-U power noise issue, change PR417 (PU16-FB2) from 2K to 2.1K
(to setting NV_VDD voltage on G73M-U from 1.2V to 1.21V)
- 21.(page26)NV_VDD on G73M-U power noise issue,modify BOM configuration,
(1)G73M-U (H) C352,C362,C363,C364 on 22uF / X5R / 0805(1C-2B70226-M100)
(2)G72 (L) / G73 (M) C352,C362,C363,C364 on 10uF / X5R / 0805(1C-2B70106-M100)
- 22.(page31) CN3 (LVDS CONNECTOR) update OrCAN symbol



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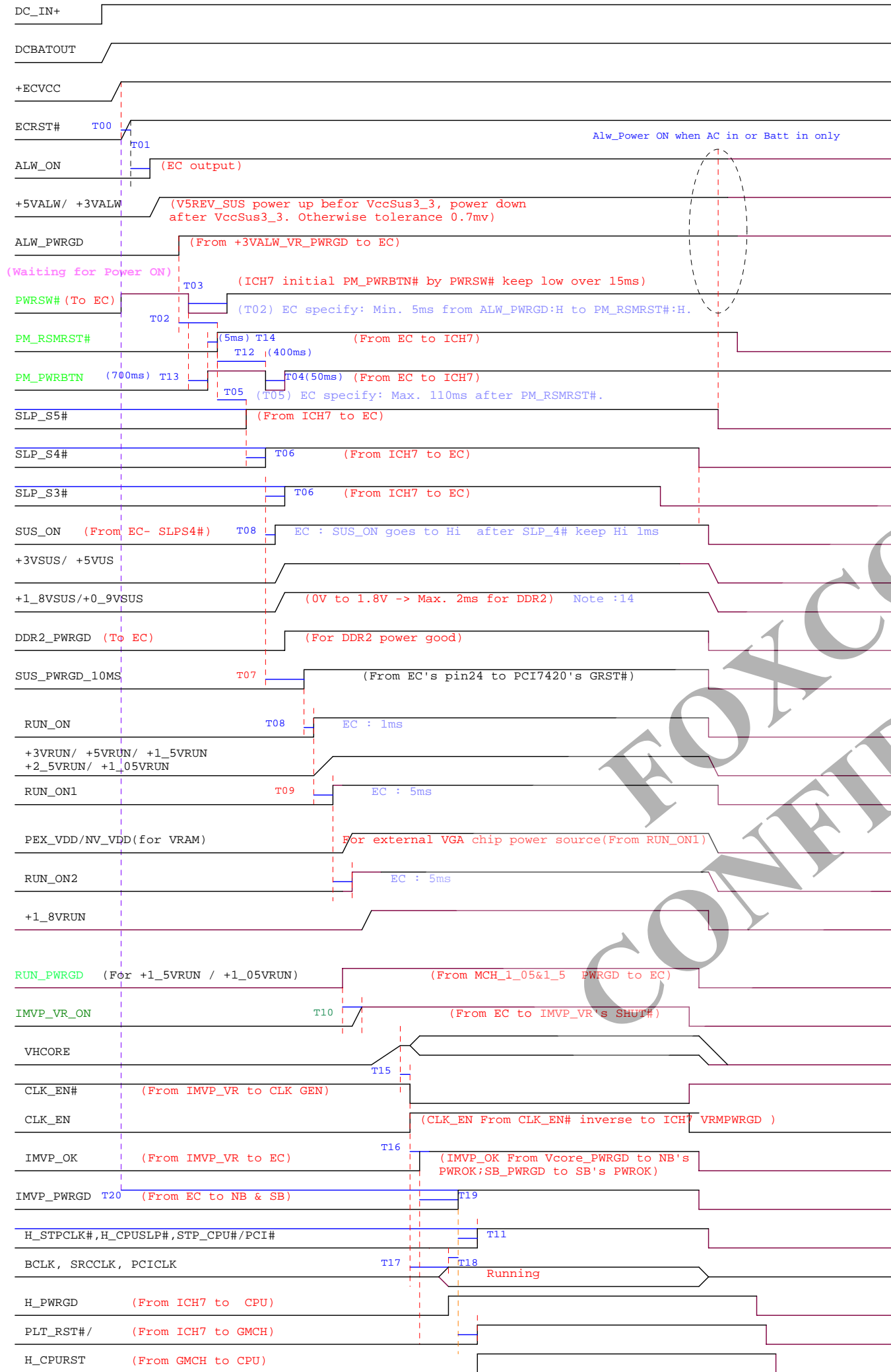
Title History(PVT)		
Size A3	Document Number (MS20-1-01)MainBoard (MBX-156)	Rev 1.00
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MS20 Power On Sequence Block Diagram



MS20 Power On Sequence Timing

Version : 0.1
 Modified date : 2006/4/6



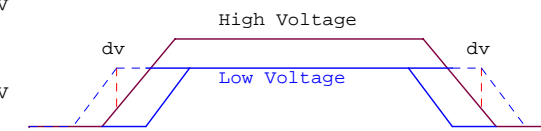
NOTE : (EC KB3910 Min. response time is 1ms)

- T00 : R=47K , C = 0.1uF is ENE recommend value please refer to KB3910B0-AN4A-200
- T01 : When RTC battery already is present, this timing is always meet specification, so we don't control it.
- T02 : ALW_PWRGD:H to PM_RSMRST#:H at least 5ms (Please refer to 16971 Page 300 of t205 timing) Doi-San request 10ms 05/17
- T04 : For MS01 SPEC Min. is 50 ms (Normal SPEC is 20ms)
- T05 : RSMRST# active High to SLP_S5# active High Max. is 110ms (Please reference Intel 16971 Page 301 of t232 timing)
- T06 (Please reference Intel 16971 Page 301 of t234 timing)
- T07 : For MS01 current SPEC Min. is 25 ms (Please refer Intel 16971 Page 301 t208 SPEC is Min 10ms)
- T08 : For MS01 current SPEC Min. is 1 ms (1ms is EC KB3910 at least response time)
- T09 : For MS01 current SPEC
- T10 : Please refer to Intel 16971 Page 300 of t214 timing
- T11 : Please refer to Intel 16971 Page 303 of t216 timing
- T12 : PM_RSMRST# ACTIVE HIGH TO PM_PWRBTN# ACTIVE LOW is 400ms (Normal SPEC is 410ms; Please reference Intel 16971 Page 301 of t232 timing)
- T13 : For MS01 current SPEC Min. is 700 ms (Normal SPEC is 1ms that EC can response)
- T14 : For MS01 current SPEC Min. is 5 ms
- DDR2 1.8V from 0V to 2V Max. is 2 ms please refer to Intel 16981 Page 304
- IMVP_OK is same with SB_PWRGD (reserved And Gate with SYS_PWRGD)
- In NV4X power sequence : NV_VDD , VRAMVDD, PEX_VDD and VRAM_TERM can ramping up anytime after +3VRUN starts ramping up. (Please refer to DG-00969_v05c Page 50 for NV4x GPU power sequencing description)
- T15 : Please refer to MAX8736 datasheet page 7 & page 25 Figure 8
- T16 : Please refer to MAX8736 datasheet page 25 Figure 8
- T17 : Please refer to Intel CK410(14690) page 53
- T18 : The ICH7 drives PLTRST# active a minimum of 1ms when initiated through the Reset Control register I/O Register CF9h)
- CPUPWRGD is an output signal that presents a logical AND of the ICH7's PWROK and VRMPWRGD signals
- T20 : From ECRST# L->H to IMVP_PWRGD L->H. If EC's 32KHz is not stable, LPC I/F will hang. So the 1sec must be guaranteed. (Requested by Doi's san 05/13)



Remark: (Item1,2,3 add Diode; Item4,5,6 add discharge circuit; Item7 for implement TV)
 SPEC please refer to Intel 16981 15.4 GMCH/ICH7M Platform Power -up Requirements)

- V5REF(+5VRUN) -> +3VRUN, dt:0.7mV
- V5REF_SUS(+5VALW) -> +3VALW, dt:0.7mV
- +2_5VRUN -> GMCH_VCC(1.05V), dt:0.7mV
- +1_5VRUN -> +GMCH(1.05V), dt:0.7mV
- +3.3VRUN -> +2_5VRUN, dt:0.3mV
- +3.3VRUN -> +5VRUN (VccLAN), dt:0.3mV
- +3_3VRUN -> +1_5VRUN(TV), dt:0.7mV



R/C delay
 (47K/
 0.1uF)

T00	T01	T02	T03	T04	T05	T06	T07	T08	T09	T10
within 10ns-2ms	Don't control	Min. 10ms	Min. 40ms	Min. 50ms	Max. 110ms	1 - 2 RTCCCLK	Min. 25ms	1ms	Min. 10ms	Min. 99ms
T11	T12	T13	T14	T15	T16	T17	T18	T19	T20	
Max. 50ns	Min. 400ms	Min. 700ms	Min. 5ms	typ 60us	Min : 3ms Max : 8ms	Max 1.8ms	Min 1ms	Min : 99ms	Min : 1s	