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29	VRAM(BYPASS) 1/4	1.0	2007/8/24
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34	CRT	1.0	2007/8/24
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47	PATA CD-ROM	1.0	2007/8/24
48	PCI (PCI BUS)	1.0	2007/8/24
49	PCI (ILINK)	1.0	2007/8/24
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54	EXPRESS	1.0	2007/8/24
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61	AUDIO(CODEC & POWER)	1.0	2007/8/24
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71	CPU_Vcore ---MAX8771	1.0	2007/8/24
72	Others power plan	1.0	2007/8/24
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80		1.0	2007/8/24

P. Leader	Check by	Design by

Project Code & Schematics Subject: M612 PVT Main Board

PCB P/N: 黃田 翰宇博德

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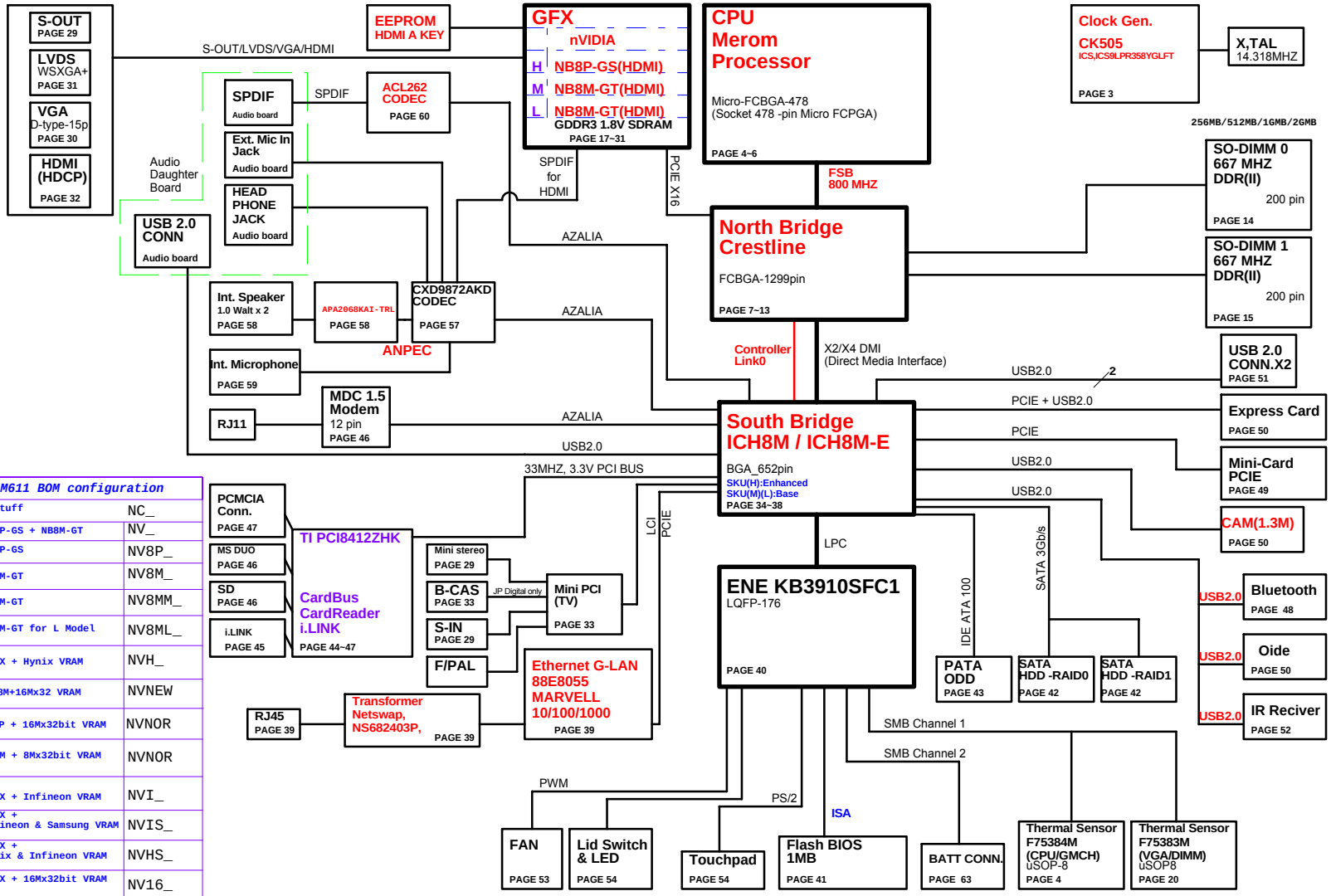
M612(Beagle Santa Rosa)Block Diagram

Red texts:
New modified



M611 BOM configuration	
unstuff	NC_
NB8P-GS + NB8M-GT	NV_
NB8P-GS	NV8P_
NB8M-GT	NV8M_
NB8M-GT	NV8MM_
NB8M-GT for L Model	NV8ML_
NB8X + Hynix VRAM	NVH_
NB8M+16Mx32 VRAM	NVNEW
NB8P + 16Mx32bit VRAM	NVNOR
NB8M + 8Mx32bit VRAM	NVNOR
NB8X + Infineon VRAM	NVI_
NB8X + Infineon & Samsung VRAM	NVIS_
NB8X + Hynix & Infineon VRAM	NVHS_
NB8X + 16Mx32bit VRAM	NV16_
NB8X + 8Mx32bit VRAM	NV8_
*JP Digital TV Tuner SKU unstuff	JDTVNC_
Mini PCI CONN,BT CONN, IR CONN,FeliCa CONN unstuff for L Model	LNC_

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Title: Block Diagram

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11/2 backup
for EMI request
close to R46

FSB Frequency Table:

FSLC	FSLB	FSLA	CPU	SRC[7:0]	PCI	FSB
1	0	1	100	100	33	/
0	0	1	133	100	33	/
0	1	1	166	100	33	667
0	1	0	200	100	33	800
0	0	0	266	100	33	/
1	0	0	333	100	33	/
1	1	0	400	100	33	/
1	1	1	(Reserved)			

If 9LP505, populate R47,R1023,C928,Q23 and depopulate R46.
Ig 9LP501, populate R46 and depopulate R47,R1023,C928,Q23.

Length as short as possible.

This dumping resistor and FB should be placed close to U18, update for MOR requirement on12/23.

pin7 setting 0=SRC8,1=ITP for pin 46,47

pin4 setting 0= Overclocking of CPU and SRC Allowed
1= Overclocking of CPU and SRC NOT allowed

pin6 setting 0= LCD_SST 100MHz differential clock.
for pin17,18 1= 27MHz non-spread SE clock,

close to terminal side (For EMI)

33 MHz Port	M610	MS90
PCI0 (pin1)	NC	NC
PCI1 (pin3)	NC	NC
PCI2 (pin4)	Debug card/EC(KBC)	Debug card
PCI3 (pin5)	PCI8402	PCI8402
PCI4 (pin6)	TV tuner	EC(KBC)
PCI5-F (pin7)	ICH8	ICH8

100 MHz Port	M610 setting configuration	S/W Setting this pin type	S/W Setting CLKREQ for this pin
SRC0 (pin13,14)	GFX PCIE_PEG	(B2b0=0) for use SRC0	
SRC1 (pin17,18)	(SRC0 /SRC1 only either one)		
SRC2 (pin21,22)	PCIE SATA		CR#A (B5b7=1;B5b6=1)
SRC3 (pin24,25)	PCIE ICH8	(B4b7=1;B5b3=0,B5b1=0) for use SRC3	
SRC4 (pin27,28)	PCIE MINI	(B2b1=0) for use SRC4	CR#B (B5b5=1,B5b4=1)
SRC6(pin40,41)	PCIE G-LAN		CR#E (not control)
SRC7(pin43,44)	NC	(B3b3=1,B6b7=0,B6b6=0) for use SRC7(not control CR#E/F)	
SRC8(pin46,47)	NC		CR#F (not control)
SRC9(pin30,31)	MCH 3GPLL		CR#G (B6b5=1)
SRC10(pin34,35)	PCIE EXPRESS		CR#H (B6b4=1)
SRC11(pin32,33)	CR#G(MCH)/CR#H(EXPRESS)	(B3b7=0,B3b6=0 for use CLKREQ G,H)	

SM bus Address :
1101001 (ICH7)
For clock generator

Connect this pin via a 10 K series resistor to the FSC pin on the processor

Connect this pin via a 2.2 K series resistor to the FSA pin on the processor,

Check List 1.301
*.CFG[2:0] do not have internal pullups or pull downs. Please refer to the latest Crestline EDS volume 1 for configuration options
*.1 k pull-up or pull-down or direct connect from processor.

MS90
only MCH_BSEL[0..2]pull down 1K

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Title: CLOCK GEN(CK505)

Size	Document Number	Rev
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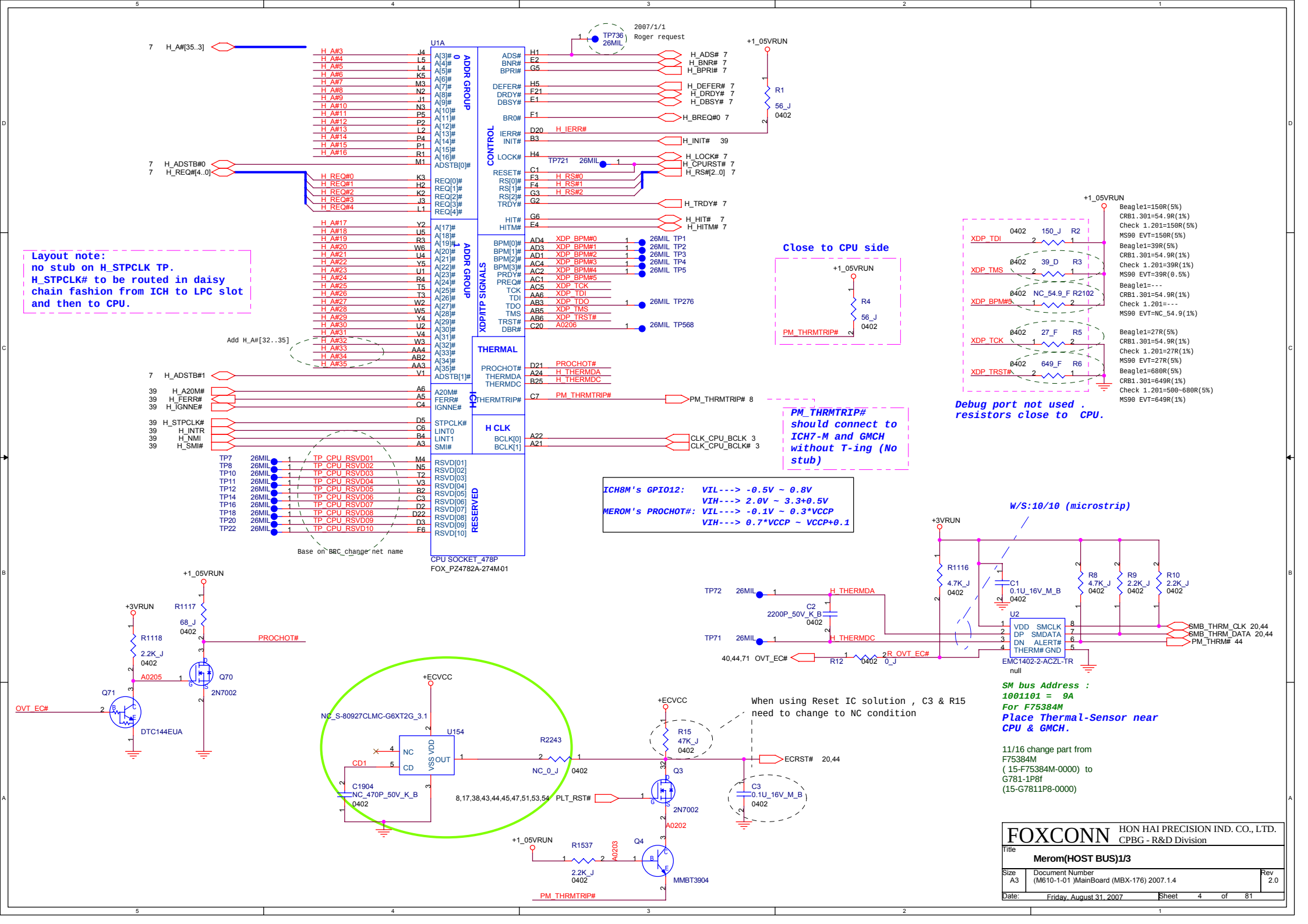
U1A
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERMAL
H CLK
RESERVED
CPU SOCKET_478P
FOX_PZ4782A-274M01
Layout note:
no stub on H_STPCLK TP.
H_STPCLK# to be routed in daisy chain fashion from ICH to LPC slot and then to CPU.
Close to CPU side
PM_THRMTRIP# should connect to ICH7-M and GMCH without T-ing (No stub)
ICH8M's GPIO12: VIL---> -0.5V ~ 0.8V
VIH---> 2.0V ~ 3.3+0.5V
MEROM's PROCHOT#: VIL---> -0.1V ~ 0.3*VCCP
VIH---> 0.7*VCCP ~ VCCP+0.1
Debug port not used . resistors close to CPU.
W/S:10/10 (microstrip)
When using Reset IC solution , C3 & R15 need to change to NC condition
SM bus Address : 1001101 = 9A
For F75384M
Place Thermal-Sensor near CPU & GMCH.
11/16 change part from F75384M
(15-F75384M-0000) to G781-1P8f
(15-G7811P8-0000)
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HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
Merom(HOST BUS)1/3
Document Number (M610-1-01)MainBoard (MBX-176) 2007.1.4
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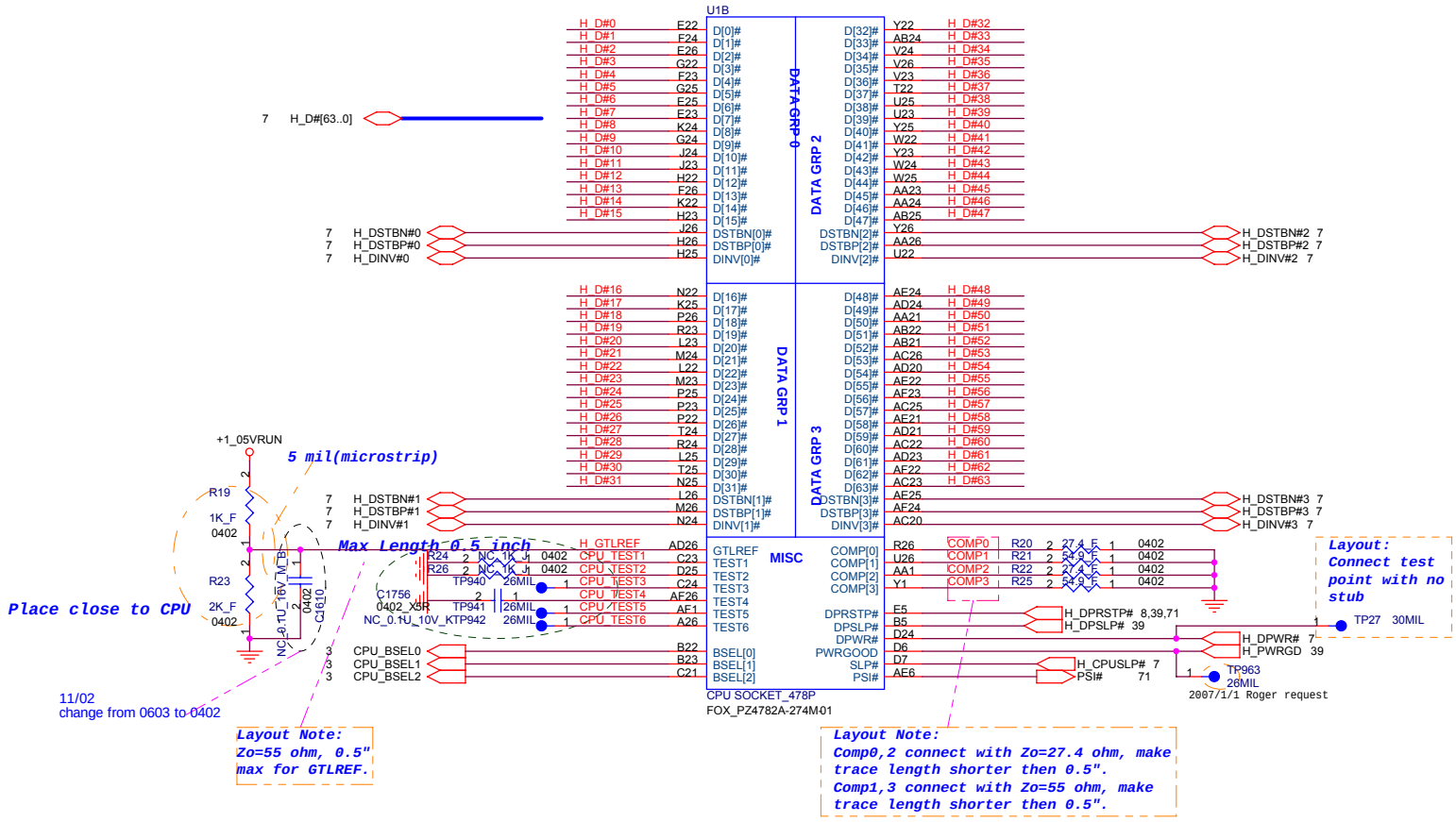

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	Merom(HOST BUS)2/3	
Size A3	Document Number (M610-1-01)MainBoard (MBX-176) 2007.1.4	Rev 2.0
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CPU_VCCA---->130mA
CPU_VCCP----->4.5A
CPU_VCC------>44A

VHCORE

C4 C5 C6 C7 C8 — 22U_6.3V_M_B — 0805

C9 C10 C11 C12 C13 — 22U_6.3V_M_B — 0805

C14 C15 C16 C17 C18 — 22U_6.3V_M_B — 0805

C19 C20 C21 C22 C23 — 22U_6.3V_M_B — 0805

C1642 C1643 C1644 C1645 — NC_10U_6.3V_M — 0805_X5R

C1646 C1647 C1648 C1649 — NC_10U_6.3V_M — 0805_X5R

C1650 C1651 C1652 C1653 — NC_10U_6.3V_M — 0805_X5R

Backup 10uF capacitors for 22uF shortage.

C1271 C1272 C1273 — NC_0.1U_16V_M_B — 0402

C1278 C1279 C1280 — 1000P_50V_K_B — 0402

U1C

CPU SOCKET_478P
FOX_PZ4782A-274M01

Beagle1=10U
CRB1.301=NO
Check 1.201=NO
MS90 EVT=NO

C1554 NC_10U_6.3V_M 0805_X5R
C24 C25 C26 C27 C28 C29 — 0.1U_25V_M_B — 0603

+1_05VRUN

100 mil

CAP26 EEFSX0D331ER 330U_2V_T

CAP7 move from page11
fix PAD location,but change
CAP val from NC_47U to 330U

+1_5VRUN

20 mil

+1_5VRUN_A_CPU

C35 10U_6.3V_M 0805_X5R
C36 0.01U_25V_M_B 0402

R28 0_J 0402

LAYOUT NOTE:
Place 0.01uF
near PIN B26

VID0 R29 VID1 R30 VID2 R31 VID3 R32 VID4 R33 VID5 R35 VID6 R36 — 0_J — 0402

VID0 71
VID1 71
VID2 71
VID3 71
VID4 71
VID5 71
VID6 71

R34 100_F 0402

VCCSENSE AF7 → VCCSENSE 71

VSSSENSE AE7 → VSSSENSE 71

Same Length

R37 100_F 0402

Layout Note: Route
VCCSENSE traces at 27.4
Ohms with 50 mil spacing.
Place PU and PD within 1
inch of cpu.

width=18 mil
spacing=7 mil

(Design check 1.301) 2006.9.3
No Stuff 27.4 ± 1% pull-down to GND
near Intel MVP 6 controller for testing purposes.

MS90 check

U1D

CPU SOCKET_478P
FOX_PZ4782A-274M01

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Title: Merom(POWER/GND)

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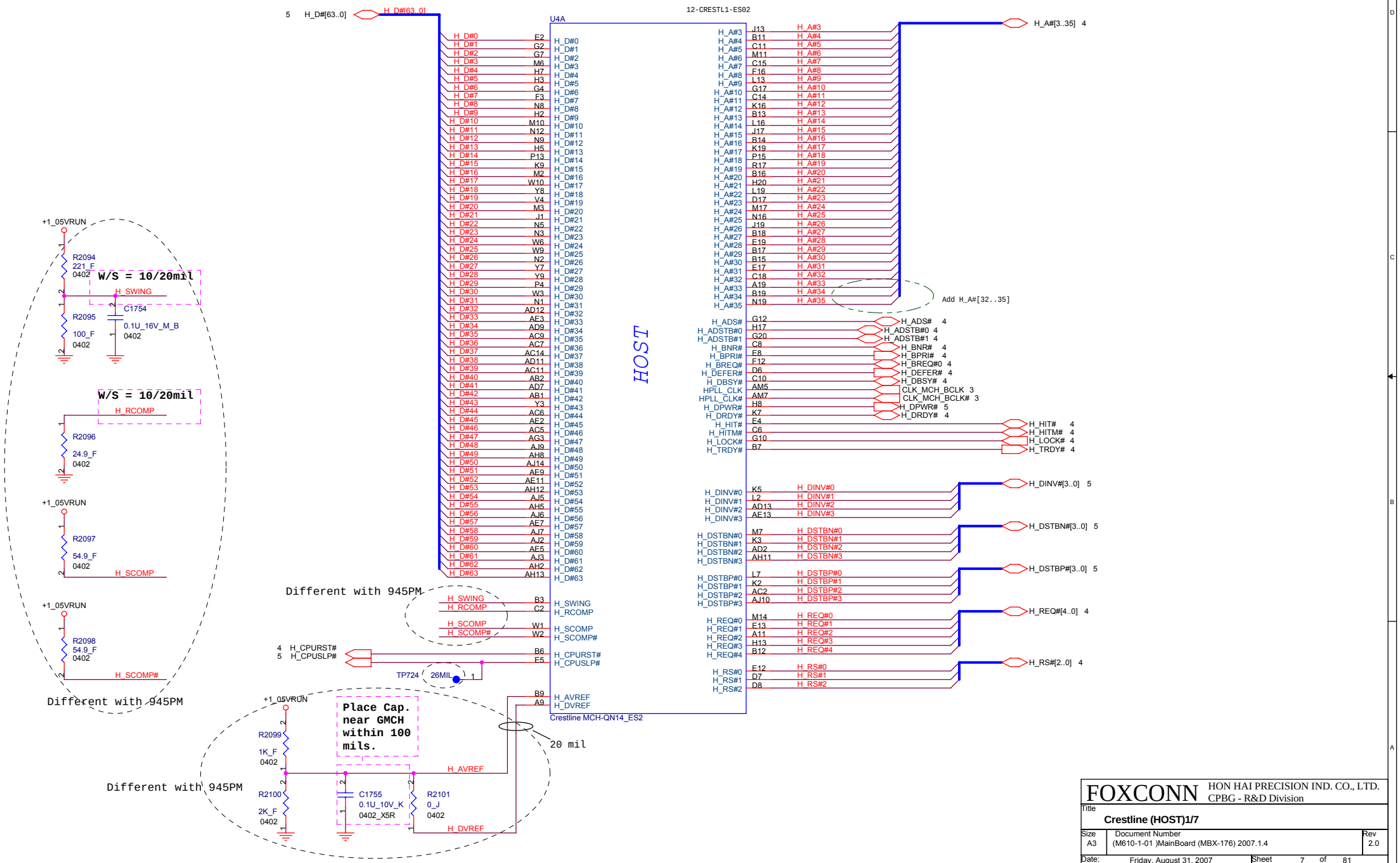

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	Crestline (HOST)1/7	
Size A3	Document Number (M610-1-01)MainBoard (MBX-176) 2007.1.4	Rev 2.0
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U4B

RSVD
DDR MUXING
CLK
DMI
CFG
GRAPHICS VID
PM
ME
MISC
NC

RSVD1 RSVD2 RSVD3 RSVD4 RSVD5 RSVD6 RSVD7 RSVD8 RSVD9 RSVD10 RSVD11 RSVD12 RSVD13 RSVD14

TP881 TP882 TP883 TP884 TP885 TP902 TP886 TP887 TP888 TP889 TP890 TP891 TP892 TP893 26MIL
MCH_RSVD_1 MCH_RSVD_2 MCH_RSVD_3 MCH_RSVD_4 MCH_RSVD_5 MCH_RSVD_6 MCH_RSVD_7 MCH_RSVD_8 MCH_RSVD_9 MCH_RSVD_10 MCH_RSVD_11 MCH_RSVD_12 MCH_RSVD_13 MCH_RSVD_14
P36 P37 R35 N35 AR12 AR13 AM12 AN13 J12 AR37 AM36 AL36 AM37 D20

RSVD20 RSVD21 RSVD22 RSVD23 RSVD24 RSVD25 RSVD26 RSVD27 RSVD28 RSVD29 RSVD30 RSVD31 SA_MA14 SB_MA14 RSVD34 RSVD35 RSVD36 LVDSA_DATA#3 LVDSA_DATA3 RSVD39 RSVD40 RSVD41 RSVD42 RSVD43 RSVD44 RSVD45

TP894 TP895 TP896 TP897 TP898 TP899 TP900 TP901 TP903 TP904 TP905 TP906 TP907 TP908 TP909 TP976 TP977 TP910 TP911 TP912 TP913 TP914 TP915 TP916 26MIL
MCH_RSVD_20 MCH_RSVD_21 MCH_RSVD_22 MCH_RSVD_23 MCH_RSVD_24 MCH_RSVD_25 MCH_RSVD_26 MCH_RSVD_27 MCH_RSVD_28 MCH_RSVD_29 MCH_RSVD_30 MCH_RSVD_31 MCH_RSVD_34 MCH_RSVD_35 MCH_RSVD_36 GM_ODD_RXIN3- GM_ODD_RXIN3+ MCH_RSVD_39 MCH_RSVD_40 MCH_RSVD_41 MCH_RSVD_42 MCH_RSVD_43 MCH_RSVD_44 MCH_RSVD_45
H10 B51 BJ20 BK22 BF19 BH20 BK18 BJ18 BF23 BG23 BC23 BD24 BJ29 BE24 BH39 AW20 BK20 C48 D47 B44 C44 A35 B37 B36 B34 C34

DDR SYSTEM MEM
MS90 /CRB
14,16 M_A_A14
15,16 M_B_A14
M_A_A14
M_B_A14

LVDS
MS90 /CRB

MCH_CFG_9 (PCIE Graphics Lane)	Low = Reverse Lane High = Normal operation

For layout convenience

CFG[2:0]
010 = FSB 800 MHz
011 = FSB 667 MHz

3 MCH_BSEL0 P27
3 MCH_BSEL1 N27
3 MCH_BSEL2 N24

TP978 TP979 TP980 TP981 TP982 TP983 TP984 TP985 TP986 TP987 TP988 TP989 TP990 TP991 TP992 TP993 TP994 TP995 26MIL
MCH_CFG_3 MCH_CFG_4 MCH_CFG_5 MCH_CFG_6 MCH_CFG_7 MCH_CFG_8 MCH_CFG_9 MCH_CFG_10 MCH_CFG_11 MCH_CFG_12 MCH_CFG_13 MCH_CFG_14 MCH_CFG_15 MCH_CFG_16 MCH_CFG_17 MCH_CFG_18 MCH_CFG_19 MCH_CFG_20
C21 C23 F23 N23 G23 J20 C20 R24 L23 J23 E23 E20 K23 M20 M24 L32 N33 L35

CFG0 CFG1 CFG2 CFG3 CFG4 CFG5 CFG6 CFG7 CFG8 CFG9 CFG10 CFG11 CFG12 CFG13 CFG14 CFG15 CFG16 CFG17 CFG18 CFG19 CFG20

CFG[17:3] internal pull-up
CFG[20:18] internal pull-down

Wait to confirm with Page 13 / CRB

40 PM_BMBUSY# G41
5,39,71 H_DPRSTP# L39
14 PM_EXTTS#0 L36
15 PM_EXTTS#1 J36
49,44 IMVP_PWRGD AW49
4,17,38,43,44,45,47,51,53,54 PLT_RST# AV20
4 PM_THRMTRIP# N20
40,71 DPRSLVPR G36

R109 1_100_J 0402 PLT_RST# R
PM_THRMTRIP#

PM_BM_BUSY# PM_DPRSTP# PM_EXT_TS#0 PM_EXT_TS#1 PWROK RSTIN# THERMTRIP# DPRSLVPR

Design check 1.201
DDR2 Connect to PM_EXT_TS#0/1 pins
of GMCH, pull up with 10K to Vcc3_3

+3VRUN
R2088 10K_J 0402 PM_EXTTS#1
R2091 10K_J 0402 PM_EXTTS#0
20,44 DDR_ALERT# R1143 0_J 0402 PM_EXTTS#0

Form (U8)thermal sanser & (EC)

TP923 TP924 TP925 TP926 TP927 TP928 TP929 TP930 TP931 TP932 TP933 TP934 TP935 TP936 TP938 TP939 26MIL
MCH_NC1 MCH_NC2 MCH_NC3 MCH_NC4 MCH_NC5 MCH_NC6 MCH_NC7 MCH_NC8 MCH_NC9 MCH_NC10 MCH_NC11 MCH_NC12 MCH_NC13 MCH_NC14 MCH_NC15 MCH_NC16
BJ51 BK51 BK50 BL50 BL49 BL3 BL2 BK1 BJ1 E1 A5 C51 B50 A50 A49 BK2

NC1 NC2 NC3 NC4 NC5 NC6 NC7 NC8 NC9 NC10 NC11 NC12 NC13 NC14 NC15 NC16

Crestline MCH-QN14_ES2

SM_CK0 SM_CK1 SM_CK3 SM_CK4 AV29 BB23 BA25 AV23 M_CLK_DDR0 14 M_CLK_DDR1 14 M_CLK_DDR2 15 M_CLK_DDR3 15
SM_CK#0 SM_CK#1 SM_CK#3 SM_CK#4 AW30 BA23 AW25 AW23 M_CLK_DDR#0 14 M_CLK_DDR#1 14 M_CLK_DDR#2 15 M_CLK_DDR#3 15
SM_CKE0 SM_CKE1 SM_CKE3 SM_CKE4 BE29 AY32 BD39 BG37 M_CKE0 14,16 M_CKE1 14,16 M_CKE2 15,16 M_CKE3 15,16
SM_CS#0 SM_CS#1 SM_CS#2 SM_CS#3 BG20 BK16 BG16 BE13 M_CS#0 14,16 M_CS#1 14,16 M_CS#2 15,16 M_CS#3 15,16
SM_ODT0 SM_ODT1 SM_ODT2 SM_ODT3 BH18 BJ15 BJ14 BE16 M_ODT0 14,16 M_ODT1 14,16 M_ODT2 15,16 M_ODT3 15,16

SM_RCOMP BL15 SM_RCOMP R2076 1 20_F 2 0402 +1_8VSUS
SM_RCOMP# BK14 SM_RCOMP# R2077 1 20_F 2 0402
SM_RCOMP_VOH BK31 SM_RCOMP_VOH
SM_RCOMP_VOL BL31 SM_RCOMP_VOL
SM_VREF0 AR49 SMDDR_VREF
SM_VREF1 AW4

+1_8VSUS
R2073 1K_F 0402 waiting change 0.1%
SM_RCOMP_VOH
R2074 3.01K_F 0402
C1745 0.01U_16V_K_B 0402
C1746 2.2U_10V_Y 0603_Y5V
SM_RCOMP_VOL
R2075 1K_F 0402 waiting change 0.1%
C1747 0.01U_16V_K_B 0402
C1748 2.2U_10V_Y 0603_Y5V

Note:If the voltage regulator for the system memory interface already supplies a VREF output and meets the voltage tolerance and current requirements for these pins, then a voltage divider would not be needed.

DPLL_REF_CLK B42 DREFCLK
DPLL_REF_CLK# C42 DREFCLK#
DPLL_REF_SSCLK H48 DREFSSCLK
DPLL_REF_SSCLK# H47 DREFSSCLK#
PEG_CLK K44 CLK_MCH_3GPLL 3
PEG_CLK# K45 CLK_MCH_3GPLL# 3

DDRDIMM_VREF
R2079 0_J 0402
SMDDR_VREF
C1751 0.1U_16V_M_B 0402
C1752 0.1U_16V_M_B 0402

DMI_RXN0 DMI_RXN1 DMI_RXN2 DMI_RXN3 AN47 AJ38 AN42 AN46 DMI_TXN0 DMI_TXN1 DMI_TXN2 DMI_TXN3 DMI_TXN[3:0] 38
DMI_RXP0 DMI_RXP1 DMI_RXP2 DMI_RXP3 AM47 AJ39 AN41 AN45 DMI_TXP0 DMI_TXP1 DMI_TXP2 DMI_TXP3 DMI_TXP[3:0] 38
DMI_TXN0 DMI_TXN1 DMI_TXN2 DMI_TXN3 AJ46 AJ41 AM40 AM44 DMI_RXN0 DMI_RXN1 DMI_RXN2 DMI_RXN3 DMI_RXN[3:0] 38
DMI_TXP0 DMI_TXP1 DMI_TXP2 DMI_TXP3 AJ47 AJ42 AM39 AM43 DMI_RXP0 DMI_RXP1 DMI_RXP2 DMI_RXP3 DMI_RXP[3:0] 38

External Graphics (GMCH CRT/TVOUT Disable)
R2082 NV_0_J 0402 DREFCLK
R2083 NV_0_J 0402 DREFCLK#
R2084 NV_0_J 0402 DREFSSCLK
R2085 NV_0_J 0402 DREFSSCLK#

GFX_VID0 GFX_VID1 GFX_VID2 GFX_VID3 GFX_VR_EN E35 A39 C38 B39 E36 DFGT_VID_0 DFGT_VID_1 DFGT_VID_2 DFGT_VID_3 DFGT_VR_EN
26MIL TP971 26MIL TP972 26MIL TP973 26MIL TP974 26MIL TP975

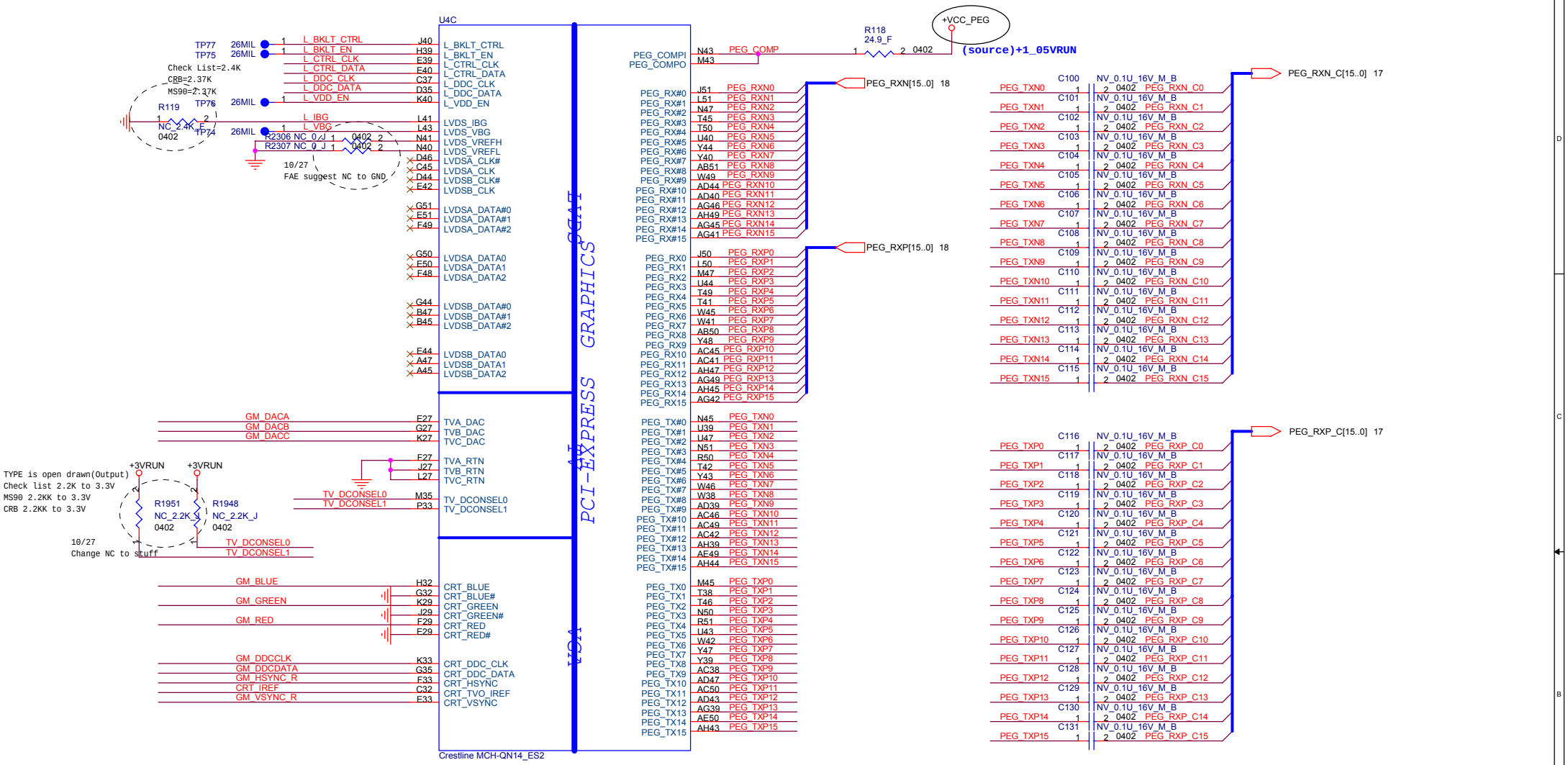
CL_CLK AM49 CL_CLK0 40
CL_DATA AK50 CL_DATA0 40
CL_PWROK AT43 MPWROK 40
CL_RST# AN49 CL_RST#0 40
CL_VREF AM50 MCH_CLVREF

+1_25VRUN
R2086 1K_F 0402
R2087 392_F 0402
C1753 0.1U_10V_K 0402_X5R

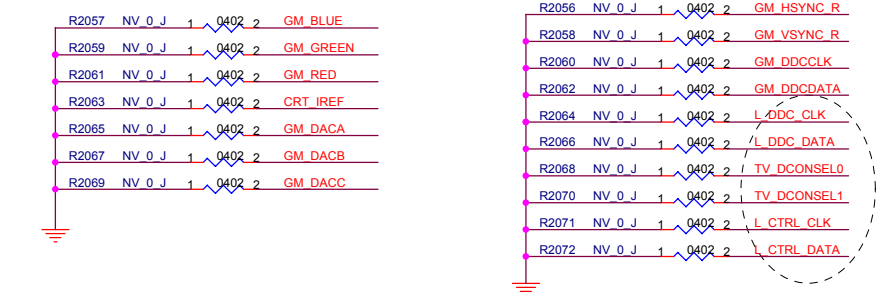
SDVO_CTRL_CLK H35 SDVO_CTRLCLK
SDVO_CTRL_DATA K36 SDVO_CTRLDATA
CLKREQ# G39 MCH_CLK_REQ#
ICH_SYNC# G40
R2089 NV_0_J 0402
R2090 NV_0_J 0402
MCH_CLK_REQ# 3
MCH_ICH_SYNC# 40
MCH_CLK_REQ# 1 26MIL TP937

TEST1 A37 MCH_TEST_1
TEST2 R32 MCH_TEST_2
R2092 20K_J 0402
R2093 0_J 0402

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	Crestline (DMI)2/7
Size A3	Document Number (M610-1-01)MainBoard (MBX-176) 2007.1.4 Rev 2.0
Date: Friday, August 31, 2007	Sheet 8 of 81

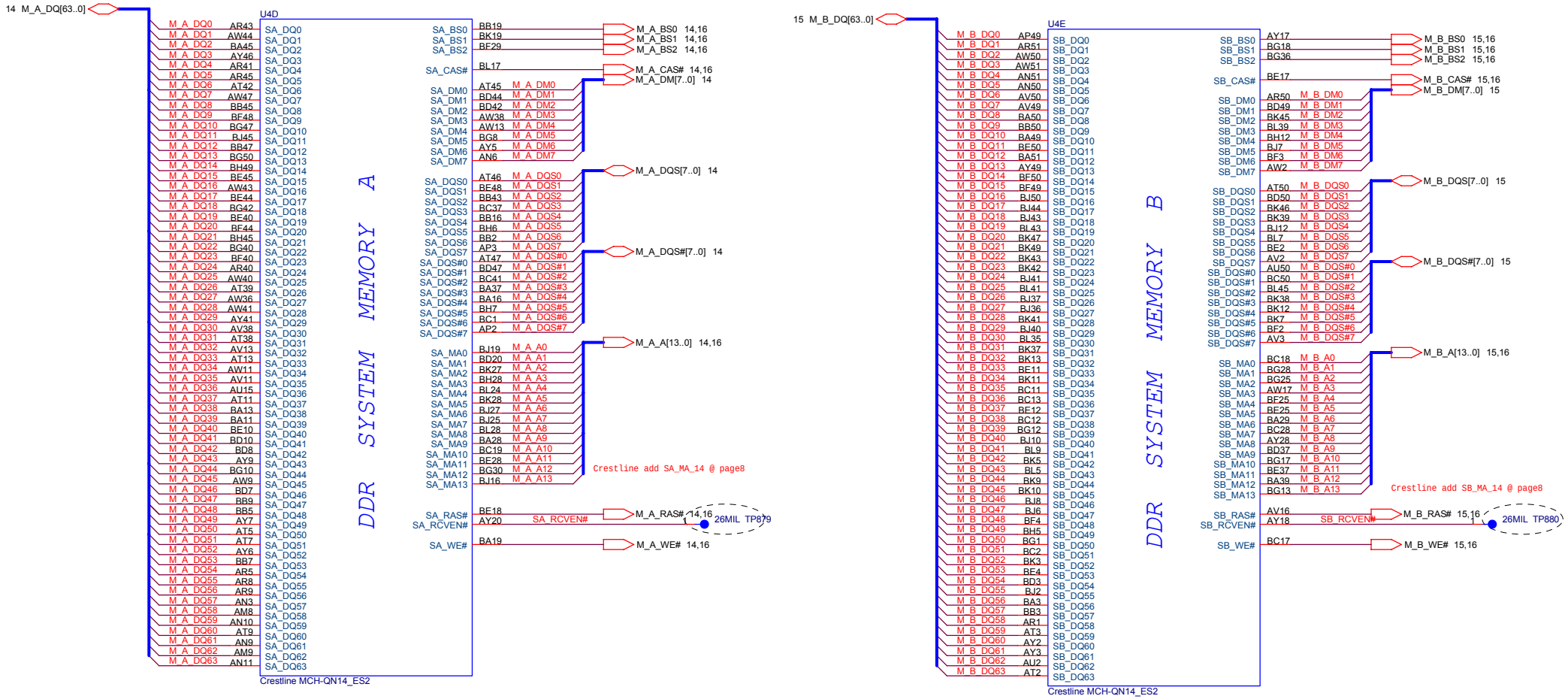


External Graphics (GMCH CRT/TVOUT Disable)



Base on below document:
Mobile Merom Processor and Crestline Chipset
- Santa Rosa Platform Design Guide-21112,1.0
.pvd.pdf (May 2006/ Rev 1.0)page 193
Table 82. External Graphics (GMCH Integrated Graphics Disable)
Connect these signals to GND

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	Crestline(GRAPHIC)3/7	
Size A3	Document Number (M610-1-01)MainBoard (MBX-176) 2007.1.4	Rev 2.0
Date: Friday, August 31, 2007	Sheet 9 of 81	

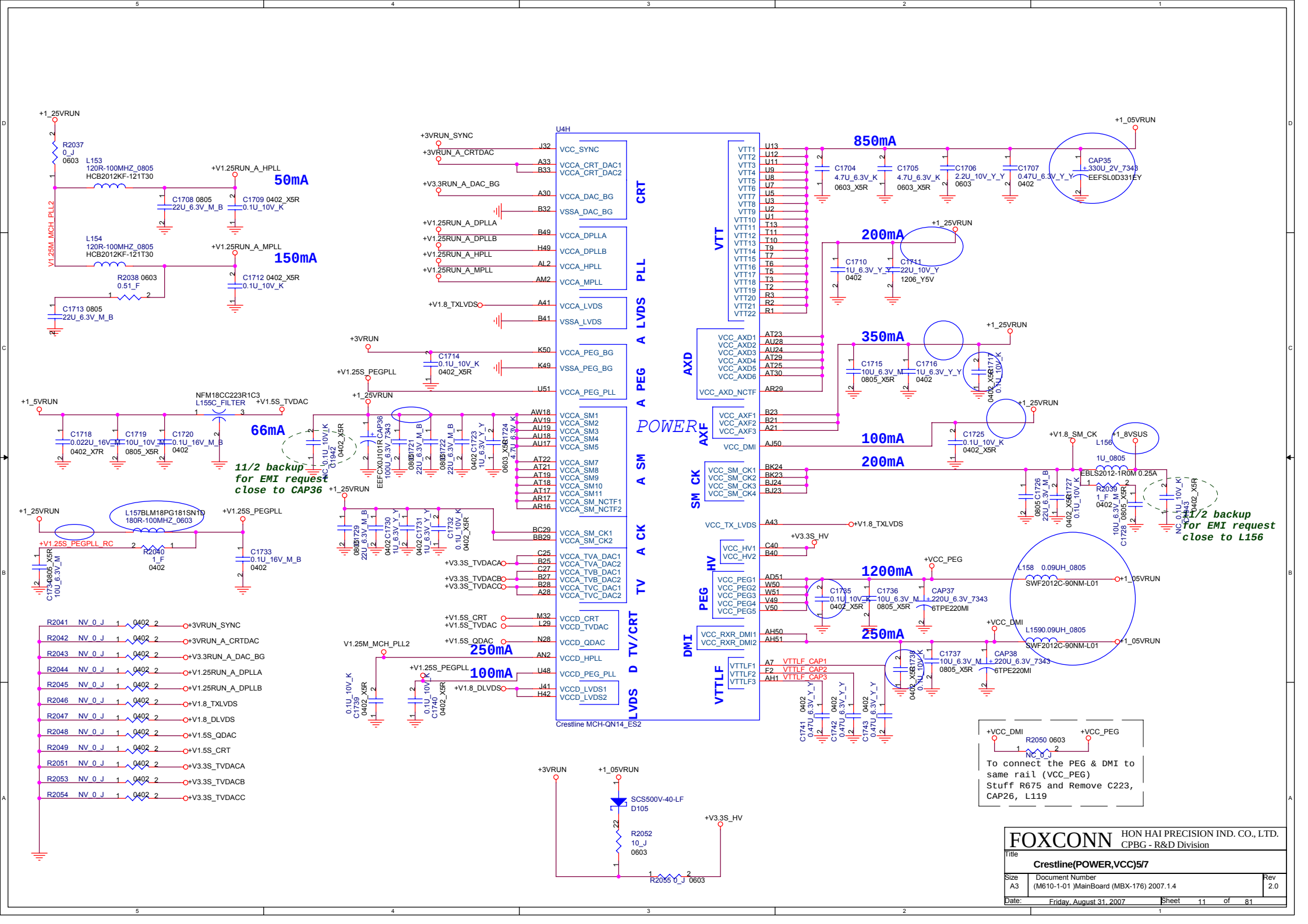


FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: **Crestline(DDRII)4/7**

Size	Document Number	Rev
A3	(M610-1-01)MainBoard (MBX-176) 2007.1.4	2.0

Date: Friday, August 31, 2007 Sheet 10 of 81

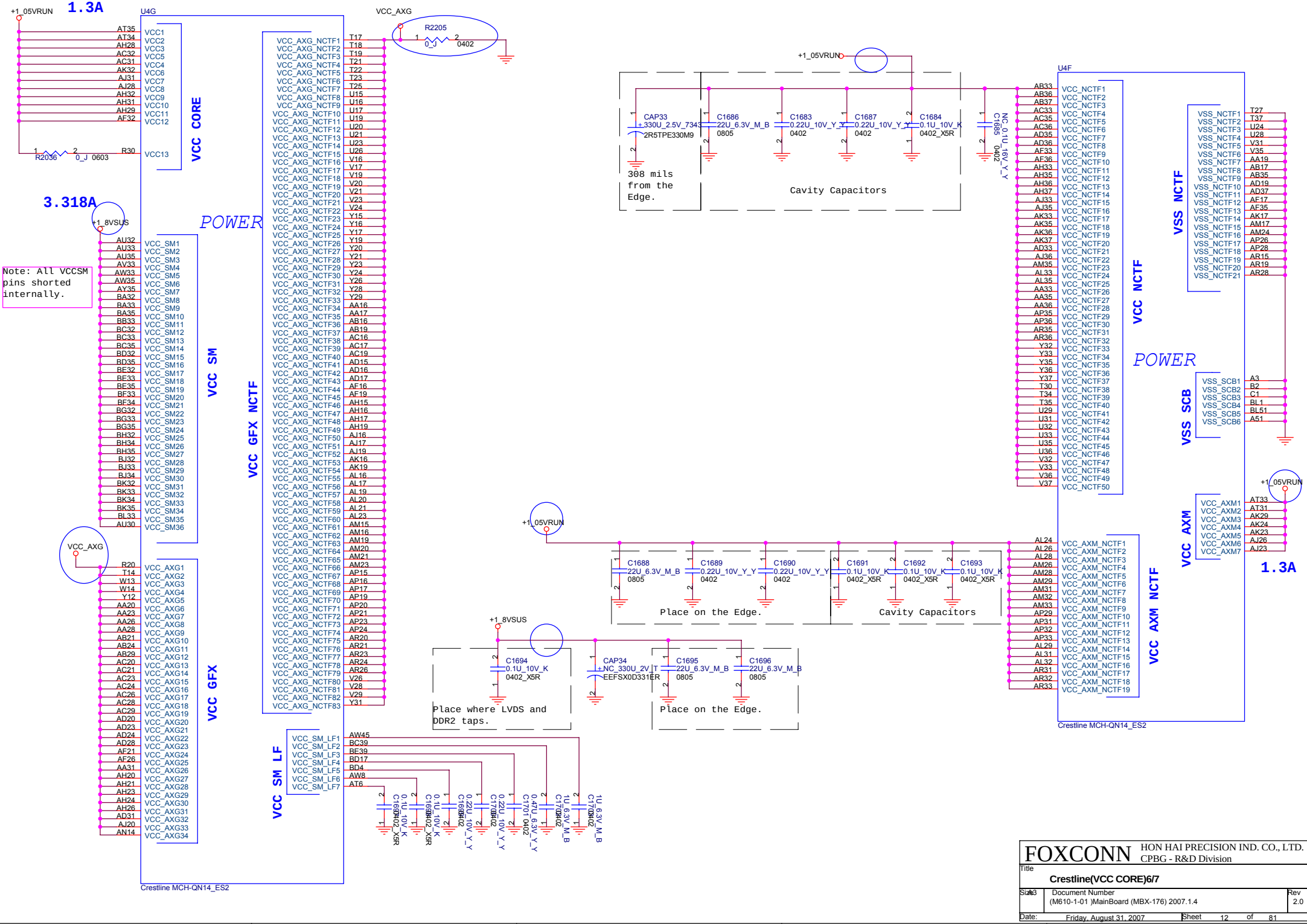


FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: Crestline(POWER,VCC)5/7

Size	Document Number	Rev
A3	(M610-1-01)MainBoard (MBX-176) 2007.1.4	2.0

Date: Friday, August 31, 2007 Sheet 11 of 81

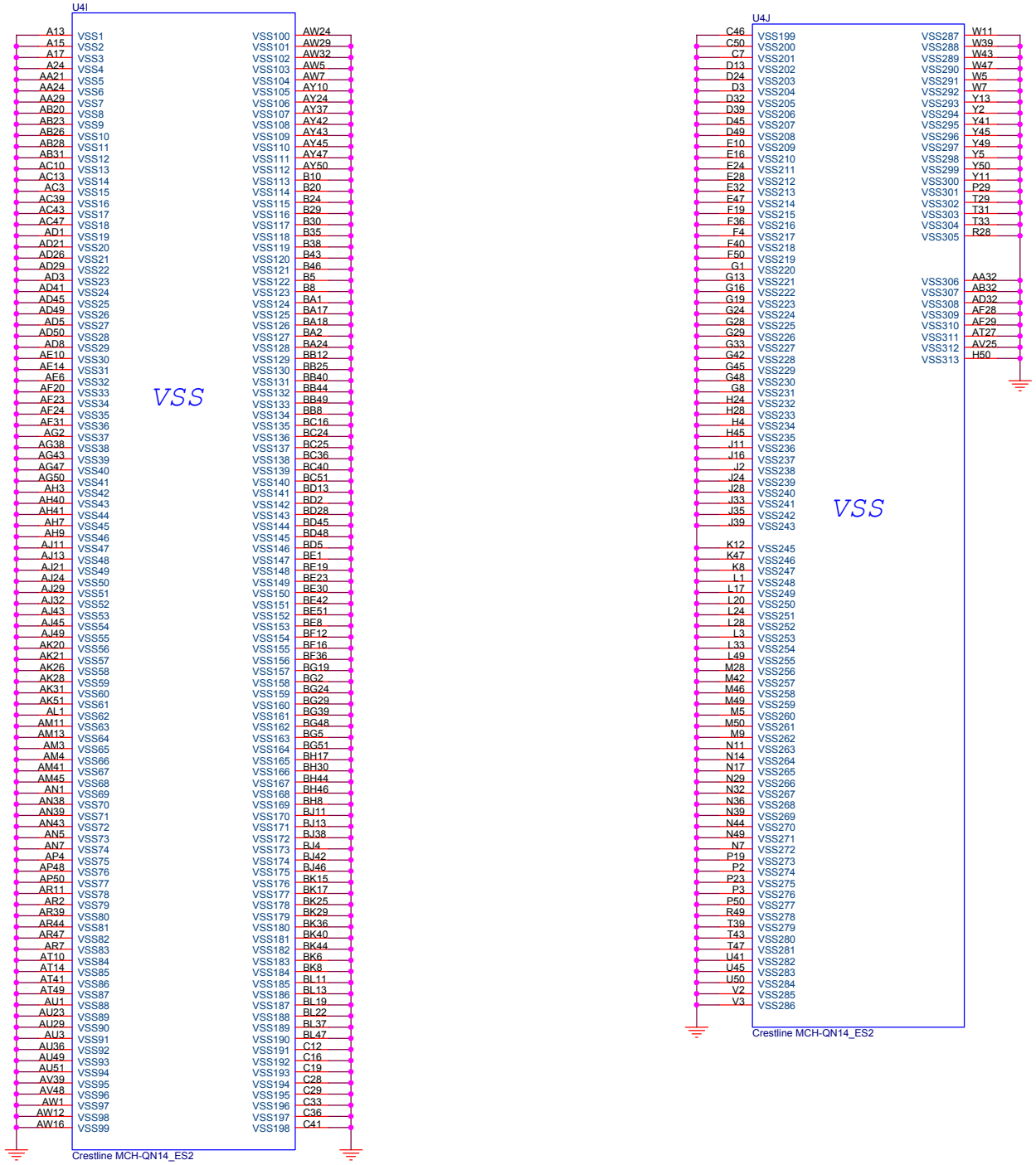


FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

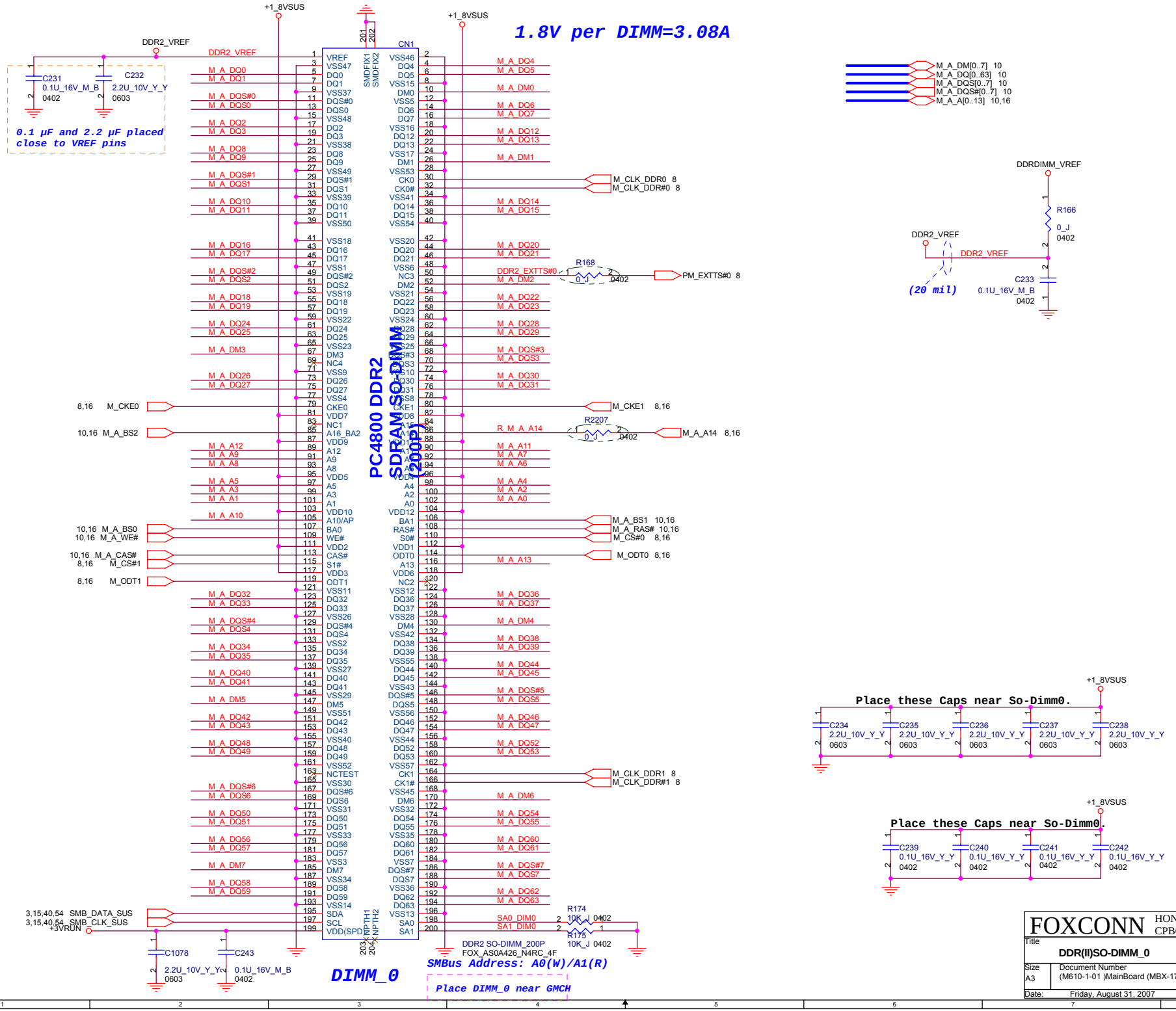
Title: Crestline(VCC CORE)6/7

Size: A3 | Document Number: (M610-1-01)MainBoard (MBX-176) 2007.1.4 | Rev: 2.0

Date: Friday, August 31, 2007 | Sheet 12 of 81



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	Crestline (VSS)7/7
Size: A3	Document Number: (M610-1-01)MainBoard (MBX-176) 2007.1.4
Rev	2.0
Date:	Friday, August 31, 2007
Sheet	13 of 81

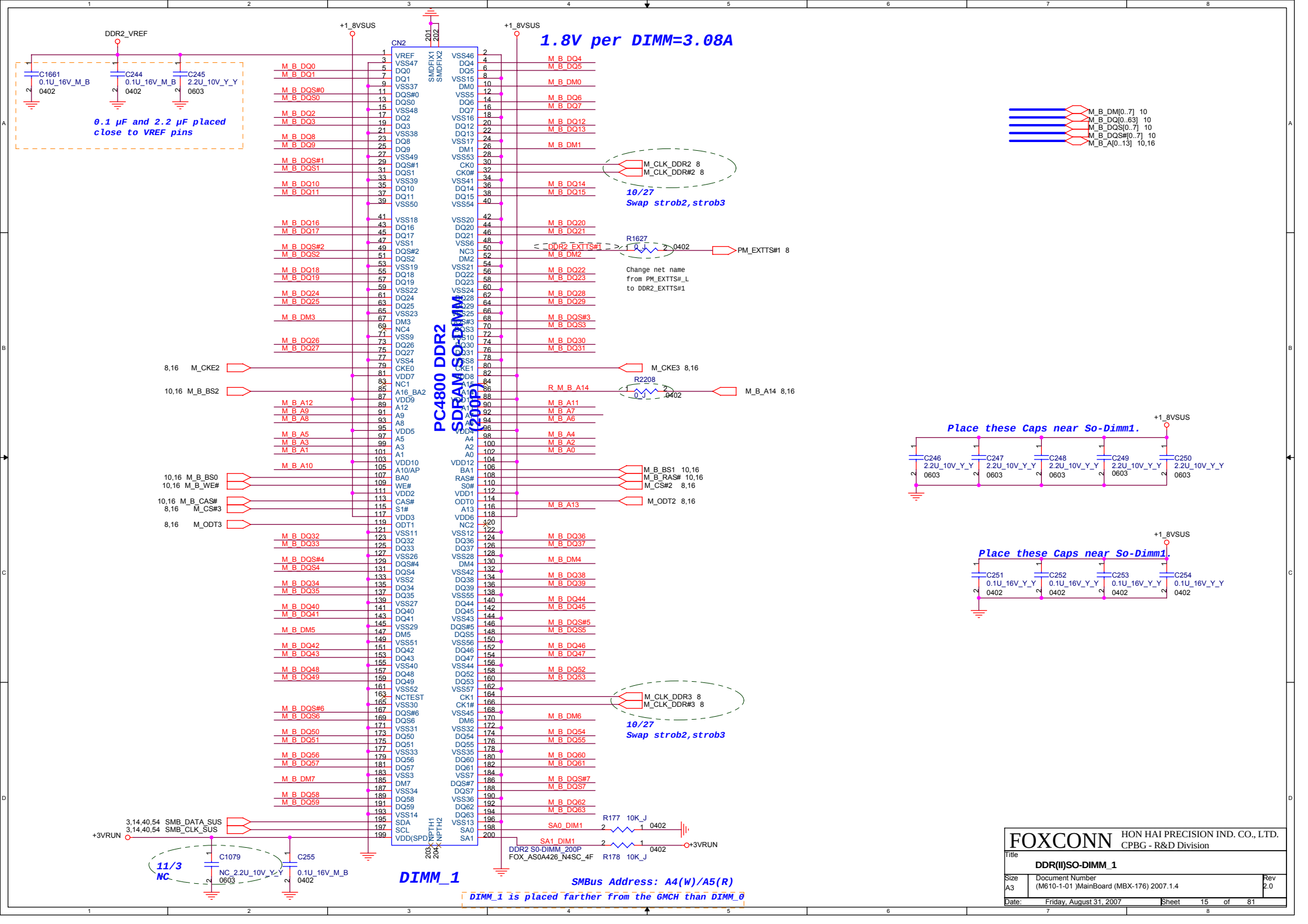


FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: DDR(II)SO-DIMM_0

Size	Document Number	Rev
A3	(M610-1-01)MainBoard (MBX-176) 2007.1.4	2.0

Date: Friday, August 31, 2007 Sheet 14 of 81

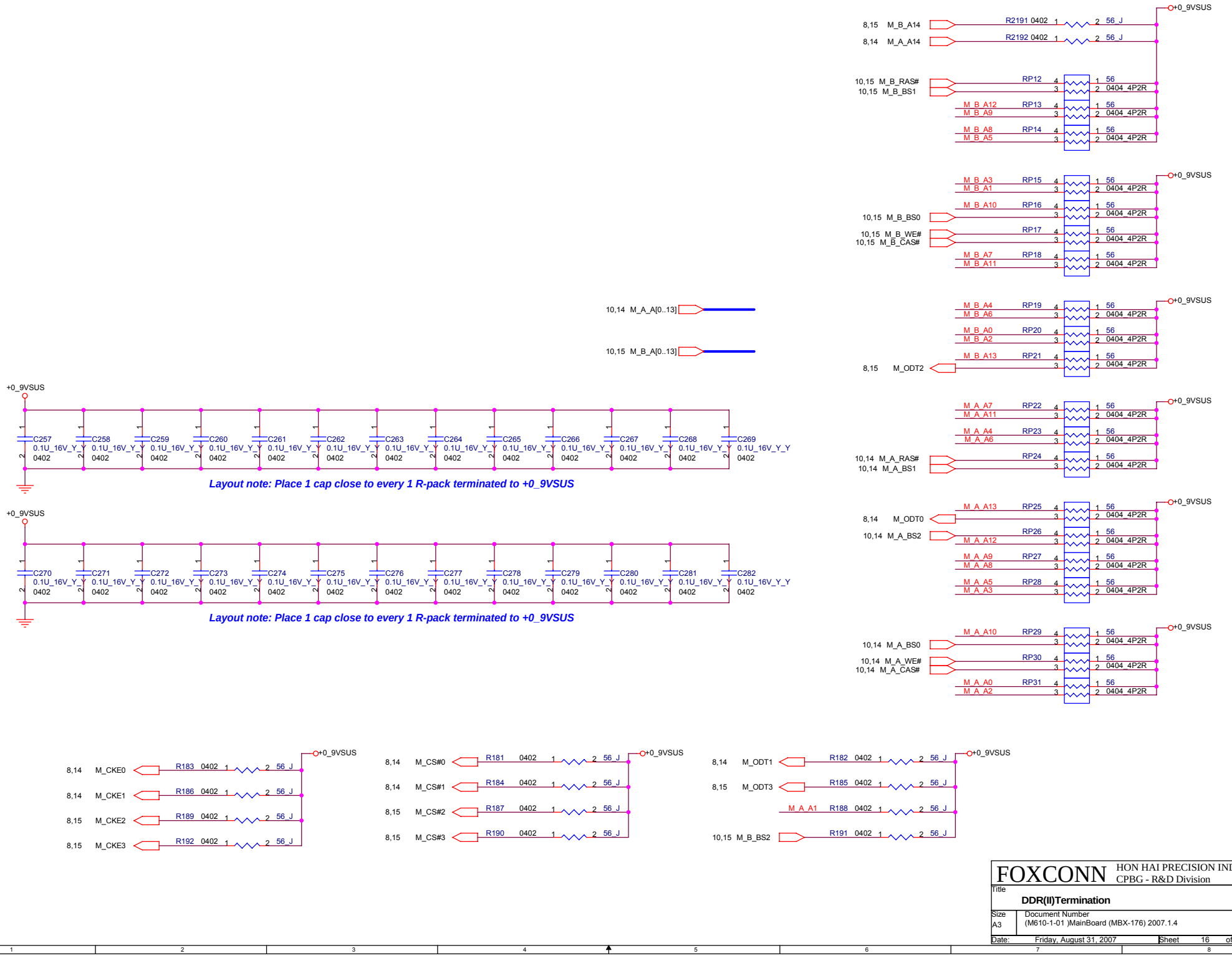


FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: DDR(II)SO-DIMM_1

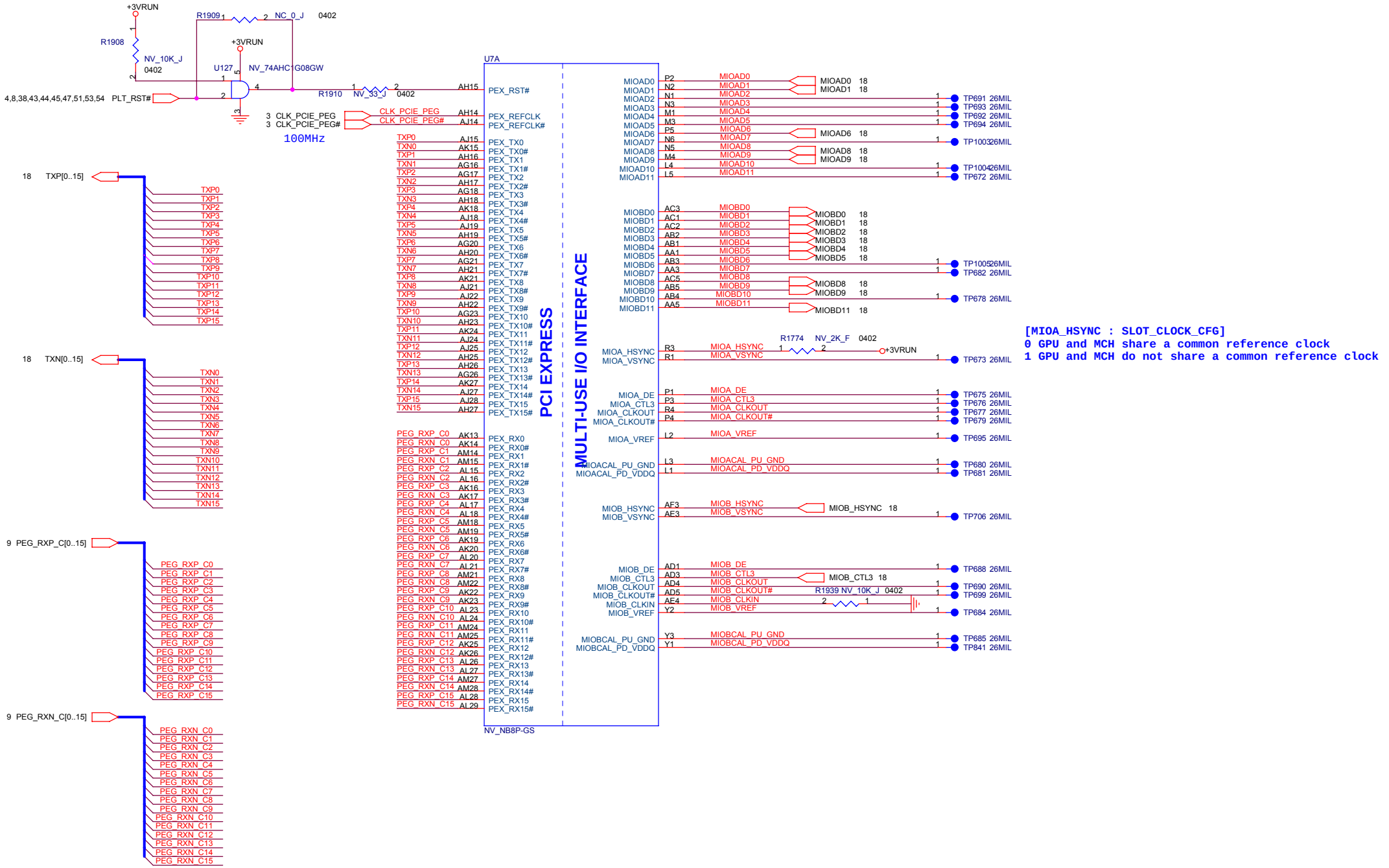
Size: A3 | Document Number: (M610-1-01)MainBoard (MBX-176) 2007.1.4 | Rev: 2.0

Date: Friday, August 31, 2007 | Sheet 15 of 81

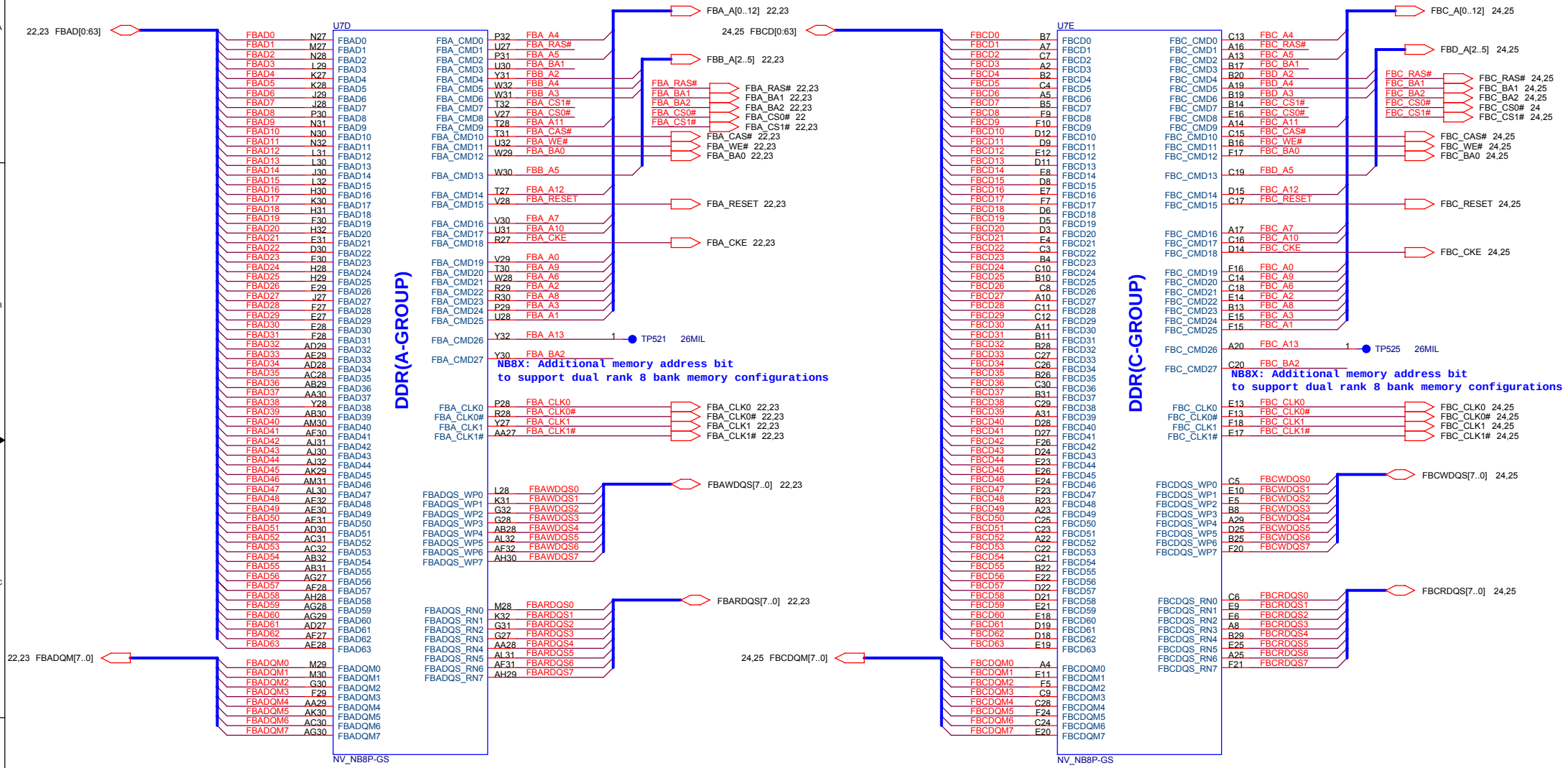


FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	DDR(II)Termination	
Size A3	Document Number (M610-1-01)MainBoard (MBX-176) 2007.1.4	Rev 2.0
Date: Friday, August 31, 2007	Sheet 16 of 81	

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	VGA (PCI-EXPRESS/STRAP) 2 OF 8
Size A3	Document Number (M610-1-01)MainBoard (MBX-176) 2007.1.4 2.0 Rev
Date: Friday, August 31, 2007	Sheet 18 of 81



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	VGA (PCI EXPRESS) 1 OF 8	
Size A3	Document Number (M610-1-01)MainBoard (MBX-176) 2007.1.4	Rev 2.0
Date: Friday, August 31, 2007	Sheet 17 of 81	



FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: VGA (GDDR) 3 OF 8

Size	Document Number	Rev
A3	(M610-1-01)MainBoard (MBX-176) 2007.1.4	2.0

Date: Friday, August 31, 2007 Sheet 19 of 81

SM bus Address :
1001100(EC)
For F75383M

Use GPU internal thermal sensor
Change R2328,R2329 form NC to mount

4,44 SMB_THRM_CLK
4,44 SMB_THRM_DATA
R2328 NV_0_J 0402
R2329 NV_0_J 0402
SMB_THRM_CLK
SMB_THRM_DATA
NV_I2CS_SCL
NV_I2CS_SDA

HDCP
HDCP_SCL
HDCP_SDA

Backup
NV_I2CC_SCL
NV_I2CC_SDA

HDMI DDC
36 NV_I2CB_SCL
36 NV_I2CB_SDA
NV_I2CB_SCL
NV_I2CB_SDA

CRT DDC
34 NV_I2CA_SCL
34 NV_I2CA_SDA
NV_I2CA_SCL
NV_I2CA_SDA

U7F

I2C
I2CS_SCL C1
I2CS_SDA B1
I2CH_SCL G3
I2CH_SDA H3
I2CC_SCL G2
I2CC_SDA G1
I2CB_SCL H4
I2CB_SDA J4
I2CA_SCL K2
I2CA_SDA J3

ROM
ROMCS# AA4
ROM_SO AA6
ROM_SI W2
ROM_SCLK AA7

TEST SIGNAL
IFPAB_VPROBE AM4
IFPCD_VPROBE AK3
PEX_TSTCLK_OUT AM12
PEX_TSTCLK_OUT# AM11
FBA_DEBUG AC27
FBC_DEBUG F12
TESTMODE H2
JTAG_TCK AJ11
JTAG_TMS AK11
JTAG_TDI AK12
JTAG_TDO AL12
JTAG_TRST_N AL13

CRYSTAL
XTALSSIN T1
XTALOUTBUFF T2
XTALIN U1
XTALOUT U2

GENERAL SIGNALS
THERMDN J1
THERMDP K1
BUFRST# F3
STEREO T3
SWAPRDY_A M6
MEMSTRAPSEL0 AF26
MEMSTRAPSEL1 AD26
MEMSTRAPSEL2 AH31
MEMSTRAPSEL3 AH32

GPIO
GPIO0 K3
GPIO1 H1
GPIO2 K5
GPIO3 G5
GPIO4 E2
GPIO5 J5
GPIO6 G6
GPIO7 K6
GPIO8 E1
GPIO9 D2
GPIO10 H5
GPIO11 F4
GPIO12 E3
GPIO13 U3
GPIO14 U4

NV_NB8P-GS

NV_THERMDN
NV_THERMDP
C485 0402 NV_2200P_50V_K_B
BUFRST# 1 TP100626MIL
STEREO 1 TP137 26MIL
SWAPRDY 1 TP696 26MIL
MEMSTRAPSEL3 1 TP139 26MIL
TP_MEMSTRAPSEL2 1 TP948 26MIL
MEMSTRAPSEL1 1 TP142 26MIL
MEMSTRAPSEL0 1 TP143 26MIL

U8
THERM# GND
D- ALERT#
D+ SDA
VCC SCL
G781P8f
DDR_ALERT#
SMB_THRM_DATA
SMB_THRM_CLK
DDR_ALERT# 8,44
+3VRUN
R289 2.2K_J 0402
C486 0.1U_16V_M_B 0402
OVT_GFX#
R293 NC_0_J 0402
NV_GPIO8
R2347 NC_0_J 0402
R1778 NC_10K_J 0402

11/16 change part from F75383M(VERISION:0.28P) (15-F75383M-1000) to G781P8f (15-G781P80-0000)

To GPU

Backup GPIO8 for GPU thermal trigger signal
Change R293 from mount to NC for using internal thermal sensor

From EC

+3VRUN
R2128 NV_I2CS_SCL NV_2.2K_J 0402
R2129 NV_I2CS_SDA NV_2.2K_J 0402
R1056 NV_I2CC_SCL NV_2.2K_J 0402
R1057 NV_I2CC_SDA NV_2.2K_J 0402
R1385 NV_I2CB_SCL NV_2.2K_J 0402
R1386 NV_I2CB_SDA NV_2.2K_J 0402
R1225 NV_I2CA_SCL NV_2.2K_J 0402
R1228 NV_I2CA_SDA NV_2.2K_J 0402

26MIL TP605 ROM_CS#
26MIL TP570 ROM_SO
26MIL TP1062 TP_ROM_SI
26MIL TP687 ROM_SCLK
26MIL TP697 IFPAB_VPROBE
26MIL TP698 IFPCD_VPROBE
26MIL TP606 PEX_TSTCLK_OUT
26MIL TP607 PEX_TSTCLK_OUT#
26MIL TP1063
26MIL TP1064
R303 NV_10K_J 0402 TESTMODE

+3VRUN
R1776 NV_JTAG_TDI NV_10K_J 0402
R1777 NV_JTAG_TMS NV_10K_J 0402
R1462 NV_JTAG_TRST# NV_10K_J 0402
R1461 NV_JTAG_TCK NV_10K_J 0402
26MIL TP150 NV_JTAG_TDO

NV_JTAG_TCK
NV_JTAG_TMS
NV_JTAG_TDI
NV_JTAG_TDO
NV_JTAG_TRST#

GPIO0 K3 NV_GPIO0 R2130 NV_0_J 0402 NV_HDMI_DET_3 33,36
GPIO1 H1 NV_GPIO1 R301 NV_100K_J 0402
GPIO2 K5 NV_BRADJ NV_BRADJ 35
GPIO3 G5 NV_LCDVCC_EN# NV_LCDVCC_EN# 35
GPIO4 E2 NV_INV_EN NV_INV_EN 35
GPIO5 J5 VGA_GPIO51 VGA_GPIO5 74
GPIO6 G6 NV_GPIO6 R2359 0402 NC_0_J TP950 26MIL
GPIO7 K6 NV_GPIO7 TP713 26MIL
GPIO8 E1 NV_GPIO8 R2348 NC_0_J 0402 ECRST# 4,44
GPIO9 D2 OVT_GFX# OVT_GFX# 44
GPIO10 H5 NV_PWR_MIZER NV_PWR_MIZER 27
GPIO11 F4 NV_RSET_CTL R1820 NC_0_J 0402 HDMI_CEC 36
GPIO12 E3 NV_GPIO12 TP951 26MIL
GPIO13 U3 NV_GPIO13 TP952 26MIL
GPIO14 U4 NV_GPIO14 TP953 26MIL

NVIDIA FAE suggestion:
Change GPU thermal alert signal input from GPIO8 to GPIO9.
Delete TP522 and pull-up GPIO8 (R2332 2.2K to +3VRUN)

XTALSSIN T1 R1058 1 0_J 2 0402 R_SRCC1_27M_SS 3
XTALOUTBUFF T2
XTALIN U1 R1059 1 0_J 2 0402 R_SRCT1_27M_NON 3
U2 XTALOUT
Y2 NC_27MHZ_20P_20PPM ITTI_L5020-27.000-20
NV_XTALOUT
C494 NC_27P_50V_J_N 0402
C495 NC_27P_50V_J_N 0402

2007/1/4 Update

GPIO	I/O	Internal pull low	GPIO TABLE	
GPIO0	I	Yes	HDMI Hot Plug Detect 0(HPD0)	Active High
GPIO1	I	Yes	DVI Hot Plug Detect 1(HPD1)	Active High
GPIO2	O	Yes	LCD BL Brightness(LCD0_BL_PWM)	Active High
GPIO3	O	No	Panel Power(LCD0_VDD)	Active Low
GPIO4	O	Yes	LCD Backlight enable(LCD0_BL_EN)	Active High
GPIO5	O	Yes	GPU Power Downgrade for NV_VDD	Active Low
GPIO8	O	No	Thermal Alert Output (>125 Degree)	Active Low
GPIO9	I	No	System Power Limit Alert Input	Active Low
GPIO10	O	No	Memory Vref switch(MEM_VREF)	Active High
GPIO11	I/O	No	HDMI CEC Function Backup	

NV_BRADJ 0402 NV_10K_J R2315
NV_INV_EN 0402 NV_10K_J R2316
+3VRUN
NV_GPIO8 0402 NV_2.2K_J R2332
OVT_GFX# 0402 NV_2.2K_J R2333

Change R2333 from NC to mount for using internal thermal sensor

02/12/07 PVT Change

9/18 FAE suggest If use internal spread function,
U10 and related components can be NC.
10/19 Change R319,R320 from NC_ to NV_ for use internal spread spectrum.

+3VRUN
R1542 NC_10K_J 0402
SS_S0
R1543 NC_10K_J 0402
R319 NC_10K_J 0402
C492 NC_1U_10V_Y_Y 0603
C493 NC_1000P_50V_M_B 0402
XTALOUTBUFF
XTALSSIN
R316 NC_22_J 0402
R317 NC_22_J 0402
R320 NC_10K_J 0402
R321 NC_10K_J 0402
U10
X1/ICLK X2
GND VDD
S0 PD#
SSCLK REFCLK
NC_MK1726-08
XTALOUTBUFF_R
SS_S0
VGA27MSSOUT
REFCLK1
TP156 26MIL

Tis chip can use MK1726 or P1819B

R316 place near GPU
R317 place near spectrum chip

SPREAD SPECTRUM SETTING FOR MK

S0	SPREAD DIRECTION	Spread Percentage(%)
0	DOWN	-1.8
M	DOWN	-0.6
1	DOWN	-2.5

SPREAD SPECTRUM SETTING FOR P1819B

SRS PIN3	SPREAD DIRECTION	Spread Percentage(%)
0	DOWN	-1.25
1	DOWN	-1.75

0 = connect to GND
M= unconnected
1 = connect directly to VDD

nVidia support Down -1.25%

+3VRUN
R1105 NV_10K_J 0402
C1139 NV_0.1U_16V_M_B 0402
HDCP_SCL
HDCP_SDA
U82
SCL VCC
NC1 NC3
NC2 NC4
SDA GND
EEPROM_SOIC-8P_8KB
190-00001-0001-003
R1134 NV_10K_J 0402

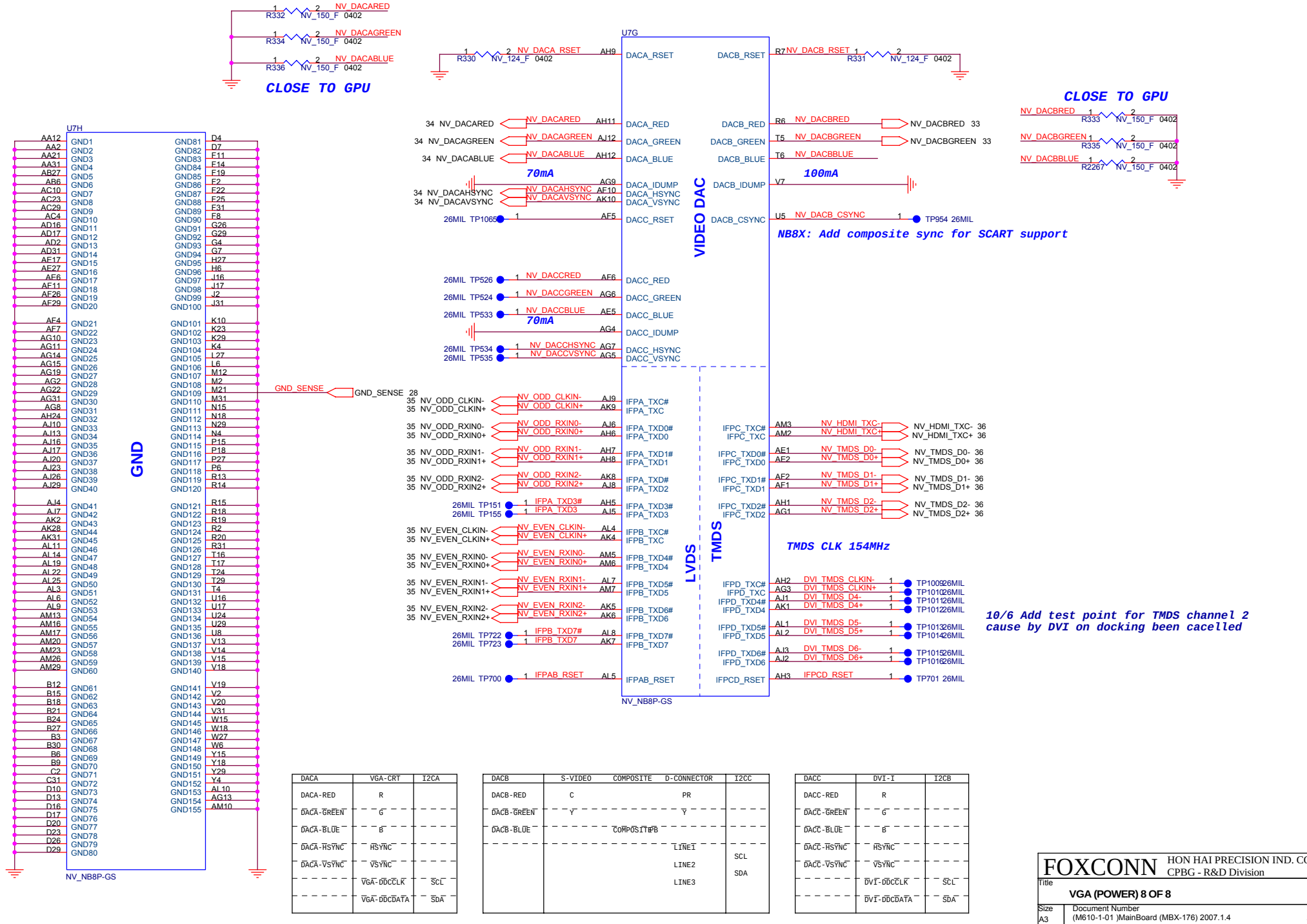
HDCP ROM

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: VGA (POWER) 7 OF 8

Size	Document Number	Rev
A3	(M610-1-01)MainBoard (MBX-176) 2007.1.4	2.0

Date: Friday, August 31, 2007 Sheet 20 of 81



DACA	VGA-CRT	I2CA
DACA-RED	R	
DACA-GREEN	G	
DACA-BLUE	B	
DACA-HSYNC	HSYNC	
DACA-VSYNC	VSYNC	
	VGA-DDCCLK	SCL
	VGA-DDCDATA	SDA

DACB	S-VIDEO	COMPOSITE	D-CONNECTOR	I2CC
DACB-RED	C		PR	
DACB-GREEN	Y		Y	
DACB-BLUE		COMPOSITE	PB	
			LINE1	SCL
			LINE2	SDA
			LINE3	

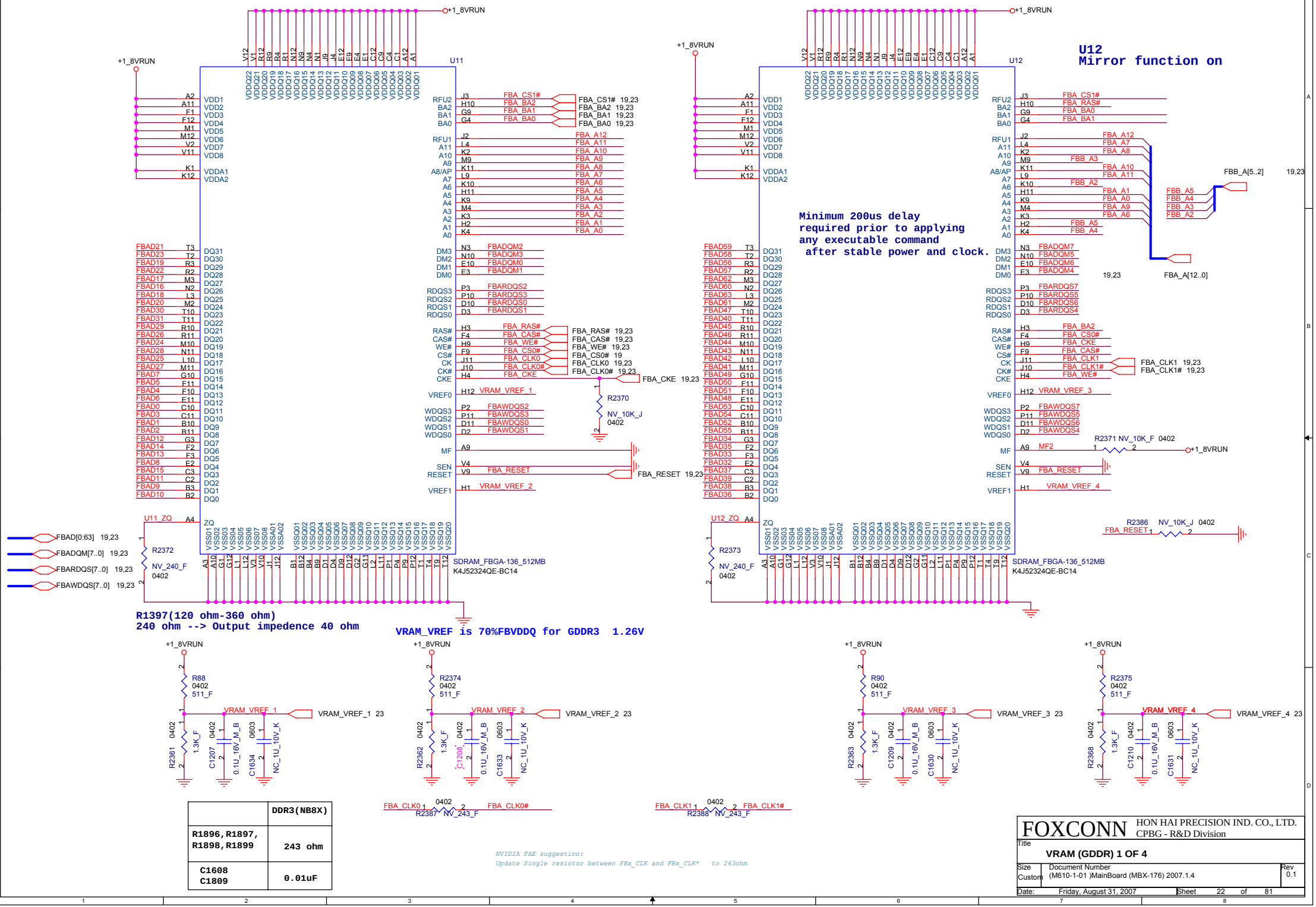
DACC	DVI-I	I2CB
DACC-RED	R	
DACC-GREEN	G	
DACC-BLUE	B	
DACC-HSYNC	HSYNC	
DACC-VSYNC	VSYNC	
	DVI-DDCCLK	SCL
	DVI-DDCDATA	SDA

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: VGA (POWER) 8 OF 8

Size: A3 | Document Number: (M610-1-01)MainBoard (MBX-176) 2007.1.4 | Rev: 2.0

Date: Friday, August 31, 2007 | Sheet 21 of 81



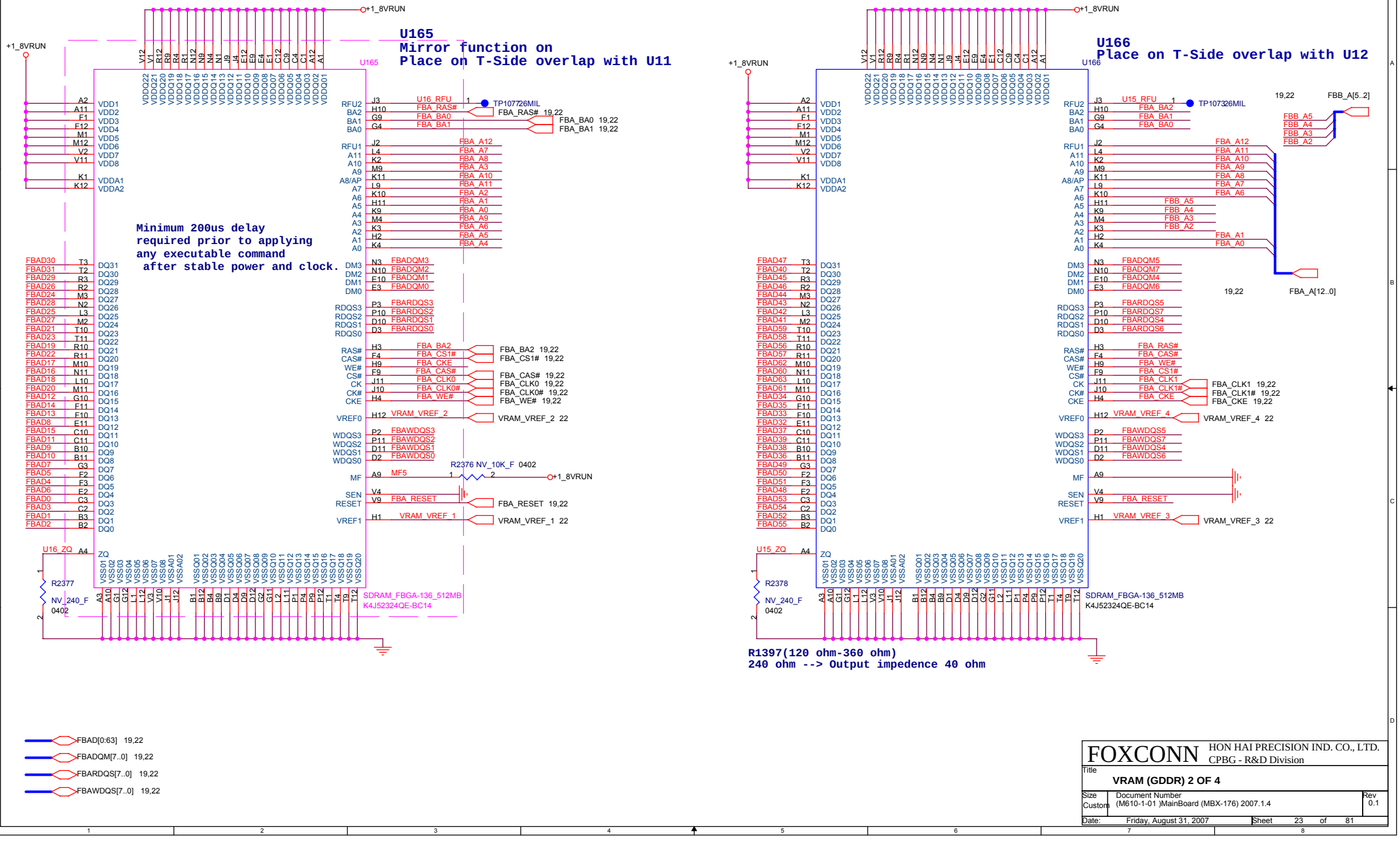
	DDR3(NB8X)
R1896,R1897, R1898,R1899	243 ohm
C1608 C1809	0.01uF

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: VRAM (GDDR) 1 OF 4

Size: Custom | Document Number: (M610-1-01)MainBoard (MBX-176) 2007.1.4 | Rev: 0.1

Date: Friday, August 31, 2007 | Sheet 22 of 81

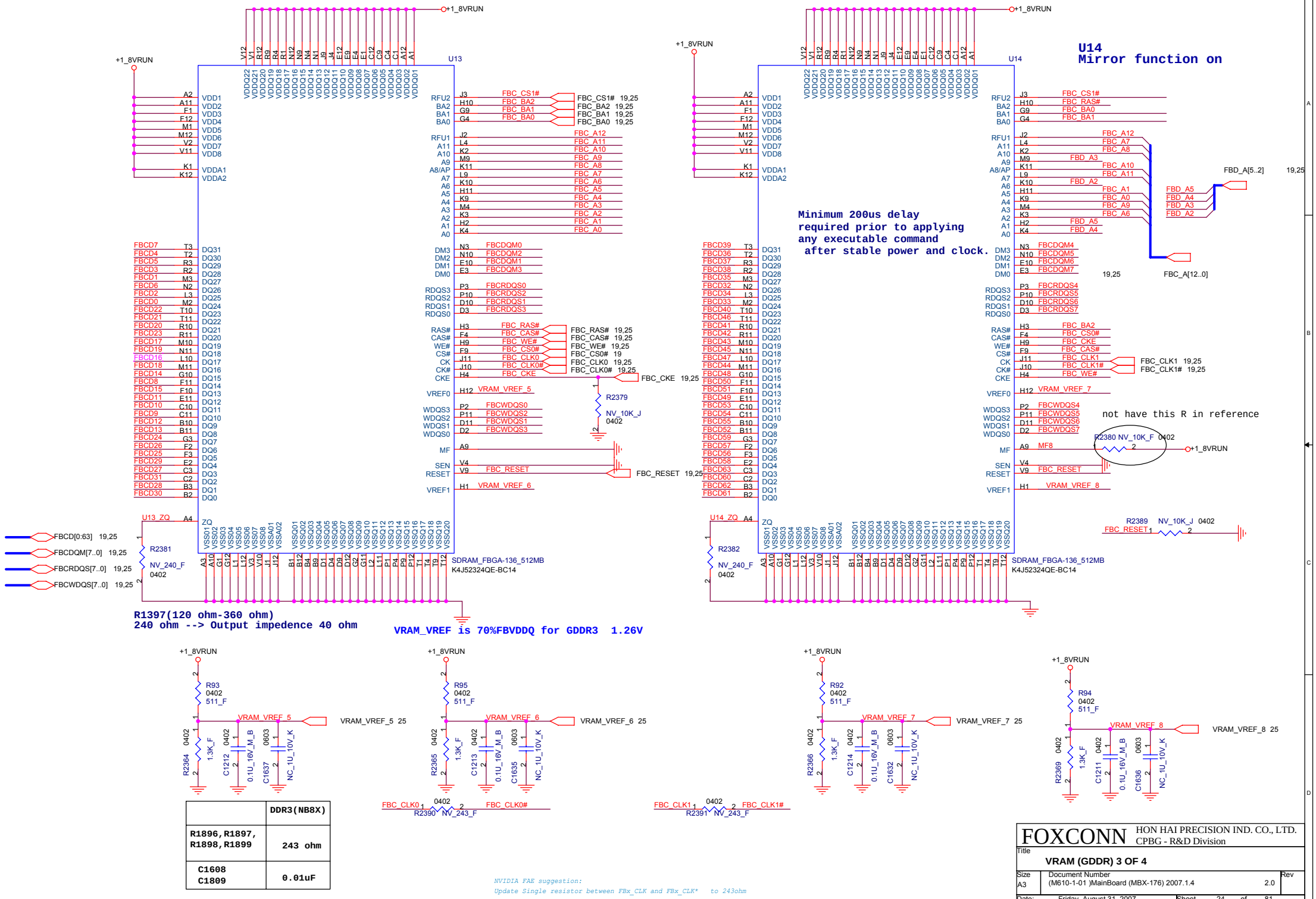


FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: VRAM (GDDR) 2 OF 4

Size: Custom | Document Number: (M610-1-01)MainBoard (MBX-176) 2007.1.4 | Rev: 0.1

Date: Friday, August 31, 2007 | Sheet 23 of 81



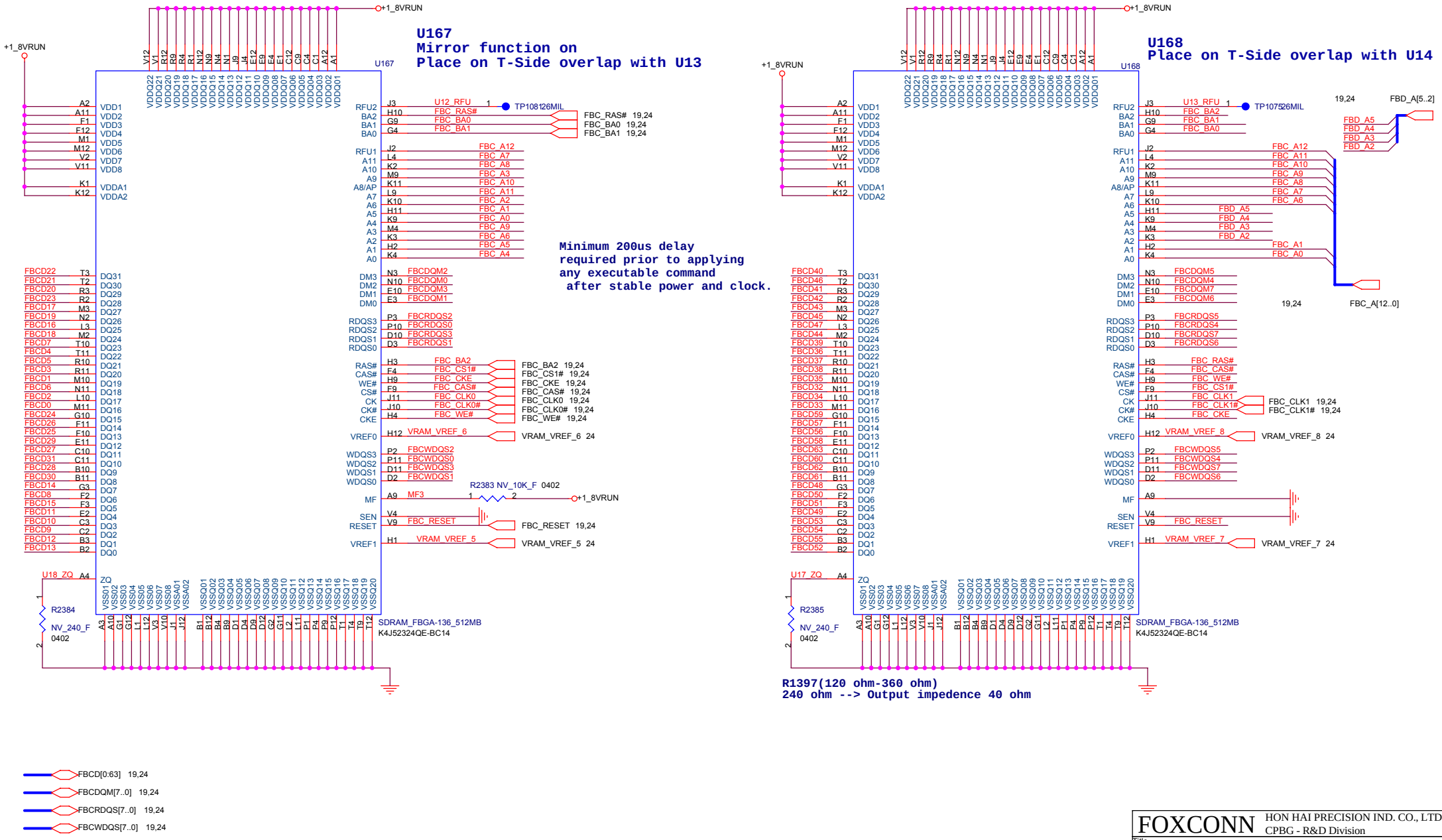
	DDR3(NB8X)
R1896,R1897, R1898,R1899	243 ohm
C1608 C1809	0.01uF

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: VRAM (GDDR) 3 OF 4

Size: A3 | Document Number: (M610-1-01)MainBoard (MBX-176) 2007.1.4 | Rev: 2.0

Date: Friday, August 31, 2007 | Sheet 24 of 81

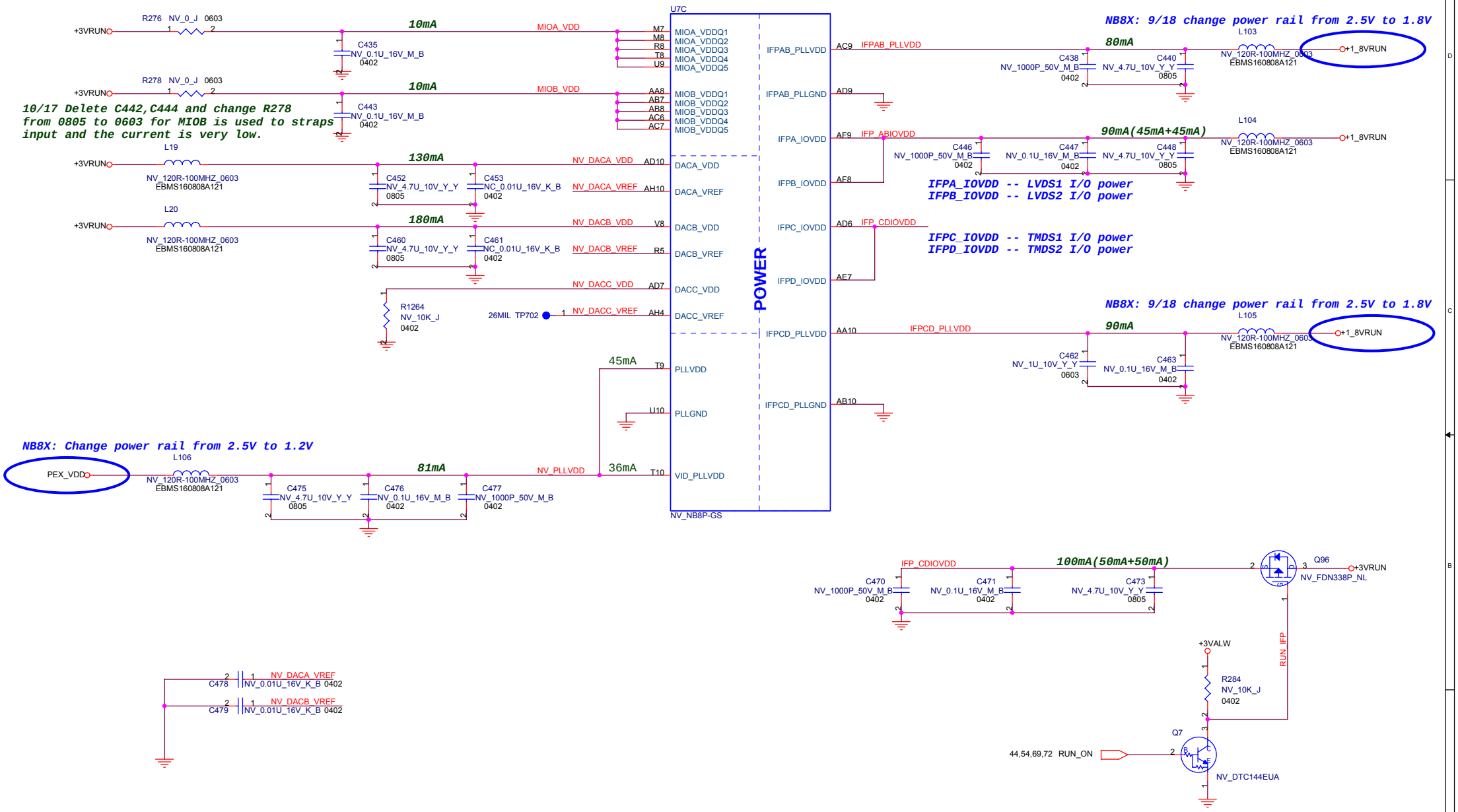


FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

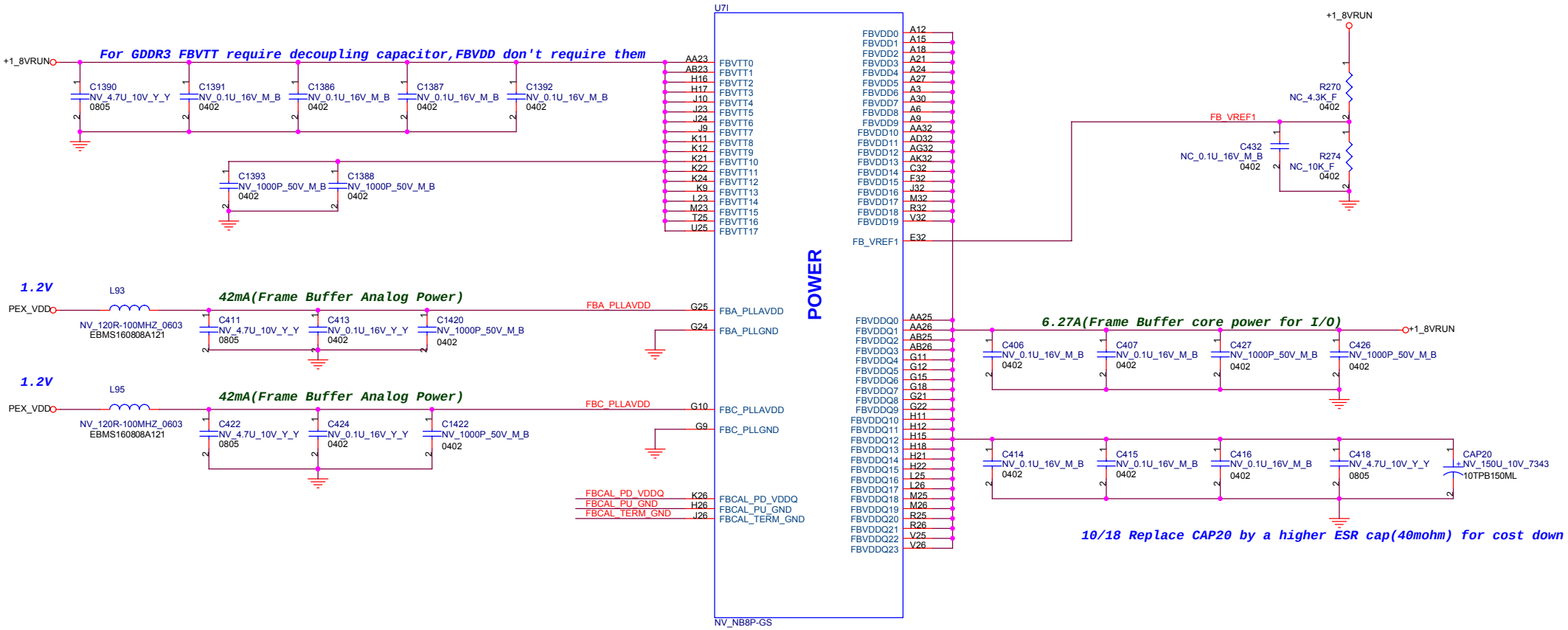
Title: VRAM (GDDR) 4 OF 4

Size	Document Number	Rev
Custom	(M610-1-01)MainBoard (MBX-176) 2007.1.4	2.0

Date: Friday, August 31, 2007 Sheet 25 of 81



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	VGA (POWER) 6 OF 8	
Size A3	Document Number (M610-1-01)MainBoard (MBX-176) 2007.1.4	Rev 2.0
Date: Friday, August 31, 2007	Sheet 26 of 81	



NVIDIA 07/1/5 update

	DDR3(NB8M-GT)	DDR3(NB8P-GS)
FBCAL_PD_VDDQ	45.3 ohm	45.3 ohm
FBCAL_PU_GND	24.9 ohm	24.9 ohm
FBCAL_TERM_GND	40.2 ohm	40.2 ohm

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: VGA (POWER) 5 OF 8

Size: A3 | Document Number: (M610-1-01)MainBoard (MBX-176) 2007.1.4 | Rev: 2.0

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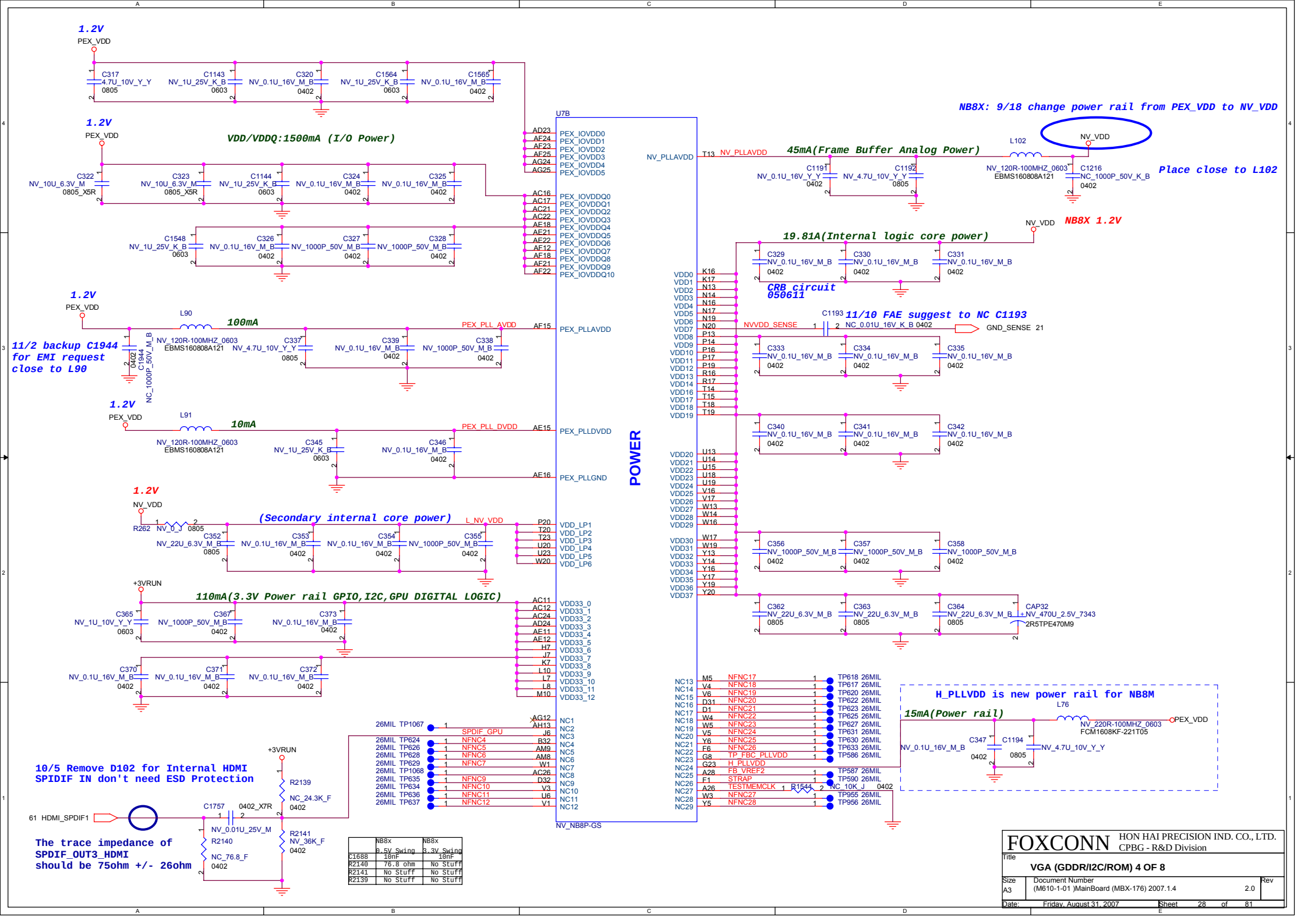
1.2V
PEX_VDD
C317 4.7U_10V_Y_Y 0805
C1143 NV_1U_25V_K_B 0603
C320 NV_0.1U_16V_M_B 0402
C1564 NV_1U_25V_K_B 0603
C1565 NV_0.1U_16V_M_B 0402
VDD/VDDQ:1500mA (I/O Power)
C322 NV_10U_6.3V_M 0805_X5R
C323 NV_10U_6.3V_M 0805_X5R
C1144 NV_1U_25V_K_B 0603
C324 NV_0.1U_16V_M_B 0402
C325 NV_0.1U_16V_M_B 0402
C1548 NV_1U_25V_K_B 0603
C326 NV_0.1U_16V_M_B 0402
C327 NV_1000P_50V_M_B 0402
C328 NV_1000P_50V_M_B 0402
U7B
PEX_IOVDD0
PEX_IOVDD1
PEX_IOVDD2
PEX_IOVDD3
PEX_IOVDD4
PEX_IOVDD5
PEX_IOVDDQ0
PEX_IOVDDQ1
PEX_IOVDDQ2
PEX_IOVDDQ3
PEX_IOVDDQ4
PEX_IOVDDQ5
PEX_IOVDDQ6
PEX_IOVDDQ7
PEX_IOVDDQ8
PEX_IOVDDQ9
PEX_IOVDDQ10
NV_PLLAVDD
PEX_PLLAVDD
PEX_PLLDVDD
PEX_PLLGND
VDD_LP1
VDD_LP2
VDD_LP3
VDD_LP4
VDD_LP5
VDD_LP6
VDD33_0
VDD33_1
VDD33_2
VDD33_3
VDD33_4
VDD33_5
VDD33_6
VDD33_7
VDD33_8
VDD33_9
VDD33_10
VDD33_11
VDD33_12
NC1
NC2
NC3
NC4
NC5
NC6
NC7
NC8
NC9
NC10
NC11
NC12
NV_NB8P-GS
POWER
1.2V
PEX_VDD
L90
100mA
PEX_PLL_AVDD
11/2 backup C1944 for EMI request close to L90
C1944 NC_1000P_50V_M_B 0402
NV_120R-100MHZ_0603 EBMS160808A121
C337 NV_4.7U_10V_Y_Y 0805
C339 NV_0.1U_16V_M_B 0402
C338 NV_1000P_50V_M_B 0402
1.2V
PEX_VDD
L91
10mA
PEX_PLL_DVDD
NV_120R-100MHZ_0603 EBMS160808A121
C345 NV_1U_25V_K_B 0603
C346 NV_0.1U_16V_M_B 0402
1.2V
NV_VDD
R262 NV_0_J 0805
(Secondary internal core power)
L_NV_VDD
C352 NV_22U_6.3V_M_B 0805
C353 NV_0.1U_16V_M_B 0402
C354 NV_0.1U_16V_M_B 0402
C355 NV_1000P_50V_M_B 0402
+3VRUN
110mA(3.3V Power rail GPIO,I2C,GPU DIGITAL LOGIC)
C365 NV_1U_10V_Y_Y 0603
C367 NV_1000P_50V_M_B 0402
C373 NV_0.1U_16V_M_B 0402
C370 NV_0.1U_16V_M_B 0402
C371 NV_0.1U_16V_M_B 0402
C372 NV_0.1U_16V_M_B 0402
26MIL TP1067
SPDIF_GPU
26MIL TP624
NFNC4
26MIL TP626
NFNC5
26MIL TP628
NFNC6
26MIL TP629
NFNC7
26MIL TP1068
26MIL TP635
NFNC9
26MIL TP634
NFNC10
26MIL TP636
NFNC11
26MIL TP637
NFNC12
10/5 Remove D102 for Internal HDMI SPIDIF IN don't need ESD Protection
+3VRUN
R2139 NC_24.3K_F 0402
61 HDMI_SPDIF1
C1757 0402_X7R
R2140 NV_0.01U_25V_M
R2141 NV_36K_F 0402
NC_76.8_F 0402
The trace impedance of SPDIF_OUT3_HDMI should be 75ohm +/- 26ohm
NB8x 0.5V Swing
NB8x 3.3V Swing
C1688 10nF 10nF
R2140 76.8 ohm No Stuff
R2141 No Stuff No Stuff
R2139 No Stuff No Stuff
NB8X: 9/18 change power rail from PEX_VDD to NV_VDD
NV_VDD
L102
NV_120R-100MHZ_0603 EBMS160808A121
C1216 NC_1000P_50V_K_B 0402
Place close to L102
45mA(Frame Buffer Analog Power)
C1191 NV_0.1U_16V_Y_Y 0402
C1192 NV_4.7U_10V_Y_Y 0805
NB8X 1.2V
19.81A(Internal logic core power)
C329 NV_0.1U_16V_M_B 0402
C330 NV_0.1U_16V_M_B 0402
C331 NV_0.1U_16V_M_B 0402
CRB circuit 050611
C1193 11/10 FAE suggest to NC C1193
NVVDD_SENSE
NC_0.01U_16V_K_B 0402
GND_SENSE 21
C333 NV_0.1U_16V_M_B 0402
C334 NV_0.1U_16V_M_B 0402
C335 NV_0.1U_16V_M_B 0402
C340 NV_0.1U_16V_M_B 0402
C341 NV_0.1U_16V_M_B 0402
C342 NV_0.1U_16V_M_B 0402
C356 NV_1000P_50V_M_B 0402
C357 NV_1000P_50V_M_B 0402
C358 NV_1000P_50V_M_B 0402
C362 NV_22U_6.3V_M_B 0805
C363 NV_22U_6.3V_M_B 0805
C364 NV_22U_6.3V_M_B 0805
CAP32 NV_470U_2.5V_7343 2R5TPE470M9
H_PLLVDD is new power rail for NB8M
15mA(Power rail)
L76
NV_220R-100MHZ_0603 FCM1608KF-221T05
C347 NV_0.1U_16V_M_B 0402
C1194 NV_4.7U_10V_Y_Y 0805
NFNC17
NFNC18
NFNC19
NFNC20
NFNC21
NFNC22
NFNC23
NFNC24
NFNC25
NFNC26
TP_FBC_PLLVDD
H_PLLVDD
FB_VREF2
STRAP
TESTMEMCLK
R1544 NC_10K_J 0402
NFNC27
NFNC28
TP618 26MIL
TP617 26MIL
TP620 26MIL
TP622 26MIL
TP623 26MIL
TP625 26MIL
TP627 26MIL
TP631 26MIL
TP630 26MIL
TP633 26MIL
TP586 26MIL
TP587 26MIL
TP590 26MIL
TP955 26MIL
TP956 26MIL
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
Title
VGA (GDDR/I2C/ROM) 4 OF 8
Size A3
Document Number (M610-1-01)MainBoard (MBX-176) 2007.1.4
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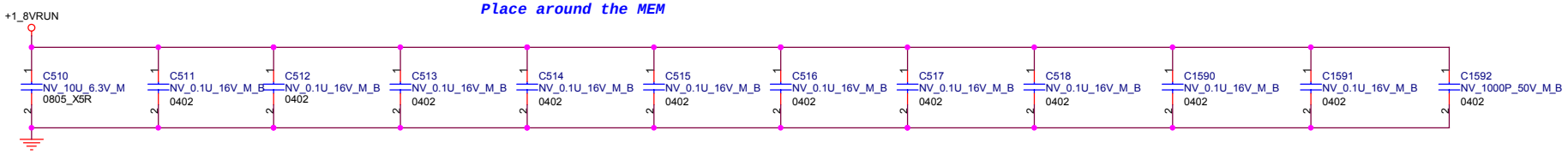
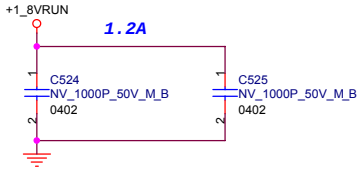
Decoupling for T-U11 MEMORY

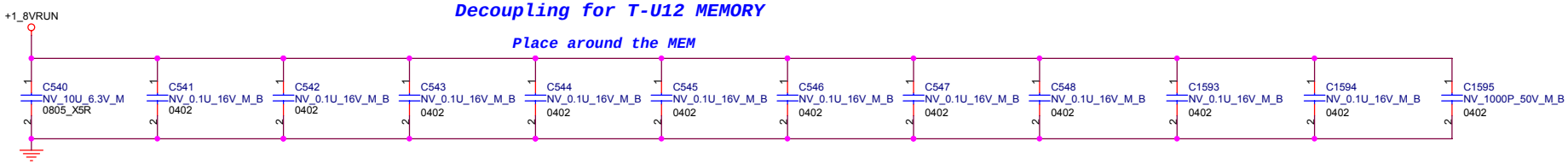
Place around the MEM

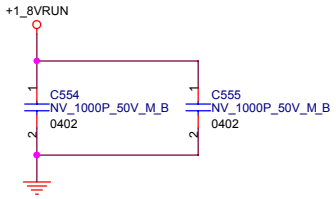




Decoupling for T-U12 MEMORY

Place around the MEM





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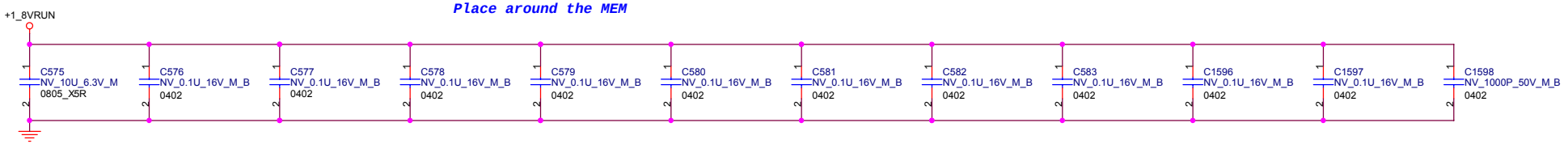
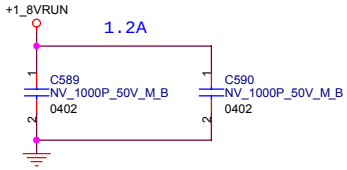
Decoupling for T-U13 MEMORY

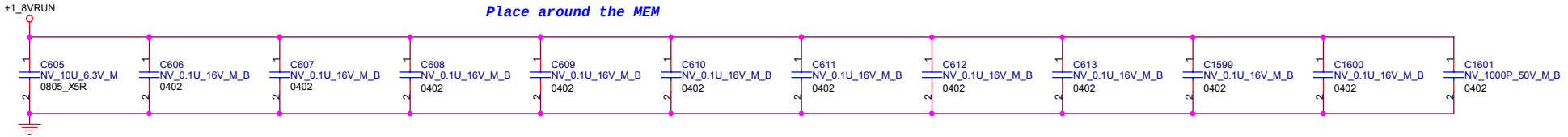
Place around the MEM

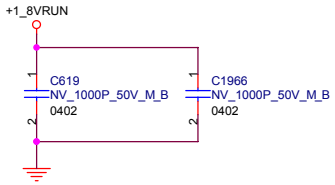




Decoupling for T-U14 MEMORY

Place around the MEM





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Title: **VRAM (POWERBYPASS) 4 OF 4**

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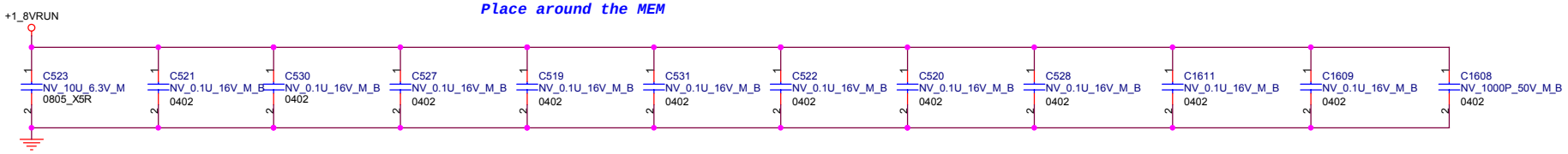
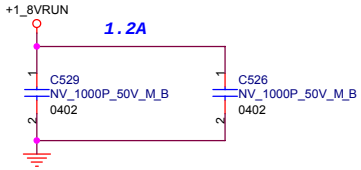
Decoupling for B-U165 MEMORY

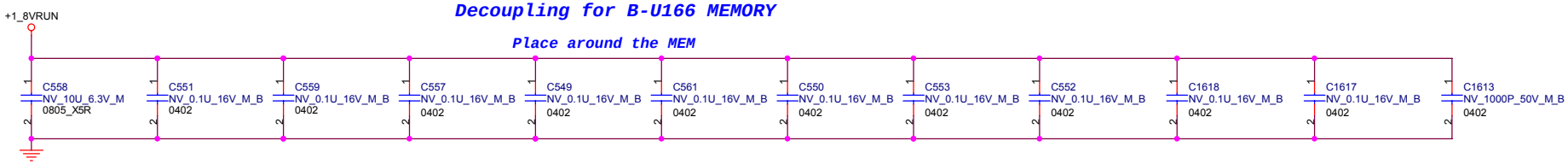
Place around the MEM

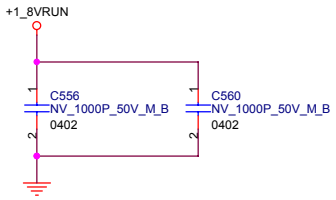




Decoupling for B-U166 MEMORY

Place around the MEM





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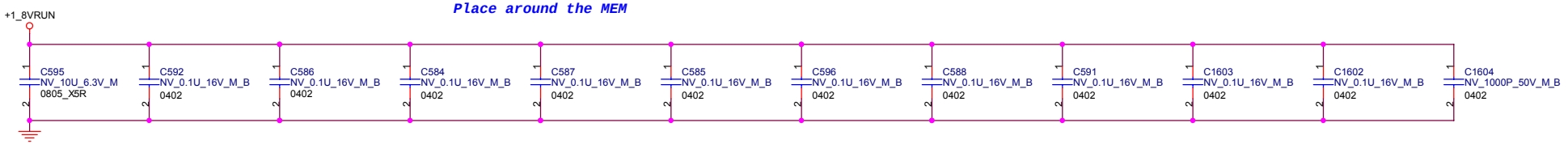
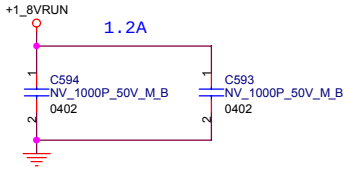
Decoupling for B-U167 MEMORY

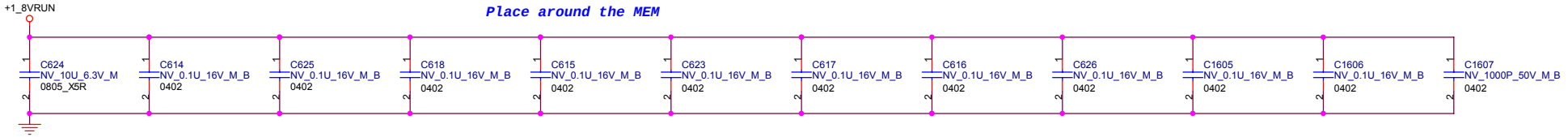
Place around the MEM

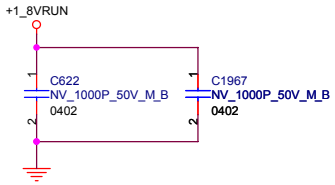




Decoupling for B-U168 MEMORY

Place around the MEM





FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
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Size A3	Document Number (M610-1-01)MainBoard (MBX-176) 2007.1.4	Rev 2.0
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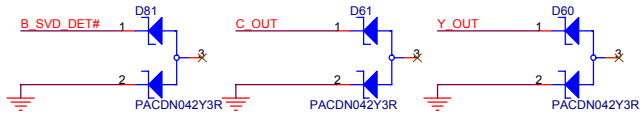
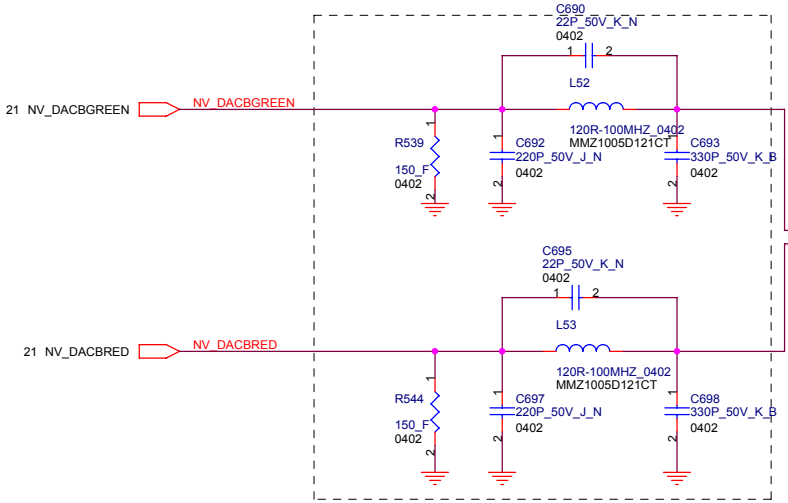
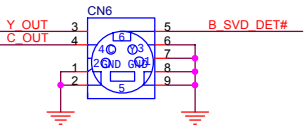
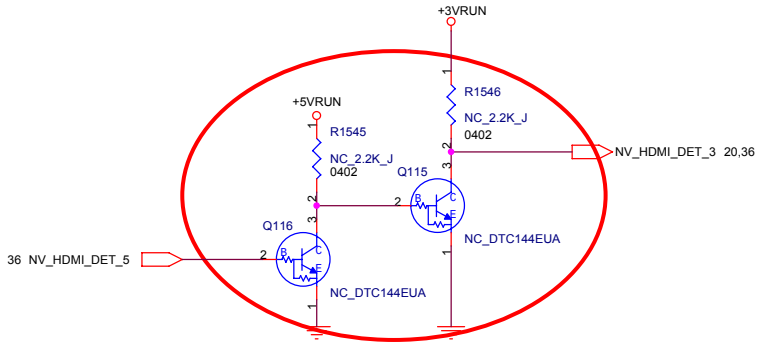


These compoent close to S-Video connector within 700 mil



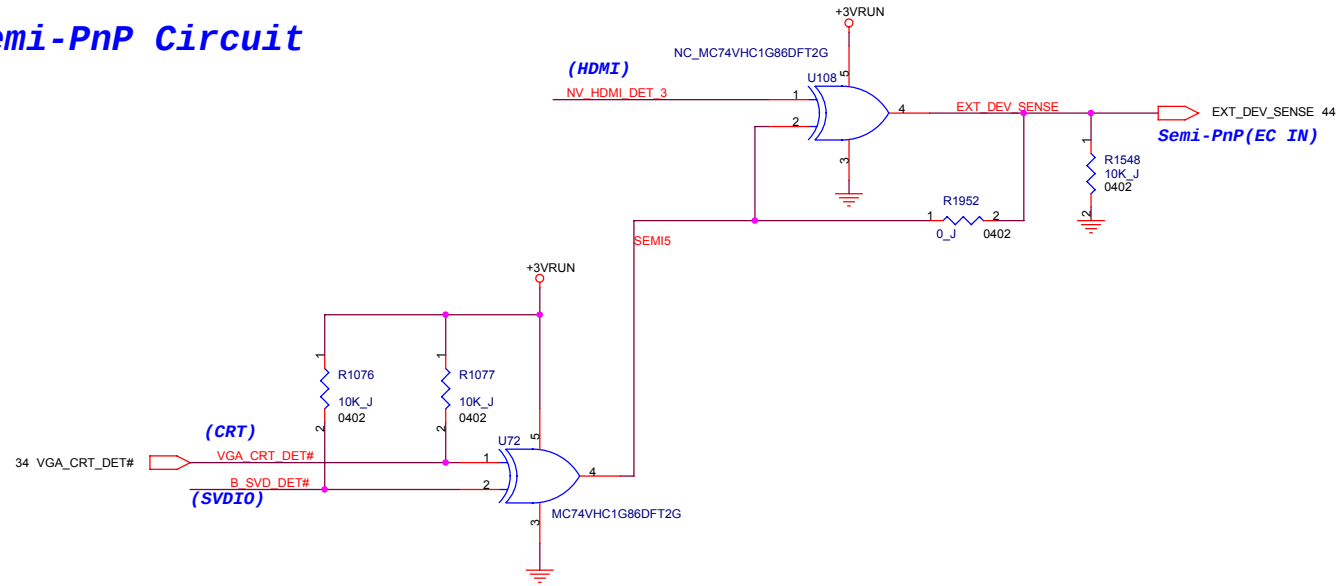
S-VIDEO CONNECTOR





PS101 HPD has level shift function, so backup this circuit
Change Q115,Q116,R1545,R1546 to NC

Semi-PnP Circuit



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	S-VIDEO/Semi-PnP	
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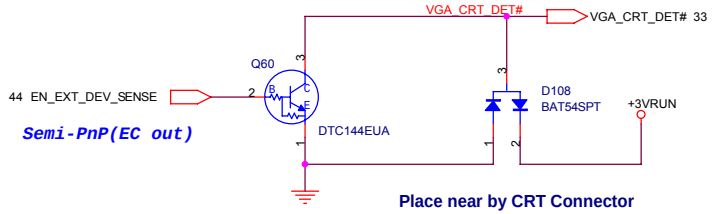
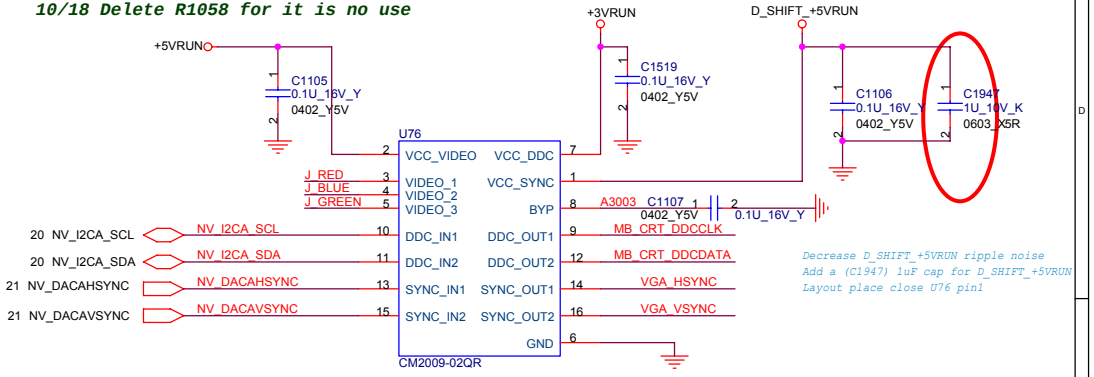
CRT CONNECTOR

10/18 Delete R1058 for it is no use



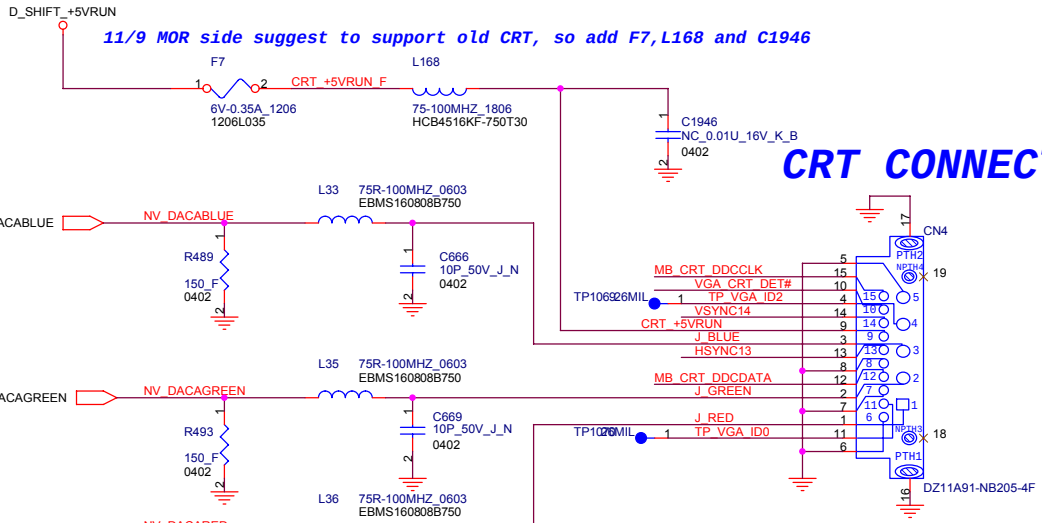
Semi-PnP(EC out)

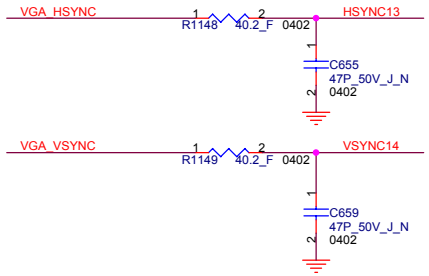
Place near by CRT Connector



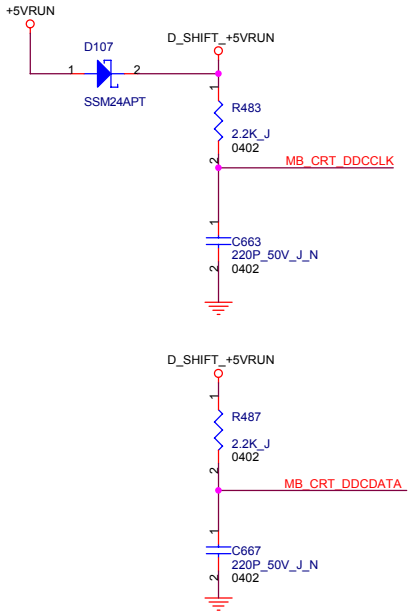
Decrease D_SHIFT_+5VRUN ripple noise
Add a (C1947) 1uF cap for D_SHIFT_+5VRUN
Layout place close U76 pin1

11/9 MOR side suggest to support old CRT, so add F7,L168 and C1946





11/8 Change R1148,R1149 from 0ohm to 40ohm for meet CM2009-02 termination Spec



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: CRT		
Size: A3	Document Number: (M610-1-01)MainBoard (MBX-176) 2007.1.4	Rev: 2.0
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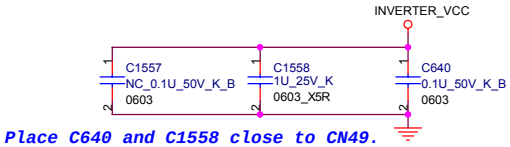
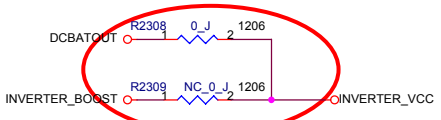
LVDS CONNECTOR

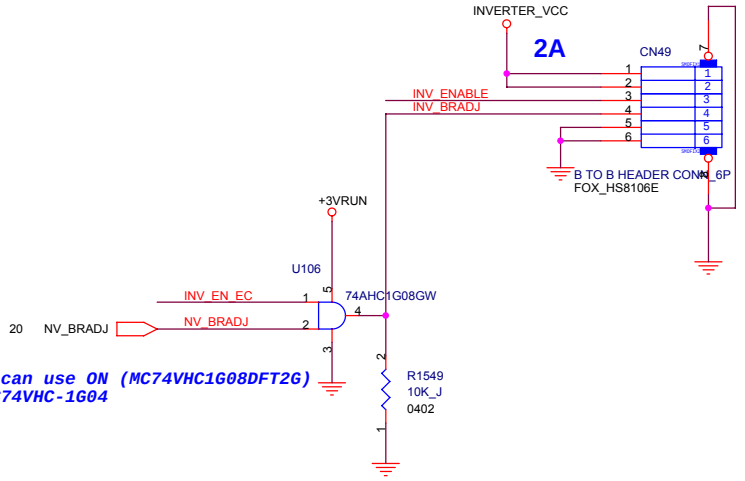


Place C640 and C1558 close to CN49.

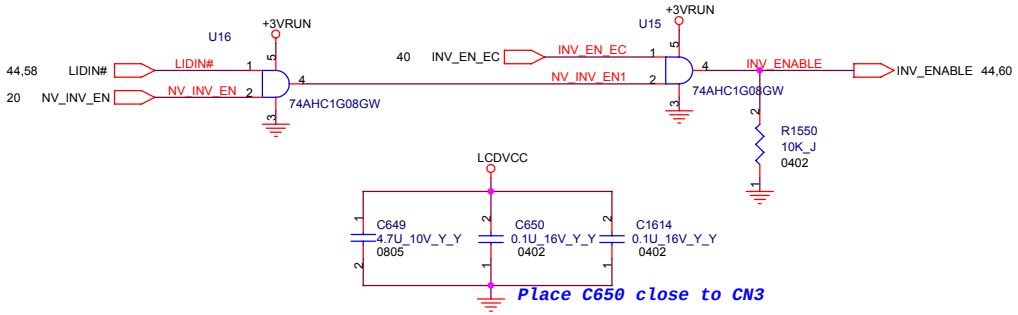


Backup Inverter boost circuit and use DCBATOUT as INVERTER_VCC
Change R2308 from NC to mount
Change R2309 from mount to NC

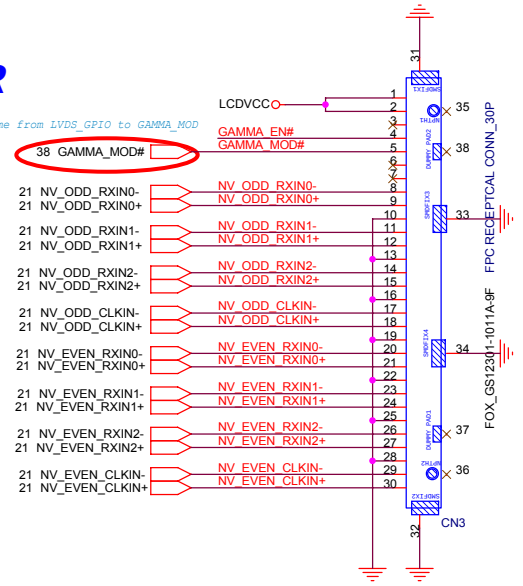
INVERTER CONNECTOR

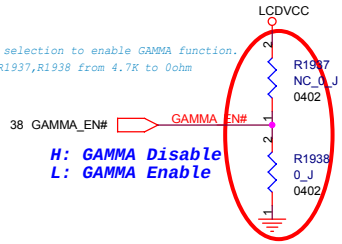


U106,U15,U16 can use ON (MC74VHC1G08DFT2G)
H.H. PN:14-MC74VHC-1G04

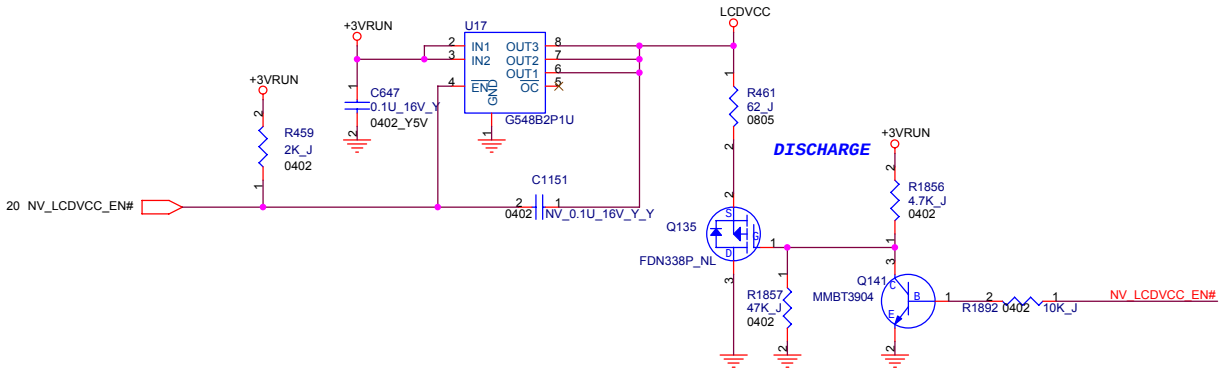


Place C650 close to CN3

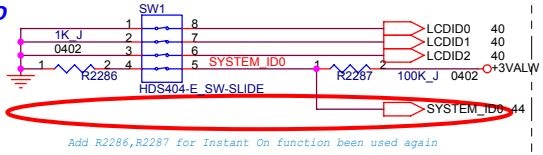




Current limit is from 1.1A to 2.1A.



PANEL ID



Type	WXGA+	WXGA+	WUXGA	WUXGA
Size	17" wide	17" wide	17" wide	17" wide
Vender	LG.PHILIPS	LG.PHILIPS	SHARP	SHARP
Device Name	LP171WP74-TLA1	LP171WP7-TLA1	LQ170M11LA4G	LQ170M11LA4B
Panel ID Check[2..0]	1 Lamps(New) 010	2 Lamps(New) 001	2 Lamps(New) 100	2 Lamps(Old) 101

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Title: LVDS

Size: A3 | Document Number: (M610-1-01)MainBoard (MBX-176) 2007.1.4 | Rev: 2.0

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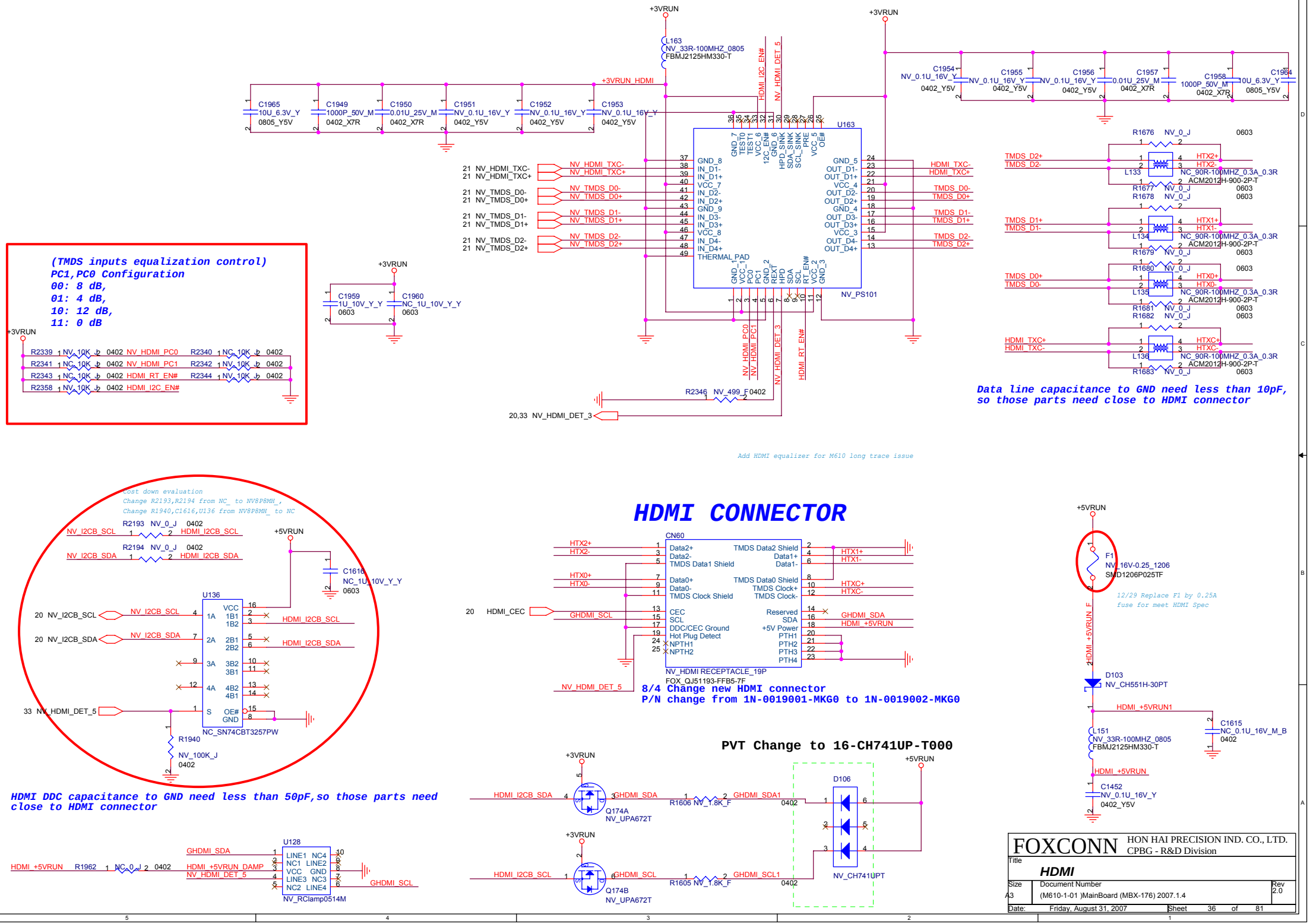
(TMDS inputs equalization control)
PC1,PC0 Configuration
00: 8 dB,
01: 4 dB,
10: 12 dB,
11: 0 dB
Data line capacitance to GND need less than 10pF, so those parts need close to HDMI connector
Add HDMI equalizer for M610 long trace issue
HDMI CONNECTOR
8/4 Change new HDMI connector
P/N change from 1N-0019001-MKG0 to 1N-0019002-MKG0
PVT Change to 16-CH741UP-T000
Cost down evaluation
Change R2193,R2194 from NC_ to NV8P8MH_,
Change R1940,C1616,U136 from NV8P8MH_ to NC
HDMI DDC capacitance to GND need less than 50pF,so those parts need close to HDMI connector
NV_PS101
NC_SN74CBT3257PW
NV_RClamp0514M
NV_CH741UPT
NV_HDMI RECEPTACLE_19P
FOX_QJ51193-FFB5-7F
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HON HAI PRECISION IND. CO., LTD.
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HDMI
(M610-1-01)MainBoard (MBX-176) 2007.1.4
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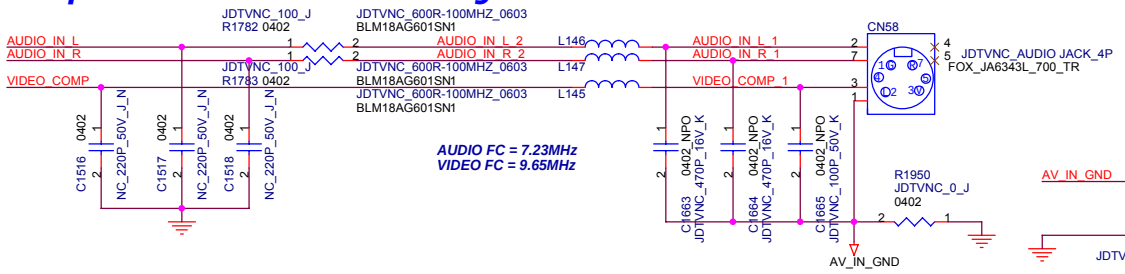
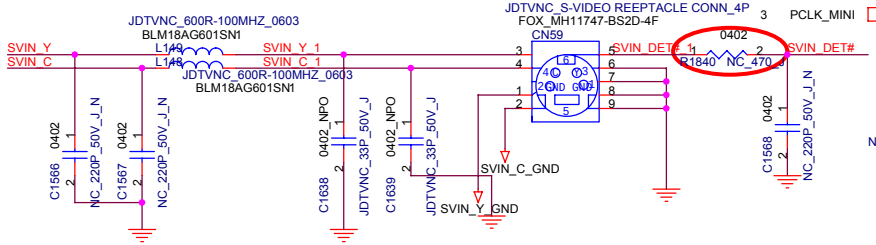
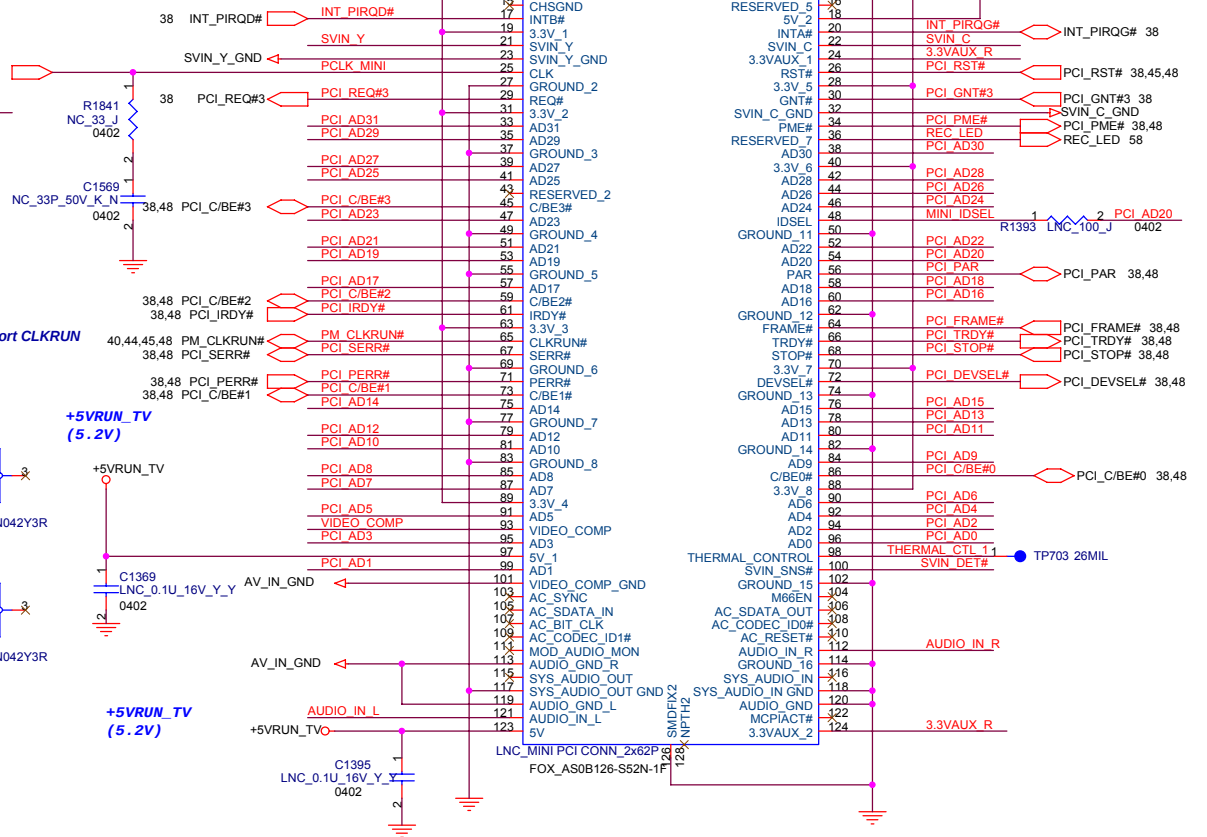
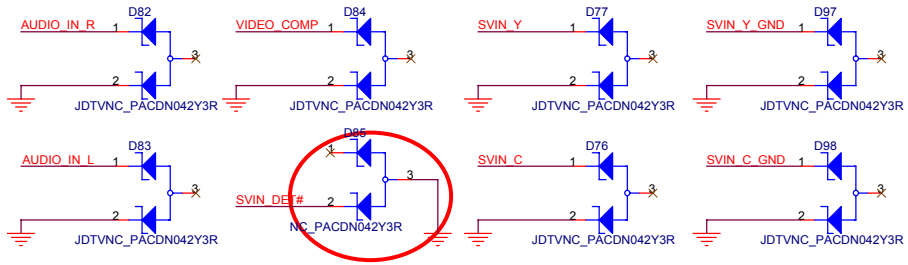
Special mini stereo jack



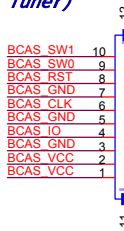
S-VIDEO IN



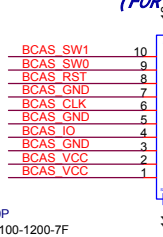




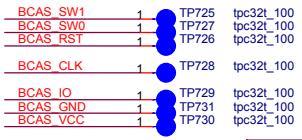
B-CAS connentor (Close to TV Tuner)

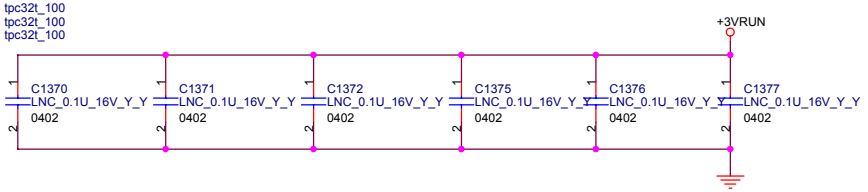


FFC CONNECT TO TV TUNER BOARD (FOR JP DIAGITAL)



BFT Test Pad





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Title: **MINI-PCI CONN.**

Size	Document Number	Rev
A3	(M610-1-01)MainBoard (MBX-176) 2007.1.4	2.0

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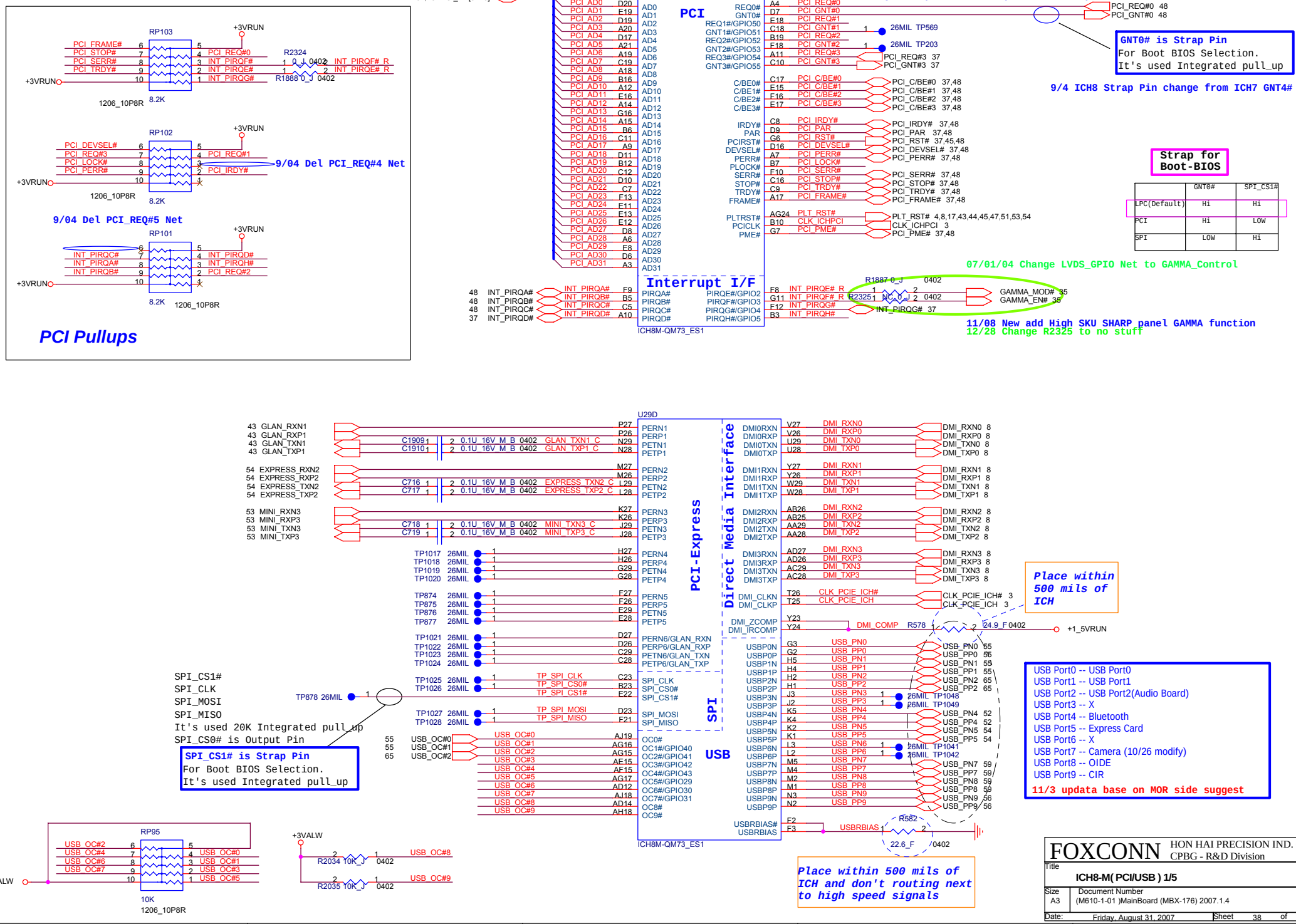
Difference ICH7&ICH8
1.Del REQ4/GNT4,REQ5/GNT5
2.Change Strap Pin station(GNT4#-->GNT0#)
GNT0# is Strap Pin
For Boot BIOS Selection.
It's used Integrated pull_up
9/4 ICH8 Strap Pin change from ICH7 GNT4#
Strap for Boot-BIOS
9/04 Del PCI_REQ#4 Net
9/04 Del PCI_REQ#5 Net
PCI Pullups
07/01/04 Change LVDS_GPIO Net to GAMMA_Control
11/08 New add High SKU SHARP panel GAMMA function
12/28 Change R2325 to no stuff
SPI_CS1#
SPI_CLK
SPI_MOSI
SPI_MISO
It's used 20K Integrated pull_up
SPI_CS0# is Output Pin
SPI_CS1# is Strap Pin
For Boot BIOS Selection.
It's used Integrated pull_up
Place within 500 mils of ICH
Place within 500 mils of ICH and don't routing next to high speed signals
USB Port0 -- USB Port0
USB Port1 -- USB Port1
USB Port2 -- USB Port2(Audio Board)
USB Port3 -- X
USB Port4 -- Bluetooth
USB Port5 -- Express Card
USB Port6 -- X
USB Port7 -- Camera (10/26 modify)
USB Port8 -- OIDE
USB Port9 -- CIR
11/3 updata base on MOR side suggest
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ICH8-M(PCI/USB) 1/5
Document Number (M610-1-01)MainBoard (MBX-176) 2007.1.4
Rev 2.0
Friday, August 31, 2007
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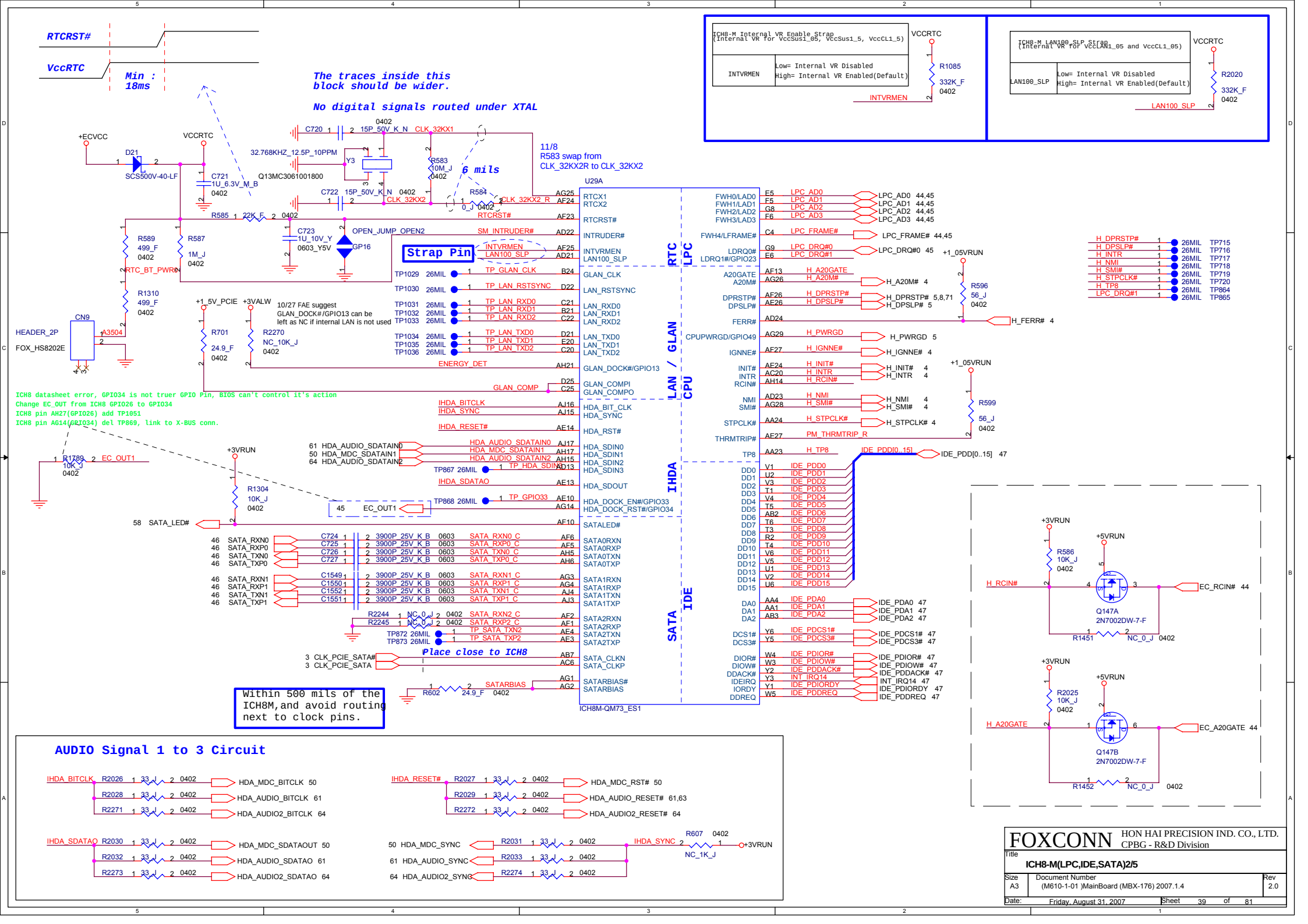
RTCRST#
VccRTC
Min : 18ms
The traces inside this block should be wider.
No digital signals routed under XTAL
11/8
R583 swap from CLK_32KX2R to CLK_32KX2
6 mils
Strap Pin
ICH8-M Internal VR Enable Strap (Internal VR for VccSus1_05, VccSus1_5, VccCL1_5)
INTVRMEN
Low= Internal VR Disabled
High= Internal VR Enabled(Default)
ICH8-M LAN100_SLP Strap (Internal VR for VccLAN1_05 and VccCL1_05)
LAN100_SLP
Low= Internal VR Disabled
High= Internal VR Enabled(Default)
ICH8 datasheet error, GPIO34 is not truer GPIO Pin, BIOS can't control it's action
Change EC_OUT from ICH8 GPIO26 to GPIO34
ICH8 pin AH27(GPIO26) add TP1051
ICH8 pin AG14(GPIO34) del TP869, link to X-BUS conn.
10/27 FAE suggest
GLAN_DOCK#/GPIO13 can be left as NC if internal LAN is not used
Place close to ICH8
Within 500 mils of the ICH8M,and avoid routing next to clock pins.
ICH8M-QM73_ES1
AUDIO Signal 1 to 3 Circuit
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ICH8-M(LPC,IDE,SATA)2/5
A3
(M610-1-01)MainBoard (MBX-176) 2007.1.4
2.0
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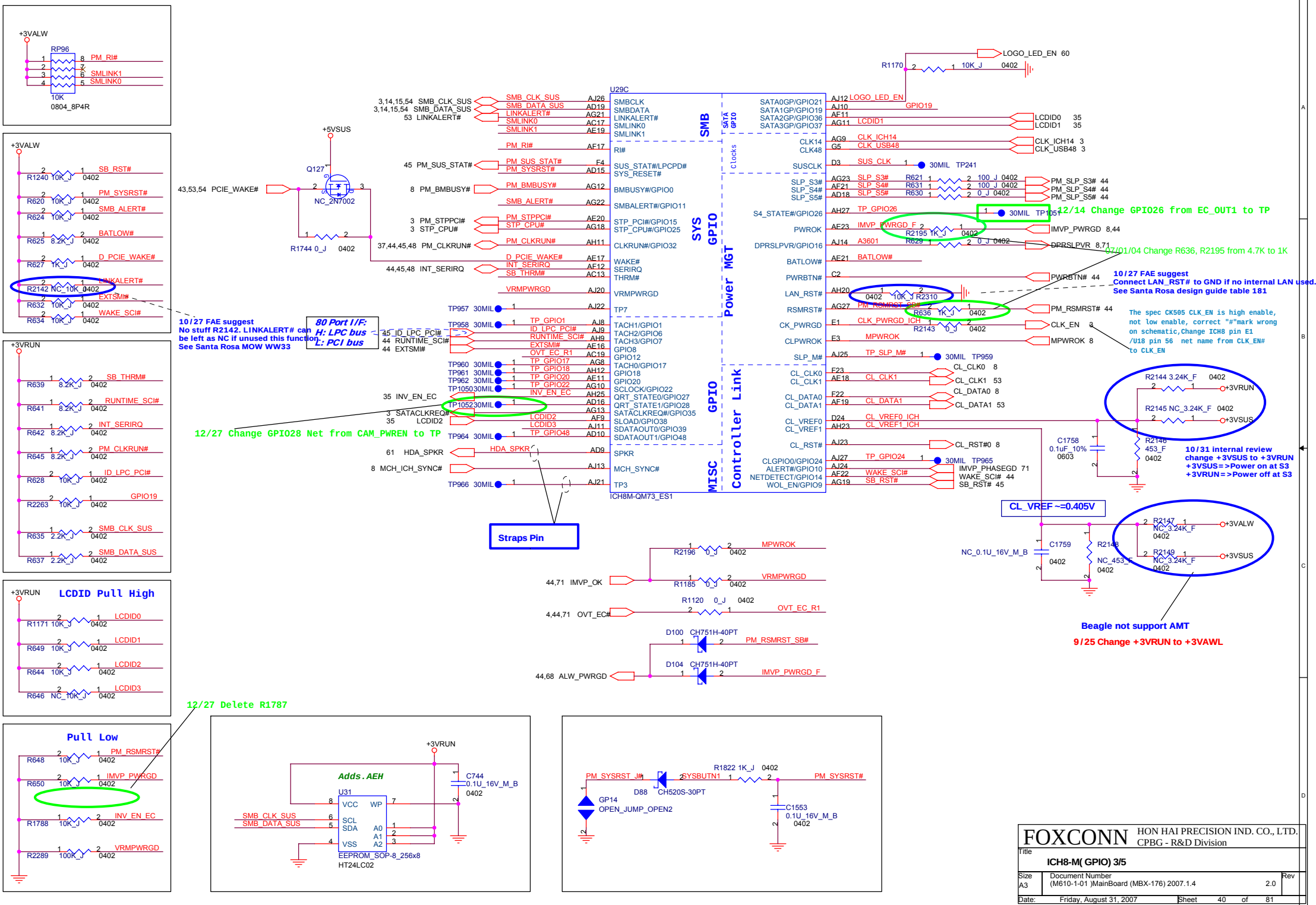
39
81



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Title: ICH8-M(GPIO) 3/5

Size: A3 | Document Number: (M610-1-01)MainBoard (MBX-176) 2007.1.4 | Rev: 2.0

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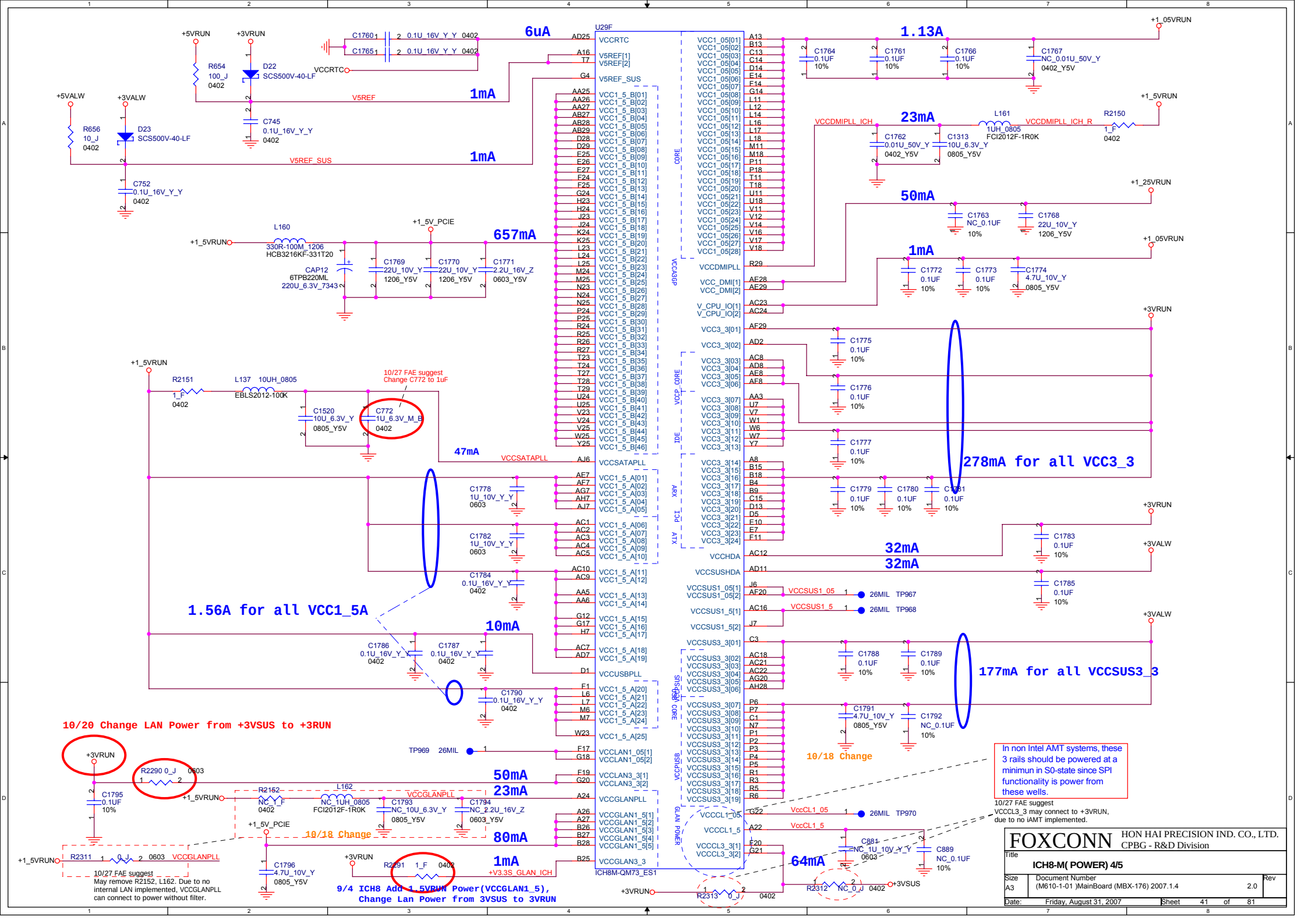
U29F
ICH8M-QM73_ES1
6uA
1mA
1mA
657mA
47mA
1.56A for all VCC1_5A
10mA
1.13A
23mA
50mA
1mA
278mA for all VCC3_3
32mA
32mA
177mA for all VCCSUS3_3
64mA
80mA
50mA
23mA
1mA
10/20 Change LAN Power from +3VSUS to +3RUN
10/18 Change
10/18 Change
9/4 ICH8 Add 1.5VRUN Power(VCCGLAN1_5), Change Lan Power from 3VSUS to 3VRUN
10/27 FAE suggest Change C772 to 1uF
10/27 FAE suggest
May remove R2152, L162. Due to no internal LAN implemented, VCCGLANPLL can connect to power without filter.
In non Intel AMT systems, these 3 rails should be powered at a minimun in S0-state since SPI functionality is power from these wells.
10/27 FAE suggest
VCCCL3_3 may connect to +3VRUN, due to no iAMT implemented.
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ICH8-M(POWER) 4/5
Document Number (M610-1-01)MainBoard (MBX-176) 2.0
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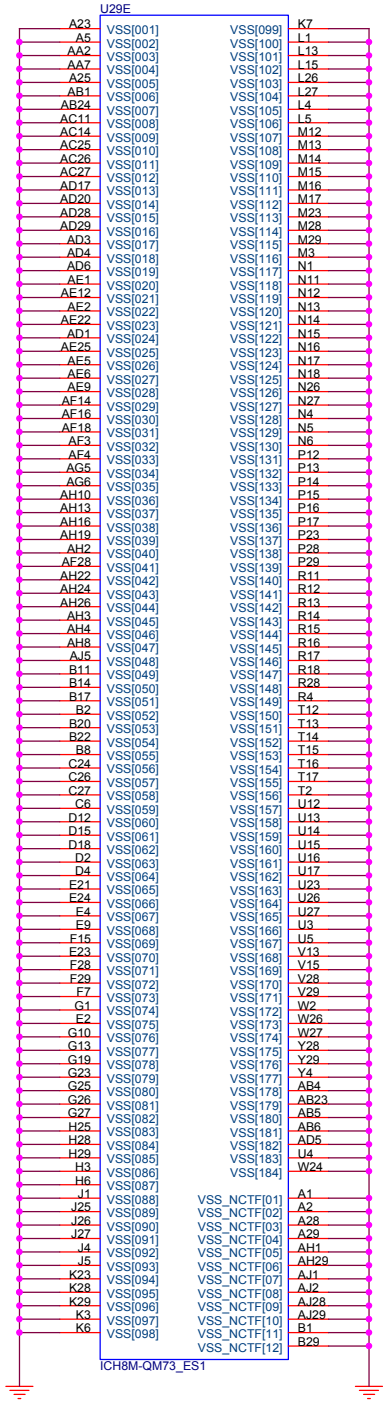

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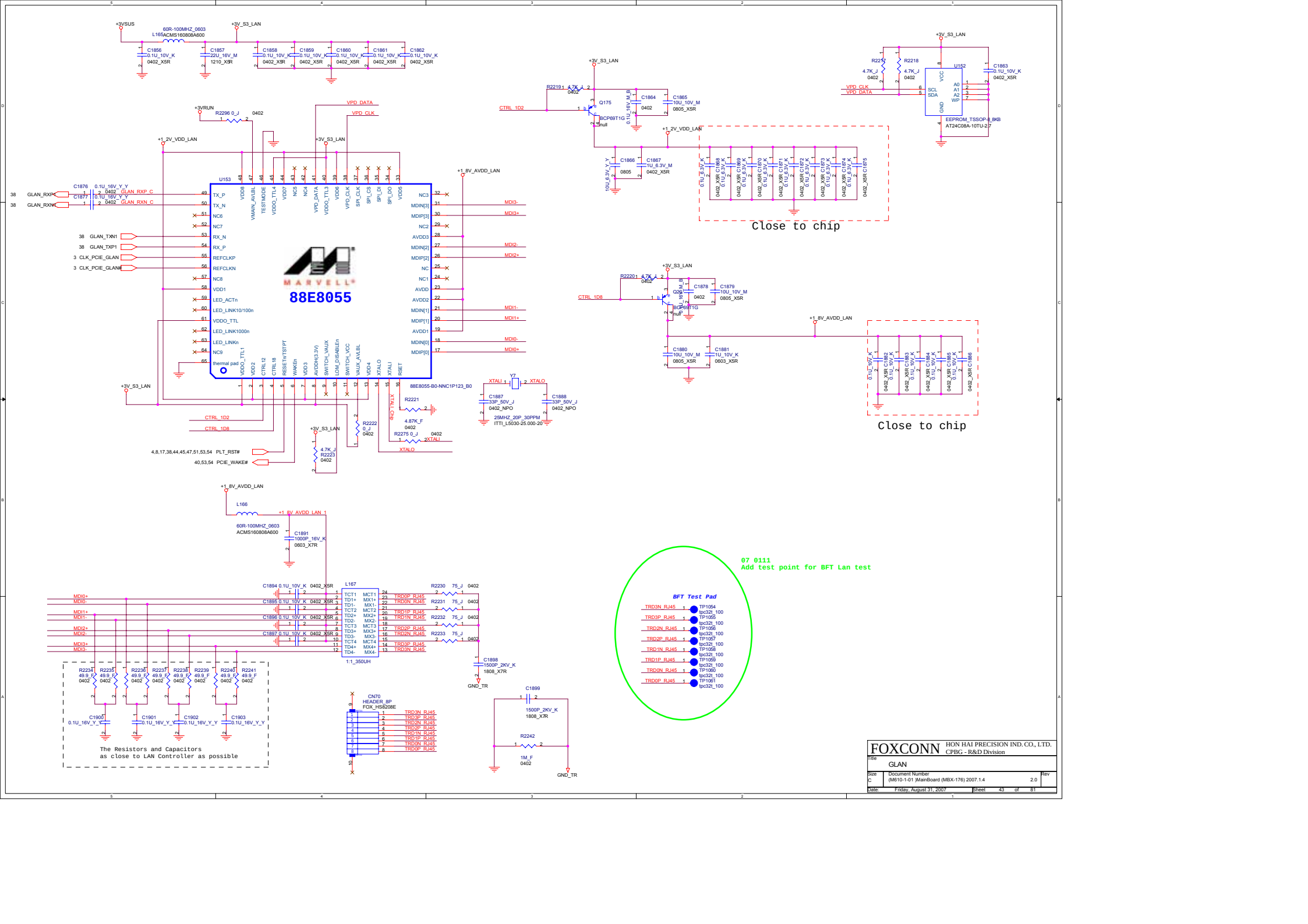
Title: ICH8-M(GND) 5/5		
Size: A3	Document Number: (M610-1-01)MainBoard (MBX-176) 2007.1.4	Rev: 2.0
Date: Friday, August 31, 2007	Sheet 42 of 81	


88E8055
Close to chip
Close to chip
07 0111
Add test point for BFT Lan test
BFT Test Pad
The Resistors and Capacitors
as close to LAN Controller as possible
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HON HAI PRECISION IND. CO., LTD.
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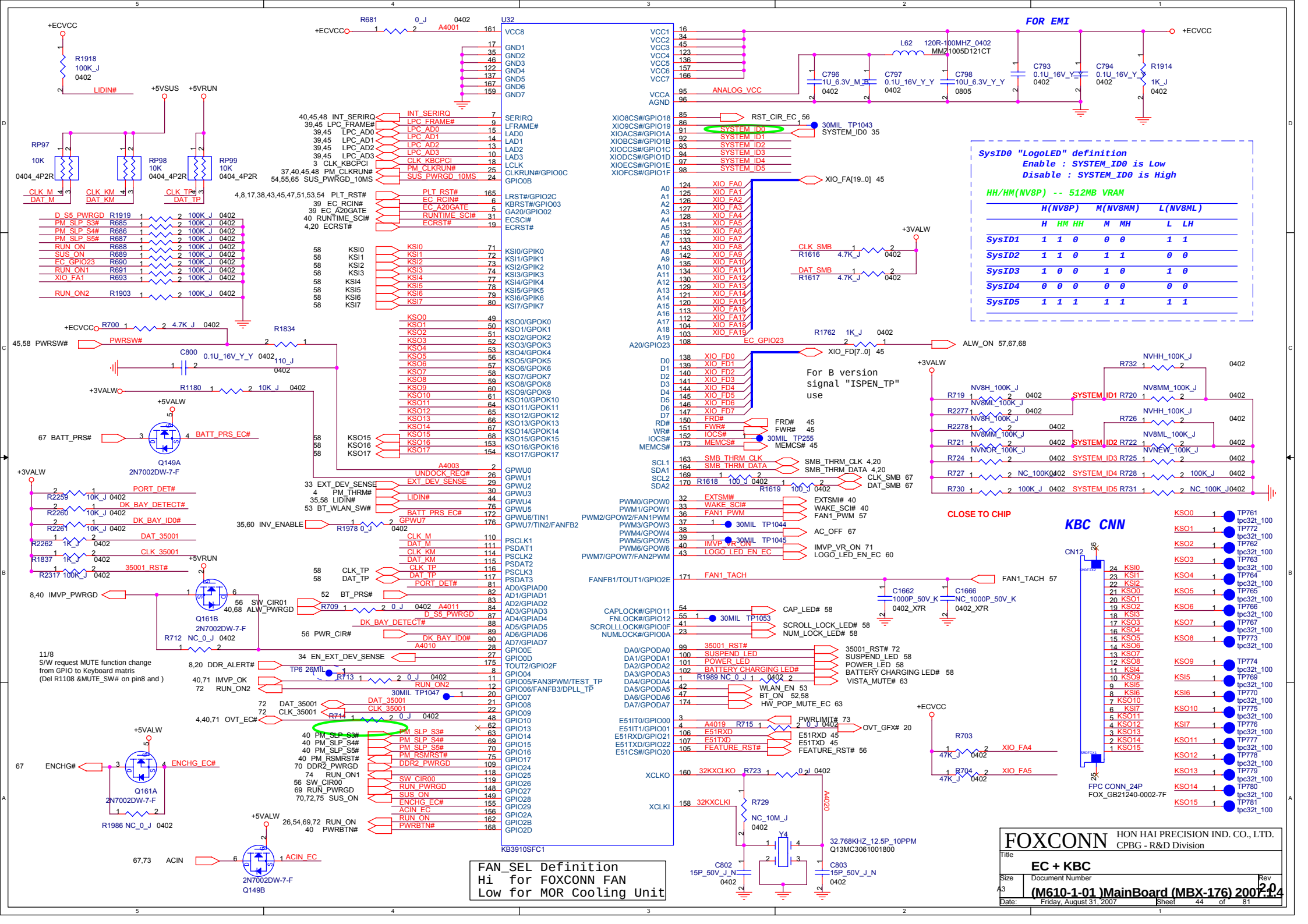
GLAN
Friday, August 31, 2007


FOR EMI
SysID0 "LogoLED" definition
Enable : SYSTEM_ID0 is Low
Disable : SYSTEM_ID0 is High
HH/HM(NV8P) -- 512MB VRAM
H(NV8P) M(NV8MM) L(NV8ML)
H HM HH M MH L LH
SysID1 1 1 0 0 0 1 1
SysID2 1 1 0 1 1 0 0
SysID3 1 0 0 1 0 1 0
SysID4 0 0 0 0 0 0 0
SysID5 1 1 1 1 1 1 1
For B version signal "ISPEN_TP" use
CLOSE TO CHIP
KBC CNN
FAN_SEL Definition
Hi for FOXCONN FAN
Low for MOR Cooling Unit
11/8
S/W request MUTE function change from GPIO to Keyboard matris
(Del R1108 &MUTE_SW# on pin8 and)
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
Title
EC + KBC
Size A3
Document Number
(M610-1-01)MainBoard (MBX-176) 2007-1-4
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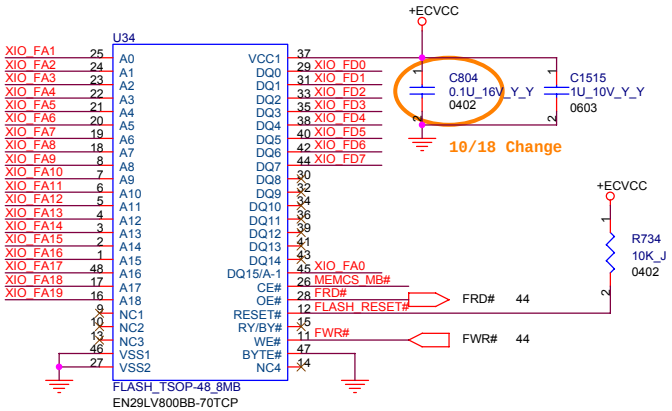
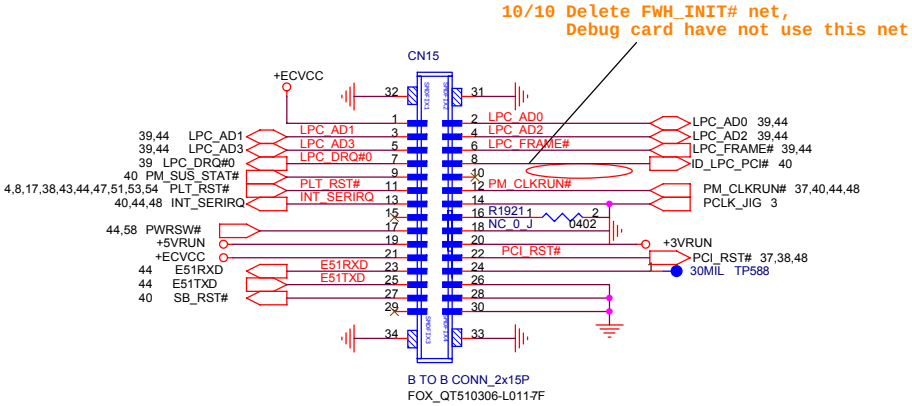
FLASH BIOS

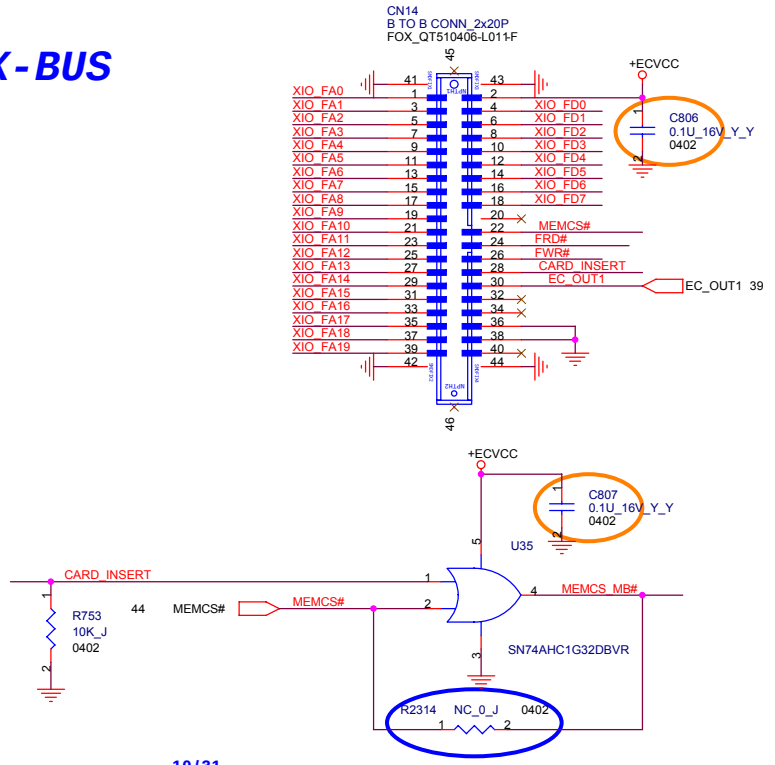
44 XIO_FA[19..0]
44 XIO_FD[7..0]



JIG-120



X-BUS



10/31
At M610 MP don't use X-BUS
CN14,U35,R753,C807 need NC
R2314 need stuff

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Title: **Flash ROM + Jig-120 + XBUS**

Size	Document Number	Rev
A3	(M610-1-01)MainBoard (MBX-176) 2007-1-4	2.0

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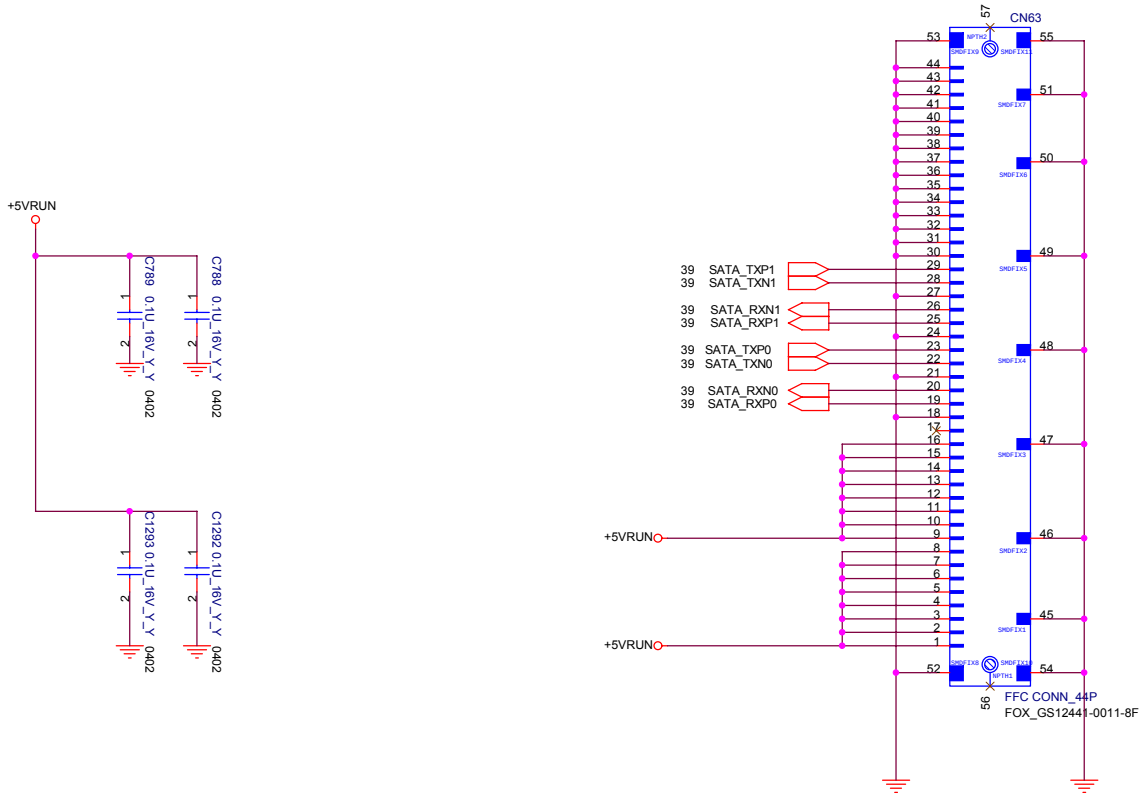

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	**SATA HDD RAID**	
Size A3	Document Number (M610-1-01)MainBoard (MBX-176) 2007.1.4	Rev 2.0
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11/3
MOR side suggest IRQ and IORDY pin
add pull up resistance by +5VRUN
(NC: R993 and R996)
Refer to MS90 schematics.

CD-ROM CONN

ODD must Master
H: Slave
L: Master

39 IDE_PDD[0..15] — IDE_PDD[0..15]

+5VRUN +3VRUN +5VRUN +3VRUN

R997 4.7K_J 0402
R993 NC_4.7K_J 0402
R998 8.2K_J 0402
R996 NC_8.2K_J 0402

R994 0_J 0402
TP107126MIL

C1025 4.7U_10V_Y_Y 0805
C1024 1000P_50V_M_B 0402
C1023 0.1U_16V_Y_Y 0402
C1667 0.1U_16V_Y_Y 0402
+5VRUN

C1908 NC_0.1U_16V_Y_Y 0402

R995 10K_J 0402

R990 47_J 0402
4,8,17,38,43,44,45,51,53,54 PLT_RST#

C1668 100P_50V_K 0402_NPO
C1906 NC_0.1U_16V_Y_Y 0402
C1905 NC_0.1U_16V_Y_Y 0402

C1907 NC_0.1U_16V_Y_Y 0402

CN32
FOX_QT8H0506-H111R-4F
B TO B CONN_50P

49	NC_1	NC_2	50
47	CSEL	GND_8	48
45	GND_3	GND_7	46
43	GND_2	GND_6	44
41	+5V_2	+5V_5	42
39	+5V_1	+5V_4	40
37	DASP#	+5V_3	38
35	CS1FX#	CS3FX#	36
33	DA0	DA2	34
31	DA1	PDIAG#	32
29	INTRQ	IOCS16#	30
27	IORDY	DMACK#	28
25	DIOW#	GND_5	26
23	GND_1	DIOR#	24
21	DD0	DMARQ	22
19	DD1	DD15	20
17	DD2	DD14	18
15	DD3	DD13	16
13	DD4	DD12	14
11	DD5	DD11	12
9	DD6	DD10	10
7	DD7	DD9	8
5	RESET#	DD8	6
3	AUDIO_GND	GND_4	4
1	AUDIO_L	AUDIO_R	2

PTH_1 NPTH1 51 53
PTH NPTH2 52 54

ODD_NC_1
CSEL2
ODD_NC_2

39 IDE_PDCS1# — IDE_PDCS1#
39 IDE_PDA0 — IDE_PDA0
39 IDE_PDA1 — IDE_PDA1
39 INT_IRQ14 — INT_IRQ14
39 IDE_PDIORDY — IDE_PDIORDY
39 IDE_PDIOW# — IDE_PDIOW#

IDE_PDCS3# — IDE_PDCS3# 39
IDE_PDA2 — IDE_PDA2 39
TP_PDIAG
IOCS16#
IDE_PDDACK# — IDE_PDDACK# 39
IDE_PDIOR# — IDE_PDIOR# 39
IDE_PDDREQ — IDE_PDDREQ 39

IDE_PDD0
IDE_PDD1
IDE_PDD2
IDE_PDD3
IDE_PDD4
IDE_PDD5
IDE_PDD6
IDE_PDD7
ODD_RESET#

IDE_PDD15
IDE_PDD14
IDE_PDD13
IDE_PDD12
IDE_PDD11
IDE_PDD10
IDE_PDD9
IDE_PDD8

VR1 IDE_PDD7 — NC_VPORT0603100MV05_VR
VR2 IDE_PDD6 — NC_VPORT0603100MV05_VR
VR3 IDE_PDD5 — NC_VPORT0603100MV05_VR
VR4 IDE_PDD4 — NC_VPORT0603100MV05_VR
VR5 IDE_PDA1 — NC_VPORT0603100MV05_VR
VR6 IDE_PDA0 — NC_VPORT0603100MV05_VR
VR7 TP_PDIAG — NC_VPORT0603100MV05_VR

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Title: PATA CD-ROM

Size	Document Number	Rev
A3	(M610-1-01)MainBoard (MBX-176) 2007.1.4	2.0

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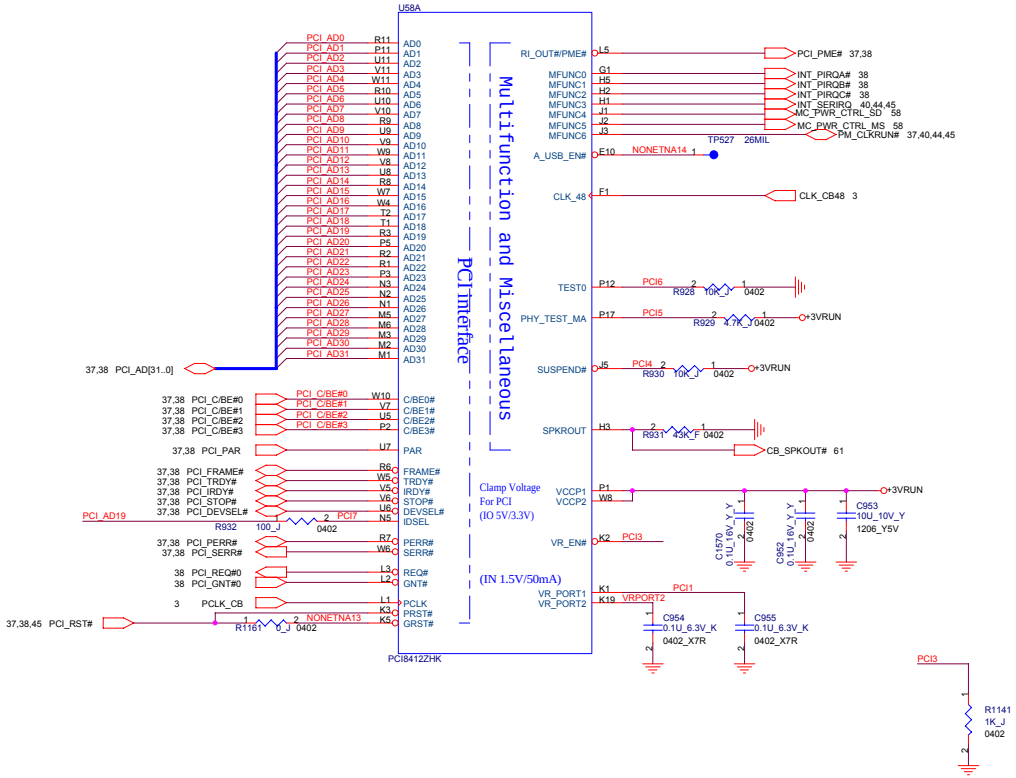
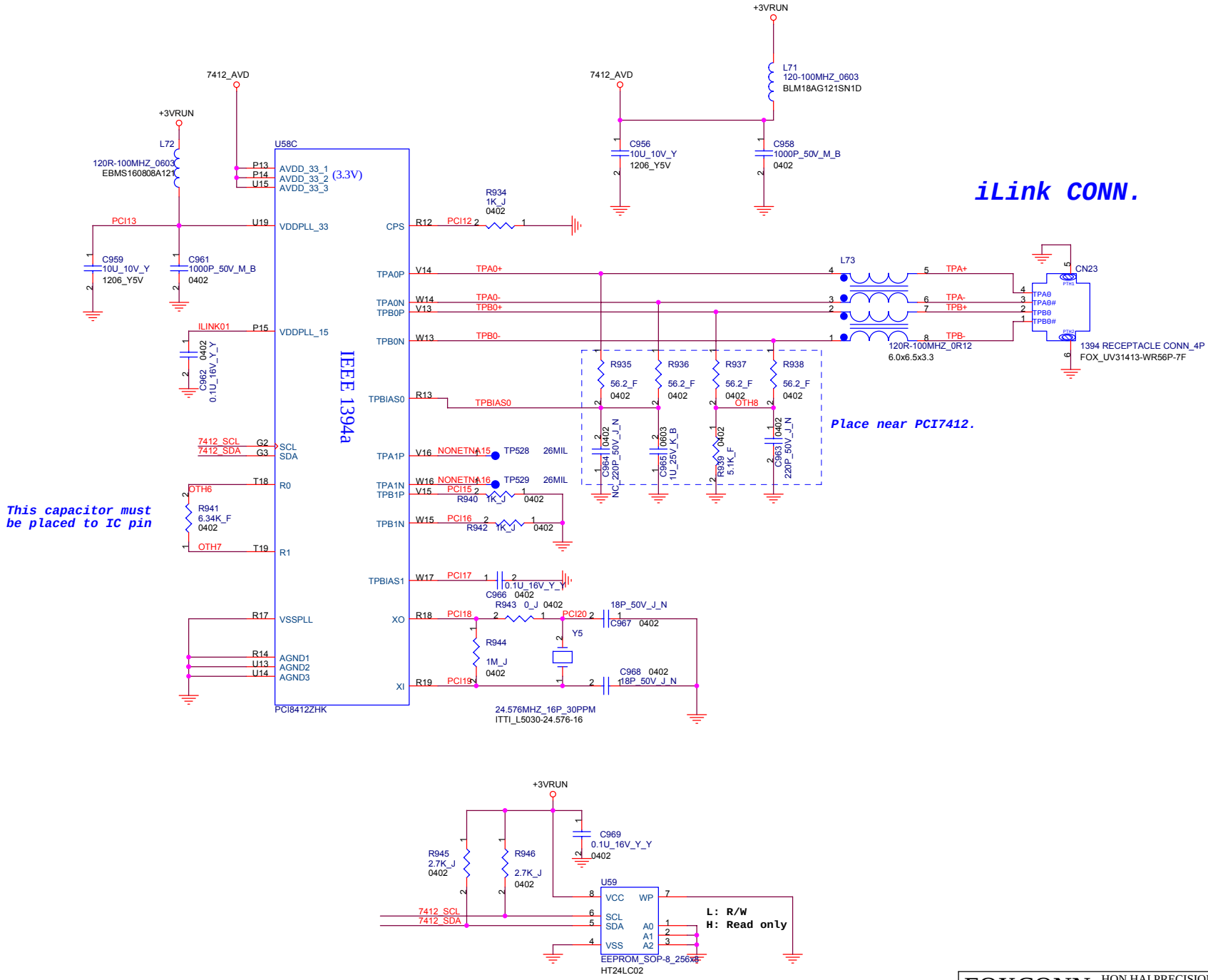
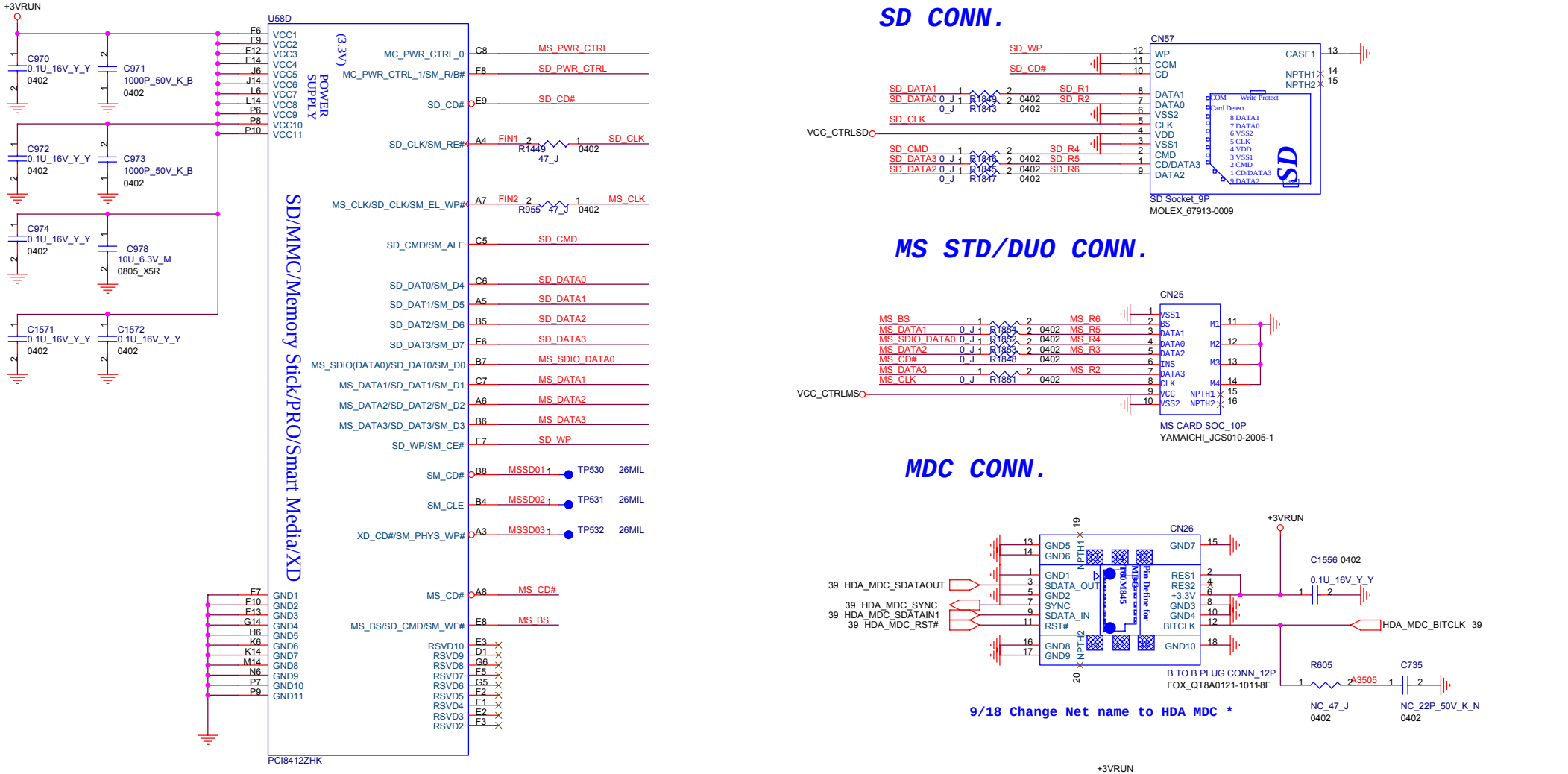


FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: PCI (PCI BUS)		
Size: Custom	Document Number: (M610-1-01)MainBoard (MBX-176) 2007.1.4	Rev: 2.0
Date: Friday, August 31, 2007	Sheet 48 of 81	



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	PCI (ILINK)
Size A3	Document Number (M610-1-01)MainBoard (MBX-176) 2007.1.4 2.0
Rev	
Date: Friday, August 31, 2007	Sheet 49 of 81



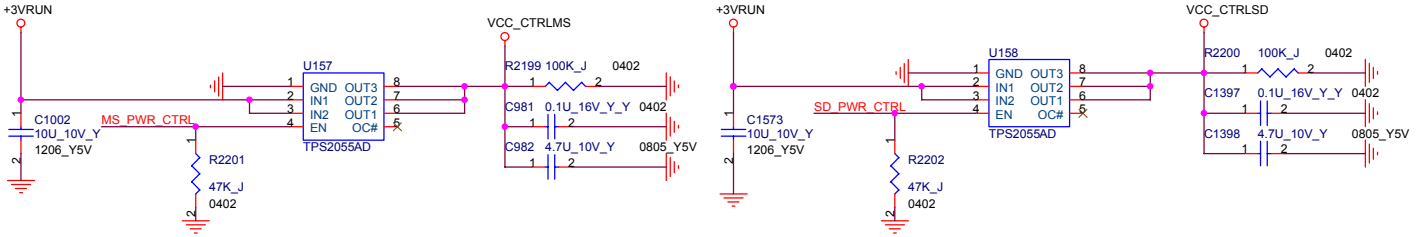
SD CONN.

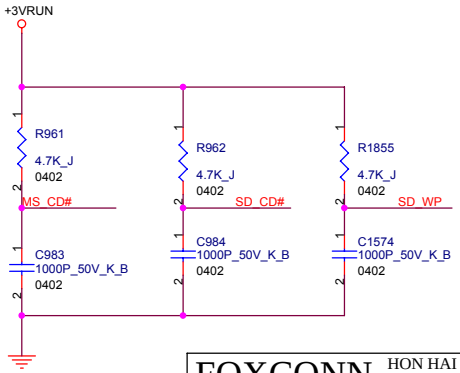
MS STD/DUO CONN.

MDC CONN.

9/18 Change Net name to HDA_MDC_*

02/12/07 PVT Change MS Power switch to TPS2055





FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: **PCI (MS-DUO/MDC)**

Size	Document Number	Rev
A3	(M610-1-01)MainBoard (MBX-176) 2007.1.4	2.0

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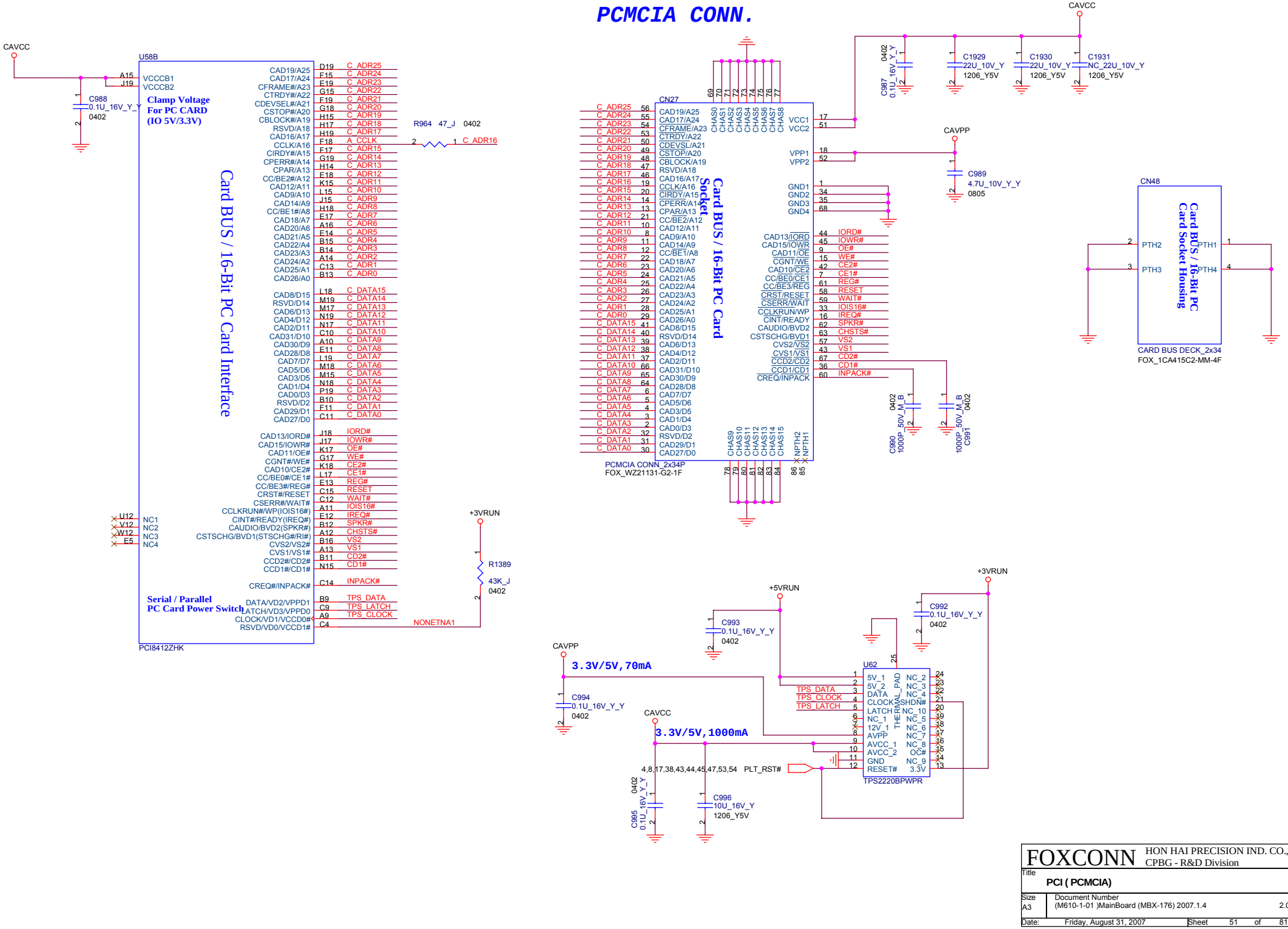
PCMCIA CONN.



FOXCONN HON HAI PRECISION IND. CO., LTD.
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Title: PCI (PCMCIA)

Size	Document Number	Rev
A3	(M610-1-01)MainBoard (MBX-176) 2007.1.4	2.0

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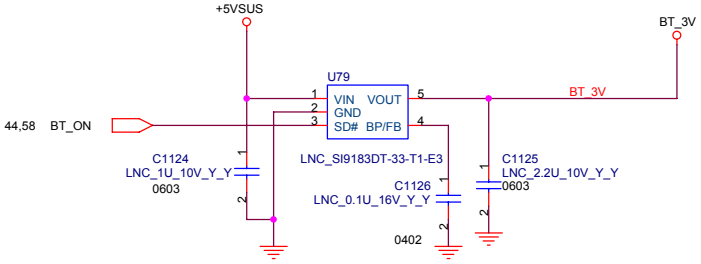
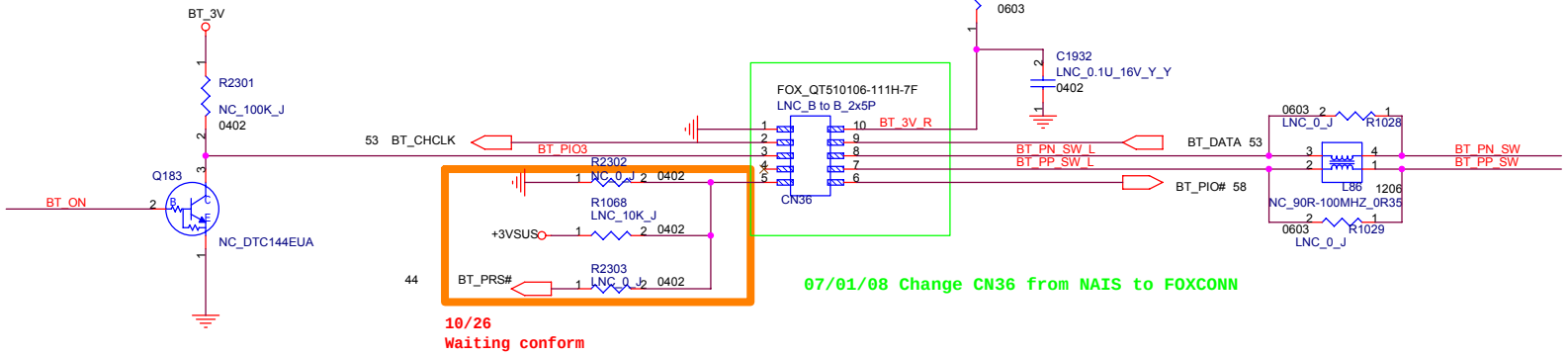


Bluetooth connector

10/26
New Blue tooth module



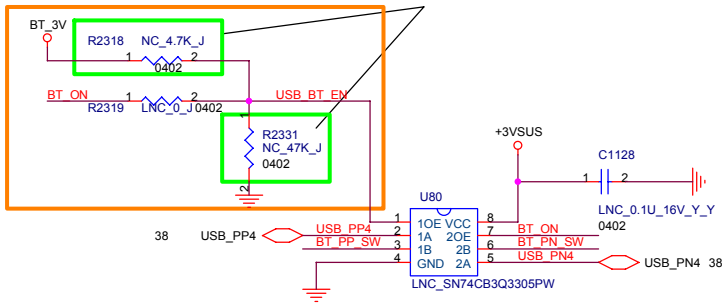
10/26
Waiting conform

07/01/08 Change CN36 from NAIS to FOXCONN

11/04 Change U80 Enable from BT_ON to BT_3V
U79 LDO Ton Max is 1000us
U80 BUS Switch Ton Max is 5ns

12/27 Change Bluetooch circuit Value to LNC_* for M610 DVT L SKU

12/14 Change R2318 from 1K to 4.7K, Add one 47K pull up resistance



To solve U80 enable pin (net name USB_BT_EN)floating during U79 (BT_3V from LDO)BT_ON desable,
Add Pull low 47K(R2331) at net USB_BT_EN, Change R2318 from 10K to 1K.

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: FAN/Bluetooth		
Size: A3	Document Number: (M610-1-01)MainBoard (MBX-176) 2007.1.4	Rev: 2.0
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Mini-PCIE Card connector

SW16
1BS007-12110-002-7F_SW_SMD7

+3VSUS
R1758 10K_J 0402
BT_WLAN_SW# 44

CN39
MINI PCIE_52P
FOX_AS0B226_S40K_4F

TP858
tpc32t_100

CN18
MINI PCI_52P
FOX_AS0B226_S40N_4F

40,43,54 PCIE_WAKE#
3 MINI_CARD_DET#
R1162 0_J 0402
3 CLK_PCIE_MINI#
3 CLK_PCIE_MINI
TP263 30MIL
TP264 30MIL
A4303
A4304

38 MINI_RXN3
38 MINI_RXP3
38 MINI_TXN3
38 MINI_TXP3

R2153 1 0_J 2 0402
R2154 1 0_J 2 0402
CL_CLK1_KEDRON
CL_DATA1_KEDRON
CL_RST1_KEDRON

11/15
E-ECN change NC to mount
(MOR side command)

WIRELESS_DATA
WIRELESS_CHCLK

1	WAKE#	+3_3V1	2
3	BT_DATA	GND1	4
5	BT_CHCLK	+1_5V1	6
7	CLKREQ#	RESERVED1	8
9	GND2	RESERVED2	10
11	REFCLK-	RESERVED3	12
13	REFCLK+	RESERVED4	14
15	GND3	RESERVED5	16
17	RESERVED6	GND4	18
19	RESERVED7	W_DISABLE#	20
21	GND5	PERST#	22
23	PERn0	+3_3Vaux	24
25	PERp0	GND6	26
27	GND7	+1_5V2	28
29	GND8	RESERVED8	30
31	PETn0	RESERVED9	32
33	PETp0	GND9	34
35	GND10	RESERVED10	36
37	RESERVED11	RESERVED12	38
39	RESERVED13	GND11	40
41	RESERVED14	NC1	42
43	RESERVED15	LED_WLAN#	44
45	RESERVED16	NC2	46
47	RESERVED17	+1_5V3	48
49	RESERVED18	GND12	50
51	RESERVED19	+3_3V2	52

MINI_PCIE_+3_3V
MINI_PCIE_+1_5V
MINI_PCIE_+3VAUX
WLAN_EN 44
PLT_RST# 4,8,17,38,43,44,45,47,51,54

A4305 30MIL TP265
A4306 30MIL TP266
A4307 30MIL TP267
A4308 30MIL TP268
A4309 30MIL
MINI_CARD_S_LED#
A4311 30MIL TP270

R2246 2 0_J 1 0603

R1926 NC_0_J 0402
Q154
2N7002ESPT
null
MINI_CARD_LED# 58
WLAN_EN

12/27 Change WLAN LED control signal from WLAN_EN to WLAN_LED_EN

10/27 FAE suggest
CL_CK1/CL_DATA1/CL_VREF1 can be left as NC if unused iAMT. Don't need to connect to WLAN card.

40 CL_CLK1 — CL_CLK1 — R2247 NC_0_J 0603 — CL_CLK1_KEDRON
40 CL_DATA1 — CL_DATA1 — R2248 NC_0_J 0603 — CL_DATA1_KEDRON
40 LINKALERT# — LINKALERT# — R2249 NC_0_J 0603 — CL_RST1_KEDRON

+3VSUS
R1067 0_J 0603
MINI_PCIE_+3VAUX
C814 0.1U_16V_Y_Y 0402
C1961 22U_10V_Y 1206_Y5V

+3VRUN
R760 1 2 0_J 0805
MINI_PCIE_+3_3V
C815 0.1U_16V_Y_Y 0402
C819 4.7U_10V_Y_Y 0805
C816 NC_22U_10V_Y_Y 1206

+1_5VRUN
R761 1 2 0_J 0805
MINI_PCIE_+1_5V
C822 0.1U_16V_Y_Y 0402
C824 4.7U_10V_Y_Y 0805
C823 NC_22U_10V_Y_Y 1206

WIRELESS_CHCLK — R1257 LNC_0_J 0603 — BT_CHCLK 52

11/04 Change U96 Power from BT_3V to +3VSUS

BT_3V
R2320 LNC_10K_J 0402
R2323 LNC_100K_J 0402
+3VSUS BT_3V
R2321 NC_0_J 0402
R2322 NC_0_J 0402
U96
LNC_74AHC1G08GW
WIRELESS_DATA
BT_DATA 52
R1912 100K_J 0402
R1258 NC_0_J 0603

12/27 Change Bluetooch circuit Value to LNC_* for M610 DVT L SKU

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	Mini-PCIE Card	
Size A3	Document Number (M610-1-01)MainBoard (MBX-176) 2007.1.4	Rev 2.0
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EXPRESS Card

VOLTAGE INPUTS(1)			LOGIC INPUTS			VOLTAGE OUTPUTS(2)			MODE(3)
AUXIN	3.3VIN	1.5VIN	SHDN	STBY	OP (4)	AUXOUT	3.3VOUT	1.5VOUT	
Off	x	x	x	x	x	Off	Off	Off	OFF
On	x	x	0	x	x	GND	GND	GND	Shutdown
On	x	x	1	x	1	GND	GND	GND	No Card
On	On	On	1	0	0	On	Off	Off	Standby
On	On	On	1	1	0	On	On	On	Card Inserted

U36
TPS2231PW

MOR not agree use ENE chip for second source
Change Express Card Power Switch (U36) from ENE P2231TF to TI TPS2231PW

Constant-voltage +1_5VSUS

12/29 Load current test fial, 1.8V transfer 1.5V drop
Voltage too large.12/27 Change Q180 from
17-NDS355A-N000 to 17-S12316D-ST00,
Change Q180 Power from +1_8VSUS to +3VSUS

650mA

Supply Max 275mA

Supply Max 1300mA

Supply Max 650mA

CN19
CARD CONNECTOR_26P
FOX_1CH4310C-DK

CN47
EXPRESS CARD HOUSING_26P
FOX_1CX43203-TC

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: EXPRESS CARD		
Size: A3	Document Number: (M610-1-01)MainBoard (MBX-176) 2007.1.4	Rev: 2.0
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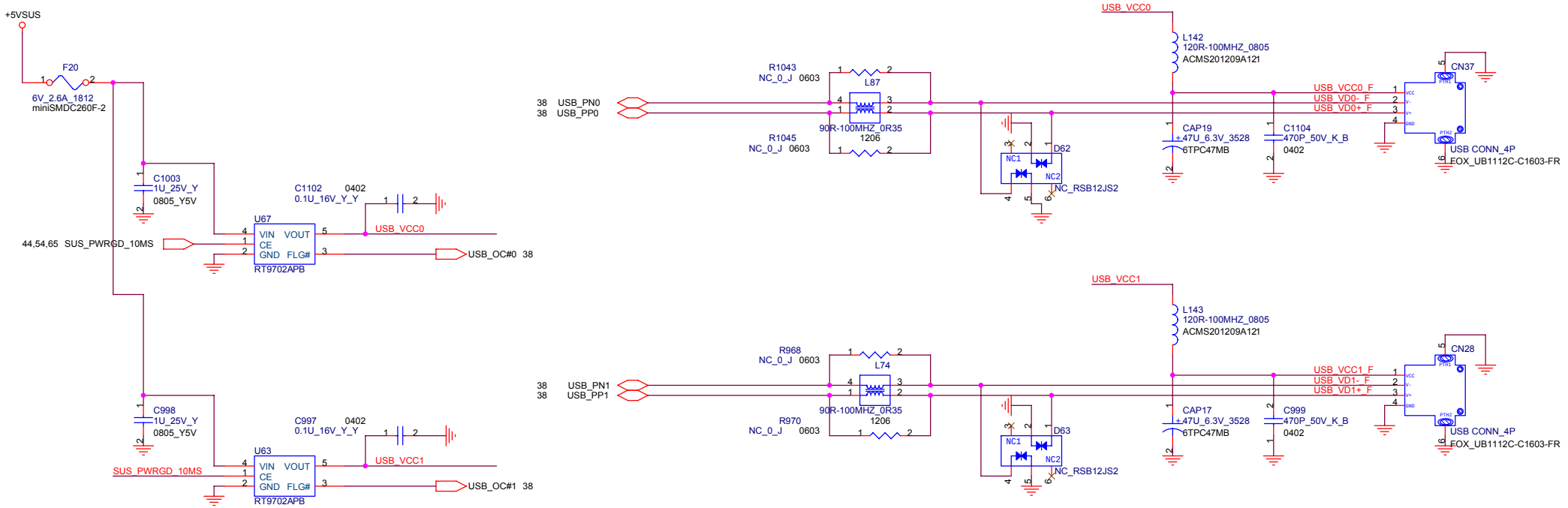
USB connector *2



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	**USB2.0/DOCKING CONN.**	
Size A3	Document Number (M610-1-01)MainBoard (MBX-176) 2007.1.4	Rev 2.0
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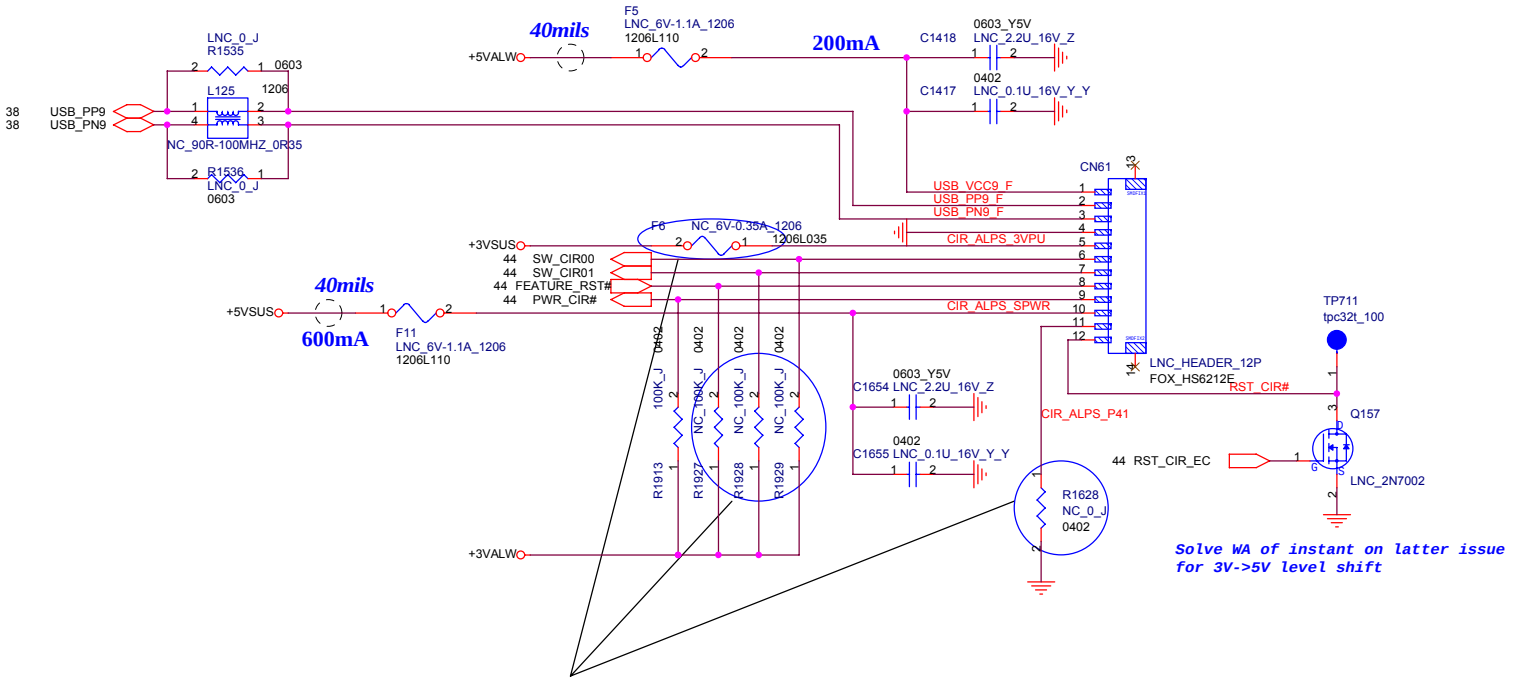
IR Rreceiver connector

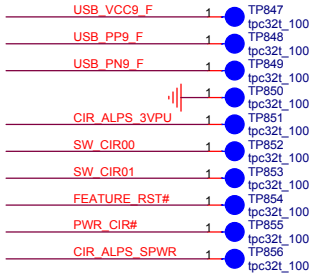


Solve WA of instant on latter issue for 3V->5V level shift

Button		SW1	SW0
VAIO button	Kick Instant On	L	L
Green button	Kick Windows	L	H
Shortcut button	Kick Windows	H	L
Standby button	Kick Windows	H	H

9/26 FOR NEW SMK IR module compatily
1.Change stuff to NC:F6,R1927,R1928,R1929,
2.EC Page GPIO20(105),GPIAD2(83) pin swape

12/27 Change CIR circuit Value to LNC_* for M610 DVT L SKU



Num	Signal Name	I/O	Comment	Difference from ALPS.
1	+5VALW	VCC		<-
2	USB+	I/O		<-
3	USB-	I/O		<-
4	GND	GND		<-
5	+3VSUS	-	Not for use. Because SMK's IC use internal pull up resistor for D-.	ALPS's IC use this signal as a pull up plane of D- for low speed detection.
6	SW0	O	Use for detecting of the remote button. 3.3V CMOS output.	3.3V open drain output.
7	SW1	O	Use for detecting of the remote button. 3.3V CMOS output.	3.3V open drain output.
8	FeatureRST#	I	Software reset signal. (3.3V internal pull up resistor.)	Use for detecting of the remote button. 3.3V open drain output.
9	PWR#	O	Power on request signal. Open drain output.	<-
10	SPWR	I	Power OK signal. 5V input.	<-
11	EN	-	Not for use.	Low: Disable instant on feature Open or High: Enable instant on feature (3.3V internal pull up resistor.)
12	HardRST#	I	Hardware reset.	<-

At Only USB Internal CIR, it's USB Power

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: **LED/LID SW#/Touch PAD**

Size	Document Number	Rev
A3	(M610-1-01)MainBoard (MBX-176) 2007.1.4	2.0

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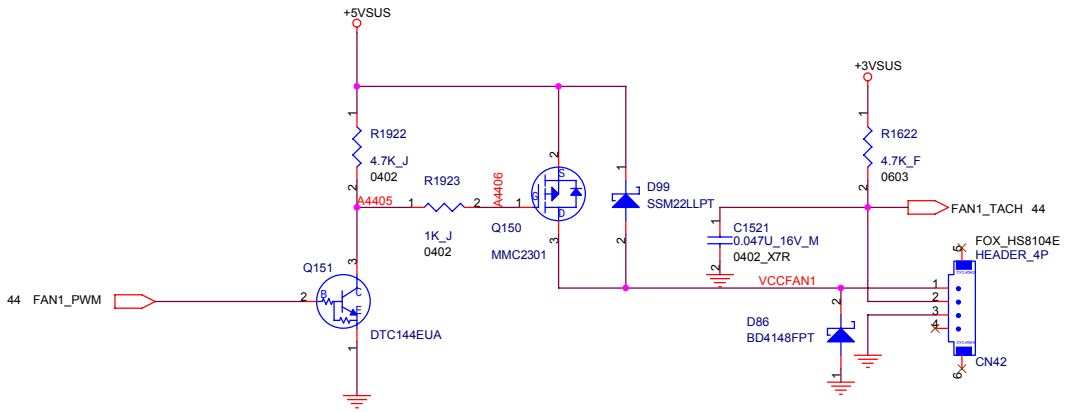
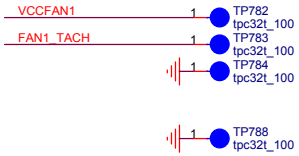
FAN circuit

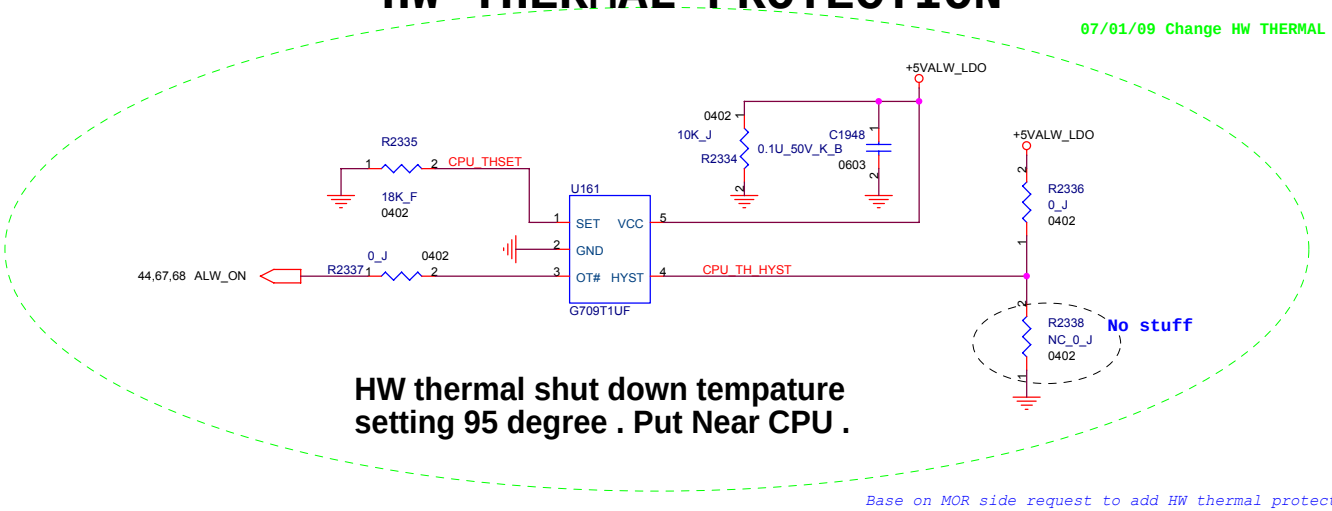


FAN1



HW THERMAL PROTECTION

07/01/09 Change HW THERMAL PROTECTION circuit to stuff

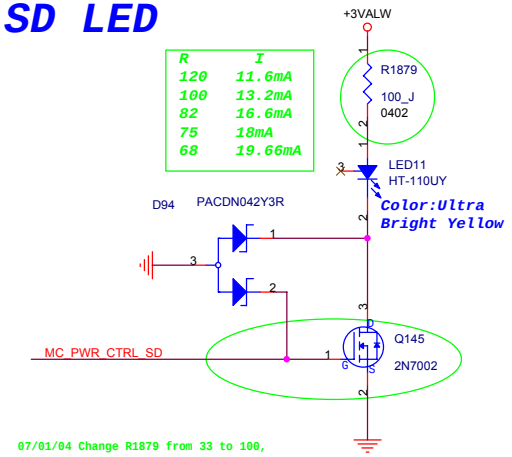


HW thermal shut down tempature setting 95 degree . Put Near CPU .

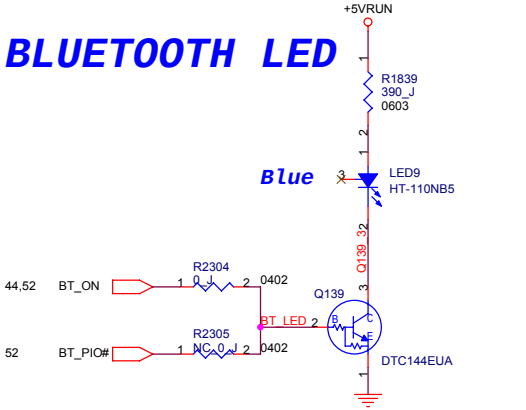
Base on MOR side request to add HW thermal protection circuit

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	FAN / HW THERMAL PROTECTION	
Size A3	Document Number (M610-1-01)MainBoard (MBX-176) 2007.1.4	Rev 2.0
Date: Friday, August 31, 2007	Sheet 57 of 81	

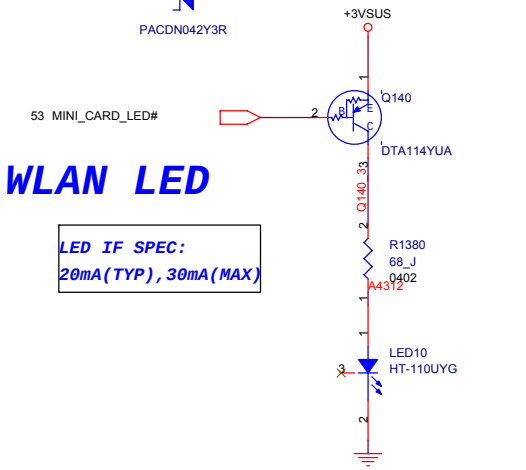
SD LED



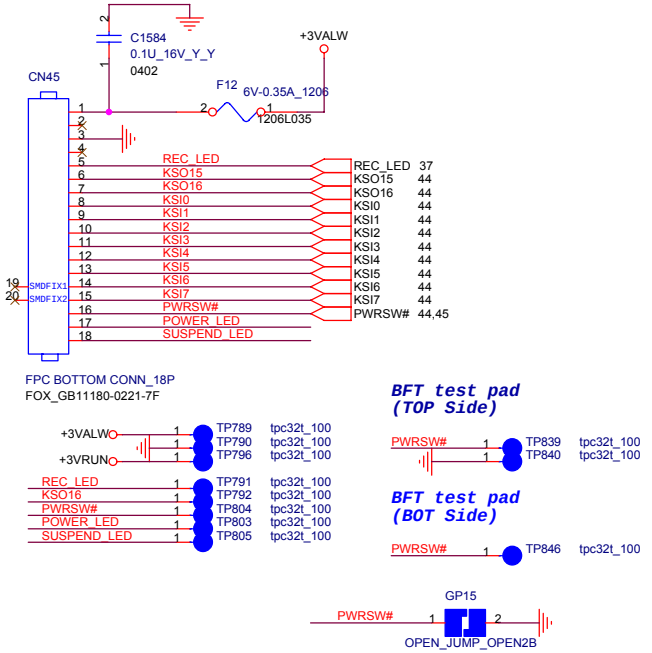
BLUETOOTH LED



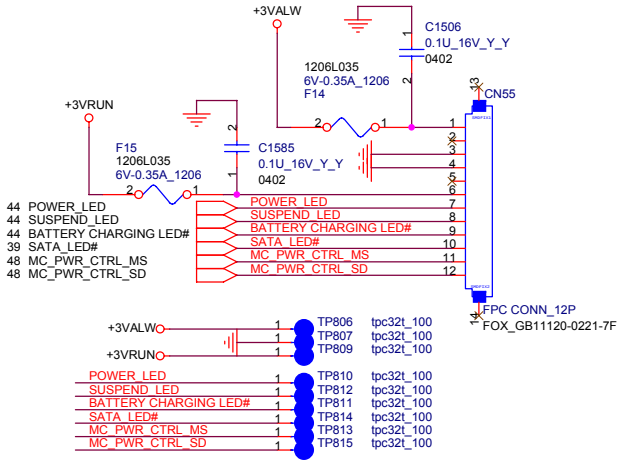
WLAN LED



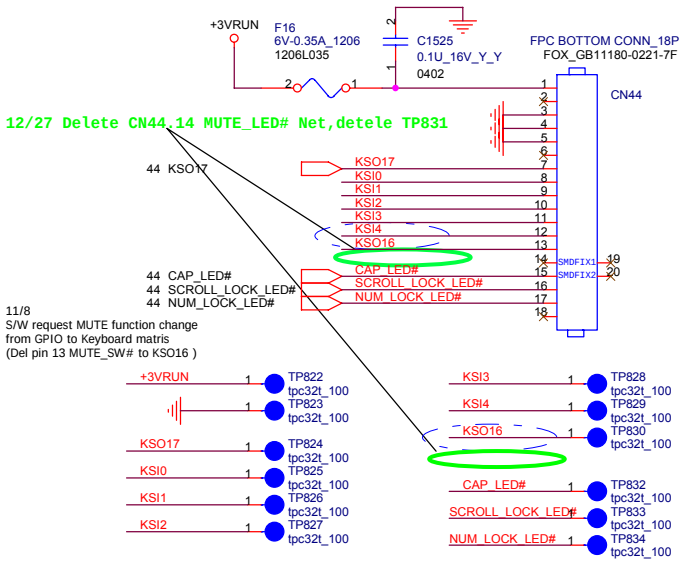
To Power Button Board Connector



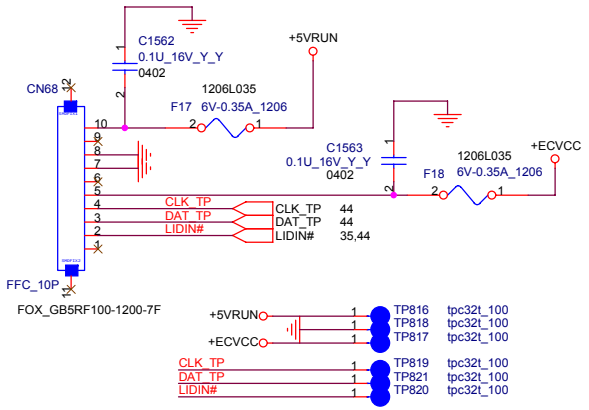
To LED Board Connector



To AV Function Board Connector



To Touch Pad Board Connector



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	POWER BD + HOT KEY BD + T/P&LED BD + LOGO LED	
Size: A3	Document Number: (M610-1-01)MainBoard (MBX-176) 2007-4	Rev: 2.0
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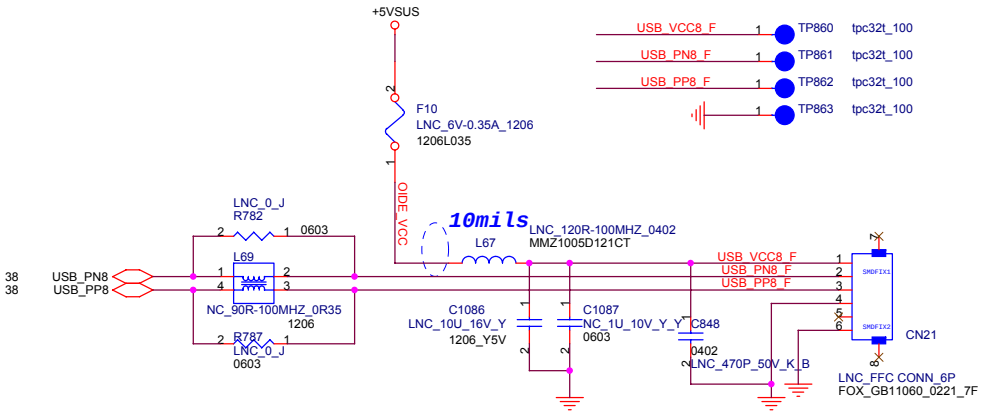
OIDE Connector

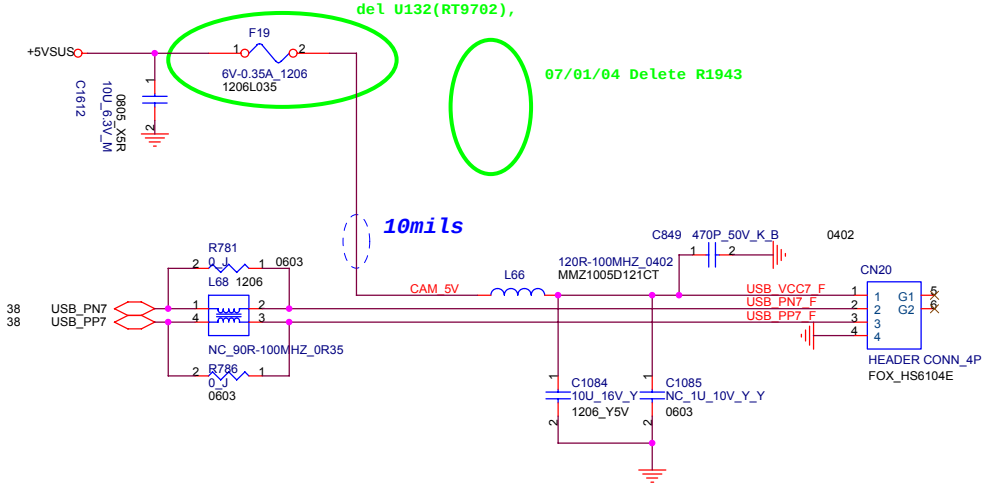


2006.1.4pin swape for ME request

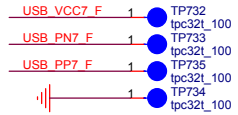
12/27 Change Felica circuit Value to LNC_* for M610 DVT L SKU

CAMERA Connector

12/22
Base on MOR side suggest to modify cammera power source circuit,
Add F19(LITTLELFUSE 0.35A) between net +5VSUS and CAM_5V,
del U132(RT9702),



12/21 BFT Test Pad



FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: CAM/OIDE

Size	Document Number	Rev
A3	(M610-1-01)MainBoard (MBX-176) 2007.1.4	2.0

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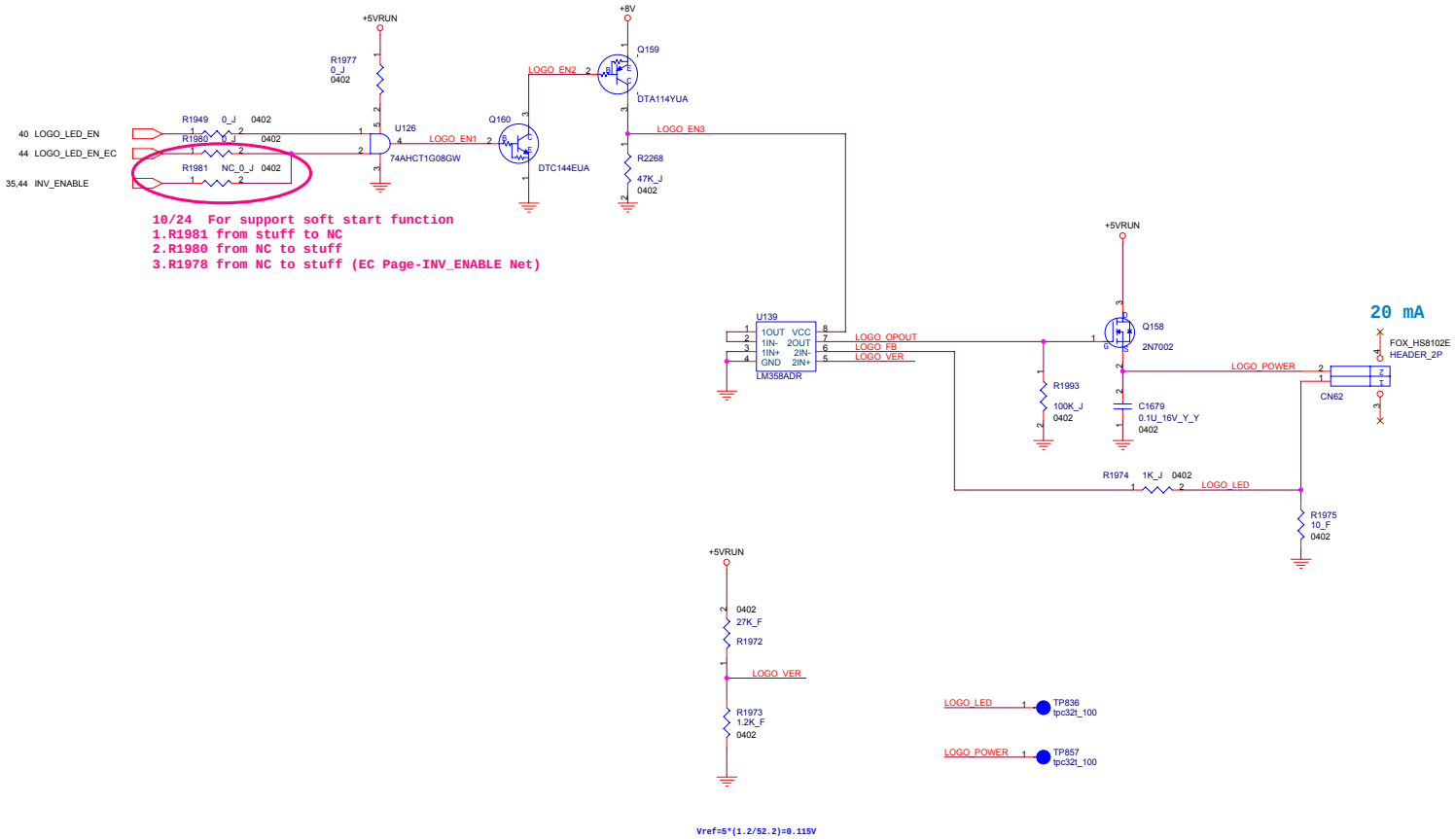
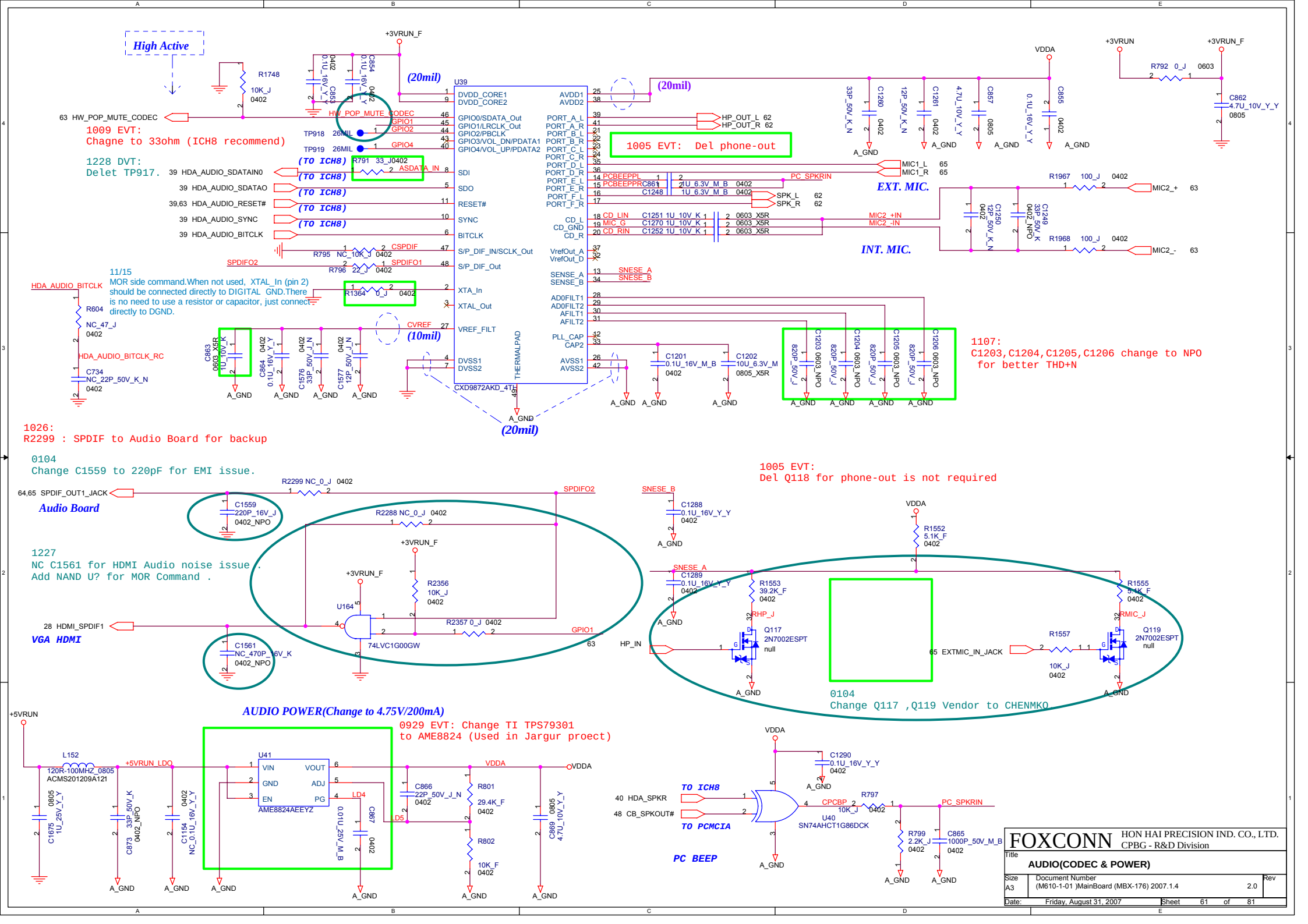
Constant-Current SONY LOGO LED



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: Logo LED / +1_5VSUS		
Size: Custom	Document Number: (M610-1-01)MainBoard (MBX-176) 2007.1.4	Rev: 2.0
Date: Friday, August 31, 2007	Sheet 60 of 81	


High Active
1009 EVT:
Chagne to 33ohm (ICH8 recommend)
1228 DVT:
Delet TP917.
11/15
MOR side command.When not used, XTAL_In (pin 2) should be connected directly to DIGITAL GND.There is no need to use a resistor or capacitor, just connect directly to DGND.
1005 EVT: Del phone-out
EXT. MIC.
INT. MIC.
1107:
C1203,C1204,C1205,C1206 change to NPO for better THD+N
1026:
R2299 : SPDIF to Audio Board for backup
0104
Change C1559 to 220pF for EMI issue.
Audio Board
1227
NC C1561 for HDMI Audio noise issue .
Add NAND U? for MOR Command .
VGA HDMI
1005 EVT:
Del Q118 for phone-out is not required
0104
Change Q117 ,Q119 Vendor to CHENMKO
AUDIO POWER(Change to 4.75V/200mA)
0929 EVT: Change TI TPS79301
to AME8824 (Used in Jargur proect)
TO ICH8
TO PCMCIA
PC BEEP
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
AUDIO(CODEC & POWER)
Document Number
(M610-1-01)MainBoard (MBX-176) 2007.1.4
2.0
Friday, August 31, 2007
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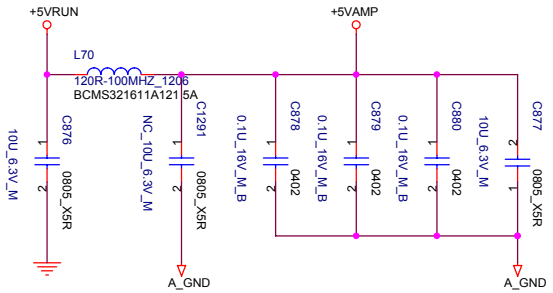
0920
Add 2PCS CAP39,CAP40 100_6.3V_M
Delet CAP24,CAP25

1103
Change CAP39 and CAP40 Vendor from NIPPON CHEMI-CON to LELON

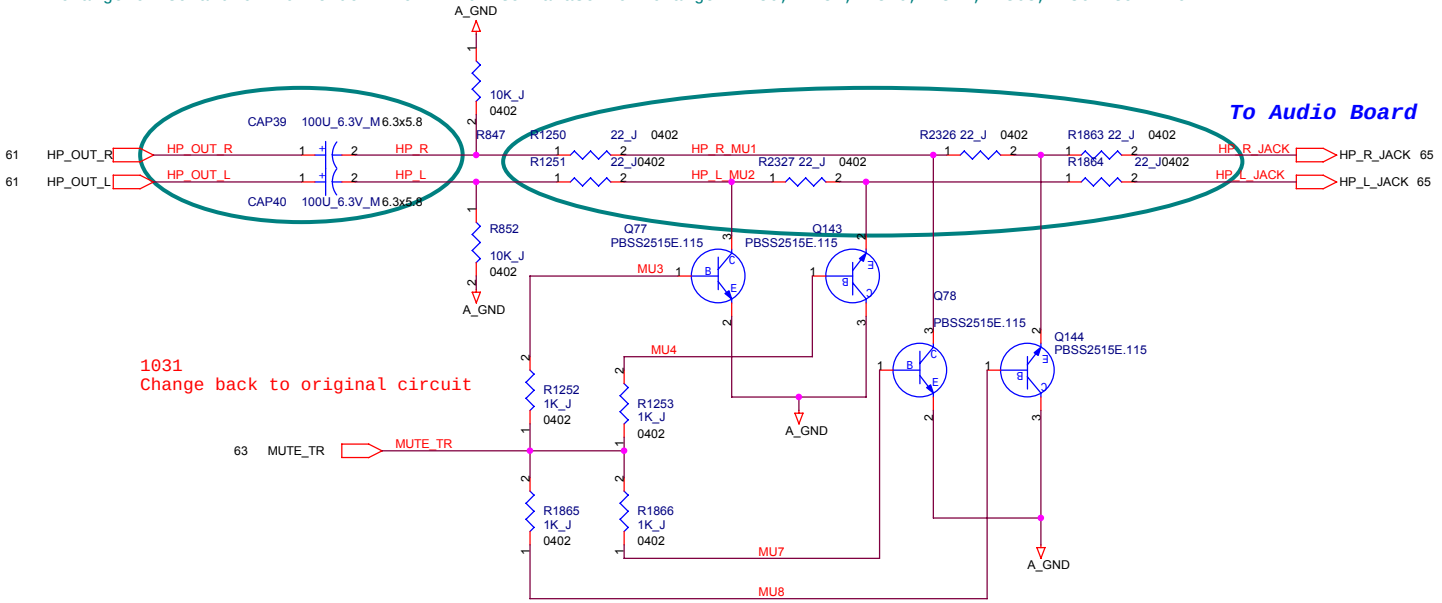
1228
Change CAP39 and CAP40 Vendor from LELON to Panasonic

1229
Change R1250,R1251,R2326,R2327,R1863,R1864 to 22 ohm.

Max 1.7A



To Audio Board

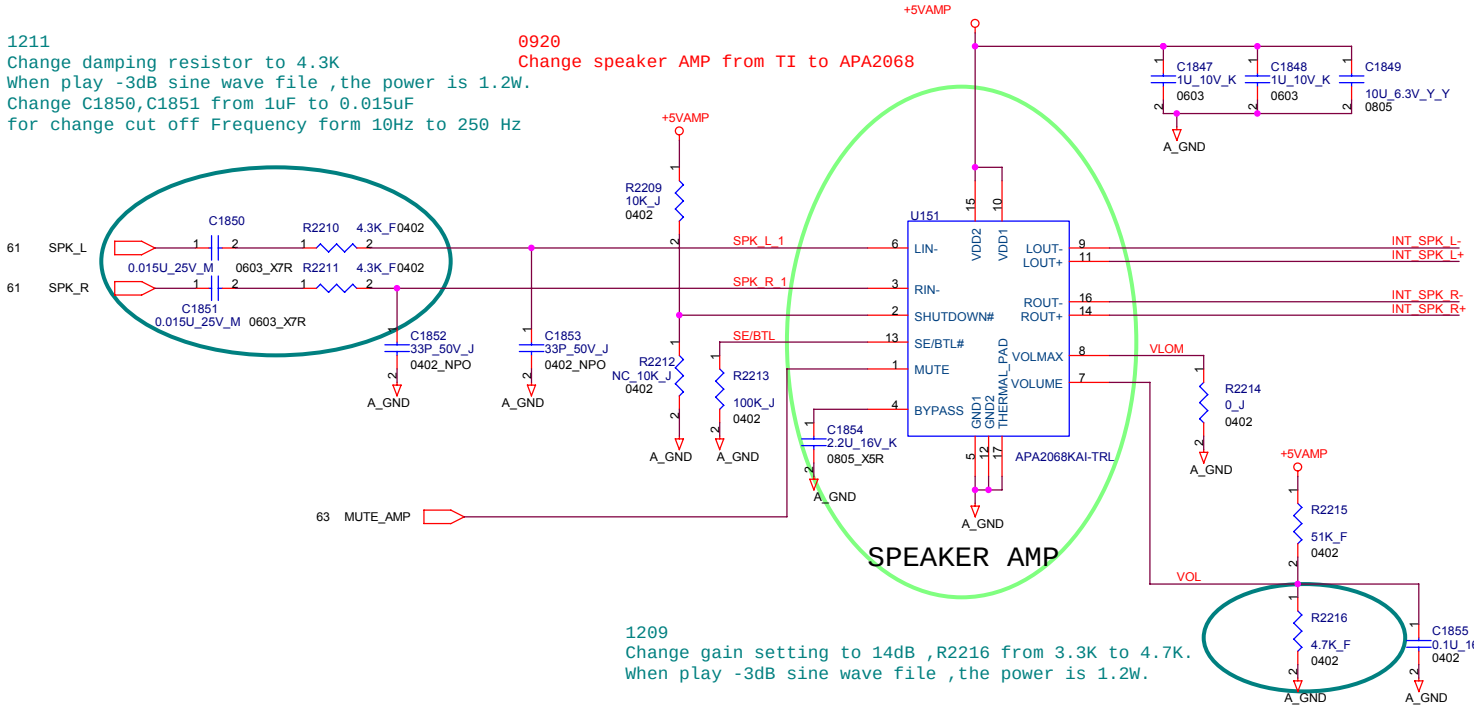


1031
Change back to original circuit

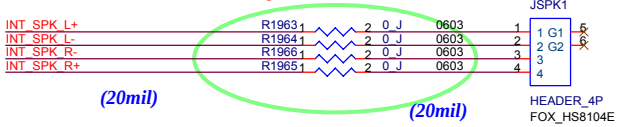
INTERNAL SPEAKER

1211
Change damping resistor to 4.3K
When play -3dB sine wave file ,the power is 1.2W.
Change C1850,C1851 from 1uF to 0.015uF
for change cut off Frequency form 10Hz to 250 Hz

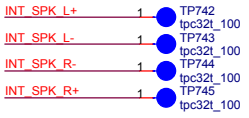
0920
Change speaker AMP from TI to APA2068



0920
Change to 0ohm 0603



BFT Test Pad



Gain setting table

Gain	R2216	Voltage
8dB	9.1K	0.77V
10dB	7.68K	0.65V
12dB	6.2K	0.54V
14dB	4.7K	0.43V
16dB	3.3K	0.31V

1209
Change gain setting to 14dB ,R2216 from 3.3K to 4.7K.
When play -3dB sine wave file ,the power is 1.2W.

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: AUDIO(AMP & HP & SPK)

Size: A3 | Document Number: (M610-1-01)MainBoard (MBX-176) 2007.1.4 | Rev: 2.0

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1004
Change U45, U140 as NC
For Headphone in mute speaker out
isn't supported in Dos mode
1005
Phone-out is not required

Circuit setting table

Circuit 0 (Beagle)	Circuit 1 No support Dos mute (Default)	Circuit 2 Support Dos mute	component
Stuff	NC	Stuff	U45
NC	NC	Stuff	U140
NC	Stuff	NC	R1985
Stuff	NC	NC	R1984

1025
Change Mute control circuit
(Same with MS30/50/90)

0111'07
Change Q181 from 17-MMBT390-4000
to 17-MMBT390-4001 for PUR can't buy issue

1227
Change R1321 and R1325 from 4.7k_J to 4.7K_F
for MOR Side Command.

0104
Change R1361 From 33k to 22k For improve Mute_TR signal quality well.

1005
Del phone-out mute circuit
for phone-out is not required

From EC/CODEC MUTE .

INTERNAL MIC(Non)

BFT Test Pad

Title	AUDIO (MUTE & INTMIC)
Size	A3
Document Number	(M610-1-01)MainBoard (MBX-176) 2007.1.4
Rev	1.0
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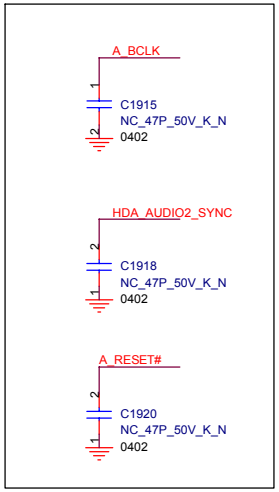
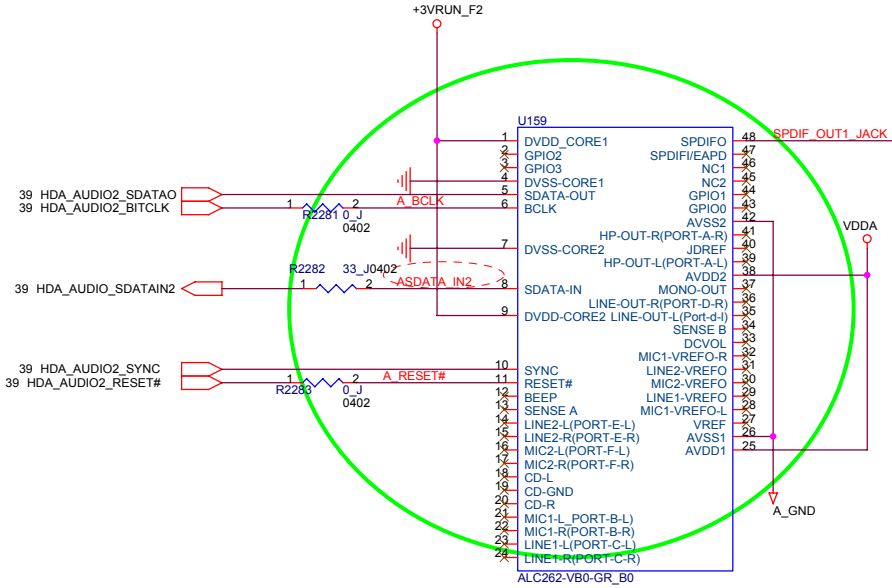
FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

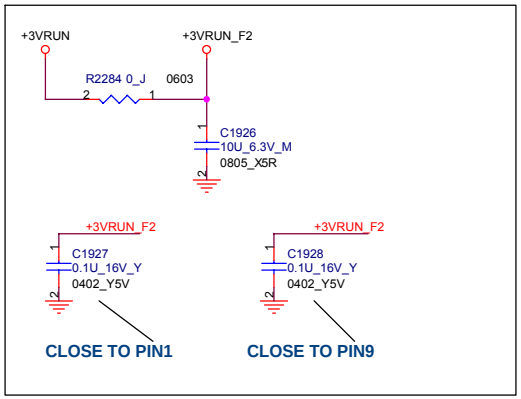
Anti-Glitch



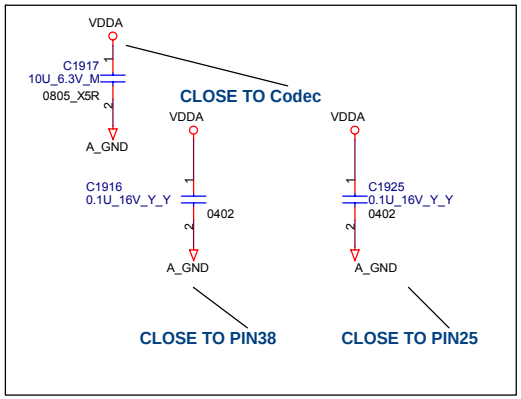


1018
Change ALC262 to ALC268.
(If ALC268 sample schdule delay, change to ALC262)
1024
Change SPDIF of Second codec to MB optical out
1102
Change ALC268 to ACL262

Decoupling Caps, place close to power pin.



Decoupling Caps, place close to power pin.



FOXCONN HON HAI PRECISION IND. CO., LTD.
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Title: **AUDIO (Secod Codec for HDMI SPDIF)**

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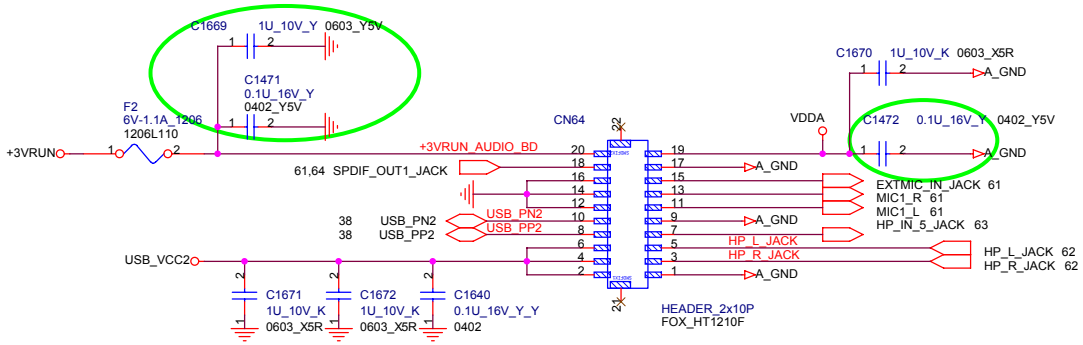
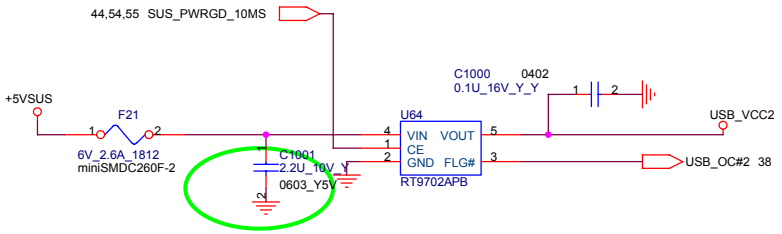
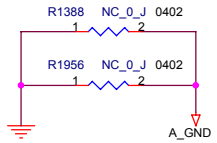
Audio Board connector



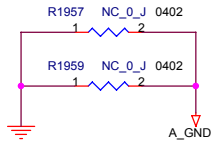


Backup two jumper resistors for bridge between GND and A_GND

Close screw hole H3

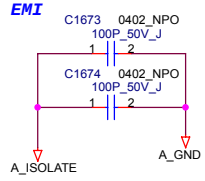


Close screw hole H5

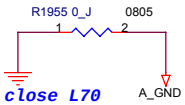


Isolate screw hole H4, and add EMI/ESD solution

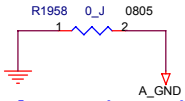
EMI



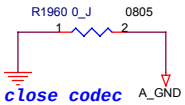
Add jumper resistor for Return patch



close L70

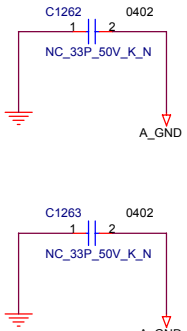


close U41(+5VRUN)

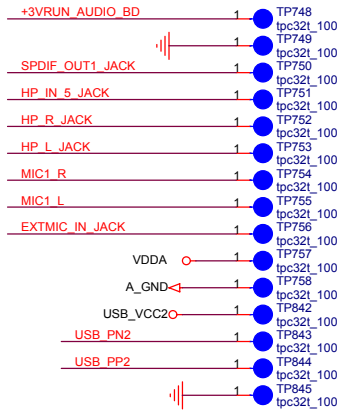


close codec (the same with MS20)

Original EMI back up solution to continue with MS20(bridge between GND and A_GND)



BFT Test Pad



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: **Audio Board conn**		
Size: A3	Document Number: (M610-1-01)MainBoard (MBX-176) 2007.1.4	Rev: 2.0
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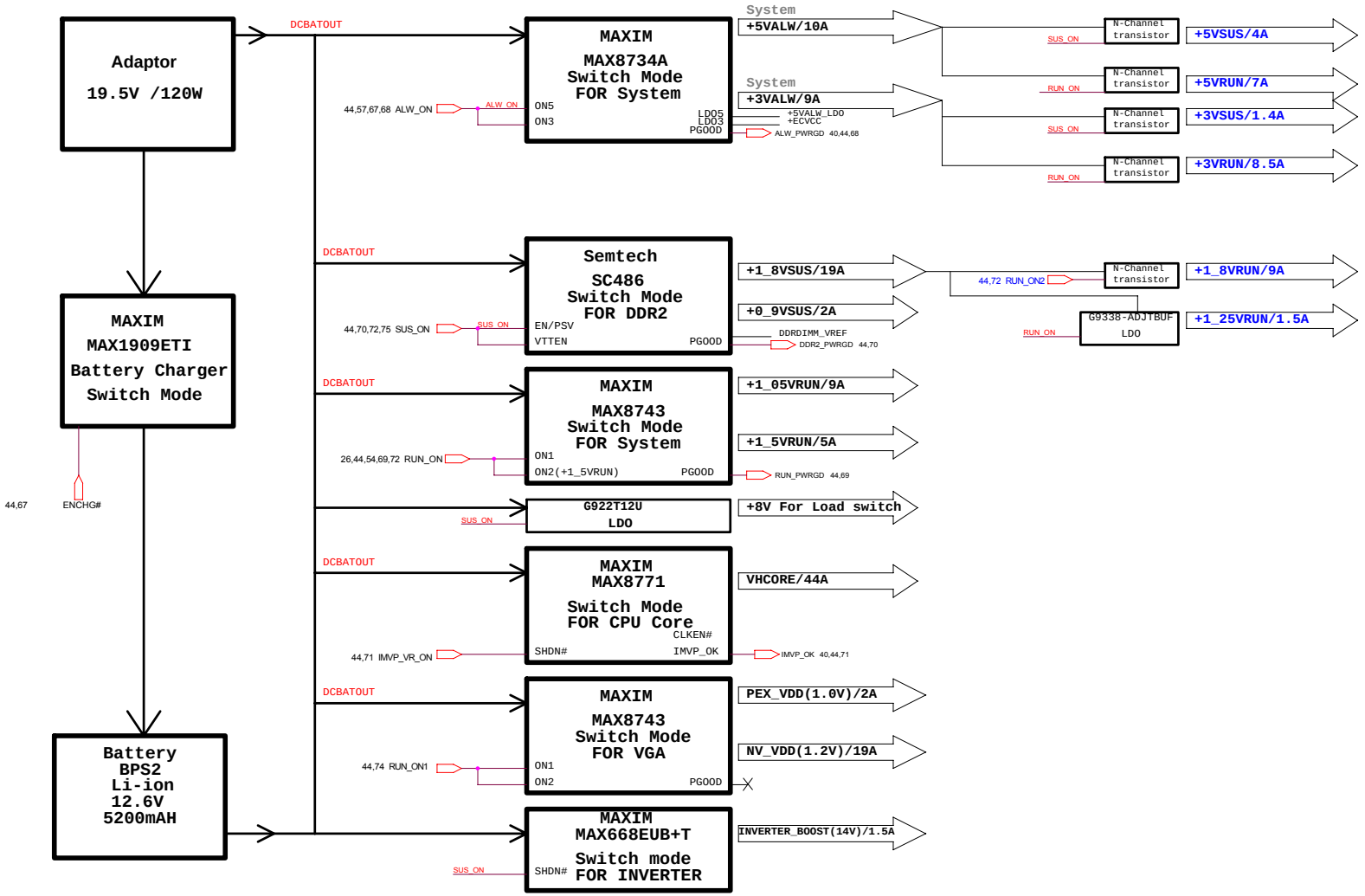

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: Power Design Diagram-ZG

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A2	(M610-1-01)MainBoard (MBX-176) 2006.12.29	2.0

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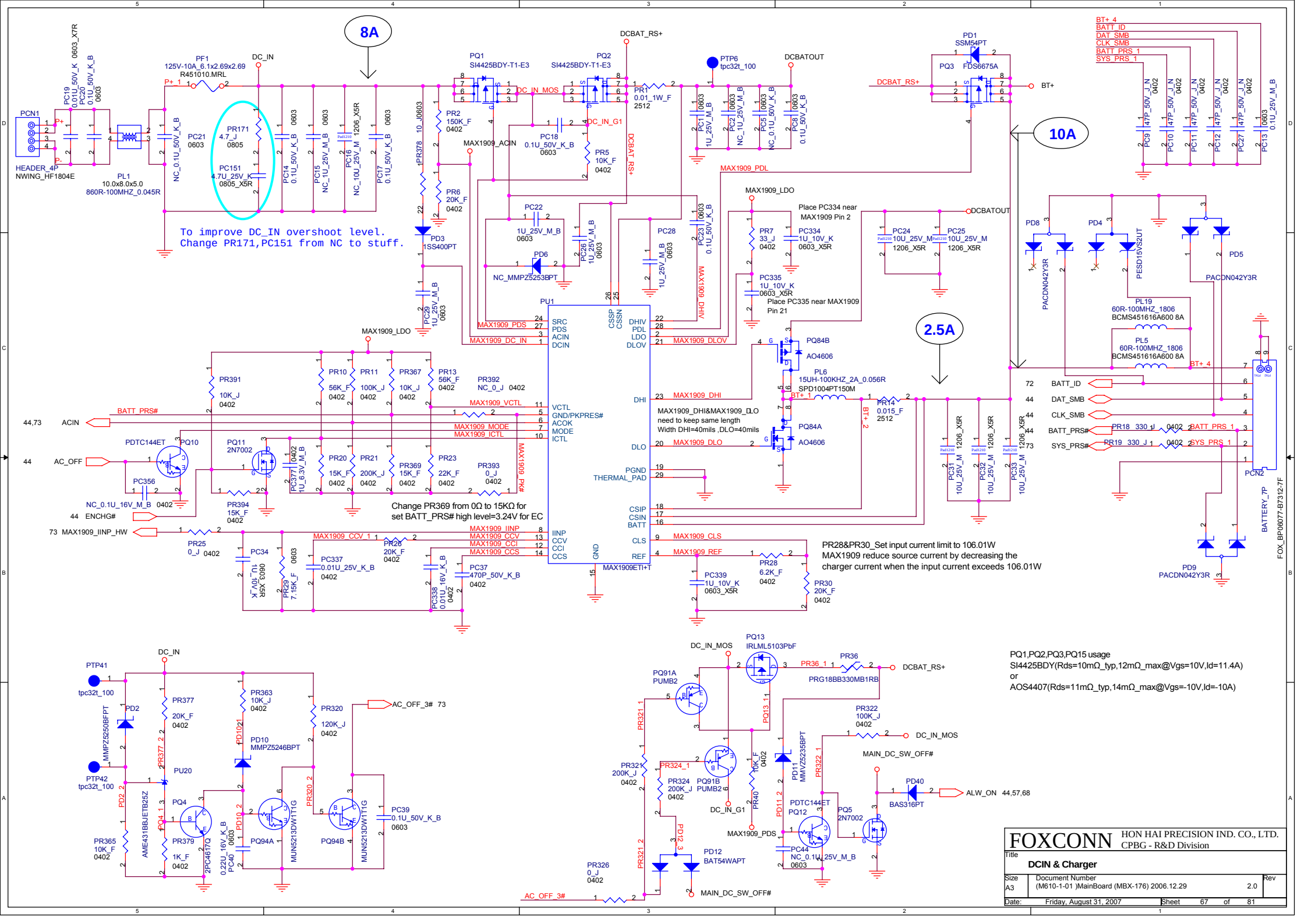
8A
10A
2.5A
DC_IN
DCBAT_RS+
DCBATOUT
BT+
PF1
125V-10A_6.1x2.69x2.69
R451010.MRL
PQ1
SI4425BDY-T1-E3
PQ2
SI4425BDY-T1-E3
PTP6
tpc32t_100
PD1
SSM54PT
PQ3
FDS6675A
PCN1
HEADER_4P
NWING_HF1804E
PL1
10.0x8.0x5.0
860R-100MHZ_0.045R
PR171
4.7_J
0805
PC151
4.7U_25V_K
0805_X5R
To improve DC_IN overshoot level.
Change PR171,PC151 from NC to stuff.
PR1
0.01_1W_F
2512
PR2
150K_F
0402
PR5
10K_F
0402
PR6
20K_F
0402
PC18
0.1U_50V_K_B
0603
DC_IN_MOS
DC_IN_G1
DCBAT_RS+
MAX1909_ACIN
PD3
1SS400PT
PD6
NC_MMPZ5253BPT
PC22
1U_25V_M_B
0603
PC28
1U_25V_M_B
0603
PC29
1U_25V_M_B
0603
PU1
MAX1909_PDS
MAX1909_DC_IN
MAX1909_LDO
MAX1909_PDL
MAX1909_DLOV
MAX1909_DHIV
SRC
PDS
ACIN
DCIN
CSSP
CSSN
DHIV
PDL
LDO
DLOV
VCTL
GND/PKPRES#
ACOK
MODE
ICTL
DHI
DLO
PGND
THERMAL_PAD
CSIP
CSIN
BATT
CLS
REF
IINP
CCV
CCI
CCS
GND
MAX1909ETI+T
MAX1909_VCTL
MAX1909_MODE
MAX1909_ICTL
MAX1909_DHI
MAX1909_DLO
MAX1909_CLS
MAX1909_REF
MAX1909_IINP
MAX1909_CCV
MAX1909_CCI
MAX1909_CCS
MAX1909_CCV_1
MAX1909_PK#
PR391
10K_J
0402
PR10
56K_F
0402
PR11
100K_J
0402
PR367
10K_J
0402
PR13
56K_F
0402
PR392
NC_0_J
0402
PR20
15K_F
0402
PR21
200K_J
0402
PR369
15K_F
0402
PR23
22K_F
0402
PR393
0_J
0402
PR394
15K_F
0402
PR25
0_J
0402
PR28
20K_F
0402
PR29
7.15K_F
0402
PC34
1U_10V_K
0603_X5R
PC337
0.01U_25V_K_B
0402
PC338
0.01U_16V_K_B
0402
PC37
470P_50V_K_B
0402
PC377
1U_6.3V_M_B
0402
PQ10
PDTC144ET
PQ11
2N7002
PC356
NC_0.1U_16V_M_B
0402
BATT_PRS#
AC_OFF
ENCHG#
MAX1909_IINP_HW
ACIN
Change PR369 from 0Ω to 15KΩ for
set BATT_PRS# high level=3.24V for EC
PR7
33_J
0402
PC334
1U_10V_K
0603_X5R
PC335
1U_10V_K
0603_X5R
Place PC334 near
MAX1909 Pin 2
Place PC335 near MAX1909
Pin 21
PC24
10U_25V_M
1206_X5R
PC25
10U_25V_M
1206_X5R
PQ84B
AO4606
PQ84A
AO4606
PL6
15UH-100KHZ_2A_0.056R
SPD1004PT150M
PR14
0.015_F
2512
MAX1909_DHI&MAX1909_DLO
need to keep same length
Width DHI=40mils ,DLO=40mils
PC31
10U_25V_M
1206_X5R
PC32
10U_25V_M
1206_X5R
PC33
10U_25V_M
1206_X5R
PR339
1U_10V_K
0603_X5R
PR28
6.2K_F
0402
PR30
20K_F
0402
PR28&PR30_Set input current limit to 106.01W
MAX1909 reduce source current by decreasing the
charger current when the input current exceeds 106.01W
PD8
PACDN042Y3R
PD4
PESD15VS2UT
PD5
PACDN042Y3R
PD9
PACDN042Y3R
PL19
60R-100MHZ_1806
BCMS451616A600 8A
PL5
60R-100MHZ_1806
BCMS451616A600 8A
PCN2
BATTERY_7P
FOX_BP06077-B7312-7F
BATT_ID
DAT_SMB
CLK_SMB
BATT_PRS#
SYS_PRS#
PR18 330_J
PR19 330_J
BT+ 4
BATT_PRS_1
SYS_PRS_1
PC9 47P_50V_J_N
PC10 47P_50V_J_N
PC11 47P_50V_J_N
PC12 47P_50V_J_N
PC27 47P_50V_J_N
PC13 0.1U_25V_M_B
PTP41
PTP42
tpc32t_100
PD2
MMPZ5250BFPT
PD10
MMPZ5246BPT
PU20
PQ4
AME4318BJETB25Z
2PC4617G
PR377
20K_F
0402
PR363
10K_J
0402
PR320
120K_J
0402
PR365
10K_F
0402
PR379
1K_F
0402
PC40
0.22U_16V_K_B
0603
PQ94A
PQ94B
MUN5213DW1T1G
PC39
0.1U_50V_K_B
0603
AC_OFF_3# 73
PQ13
IRLML5103PbF
PR36
PRG18BB330MB1RB
PQ91A
PUMB2
PQ91B
PUMB2
PR321
200K_J
0402
PR324
200K_J
0402
PR322
100K_J
0402
PD11
MMVZ5235BPT
PD12
BAT54WAPT
PR326
0_J
0402
PR40
10K_F
0402
PQ12
PDTC144ET
PQ5
2N7002
PC44
NC_0.1U_25V_M_B
0603
PD40
BAS316PT
ALW_ON 44,57,68
MAIN_DC_SW_OFF#
DC_IN_MOS
DC_IN_G1
MAX1909_PDS
AC_OFF_3#
PQ1,PQ2,PQ3,PQ15 usage
SI4425BDY(Rds=10mΩ_typ,12mΩ_max@Vgs=10V,Id=11.4A)
or
AOS4407(Rds=11mΩ_typ,14mΩ_max@Vgs=-10V,Id=-10A)
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
Title
DCIN & Charger
Size
A3
Document Number
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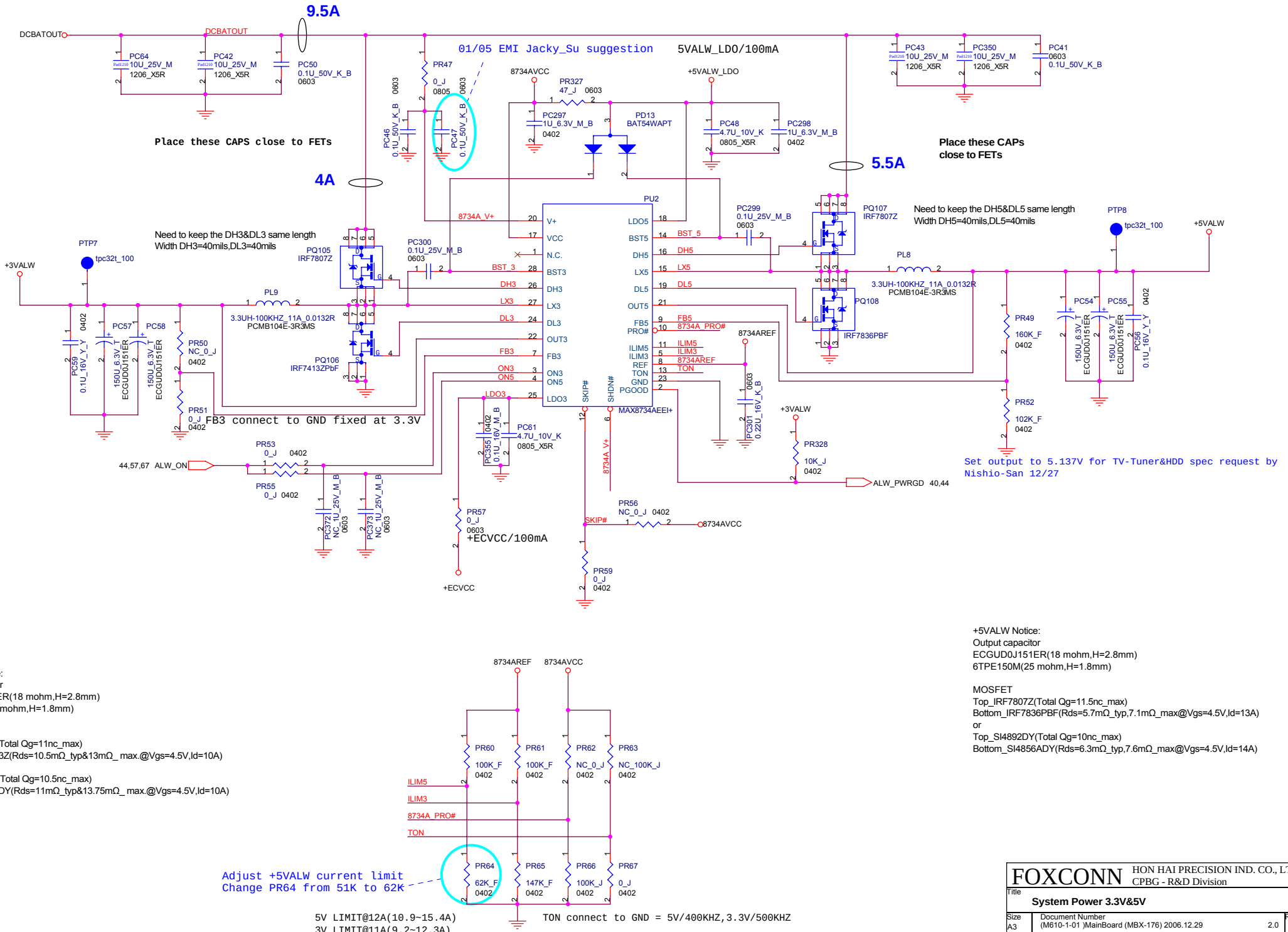

+3VALW Notice:
Output capacitor
ECGUD0J151ER(18 mohm,H=2.8mm)
6TPE150M(25 mohm,H=1.8mm)

MOSFET
Top_IRF7807Z(Total Qg=11nc_max)
Bottom_IRF7413Z(Rds=10.5mΩ_typ&13mΩ_ max.@Vgs=4.5V,Id=10A)
or
Top_SI4892DY(Total Qg=10.5nc_max)
Bottom_SI4392DY(Rds=11mΩ_typ&13.75mΩ_ max.@Vgs=4.5V,Id=10A)

+5VALW Notice:
Output capacitor
ECGUD0J151ER(18 mohm,H=2.8mm)
6TPE150M(25 mohm,H=1.8mm)

MOSFET
Top_IRF7807Z(Total Qg=11.5nc_max)
Bottom_IRF7836PBF(Rds=5.7mΩ_typ,7.1mΩ_max@Vgs=4.5V,Id=13A)
or
Top_SI4892DY(Total Qg=10nc_max)
Bottom_SI4856ADY(Rds=6.3mΩ_typ,7.6mΩ_max@Vgs=4.5V,Id=14A)

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title	System Power 3.3V&5V		
Size A3	Document Number (M610-1-01)MainBoard (MBX-176) 2006.12.29		Rev 2.0
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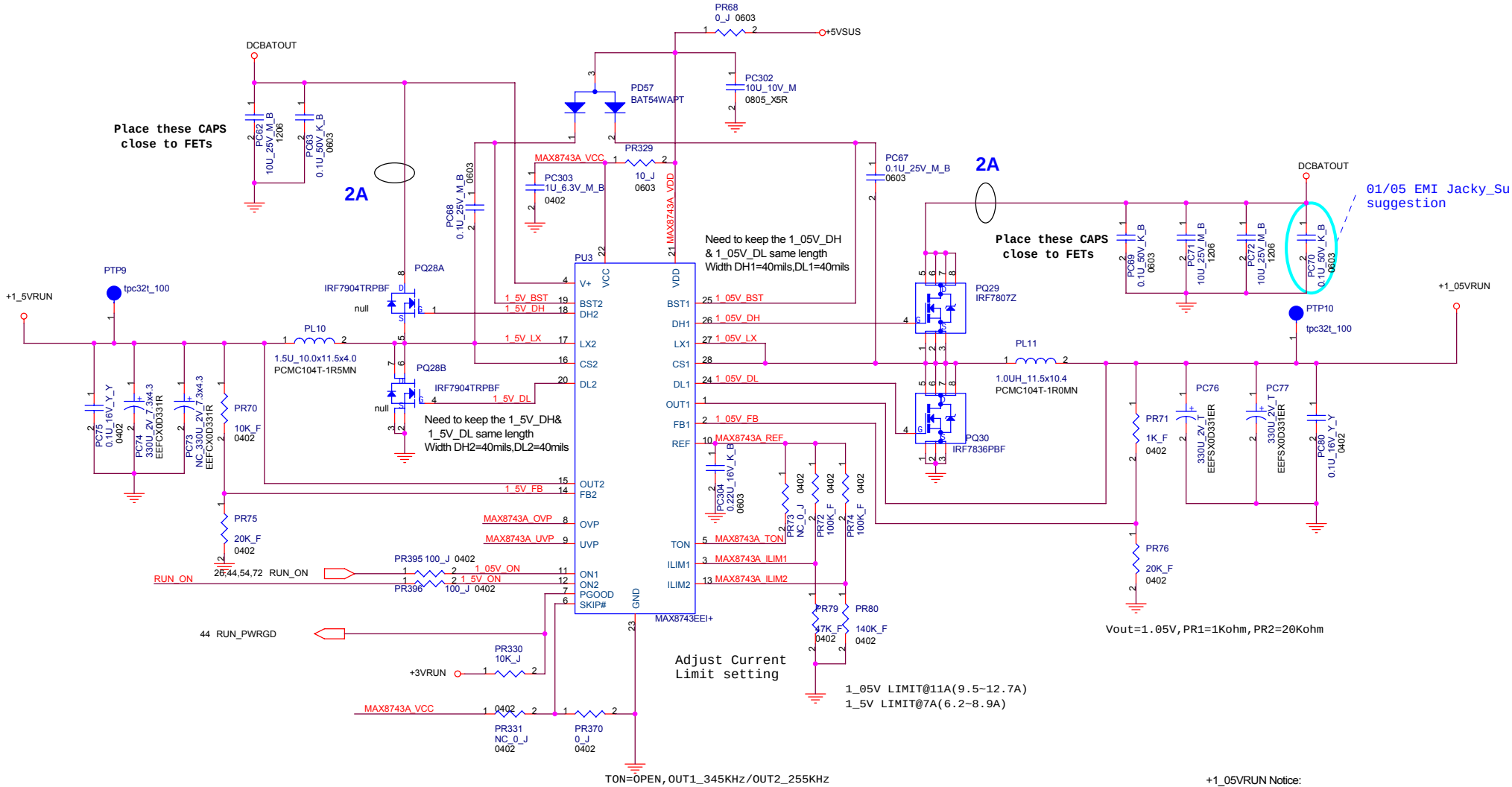

+1_5VRUN Notice:
Output capacitor
EEFCX0D331R(ESR=15 mohm,H=1.9mm,Arms=2.7A)
2R5TPE330MF(ESR=15 mohm,H=1.8mm,Arms=3.1A)

MOSFET(Top+Bottom)
IRF7902PBF(Low side Rds=14.3mΩ_typ,20.5mΩ_max@Vgs=4.5V,Id=7.2A)
Si4816DY(Low side Rds=15mΩ_typ,18.5mΩ_max@Vgs=4.5V,Id=8.6A)

+1_05VRUN Notice:
Output capacitor usage
EEFSX0D331ER(ESR=9mohm,H=1.9mm,Arms=3.0A)
2R5TPE330M9(ESR=9mohm,H=1.8mm,Arms=3.9A)

MOSFET
Top_IRF7807Z(Total Qg=11.5nc_max)
Bottom_IRF7836PBF(Rds=5.7mΩ_typ,7.1mΩ_max@Vgs=4.5V,Id=13A)
or
Top_SI4892DY(Total Qg=10nc_max)
Bottom_SI4856ADY(Rds=6.3mΩ_typ,7.6mΩ_max@Vgs=4.5V,Id=14A)

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: 1.5V/1.05V

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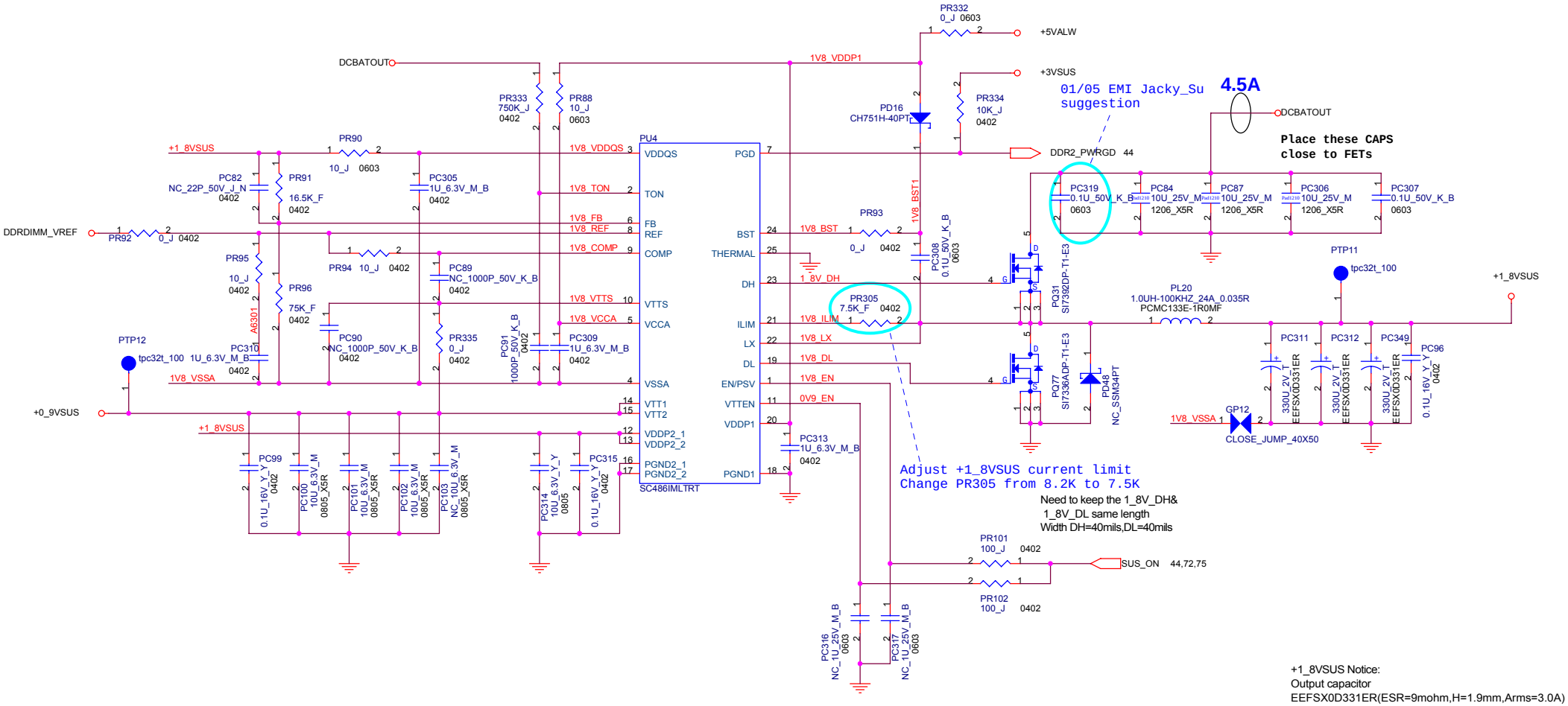

+1_8VSUS Notice:
Output capacitor
EEFSX0D331ER(ESR=9mohm,H=1.9mm,Arms=3.0A)
2R5TPE330M9(ESR=9mohm,H=1.8mm,Arms=3.9A)

MOSFET
Top_SI7392DP(Total Qg=15nc_max)
Bottom_SI7336ADP(Rds=3.1mΩ_typ,4.0mΩ_max@19A)
or
Top_NTMFS4707N(Total Qg=15nc_max)
Bottom_NTMFS4119N(Rds=3.1mΩ_typ,4.8mΩ_max@25A)

1_8V LIMIT@22A(20.2~25A)

FOXCONN HON HAI PRECISION IND. CO., LTD.
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Title: DDRII 1.8V/0.9V

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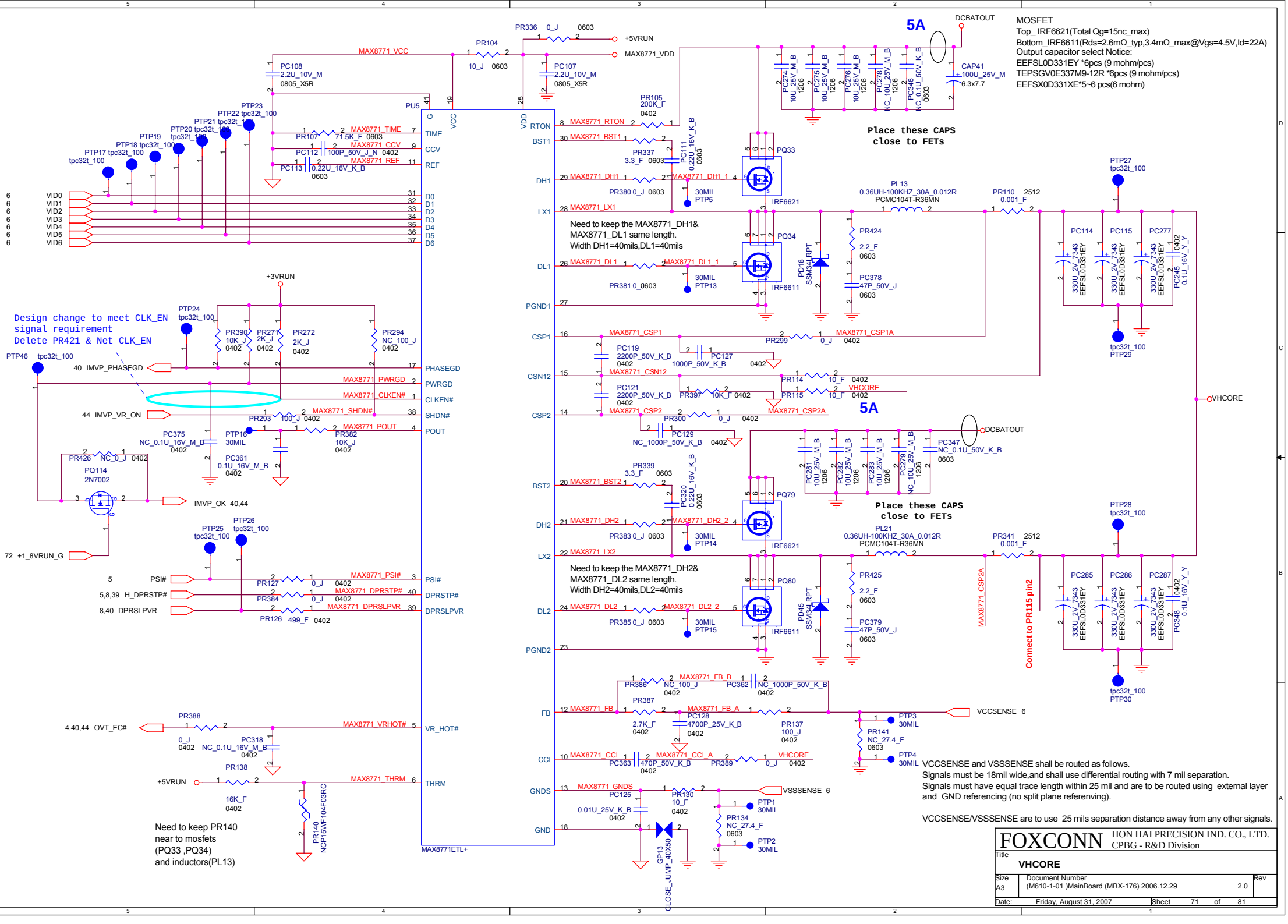
MOSFET
Top_ IRF6621(Total Qg=15nc_max)
Bottom_IRF6611(Rds=2.6mΩ_typ,3.4mΩ_max@Vgs=4.5V,Id=22A)
Output capacitor select Notice:
EEFSL0D331EY *6pcs (9 mohm/pcs)
TEPSGV0E337M9-12R *6pcs (9 mohm/pcs)
EEFSX0D331XE*5~6 pcs(6 mohm)
5A
DCBATOUT
Place these CAPS close to FETs
Need to keep the MAX8771_DH1& MAX8771_DL1 same length. Width DH1=40mils,DL1=40mils
Need to keep the MAX8771_DH2& MAX8771_DL2 same length. Width DH2=40mils,DL2=40mils
Design change to meet CLK_EN signal requirement Delete PR421 & Net CLK_EN
Connect to PR115 pin2
Need to keep PR140 near to mosfets (PQ33 ,PQ34) and inductors(PL13)
VCCSENSE and VSSSENSE shall be routed as follows.
Signals must be 18mil wide,and shall use differential routing with 7 mil separation.
Signals must have equal trace length within 25 mil and are to be routed using external layer and GND referencing (no split plane referenving).
VCCSENSE/VSSSENSE are to use 25 mils separation distance away from any other signals.
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
Title
VHCORE
Size A3
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PQ50
SI4800BDY(Rds=45mΩ_max@Vgs=3V,Id=9A)
or
IRF7402Z(Rds=50mΩ_max@Vgs=2.7V,Id=3.5A)

4A

PQ53
IRF7836PBF(Rds=5.7mΩ_typ,7.1mΩ_max@Vgs=4.5V,Id=13A)
or
SI4856ADY(Rds=6.3mΩ_typ,7.6mΩ_max@Vgs=4.5V,Id=14A)

9A

PQ97
IRF7836PBF(Rds=5.7mΩ_typ,7.1mΩ_max@Vgs=4.5V,Id=13A)
or
SI4856ADY(Rds=6.3mΩ_typ,7.6mΩ_max@Vgs=4.5V,Id=14A)

7A

PQ112
SI4800BDY(Rds=45mΩ_max@Vgs=3V,Id=9A)
or
IRF7402Z(Rds=50mΩ_max@Vgs=2.7V,Id=3.5A)

0.3A

+5VRUN_TV for TV Tuner ,Spec=5.2V_Min

PQ99
IRF7836PBF(Rds=5.7mΩ_typ,7.1mΩ_max@Vgs=4.5V,Id=13A)
or
SI4856ADY(Rds=6.3mΩ_typ,7.6mΩ_max@Vgs=4.5V,Id=14A)

8.5A

PQ7
SI4800BDY(Rds=30mΩ_max@Vgs=4.5V,Id=7A)
or
IRF7402Z(Rds=35mΩ_max@Vgs=4.5V,Id=4.1A)

1.5A

30mA

for load switch

Discharge circuit for power-off

11/16 PC159
shortage issue
Change X5R (1C-2B20474-M000)
to X7R (1C-2B20474-K000)

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title: Other power plan			
Size: A3	Document Number: (M610-1-01)MainBoard (MBX-176) 2006.12.29		Rev: 2.0
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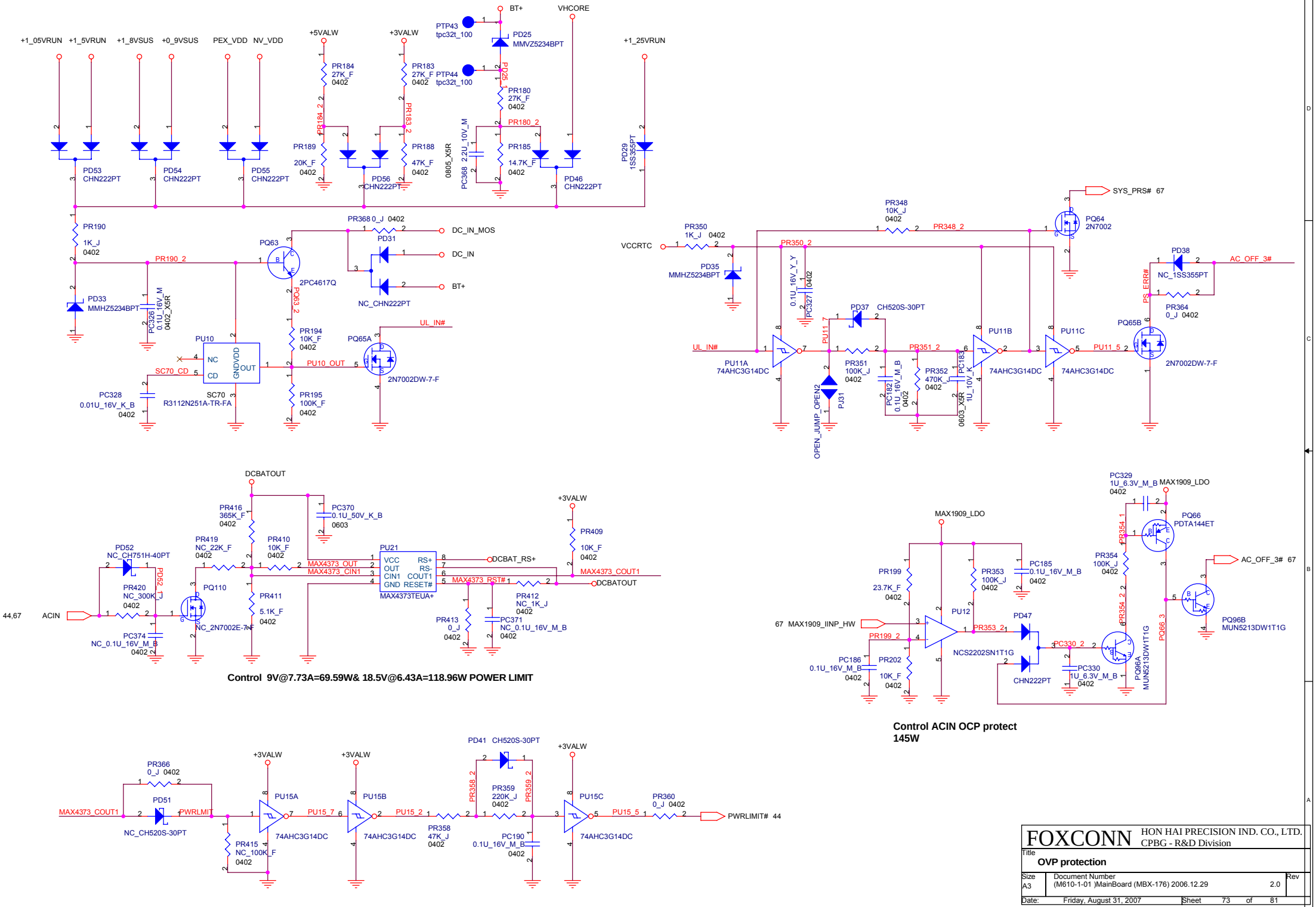
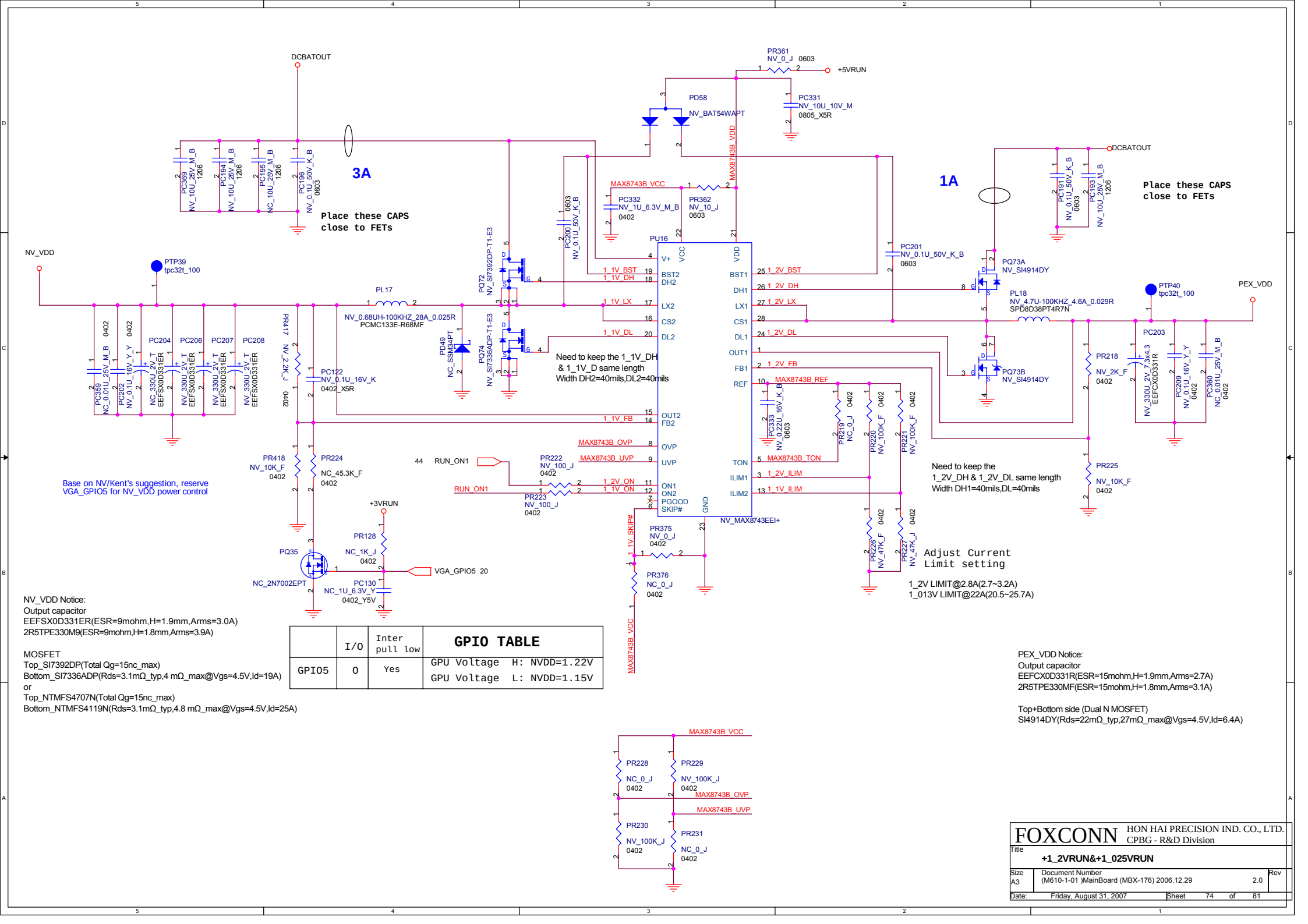


FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title: OVP protection			
Size: A3	Document Number: (M610-1-01)MainBoard (MBX-176) 2006.12.29		Rev: 2.0
Date: Friday, August 31, 2007	Sheet 73 of 81		



	I/O	Inter pull low	GPIO TABLE
GPIO5	O	Yes	GPU Voltage H: NVDD=1.22V GPU Voltage L: NVDD=1.15V

NV_VDD Notice:
Output capacitor
EEFSX0D331ER(ESR=9mohm,H=1.9mm,Arms=3.0A)
2R5TPE330M9(ESR=9mohm,H=1.8mm,Arms=3.9A)

MOSFET
Top_SI7392DP(Total Qg=15nc_max)
Bottom_SI7336ADP(Rds=3.1mΩ_typ,4 mΩ_max@Vgs=4.5V,Id=19A)
or
Top_NTMFS4707N(Total Qg=15nc_max)
Bottom_NTMFS4119N(Rds=3.1mΩ_typ,4.8 mΩ_max@Vgs=4.5V,Id=25A)

PEX_VDD Notice:
Output capacitor
EEFCX0D331R(ESR=15mohm,H=1.9mm,Arms=2.7A)
2R5TPE330MF(ESR=15mohm,H=1.8mm,Arms=3.1A)

Top+Bottom side (Dual N MOSFET)
SI4914DY(Rds=22mΩ_typ,27mΩ_max@Vgs=4.5V,Id=6.4A)

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: +1_2VRUN&+1_025VRUN

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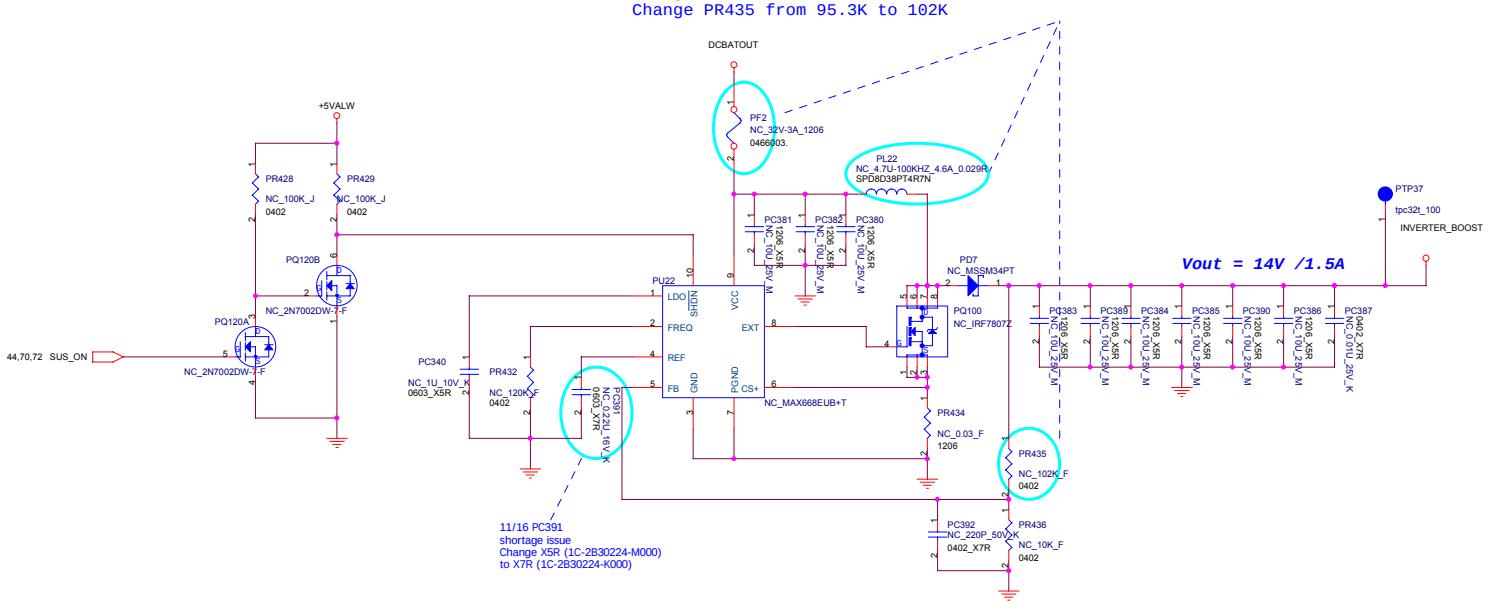
Boost cirsuit design change.
Add PF2 (32V-3A_1206) fuse for boost circuit,
Change PL22 from 8UH-100KHZ_2.5A_0.07R to 4.7U-100KHZ_4.6A_0.029R.
Change PR435 from 95.3K to 102K



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: STEP_UP		
Size: Custom	Document Number: (M610-1-01)MainBoard (MBX-176) 2006.12.29	Rev: 2.0
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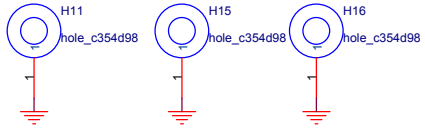
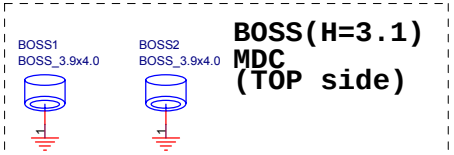
HOLE

Type 1

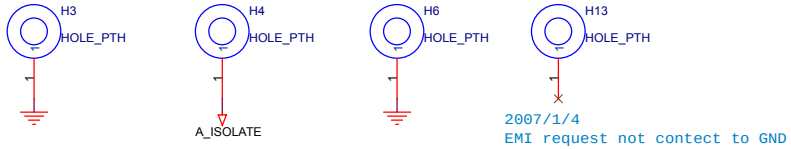


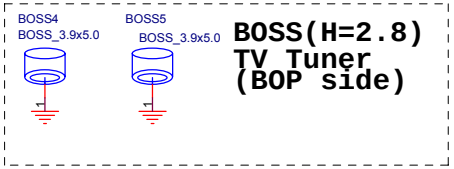
Type 2



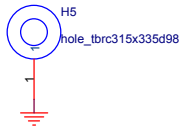
Type 3

Type 4

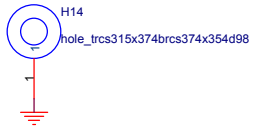




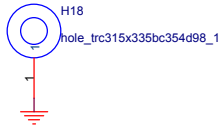
Type 5



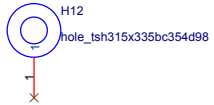
Type 6



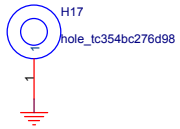
Type 7



Type 8

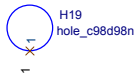


Type 9



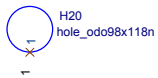
Type CPU

Type NPTH Guide (spherical)HOLD

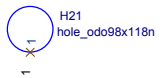


close H1

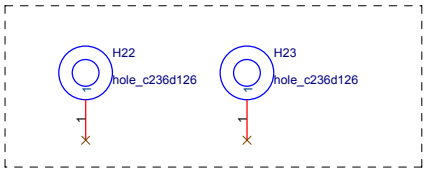
Type NPTH Guide (oval-shaped)HOLD



close H6



close H17



VRAM Thermal Solution

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	HOLE & BOSS	
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M612 DVT2 Change Circuit

1.(Page 17~32) 07/08/17 Modify Page from 17 to 32 for 8pcs Vram.(512MB:16MBx32bx8pcs)

2. (Page 4) 07/08/29 For support Penryn-CPU, change U2-CPU Thermal Senser from GMT to SMSC.

3. (Page 44) 07/08/29 Change System ID to M612 Type

4. (Page 76) 07/08/29 Add H22,H23 for VRAM thermal solution

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: *History(EVT to MP)*		
Size: A3	Document Number: (M610-1-01)MainBoard (MBX-176) 2007.1.4	Rev: 2.0
Date: Friday, August 31, 2007	Sheet 77 of 81	