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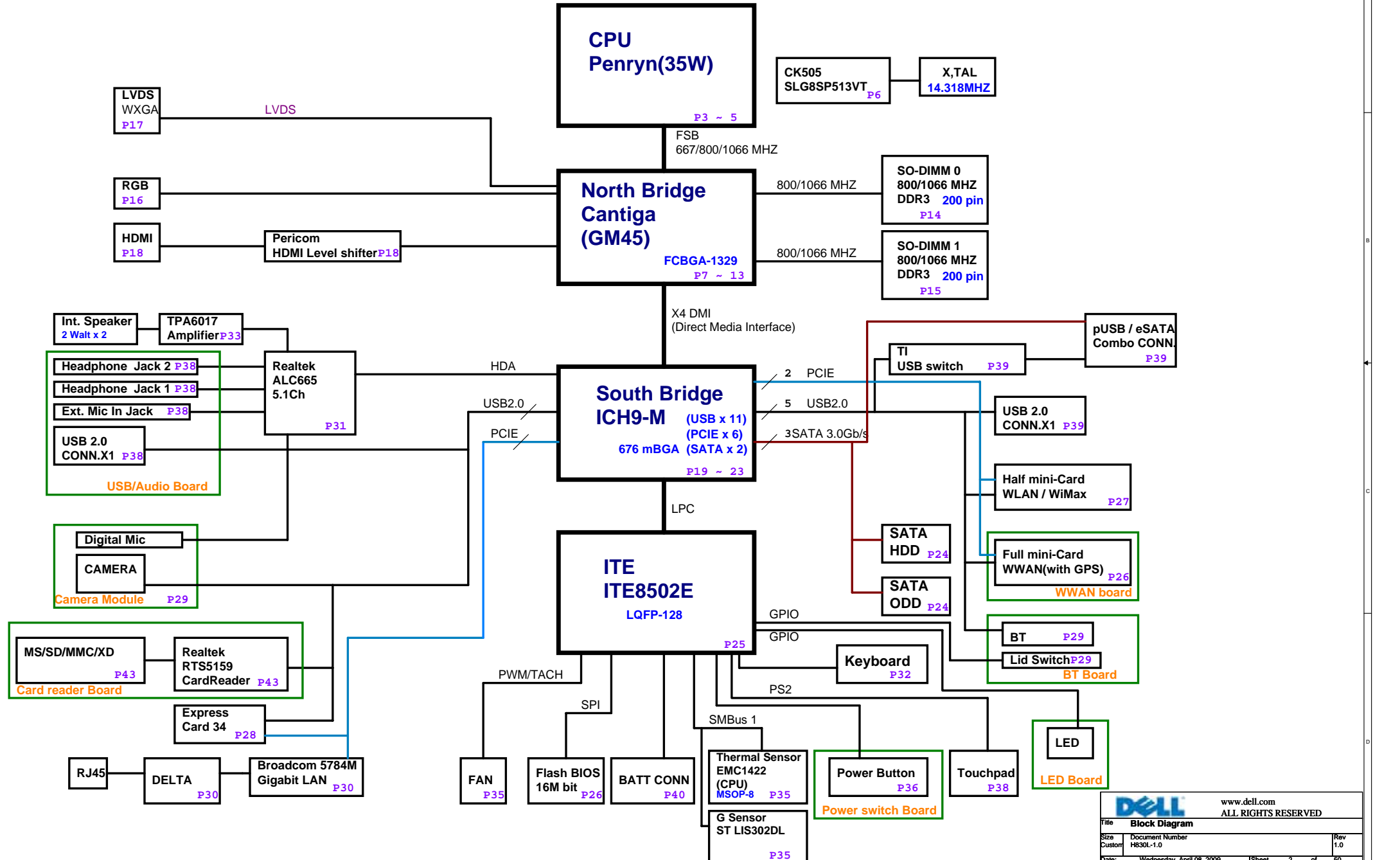
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**Project Code & Schematics Subject:** H830-L Main Board 6L

PCB P/N:	1P-0093200-6010 (NANYA)
	1P-0093J00-6010 (IRIS)
	1P-0093500-6010 (HANNSTAR)
BT DB P/N:	1P-1093200-6010 (NANYA)
	1P-1093J03-6010 (IRIS)
	1P-1093503-6010 (HANNSTAR)
LED DB P/N:	1P-1093201-6010 (NANYA)
	1P-1093J01-6010 (IRIS)
	1P-1093502-6010 (HANNSTAR)
P/B DB P/N:	1P-1093202-6010 (NANYA)
	1P-1093J00-6010 (IRIS)
	1P-1093501-6010 (HANNSTAR)

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# H830(Montevina UMA)



7 H\_AA[3..35]

7 H\_ADSTB#0

7 H\_REQ#4[0..4]

7 H\_ADSTB#1

20 H\_A20M#

20 H\_FERR#

20 H\_IGNNE#

20 H\_STPCLK#

20 H\_INTR

20 H\_NMI

20 H\_SMI#

- TP22 tpc20 -1 TP CPU RSVD01 M4
- TP25 tpc20 -1 TP CPU RSVD02 N5
- TP13 tpc20 -1 TP CPU RSVD03 T2
- TP18 tpc20 -1 TP CPU RSVD04 V3
- TP5 tpc20 -1 TP CPU RSVD05 B2
- TP21 tpc20 -1 CPU TEST7 C3
- TP12 tpc20 -1 TP CPU RSVD07 D2
- TP31 tpc20 -1 TP CPU RSVD08 D22
- TP17 tpc20 -1 TP CPU RSVD09 D3
- TP26 tpc20 -1 TP CPU RSVD10 F6

CPU SOCKET\_478P  
FOX\_P24782A-274M-01

- H\_A#3 J4
- H\_A#4 L5
- H\_A#5 L4
- H\_A#6 K5
- H\_A#7 M3
- H\_A#8 N2
- H\_A#9 J1
- H\_A#10 N3
- H\_A#11 P5
- H\_A#12 P2
- H\_A#13 L2
- H\_A#14 P4
- H\_A#15 P1
- H\_A#16 R1

- H\_REQ#0 K3
- H\_REQ#1 H2
- H\_REQ#2 K2
- H\_REQ#3 J3
- H\_REQ#4 L1

- H\_A#17 Y2
- H\_A#18 U5
- H\_A#19 R3
- H\_A#20 W6
- H\_A#21 U4
- H\_A#22 Y5
- H\_A#23 U1
- H\_A#24 R4
- H\_A#25 T5
- H\_A#26 T3
- H\_A#27 W2
- H\_A#28 W5
- H\_A#29 Y4
- H\_A#30 U2
- H\_A#31 V4
- H\_A#32 W3
- H\_A#33 AA4
- H\_A#34 AB2
- H\_A#35 AA3

- A20M# A6
- FERR# A5
- IGNNE# C4

- H\_STPCLK# D5
- LINT0 C6
- LINT1 B4
- SMI# A3

- RSVD[01] M4
- RSVD[02] N5
- RSVD[03] T2
- RSVD[04] V3
- RSVD[05] B2
- RSVD[06] C3
- RSVD[07] D2
- RSVD[08] D22
- RSVD[09] D3
- RSVD[10] F6

ADDR GROUP 0

CONTROL

ADDR GROUP 1  
STVNS/TP/JL/CLK

THERMAL

H CLK

RESERVED

- ADS# H1
- BNR# E2
- BPRI# G5
- DEFER# H5
- DRDY# F21
- DBSY# E1
- BR0# F1
- IERR# D20
- INIT# B3
- LOCK# H4
- RESET# C1
- RS[0]# E3
- RS[1]# F4
- RS[2]# G3
- TRDY# G2
- HIT# G6
- HITM# E4

- H\_IERR#
- H\_LOCK# 7
- H\_CPURST# 7,26
- H\_RS#[2..0] 7
- H\_TRDY# 7
- H\_HIT# 7
- H\_HITM# 7

- AD4 XDP\_BPM#0 tpc20 TP24
- AD3 XDP\_BPM#1 tpc20 TP20
- AD1 XDP\_BPM#2 ICT\_TP
- AC4 XDP\_BPM#3 tpc20 TP23
- AC2 XDP\_BPM#4 tpc20 TP14
- AC1 XDP\_BPM#5 tpc20 TP14
- PREQ# AC5
- TCK AA6
- TDI AB3
- XDP\_TDO AB3
- XDP\_TMS AB5
- XDP\_TRST# AB6
- DBR# C20

- PROCHOT# D21
- THERMDA A24
- THERMDC B25
- THERMTRIP# C7
- CLK\_CPU\_BCLK 6
- CLK\_CPU\_BCLK# 6

- A22
- A21

tpc20 TP10

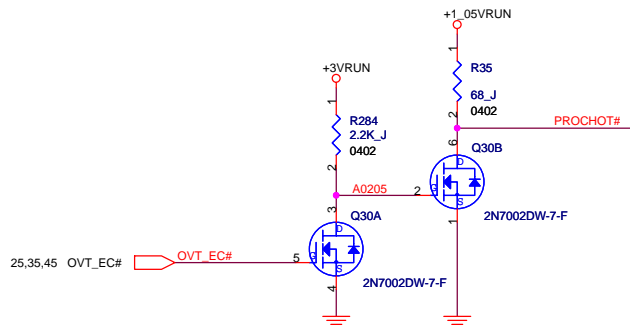
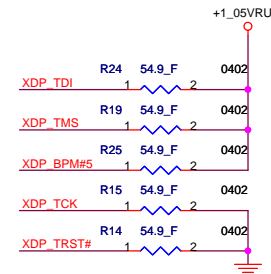
R34  
56\_J  
0402

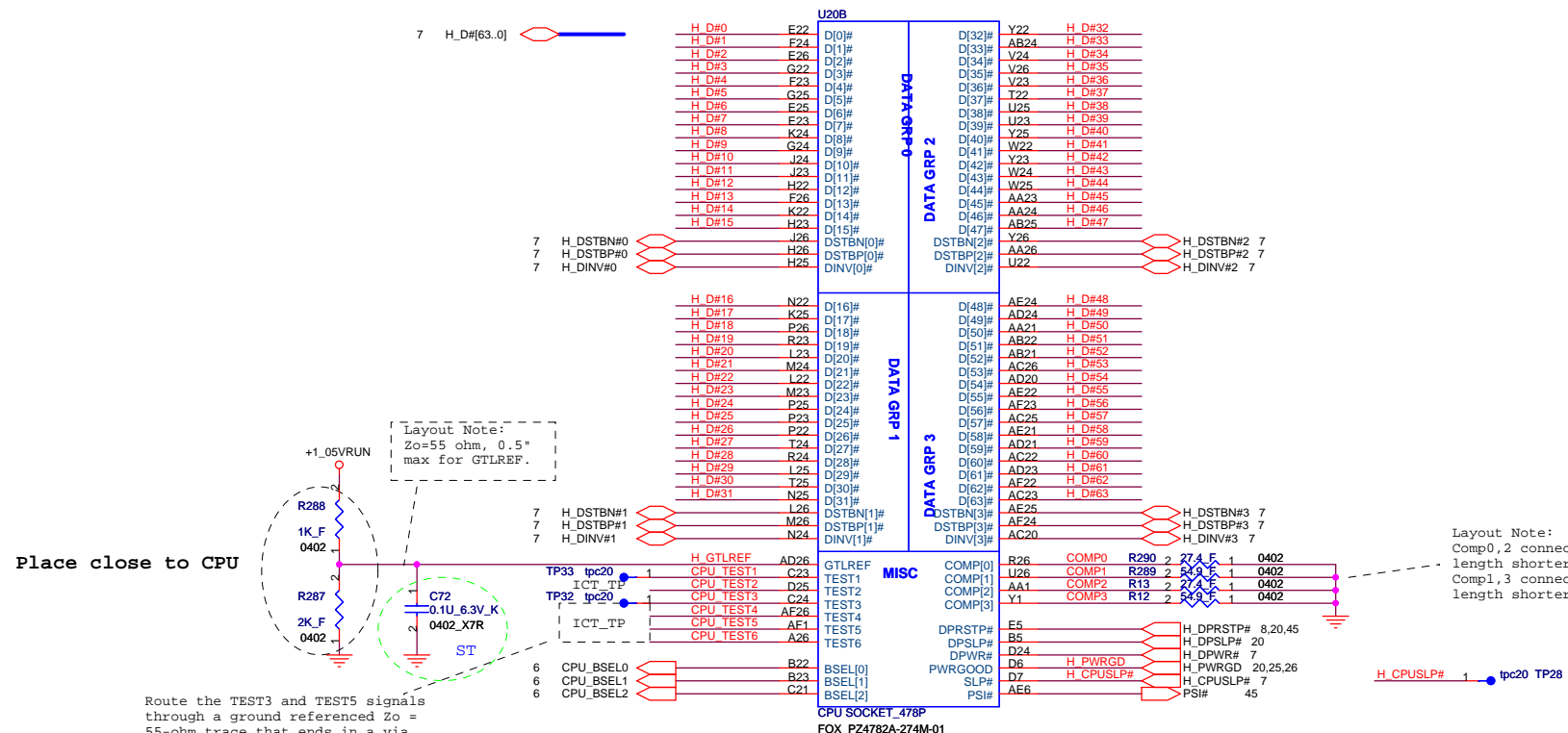
H\_ADS# 7  
H\_BNR# 7  
H\_BPRI# 7  
H\_DEFER# 7  
H\_DRDY# 7  
H\_DBSY# 7  
H\_BREQ#0 7

H\_LOCK# 7  
H\_CPURST# 7,26  
H\_RS#[2..0] 7  
H\_TRDY# 7  
H\_HIT# 7  
H\_HITM# 7

tpc20 TP24  
tpc20 TP20  
tpc20 TP23  
tpc20 TP14  
tpc20 TP14

CLK\_CPU\_BCLK 6  
CLK\_CPU\_BCLK# 6





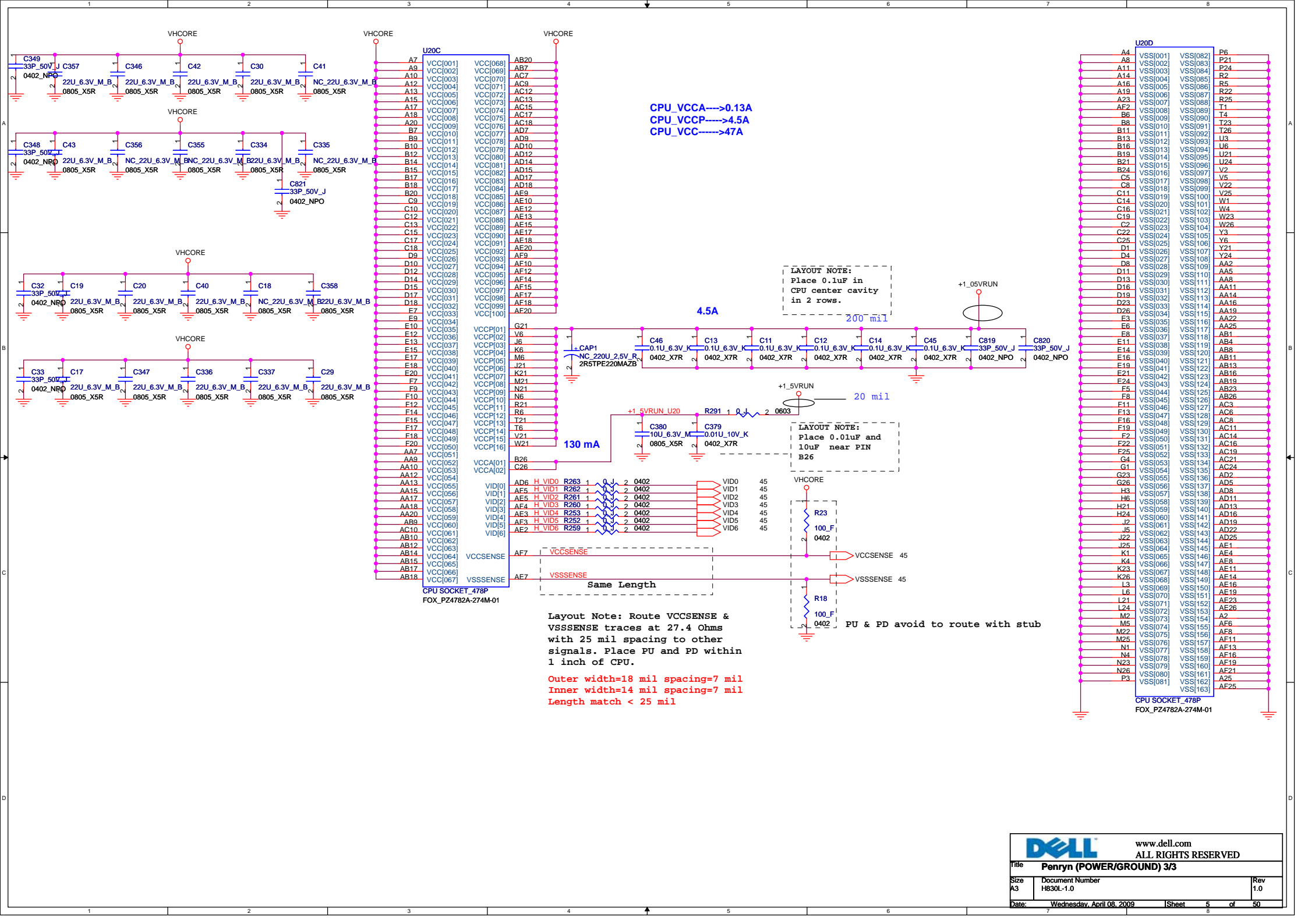
7 H\_D#[63..0]

Layout Note:  
Zo=55 ohm, 0.5"  
max for GTLREF.

Layout Note:  
Comp0,2 connect with Zo=27.4 ohm, make trace  
length shorter then 0.5". Width=18mil(MS)  
Comp1,3 connect with Zo=55 ohm, make trace  
length shorter then 0.5". Width=5mil(MS)

Place close to CPU

Route the TEST3 and TEST5 signals  
through a ground referenced Zo =  
55-ohm trace that ends in a via  
that is near a GND via and is  
accessible through an oscilloscope  
connection. TEST4 and TEST6 and  
TEST7 pins can be left NC.



CPU\_VCCA---->0.13A  
 CPU\_VCCP---->4.5A  
 CPU\_VCC---->47A

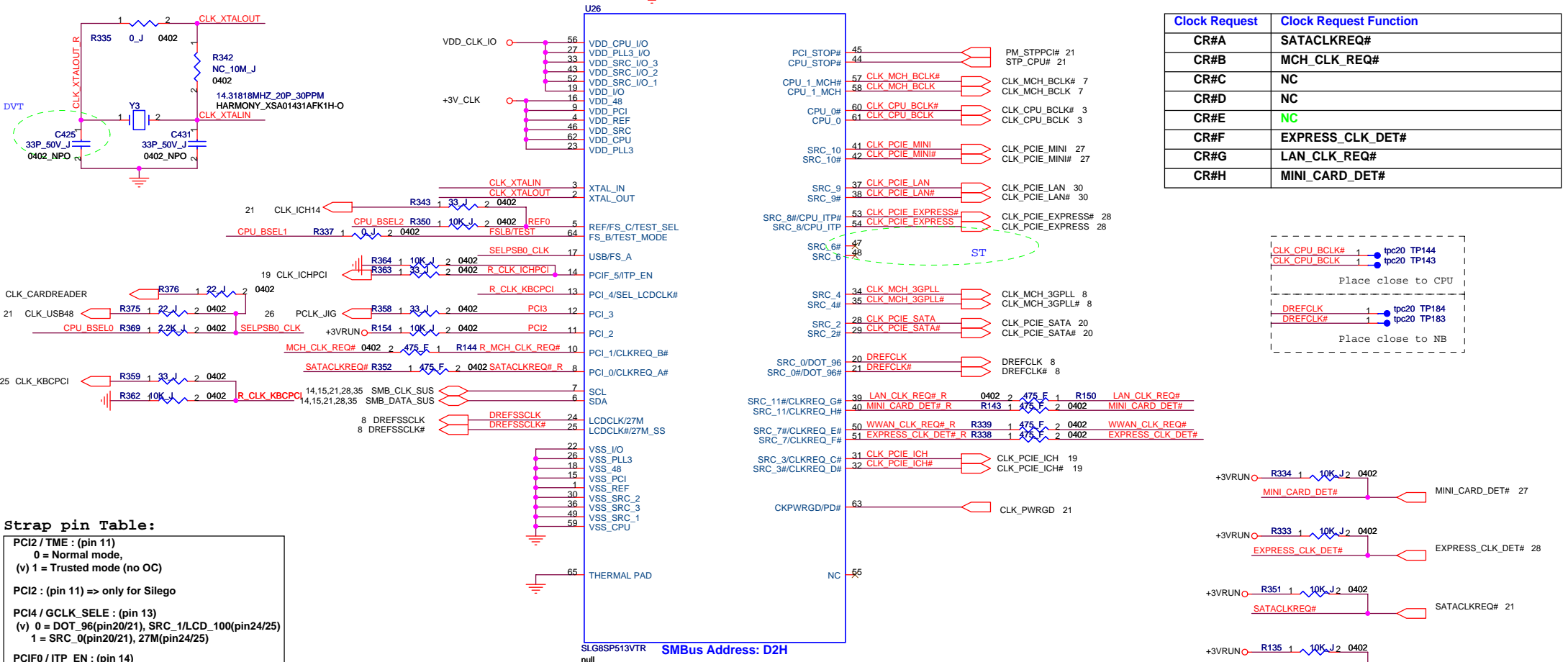
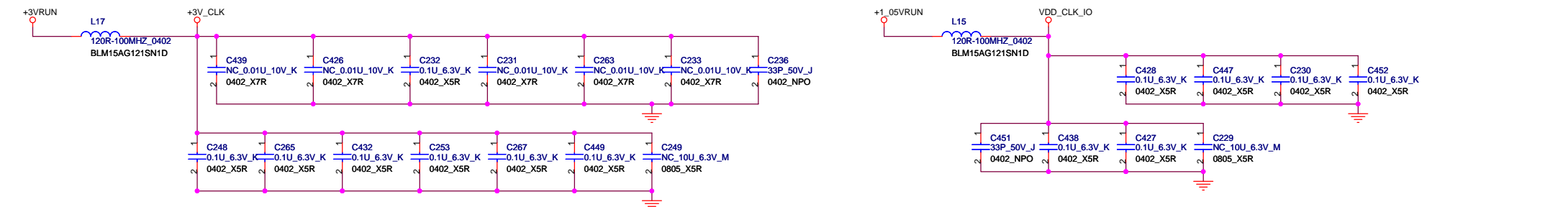
LAYOUT NOTE:  
 Place 0.1uF in  
 CPU center cavity  
 in 2 rows.

LAYOUT NOTE:  
 Place 0.01uF and  
 10uF near PIN  
 B26

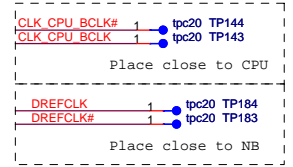
Layout Note: Route VCCSENSE &  
 VSSSENSE traces at 27.4 Ohms  
 with 25 mil spacing to other  
 signals. Place PU and PD within  
 1 inch of CPU.

Outer width=18 mil spacing=7 mil  
 Inner width=14 mil spacing=7 mil  
 Length match < 25 mil

PU & PD avoid to route with stub



Clock Request	Clock Request Function
CR#A	SATACLKREQ#
CR#B	MCH_CLK_REQ#
CR#C	NC
CR#D	NC
CR#E	NC
CR#F	EXPRESS_CLK_DET#
CR#G	LAN_CLK_REQ#
CR#H	MINI_CARD_DET#



**Strap pin Table:**

PCI2 / TME : (pin 11)  
 0 = Normal mode,  
 (v) 1 = Trusted mode (no OC)

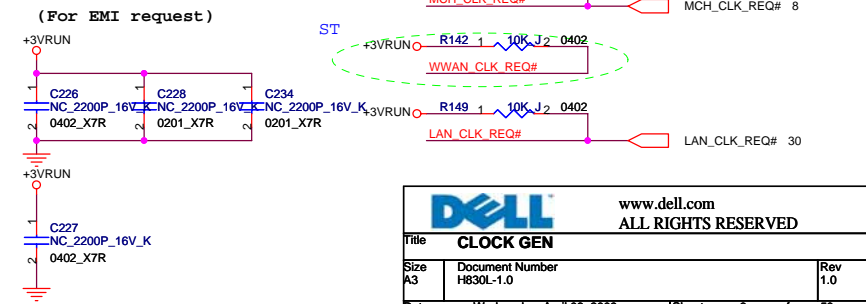
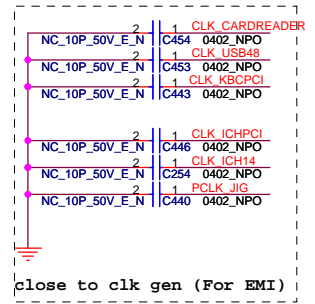
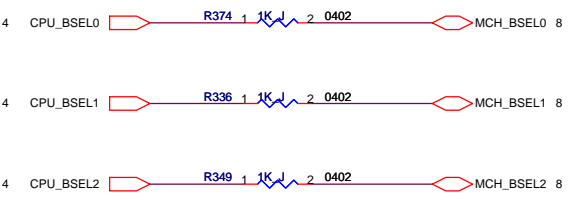
PCI2 : (pin 11) => only for Silago

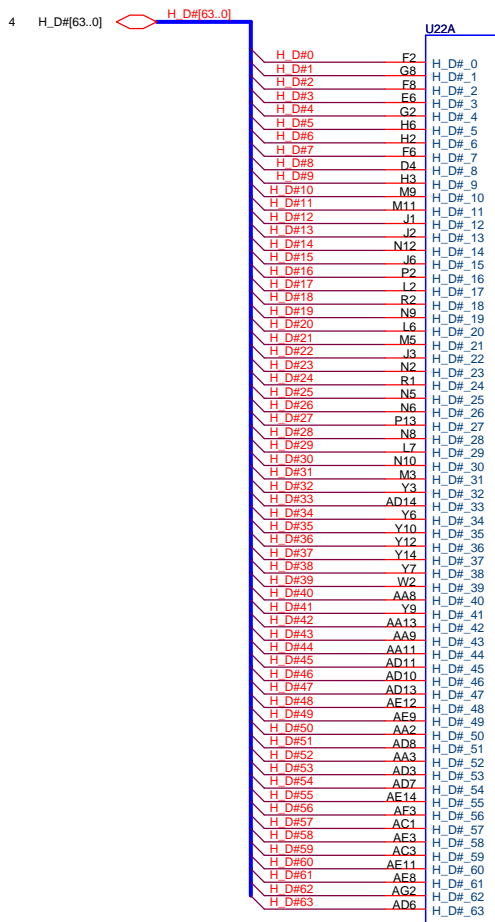
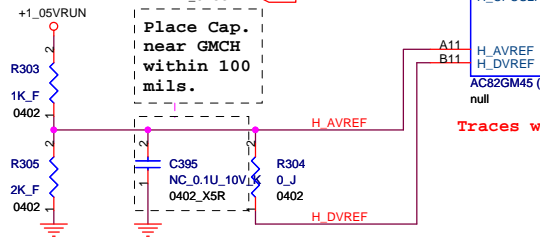
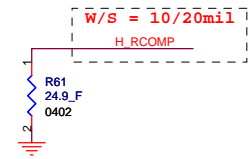
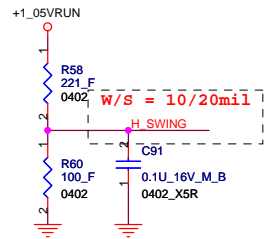
PCI4 / GCLK\_SELE : (pin 13)  
 (v) 0 = DOT\_96(pin20/21), SRC\_1/LCD\_100(pin24/25)  
 1 = SRC\_0(pin20/21), 27M(pin24/25)

PCIF0 / ITP\_EN : (pin 14)  
 (v) 0 = SRC\_8  
 1 = CPU2\_ITP

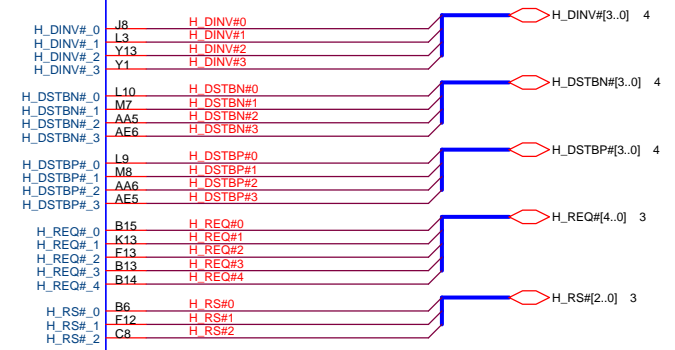
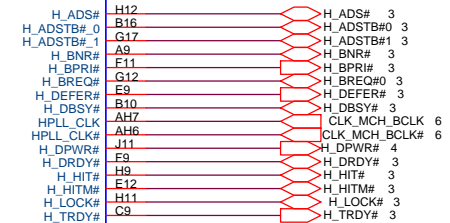
**FSB Frequency Table:**

FSLC	FSLB	FSLA	CPU SRC	PCI
0	0	0	266.66	100
0	0	1	133.33	100
0	1	0	200	100
0	1	1	166.66	100
1	0	0	333.33	100
1	0	1	100	100
1	1	0	400	100





HOST



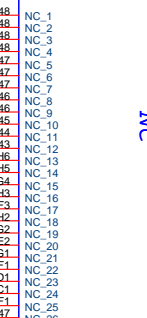
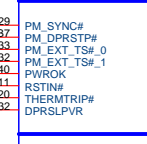
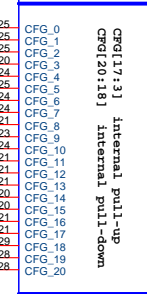
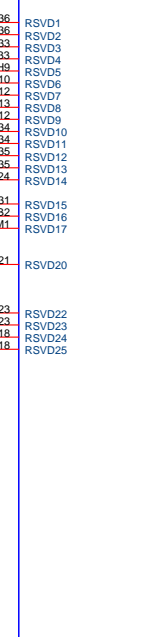
AC82GM45 (SLB94)

Traces width 10 mils.

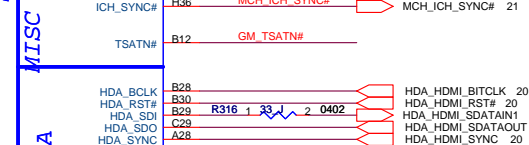
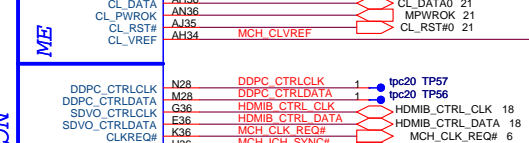
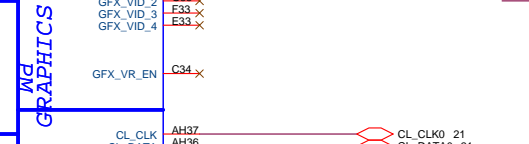
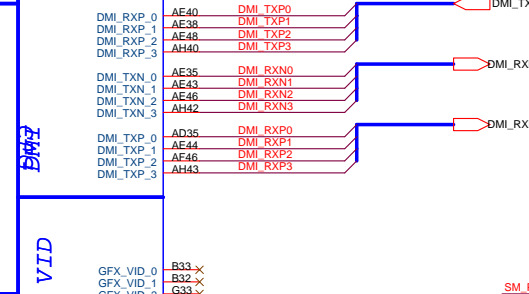
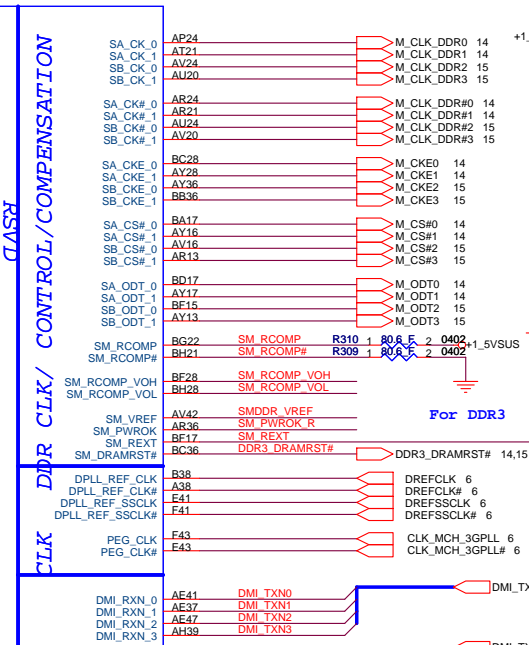


MCH_CFG_0-2 FSB Frequency	000 = FSB1066 ; 010 = FSB800 ; 011 = FSB667 ; Others = Reserved
MCH_CFG_3-4	Reserved
MCH_CFG_5 DMI X2 Select	Low = DMI X2 High = DMI X4 (Default)
MCH_CFG_6 ITPM Host Interface	Low = The ITPM Host Interface is enabled2 High = The ITPM Host Interface is disabled (default)
MCH_CFG_7 Intel Management Engine Crypto Strap	Low = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel Management Engine Crypto TLS cipher suite with confidentiality (default)
MCH_CFG_8	Reserved
MCH_CFG_9 PCIe Graphics Lane	Low = Reverse Lane High = Normal operation (default)
MCH_CFG_10 PCIe Loopback enable	Low = Enabled3 High = Disabled (default)
MCH_CFG_11	Reserved
MCH_CFG_12 ALLZ	Low = ALLZ mode enabled3 High = Disabled (default)
MCH_CFG_13 XOR	Low = XOR mode enabled3 High = Disabled (default)
MCH_CFG_14-15	Reserved
MCH_CFG_16 FSB Dynamic ODT	Low = Dynamic ODT disabled High = Dynamic ODT enabled (default)
MCH_CFG_17-18	Reserved
MCH_CFG_19 DMI Lane Reversal	Low = Normal operation (Default): Lane Numbered in Order High = Reverse Lanes DMI x4 mode [(G)MCH->ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [(G)MCH->ICH]: (3->0, 2->1)
MCH_CFG_20 Digital Display Port (SDVO/DP/iHDMI) or Concurrent with PCIe	Low = Only digital display port (SDVO/DP/iHDMI) or PCIe is operational (default) High = Digital display port (SDVO/DP/iHDMI) and PCIe are operating simultaneously via the PEG port

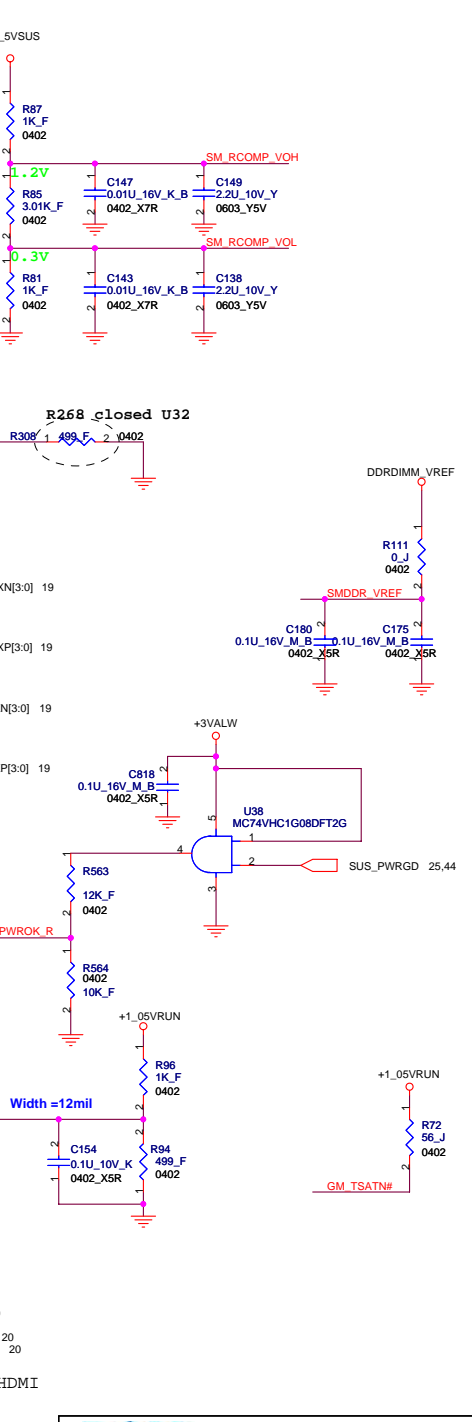
U22B



AC82GM45 (SLB94)



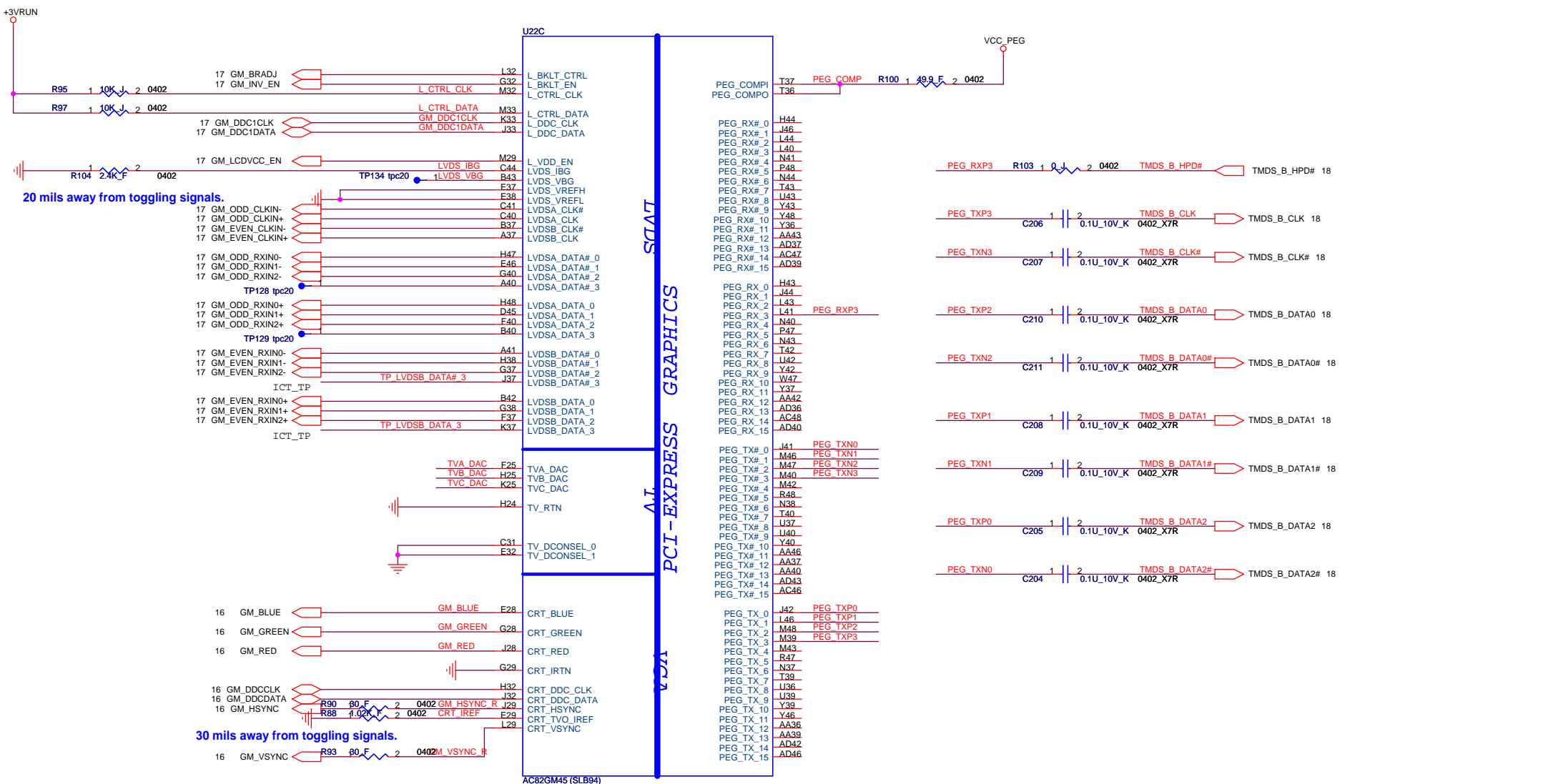
For Cantiga Internal HDMI



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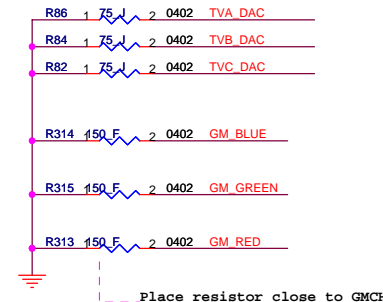
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<b>Size</b> Custom	<b>Date</b> Friday, April 10, 2009	<b>Sheet</b> 8 of 50	

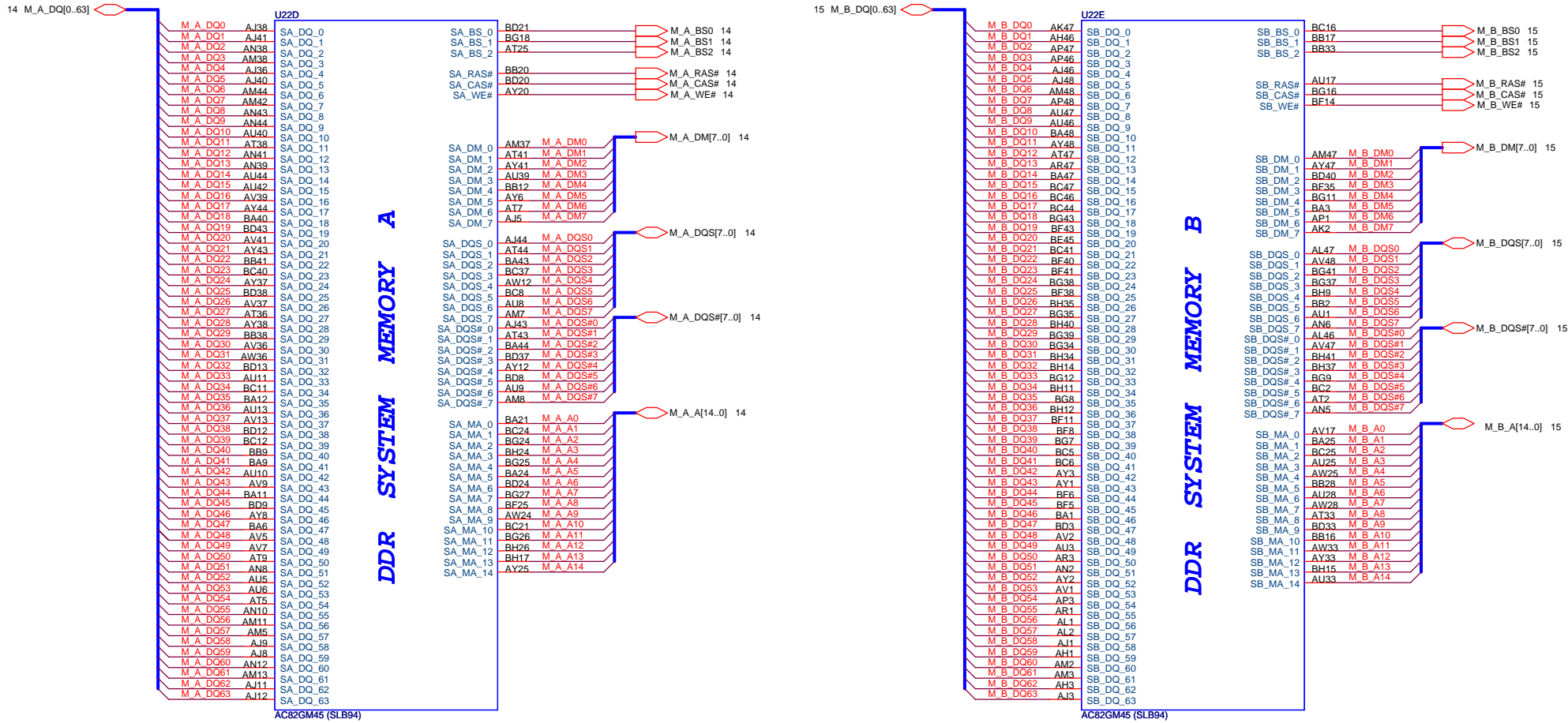


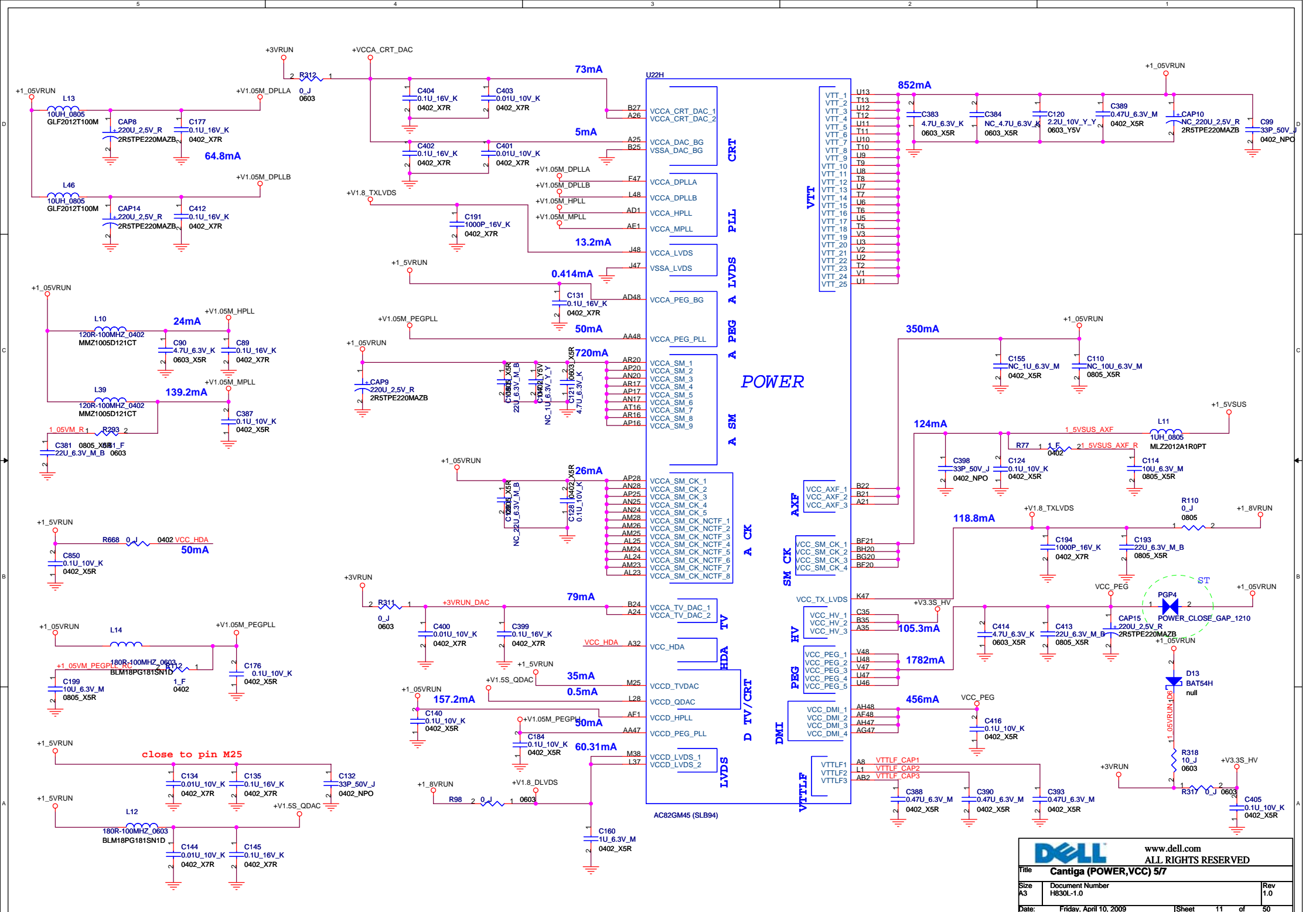


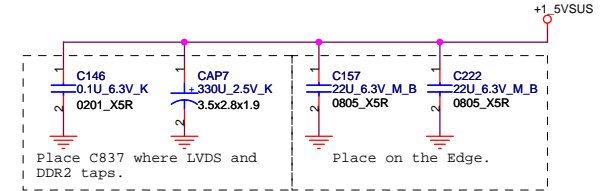
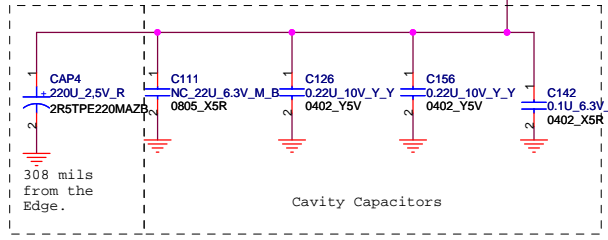
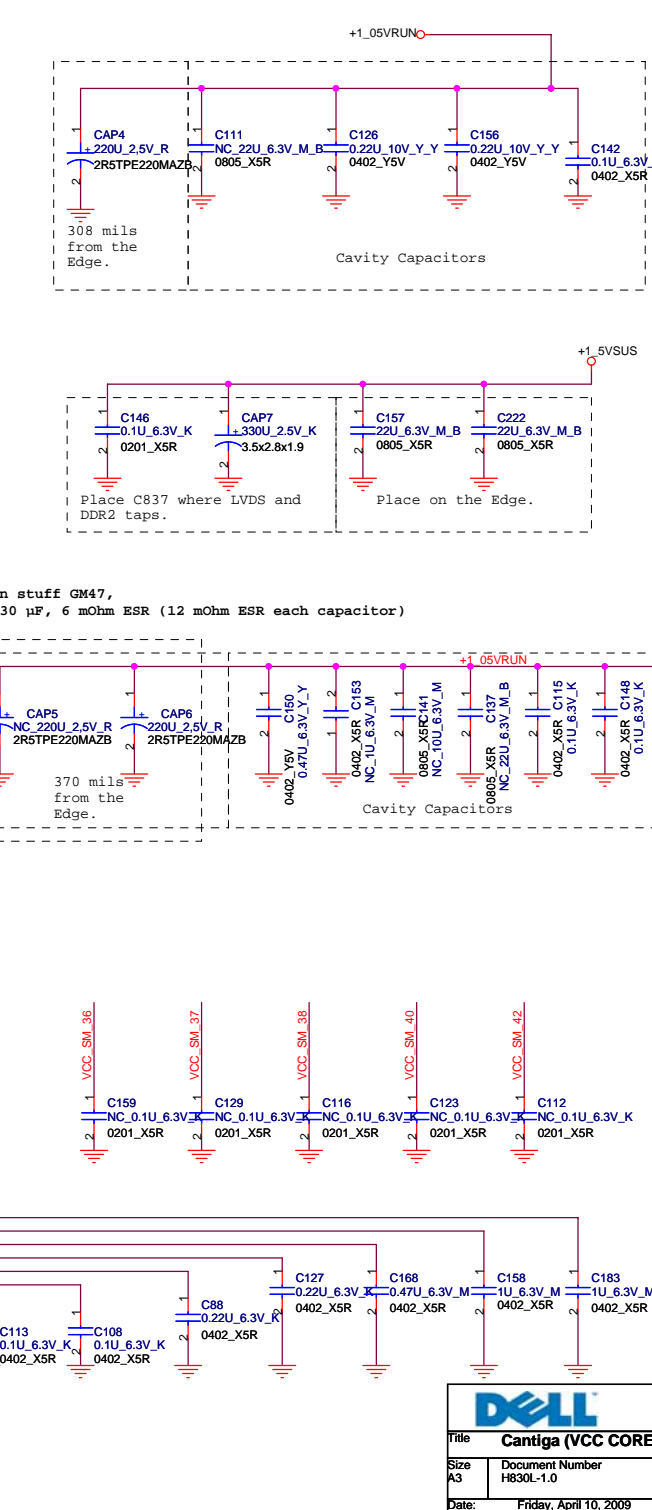
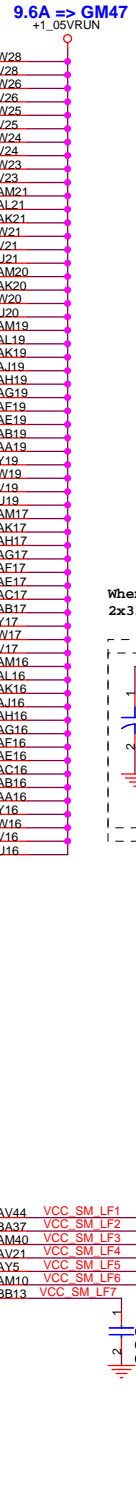
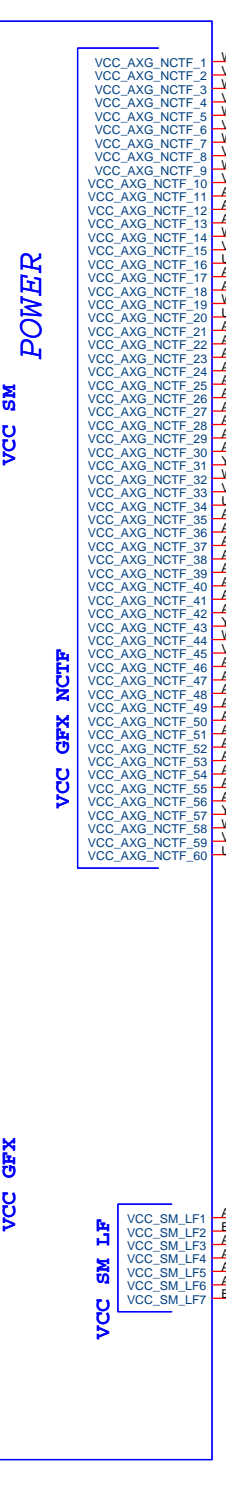
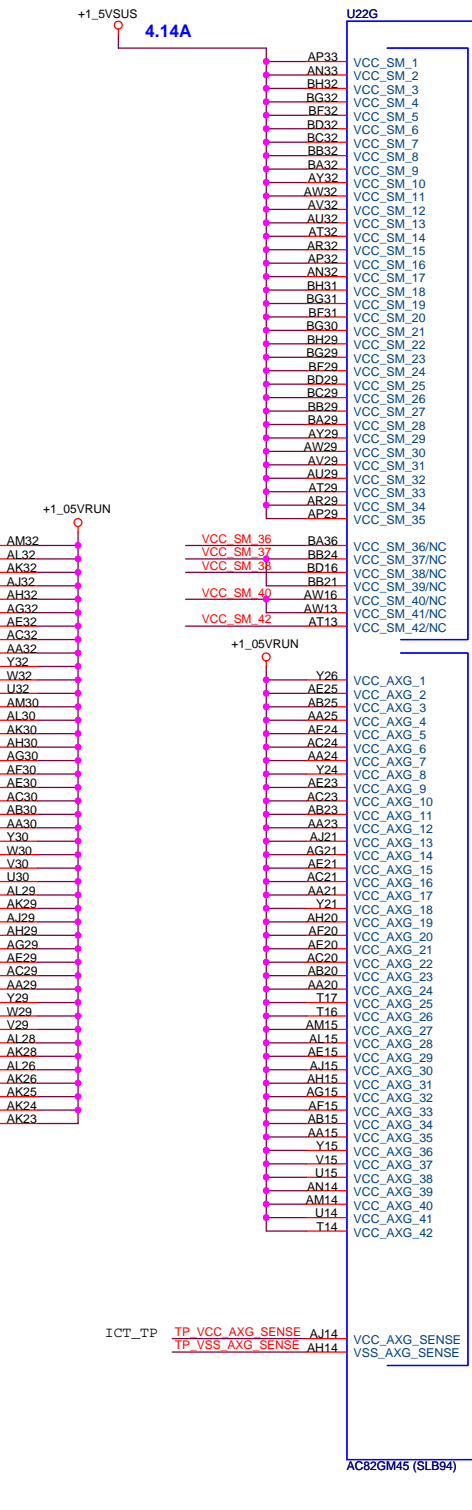
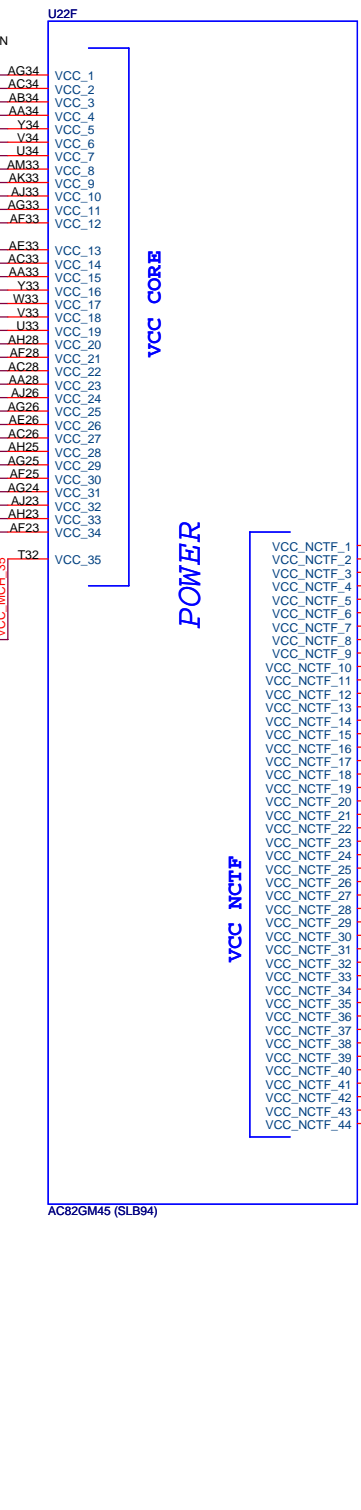
20 mils away from toggling signals.

30 mils away from toggling signals.

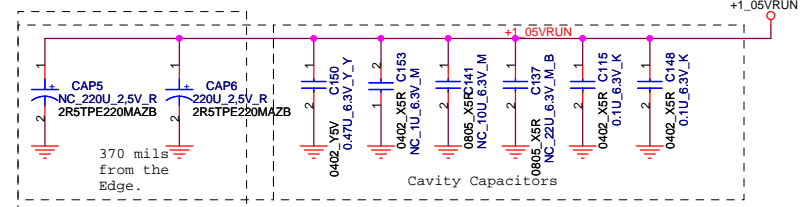








When stuff GM47,  
2x330 uF, 6 mOhm ESR (12 mOhm ESR each capacitor)

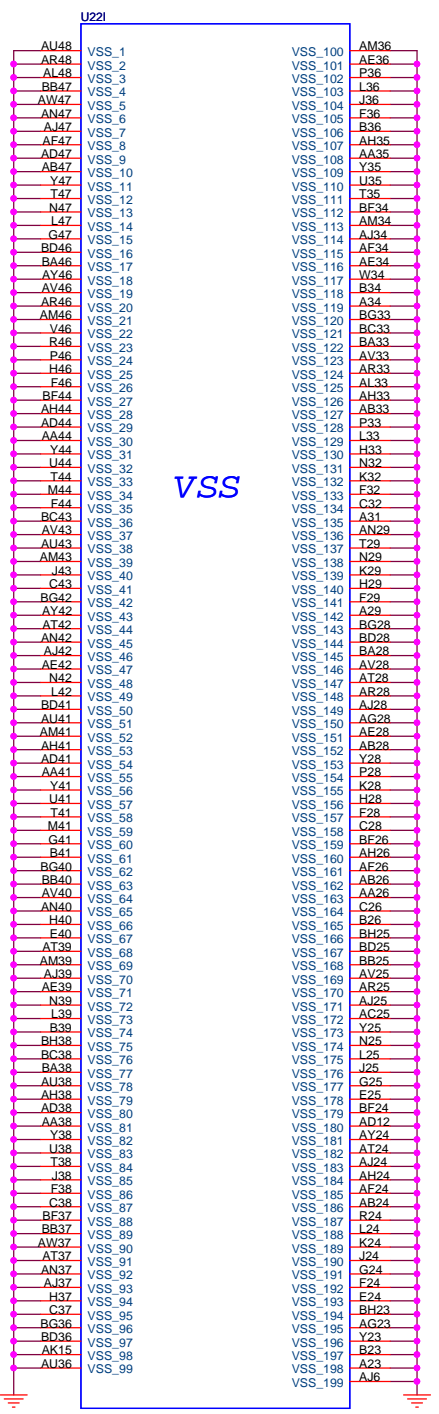


ICT\_TP TP VCC AXG SENSE AH14  
TP VSS AXG SENSE AH14

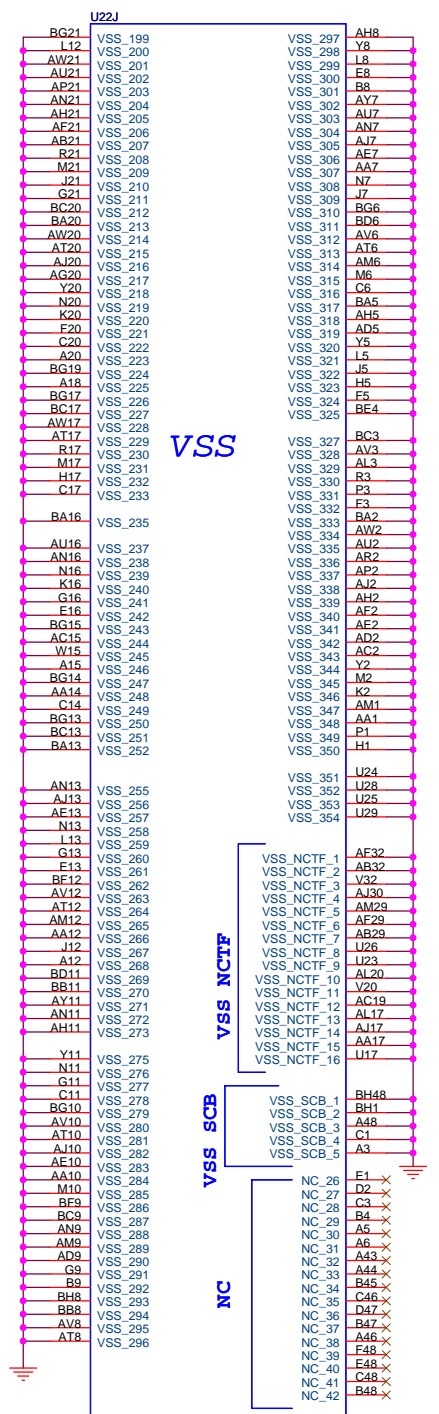
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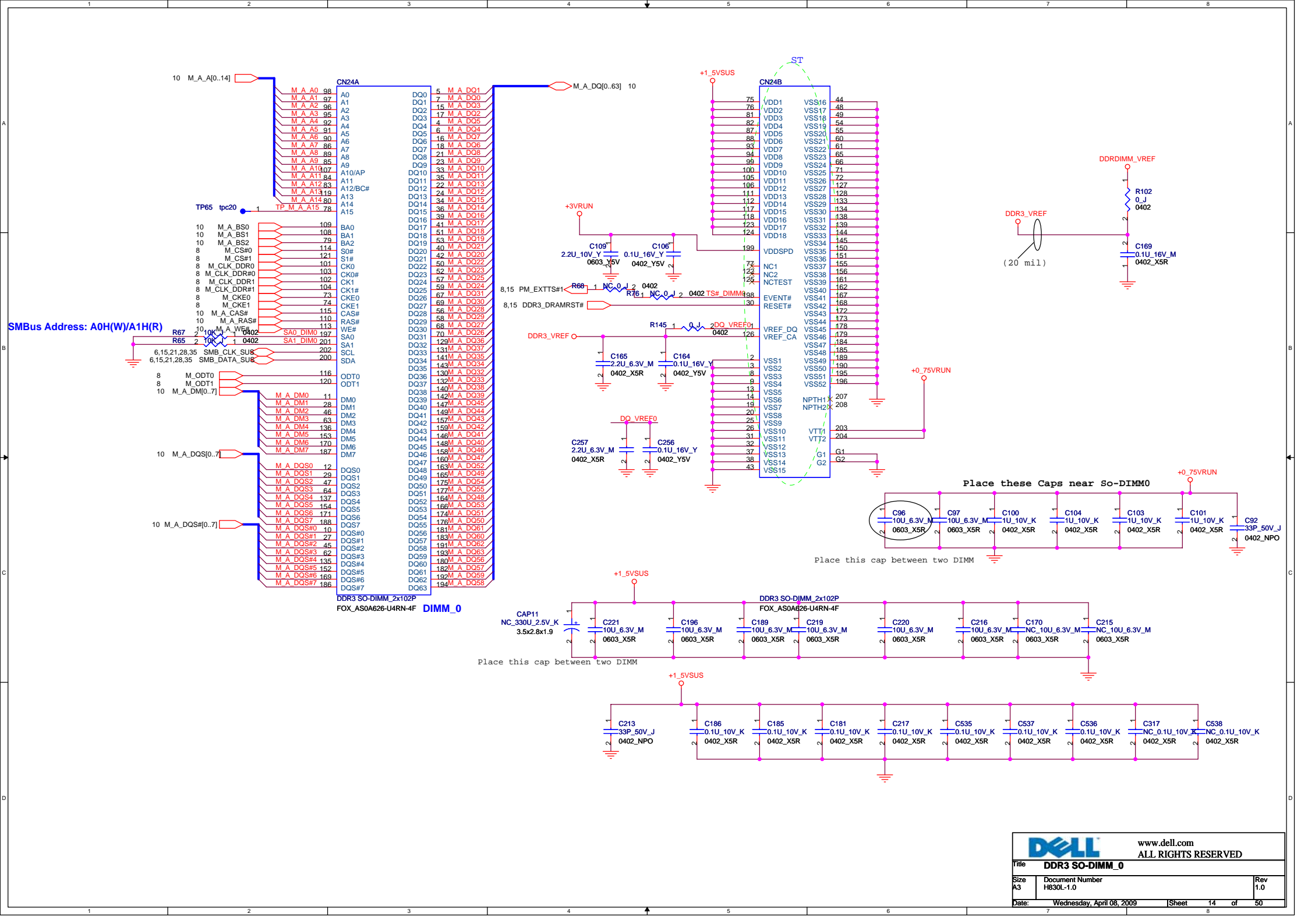


AC82GM45 (SLB94)

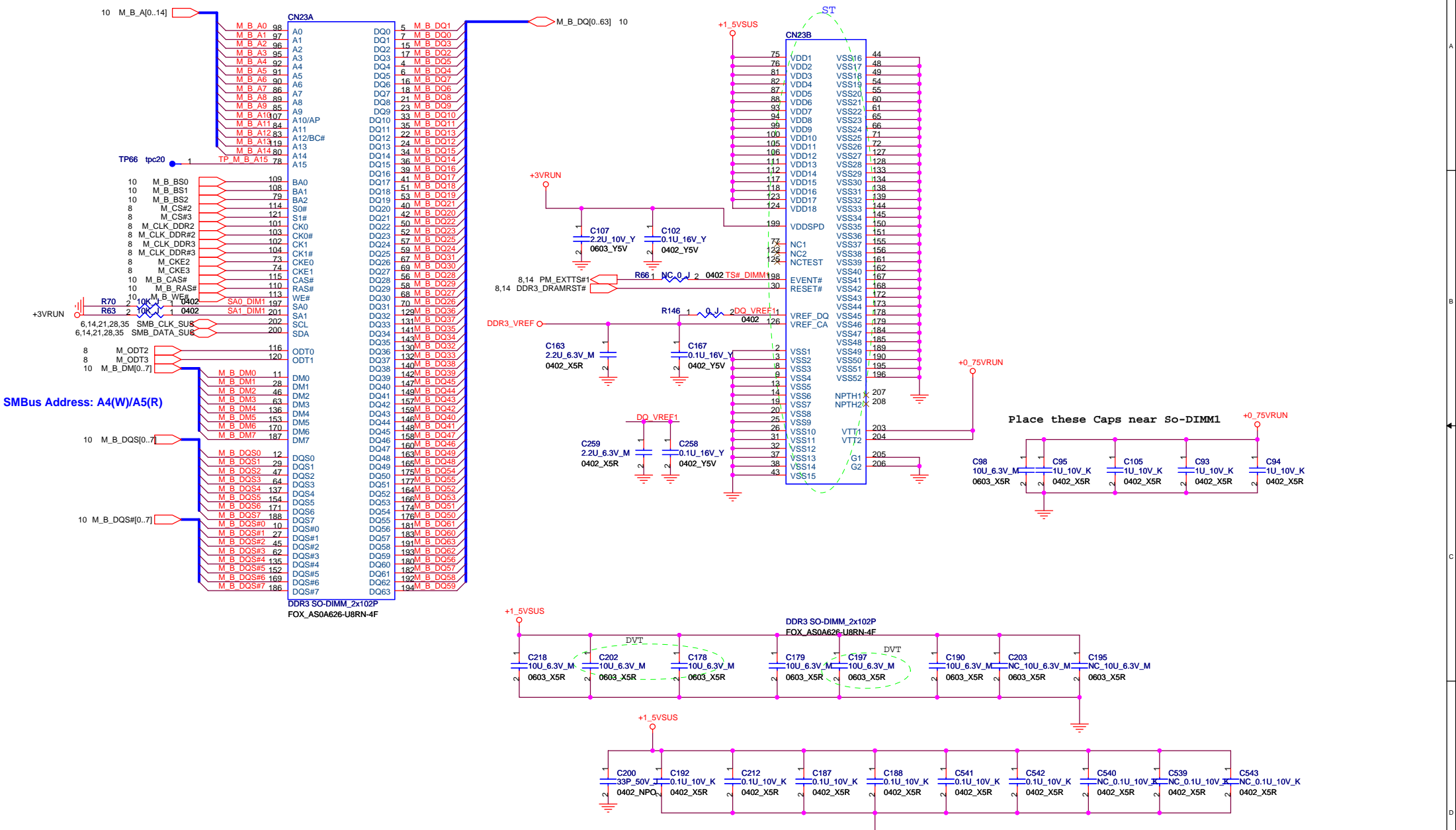
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Title **Cantiga 777**

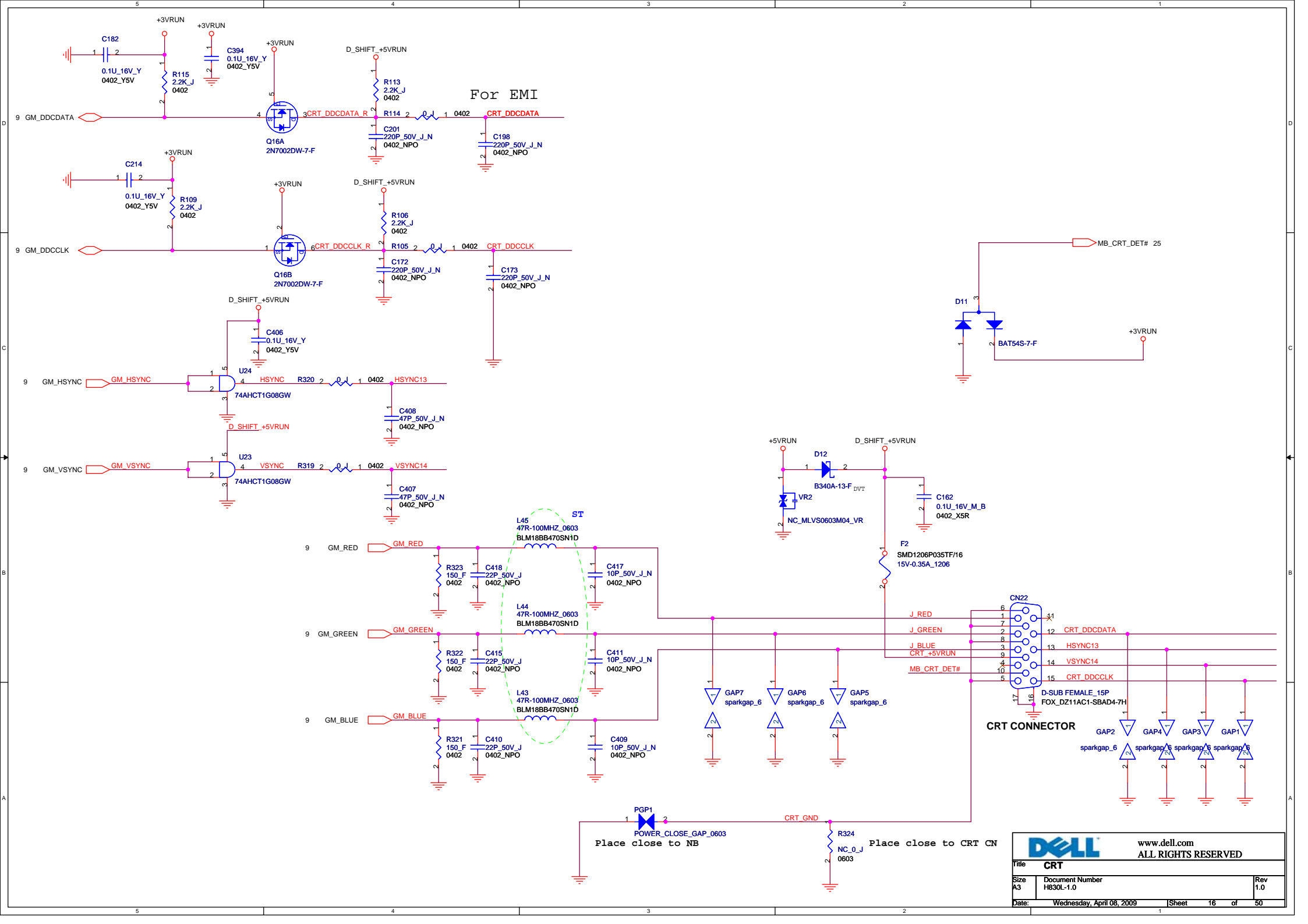
Size A3	Document Number H830L-1.0	Rev 1.0
Date Wednesday, April 08, 2009	Sheet 13	of 50











For EMI

CRT CONNECTOR

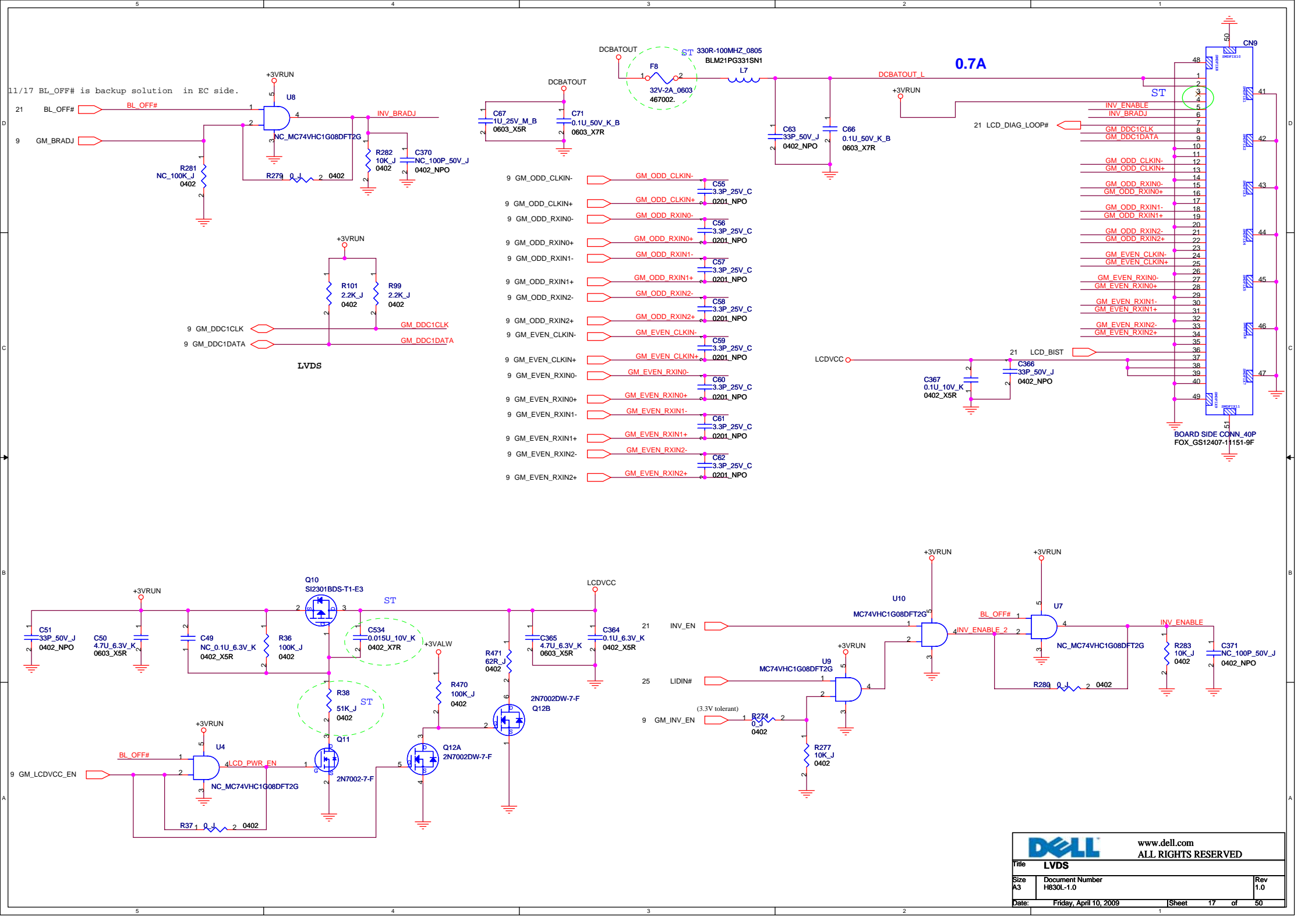
PGP1  
POWER\_CLOSE\_GAP\_0603  
Place close to NB

CRT GND

R324  
NC\_0\_J  
0603

Place close to CRT CN

<b>DELL</b>			www.dell.com ALL RIGHTS RESERVED		
Title <b>CRT</b>					
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11/17 BL\_OFF# is backup solution in EC side.

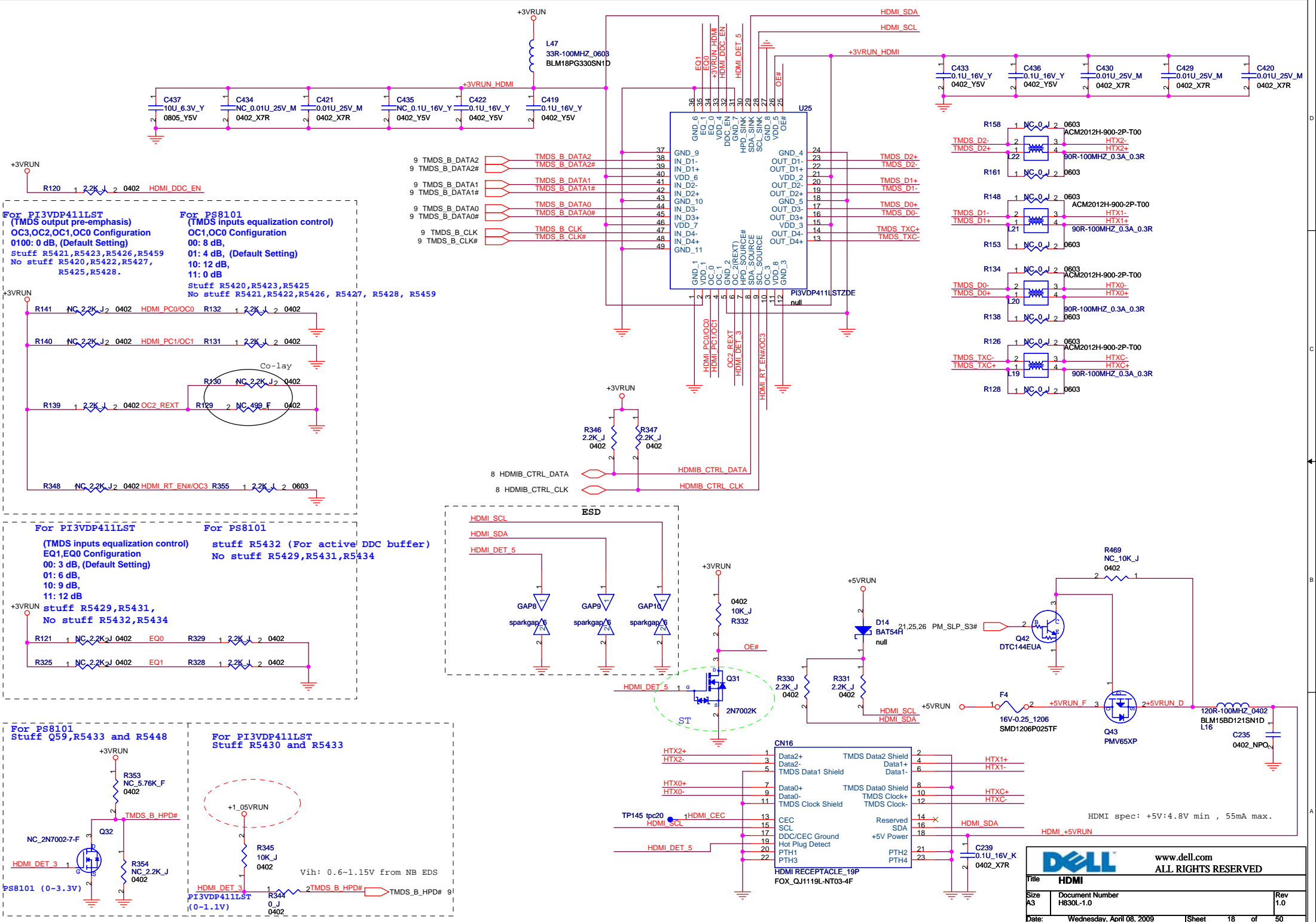
LVDS

0.7A

- 9 GM\_ODD\_CLKIN- GM\_ODD\_CLKIN- C55 3.3P\_25V\_C
- 9 GM\_ODD\_CLKIN+ GM\_ODD\_CLKIN+ C55 0.0201\_NPO
- 9 GM\_ODD\_RXIN0- GM\_ODD\_RXIN0- C56 3.3P\_25V\_C
- 9 GM\_ODD\_RXIN0+ GM\_ODD\_RXIN0+ C56 0.0201\_NPO
- 9 GM\_ODD\_RXIN1- GM\_ODD\_RXIN1- C57 3.3P\_25V\_C
- 9 GM\_ODD\_RXIN1+ GM\_ODD\_RXIN1+ C57 0.0201\_NPO
- 9 GM\_ODD\_RXIN2- GM\_ODD\_RXIN2- C58 3.3P\_25V\_C
- 9 GM\_ODD\_RXIN2+ GM\_ODD\_RXIN2+ C58 0.0201\_NPO
- 9 GM\_ODD\_RXIN2- GM\_ODD\_RXIN2- C59 3.3P\_25V\_C
- 9 GM\_ODD\_RXIN2+ GM\_ODD\_RXIN2+ C59 0.0201\_NPO
- 9 GM\_ODD\_RXIN0- GM\_ODD\_RXIN0- C60 3.3P\_25V\_C
- 9 GM\_ODD\_RXIN0+ GM\_ODD\_RXIN0+ C60 0.0201\_NPO
- 9 GM\_ODD\_RXIN1- GM\_ODD\_RXIN1- C61 3.3P\_25V\_C
- 9 GM\_ODD\_RXIN1+ GM\_ODD\_RXIN1+ C61 0.0201\_NPO
- 9 GM\_ODD\_RXIN2- GM\_ODD\_RXIN2- C62 3.3P\_25V\_C
- 9 GM\_ODD\_RXIN2+ GM\_ODD\_RXIN2+ C62 0.0201\_NPO

- 1 INV\_ENABLE
- 2 INV\_BRADJ
- 3 GM\_DDC1CLK
- 4 GM\_DDC1DATA
- 5 GM\_ODD\_CLKIN-
- 6 GM\_ODD\_CLKIN+
- 7 GM\_ODD\_RXIN0-
- 8 GM\_ODD\_RXIN0+
- 9 GM\_ODD\_RXIN1-
- 10 GM\_ODD\_RXIN1+
- 11 GM\_ODD\_RXIN2-
- 12 GM\_ODD\_RXIN2+
- 13 GM\_ODD\_RXIN0-
- 14 GM\_ODD\_RXIN0+
- 15 GM\_ODD\_RXIN1-
- 16 GM\_ODD\_RXIN1+
- 17 GM\_ODD\_RXIN2-
- 18 GM\_ODD\_RXIN2+
- 19 GM\_ODD\_RXIN0-
- 20 GM\_ODD\_RXIN0+
- 21 GM\_ODD\_RXIN1-
- 22 GM\_ODD\_RXIN1+
- 23 GM\_ODD\_RXIN2-
- 24 GM\_ODD\_RXIN2+
- 25 GM\_ODD\_RXIN0-
- 26 GM\_ODD\_RXIN0+
- 27 GM\_ODD\_RXIN1-
- 28 GM\_ODD\_RXIN1+
- 29 GM\_ODD\_RXIN2-
- 30 GM\_ODD\_RXIN2+
- 31 GM\_ODD\_RXIN0-
- 32 GM\_ODD\_RXIN0+
- 33 GM\_ODD\_RXIN1-
- 34 GM\_ODD\_RXIN1+
- 35 GM\_ODD\_RXIN2-
- 36 GM\_ODD\_RXIN2+
- 37 LCD\_BIST
- 38 LCD\_DIAG\_LOOP#
- 39
- 40
- 41
- 42
- 43
- 44
- 45
- 46
- 47
- 48
- 49

BOARD SIDE CONN\_40P  
FOX\_GS12407-11151-9F



**For PI3VDP411LST (TMDS output pre-emphasis)**  
 OC3,OC2,OC1,OC0 Configuration  
 0100: 0 dB, (Default Setting)  
 stuff R5421,R5423,R5426,R5459  
 No stuff R5420,R5422,R5427,  
 R5425,R5428.

**For PS8101 (TMDS inputs equalization control)**  
 OC1,OC0 Configuration  
 00: 8 dB,  
 01: 4 dB, (Default Setting)  
 10: 12 dB,  
 11: 0 dB  
 Stuff R5420,R5423,R5425  
 No stuff R5421,R5422,R5426, R5427, R5428, R5459

**For PI3VDP411LST (TMDS inputs equalization control)**  
 EQ1,EQ0 Configuration  
 00: 3 dB, (Default Setting)  
 01: 6 dB,  
 10: 9 dB,  
 11: 12 dB  
 stuff R5429,R5431,  
 No stuff R5432,R5434

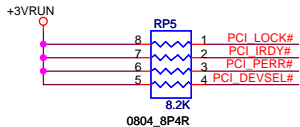
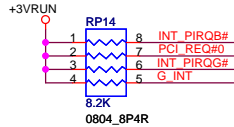
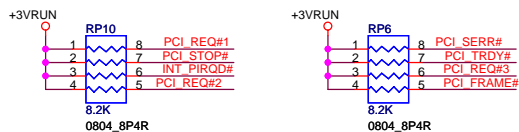
**For PS8101**  
 stuff R5432 (For active DDC buffer)  
 No stuff R5429,R5431,R5434

**For PS8101**  
 Stuff Q59,R5433 and R5448

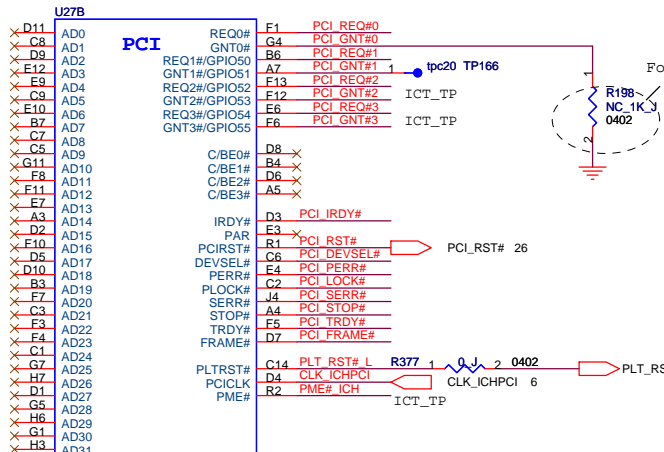
**For PI3VDP411LST**  
 Stuff R5430 and R5433

HDMI spec: +5V:4.8V min , 55mA max.

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File	HDMI		
Size	A3	Document Number	H830L-1.0
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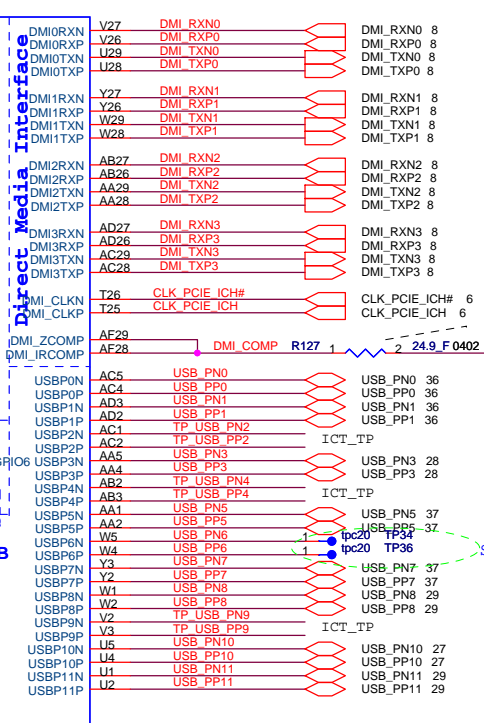
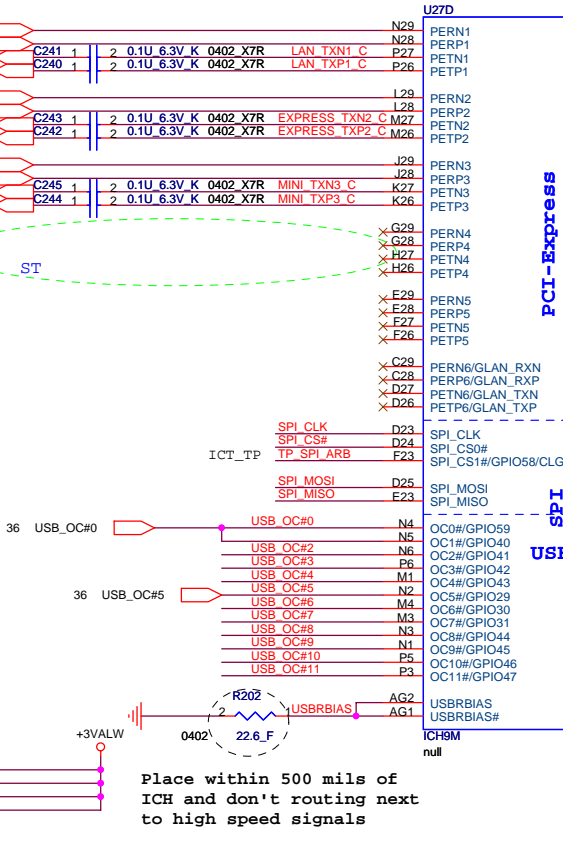
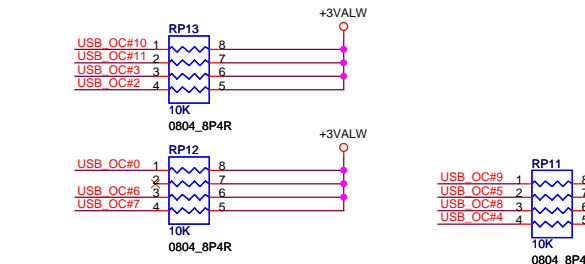
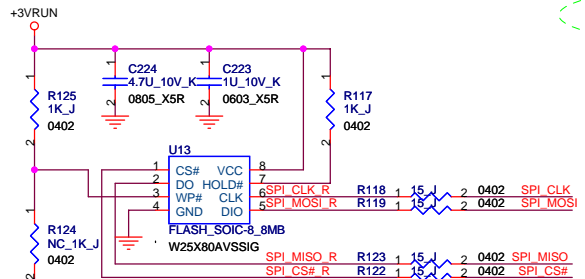
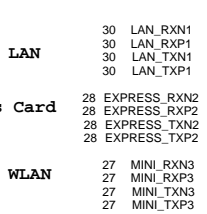
PCI Pullups



For Boot BIOS Selection.

**Strap for Boot-BIOS**

	GNT0#	SPI_CS1#
LPC(Default)	Hi	Hi
PCI	Hi	Low
SPI	Low	Hi



Place within 500 mils of ICH

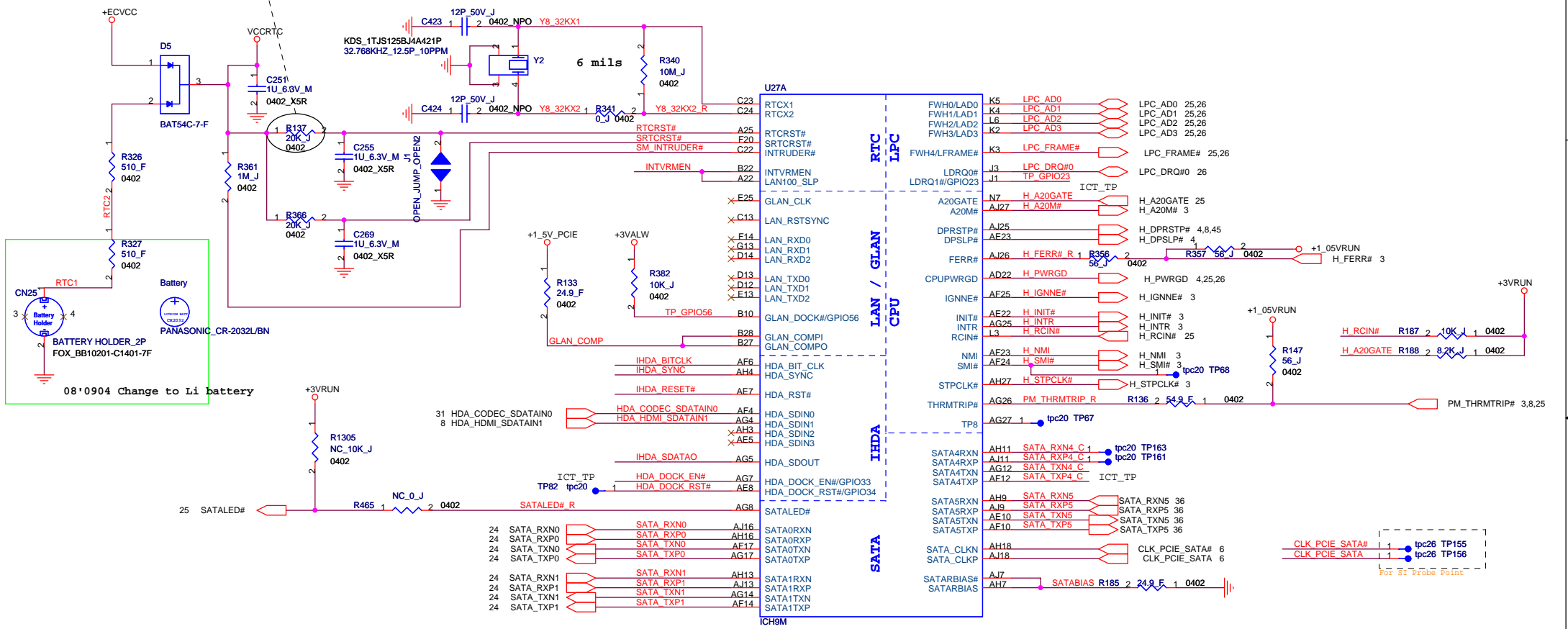
USB PORT	Function
PORT-0	Ext. Port
PORT-1	Ext. Port
PORT-2	
PORT-3	EXPRESS CARD
PORT-4	
PORT-5	Ext. Port
PORT-6	ST
PORT-7	Card reader
PORT-8	Bluetooth
PORT-9	
PORT-10	WLAN/WiMAX
PORT-11	Camera

Place within 500 mils of ICH and don't routing next to high speed signals



The traces inside this block should be wider.

Internal VRM enabled for VccSus1_05, VccSus1_5, VccCl1_5, VccLAN1_05 and VccCl1_05	
INTVRMEN	Low= Internal VR Disabled High= Internal VR Enabled(Default)



RTCX1	K5	LPC_AD0	LPC_AD0	25,26
RTCX2	K4	LPC_AD1	LPC_AD1	25,26
	L6	LPC_AD2	LPC_AD2	25,26
	K2	LPC_AD3	LPC_AD3	25,26
	K3	LPC_FRAME#	LPC_FRAME#	25,26
	J3	LPC_DRQ#0	LPC_DRQ#0	26
	J1	TP_GPIO23		
	N7	H_A20GATE	H_A20GATE	25
	AJ27	H_A20M#	H_A20M#	3
	AJ25	H_DPRSTP#	H_DPRSTP#	4,8,45
	AE23	H_DPSLP#	H_DPSLP#	4
	AJ26	H_FERR# R	H_FERR#	3
	AD22	H_PWRGD	H_PWRGD	4,25,26
	AE25	H_IGNNE#	H_IGNNE#	3
	AE22	H_INIT#	H_INIT#	3
	AG25	H_INTR	H_INTR	3
	L3	H_RCIN#	H_RCIN#	25
	AE23	H_NMI	H_NMI	3
	AE24	H_SMI#	H_SMI#	3
	AH27	H_STPCLK#	H_STPCLK#	3
	AG26	PM_THRMTRIP#	PM_THRMTRIP#	3,8,25
	AH11	SATA_RXN4 C	SATA_RXN4	36
	AJ11	SATA_RXP4 C	SATA_RXP4	36
	AG12	SATA_TXN4 C	SATA_TXN4	36
	AE12	SATA_TXP4 C	SATA_TXP4	36
	AH9	SATA_RXN5	SATA_RXN5	36
	AJ9	SATA_RXP5	SATA_RXP5	36
	AE10	SATA_TXN5	SATA_TXN5	36
	AE10	SATA_TXN5	SATA_TXN5	36
	AE10	SATA_TXN5	SATA_TXN5	36
	AH18	CLK_PCIE_SATA#	CLK_PCIE_SATA#	6
	AJ18	CLK_PCIE_SATA	CLK_PCIE_SATA	6
	AJ7	SATARBIAS#	SATARBIAS#	
	AH7	SATARBIAS	SATARBIAS	

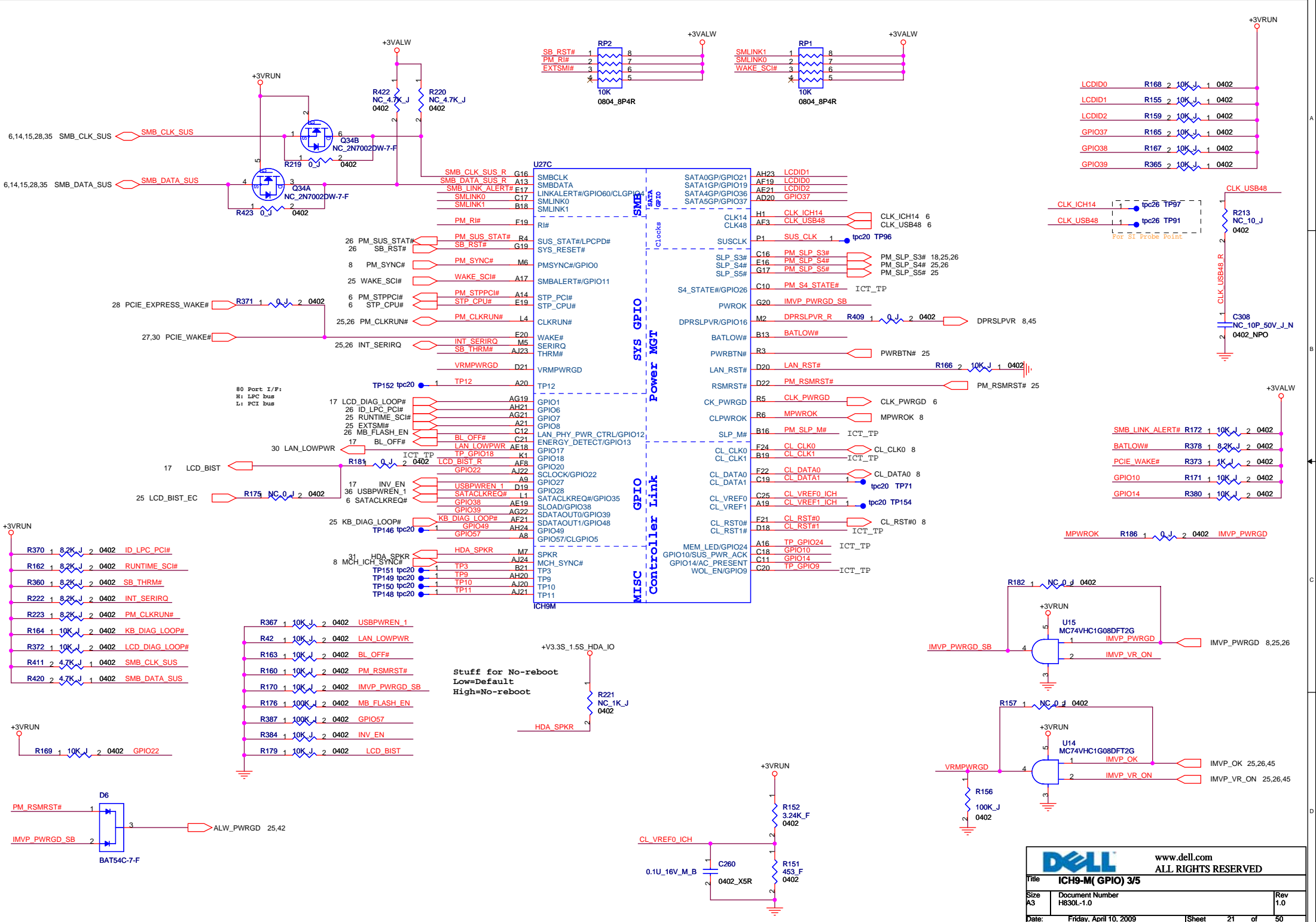


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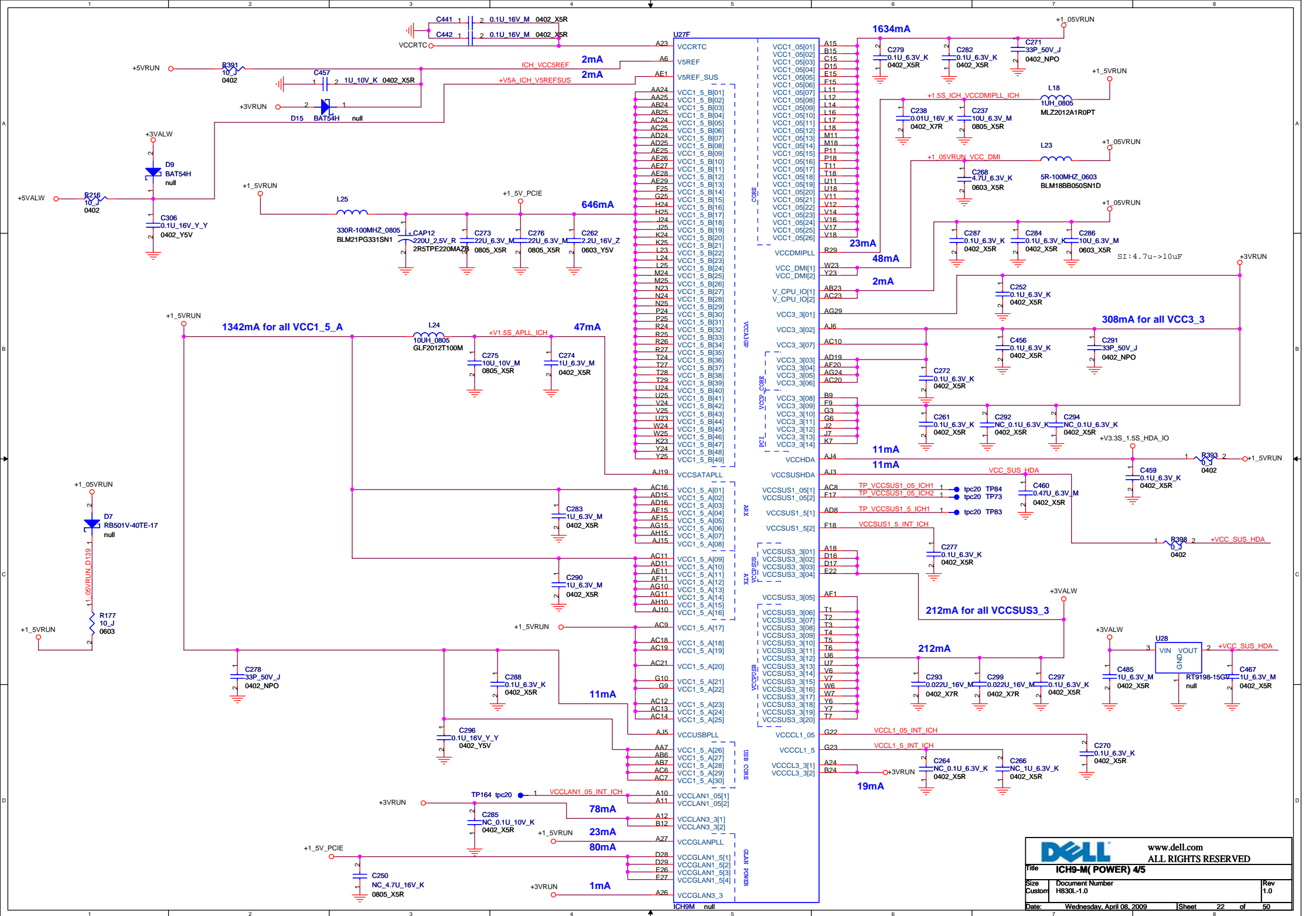
Title: **ICH9-M (LPC,IDE,SATA) 2/5**


Size: A3 Document Number: H830L-1.0 Rev: 1.0

Date: Friday, April 10, 2009 Sheet: 20 of 50









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Size	Document Number	Rev 1.0	
Custom	H830L-1.0		
Date:	Wednesday, April 08, 2009	Sheet	22 of 50

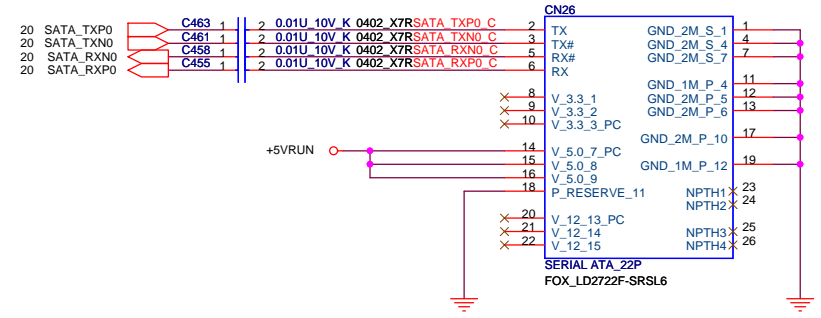
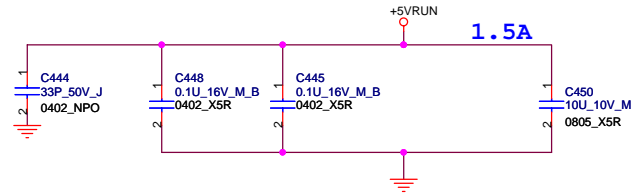


U27E		
AA26	VSS[001]	VSS[107]
AA27	VSS[002]	VSS[108]
AA3	VSS[003]	VSS[109]
AA6	VSS[004]	VSS[110]
AB1	VSS[005]	VSS[111]
AA23	VSS[006]	VSS[112]
AB28	VSS[007]	VSS[113]
AB29	VSS[008]	VSS[114]
AB4	VSS[009]	VSS[115]
AB5	VSS[010]	VSS[116]
AC17	VSS[011]	VSS[117]
AC26	VSS[012]	VSS[118]
AC27	VSS[013]	VSS[119]
AC3	VSS[014]	VSS[120]
AD1	VSS[015]	VSS[121]
AD10	VSS[016]	VSS[122]
AD12	VSS[017]	VSS[123]
AD13	VSS[018]	VSS[124]
AD14	VSS[019]	VSS[125]
AD17	VSS[020]	VSS[126]
AD18	VSS[021]	VSS[127]
AD21	VSS[022]	VSS[128]
AD28	VSS[023]	VSS[129]
AD29	VSS[024]	VSS[130]
AD4	VSS[025]	VSS[131]
AD5	VSS[026]	VSS[132]
AD6	VSS[027]	VSS[133]
AD7	VSS[028]	VSS[134]
AD9	VSS[029]	VSS[135]
AE12	VSS[030]	VSS[136]
AE13	VSS[031]	VSS[137]
AE14	VSS[032]	VSS[138]
AE16	VSS[033]	VSS[139]
AE17	VSS[034]	VSS[140]
AE2	VSS[035]	VSS[141]
AE20	VSS[036]	VSS[142]
AE24	VSS[037]	VSS[143]
AE3	VSS[038]	VSS[144]
AE4	VSS[039]	VSS[145]
AE6	VSS[040]	VSS[146]
AE9	VSS[041]	VSS[147]
AE13	VSS[042]	VSS[148]
AE16	VSS[043]	VSS[149]
AE18	VSS[044]	VSS[150]
AE22	VSS[045]	VSS[151]
AH26	VSS[046]	VSS[152]
AE28	VSS[047]	VSS[153]
AE27	VSS[048]	VSS[154]
AF5	VSS[049]	VSS[155]
AF7	VSS[050]	VSS[156]
AF9	VSS[051]	VSS[157]
AG13	VSS[052]	VSS[158]
AG16	VSS[053]	VSS[159]
AG18	VSS[054]	VSS[160]
AG20	VSS[055]	VSS[161]
AG23	VSS[056]	VSS[162]
AG3	VSS[057]	VSS[163]
AG6	VSS[058]	VSS[164]
AG9	VSS[059]	VSS[165]
AH12	VSS[060]	VSS[166]
AH14	VSS[061]	VSS[167]
AH17	VSS[062]	VSS[168]
AH19	VSS[063]	VSS[169]
AH2	VSS[064]	VSS[170]
AH22	VSS[065]	VSS[171]
AH25	VSS[066]	VSS[172]
AH28	VSS[067]	VSS[173]
AH5	VSS[068]	VSS[174]
AH8	VSS[069]	VSS[175]
AJ12	VSS[070]	VSS[176]
AJ14	VSS[071]	VSS[177]
AJ17	VSS[072]	VSS[178]
AJ8	VSS[073]	VSS[179]
B11	VSS[074]	VSS[180]
B14	VSS[075]	VSS[181]
B17	VSS[076]	VSS[182]
B2	VSS[077]	VSS[183]
B20	VSS[078]	VSS[184]
B23	VSS[079]	VSS[185]
B5	VSS[080]	VSS[186]
B8	VSS[081]	VSS[187]
C26	VSS[082]	VSS[188]
C27	VSS[083]	VSS[189]
E11	VSS[084]	VSS[190]
E14	VSS[085]	VSS[191]
E18	VSS[086]	VSS[192]
E2	VSS[087]	VSS[193]
E21	VSS[088]	VSS[194]
E24	VSS[089]	VSS[195]
E5	VSS[090]	VSS[196]
E8	VSS[091]	VSS[197]
F16	VSS[092]	VSS[198]
F28	VSS[093]	
F29	VSS[094]	VSS_NCTF[01]
G12	VSS[095]	VSS_NCTF[02]
G14	VSS[096]	VSS_NCTF[03]
G18	VSS[097]	VSS_NCTF[04]
G21	VSS[098]	VSS_NCTF[05]
G24	VSS[099]	VSS_NCTF[06]
G26	VSS[100]	VSS_NCTF[07]
G27	VSS[101]	VSS_NCTF[08]
G8	VSS[102]	VSS_NCTF[09]
H2	VSS[103]	VSS_NCTF[10]
H23	VSS[104]	VSS_NCTF[11]
H28	VSS[105]	VSS_NCTF[12]
H29	VSS[106]	

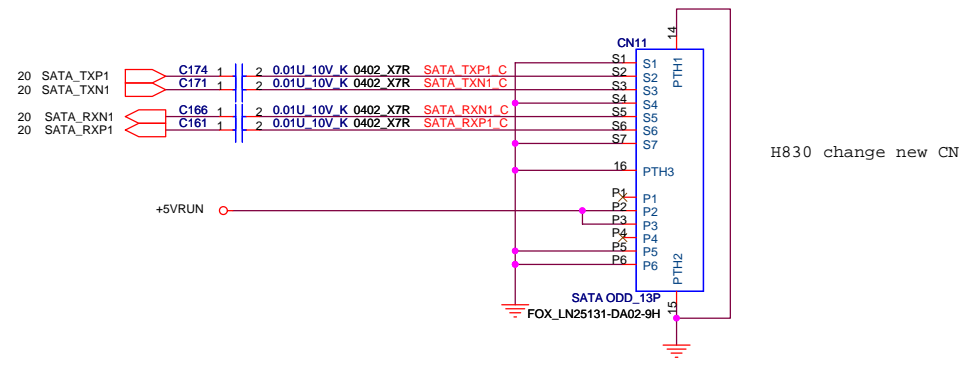
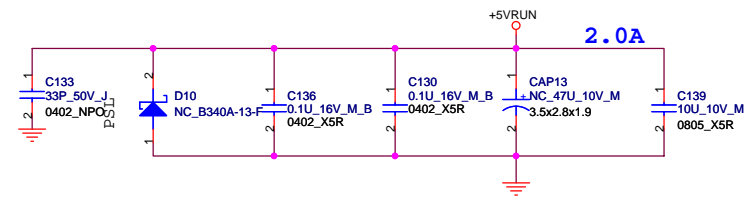
ICH9M

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Title <b>ICH9-M( GND) 5/5</b>			
Size A3	Document Number H830L-1.0	Rev 1.0	
Date:	Wednesday, April 08, 2009	Sheet	23 of 50

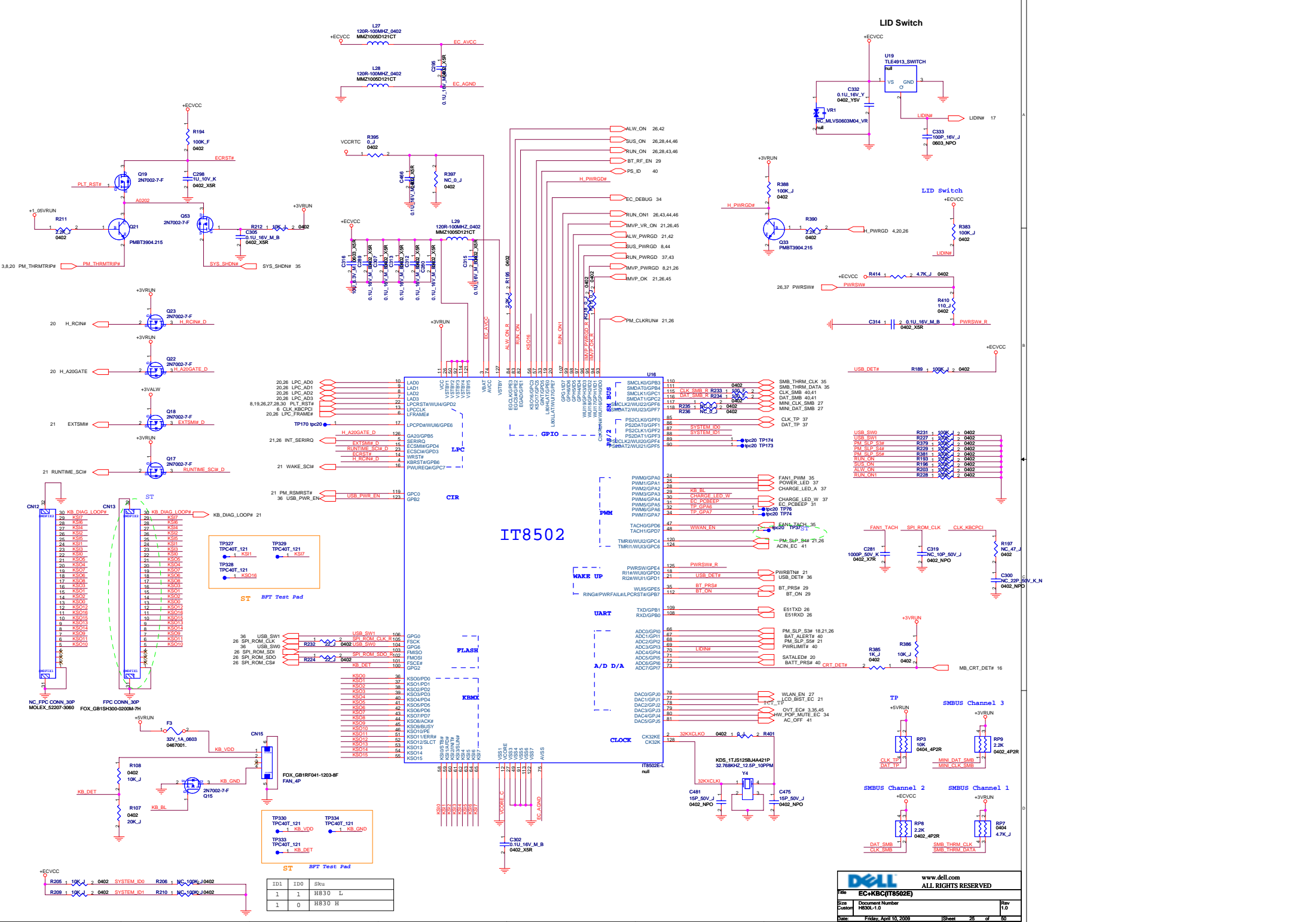
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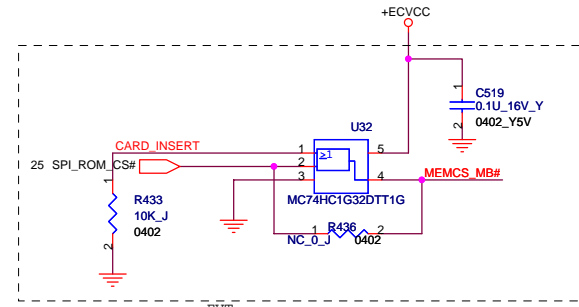
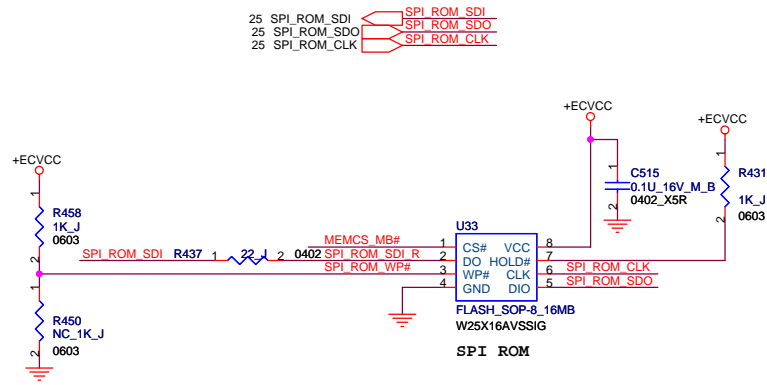
# SATA ODD CONN



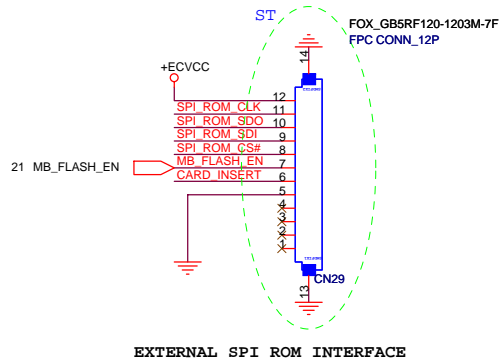
**ODD CON ADAPTER**  
Add CN68 need 2N-0013009-FKG0 in BOM



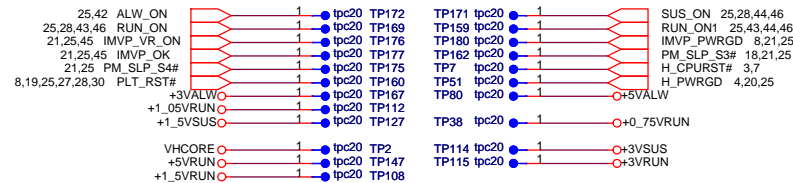
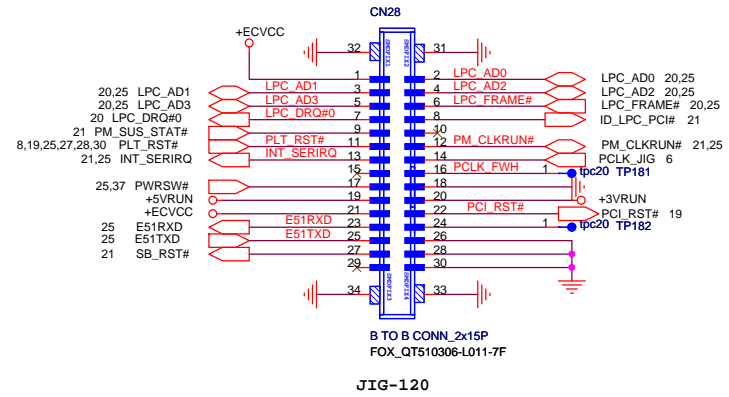
ID1	ID0	Stu
1	1	H830 L
1	0	H830 H

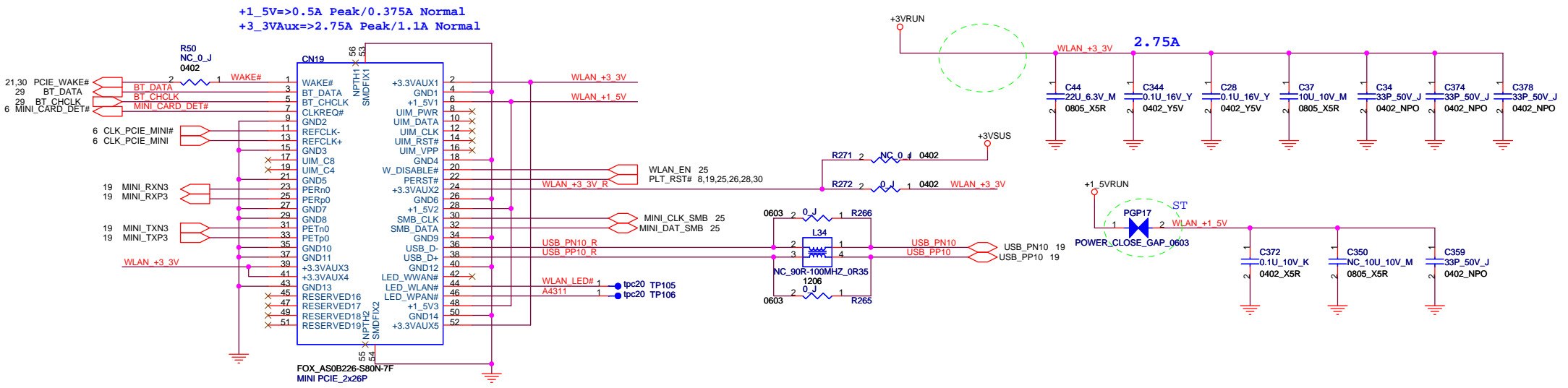


EVT  
When MP, change U11 no stuff, R233 stuff

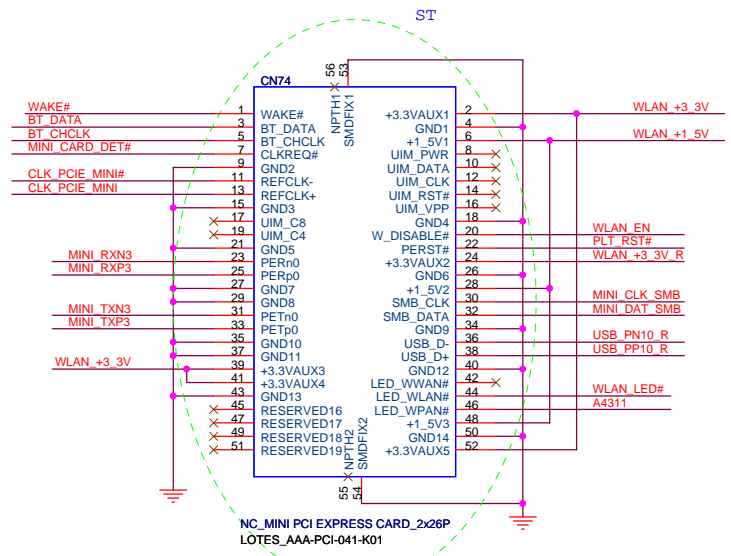


EXTERNAL SPI ROM INTERFACE



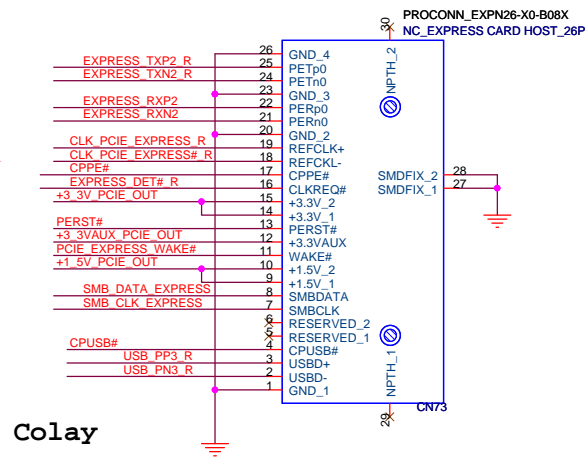
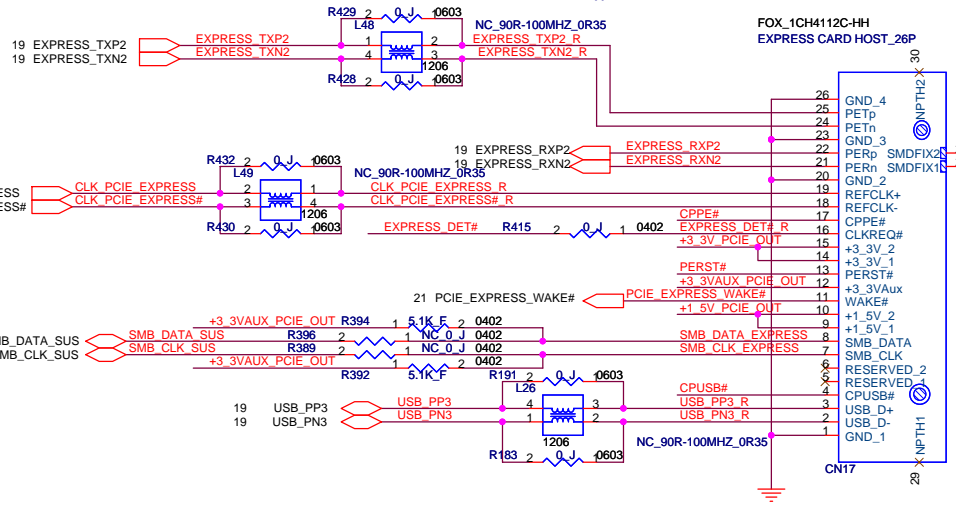
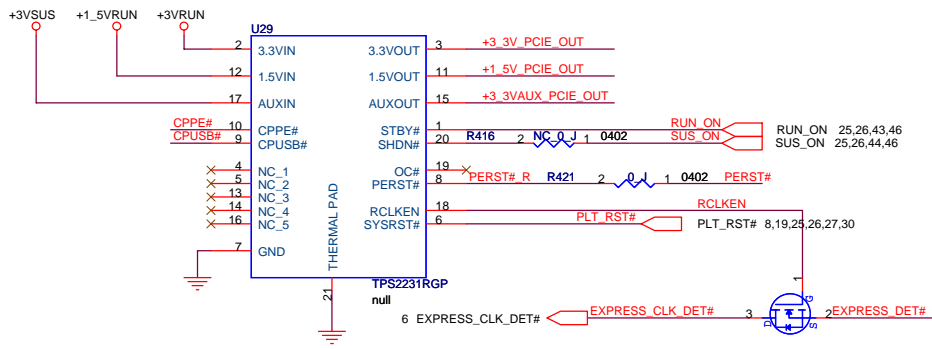


Half Mini Card for WLAN or WiMAX

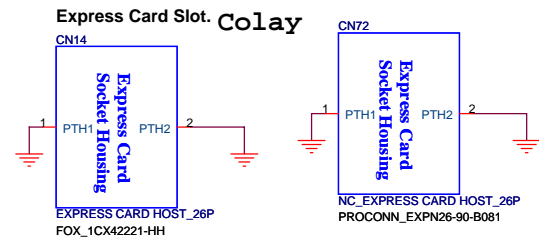
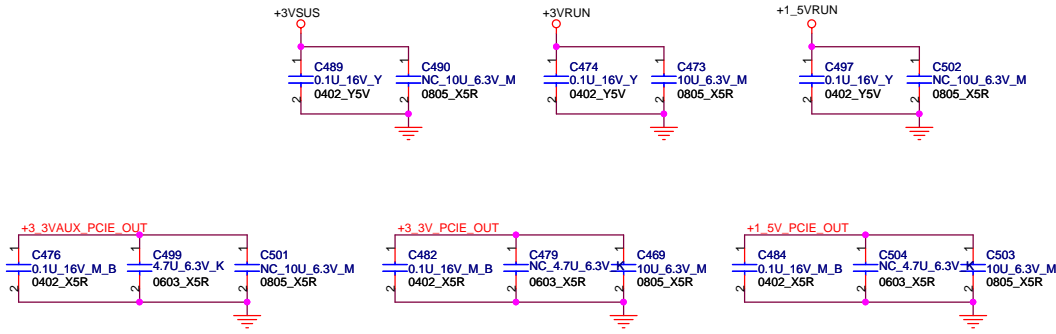


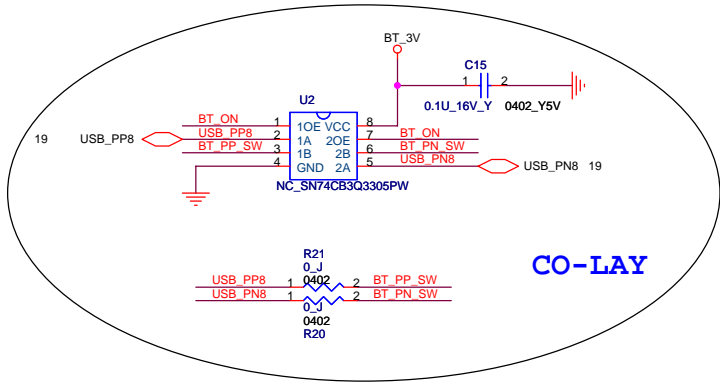
Colay: Half Mini Card CN second source

**+1.5V=>650mA**  
**+3.3VAux=>275mA**  
**+3.3V=>1.3A**  
**Express Card Power Switch**

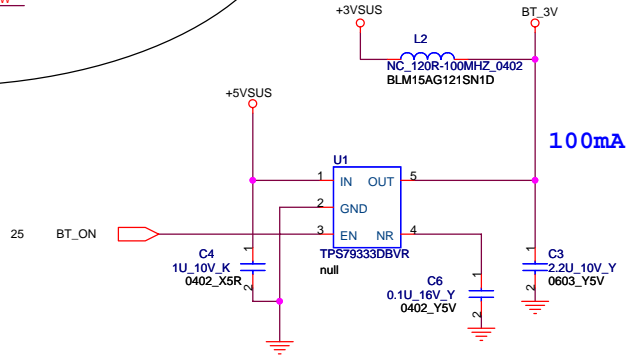


Colay



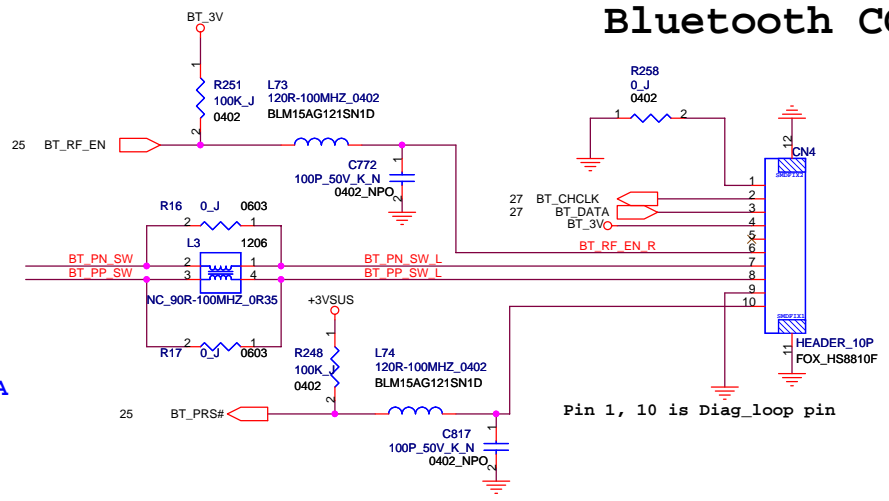


CO-LAY



100mA

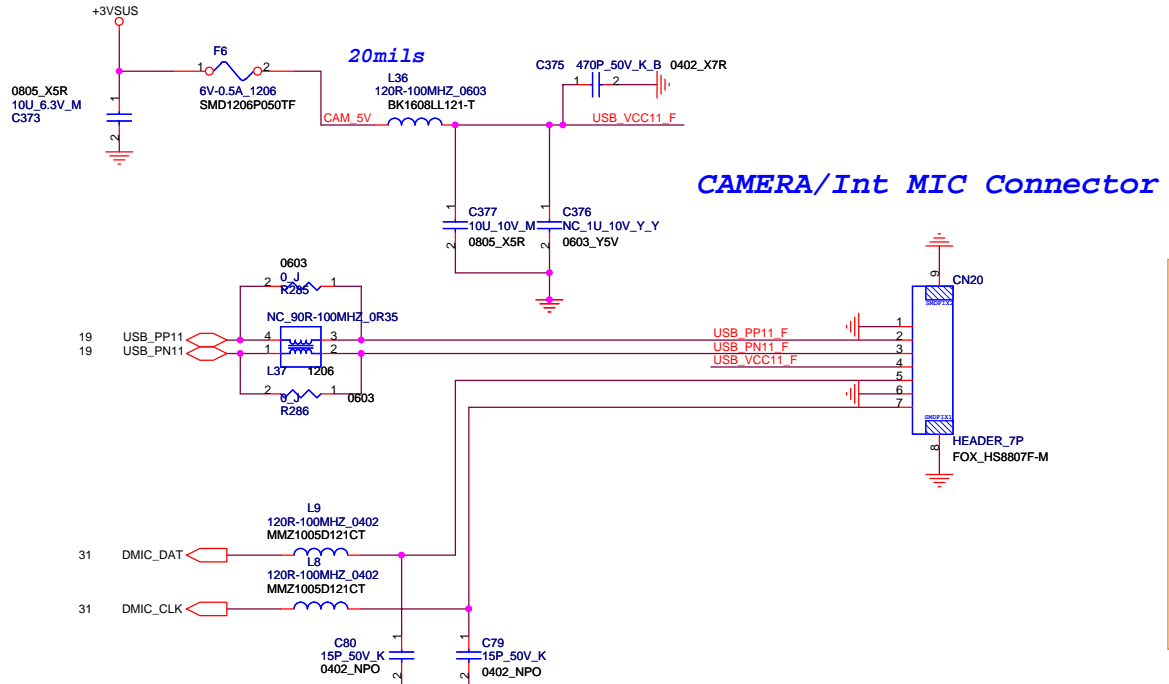
### Bluetooth CONN.



Pin 1, 10 is Diag\_loop pin

- TP344 TPC40B\_121
  - TP343 TPC40B\_121
  - TP342 TPC40B\_121
  - TP339 TPC40B\_121
  - TP338 TPC40B\_121
  - TP340 TPC40B\_121
  - TP341 TPC40B\_121
  - TP345 TPC40B\_121
  - TP346 TPC40B\_121
- ST BFT Test Pad

### Bluetooth



### CAMERA/Int MIC Connector

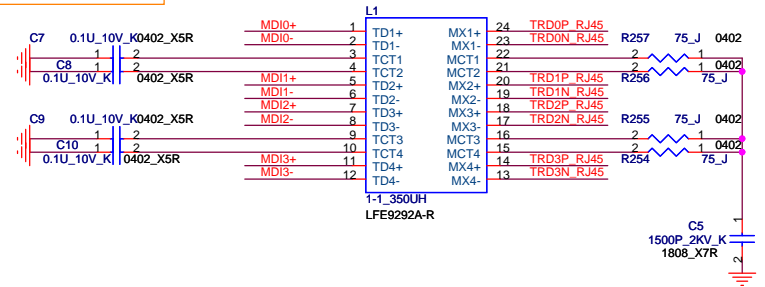
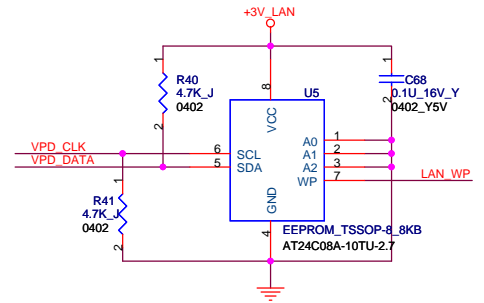
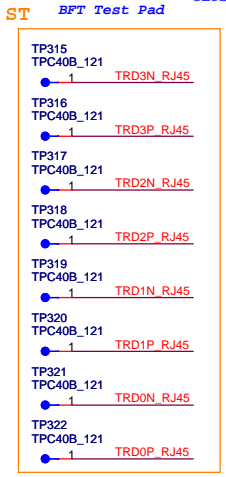
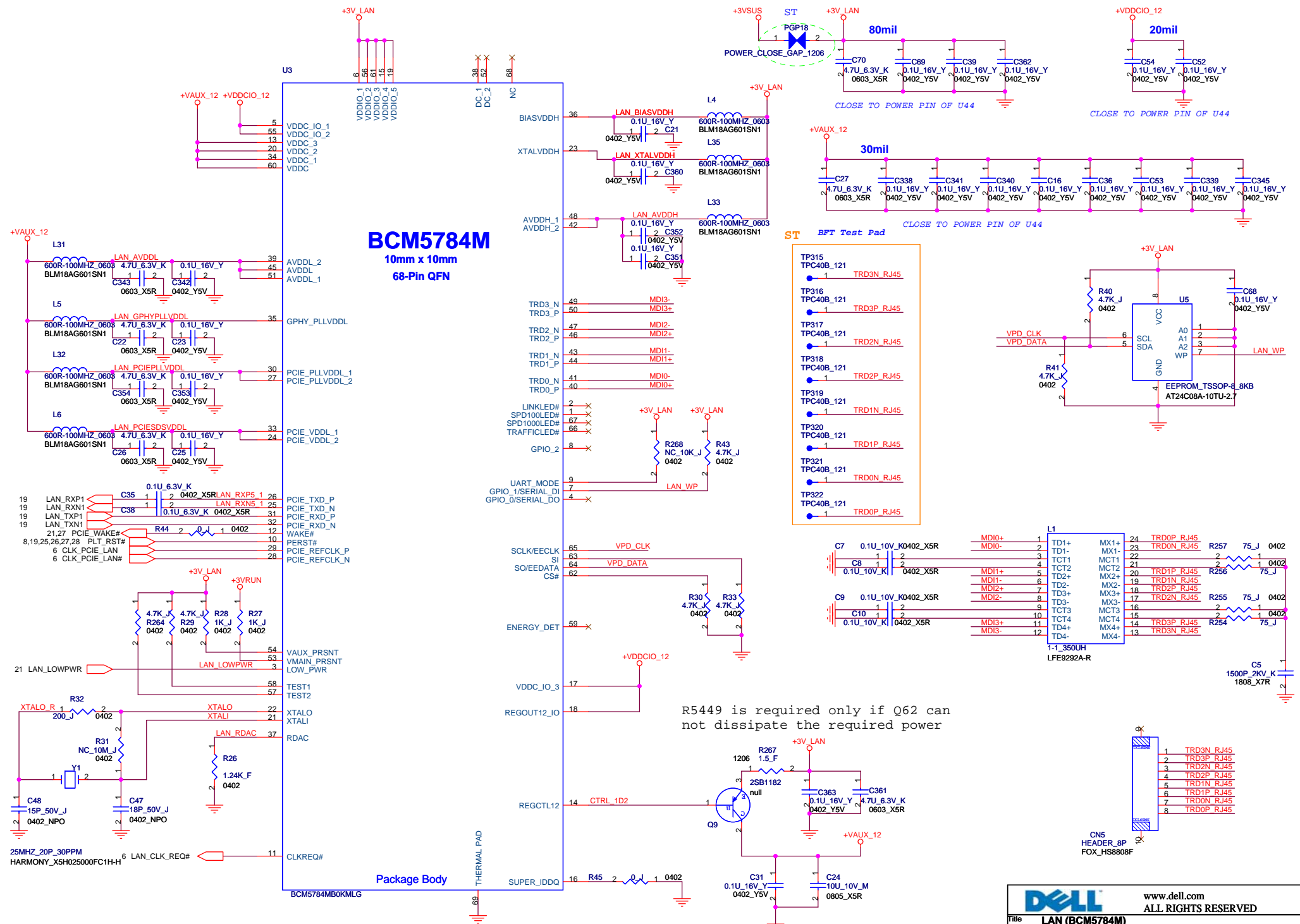
- TP305 TPC40B\_121
  - TP306 TPC40B\_121
  - TP307 TPC40B\_121
  - TP308 TPC40B\_121
  - TP309 TPC40B\_121
  - TP310 TPC40B\_121
  - TP311 TPC40B\_121
- ST BFT Test Pad

### Camera & Digi MIC

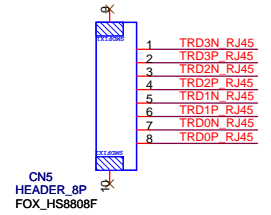


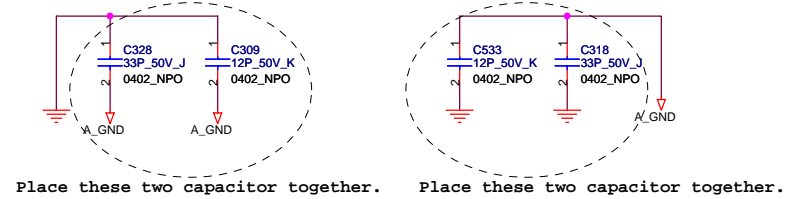
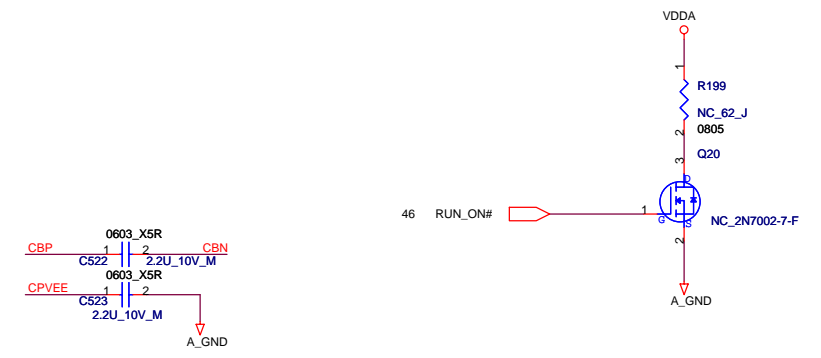
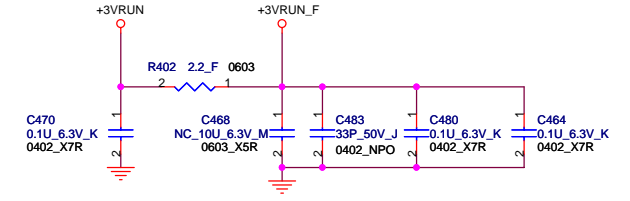
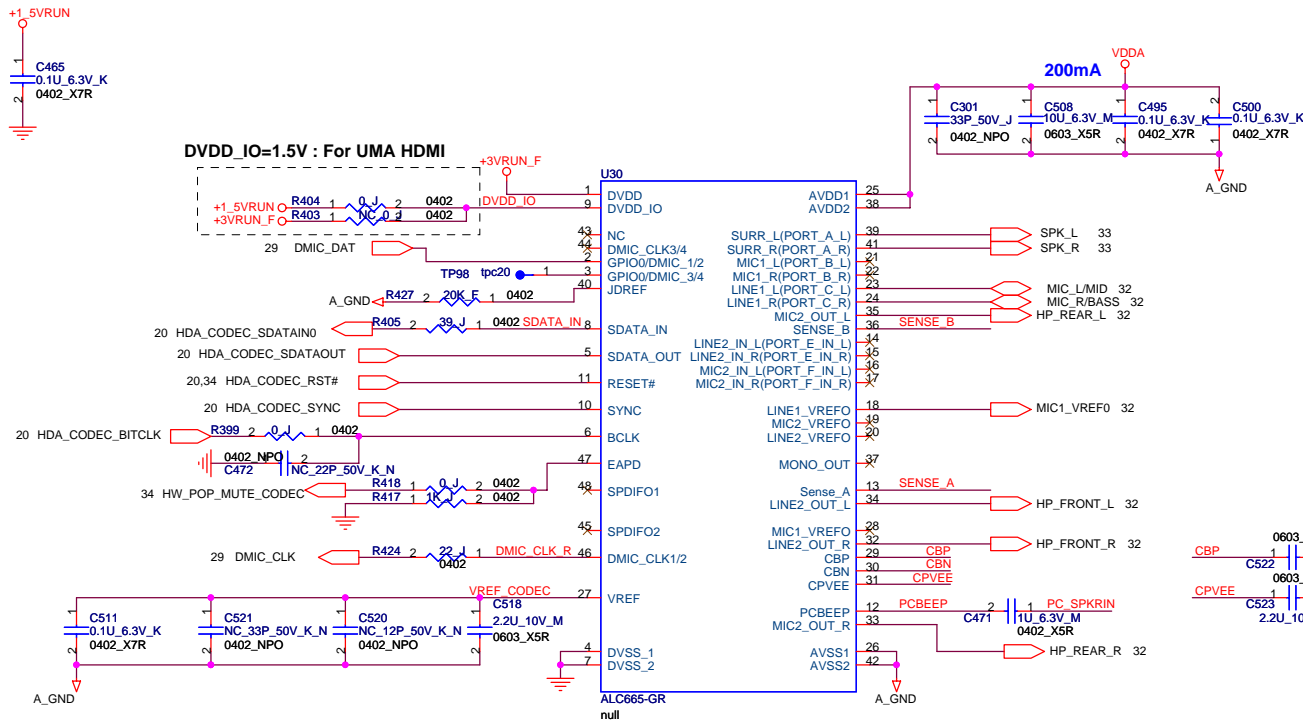
# BCM5784M

10mm x 10mm  
68-Pin QFN

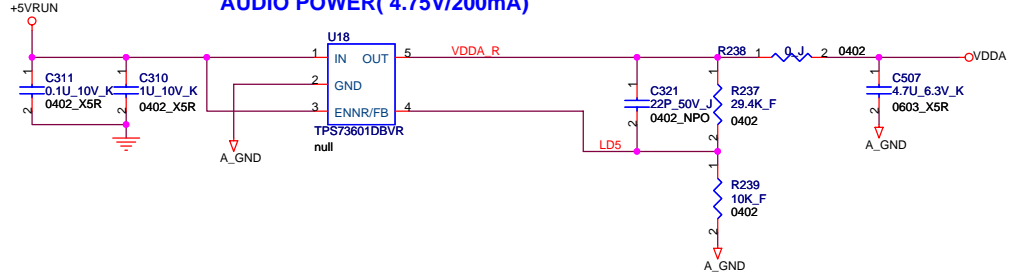


R5449 is required only if Q62 can not dissipate the required power

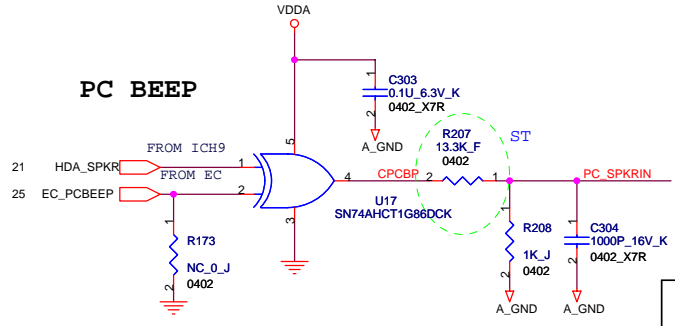




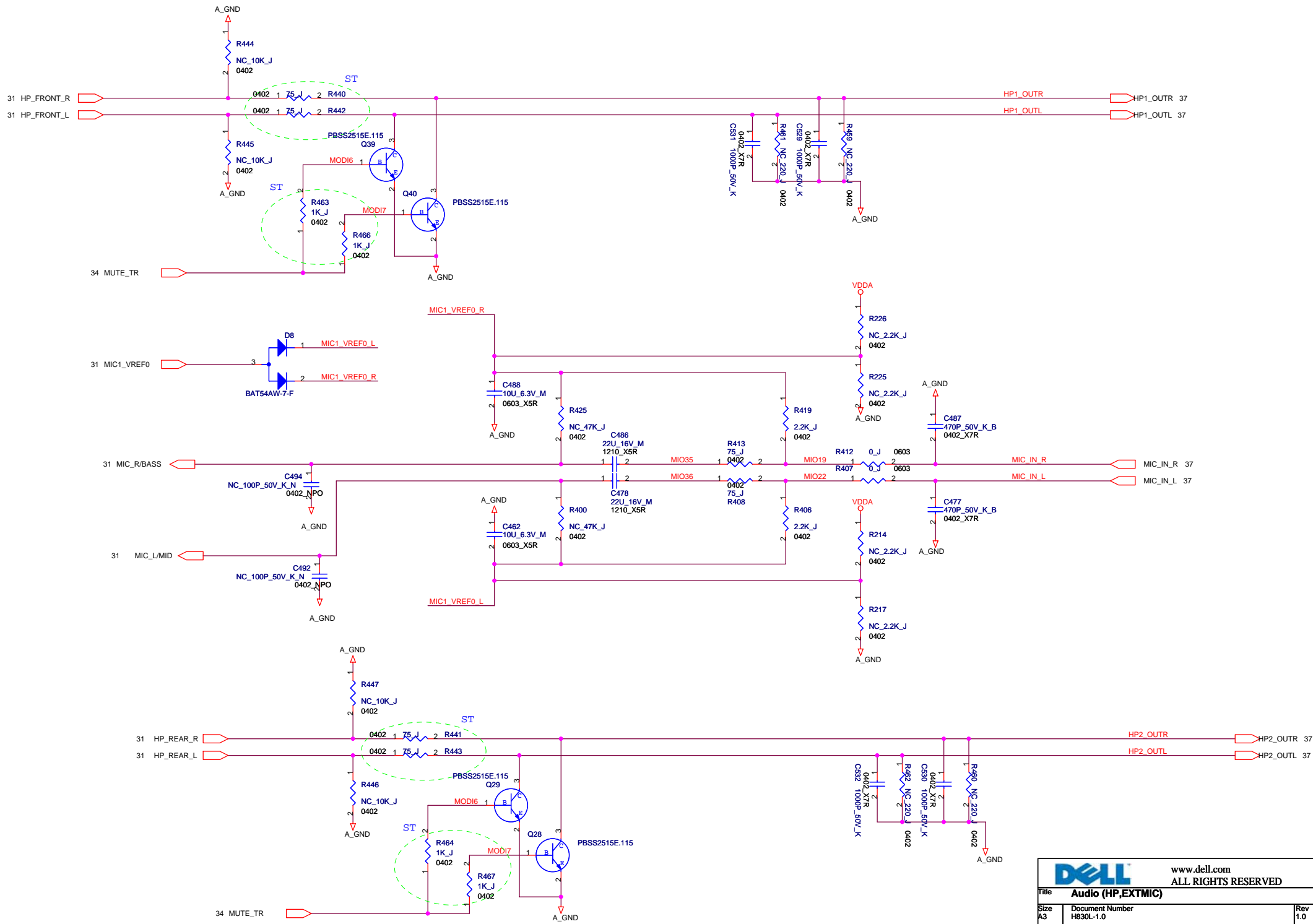
**AUDIO POWER (4.75V/200mA)**

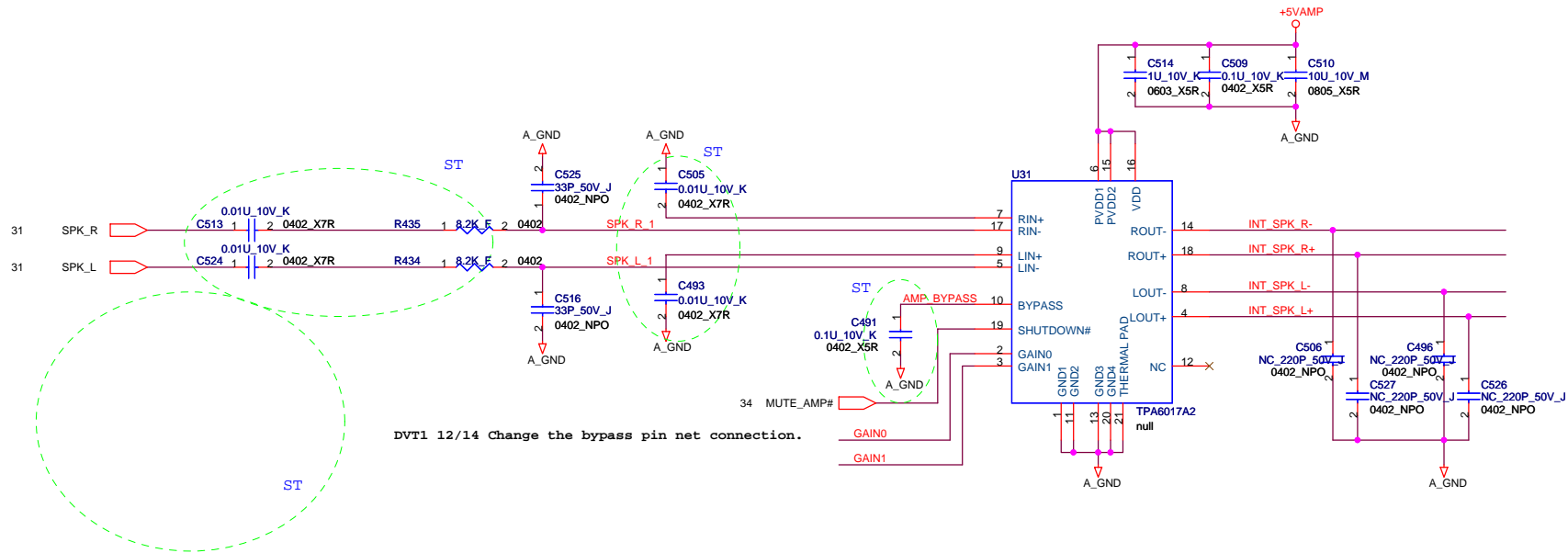
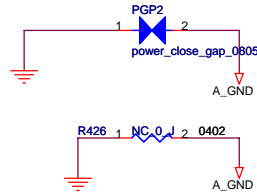
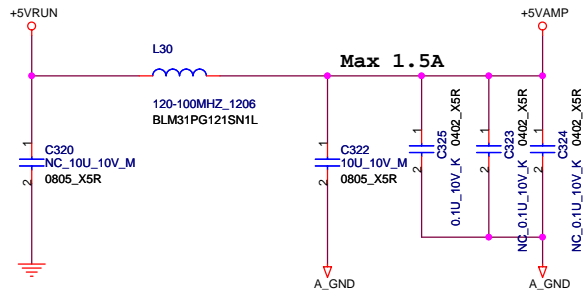


**PC BEEP**

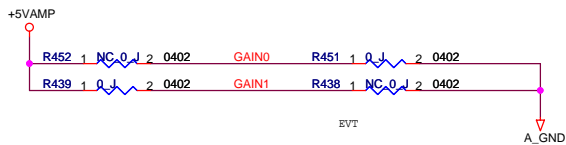


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Title	Audio (CODEC & POWER)				
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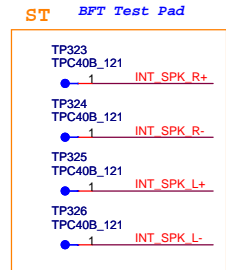
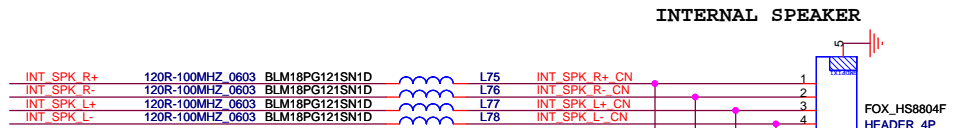
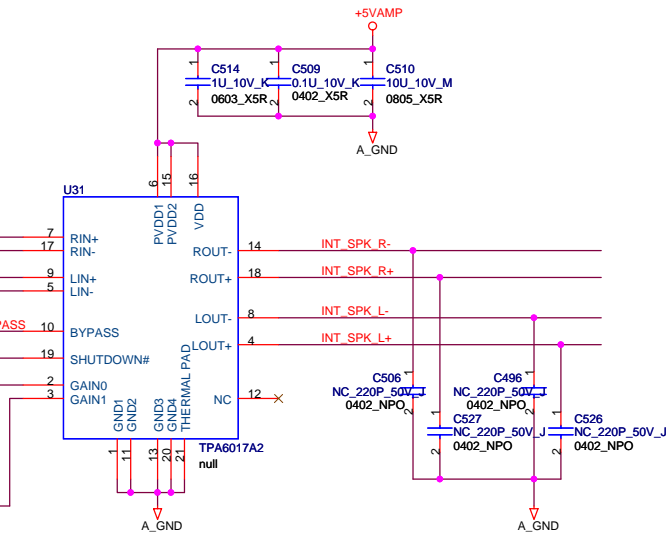
DVT1 12/14 Change the bypass pin net connection.

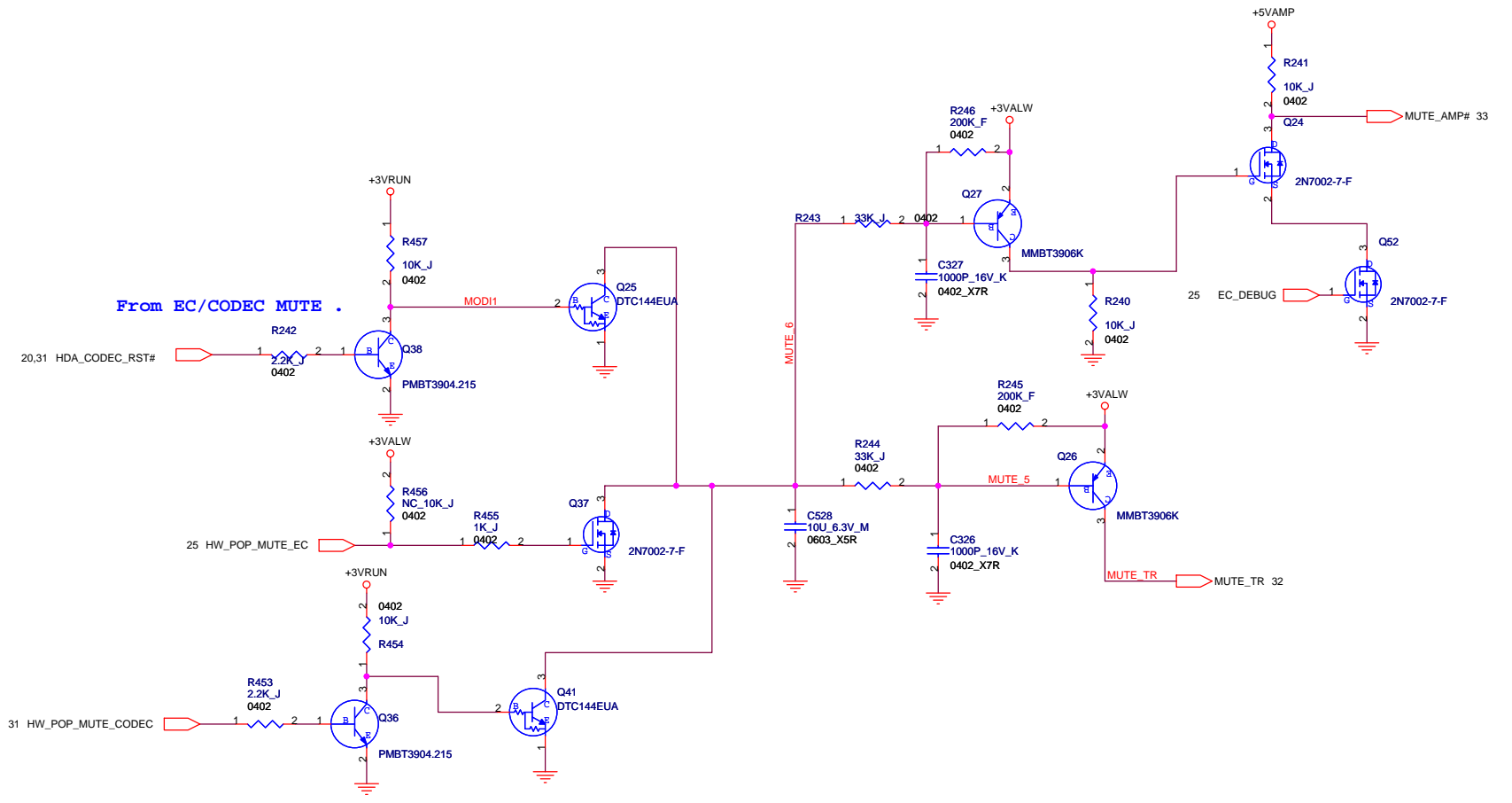


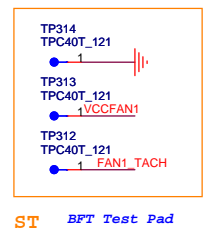
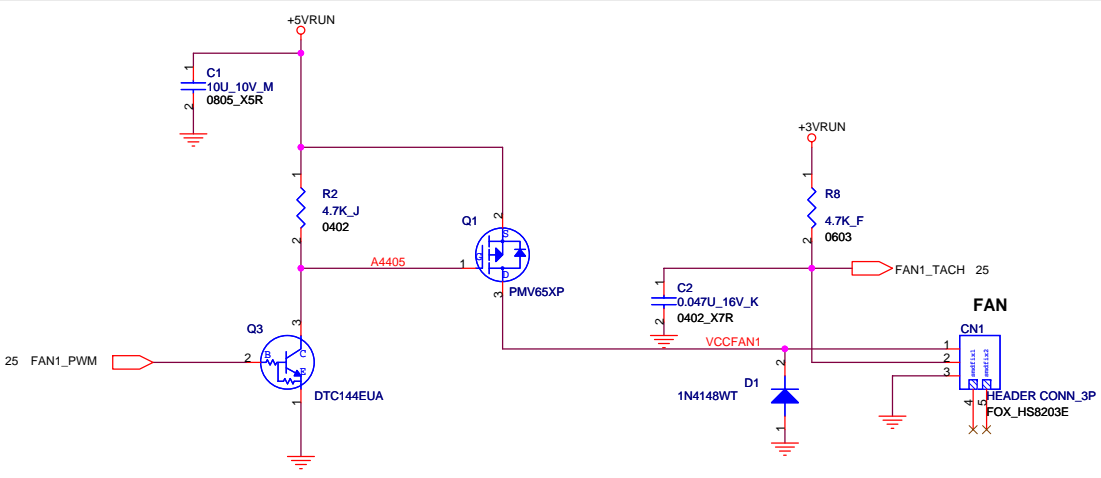
**SPEAKER AMP**

	GAIN0	GAIN1
6 dB	0	0
10 dB	0	1
15.6 dB	1	0
21.6 dB	1	1

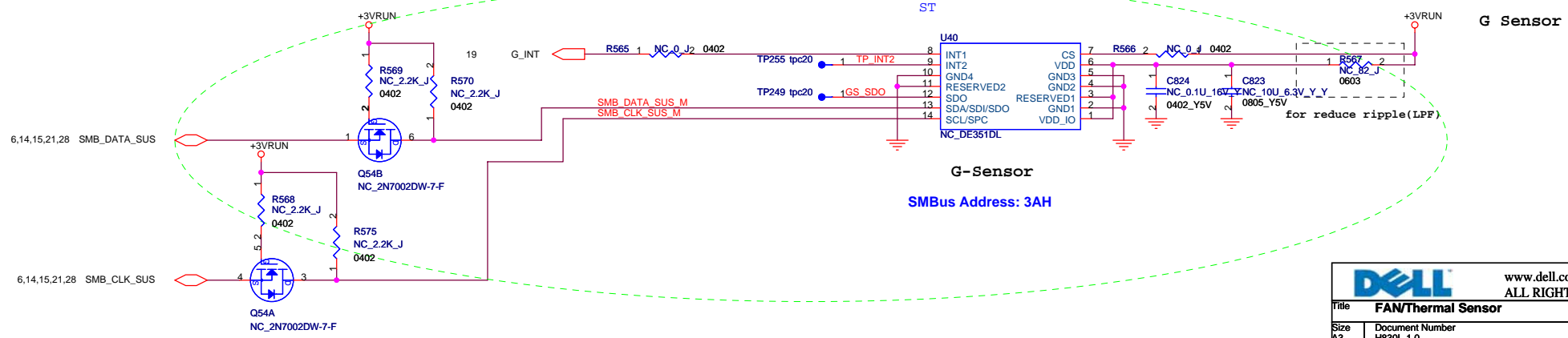
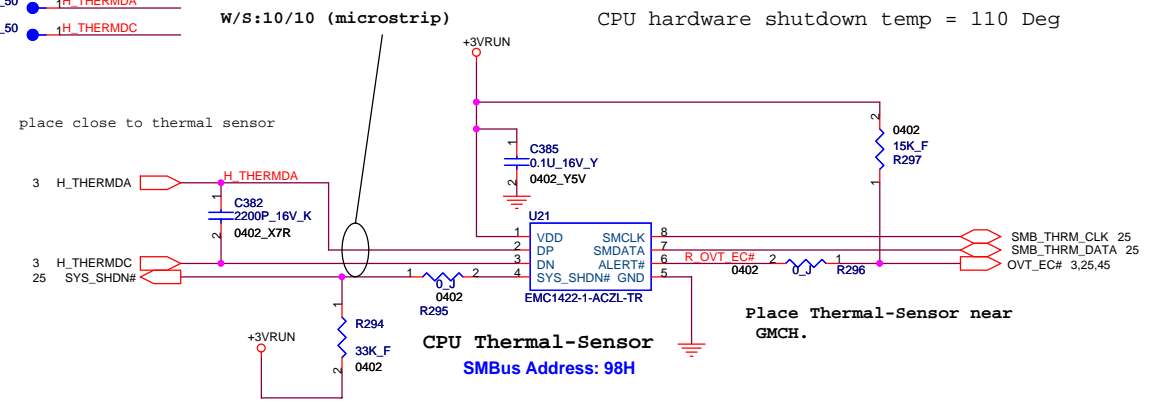
$dB = 20 \log Gain$   
 If set 10dB, gain is 3.162.  
 $P_o = \{(1.2V_{rms} * 3.162)^2\} / 4 = 3.599 W$

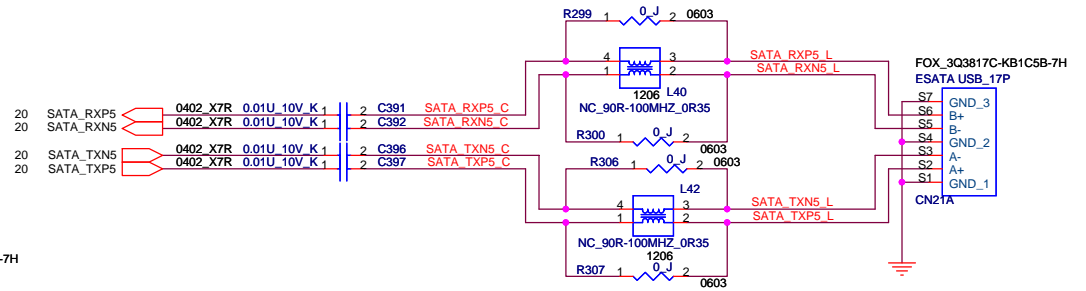
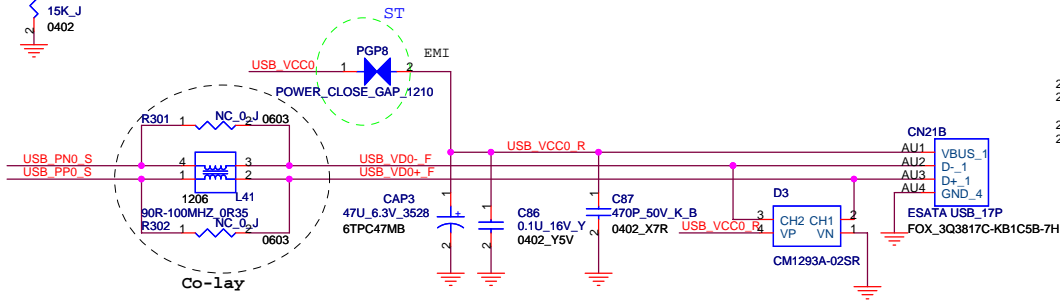
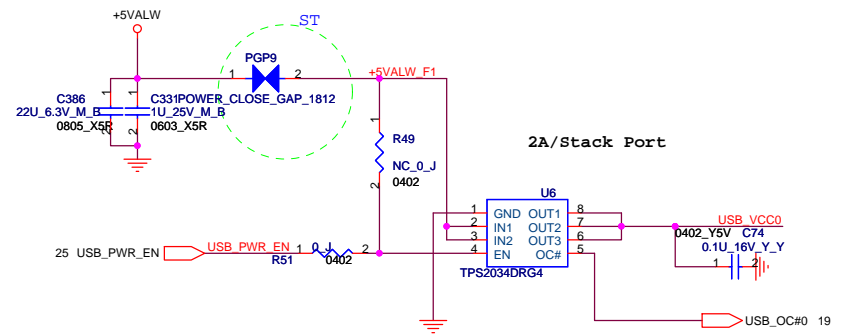
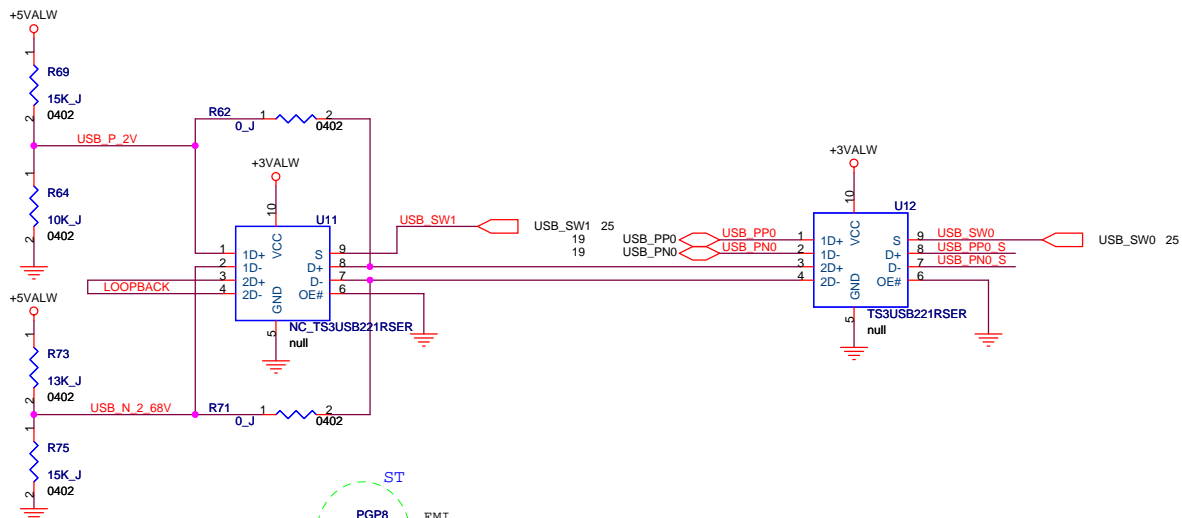




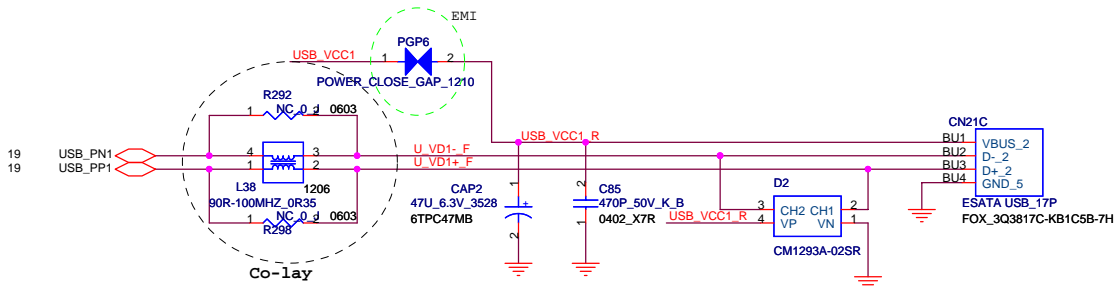


TP109 tpc40t\_50 ● H\_THERMDA  
 TP110 tpc40t\_50 ● H\_THERMDC

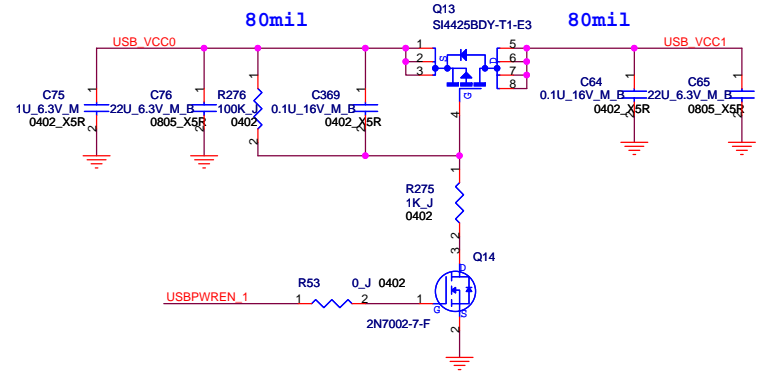




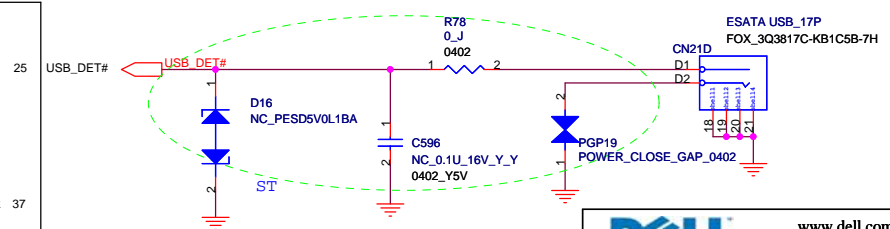
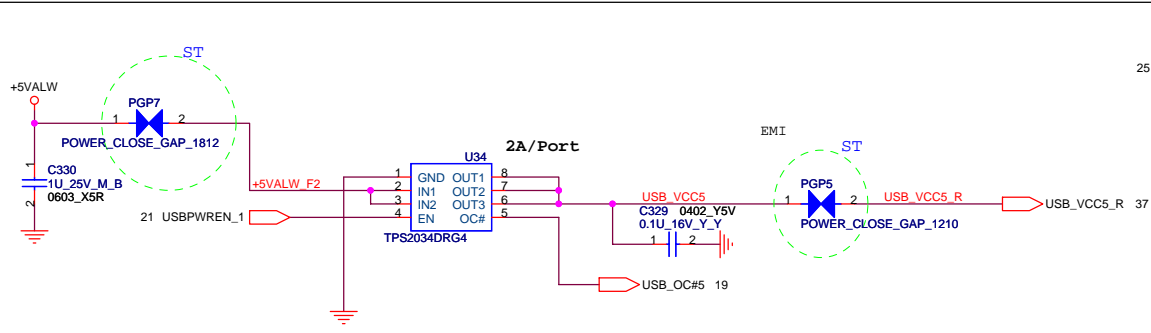
For ESD.



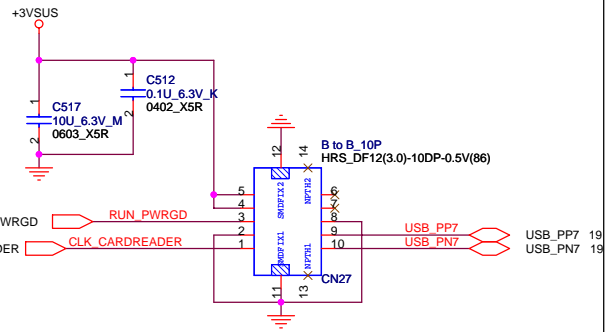
For ESD.



## USB + e-SATA on MB





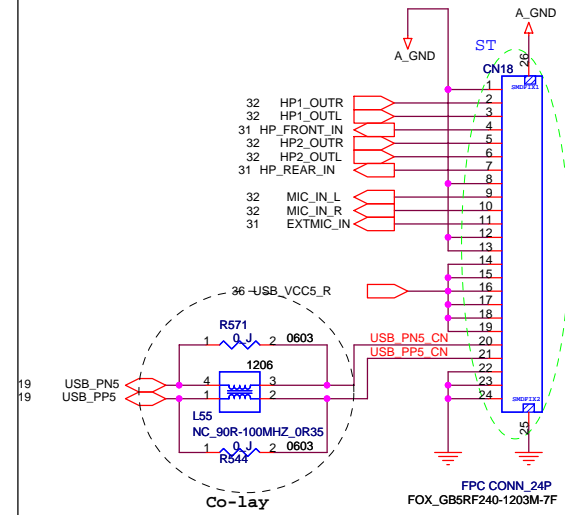


Cardreader Board

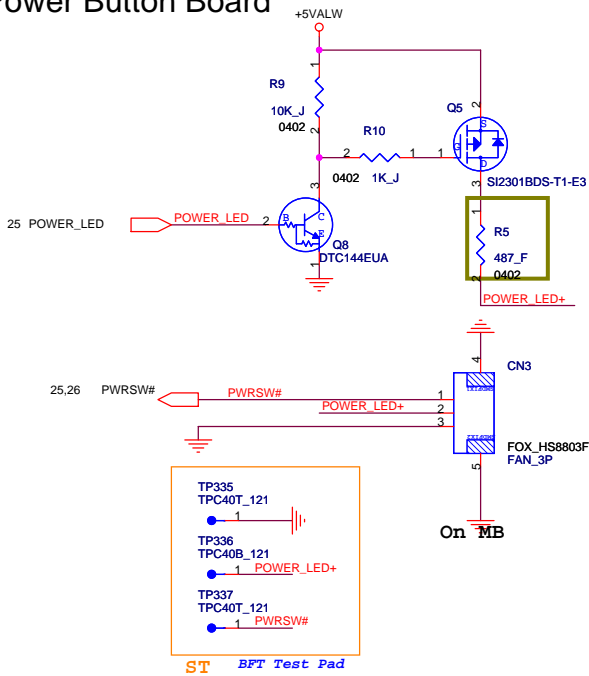
ST

WWAN Board

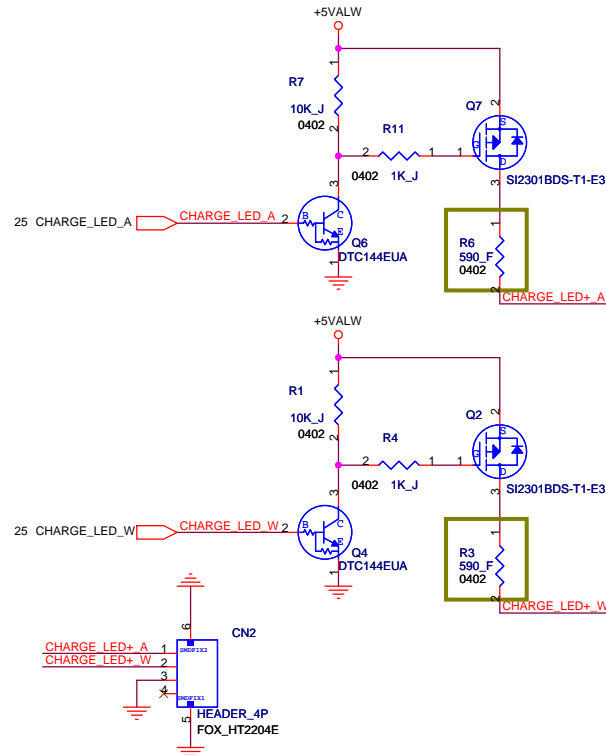
### Audio\_USB Board On MB



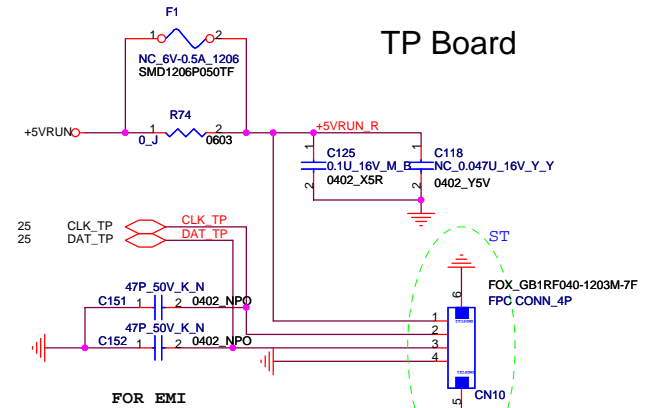
### Power Button Board



### LED Board

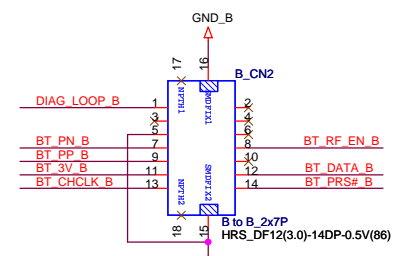
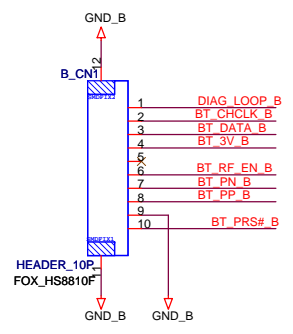
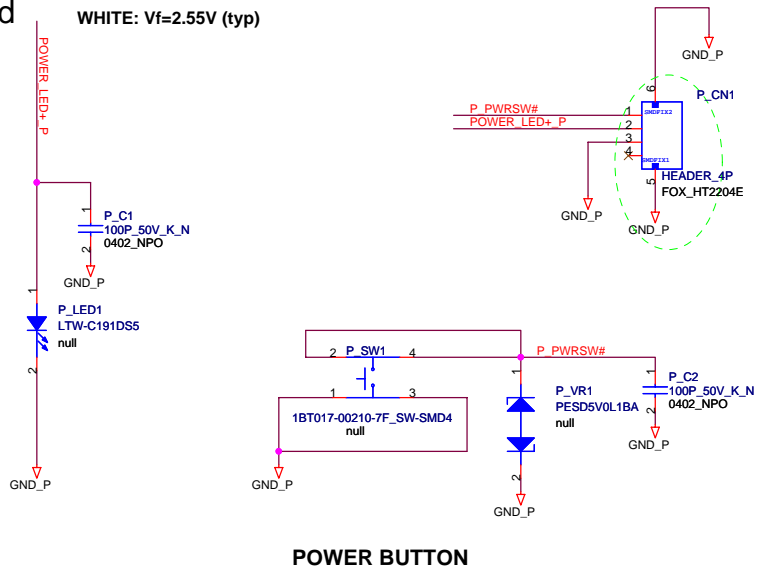


### TP Board

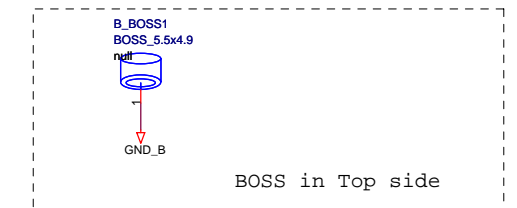


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Title <b>DB board connector (MB)</b>			
Size A3	Document Number H830L-1.0	Rev 1.0	
Date:	Wednesday, April 08, 2009	Sheet 37	of 50

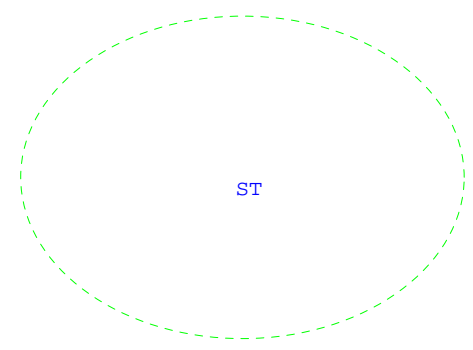
# Power Button Board



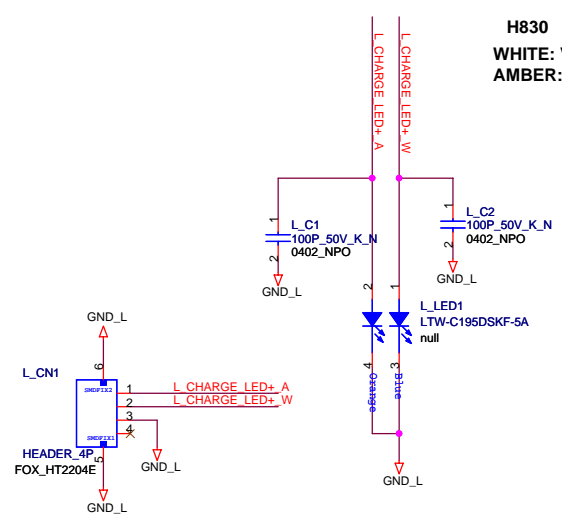
# Bluetooth CONN.



# Bluetooth Board



# LED Board



**Adaptor**  
19.5V  
65W

**MAX 8731A**  
SMBus L2  
Battery Charger  
Switch Mode  
PAGE 44

**Battery Pack**  
56Wh  
85Wh

**MAXIM**  
**MAX17020**  
Switch Mode  
For System Power  
PAGE 45

ON1 LDO  
ON2 PGOOD1  
PGOOD2

**TI**  
**TPS51117RGYRG4**  
Switch Mode  
For System CPUVIO  
PAGE 46

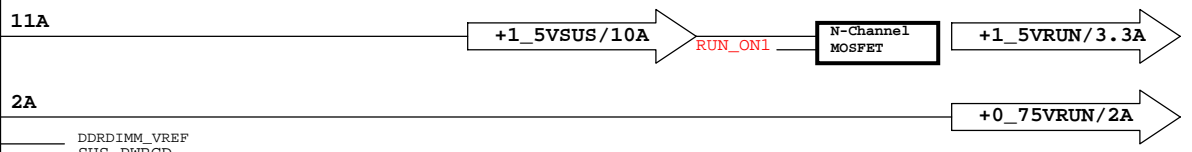
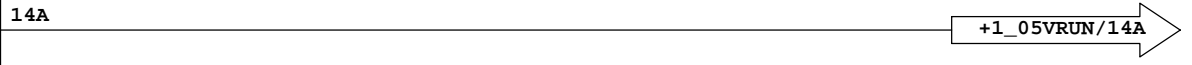
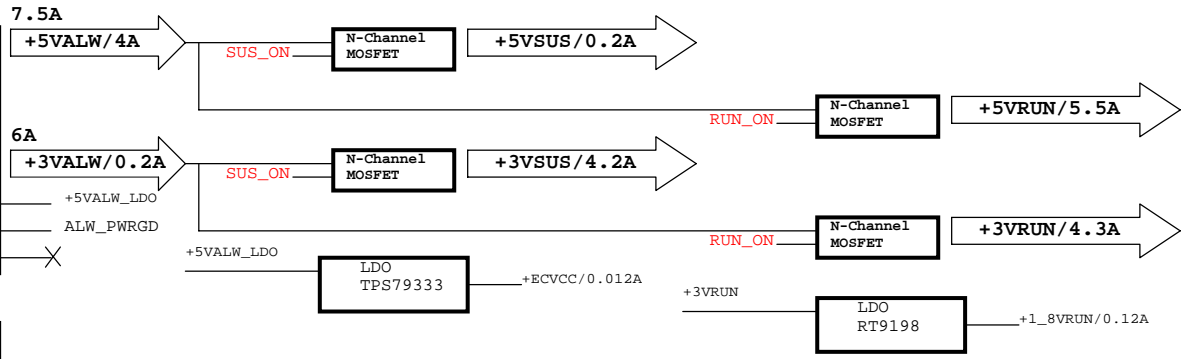
EN/PSV PGOOD  
RUN\_PWRGD

**MAXIM**  
**MAX17000**  
Switch Mode  
For DDR3  
PAGE 47

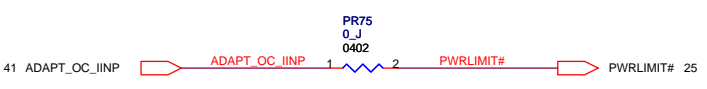
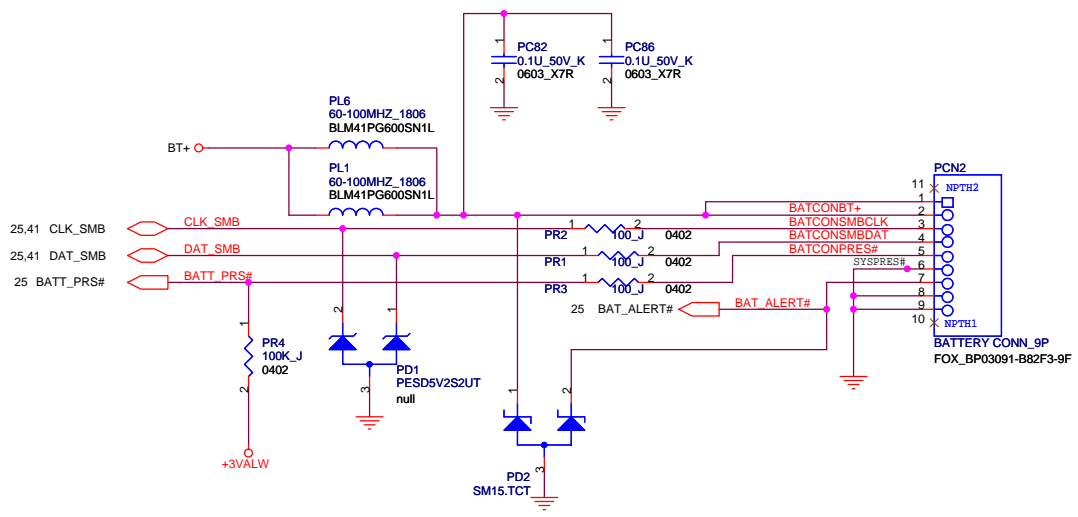
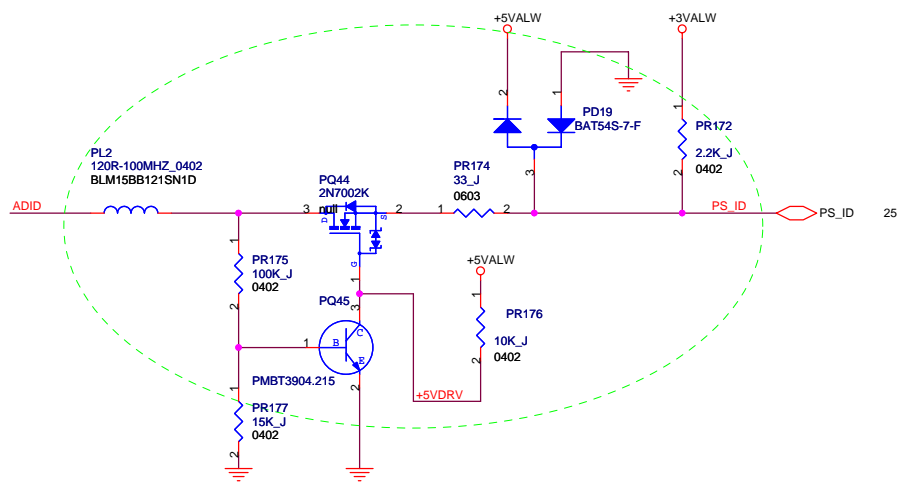
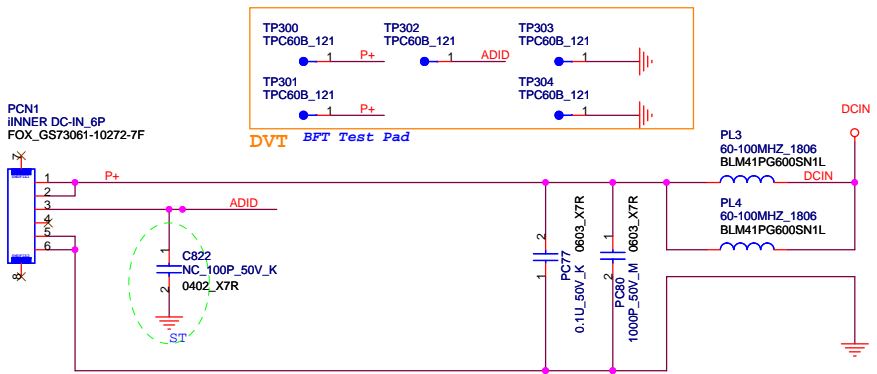
SHDN# VTRR  
STDBY# PGOOD1  
PGOOD2

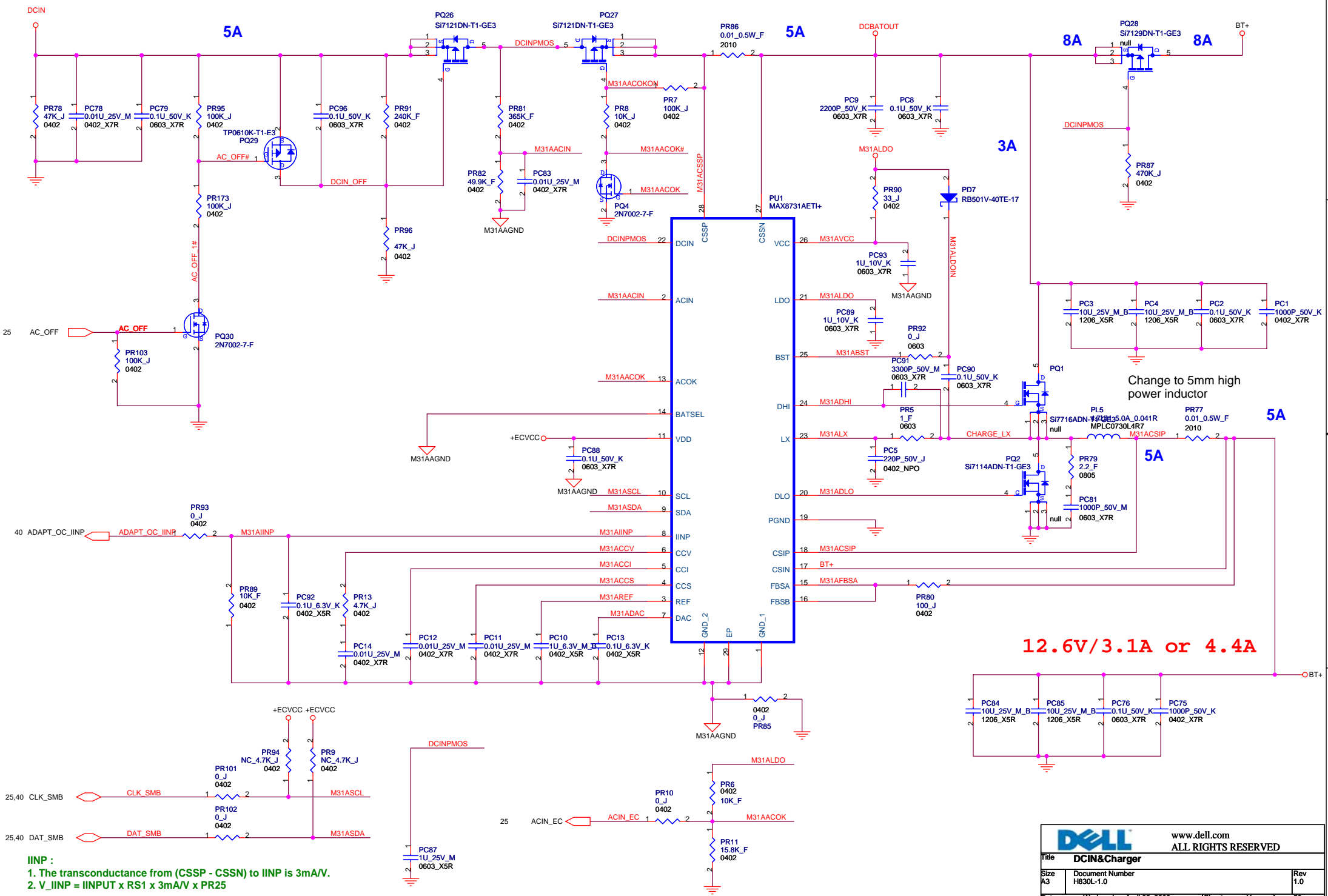
**INTERSIL**  
**ISL6266A**  
Switch Mode  
For CPU Core  
PAGE 48

CLK\_EN#  
VR\_ON PGOOD  
IMVP\_OK



<http://www.fangyuannb.com> <http://shop63900485.taobao.com>

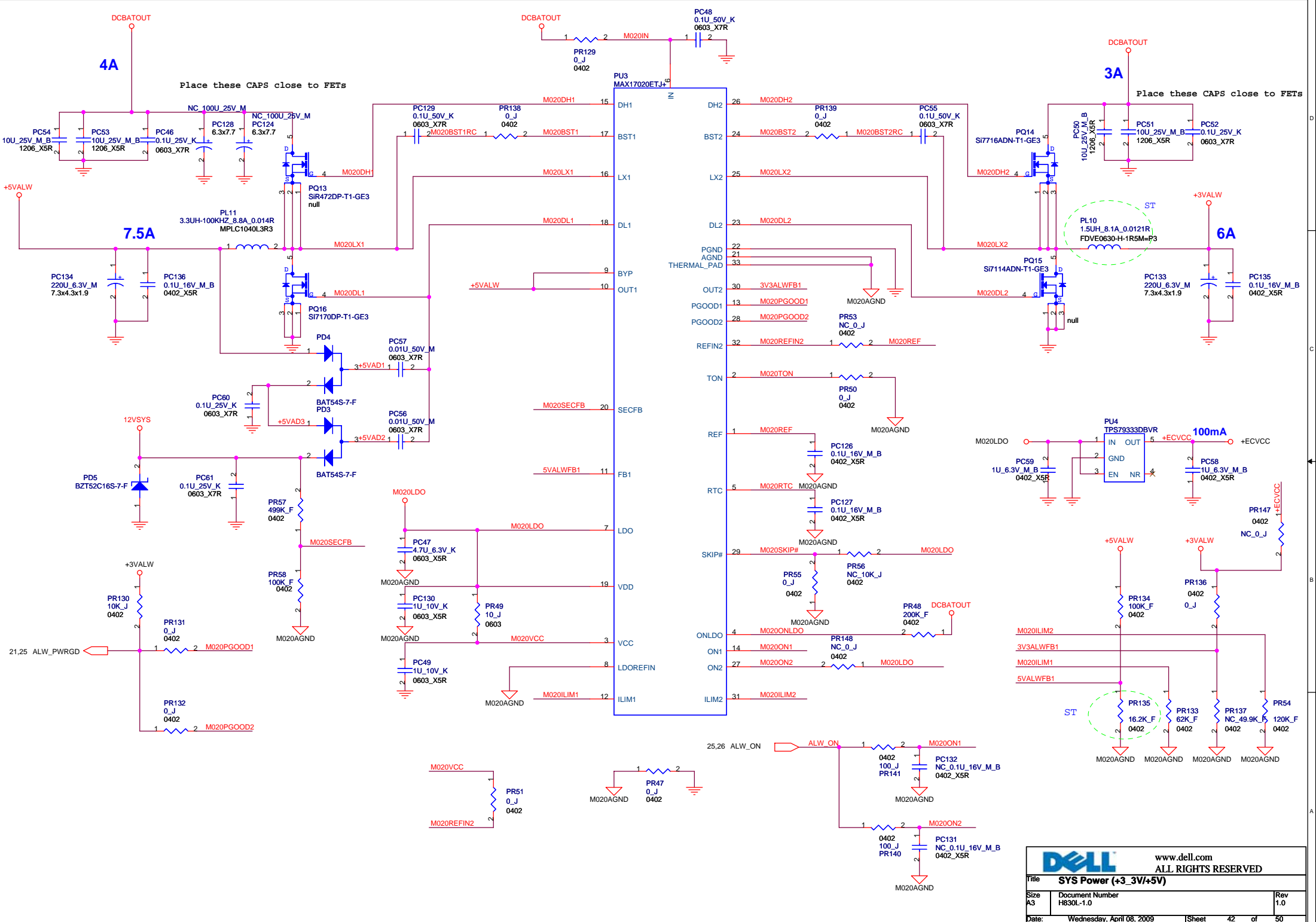


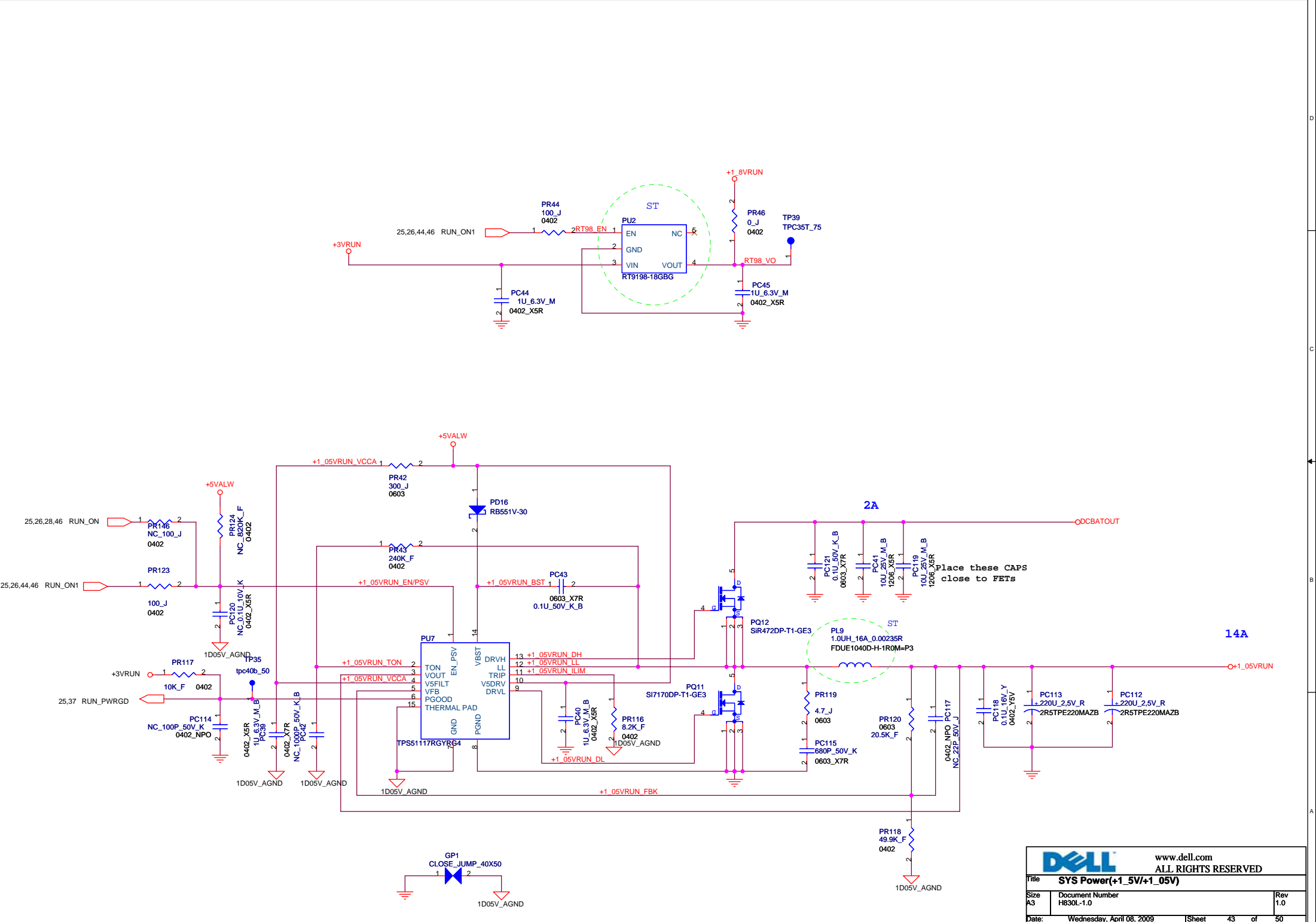


**IINP :**  
 1. The transconductance from (CSSP - CSSN) to IINP is 3mA/V.  
 2.  $V_{IINP} = IINP \times RS1 \times 3mA/V \times PR25$

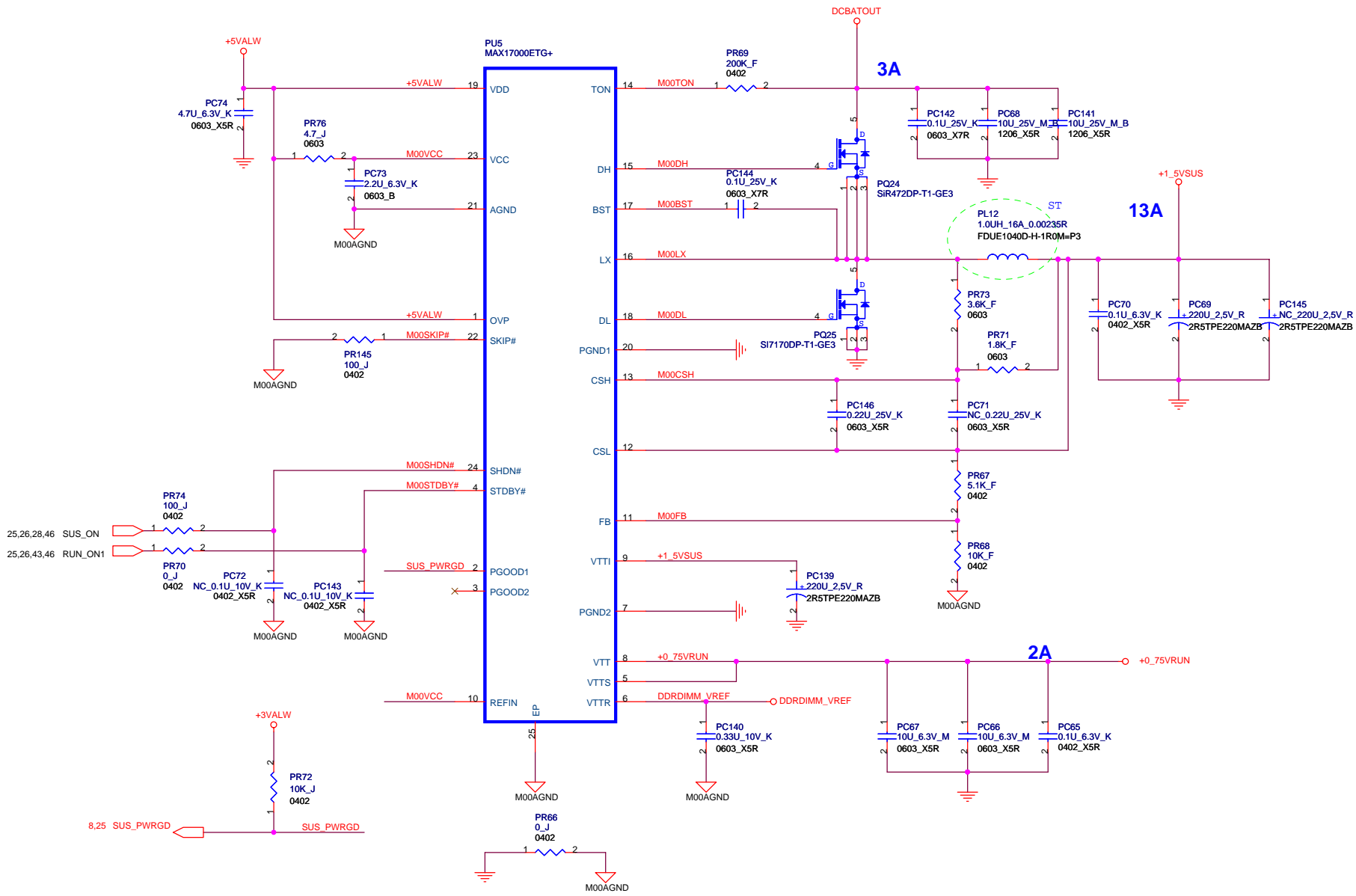
**12.6V/3.1A or 4.4A**

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Title <b>DCIN&amp;Charger</b>			
Size A3	Document Number H830L-1.0	Rev 1.0	
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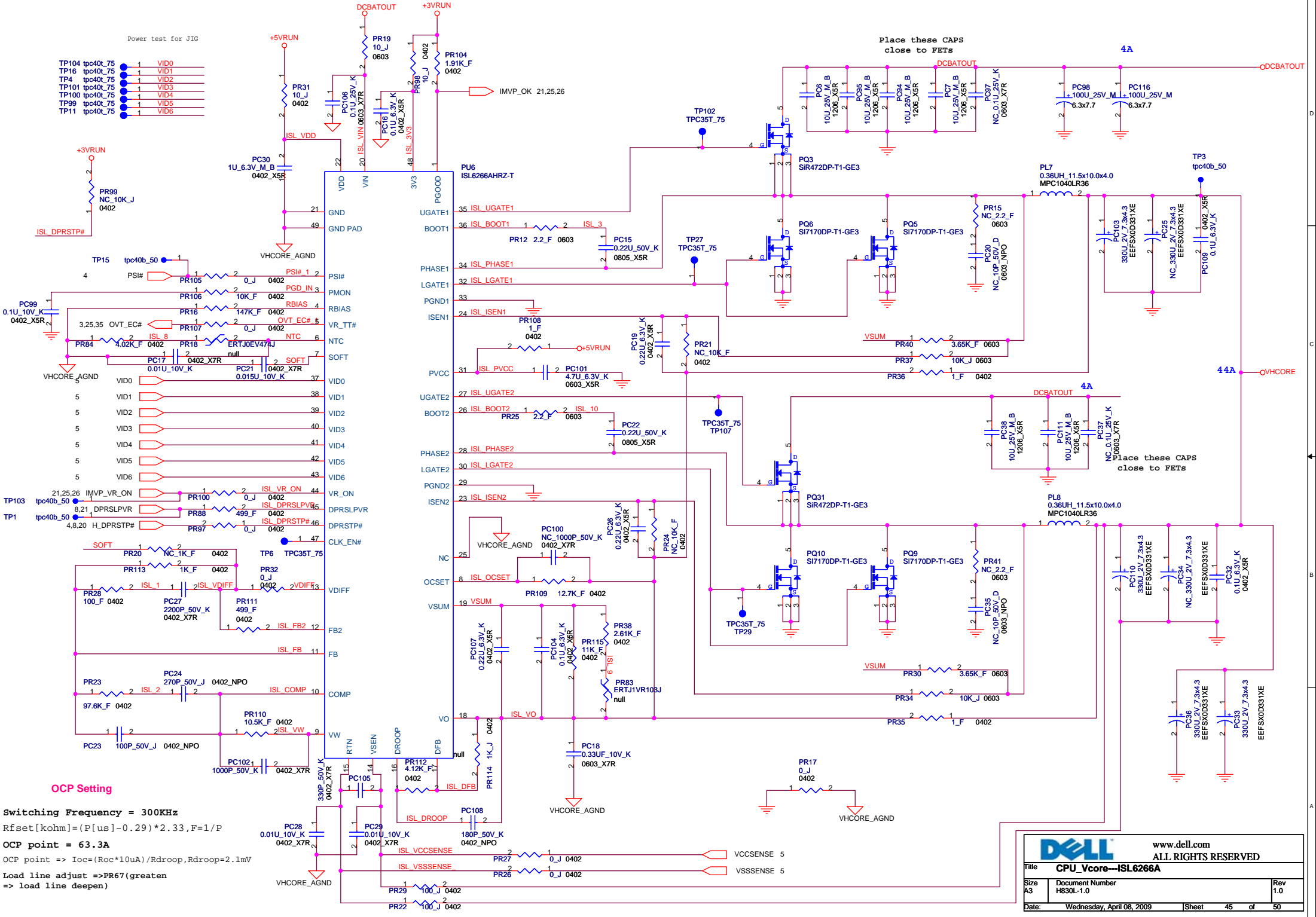






Power test for JIG

- TP104 tpc40l\_75 1 VID0
- TP16 tpc40l\_75 1 VID1
- TP4 tpc40l\_75 1 VID2
- TP101 tpc40l\_75 1 VID3
- TP100 tpc40l\_75 1 VID4
- TP99 tpc40l\_75 1 VID5
- TP11 tpc40l\_75 1 VID6

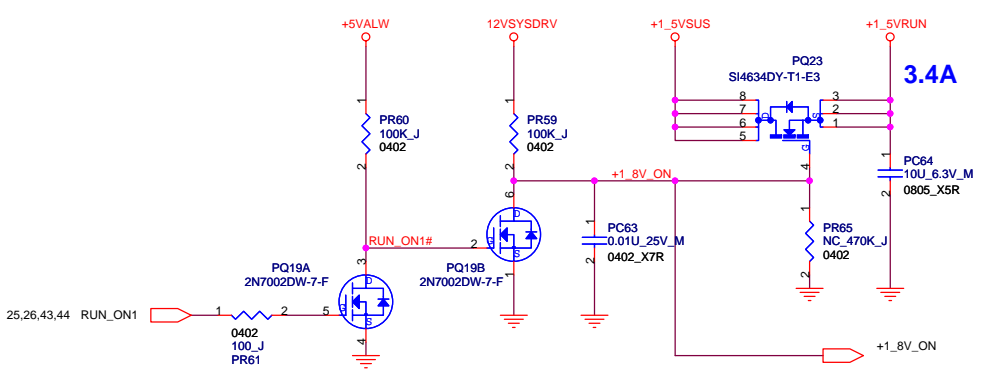
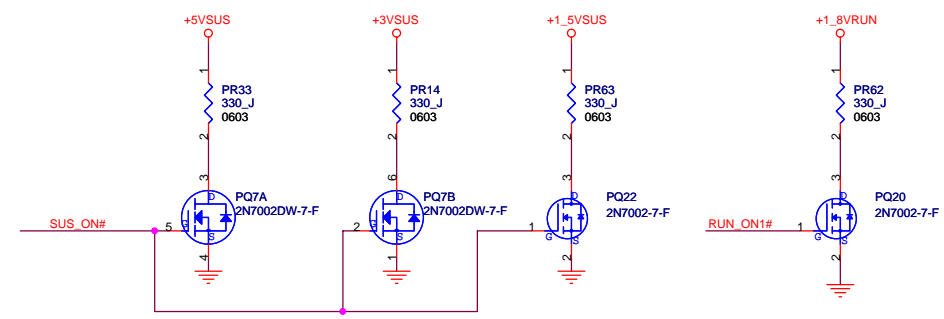
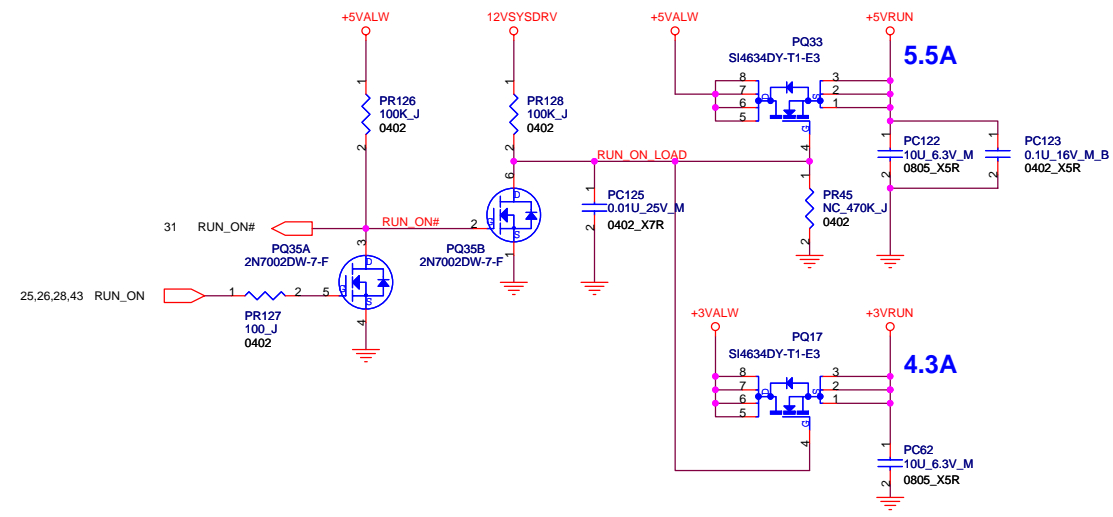
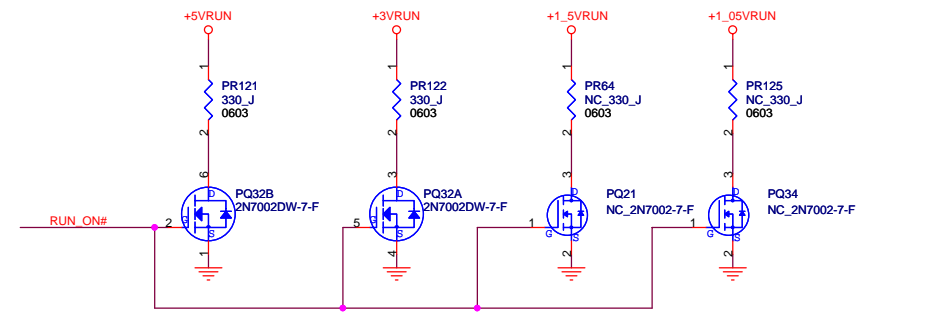
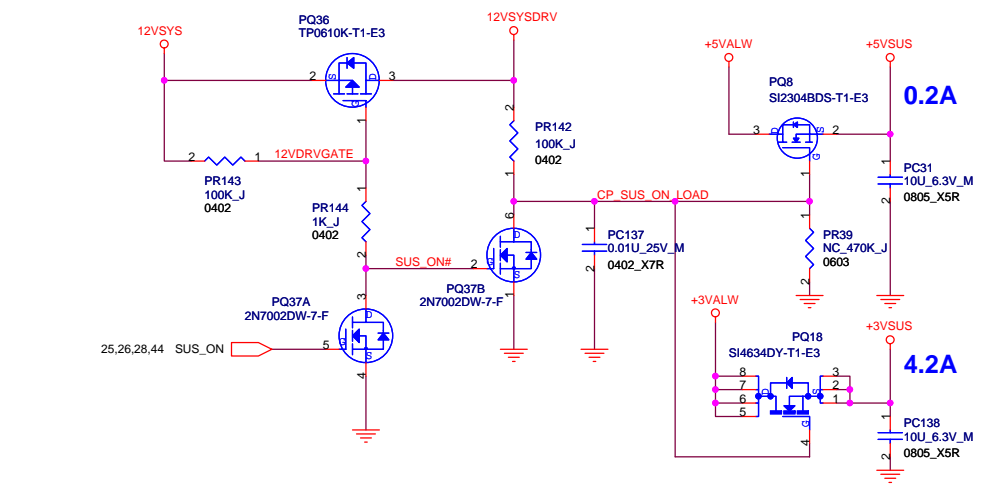


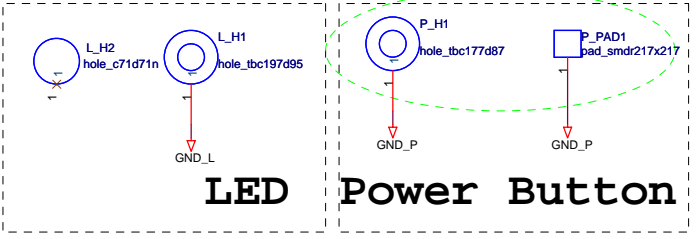
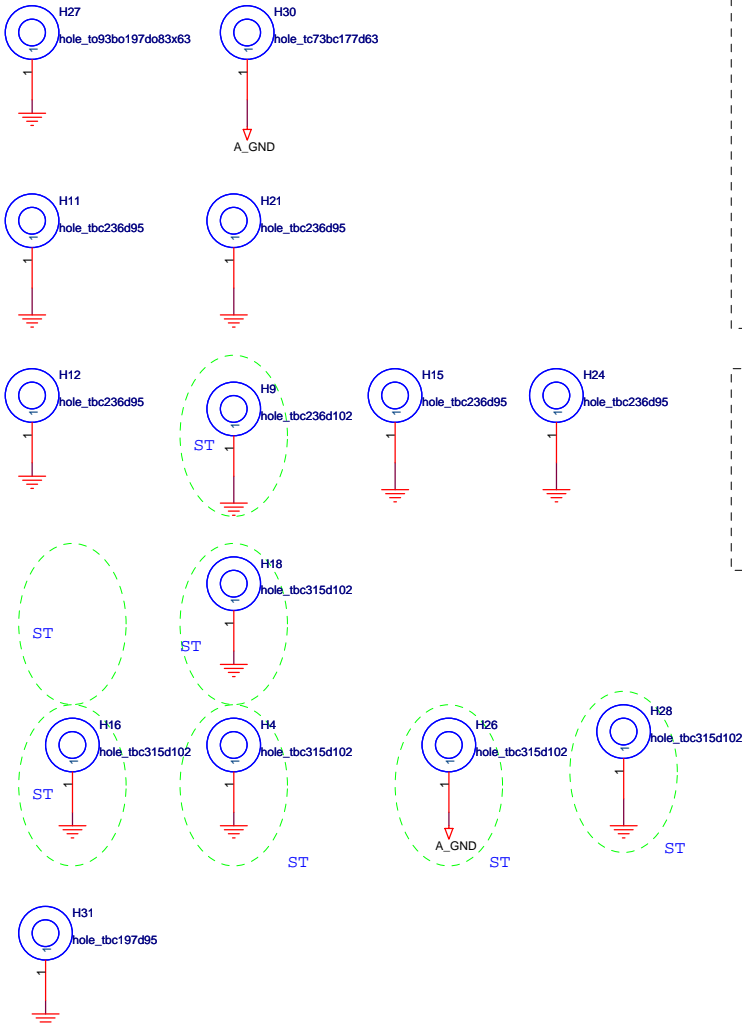
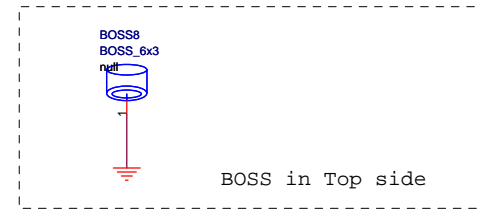
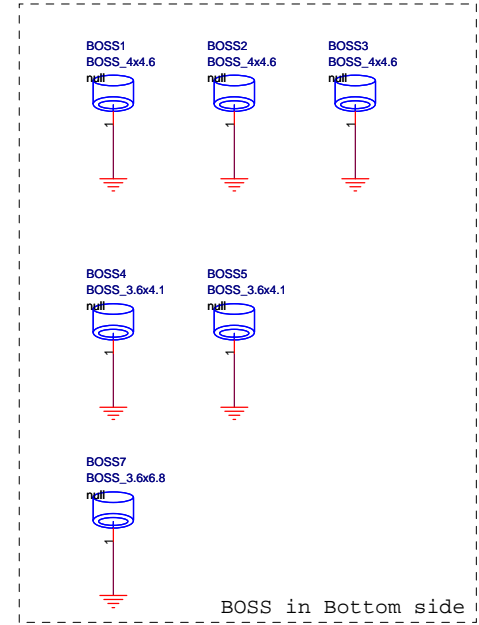
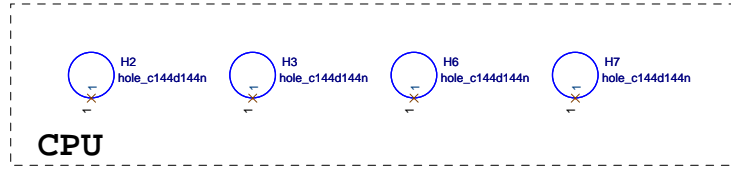
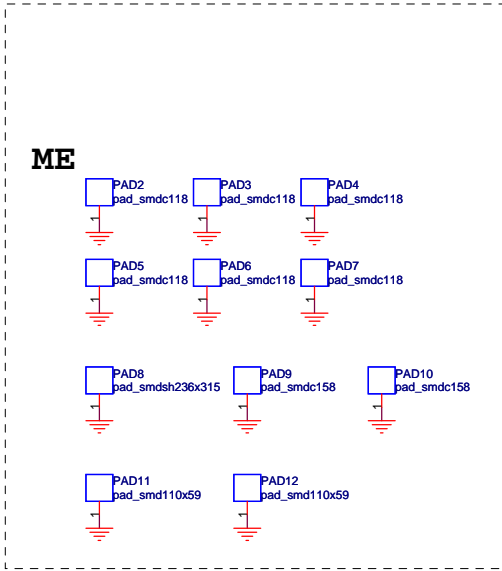
**OCP Setting**

**Switching Frequency = 300KHz**  
 $R_{fset} [kohm] = (P_{us} - 0.29) * 2.33, F=1/P$   
**OCP point = 63.3A**  
 $OCP\ point \Rightarrow I_{oc} = (R_{oc} * 10uA) / (R_{droop} * R_{droop} = 2.1mV)$   
**Load line adjust => PR67(greaten => load line deepen)**

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Title <b>CPU_Vcore-<u>ISL6266A</u></b>		
Size <b>A3</b>	Document Number <b>H830L-1.0</b>	Rev <b>1.0</b>
Date: <b>Wednesday, April 08, 2009</b>	Sheet <b>45</b>	of <b>50</b>





## H830-L EVT -> DVT

### (2008/12/29)

- P.25 Change KB CN: CN13 to Stuff; CN12 to NC for ME requirement.
- P.28 Change Express Card CN: CN14, CN17 to Foxconn for ME requirement.
- P.37 Change WWAN CN: CN8 to Stuff; CN7 to NC for ME requirement.
- P.41 Change PR87 to 470K from 100K to fix part number error.
- P.41 Change PR6 to 10K from 100K to fix part number error.
- P.41 Change PR89 to 10K from 8.45K to fix part number error.
- P.41 Change PR77, PR86 to CYTEC from WALSIN for purchase requirement.
- P.42 Change PR136 to 27K from 33K for fine tune voltage.
- P.42 Change PR56 to NC ; PR55 to stuff to fix 3V/5V over-spec issue.
- P.43 Change PQ11 to SI7170DP-T1-GE3 from Sir466DP-T1-GE3.
- P.45 Change PR108, PR36, PR35 to lohm from 100K to fix part number error.
- P.45 Change PR20 to NC for ISL6266A improved by internal circuit.

### (2008/12/31)

- P.25/29/30/33/35/37/40 Add test point TP300~TP337 for DVT BFT test.

### (2009/01/06)

- P.18 Change L47 vender to PSL vender Murata.
- P.29 Add TP338~TP to solve PC\_BEEP issue.
- P.33 Add Q50, R468,R560,C816,C792 to solve PC\_BEEP issue.
- P.34 Add Q41 to solve speaker mute issue.
- P.37 Change CN3 to 4pin CN from 3pin to avoid confusing with LED Brd CN.
- P.38 Reverse L\_SMD1 to follow cable pin definition.

### (2009/01/08)

- P.20 Change RTC battery part number to CR-2032L/BN from CR-2032L/BE for PUR.
- P.40 Add PU PR172 for PS\_ID.
- P.24 Change CN26 (HDD CN) footprint for ME request.
- P.24 Change CN26 (HDD CN) footprint for ME request.
- P.19 Change R124 to NC for no necessary.

### (2009/01/09)

- P.14/15 Change C221,C196,C219,C220,C202,C178,C197 to stuff to follow H830H.
- P.38 Change R299,R300,R306,R307 to Stuff; L40,L42 to NC to solve e-sata issue.
- P.20 Change C423, C424 to 12pF from 15pF for crystal Y2 precision.
- P.30 Change C48 to 15pF, C47 to 18pF for crystal Y1 precision.
- P.25 Change C481 to 15pF, C475 to 15pF for crystal Y4 precision.
- P.06 Change C425 to 27pF for crystal Y3 precision.
- P.21 Change USBPWREN\_1 to SB GPIO28; GPIO22 connect +3VRUN to solve USB S3 auto resume issue.
- P.40 Change TP300, TP301,TP302,TP303,TP304 to TPC60B\_75 for TE request.
- P.41/42 Change PQ2, PQ15 to Si7114ADN-T1-GE3 for power request.
- P.43 Change PQ11 to SI7170DP-T1-GE3 for power request.
- P.34 Add Q52 and connect EC\_DEBUG to EC to solve PC\_BBEP issue.

### (2009/01/09-2)

- P.30 Change Y1 to X5H025000FC1H-H for vender suggest.
- P.20 Change RTC Battery CN25 to BB10201-C1401-7F for ME request.

### (2009/01/12)

- P.36 Change U6,U34 to HF part RT9703GS for vender suggest.

### (2009/01/14)

- P.38 Change L\_SMD1 to L\_CN1 for ME request.
- P.48 Del H1,H10 & H23 for ME request.
- P.43 Change PU2 to RT9198-18PBG from RT9198-18GBG for PUR request.
- P.36 Change U6,U34 back to LF part RT9703PS for vender lead time issue.

### (2009/01/16)

- P.36 Del eSATA Choke L40 and L42 for improve SI.
- P.18 Change HMDI CN CN16 to DIP type for factory EE request.
- P.37 Change PWR BTN CN CN3 to 3pin and LED Brd CN CN2 to 4pin for ME request.

### (2009/01/19)

- P.41 Add PR173 for solve PQ29 derating issue.
- P.42 Move PC124 to DCIN5VALW for power request.
- P.06 Change C425 to 33pF for crystal Y3 precision.

### (2009/01/20)

- P.43 Add PD16 for power request.
- P.08 Add U38, C818, R563,R564 to solve SUS\_PWRGD level drop issue.
- P.05 Add C819, C820, C821 for RF request.
- P.27 Del D4 and add R469, Q42 and Q43 to solve HDMI CN VCC issue.
- P.42 Del PR52 and change PR51 to 0ohm;change PR53 to NC for power request.
- P.47 Add PAD2~PAD12 for ME request.

### (2009/01/21)

- P.17 Change R269 to 62ohm and stuff R360 and Q12; add C534 to solve panel power sequence issue.
- P.36 Change USB power switch U34, U6 to TPS2034DRG4 (low Rds on).
- P.38 Add BC\_CN4 and BC\_CN3 for BT second source.
- P.52 Add PR146 NC for resevering power sequence test.

### (2009/02/02)

- P.31 Change C518 to 2.2uF from 10uF to solve S3 pop noise issue.
- P.47 Connect H30 to AGND from GND.
- P.37 Increase USB\_VCC5\_R to 6pin from 4pin and decrease AGND, GND pin to improve voltage drop.

### (2009/02/02)

- P.37 Del colay connector CN6 for ME request.

### (2009/02/05)


- P.47 Del BOSS6 for ME request.
- P.38 Add BC\_TP1, BC\_TP2.
- P.25 Change Q21B(3904) to Q53 (2N7002) to prevent current leakage.
- P. Change test point to ICT test point: TP111,TP113,TP116,TP117,TP118,TP119,TP120,TP121,TP122,TP123,TP124,TP125,TP126,TP130,TP131,TP132,TP133,TP135,TP136,TP137,TP139,TP140,TP141,TP142,TP153,TP157,TP158,TP178,TP179,TP34,TP36,TP37,TP40,TP41,TP42,TP44,TP45,TP46,TP47,TP49,TP58,TP60,TP62,TP63,TP64,TP69,TP70,TP72,TP75,TP77,TP78,TP79,TP8,TP85,TP86,TP87,TP88,TP89,TP9,TP90,TP92,TP93,TP94,TP95,
- P.35 Add U39,U40,R565,R568,R569,R570,R566,R567,C823 for G sensor function.

### (2009/02/06)

- P.47 Del BOSS6 for ME request.
- P.31 Change LDO U18 to TPS73601DBVR for current limit up to 400mA.
- P.31 Change R478 to 0ohm from 22ohm for SI.
- P.37 Add L55, R544, R571 for EMI.
- P.20 Add R465,R1305 and SATALED# for HDD LED.
- P.35 Add Q54, R575, TP255, TP249 for G sensor function.
- P.28 Add CN72, CN73 for expresscard CN second source.

### (2009/02/07)

- P.36 Change D2,D3 to PSL vender.
- P.51 Change PR136 to 0 ohm and PR137 to NC to solve +3VALW level too high issue.

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## H830-L DVT

(2009/02/10)

- P.16 Change C418,C415 & C410 to 22pF for EMI requirement.
- P.29 Add L73, L74,C772 & C817 for EMI requirement.
- P.16 Change L45,L44,L43 to BLM18BB750SN1D for RGB Tr, Tf issue.
- P.33 Del R54,R55,R56,R57 and add L75,L76,L77,L78 for EMI issue.

(2009/02/11)

- P.40 Add C822 1000pF on PCN1 pin 3 for EMI requirement.
- P.42 Change PR54 to 120k for 3.3V OCP Change.
- P.43 Change PR43 to 240k for 1.05V Frequency Change.
- P.44 Change PR43 to 1.8k for 1.5V OCP Change
- P.41 Change PQ28 to Si7129DN-T1-GE3 for Id Derating Fail
- P.44 Change PC69,PC139 to 220uF, for Power IC issue,Maxim FAE instance
- P.43 Change PC112,PC113 to 220uF, for Power IC issue,TI FAE instance.
- P.44 Change PC145(NC) to 220uF, for Power IC issue,Maxim FAE instance
- P.45 Change PC143 to 0.1uF for For Vhcore loadline and transient.
- P.45 Change PR111 to 499ohm for Vhcore loadline and transient
- P.45 Change PR112 to 4.12Kohm for Vhcore loadline and transient
- P.42 Add PR147(NC) 0ohm for +3D3VALWVO from +ECVCC,for PT energy star test.
- P.42 Add PR148(NC) 0ohm for M020ON2 from M020LDO,for PT energy star test.

(2009/02/12)

- P.30 Change R26 to 1.1K from 1.24k for LAN SI issue.

(2009/02/13)

- P.38 Add BC\_BOSS1 for BT2 Brd nut.
- P.14/15 Add C535,C537,C538,C317,C538,C541,C542,C540,C539,C543 for DDR EMI issue.
- P.42 Add PC146 and NC PC71 for DDR power.
- P.30 Change R26 to 1.24K from 1.1k for LAN SI issue.
- P.40 Add PCN2 toBP03091-B82F3-9F for ME request.
- P.16 Change F2 to SMD1206P035TF/16 for fuse derating issue.
- P.36 Change F5,F7 to SMD1812P260TF for fuse derating issue.

(2009/02/17)

- P.20 Change R1035,R465 to NC to reserve for SATA LED.

## H830-L PT -> ST

(2009/03/08)

- P.33 Change Q50,R468,C816,C792 to NC because new version Codec solved PC-Beep issue (PT implement. E-ECN)
- P.21 Change RTC battery part number to CR-2032L/BN from CR-2032L/BE for PUR request.
- P.35 Change U40 G-sensor part number to DE351DL for request.
- P.41~45 Remove Power open gap PJ1,PJ2,PJ3,PJ4,PJ5,PJ6,PJ7,PJ8,PJ9,PJ10,PJ11,PJ12,PJ13,PJ14,PJ15,PJ16,PJ17 for power request.
- P.42 Change PR135 to 16.2K ohm to solve +5VALW voltage too high issue.

(2009/03/15)

- P.42 Change PR135 to 16.2K ohm to solve +5VALW voltage too high issue.
- P.17 Change R38 to 51K and C534 to 0.015uF tol solve LCD power sequence issue.
- P.25/26/37 Change CN13,CN29,CN18,CN10 material to met tin for ME request.
- P.40 Add PR175, PR177, PQ45,PQ44,PR176, PD19,PR174, and del PD5; change C822 to NC\_100pF for AD\_ID(PS\_ID) protection.
- P.18 Change Q31 to 2N7002K for HDMI detection pin ESD protection.
- P.36 Reserve D16 PESD5V0L1BA NC for USB port detection pin ESD.

(2009/03/16)

- P.38 Change P\_SMD1 to P\_CN1 for ME request.

(2009/03/16)

- P.17 Add fuse F8 for LVDS power protection.

(2009/03/17)

- P.17 Add fuse F8 for LVDS power protection.
- P.37 Change CN8 to 18pin and del C368,C498,C73,C72 for del PCIe interface of WWAN DB.

(2009/03/26)

- P.17 LVDS CN, change +3VRUN to pin 10 from pin4 to prevent DCBATOUT short to +3VRUN.
- P.47 Del H20 and modify H4,H18,H26,H9,H16,H28 for ME request.
- P.20 Del C246,C247 for del PCIe interface of WWAN DB.
- P.04 Add C72 to solve H\_GTLREF Vpp over-spec issue.
- P.47 Modify P\_H1 and P\_PAD1 for ME request.
- P.37 Change WWAN DB CN +3VALW to 8pin from 7pin.
- P.27 Add CN74 WLAN CN second source colay with CN17 for ME request.

(2009/03/27)

- P.17 LVDS CN, change +3VRUN to pin 10 from pin4 to prevent DCBATOUT short to +3VRUN.

(2009/03/27-2)

- P.37 Modify WWAN CN8 pin define.
- P.26 LVDS CN, change +3VRUN to pin 4, pin3 to NC prevent DCBATOUT short to +3VRUN.

(2009/03/27-3)

- P.31 Change R207 to 13.3K for Realtek recomment.

(2009/03/31)

- P.18 Change R386 to NC for 27MHz XTAL.
- P.33 Change R435,R434 to 8.2K for 6ohm SPK.
- P.14/15 Change DDR CN package: CN24 to AS0A626-U4RN-4F, CN23 to AS0A626-U8RN-4F for SMT.
- P.43 Change PU2 to RT9198-18GBG (HF part)for PUR request.

(2009/04/02)

- P.33 Change C81,C82,C83 and C84 to NC for EMI request.
- P.33 Del Q50,R468,R560,C816,C792 to del reservation for PCBeep.

(2009/04/03)

- P.16 Change L43,L44,L45 to BLM18BB470SN1D to solve VGA SI issue.
- P.19/25/38 Del CN8,C78,C225,C77 add TP34,TP36,TP37 for WWAN CN PCIe interface cancelled.

(2009/04/05)

- P.40 Change BFT Testpoint TP300, TP301,TP302, TP303,TP304 to TPC60B\_121 for TE request.
- P.25/35/37 Change BFT Testpoint TP327,TP328,TP329,TP330,TP333,TP334,TP312, TP313,TP314,TP335,TP337 to tpc40t\_121 for TE request.
- P.29/30/33/37 Change BFT Testpoint TP305,TP306,TP307,TP308,TP310,TP338,TP339, TP340,TP341,TP342,TP343,TP344,TP345,TP346,TP309,TP311 TP315,TP316,TP317, TP318,TP319,TP320,TP321,TP322 ,TP323,TP324,TP325,TP326,TP336 to tpc40B\_121 for TE request.

(2009/04/08)

- P.42 Change PL\_10 to FDVE0630-H-1R5M=P3 (HF part) for power request.
- P.43 Change PL\_9 to FDUE1040D-H-1R0M=P3 (HF part) for power request.
- P.44 Change PL\_12 to FDUE1040D-H-1R0M=P3 (HF part) for power request.

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**(2009/04/08)**


- P.17 Change F8 to 467002 (32V-2A\_0603) forLVDS VCC protection.
- P.38 Del BC\_CN4,BC\_CN3,BC\_BOSS1,BC\_TP1,BC\_TP2 for BT2 board is not necessary.

**(2009/04/09)**

- P.35 Change R568,R575, Q54,R569,R570,R565,U40,C824,R566,C823,R567 to NC for cancelling support G-sensor.
- P.33 Change C513,C524,C505,C493 to 0.01uF;C491 to 0.1uF for speaker pop noise.
- P.17 Del R270 0ohm for no necessary.
- P.27 Del R39 0ohm and change R278 to close gap PGP17.
- P.11 Change R116 0ohm to close gap PGP4.
- P.36 Change R247,R47,R52 0ohm to close gap PGP5,PGP6,PGP8.
- P.36 Change F5,F7 to close gap PGP7,PGP9.

**(2009/04/10)**

- P.30 Change R48 0ohm to close gap PGP18.
- P.45 Add C596 NC and PGP19 for USB detection softstart.
- P.32 Change R463,R446,R464,R467 to 1K ohm to solve pop noise..

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