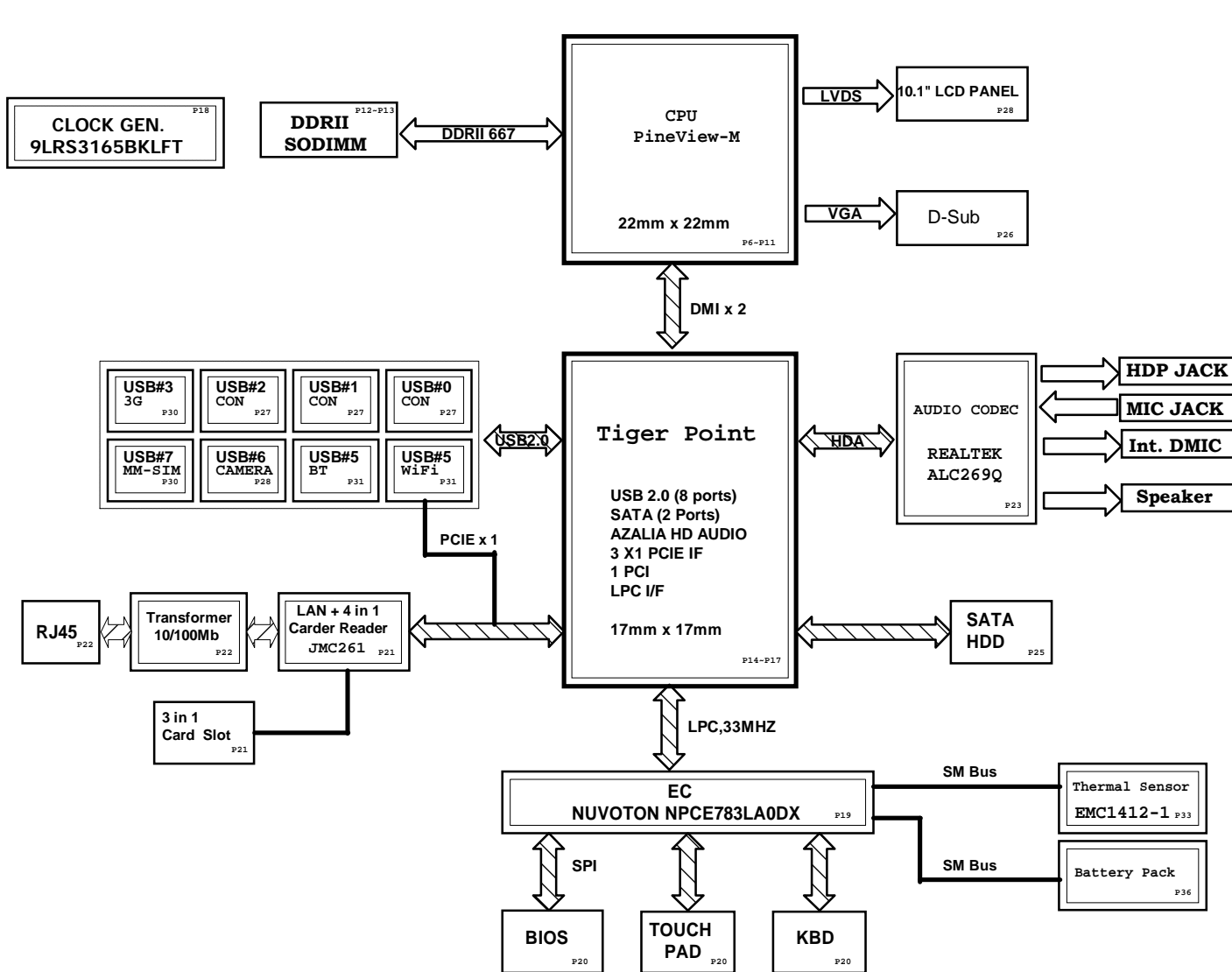


M9F1 Block Diagram R1.0



TI Charger BQ24753ARHBR P.36	
Inputs	Outputs
DC_IN	DCBATOUT
	BT+

System DC/DC TPS51125RGER P.37	
Inputs	Outputs
DCBATOUT	+3VALW
	+5VALW
	+5VALW_LDO
	+5CVCC

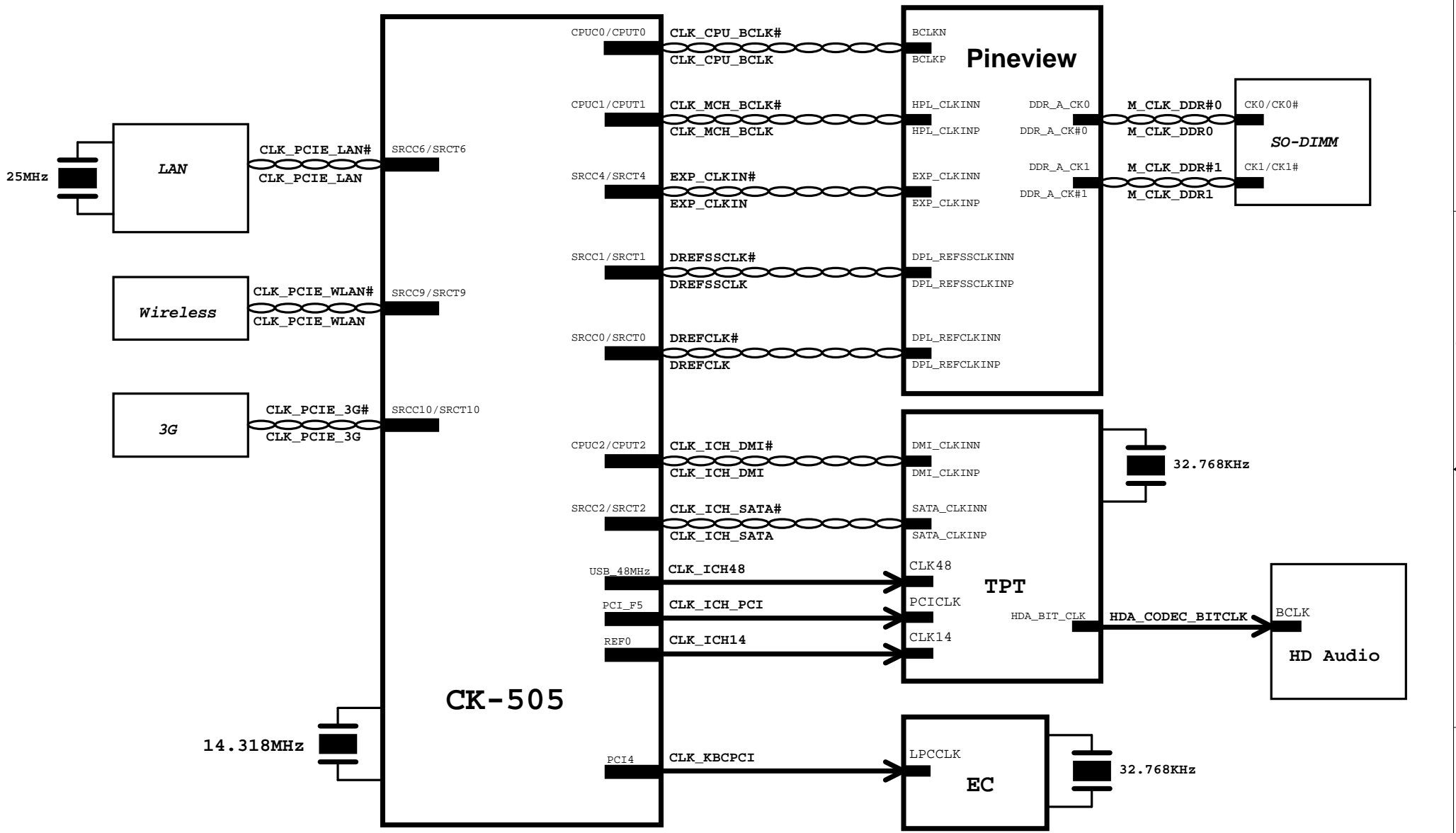
System DC/DC TPS51124RGER P.38	
Inputs	Outputs
DCBATOUT	+1_8VSUS
	VCCGFX

CPU DC/DC MAX8796GTJ+ P.39	
INPUTS	OUTPUT
DCBATOUT	VHCORE

System DC/DC G2998BP11U P.40	
Inputs	Outputs
+1_8VSUS	+0_9VRUN

System DC/DC G9731P11U P.40	
Inputs	Outputs
+1_8VSUS	+1_5VRUN

System DC/DC G9731P11U P.40	
Inputs	Outputs
+1_8VSUS	+1_05VRUN



CCPBG		
Clock distribution		
Size A3	Document Number M9F1	Rev 0.1
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Pine Trail Power Flowchart for M9F1

Voltage Rails

O MEANS ON X MEANS OFF


power plane / State	+5VALW_LDO +ECVCC	+5VALW +3VALW	+3VSUS +1_8VSUS	+5VRUN +3VRUN +1_8VRUN +1_5VRUN +1_05VRUN +0_9VRUN VCCGFX VHCORE
S0	O	O	O	O
S3	O	O	O	X
S5/AC, S4	O	O	X	X
S5 Battery only	O	X	X	X
S5 S4/AC & Battery don't exist (G3)	X	X	X	X

S3 : STR

S4 : STD

S5 : SOFT OFF

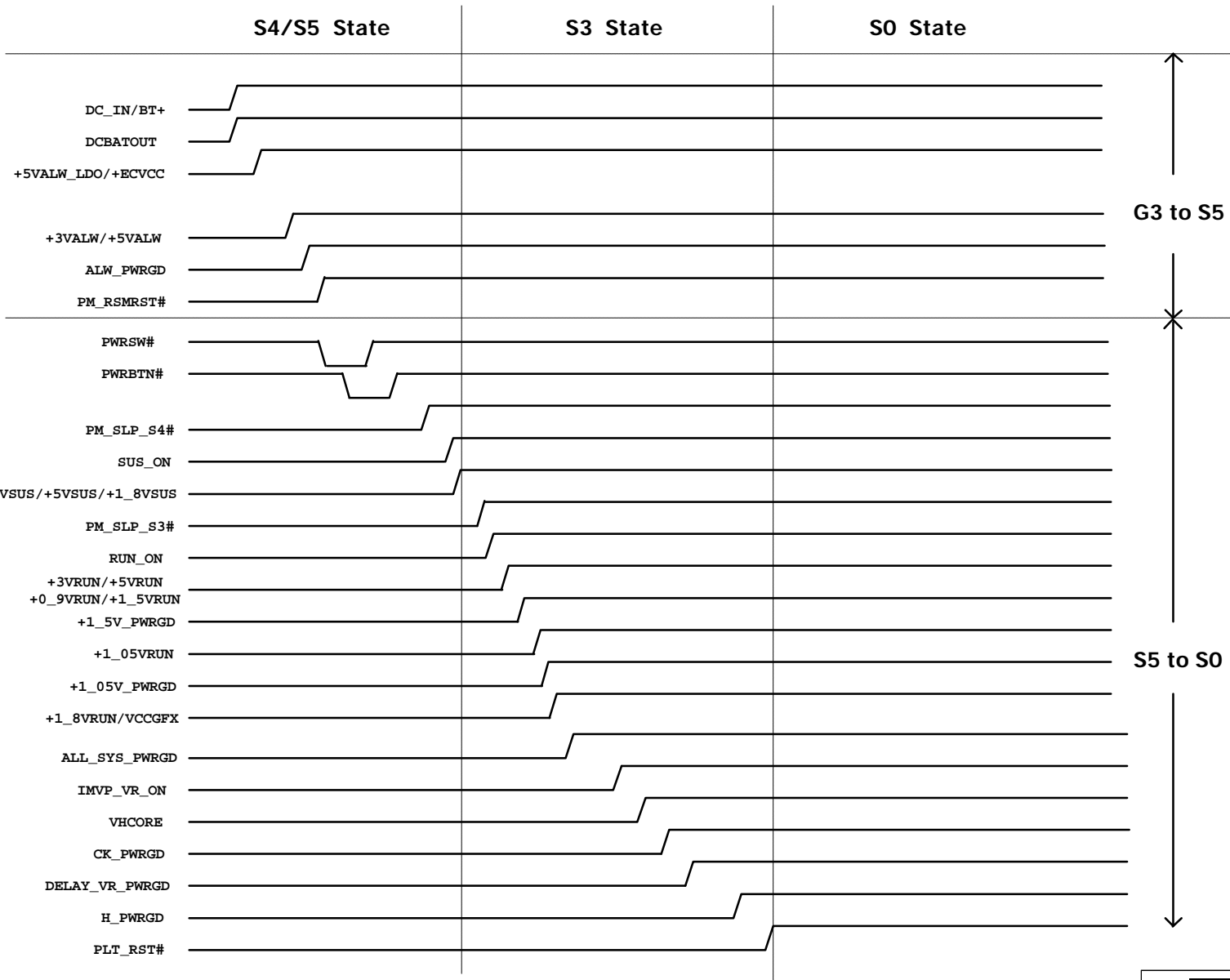
G3 : ME OFF

			
CCPBG			
Title			
Power Flowchart			
Size	Document Number	Rev	
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Date:	Wednesday, March 17, 2010	Sheet	3 of 44

Pine Trail Power On Sequence

<http://hobi-elektronika.net>

REV : 2009/08/17

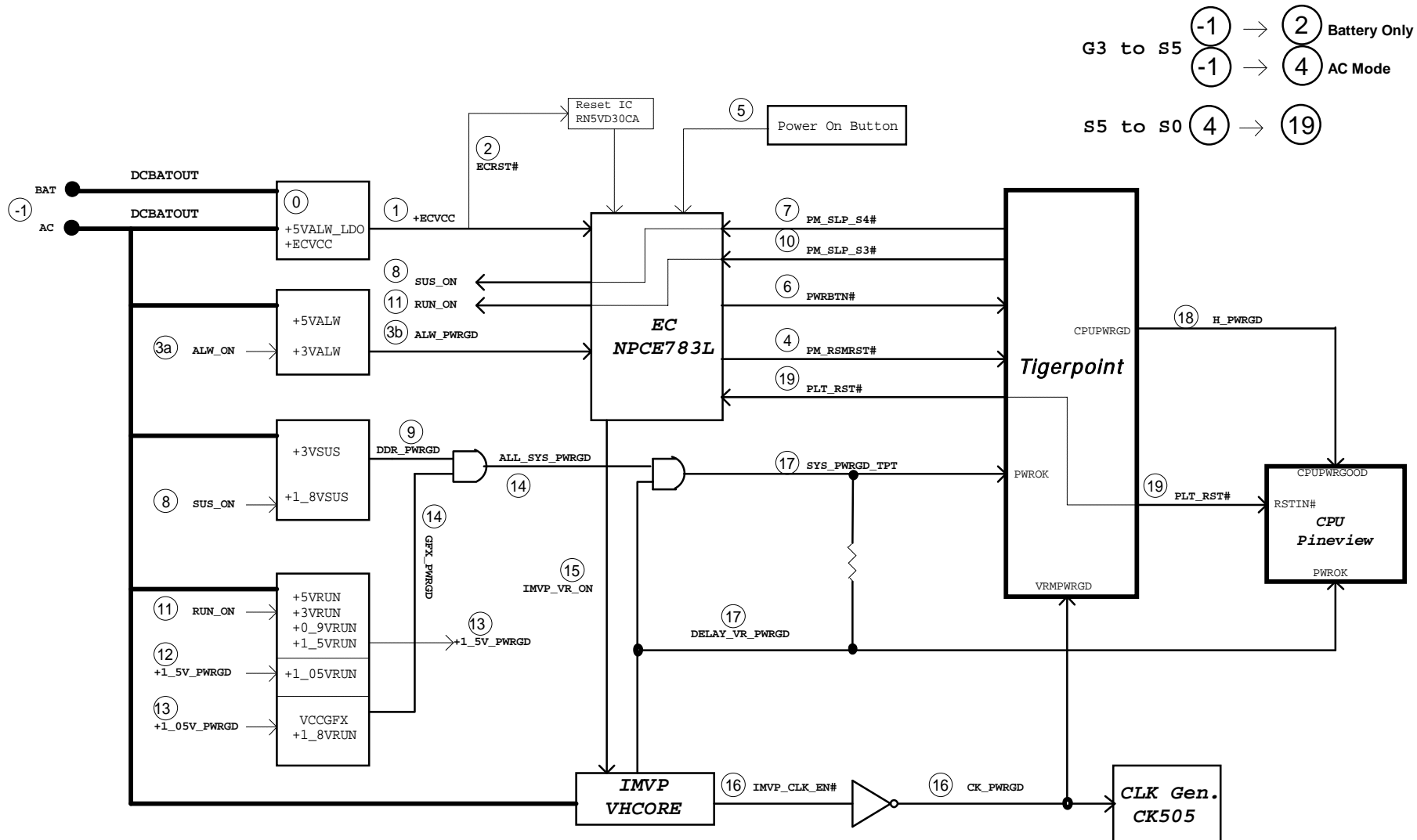


G3 to S5

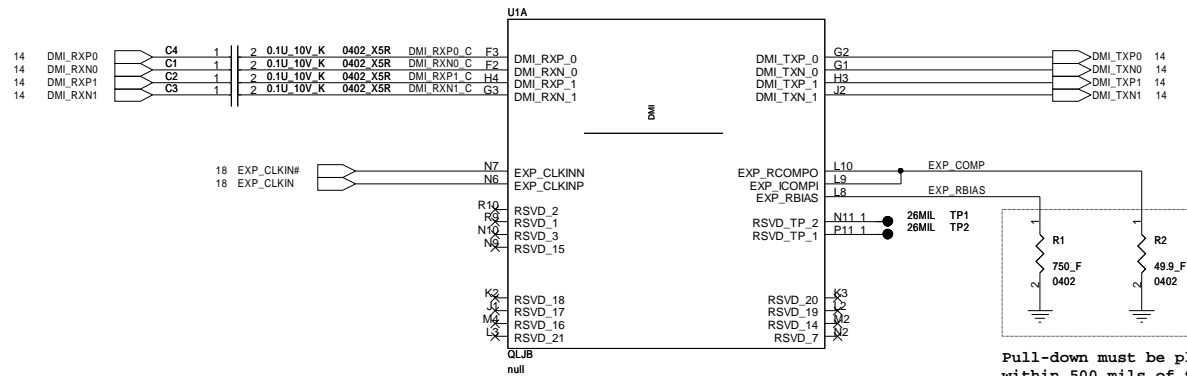
S5 to S0

CCPBG		
Power On Sequence(1)		
Size	Document Number	Rev
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Pine Trail Power On Sequence

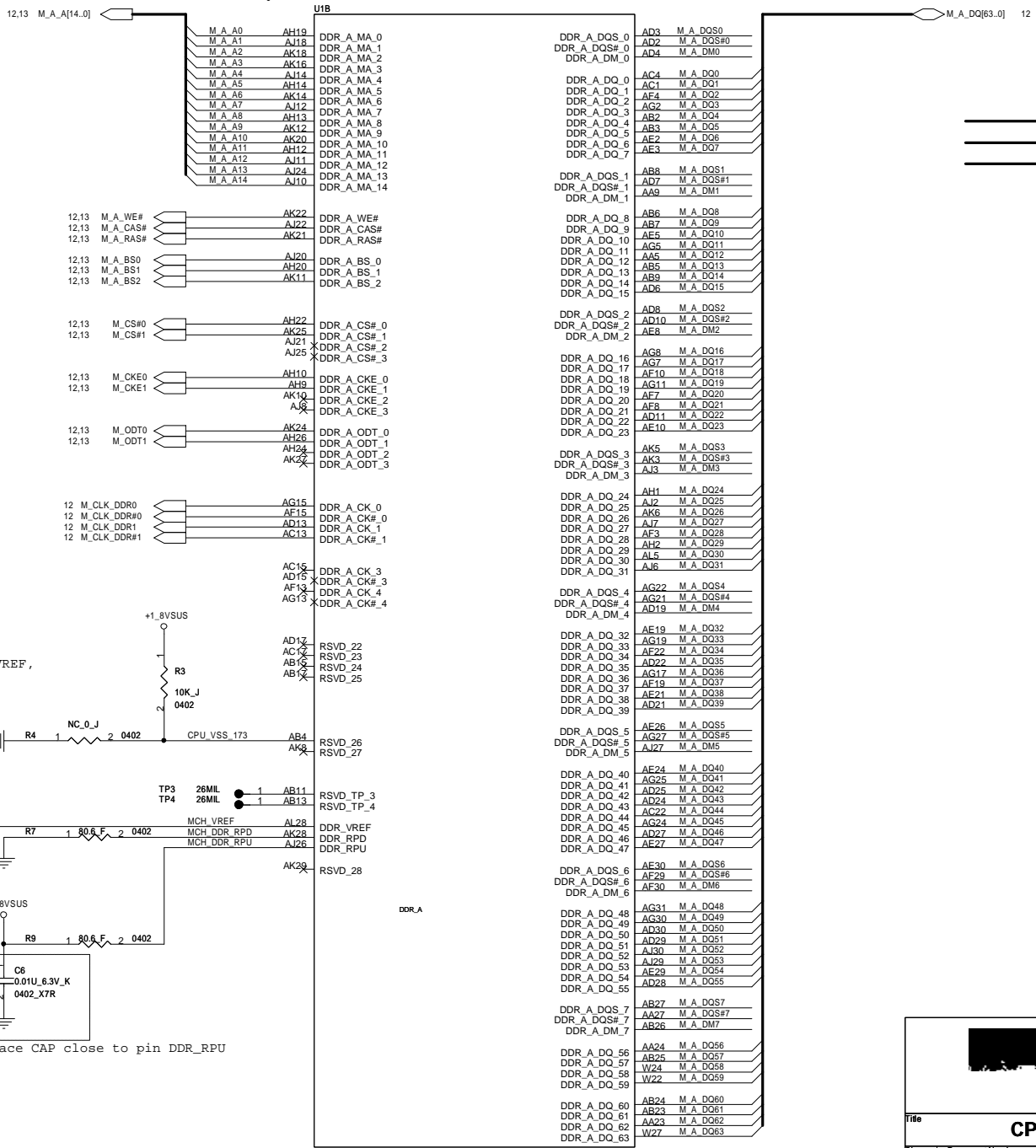


CCPBG			
Power On Sequence(2)			
<small>Title</small>			
<small>Size</small>	<small>Document Number</small>	M9F1	<small>Rev</small>
<small>Custom</small>			0.1
<small>Date</small>	<small>Wednesday, March 17, 2010</small>	<small>Sheet</small>	<small>5 of 44</small>

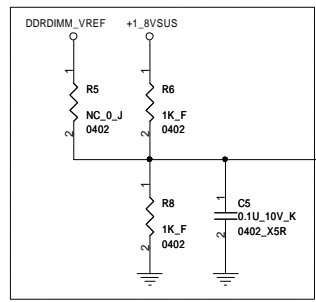


Pull-down must be placed within 500 mils of the processor.

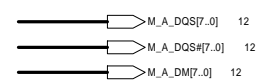
CCPBG		
CPU- Pineview (1)		
Size A3	Document Number M9F1	Rev 0.1
Date: Wednesday, March 17, 2010 Sheet 6 of 44		



Place resistors close to MCH PINS ON MCH_VREF,
Place 0.1uF CAP close to MCH.



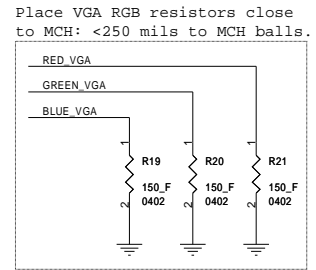
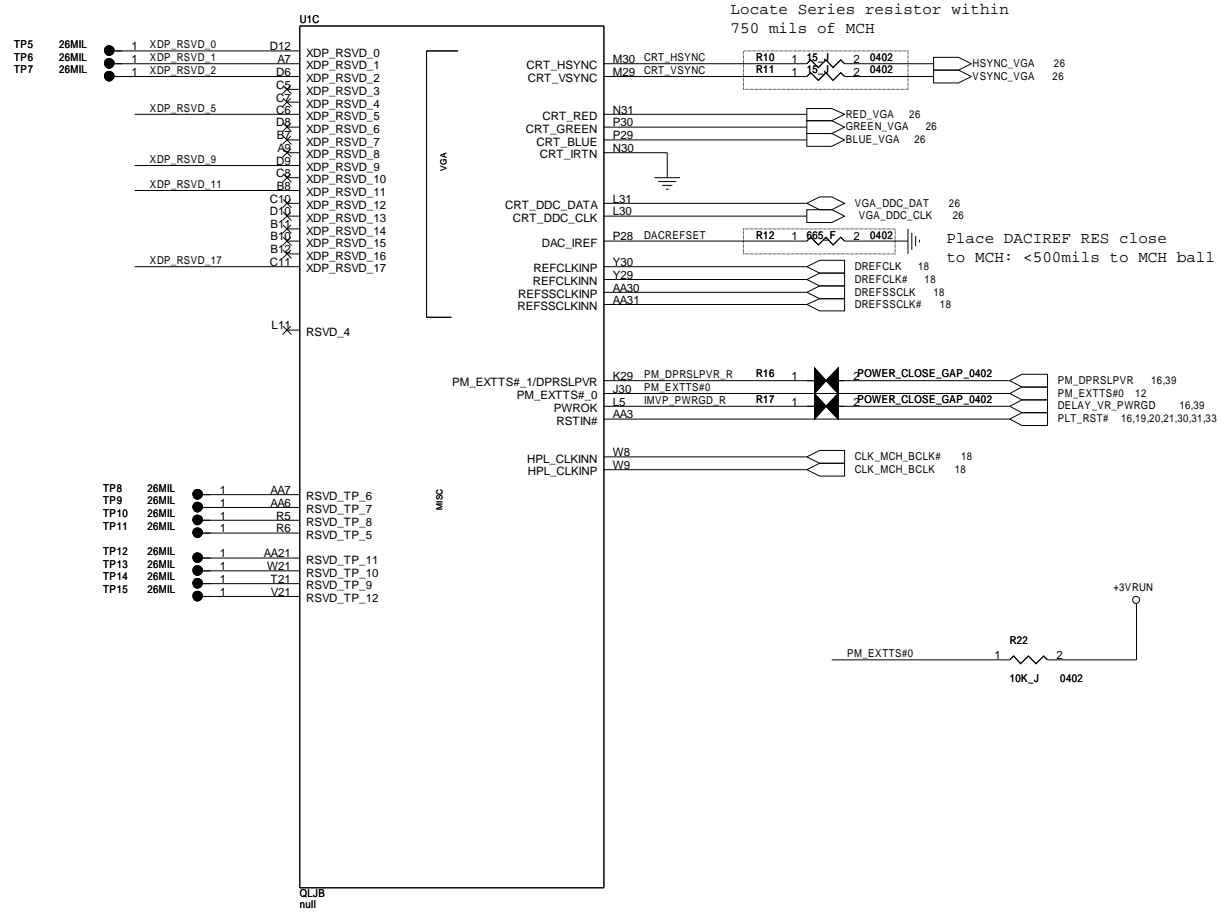
Place CAP close to pin DDR_RPU



CCPBG

Title CPU- Pineview (2)

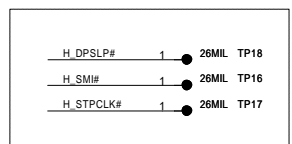
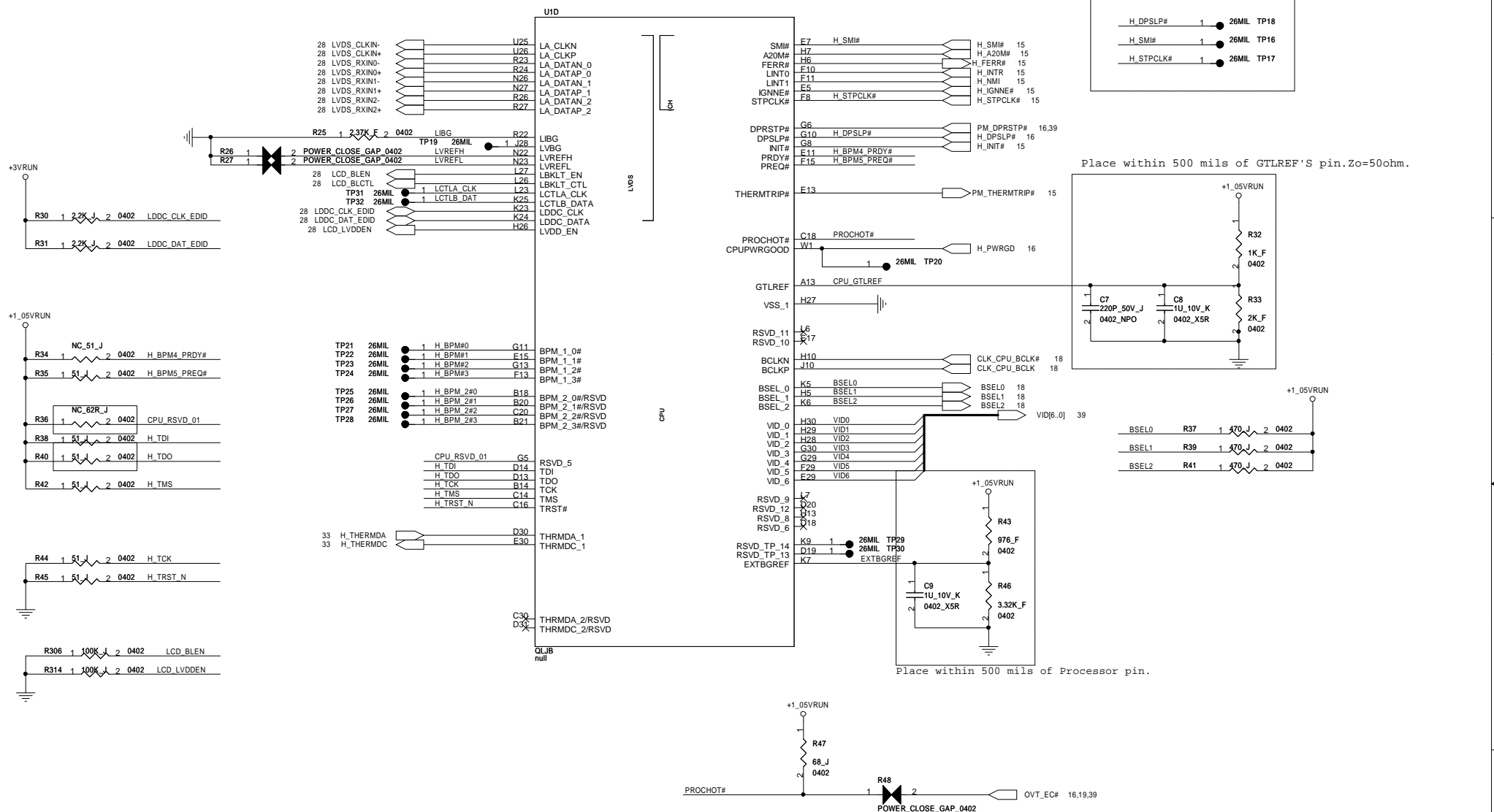
Size A3	Document Number M9F1	Rev 0.1
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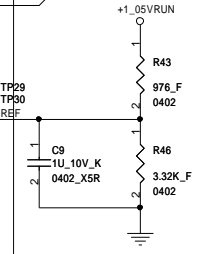
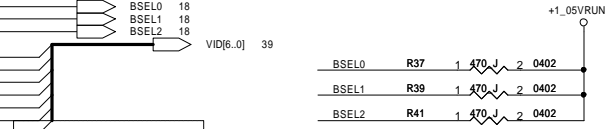
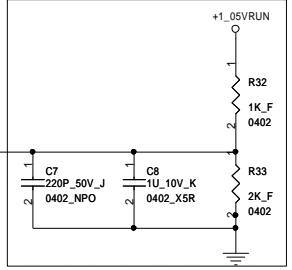
CCPBG

Title CPU- Pineview (3)

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Place within 500 mils of GTLREF'S pin. Zo=50ohm.

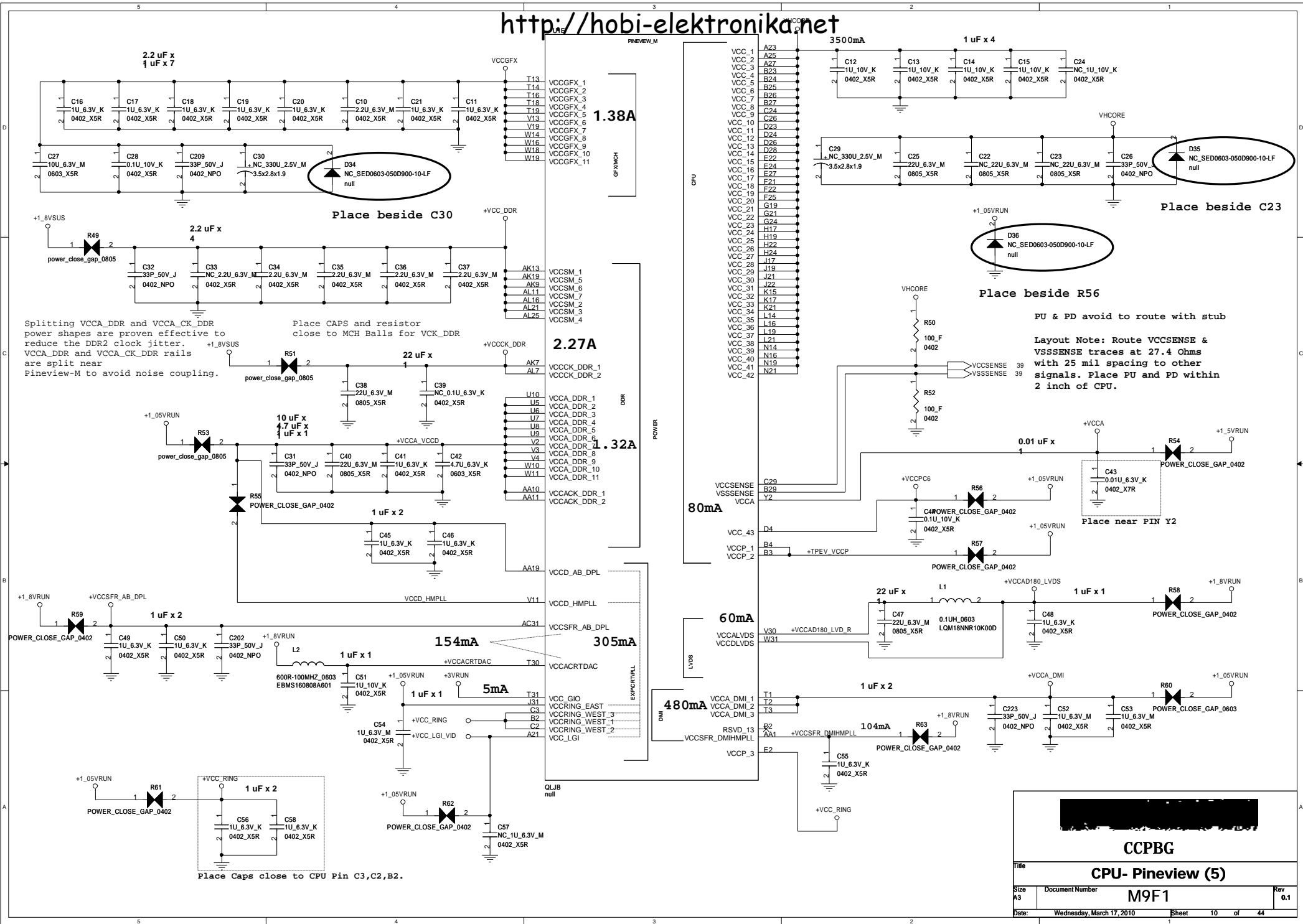


Place within 500 mils of Processor pin.

CCPBG

Title CPU- Pineview (4)

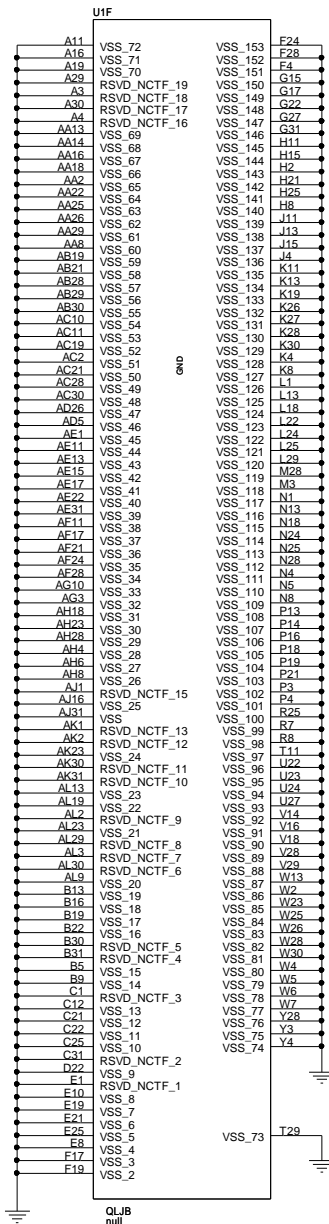
Size A3	Document Number M9F1	Rev 0.1
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CCPBG

Title
CPU- Pineview (5)

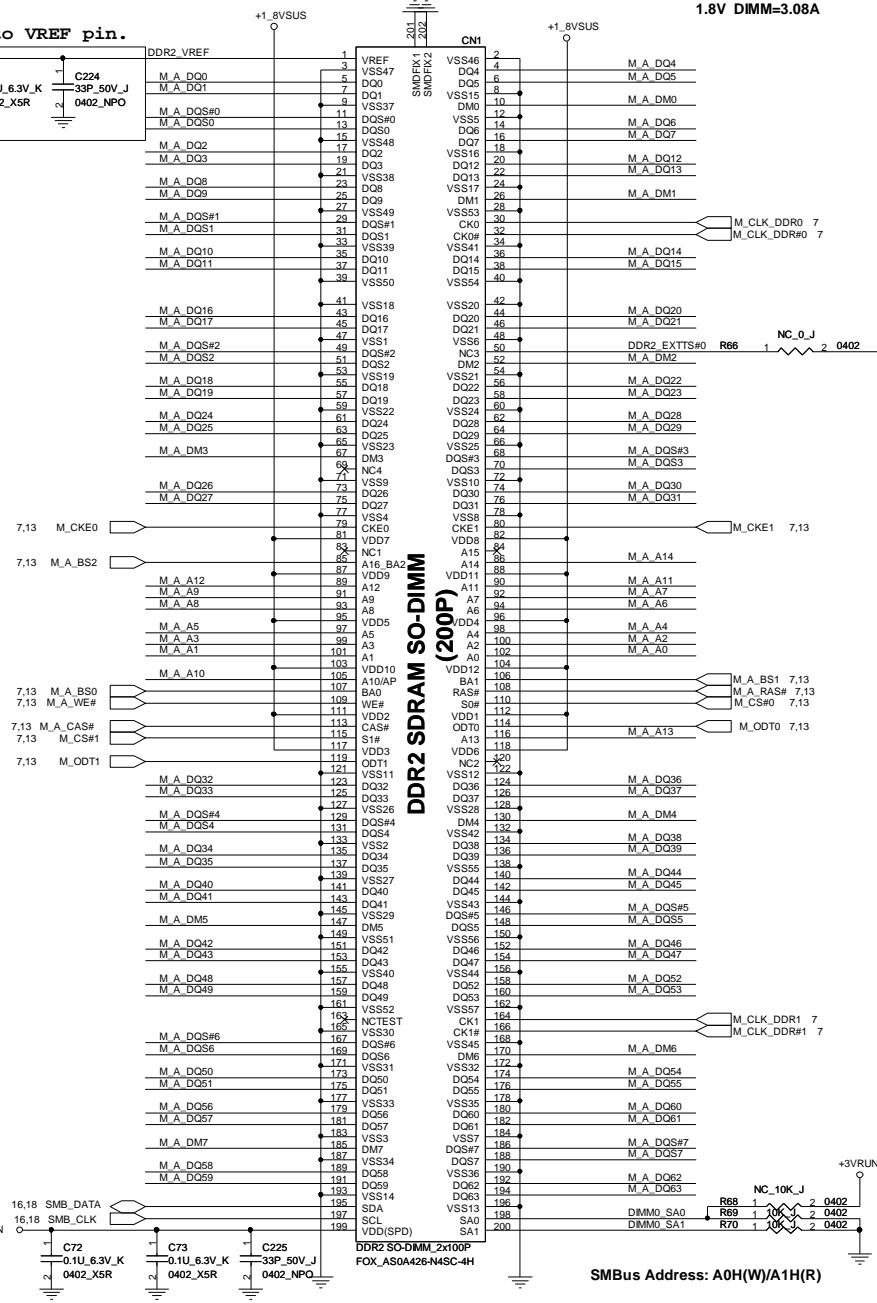
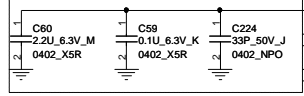
Size A3	Document Number M9F1	Rev 0.1
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CCPBG		
CPU- Pineview (6)		
Size A3	Document Number M9F1	Rev 0.1
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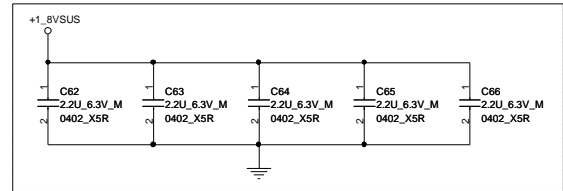
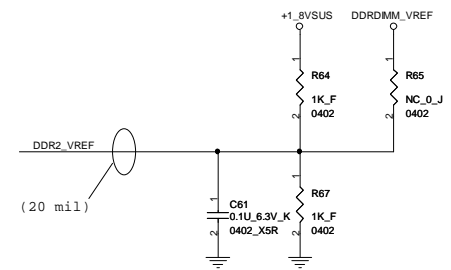
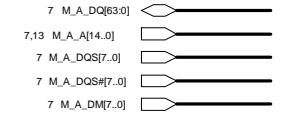
1.8V DIMM=3.08A

Place close to VREF pin.

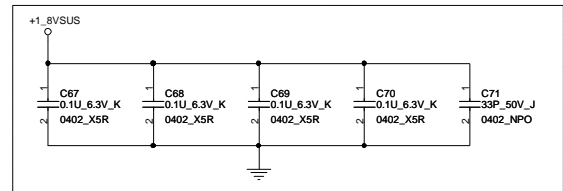


DDR2 SDRAM (200P)

SMBus Address: A0H(W)/A1H(R)



Place these Caps near So-DIMM0

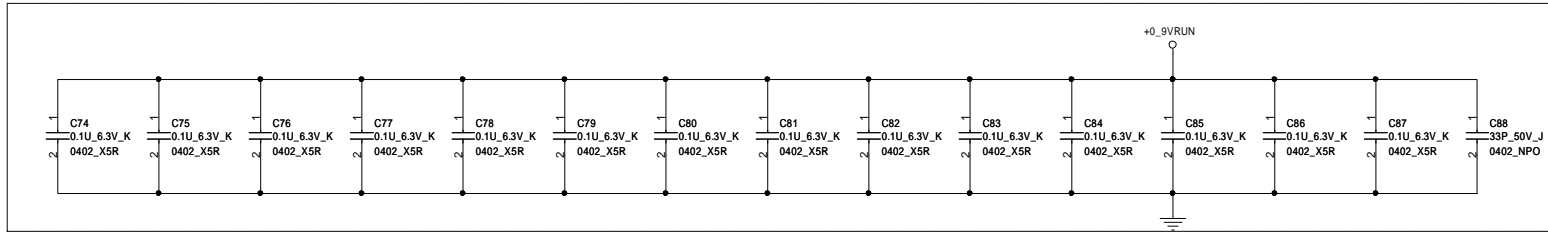


Place these Caps near So-DIMM0

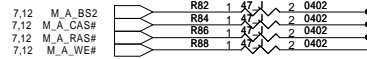
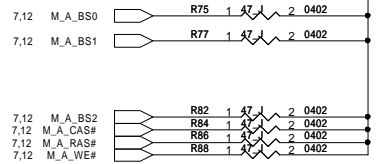
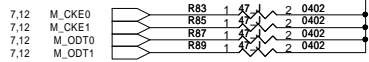
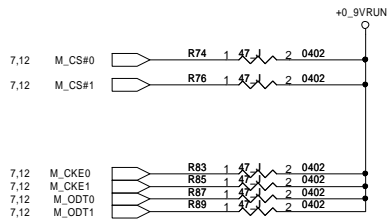
CCPBG

DDRII(SO-DIMM0)

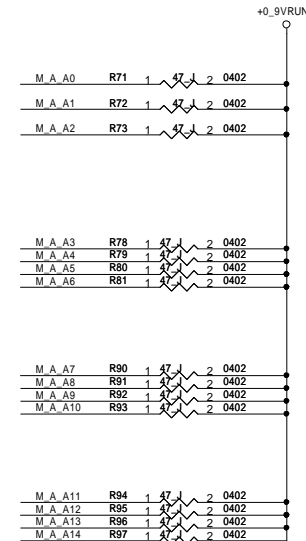
Title	DDRII(SO-DIMM0)	
Size	Document Number	Rev
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Place one cap close to every two pull-up resistors terminated to +0_9VRUN.



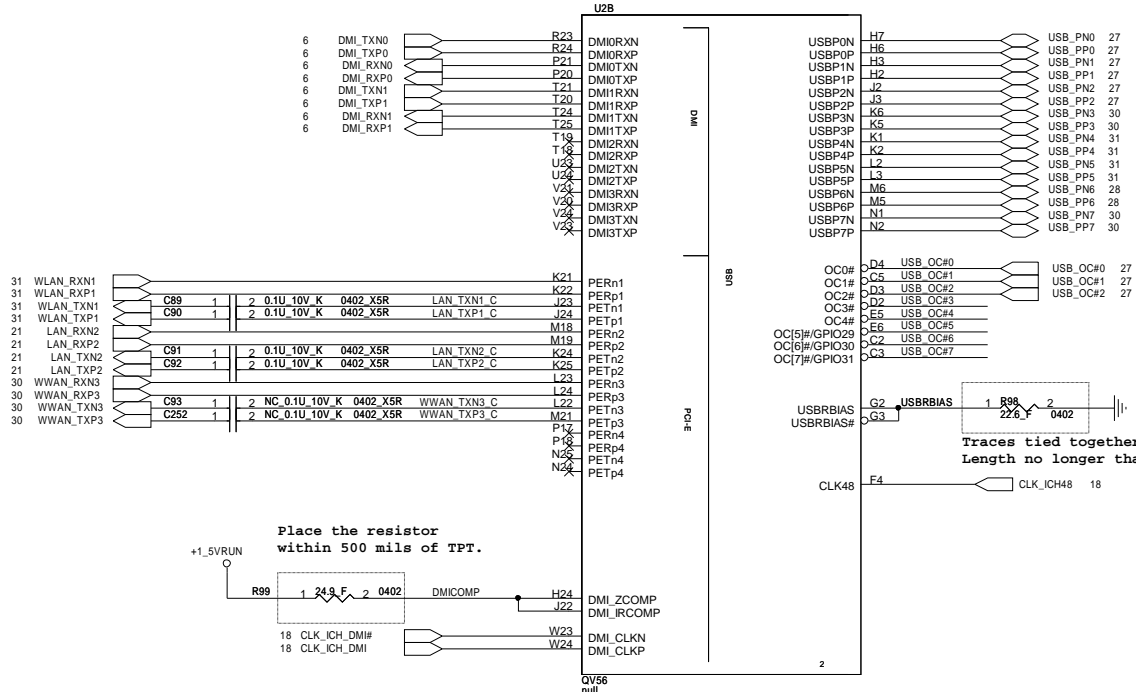
7.12 M_A_A[14.0]



CCPBG

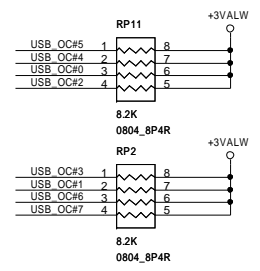
DDRII (Termination)

Size	Document Number	Rev
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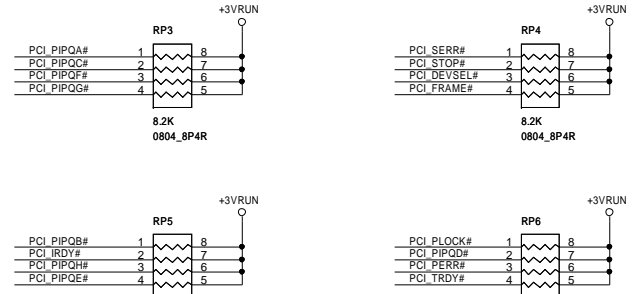


USB port table

Port0	External USB1
Port1	External USB2
Port2	External USB3
Port3	WWAN (3G/GPS)
Port4	WLAN(WIFI)
Port5	Bluetooth
Port6	Camera module
Port7	MM-SIM



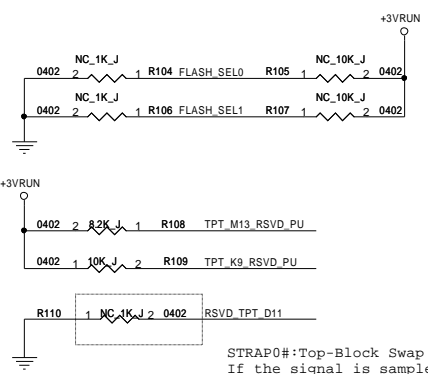
Traces tied together close to Pin
Length no longer than 200 mils to Resistor.



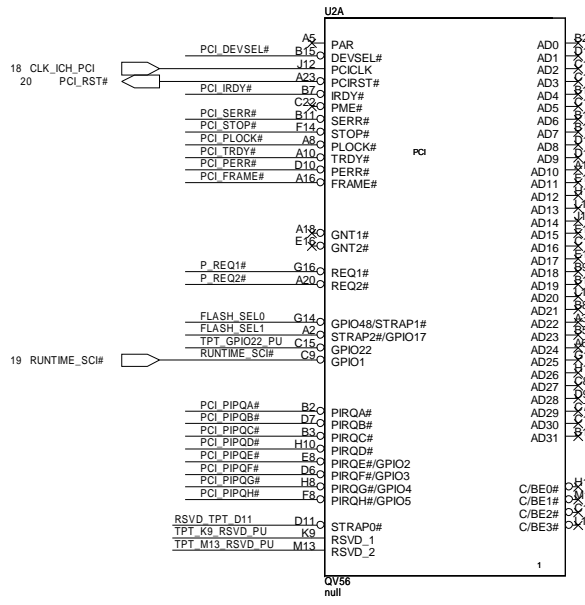
Strapping Options Flash

STRAP2#/ GPIO17	STRAP1#/ GPIO48	Routing
0	1	SPI
1	0	PCI
1	1	LPC

STRAP2#/GPIO17 and STRAP1#/GPIO48
have weak internal pull-ups



STRAP0# : Top-Block Swap Override.
If the signal is sampled low,
this indicates that the system is
strapped to the "top-block swap" mode
(Tiger Point inverts A16 for all cycles targeting FWH BIOS space)



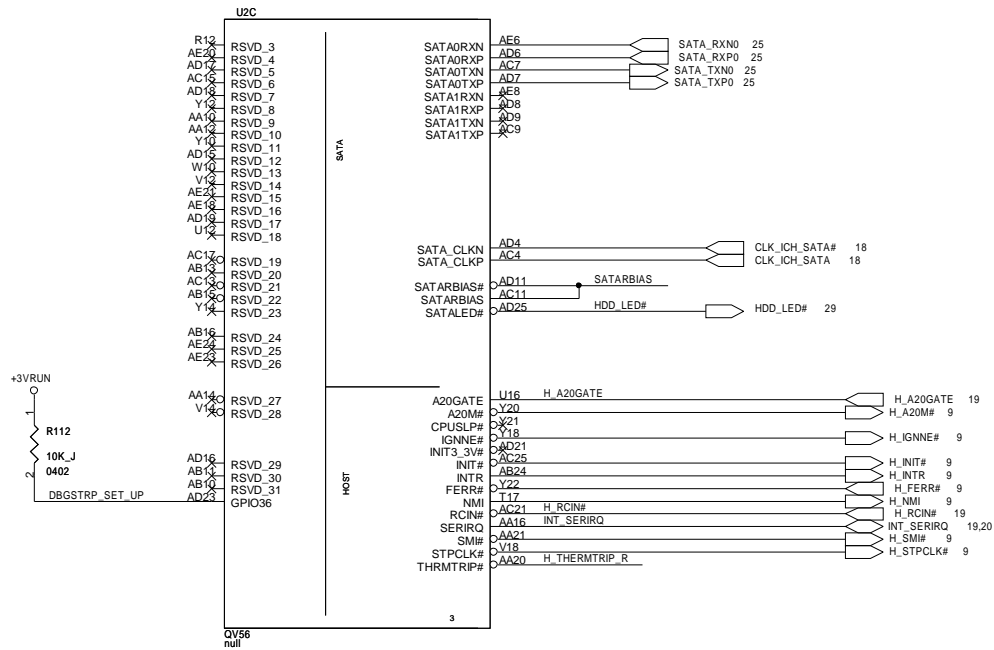
TPT Strap Pin

Strap Pin	Internal PU/PD	External PU/PD
STRAP0#	PU 20K	PU 10K(NC) to +3VRUN/PD 1K(NC)
STRAP1#	PU 20K	PU 10K(NC) to +3VRUN/PD 1K(NC)
STRAP2#	PU 20K	PU 10K(NC) to +3VRUN/PD 1K(NC)

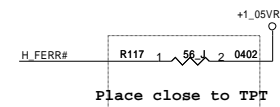
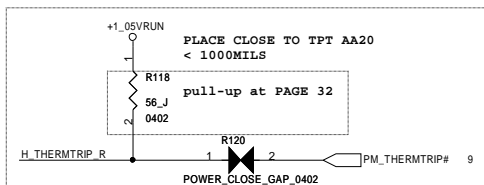
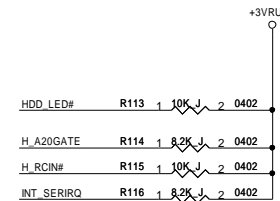
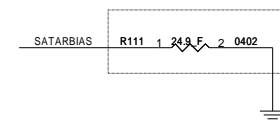
CCPBG

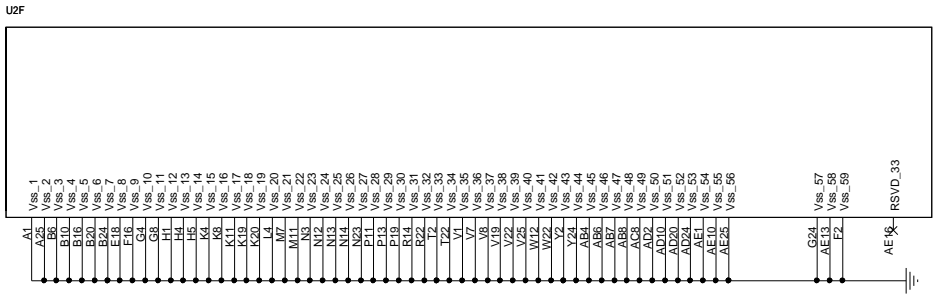
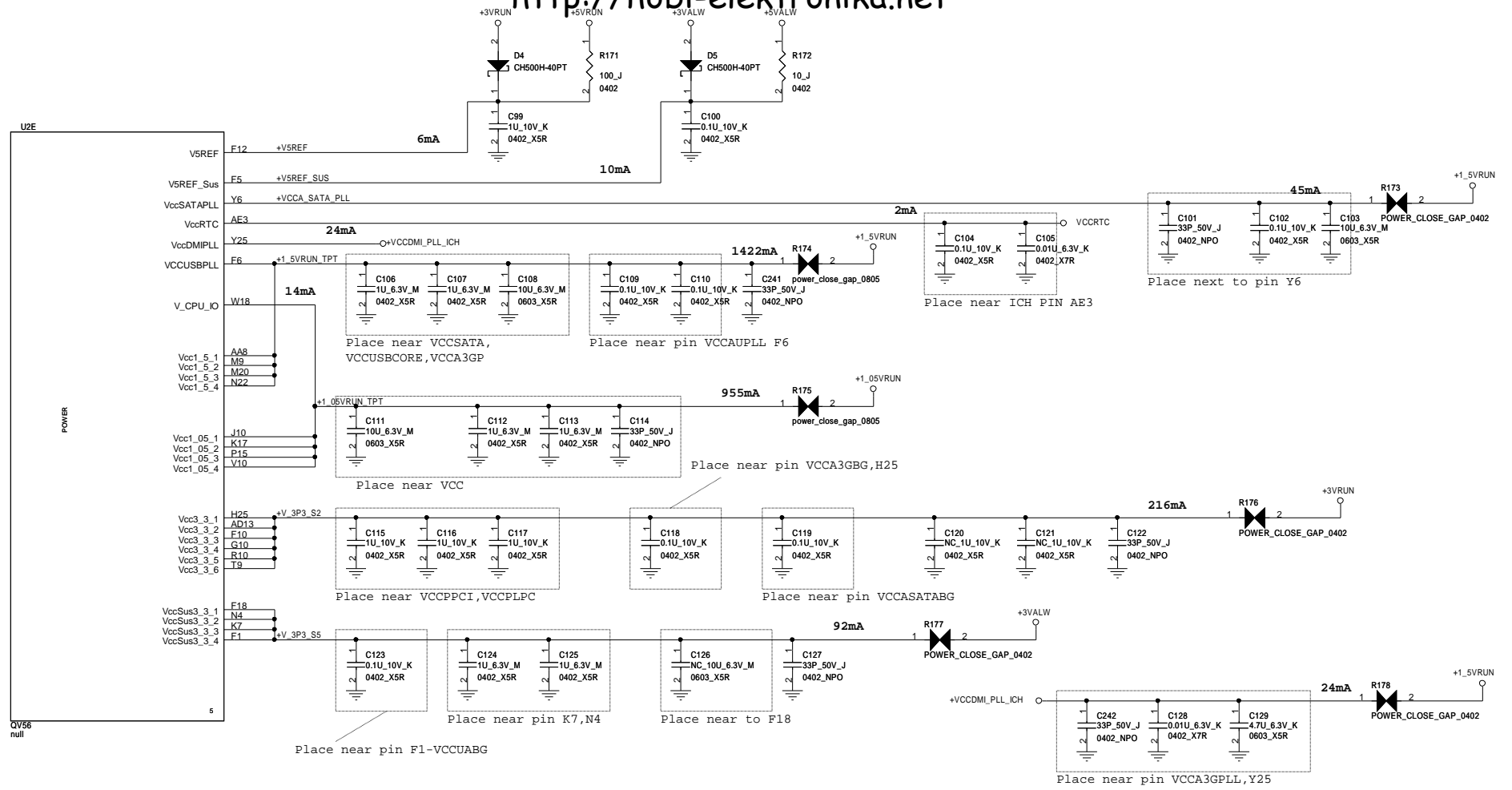
Tiger Point (1)

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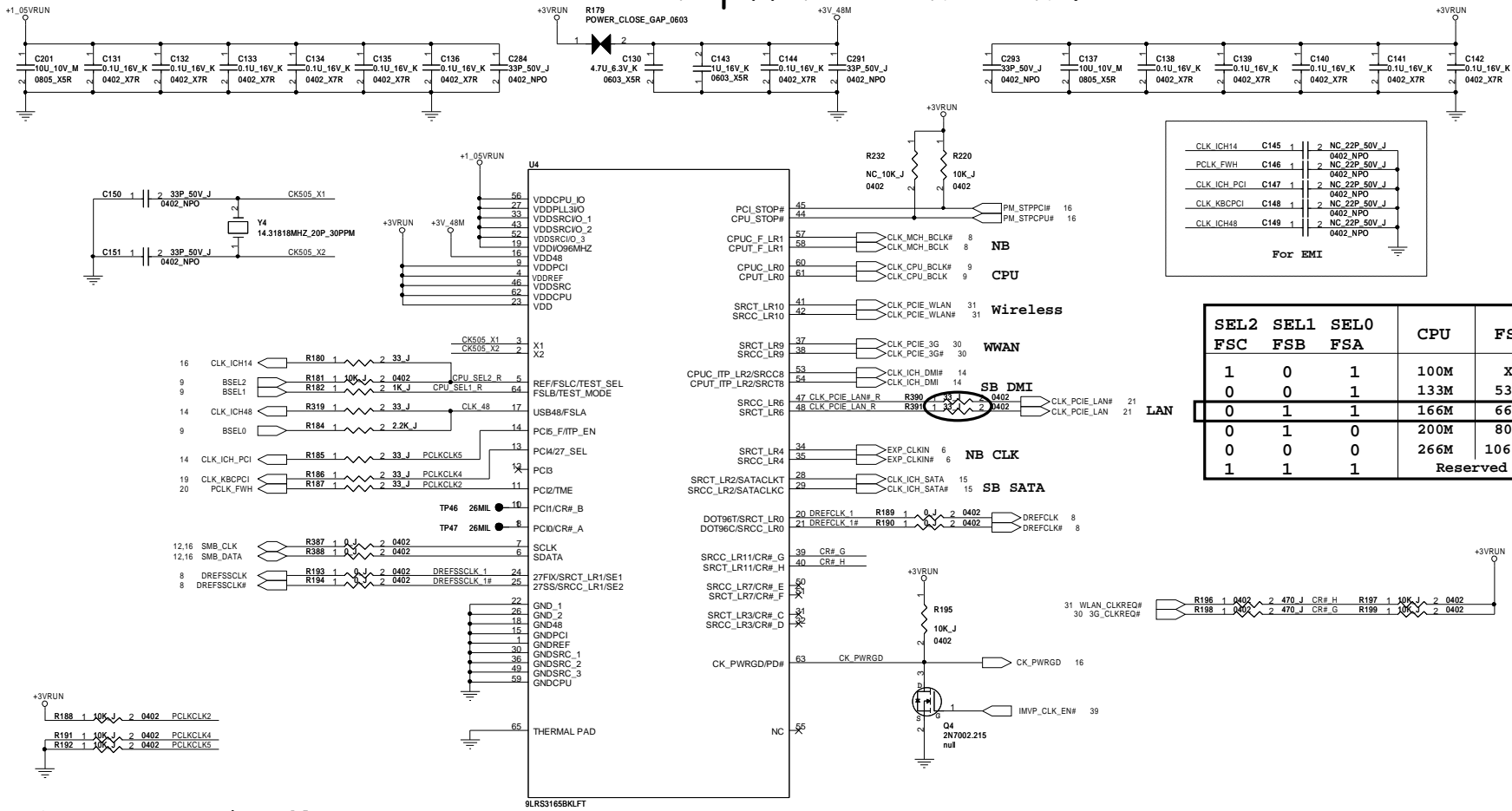


PLACE SATARBIAS RESISTORS CLOSE TO ICH: <500 MILS TO ICH BALLS





CCPBG			
Title			
Tiger Point (4)			
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CLK_ICH14	C145	1	2	NC	22P	50V	J
PCLK_FWH	C146	1	2	NC	22P	50V	J
CLK_ICH_PCI	C147	1	2	NC	22P	50V	J
CLK_KBCPCI	C148	1	2	NC	22P	50V	J
CLK_ICH48	C149	1	2	NC	22P	50V	J

For EMI

SEL2	SEL1	SEL0	CPU	FSB
FSC	FSB	FSA		
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M
1	1	1	Reserved	

ICS9LPRS365YGLFT setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overlocking of CPU and SRC Allowed 1= overlocking of cpu and src not allowed
PCI3	
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-18, Pin13 as D0996, Pin14 as D0994 1 = Pin17 as 27MHz, Pin 18 as 27MHz SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 = SRC8/SRC6# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1= CR#_C controls SRC2 pair

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1= CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7# enabled (default) 1= CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1= CR#_F controls SRC6
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1= CR#_G controls SRC6
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1= CR#_H controls SRC6

CCPBG

CLOCK GEN

File _____

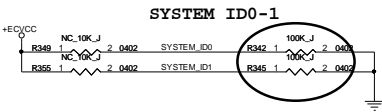
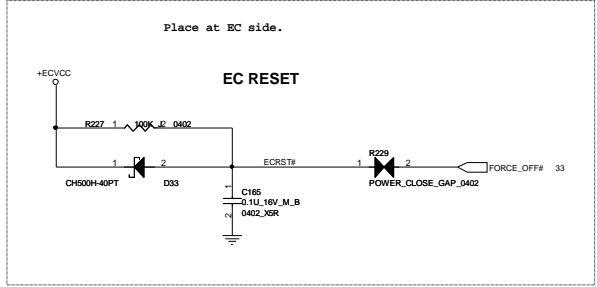
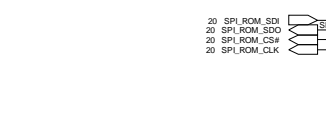
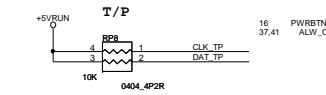
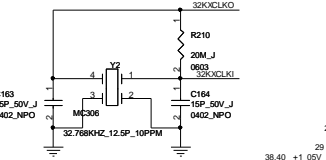
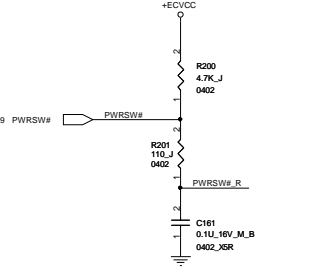
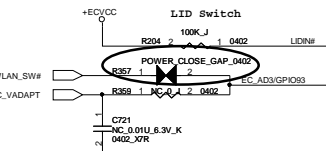
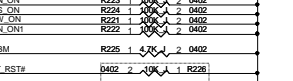
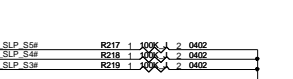
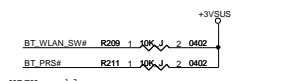
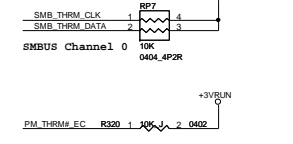
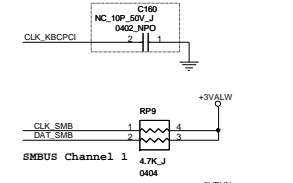
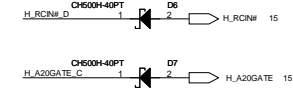
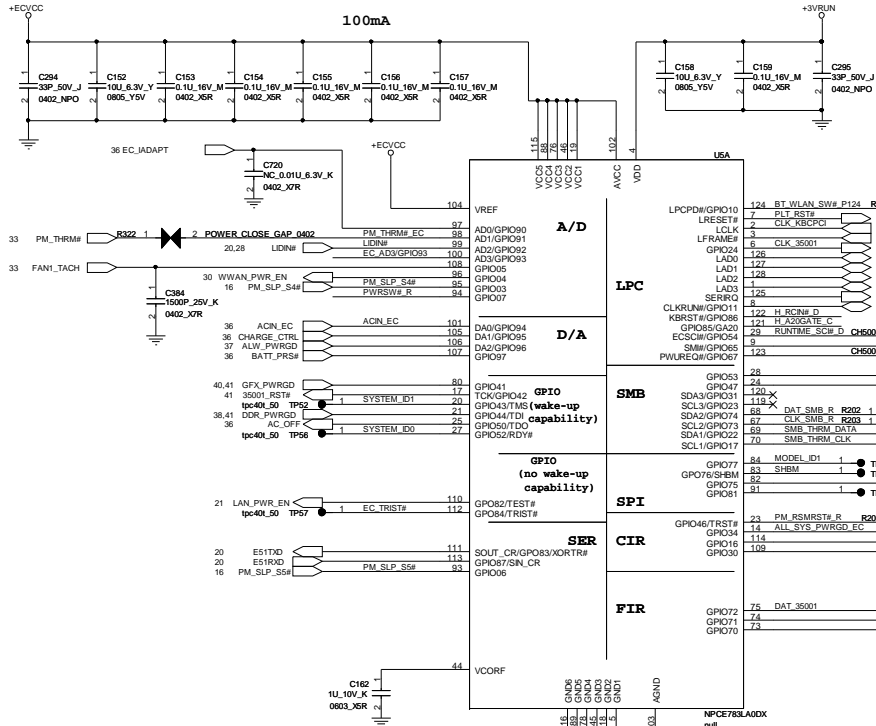
Size Custom Document Number **M9F1** Rev **0.1**

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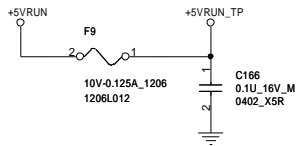
Use EC to implement power limit
Wireless switch should use U5.124, reserve U5.100 A/D for detecting voltage level
(Default setting -- Hardware Power Limit)
If use EC to implement, it should do setting as below.

Stff
C720, C721, R233, R359, PR144, PR145, PR146

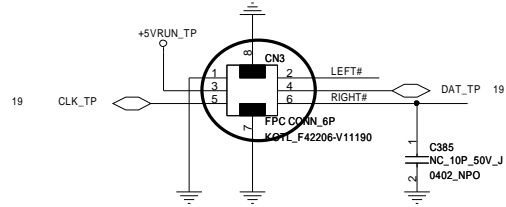
NC
R357, PR139, PU9, PC115, PC116, PR118, PR123, PR124



CCPBG
EC (NPCE783L)
Title
Size Custom Document Number M9F1 Rev 0.1
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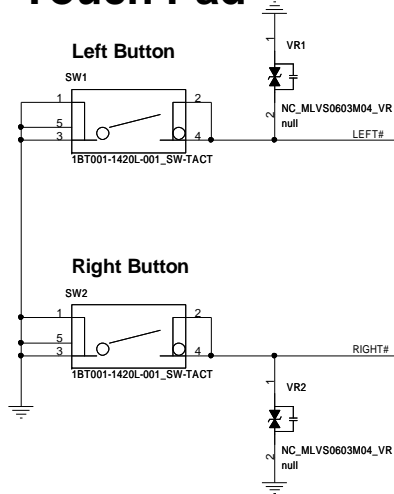
Touch Pad CONN.



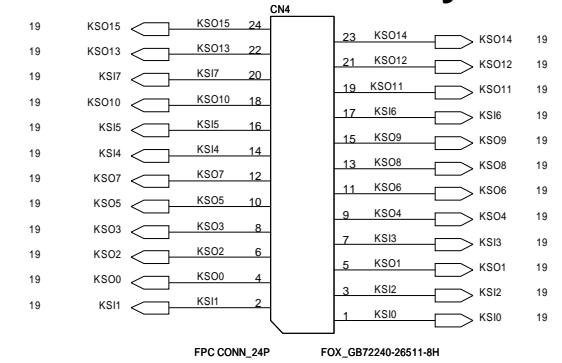
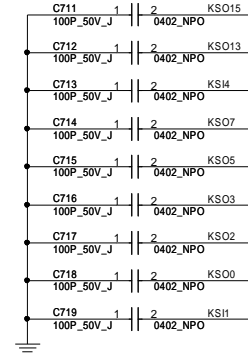
BFT Test Point for Touch Pad (BOTTOM side)

tpc60b_100	TP100	1	GND
tpc60b_100	TP109	1	LEFT#
tpc60b_100	TP110	1	RIGHT#
tpc60b_100	TP111	1	DAT_TP
tpc60b_100	TP112	1	CLK_TP
tpc60b_100	TP113	1	+5VVRUN_TP

Touch Pad



Keyboard

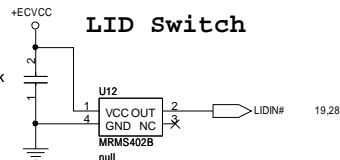


Place these caps close to CN4.

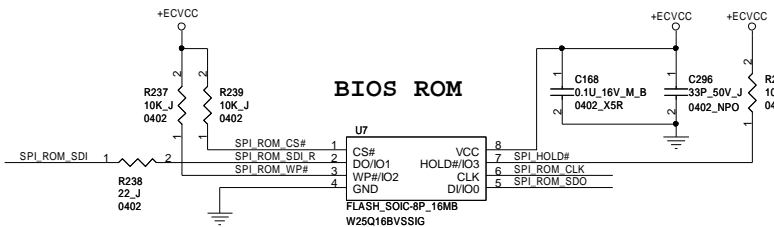
BFT Test Point for Keyboard (BOTTOM side)

tpc60b_100	TP96	1	KSI4
tpc60b_100	TP97	1	KSO7
tpc60b_100	TP98	1	KSO5
tpc60b_100	TP99	1	KSI2

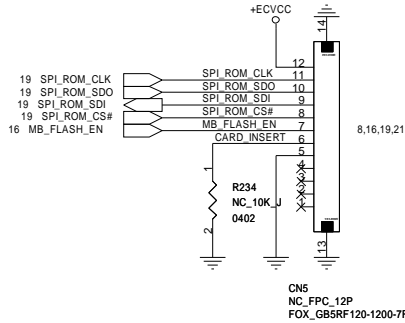
tpc40L_75	TP101	1	SPI_ROM_CS#
tpc40L_75	TP102	1	SPI_ROM_SDI_R
tpc40L_75	TP103	1	SPI_ROM_WP#
tpc40L_75	TP104	1	GND
tpc40L_75	TP105	1	+ECVCC
tpc40L_75	TP106	1	SPI_HOLD#
tpc40L_75	TP107	1	SPI_ROM_CLK
tpc40L_75	TP108	1	SPI_ROM_SDO



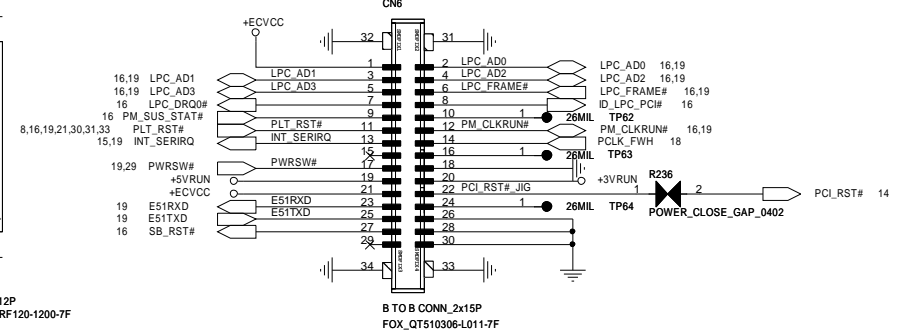
BIOS ROM



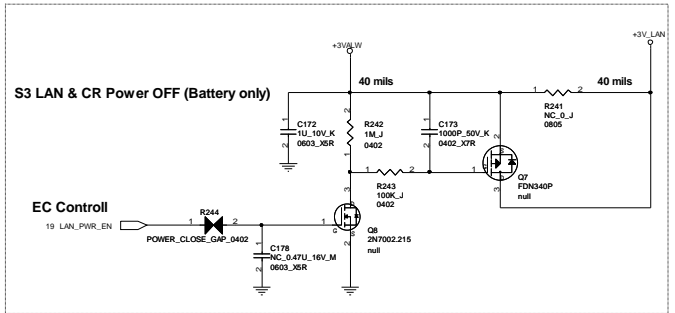
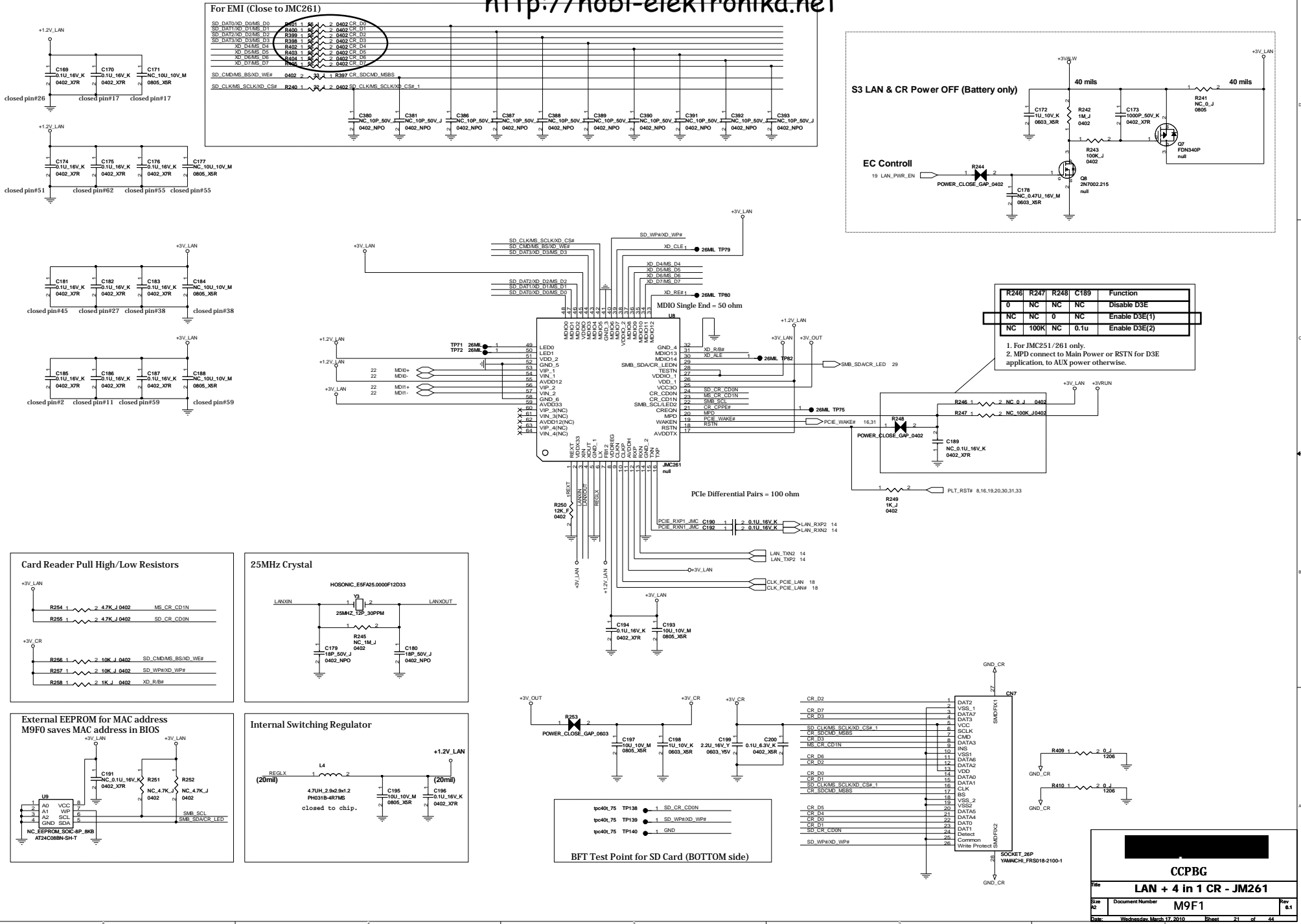
EXTERNAL SPI ROM INTERFACE



Debug Port

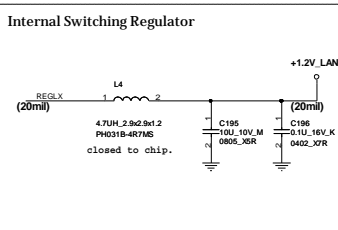
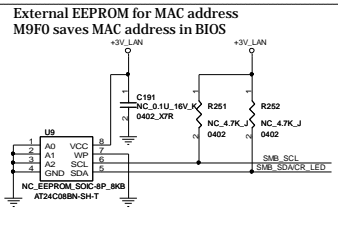
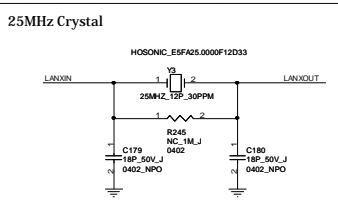
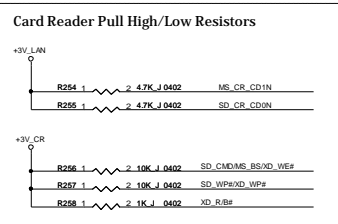


CCPBG		
Title		
KB/TP/Debug Port		
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R246	R247	R248	C189	Function
0	NC	NC	NC	Disable D3E
NC	NC	0	NC	Enable D3E(1)
NC	100K	NC	0.1u	Enable D3E(2)

1. For JMC251/261 only.
 2. MPD connect to Main Power or RSTN for D3E application, to AUX power otherwise.



CCPBG

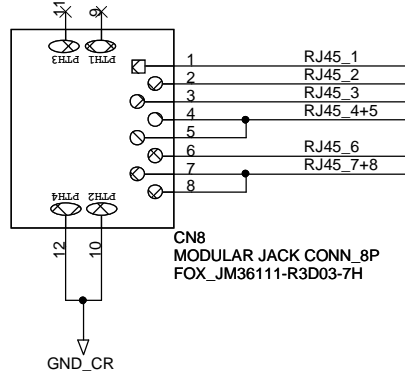
LAN + 4 in 1 CR - JM261

Rev: 0.1

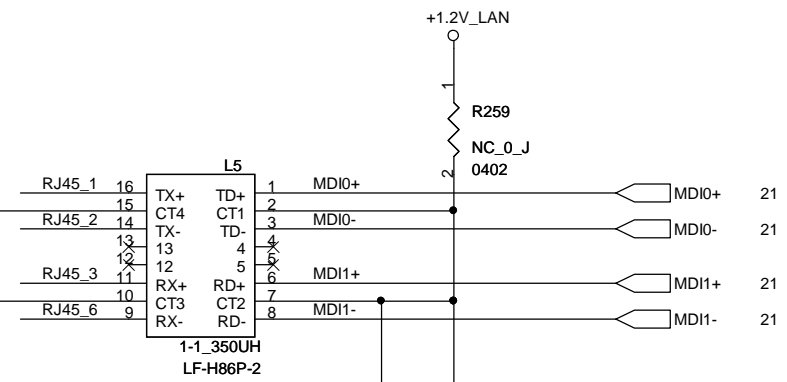
Document Number: M9F1

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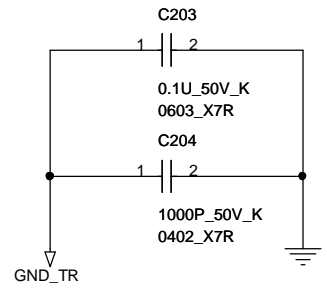
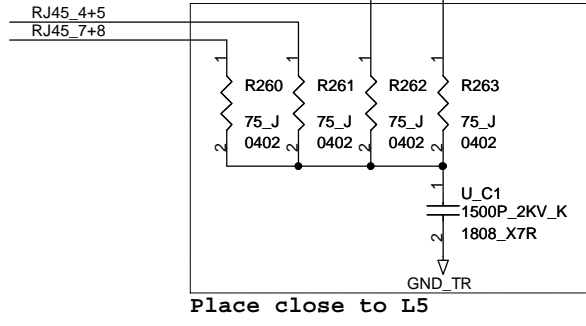
Zdiff = 100 Ohm



C205, C206 close to Pin2, Pin7 of L5 each

BFT Test Point for RJ45 (BOT side)

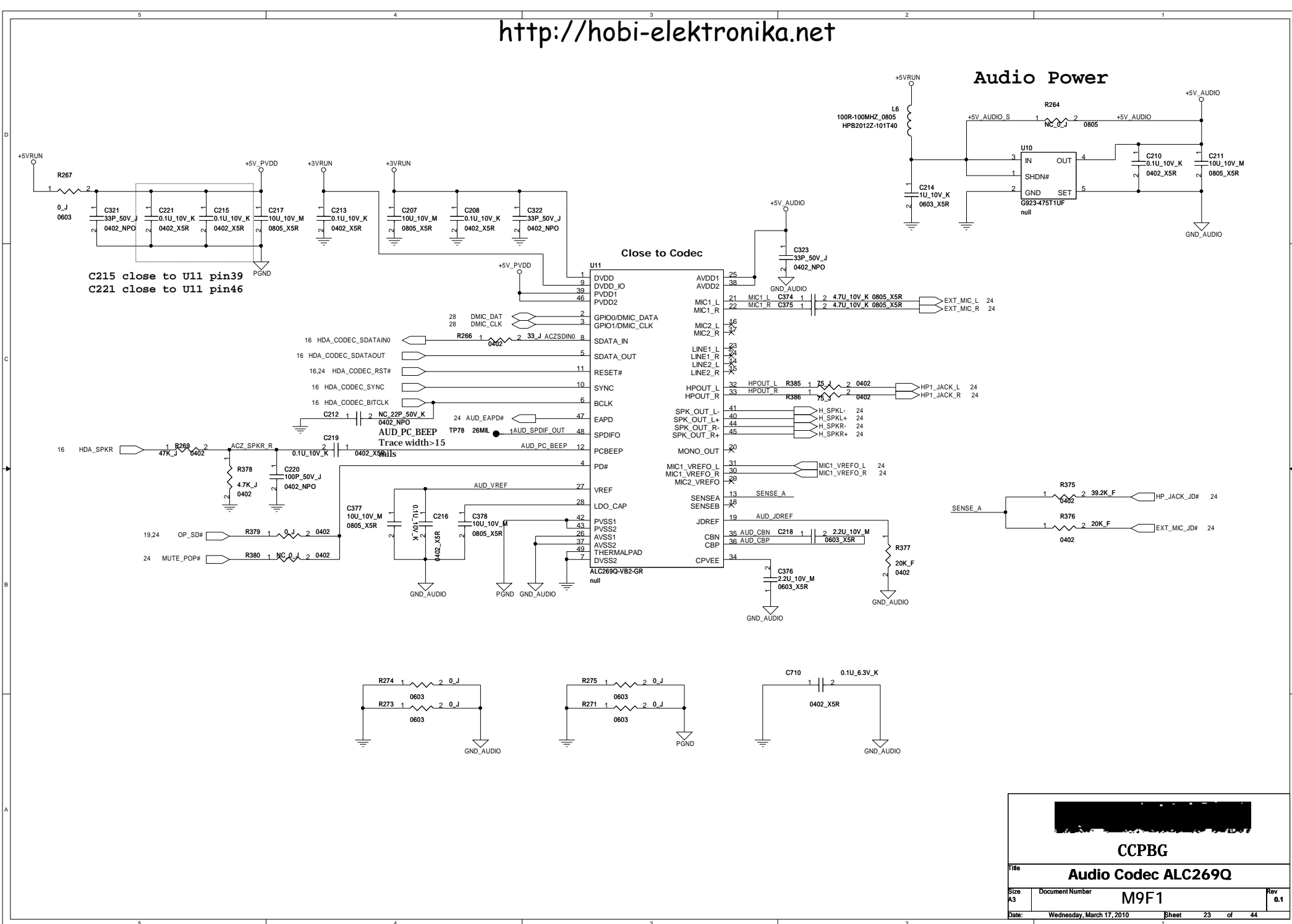
tpc40t_75	TP153	●	1	RJ45_1
tpc40t_75	TP154	●	1	RJ45_2
tpc40t_75	TP155	●	1	RJ45_3
tpc40t_75	TP156	●	1	RJ45_4+5
tpc40t_75	TP157	●	1	RJ45_6
tpc40t_75	TP158	●	1	RJ45_7+8



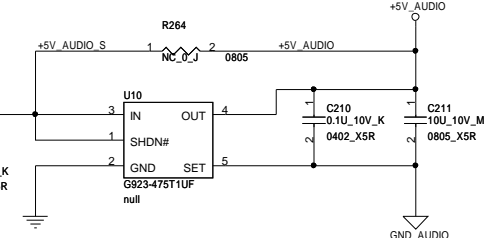
CCPBG

Title: **Transformer & RJ45**

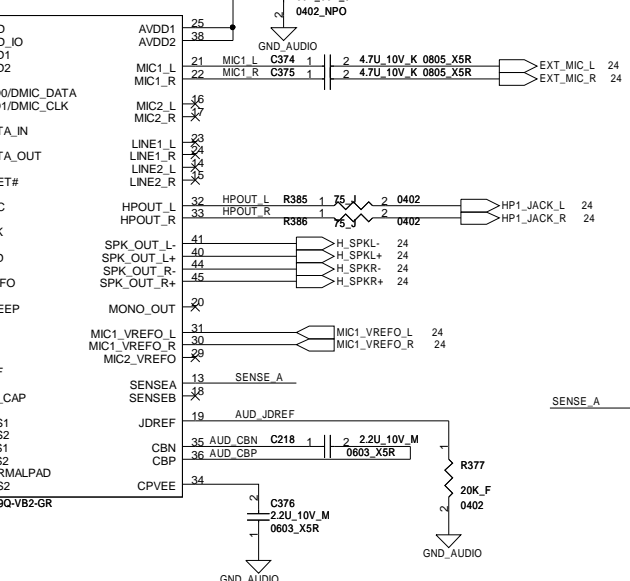
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Audio Power



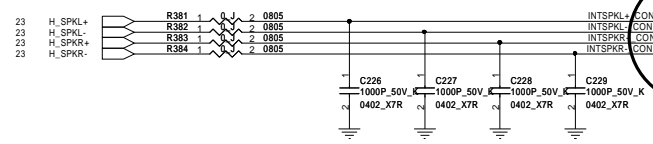
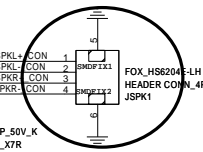
Close to Codec



C215 close to U11 pin39
C221 close to U11 pin46

AUD_PC_BEEP
Trace width > 15

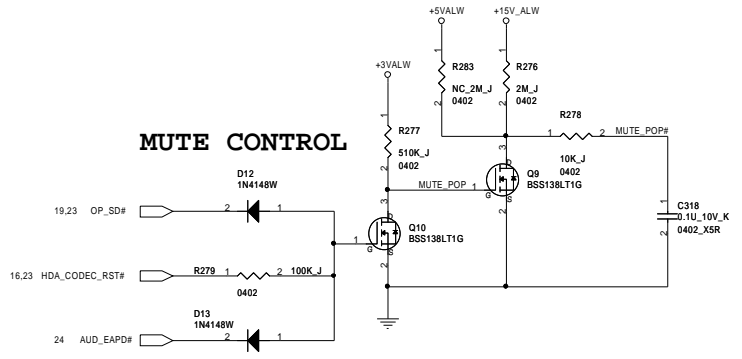
CCPBG		
Title Audio Codec ALC269Q		
Size A3	Document Number M9F1	Rev 0.1
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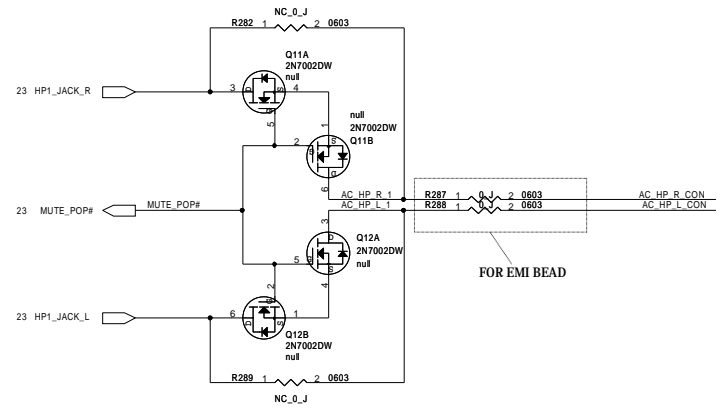
BFT Test Point for Speaker (BOTTOM side)

tpc60b_100	TP87	1	INTSPKL+ CON
tpc60b_100	TP88	1	INTSPKL- CON
tpc60b_100	TP89	1	INTSPKR+ CON
tpc60b_100	TP90	1	INTSPKR- CON

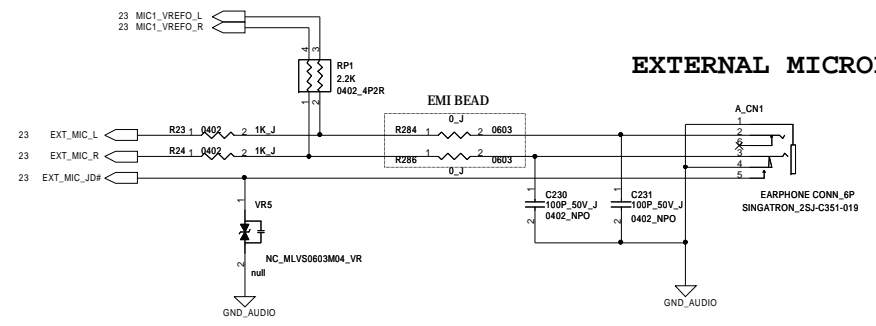
MUTE CONTROL



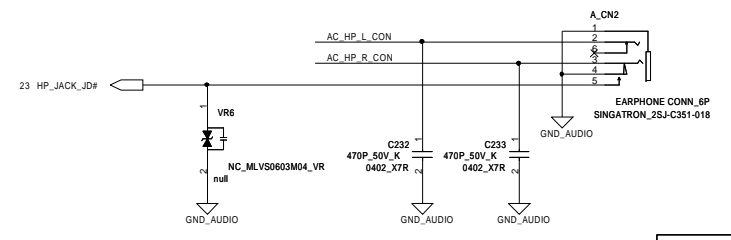
HP CONN



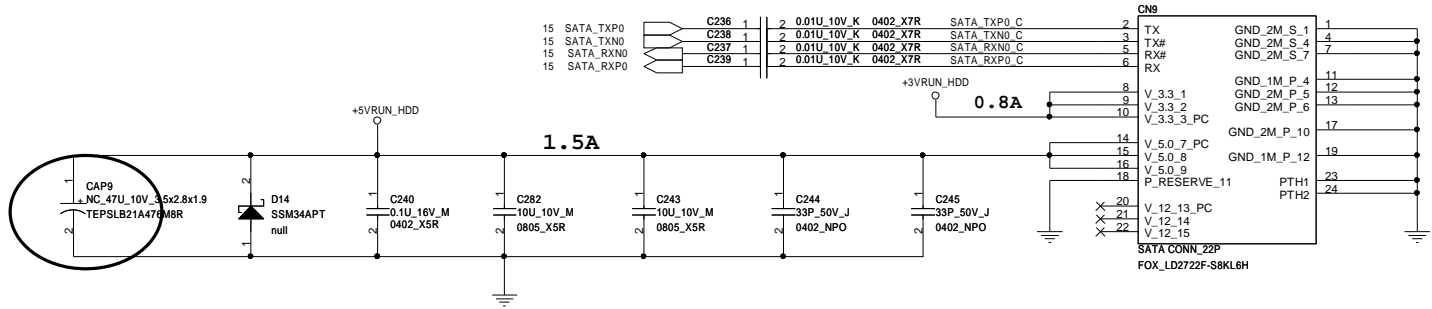
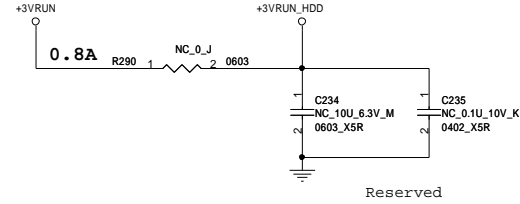
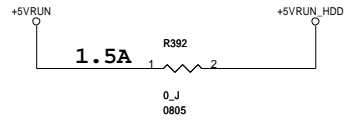
EXTERNAL MICROPHONE



HEADPHONE

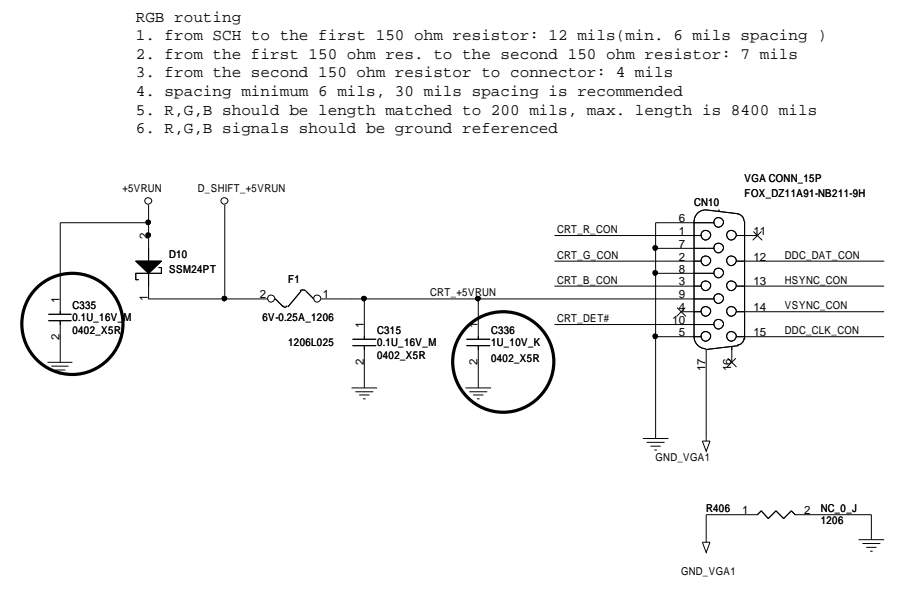
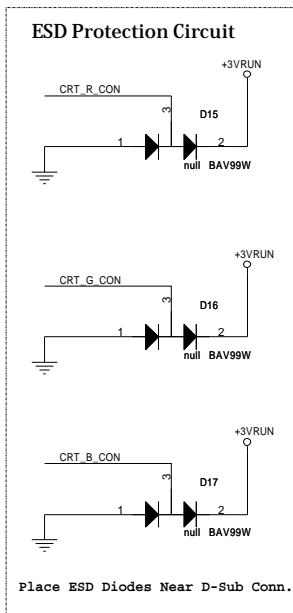
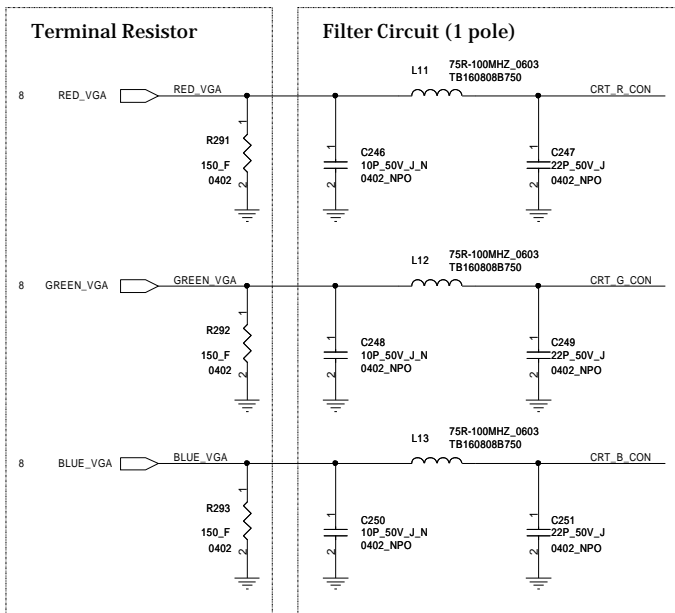


CCPBG			
MIC & Audio Jack			
Title	M9F1		
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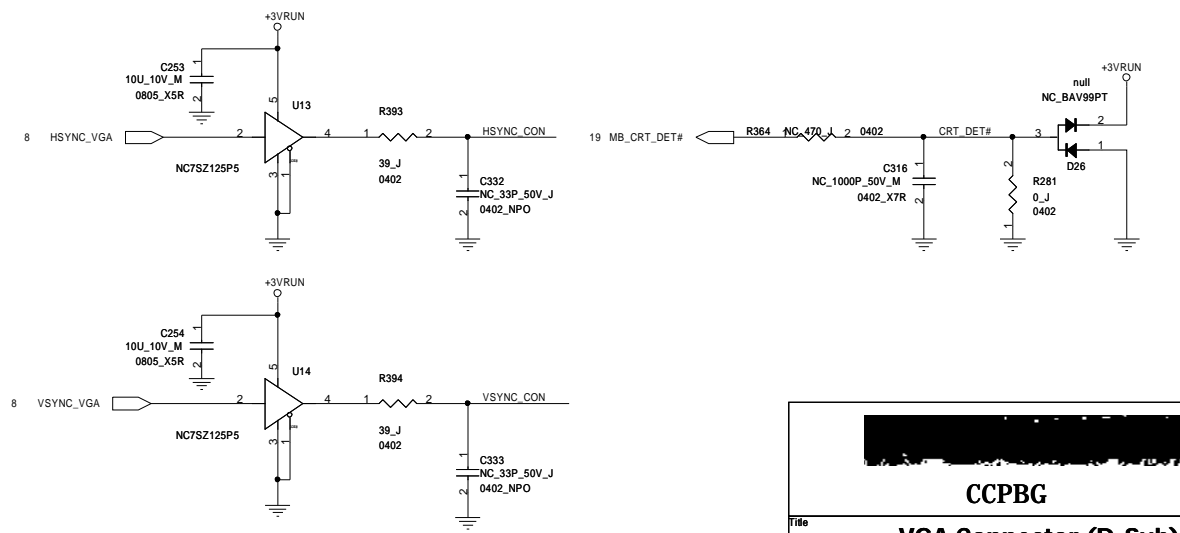
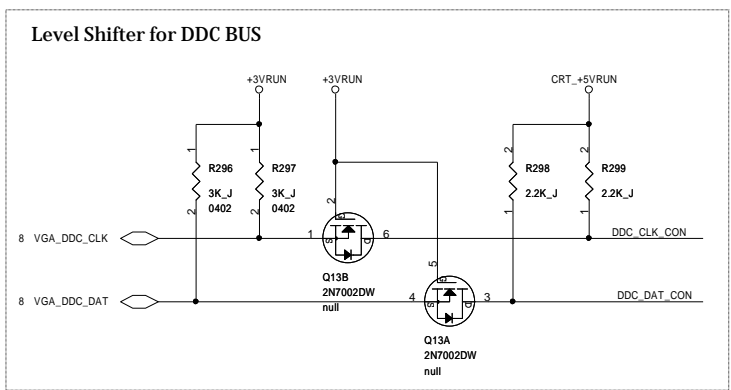


SATA HDD CONN.

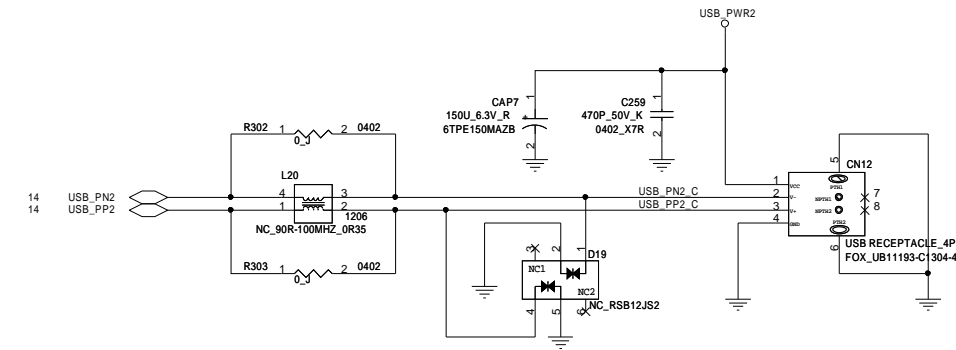
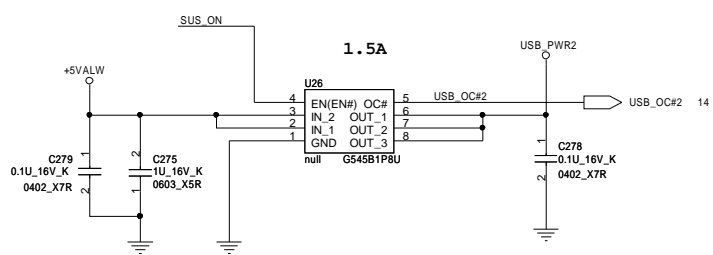
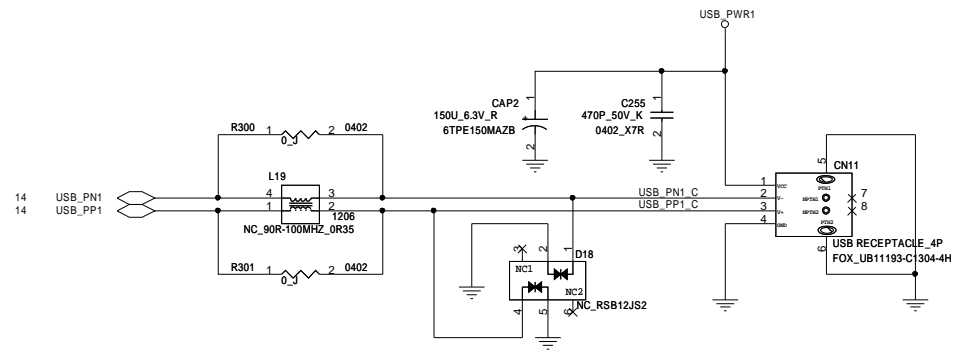
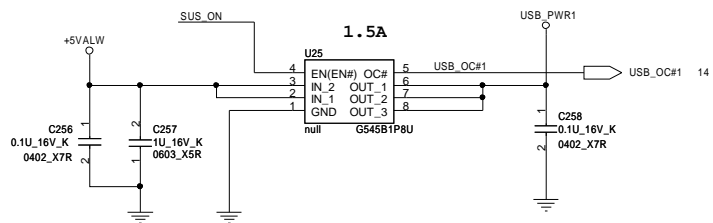
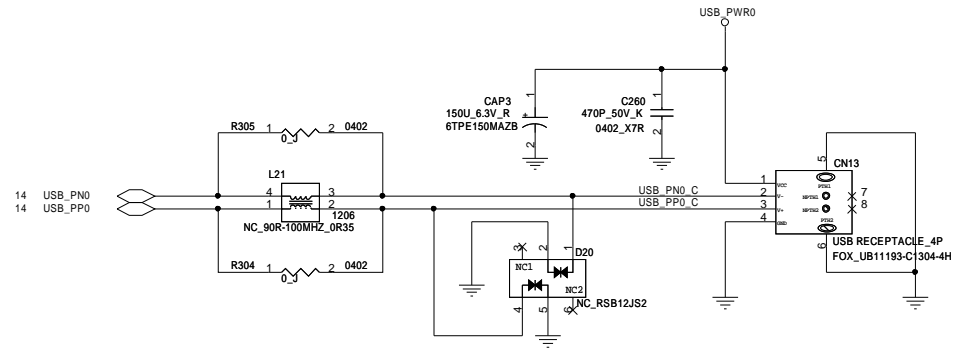
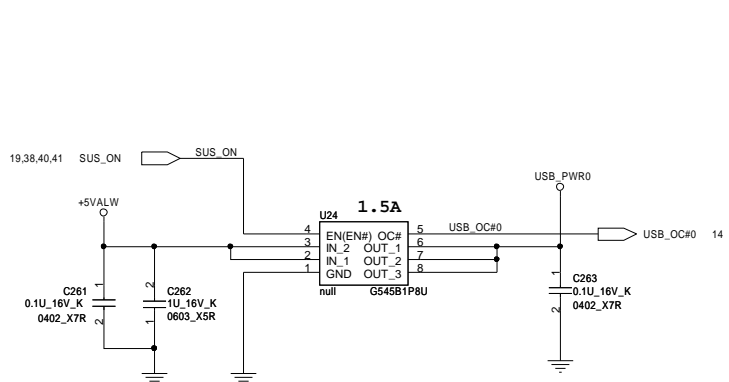
CCPBG		
SATA HDD		
Size A3	Document Number M9F1	Rev 0.1
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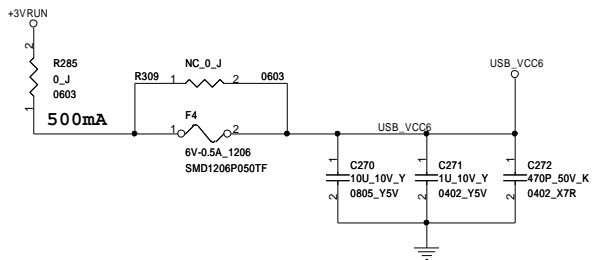
The 150 Ohm resistors near VGA connector and minimizing length to filter. The filters to VGA connector maximum distance 800 mils.



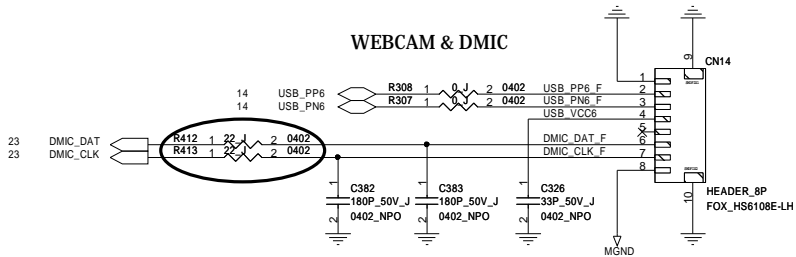
CCPBG			
VGA Connector (D-Sub)			
Title	Document Number		
Size	M9F1		Rev
A3			0.1
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CCPBG		
USB Connector x 3		
Size	Document Number	Rev
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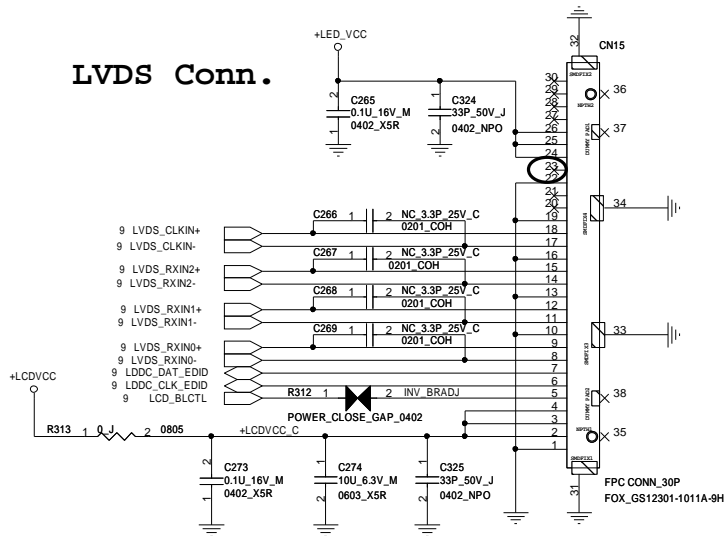
WEBCAM & DMIC



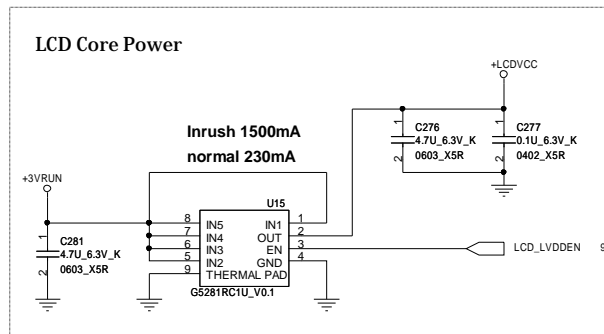
BFT Test Point for Camera (BOTTOM side)

tpc40t_75	TP147	1	USB_PP6_F
tpc40t_75	TP148	1	USB_PN6_F
tpc40t_75	TP149	1	USB_VCC6
tpc40t_75	TP150	1	DMIC_DAT_F
tpc40t_75	TP151	1	DMIC_CLK_F
tpc40t_75	TP152	1	MGND

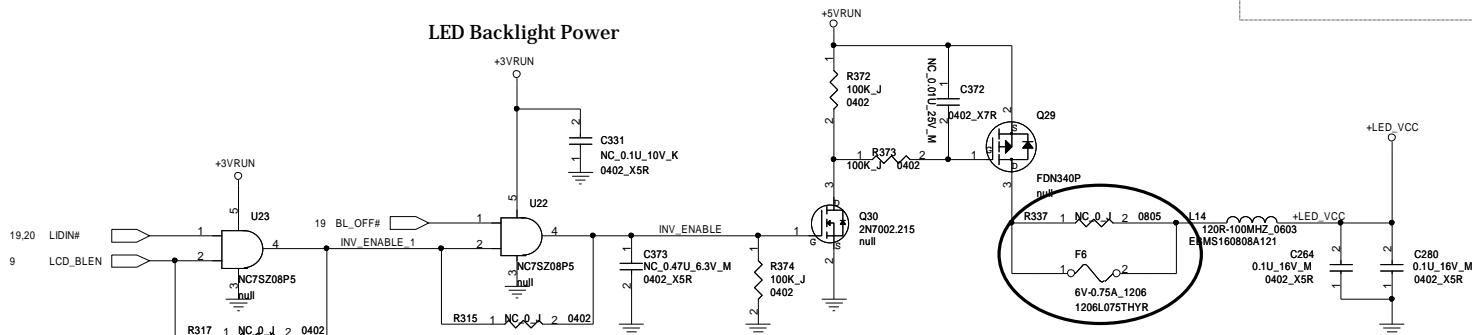
LVDS Conn.



LCD Core Power



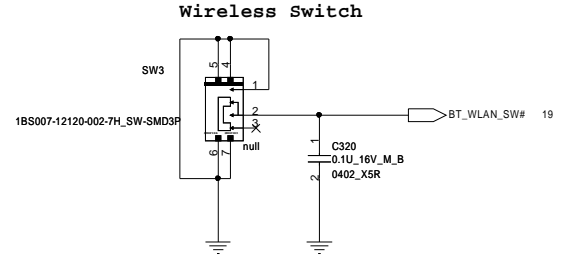
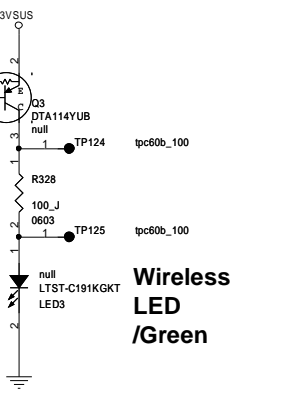
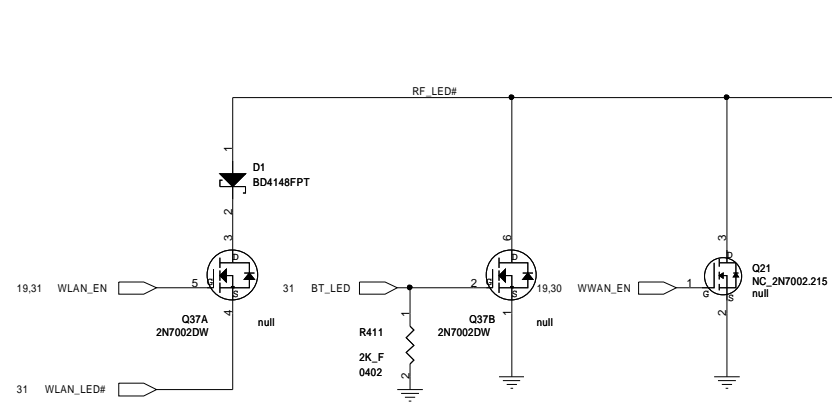
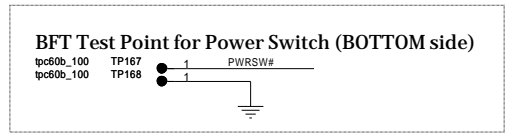
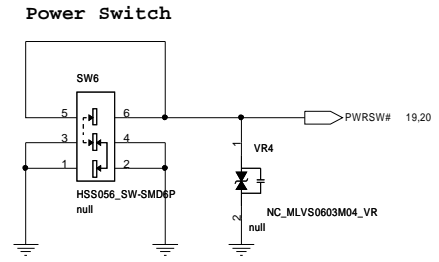
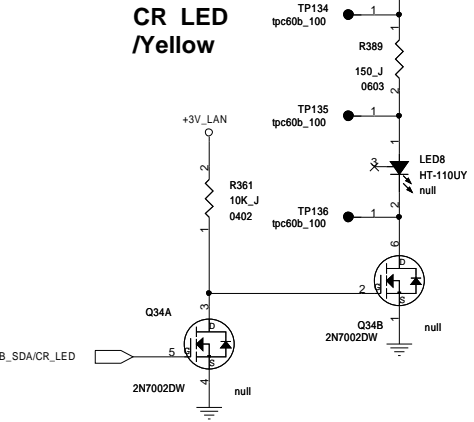
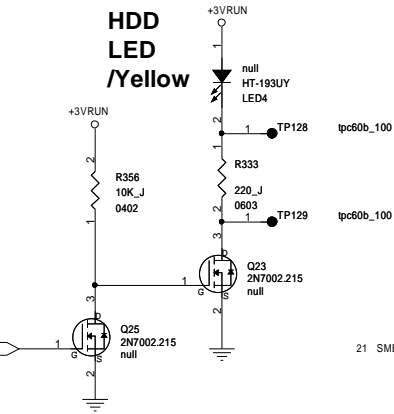
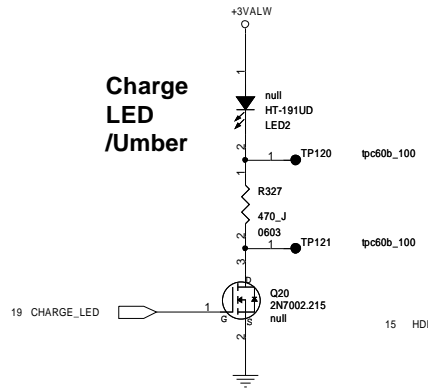
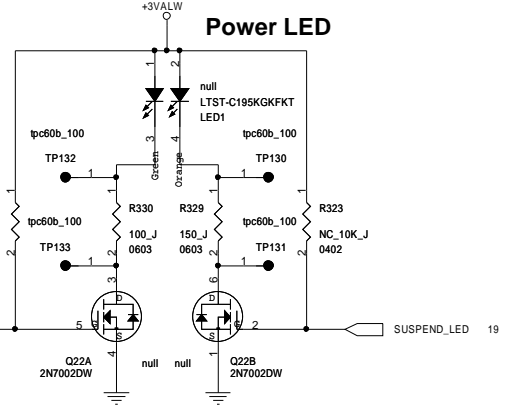
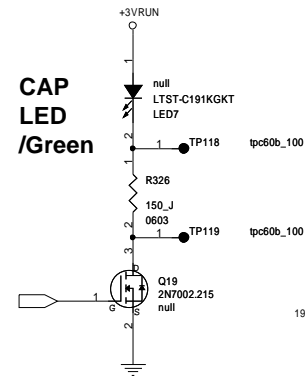
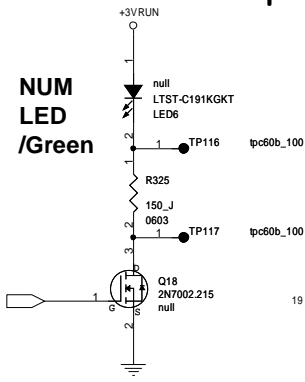
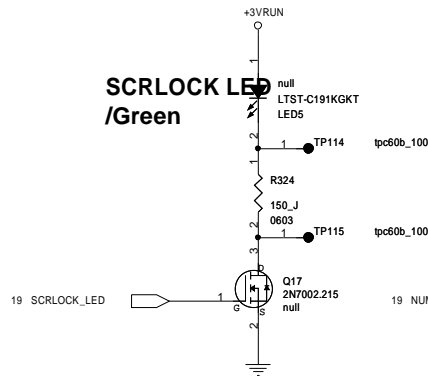
LED Backlight Power



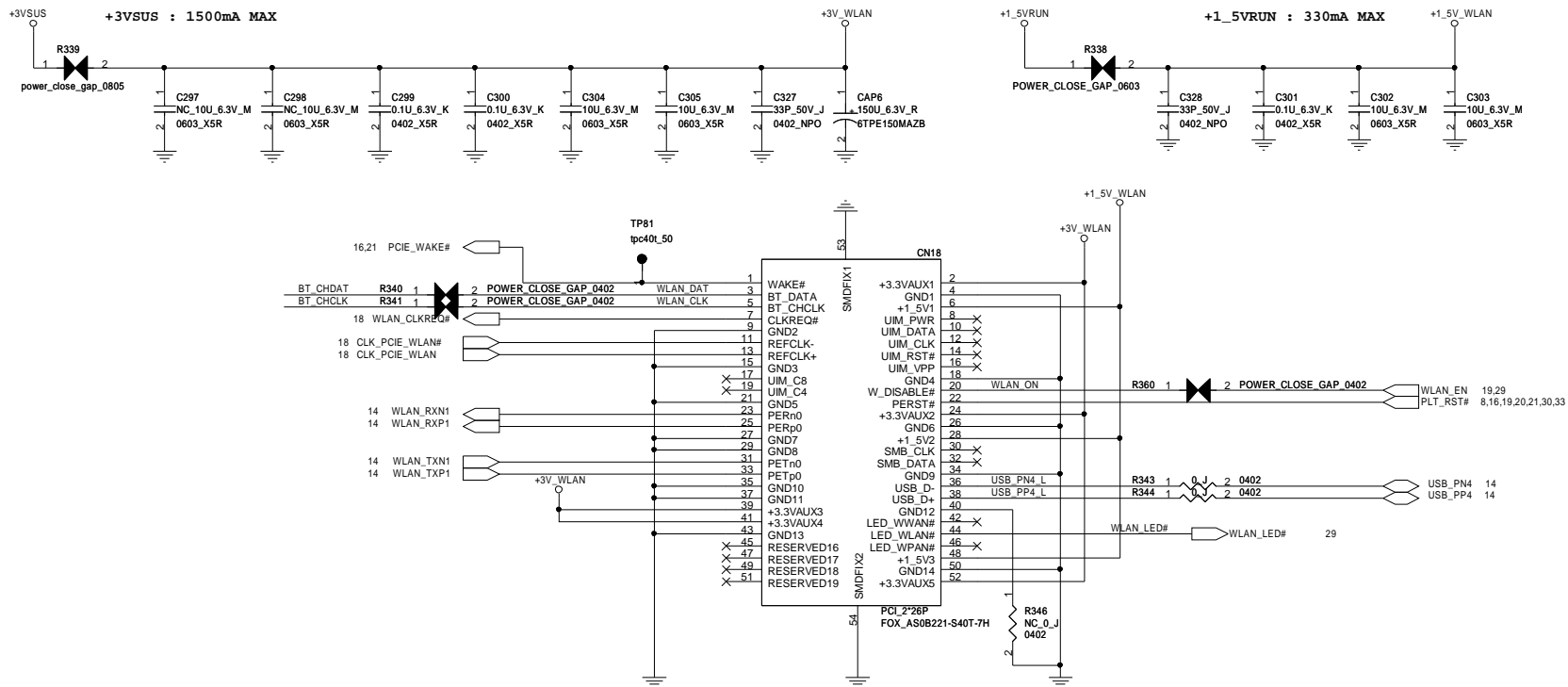
CCPBG

LVDS & WEBCAM

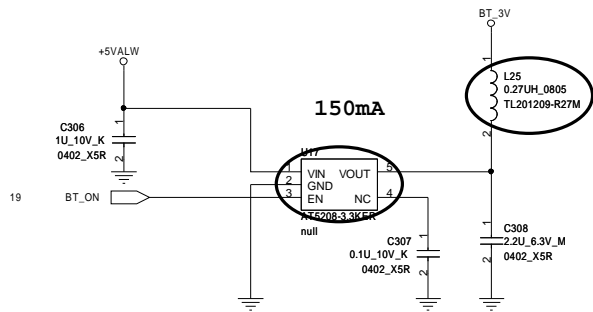
Title	LVDS & WEBCAM	
Size	Document Number	Rev
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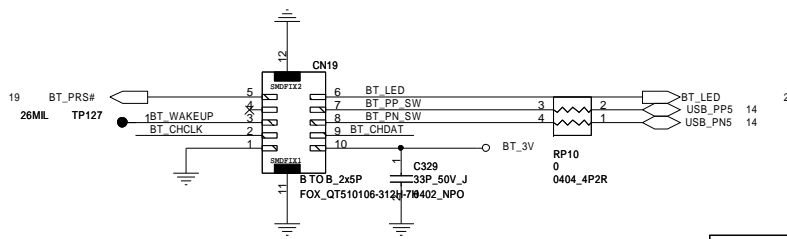
CCPBG		
Title		
Power Switch & LED		
Size	Document Number	Rev
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Half Size Mini Card



Bluetooth CONN.



tpc40L_75	TP141	● 1	BT_PRS#
tpc40L_75	TP142	● 1	BT_3V
tpc40L_75	TP143	● 1	GND

BFT Test Point for Bluetooth (BOTTOM side)

CCPBG

Mini PCIE - WIFI & BT

Title: **Mini PCIE - WIFI & BT**

Size: Custom Document Number: **M9F1** Rev: 0.1

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D

D

C


C

B

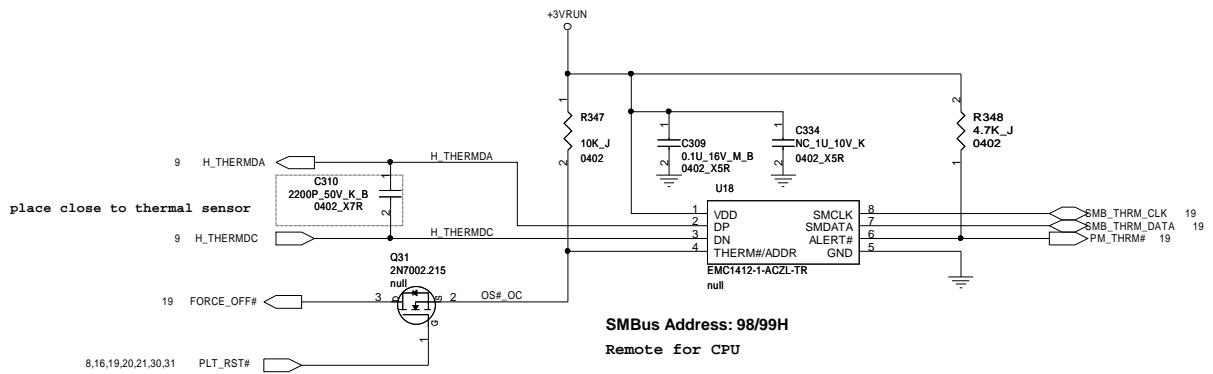
B

A

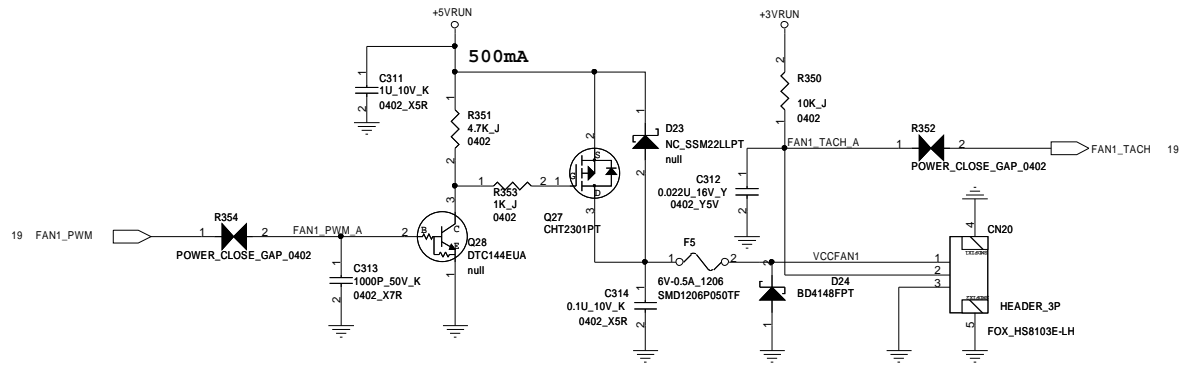
A

		
CCPBG		
Title Reserved		
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CPU Thermal Sensor



FAN



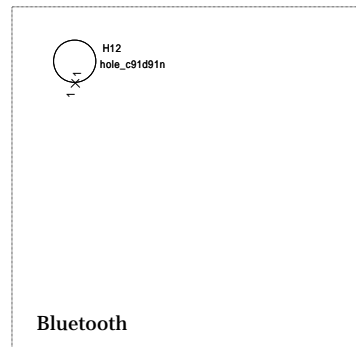
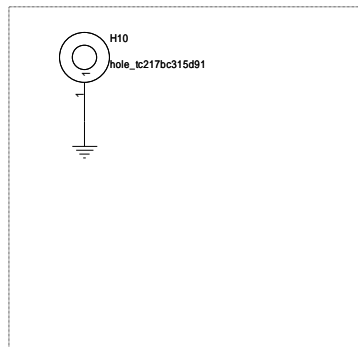
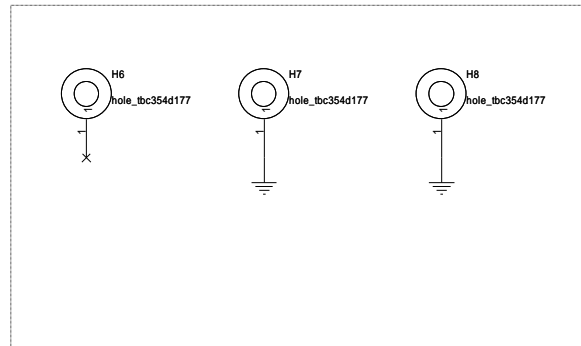
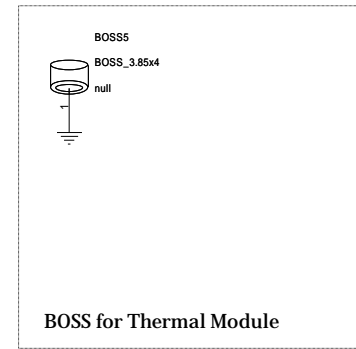
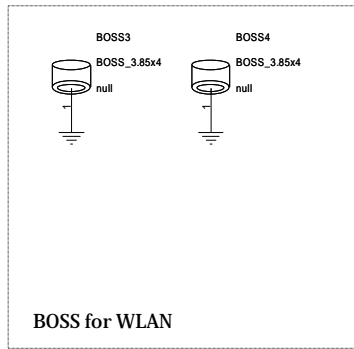
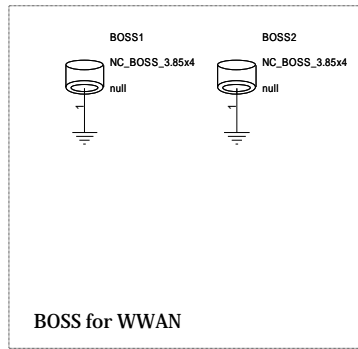
BFT Test Point for FAN (BOT side)


tpc60b_100	TP83	1	VCCFAN1
tpc60b_100	TP84	1	FAN1_TACH_A
tpc60b_100	TP85	1	GND
tpc60b_100	TP86	1	FAN1_PWM_A

CCPBG

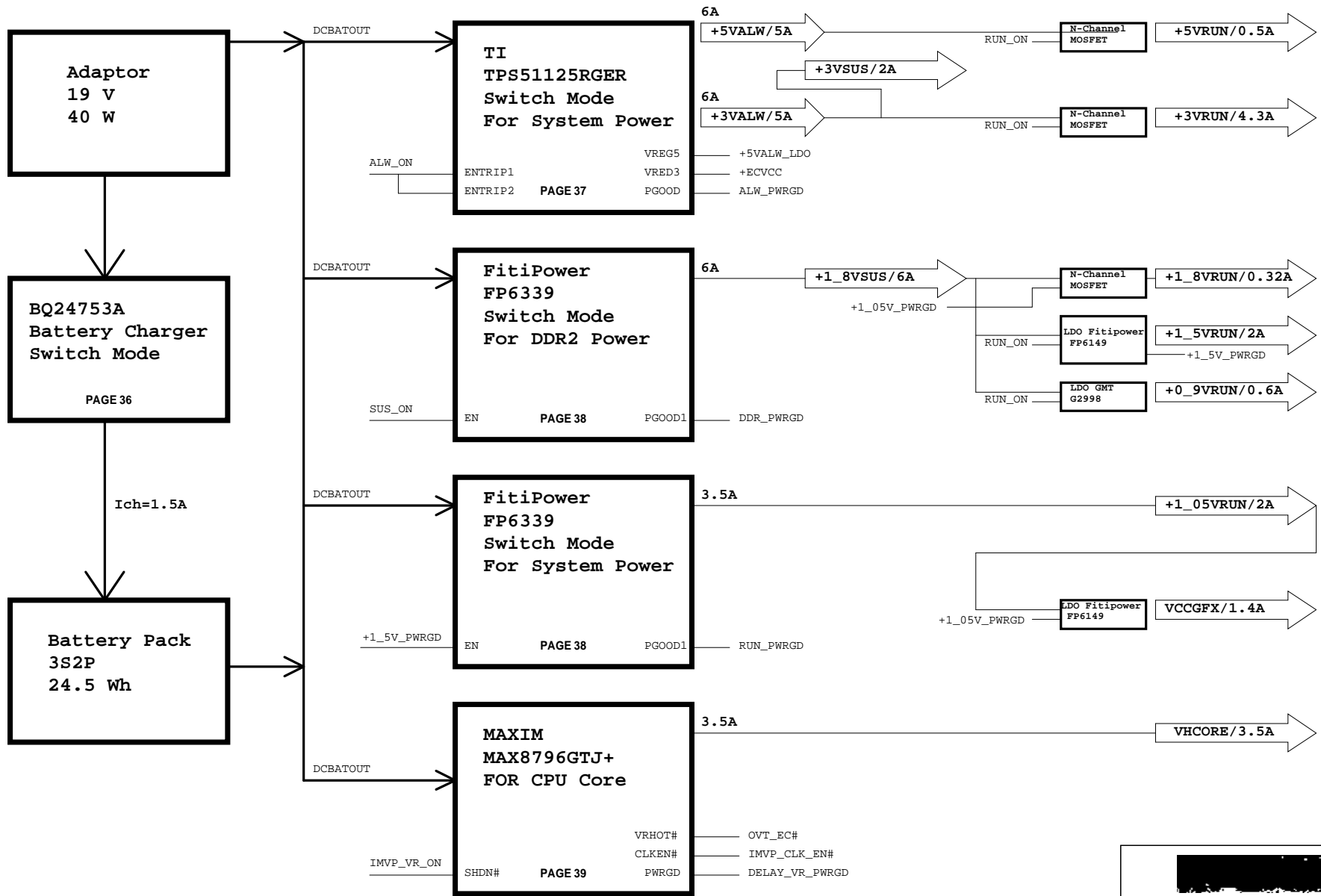
Title Thermal & Fan

Size A3	Document Number M9F1	Rev 0.1
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CCPBG			
Title			
ME NUT & EMI			
Size	Document Number	Rev	
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M9F1 Power Block Diagram

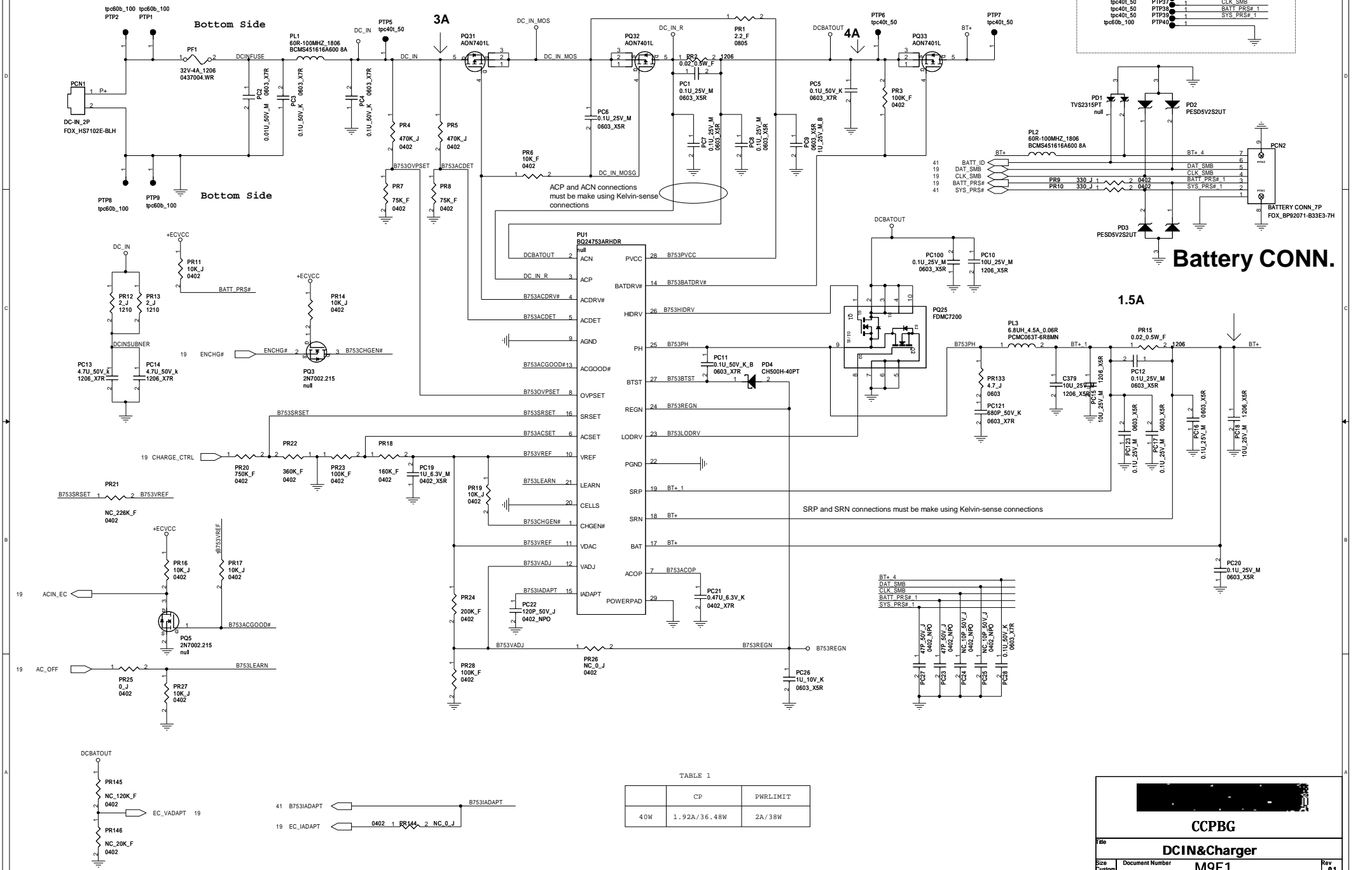


CCPBG		
Power Block Diagram		
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M9F1 DCIN&Charger

BFT Test Point for Battery (BOTTOM side)

tpc60b_100	PTP9	1	BATT ID
tpc40l_50	PTP30	1	BATT ID
tpc40l_50	PTP30	1	DAT SMB
tpc40l_50	PTP30	1	CLK SMB
tpc40l_50	PTP30	1	BATT_PRS# 1
tpc40l_50	PTP30	1	SYS_PRS# 1
tpc60b_100	PTP40	1	



ACP and ACN connections must be make using Kelvin-sense connections

SRP and SRN connections must be make using Kelvin-sense connections

Battery CONN.

TABLE 1

	CP	PWRLIMIT
40W	1.92A/36.48W	2A/38W

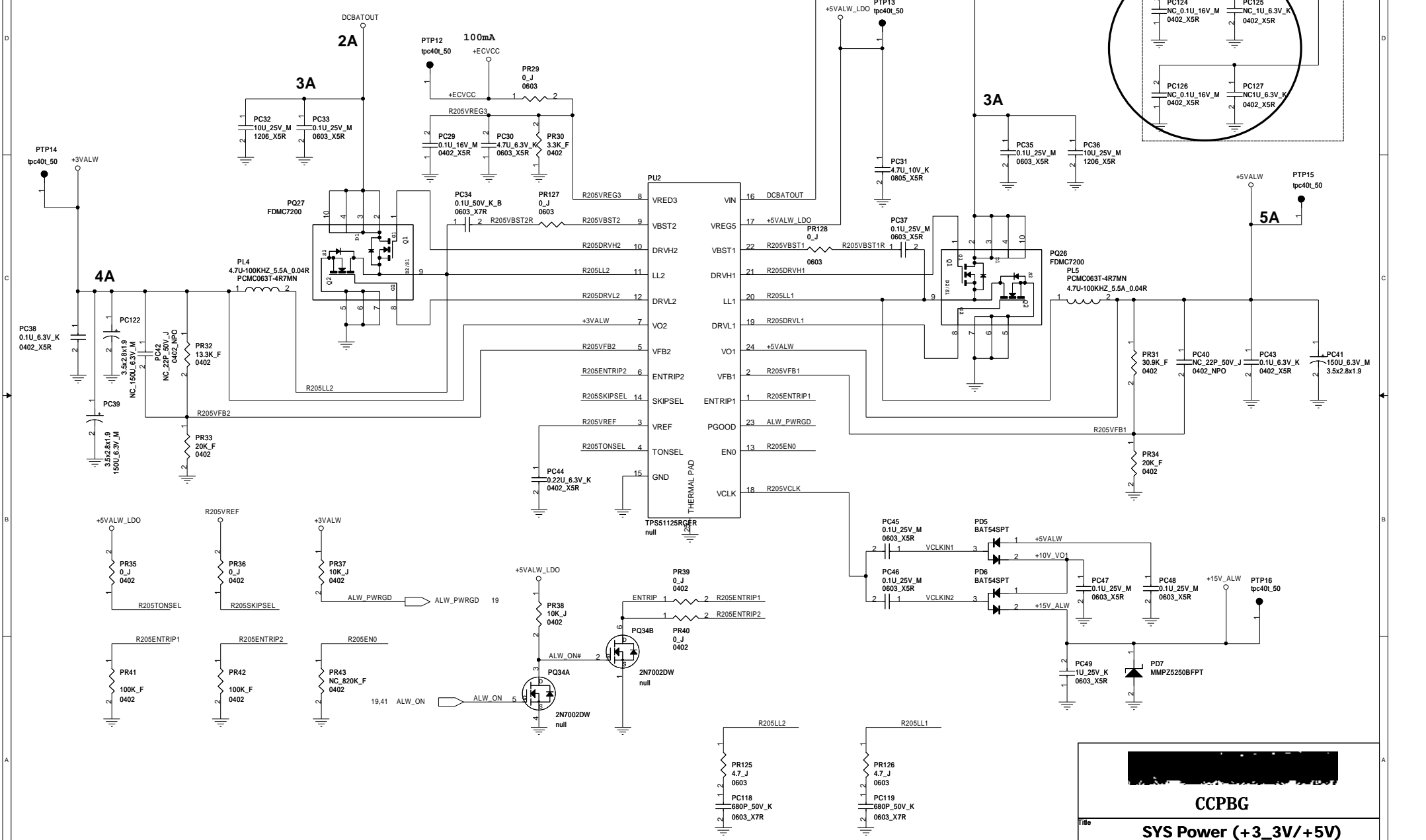
CCPBG

File: **DCIN&Charger**

Size: Custom Document Number: **M9F1** Rev: 0.1

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M9F0 SYS Power (+3_3V/+5V)

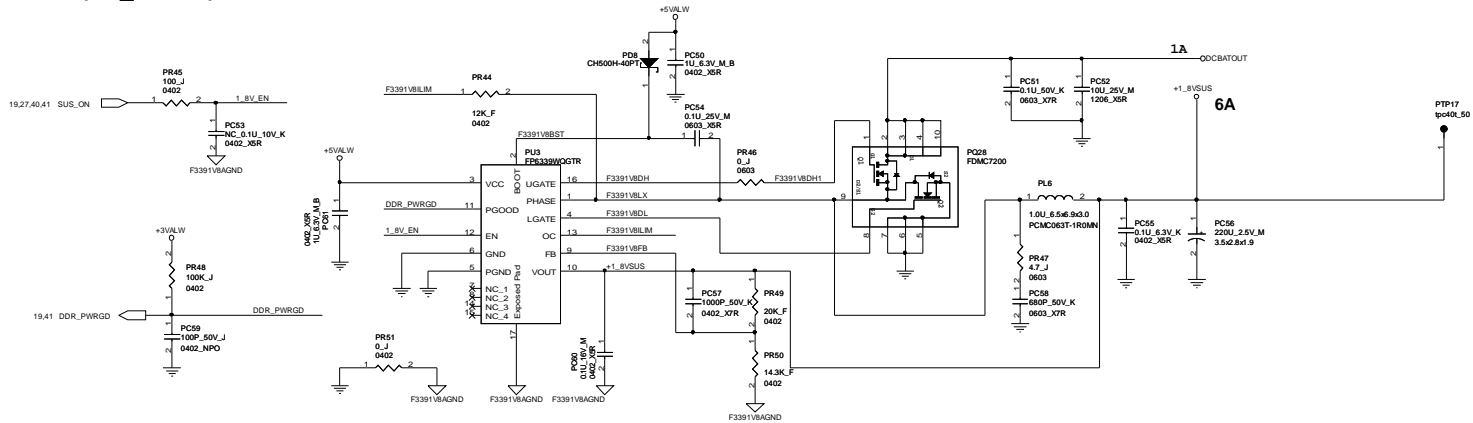


CCPBG

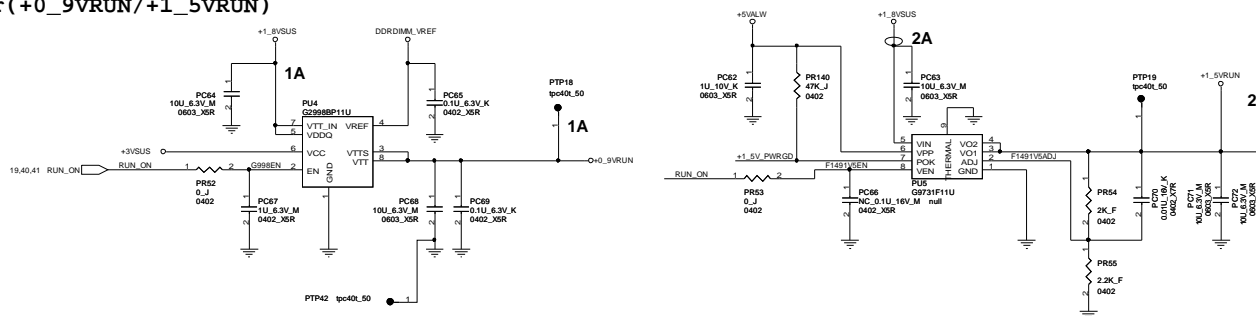
Title: **SYS Power (+3_3V/+5V)**

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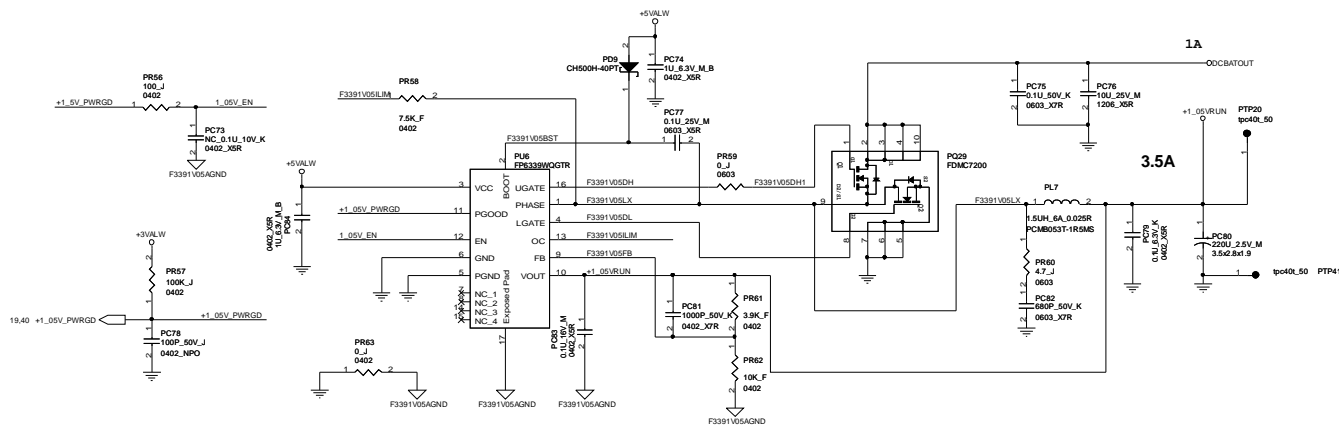
M9F1 SYS Power(+1_8VSUS)



M9F1 SYS Power(+0_9VRUN/+1_5VRUN)

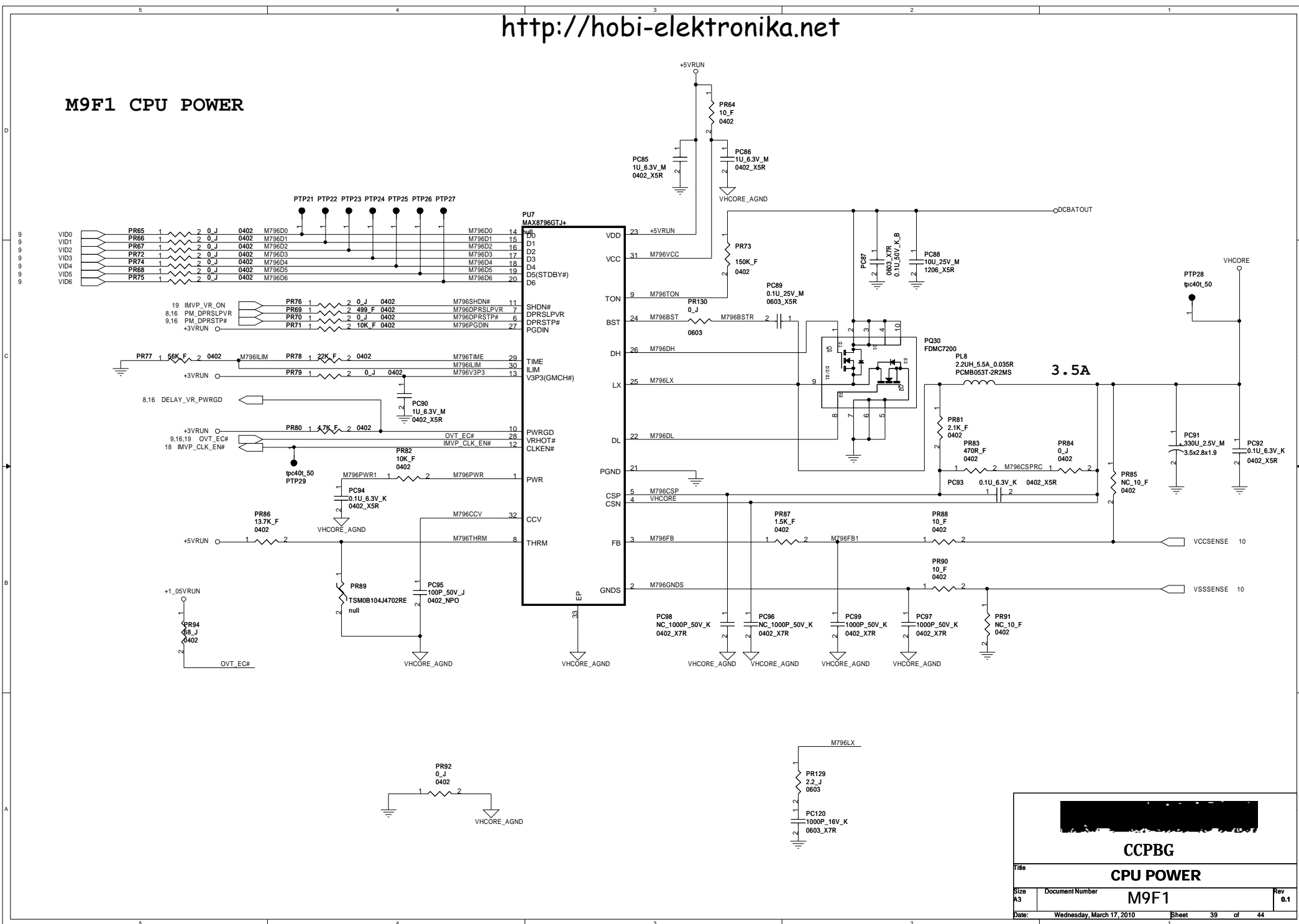


M9F1 SYS Power(+1_05V)



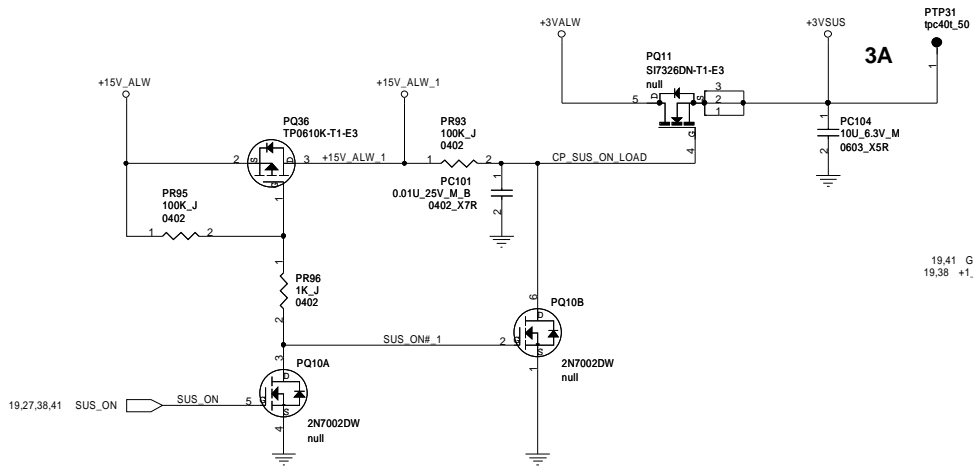
CCPBG		
SYS Power(+1_8V/+1_05V)		
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M9F1 CPU POWER

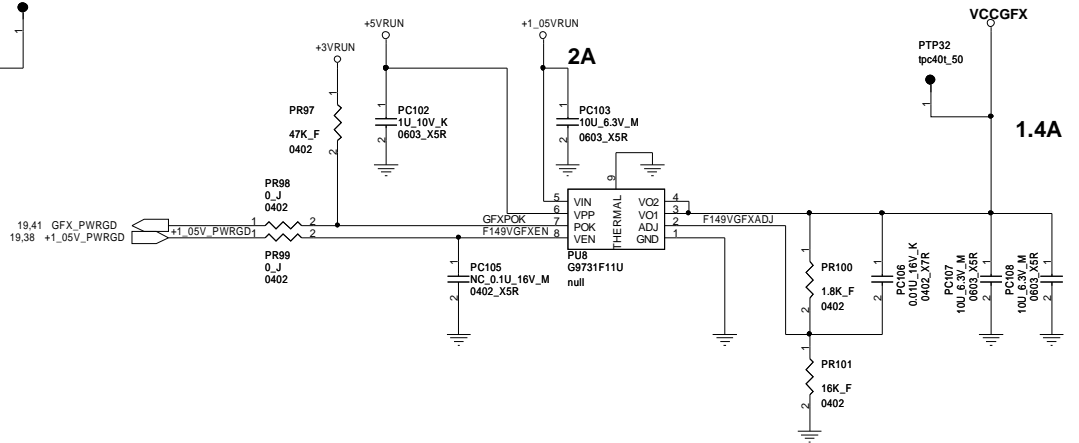


CCPBG		
CPU POWER		
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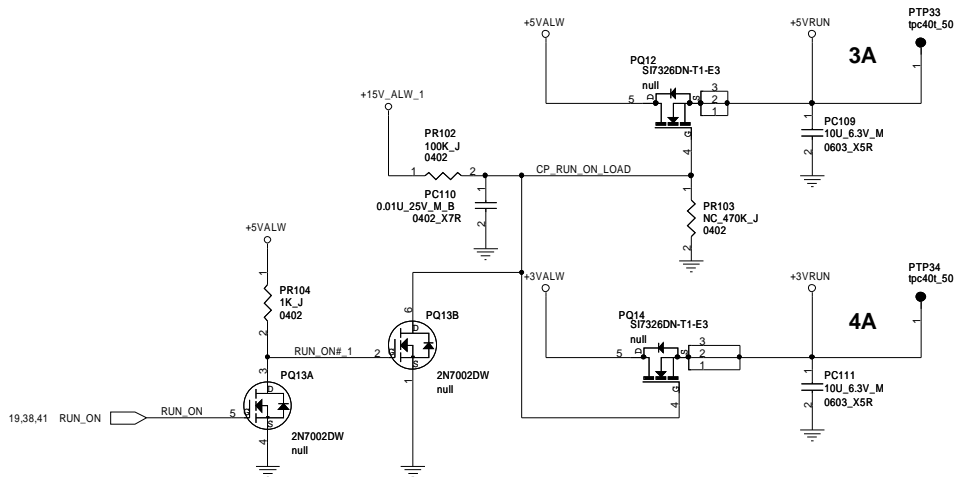
M9F1 Others power plan (+3VSUS)



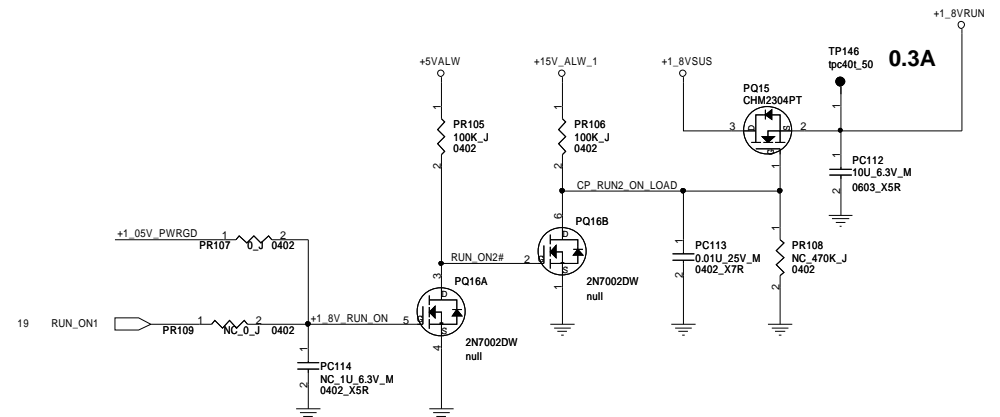
M9F1 GFX Power (VCCGFX/+0.89V)



M9F1 Others power plan (+5VRUN/+3VRUN)



M9F1 Others power plan (+1_8VRUN)



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Others power plan		
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M9F1 EVT

2010/01/27

1. P22, Remove net "GND_VGA" and make CN8.9 & CN8.11 no connect
2. P26, Remove net "GND_VGA" and make CN10.16 no connect
3. P26, Delete R407

2010/02/01

1. P21, Change R409 and R410 footprints from 0805 to 1206.
2. P26, Change R406 footprint from 0805 to 1206.

2010/02/02


1. P28, Add U23, Reserve R317 for Lid Switch control LVDS backlight.
2. P19, Delete RF_LED#.
3. P29, Add Q37, D1, Q3, Reserve D2, R411 for wireless LED.
4. P30, Add WWAN_LED#.
5. P31, Delete TP91, TP126.
6. P34, Unconnect H6 to GND.
7. P36, Add PR139, PR144 for powerlimit EC control.
8. P41, NC PC116, PU9, PR118, PC115, PR122, PR123, PR124 for powerlimit EC control.
9. P19, Add C720.
10. P40, Change PQ11, PQ12, PQ14 to SI7326DN-T1-E3.
11. U39 Co-layout with U12.

2010/02/03

1. P19, Add C721.
2. P36, Add PR145, PR146.
3. P36, Change PR18 to 160K.
4. P19, Change EC_VADAPT to U5.100, BT_WLAN_SW# to U5.124.
5. P21, Reserve C381, C386, C387, C388, C389, C390, C391, C392, C393.
6. P29, Delete D2.
7. P30, Delete WWAN_LED#.
8. P37, Stuff PC39, NC PC122.
9. P28, NC CN15.32, CN15.34.

2010/02/04

1. P29, Change R411 to 100K.

			
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M9F1 DVT

2010/02/05

1. P26, Change U13, U14 to 14-NC7S212-5P00.

2010/02/10

1. P19, Add R233 to reserve one GPIO for BT_WLAN_SW# (default NC, use U5.100 to be wireless switch)
2. P19, Add R357 and R359 to reserve U5.100 for wireless switch and power limit (default R357 is 0ohm and R359 is NC)
3. P19, set C720 and C721 to be NC.
4. P16, stuff PU9, PC116, PR118, PC115, PR123 and PR124 for hardware power limit
5. P41, Set R136 and R138 to be NC, and set R270 and R272 to be 10K. MB ID = 00 for M9F1

2010/02/22

1. P20, Delete U39
2. P28, CN15.32 and CN15.34 connects to GND.
3. P16, Change CN2 to 1N-0002009-M1T0.
5. P34, Delete SPR1.
6. P36, Change PCN2 to 2N-000700Y-MKG0.
7. P29, Change R411 to 2K.

2010/02/23

1. P41, NC PR132, PR110, PR111, PR112, PR113, PR114, PR115, PR131, PR116, PR143, PQ7, PQ37, PQ39, PQ40, PQ6, PQ45.



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M9F1 PVT

2010/03/11

1. P24, Change JSPK1 to 1N-000400C-M1T0.
2. P31, Change U17 to 15-AT52083-0000, change R358 to L25 .
3. P20, Change CN3 to 1N-0006004-FXT0.
4. P28, Change CN15.23 from GND to NC.
5. P28, Change L23, L24 to R412, R413.
6. P36, Delete PR139.
7. P19, Change R357 to close jump.
8. P26, Add C335, C722.
9. P21, Change R398, R399, R400, R401, R402, R403, R404, R405 to 56ohm.

2010/03/12


1. P19, Stuff R342, R345 for system ID.
2. P25, Reserve CAP9.
3. P10, Reserve D34, D35, D36.

2010/03/15

1. P26, C722 change to C336
2. P24, JSPK1 changes net name for speaker pin compatible
3. P37, Add PC124, PC125, PC126 and PC127 for EMC
4. P18, Add R390, R391.
5. P25, Change CAP9 to 1C-44R0476-M200.
6. P21, Change R409, R410 to stuff.

2010/03/15

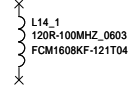
1. P28, Change F6 to 1M-F6V0A75-0002, NC R337.
2. P18, Change R390, R391 to 33ohm.

		
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PVT Change Note		
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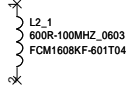
Main Source: 1L-DPCMC06-3T07.
2nd Source: 1L-DSLH063-0600.



Main Source: 1L-BEBMS16-0800.
2nd Source: 1L-BFCM160-8K08.



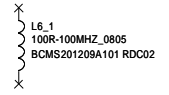
Main Source: 1L-BEBMS06-A600.
2nd Source: 1L-BFCM160-8K06.



Main Source: 1L-DL0M18N-NR01.
2nd Source: 1L-DFC1160-8F01.

L1

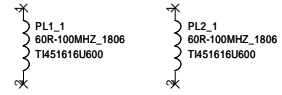
Main Source: 1L-BHPB082-1000.
2nd Source: 1L-BBCMS20-1202.



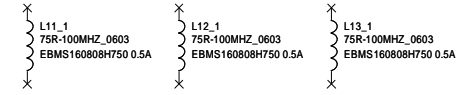
Main Source: 1T-00004U7-0000.
2nd Source: 1L-DSLH063-0400.



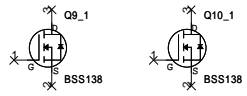
Main Source: 1L-BBCMS45-1600.
2nd Source: 1L-BT14516-1601.



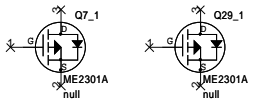
Main Source: 1L-BTB1608-0804.
2nd Source: 1L-BEBMS16-080D.



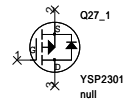
Main Source: 17-BSS138L-T100.
2nd Source: 17-BSS1380-0000.



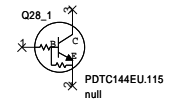
Main Source: 17-FDN340P-0000.
2nd Source: 17-ME2301A-0000.



Main Source: 17-CHT2301-PT00.
2nd Source: 17-YSP2301-0000.

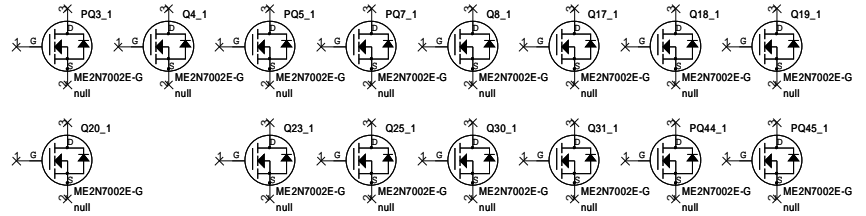
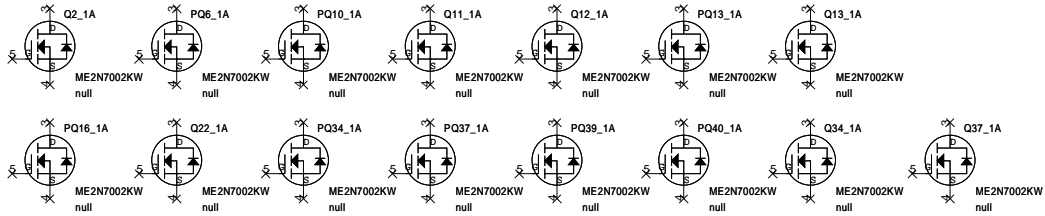


Main Source: 17-DTC144E-UA00.
2nd Source: 17-PDTC144-EU00.

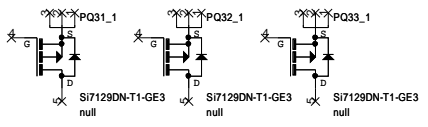


Main Source: 17-2N7002D-W001.
2nd Source: 17-ME2N700-2K00.

Main Source: 17-2N70020-0001.
2nd Source: 17-ME2N700-2E01.

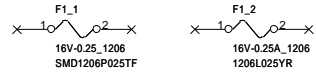


Main Source: 17-A0N7401-L000.
2nd Source: 17-S17129D-NT00.



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Main Source: 1M-F6V0A25-F000.
2nd Source: 1M-F16VA25-F000.



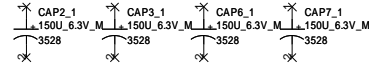
Main Source: 1M-F10V0A1-F000.
2nd Source: 1M-F30VA12-F000.

F9

Main Source: 1C-30R0157-M100.
2nd Source: 1C-41X0157-M100.



Main Source: 1C-41R0157-M100.
2nd Source: 1C-33R0157-M101.



Main Source: 1C-30R0227-MX00.
2nd Source: 1C-41R0227-MX01.



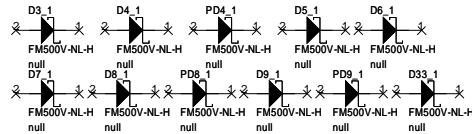
Main Source: 16-BAT545P-T000.
2nd Source: 16-BAT54S0-0002.

PD5, PD6

Main Source: 16-MMP2525-0B01.
2nd Source: 16-MM3220V-C000.



Main Source: 16-CH500H4-0P00.
2nd Source: 16-FM500VN-L000.



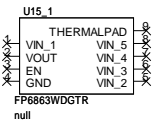
Main Source: 16-CH520S3-0P00.
2nd Source: 16-RB520S0-0000.



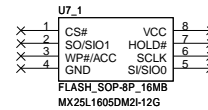
Main Source: 16-1SS400P-T000.
2nd Source: 16-1SS4000-0001.



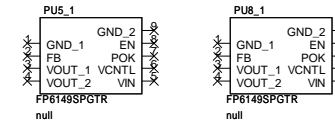
Main Source: 15-G5281RC-V000.
2nd Source: 15-FP6863W-0000.



Main Source: 13-W25016B-7001.
2nd Source: 13-MX25L16-7003.



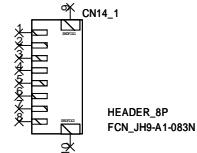
Main Source: 15-G9731F1-0000.
2nd Source: 15-FP6149S-0000.



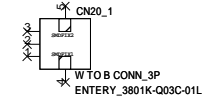
Main Source: 1N-0030000-MKG0.
2nd Source: 1N-003000F-FKGO.

CN15

Main Source: 1N-0008006-M1T0.
2nd Source: 1N-0008000-F1T0.

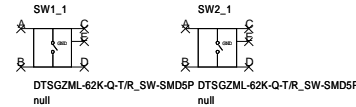
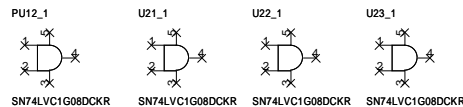


Main Source: 1N-0003004-M1T0.
2nd Source: 1N-0003001-MXT0.



Main Source: 14-NC7S208-P500.
2nd Source: 14-SN74LVC-1G14.

Main Source: 19-1BT0011-1000.
2nd Source: 19-DTSG2ML-1000.



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2nd Source_2		
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