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28	TV-Tuner Connector	SD	68	Audio (Power)	SD
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DVT2 BOM Control Table

VALUE Head	CA_	AT_	M86_	M82_	NC_
UMA	stuff	Un-stuff	Un-stuff	Un-stuff	Un-stuff
Discrete VGA with M86	Un-stuff	stuff	stuff	Un-stuff	Un-stuff
Discrete VGA with M82	Un-stuff	stuff	Un-stuff	stuff	Un-stuff

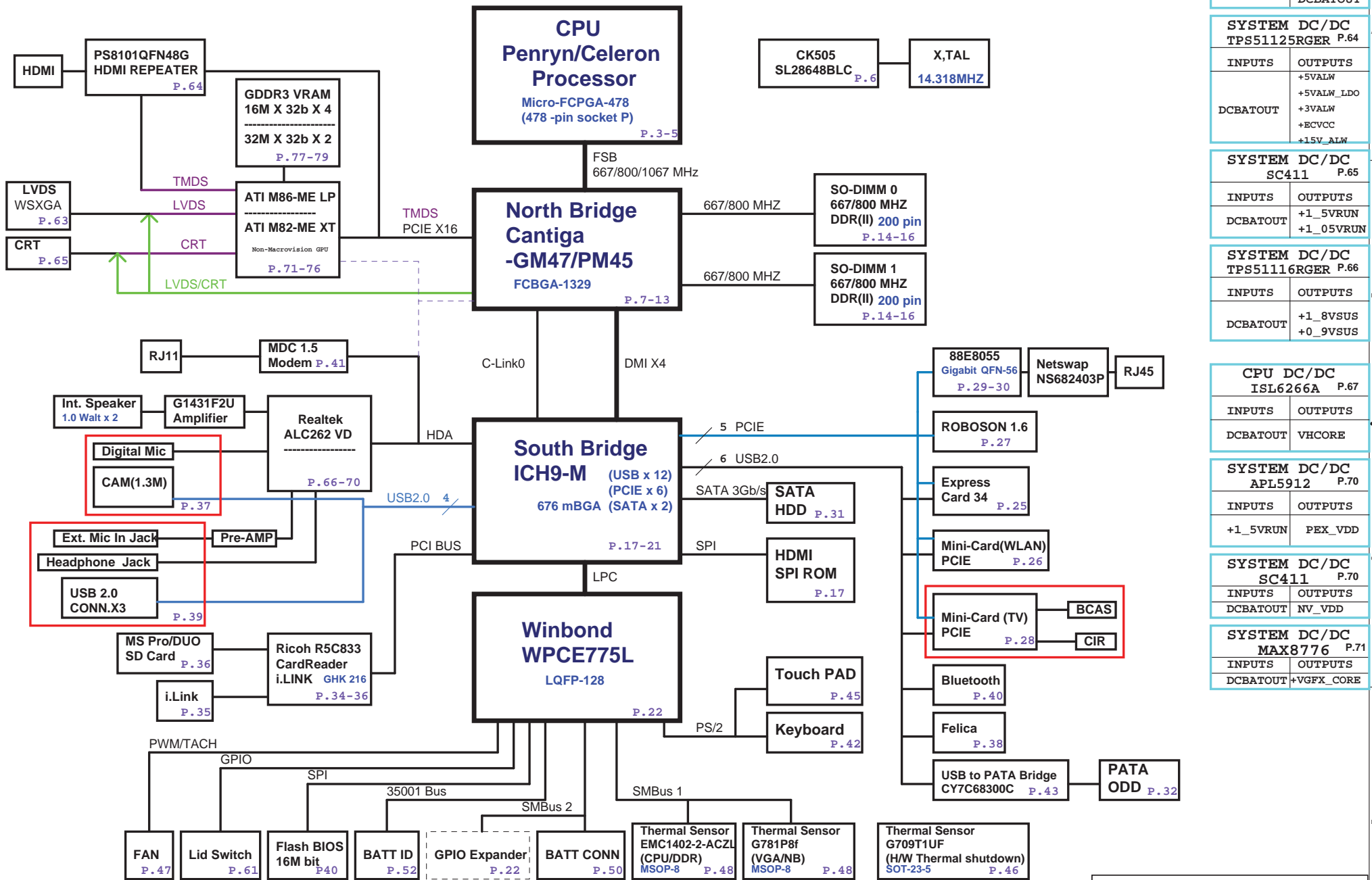
Project Code & Schematics Subject: M760 Main Board

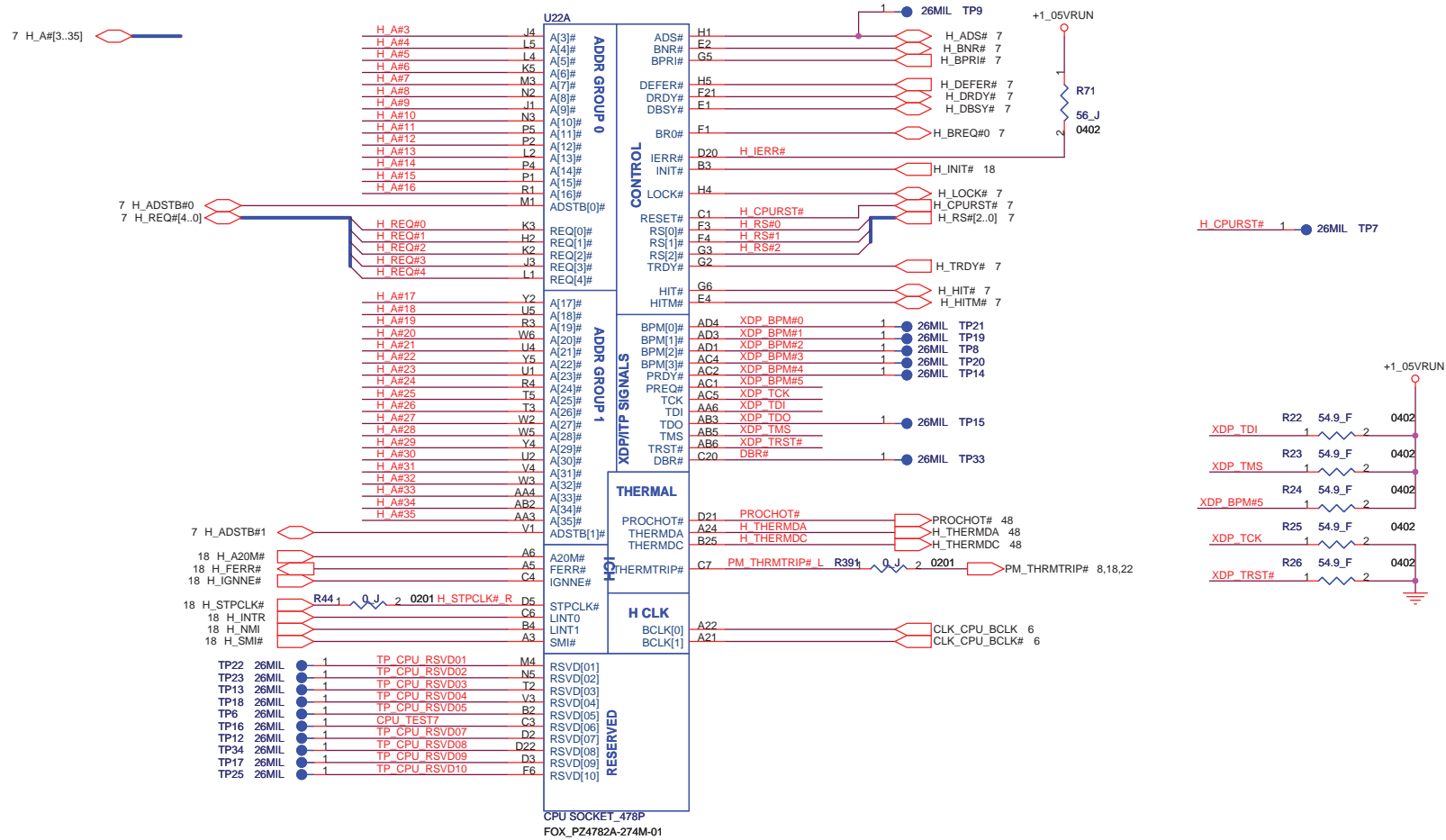
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 HANNSTAR (1P-0083500-8010)
 IRIS (1P-0083J01-8010)

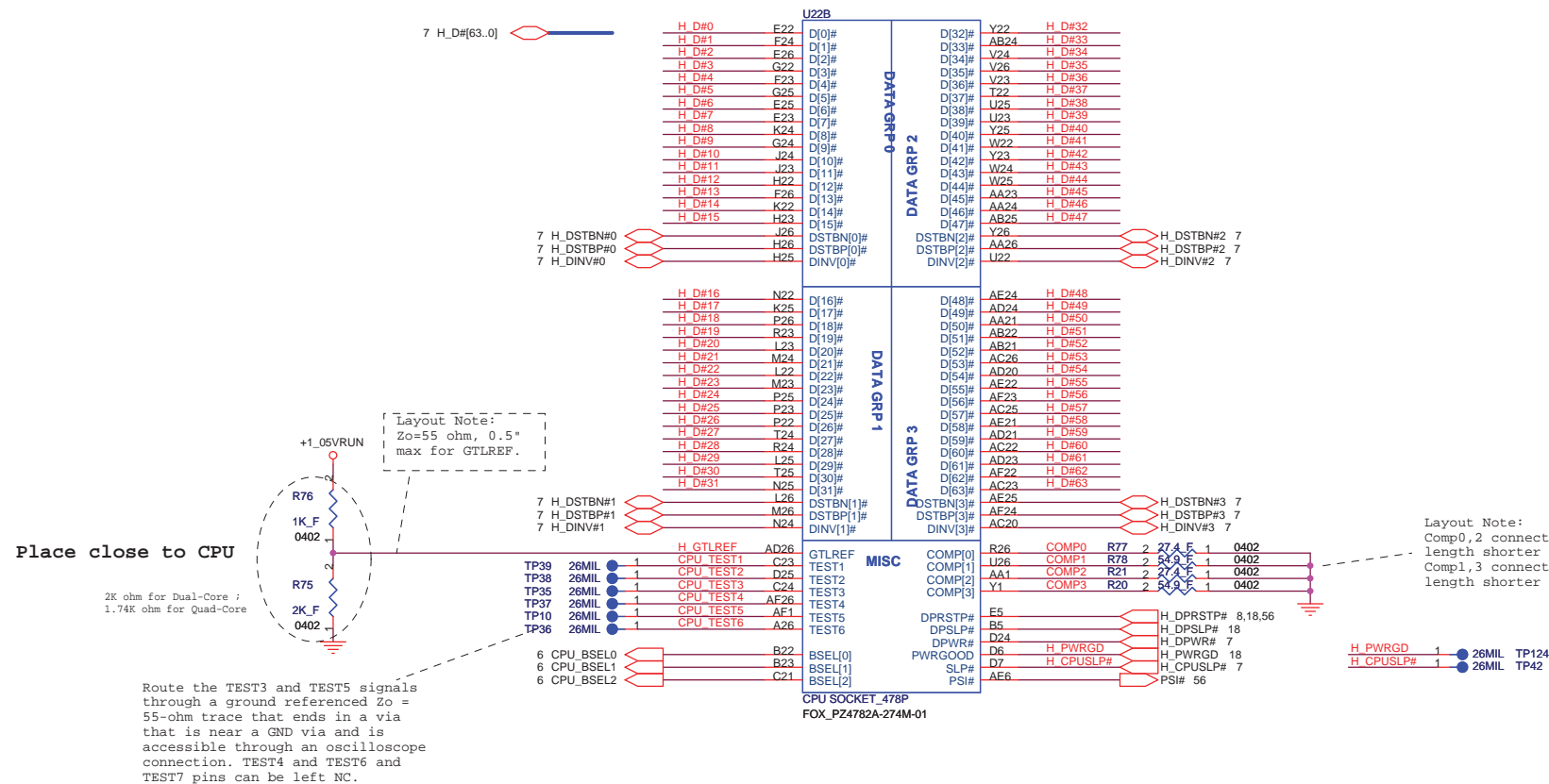
P. Leader	Check by	Design by
JERRY HSIAO	JERRY HSIAO	TONY CHENG

FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
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M760 (IRX-4370) Montevina + M86-LP/M82-XT







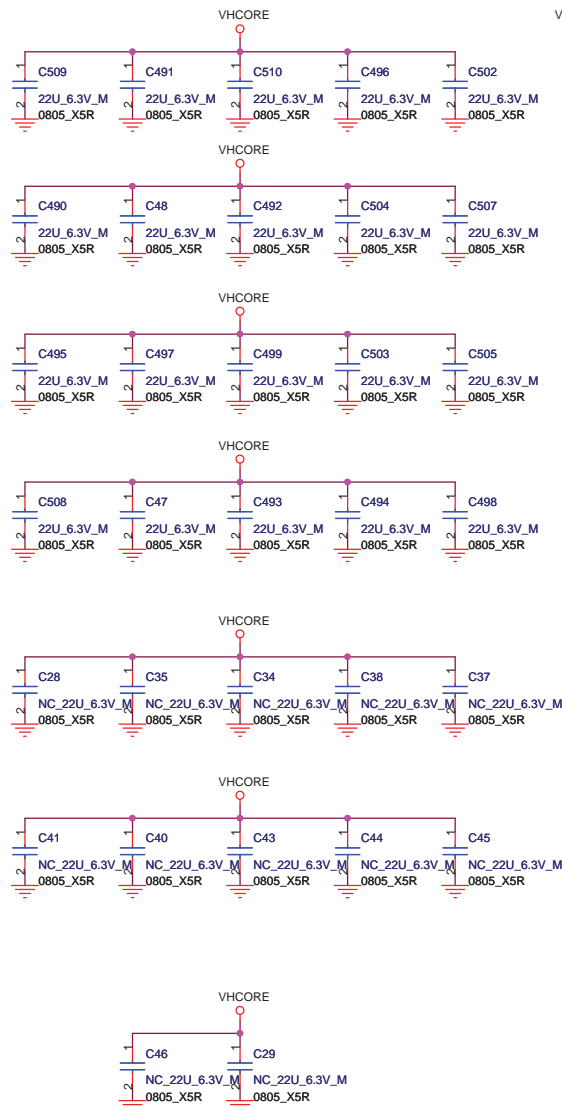
Place close to CPU

2K ohm for Dual-Core ;
1.74K ohm for Quad-Core

Route the TEST3 and TEST5 signals through a ground referenced $Z_o = 55$ -ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection. TEST4 and TEST6 and TEST7 pins can be left NC.

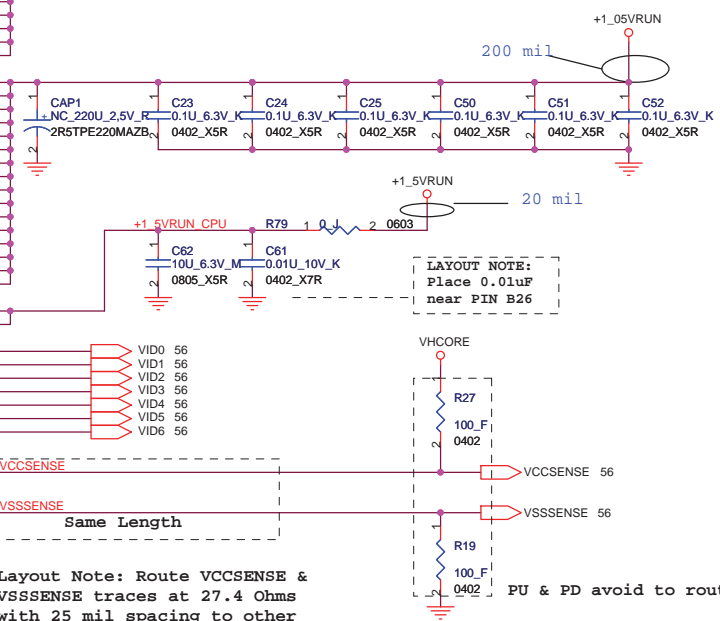
Layout Note:
 $Z_o = 55$ ohm, 0.5" max for GTLREF.

Layout Note:
Comp0,2 connect with $Z_o = 27.4$ ohm, make trace length shorter then 0.5". Width=20mil(MS)
Comp1,3 connect with $Z_o = 55$ ohm, make trace length shorter then 0.5". Width=5mil(MS)



Pin	Signal	Signal	Signal
A7	VCC[001]	AB20	VCC[068]
A9	VCC[002]	AB7	VCC[069]
A10	VCC[003]	AC7	VCC[070]
A12	VCC[004]	AC9	VCC[071]
A13	VCC[005]	AC12	VCC[072]
A15	VCC[006]	AC13	VCC[073]
A17	VCC[007]	AC15	VCC[074]
A18	VCC[008]	AC17	VCC[075]
A20	VCC[009]	AC18	VCC[076]
B7	VCC[010]	AD7	VCC[077]
B9	VCC[011]	AD9	VCC[078]
B10	VCC[012]	AD10	VCC[079]
B12	VCC[013]	AD12	VCC[080]
B14	VCC[014]	AD14	VCC[081]
B15	VCC[015]	AD15	VCC[082]
B17	VCC[016]	AD17	VCC[083]
B18	VCC[017]	AD18	VCC[084]
B20	VCC[018]	AE9	VCC[085]
C9	VCC[019]	AE10	VCC[086]
C10	VCC[020]	AE12	VCC[087]
C12	VCC[021]	AE13	VCC[088]
C13	VCC[022]	AE15	VCC[089]
C15	VCC[023]	AE17	VCC[090]
C17	VCC[024]	AE18	VCC[091]
C18	VCC[025]	AE20	VCC[092]
D8	VCC[026]	AF9	VCC[093]
D10	VCC[027]	AF10	VCC[094]
D12	VCC[028]	AF12	VCC[095]
D14	VCC[029]	AF14	VCC[096]
D15	VCC[030]	AF15	VCC[097]
D17	VCC[031]	AF17	VCC[098]
D18	VCC[032]	AF18	VCC[099]
E7	VCC[033]	AF20	VCC[100]
E9	VCC[034]		
E10	VCC[035]		
E12	VCC[036]		
E13	VCC[037]		
E15	VCC[038]		
E17	VCC[039]		
E18	VCC[040]		
E20	VCC[041]		
F7	VCC[042]		
F9	VCC[043]		
F10	VCC[044]		
F12	VCC[045]		
F14	VCC[046]		
F15	VCC[047]		
F17	VCC[048]		
F18	VCC[049]		
F20	VCC[050]		
AA7	VCC[051]		
AA9	VCC[052]		
AA10	VCC[053]		
AA12	VCC[054]		
AA13	VCC[055]		
AA15	VCC[056]		
AA17	VCC[057]		
AA18	VCC[058]		
AA20	VCC[059]		
AB9	VCC[060]		
AC10	VCC[061]		
AB10	VCC[062]		
AB12	VCC[063]		
AB14	VCC[064]		
AB15	VCC[065]		
AB17	VCC[066]		
AB18	VCC[067]		

CPU_VCCA---->0.13A
 CPU_VCCP---->4.5A
 CPU_VCC---->47A (design target)

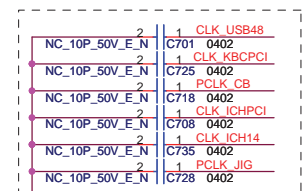
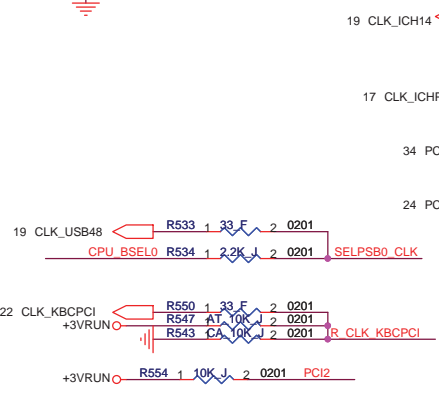
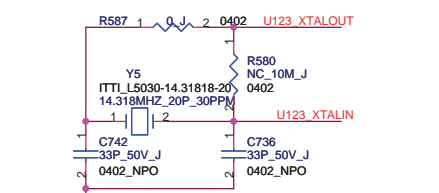
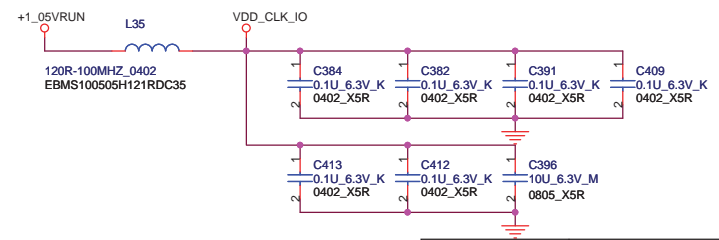
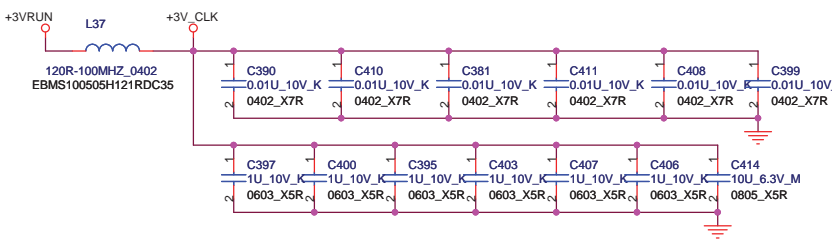


Layout Note: Route VCCSENSE & VSSSENSE traces at 27.4 Ohms with 25 mil spacing to other signals. Place PU and PD within 2 inch of CPU.

Outer width=20 mil spacing=7 mil
 Inner width=14 mil spacing=7 mil
 Length match < 25 mil

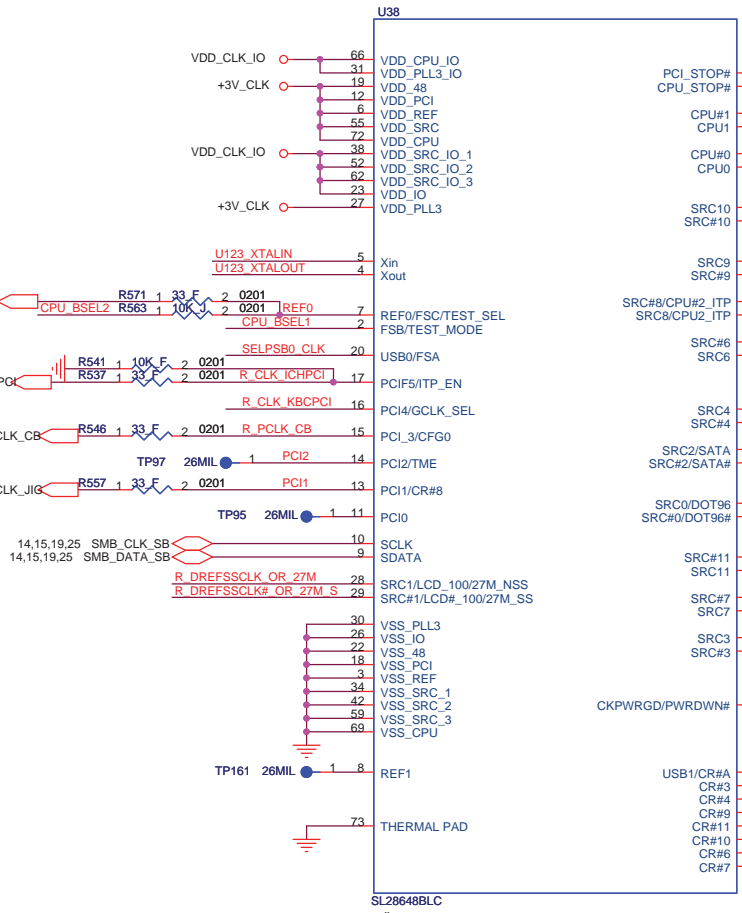
Pin	Signal	Signal	Signal
A4	VSS[001]	P6	VSS[082]
A8	VSS[002]	P21	VSS[083]
A11	VSS[003]	P24	VSS[084]
A14	VSS[004]	R2	VSS[085]
A16	VSS[005]	R5	VSS[086]
A19	VSS[006]	R22	VSS[087]
A23	VSS[007]	R25	VSS[088]
AF2	VSS[008]	T1	VSS[089]
B6	VSS[009]	T4	VSS[090]
B8	VSS[010]	T23	VSS[091]
B11	VSS[011]	T26	VSS[092]
B13	VSS[012]	U6	VSS[093]
B16	VSS[013]	U21	VSS[094]
B19	VSS[014]	U24	VSS[095]
B21	VSS[015]	V2	VSS[096]
B24	VSS[016]	V5	VSS[097]
C5	VSS[017]	V22	VSS[098]
C8	VSS[018]	V25	VSS[099]
C11	VSS[019]	W1	VSS[100]
C14	VSS[020]	W4	VSS[101]
C16	VSS[021]	W23	VSS[102]
C19	VSS[022]	W26	VSS[103]
C2	VSS[023]	Y3	VSS[104]
C22	VSS[024]	Y6	VSS[105]
C25	VSS[025]	Y21	VSS[106]
D4	VSS[026]	Y24	VSS[107]
D8	VSS[027]	AA2	VSS[108]
D9	VSS[028]	AA5	VSS[109]
D11	VSS[029]	AA8	VSS[110]
D13	VSS[030]	AA11	VSS[111]
D16	VSS[031]	AA14	VSS[112]
D19	VSS[032]	AA16	VSS[113]
D23	VSS[033]	AA19	VSS[114]
D26	VSS[034]	AA22	VSS[115]
E3	VSS[035]	AA25	VSS[116]
E6	VSS[036]	AB1	VSS[117]
E8	VSS[037]	AB4	VSS[118]
E11	VSS[038]	AB8	VSS[119]
E14	VSS[039]	AB11	VSS[120]
E16	VSS[040]	AB13	VSS[121]
E19	VSS[041]	AB16	VSS[122]
E21	VSS[042]	AB19	VSS[123]
E24	VSS[043]	AB23	VSS[124]
F5	VSS[044]	AB26	VSS[125]
F8	VSS[045]	AC3	VSS[126]
F11	VSS[046]	AC6	VSS[127]
F13	VSS[047]	AC8	VSS[128]
F16	VSS[048]	AC11	VSS[129]
F19	VSS[049]	AC14	VSS[130]
F2	VSS[050]	AC16	VSS[131]
F22	VSS[051]	AC19	VSS[132]
F25	VSS[052]	AC21	VSS[133]
G4	VSS[053]	AC24	VSS[134]
D19	VSS[054]	AD2	VSS[135]
G23	VSS[055]	AD5	VSS[136]
G26	VSS[056]	AD8	VSS[137]
H3	VSS[057]	AD11	VSS[138]
H6	VSS[058]	AD13	VSS[139]
H21	VSS[059]	AD16	VSS[140]
H24	VSS[060]	AD19	VSS[141]
J2	VSS[061]	AD22	VSS[142]
J5	VSS[062]	AD25	VSS[143]
J22	VSS[063]	AE1	VSS[144]
J25	VSS[064]	AE4	VSS[145]
K4	VSS[065]	AE8	VSS[146]
K11	VSS[066]	AE11	VSS[147]
K23	VSS[067]	AE14	VSS[148]
K26	VSS[068]	AE16	VSS[149]
L3	VSS[069]	AE19	VSS[150]
L6	VSS[070]	AE23	VSS[151]
L21	VSS[071]	AE26	VSS[152]
L24	VSS[072]	A2	VSS[153]
M2	VSS[073]	AF6	VSS[154]
M5	VSS[074]	AF8	VSS[155]
M22	VSS[075]	AF11	VSS[156]
M25	VSS[076]	AF13	VSS[157]
N1	VSS[077]	AF16	VSS[158]
N4	VSS[078]	AF19	VSS[159]
N23	VSS[079]	AF21	VSS[160]
N26	VSS[080]	A25	VSS[161]
P3	VSS[081]	AF25	VSS[162]
			VSS[163]

CPU SOCKET_478P
 FOX_PZ4782A-274M-01



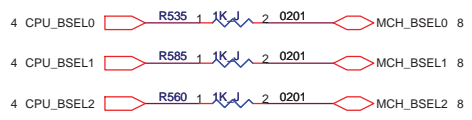
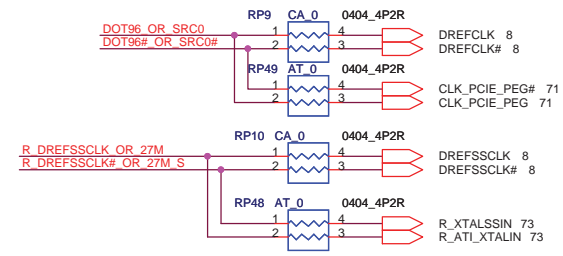
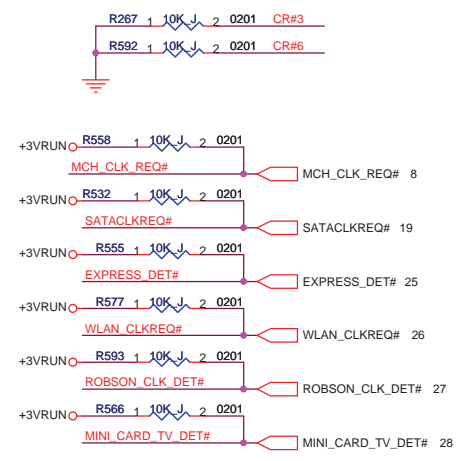
FSB Frequency Table:

FSLC	FSLB	FSLA	CPU	SRC	PCI
0	0	0	266.66	100	33
0	0	1	133.33	100	33
0	1	0	200	100	33
0	1	1	166.66	100	33
1	0	0	333.33	100	33
1	0	1	100	100	33
1	1	0	400	100	33



SMBUS Address:D2H

Clock Request	Clock Request Function
CR#3	CLK_PCIE_ICH#
CR#4	EXPRESS_DET#
CR#6	CLK_PCIE_LAN#
CR#7	ROBSON_CLK_DET#
CR#9	MCH_CLK_REQ#
CR#10	WLAN_CLKREQ#
CR#11	MINI_CARD_TV_DET#
CR#A	SATACLKREQ#



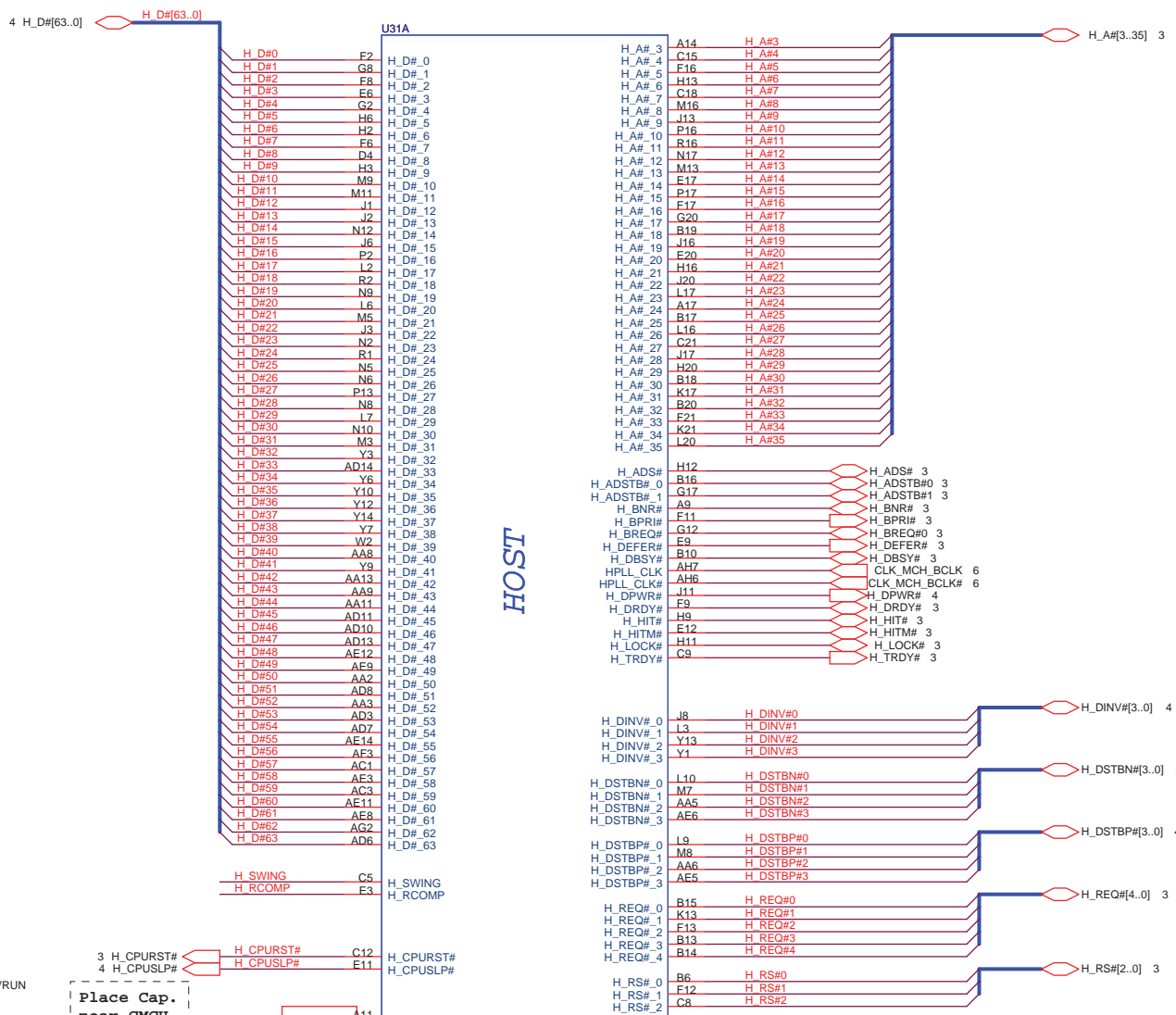
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Title: **CLOCK GEN**

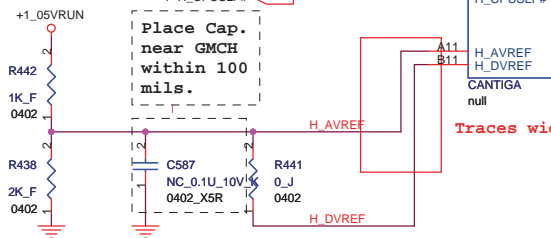
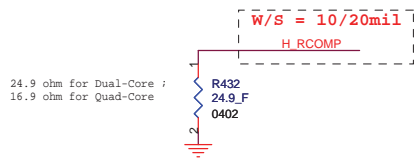
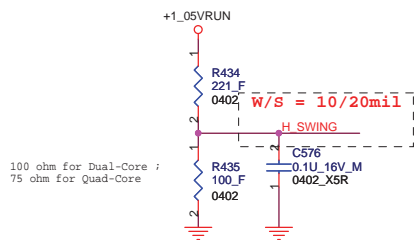
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HOST

Traces width 10 mils.



MCH_CFG_0-2 FSB Frequency	000 = FSB1066 ; 010 = FSB800; 011 = FSB667 ; Others = Reserved
MCH_CFG_3-4	Reserved
MCH_CFG_5 DMI X2 Select	Low = DMI X2 High = DMI X4 (Default)
MCH_CFG_6 ITPM Host Interface	Low =The ITPM Host Interface is enabled2 High = The ITPM Host Interface is disabled (default)
MCH_CFG_7 Intel Management Engine Crypto Strap	Low = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel Management Engine Crypto TLS cipher suite with confidentiality (default)
MCH_CFG_8	Reserved
MCH_CFG_9 PCIe Graphics Lane	Low = Reverse Lane High = Normal operation
MCH_CFG_10 PCIe Loopback enable	Low = Enabled3 High = Disabled (default)
MCH_CFG_11	Reserved
MCH_CFG_12 ALLZ	Low = ALLZ mode enabled3 High = Disabled (default)
MCH_CFG_13 XOR	Low = XOR mode enabled3 High = Disabled (default)
MCH_CFG_14-15	Reserved
MCH_CFG_16 FSB Dynamic ODT	Low = Dynamic ODT disabled High = Dynamic ODT enabled (default)
MCH_CFG_17-18	Reserved
MCH_CFG_19 DMI Lane Reversal	Low = Normal operation (Default): Lane Numbered in Order High = Reverse Lanes DMI x4 mode [(G)MCH->ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [(G)MCH->ICH]: (3->0, 2->1)
MCH_CFG_20 Digital Display Port (SDVO/DP/iHDMI) or Concurrent with PCIe	Low = Only digital display port (SDVO/DP/iHDMI) or PCIe is operational (default) High = Digital display port (SDVO/DP/iHDMI) and PCIe are operating simultaneously via the PEG port

U31B

- X M36 RSVD1
- X N36 RSVD2
- X R33 RSVD3
- X T33 RSVD4
- X AH9 RSVD5
- X AH10 RSVD6
- X AH12 RSVD7
- X AH13 RSVD8
- X K12 RSVD9
- X AL34 RSVD10
- X AK34 RSVD11
- X AN35 RSVD12
- X AM35 RSVD13
- X T24 RSVD14
- X B31 RSVD15
- X B2 RSVD16
- X M1 RSVD17
- X Y21 RSVD20
- X G23 RSVD22
- X BF23 RSVD23
- X BH18 RSVD24
- X BF18 RSVD25

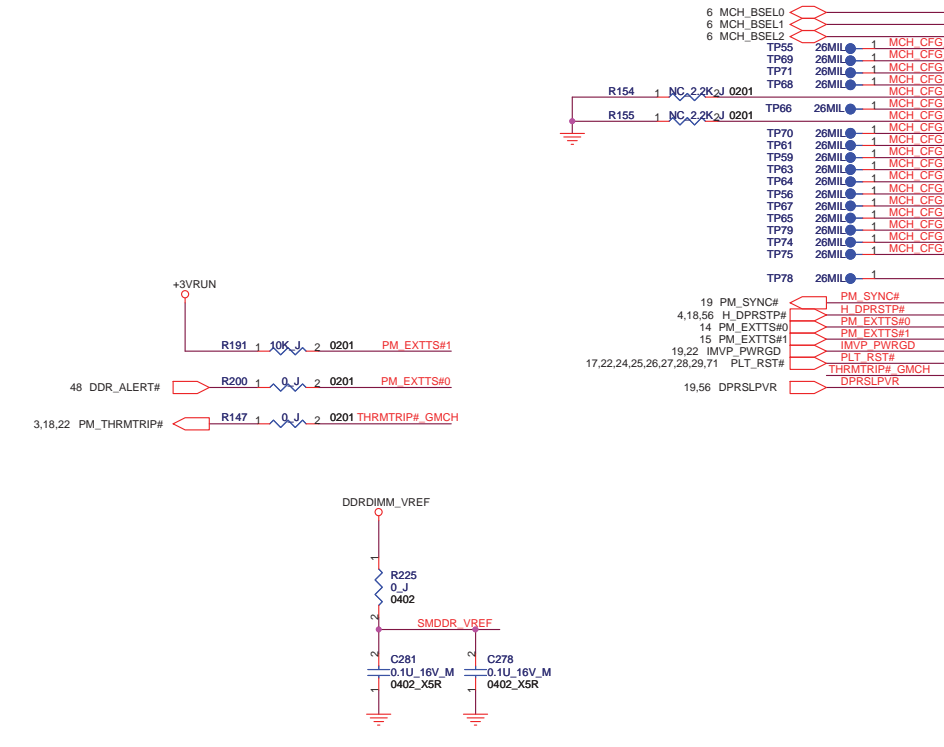
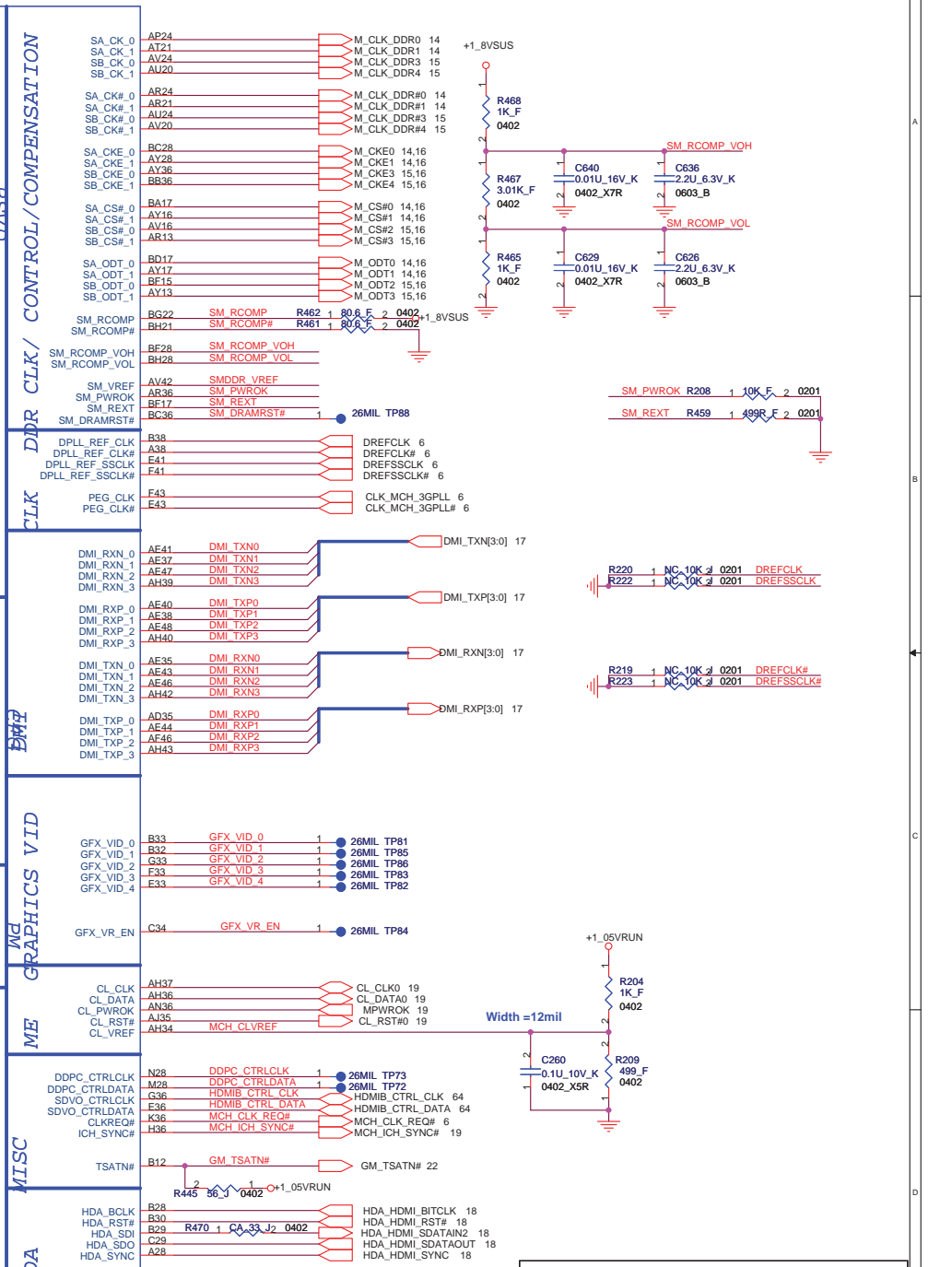
- X G23 RSVD22
- X BF23 RSVD23
- X BH18 RSVD24
- X BF18 RSVD25

- T25 CFG_0
- R25 CFG_1
- P25 CFG_2
- P20 CFG_3
- P24 CFG_4
- C25 CFG_5
- N24 CFG_6
- M24 CFG_7
- E21 CFG_8
- C23 CFG_9
- N21 CFG_10
- P21 CFG_11
- T21 CFG_12
- R20 CFG_13
- L21 CFG_14
- M20 CFG_15
- L21 CFG_16
- P29 CFG_17
- R28 CFG_18
- R28 CFG_19
- T28 CFG_20

- R29 PM_SYNC#
- B7 H_DPRSTP#
- N33 PM_EXTSTS#0
- P32 PM_EXTSTS#1
- AT40 IMVP_PWRGD
- AT11 PLT_RST#
- R32 THRMTRIP#_GMCH
- R32 DPRSLPVR

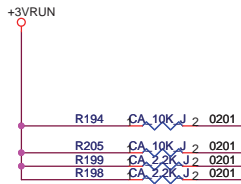
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- NC_2
- NC_3
- NC_4
- NC_5
- NC_6
- NC_7
- NC_8
- NC_9
- NC_10
- NC_11
- NC_12
- NC_13
- NC_14
- NC_15
- NC_16
- NC_17
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- NC_25
- NC_26

CANTIGA
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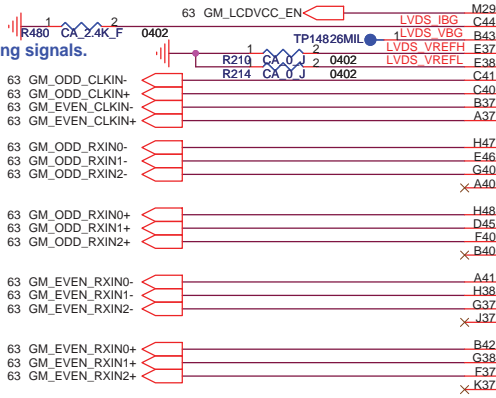


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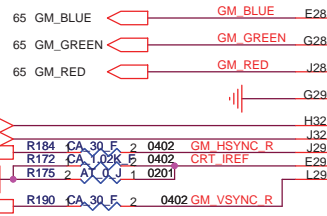
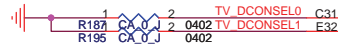
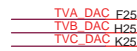
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Title Cantiga (DMI) 2/7			
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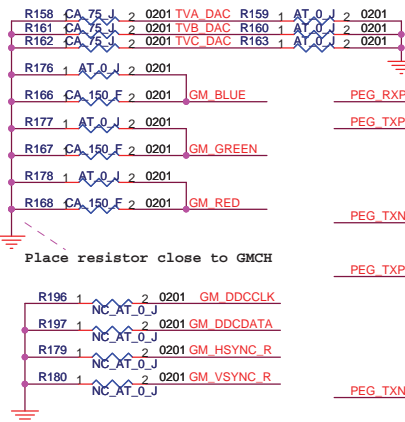
20 mils away from toggling signals.



If CRT/TV-OUT Disable
Please change R158,R161,R162 from 75R to 0R



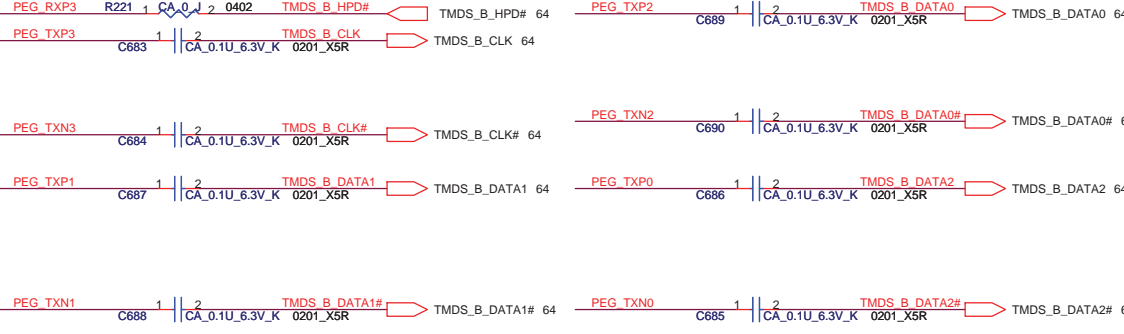
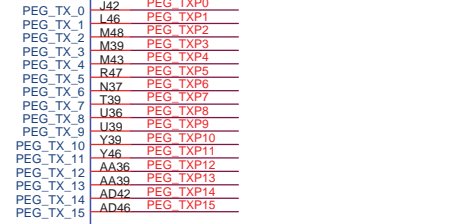
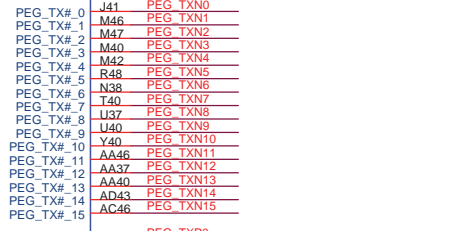
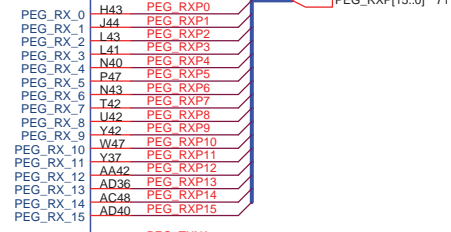
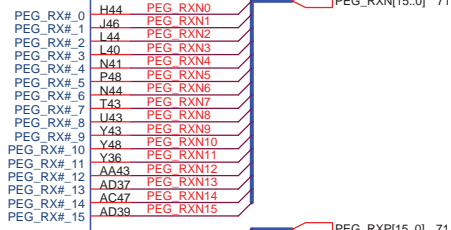
30 mils away from toggling signals.



Place resistor close to GMCH



PCI - EXPRESS GRAPHICS



14 M_A_DQ[63..0]

M A DQ0	AJ38
M A DQ1	AJ41
M A DQ2	AN38
M A DQ3	AM38
M A DQ4	AJ36
M A DQ5	AJ40
M A DQ6	AM44
M A DQ7	AM42
M A DQ8	AN43
M A DQ9	AN44
M A DQ10	AU40
M A DQ11	AT38
M A DQ12	AN41
M A DQ13	AN39
M A DQ14	AU44
M A DQ15	AU42
M A DQ16	AV39
M A DQ17	AY44
M A DQ18	BA40
M A DQ19	BD43
M A DQ20	AV41
M A DQ21	AY43
M A DQ22	BB41
M A DQ23	BC40
M A DQ24	AY37
M A DQ25	BD38
M A DQ26	AV37
M A DQ27	AT36
M A DQ28	AY38
M A DQ29	BB38
M A DQ30	AV36
M A DQ31	AW36
M A DQ32	BD13
M A DQ33	AU11
M A DQ34	BC11
M A DQ35	BA12
M A DQ36	AU13
M A DQ37	AV13
M A DQ38	BD12
M A DQ39	BC12
M A DQ40	BD9
M A DQ41	BA9
M A DQ42	AU10
M A DQ43	AV9
M A DQ44	BA11
M A DQ45	BD9
M A DQ46	AY8
M A DQ47	BA6
M A DQ48	AV5
M A DQ49	AV7
M A DQ50	AT9
M A DQ51	AN8
M A DQ52	AU5
M A DQ53	AU6
M A DQ54	AT5
M A DQ55	AN10
M A DQ56	AM11
M A DQ57	AM5
M A DQ58	AJ9
M A DQ59	AJ8
M A DQ60	AM12
M A DQ61	AM13
M A DQ62	AJ11
M A DQ63	AJ12

DDR SYSTEM MEMORY A

SA_BS_0	BD21	M_A_BS0	14,16
SA_BS_1	BG18	M_A_BS1	14,16
SA_BS_2	AT25	M_A_BS2	14,16
SA_RAS#	BB20	M_A_RAS#	14,16
SA_CAS#	BD20	M_A_CAS#	14,16
SA_WE#	AY20	M_A_WE#	14,16
SA_DM_0	AM37	M_A_DM0	14
SA_DM_1	AT41	M_A_DM1	
SA_DM_2	AY41	M_A_DM2	
SA_DM_3	AU39	M_A_DM3	
SA_DM_4	BB12	M_A_DM4	
SA_DM_5	AY6	M_A_DM5	
SA_DM_6	AT7	M_A_DM6	
SA_DM_7	AJ5	M_A_DM7	
SA_DQS_0	AJ44	M_A_DQS0	14
SA_DQS_1	AT44	M_A_DQS1	
SA_DQS_2	BA43	M_A_DQS2	
SA_DQS_3	BC37	M_A_DQS3	
SA_DQS_4	AW12	M_A_DQS4	
SA_DQS_5	BC8	M_A_DQS5	
SA_DQS_6	AU8	M_A_DQS6	
SA_DQS_7	AM7	M_A_DQS7	
SA_DQS#_0	AJ43	M_A_DQS#0	14
SA_DQS#_1	AT43	M_A_DQS#1	
SA_DQS#_2	BA44	M_A_DQS#2	
SA_DQS#_3	BD37	M_A_DQS#3	
SA_DQS#_4	AY12	M_A_DQS#4	
SA_DQS#_5	BD8	M_A_DQS#5	
SA_DQS#_6	AU9	M_A_DQS#6	
SA_DQS#_7	AM8	M_A_DQS#7	
SA_MA_0	BA21	M_A_A0	14,16
SA_MA_1	BC24	M_A_A1	
SA_MA_2	BG24	M_A_A2	
SA_MA_3	BH24	M_A_A3	
SA_MA_4	BG25	M_A_A4	
SA_MA_5	BA24	M_A_A5	
SA_MA_6	BD24	M_A_A6	
SA_MA_7	BG27	M_A_A7	
SA_MA_8	BF25	M_A_A8	
SA_MA_9	AW24	M_A_A9	
SA_MA_10	BC21	M_A_A10	
SA_MA_11	BH26	M_A_A11	
SA_MA_12	BH17	M_A_A12	
SA_MA_13	AY25	M_A_A13	
SA_MA_14	AY25	M_A_A14	

CANTIGA null

15 M_B_DQ[63..0]

M B DQ0	AK47
M B DQ1	AH46
M B DQ2	AP47
M B DQ3	AP46
M B DQ4	AJ46
M B DQ5	AJ48
M B DQ6	AM48
M B DQ7	AP48
M B DQ8	AU47
M B DQ9	AU46
M B DQ10	BA48
M B DQ11	AY48
M B DQ12	AT47
M B DQ13	AR47
M B DQ14	BA47
M B DQ15	BC47
M B DQ16	BC46
M B DQ17	BC44
M B DQ18	BF43
M B DQ19	BF43
M B DQ20	BE45
M B DQ21	BC41
M B DQ22	BF41
M B DQ23	BC38
M B DQ24	BF38
M B DQ25	BF38
M B DQ26	BH35
M B DQ27	BG35
M B DQ28	BH40
M B DQ29	BG39
M B DQ30	BG34
M B DQ31	BH34
M B DQ32	BH14
M B DQ33	BG12
M B DQ34	BH11
M B DQ35	BG8
M B DQ36	BH12
M B DQ37	BF11
M B DQ38	BF8
M B DQ39	BG7
M B DQ40	BC5
M B DQ41	BC5
M B DQ42	AY3
M B DQ43	AY1
M B DQ44	BF6
M B DQ45	BF5
M B DQ46	BA1
M B DQ47	BD3
M B DQ48	AV2
M B DQ49	AU3
M B DQ50	AR3
M B DQ51	AN2
M B DQ52	AV1
M B DQ53	AV1
M B DQ54	AP3
M B DQ55	AR1
M B DQ56	AL1
M B DQ57	AL2
M B DQ58	AJ1
M B DQ59	AH1
M B DQ60	AM2
M B DQ61	AM3
M B DQ62	AH3
M B DQ63	AJ3

DDR SYSTEM MEMORY B

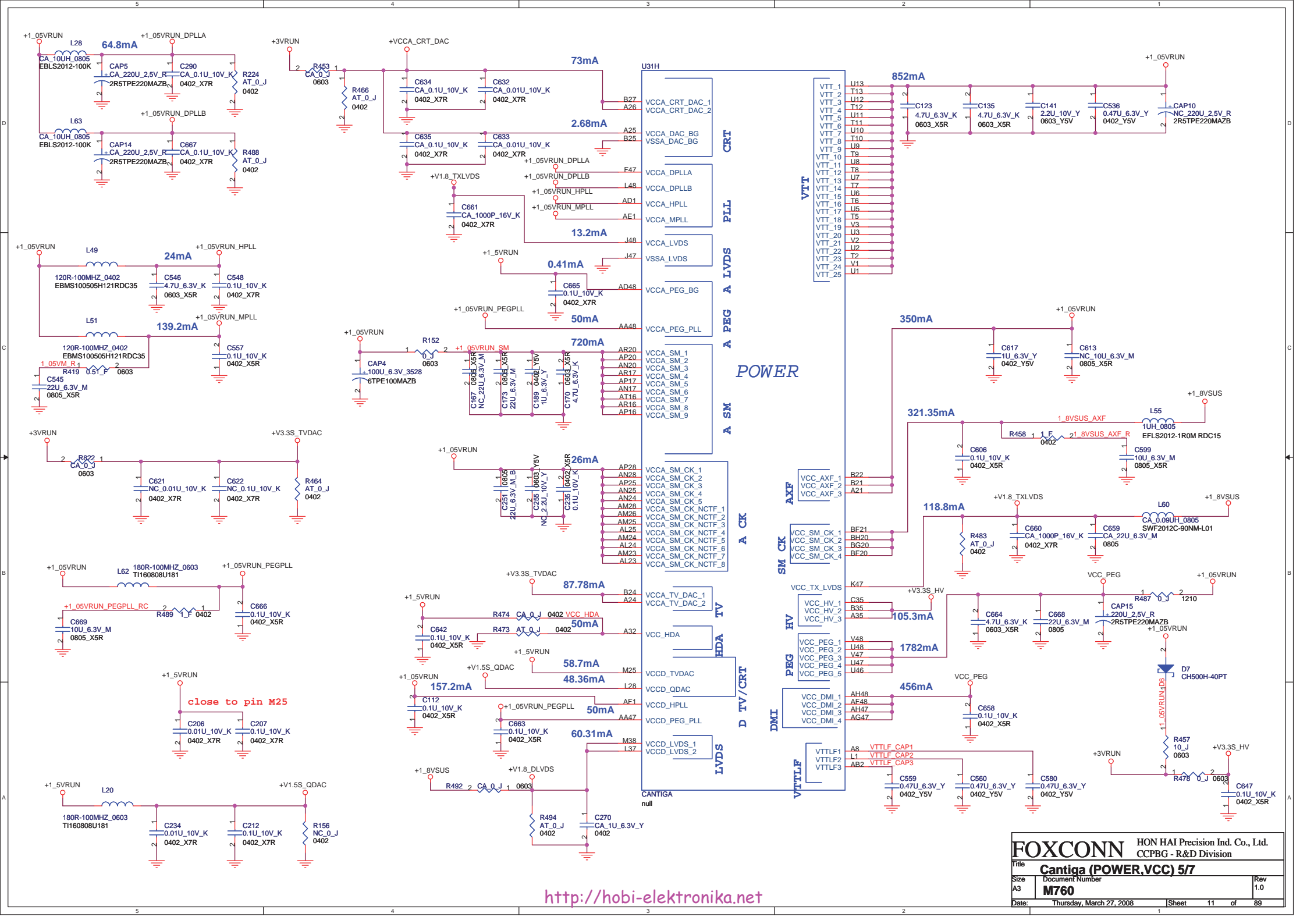
SB_DS_0	BC16	M_B_BS0	15,16
SB_DS_1	BB17	M_B_BS1	15,16
SB_DS_2	BB33	M_B_BS2	15,16
SB_RAS#	AU17	M_B_RAS#	15,16
SB_CAS#	BG16	M_B_CAS#	15,16
SB_WE#	BF14	M_B_WE#	15,16
SB_DM_0	AM47	M_B_DM0	15
SB_DM_1	AY47	M_B_DM1	
SB_DM_2	BD40	M_B_DM2	
SB_DM_3	BF35	M_B_DM3	
SB_DM_4	BG11	M_B_DM4	
SB_DM_5	BA3	M_B_DM5	
SB_DM_6	AP1	M_B_DM6	
SB_DM_7	AK2	M_B_DM7	
SB_DQS_0	AL47	M_B_DQS0	15
SB_DQS_1	AV48	M_B_DQS1	
SB_DQS_2	BG41	M_B_DQS2	
SB_DQS_3	BG37	M_B_DQS3	
SB_DQS_4	BH9	M_B_DQS4	
SB_DQS_5	BB2	M_B_DQS5	
SB_DQS_6	AU11	M_B_DQS6	
SB_DQS_7	AN6	M_B_DQS7	
SB_DQS#_0	AL46	M_B_DQS#0	15
SB_DQS#_1	AV47	M_B_DQS#1	
SB_DQS#_2	BH41	M_B_DQS#2	
SB_DQS#_3	BH37	M_B_DQS#3	
SB_DQS#_4	BG9	M_B_DQS#4	
SB_DQS#_5	AT2	M_B_DQS#5	
SB_DQS#_6	AN5	M_B_DQS#6	
SB_DQS#_7	AN5	M_B_DQS#7	
SB_MA_0	AV17	M_B_A0	15,16
SB_MA_1	BA25	M_B_A1	
SB_MA_2	BC25	M_B_A2	
SB_MA_3	AU25	M_B_A3	
SB_MA_4	AW25	M_B_A4	
SB_MA_5	BB28	M_B_A5	
SB_MA_6	AU28	M_B_A6	
SB_MA_7	AW28	M_B_A7	
SB_MA_8	AT33	M_B_A8	
SB_MA_9	BD33	M_B_A9	
SB_MA_10	BB16	M_B_A10	
SB_MA_11	AW33	M_B_A11	
SB_MA_12	AY33	M_B_A12	
SB_MA_13	BH15	M_B_A13	
SB_MA_14	AU33	M_B_A14	

CANTIGA null

FOXCONN HON HAI Precision Ind. Co., Ltd.
 CCPBG - R&D Division

Title: **Cantiga (DDRII) 4/7**

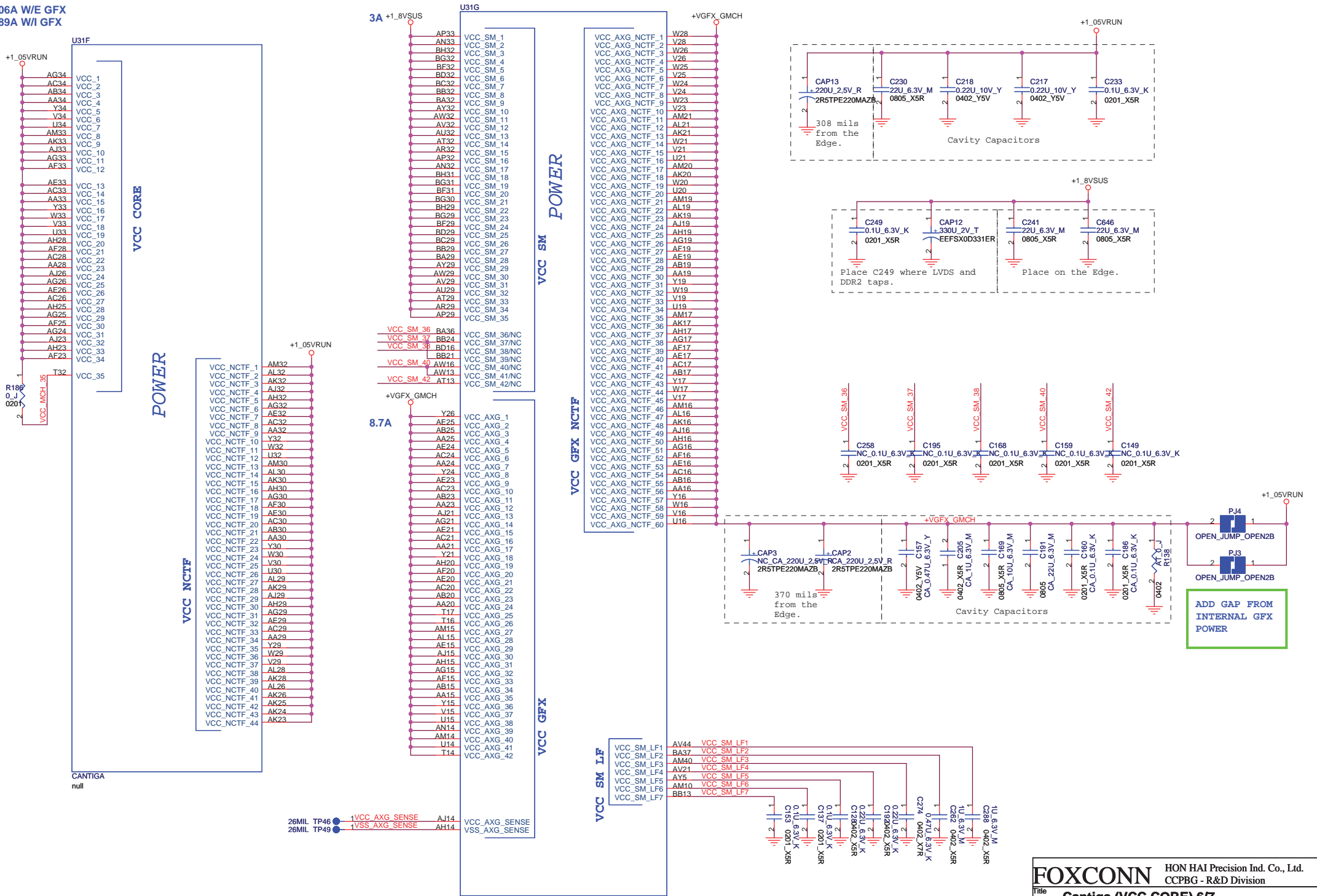
Size A3	Document Number M760	Rev 1.0
Date: Thursday, March 27, 2008	Sheet 10 of 89	



<http://hobi-elektronika.net>

FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: Cantiga (POWER,VCC) 5/7			
Size	Document Number		Rev
A3	M760		1.0
Date:	Thursday, March 27, 2008	Sheet	11 of 89

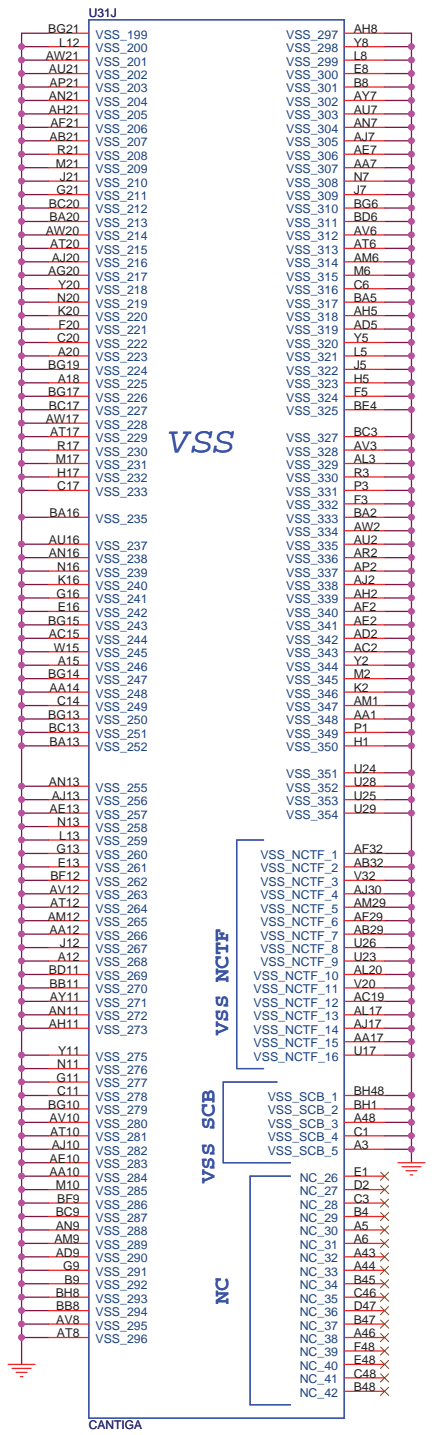
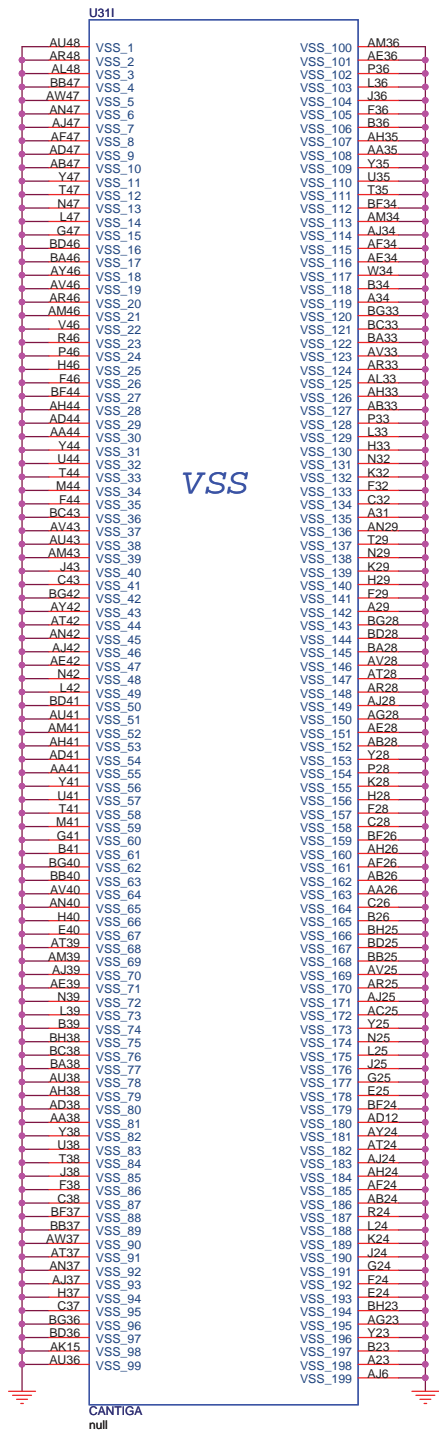
3.06A W/E GFX
2.89A W/I GFX



26MIL TP46 1VCC AXG SENSE AH14
26MIL TP49 1VSS AXG SENSE AH14

<http://hobi-elektronika.net>

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Title: Cantiga (VCC CORE) 6/7			
Size: A3	Document Number: M760	Date: Thursday, March 27, 2008	Rev: 1.0
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VSS

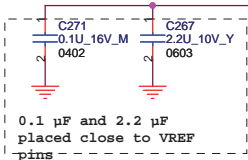
VSS

VSS NCTF

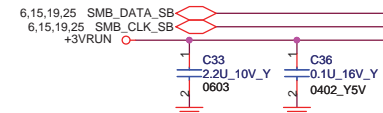
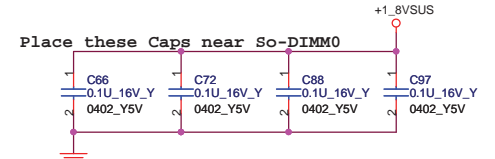
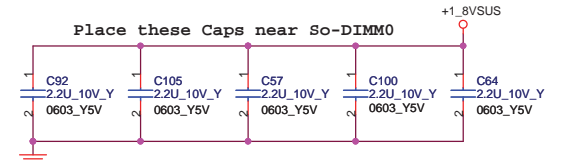
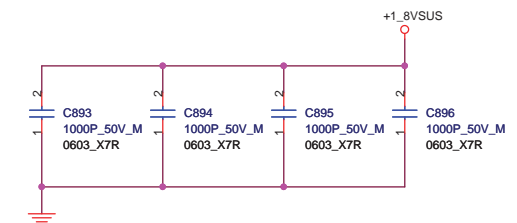
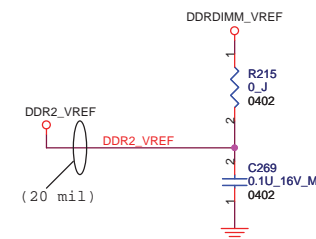
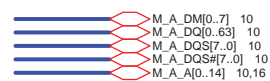
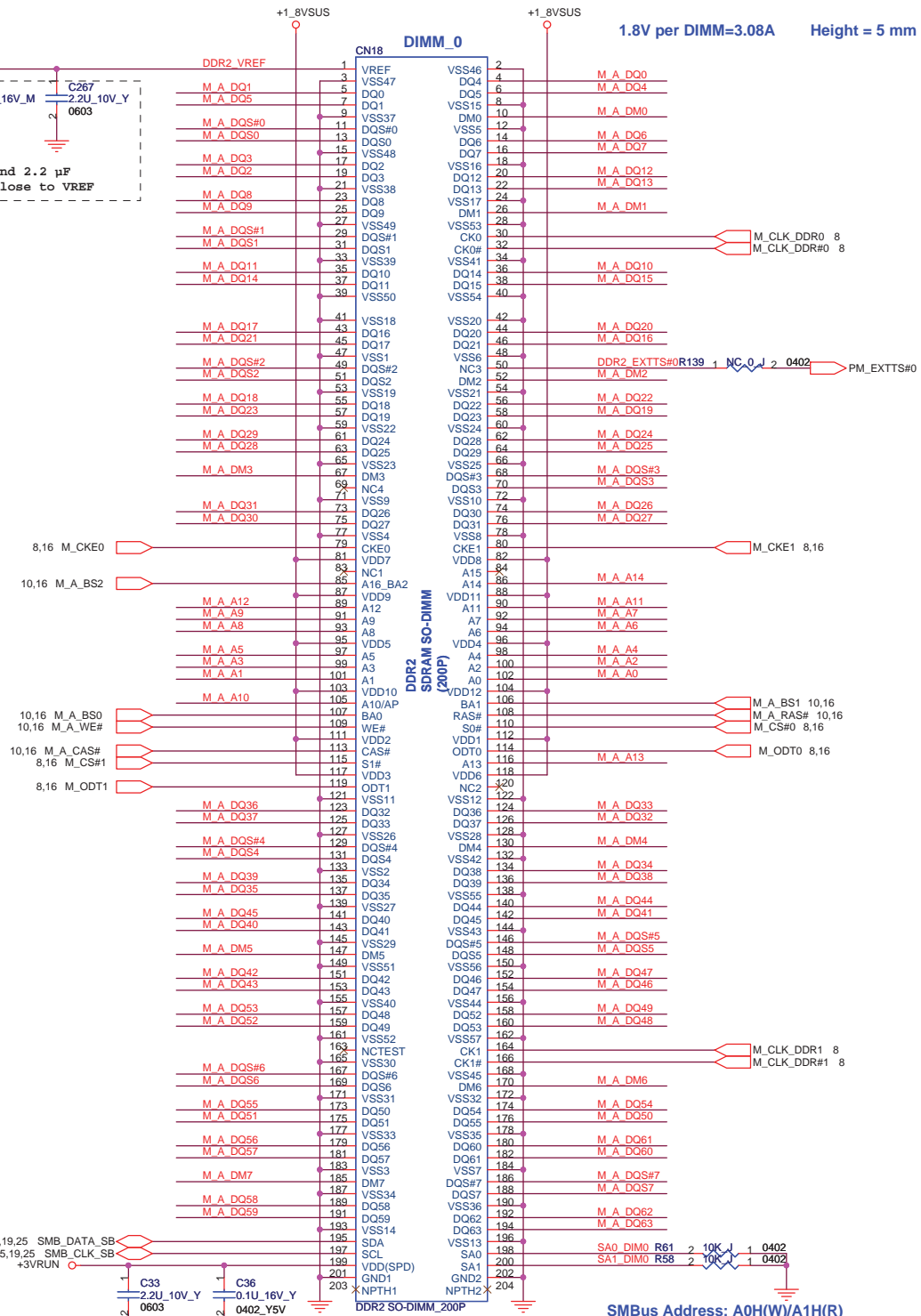
VSS SCB

NC

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title	Cantiga (VSS) 777		
Size	Document Number	Rev	
A3	M760	1.0	
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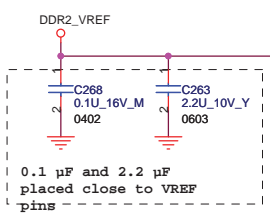
0.1 uF and 2.2 uF placed close to VREF pins



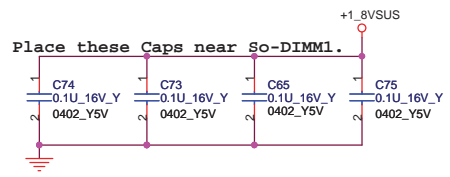
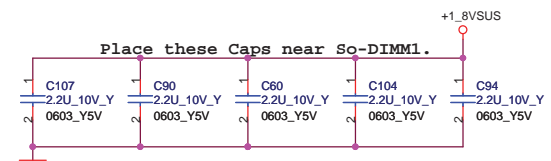
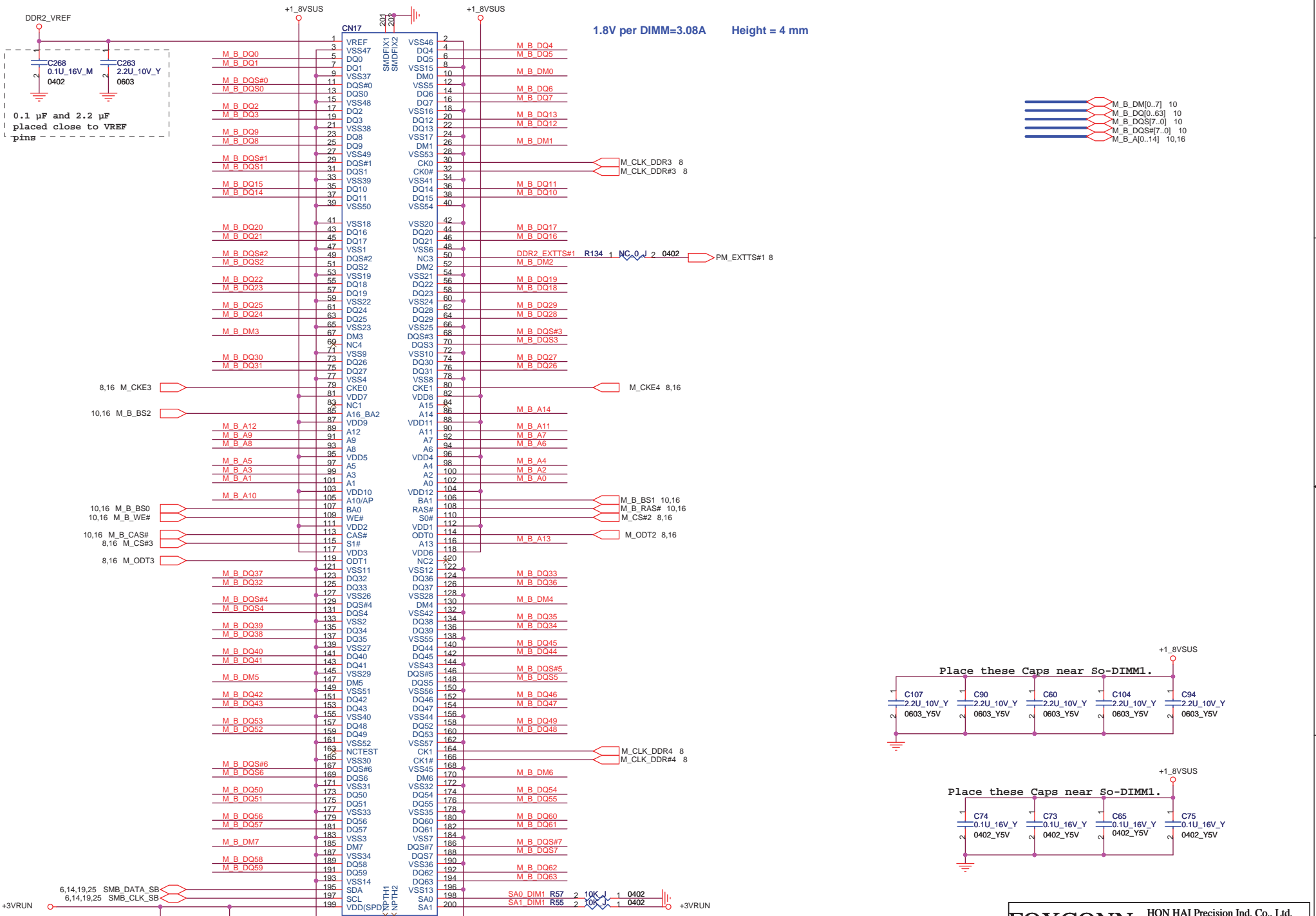
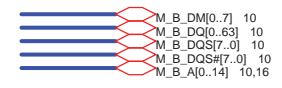
SMBus Address: A0H(W)/A1H(R)

<http://www.chipshack.com>

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title: DDR(II)SO-DIMM_0			
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1.8V per DIMM=3.08A Height = 4 mm

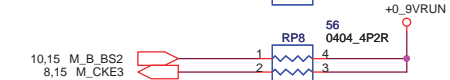
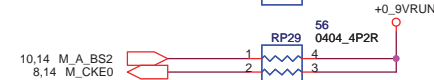
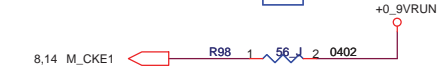
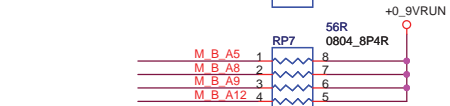
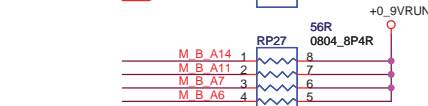
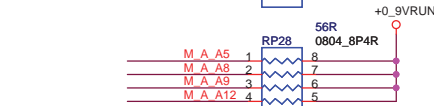
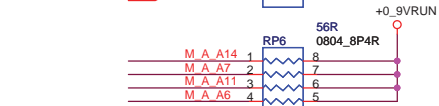
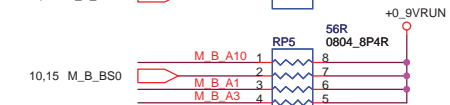
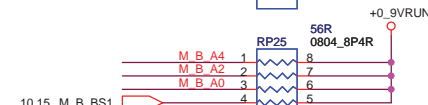
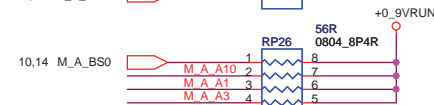
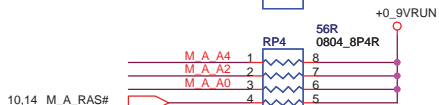
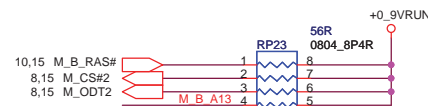
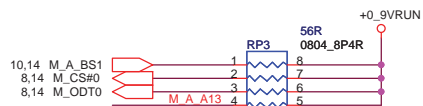
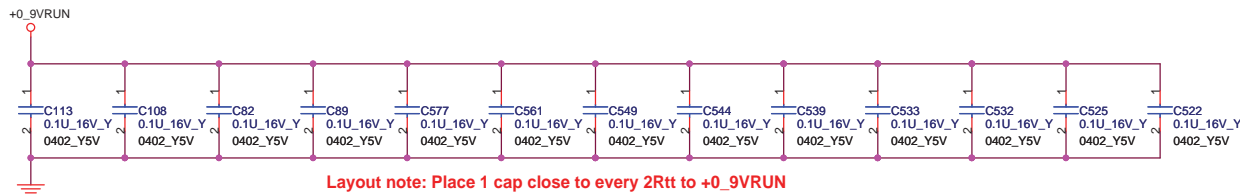
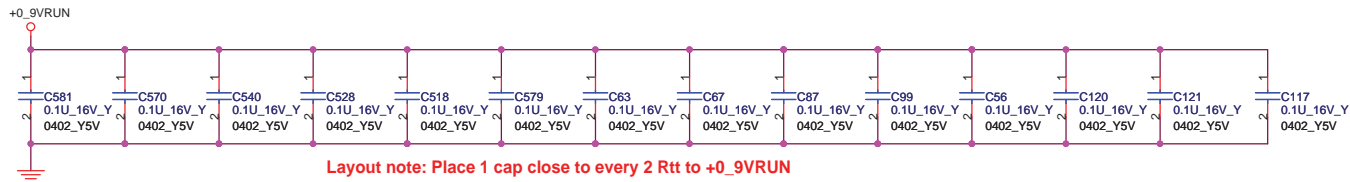


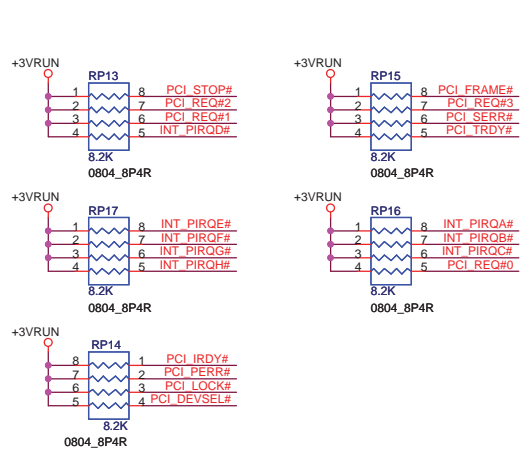
203 XDP1H1
204 XNPTH2
DIMM_1
DDR2_200P
FOX_AS0A426-N6SN-7F

SMBus Address: A4(W)/A5(R)

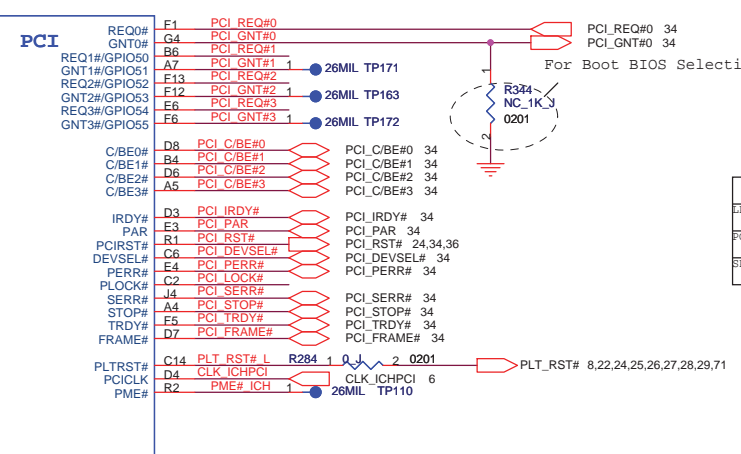
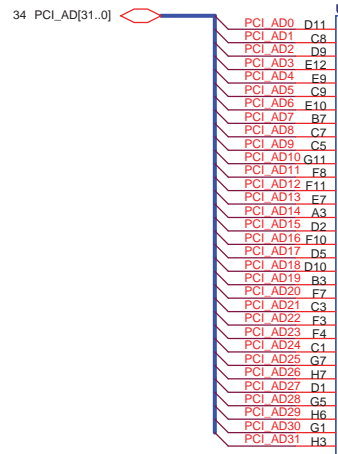
DIMM_1 is placed here from the DIMM pin list

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title DDR(II)SO-DIMM_1			
Size	Document Number		Rev
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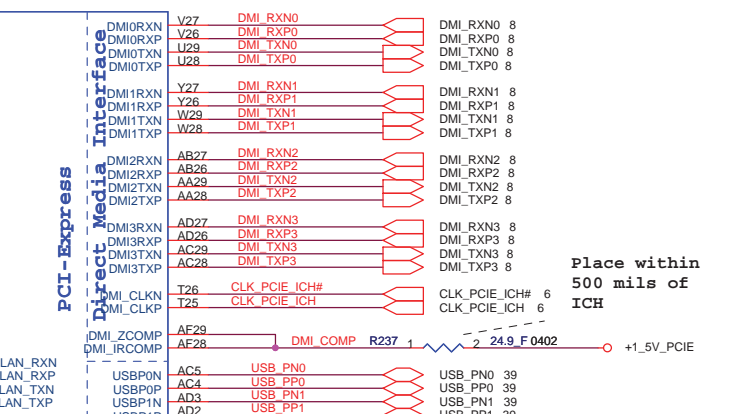
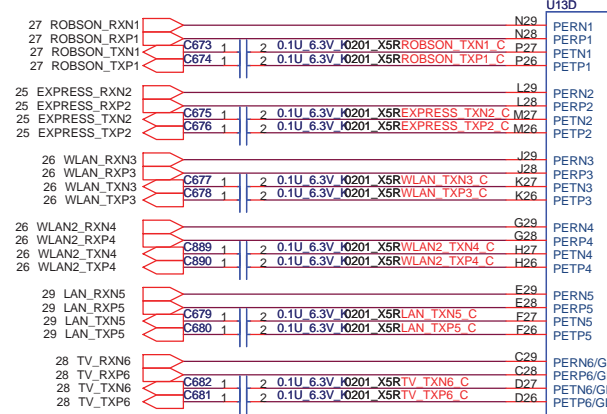


PCI Pullups

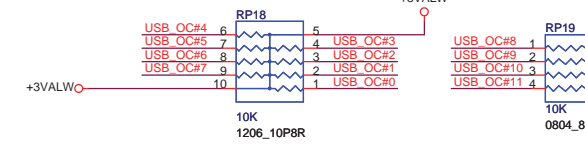
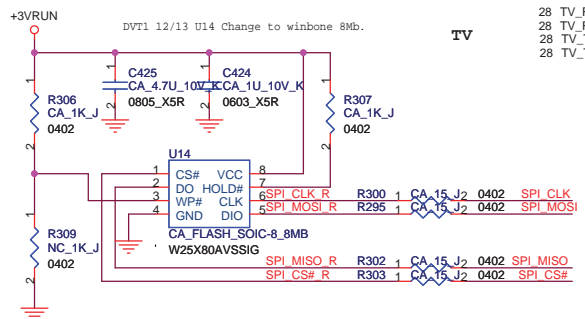


Strap for Boot-BIOS

	GNT#0	SPI_CS1#
IPC(Default)	HI	HI
PCI	HI	LOW
SPI	LOW	HI



USB PORT	Function
PORT-0	SIDE-1
PORT-1	SIDE-2
PORT-2	SIDE-3
PORT-3	EXPRESS CARD
PORT-4	Bluetooth
PORT-5	PATA ODD Bridge
PORT-6	Wireless LAN2
PORT-7	Camera
PORT-8	Felica
PORT-9	CIR
PORT-10	Wireless LAN
PORT-11	



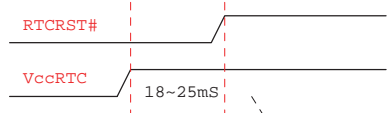
Place within 500 mils of ICH and don't routing next to high speed signals

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: **ICH9-M (PCI/USB) 1/5**

Size A3	Document Number M760	Rev 1.0
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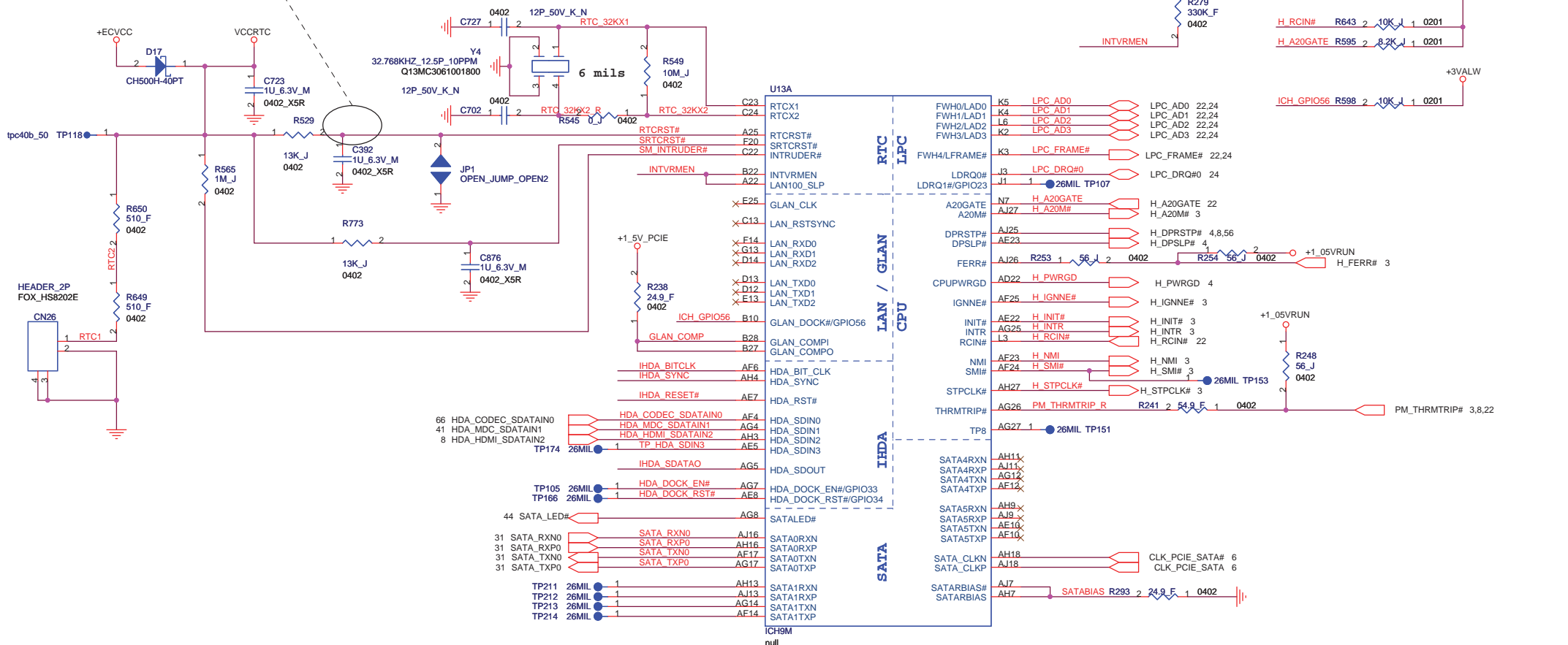
Date: Thursday, March 27, 2008 Sheet 17 of 89



The traces inside this block should be wider.

Internal VRM enabled for VccSua1_05, VccSua1_5, VccCL1_5, VccLAN1_05 and VccCL1_05

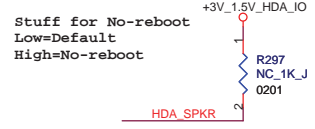
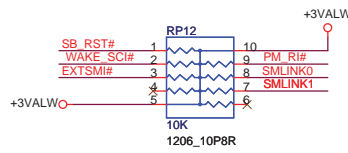
INTVRMEN	Low= Internal VR Disabled High= Internal VR Enabled(Default)
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FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: **ICH9-M (LPC,IDE,SATA) 2/5**

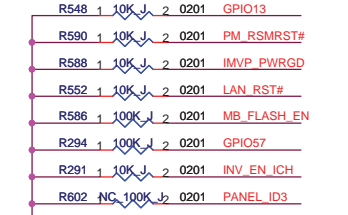
Size A3	Document Number M760	Rev 1.0
Date: Thursday, March 27, 2008	Sheet 18 of 89	



SW1: DISPLAY OUTOUT SELECTION (FOR DEBUG ONLY)

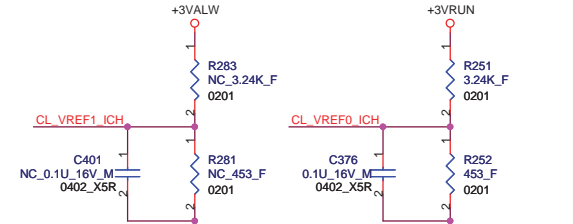
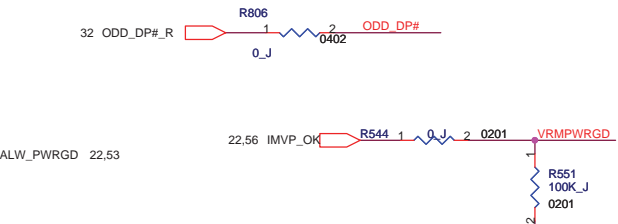
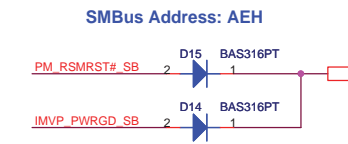
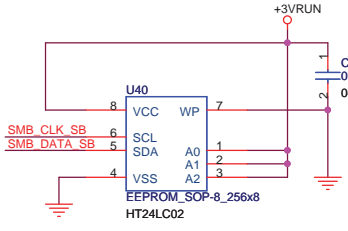
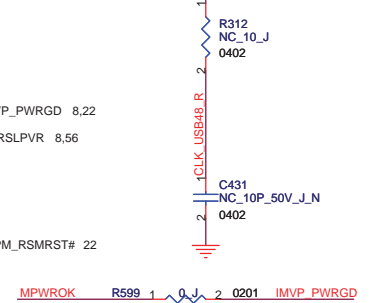
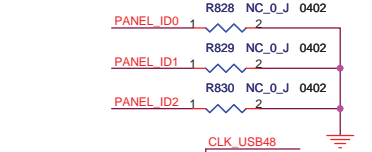
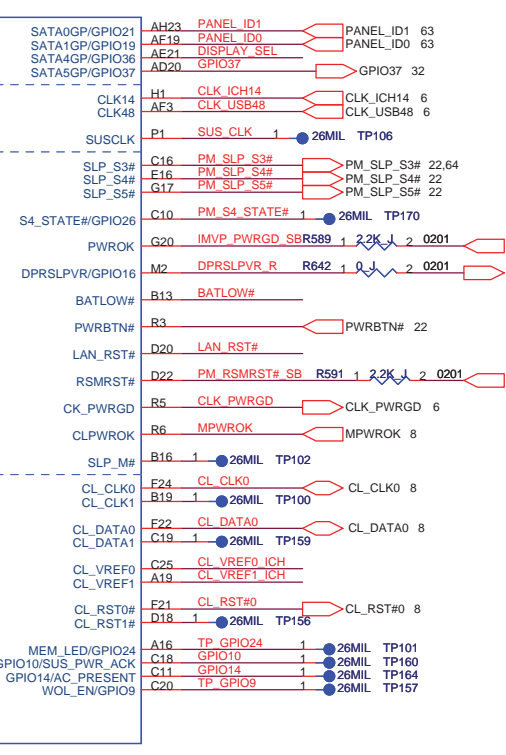
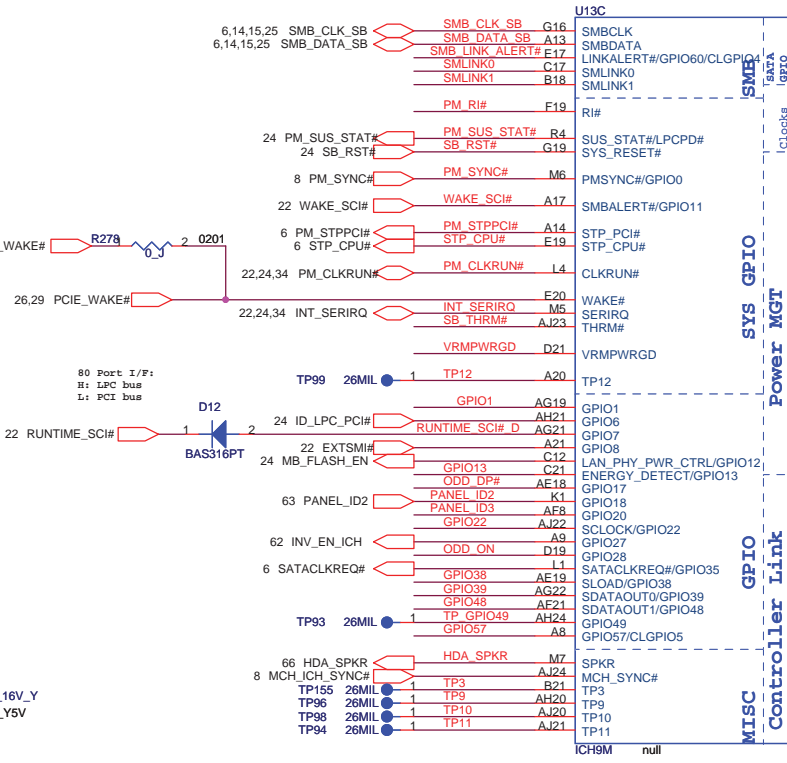
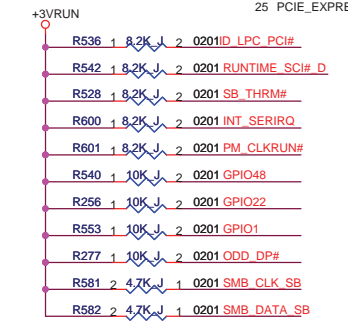
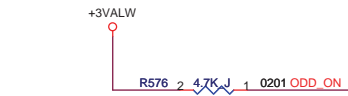
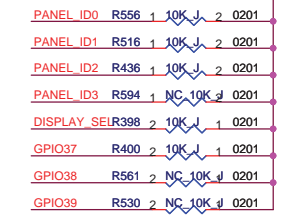
DISPLAY_SEL	
0	CRT
1	LVDS

EVT2 11/2 The LVDS cable contain the IDs. +3VRUN



PANEL ID

Type	---	---	---	WXGA (EVT Only)
Size	---	---	---	15.4W
Vender	Sharp	Sharp	Sharp	LPL
Device Name	Eastwood1	Eastwood2	Eastwood3	LP154WX4 TLC5
Panel ID [3..0]	0 0 1	0 1 0	0 1 1	0 0 0

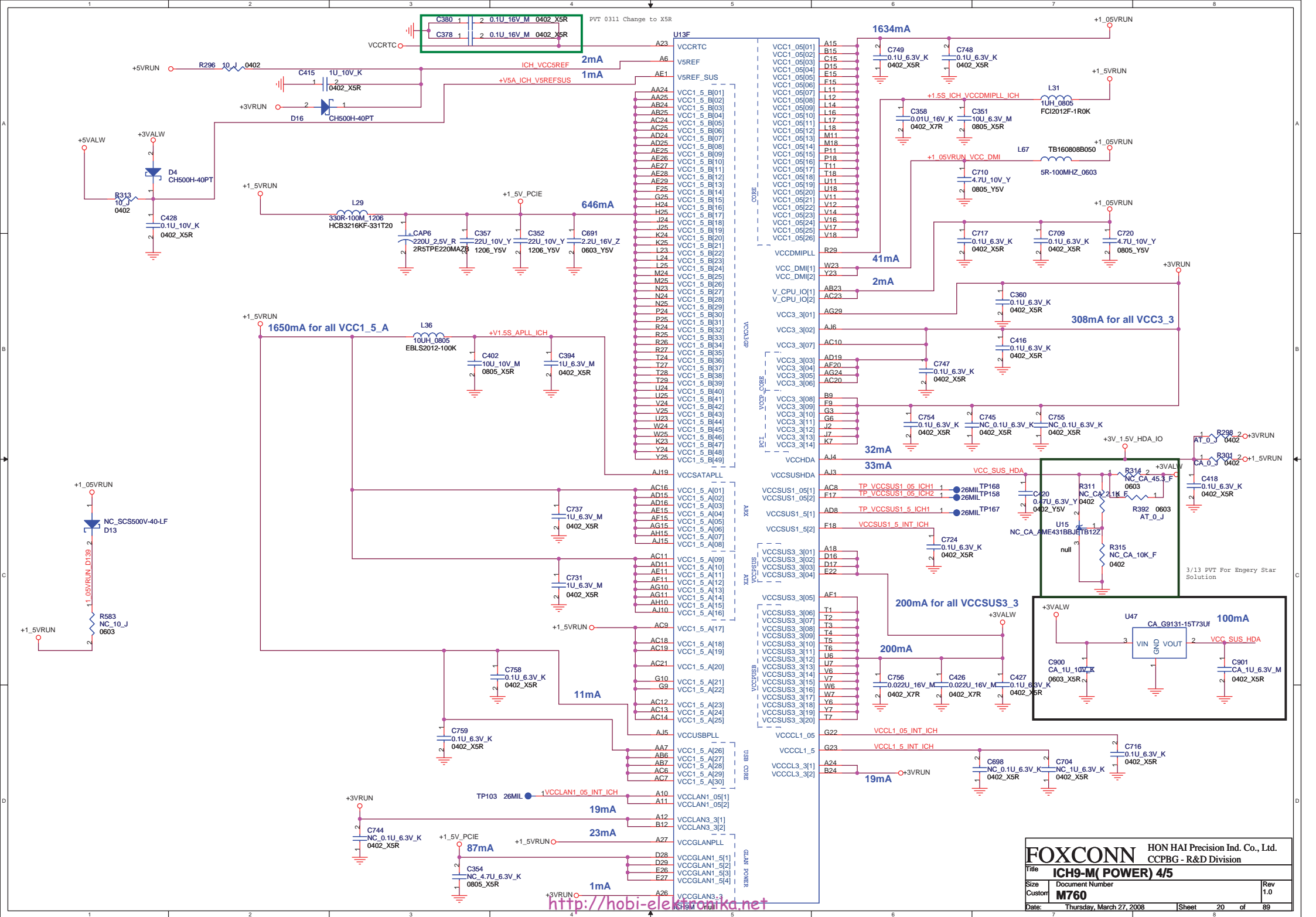


<http://hobi-elektronika.net>

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Title: **ICH9-M (GPIO) 3/5**

Size: A3
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Title: **ICH9-M (POWER) 4/5**

Size: Document Number
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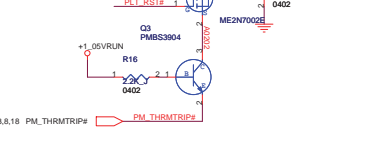
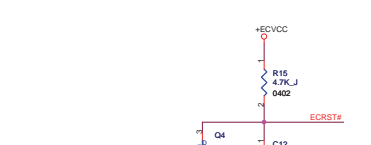
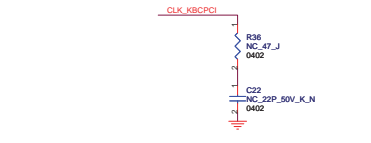
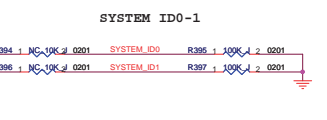
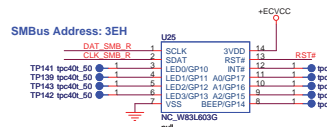
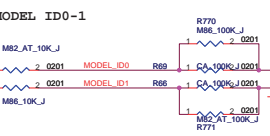
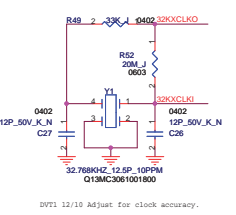
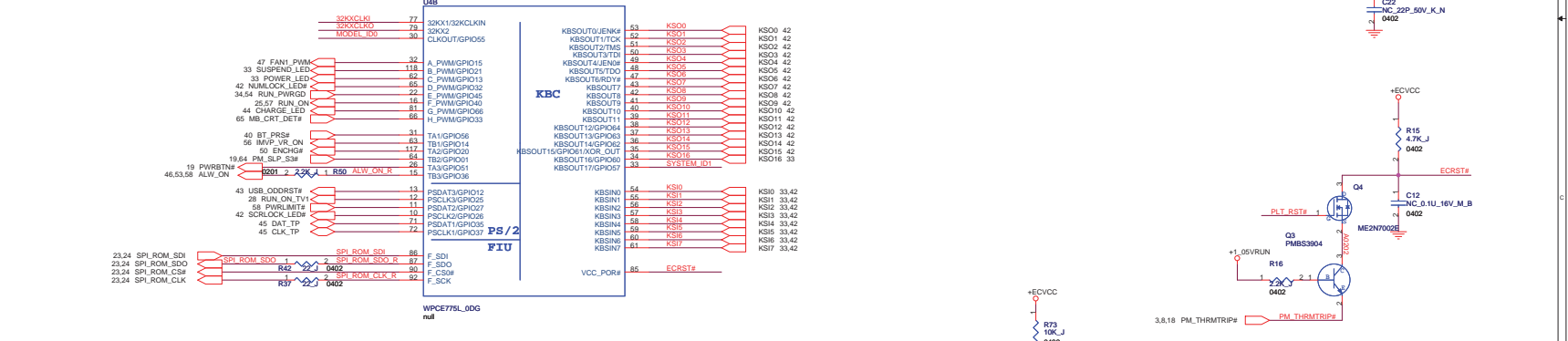
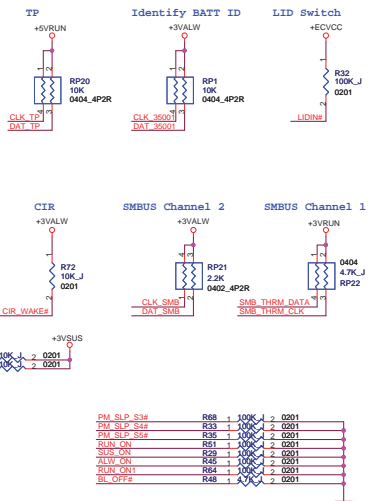
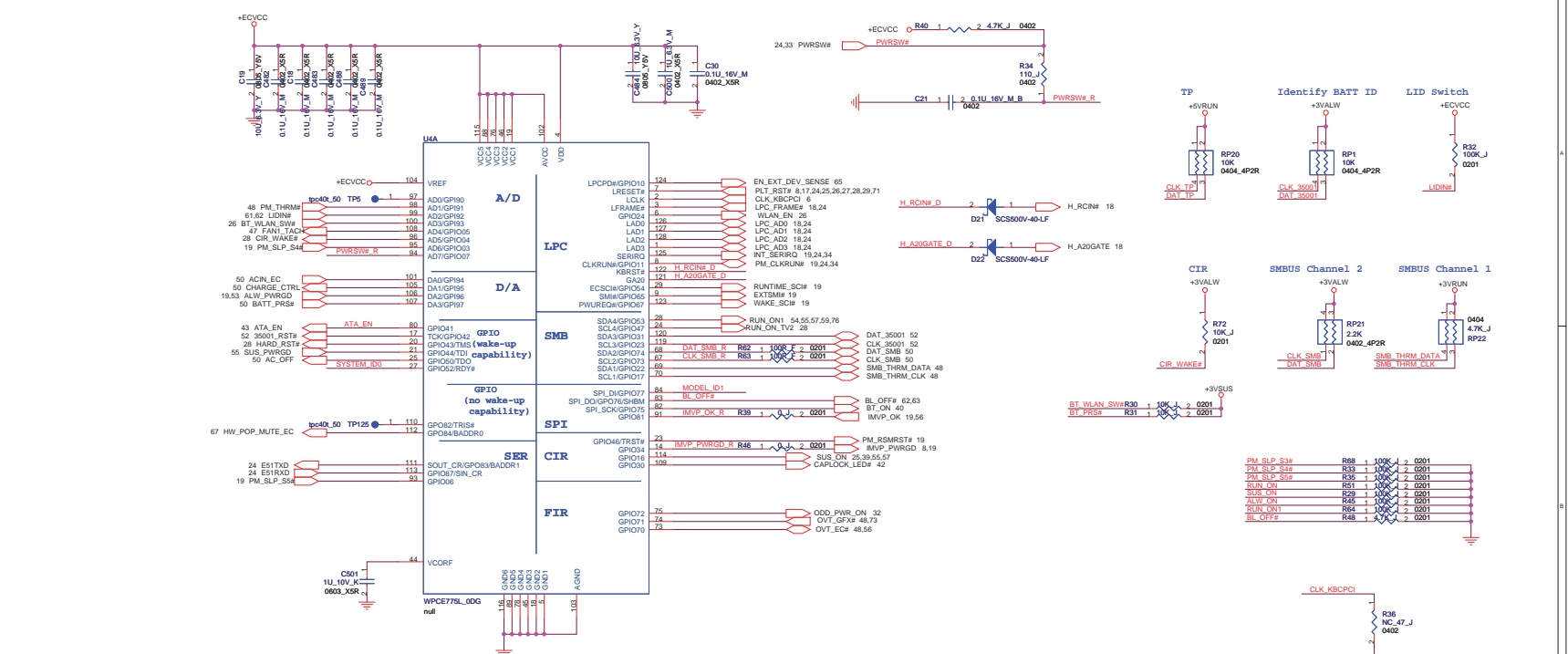
<http://hobi-ele.com/kd.net>

U13E		
AA26	VSS[001]	VSS[107]
AA27	VSS[002]	VSS[108]
AA3	VSS[003]	VSS[109]
AA6	VSS[004]	VSS[110]
AB1	VSS[005]	VSS[111]
AA23	VSS[006]	VSS[112]
AB28	VSS[007]	VSS[113]
AB23	VSS[008]	VSS[114]
AB4	VSS[009]	VSS[115]
AB5	VSS[010]	VSS[116]
AC17	VSS[011]	VSS[117]
AC26	VSS[012]	VSS[118]
AC27	VSS[013]	VSS[119]
AC3	VSS[014]	VSS[120]
AD1	VSS[015]	VSS[121]
AD10	VSS[016]	VSS[122]
AD12	VSS[017]	VSS[123]
AD13	VSS[018]	VSS[124]
AD14	VSS[019]	VSS[125]
AD17	VSS[020]	VSS[126]
AD18	VSS[021]	VSS[127]
AD21	VSS[022]	VSS[128]
AD28	VSS[023]	VSS[129]
AD29	VSS[024]	VSS[130]
AD4	VSS[025]	VSS[131]
AD5	VSS[026]	VSS[132]
AD6	VSS[027]	VSS[133]
AD7	VSS[028]	VSS[134]
AD9	VSS[029]	VSS[135]
AE12	VSS[030]	VSS[136]
AE13	VSS[031]	VSS[137]
AE14	VSS[032]	VSS[138]
AE16	VSS[033]	VSS[139]
AE17	VSS[034]	VSS[140]
AE2	VSS[035]	VSS[141]
AE20	VSS[036]	VSS[142]
AE24	VSS[037]	VSS[143]
AE3	VSS[038]	VSS[144]
AE4	VSS[039]	VSS[145]
AE6	VSS[040]	VSS[146]
AE9	VSS[041]	VSS[147]
AF13	VSS[042]	VSS[148]
AF16	VSS[043]	VSS[149]
AF18	VSS[044]	VSS[150]
AF22	VSS[045]	VSS[151]
AH26	VSS[046]	VSS[152]
AF26	VSS[047]	VSS[153]
AF27	VSS[048]	VSS[154]
AF5	VSS[049]	VSS[155]
AF7	VSS[050]	VSS[156]
AF9	VSS[051]	VSS[157]
AG13	VSS[052]	VSS[158]
AG18	VSS[053]	VSS[159]
AG18	VSS[054]	VSS[160]
AG20	VSS[055]	VSS[161]
AG23	VSS[056]	VSS[162]
AG3	VSS[057]	VSS[163]
AG6	VSS[058]	VSS[164]
AG9	VSS[059]	VSS[165]
AH12	VSS[060]	VSS[166]
AH14	VSS[061]	VSS[167]
AH17	VSS[062]	VSS[168]
AH19	VSS[063]	VSS[169]
AH2	VSS[064]	VSS[170]
AH22	VSS[065]	VSS[171]
AH25	VSS[066]	VSS[172]
AH28	VSS[067]	VSS[173]
AH5	VSS[068]	VSS[174]
AH8	VSS[069]	VSS[175]
AJ12	VSS[070]	VSS[176]
AJ14	VSS[071]	VSS[177]
AJ17	VSS[072]	VSS[178]
AJ8	VSS[073]	VSS[179]
B11	VSS[074]	VSS[180]
B14	VSS[075]	VSS[181]
B17	VSS[076]	VSS[182]
B2	VSS[077]	VSS[183]
B20	VSS[078]	VSS[184]
B23	VSS[079]	VSS[185]
B5	VSS[080]	VSS[186]
B8	VSS[081]	VSS[187]
C26	VSS[082]	VSS[188]
C27	VSS[083]	VSS[189]
E11	VSS[084]	VSS[190]
E14	VSS[085]	VSS[191]
E18	VSS[086]	VSS[192]
E2	VSS[087]	VSS[193]
E21	VSS[088]	VSS[194]
E24	VSS[089]	VSS[195]
E5	VSS[090]	VSS[196]
E8	VSS[091]	VSS[197]
F16	VSS[092]	VSS[198]
F28	VSS[093]	
F29	VSS[094]	VSS_NCTF[01]
G12	VSS[095]	VSS_NCTF[02]
G14	VSS[096]	VSS_NCTF[03]
G18	VSS[097]	VSS_NCTF[04]
G21	VSS[098]	VSS_NCTF[05]
G24	VSS[099]	VSS_NCTF[06]
G26	VSS[100]	VSS_NCTF[07]
G27	VSS[101]	VSS_NCTF[08]
G8	VSS[102]	VSS_NCTF[09]
H2	VSS[103]	VSS_NCTF[10]
H23	VSS[104]	VSS_NCTF[11]
H28	VSS[105]	VSS_NCTF[12]
H29	VSS[106]	

ICH9M
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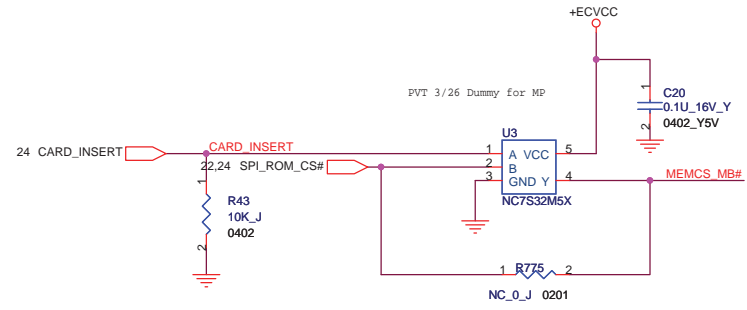
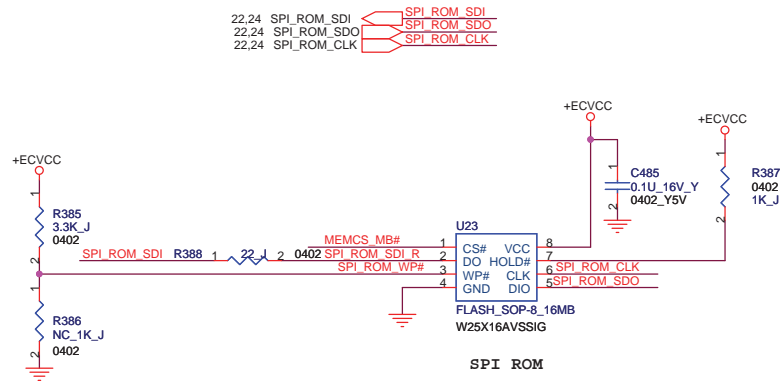
<http://hobi-elektronika.net>

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
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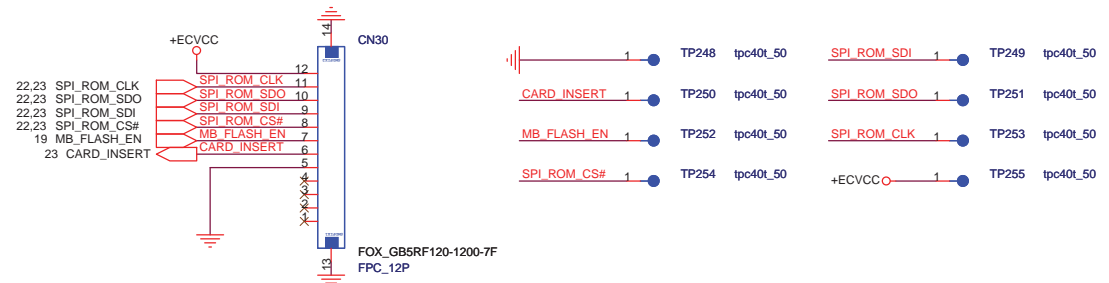


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0	0	UMA
0	1	DISCRETE (M82)
1	0	DISCRETE (M86)

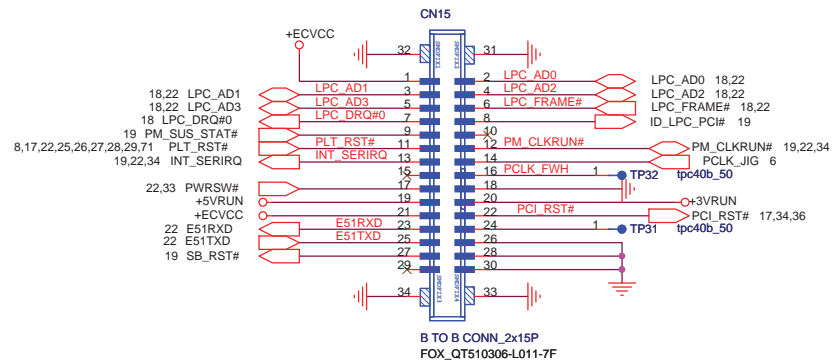
ID1	ID0	SKU
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0	1	RESERVED
1	0	RESERVED



PVT 3/26 Dummy for MP

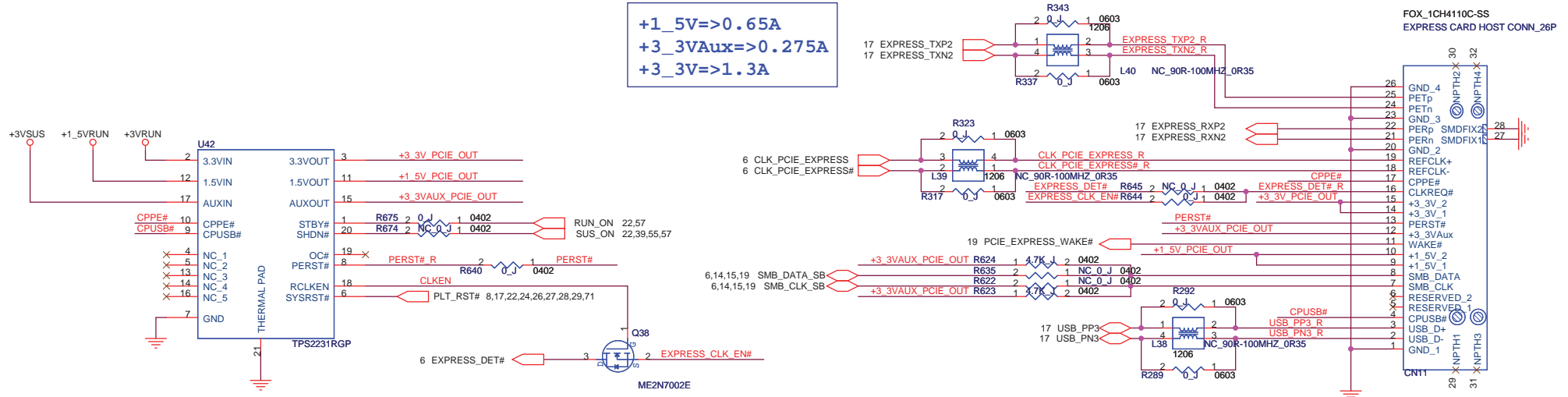


EXTERNAL SPI ROM INTERFACE

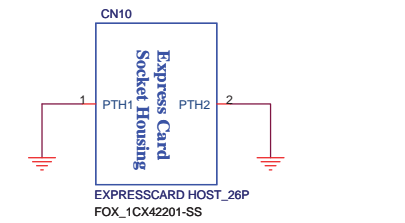
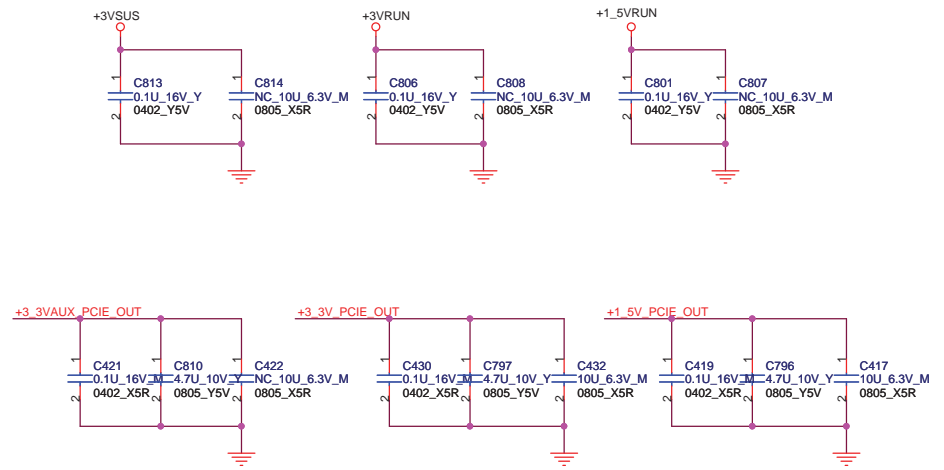


JIG-120

FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title Debug Port			
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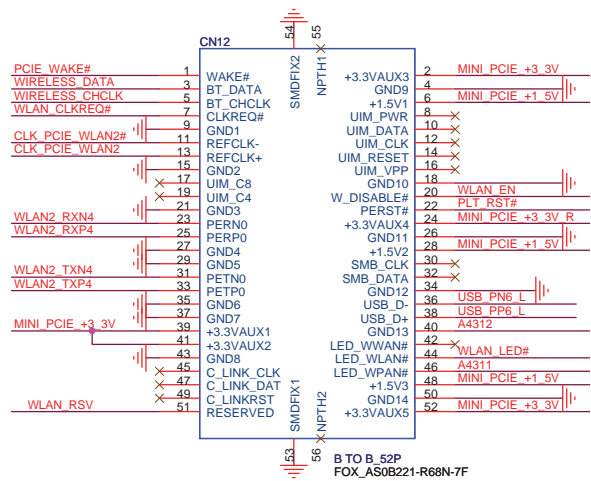


Express Card Slot.

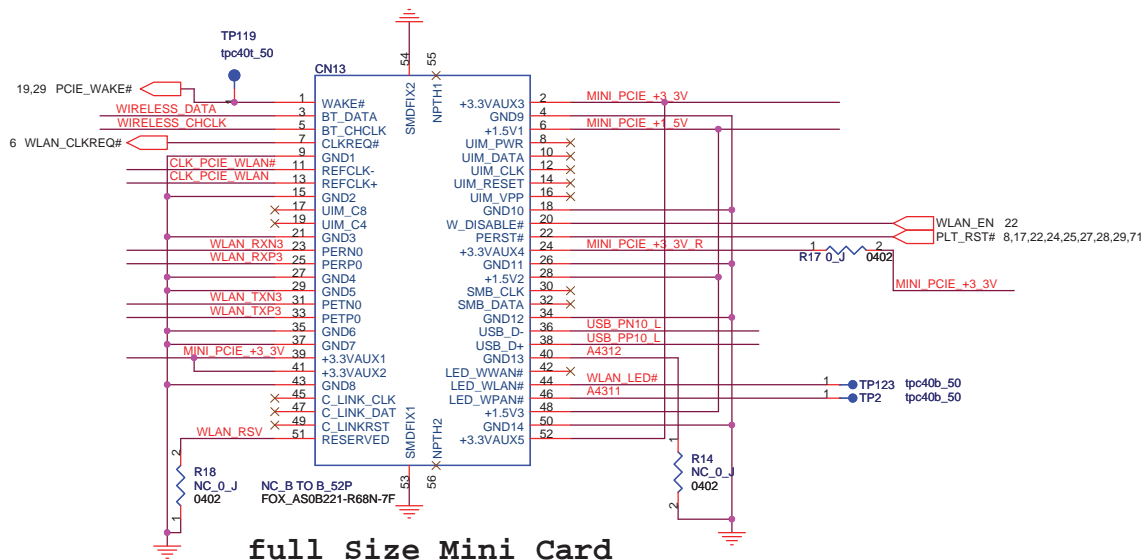


Express Card Housing.

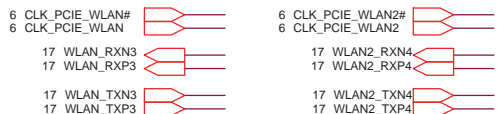
+1_5V=>0.65A
 +3_3VAux=>0.275A
 +3_3V=>1.3A



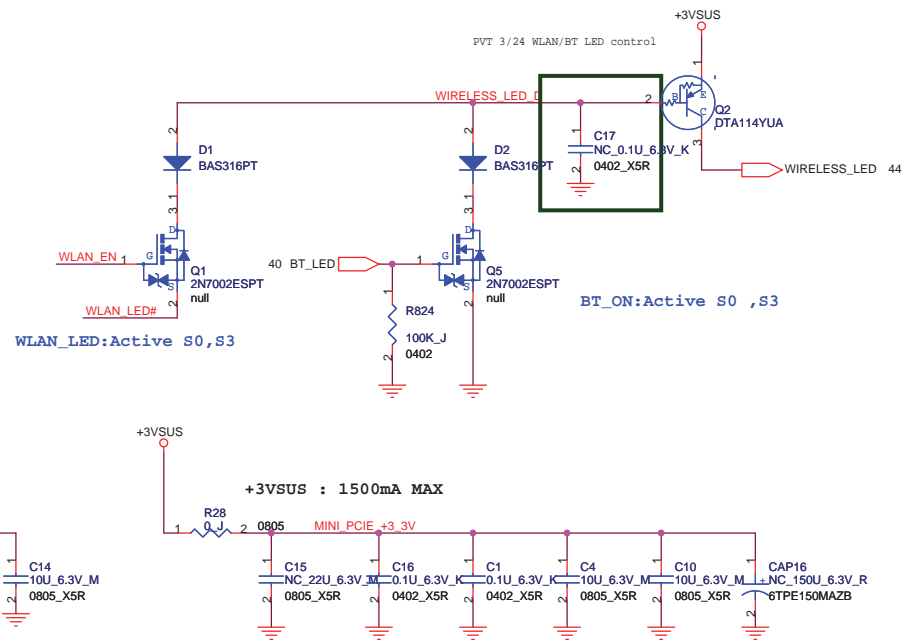
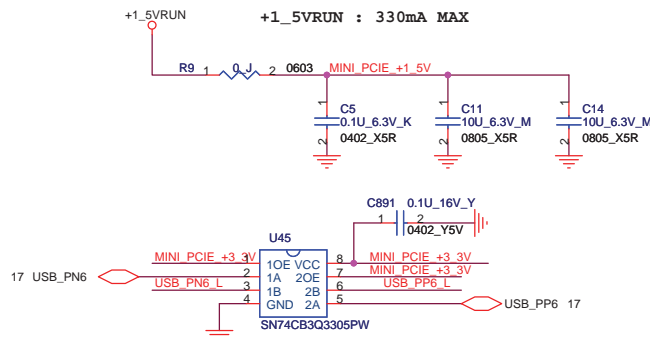
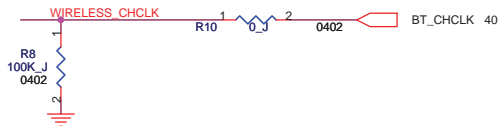
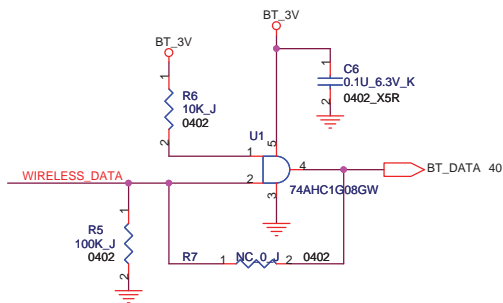
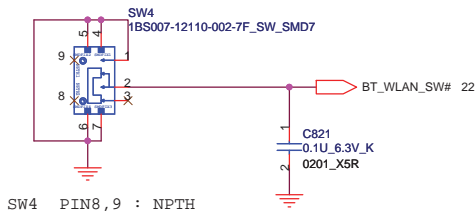
Half Size Mini Card



full size Mini Card

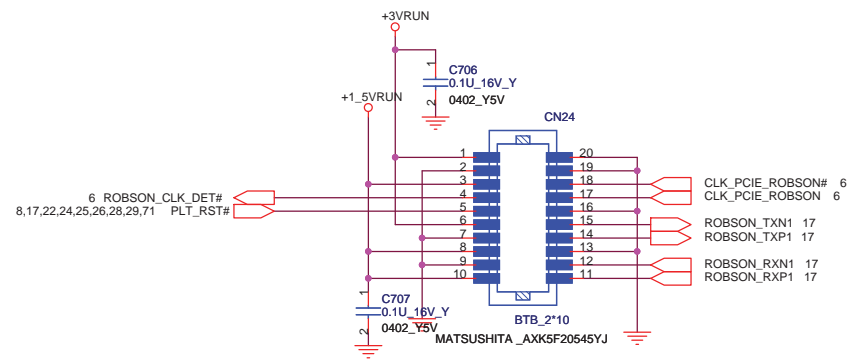


WLAN Switch

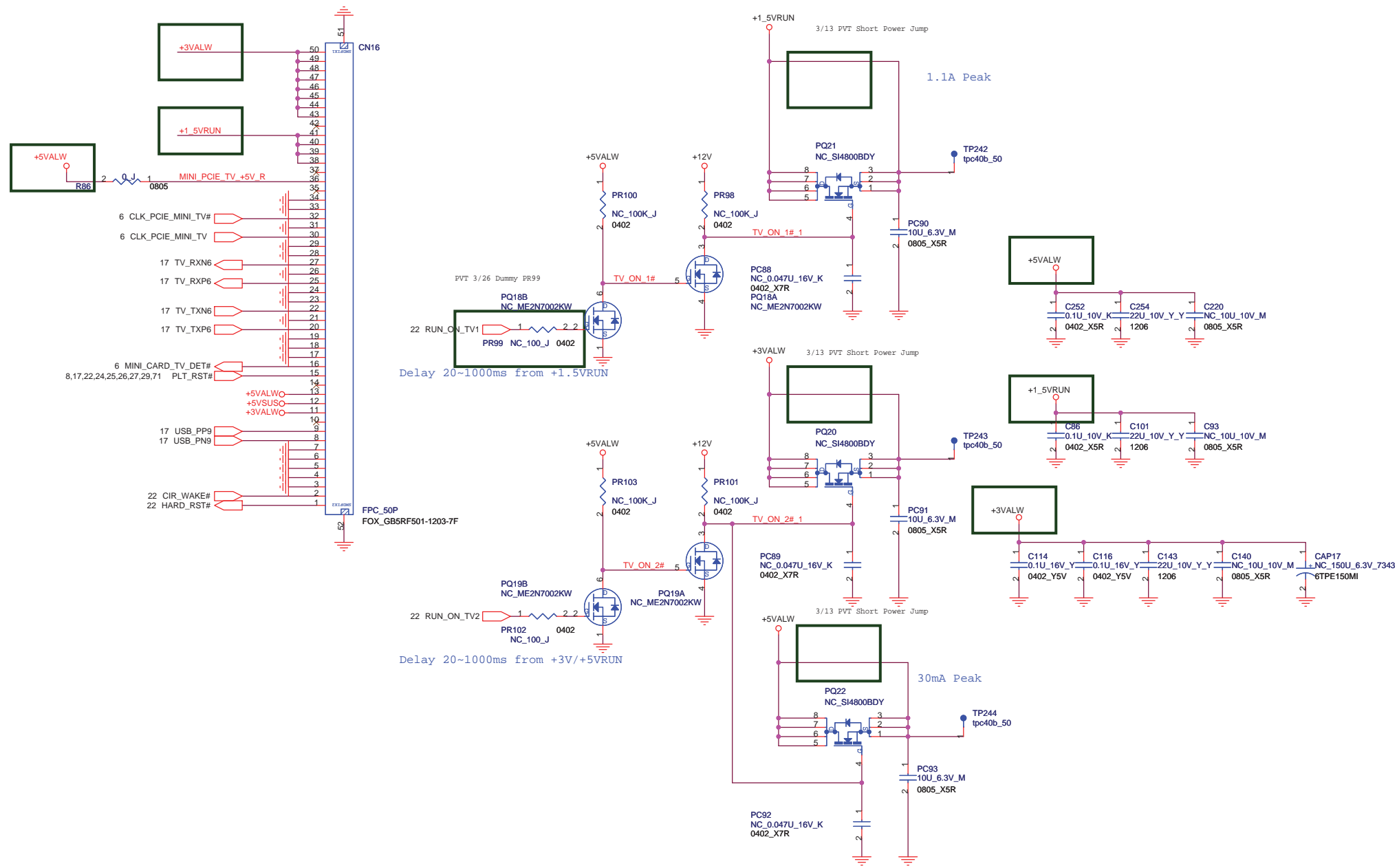


Dummy R17,R9,C5,C11,C14 when use Echo Peak and Shirley Peak

FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	Mini-PCIE Card (WLAN)	
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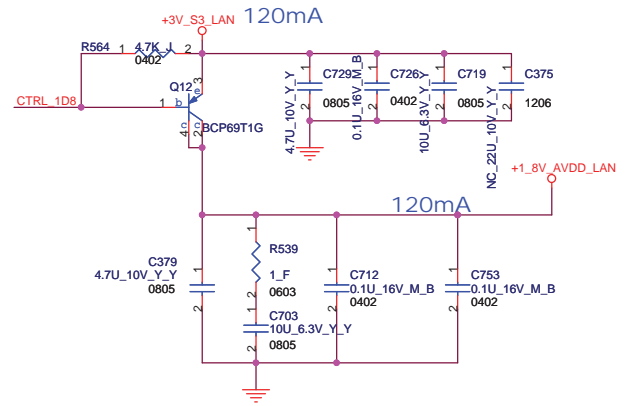
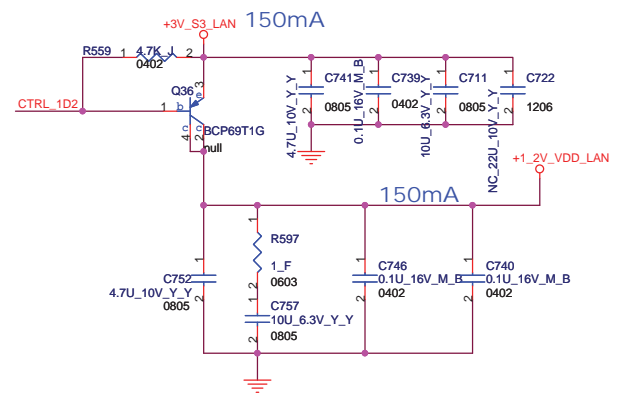
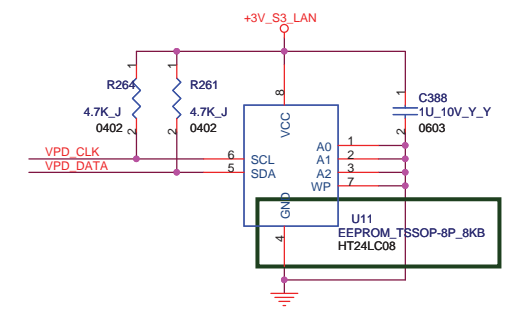
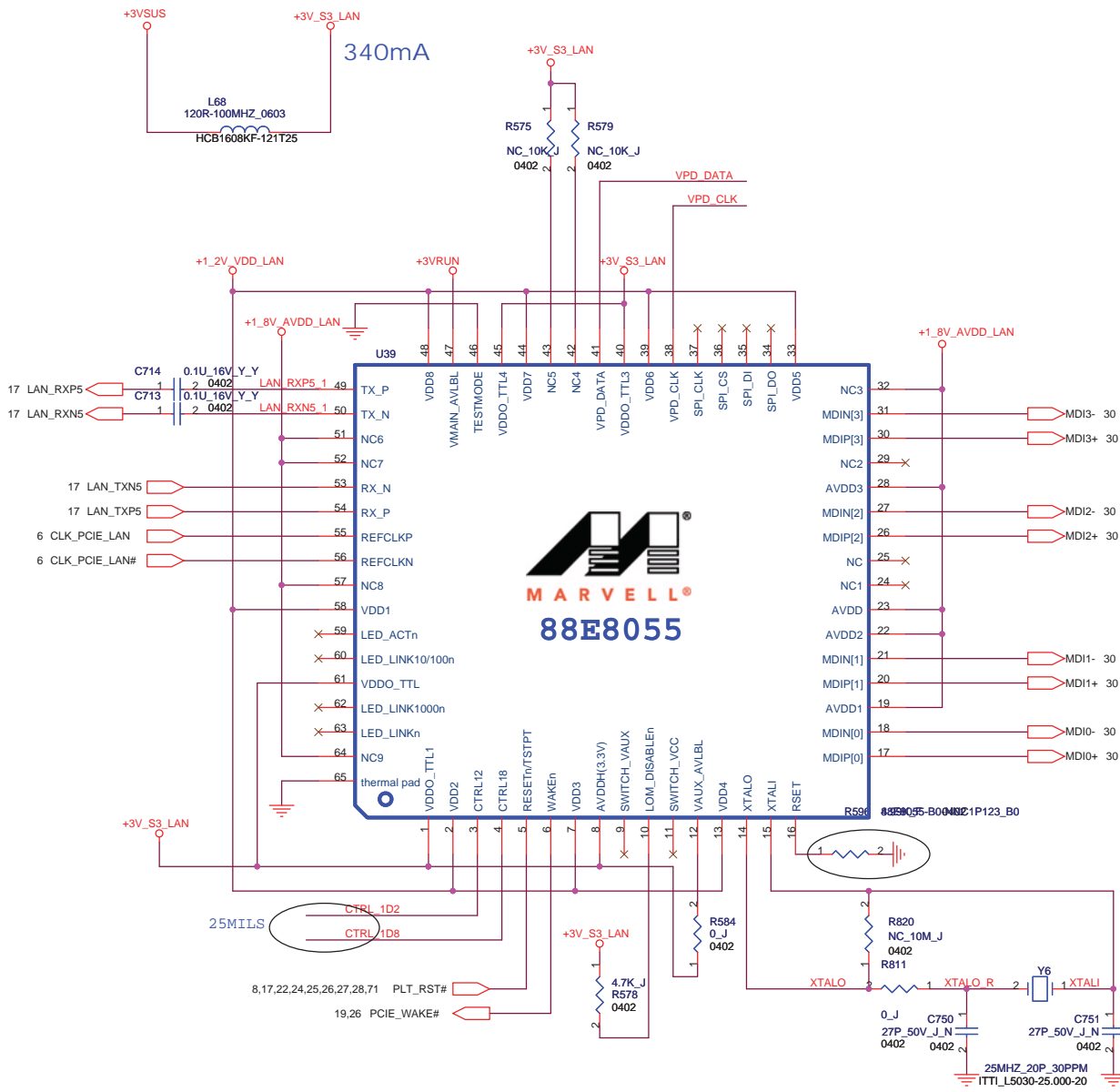


Robson 1.6 Module



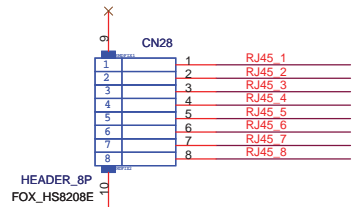
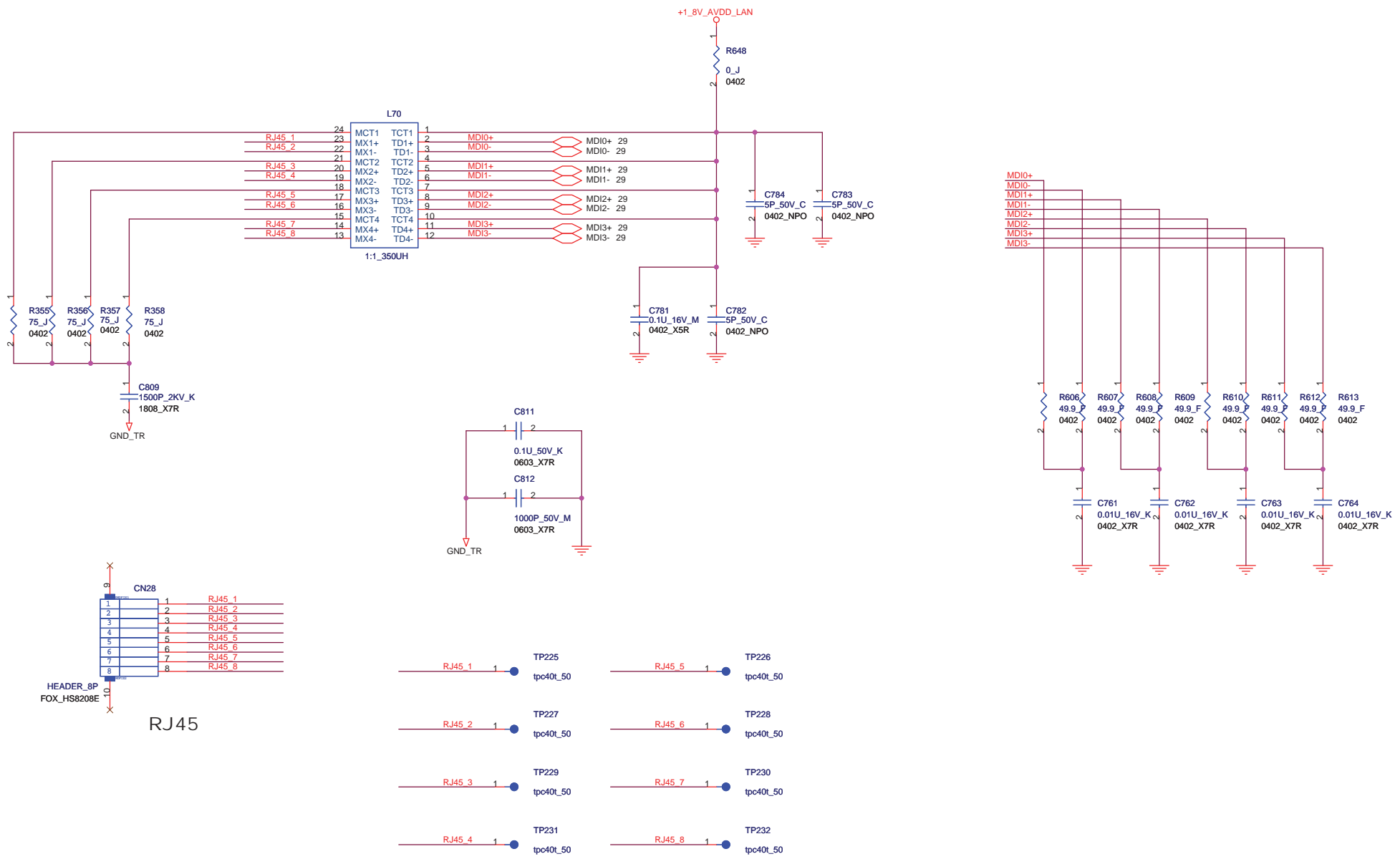
Delay 20-1000ms from +1.5VRUN

Delay 20-1000ms from +3V/+5VRUN

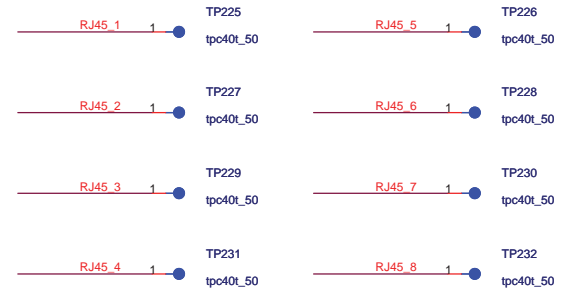


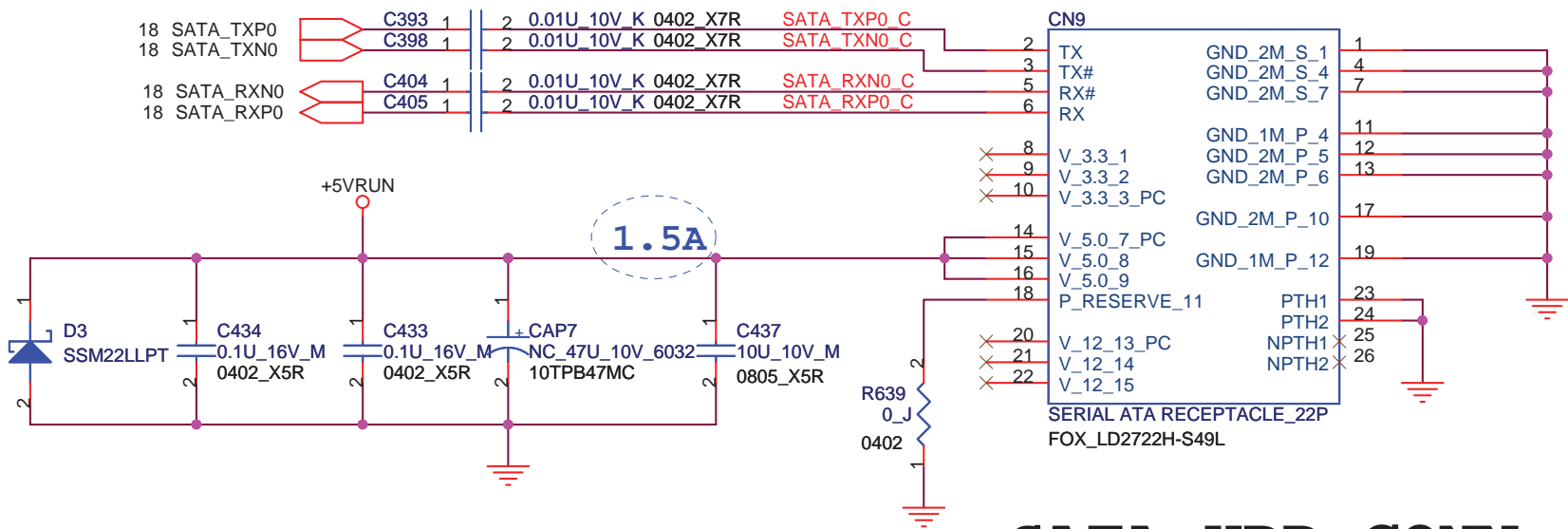
DVT1 12/18 Add series resistor for frequency adjust.

FOXCONN		HON HAI PRECISION IND. CO., LTD.	
		CPBG - R&D Division	
Title			
LAN (88E8055)(1/2)			
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RJ45





SATA HDD CONN

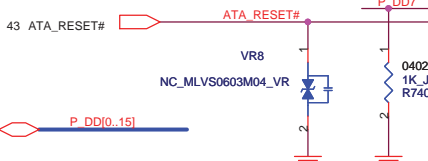
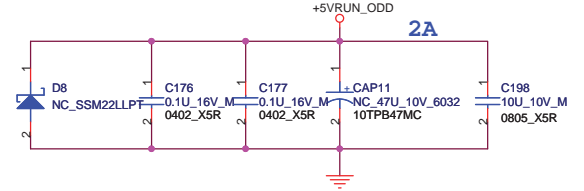
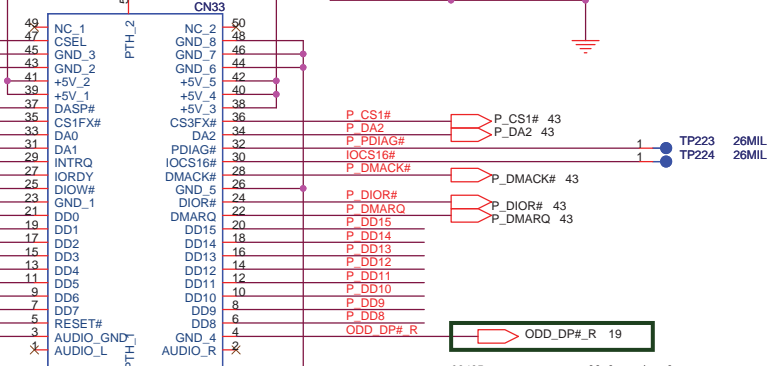
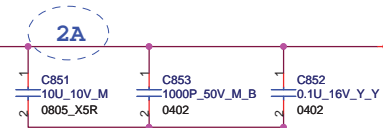
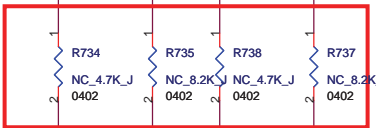
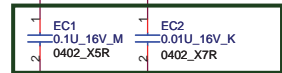
FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title SATA HDD			
Size A	Document Number M760	Rev 1.0	
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4/17 (MS90)
Follow Adoi san suggest ODD: Master/HDD:Slave

H: Slave
L: Master
ODD must Master

- 44 ODD_LED#
- 43 P_CS0#
- 43 P_DAO#
- 43 P_DA1#
- 43 P_INTRQ
- 43 P_IORDY#
- 43 P_DIOW#

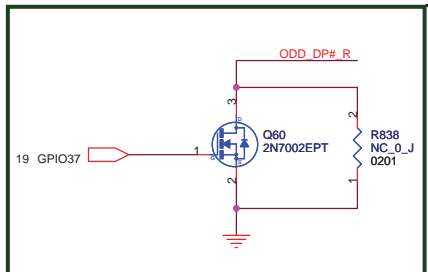
- ODD_LED#
- P_CS0#
- P_DAO#
- P_DA1#
- P_INTRQ
- P_IORDY#
- P_DIOW#



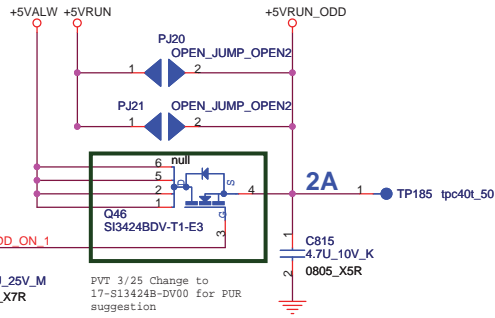
03/27 PVT Reserve pull low signal for odd detection.

For ESD.

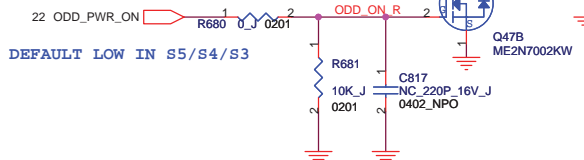
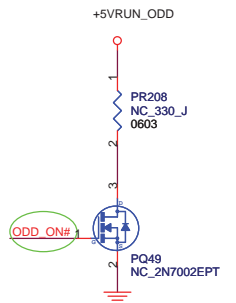
PATA ODD CONN



PVT 3/27 For ODD_DP# function improvement

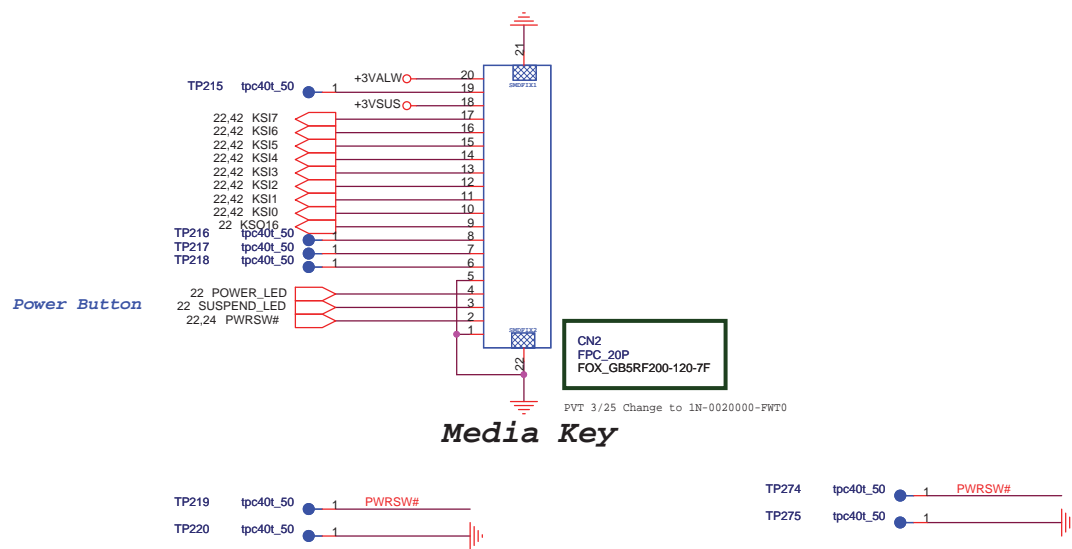


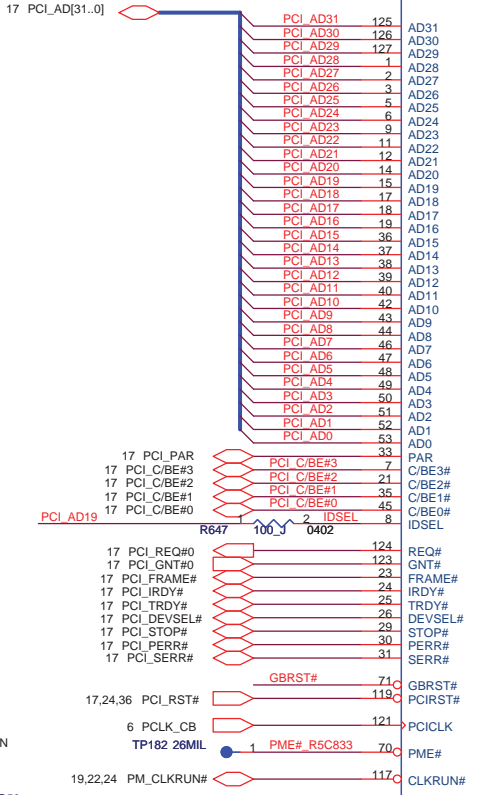
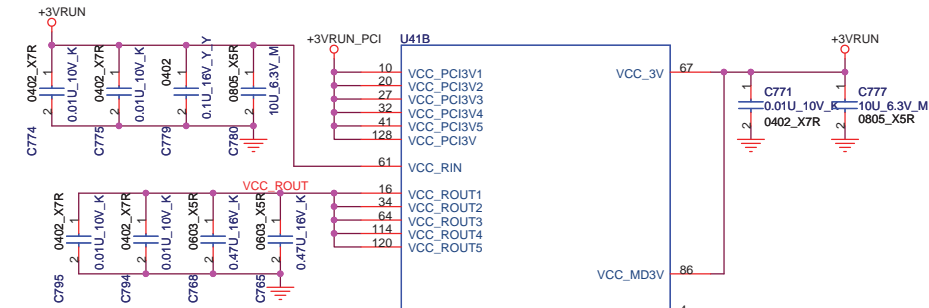
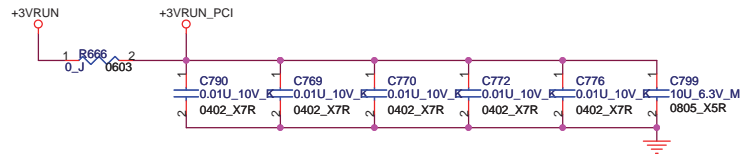
PVT 3/25 Change to 17-Si3424B-DV00 for PUR suggestion



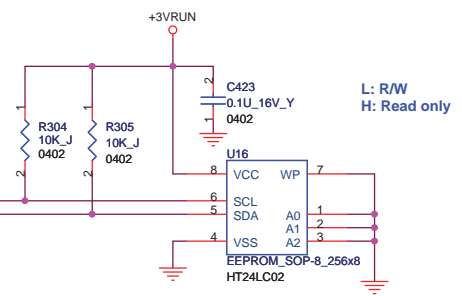
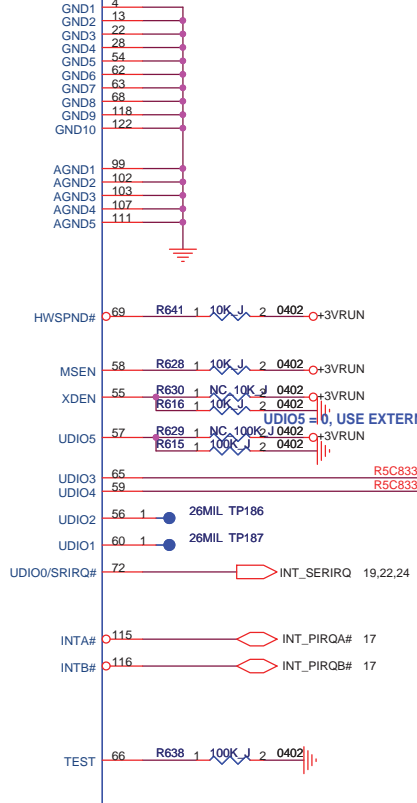
DEFAULT LOW IN S5/S4/S3

FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title PATA ODD		
Size A3	Document Number M760	Rev 1.0
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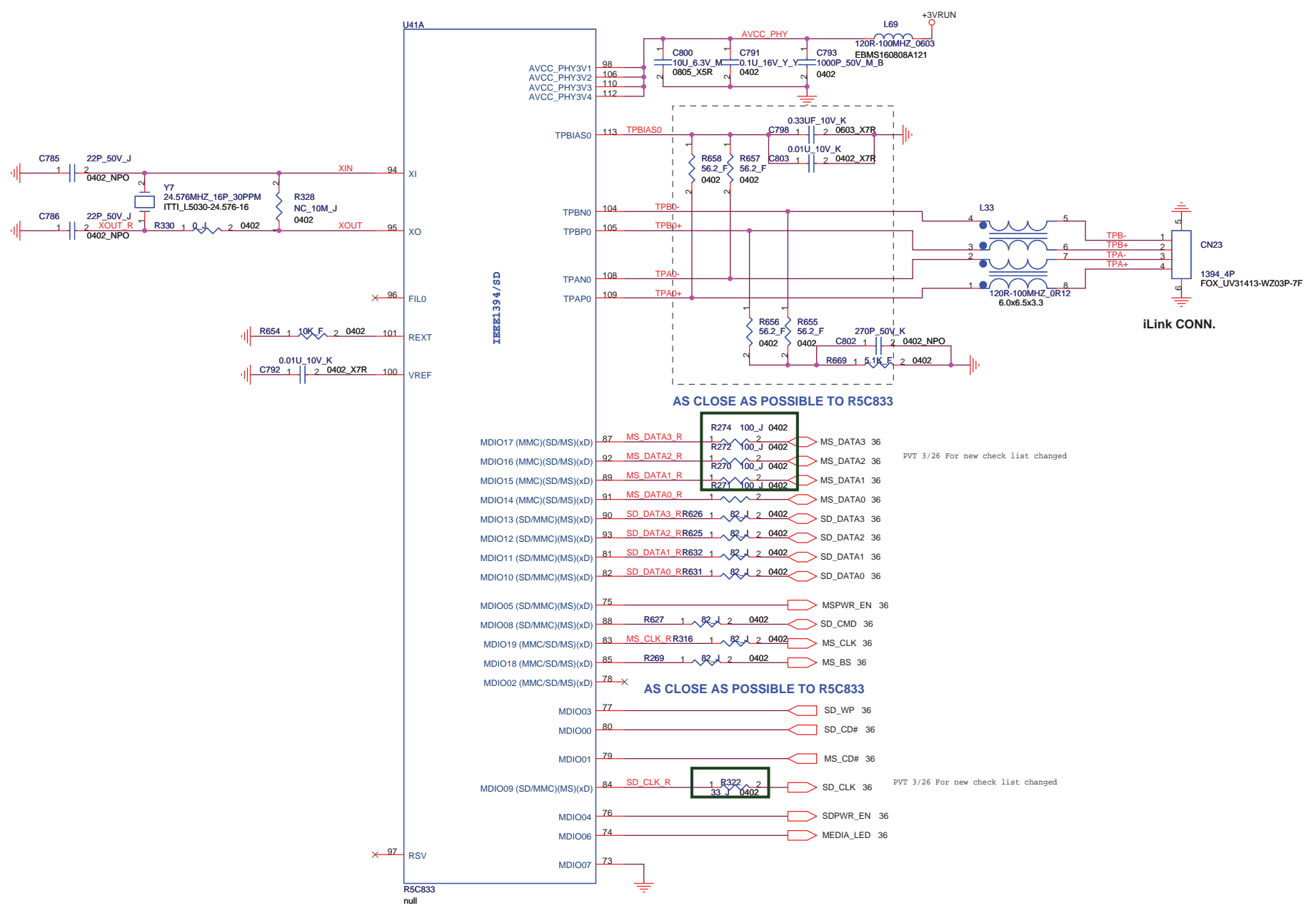




PCI / OTHER



<http://hobi-elektronika.net>

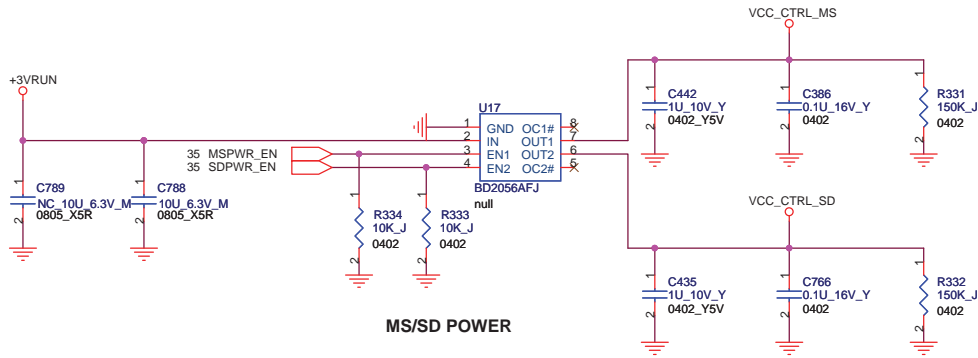


AS CLOSE AS POSSIBLE TO R5C833

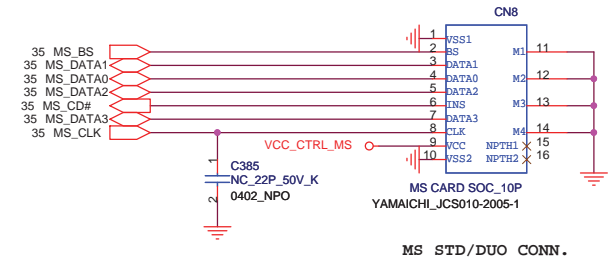
PVT 3/26 For new check list changed

PVT 3/26 For new check list changed

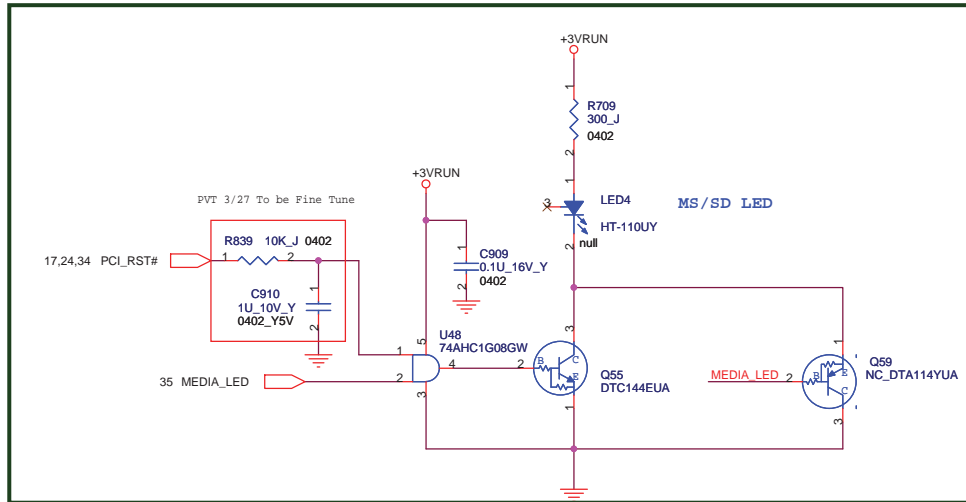
FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title PCI (I LINK)		CCPBG - R&D Division	
Size A3	Document Number M760	Rev 1.0	
Date:	Thursday, March 27, 2008	Sheet	35 of 89



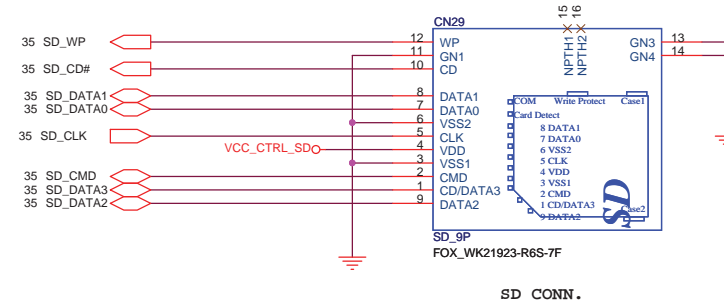
MS/SD POWER



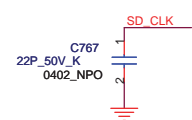
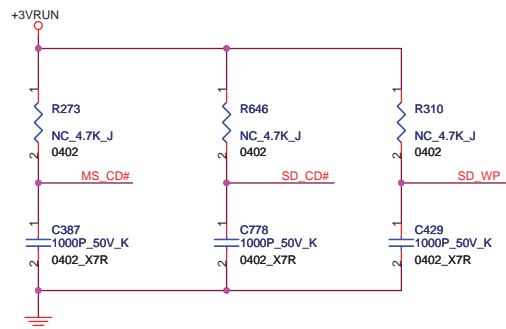
MS STD/DUO CONN.



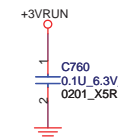
PVT 3/27 Reserve the MEDIA_LED control Active Low Schematic



SD CONN.

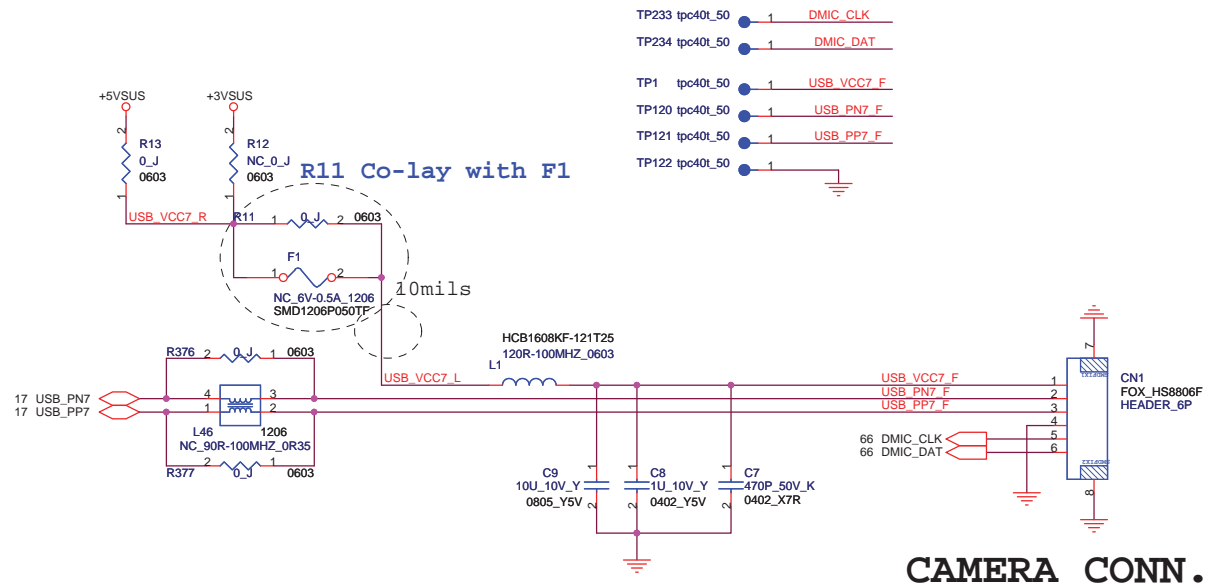


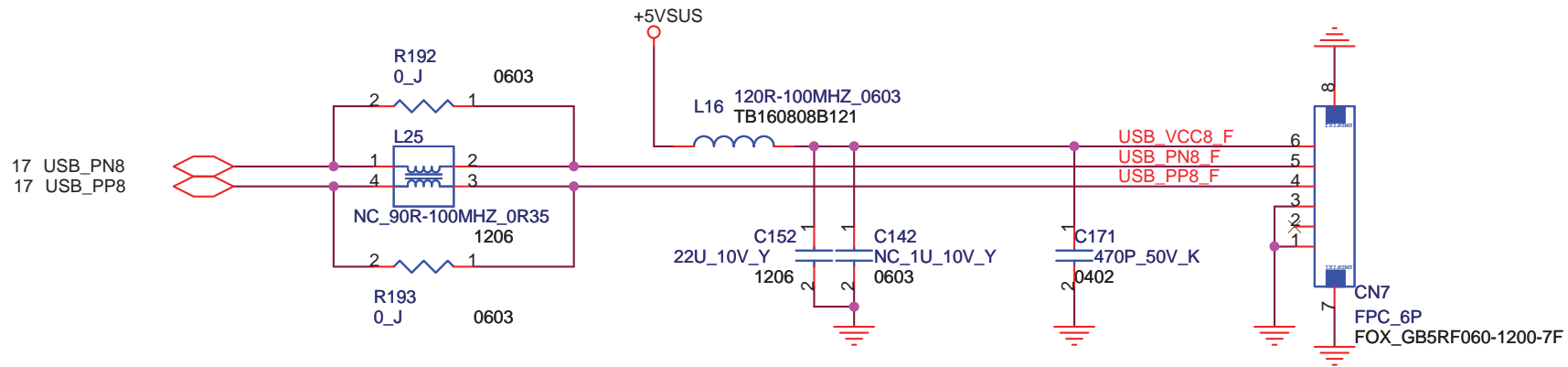
For EMI



<http://hobi-elektronika.net>

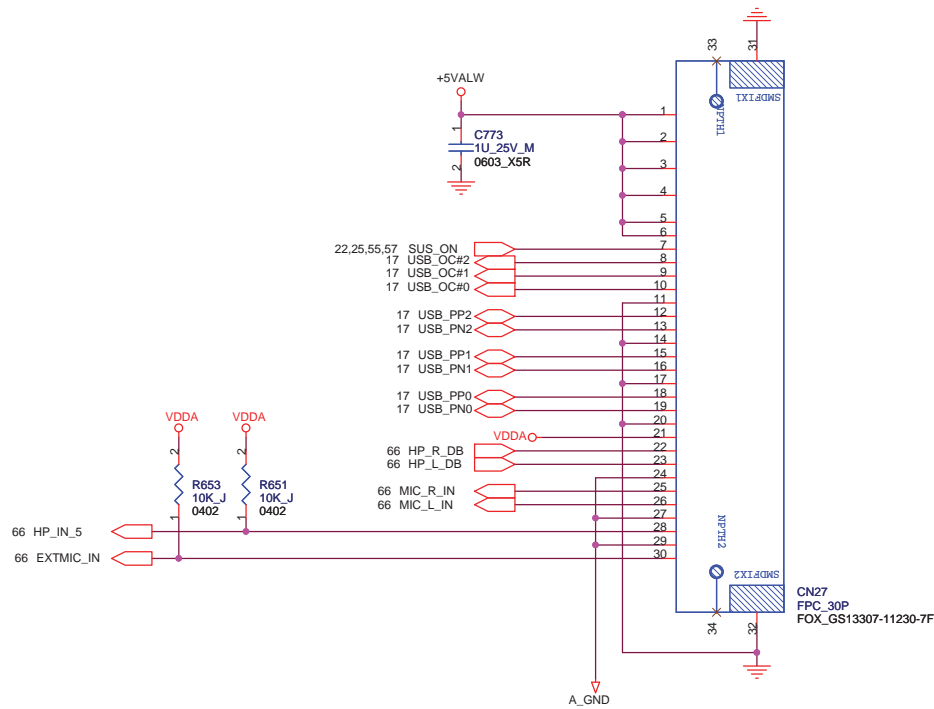
FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		Title PCI (MS&SD)	
		Size A3	Document Number M760
Date: Thursday, March 27, 2008	Sheet 36	Rev 1.0 of 89	

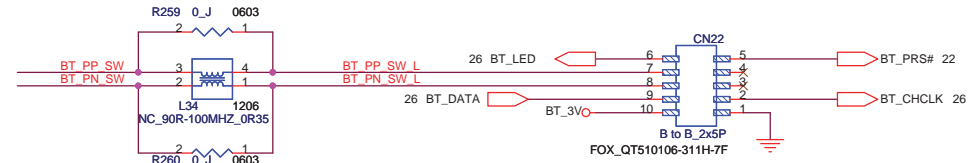
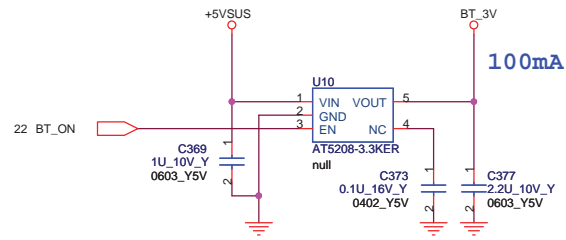




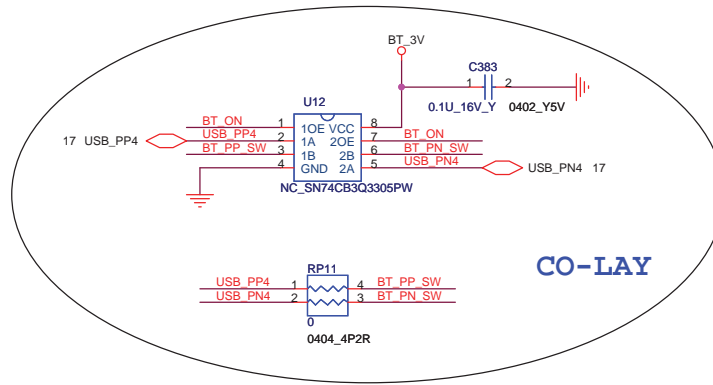
Felica Connector

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title FELICA			
Size A	Document Number M760	Rev 1.0	
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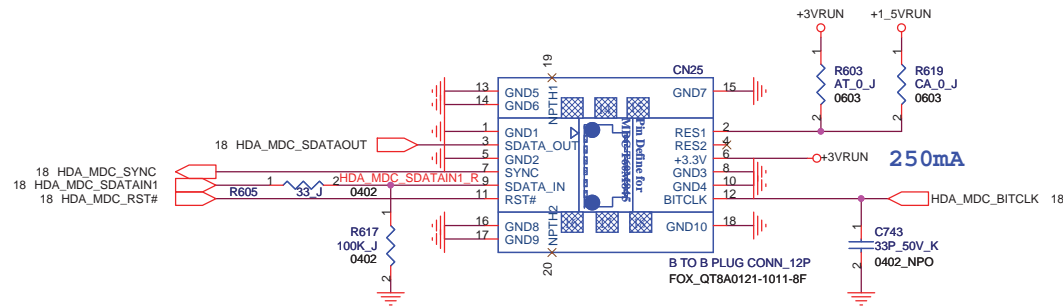
Bluetooth CONN.



CO-LAY

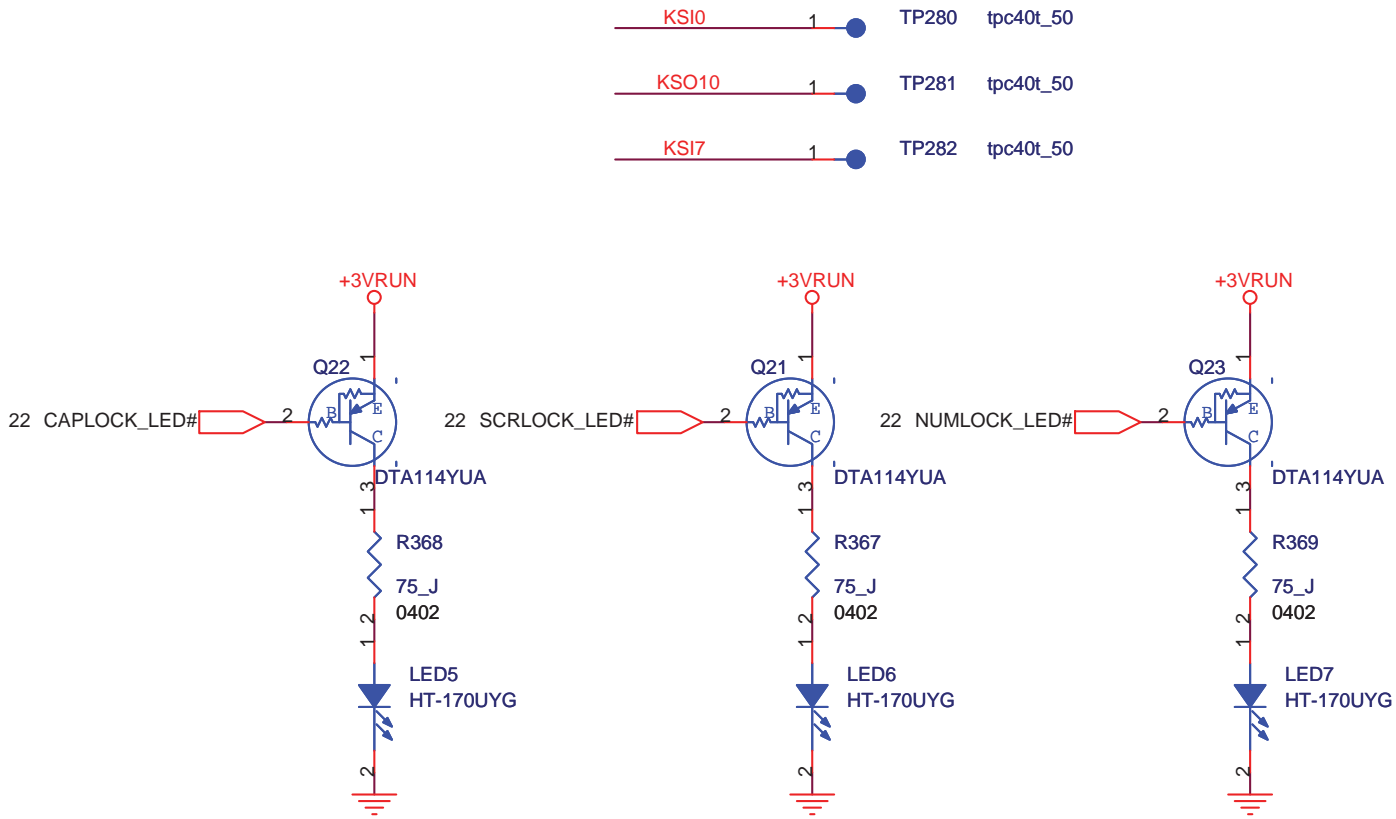
FOXCONN			HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
Title	Bluetooth		
Size	Document Number	Rev	
A3	M760	1.0	
Date:	Thursday, March 27, 2008	Sheet	40 of 89

MDC CONN.

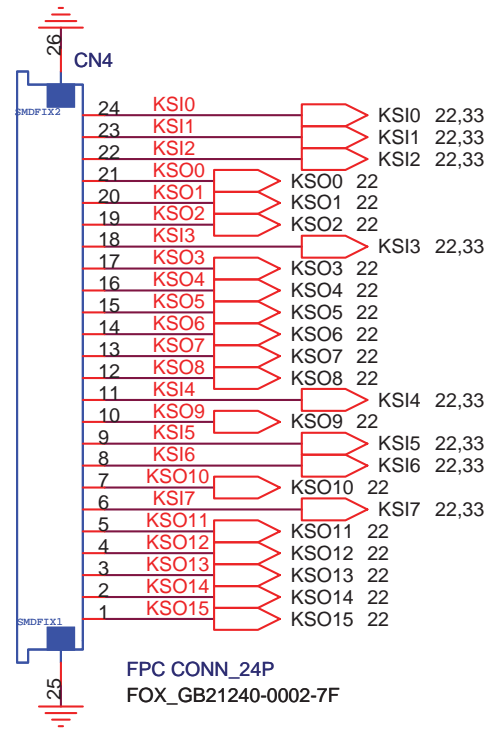


MS90 modem module only (1.5V)

FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
Title	MDC	
Size	Document Number	Rev
A3	M760	1.0
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- KSI0 1 TP280 tpc40t_50
- KSO10 1 TP281 tpc40t_50
- KSI7 1 TP282 tpc40t_50



KBC CNN

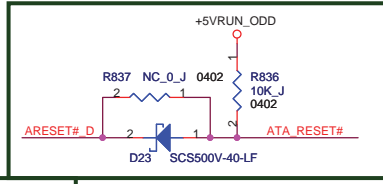
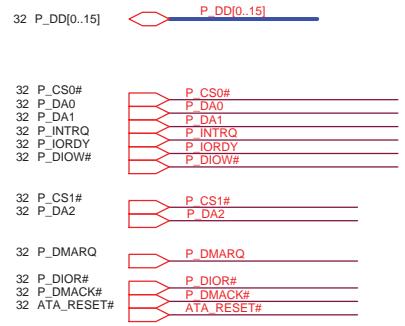
FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title KB Connector			
Size A	Document Number M760	Rev 1.0	
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USB2.0-->PATA BRIDGE

20070829(ODD_RESET#):
 1. Change from 0.22uF to 0.1uF net-work with a 10ms time constant;
 2. Add a diode to avoid potential voltage feedback.

Max=85mA
 Place the bypass capacitors as close to the chip VCC pin

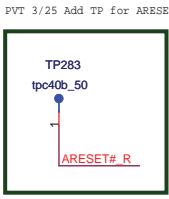
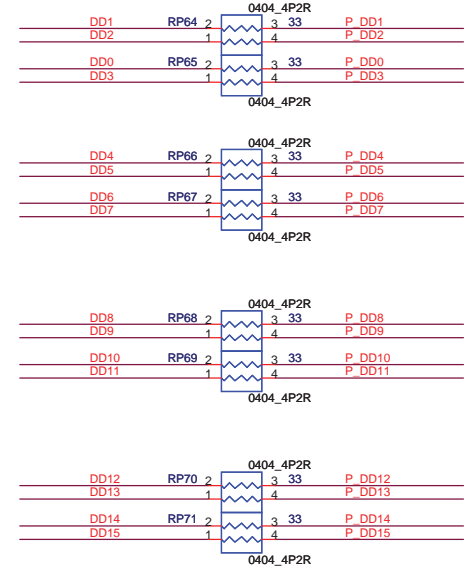
07'09/10:
 Change Crystal & add Cap
 must place crystal as close to Pin as possible



PVT 3/27 Add the power leakage solution

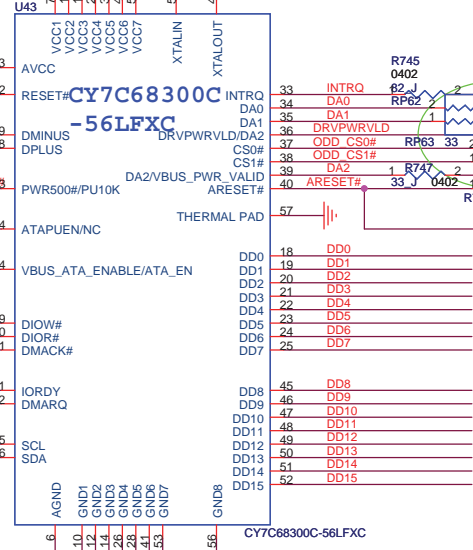
PVT 3/25 Reserve the Power Source to +3VSUS by MOR

*Layout Note:
 Please place these Series R close IC Pin



07'0924:
 For part not approve, Change

07'0928:
 Follow PAE suggestion, connect ARESET# instead of GND.
 CY7C68300 Ver. A has issue: EEPROM Data will lost.
 07'08/30(follow demo SCH):
 1. Address : '100';
 2. WP connect to ARESET#



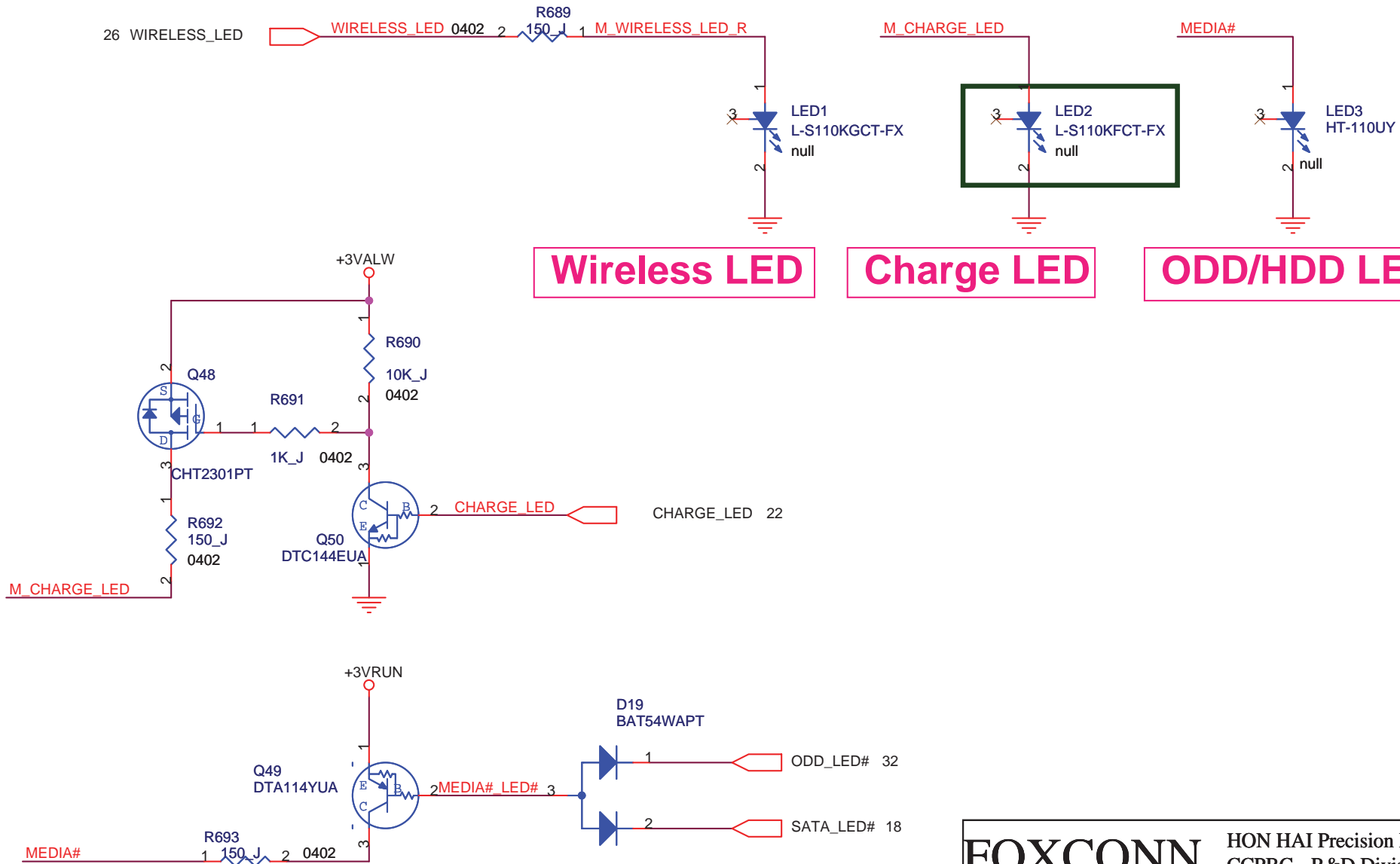
FOXCONN HON HAI PRECISION IND. CO., LTD.
 CPBG - R&D Division

Title: **USB 2.0 to PATA ODD (CY7C68300C-56LFXC)**

Size A3 Document Number **M760** Rev 1.0

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PVT 3/18 Change back to DVT1 solution

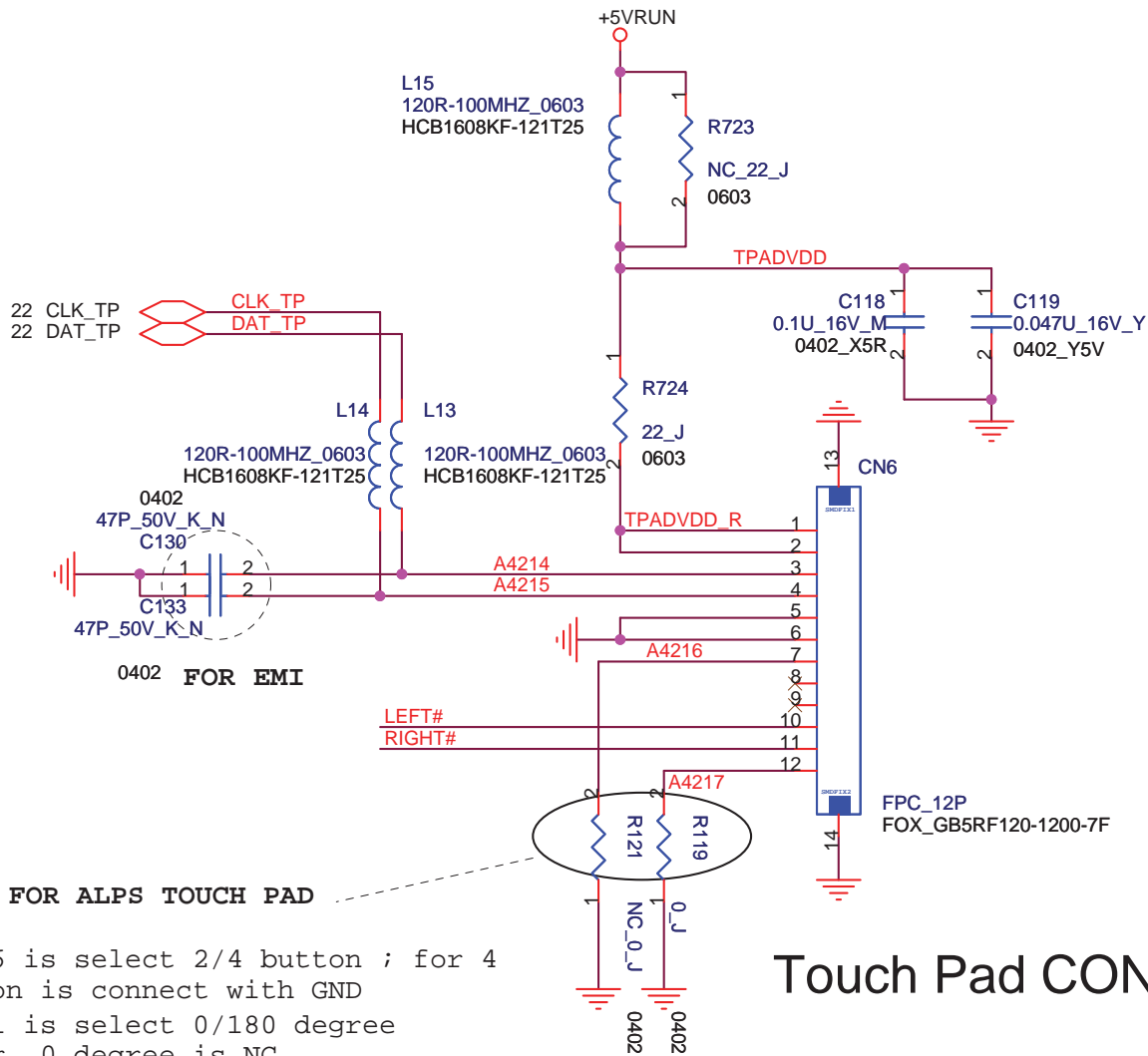


Wireless LED

Charge LED

ODD/HDD LED

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title Status LED			
Size A	Document Number M760	Rev 1.0	
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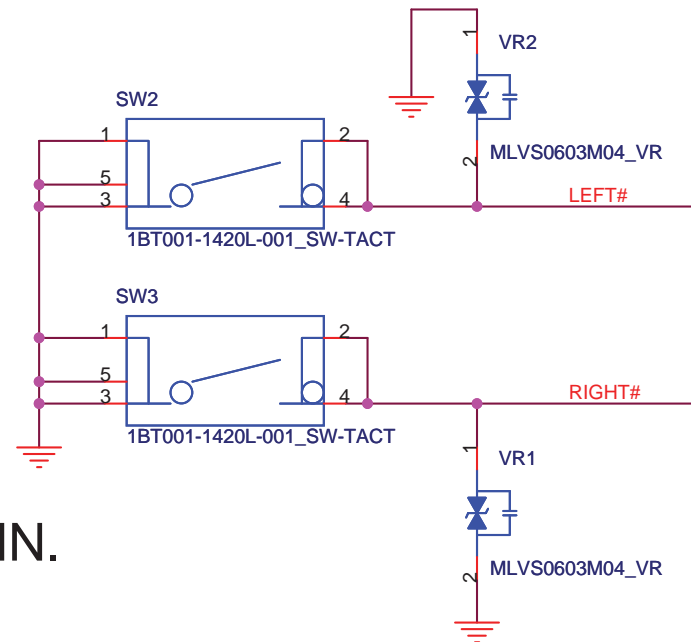


FOR ALPS TOUCH PAD

PIN 6 is select 2/4 button ; for 4 button is connect with GND
 PIN 1 is select 0/180 degree
 ; for 0 degree is NC

Touch Pad CONN.

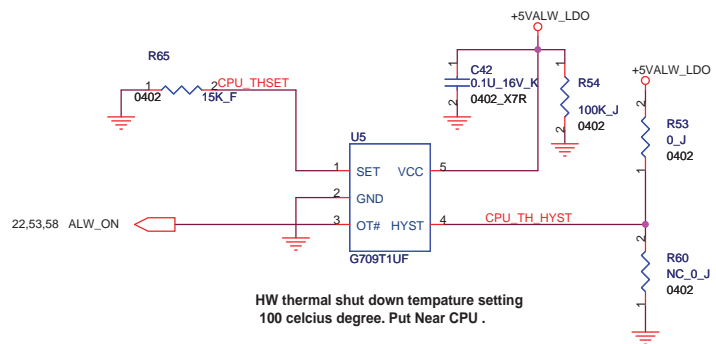
TP_LEFT Button

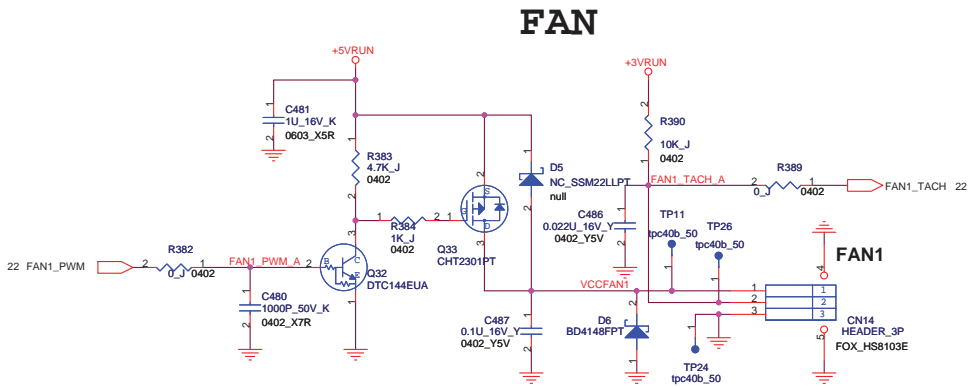


TP_Right Button

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title Touch Pad			
Size A	Document Number M760	Rev 1.0	
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HW THERMAL PROTECTION

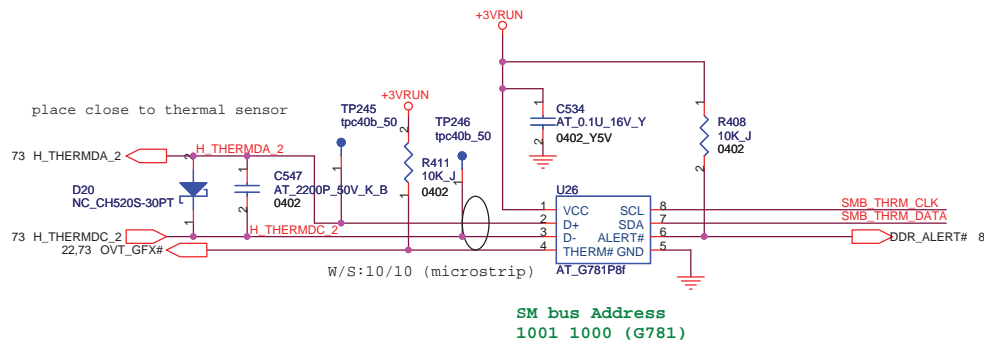




<http://hobi-elektronika.net>

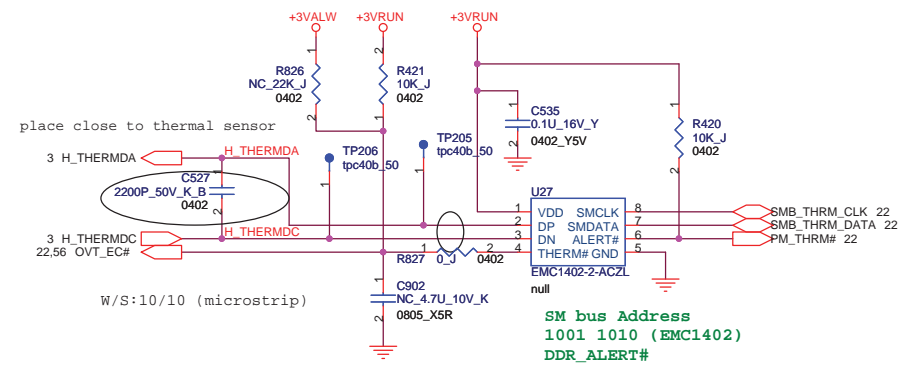
FOXCONN		HON HAI Precision Ind. Co., Ltd.
File: FAN		CCPBG - R&D Division
Size: Custom	Document Number: M760	Rev: 1.0
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GMCH/VGA SENSOR G781P8f

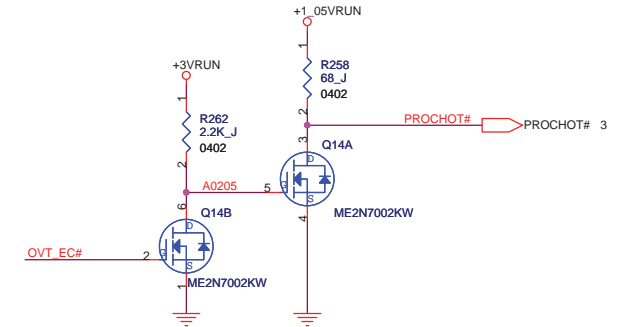


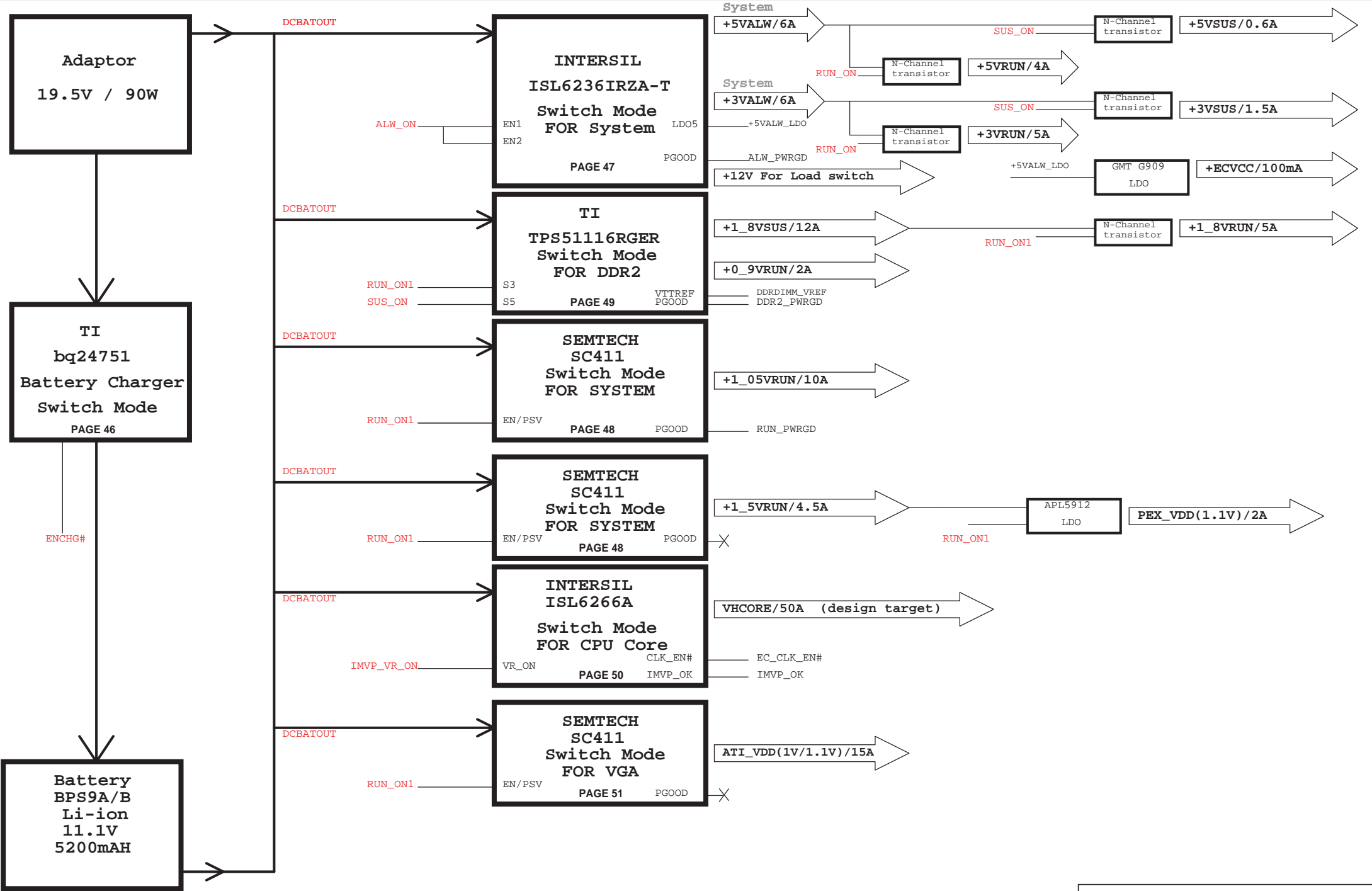
Place Thermal-Sensor near NB

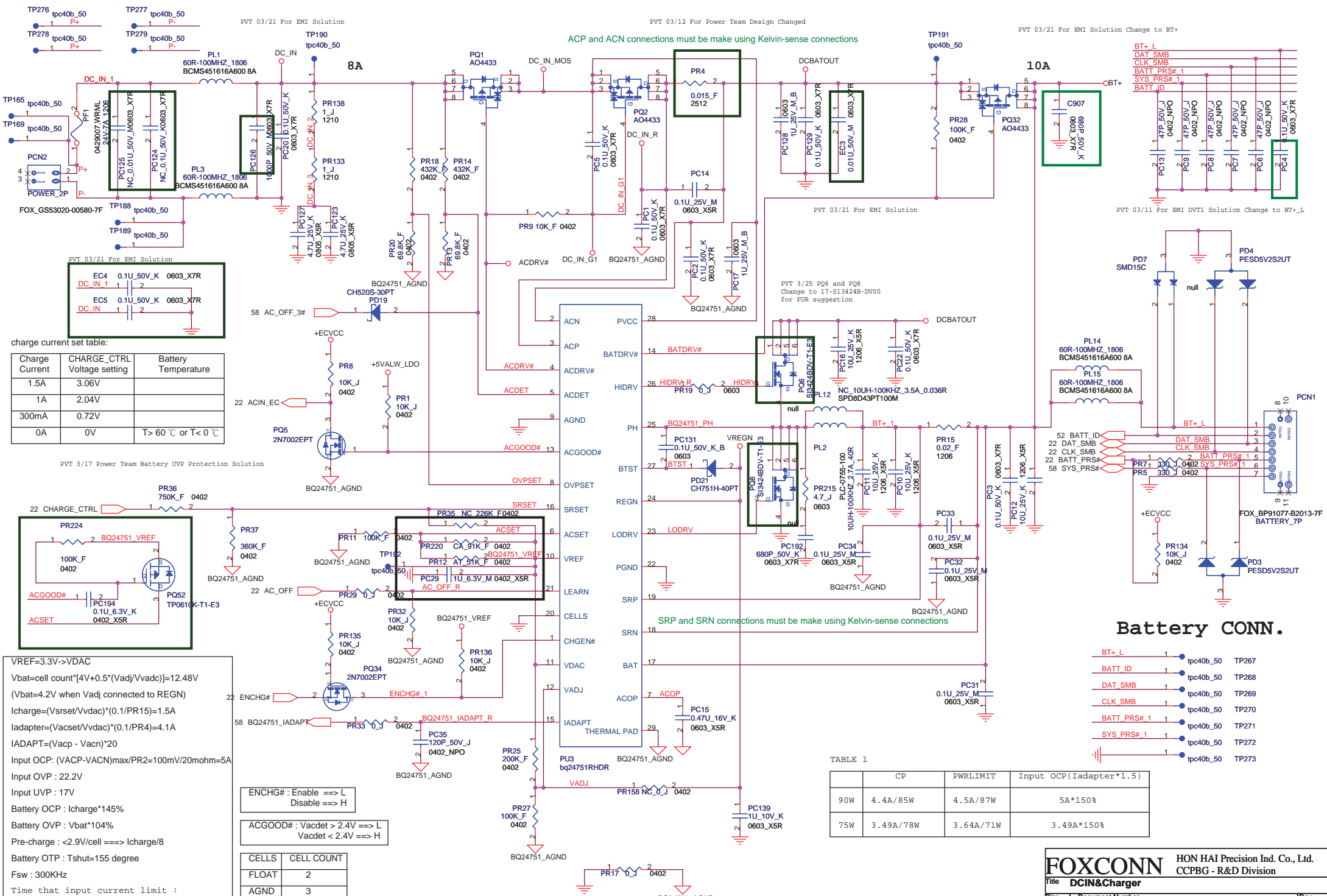
CPU/GMCH/DDR SENSOR EMC1402-2-ACZL



Place Thermal-Sensor near DDR







charge current set table:

Charge Current	CHARGE_CTRL Voltage setting	Battery Temperature
1.5A	3.06V	
1A	2.04V	
300mA	0.72V	
0A	0V	T > 60 °C or T < 0 °C

VREF=3.3V->VDAC
 $V_{bat} = \text{cell count} * [4V + 0.5 * (V_{adj} / V_{vdc})] = 12.48V$
 $(V_{bat} = 4.2V \text{ when } V_{adj} \text{ connected to } REGN)$
 $I_{charge} = (V_{rsset} / V_{vdc}) * (0.1 / PR15) = 1.5A$
 $I_{adapter} = (V_{acset} / V_{vdc}) * (0.1 / PR4) = 4.1A$
 $IADAPT = (V_{acp} - V_{vacn}) * 20$
 Input OCP: $(V_{acp} - V_{vacn})_{max} / PR2 = 100mV / 20m\Omega = 5A$
 Input OVP: 22.2V
 Input UVP: 17V
 Battery OCP: $I_{charge} * 145\%$
 Battery OVP: $V_{bat} * 104\%$
 Pre-charge: $< 2.9V / \text{cell} ==> I_{charge} / 8$
 Battery OTP: $T_{shut} = 155 \text{ degree}$
 $F_{sw} = 300KHz$
 Time that input current limit:
 $t = (C_{acop} * 2) / (18\mu A / V * (V_{PVCC} - ACN)) = 0.48s$

ENCHG# : Enable ==> L
 Disable ==> H

ACGOOD# : $V_{acdet} > 2.4V ==> L$
 $V_{acdet} < 2.4V ==> H$

CELLS	CELL COUNT
FLOAT	2
AGND	3
VREF	4

TABLE 1

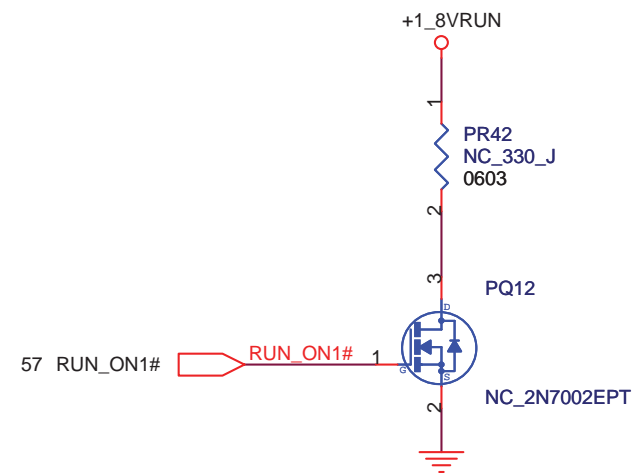
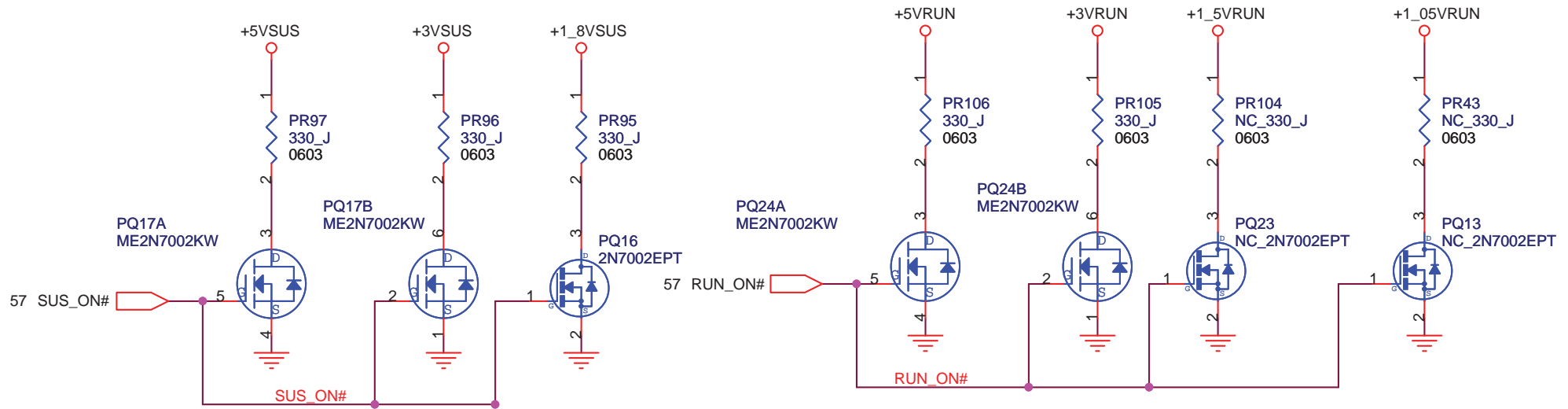
	CP	PWRLIMIT	Input OCP (Iadapter*1.5)
90W	4.4A/85W	4.5A/87W	5A*150%
75W	3.49A/78W	3.64A/71W	3.49A*150%

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 CCPBG - R&D Division

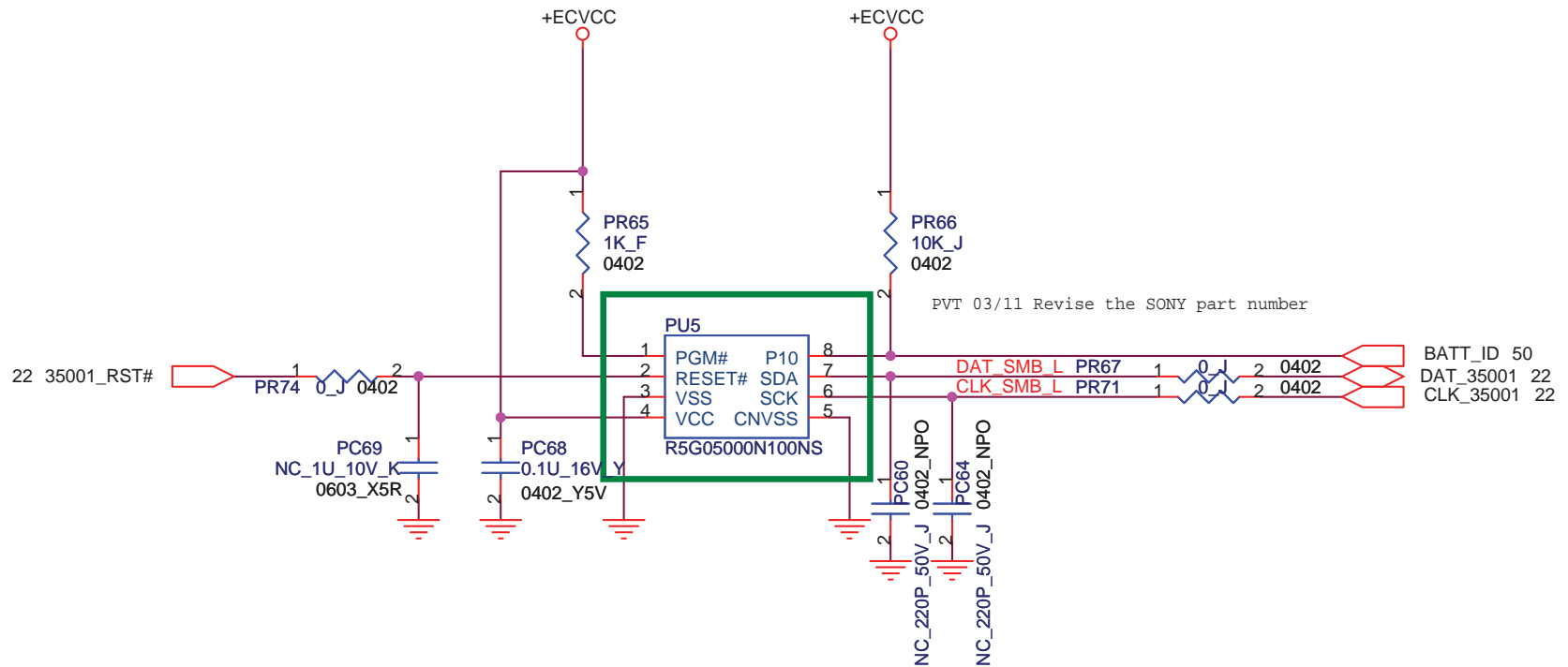
Title: **DCIN&Charger**

Size A3	Document Number M760	Rev 1.0
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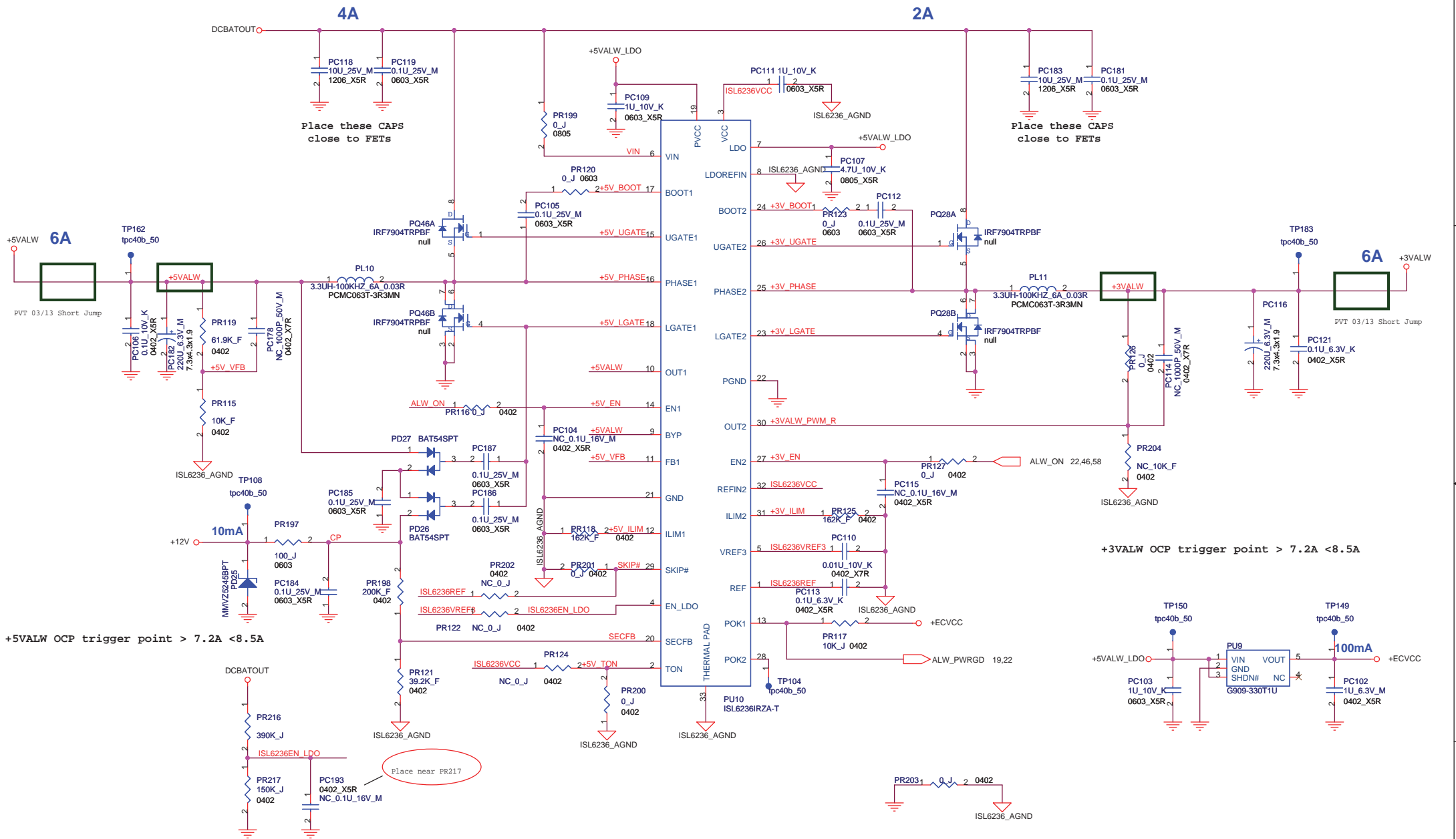
Date: Thursday, March 27, 2008 | Sheet 50 of 89



FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title DISCHARGE CIRCUIT			
Size A	Document Number M760	Rev 1.0	
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FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title			
Identify IC			
Size	Document Number		Rev
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+5VALW OCP trigger point > 7.2A < 8.5A

+3VALW OCP trigger point > 7.2A < 8.5A

TON	Operating Frequency (+5VALW/+3VALW)
VCC	200KHz/300KHz
REF (OPEN)	400KHz/300KHz
GND	400KHz/500KHz

SKIP#	Operating Mode
GND	Pulse-Skipping
REF	Ultrasonic-Skip
VCC	PWM

$$L = VOUT(VIN - VOUT) / (VIN * F * LIR * ILOAD(MAX))$$

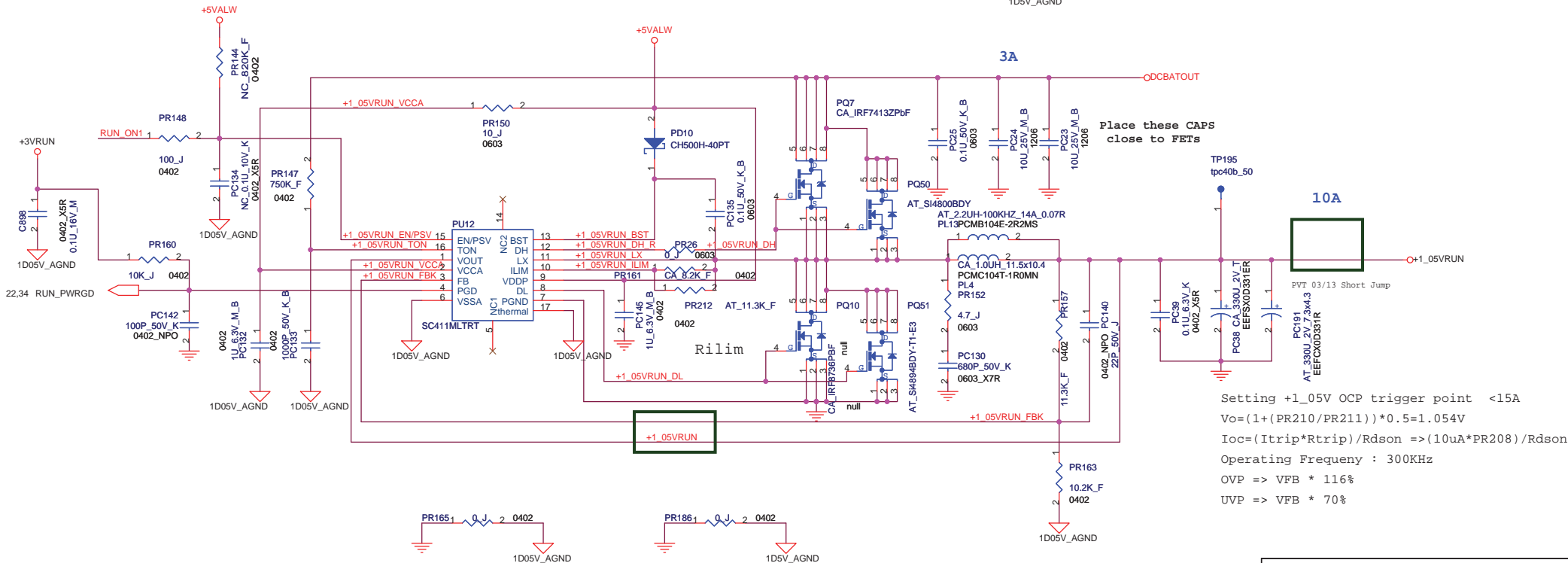
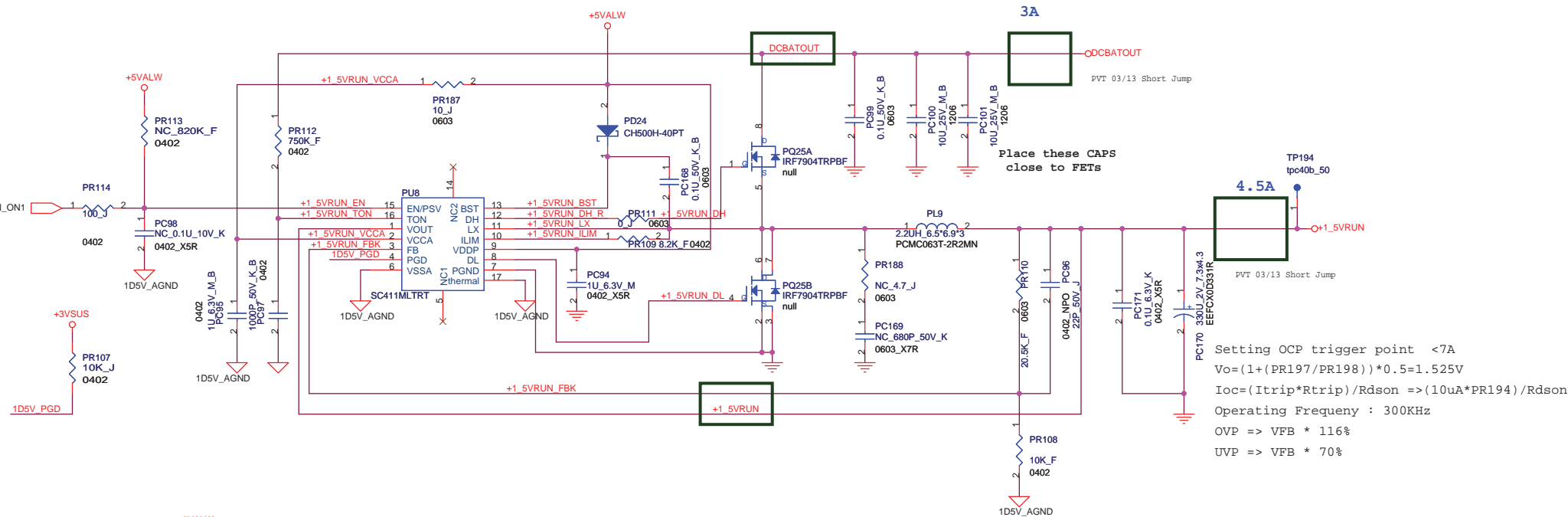
$$Rocp = (Iocp - Iripple/2) * (10 * Rds(on)) / 5u$$

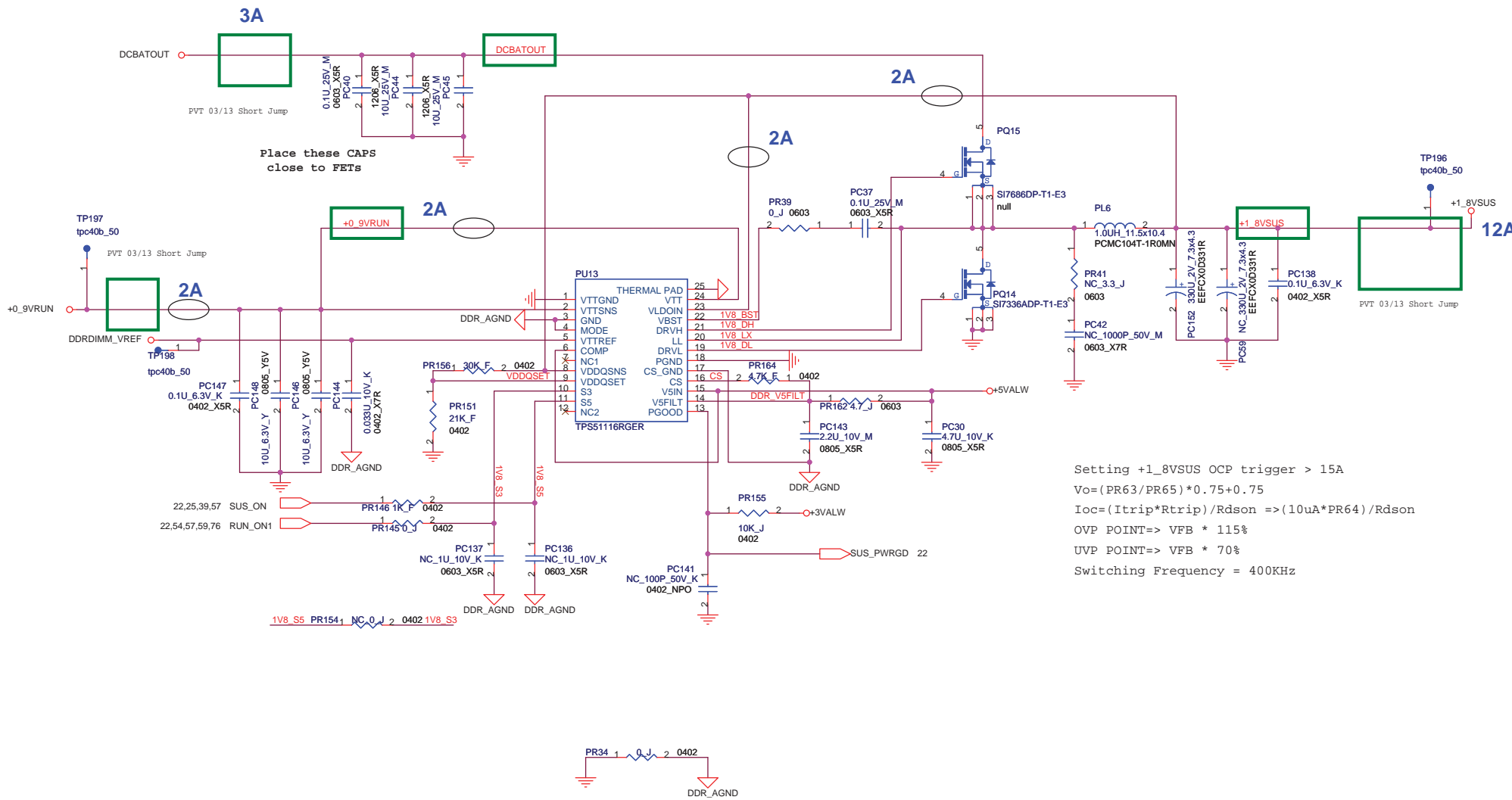
$$+5VALW = ((PR233 / PR235) + 1) * VFBI = 5.033V$$

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: **SYS Power (+3_3V/+5V)**

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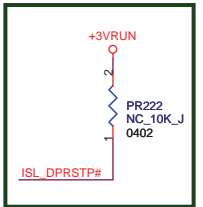




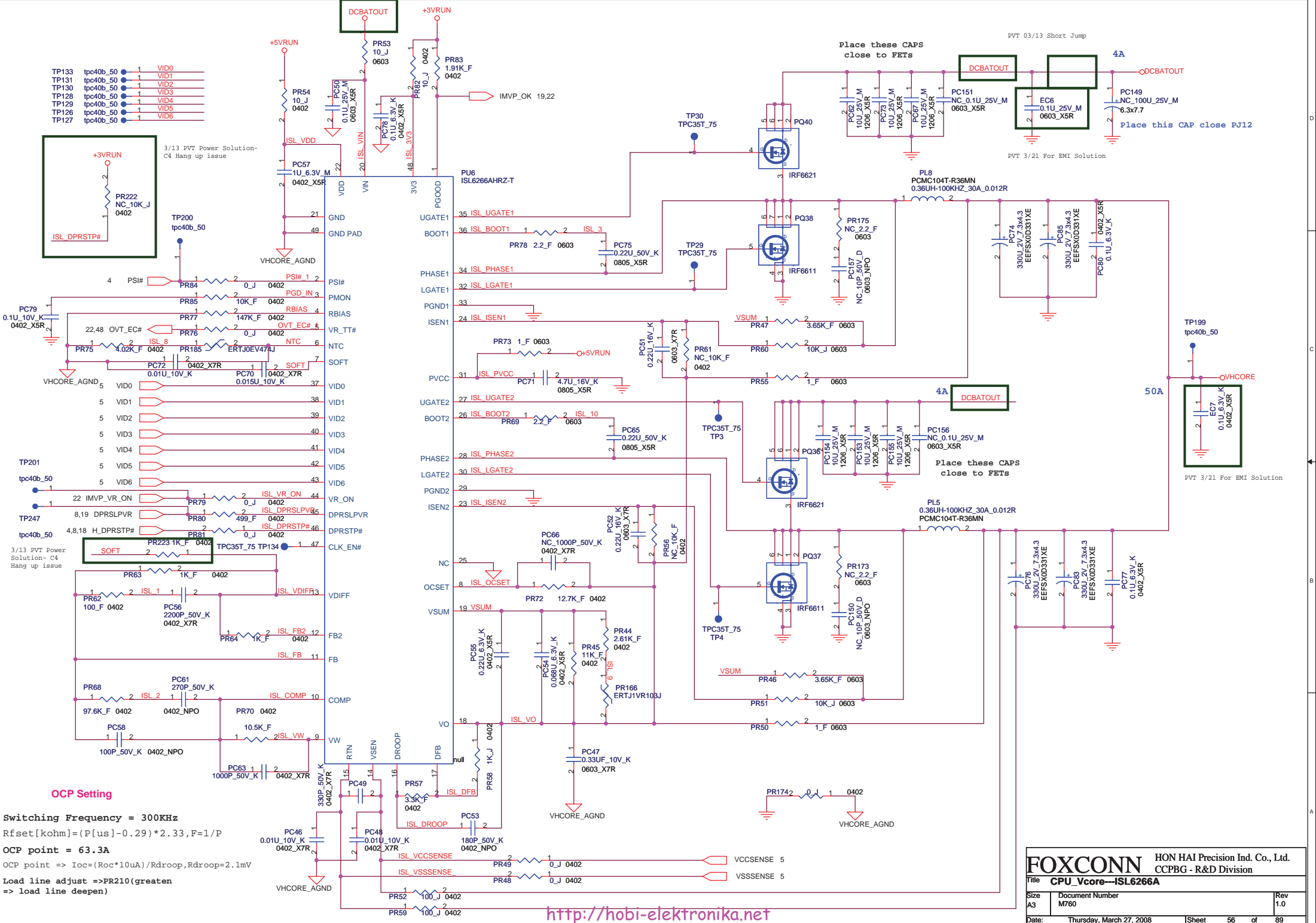
Setting +1.8VSUS OCP trigger > 15A
 $V_o = (PR63/PR65) * 0.75 + 0.75$
 $I_{oc} = (I_{trip} * R_{trip}) / R_{dson} => (10\mu A * PR64) / R_{dson}$
 OVP POINT=> VFB * 115%
 UVP POINT=> VFB * 70%
 Switching Frequency = 400KHz

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title DDR2 Power(+1.8V/+0.9V)			
Size A3	Document Number M760	Rev 1.0	
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- TP133 tpc40b_50 1 VID0
- TP131 tpc40b_50 1 VID1
- TP130 tpc40b_50 1 VID2
- TP128 tpc40b_50 1 VID3
- TP129 tpc40b_50 1 VID4
- TP126 tpc40b_50 1 VID5
- TP127 tpc40b_50 1 VID6



3/13 PVT Power Solution- C4 Hang up issue

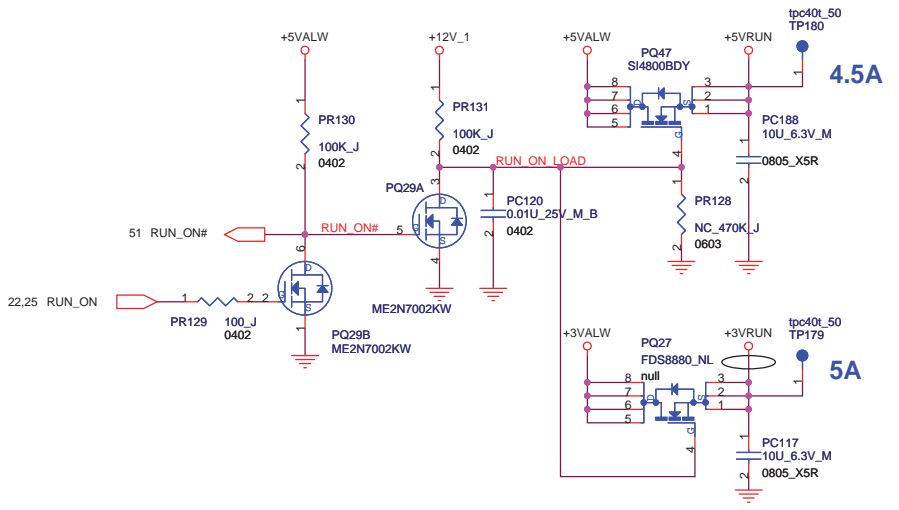
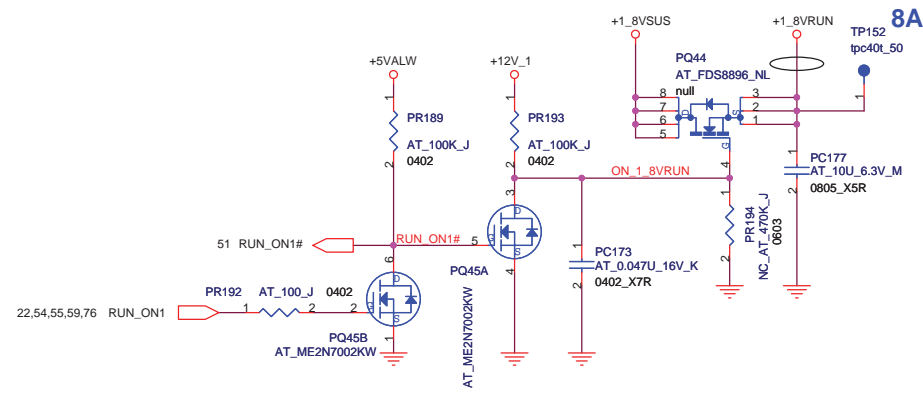
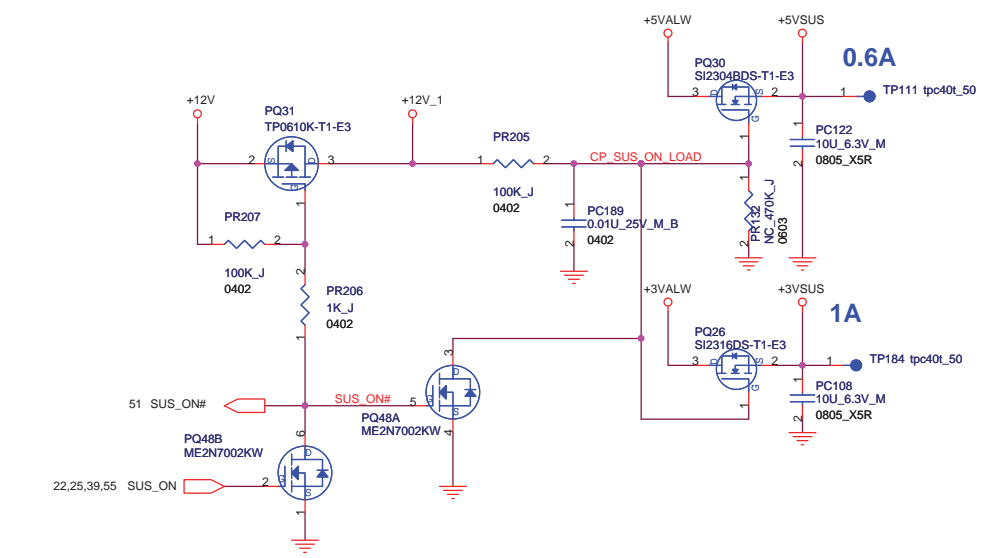


OCP Setting

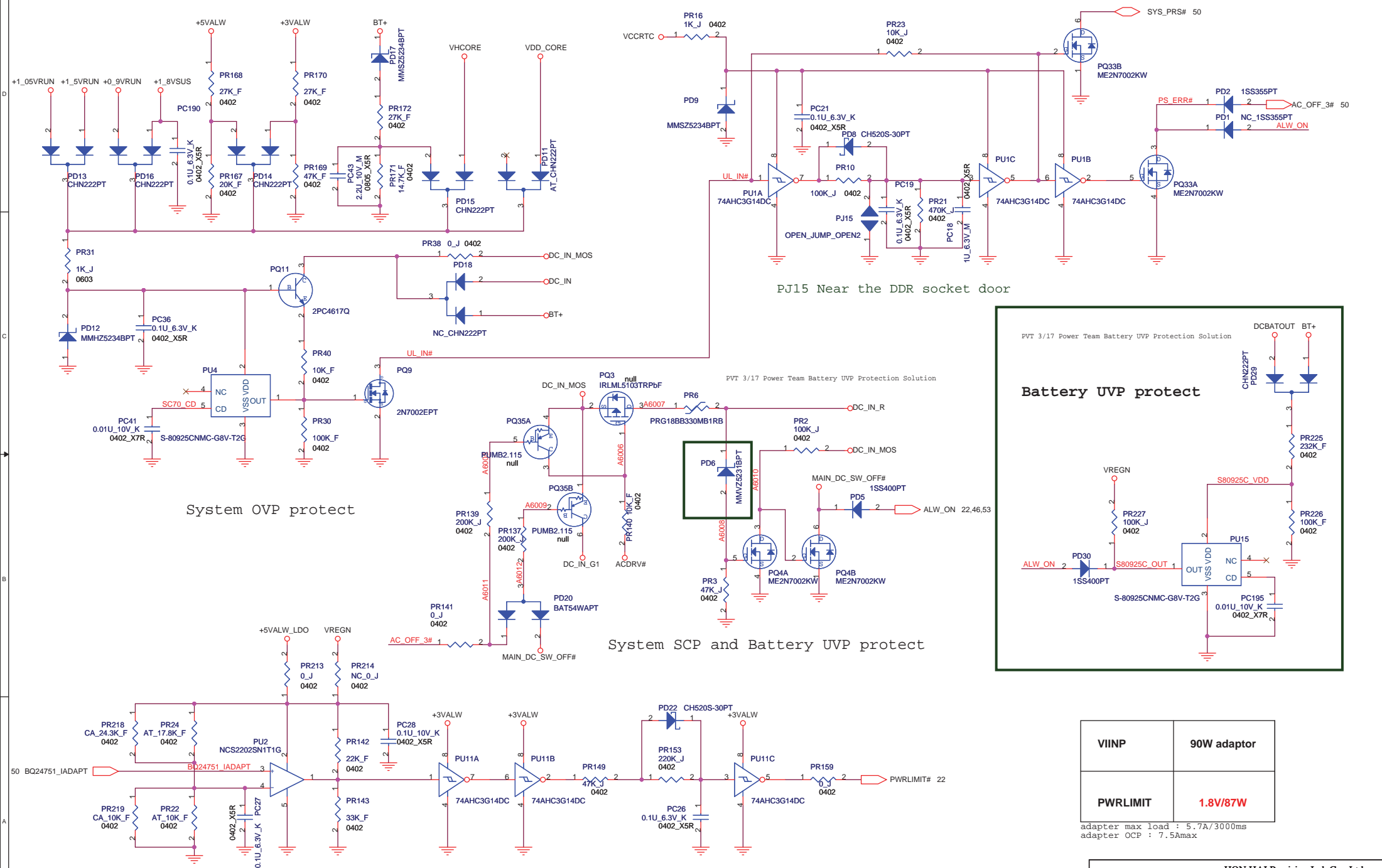
Switching Frequency = 300KHz
 $Rfset[kohm] = (P[us] - 0.29) * 2.33, F=1/P$
 OCP point = 63.3A
 OCP point => $Ioc = (Roc * 10uA) / Rdroop, Rdroop = 2.1mV$
 Load line adjust => PR210 (greaten)
 => load line deepen)

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FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title CPU_Vcore-ISL6266A		CCPBG - R&D Division	
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FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title Others power plan		CCPBG - R&D Division	
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System OVP protect

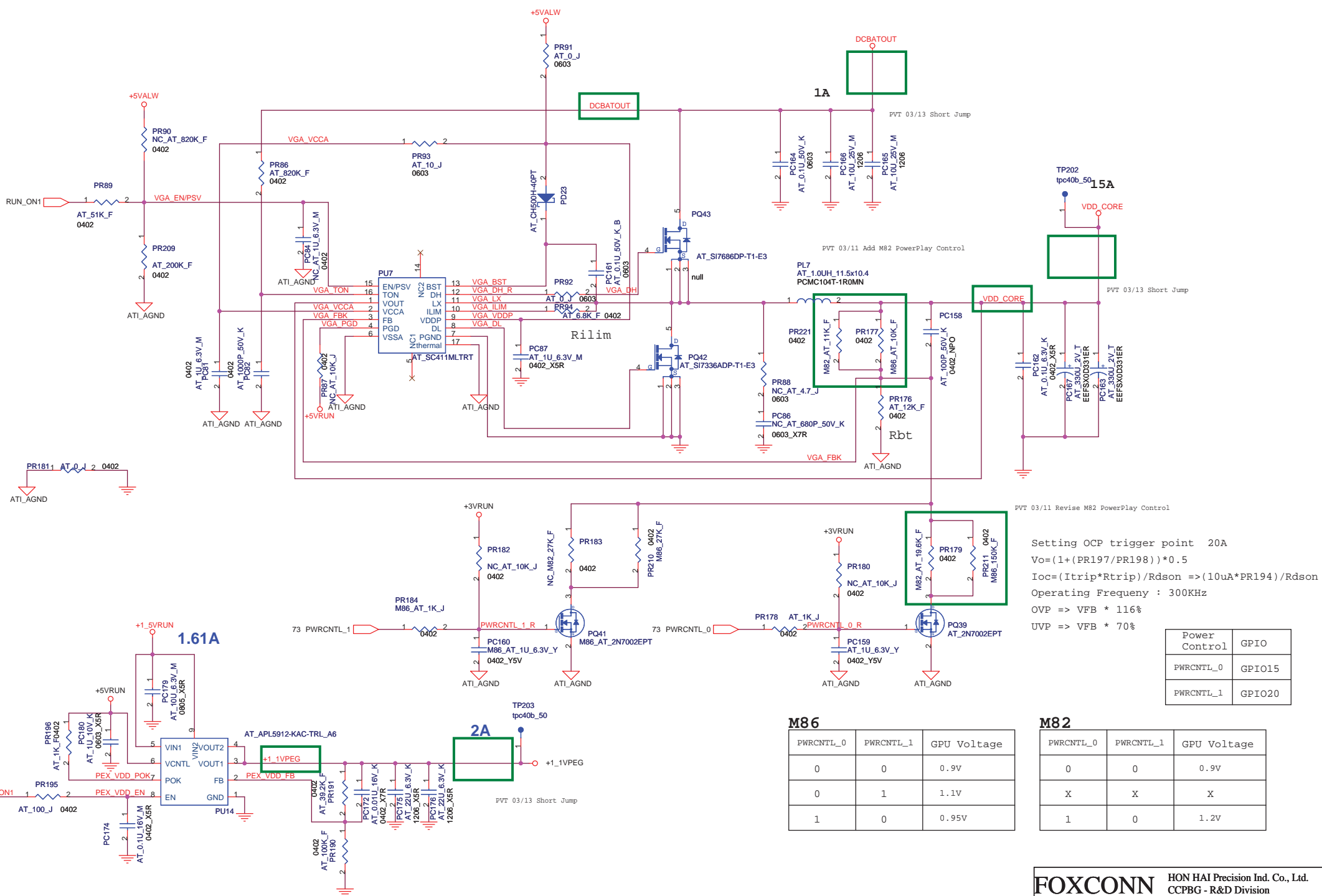
System SCP and Battery UVP protect

Battery UVP protect

PWRLIMIT Protect

VIINP	90W adaptor
PWRLIMIT	1.8V/87W

adapter max load : 5.7A/3000ms
 adapter OCP : 7.5Amax



PVT 03/11 Revise M82 PowerPlay Control

Setting OCP trigger point 20A
 $V_o = (1 + (PR197/PR198)) * 0.5$
 $I_{oc} = (I_{trip} * R_{trip}) / R_{dson} \Rightarrow (10\mu A * PR194) / R_{dson}$
 Operating Frequency : 300KHz
 OVP => VFB * 116%
 UVP => VFB * 70%

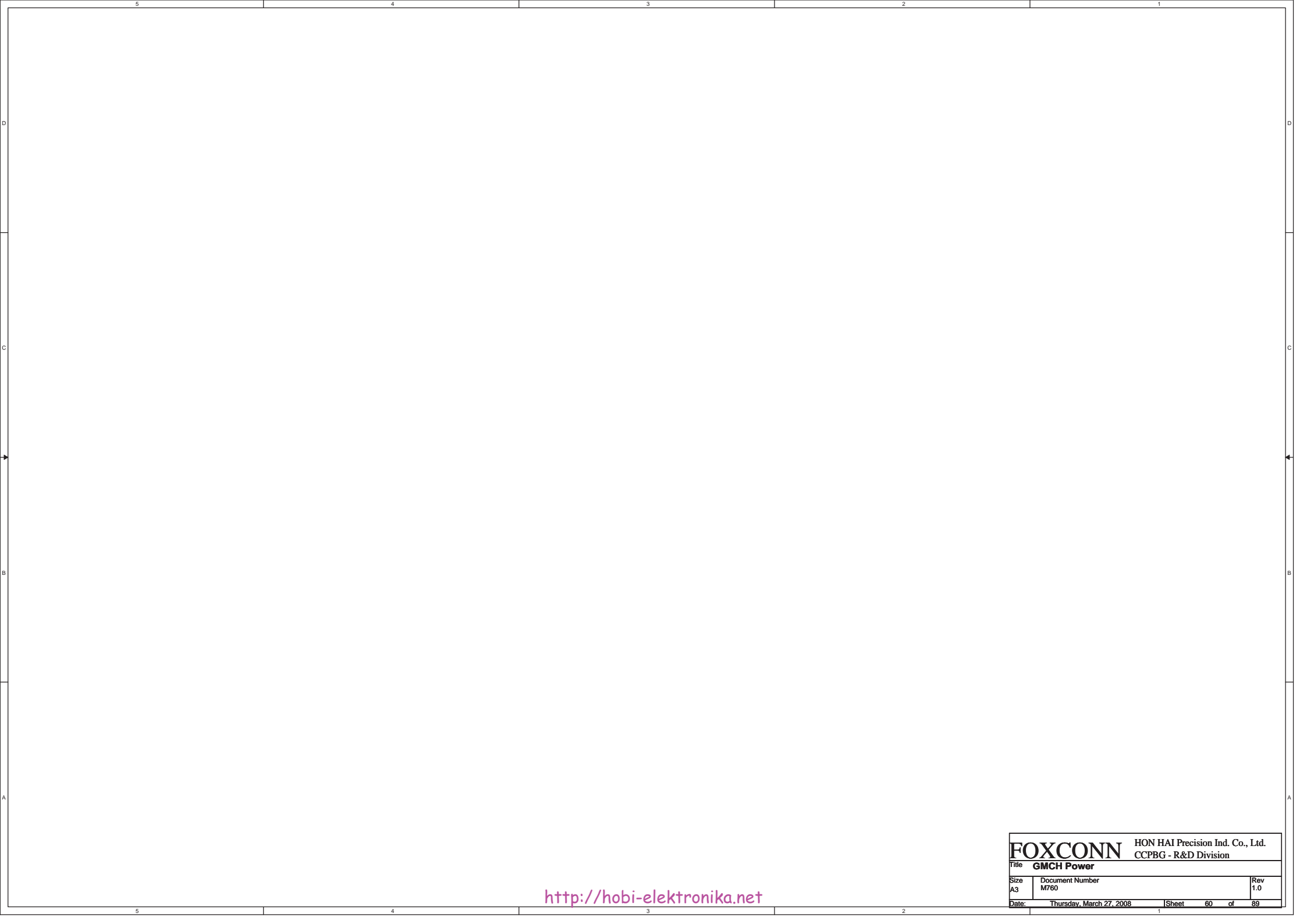
Power Control	GPIO
PWRCNTL_0	GPIO15
PWRCNTL_1	GPIO20

M86

PWRCNTL_0	PWRCNTL_1	GPU Voltage
0	0	0.9V
0	1	1.1V
1	0	0.95V

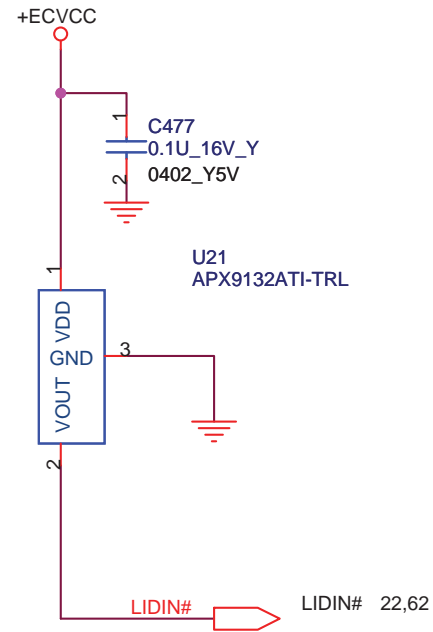
M82

PWRCNTL_0	PWRCNTL_1	GPU Voltage
0	0	0.9V
X	X	X
1	0	1.2V



<http://hobi-elektronika.net>

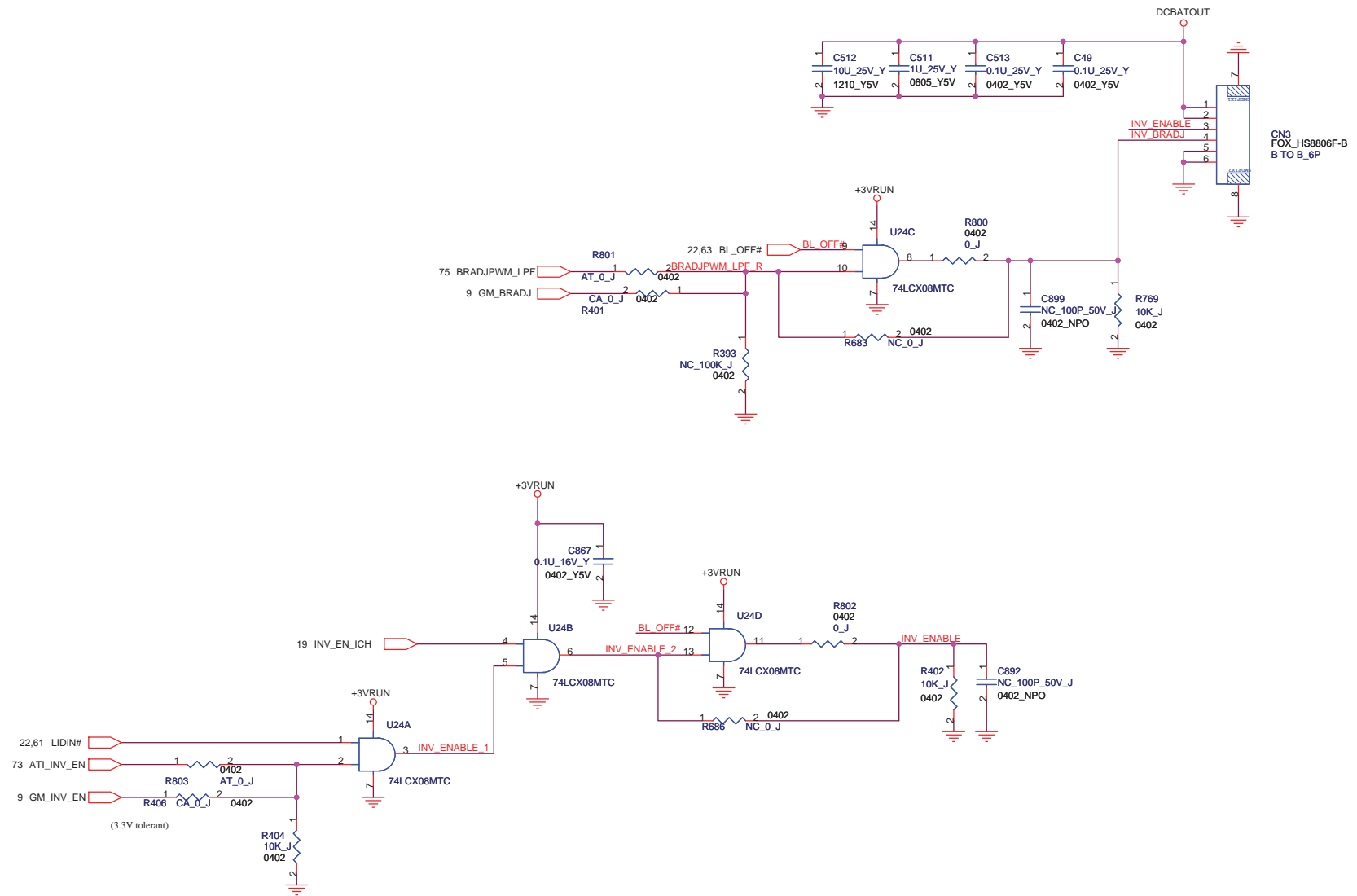
FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
Title GMCH Power		
Size A3	Document Number M760	Rev 1.0
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LID Switch

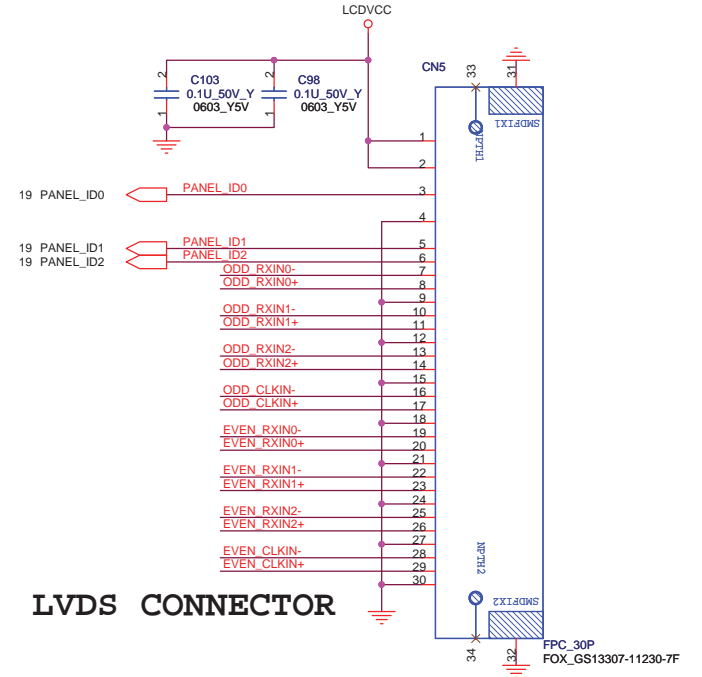
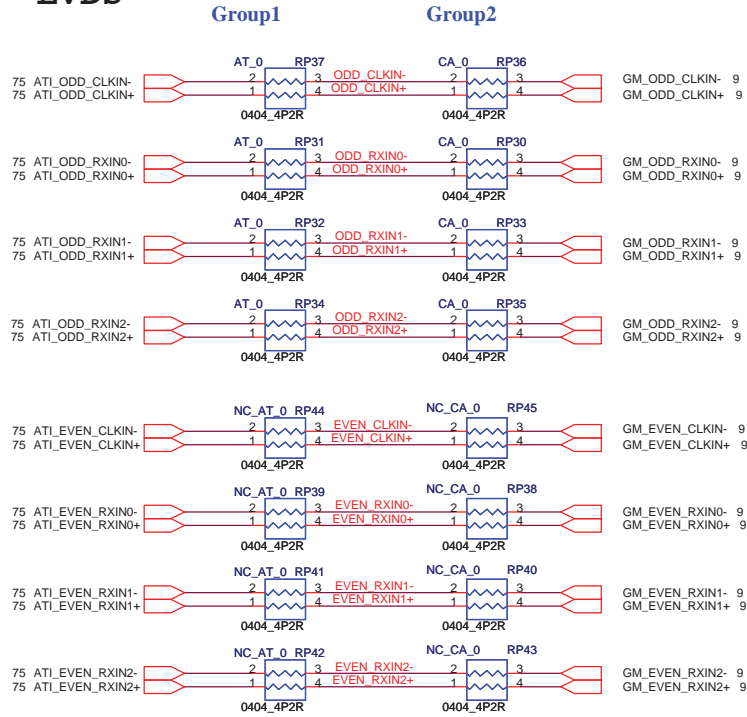
FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title LID SWITCH			
Size A	Document Number M760	Rev 1.0	
Date:	Thursday, March 27, 2008	Sheet	61 of 89

INVERTER CONN.

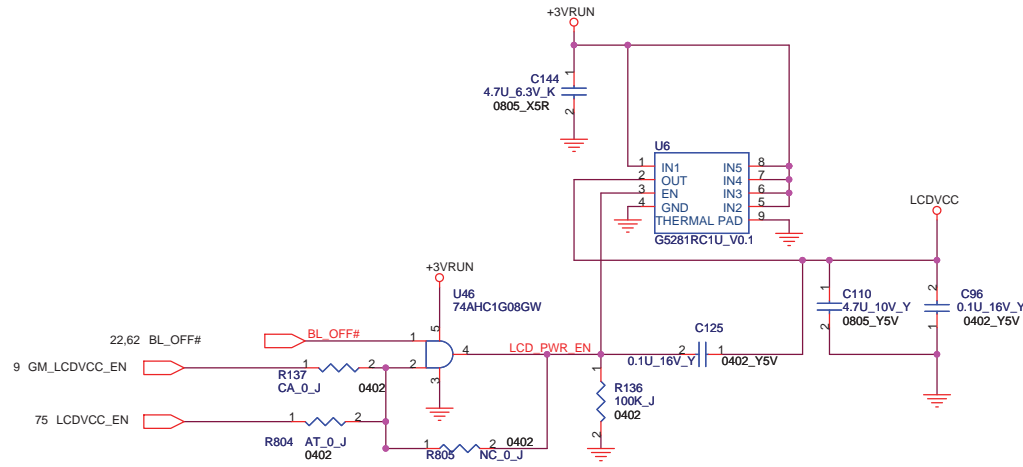


Group1, Group2 should be close

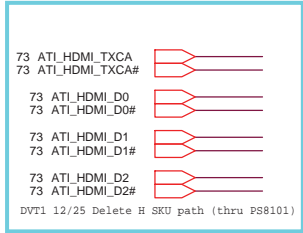
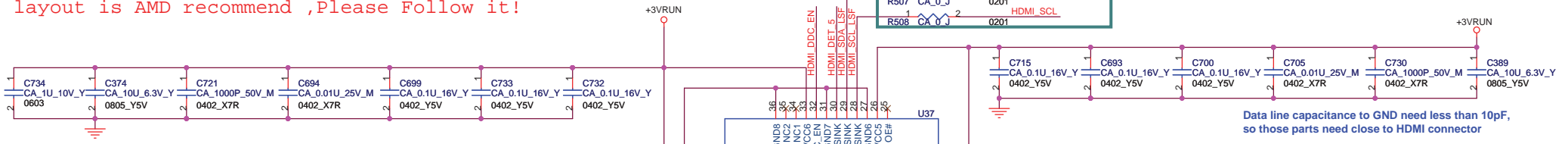
LVDS



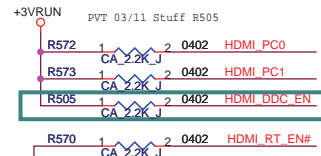
LVDS CONNECTOR



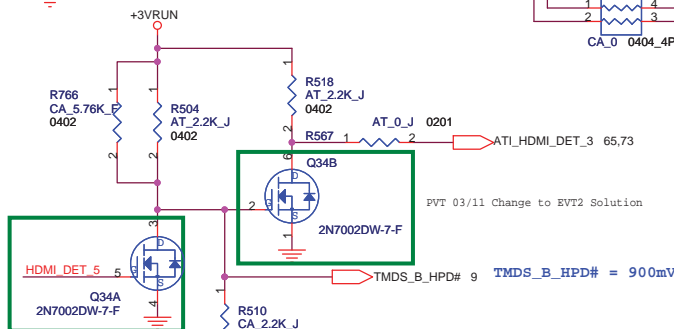
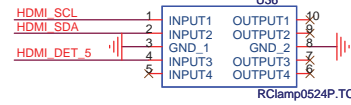
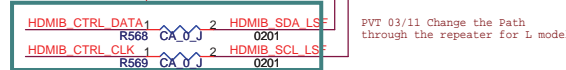
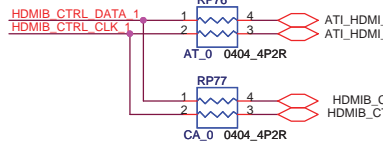
This layout is AMD recommend ,Please Follow it!



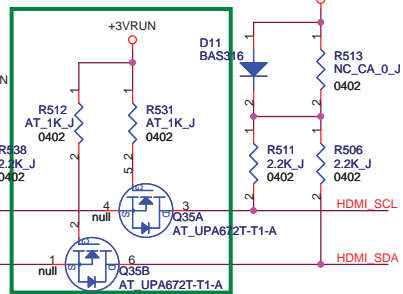
(TMDS inputs equalization control)
PC1,PC0 Configuration
00: 8 dB,
01: 4 dB,
10: 12 dB,
11: 0 dB



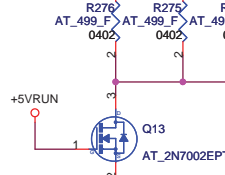
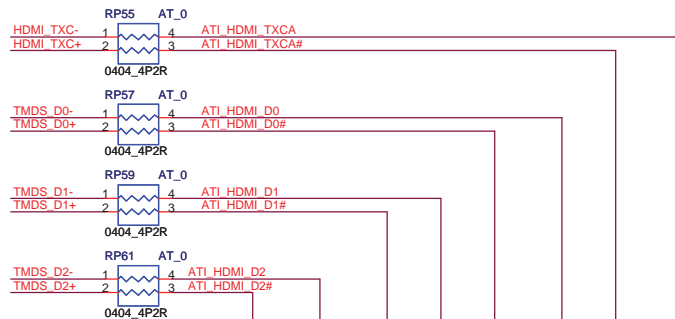
ByPass PS8101



PVT 03/11 Change to EVT2 Solution



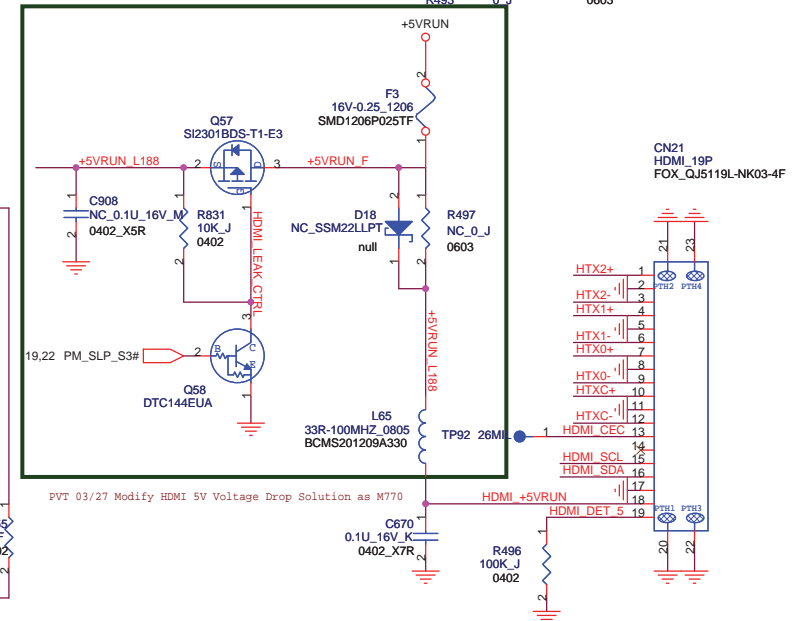
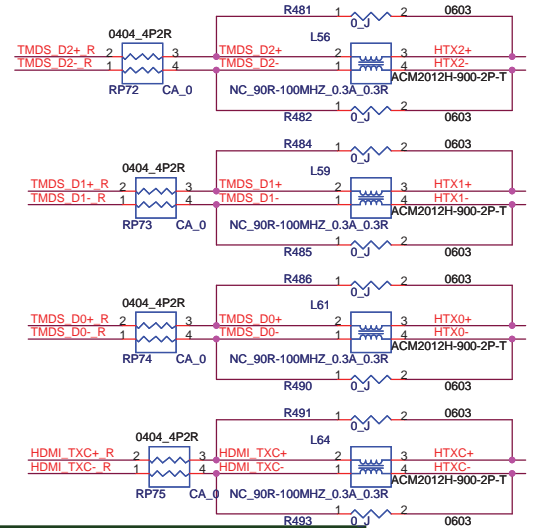
PVT 03/11 Change the Path through the repeater for L model



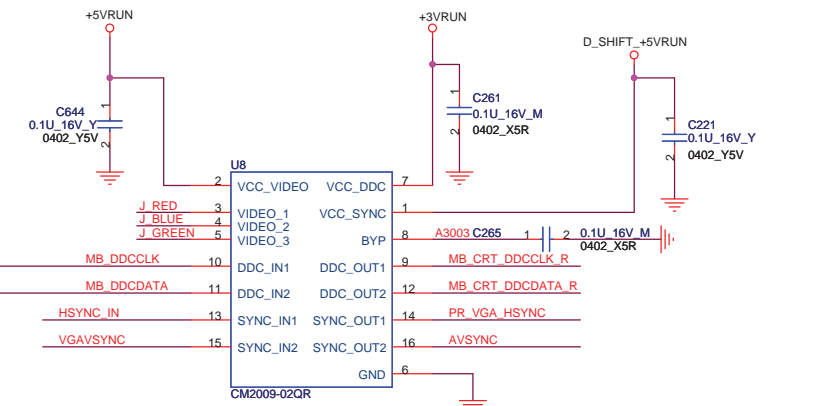
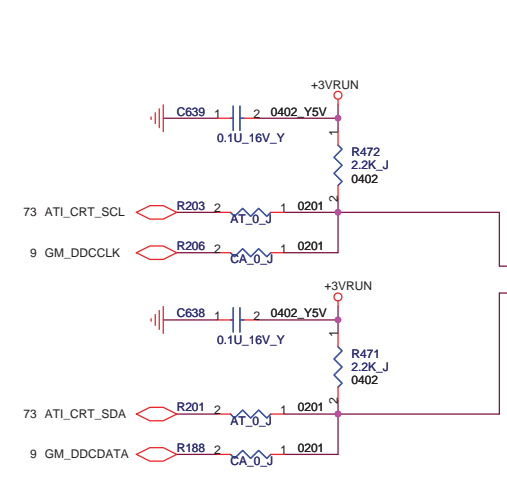
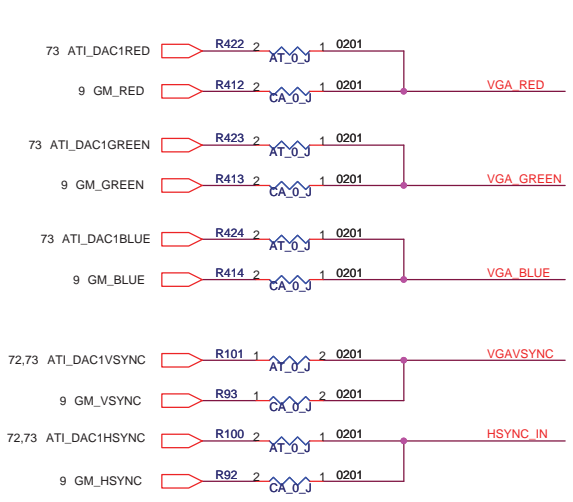
PVT 03/11 Change the Path through the repeater for L model



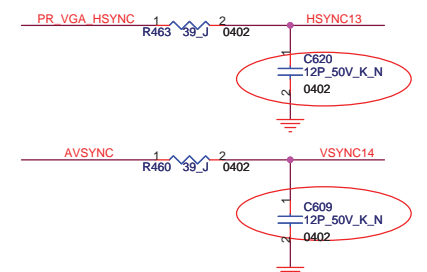
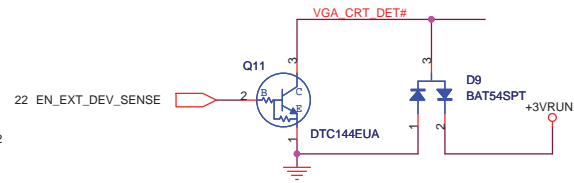
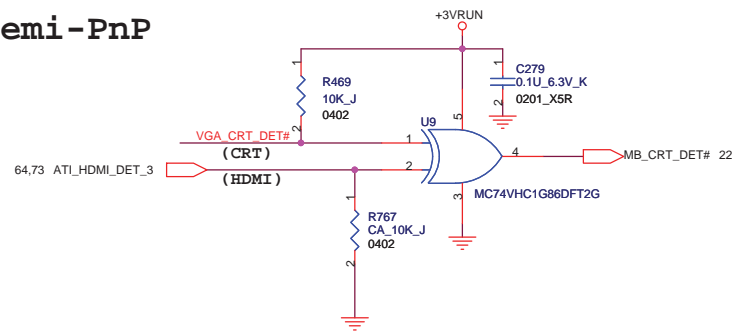
Data line capacitance to GND need less than 10pF, so those parts need close to HDMI connector



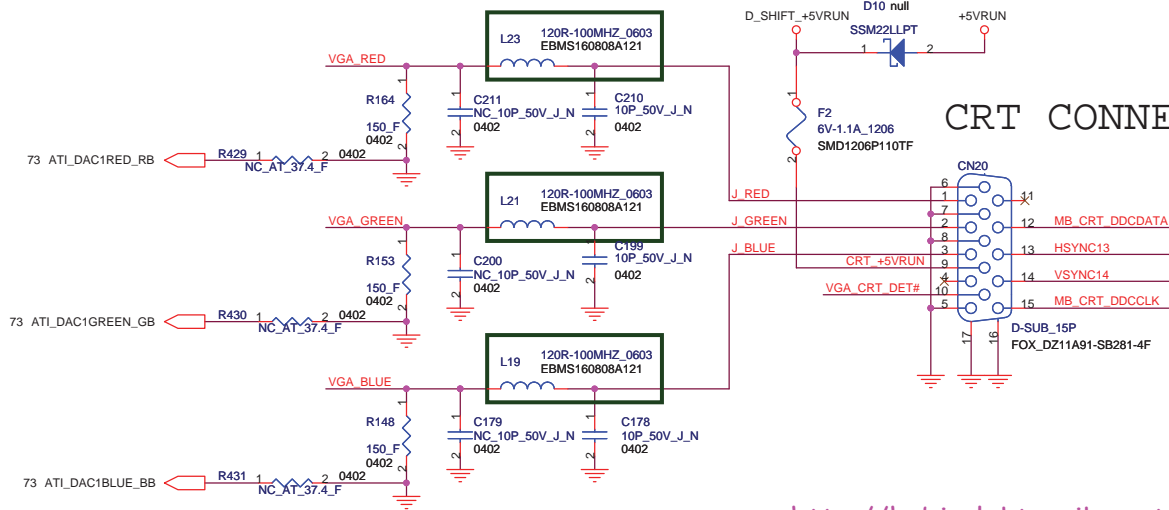
PVT 03/27 Modify HDMI 5V Voltage Drop Solution as M770



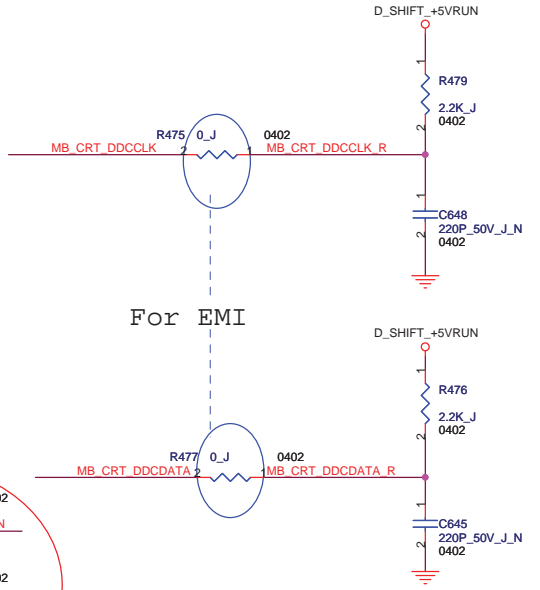
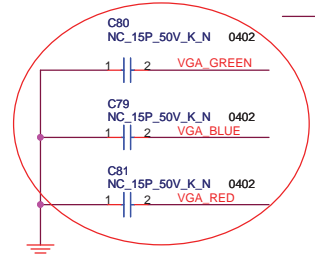
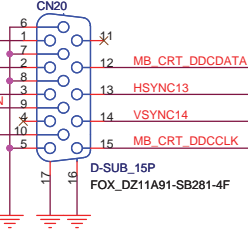
Semi-PnP



PVT 3/21 EMI Request

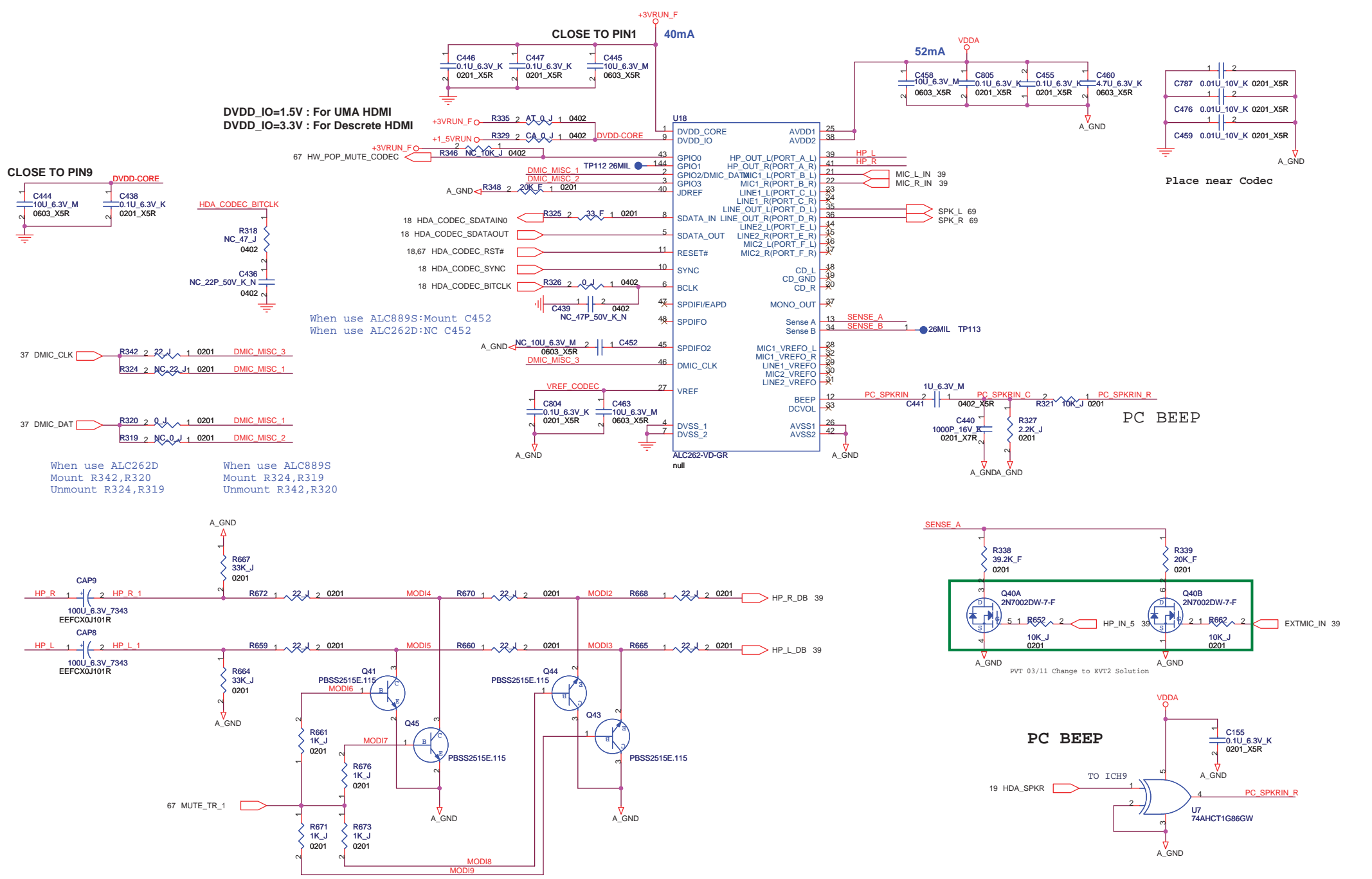


CRT CONNECTOR



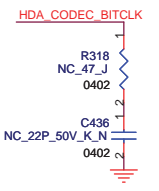
For EMI

FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	CRT	
Size	Document Number	Rev
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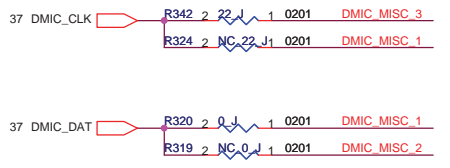


DVDD_IO=1.5V : For UMA HDMI
 DVDD_IO=3.3V : For Descrete HDMI

CLOSE TO PIN9

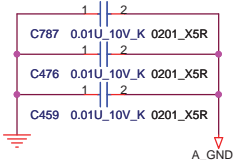
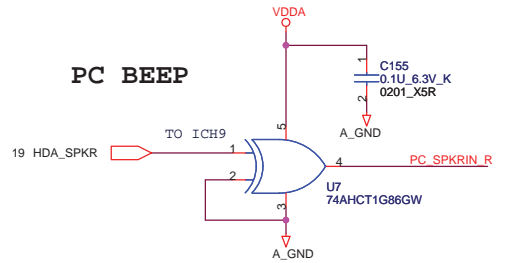
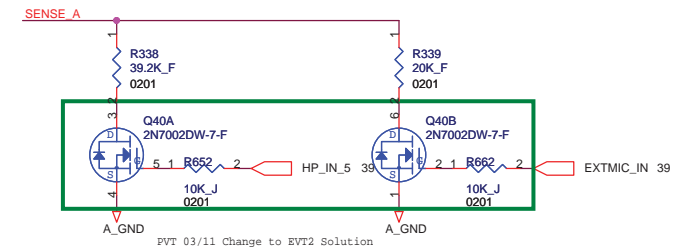
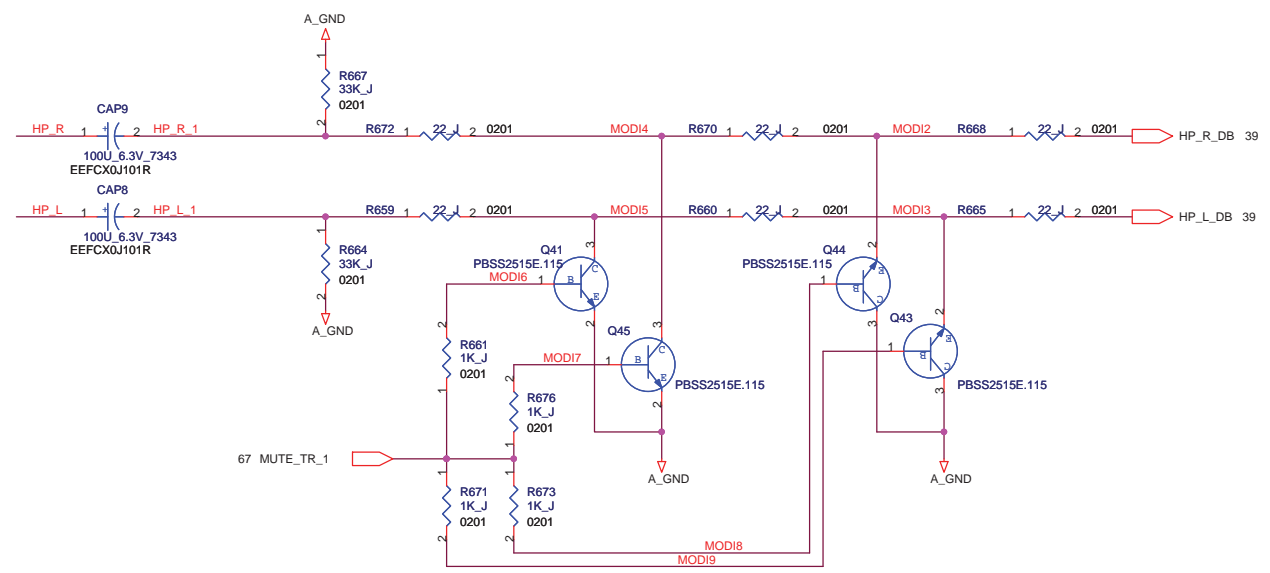


When use ALC889S:Mount C452
 When use ALC262D:NC C452



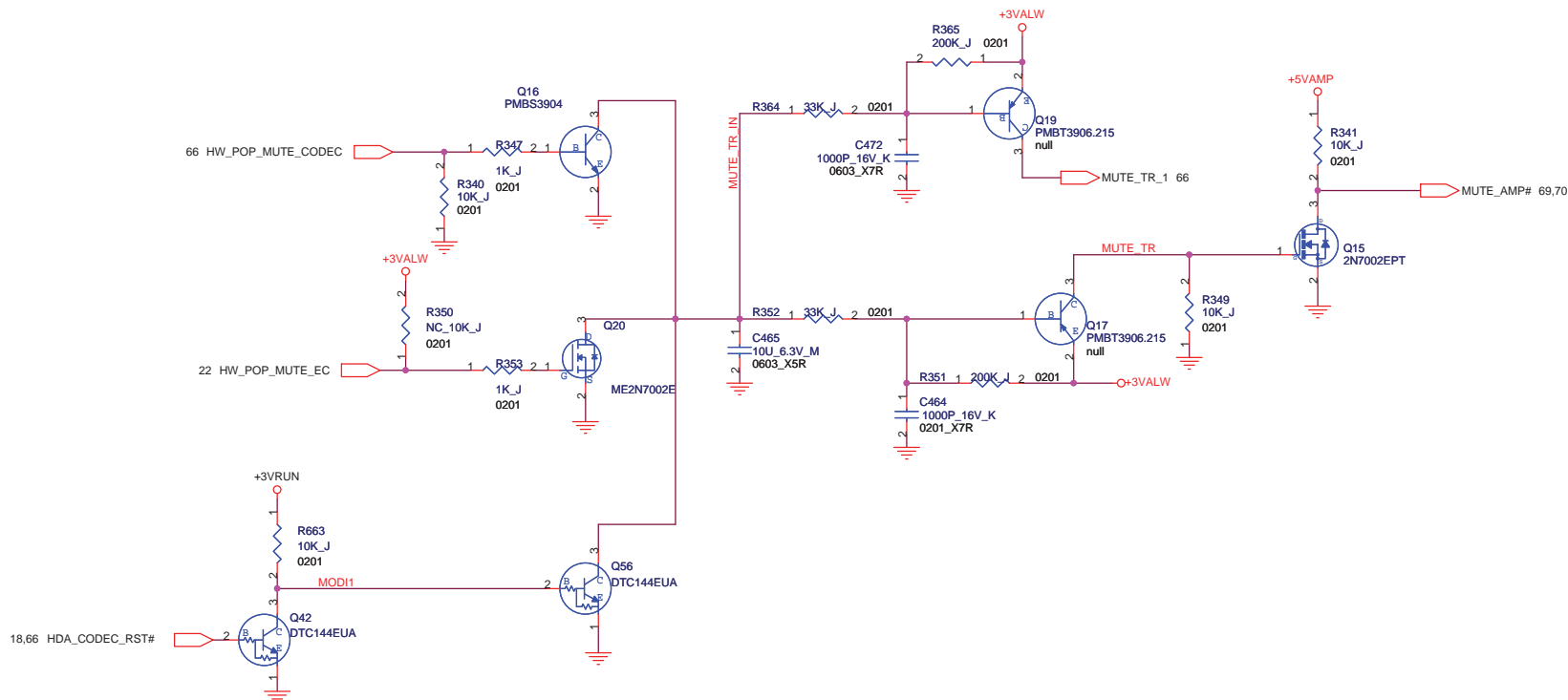
When use ALC262D
 Mount R342, R320
 Unmount R324, R319

When use ALC889S
 Mount R324, R319
 Unmount R342, R320

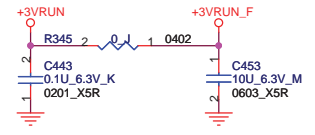
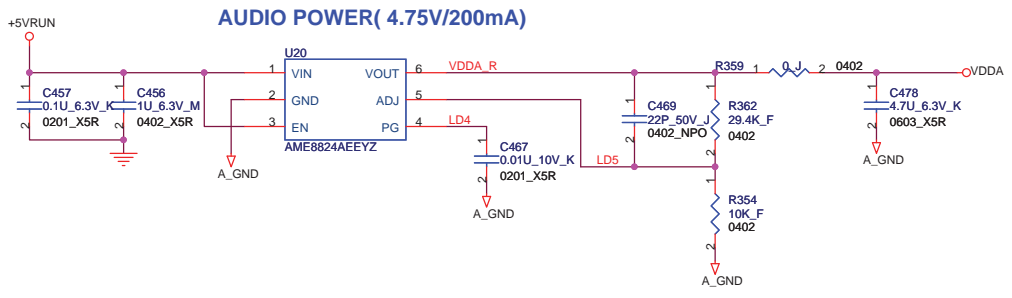


Place near Codec

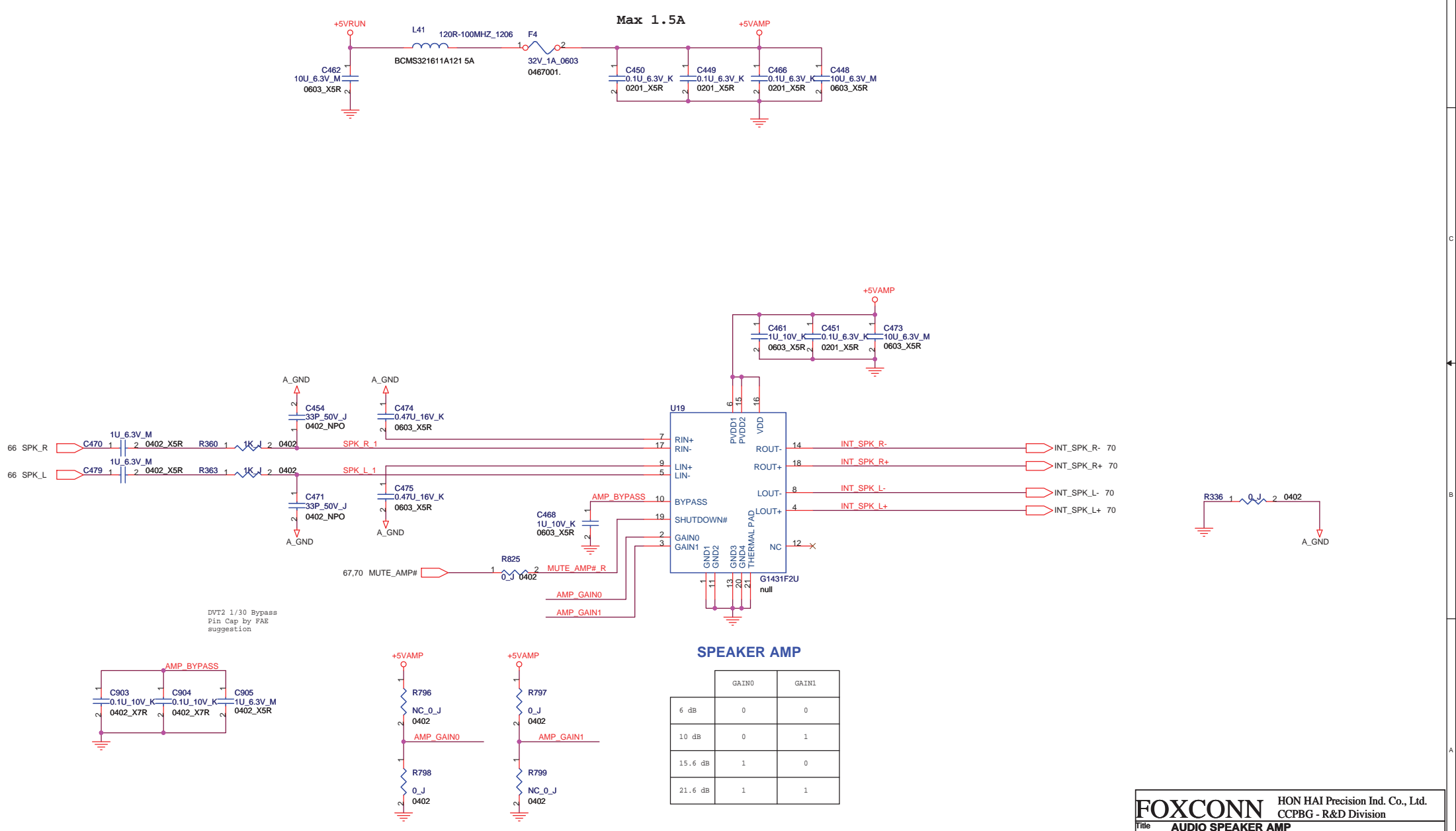
FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title AUDIO(CODEC)		CCPBG - R&D Division	
Size A3	Document Number M760	Rev 1.0	
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Q42 for 1.5V power level



FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
Title AUDIO POWER		
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DVT2 1/30 Bypass
Pin Cap by FAB
suggestion

SPEAKER AMP

	GAIN0	GAIN1
6 db	0	0
10 db	0	1
15.6 db	1	0
21.6 db	1	1

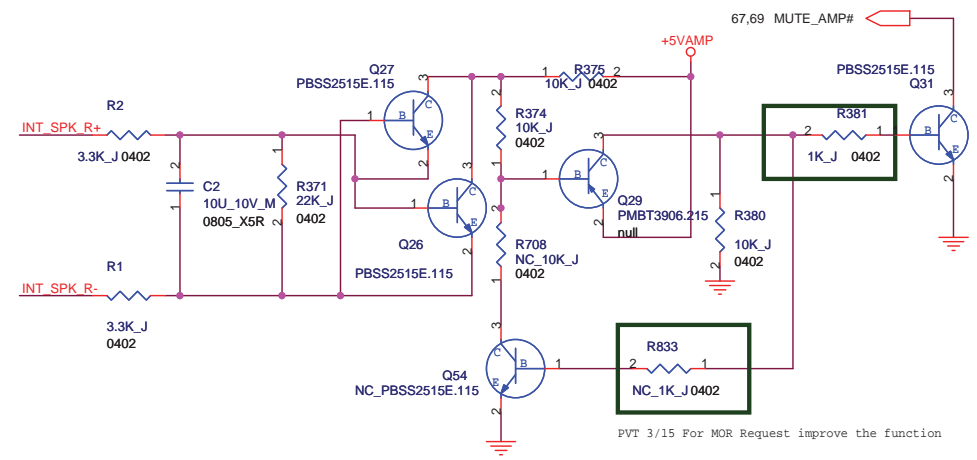
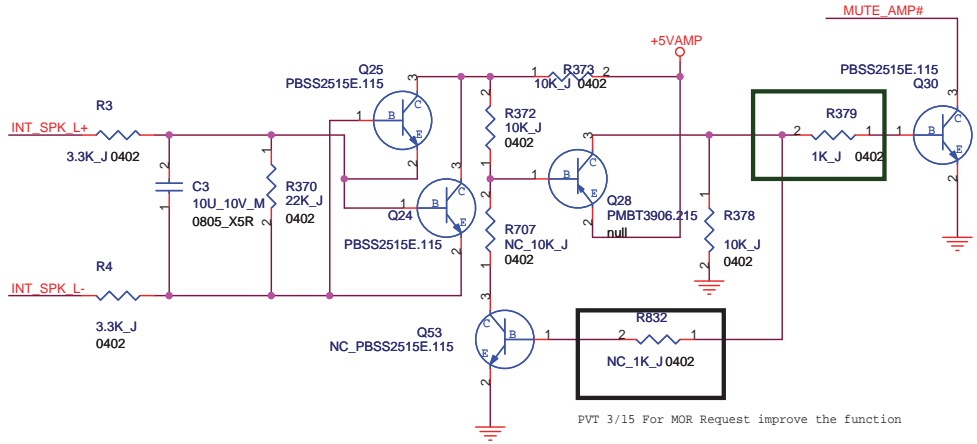
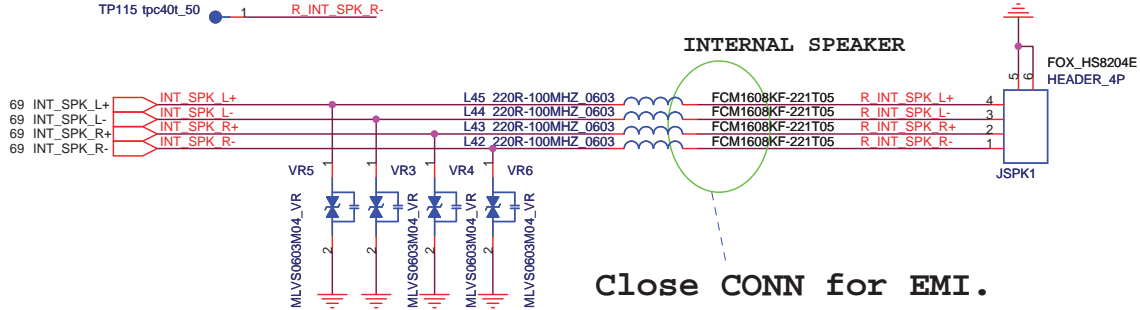
FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: **AUDIO SPEAKER AMP**

Size A3 Document Number M760 Rev 1.0



Date: Thursday, March 27, 2008 Sheet 69 of 89

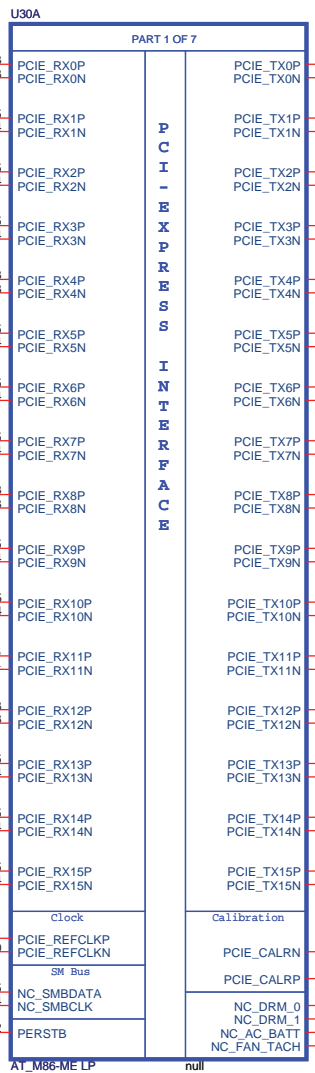
- TP114 tpc40L_50 ● 1 R_INT_SPK L+
- TP117 tpc40L_50 ● 1 R_INT_SPK L-
- TP116 tpc40L_50 ● 1 R_INT_SPK R+
- TP115 tpc40L_50 ● 1 R_INT_SPK R-



For Mor request, add the speaker cable short protection circuit

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title		AUDIO SPEAKER CONNECTOR	
Size	Document Number	Rev	
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9 PEG_RXP_C[15..0] 
 9 PEG_RXN_C[15..0] 



TXN0	1	2	AT_0.1U_6.3V_K	0201_X5R	PEG_RXN0
TXN1	1	2	AT_0.1U_6.3V_K	0201_X5R	PEG_RXN1
TXN2	1	2	AT_0.1U_6.3V_K	0201_X5R	PEG_RXN2
TXN3	1	2	AT_0.1U_6.3V_K	0201_X5R	PEG_RXN3
TXN4	1	2	AT_0.1U_6.3V_K	0201_X5R	PEG_RXN4
TXN5	1	2	AT_0.1U_6.3V_K	0201_X5R	PEG_RXN5
TXN6	1	2	AT_0.1U_6.3V_K	0201_X5R	PEG_RXN6
TXN7	1	2	AT_0.1U_6.3V_K	0201_X5R	PEG_RXN7
TXN8	1	2	AT_0.1U_6.3V_K	0201_X5R	PEG_RXN8
TXN9	1	2	AT_0.1U_6.3V_K	0201_X5R	PEG_RXN9
TXN10	1	2	AT_0.1U_6.3V_K	0201_X5R	PEG_RXN10
TXN11	1	2	AT_0.1U_6.3V_K	0201_X5R	PEG_RXN11
TXN12	1	2	AT_0.1U_6.3V_K	0201_X5R	PEG_RXN12
TXN13	1	2	AT_0.1U_6.3V_K	0201_X5R	PEG_RXN13
TXN14	1	2	AT_0.1U_6.3V_K	0201_X5R	PEG_RXN14
TXN15	1	2	AT_0.1U_6.3V_K	0201_X5R	PEG_RXN15

TXP0	1	2	AT_0.1U_6.3V_K	0201_X5R	PEG_RXP0
TXP1	1	2	AT_0.1U_6.3V_K	0201_X5R	PEG_RXP1
TXP2	1	2	AT_0.1U_6.3V_K	0201_X5R	PEG_RXP2
TXP3	1	2	AT_0.1U_6.3V_K	0201_X5R	PEG_RXP3
TXP4	1	2	AT_0.1U_6.3V_K	0201_X5R	PEG_RXP4
TXP5	1	2	AT_0.1U_6.3V_K	0201_X5R	PEG_RXP5
TXP6	1	2	AT_0.1U_6.3V_K	0201_X5R	PEG_RXP6
TXP7	1	2	AT_0.1U_6.3V_K	0201_X5R	PEG_RXP7
TXP8	1	2	AT_0.1U_6.3V_K	0201_X5R	PEG_RXP8
TXP9	1	2	AT_0.1U_6.3V_K	0201_X5R	PEG_RXP9
TXP10	1	2	AT_0.1U_6.3V_K	0201_X5R	PEG_RXP10
TXP11	1	2	AT_0.1U_6.3V_K	0201_X5R	PEG_RXP11
TXP12	1	2	AT_0.1U_6.3V_K	0201_X5R	PEG_RXP12
TXP13	1	2	AT_0.1U_6.3V_K	0201_X5R	PEG_RXP13
TXP14	1	2	AT_0.1U_6.3V_K	0201_X5R	PEG_RXP14
TXP15	1	2	AT_0.1U_6.3V_K	0201_X5R	PEG_RXP15

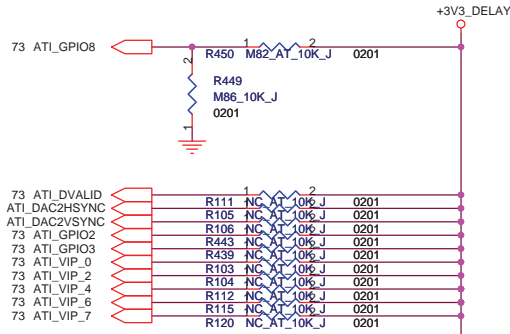
6 CLK_PCIE_PEG 
 6 CLK_PCIE_PEG# 

8,17,22,24,25,26,27,28,29 PLT_RST# 

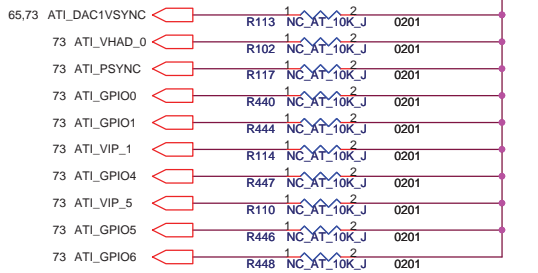
PCIE_VDDC

FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title VGA (PCI EXPRESS) 1 OF 6		
Size A3	Document Number M760	Rev 1.0
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R450 for M82 only
 1 ENABLE HD AUDIO
 0 DISABLE HD AUDIO



Internal use only. Other logic must not affect this signal during RESET.



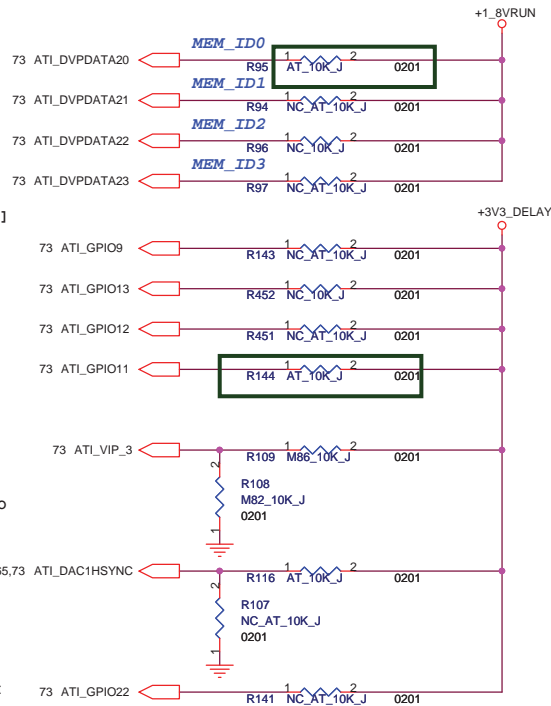
Strap for GDDR3-136ball
 AT1_DVPDATA[23 : 20]

- 0001 16Mx32 Qimonda
- 0010 16Mx32 Hynix
- 0011 16Mx32 Samsung
- 0101 32Mx32 Qimonda
- 0110 32Mx32 Hynix
- 0111 32Mx32 Samsung

PVT03/14 Set strap pin for PVT HH1 SKU
 M86-LP 256MB 32M*32 Qimonda.

If no ROM attached, GPIO[9:13:12:11]

- CONFIG{3:0}
 controls the memory aperture size.
- 128MB X000
 - 256MB X001
 - 64MB X010
 - 32MB X011
 - 512MB X100
 - 1GB X101
 - 2GB X110
 - 4GB X111



R109 for M86 only
 1 ENABLE HD AUDIO
 0 DISABLE HD AUDIO

1 HDMI ENABLE
 0 HDMI DISABLE

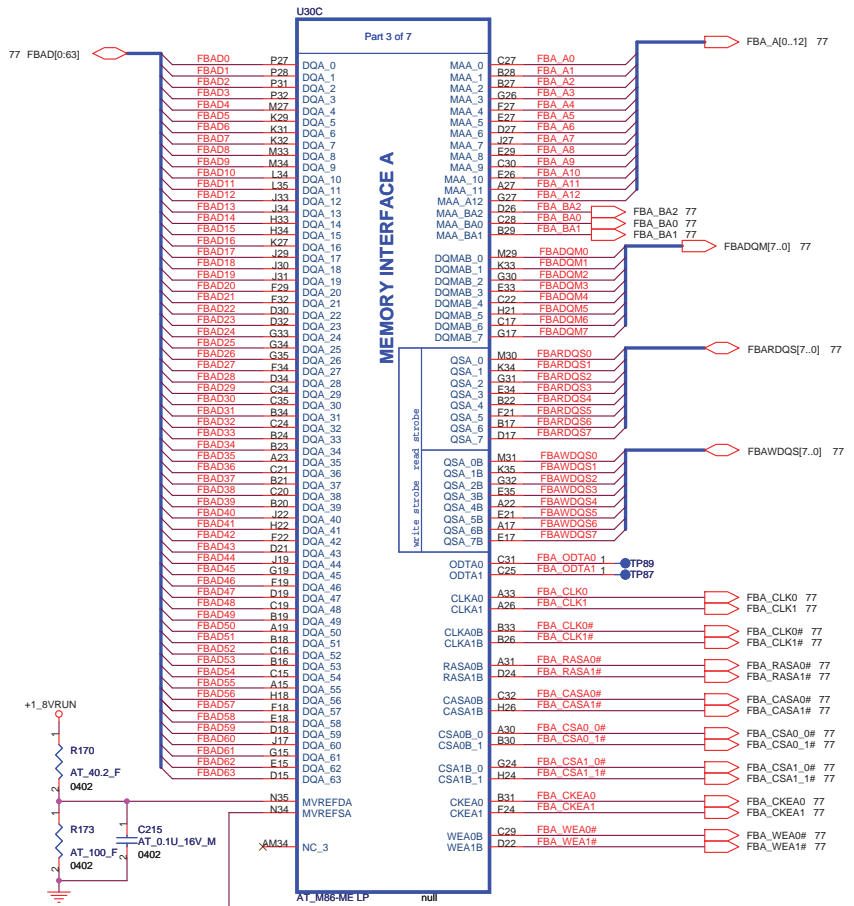
1 ENABLE EXTERNAL BIOS ROM
 0 Disable EXTERNAL BIOS ROM

CONFIGURATION STRAPS

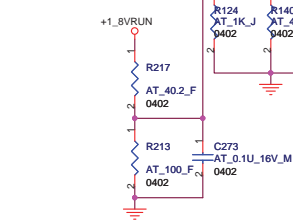
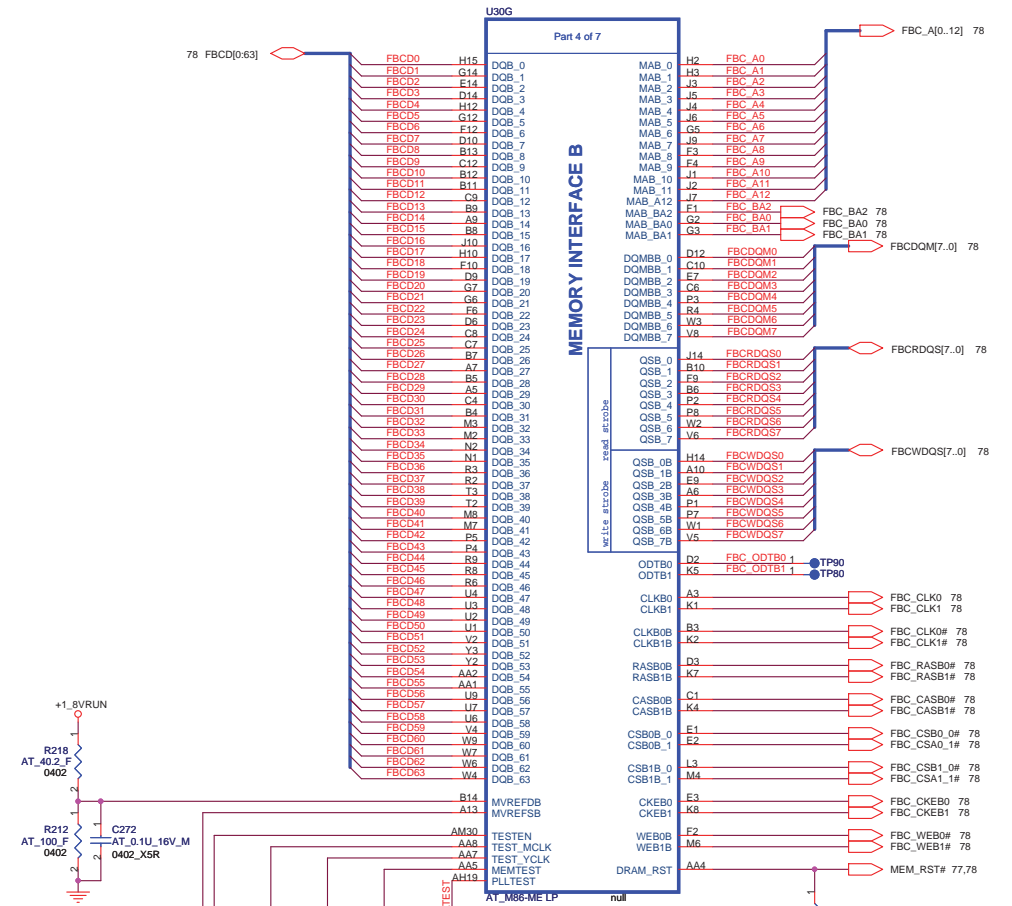
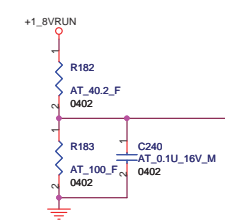
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
 0= DO NOT INSTALL RESISTOR
 1= INSTALL 10K RESISTOR
 X = DESIGN DEPENDANT
 NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
BIF_MSI_DIS	VIP1	MESSAGE SIGNAL INTERRUPT ENABLED	0
BIF_AUDIO_EN	VIP3	ENABLE HD AUDIO (SEE NOTE 1)	X
BIF_64BAR_EN_A	VIP5	64 BIT BARS DISABLED	0
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING (0: 50% Tx output swing, 1: Full Tx output swing)	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS NOT MUXED OUT	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	1
ROMIDCFG(3:0)	GPIO[13:11:9]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	X X X X
VIP_DEVICE_STRAP_ENA	VSYNC	IGNORE VIP DEVICE STRAPS	0
BIF_VGA_DIS	PSYNC	VGA ENABLED	0
BIF_HDMI_EN	HSYNC	HDMI ENABLE (SEE NOTE 2)	X
MEM_TYPE	ANY UNUSED GPIO OR DVP THAT ARE NOT CONFIG STRAPS FOR EXAMPLE DVPDATA20:23 IN THIS DESIGN	MEMORY TYPE, MAKE AND SIZE INFO	X X X X
BIF_GEN2_EN_A	GPIO_5	1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on. 0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on	0
DEBUG_I2C_ENABLE	GPIO_6	Disable DEBUG_I2C	0



DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

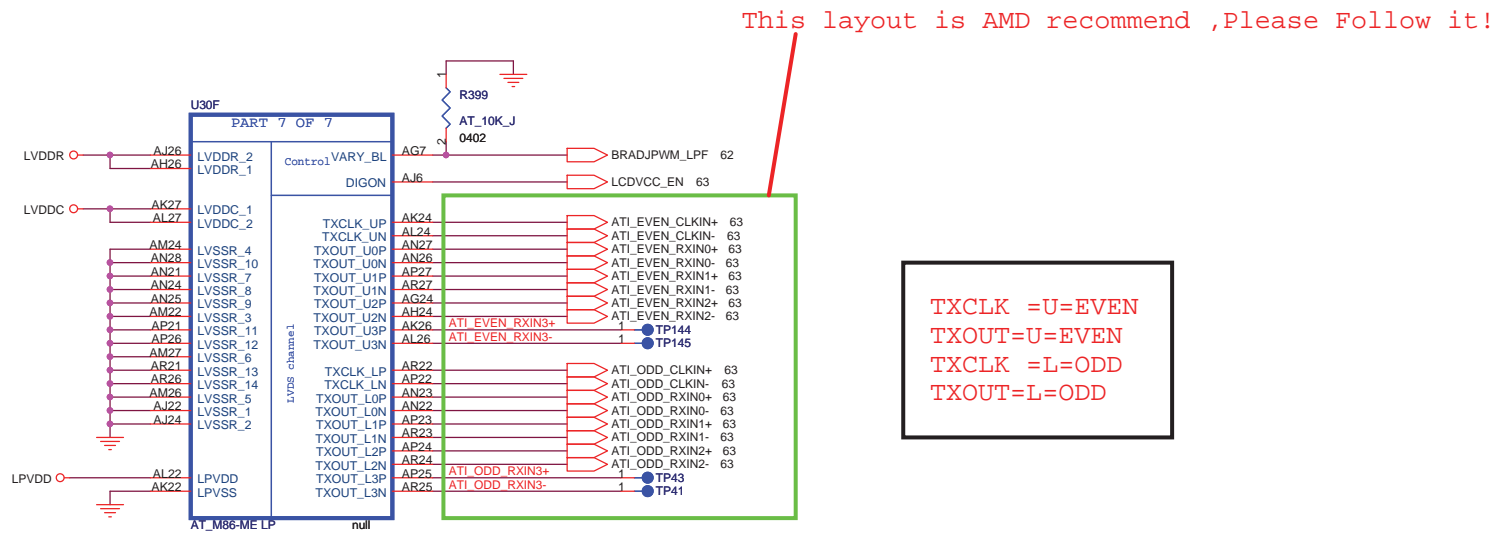


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CCPBG - R&D Division

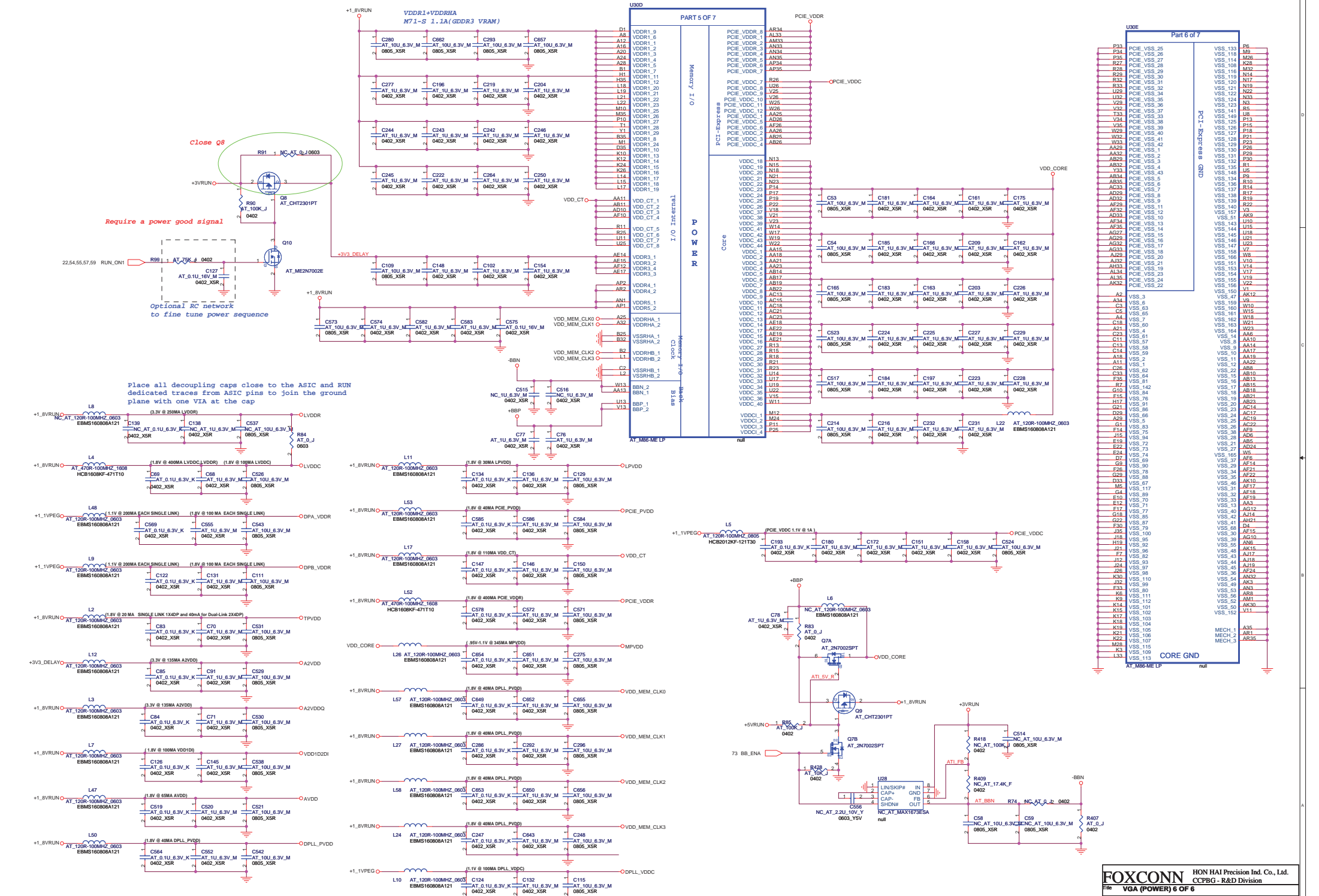
Title: **VGA (MEMORY BUS) 4 OF 6**

Size: Custom Document Number: M760 Rev: 1.0

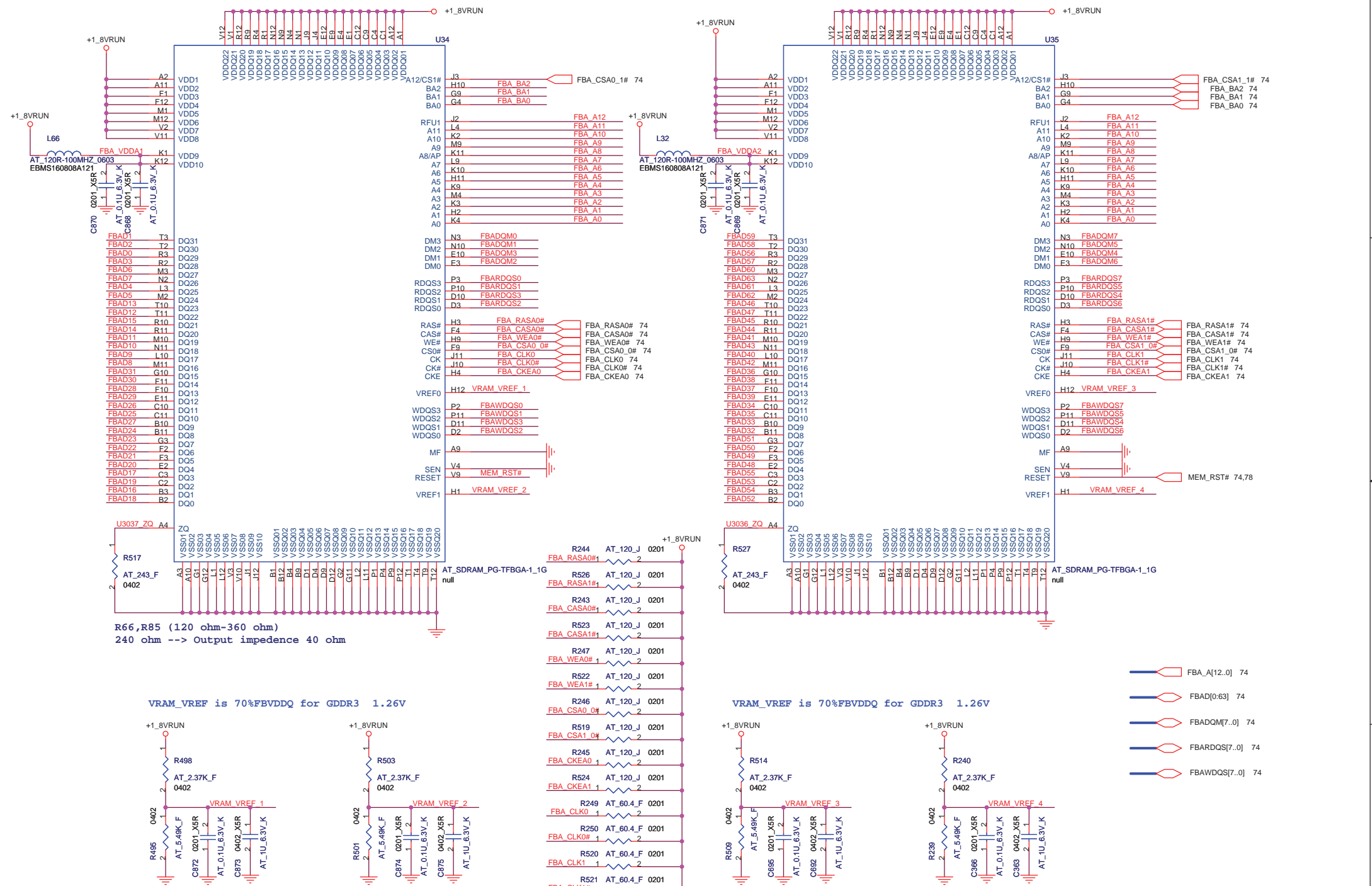
Date: Thursday, March 27, 2008 Sheet: 74 of 89

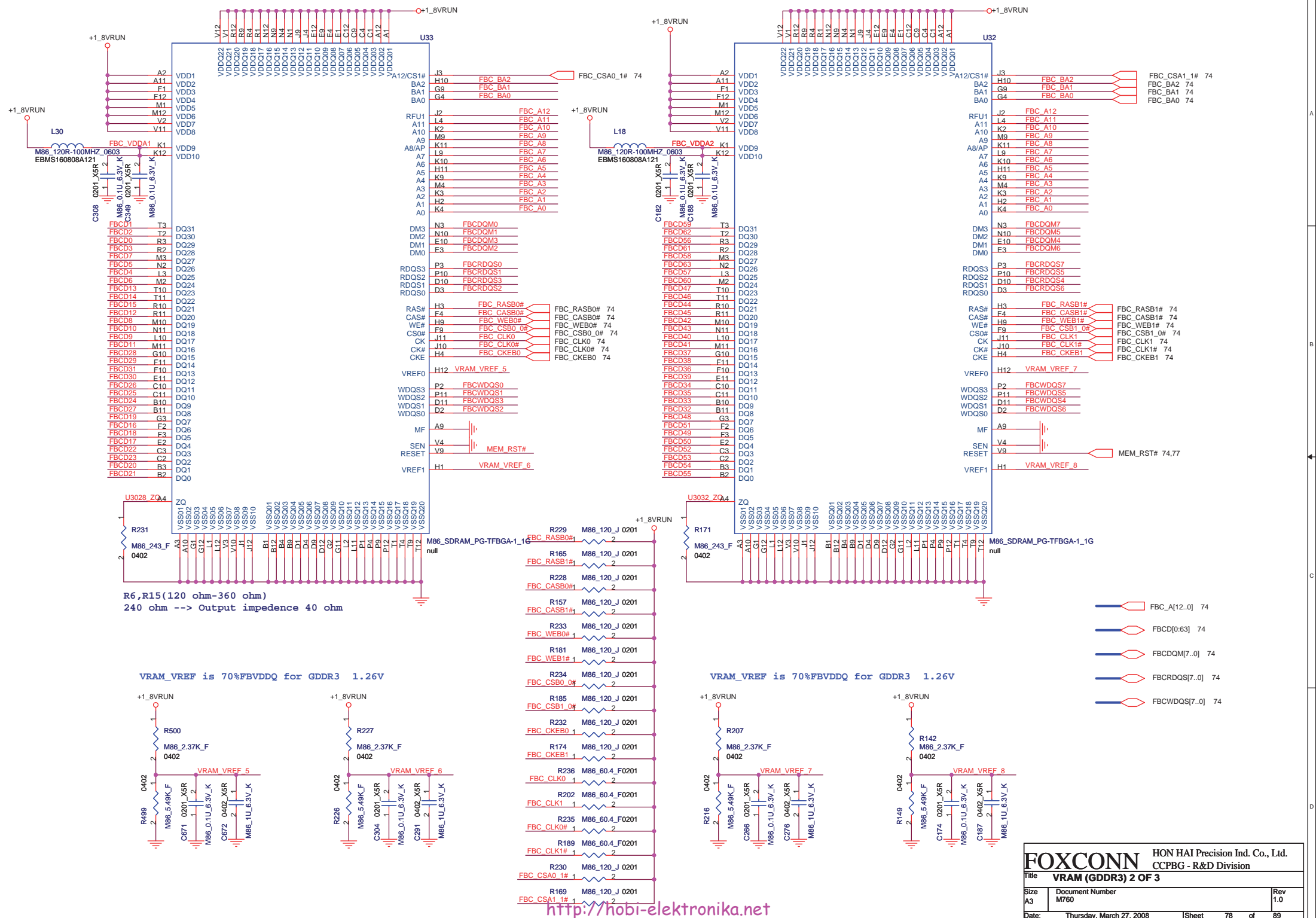


TXCLK =U=EVEN
 TXOUT=U=EVEN
 TXCLK =L=ODD
 TXOUT=L=ODD



<http://hobi-elektronika.net>





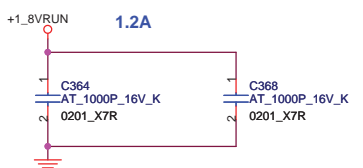
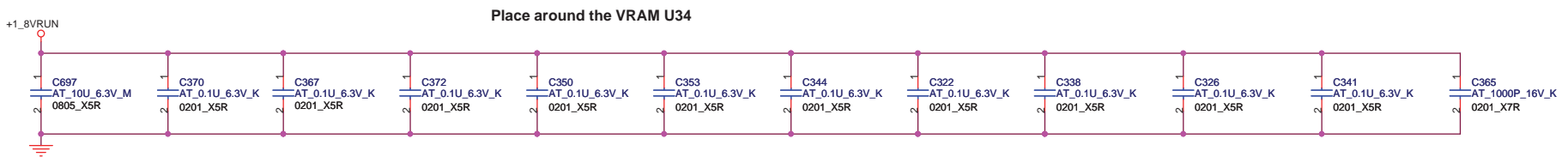
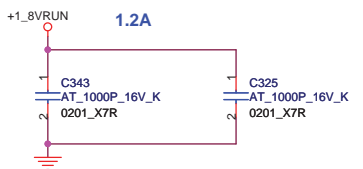
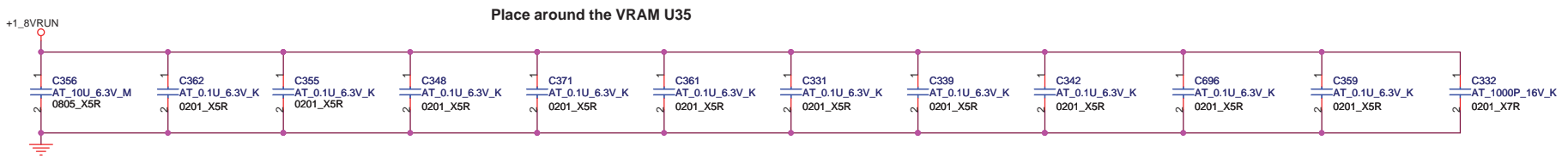
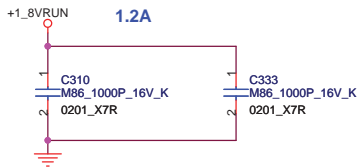
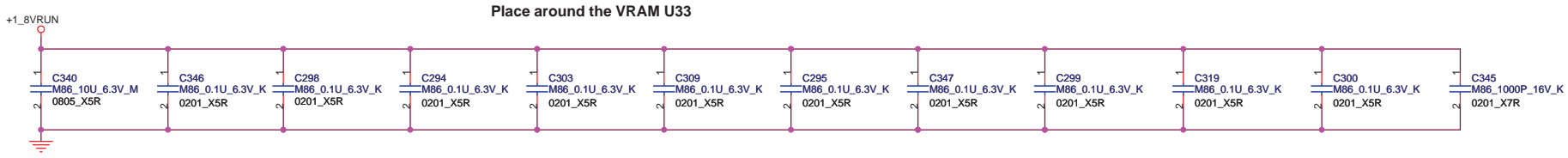
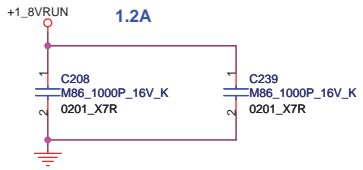
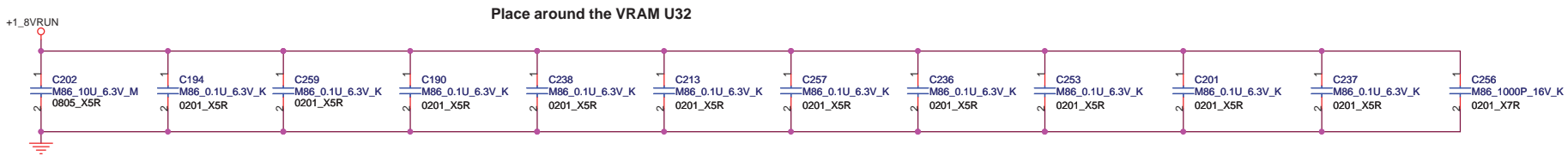
FOXCONN HON HAI Precision Ind. Co., Ltd.
 CCPBG - R&D Division

Title: **VRAM (GDDR3) 2 OF 3**

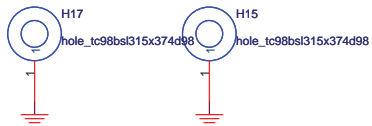
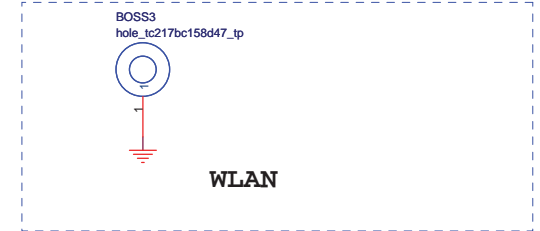
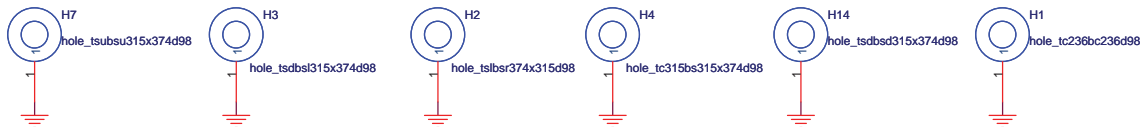
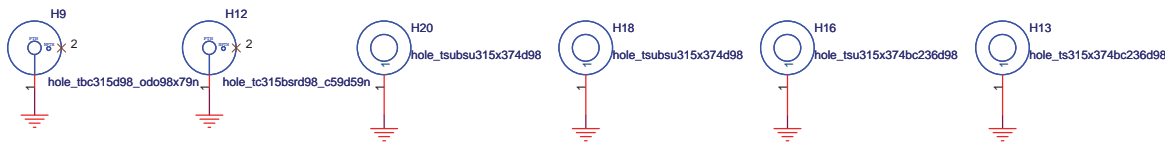
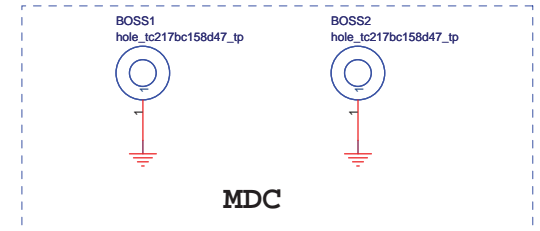
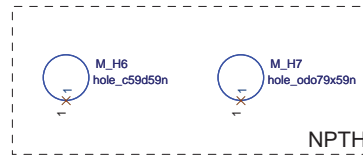
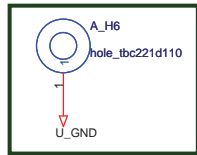
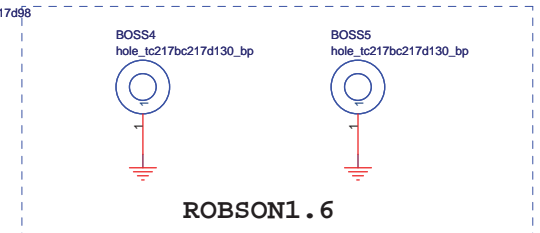
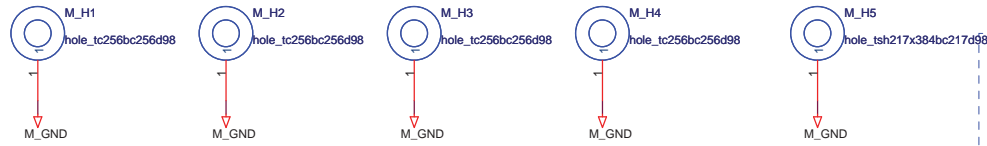
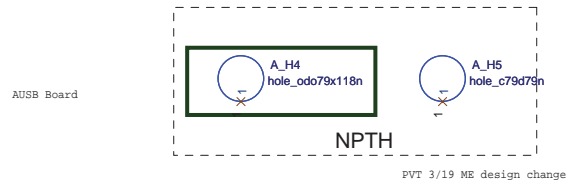
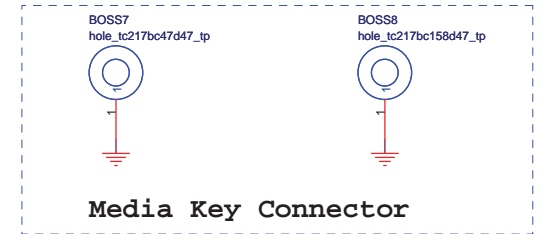
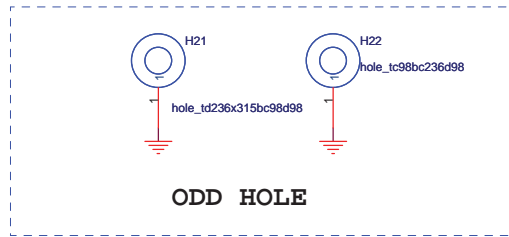
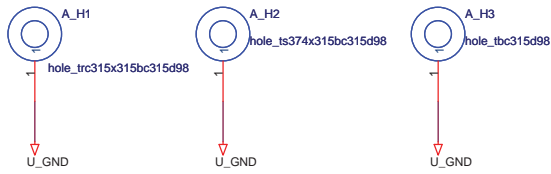
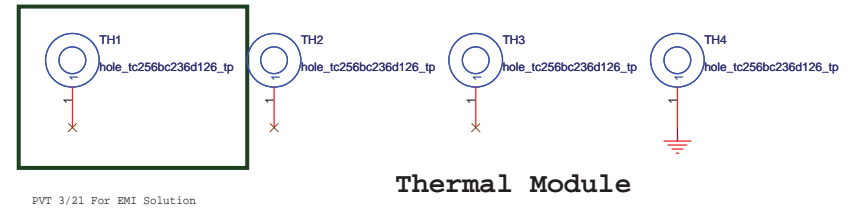
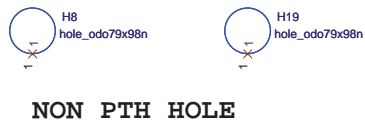
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Title		HOLE	
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2007/09/03
P.9:Reverse PCIE I/F
P.39:Change CN17 P/N
P.44:Add Power Button Connector
P.63:Change LVDS Connector P/N

2007/09/05
P.25:Change U14 P/N from Rohm to TI
P.25:Change R333,R335,R338 from 0603 to 0402
P.34:Add R762,R763,C840 for GBRST#

2007/09/07
P35.36 modify netname for MS/SD card
P14,15,16 swap DDR net for layout

2007/09/11
P.4:Delete R11,R14 and change to TP
P.8:Delete R74,R75 and change VGFX_VR_EN to TP
P.8:Delete R76 for double pull high
P.18:Delete R199,R201,Q3A/B
P.19:Change R217 from GPIO12 to GPIO13 (GPIO12 default=GPO,GPIO13 default=GPI)
P.20:Delete C290,C291,C292 and Add TP
P.20:Delete L16,C294,C295 and connect to +1.05V directly
P.22:Change RP25 from S3 power to S0 power
P.33:Delete G-Sensor function
P.35:Change R413-417,R419-423 from 0R to 33R
P.49:Change R442 from 1K to 68R
P.62:Delete R461 for simplify circuit
P.62:Change U29C-9 from VCC to INV_EN_EC
P.63:Delete R470,R471 for simplify circuit
P.63:Add C853,C854

2007/09/13
P.5:Add C855-C866 for reserved

2007/09/14
P.8:Delete R70 (Unuse) and add TP
P.8:Change R69,R71 from +1.05V to GND
P.9:Add R771-773 for H/L function
P.11:Delete R127
P.13:Delete all TP in this page
P.17:Delete R144-R146,R148-R160 and Add RP62-RP65
P.17:Delete R175,R.176,R178-R182,U5,C242,C244 and change to TP
P.17:Delete SW1,Q1,Q2,R162,R163,R166,R167,R170
P.18:Add R774
P.19:Add R775,R776 for panel ID2,3
P.19:Delete R254,R258,C254 and add TP
P.41:Add R783,R784 for H/L sku option
P.42:Add Q41-Q43,R780-R782,CAPS_LED,NUM_LED,CTRL_LED
P.50:Add PR248 for EC Charging

2007/09/15
P.6:Add R793 for enable SRC3
P.26:Delete R346 (double pull high)
P.26:Delete R779,C337,C338 (Intel WLAN spec)
P.40:Delete R431 (double pull high)
P.66:Change U37 to ALC262D (MOR drop ALC889S)

2007/09/17
P.19:Delete TP91,TP92 and change to CH+,CH-
P.19:Add GPIO18 net:TV_EEC
P.22:Delete R309,R310 and change to RUN_ON_TV1,2
P.43:Delete CIR parts and move to TV DB

2007/09/19
P.20:Add R275,R810,R811,U53 for 1.5VALW power needed
P.20:Change VCC_HDA from 3V to 1.5V
P.26:Delete SW3 (Move to Media key DB)
P.44:Delete CN26 (Move to Media key DB)
P.50:Add PR254-256,261,262 for power wave adjust
P.54:Add PR253,PR259 for power wave adjust
P.59:Add PR257-258,260 for power wave adjust
P.64:Move R618 from P.73 to here (Close to connector)
P.72:Add R816,R817,R818 for disable use
P.74:Change R650 from 243R to 240R
P.77:Add R812,R813 for 32Mx32Bit RAM config
P.78:Add R814,R815 for 32Mx32Bit RAM config

2007/09/20
Page all:Modify MON_,ATI_ to CA_,AT_
P.11:Delete R116

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2007/10/23
P.32: Add SATA ODD power saving feature circuit.
P.18: Delete SATA ODD circuit at SB side.
P.33: Move the WL & BT switch and Status LED signal to MB side.
P.44: Move the Status LED to MB side.
P.26: Move the WL & BT switch to MB side.
P.32: Change ODD from SATA to SATA.

2007/10/24
P.44: Change Status LED type.
P.34: Change the MS/SD LED control signal.
P.36: Change MS/SD LED control signal share one LED.
P.35: Change the MS/SD LED control signal.
P.72: Change the strap pin stuff and RC for default M86.
P.04: Use SBCH for PCIe SATA bridge clock.
P.70: Change Internal speaker connector form H862048 to H882048.

2007/10/29
P.57: Change *_1_SWRUN Power control signal to SWM_ON1.
P.51: Change discharge signal to SWM_ON18.
P.73/10/29 Change pull high power to *_1_SWRUN for VGA Vref correction.
P.87: Reverse the Function switch connector for EVT1 mistake.

2007/10/30
P.45: Add 22 ohm resistor for countermeasure of possible power line short.
P.45: Change P14 for the Power team test result of EVT1.
P.20: Change CLK0 to 0.87UF for customer schematic review.
P.50: Change Battery charging set table.
P.53: Change PR200 to 0 ohm for the PWM frequency change to 400KHz/500KHz.
P.59: Reserve PR209 for VGA_EN/P5V pull low.

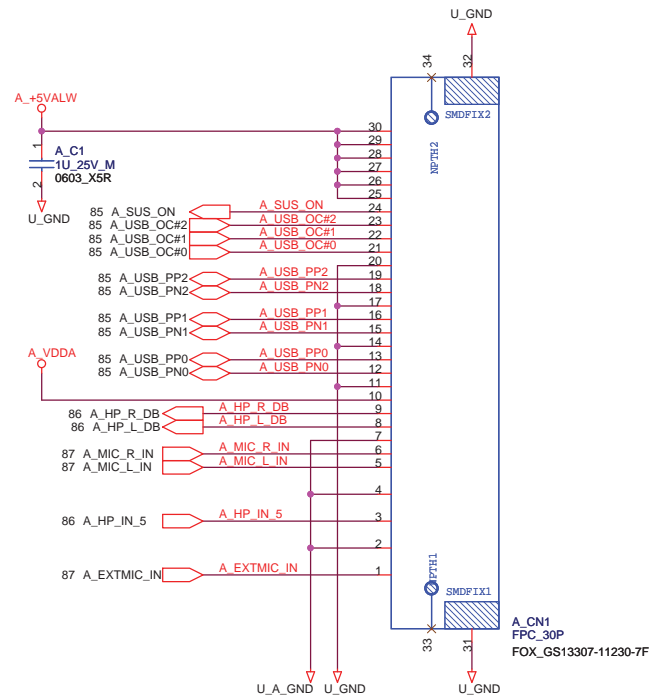
2007/10/31
P.25: Change Express card CN10 and CN11 connector to correct part.
P.56: Change WL connector CN12 and CN13 to correct part.

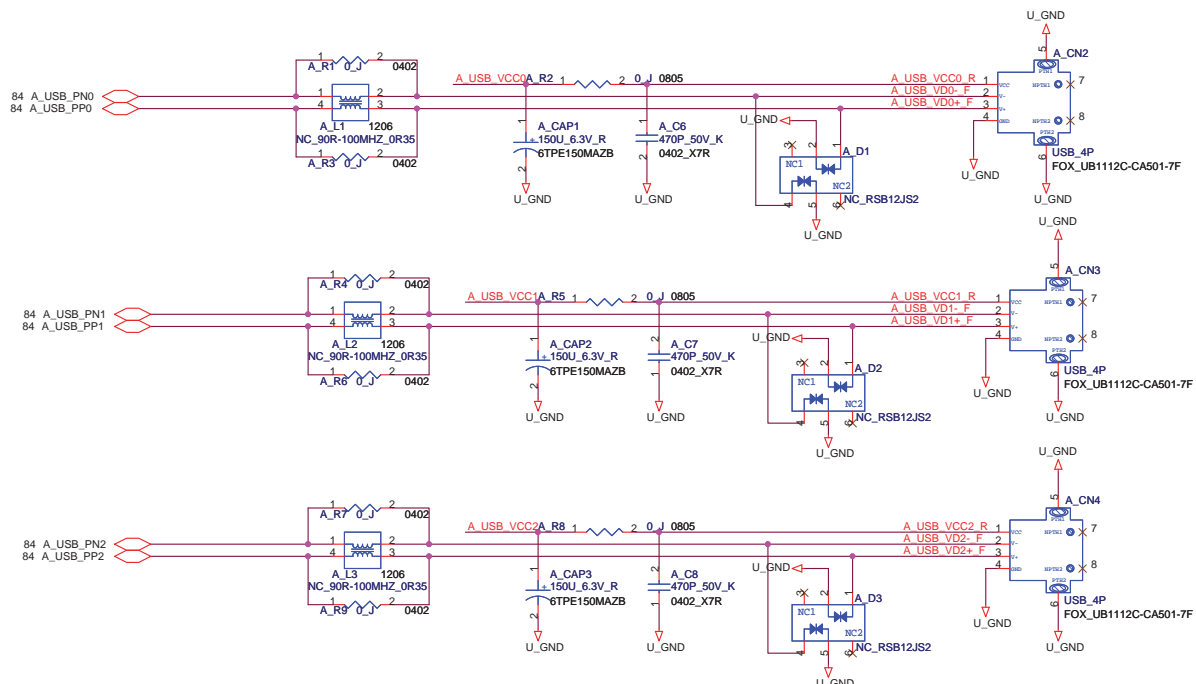
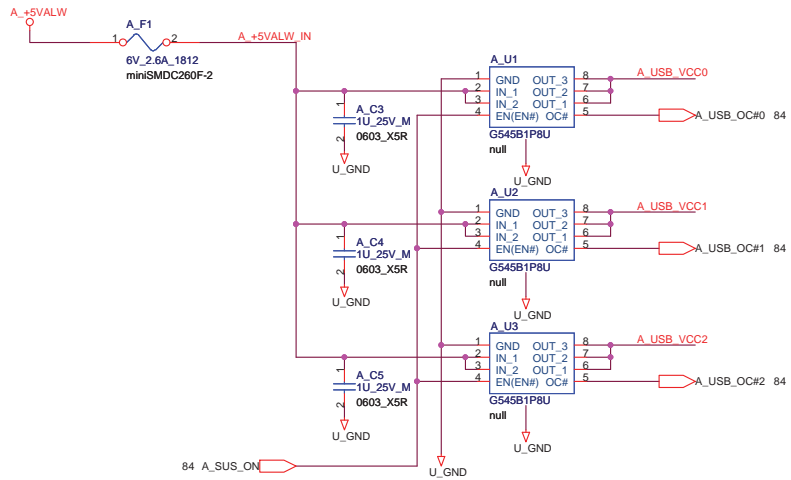
2007/11
P.64: Change the net connection of RP46 and RP53 for EVT1 net mistake.
P.75: Change the LVDS change net connection for EVT1 net mistake.
P.23: Co-Lay B775 with U3 Default is NC.
P.22: R3, R7 Adjust for clock accuracy.
P.17: Stuff for HDDP function.
P.50: Adjust charge voltage to 12.49V
P.64: Change Q35 value to CA.
P.67: Change Q30 to 2N7002E For solve the EVT1 hang '11' issue.
P.09: Reserve 150 ohm termination resistor at P/S signal, modify layout to shorten the trace stub.
P.27: Update Robson connector type.
P.22: Connect UA pin 80 for ODD power saving feature control.
P.59: Change PC158 to 100PF for power team request.
P.18: Intel recommend to add RC delay for SDR1075 timing.
P.87: Move 150 ohm resistor to power switch cable board.
P.44: Modify schematic for ODD/HDD share the LED.

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1/21-31/31
 1.006 - CLK gen - B version_RL2864882C
 2.006 - CLK gen - CLK_PCIE_MLANS2/CLK_PCIE_MLAN2 pin swap
 3.003 - CPU - R26 change to 649ohm
 4.026 - Expresscard - Change path to EXPRESS_CLK_ENH
 5.064 - HMC1 - Change D11 to RA3116 for low equal cap value
 6.007 - Ext MIC Jack - Change A_235, A_236 to 0402
 7.020 - IC93(PONER) - Change 415/107/25R
 8.011 - Cantiga(power,vcc) - Connect to Vcc3_3 no filter CA_00hm (R822) MC C621 and C622
 9.019 - IC93(GPIO) - Add R833 - If Q3 -- 85 HCU is not supported, GPIO9/MDL_EN can be connected to ground
 10.058 - OVP Protection - Power Limit Protect Setting 90M for AT - Stuff PR24 / PR22 ,75W for CA - Stuff PR218 / PR219
 11.098 - OVP Protection - Power Limit Protect Setting 80m change to *INVALID_IDD
 12.019 - IC93-M(GPIO) - CRT ID - 111 - 15.4" LCD change to 000
 13.050 - DC1W Charger - Total Power Setting PW12 AT_22K for 90M,PR220 CA_44.2K for 75W
 14.026/P40 - BT - C622 Pin# as RT_LSD MFC_PCIE_LAN - 08 pin change to RT_LSD and add pull low R824
 15.066 - HP Jack - Revised the net name to HD_R_1/HD_L_1
 16.069 - Audio Amp - Add R825 for reserved
 17.028 - TV Tuner - Reserved the C617 for TV Power
 18.028 - Mini PCIE WLAN - Reserved the C626 for WLAN Power
 19.022 - ECMPCT75 - Add the diode D21/D22 to prevent the Leakage
 20.069 - Audio Amp - U19 change to G1431F20,7550P-20(PD),2M Stereo Audio Amplifier
 21.064 - Bypass power *_OVV R31 Delete
 22.017 - IC93M - U14 BOM Changed from W25X80V8S10 to W25X80AV8S10
 23.023 - IC93M - U21 BOM Changed from W25X160V8S10 to W25X16AV8S10
 24.080 - Hole - Confirm ME, Delete H23
 25.028 - Expresscard - Revised CML Symbol footprint
 26.048 - Thermal Sensor - Reserved the HMC1402 workaround - OVT_RCS for Output Glitch on THERM# Pin During Power Up. (Vendor Suggestion)
 27.042 - Keyboard Connector- LED Display Brightness change R367,R368,R369 - 150ohm to 75ohm
 28.044 - Status LED - Change vendor of LED and LED3
 29.070 - Audio SPK Connector - Revised cable short schematic -Dummy Q83/Q84/R707/R708
 30.069 - Audio Amp - U19 pin10 change to 2.2uF for C446/CV62/CV93/CV94
 31.088 - Function SW - M_C1-M_C9 change to 100pF
 32.064 - HMC1 - Add MOS switch path and H/G bridge
 33.019 - IC93M - Add Panel ID Jumpers R828/R829/R830
 34.026 - BT - Comment change BT_DM:Active S0 ,S3
 35.058 - OVP - p015 change to PR10_2 as NDR request

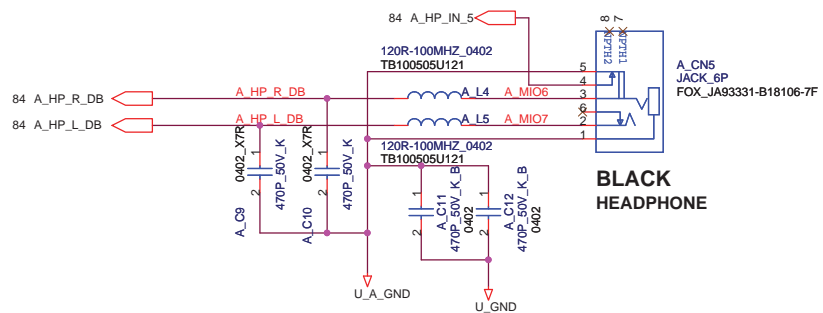
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		CCPBG - R&D Division	
Title Power Design Diagram			
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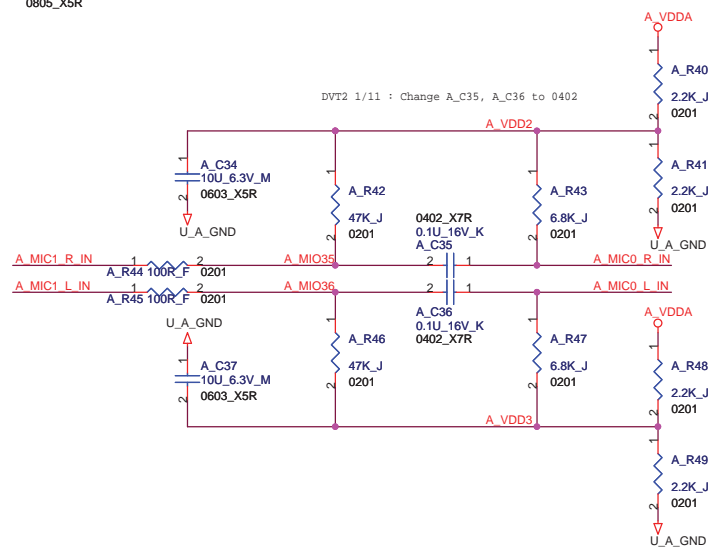
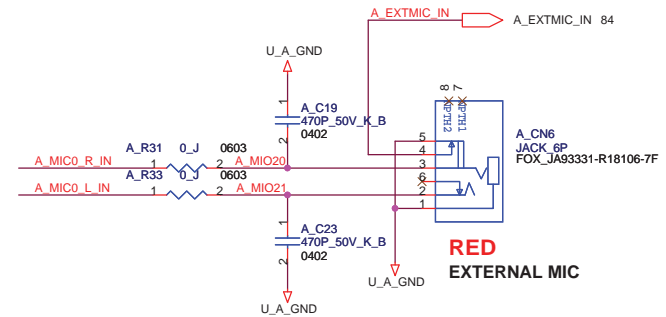
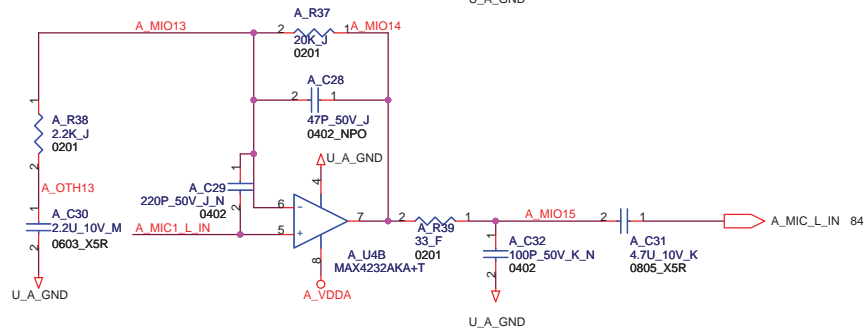
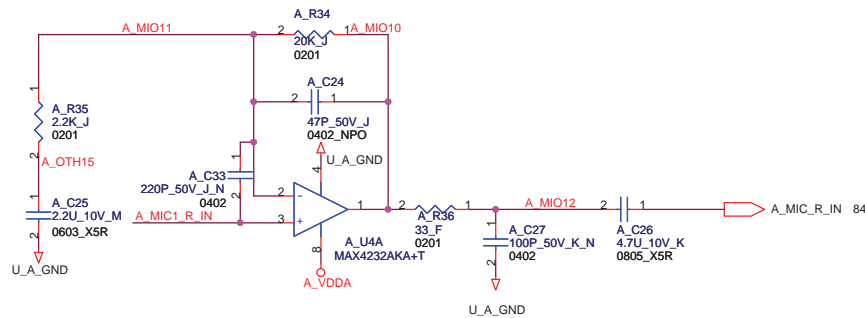




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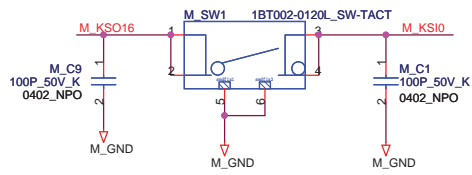
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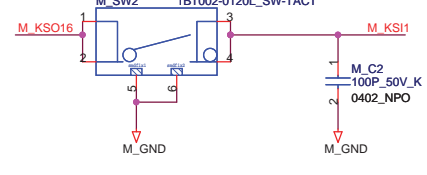


FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title Ext MIC Jack		CCPBG - R&D Division	
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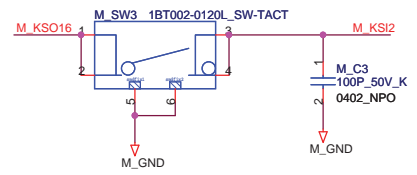
S1 (Short Cut)



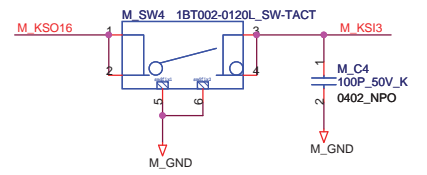
VOL-



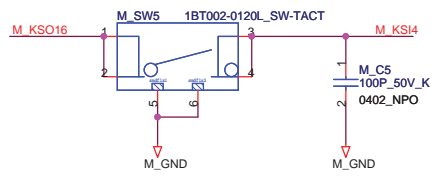
VOL+



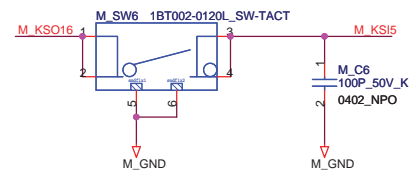
STOP



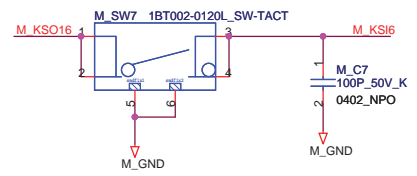
PLAY/PAUSE



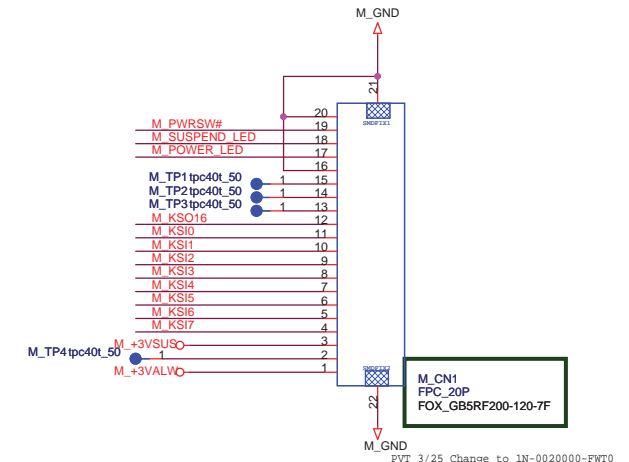
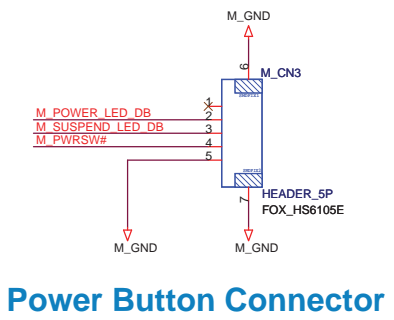
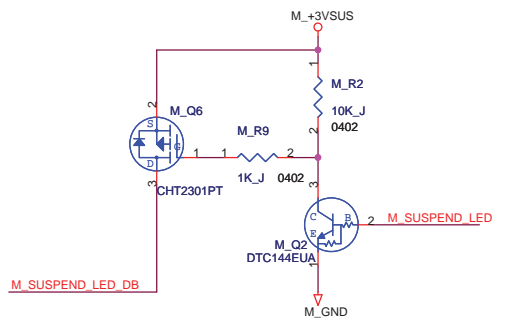
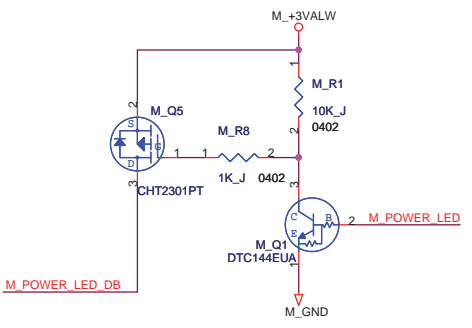
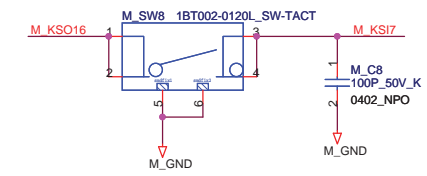
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FF



AV MODE



Power Button Connector

Media Key Connector

3/13~3/15

- P52. PU5 change part number to 15-R5G0500-0000
- P64. Stuff R505 for U37 HDMI_DCC_EN enable
- P20. C380 and C378 change to 1C-2B20104-M000
- P64. Delete Q35 and R152 ,R531 of L SKU
- P64. Stuff R507 ,R508 R568 and R569
- P59. Add PR221 for M82 PowerPlay Control
- P59. Change PR179 from 16.9K to 19.6Kohm
- P66. P64. Q34 and Q40 change to EVT2 solution
- P50. PC4 change net to BT+_L for EMI request
- P50. Add C906 and C907 for EMI request
- P50. Change PR4 to 1R-200015T-FJ00
- P50. Add PR222 and PR223 for Power Team Solution
- P32. Change ODD_DP# pin to pin23
- P20. For Engery Star Dummy U15 and R315,R314 and Stuff U47 ,C900 and C901
- P72. Change VRAM Strap pin to Q256M 32x32
- P70. Add R832/R833 for MOR request -cable short function
- P64. Add Q57 and Q58 for HDMI 5V Votage Drop Solution and Dummy D18
- P43. Add R834 +5VRUN_ODD Path 0ohm

Title		
PVT History		
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