F8V GPU Repair Guide

2010/02/08
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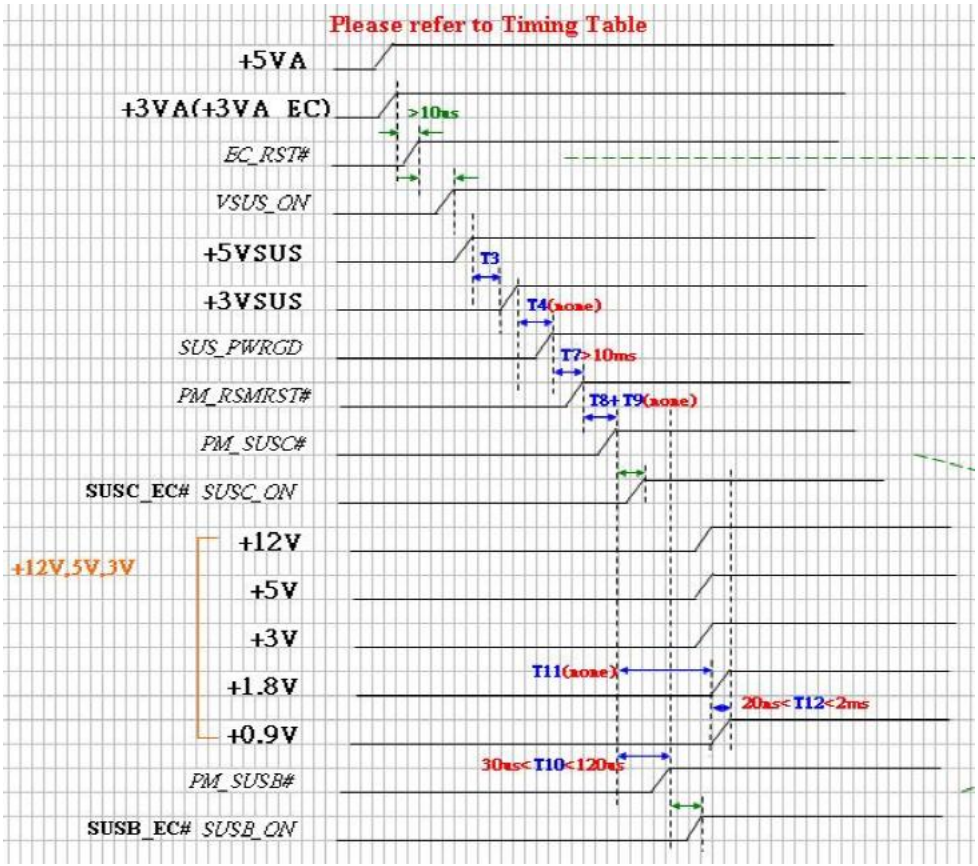

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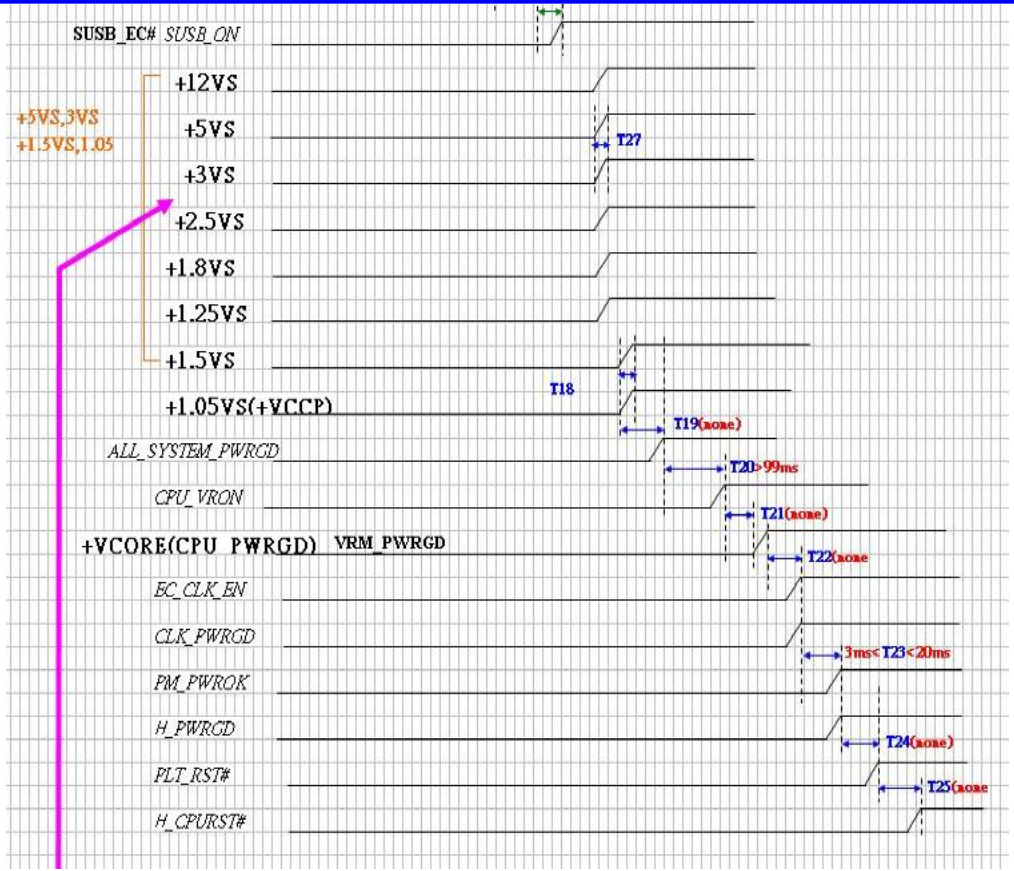

5.3 Power Up/Down Sequence

ATI VGA(M86)

An ideal power up sequence for M86 is illustrated as follows.

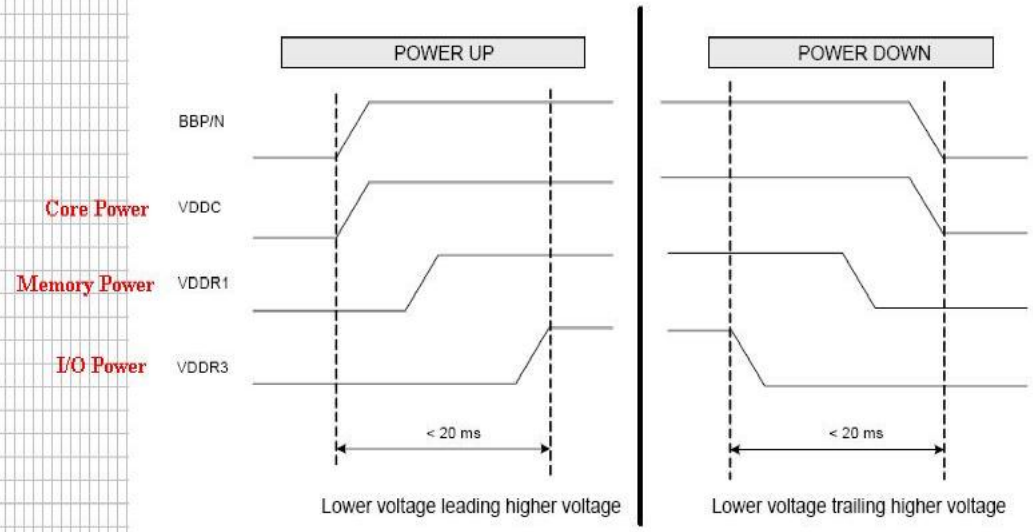

Figure 5-1 Ideal Power Up Sequence

5.3.1 General Guidelines

M86 has the following requirements with regards to power supply sequencing to avoid damaging the ASIC.

- All the ASIC supplies must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred.

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* The correct values will be filled up after measureing the SR1 borad.

Time	Specification	CRB Value	Customer Platform Designed value	Requirement	Source
T3	see requirement column	1.48ms		5VSUS must be powered up before 3VSUS, or after 3VSUS within 0.7 V. Also, 5VSUS must powerdown after 3VSUS, or before 3VSUS within 0.7 V	From ICH9 EDS t201
T4	none	1.56ms			
T7	>10ms	240ms		SUS_PWRGD supplies active to LAN_RST# inactive,PM_RSMRST# inactive	From ICH9 EDS t204
T8	none	99.4ms			
T9	none	30.8us			
T10	30us<T<120us	61.2us		1RTC clock<T10<4RTC clock 1RTC clock approximately from 28.992 us to 32.044us T10 Max value much larger than the Min (e.g. up to 3 seconds). With the installation of the Intel Manageability Engine firmware, the Max value of T10 is 99ms. Without the installation of the firmware, the Max value is 4RTC clocks.	From ICH9 EDS t234
T11	none	736us			
T12	20ns<T<2ms	1.88ms		1. When powered on, the 1.8 V rail must ramp up from 0 V to 1.8V within 2 ms. The 2 ms timing requirement is needed to ensure proper power on of the DDR2 memory devices. 2. To protect against ESD issue, MCH requires that the DRAM_PWROK never be driven high before the DDR voltage plane has ramped to stable value. Power up (G3/S5/S4 to S0): DRAM rails must be stable for 20ns, or more, prior to the assertion of DRAM_PWROK	1. Montevina Design Guide section 5.3.8.1, DDR2 Power sequencing 2. From DDR3 spec
T18	see requirement column	1.192ms		1.5VS must powerup before 1.05VS or after 1.05VS within 0.7 V 1.05VS must powerdown before 1.5VS or after 1.5VS within 0.7 V	From ICH9 EDS t211

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T18	see requirement column	1.192ms		1.5VS must powerup before 1.05VS or after 1.05VS within 0.7 V 1.05VS must powerdown before 1.5VS or after 1.5VS within 0.7 V	From ICH9 EDS t211
T19	none	2.352ms			
T20	>99ms	302ms		Vcc* supplies to be valid for at least 99 ms before PM_PWROK goes high to comply with the PCI Specification Rev 2.3*.In addition, the PCI clocks should be running for at least 1 ms before PM_PWROK goes high GMCH PM_PWROK Requirement All (G)MCH power supplies should be valid at least 99 ms before PM_PWROK assertion.	From ICH9 EDS t214
T21	none	150us			
T22	none	10us			
T23	3ms<T<20ms	7.76ms		1. VRMPWRGD active to PM_PWROK active 2.GMCH PWROK requirement (G)MCH clocks should be running and stable at least 1 μs before PM_PWROK assertion. 3. Delay from EC_CLK_EN to PM_PWRGD	t212 2. Cantiga EDS rev0.7 section 9.9 PWROK Timing Requirements for Power-
T24	none	1.08ms			Penryn EMTS spec
T25	none	1ms			Penryn EMTS spec
T27	see requirement column			5VS must be powered up before 3VS, or after 3VS within 0.7 V. Also, 5VS must powerdown after 3VS, or before 3VS within 0.7 V	From ICH9 EDS t209
T31	>5us			SLP_S3# active to Vcc supplies inactive (nominal voltage -5%)	From ICH9 EDS t307
T32	>500us			SLP_M# active to RSMRST# active	From ICH9 EDS t313
T33	>20ns			PWROK, VRMPWRGD inactive to Vcc supplies inactive (nominal voltage -5%)	From ICH9 EDS t290
T34	T34>97us			PWROK must deassert for a minimum of three RTC clock periods in order for the ICH9 to fully reset the power and properly generate the PLTRST# output.	From ICH9 EDS description of PWROK
T35	>20ns			SM_PWROK must go low 20ns prior to the DRAM rail ramping down more than 10% of DDR voltage value (Requirement for DDR3)	DDR3 Spec

* Vcc includes Vcc1_5_A(1.5VS), Vcc1_5_B(1.5VS), Vcc3_3(3VS), Vcc1_05(1.05VS), VccUSBPLL(1.5VS), VccDMIPLL(1.5VS), VccSATAPLL(1.5VS), and V5REF(5VS). EDS note1 : Figure 8-15

5.3.1 General Guidelines

M86 has the following requirements with regards to power supply sequencing to avoid damaging the ASIC.

- All the ASIC supplies must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred.
- VDDC (including VDDCI & MPVDD) should ramp first.
- BBP must ramp up before or at the same time as VDDC but not after (i.e. ensure that BBP>=VDDC at all times).
- Ensure that BBN<=VSS at all times.
- 1.1-V rails should ramp before, or together with, the 1.8-V rails. The 1.1-V nominal rails should never lag the 1.8-V nominal rails by more than 1.1 V within a 1-ms window.
- 1.8-V rails should ramp before the 3.3-V rails. (If 1.8 V does not precede 3.3 V, then a momentary pulse may be observed on the 3.3-V GPIOs (e.g. GPIO_19_CTF).
- Rails of the same nominal voltage level should ramp together if design constraints allow.
- DDC3DATA_DP3_AUXN, DDC4DATA_DP4_AUXN, DDC3CLK_DP3_AUXP, and DDC4CLK_DP4_AUXP must be pulled high before VDDC is powered up.
- VDDC must ramp before DPx_VDDR and DPx_PVDD; DPx_VDDR should ramp with, or before, DPx_PVDD.

Note: For the purpose of sequencing description, VDDR1 represents VDDR1 & VDDRHx, and is considered to be a 1.8-V nominal rail.

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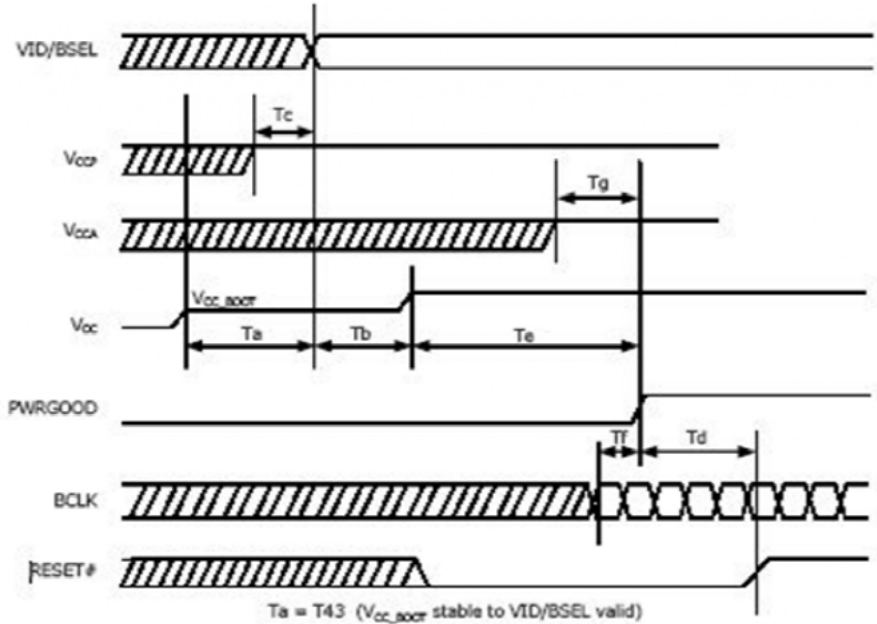
Power Up Sequence



Ta = T43 (V_{CC_BOOT} stable to VID/BSEL valid)
Tb = T44 (VID/BSEL valid to Vcc stable)
Tc = T48 (V_{CCP} stable to VID/BSEL valid)
Td = T36 (PWRGOOD assertion to RESET# de-assertion)
Te = T41 (V_{CC} stable to PWRGOOD assertion)
Tf = T37 (BCLK stable to PWRGOOD assertion)
Tg = T49 (V_{CCA} stable to PWRGOOD assertion)

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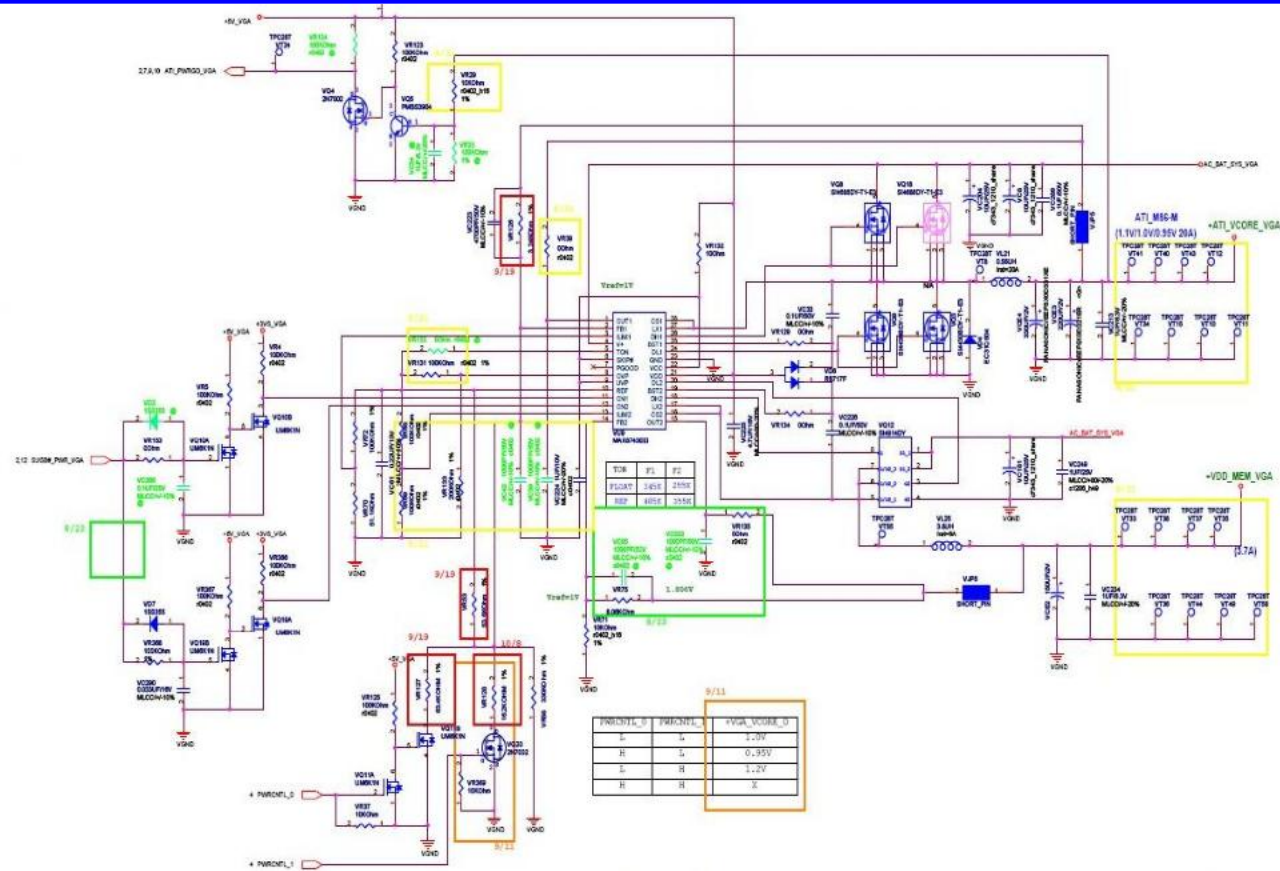

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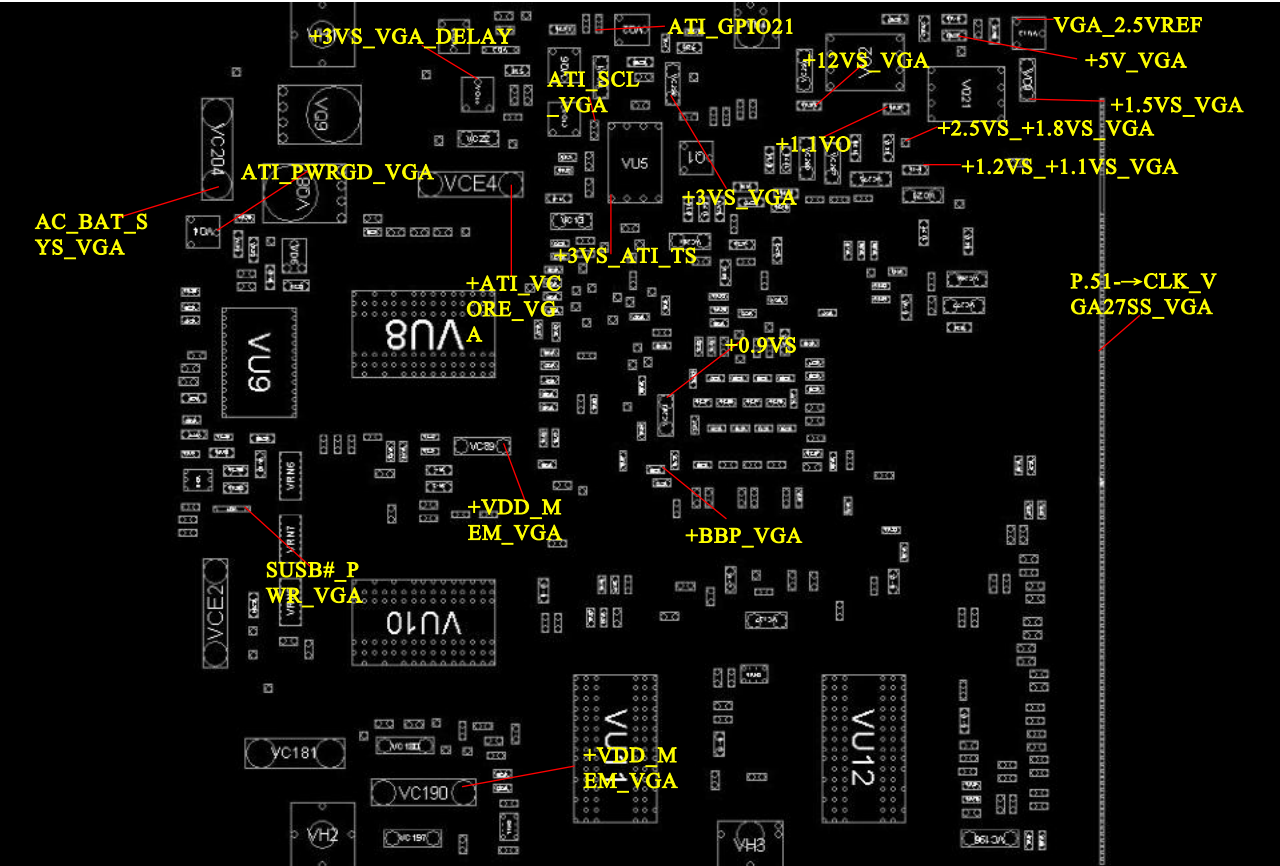

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