

Compal confidential

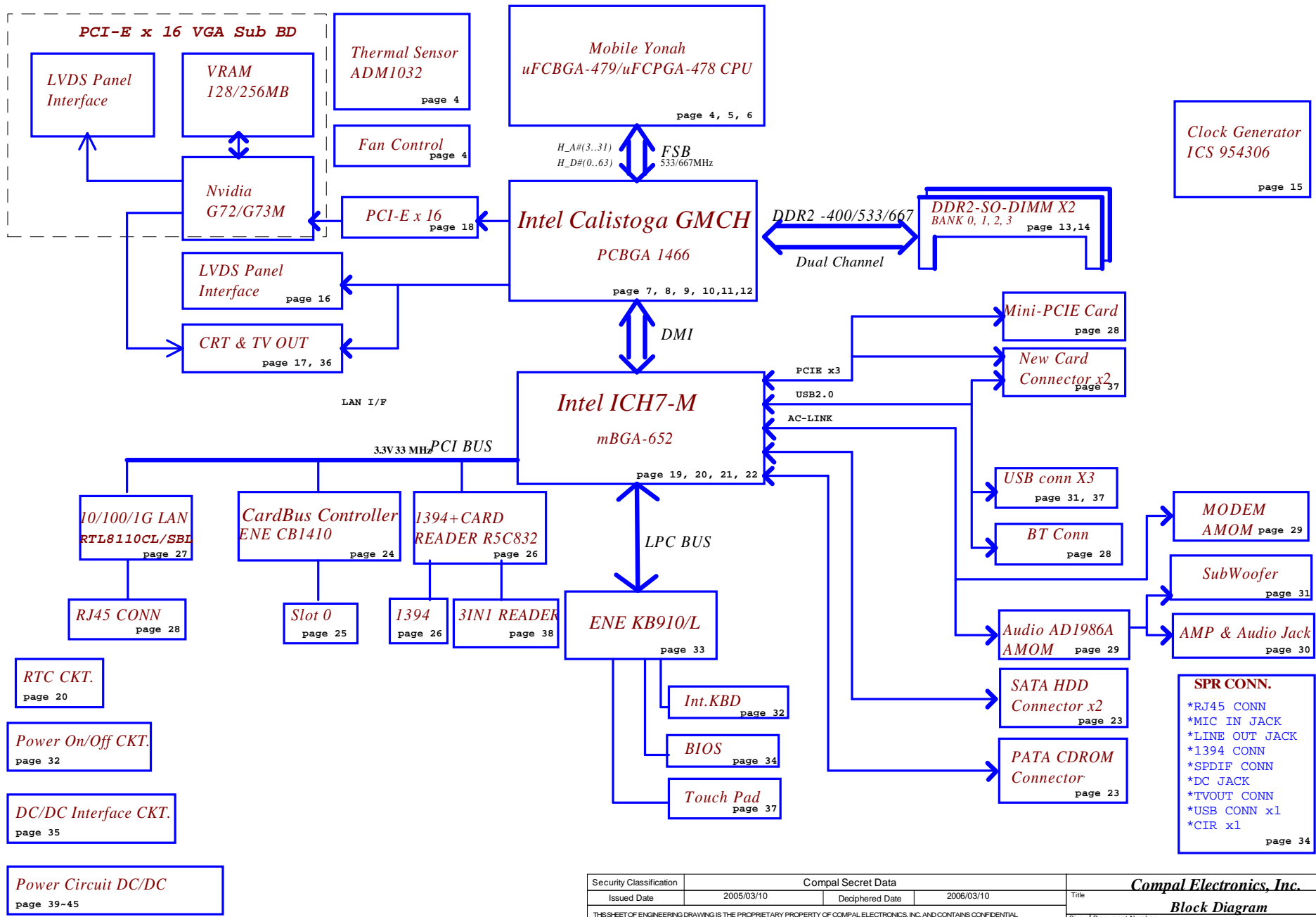
IGL50/51 Schematics Document

Mobile Yonah uFCPGA with Intel
Calistoga_GM/PM+ICH7-M core logic

2006-07-31

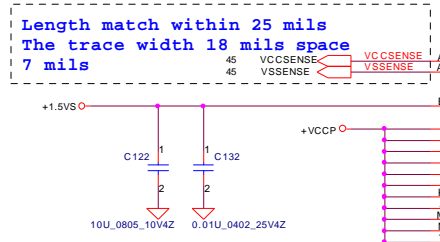
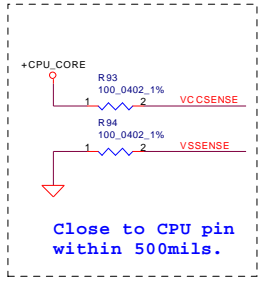
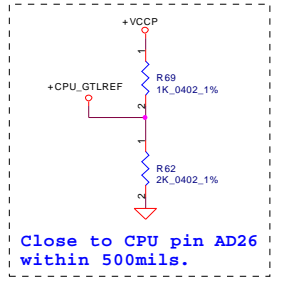
REV:0.2

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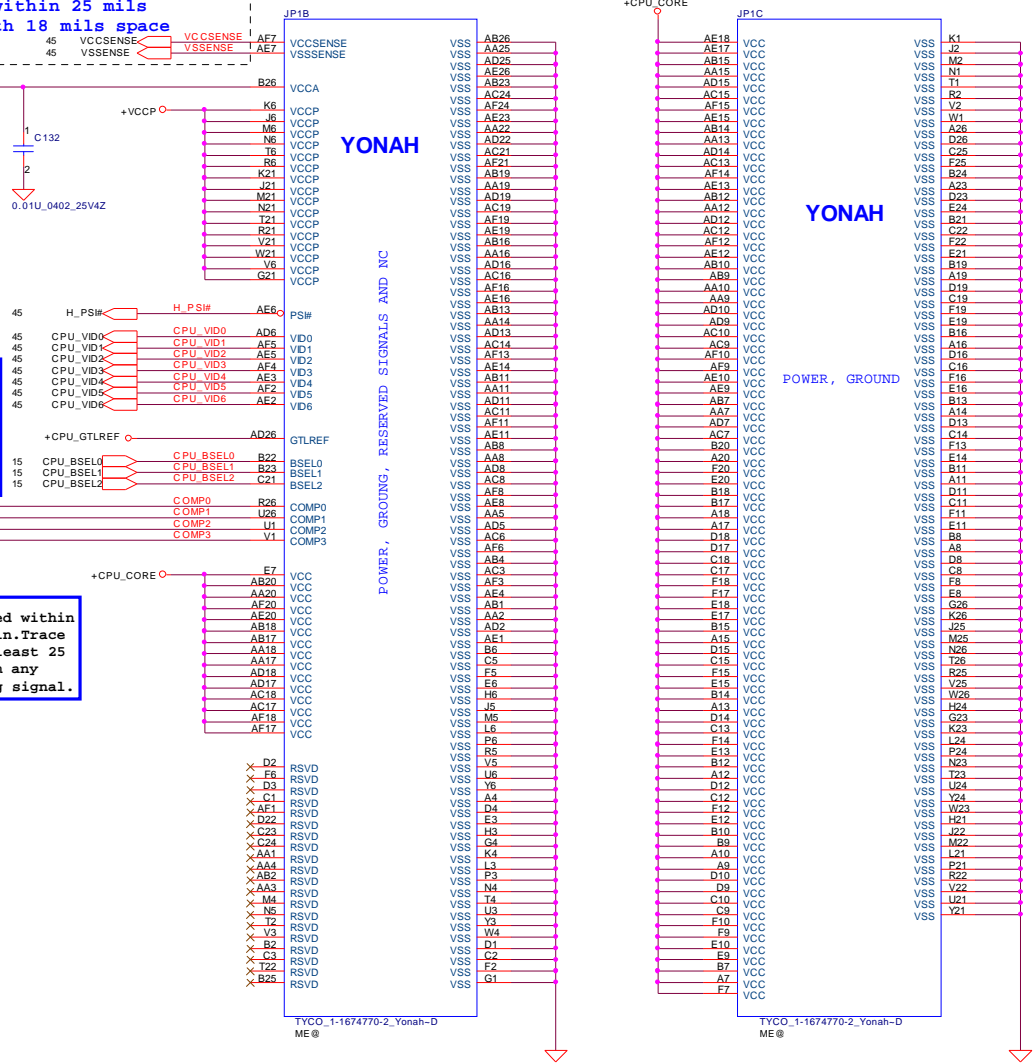
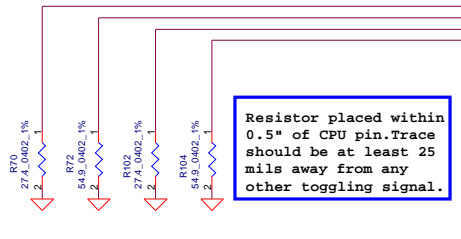


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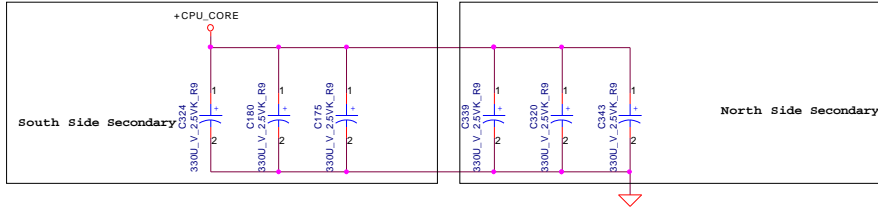
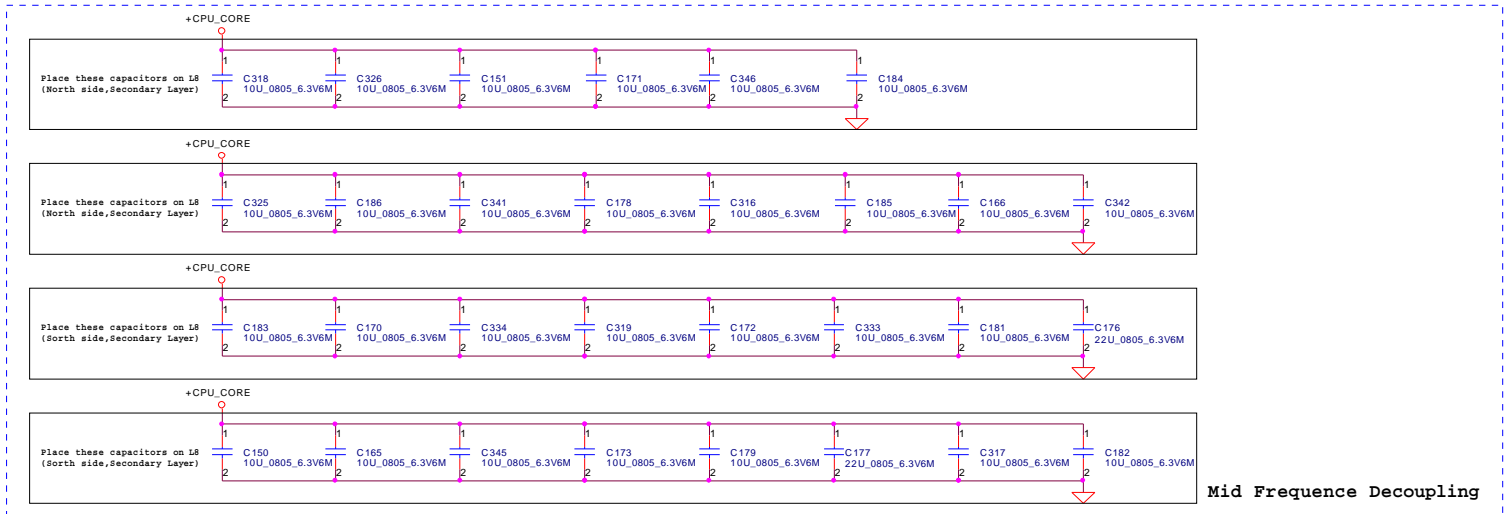
Compal Electronics, Inc.		
Title Block Diagram		
Size	Document Number	Rev
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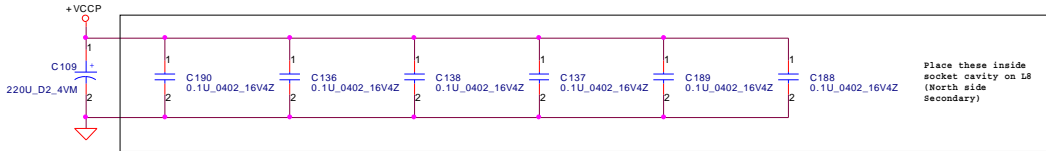
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1



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Date	日期	日期	日期	Rev
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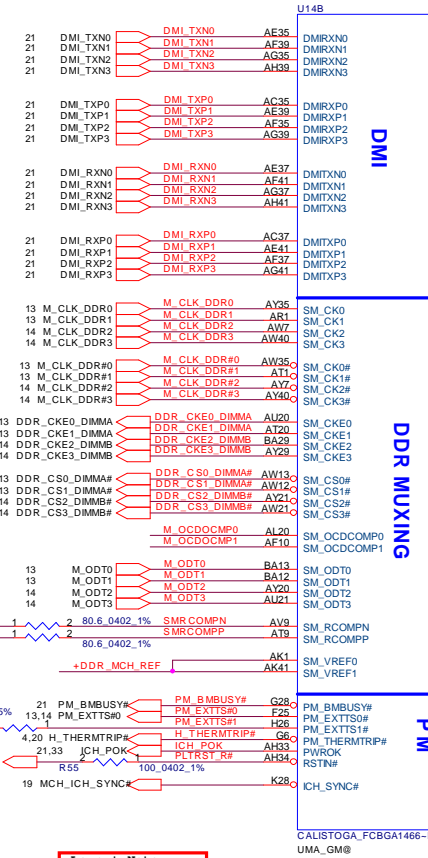
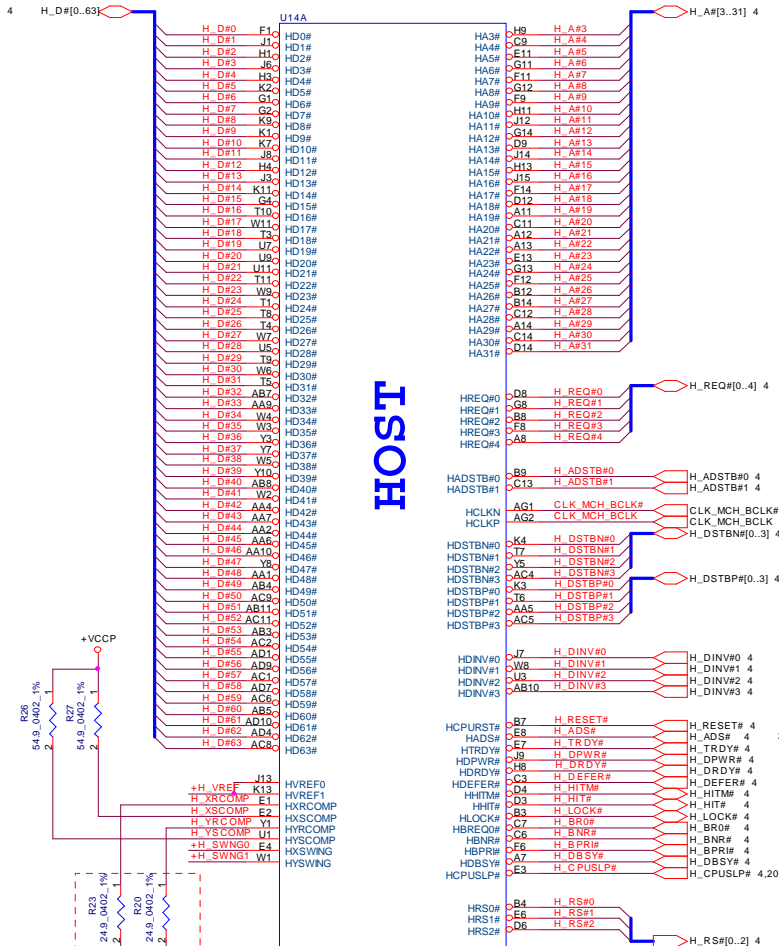


**ESR <= 1.5m ohm
Capacitor > 1980uF**

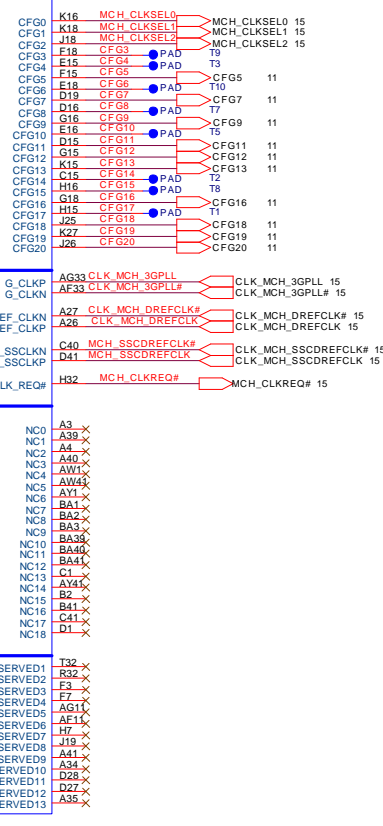


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CPU Bypass capacitors	
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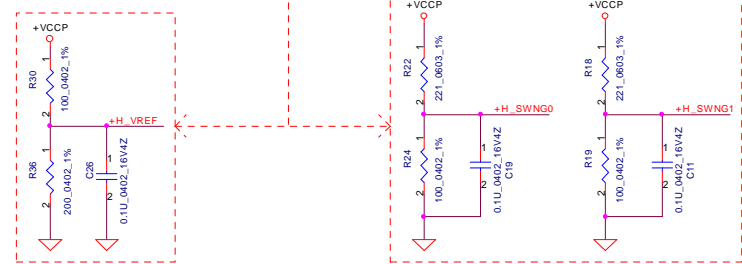


Description at page15



Layout Note:
H_XRCOMP / H_YRCOMP / H_VREF / H_SWNG0 / H_SWNG1 trace width and spacing is 10/20.

Layout Note:
+DDR_MCH_REF trace width and spacing is 20/20.



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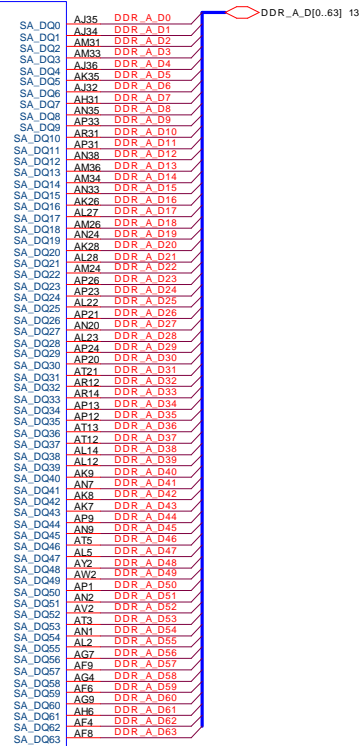
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Calistoga (1/6)		
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check layout

CALISTOGA_FCBGA1466-D
UMA_GM®

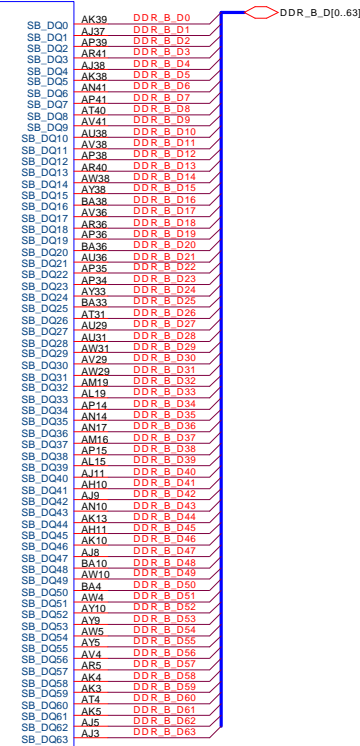
DDR SYS MEMORY A



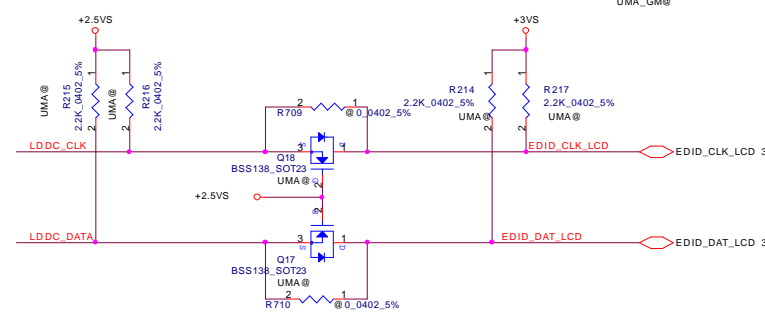
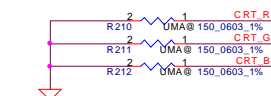
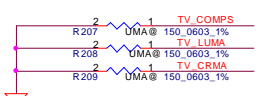
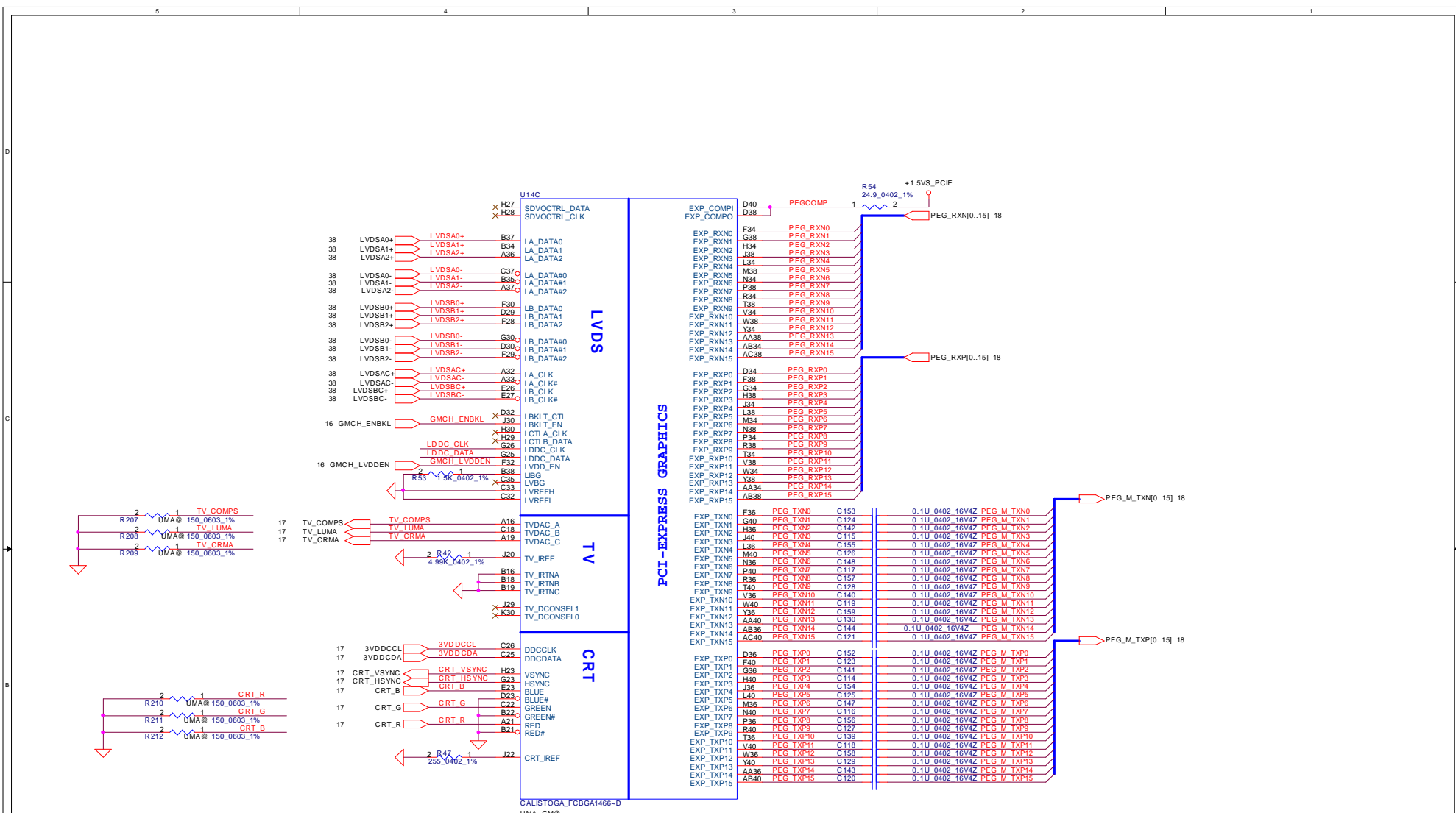
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CALISTOGA_FCBGA1466-D
UMA_GM®

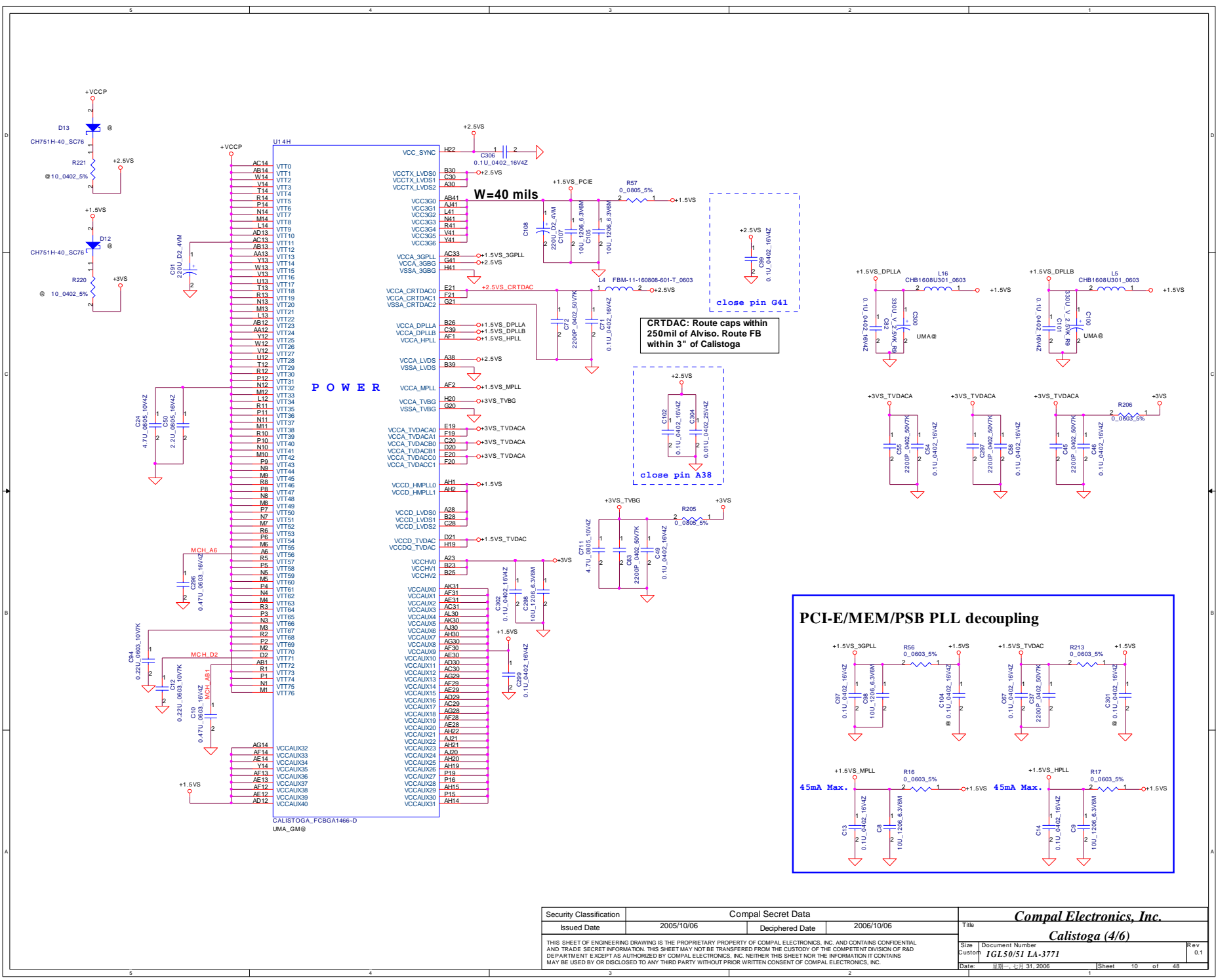
DDR SYS MEMORY B



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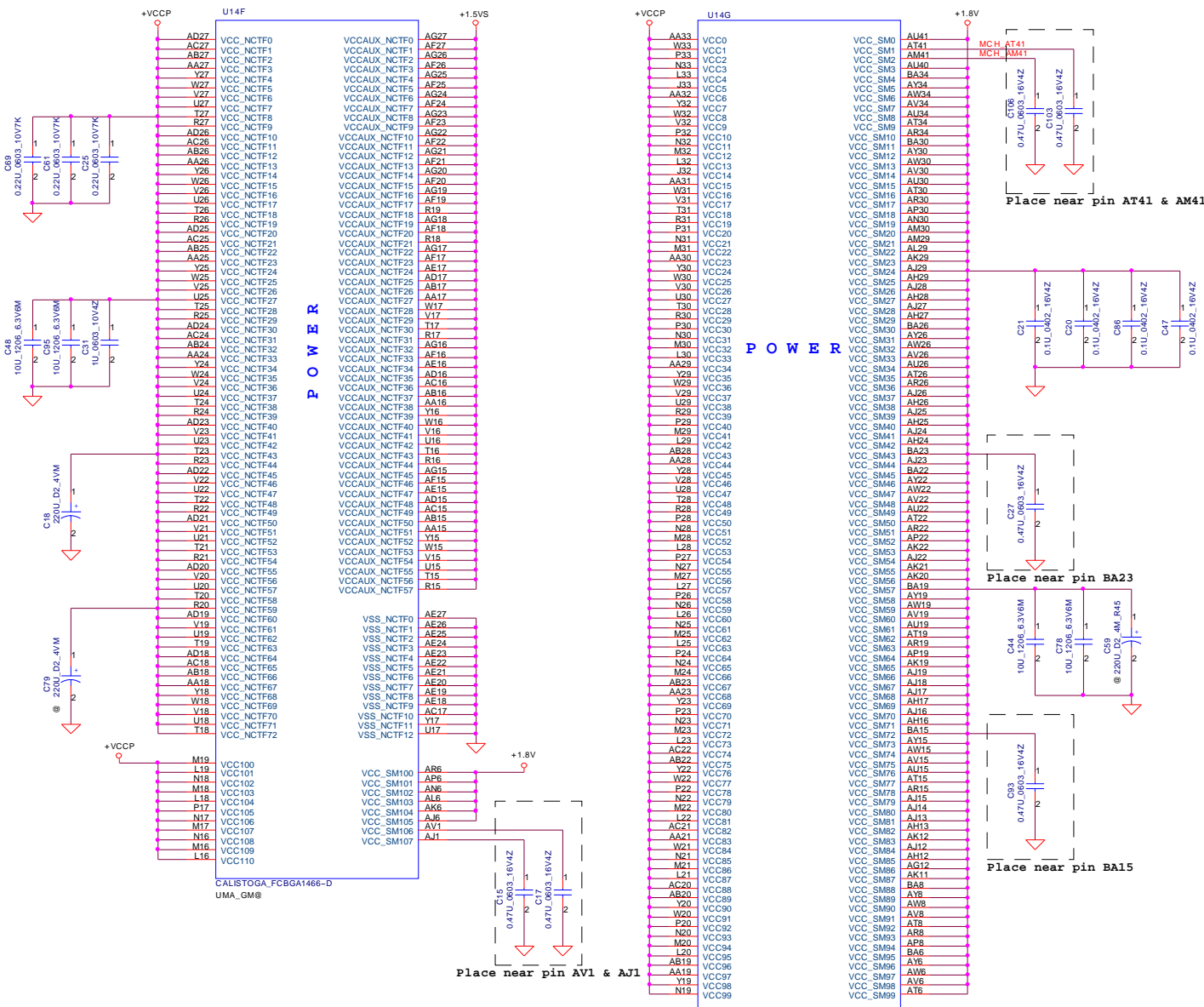
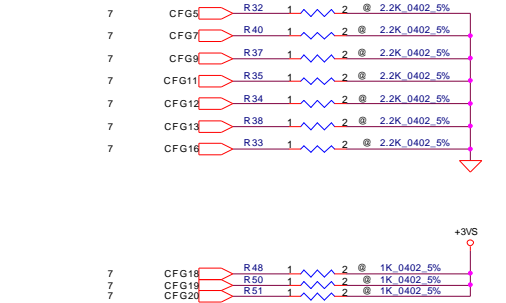
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Strap Pin Table

CFG[3:17] have internal pull up

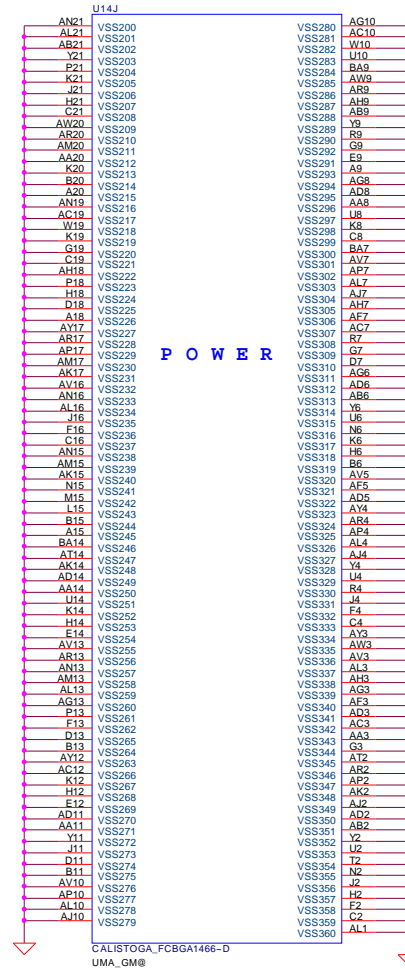
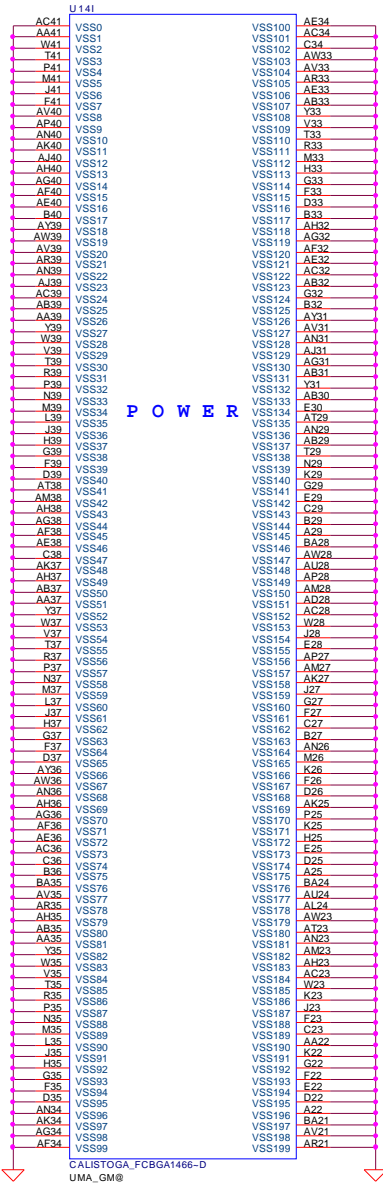
CFG[19:18] have internal pull down

CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 * (Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU * (Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation (Default) *
CFG6	0 = Reserved
PSB 4X CLK Enable	1 = Calistoga *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation * (Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled * (Default)
CFG10 CFG18	10 = 1.05V * (Default) 01 = 1.5V
CFG19	0 = Normal Operation * (Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present * (Default) 1 = SDVO Device Present
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. * (Default) 1 = PCIE/SDVO are operating simu.



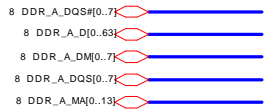
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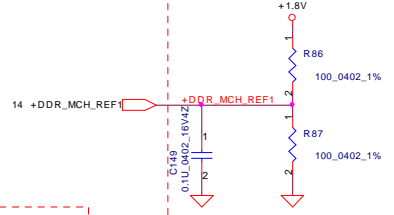


POWER

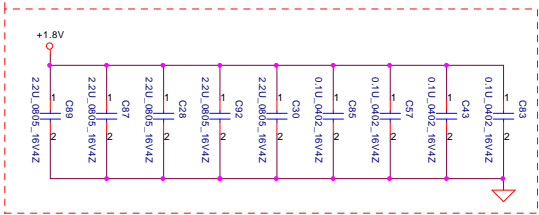
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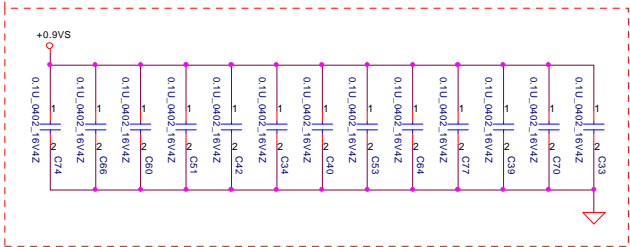
Layout Note:
+DDR_MCH_REF
trace width and
spacing is 20/20.



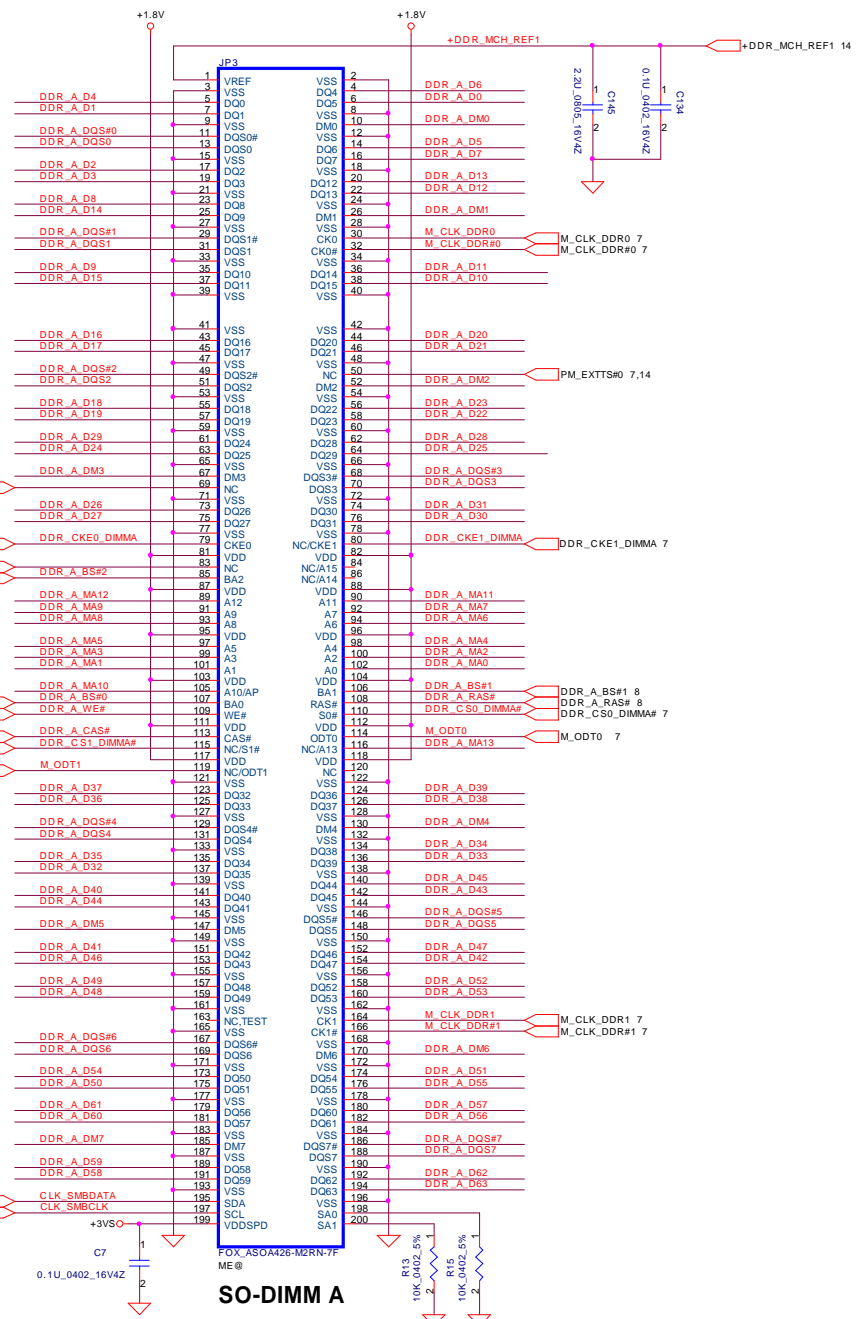
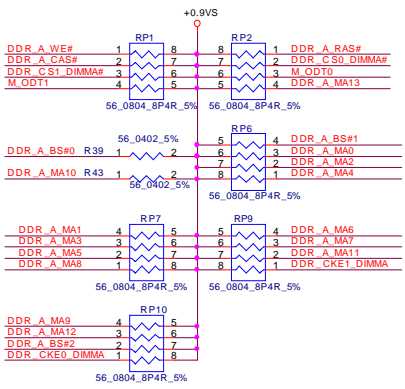
Layout Note:
Place near JP41



Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS



Layout Note:
Place these resistor
closely JP41,all
trace length Max<1.5"



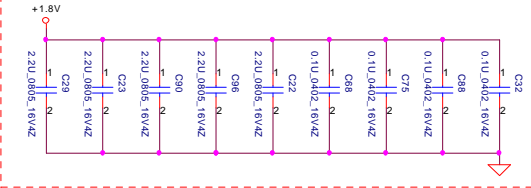
SO-DIMM A
Top side

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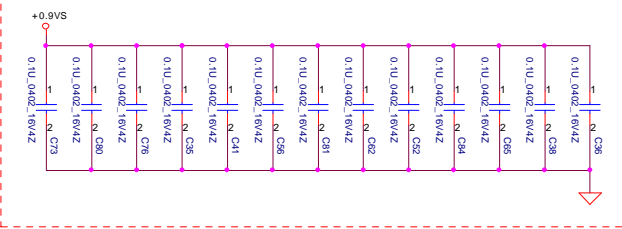
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DDR II - SODIMM SLOT I		
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- 8 DDR_B_DQS#[0..7]
- 8 DDR_B_D[0..63]
- 8 DDR_B_DM[0..7]
- 8 DDR_B_DQS[0..7]
- 8 DDR_B_MA[0..13]

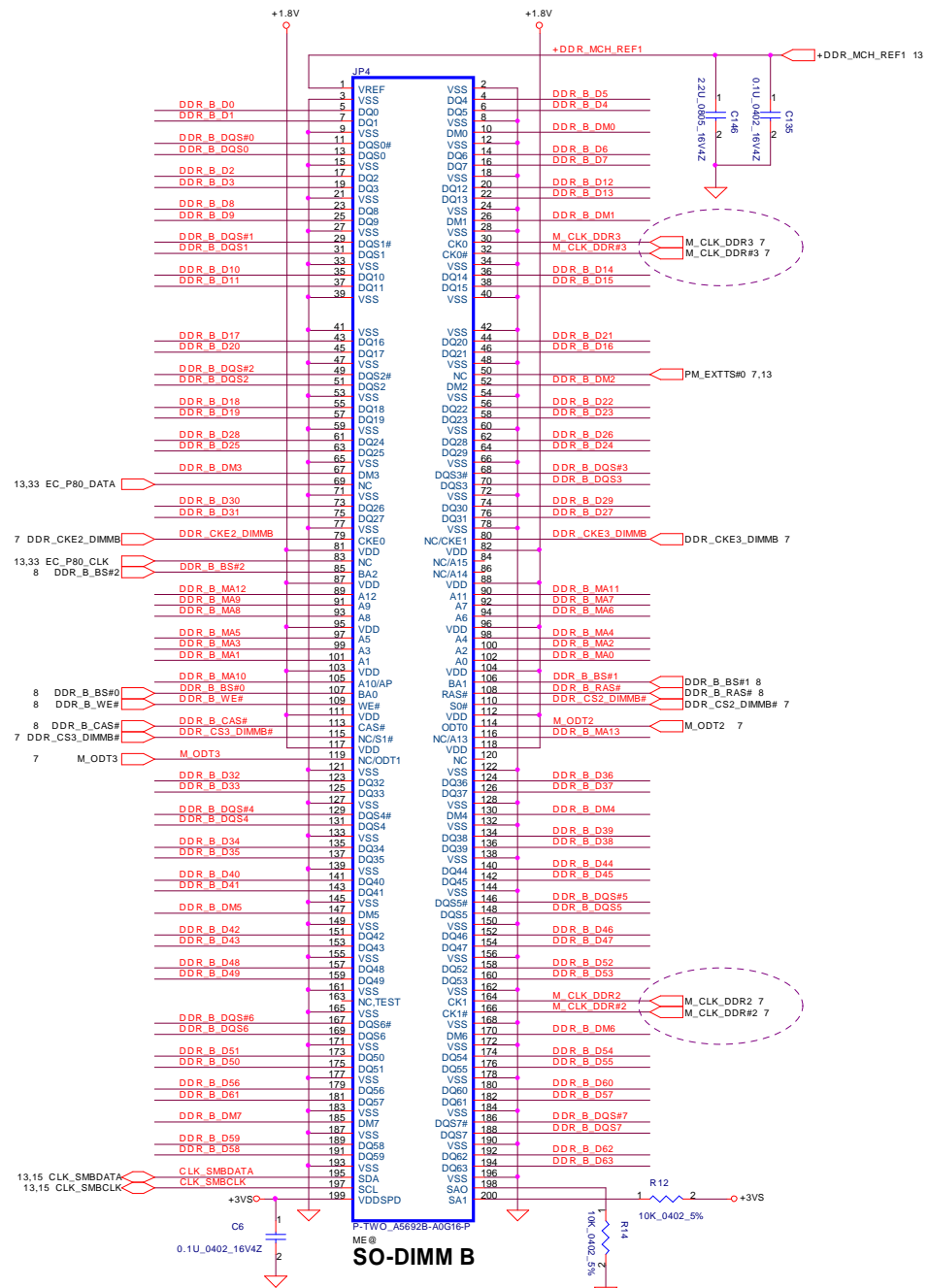
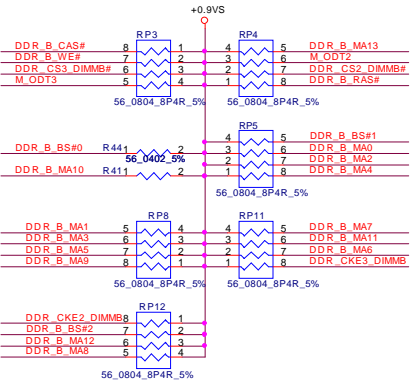
Layout Note:
Place near JP42



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistor closely JP42, all trace length Max=1.5"



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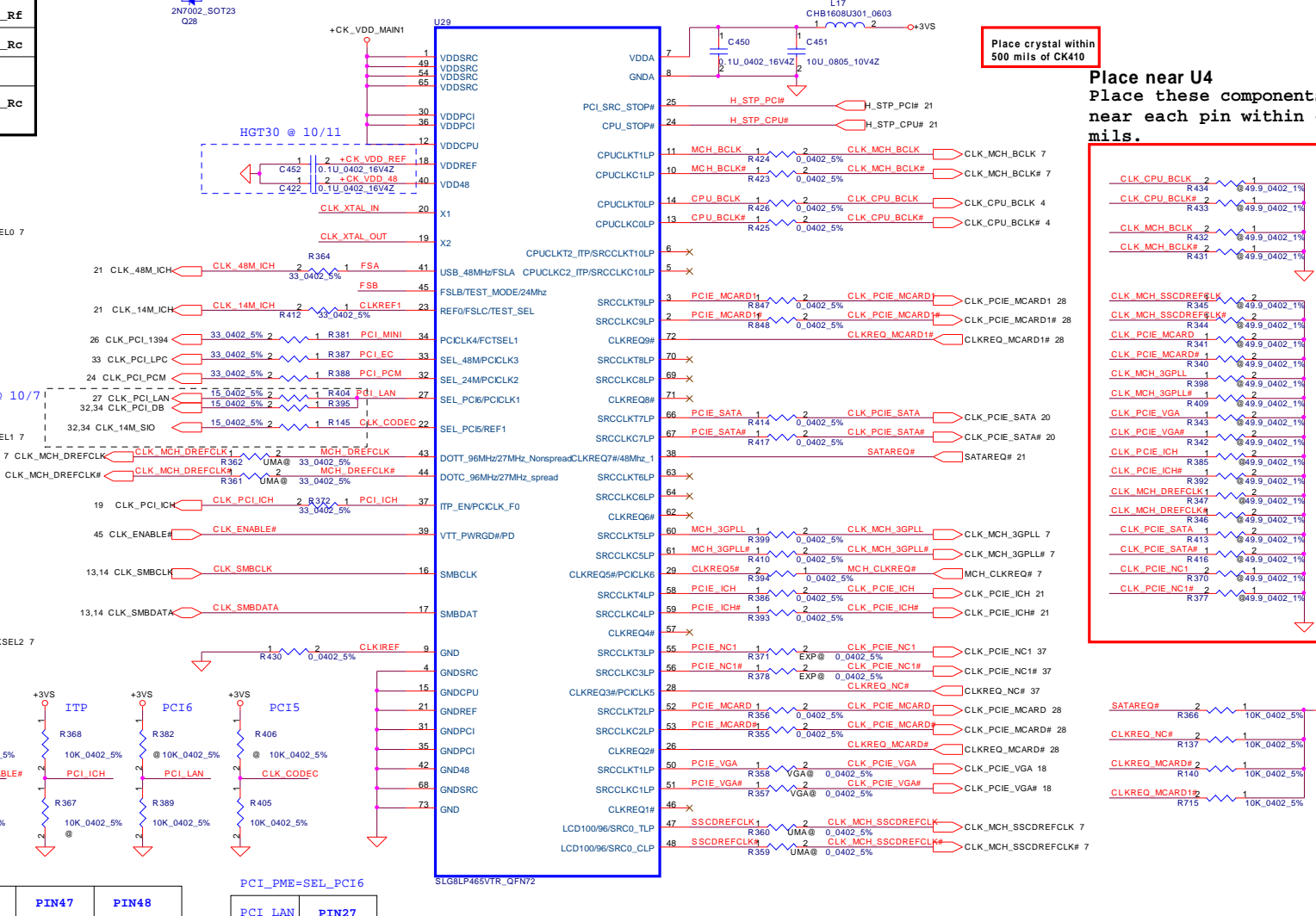
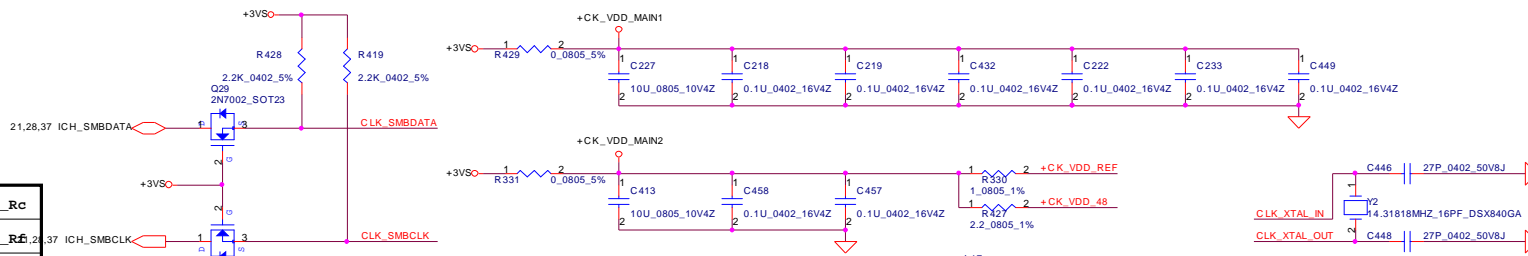
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DDR II - SODIMM SLOT2		
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FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	1	133	100	33.3
0	1	1	166	100	33.3

Table : ICS954306

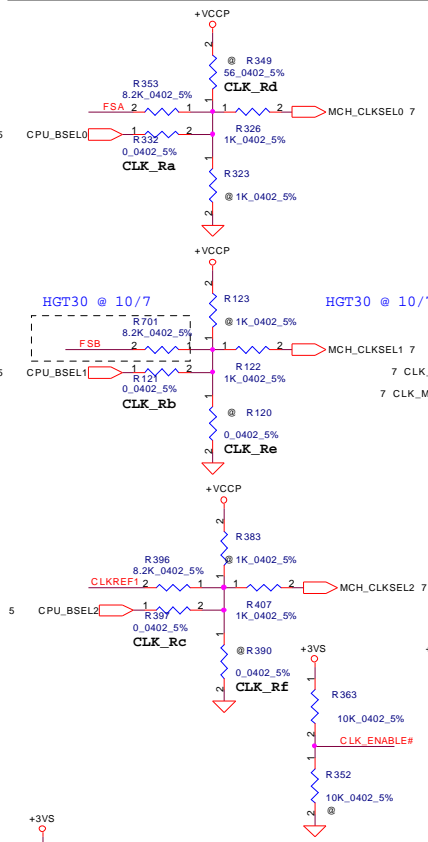
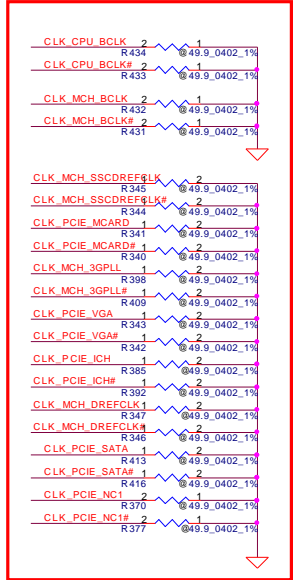
FSB Frequency Set:

CPU Driven	Stuff	CLK_Ra	CLK_Rb	CLK_Rc
	* (Default)	No Stuff	CLK_Rd	CLK_Re
533MHz	Stuff	CLK_Rd	CLK_Re	CLK_Rf
	No Stuff	CLK_Ra	CLK_Rb	CLK_Rc
667MHz	Stuff	CLK_Rd	CLK_Re	CLK_Rf
	No Stuff	CLK_Ra	CLK_Rb	CLK_Rc



Place crystal within 500 mils of CK410

Place near U4
Place these components near each pin within 40 mils.



PCI_MINI = FCTSEL1

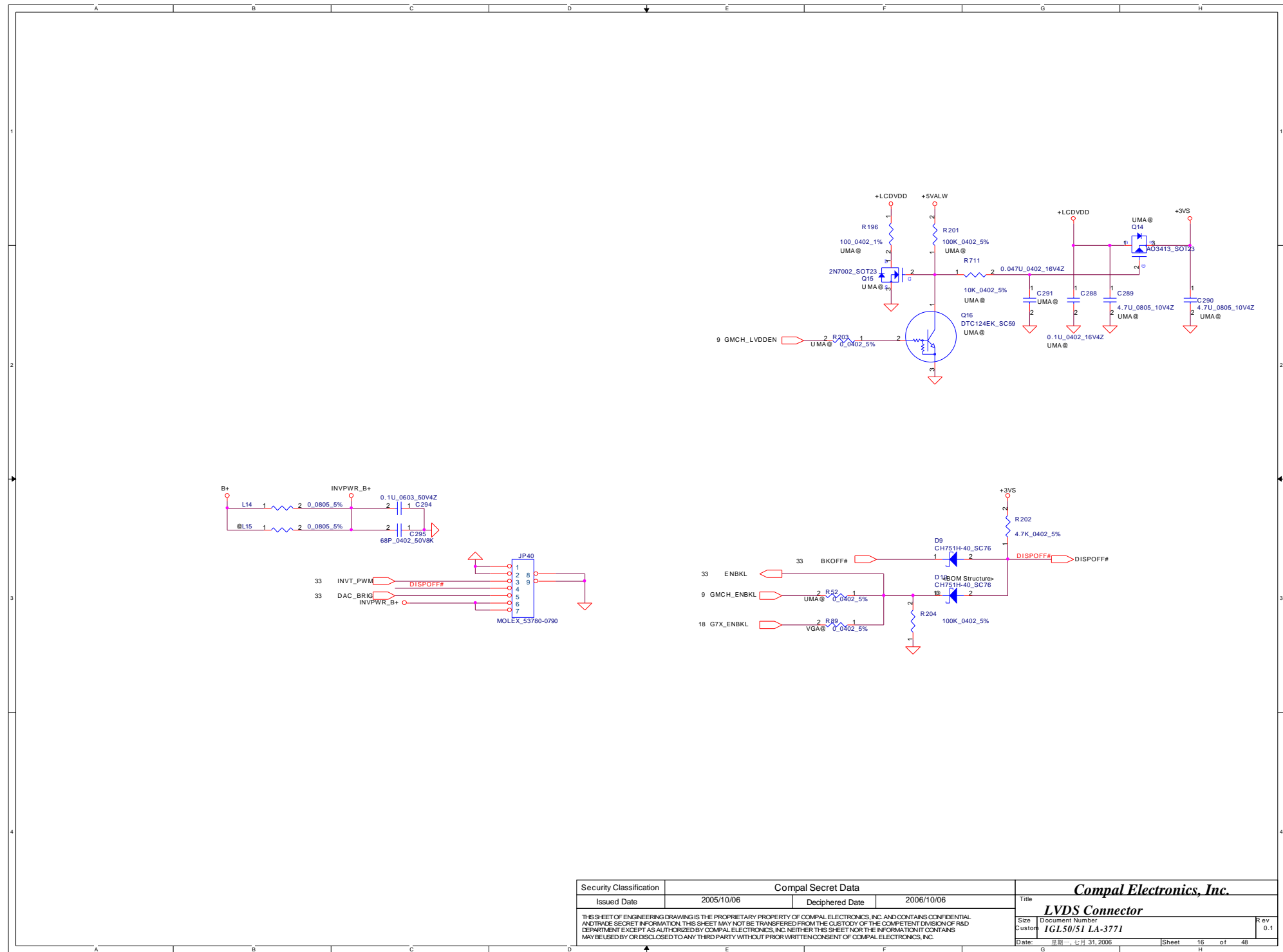
FCTSEL1 (PIN34)	PIN43	PIN44	PIN47	PIN48
0	DOT96T	DOT96C	96/100M_T	96/100M_C
1	27Mout	27MSout	SRCT0	SRCC0

PCI_PME=SEL_PCI6

PCI_LAN	PIN27
0	CLKREQ5
1	PCICLK6

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Compal Electronics, Inc.			
Clock generator			
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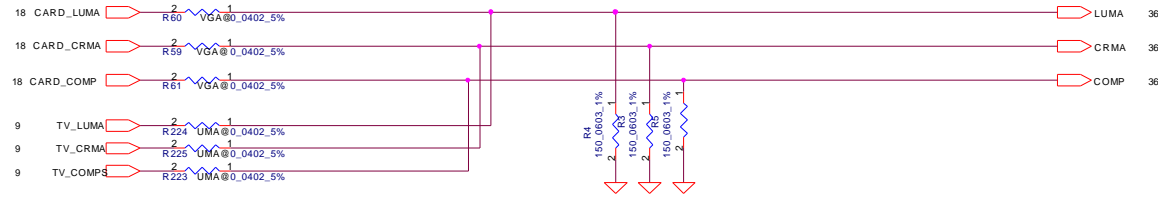


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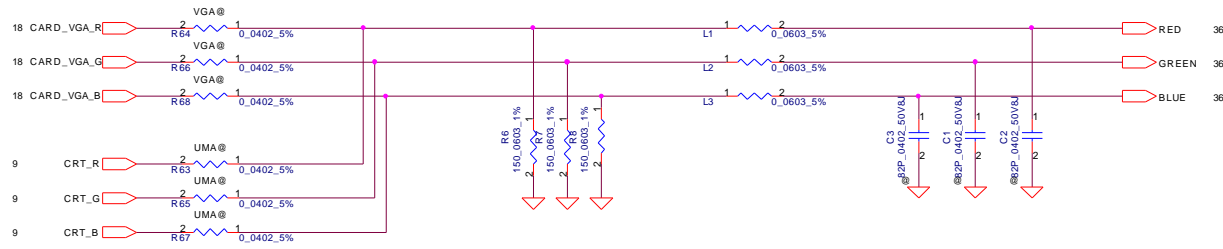
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LVDS Connector		
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TV-OUT Conn.

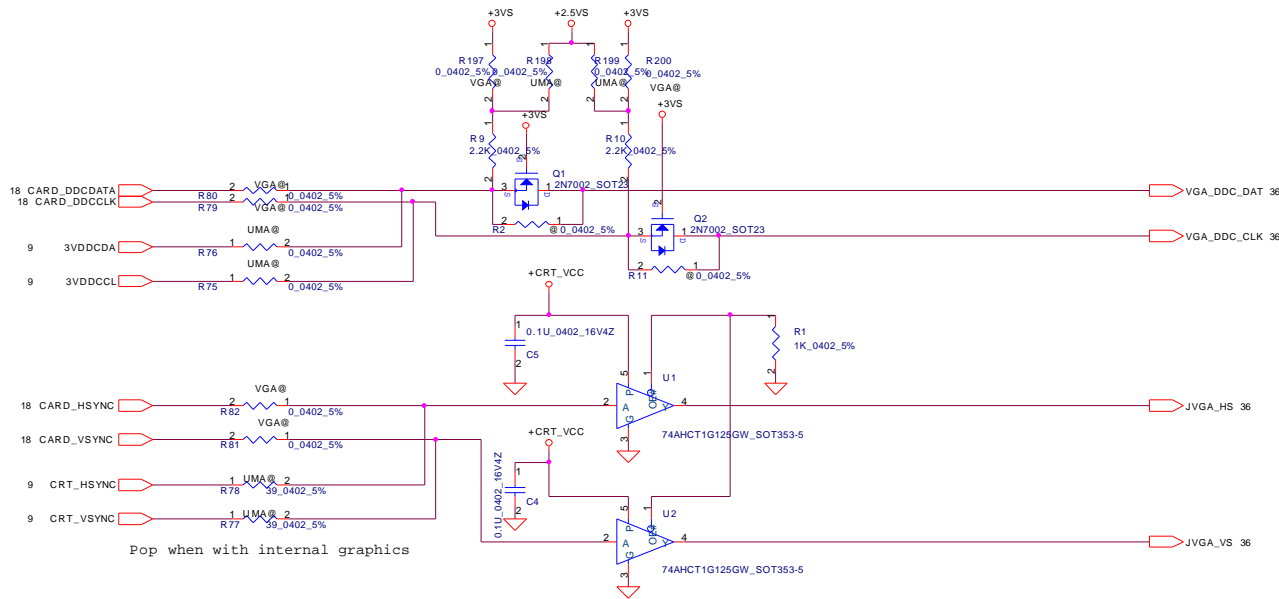


Pop when with internal graphics

CRT Conn.



Pop when with internal graphics

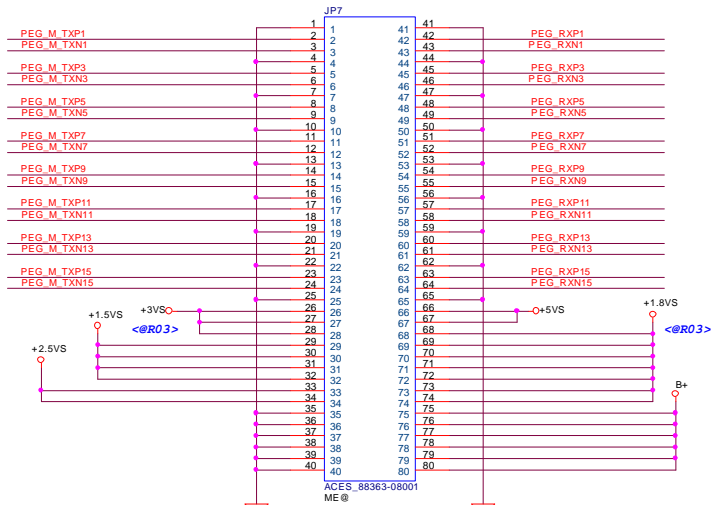


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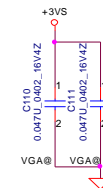
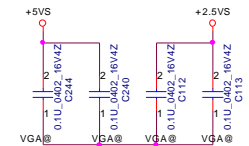
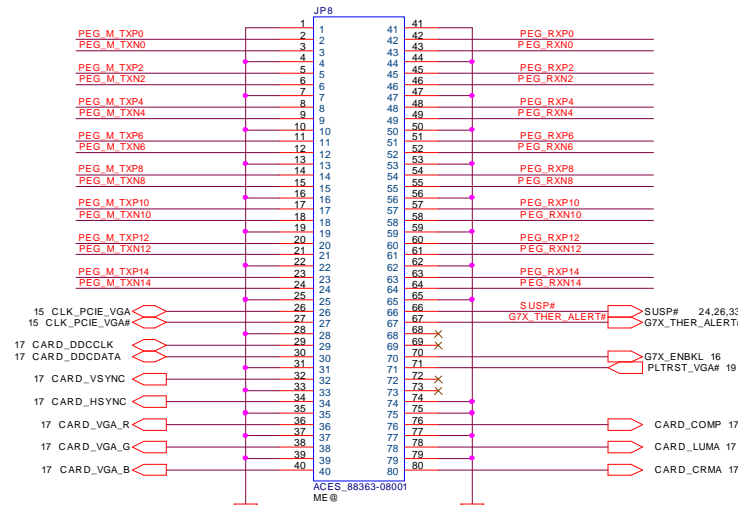
Compal Electronics, Inc.		
CRT & TVout		
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Date:	日期: 七月 31, 2006	Sheet 17 of 48

MAX. 4.06A @ 1.8V
 MAX. 130mA @ 2.5V
 MAX. 655mA @ 3.3V

PEG_M_TXP[0..15] PEG_M_TXN[0..15] 9
 PEG_M_TXN[0..15] PEG_M_TXN[0..15] 9
 PEG_RXP[0..15] PEG_RXP[0..15] 9
 PEG_RXN[0..15] PEG_RXN[0..15] 9



< New Add Pin.28 for +3VS, Pin.68 for +1.8VS @R03 >

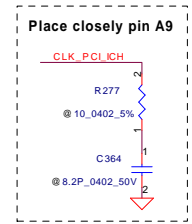
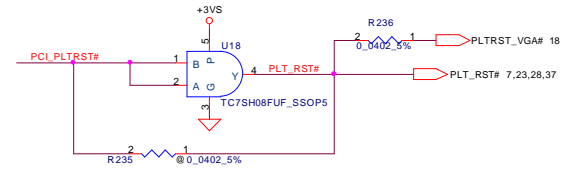
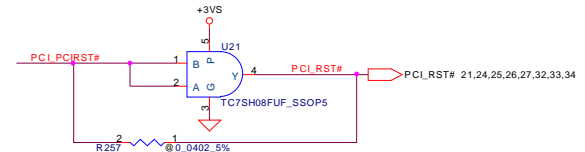
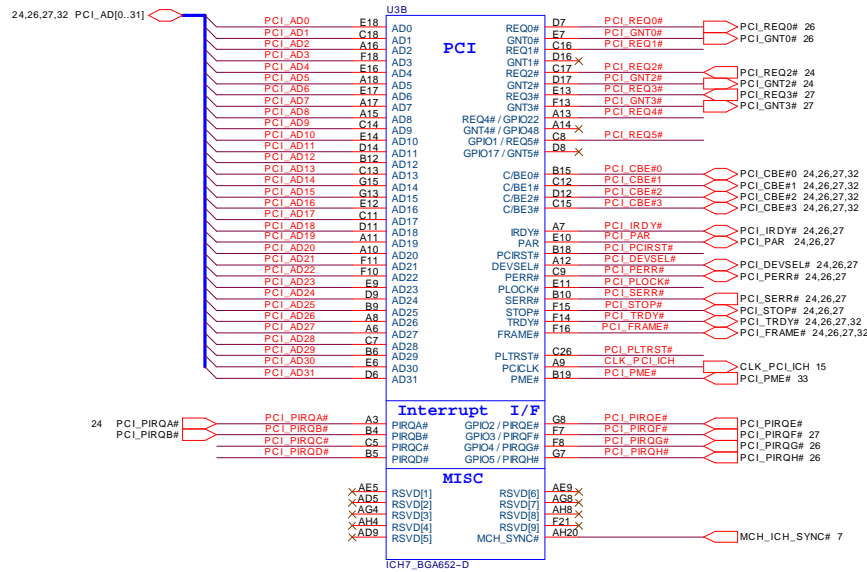
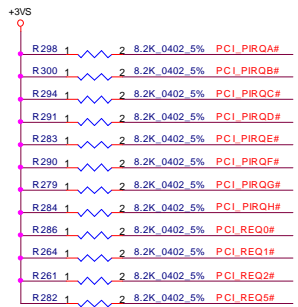
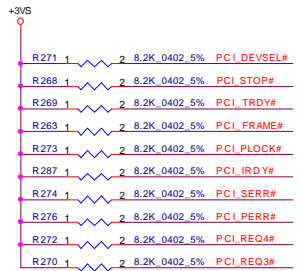


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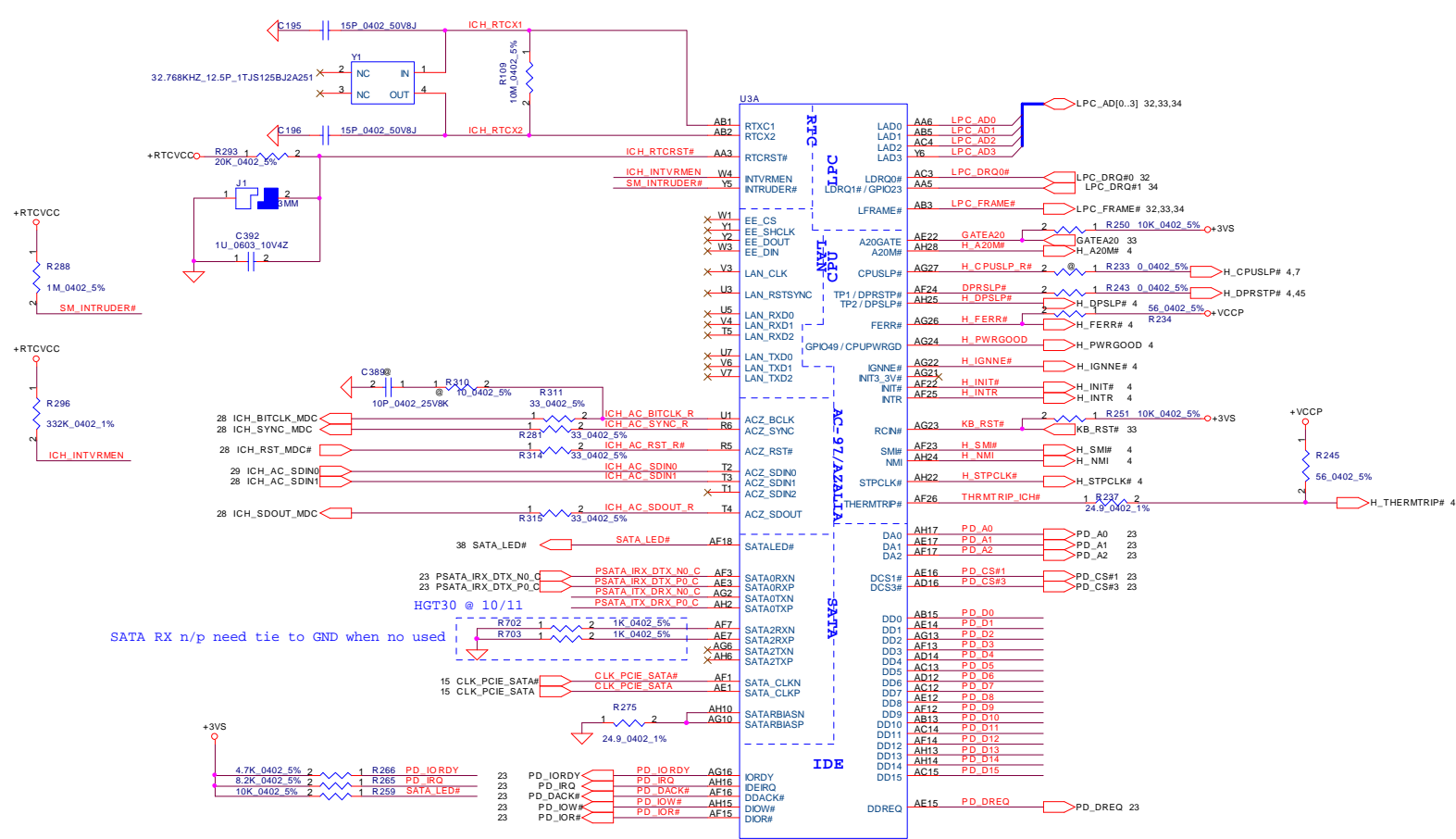
VGA/B connector

Title	VGA/B connector		Rev	0.1
Size	Document Number	IGL50/51 LA-3771		
Customer				
Date:	星期一, 七月 31, 2006	Sheet	18	of 48

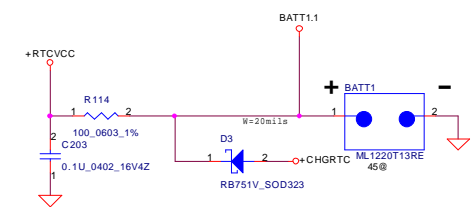
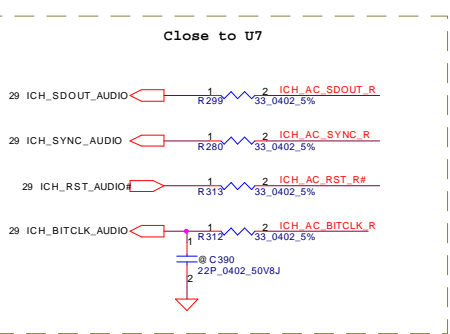
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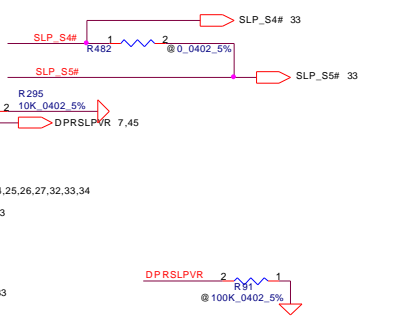
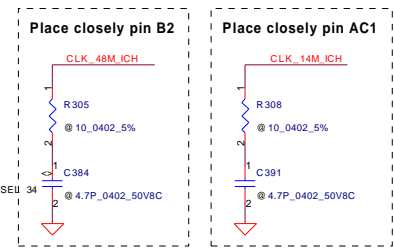
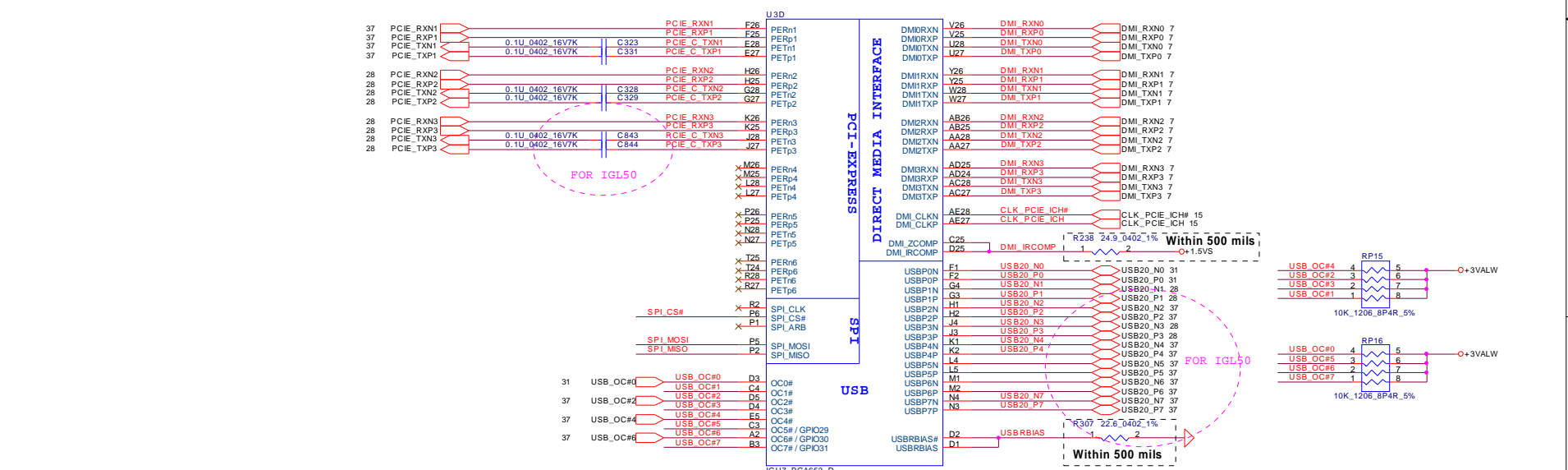
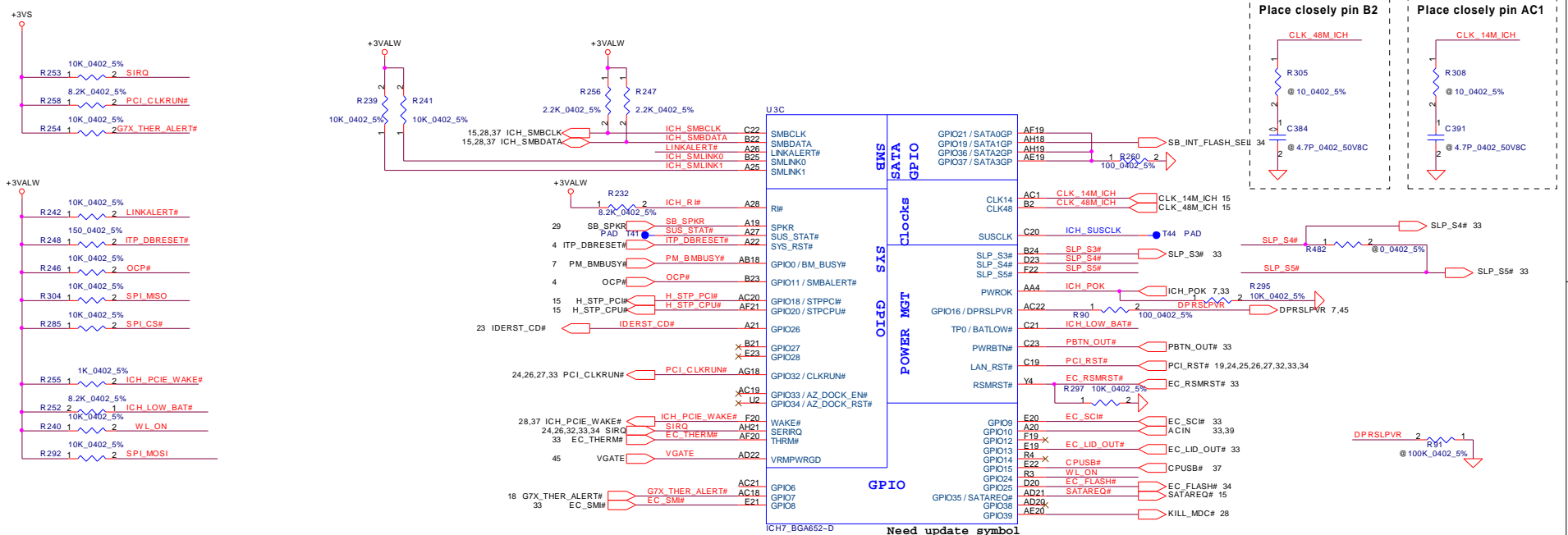
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				Date	Rev 0.1
				2006-07-31	Sheet 19 of 48



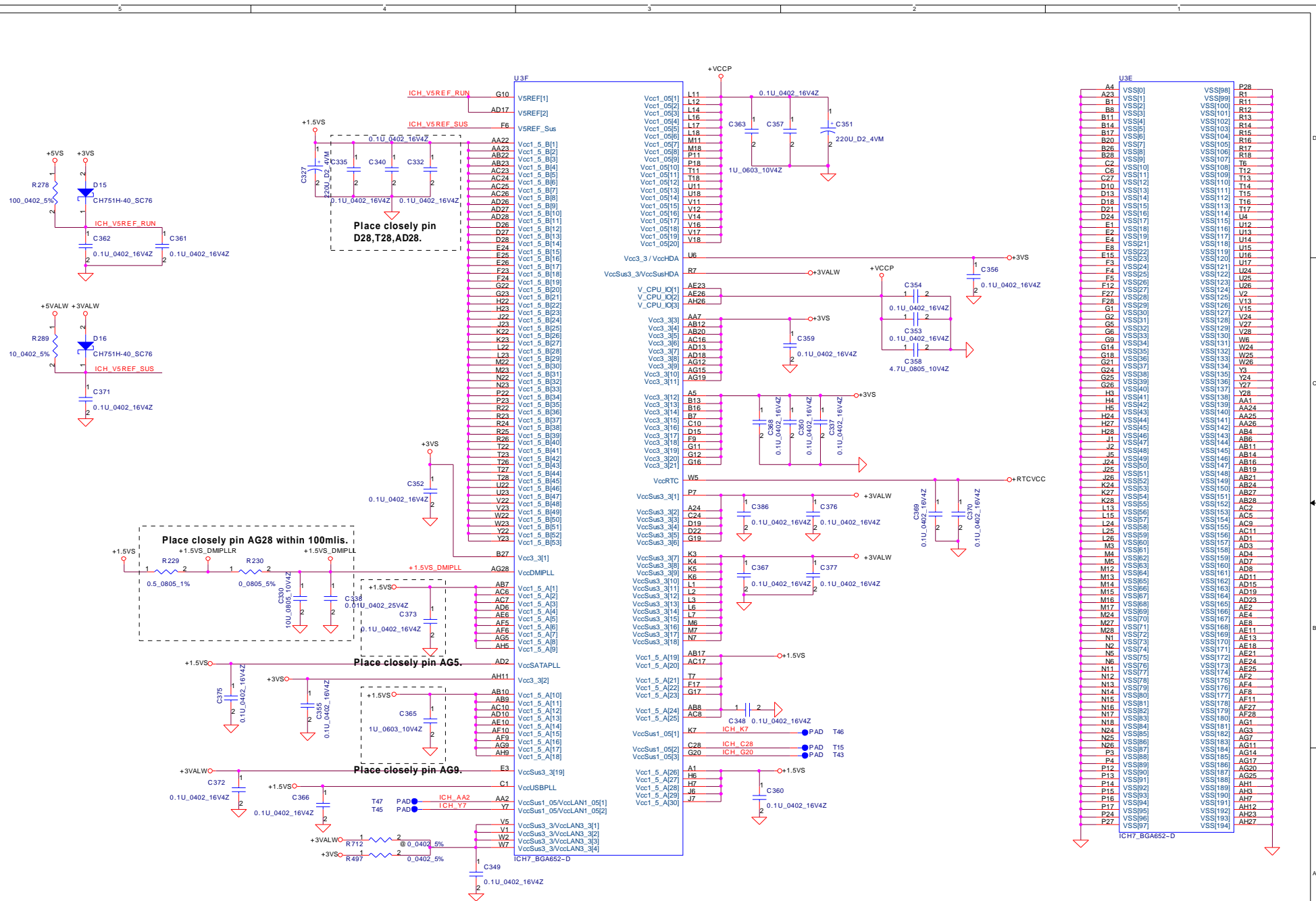
SATA RX n/p need tie to GND when no used



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Size	Document Number			Customer	Rev
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Date:	日期: 七月 31, 2006	Sheet	20	of	48

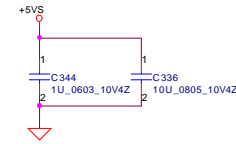
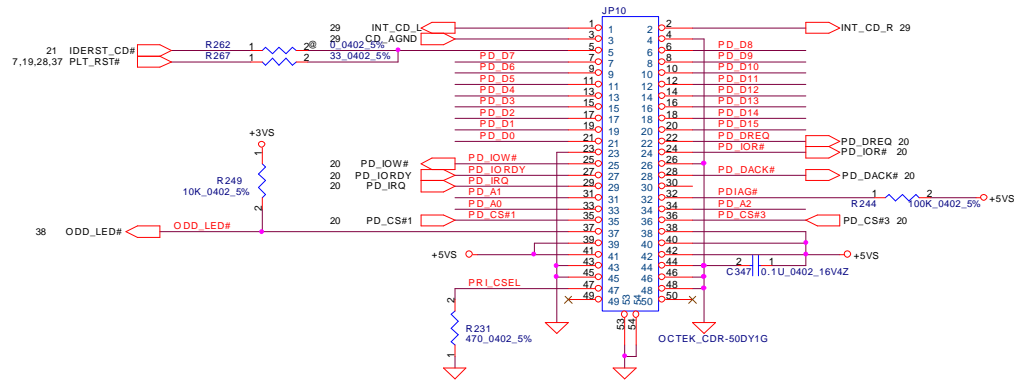
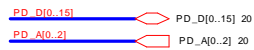
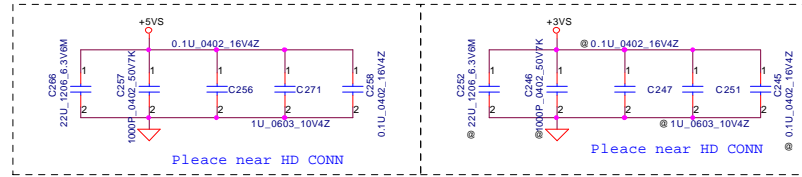
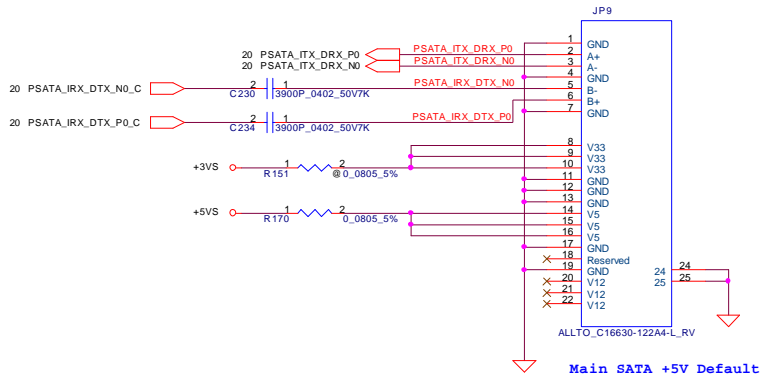


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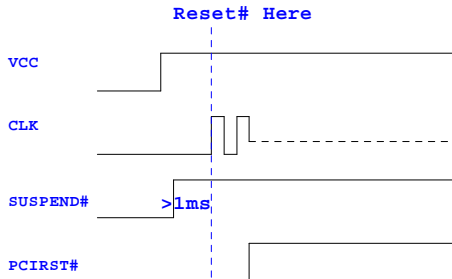
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Title	Document Number	Rev
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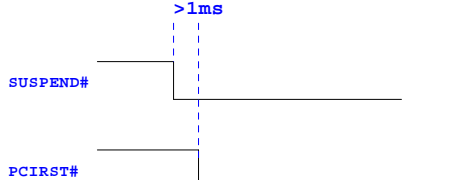


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Date:	日期: 七月 31, 2006	Sheet	23 of 48	Rev 0.1

Power on RESET#

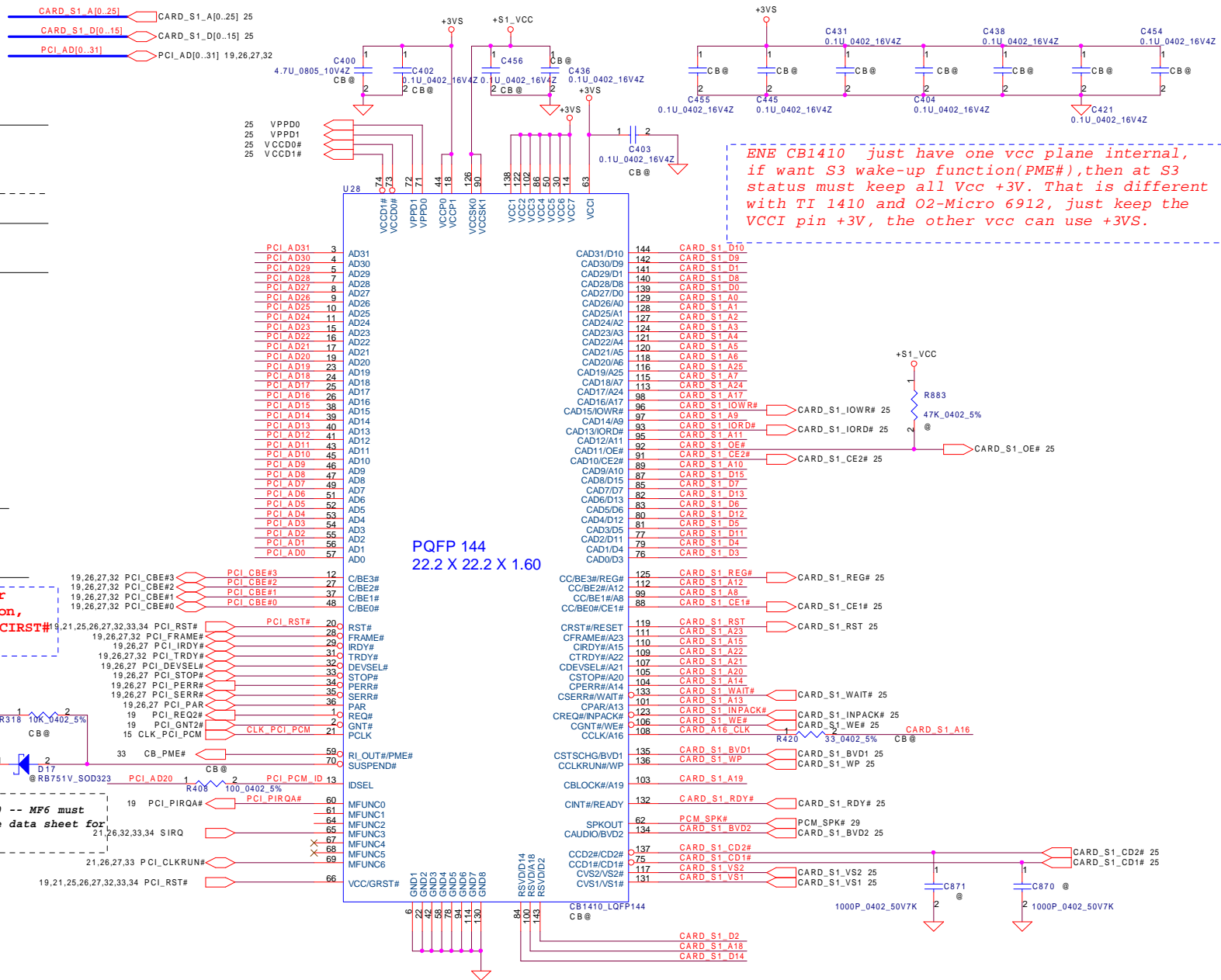


Entry S3



SUSPEND# will gate the PCIRST# or GRST#, so need S3 wake-up function, SUSPEND# must be LOW ahead the PCIRST# about 1ms.

Note: MF0 -- MF6 must refer the data sheet for design.



ENE CBI140 just have one vcc plane internal, if want S3 wake-up function(PMB#), then at S3 status must keep all Vcc +3V. That is different with TI 1410 and O2-Micro 6912, just keep the VCCI pin +3V, the other vcc can use +3VS.

PQC140
22.2 X 22.2 X 1.60

PCI AD31	3	AD31
PCI AD30	4	AD30
PCI AD29	5	AD29
PCI AD28	7	AD28
PCI AD27	8	AD27
PCI AD26	9	AD27
PCI AD25	10	AD26
PCI AD24	11	AD24
PCI AD23	15	AD25
PCI AD22	16	AD23
PCI AD21	17	AD22
PCI AD20	19	AD20
PCI AD19	23	AD19
PCI AD18	24	AD18
PCI AD17	25	AD18
PCI AD16	26	AD17
PCI AD15	38	AD16
PCI AD14	39	AD14
PCI AD13	40	AD13
PCI AD12	41	AD12
PCI AD11	43	AD12
PCI AD10	45	AD11
PCI AD9	46	AD9
PCI AD8	47	AD8
PCI AD7	49	AD8
PCI AD6	51	AD7
PCI AD5	52	AD5
PCI AD4	53	AD4
PCI AD3	54	AD3
PCI AD2	54	AD3
PCI AD1	56	AD2
PCI AD0	57	AD0

CAD31/D10	144	CARD S1 D10
CAD30/D9	142	CARD S1 D9
CAD29/D1	141	CARD S1 D1
CAD28/D8	138	CARD S1 D8
CAD27/D0	129	CARD S1 A0
CAD26/A0	128	CARD S1 A1
CAD25/A1	127	CARD S1 A2
CAD24/A2	124	CARD S1 A3
CAD23/A3	121	CARD S1 A4
CAD22/A4	120	CARD S1 A5
CAD21/A5	118	CARD S1 A6
CAD20/A6	116	CARD S1 A25
CAD19/A25	115	CARD S1 A7
CAD18/A7	113	CARD S1 A24
CAD17/A24	98	CARD S1 A17
CAD16/A17	96	CARD S1 IOWR#
CAD15/IOWR#	97	CARD S1 IORD#
CAD14/A9	83	CARD S1 IORD#
CAD13/IORD#	95	CARD S1 A11
CAD12/A11	92	CARD S1 OE#
CAD11/OE#	91	CARD S1 CE2#
CAD10/CE2#	89	CARD S1 A10
CAD9/A10	87	CARD S1 D15
CAD8/D15	85	CARD S1 D7
CAD7/D7	82	CARD S1 D13
CAD6/D13	83	CARD S1 D6
CAD5/D6	80	CARD S1 D12
CAD4/D12	81	CARD S1 D5
CAD3/D5	77	CARD S1 D11
CAD2/D11	79	CARD S1 D4
CAD1/D4	76	CARD S1 D3
CAD0/D3		

PCI CBE#3	12	C/BE#3
PCI CBE#2	27	C/BE#2
PCI CBE#1	37	C/BE#1
PCI CBE#0	48	C/BE#0
PCI RST#	20	RST#
PCI FRAME#	28	FRAME#
PCI IRDY#	29	IRDY#
PCI TRDY#	31	TRDY#
PCI DEVSEL#	32	DEVSEL#
PCI STOP#	33	STOP#
PCI PERR#	34	PERR#
PCI SERR#	35	SERR#
PCI PAR#	36	PAR#
PCI REQ2#	1	REQ#
PCI GNT2#	2	GNT#
CLK_PCI_PCM	21	CLK
CB_PME#	59	RL_OUT#/PME#
PCI AD20	1	SUSPEND#
PCI PIRQA#	60	IDSEL
PCI PIRQB#	61	MFUNC0
PCI PIRQC#	62	MFUNC1
PCI PIRQD#	63	MFUNC2
PCI PIRQE#	64	MFUNC3
PCI PIRQF#	65	MFUNC4
PCI PIRQG#	66	MFUNC5
PCI PIRQH#	67	MFUNC6
PCI SIRQ	21,26,32,33,34	SIRQ
PCI_CLKRUN#	21,26,27,33	CLKRUN#
PCI_RST#	19,21,25,26,27,32,33,34	RST#

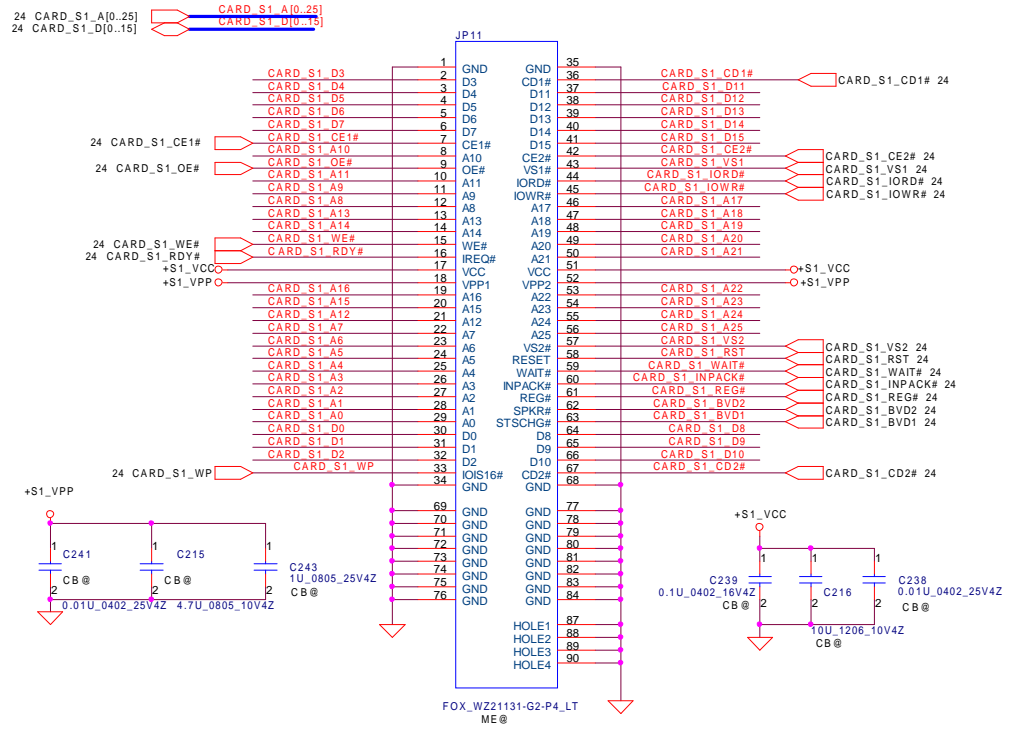
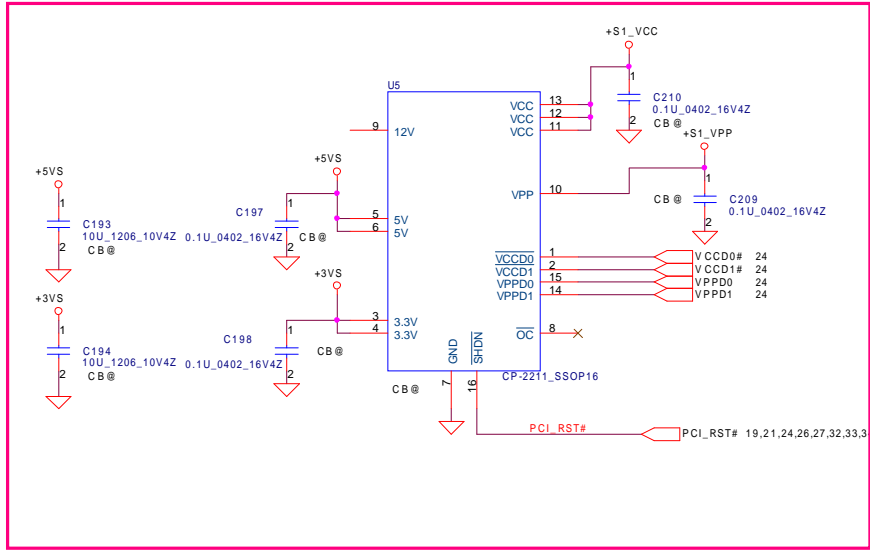
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CC/BE1#/A8	99	CARD S1 A8
CC/BE0#/CE1#	88	CARD S1 CE1#
CRST#/RESET	119	CARD S1 RST
CFRAME#/A23	111	CARD S1 A23
CRDY#/A15	110	CARD S1 A15
CTRDY#/A22	109	CARD S1 A22
CDEVSEL#/A21	107	CARD S1 A21
CSTOP#/A20	105	CARD S1 A20
CPERR#/A14	104	CARD S1 A14
CSERR#/A7#	133	CARD S1 WAIT#
CPAR/A13	101	CARD S1 A13
CREQ#/INPACK#	123	CARD S1_INPACK#
CAGNT#/WE#	108	CARD S1_WE#
CCLK/A16	108	CARD S1_A16
CSTSCHG/BVD1	135	CARD S1_BVD1
CCLKRUN#/WP	136	CARD S1_WP
CBLOCK#/A19	103	CARD S1 A19
CINT#/READY	132	CARD S1_RDY#
SPKOUT	62	PCM_SPK#
CAUDIO/BVD2	134	CARD S1_BVD2
CCD2#/CD2#	137	CARD S1_CD2#
CCD1#/CD1#	137	CARD S1_CD1#
CVS2/VS2#	131	CARD S1_VS2
CVS1/VS1#	131	CARD S1_VS1

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Title CB ENE1410(One Solt)		
Size	Document Number	Rev
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PROPRIETARY NOTE

PCMCIA Power Controller



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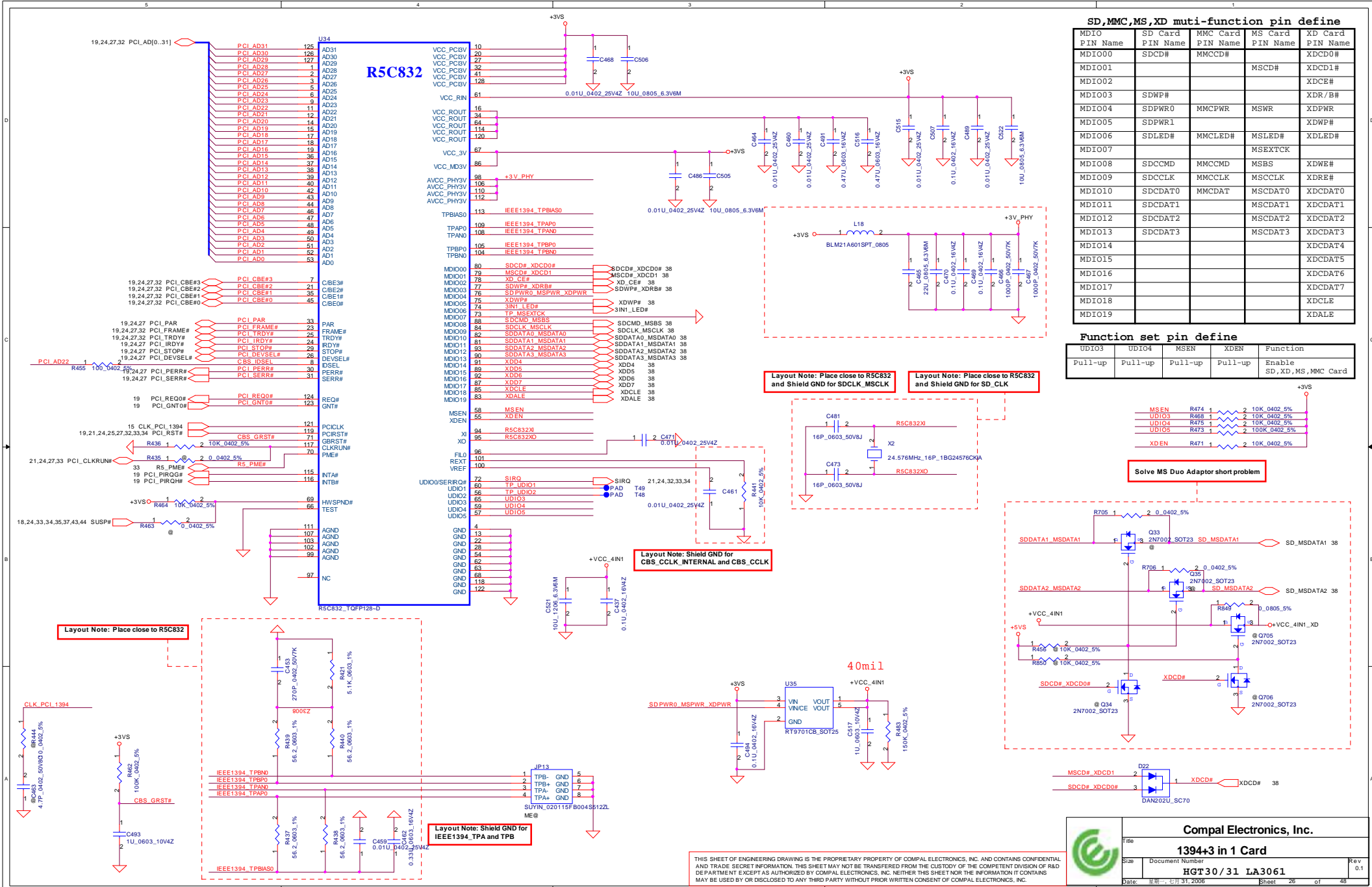
SD,MMC,MS,XD muti-function pin define

MDIO PIN Name	SD Card PIN Name	MMC Card PIN Name	MS Card PIN Name	XD Card PIN Name
MDIO00	SDCD#	MMCCD#		XDCD0#
MDIO01			MSCD#	XDCD1#
MDIO02				XDCB#
MDIO03	SDWP#		XDR/#	
MDIO04	SDPWR0	MMCPWR	MSWR	XDPWR
MDIO05	SDPWR1			XDWP#
MDIO06	SDLED#	MMCLEB#	MSLED#	XDLED#
MDIO07			MSEXTC#	
MDIO08	SDCCMD	MMCCMD	MSB#	XDWE#
MDIO09	SDCCLK	MMCCLK	MSCCLK	XDRE#
MDIO10	SDCDAT0	MMCDAT	MSCDAT0	XDCDAT0
MDIO11	SDCDAT1		MSCDAT1	XDCDAT1
MDIO12	SDCDAT2		MSCDAT2	XDCDAT2
MDIO13	SDCDAT3		MSCDAT3	XDCDAT3
MDIO14				XDCDAT4
MDIO15				XDCDAT5
MDIO16				XDCDAT6
MDIO17				XDCDAT7
MDIO18				XDCLC
MDIO19				XDALE

Function set pin define

UDIO3	UDIO4	MSEN	XDEN	Function
Pull-up	Pull-up	Pull-up	Pull-up	Enable SD, XD, MS, MMC Card

R5C832



Layout Note: Place close to R5C832 and Shield GND for SDCLK, MSCLK and Shield GND for SD, CLK

Layout Note: Place close to R5C832 and Shield GND for SDCLK, MSCLK

Layout Note: Place close to R5C832 and Shield GND for SD, CLK

Solve M5 Duo Adaptor short problem


Layout Note: Shield GND for CBS_CCLK, INTERNAL and CBS_CCLK

40mil

Layout Note: Shield GND for IEEE1394_TPA and TPB

Layout Note: Place close to R5C832

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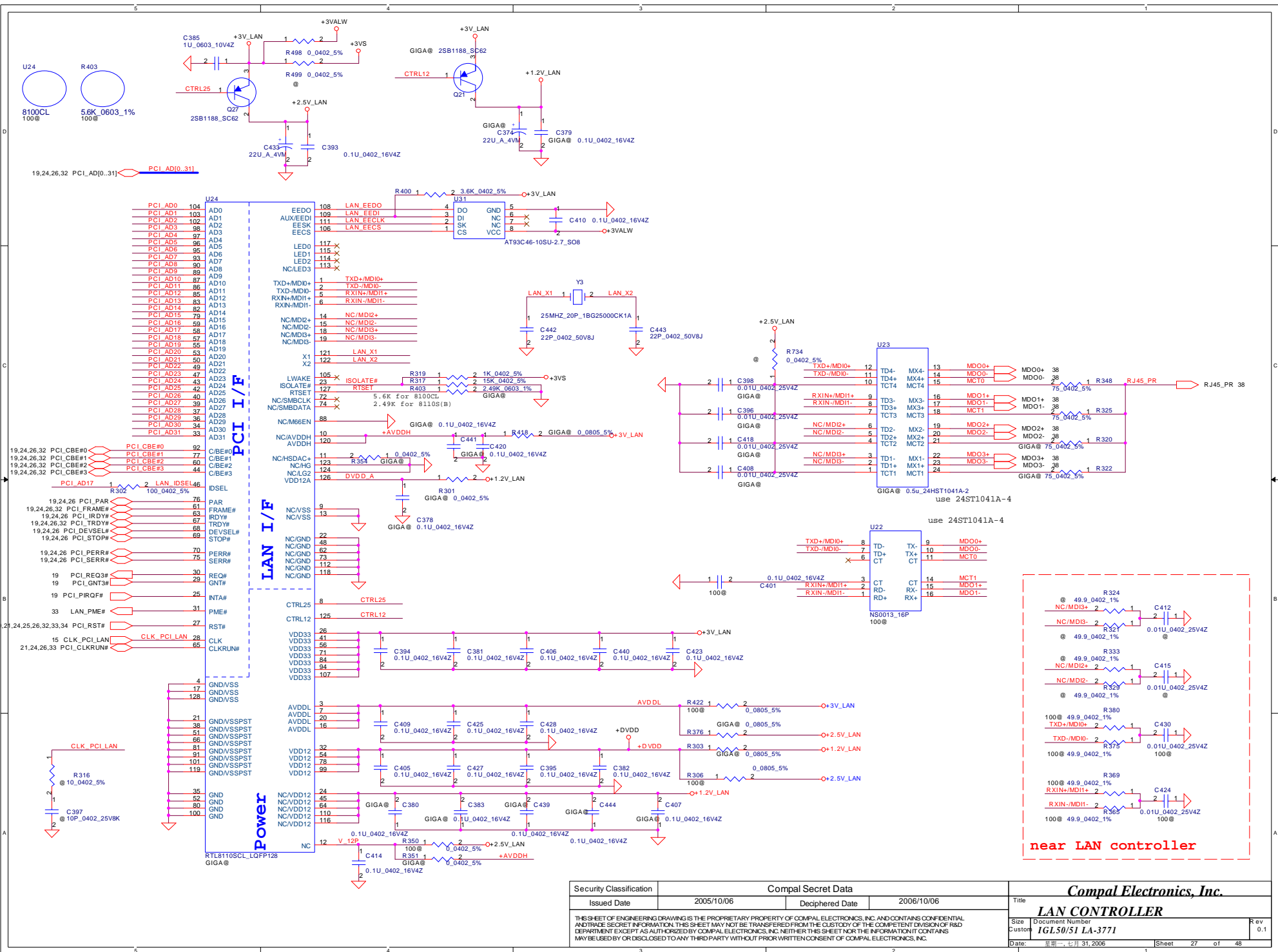
Compal Electronics, Inc.

Title
1394+3 in 1 Card

Doc Number
HGT30 / 31 LA3061

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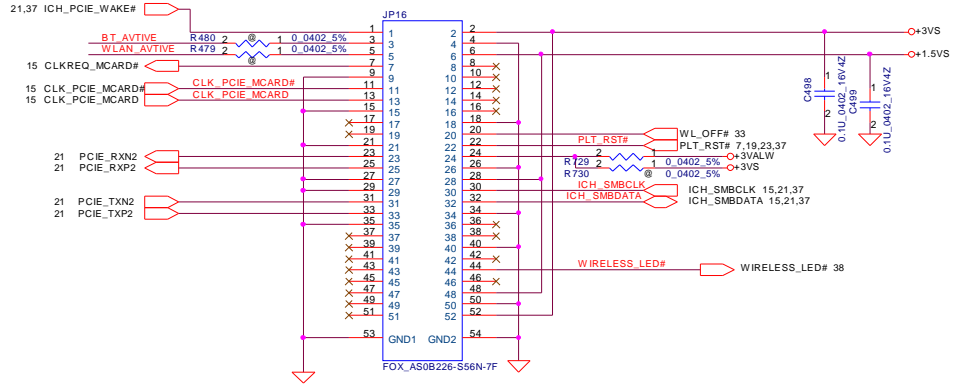
Rev 0.1



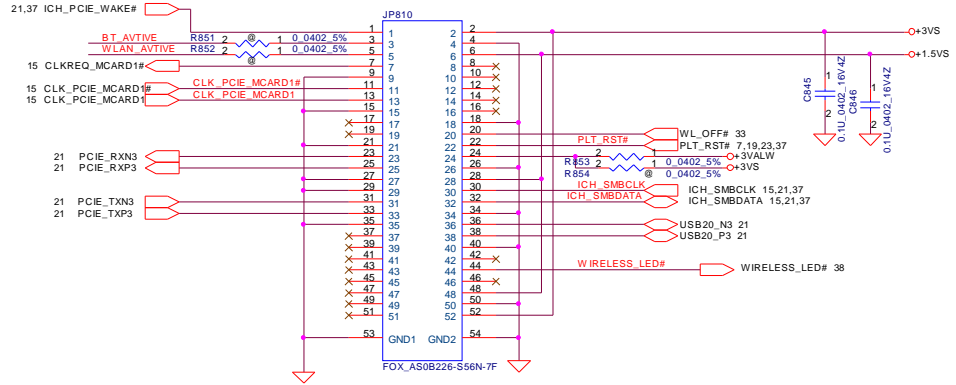
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LAN CONTROLLER		
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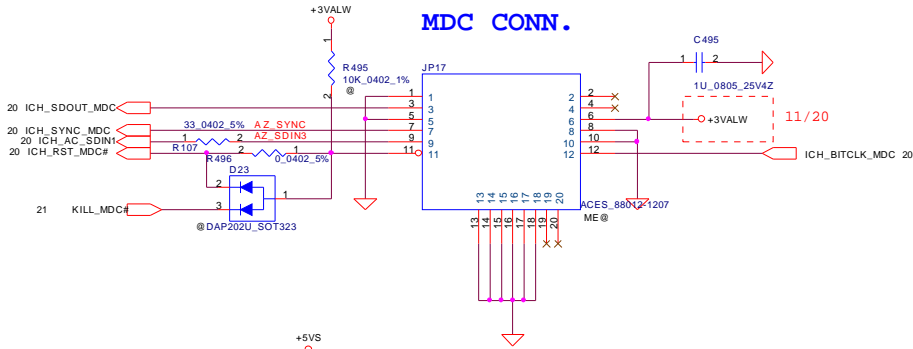
Mini-Express Card(Slot 1-WLAN)



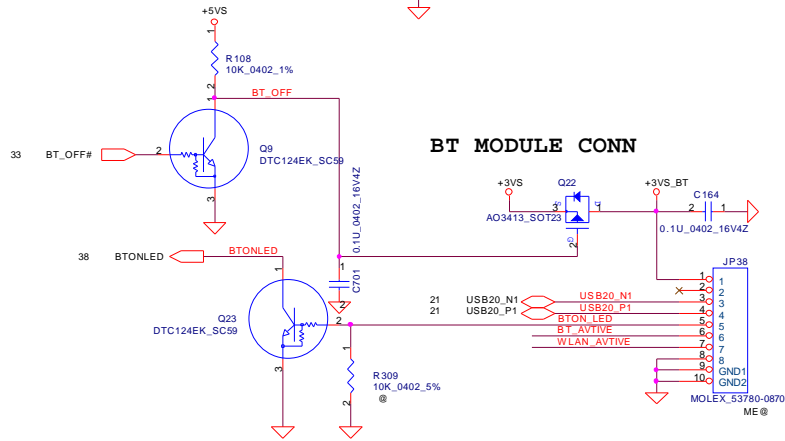
Mini-Express Card(Slot 2-WLAN)



MDC CONN.

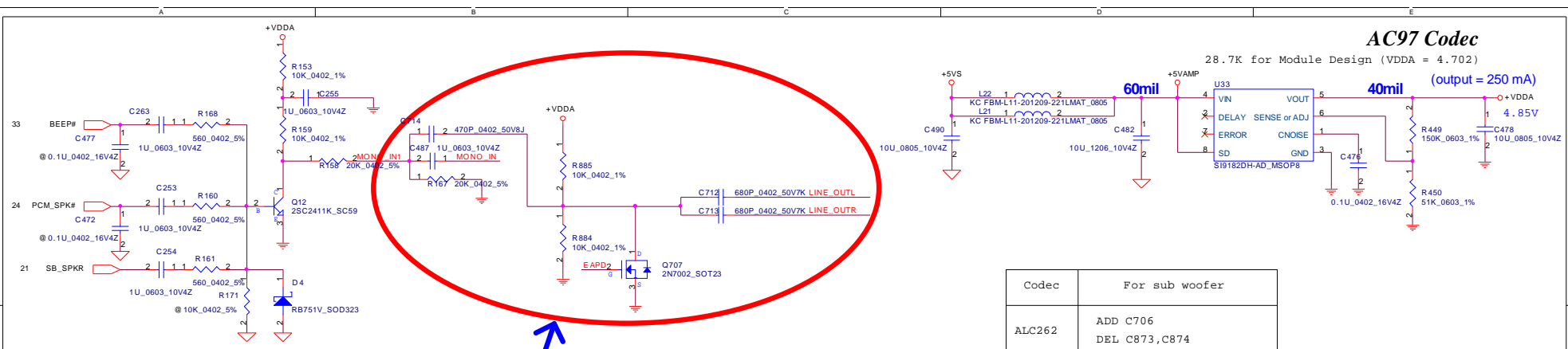


BT MODULE CONN



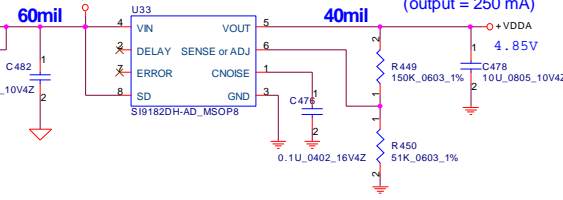
Security Classification	Compal Secret Data	
Issued Date	2005/10/06	Deciphered Date 2006/10/06
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Compal Electronics, Inc.		
Mini Card / MDC CONN		
Size	Document Number	Rev
Customer	IGL50/51 LA-3771	0.1
Date:	日期: 七月 31, 2006	Sheet 28 of 48

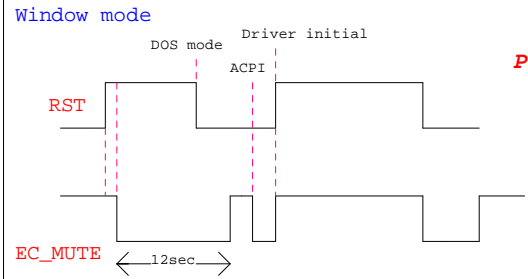


AC97 Codec

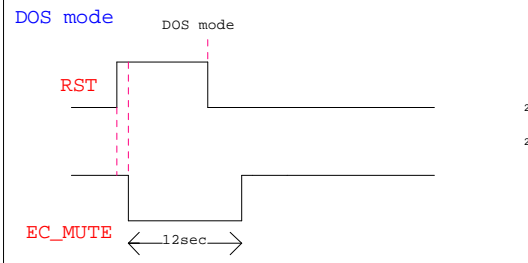
28.7K for Module Design (VDDA = 4.702)



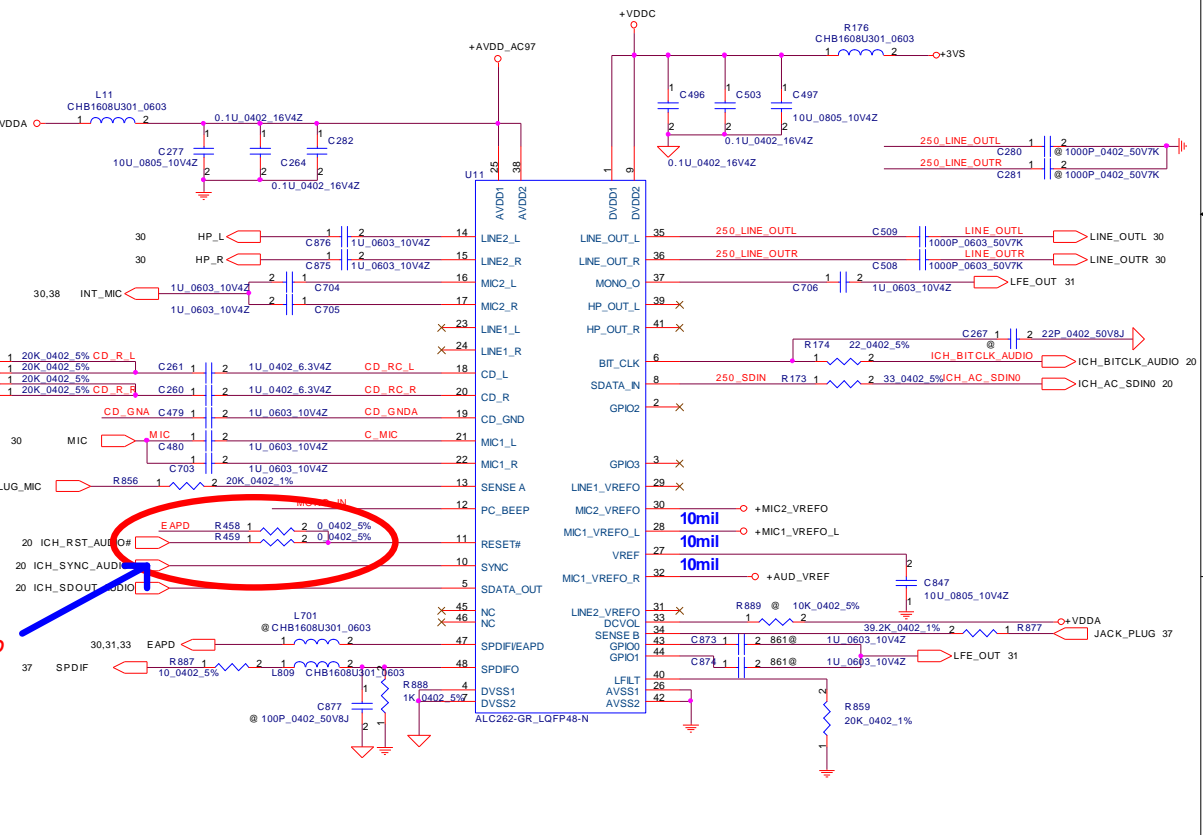
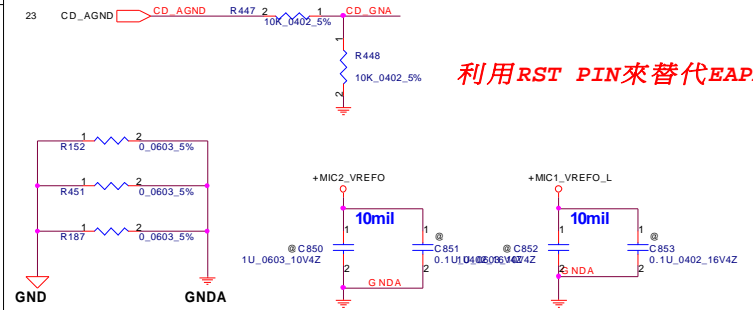
Codec	For sub woofer
ALC262	ADD C706 DEL C873, C874
ALC861D	ADD C873, C874 DEL C706



PC Beep for DOS mode

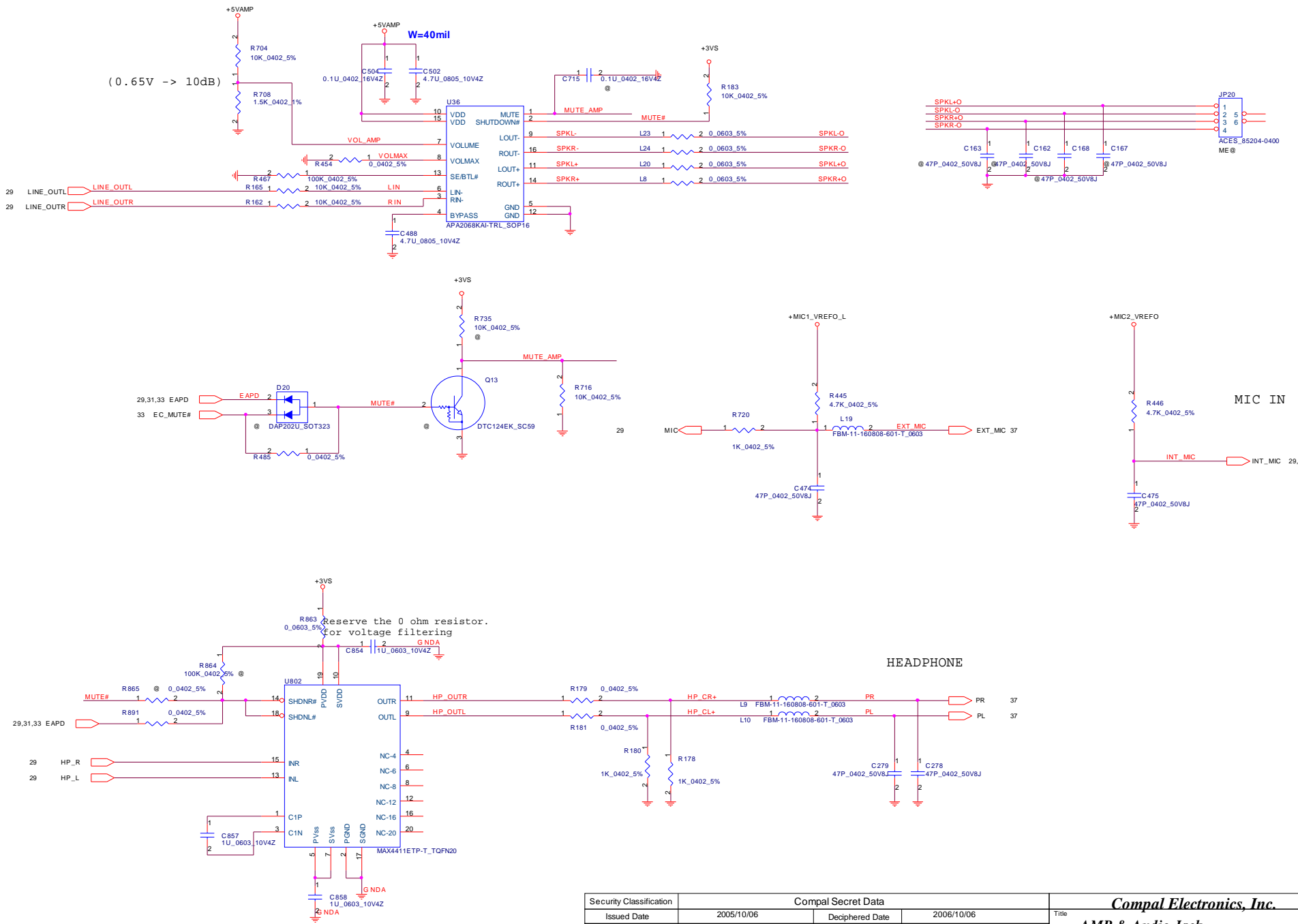


利用 RST PIN 來替代 EAPD



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Compal Electronics, Inc.		
Title: ALC262 Codec		
Size	Document Number	Rev
Custom	1GL50/51 LA-3771	0.1
Date	日期: 七月 31, 2006	Sheet 29 of 48

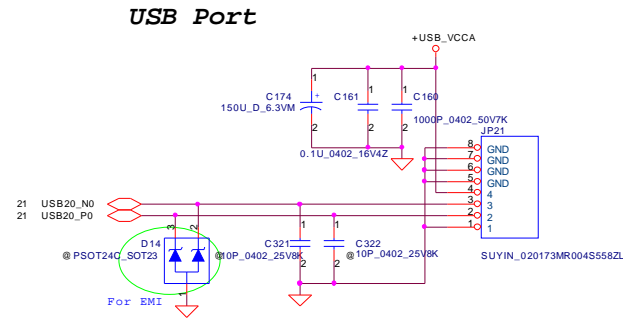
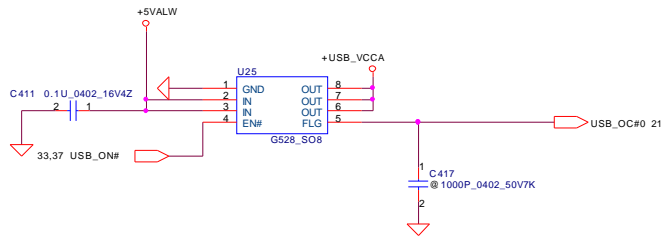
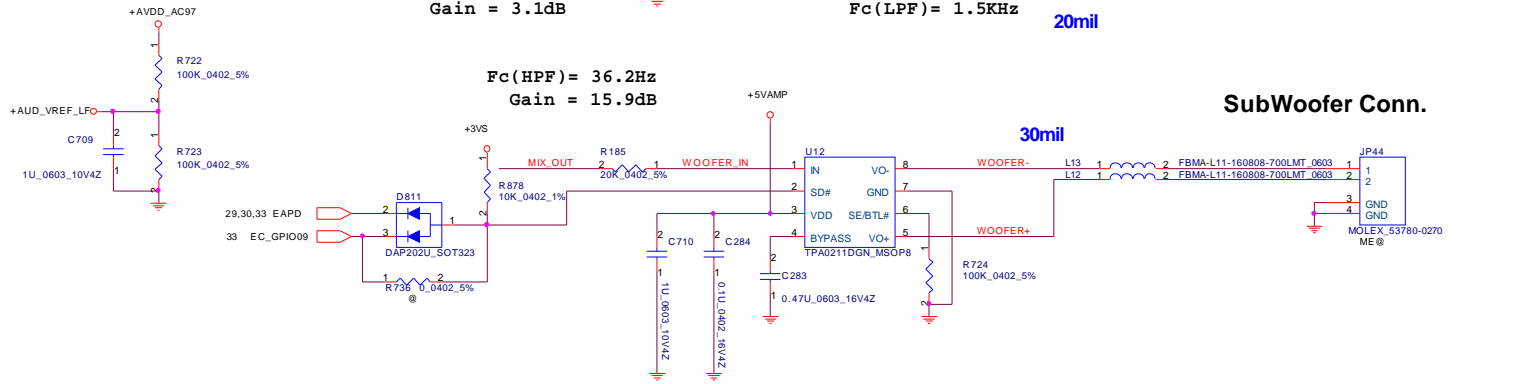
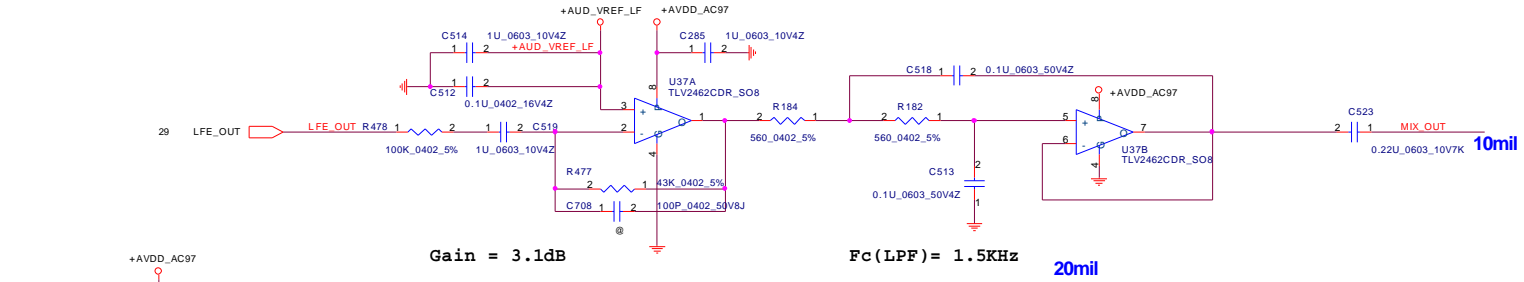


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Issued Date	2005/10/06	Deciphered Date
		2006/10/06
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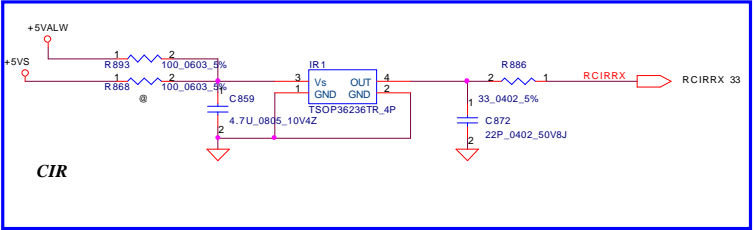
Compal Electronics, Inc.		
AMP & Audio Jack		
Size	Document Number	Rev
Custom	IGL50/51 LA-3771	0.1
Date:	日期: 七月 31, 2006	Sheet 30 of 48

SUBWOOFER (Reserved for C38)

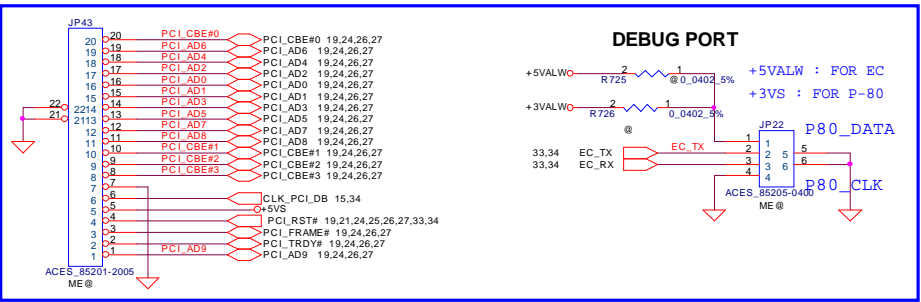
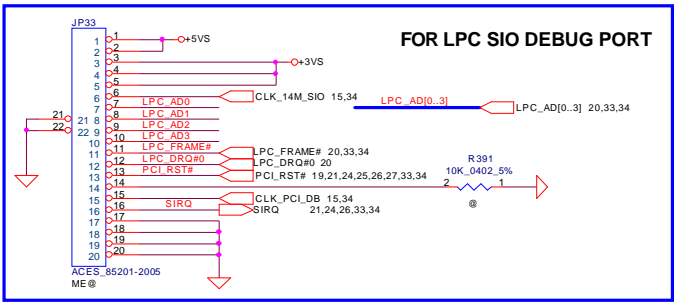
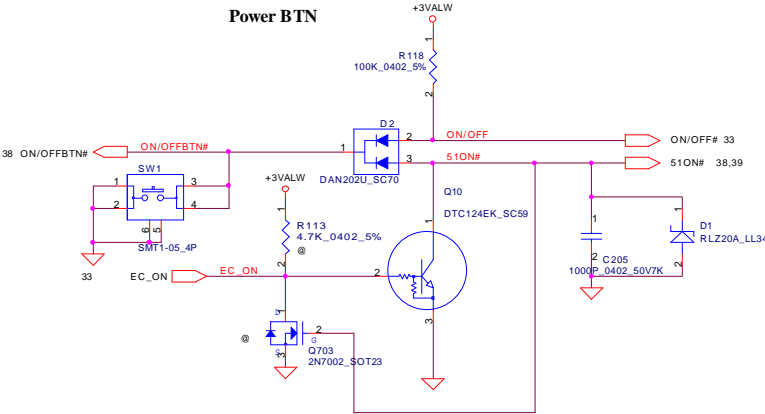
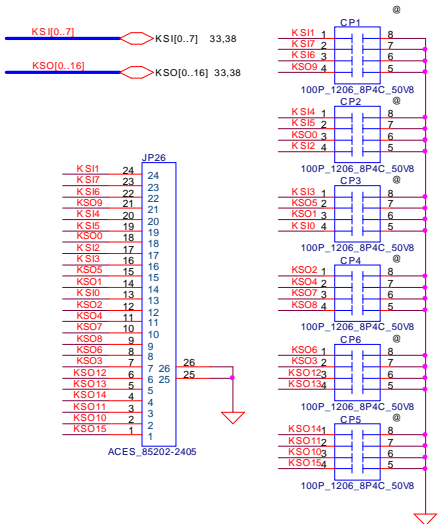
WOOFER@



Security Classification	Compal Secret Data		Title	
Issued Date	2005/10/06	Deciphered Date	2006/10/06	Bluetooth & USB CONN.
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Date:	星期二, 六月 01, 2006	Sheet	31	of 48



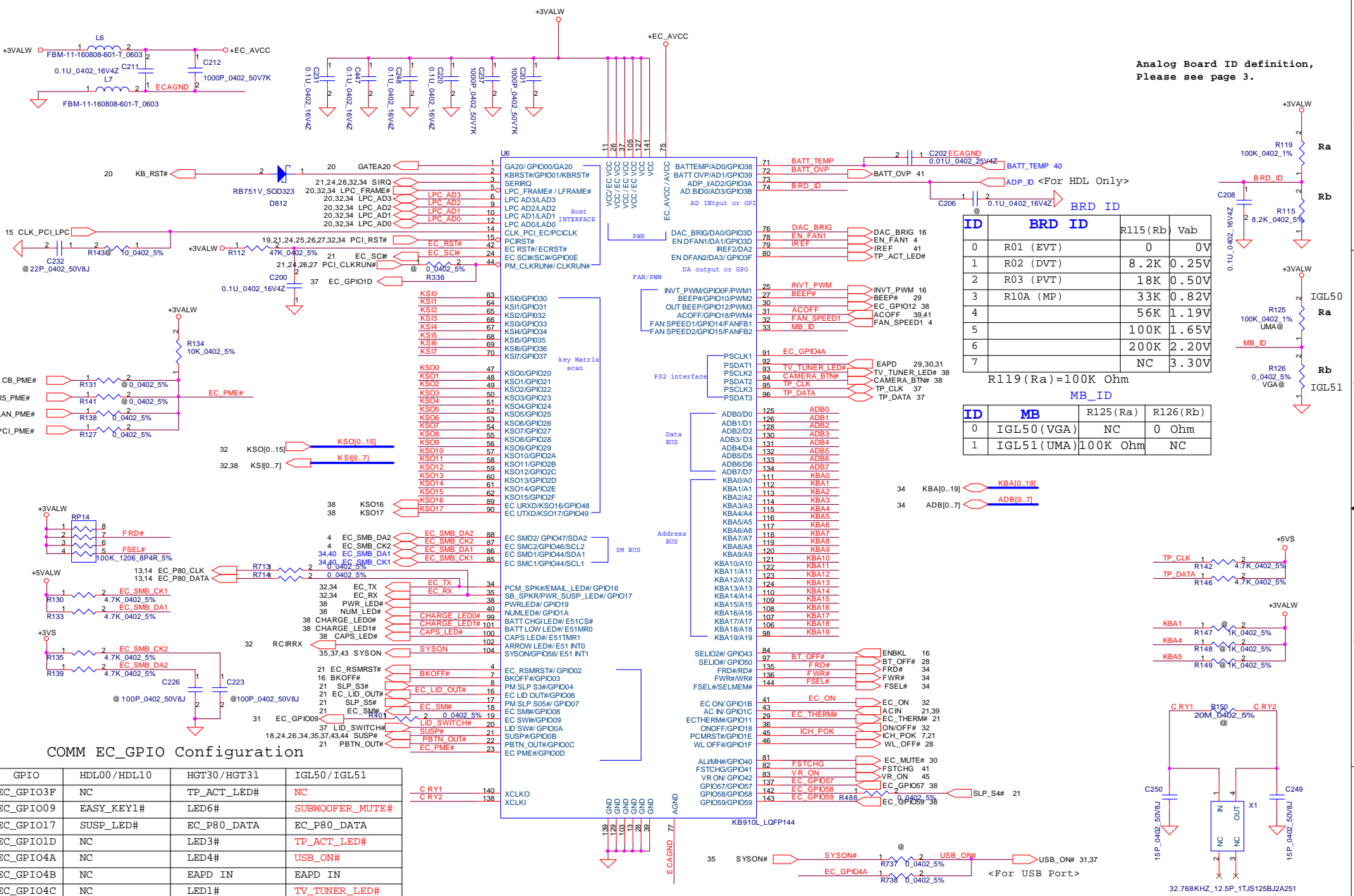
INT_KBD CONN.(TYPE "D" KB)



Security Classification	Compal Secret Data	
Issued Date	2005/10/06	Deciphered Date
		2006/10/06
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Compal Electronics, Inc.	
KBD_ON/OFF,T/P,LED/B,DEBUG	
Size	Document Number
Customer	IGL50/51 LA-3771
Date	Rev
日期: 06年 七月 31, 2006	0.1
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Analog Board ID definition, Please see page 3.



ID	BRD ID	R115 (Rb)	Vab
0	R01 (EVT)	0	0V
1	R02 (DVT)	8.2K	0.25V
2	R03 (PVT)	18K	0.50V
3	R10A (MP)	33K	0.82V
4		56K	1.19V
5		100K	1.65V
6		200K	2.20V
7		NC	3.30V

R119 (Ra) = 100K Ohm

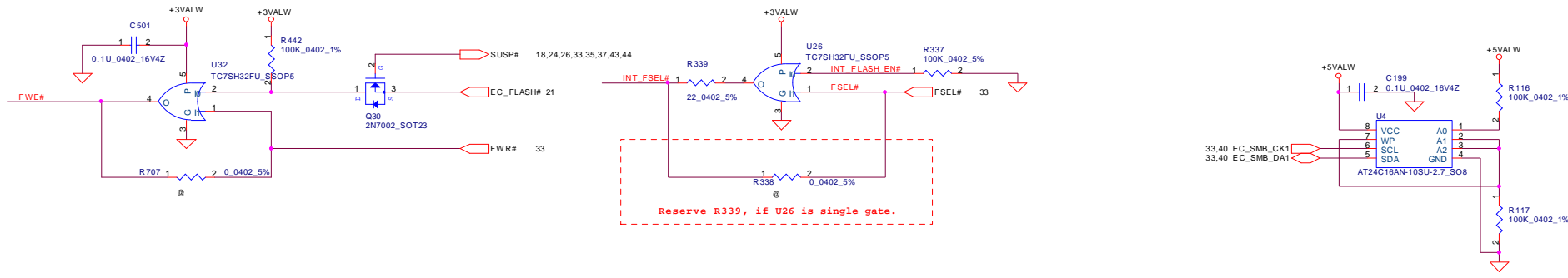
ID	MB	R125 (Ra)	R126 (Rb)
0	IGL50 (VGA)	NC	0 Ohm
1	IGL51 (UMA)	100K Ohm	NC

COMM EC_GPIO Configuration

PIN	GPIO	HDL00/HDL10	HGT30/HGT31	IGL50/IGL51
80	EC_GPIO3F	NC	TP_ACT_LED#	NC
19	EC_GPIO09	EASY_KEY1#	LED6#	SUBWOOFER_MUTE#
35	EC_GPIO17	SUSP_LED#	EC_P80_DATA	EC_P80_DATA
44	EC_GPIO1D	NC	LED3#	TP_ACT_LED#
91	EC_GPIO4A	NC	LED4#	USB_ON#
92	EC_GPIO4B	NC	EAPD IN	EAPD IN
93	EC_GPIO4C	NC	LED1#	TV_TUNER_LED#
94	EC_GPIO4D	NC	LED2#	CAMERA_BTN#
102	EC_GPIO55	NC	LED5#	RCIRRX
97	EC_GPIO50	MEDIA#	BT_OFF#	BT_OFF#
137	EC_GPIO57	VOL_UP#	NOVO_BTN#	NOVO_BTN#
142	EC_GPIO58	VOL_DOWN#	SLP_S4#	SLP_S4#
143	EC_GPIO59	KILL_SW#	WIRE_LAN_BTN#	RF_BTN#
30	EC_GPIO12	AMP_MUTE	TP_LOCK_LED#	SUBWOOFER_BTN#

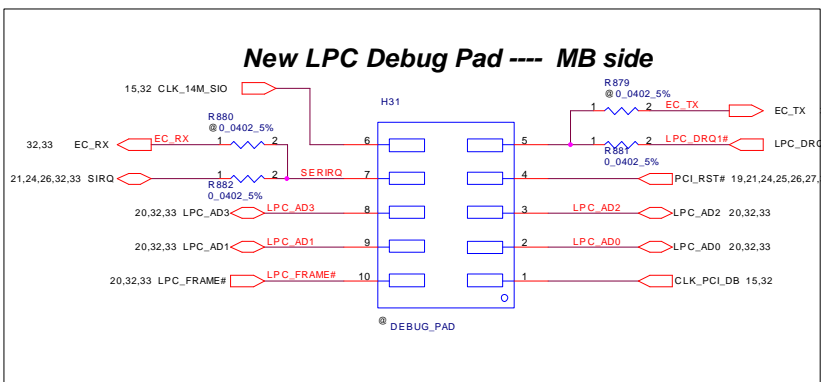
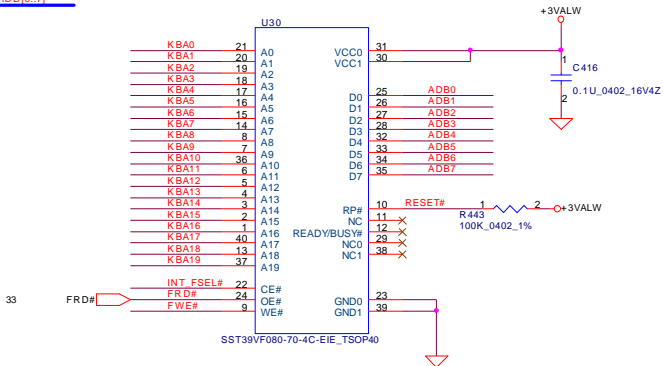
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Issued Date	2005/10/06	Deciphered Date	2006/10/06
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Compal Electronics, Inc.	
Title	ENE-KB910L
Size	Document Number
Customer	IGL50/51 LA-3771
Date	日期: 七月 31, 2006
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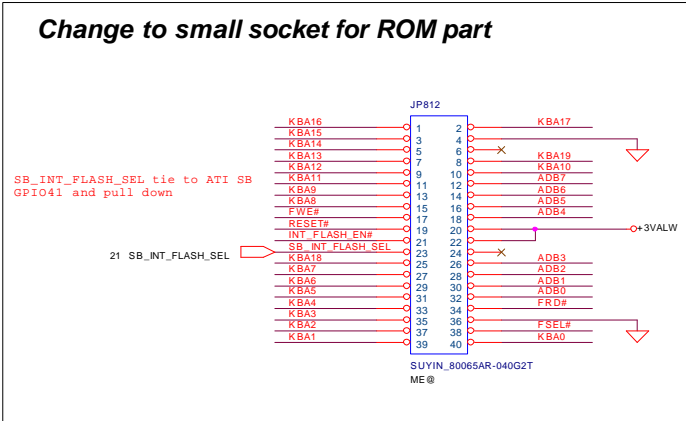


- 33 KBA[0..19]
- 33 ADB[0..7]

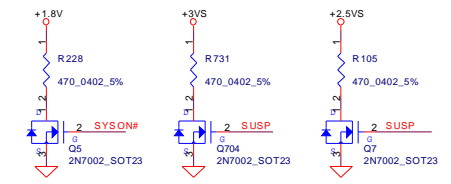
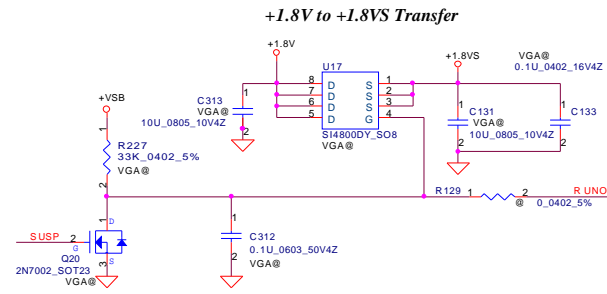
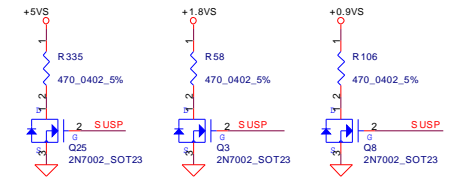
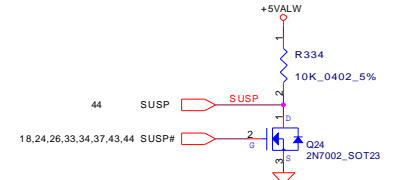
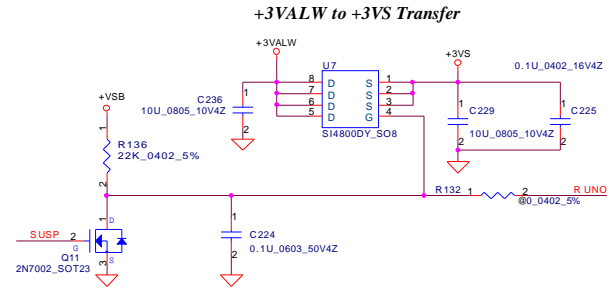
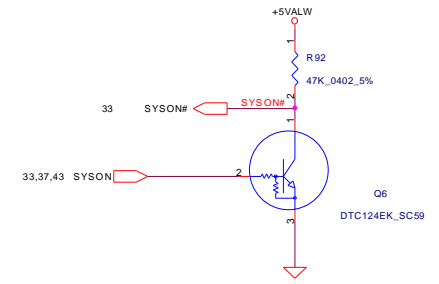
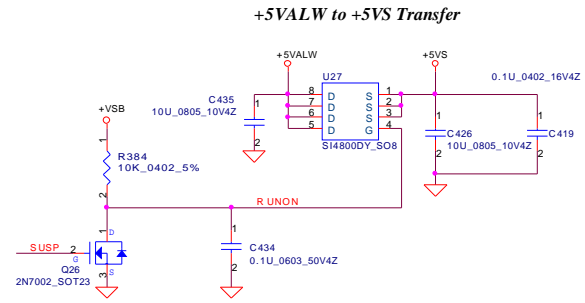
1MB Flash ROM



Under DDR ME Assignment Area
Keep Resistor near Debug Pad and in the same side
Standard side DIMM ---- Pin 1 near DIMM
Reverse side DIMM ---- Pin 1 keep away DIMM



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			Custom	IGL50/S1 LA-3771	0.1
			Date:	星期一, 七月 31, 2006	Sheet 34 of 48

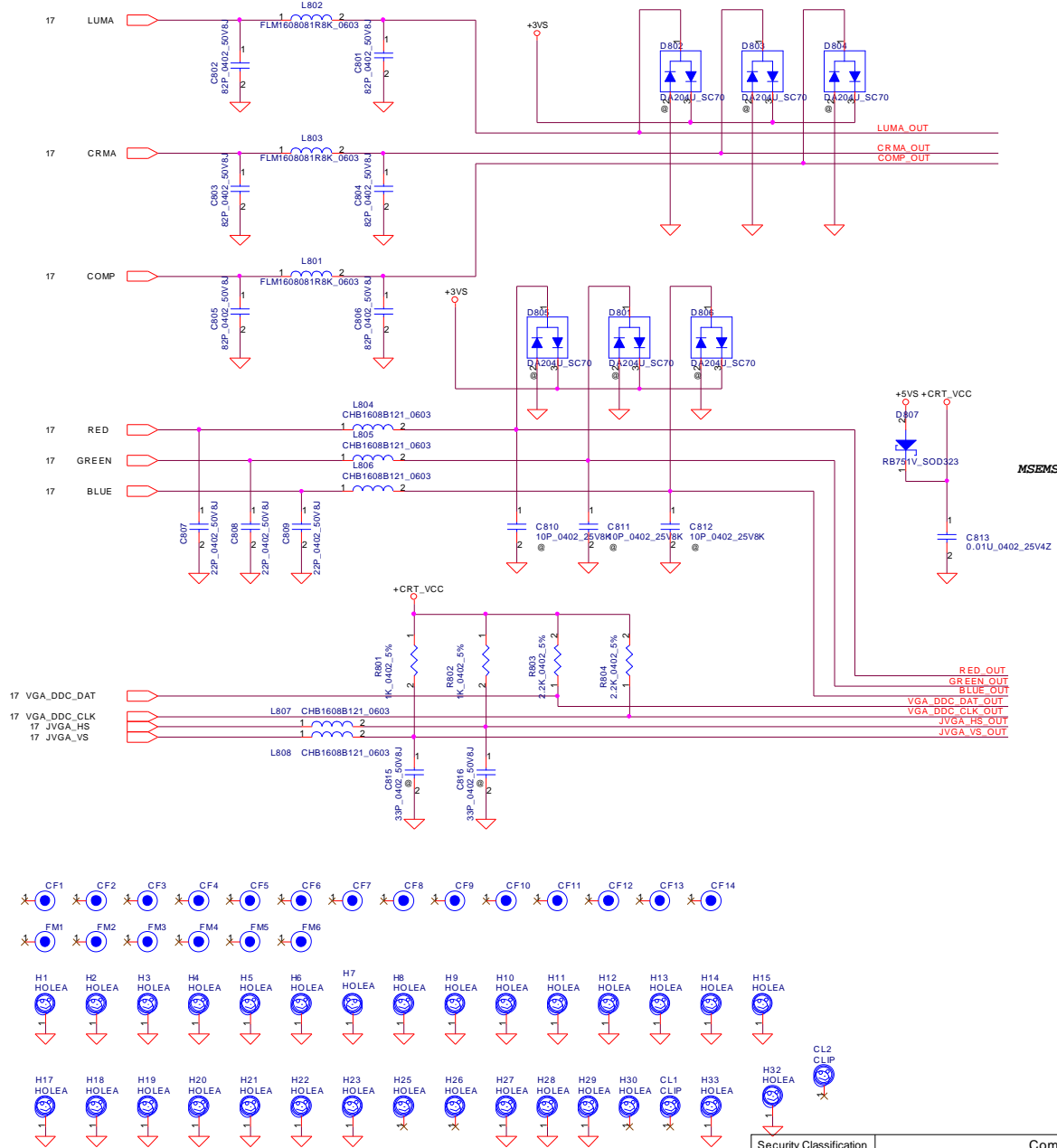


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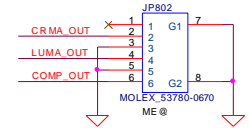
Compal Electronics, Inc.	
DC/DC Circuit	
Size	Document Number
Custody	IGL50/51 LA-3771
Date:	Rev: 0.1
日期: 星期一, 七月 31, 2006	Sheet 35 of 48

VGA I/O PORT Connector

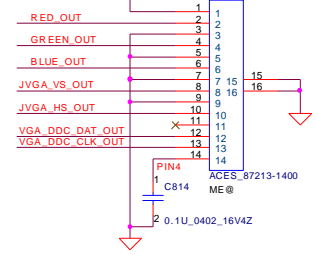
CLOSE TO JTVOUT1



S-VIDEO



DSUB



PIN ASSIGNMENT

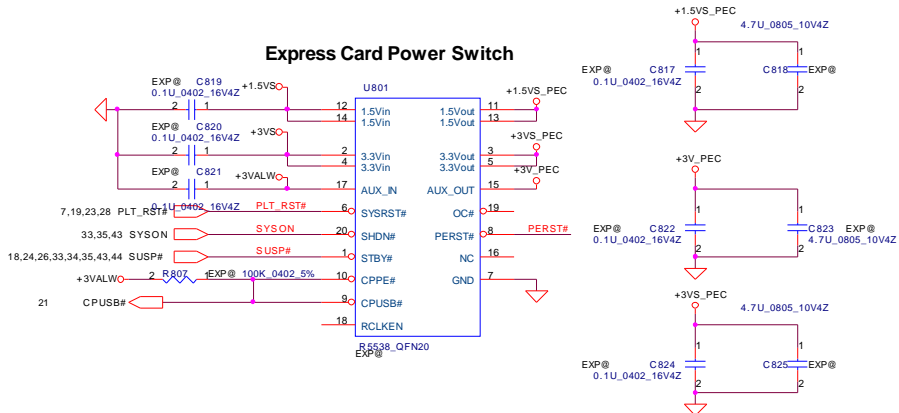
PIN	D-SUB	FUNCTION	PIN	SVIDEO	FUNCTION
1	9	+CRT_VCC	1	1	NC
2	1	RED	2	4	CRMA
3	6	GND	3	2	GND
4	2	GREEN	4	3	LUMA
5	7	GND	5	5	GND
6	3	BLUE	6	6	CVBS
7	8	GND			
8	14	VSYNC			
9	10	GND			
10	13	HSYNC			
11	11	SENSE			
12	12	SM_DAT			
13	15	SM_CLK			
14	4	PIN4			

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 Issued Date: 2005/03/10
 Deciphered Date: 2006/03/10
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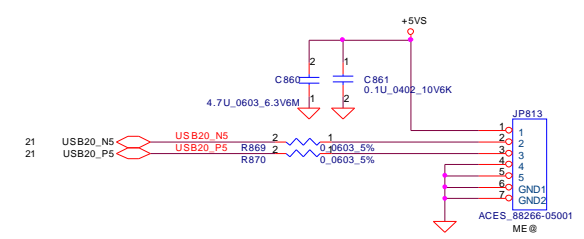
Compal Electronics, Inc.
CRT & TVout Connector
 Size: Document Number
 Customer: IGL50/51 LA-3771
 Date: 2006-07-31
 Sheet: 36 of 48
 Rev: 0.1

NEW CARD FOR C38

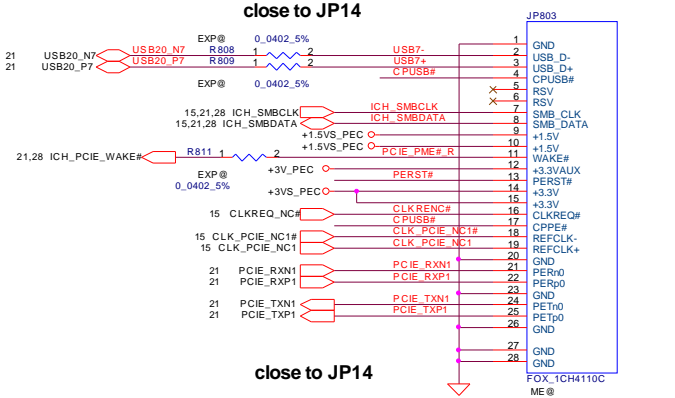
Express Card Power Switch



CMOS Camera Conn

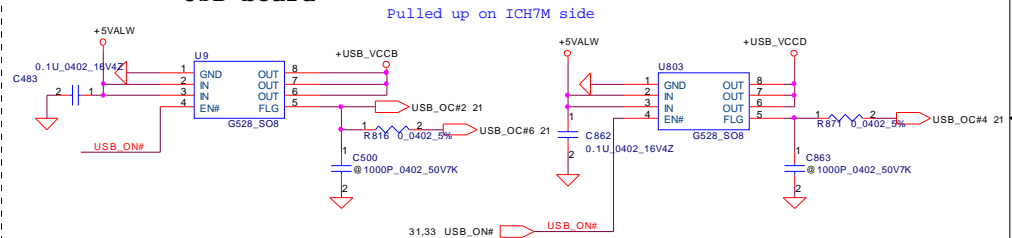


close to JP14



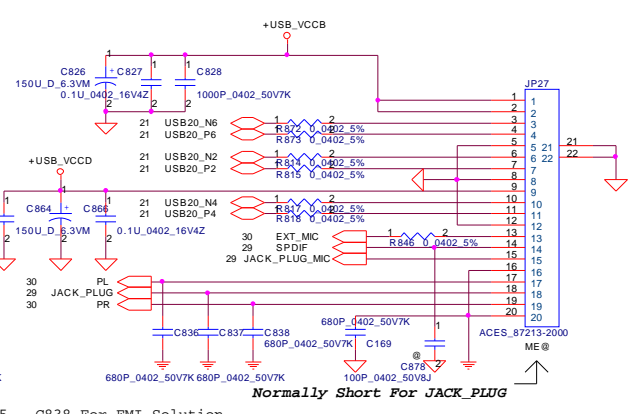
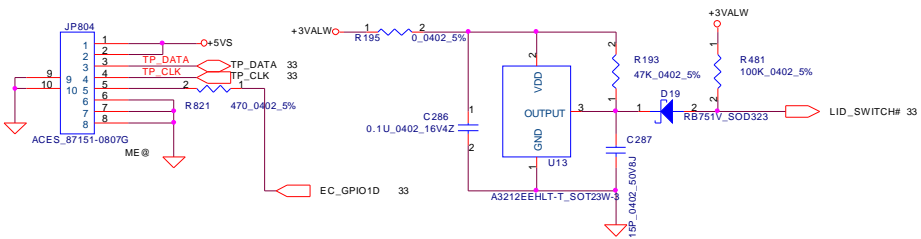
close to JP14

USB board



T/P Board

LID Switch

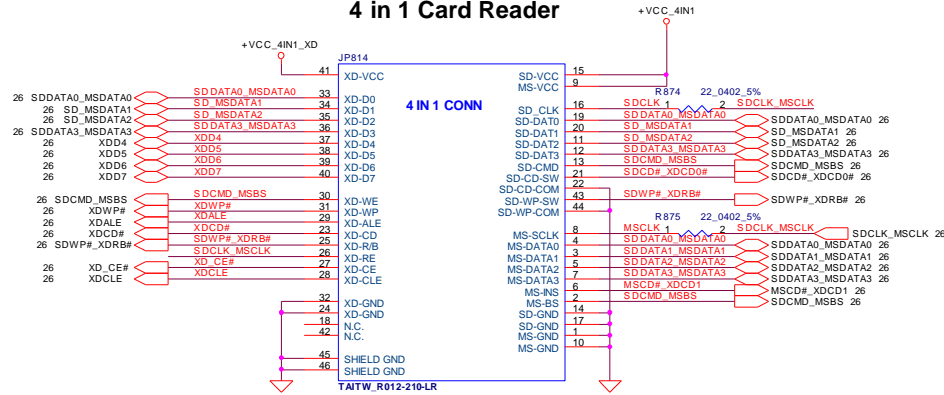


C835 ~ C838 For EMI Solution

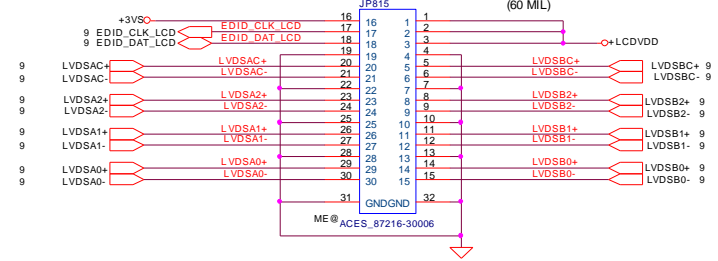
Normally Short For JACK_PLUG

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Size	Document Number			Rev
Custom	IGL50/51 LA-3771			0.1
Date	日期: 二〇〇六年一月〇一	Sheet	37	of 48

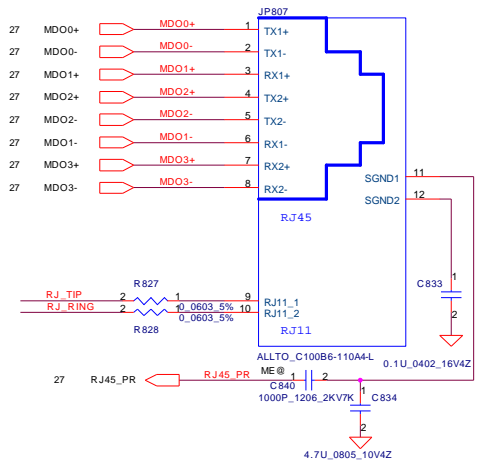
4 in 1 Card Reader



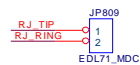
UMA LCD/PANEL Conn.



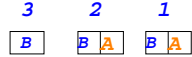
RJ11+RJ45 CONN



MDC CONN



LED Indicator

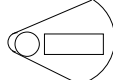


Wireless / Bluetooth LED
 Blue
 Blue
 Amber
 BATT_CHG_LED#
 BATT_LOW_LED#

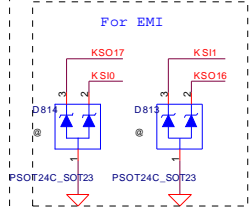
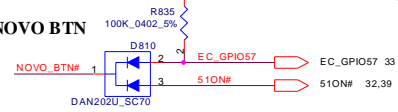
STATUS	
AC	BLUE
Chargin	Blinking Blue
Low BATT	Amber

Function	K016	K017
KEY Matrix		
K010	DW-UP	DW-DOWN
K011	DW-ENTER	MUTE

Dial Wheel

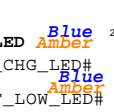


NOVO BTN

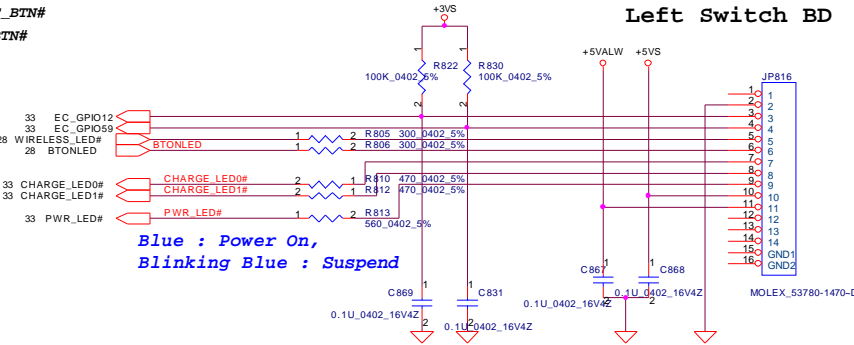


SUBWOOFER_ON/OFF_BTN# RF_ON/OFF_BTN#

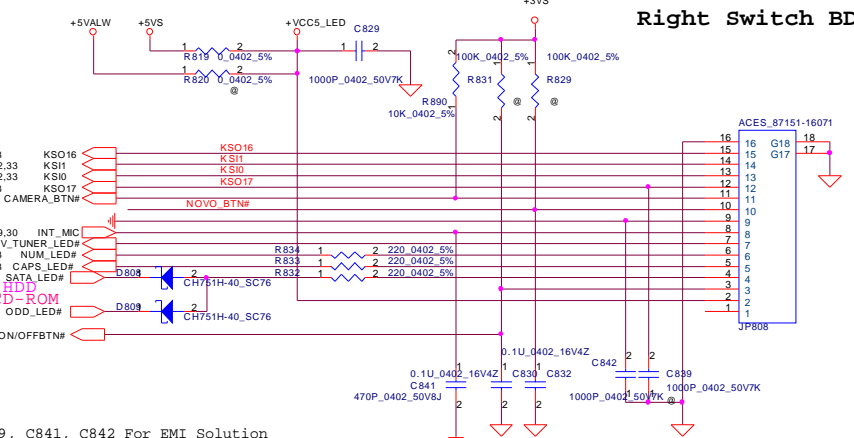
Blue
 Blue
 Amber
 CHARGE_LED0#
 CHARGE_LED1#
 PWR_LED#



Left Switch BD

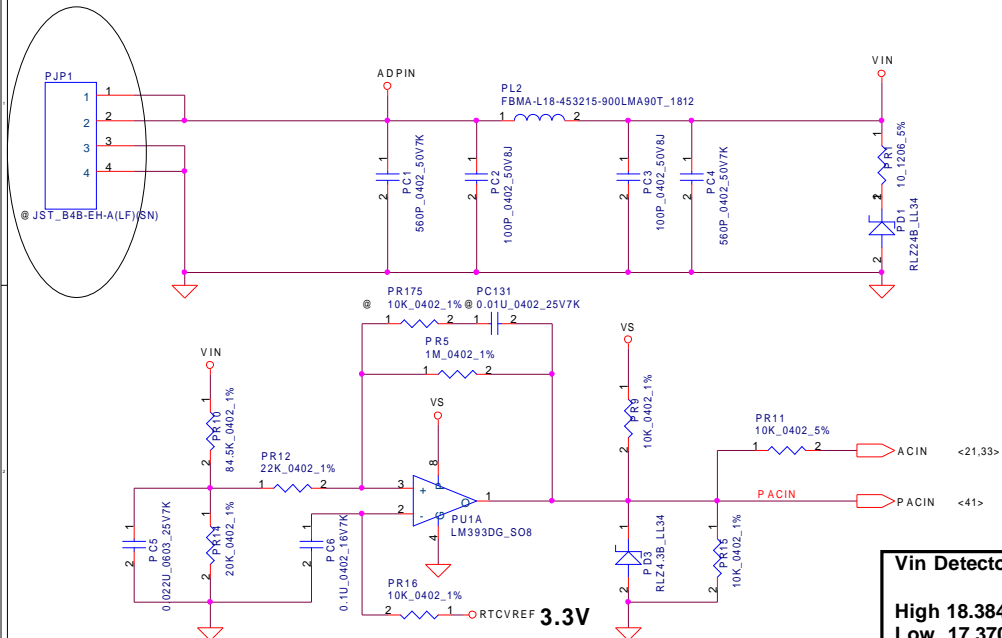


Right Switch BD



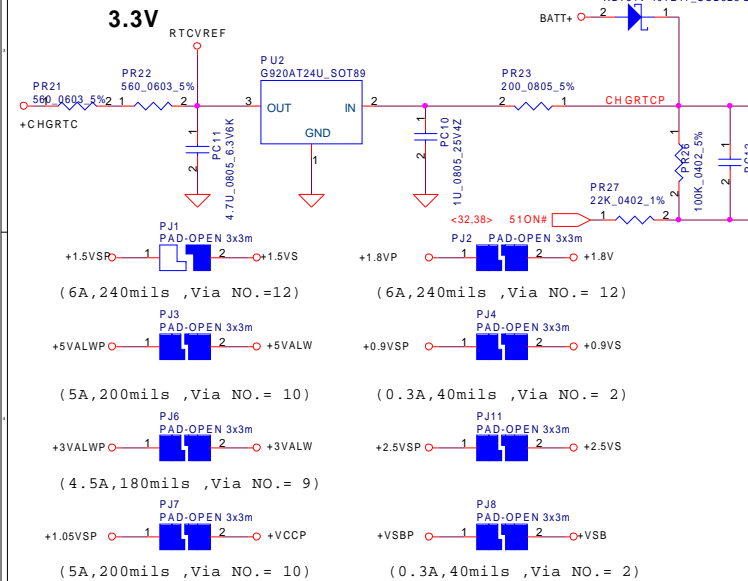
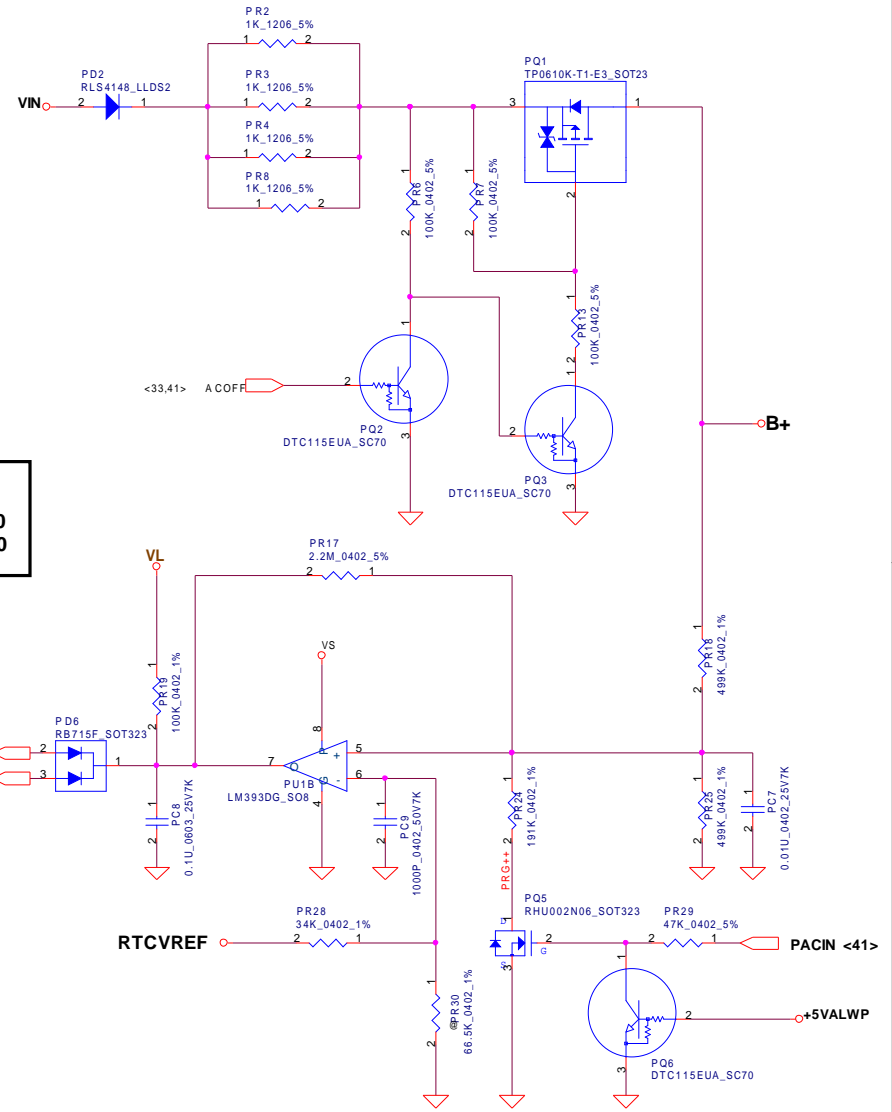
C839, C841, C842 For EMI Solution

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2005/03/10	Deciphered Date	2006/03/10	Title	INDICATE LED
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				Customer	IGL50/51 LA-3771
				Date	Rev 0.1
				Sheet	38 of 48



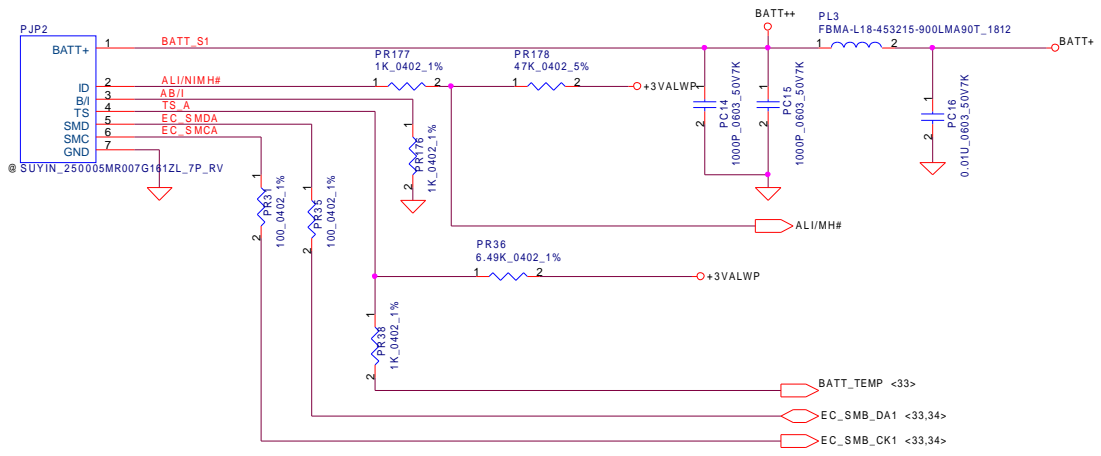
ACIN			
Precharge detector			
	Min.	typ.	Max.
H-->L	14.620V	14.853V	15.245V
L-->H	15.534V	15.970V	16.421V

BATT ONLY			
Precharge detector			
	Min.	typ.	Max.
H-->L	6.169V	6.231V	6.361V
L-->H	7.168V	7.349V	7.537V

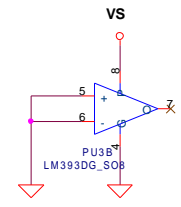
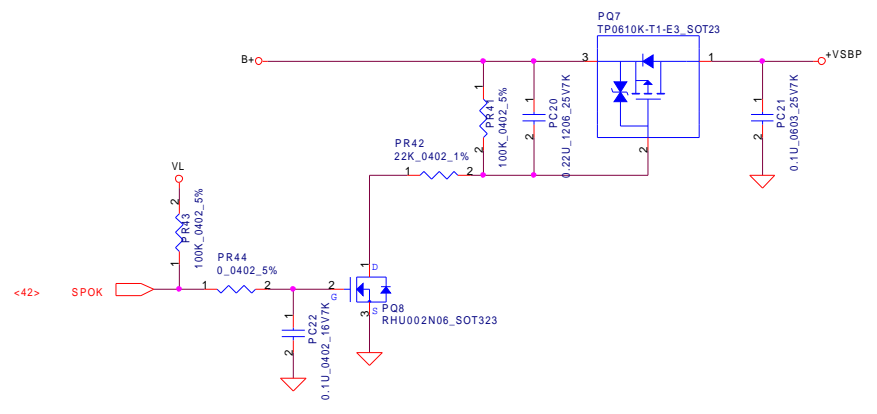
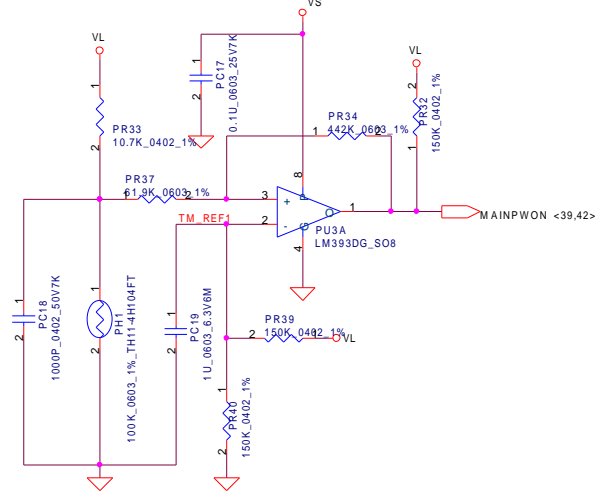


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		2006/08/01
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Title		
DCIN/DECTOR		
Size	Document Number	Rev
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PH1 under CPU bottom side :
 CPU thermal protection at 85 degree C
 Recovery at 70 degree C



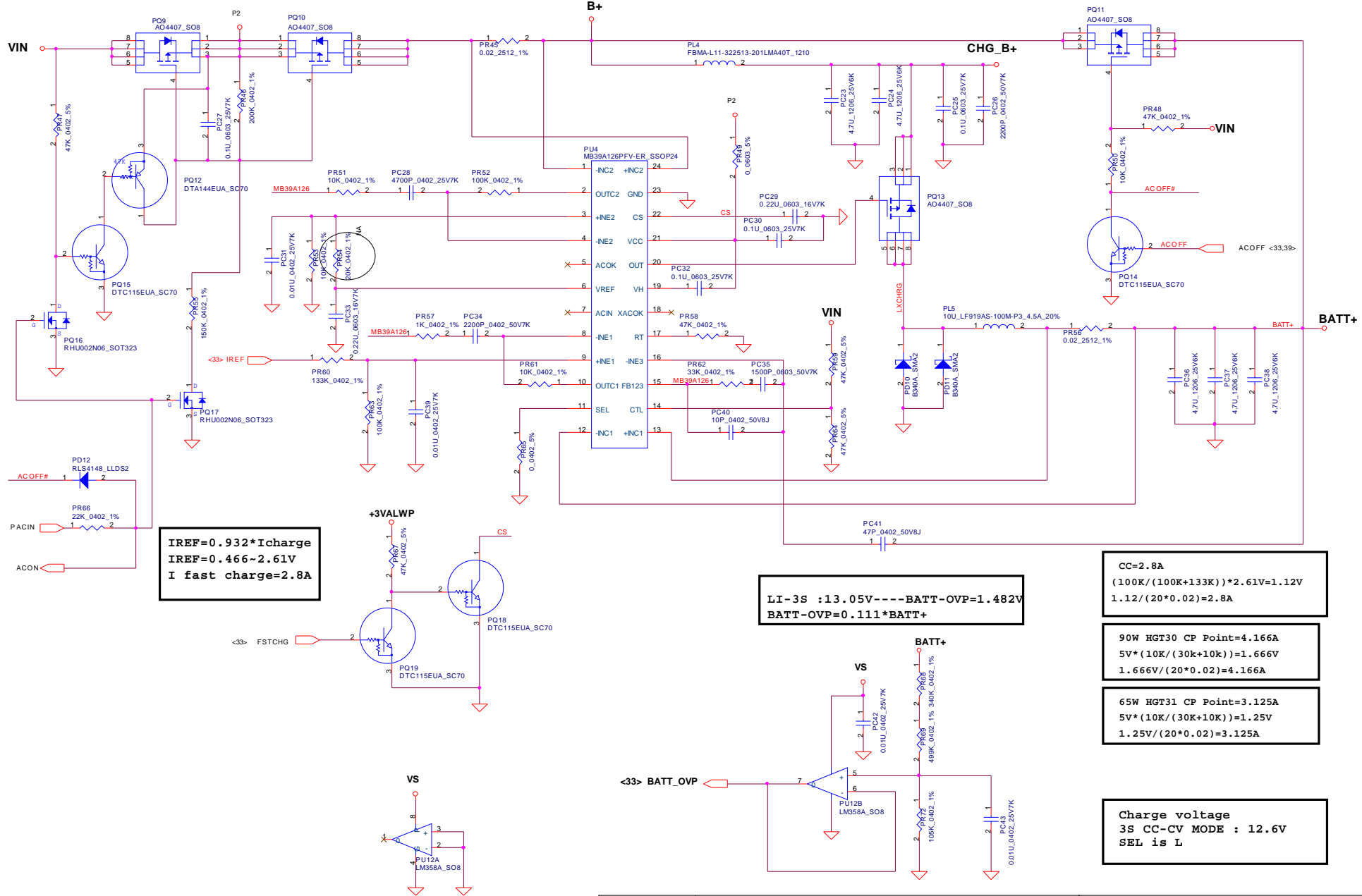
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Issued Date	2005/08/01	Deciphered Date	2006/08/01	Title	
				BATTERY CONN. / OTP	
Size B	Document Number			Rev 0.1	
Date: 星期一, 七月 31, 2006		Sheet 40 of 48			

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65W PR45=0.02_2512_1% PR54=30K_0402_1% Iadp=0~3.125A
 90W PR45=0.02_2512_1% PR54=20K_0402_1% Iadp=0~4.166A

Fosc=14100/Rt=14100/47=300KHz

Charger



IREF=0.932*Icharge
 IREF=0.466~2.61V
 I fast charge=2.8A

LI-3S :13.05V----BATT-OVP=1.482V
 BATT-OVP=0.111*BATT+

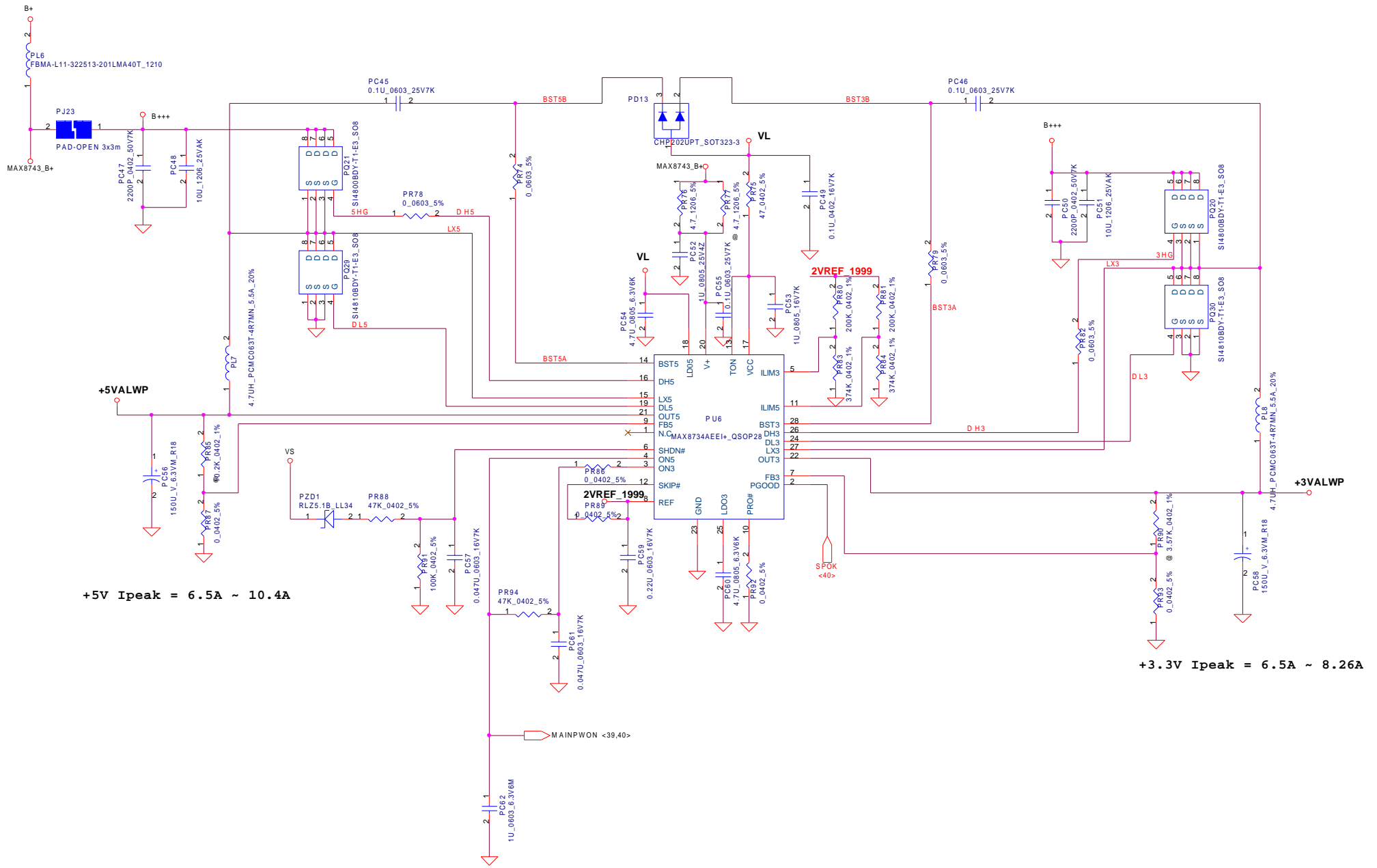
CC=2.8A
 $(100K/(100K+133K))*2.61V=1.12V$
 $1.12/(20*0.02)=2.8A$

90W HGT30 CP Point=4.166A
 $5V*(10K/(30K+10K))=1.666V$
 $1.666V/(20*0.02)=4.166A$

65W HGT31 CP Point=3.125A
 $5V*(10K/(30K+10K))=1.25V$
 $1.25V/(20*0.02)=3.125A$

Charge voltage
 3S CC-CV MODE : 12.6V
 SEL is L

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Size	B	Document Number		Rev	0.1
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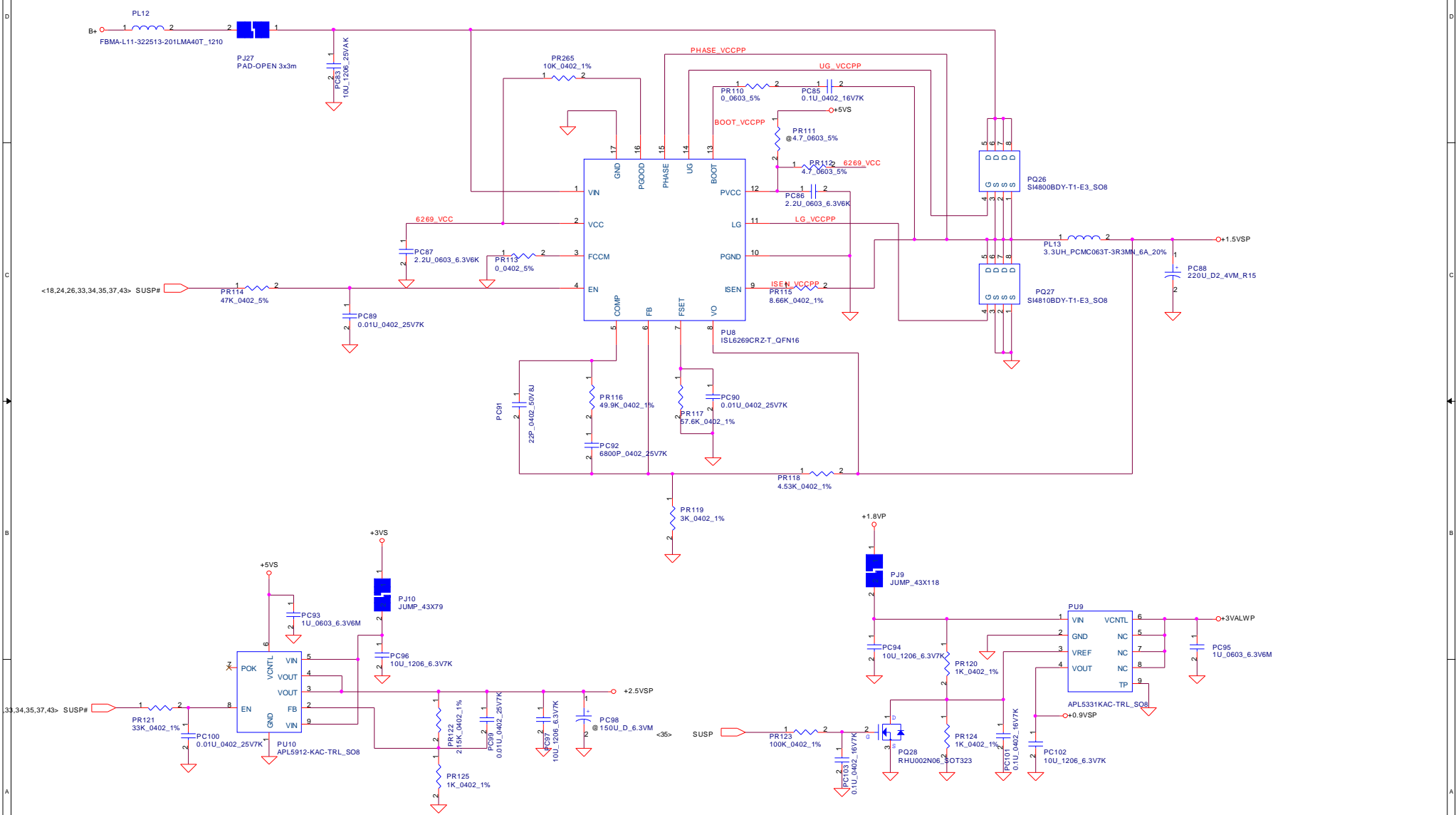


+5V Ipeak = 6.5A ~ 10.4A

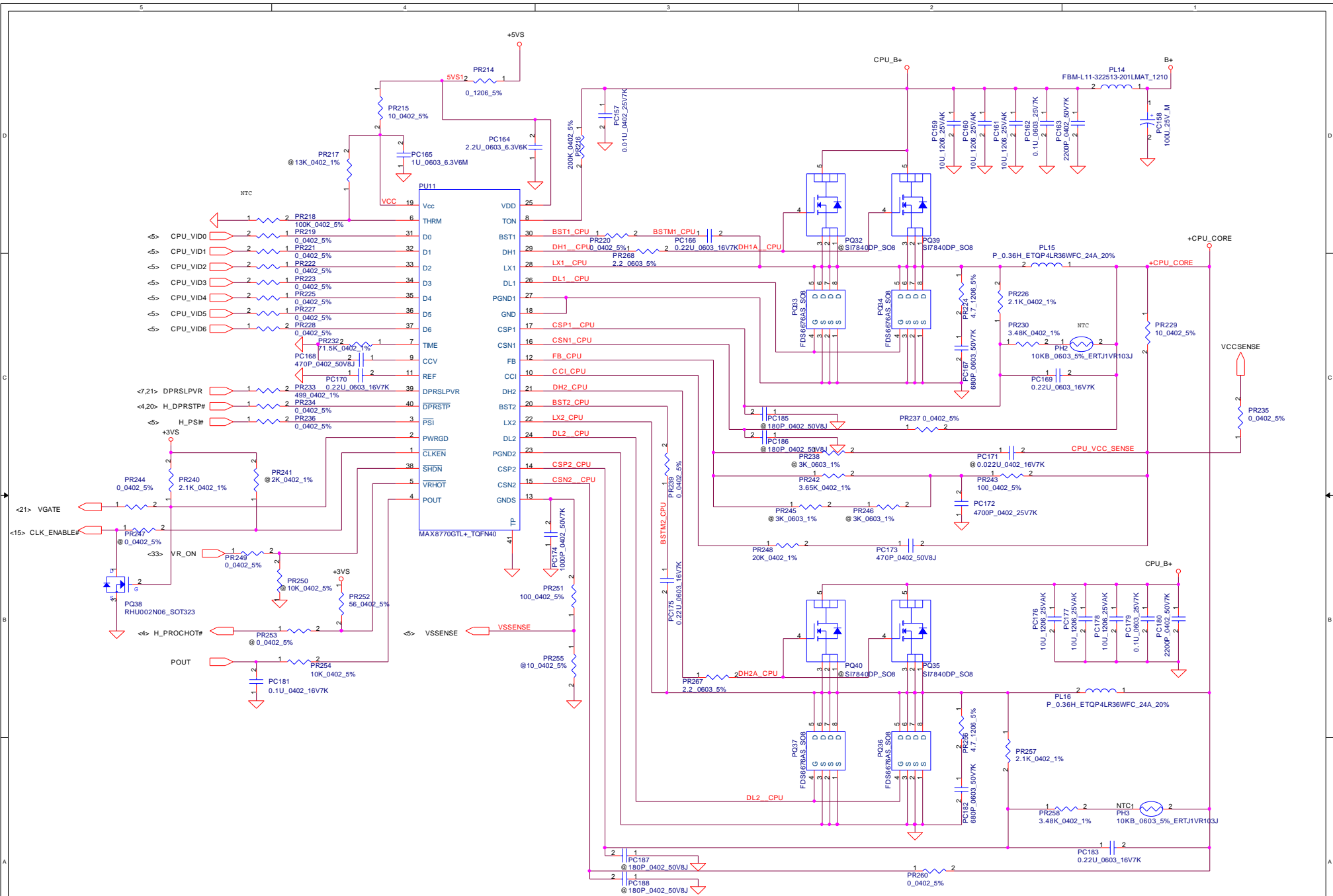
+3.3V Ipeak = 6.5A ~ 8.26A

Security Classification		Compal Secret Data		Title	
Issued Date	2005/08/01	Deciphered Date	2006/08/01	+5VALWP/+3VALWP	
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+1.5VSP Ilimit = 9.38A-12.5A



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				+VCCPP/+2.5VSP/0.9VSP
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				+CPU CORE			

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	VER	Phase
1		MODIFY 3V/5V current limit to 6.5A~8.1A/6.5A to 10.2A		42	MODIFY PR83/PR84 FROM 499K TO 374K		DVT
2		ADD or decrease CPU CORE ring with EMI solution : snubber		45	Reserve PR224//PR256: 4.7 1206 ,add PC167/PC182:680P		DVT
3		Reserve PR267,PR268 seperate in CPU CORE high side gate for EMI require		45	Reserve PR267,PR268:0 0603		DVT
4		change PJP1 from 5 pin to 4 pin		39	change PJP1 from 5 pin to 4 pin		DVT
5		modify sequecce		43	change PR179 to 100k, PC132 =0.1U		DVT
6		modify Vgate		45	add PQ38:RHU002N06,PR240:2K,delete PR247		
7		Prevent noise interference cpu_core feedback		45	Reserve PC185, PC186, PC187, PC188		
8							
9							
10							
11							
8							
9							

Compal Electronics, Inc.			
Title			
PIR (PWR)			
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			0.2
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Version change list (P.I.R. List)

Item	Fixed Issue	Rev.	PG#	Modify List	B.Ver#	Phase
1	PC Beep modify	0.2	29	Modify C714 from 0603 to 0402	0.2	DVT
2	Head Phone no sense	0.2	29	Add R892 for Audio channel B use	0.2	DVT
3	PC BEEP FOR DOS MODE	0.2	29	Change 1u to 680p	0.2	DVT
4	CIR for ALW power	0.2	32	Add R893 for CIR	0.2	DVT
5	To prevent voltage feedback to +3VS from KB_RST#	0.2	33	Add D812	0.2	DVT
6	EAPD change to AC_RST_AUDIO#	0.2	29	Change R458	0.2	DVT
7					0.2	DVT
					0.2	DVT
					0.2	DVT
8					0.2	DVT
9					0.2	DVT
10					0.2	DVT
					0.2	DVT
11					0.2	DVT

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Title PIR		
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Version change list (P.I.R. List)

Item	Fixed Issue	Rev.	PG#	Modify List	B. Ver#	Phase
12					0.3	PVT
13					0.3	PVT
14					0.3	PVT
15					0.3	PVT
16					0.3	PVT

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Compal Electronics, Inc.		
Title		
PIR		
Size	Document Number	Rev
	HGT30/31 LA-3061	0.0
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