Wistron Confidential

MV

2008/05/15 REV :-1

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Karia*

Size	Document Number	Rev
A3	KARIA - DISCRETE	SH

Date: Friday, May 16, 2008 Sheet 1 of 58

KARIA DESCRETE BLOCK DIAGRAM

Project code : 91.4V901.001
PCB P/N :
Revision : MV

SYSTEM DC/DC SC471AML	
INPUTS	OUTPUTS
B+	VGA_CORE 45

SYSTEM DC/DC TPS5116	
INPUTS	OUTPUTS
B+	+1.8V 7A 47 +0.9V 1A

SYSTEM DC/DC TPS51120	
INPUTS	OUTPUTS
B+	+5VALW 7A +3VALW 6A 46

SYSTEM DC/DC SC412A	
INPUTS	OUTPUTS
B+	+1.5VS 3A +1.05VM 13A 48

CHARGER BQ27470	
INPUTS	OUTPUTS
	BATT
BATT_A BATT_B	18V 3.0A 5V 100mA 51

CPU DC/DC ISL6260A	
INPUTS	OUTPUTS
B+	+VCC_CORE 0.844~1.3V 44A 43

PCB LAYER	
L1:	Signal 1
L2:	GND
L3:	Signal 2
L4:	Signal 3
L5:	GND
L6:	VCC
L7:	Signal 4
L8:	Signal 5
L9:	GND
L10:	Signal 6

CLK GEN
SLG8SP553
16

Intel CPU
Penryn
5,6,7

HOST BUS
FSB
667/800/1067MHz

GDDR 3
VRAM 0 58
VRAM 1 58

DDRII 800 Slot 0 14
DDRII 800 Slot 1 15
DDRII 667/800 Channel A
DDR II 667/800 Channel B

Cantiga PM
AGTL+ CPU I/F
DDR Memory I/F
INTEGRATED GRAHPICS
LVDS, CRT I/F
8,9,10,11,12,13

PCIE x 16

ATI
M82-SCE
52,53,54,55,56,57

RGB CRT
LVDS
CRT 17
LCD 18

DMI x4
Controller link 0

Smart Card ISO7816 37
1394 37
SD/MMC 37
Ricoh 5C835
CardReader
36,37
PCI

INTEL
ICH9-M
12 USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
Serial Peripheral I/F
ACPI 1.1
LPC I/F
4 SATA
PCI/PCI BRIDGE
19,20,21,22,23

SMBus
Thermal Sensor EMC2103 39
Accelerometer LIS302DLTR 24

Fingerprinter AES2810B 38
CAMERA 38
Blue Tooth
USB x 3 28

GLCI
Intel Ninevah-MM (BOAZ)
10/100/1000 25
RJ45 CONN 26

MODEM MDC V1.5 31
RJ11 CONN 31
HD Audio

USB 2.0
SATA
HDD Cnn SATA 24
SATA
ODD Cnn 24

LPC Bus
SPI

AUDIO CODEC
ADI 1984A
INTERNAL MIC
MIC IN
Headphone
PRE-AMP
TLV2462

PCIE+USB 2.0
C-LINK
PCIE x 2
TI2231
Express Card 54
Mini-Card*2
802.11abg/n
WWAN 27

KBC
SMSC KBC1091
30
TPM
SLB9635TT 29
SMSC Super I/O
LPC47N217 40

SPI
Flash ROM
32Mb x 1(AMT) 29
Tauch Pad 31
Int. KB 31
Capacitive Button 38

OP AMP
TI 6041A
SPEAKER

DOCK
PCIE*2 PS2 SATA*1 USB*2 Serial Port Parallel Port LINE IN/Out RJ45/RJ11 VGA DVI-D

<Variant Name>
Wistron Corporation
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Title: Diagram
Size: C
Document Number:
Rev: SH
Date: 2009.12.04 20:27:18
Sheet 2 of 58

Discrete PV
03/11/08:
- Page 51 - Change R118 to 287K ohm from Vox information.
- Page 43 - Change R582.2 to +3VALW from +3VS to power U89.39 (3V3)
- Page 45 - Change R232 to NO INSTALL
- Page 30 - Remove D48, connect signal directly to ADP_PRES, and uninstall R558
- Page 27 - Reserve a 1u 0603 cap (NO INSTALL) on MC2_DISALBE (same as MC1_DISABLE)
- Page 19 - Add a 0 ohm series on PLT_RST# at U113.4
- Page 33 - Add a 0 ohm series on PM_PWROK_R at R175.2
- Page 13 - Uninstall BGA_CRACK circuit: U115, U116, R740, R744, R801, & R802
- Page 23 - Uninstall BGA_CRACK circuit: U117, U118, R803, R804, R805, & R806
- Page 39 - Change R710 (SHDN_SEL) to 15K 1% to use Internal Diode for H/W critical shutdown
- Page 57 - Add a discharging FET (gate connect to Q15.D) on 3.3V_DELAY at Q42.D
- Page 25 - May require a discharging FET for +3VM_LAN at Q39.D
- Page 32 - May need to change RGB q-switches power to +5VALW or +5VS (depending on wavy impact)
- Page 51 - Change R97 to 33K from 1.27K
- Page 41 - Change DAUGTH1 pin 52 and pin 54 to +5VS from +5VALW
- Page 41 - Remove ICH_SMB_CLK/DATA from DAUGTH1 pin 32 and 34

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Title: *Change Notes List*

Size	Document Number	Rev
A3	KARIA - DISCRETE	SH

Date: Friday, May 16, 2008 Sheet 3 of 58

Voltage Rails

○ MEANS ON x MEANS OFF

State \ power plane	+BB LDO3 LDO5	+3VALW +5VALW	+1.8V +5V +0.9V	+5VS +3VS +1.8VS +1.5VS +VGA_CORE +CPU_CORE +VCCP	+3VM +1.05VM	CLOCK
S0	○	○	○	○	○	○
S3/M1	○	○	○	x	○	○
S3	○	○	○	x	○	○
S5 S4/AC	○	○	x	x	○	○
S5 S4/Battery only	○	x	x	x	x	x
S5 S4/AC & Battery don't exist	x	x	x	x	x	x

PCI Devices

EXTERNAL	IDSEL#	REQ/GNT#	PIRQ
Cardreader&1394	AD25	2	G,E

PCIE Devices

DEVICE	NUMBER	CHANNEL
UWB(no support)	1	1
WLAN	1	2
EXPRESS CARD	1	3
WWLAN	1	4
DOCKING	1	5
GIGA LAN	1	6

USB PORT	Device
0	USB1
1	Free
2	EX-P
3	WLAN
4	USB2
5	USB3
6	BLUETOOTH
7	WWAN
8	FignerPrint
9	Dock1
10	WEBCAM
11	DOCK2

Symbols	Description
DY/DUMMY	No install
1KR2J	Resistor 1K ohm ,Size 0402 ,5%
1KR3F	Resistor 1K ohm ,Size 0603 ,1%
GP	ROHS parts
NC	Pin no connect to anything
1U16V2ZY-2GP	Caps 1U ,Size 0402 Y5V
2D2U6D3V3MX	Caps 2.2U ,Size 0603 X5R

IRQ	Device
0	System Timer
1	Keyboard
2	N/A
3	Serial port (COM2) ,LAN/Modem
4	Serial port (COM1)
5	Audio/VGA
6	~~Floppy~~
7	Parallel port
8	System CMOS/Real-time clock
9	Microsoft ACPI
10	N/A,Modem,LAN
11	Mass storage control/PCI simple communication control
12	synactic PS2 port GlidePAD
13	Numeric Data Process
14	Primary IDE interface ,HDD
15	Secondary IDE interface ,CD-ROM
16	Mobile Intel Crestline Express Chipset Family Microsoft UAA Bus Drive for High Definition Audio Intel 82801H (ICH9 Family) PCI Express Root Port -27D0 Broadcom NetXtreme Gigabit Ethernet
17	Intel 82801H (ICH9 Family) PCI Express Root Port -27D2 Broadcom 802.11b/g WLAN Intel 82801H (ICH9 Family) USB Universal Host Control
18	Intel 82801H (ICH9 Family) USB Universal Host Control Richo R5C835 Integrates FlashMedia Control Richo R5C835 Gemcore based SmartCard Control
19	Intel 82801H (ICH9 Family) PCI Express Root Port -27D6 Intel 82801H (ICH9 Family) USB Universal Host Control
20	Intel 82801H (ICH9 Family) USB Universal Host Control Intel 82801H (ICH9 Family) USB2 Enhanced Host Control
21	Intel 82801H (ICH9 Family) USB Universal Host Control
22	SDA Standard Compliant SD Host Control
23	HP Mobile Data Protection Sensor

<Variant Name>

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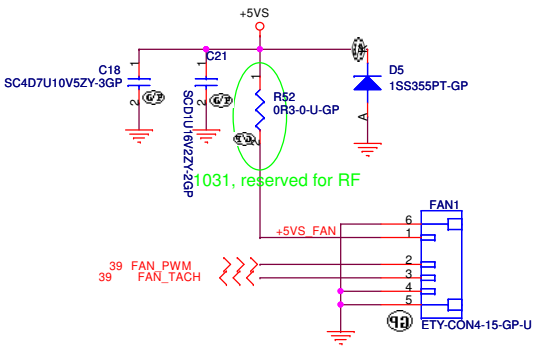
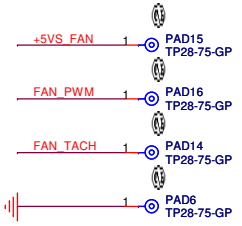
Title: Karia List

Size: A3 | Document Number: KARIA - DISCRETE | Rev: SH

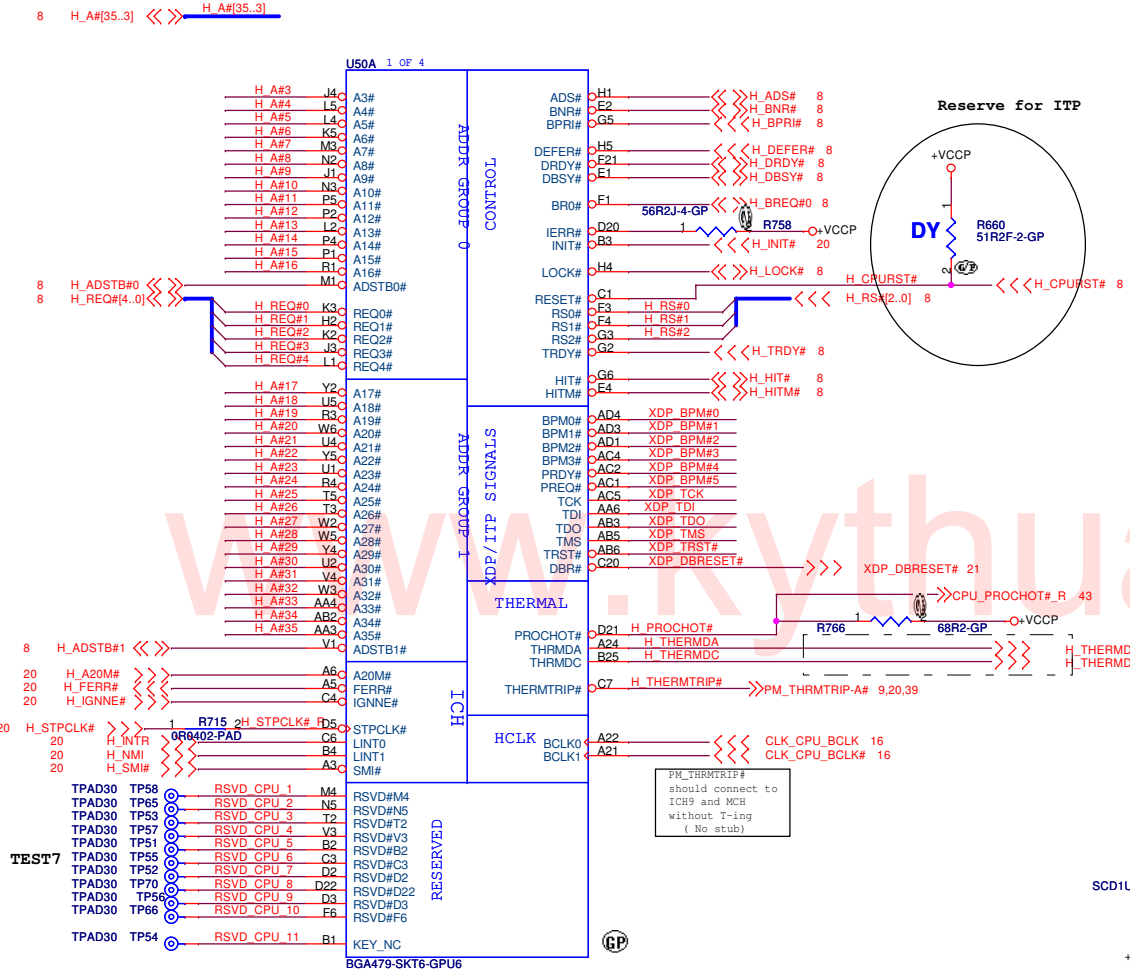
Date: Friday, May 16, 2008 | Sheet 4 of 58

4 WIRE PWM Fan Control circuit



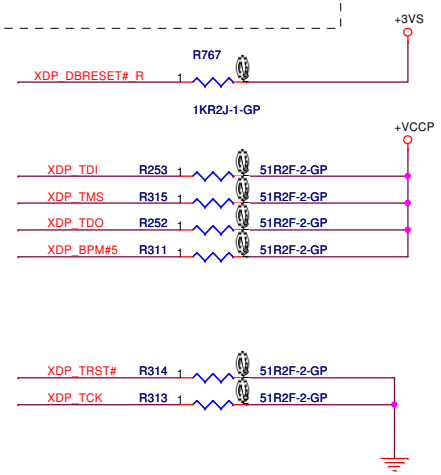


1 TDI
2 TMS
3 TRST#
4 NC
5 TCK
6 NC
7 TDO
8 BCLK#
9 BCLK
10 GND
11 FBO
12 RESET#
13 BPM5#
14 GND
15 BPM4#
16 GND
17 BPM3#
18 GND
19 BPM2#
20 GND
21 BPM1#
22 GND
23 BPM0#
24 DBA#
25 DBR#
26 VCC
27 VCC
28 VCC

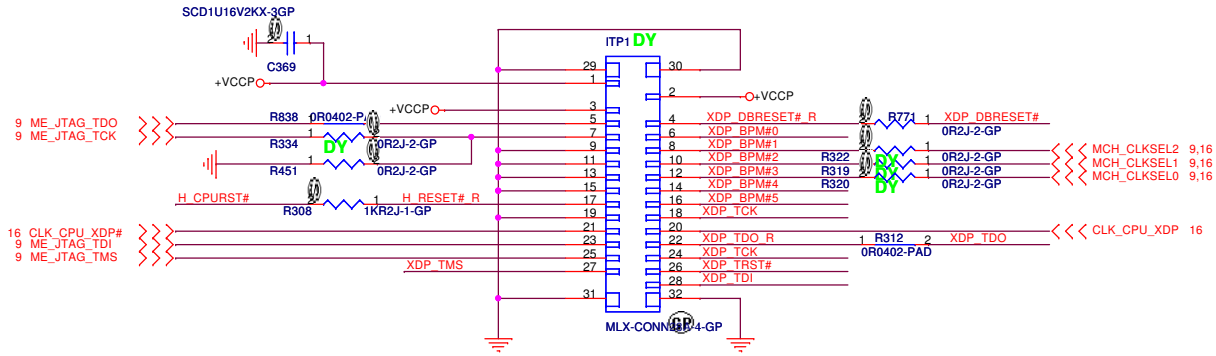


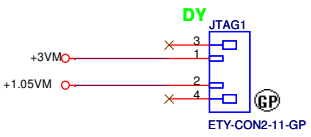
H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil

layout note : R7,R10 Pull near cpu



ITP Connector





<Variant Name>

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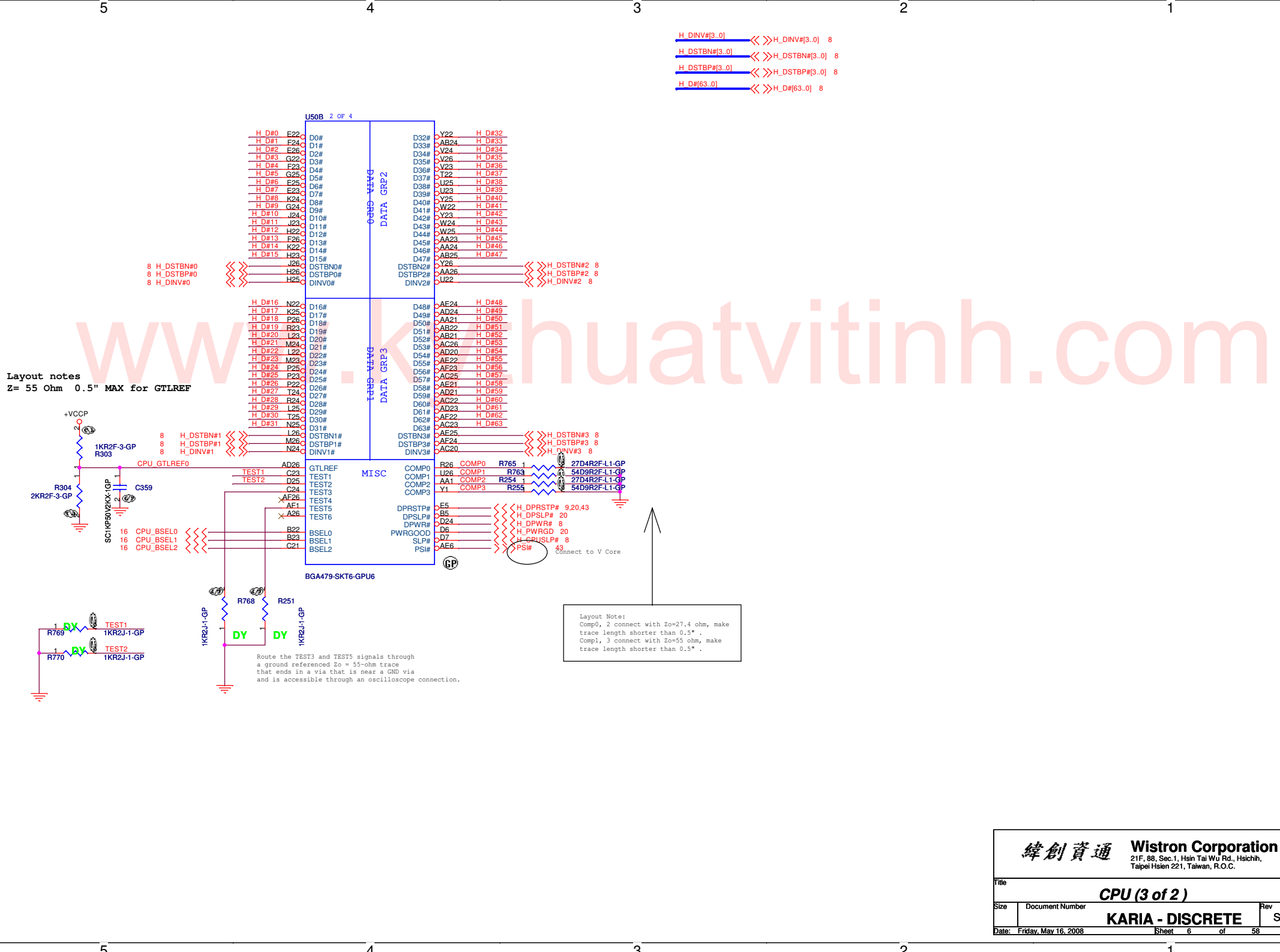
Title	CPU (1 of 2)	
Size	Document Number: KARIA - DISCRETE	Rev: SH
Date: Tuesday, May 20, 2008	Sheet 5 of 58	



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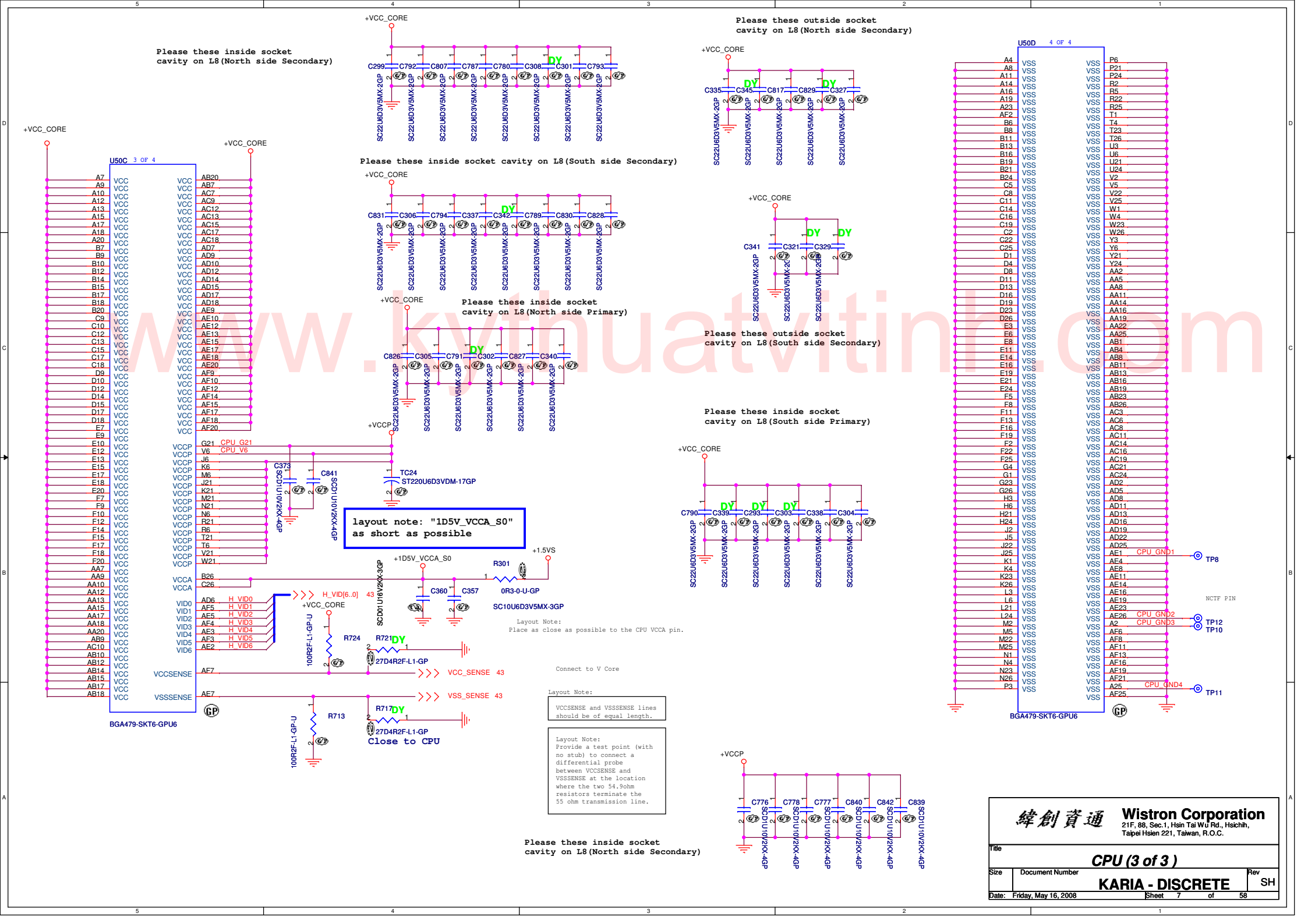
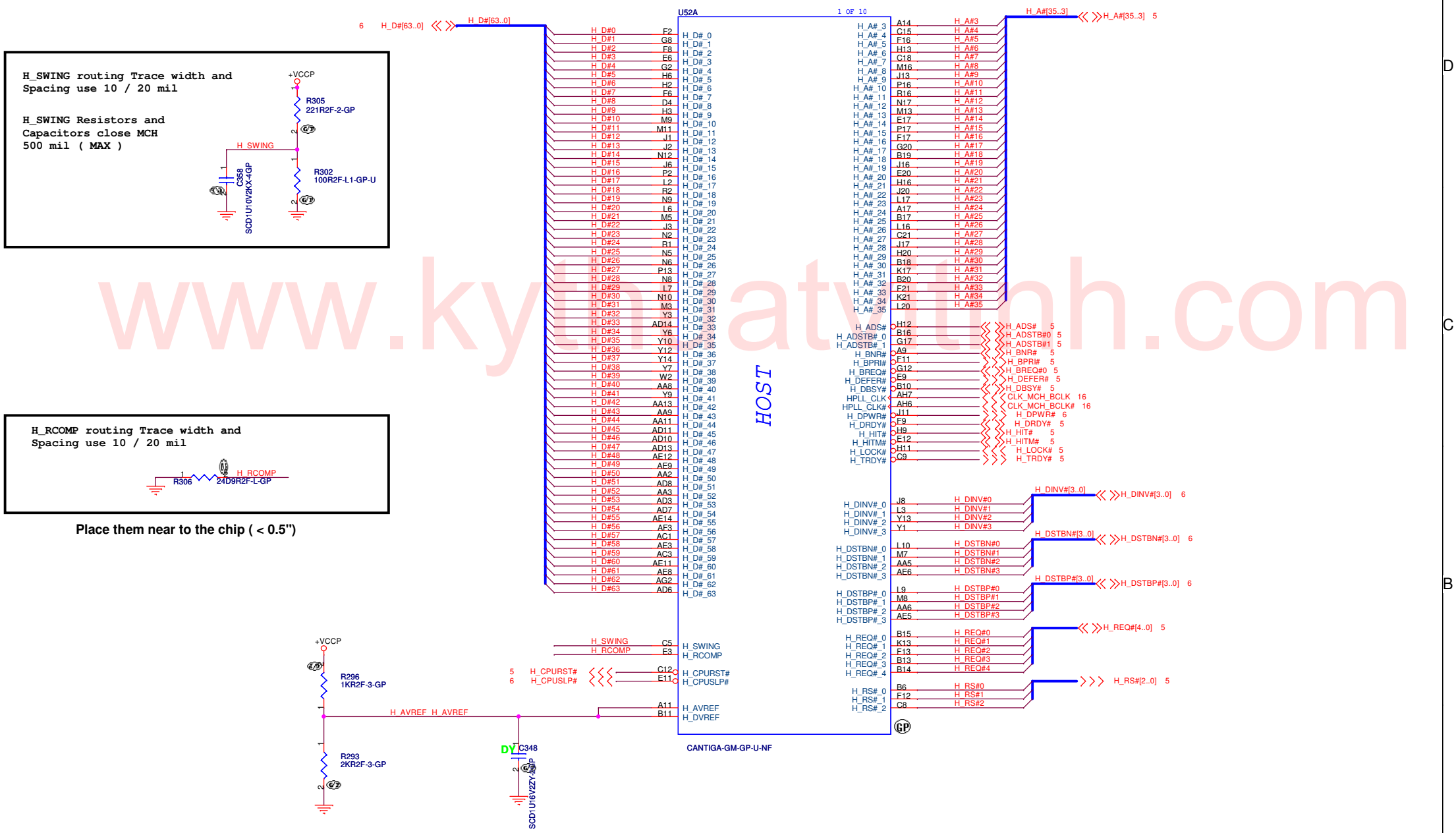
Title: **CPU (3 of 2)**

Size | Document Number: **KARIA - DISCRETE** | Rev: SH

Date: Friday, May 16, 2008 | Sheet 6 of 58





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Title: Cantiga (1 of 6)

Size | Document Number: KARIA - DISCRETE | Rev: SH

Date: Friday, May 16, 2008 | Sheet 8 of 58

Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1067MHz　011 = FSB 667MHz 010 = FSB 800MHz　Others = Reserved
CFG4:3; 8; 11; 14:15; 17; 18	Reserved
CFG5 (DMI select)	Low = DMI x 2 High = DMI x 4 *
CFG6 (ITPM Host Interface)	High = The ITPM Host Interface is disabled * Low = The ITPM Host Interface is enabled
CFG7 (Intel Management Engine Crypto Strap)	Low = Intel Management Engine Crypto Transport Layer Security (TLS) cipher site with no confidentiality High = Intel Management Engine Crypto TLS Cipher suite with confidentiality *
CFG9 (PCIE Graphics Lane)	Low = Reverse Lanes, 15->0, 14->1 etc... High = Normal operation:Lane Numbered in Order *
CFG10 (PCIE Loopback enable)	Low = Enabled High = Disabled *
CFG12 (ALLZ)	Low = ALLZ mode Enabled High = Disabled *
CFG13 (XOR)	Low = XOR mode Enabled High = Disabled *
CFG16 (FSB Dynamic ODT)	Low = Dynamic ODT Disabled High = Dynamic ODT Enabled *
CFG19 (DMI Lane Reversal)	Low = Noraml operation: Lane Numbered in Order * High = Reverse Lanes DMI x 4 mode[MCH->ICH]: (0->3, 2->1, 1->2 and 0->3) DMI x 2 mode[MCH->ICH]: (3->0, 2->1)
CFG20 (Digital Display Port (SDVO/DP /iHDMI) Concurrent with PCIE)	Low = Only Digital Display Port (SDVO/iHDMI) or PCIE is operational * High = Digital Display Port (SDVO/DP/iHDMI) and PCIE are operating simulatneously via the PEG port
SDVO_CTRLDATA (SDVO Present)	Low = No SDVO Card Present * High = SDVO Card Present
L_DDC_DATA (Local Flat Panel (LFP) Present)	Low = LFP Disabled * High = LFP Card Present; PCIE disabled
DDPC_CTRLDATA (Digital Display Present)	Low = DisplayPort Disabled * High = DisplayPort Device Present

FSB setting

CFG 5, 7, 9, 10, 12, 13, 16, 19, 20
Teenah = 4.02K
Cantiga = 2.2K

Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time

Place the 49D9 Ohm resistor within 500 mils (1.27 mm) of the (G)MCH.
49.9 OHM PN:64.49R95.6DL

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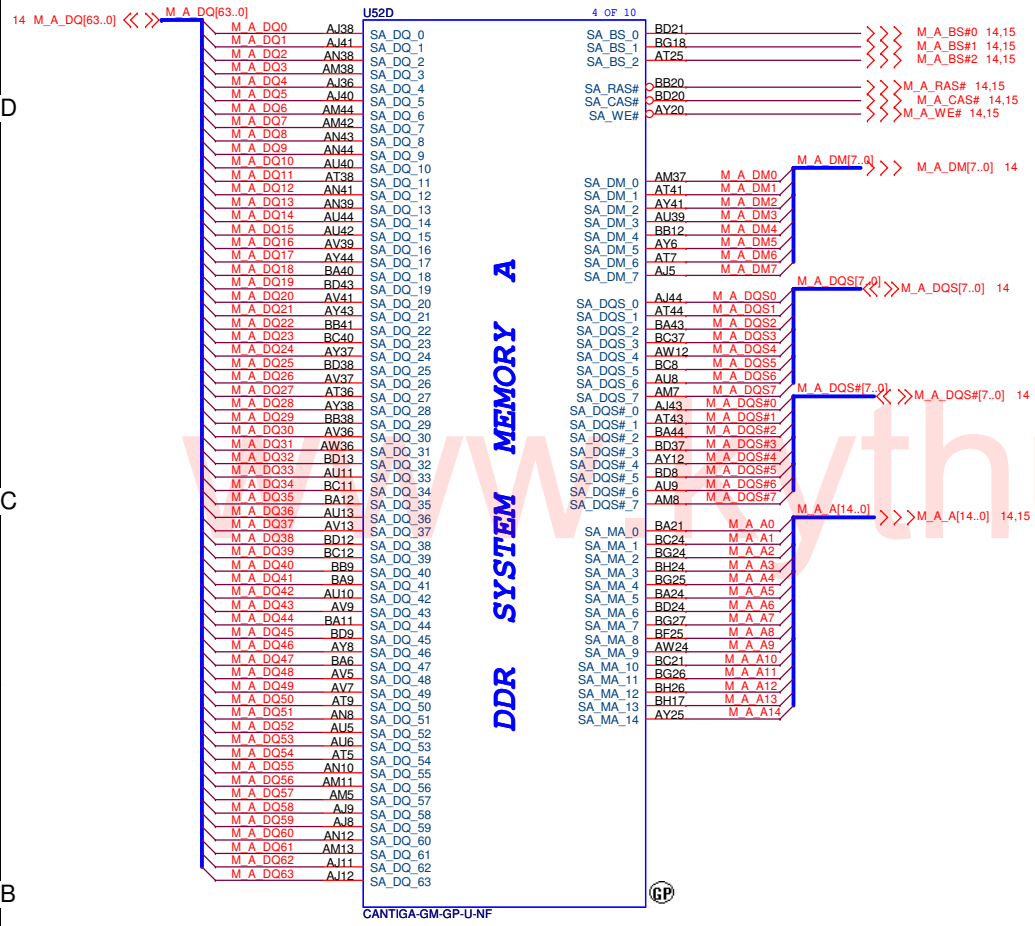
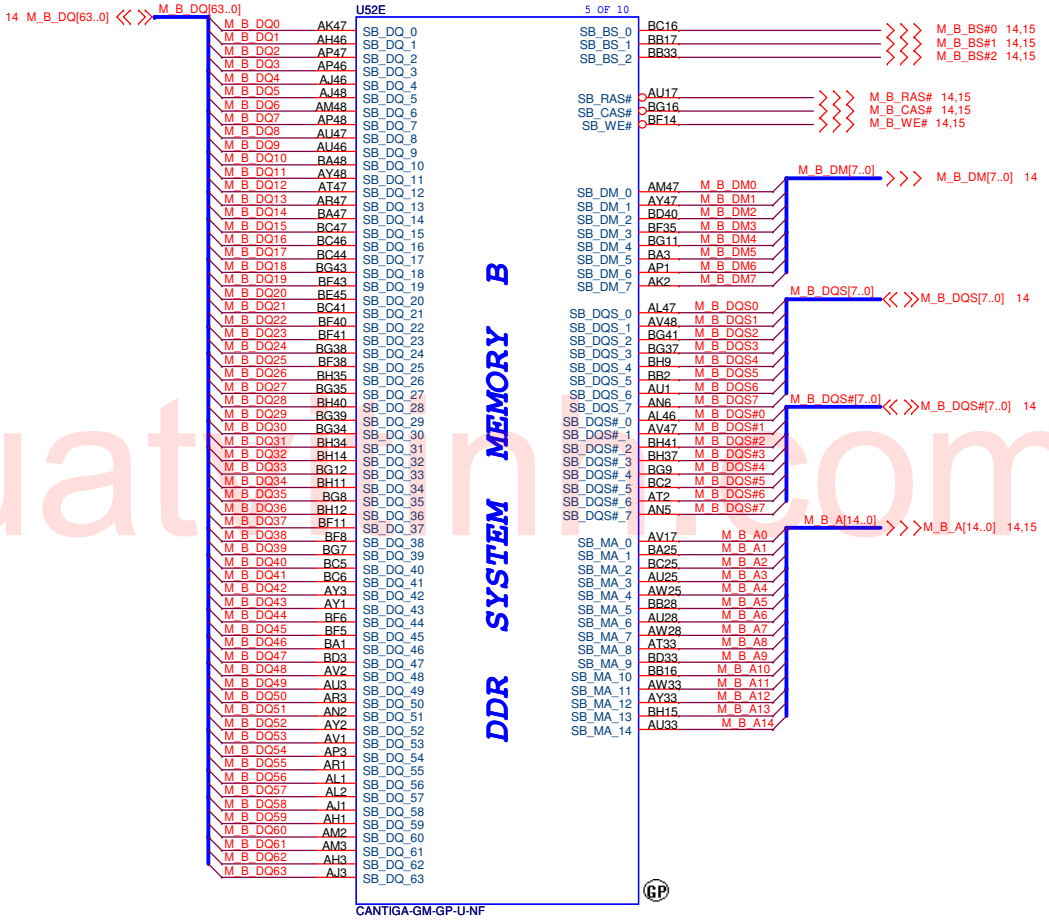
Title: Cantiga (2 of 6)	
Size:	Document Number: KARIA - DISCRETE　Rev: SH
Date: Monday, May 19, 2008	Sheet 9 of 58





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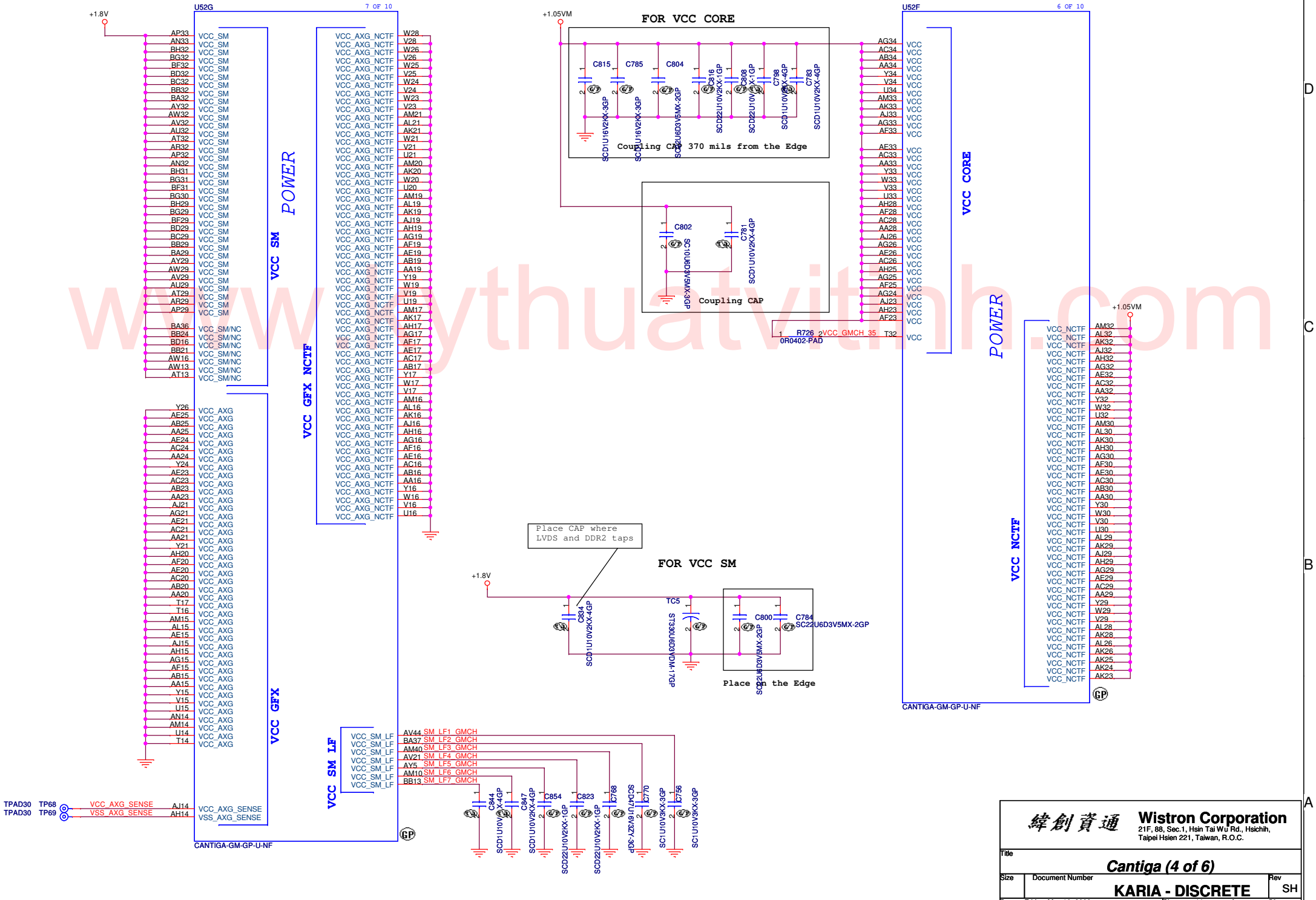
Title	***Cantiga (3 of 6)***
Size	Document Number: **KARIA - DISCRETE** Rev: SH
Date: Friday, May 16, 2008	Sheet 10 of 58



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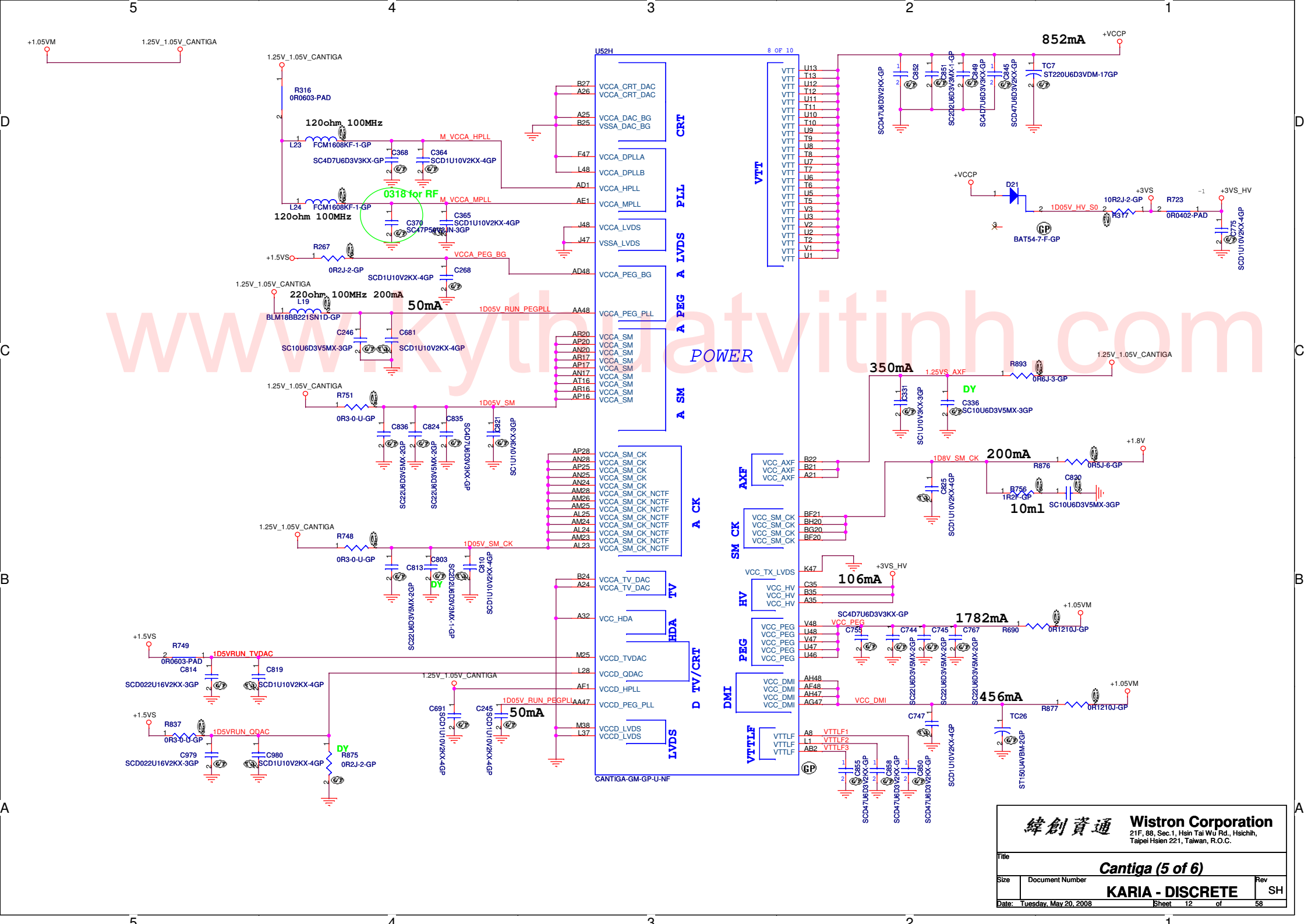
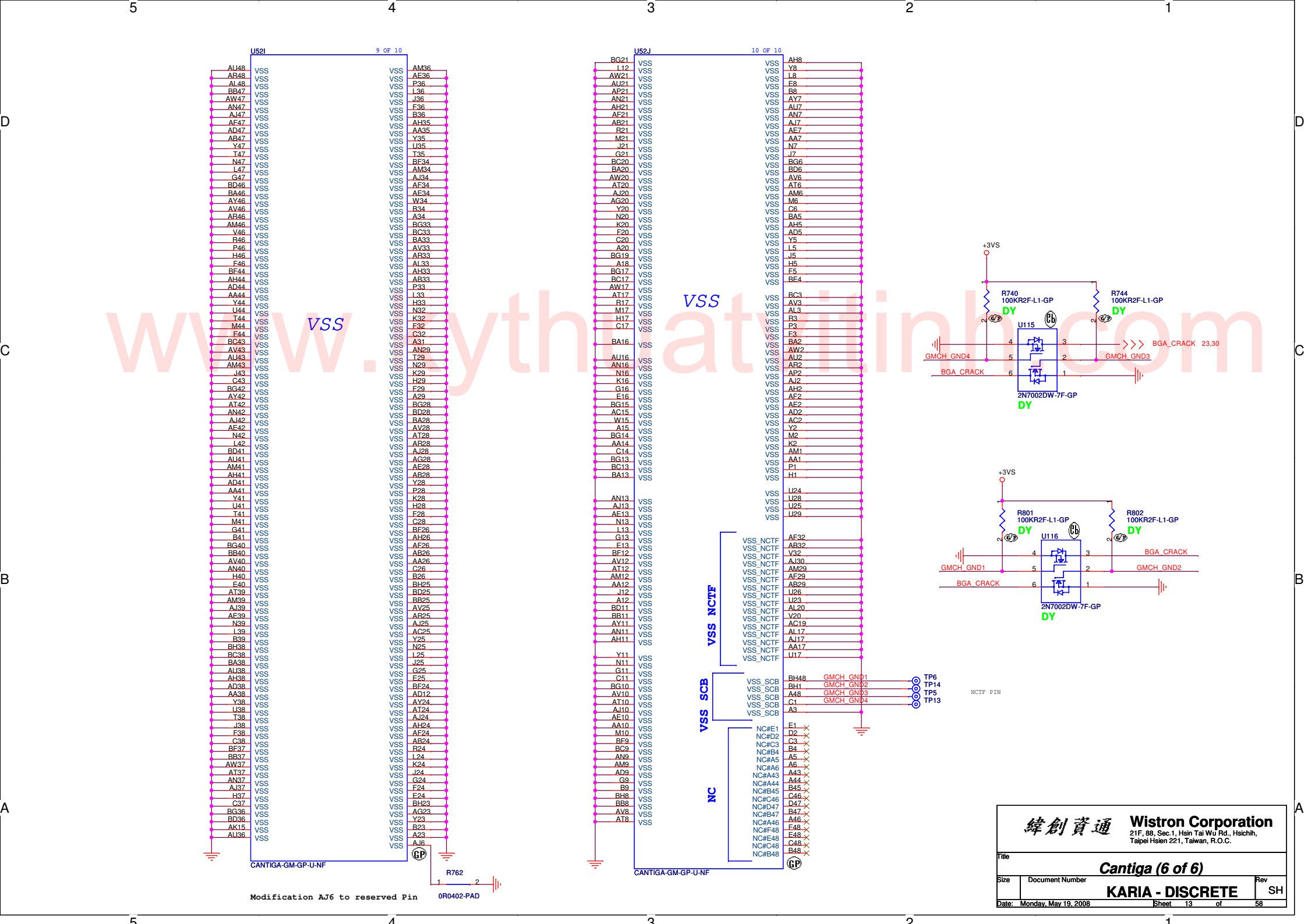
Title	***Cantiga (4 of 6)***
Size	Document Number: **KARIA - DISCRETE** Rev: SH
Date: Friday, May 16, 2008	Sheet 11 of 58





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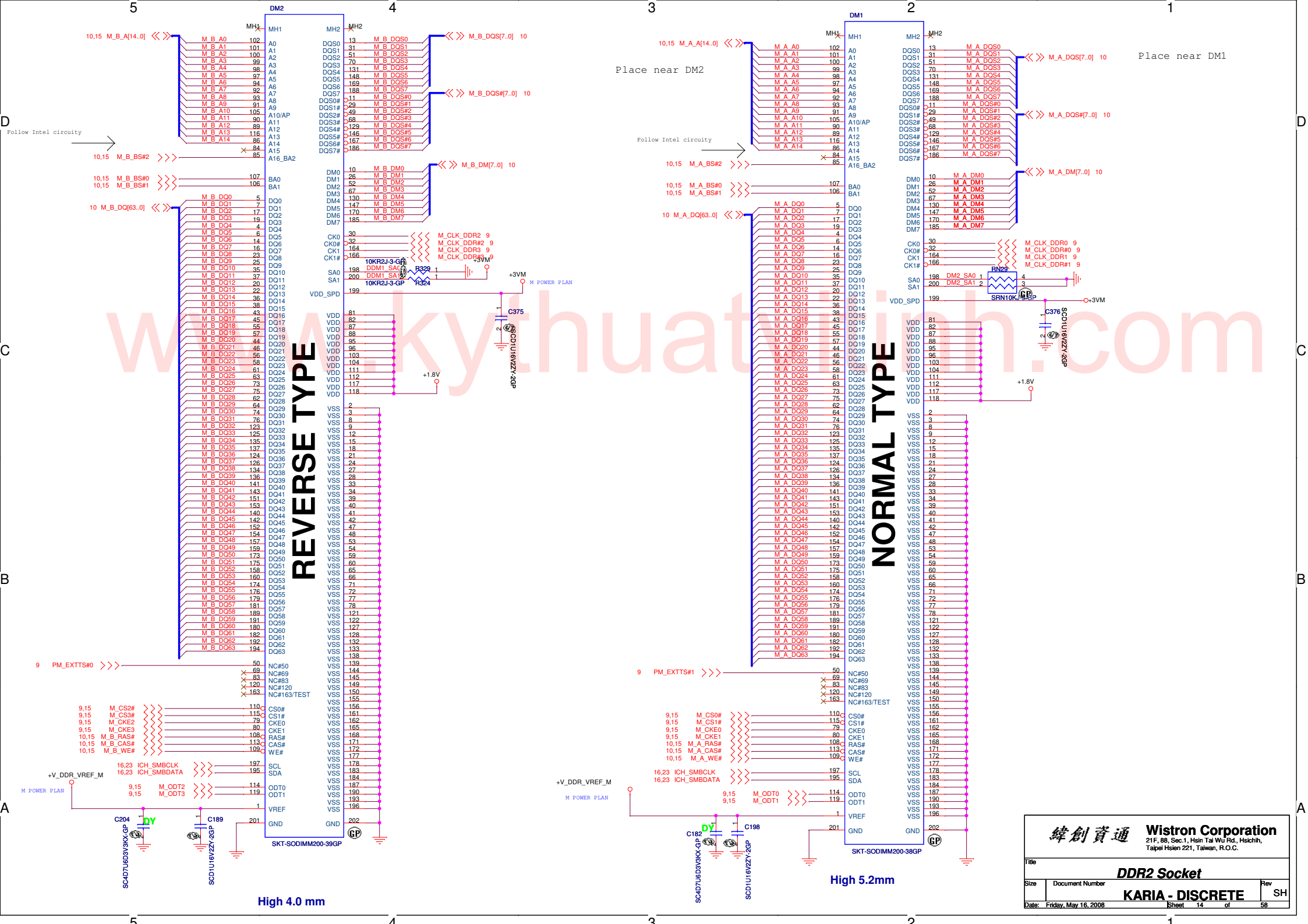
Title	Cantiga (6 of 6)
Size	Document Number: KARIA - DISCRETE
Rev	SH
Date: Monday, May 19, 2008	Sheet 13 of 58


DM2
REVERSE TYPE
SKT-SODIMM200-39GP
High 4.0 mm
Follow Intel circuitry
Place near DM2
DM1
NORMAL TYPE
SKT-SODIMM200-38GP
High 5.2mm
Place near DM1
Follow Intel circuitry
M POWER PLAN
+V_DDR_VREF_M
+3VM
+1.8V
10KR2J-3-GP
SRN10KJ-GP
SC4D7U6D3V3KX-GP
SCD1U16V2ZY-2GP
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DDR2 Socket
KARIA - DISCRETE
Date: Friday, May 16, 2008
Sheet 14 of 58

PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

+0.9V

RN18 SRN56J-5-GP
- M_CKE1 9,14
- M_A_A14
- M_A_A11
- M_A_A7

RN44 SRN56J-5-GP
- M_B_BS#1 10,14
- M_B_RAS# 10,14
- M_CS2# 9,14
- M_ODT2 9,14

RN26 SRN56J-5-GP
- M_B_A13
- M_ODT1 9,14
- M_CS1# 9,14

RN43 SRN56J-5-GP
- M_B_A6
- M_B_A4
- M_B_A2
- M_B_A0

RN21 SRN56J-5-GP
- M_A_A1
- M_A_A3
- M_A_A5
- M_A_A8

RN24 SRN56J-5-GP
- M_A_CAS# 10,14
- M_A_WE# 10,14
- M_A_BS#0 10,14
- M_A_A10

RN23 SRN56J-5-GP
- M_B_A8
- M_A_BS#1 10,14
- M_A_RAS# 10,14
- M_CS0# 9,14

RN42 SRN56J-5-GP
- M_CKE3 9,14
- M_B_A14
- M_B_A11
- M_B_A7

RN25 SRN56J-5-GP
- M_ODT0 9,14
- M_A_A13
- M_B_A5
- M_B_A3

RN19 SRN56J-5-GP
- M_A_A9
- M_A_A12
- M_A_BS#2 10,14
- M_CKE0 9,14

RN28 SRN56J-5-GP
- M_B_CAS# 10,14
- M_CS3# 9,14
- M_ODT3 9,14

RN27 SRN56J-5-GP
- M_B_A1
- M_B_A10
- M_B_BS#0 10,14
- M_B_WE# 10,14

RN20 SRN56J-5-GP
- M_CKE2 9,14
- M_B_BS#2 10,14
- M_B_A12
- M_A_A6

RN22 SRN56J-5-GP
- M_A_A4
- M_A_A2
- M_A_A0
- M_B_A9

M_A_A[14..0] >> M_A_A[14..0] 10,14

M_B_A[14..0] >> M_B_A[14..0] 10,14

Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

+0.9V

C322 C356 C284 C343 C346 C838 C806 C774 C316 C279 C760 C252 C753 C294 SCD1U16V2ZY-2GP

C772 C287 C350 C275 C286 C347 C253 C282 C251 C285 C832 C309 C277 SCD1U16V2ZY-2GP

Place these Caps near DM1

+1.8V

C811 C330 C361 C818 C786 SC2D2U6D3V3MX-1-GP

TC17 SE330U2D5VDM-LGP

C812 C843 C833 C805 SCD1U16V2ZY-2GP

Place the Cap near MCH

+1.8V

TC1 SE330U2D5VDM-LGP

Place these Caps near DM2

+1.8V

C311 C328 C334 C344 C297 SC2D2U6D3V3MX-1-GP

TC23 SE330U2D5VDM-LGP

C771 C315 C314 C822 SCD1U16V2ZY-2GP

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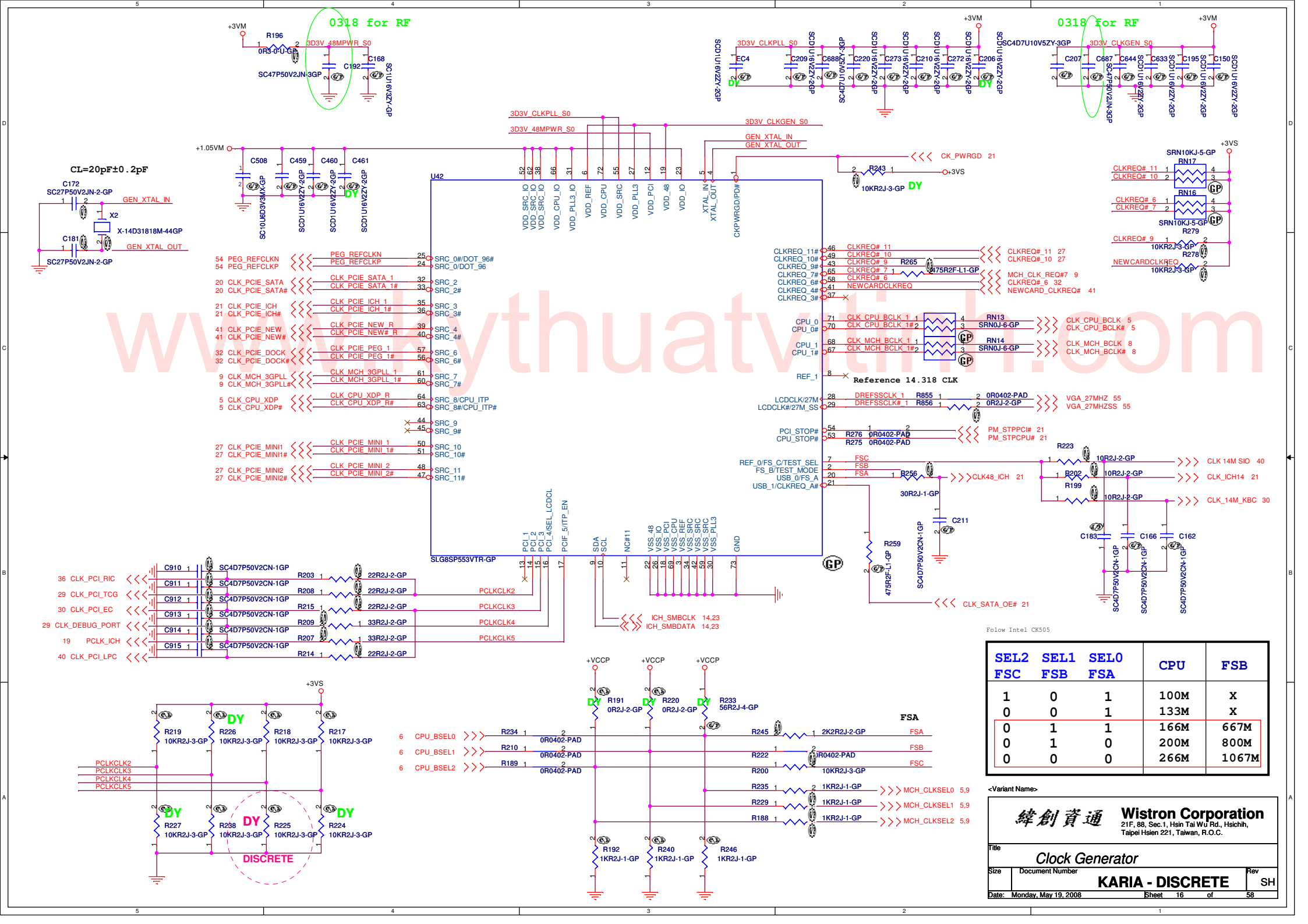
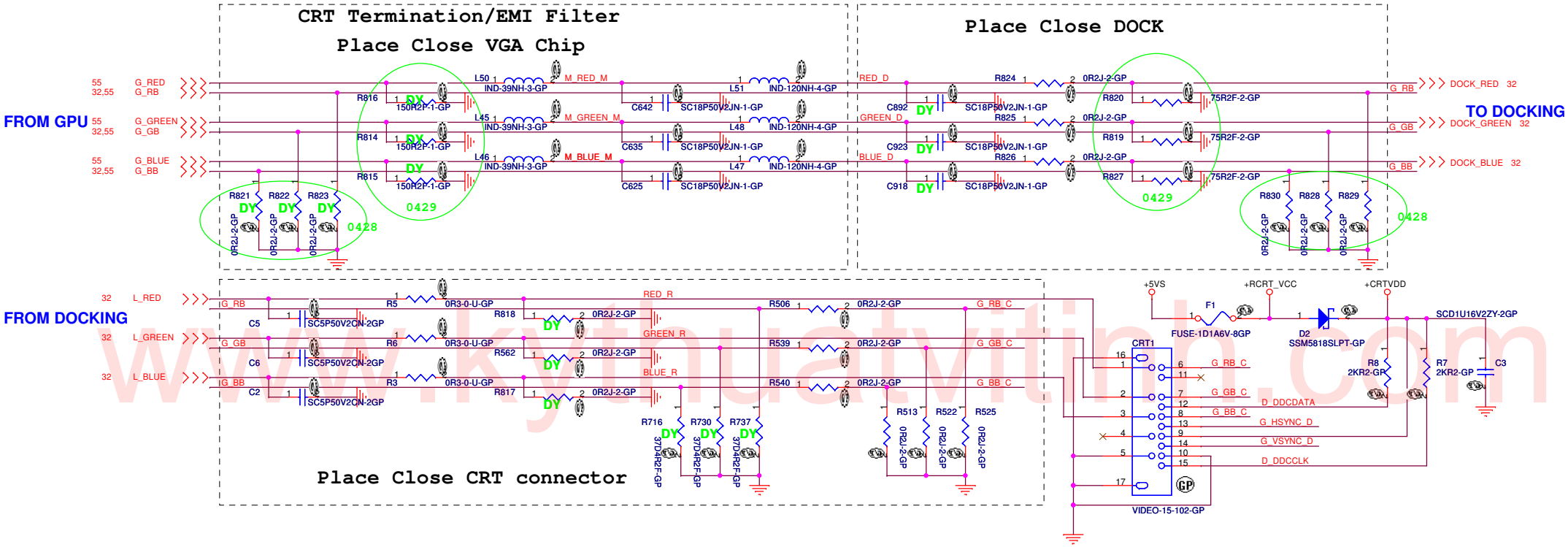
Title: DDR2 Termination Resistor

Size | Document Number: KARIA - DISCRETE | Rev: SH

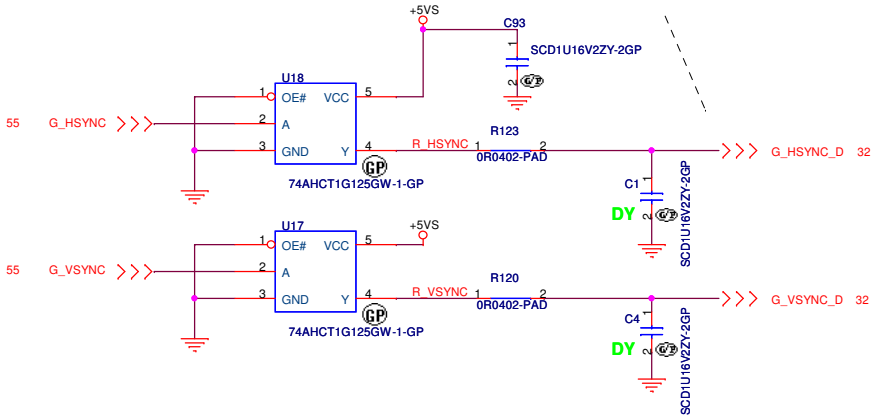
Date: Friday, May 16, 2008 | Sheet 15 of 58



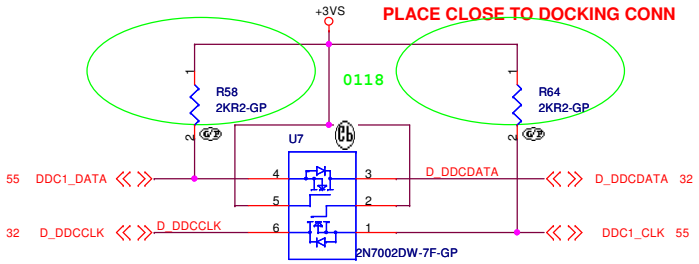
CRT



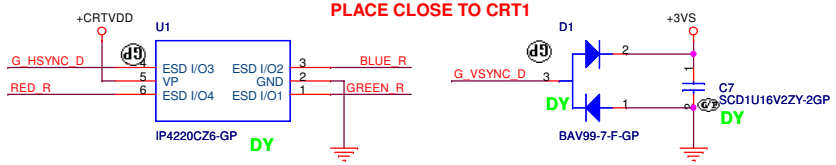
Layout Note : HSYNC & VSYNC SHOULD BE ROUTED TO DOCK CRT CONN. ,THEN TO SYSTEM CRT CONN.



PLACE CLOSE TO DOCKING CONN

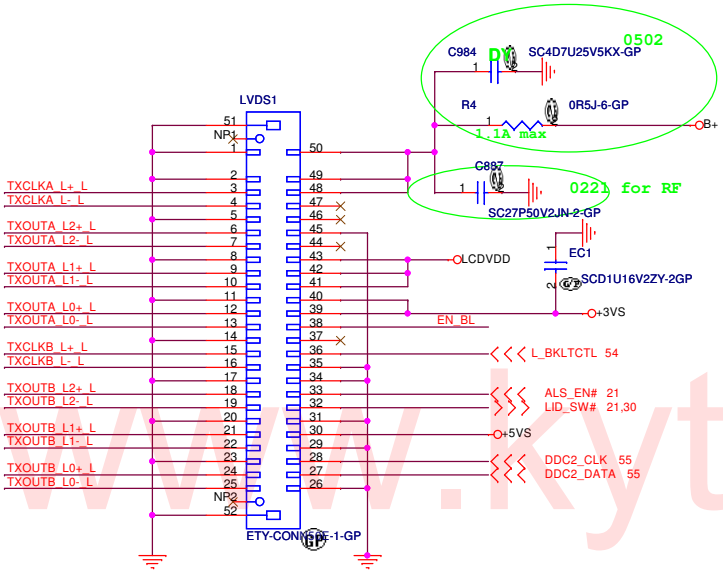


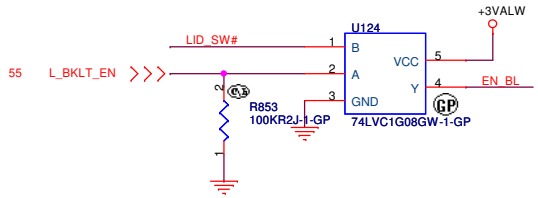
PLACE CLOSE TO CRT1

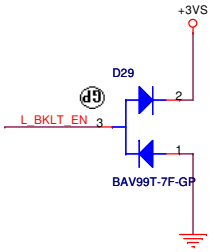


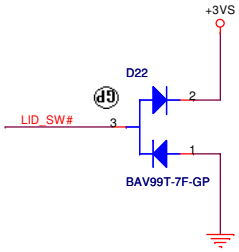
Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: **CRT CONNECTOR**		
Size: A3	Document Number: KARIA - DISCRETE	Rev: SH
Date: Monday, May 19, 2008	Sheet 17 of 58	

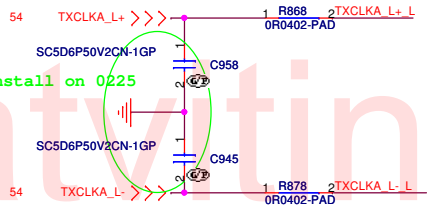
LVDS CONN

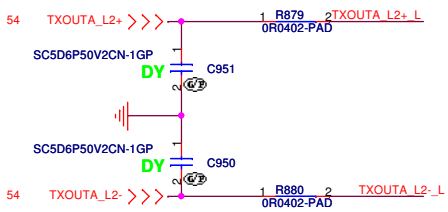


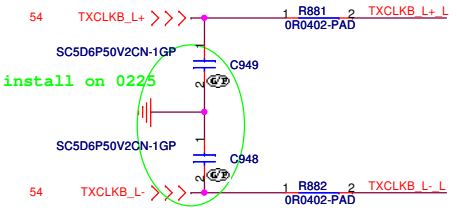


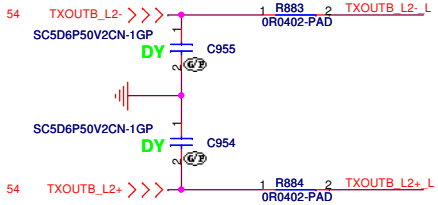


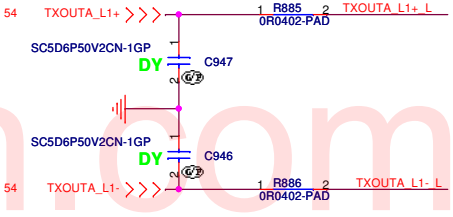


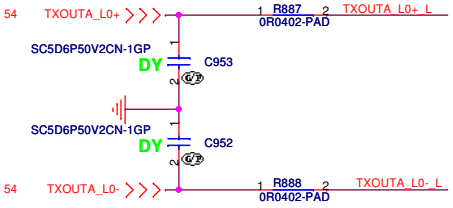


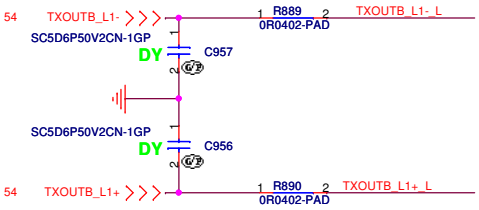


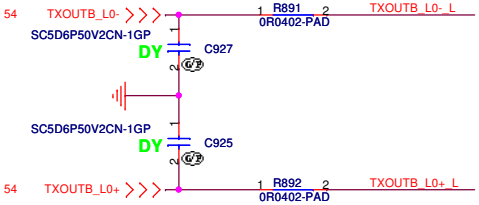




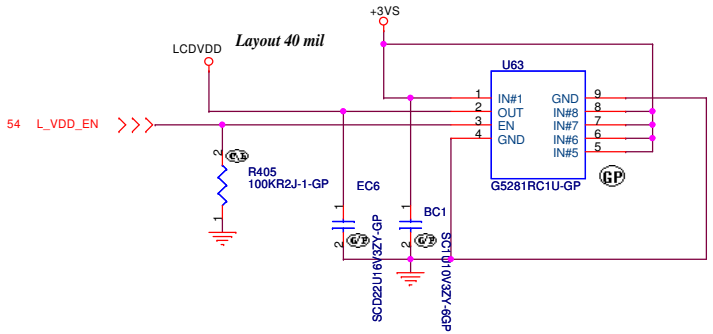








LCD POWER CIRCUIT



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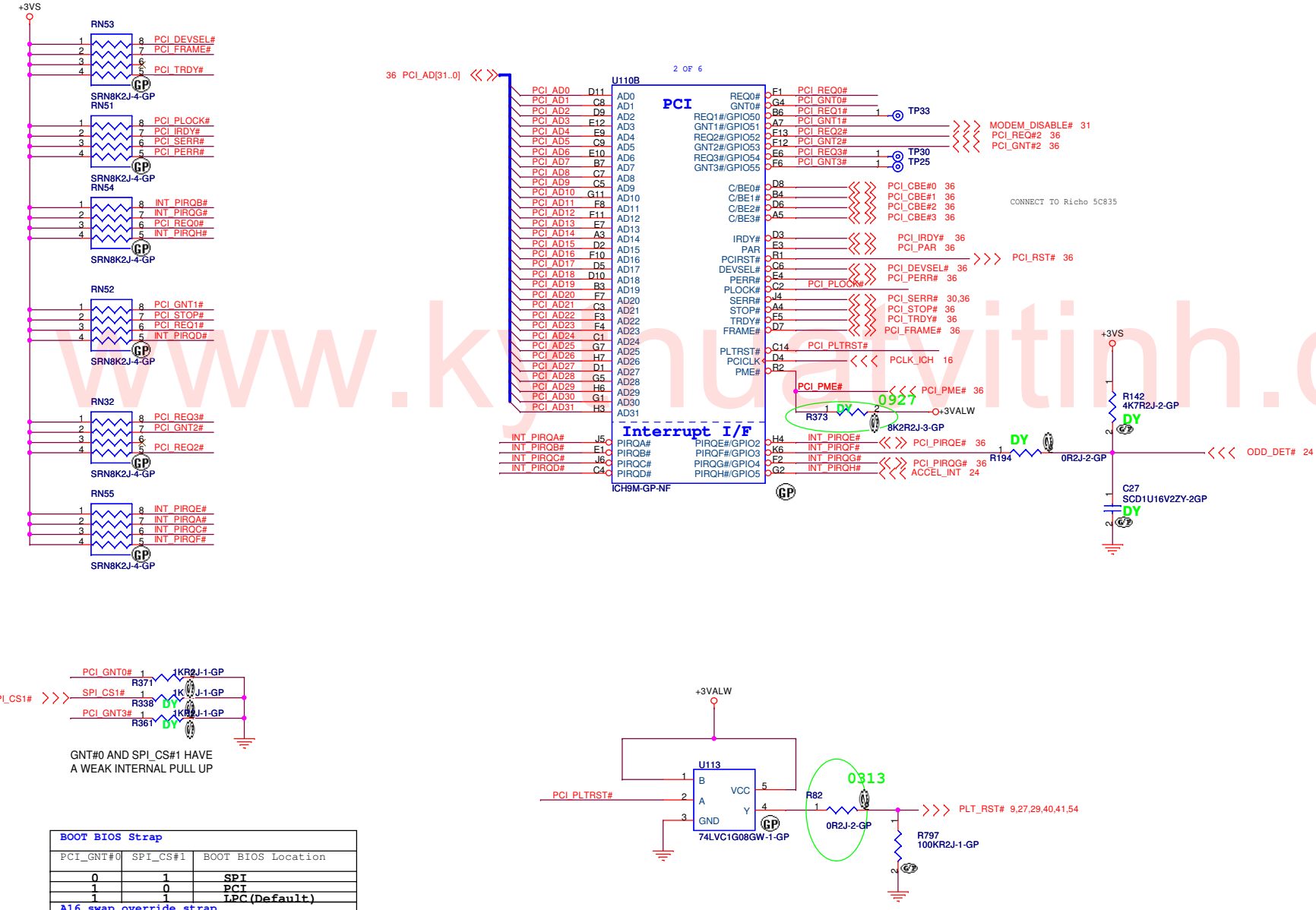
Title	***LCD CONN.***	
Size A3	Document Number **KARIA - DISCRETE**	Rev SH
Date: Friday, May 16, 2008	Sheet 18 of 58	



BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)
A16 swap override strap		
PCI_GNT#3	low = A16 swap override enable high = default	

<Variant Name>

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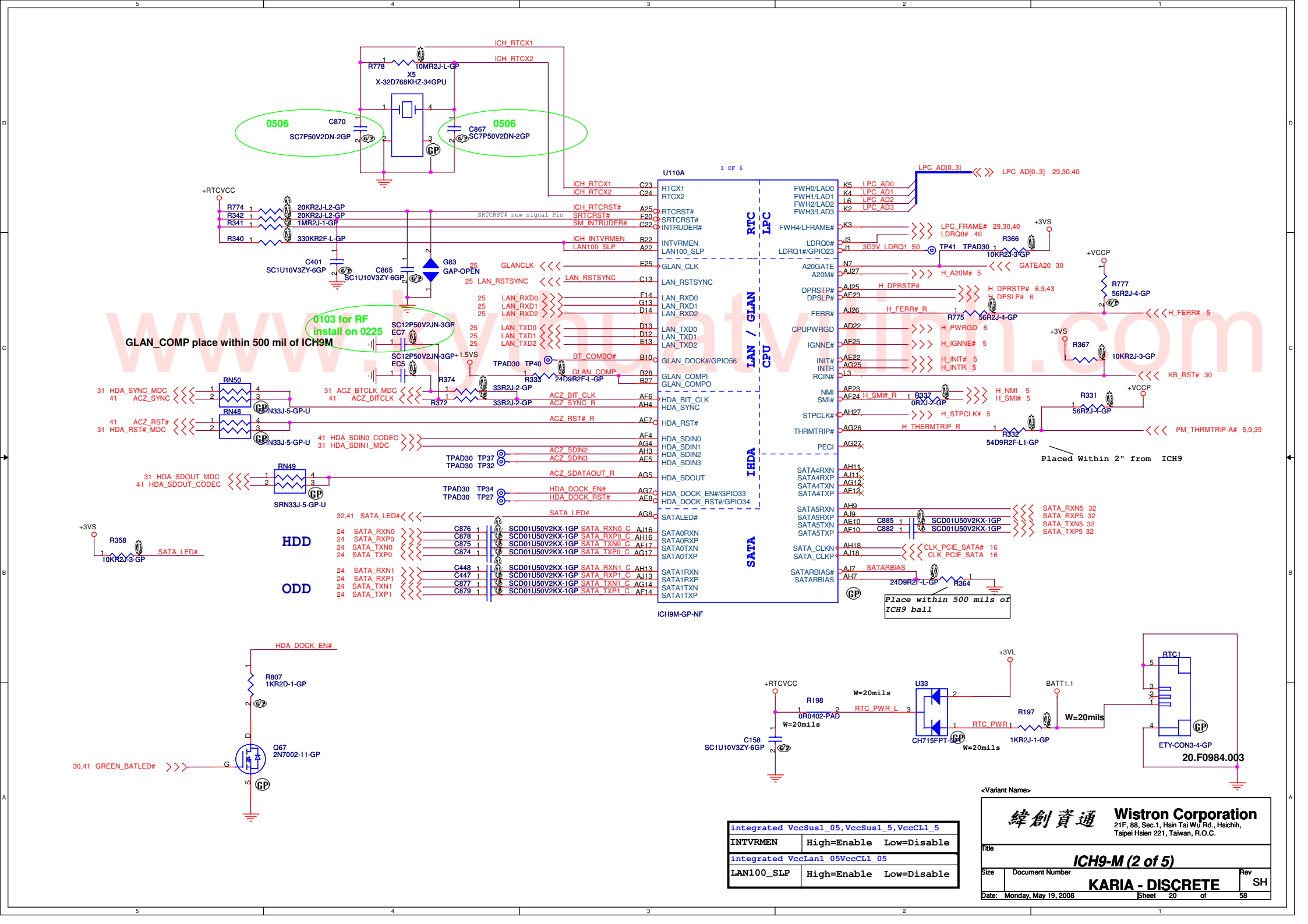
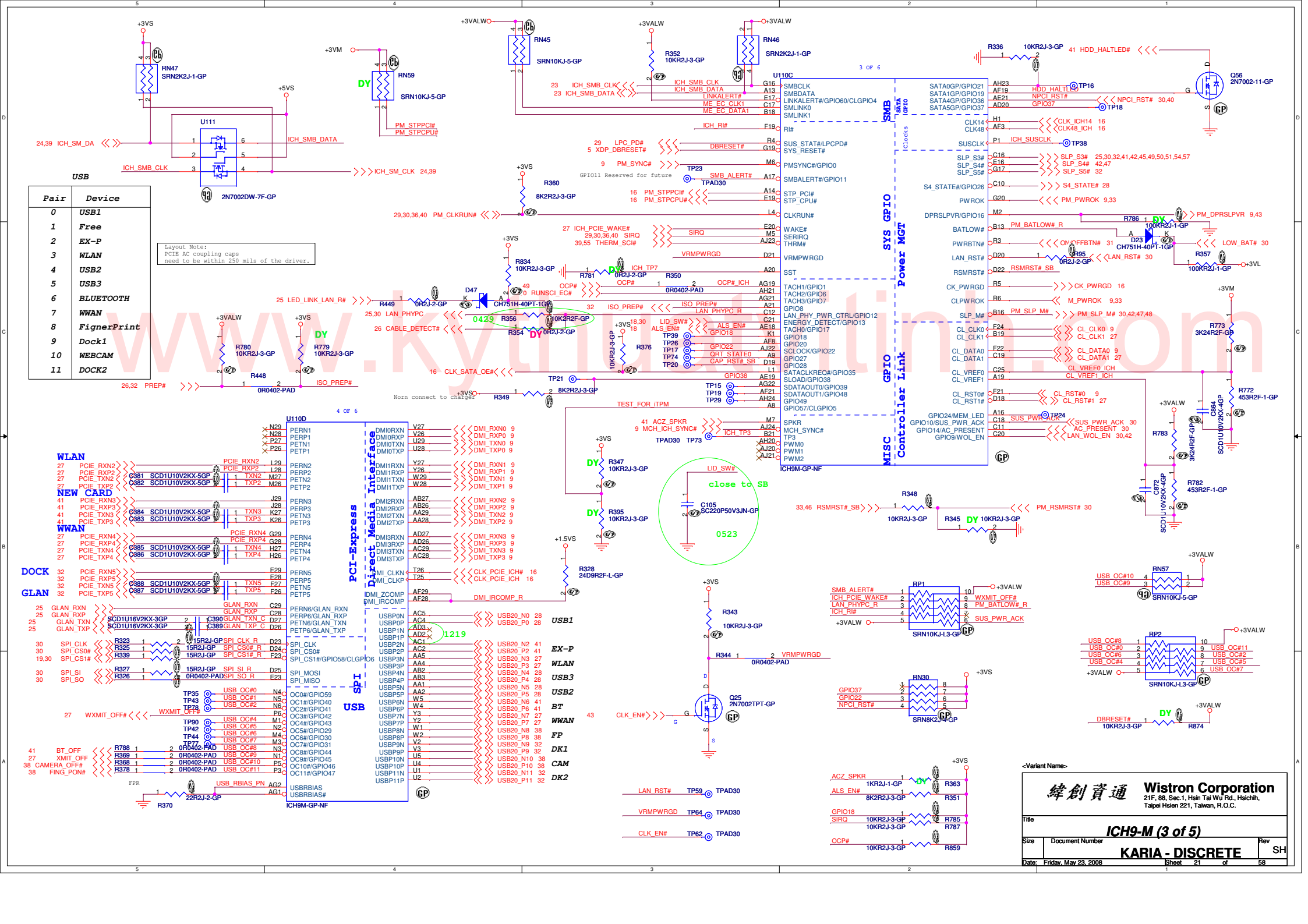
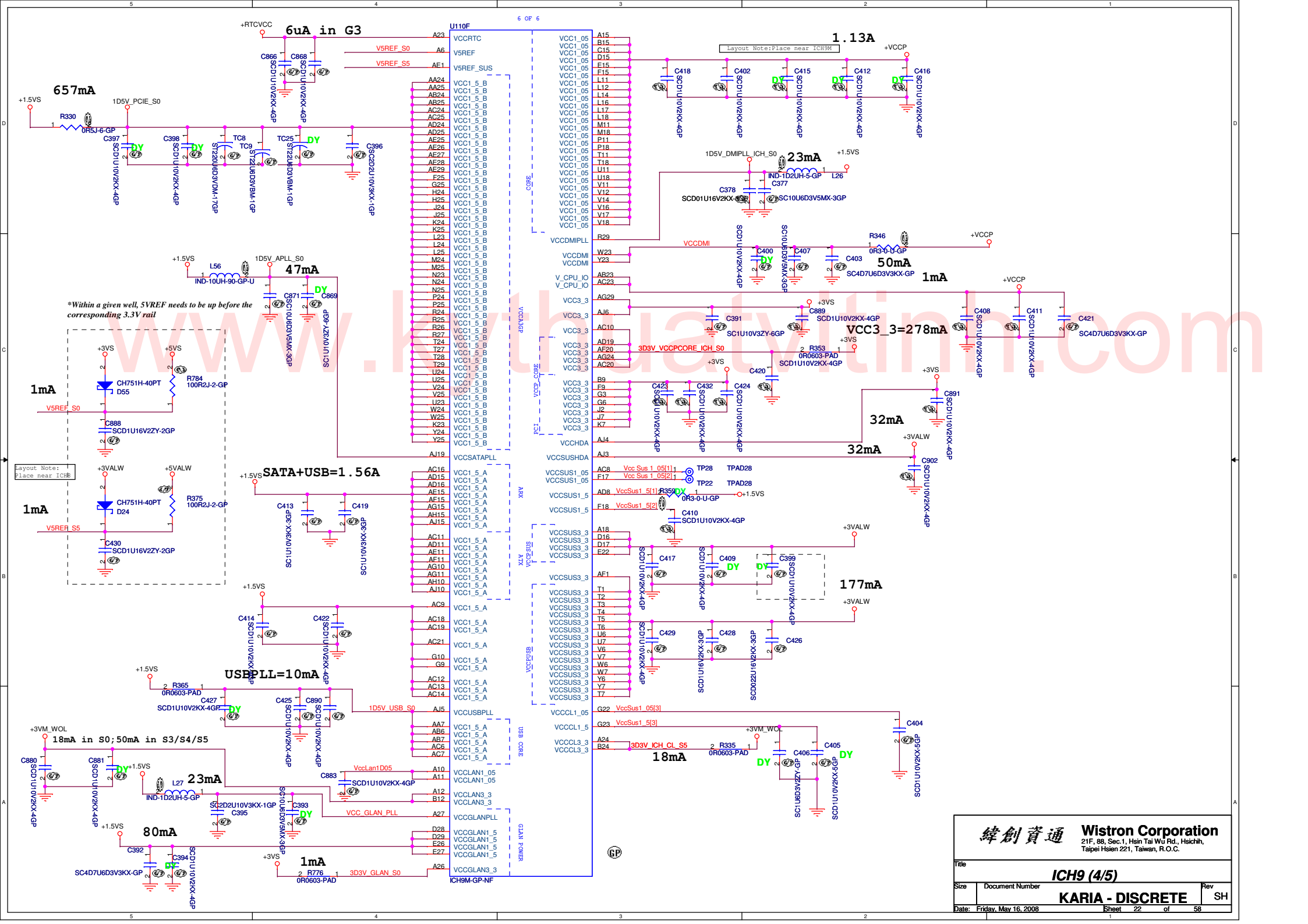
Title: ICH9-M (1 of 5)

Size | Document Number: KARIA - DISCRETE | Rev: SH

Date: Monday, May 19, 2008 | Sheet 19 of 58


ICH_RTCX1
ICH_RTCX2
R778 10MR2J-L-GP
X5
X-32D768KHZ-34GPU
0506
C870 SC7P50V2DN-2GP
C867 SC7P50V2DN-2GP
0506
+RTCVCC
R774 20KR2J-L2-GP
R342 20KR2J-L2-GP
R341 1MR2J-1-GP
R340 330KR2F-L-GP
C401 SC1U10V3ZY-6GP
C865 SC1U10V3ZY-6GP
G83 GAP-OPEN
SRTCRST# new signal Pin
ICH_RTCRST#
SRTCRST#
SM_INTRUDER#
ICH_INTVRMEN
LAN100_SLP
GLANCLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
BT_COMBO#
GLAN_COMP
GLAN_CLK
GLAN_DOCK#/GPIO56
GLAN_COMPI
GLAN_COMPO
0103 for RF
install on 0225
SC12P50V2JN-3GP EC7
SC12P50V2JN-3GP EC5
+1.5VS
TPAD30 TP40
R333 24D9R2F-L-GP
GLAN_COMP within 500 mil of ICH9M
U110A
1 OF 6
RTCX1
RTCX2
RTCRST#
SRTCRST#
INTRUDER#
INTVRMEN
LAN100_SLP
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
A20GATE
A20M#
DPRSTP#
DPSLP#
FERR#
CPUPWRGD
IGNNE#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THRMTRIP#
PECI
LPC_AD[0..3]
LPC_AD[0..3] 29,30,40
LPC_FRAME# 29,30,40
LDRQ0# 40
3D3V_LDRQ1_S0
TP41 TPAD30
R366 10KR2J-3-GP
+3VS
GATEA20 30
H_A20M# 5
H_DPRSTP# 6,9,43
H_DPSLP# 6
H_FERR# R
R775 56R2J-4-GP
H_FERR# 5
R777 56R2J-4-GP
+VCCP
H_PWRGD 6
H_IGNNE# 5
H_INIT# 5
H_INTR 5
R367 10KR2J-3-GP
KB_RST# 30
H_NMI 5
H_SMI# 5
R337 0R2J-2-GP
H_STPCLK# 5
H_THERMTRIP_R
R332 54D9R2F-L1-GP
R331 56R2J-4-GP
PM_THRMTRIP-A# 5,9,39
Placed Within 2" from ICH9
ICH9M-GP-NF
RN50
RN48
RN49
SRN33J-5-GP-U
31 HDA_SYNC_MDC
41 ACZ_SYNC
41 ACZ_RST#
31 HDA_RST#_MDC
31 HDA_SDOUT_MDC
41 HDA_SDOUT_CODEC
31 ACZ_BTCLK_MDC
41 ACZ_BITCLK
R372 33R2J-2-GP
R374 33R2J-2-GP
ACZ_BIT_CLK
ACZ_SYNC_R
ACZ_RST#_R
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT
41 HDA_SDIN0_CODEC
31 HDA_SDIN1_MDC
ACZ_SDIN2
ACZ_SDIN3
ACZ_SDATAOUT_R
TPAD30 TP37
TPAD30 TP32
TPAD30 TP34
TPAD30 TP27
HDA_DOCK_EN#
HDA_DOCK_RST#
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
SATA_LED#
SATALED#
+3VS
R358 10KR2J-3-GP
SATA_LED#
HDD
ODD
24 SATA_RXN0
24 SATA_RXP0
24 SATA_TXN0
24 SATA_TXP0
24 SATA_RXN1
24 SATA_RXP1
24 SATA_TXN1
24 SATA_TXP1
C876 C878 C875 C874
C448 C447 C877 C879
SCD01U50V2KX-1GP
SATA_RXN0_C AJ16
SATA_RXP0_C AH16
SATA_TXN0_C AE17
SATA_TXP0_C AG17
SATA_RXN1_C AH13
SATA_RXP1_C AJ13
SATA_TXN1_C AG14
SATA_TXP1_C AF14
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
C885 C882
SATA_RXN5 32
SATA_RXP5 32
SATA_TXN5 32
SATA_TXP5 32
SATA_CLKN
SATA_CLKP
CLK_PCIE_SATA# 16
CLK_PCIE_SATA 16
SATARBIAS#
SATARBIAS
R364 24D9R2F-L-GP
Place within 500 mils of ICH9 ball
HDA_DOCK_EN#
R807 1KR2D-1-GP
Q67 2N7002-11-GP
30,41 GREEN_BATLED#
+RTCVCC
R198 0R0402-PAD
W=20mils
C158 SC1U10V3ZY-6GP
U33 CH715FPT-GP
RTC_PWR_L
RTC_PWR
R197 1KR2J-1-GP
+3VL
BATT1.1
RTC1
ETY-CON3-4-GP
20.F0984.003
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
<Variant Name>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-M (2 of 5)
Size
Document Number
KARIA - DISCRETE
Rev
SH
Date: Monday, May 19, 2008
Sheet 20 of 58


USB
Pair | Device
0 | USB1
1 | Free
2 | EX-P
3 | WLAN
4 | USB2
5 | USB3
6 | BLUETOOTH
7 | WWAN
8 | FignerPrint
9 | Dock1
10 | WEBCAM
11 | DOCK2
Layout Note:
PCIE AC coupling caps
need to be within 250 mils of the driver.
WLAN
NEW CARD
WWAN
DOCK
GLAN
U110C
ICH9M-GP-NF
U110D
PCI-Express
Direct Media Interface
SPI
USB
SYS GPIO
Power MGT
GPIO
Controller Link
SMB
SATA GPIO
Clocks
MISC
USB1
EX-P
WLAN
USB3
USB2
BT
WWAN
FP
DK1
CAM
DK2
close to SB
C105
SC220P50V3JN-GP
0523
1219
Norn connect to charger
TEST_FOR_iTPM
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ICH9-M (3 of 5)
KARIA - DISCRETE
Date: Friday, May 23, 2008
Sheet 21 of 58


6 OF 6
U110F
ICH9M-GP-NF
6uA in G3
+RTCVCC
657mA
1D5V_PCIE_S0
R330
0R5J-6-GP
1.13A
Layout Note:Place near ICH9M
+VCCP
1D5V_DMIPLL_ICH_S0
23mA
IND-1D2UH-5-GP
L26
C378
SCD01U16V2KX-4GP
C377
SC10U6D3V5MX-3GP
VCCDMI
50mA
SC4D7U6D3V3KX-GP
R346
0R3-0-U-GP
1mA
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
1D5V_APLL_S0
47mA
L56
IND-10UH-90-GP-U
VCC3_3=278mA
3D3V_VCCPCORE_ICH_S0
R353
0R0603-PAD
SCD1U10V2KX-4GP
32mA
+3VALW
C902
SATA+USB=1.56A
177mA
USBPLL=10mA
R365
0R0603-PAD
1D5V_USB_S0
18mA in S0;50mA in S3/S4/S5
+3VM_WOL
L27
IND-1D2UH-5-GP
23mA
80mA
VCC_GLAN_PLL
3D3V_GLAN_S0
R776
0R0603-PAD
3D3V_ICH_CL_S5
R335
0R0603-PAD
18mA
Layout Note:
Place near ICH9
CH751H-40PT
D55
D24
R784
100R2J-2-GP
R375
100R2J-2-GP
V5REF_S0
V5REF_S5
TP28
TPAD28
TP22
TPAD28
Vcc Sus 1_05[1]
Vcc Sus 1_05[2]
VccSus1_5[1]
VccSus1_5[2]
R359
0R3-0-U-GP
VccLan1D05
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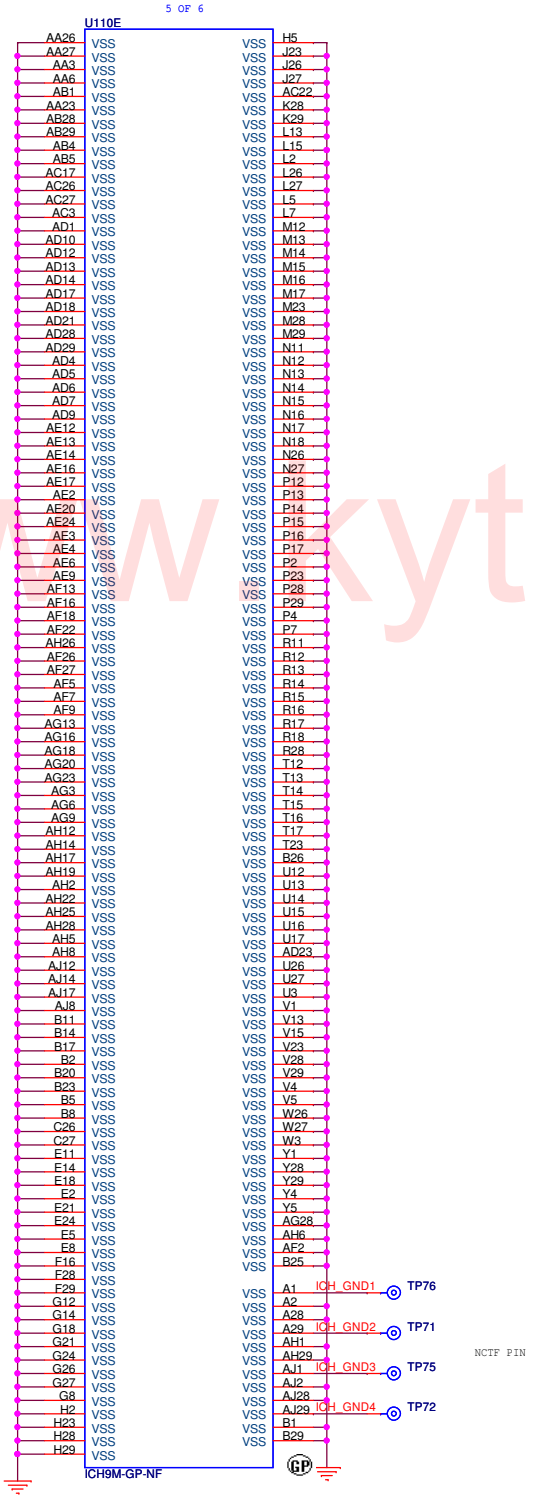
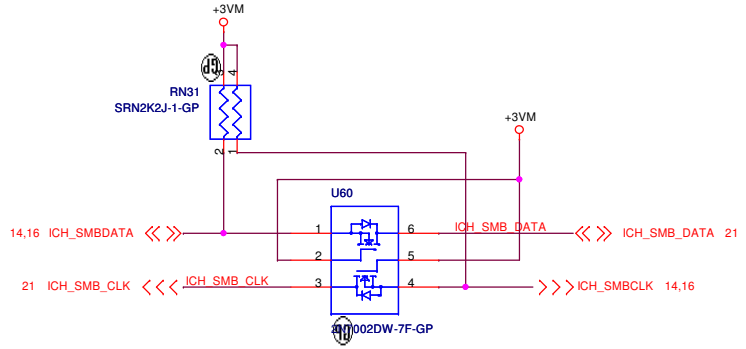
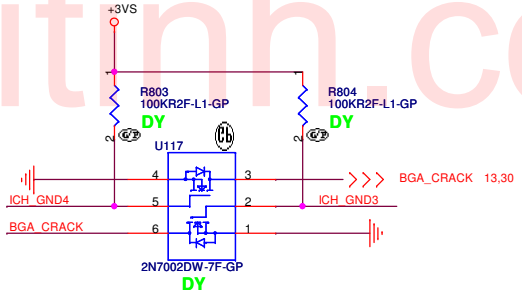
Taipei Hsien 221, Taiwan, R.O.C.
ICH9 (4/5)
KARIA - DISCRETE
Rev
SH
Date: Friday, May 16, 2008
Sheet 22 of 58

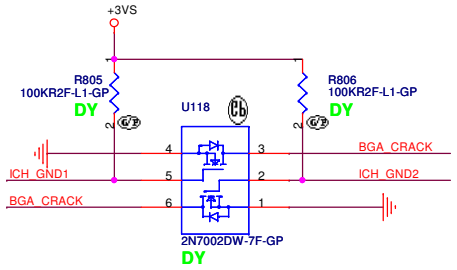




Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

SMBUS





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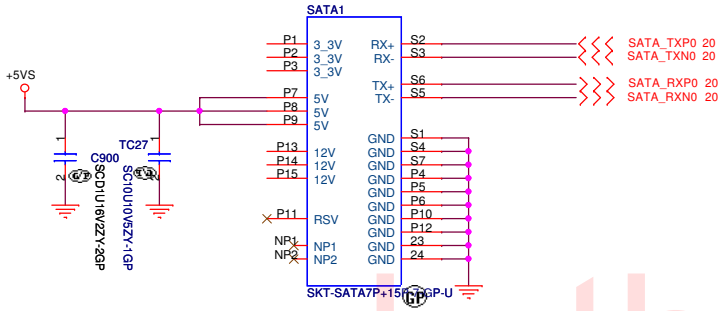
Title: **ICH9-M (5 of 5)**

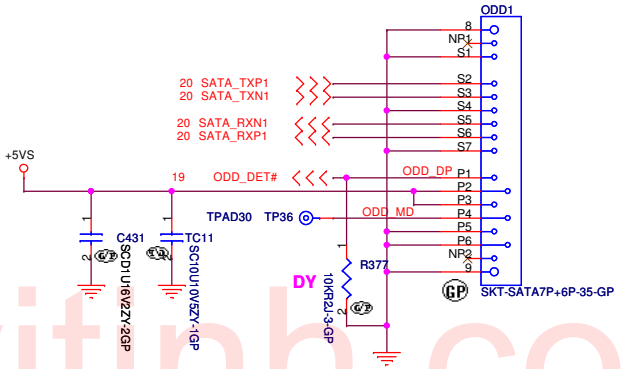
Size | Document Number: **KARIA - DISCRETE** | Rev: SH

Date: Friday, May 16, 2008 | Sheet 23 of 58

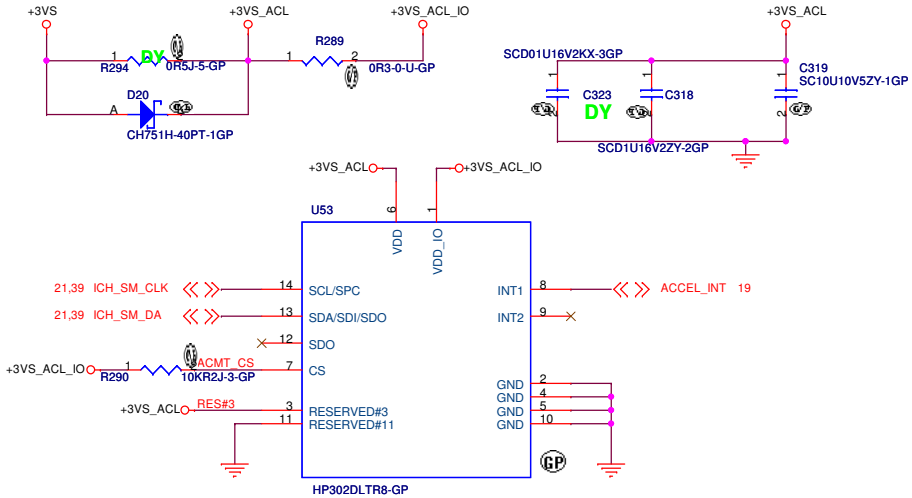
SATA HD Connector



ODD Connector



ACCELEROMETER



Must be placed in the center of the system

<Variant Name>

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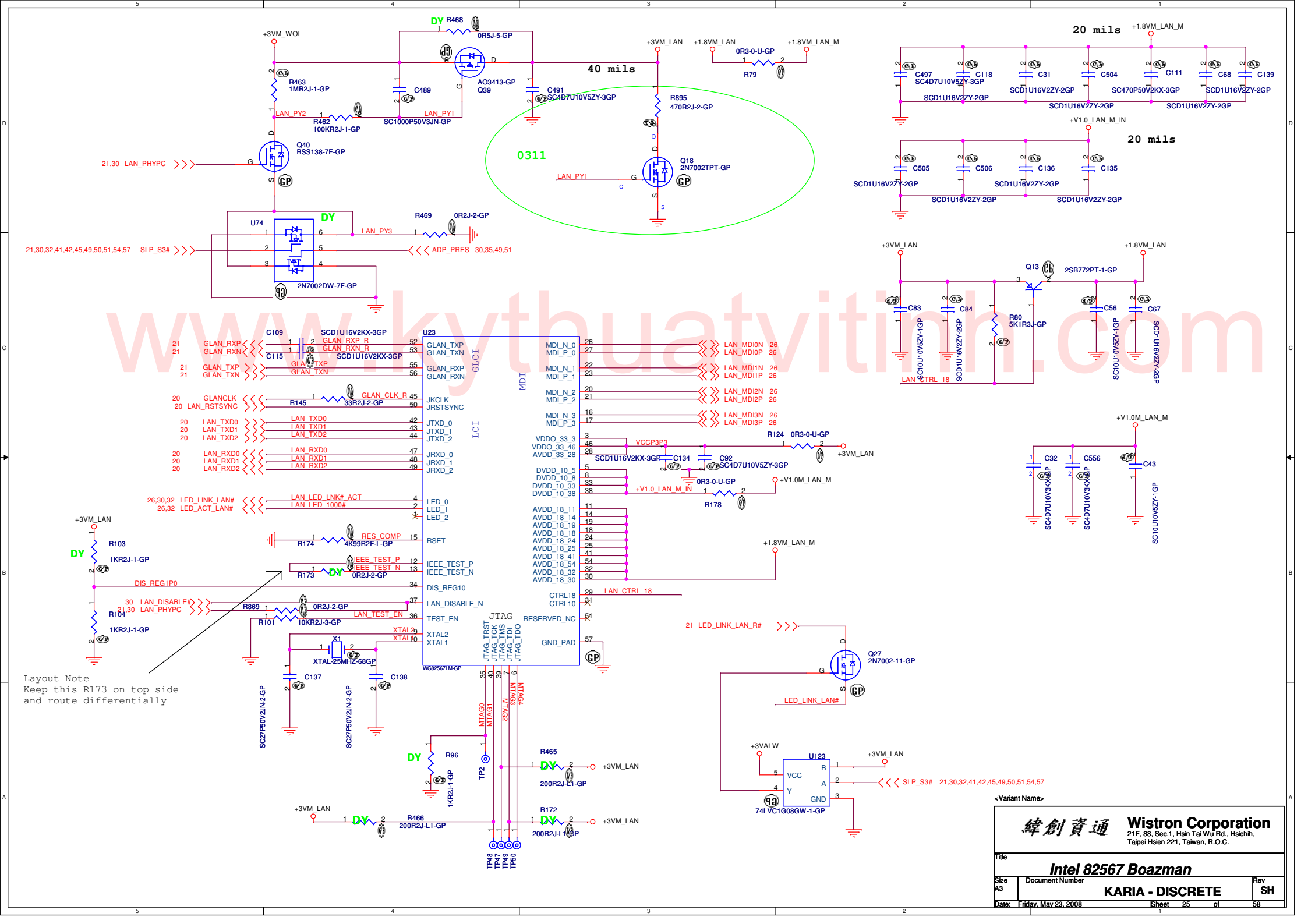
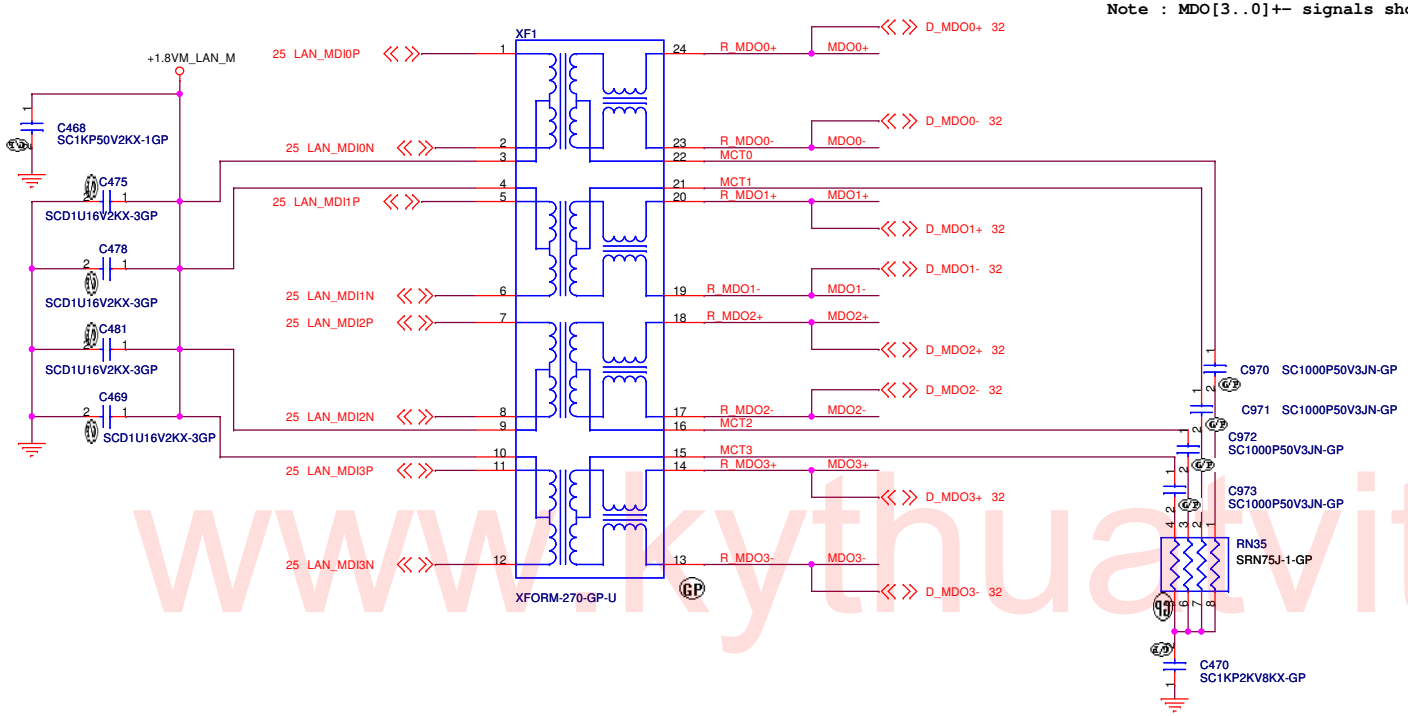
Title: ***HDD/ODD/ACCELEROMETER***

Size	Document Number	Rev
A3	KARIA - DISCRETE	SH

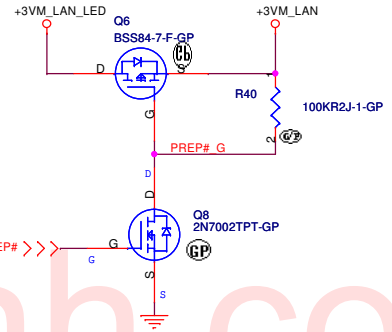
Date: Friday, May 16, 2008 Sheet 24 of 58

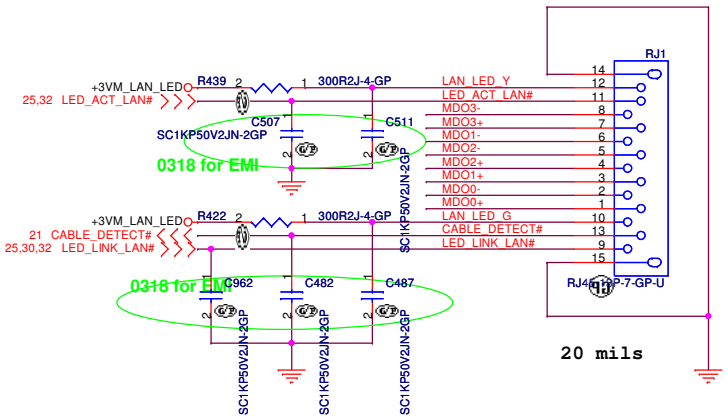


Note : MDO[3..0]+- signals should route to RJ45 first then to DOCK CONN .



LAN ENERGY DET





<Variant Name>

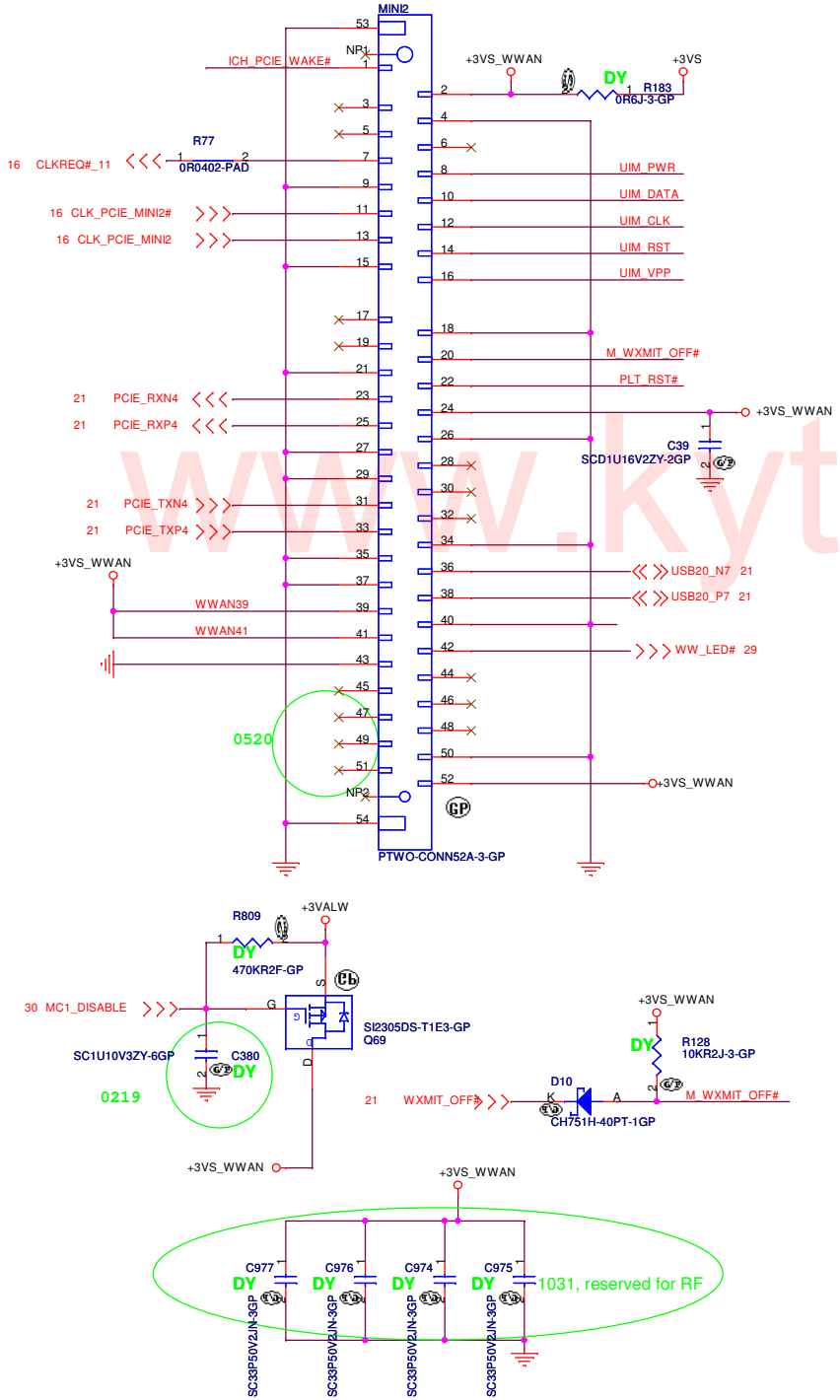
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Magnetic & RJ45***

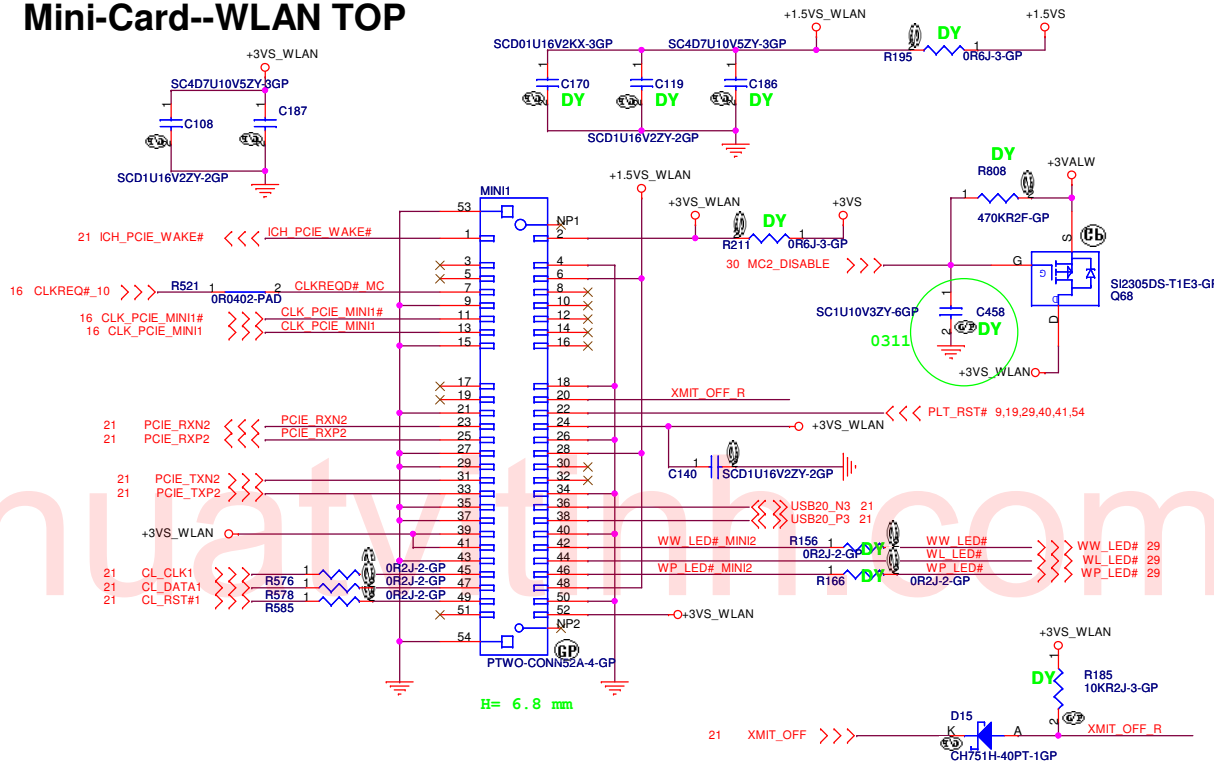
Size	Document Number	Rev
A3	KARIA - DISCRETE	SH

Date: Friday, May 16, 2008 Sheet 26 of 58

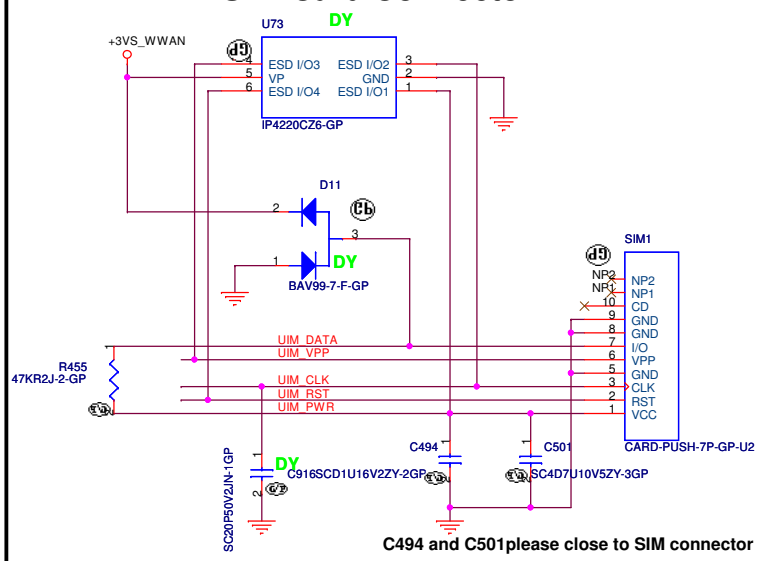
Mini-Card--WWAN BOTTOM



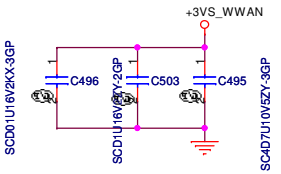
Mini-Card--WLAN TOP



Sim-Card Connector



C494 and C501please close to SIM connector



ACCELEROMETER moves to Page 24

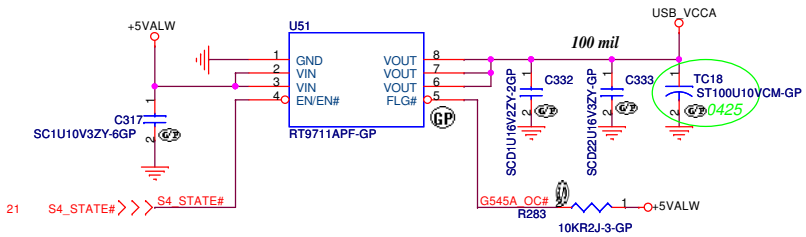
<Variant Name>

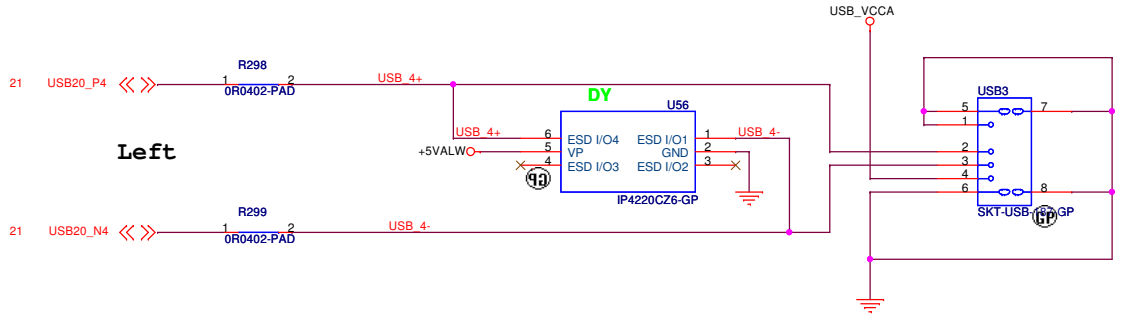
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

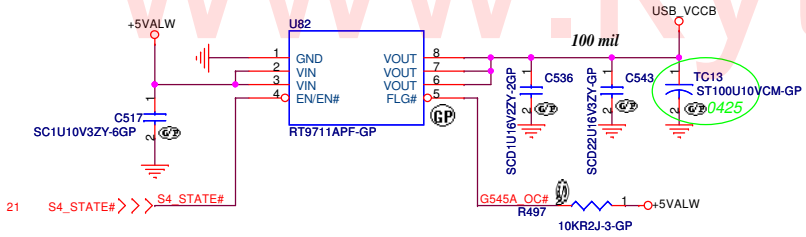
Title: **Mini-Card connectors**

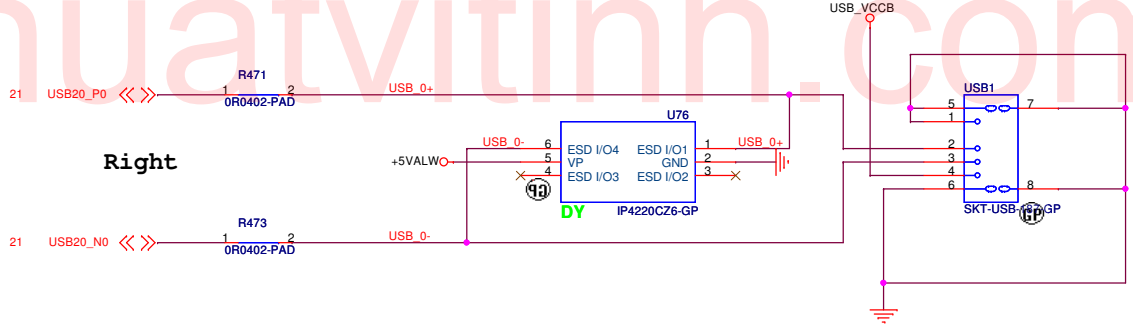
Size	Document Number	Rev
A3	KARIA - DISCRETE	SH

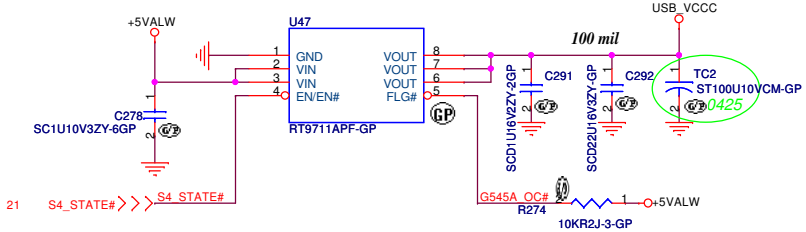
Date: Friday, May 23, 2008 Sheet 27 of 58

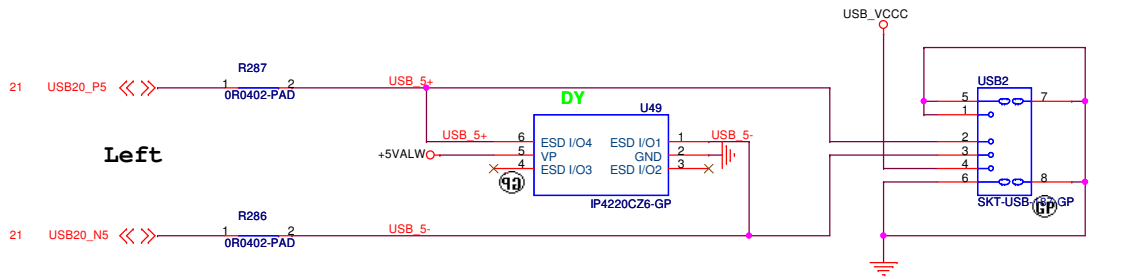












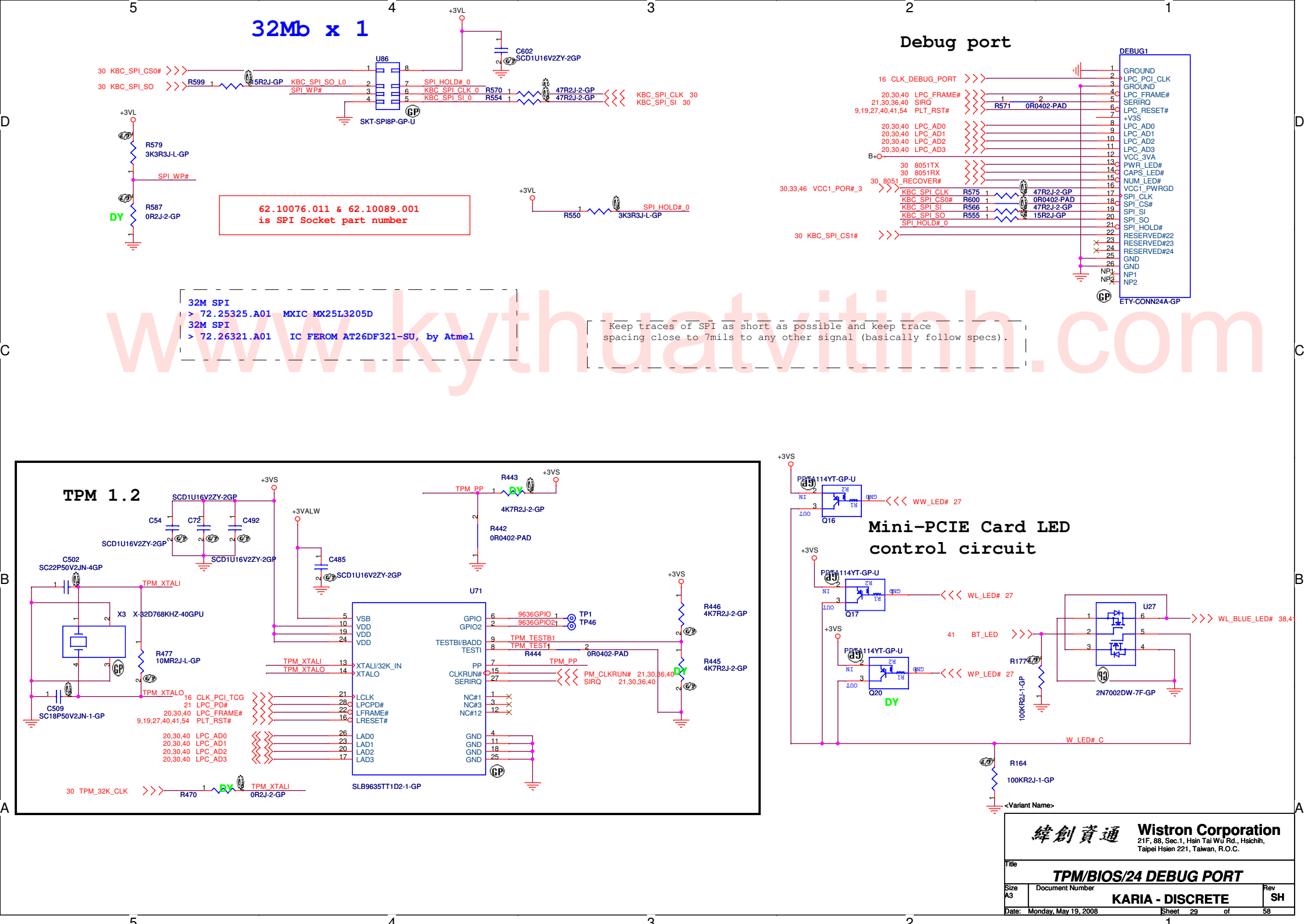
<Variant Name>

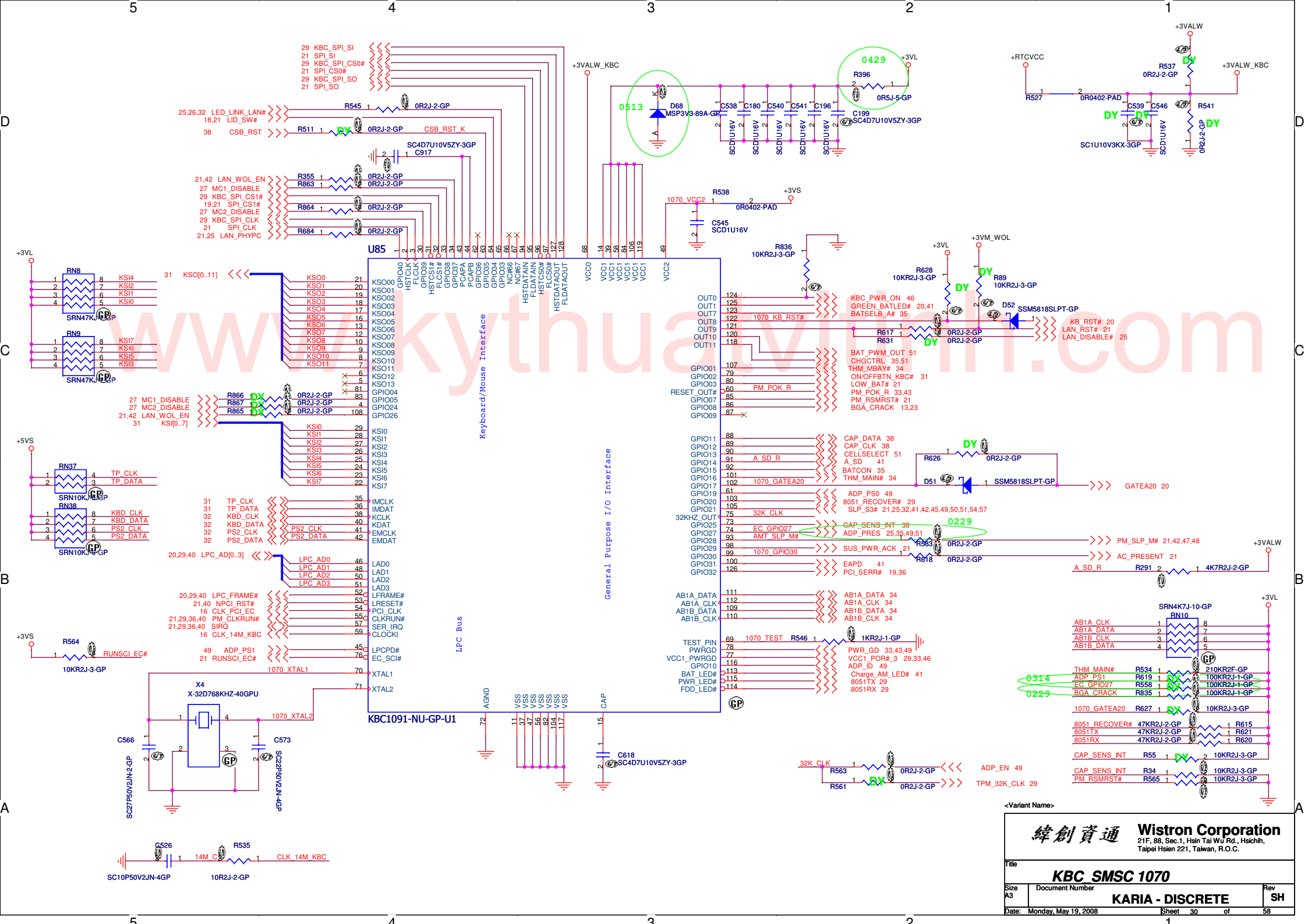
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

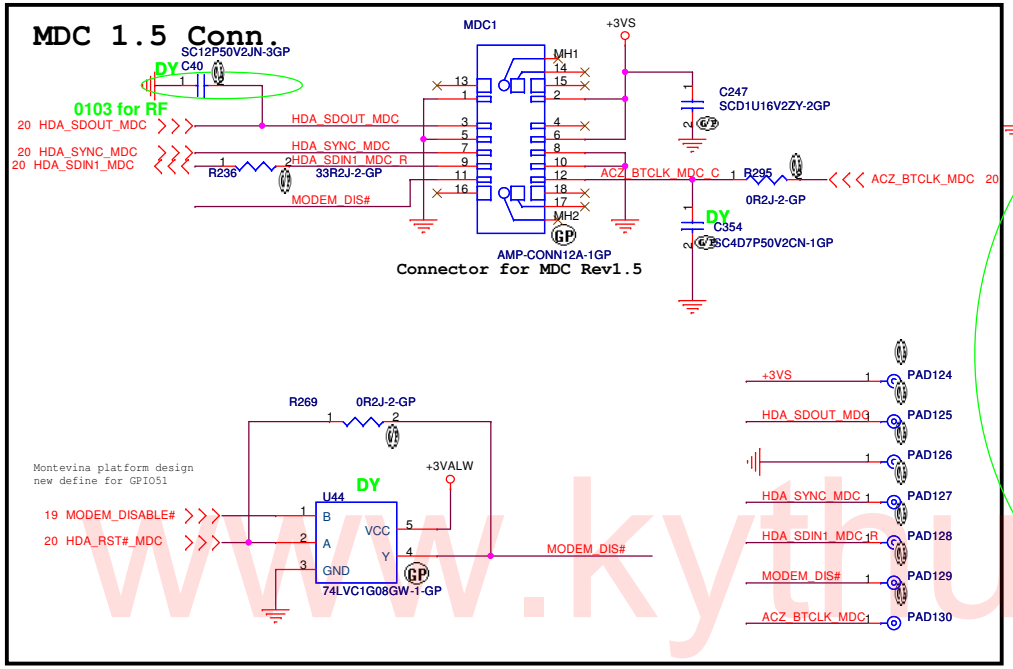
Title: **USB Connector**

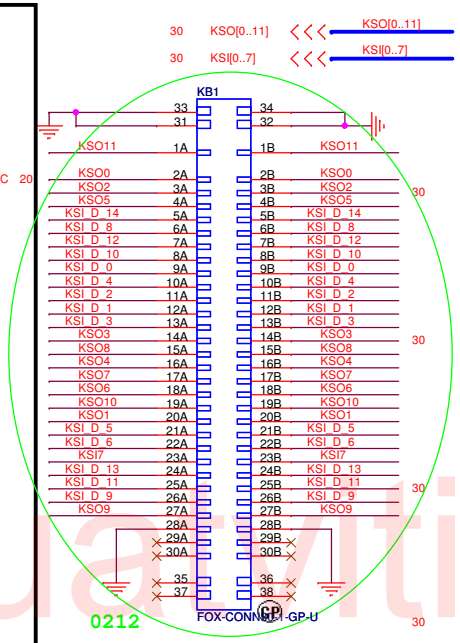
Size	Document Number	Rev
A3	KARIA - DISCRETE	SH

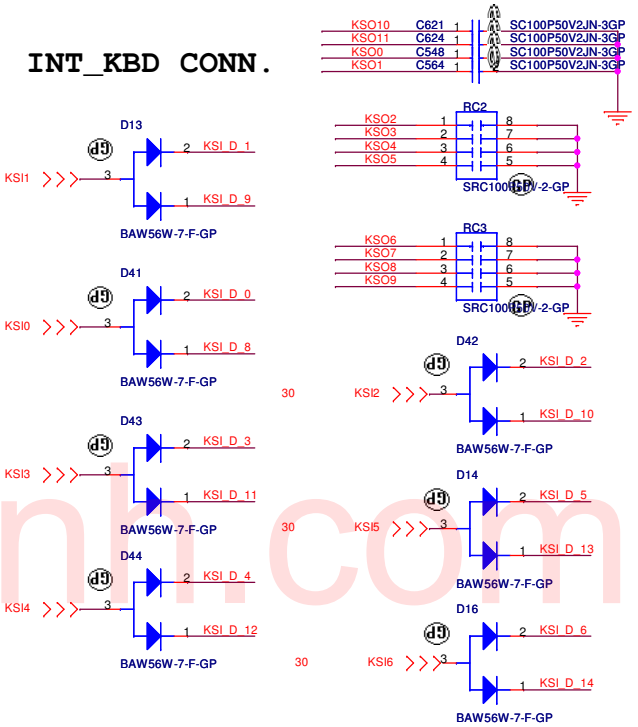
Date: Friday, May 16, 2008 Sheet 28 of 58

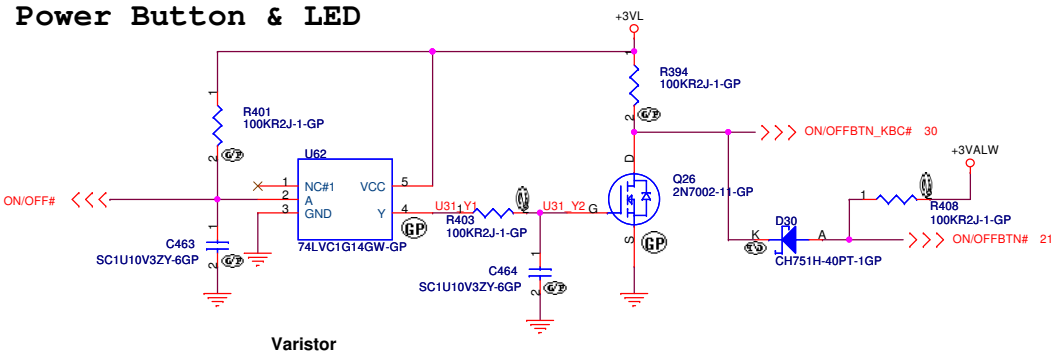


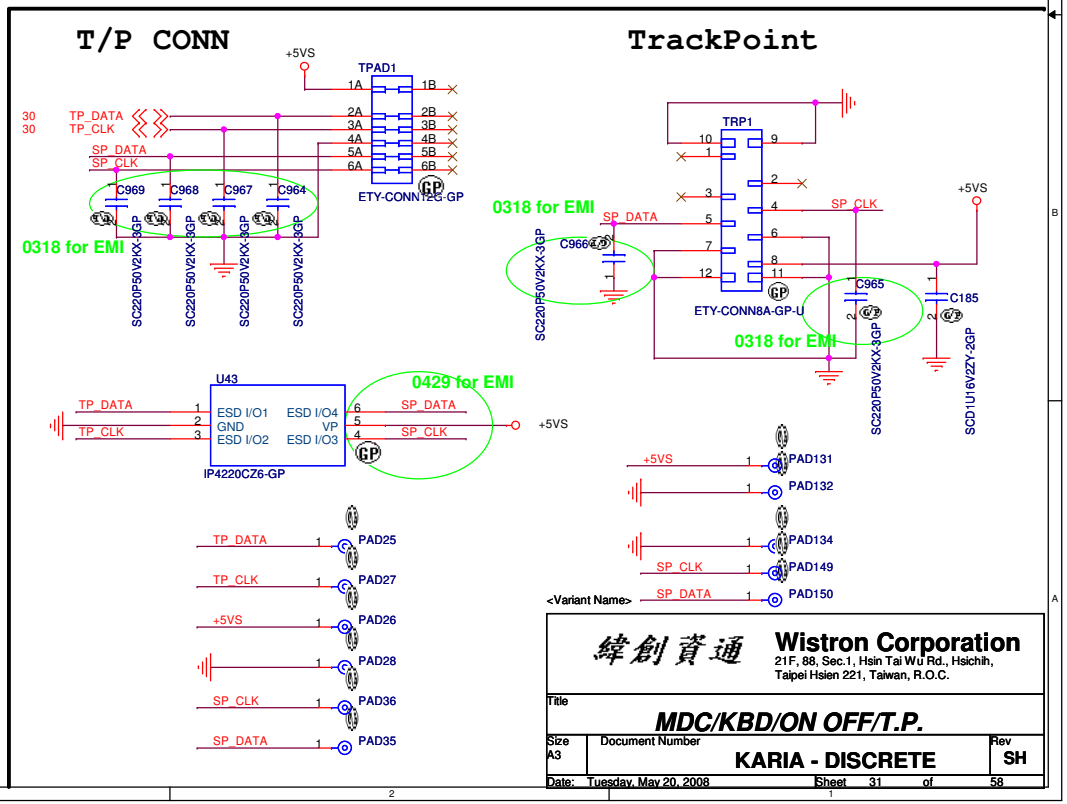






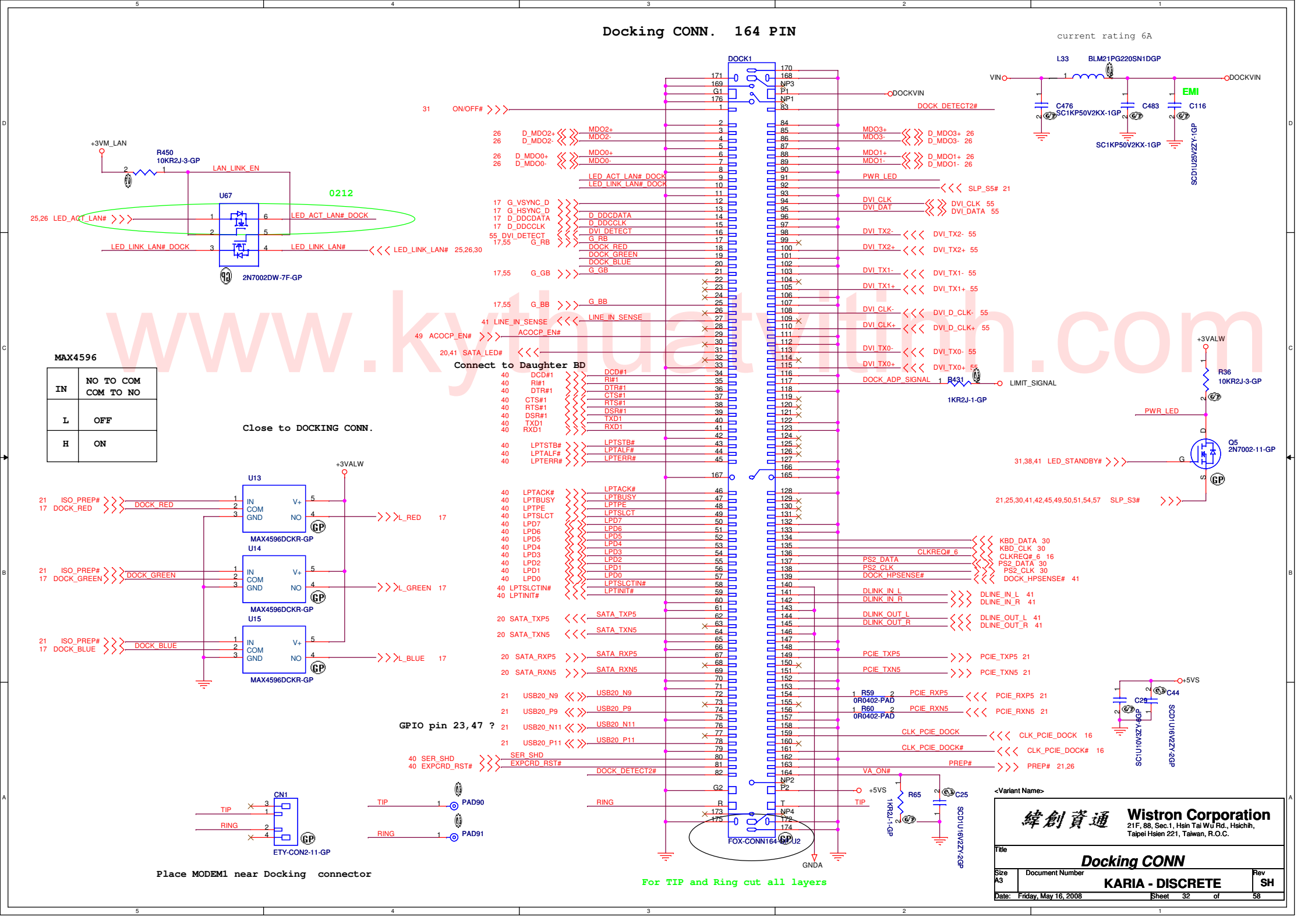






Docking CONN. 164 PIN

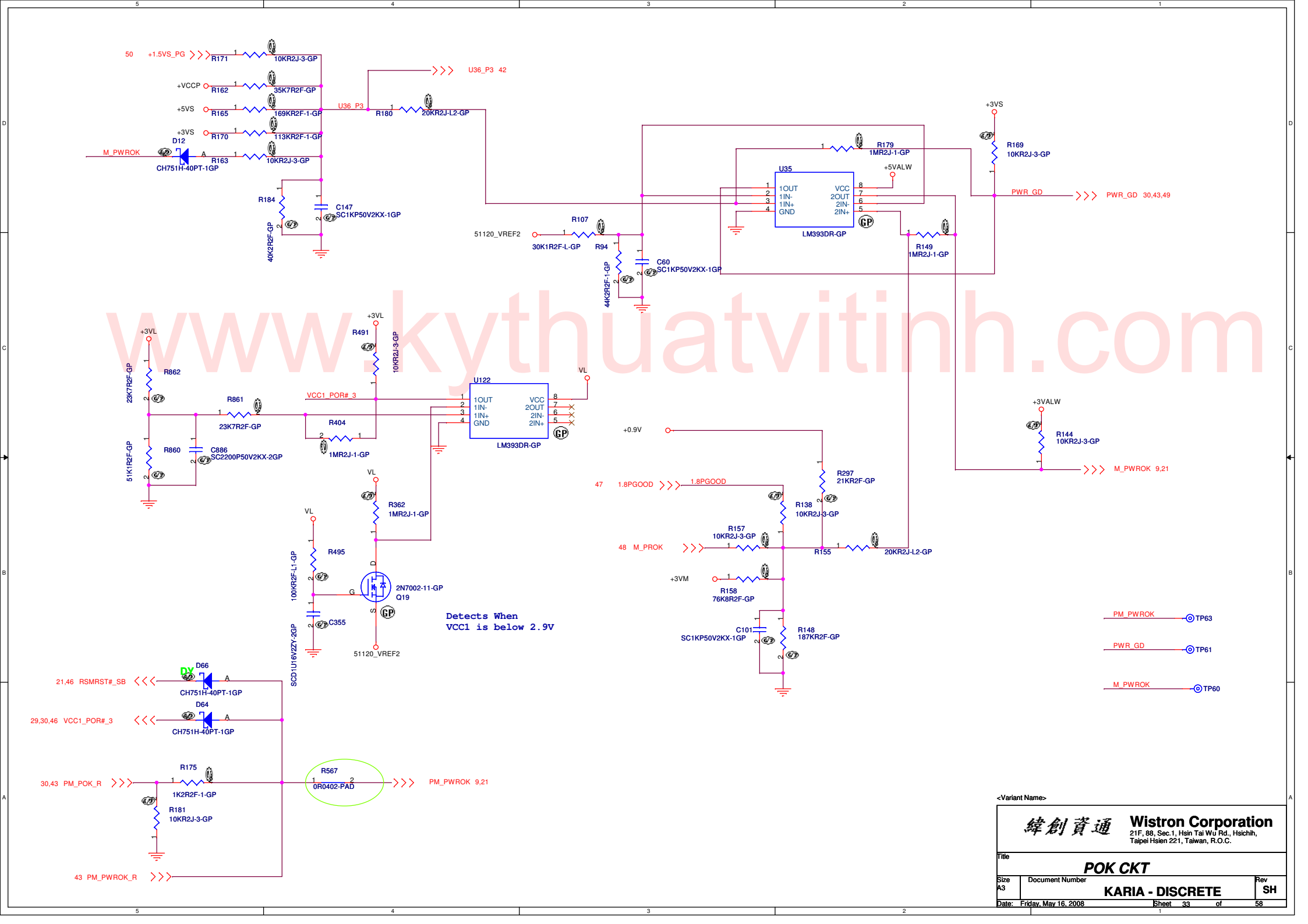
current rating 6A



Title	Docking CONN
Size A3	Document Number KARIA - DISCRETE
Rev	SH
Date: Friday, May 16, 2008	Sheet 32 of 58

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

<Variant Name>



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POK CKT

Size: A3 | Document Number: KARIA - DISCRETE | Rev: SH

Date: Friday, May 16, 2008 | Sheet 33 of 58

Adaptor in to generate DCBATOUT

Current Rating 6 A

0423

DCIN1

SKT-JACK-190-GP

LIMIT_SIGNAL

BC2 SC1KP50V2KX-1GP

DY

ADPIN

D67 PASSMJ27APT-GP

C10 SC1KP50V2KX-1GP

VIN

R11 15KR2J-1-GP

MAIN BATTERY CONNECTOR

Current Rating 6 A

BATT_A

0318 for EMI

C37 SC1KP50V2KX-1GP

BAT1

SYN-CON8-6-GP-U1

AB1A_DATA_C

AB1A_CLK_C

OCP_ADJ_C

R61 1KR2J-1-GP

C19 SC100P50V2JN-3GP

EMI

PIN 5 Voltage Feedback Circuit

D57 BAV99-5-GP

D58 BAV99-5-GP

+3VL

R71 100R2J-2-GP

R66 100R2J-2-GP

AB1A_DATA 30

AB1A_CLK 30

C33 SC100P50V2JN-3GP

C36 SC100P50V2JN-3GP

EMI

DY

C38 SC220P50V2KX-3GP

C28 SC220P50V2KX-3GP

D59 BAV99-5-GP

VL

R454 69K8R2F-GP

R453 100KR2F-L1-GP

R460 294KR3F-1-GP

49 OCP_ADJ

R457 150KR2F-L-GP

Q37 MMBT3906-3-GP

Q33 2N7002-11-GP

R440 220KR2F-GP

THM_MAIN# 30

CAPS name EMI It Reserve for EMI

BATT_A PAD115

AB1A_DATA_C PAD116

AB1A_CLK_C PAD117

OCP_ADJ_C PAD118

PAD119

BAY BATTERY CONNECTOR

Current Rating 6 A

BATT_B

0318 for EMI

C102 SCD1U25V2ZY-1GP

C518 SCD01U50V2ZY-1GP

BAT2

SYN-CON8-6-GP

AB1B_DATA_C

AB1B_CLK_C

THM_MBAY#_C

D60 BAV99-5-GP

D62 BAV99-5-GP

+3VL

R116 100R2J-2-GP

R105 100R2J-2-GP

R111 210KR2F-GP

R112 1KR2J-1-GP

AB1B_DATA 30

AB1B_CLK 30

THM_MBAY# 30

C77 SC100P50V2JN-3GP

C80 SC100P50V2JN-3GP

C73 SC100P50V2JN-3GP

EMI

D61 BAV99-5-GP

C82 SC220P50V2KX-3GP

DY

C65 SC220P50V2KX-3GP

C78 SC220P50V2KX-3GP

BATT_B PAD120

AB1B_DATA_C PAD121

AB1B_CLK_C PAD122

THM_MBAY#_C PAD123

<Variant Name>

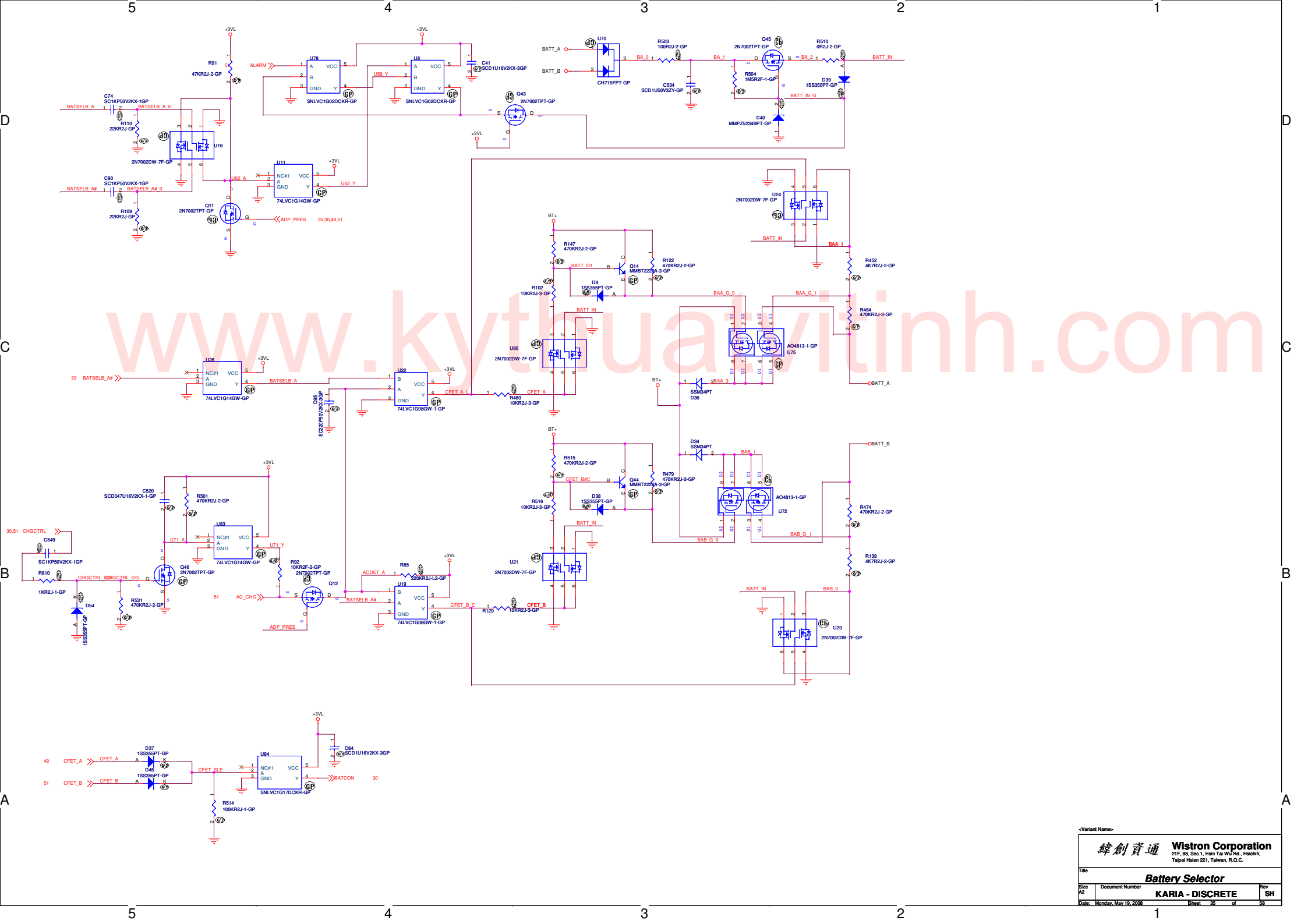
緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: DC & BATTERT CONN.

Size: A3 | Document Number: KARIA - DISCRETE | Rev: SH

Date: Friday, May 16, 2008 | Sheet 34 of 58



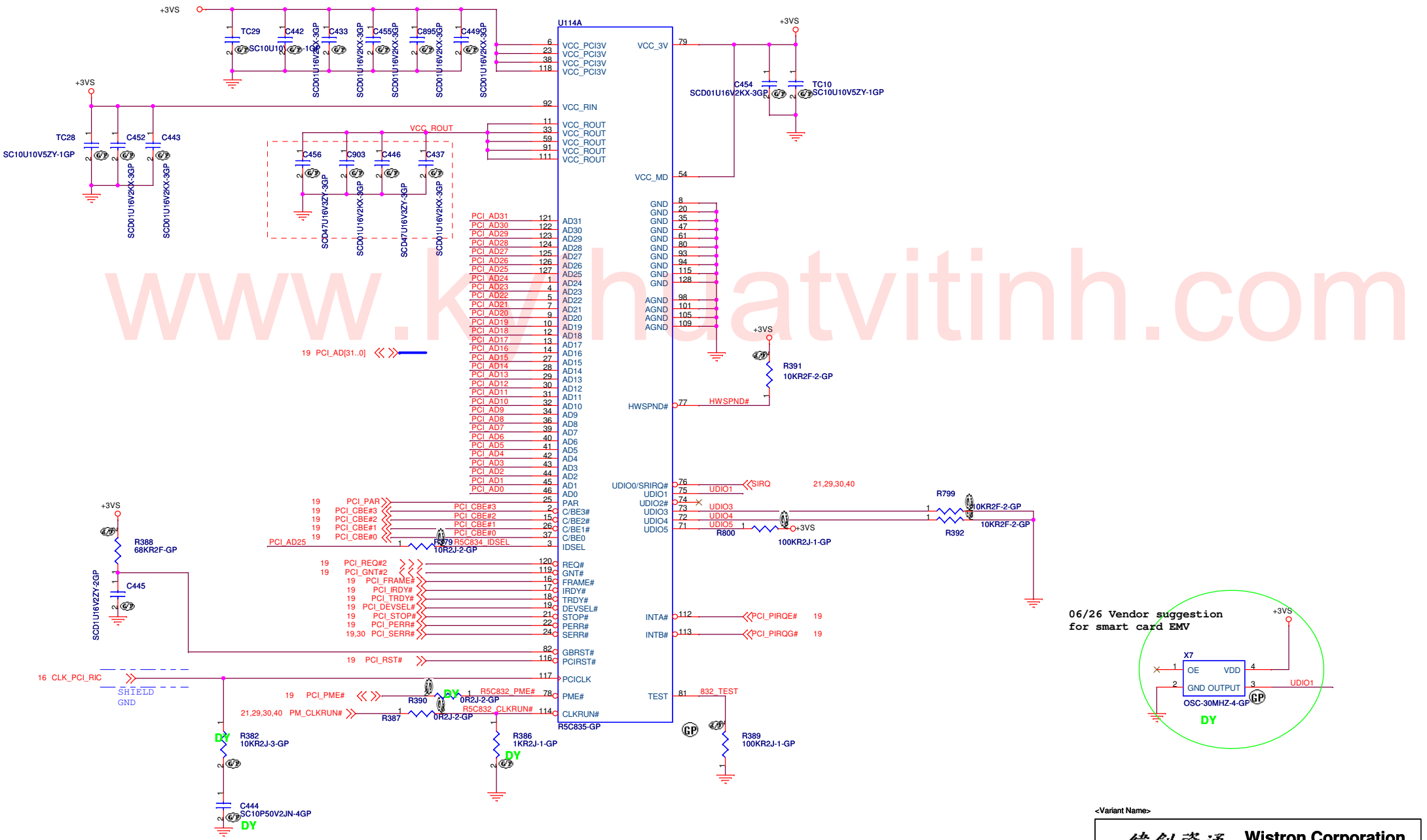
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Battery Selector

Size	Document Number	Rev
A2	KARIA - DISCRETE	SH

Date: Monday, May 19, 2008 Sheet 35 of 58



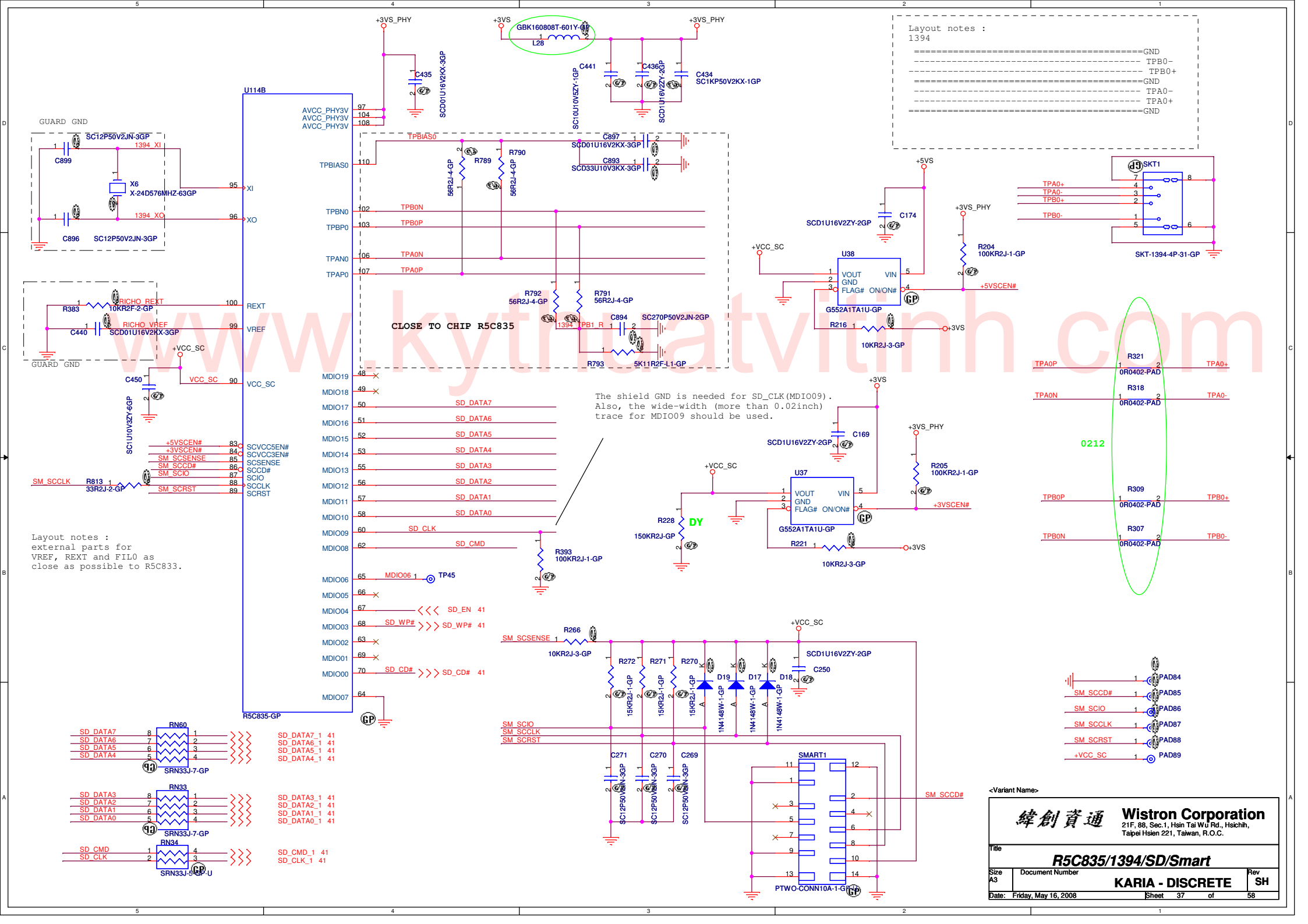
<Variant Name>

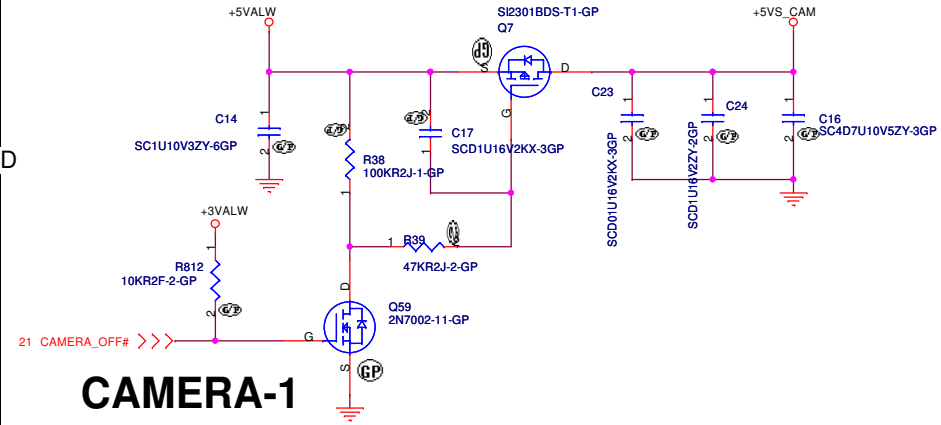
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

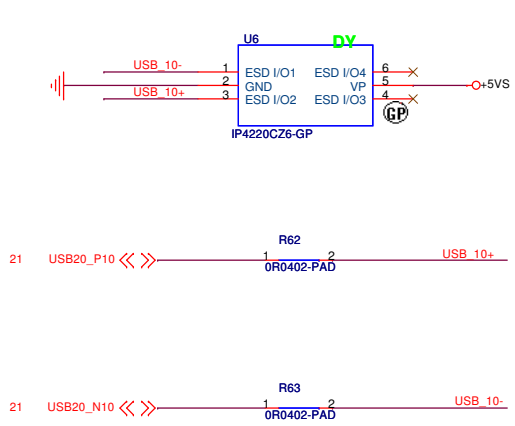
Title: R5C835/PCI

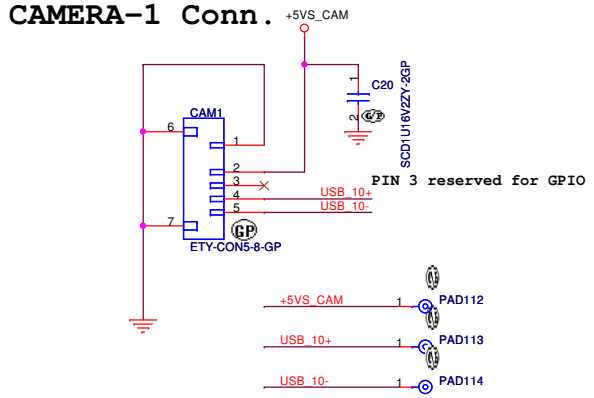
Size: A3 | Document Number: KARIA - DISCRETE | Rev: SH

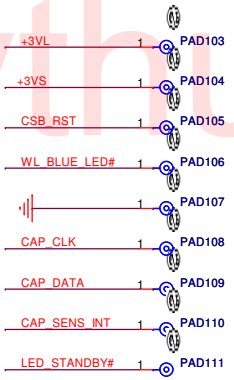
Date: Monday, May 19, 2008 | Sheet 36 of 58

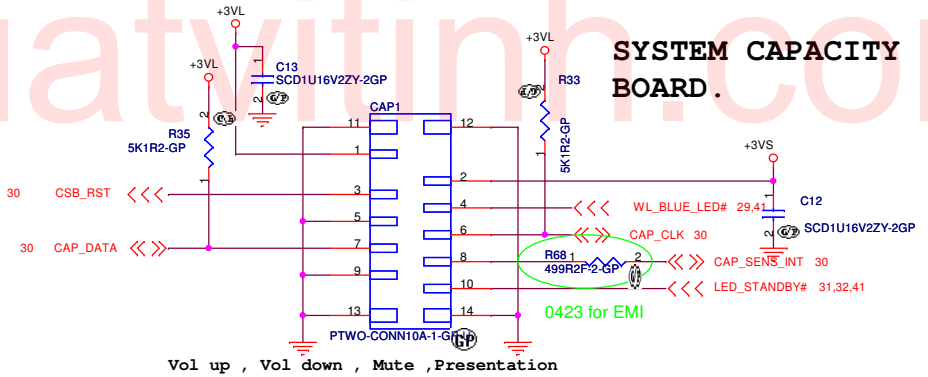

Layout notes :
1394
GND
TPB0-
TPB0+
GND
TPA0-
TPA0+
GND
U114B
R5C835-GP
CLOSE TO CHIP R5C835
The shield GND is needed for SD_CLK(MDIO09).
Also, the wide-width (more than 0.02inch)
trace for MDIO09 should be used.
Layout notes :
external parts for
VREF, REXT and FIL0 as
close as possible to R5C833.
SKT1
SKT-1394-4P-31-GP
G552A1TA1U-GP
SMART1
PTWO-CONN10A-1-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
R5C835/1394/SD/Smart
KARIA - DISCRETE
Date: Friday, May 16, 2008
Sheet 37 of 58



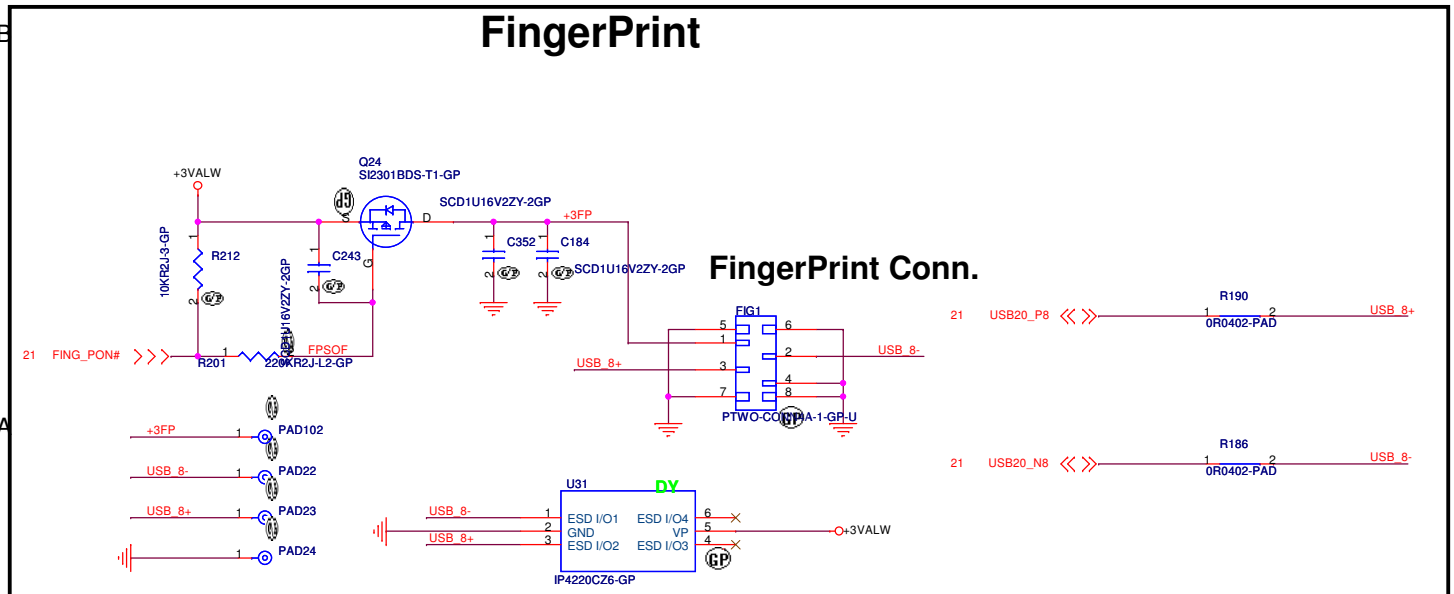


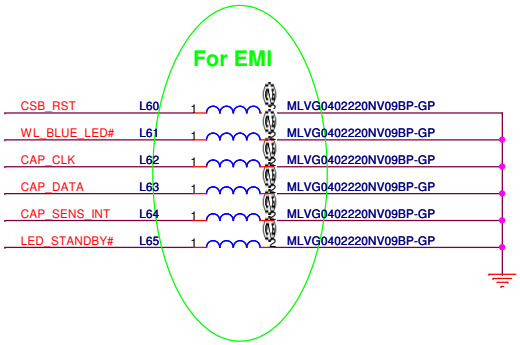






SYSTEM CAPACITY BOARD.





<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Camera/W-COM	
Size A3	Document Number KARIA - DISCRETE	Rev SH
Date: Friday, May 16, 2008	Sheet 38 of 58	

CPU TEMP:

H_THERMDA and H_THERMDC routing 10mil trace width and spacing. Locate Capacity near thermal diode

5 H_THERMDA — SC22P50V2JN-4GP C349 — H_THERMDA

CLOSE TO CPU

DY

5 H_THERMDC — H_THERMDC

55 GPU_TEMP+ — SC22P50V2JN-4GP C522 — GPU_TEMP+

DY

55 GPU_TEMP- — GPU_TEMP-

GPU DIE TEMP:
REMOTE2+ and REMOTE2- routing 10mil trace width and 10 mil spacing.

D1+ C788 1 — SC100P50V2JN-3GP — D1-

D2+ C782 1 — SC100P50V2JN-3GP — D2-

CLOSE TO BMC2103

R811 49D9R2F-GP — +3VS — SCD1U16V2KX-3GP C751

U106 EMC2103-2-AP-GP

VDD, DP1, DN1, DP2/DN3, ND2/DP3, SYS_SHDN#, ALERT#, SMCLK, SMDATA, GPIO1, GPIO2, TACH, PWM, TRIP_SET, SHDN_SEL, GND, GND

R206 10KR2J-3-GP — +3VS

H_THERMDA — R733 0R2J-2-GP — D1+
H_THERMDC — R732 0R2J-2-GP — D1-
GPU_TEMP+ — R719 0R2J-2-GP — D2+
GPU_TEMP- — R720 0R2J-2-GP — D2-

1017

SYS_SHDN#

21,55 THERM_SCI# — R686 — THERM_SCI# R — 0R2J-2-GP

21,24 ICH_SM_CLK
21,24 ICH_SM_DA

THERMTRIP#1 — TP67

FAN_TACH

0526 — R712 1K5R2F-2-GP

R710 — 15KR2F-GP — 0311

R729 10KR2J-3-GP — +3VS
R701 10KR2J-3-GP — +3VS

FAN_TACH 5
FAN_PWM 5

R848 0R2J-2-GP — PM_THRMTRIP-A# 5,9,20

R310 10KR2J-3-GP — DY — +3VS

Q70 RHU002N06-1-GP — DY

R268 10KR2J-3-GP — DY — +3VS

Q71 RHU002N06-1-GP — DY

SYS_SHDN#

G_TEMP_FAIL# — R850 0R2J-2-GP

Q58 2N7002TPT-GP

G_TEMP_FAIL 55

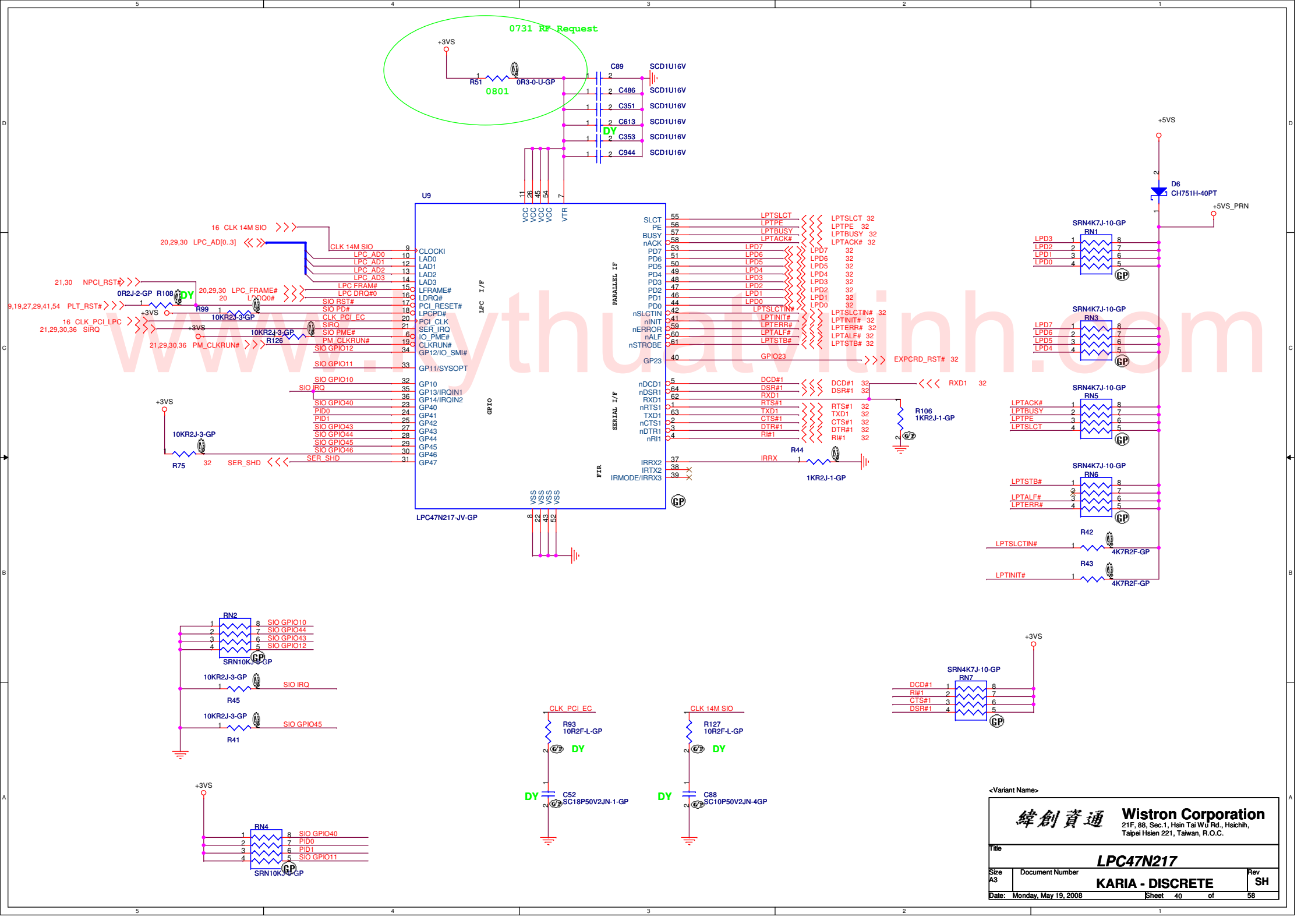
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

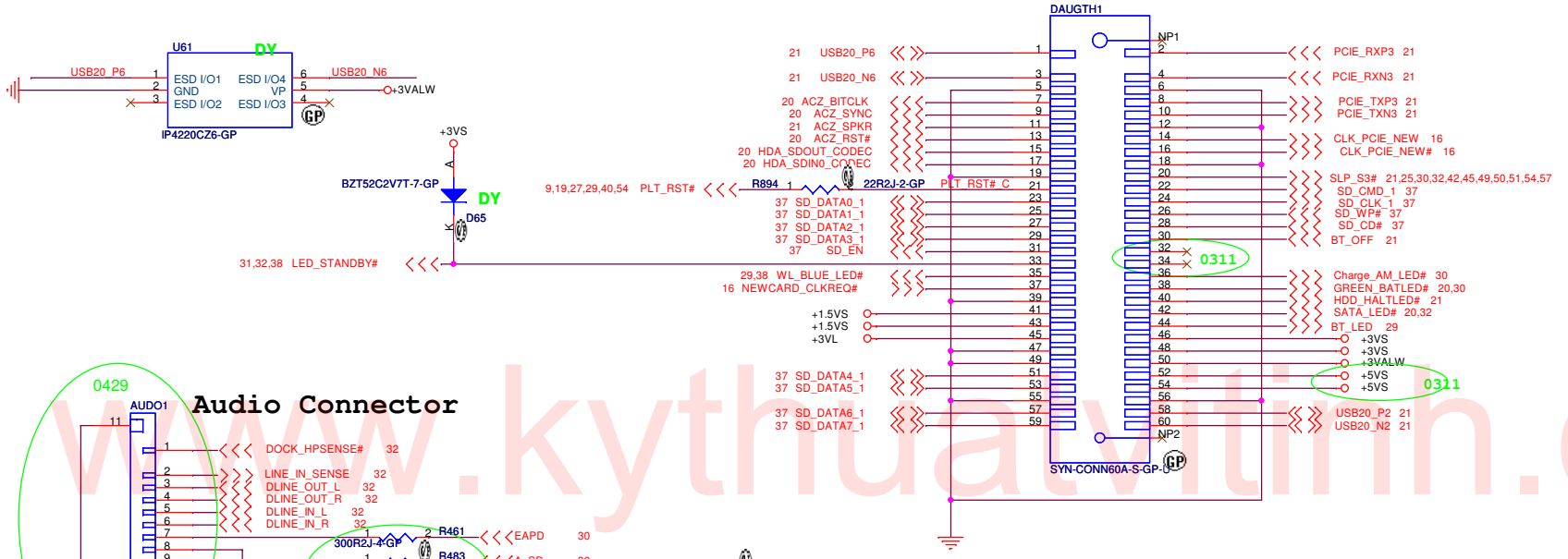
Title: ADT7473 Thermal Sensor

Size	Document Number	Rev
A3	KARIA - DISCRETE	SH

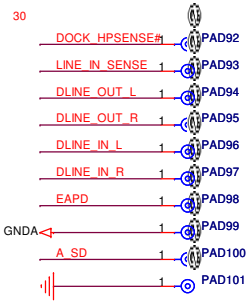
Date: Monday, May 26, 2008 Sheet 39 of 58

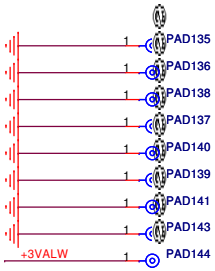


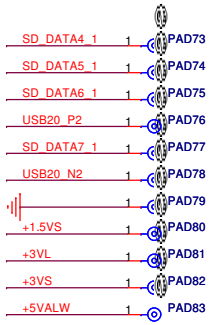
Daughter Board Connector

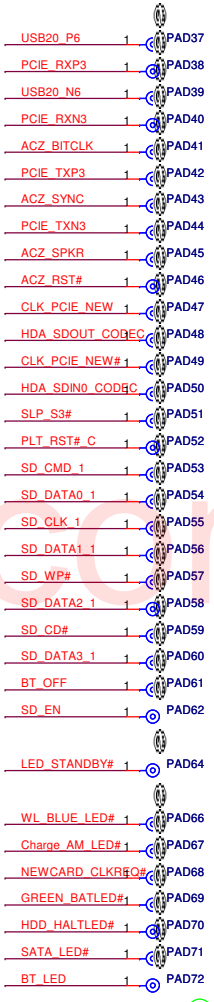


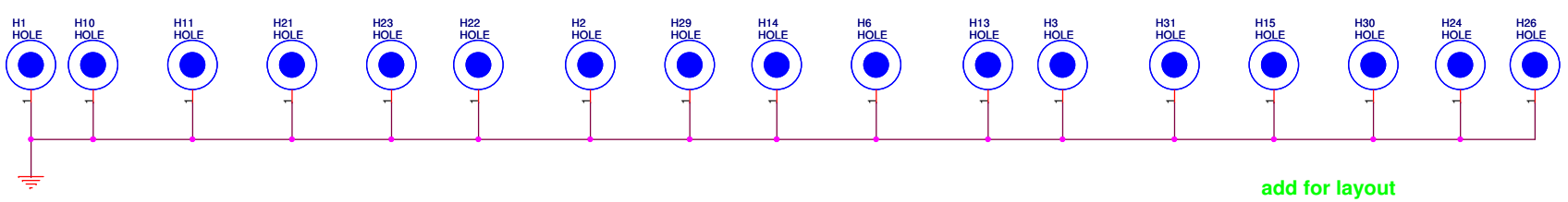
Audio Connector

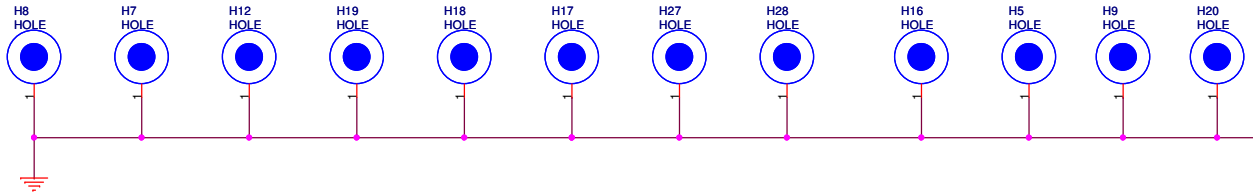


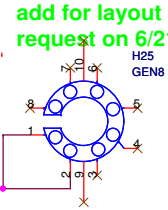


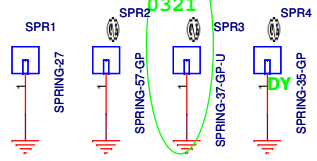












H10,H5 P/N: 34.4V908.001
H27,H28 P/N: 34.4V909.001
H9,H13 P/N:34.4V907.001
H21 P/N:34.4V910.001

add for layout request on 6/21

<Variant Name>

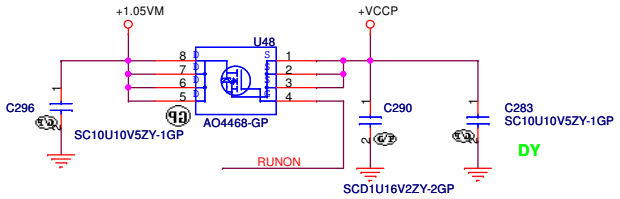
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDO/Daughter Connector

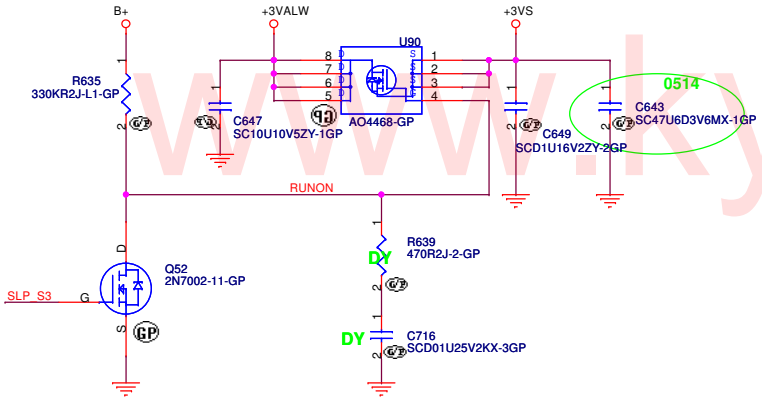
Size: A3 | Document Number: KARIA - DISCRETE | Rev: SH

Date: Friday, May 23, 2008 | Sheet 41 of 58

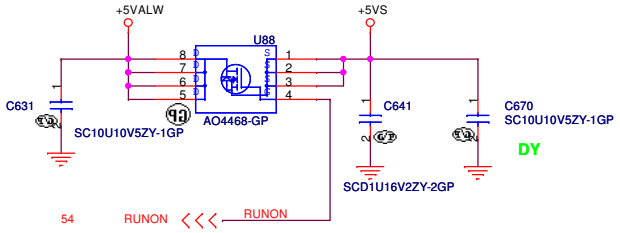
+1.05VM to +VCCP Transfer



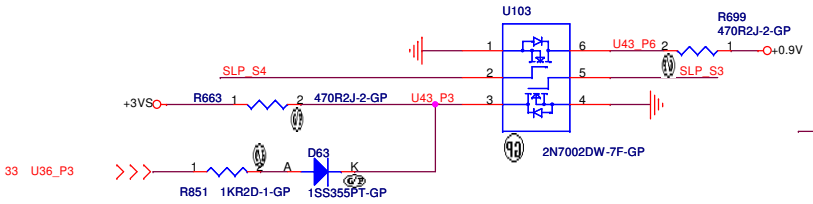
+3VALW to +3VS Transfer



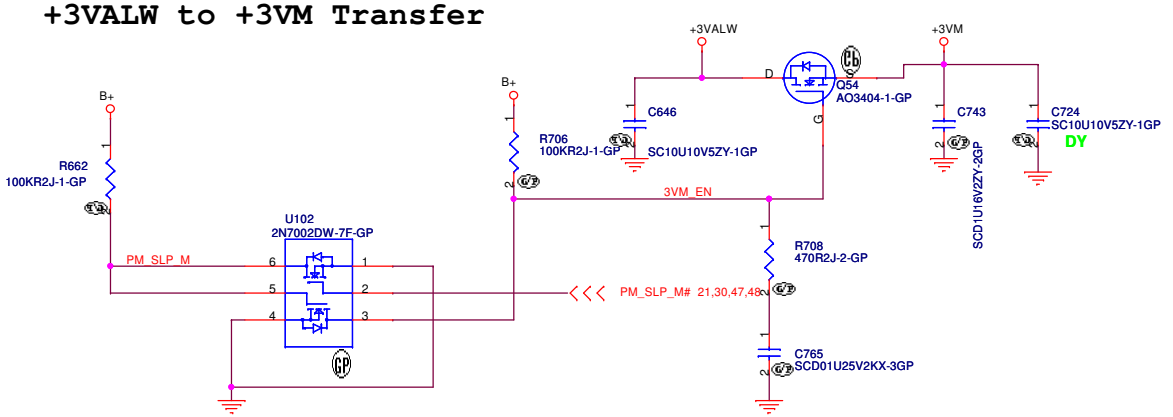
+5VALW to +5VS Transfer



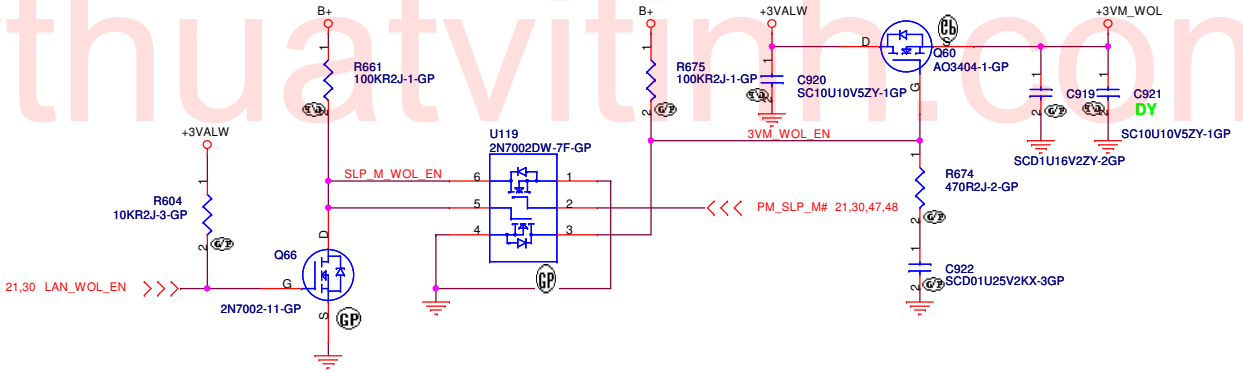
Discharge circuit-1



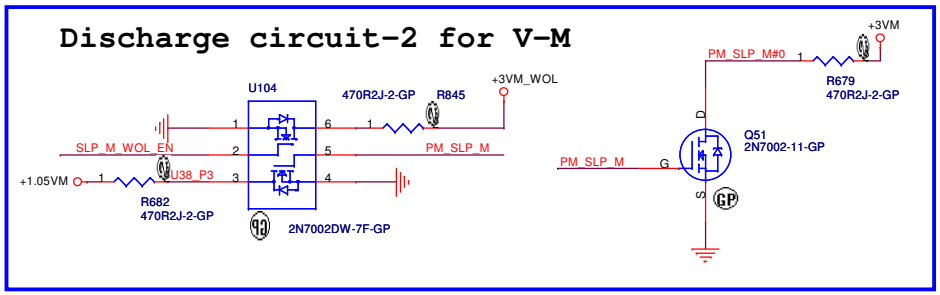
+3VALW to +3VM Transfer

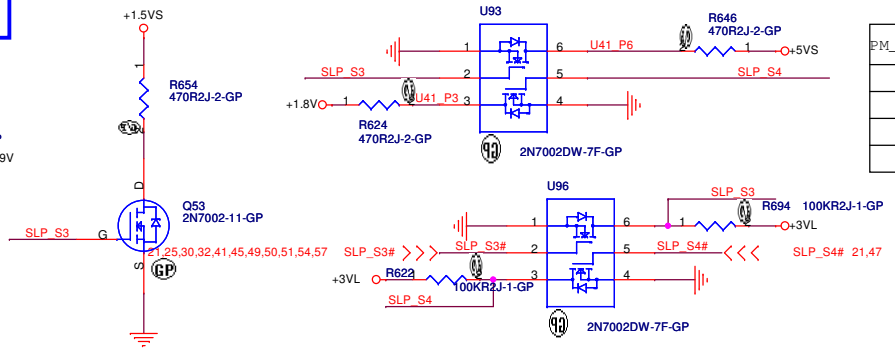


+3VALW to +3VM_WOL



Discharge circuit-2 for V-M





PM_SLP_M#	LAN_WOL_EN	+3VM_WOL	+3VM	SYSTEM STATE
0	0	0V	0V	Moff / No WOL
0	1	3.3V	0V	Legacy WOL/ Moff
1	0	3.3V	3.3V	M1
1	1	3.3V	3.3V	M1

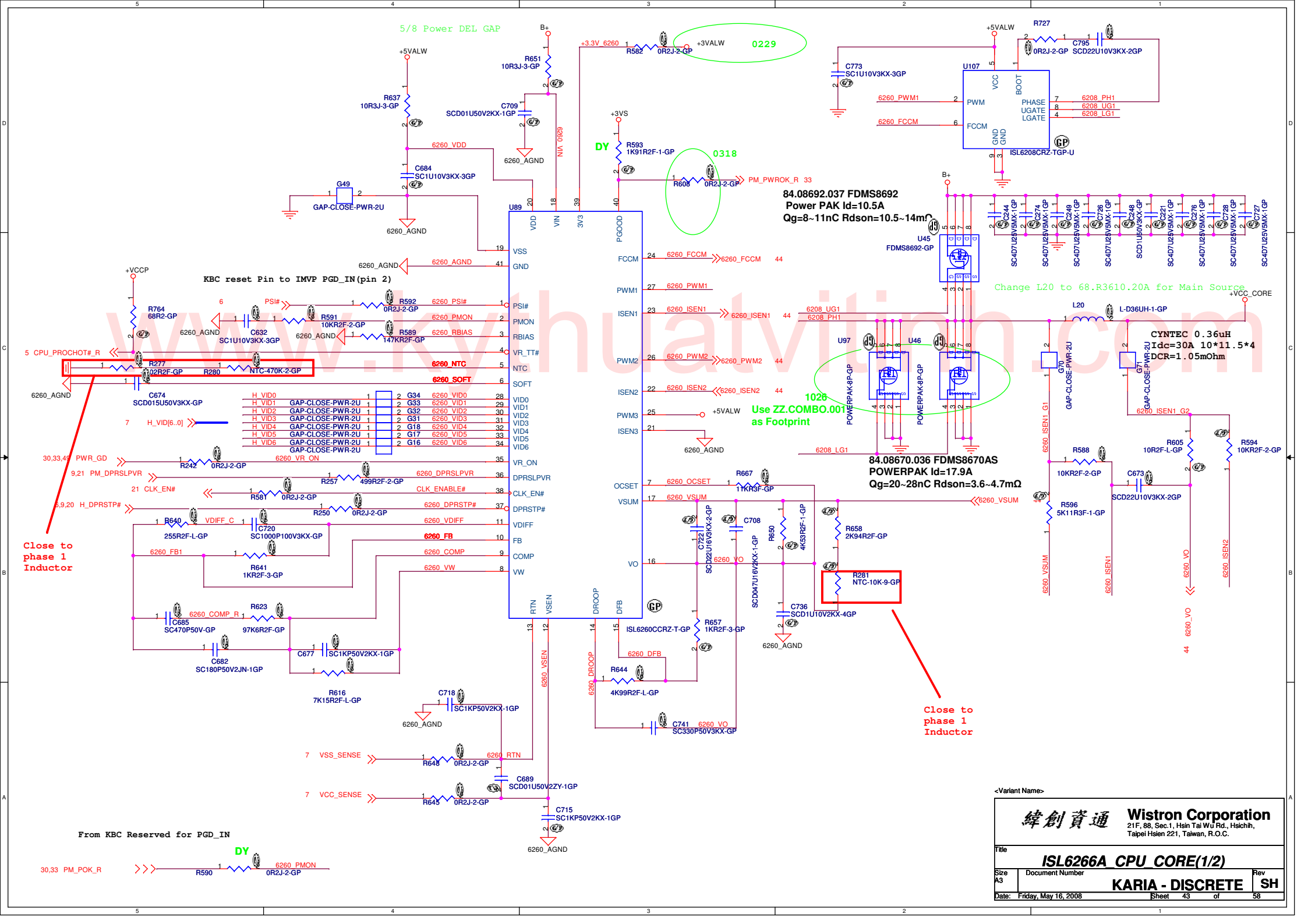
<Variant Name>

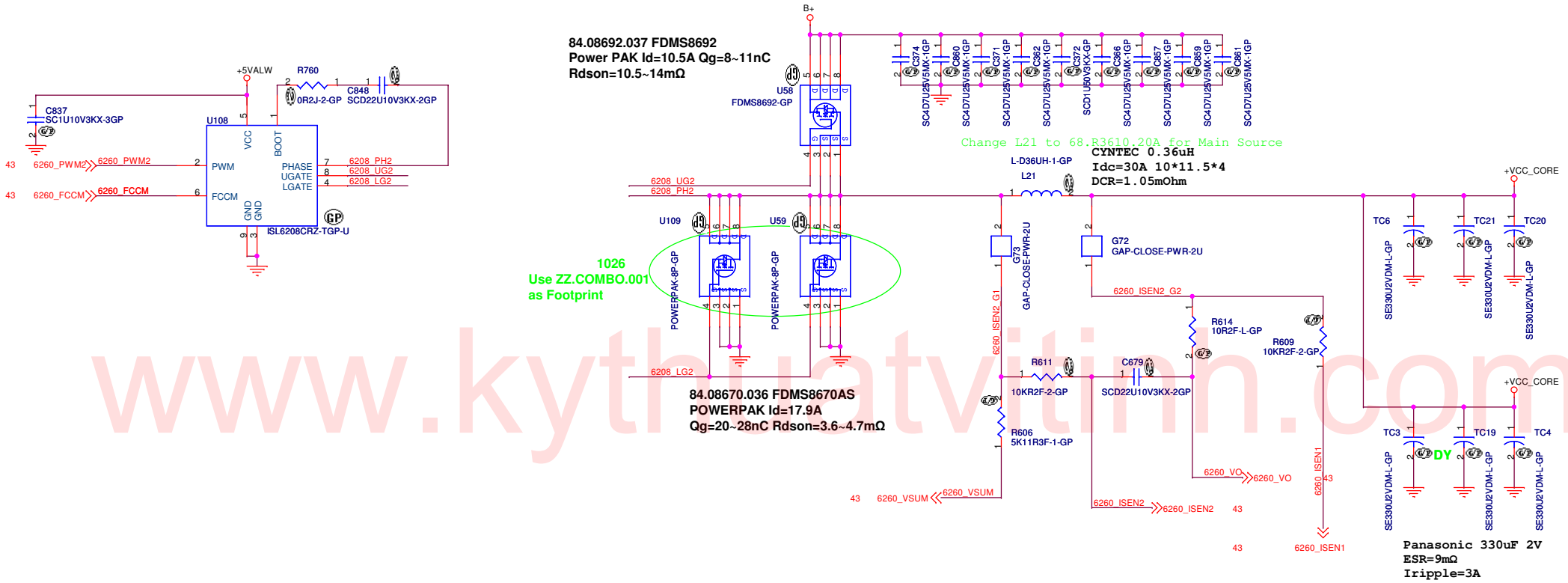
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC/DC Circuit

Size: A3 | Document Number: KARIA - DISCRETE | Rev: SH

Date: Friday, May 16, 2008 | Sheet 42 of 58


5/8 Power DEL GAP
KBC reset Pin to IMVP PGD_IN(pin 2)
Close to phase 1 Inductor
Close to phase 1 Inductor
From KBC Reserved for PGD_IN
84.08692.037 FDMS8692
Power PAK Id=10.5A
Qg=8~11nC Rdson=10.5~14mΩ
84.08670.036 FDMS8670AS
POWERPAK Id=17.9A
Qg=20~28nC Rdson=3.6~4.7mΩ
Use ZZ.COMBO.001 as Footprint
Change L20 to 68.R3610.20A for Main Source
CYNTEC 0.36uH
Idc=30A 10*11.5*4
DCR=1.05mOhm
ISL6266A_CPU_CORE(1/2)
KARIA - DISCRETE
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Friday, May 16, 2008
Sheet 43 of 58



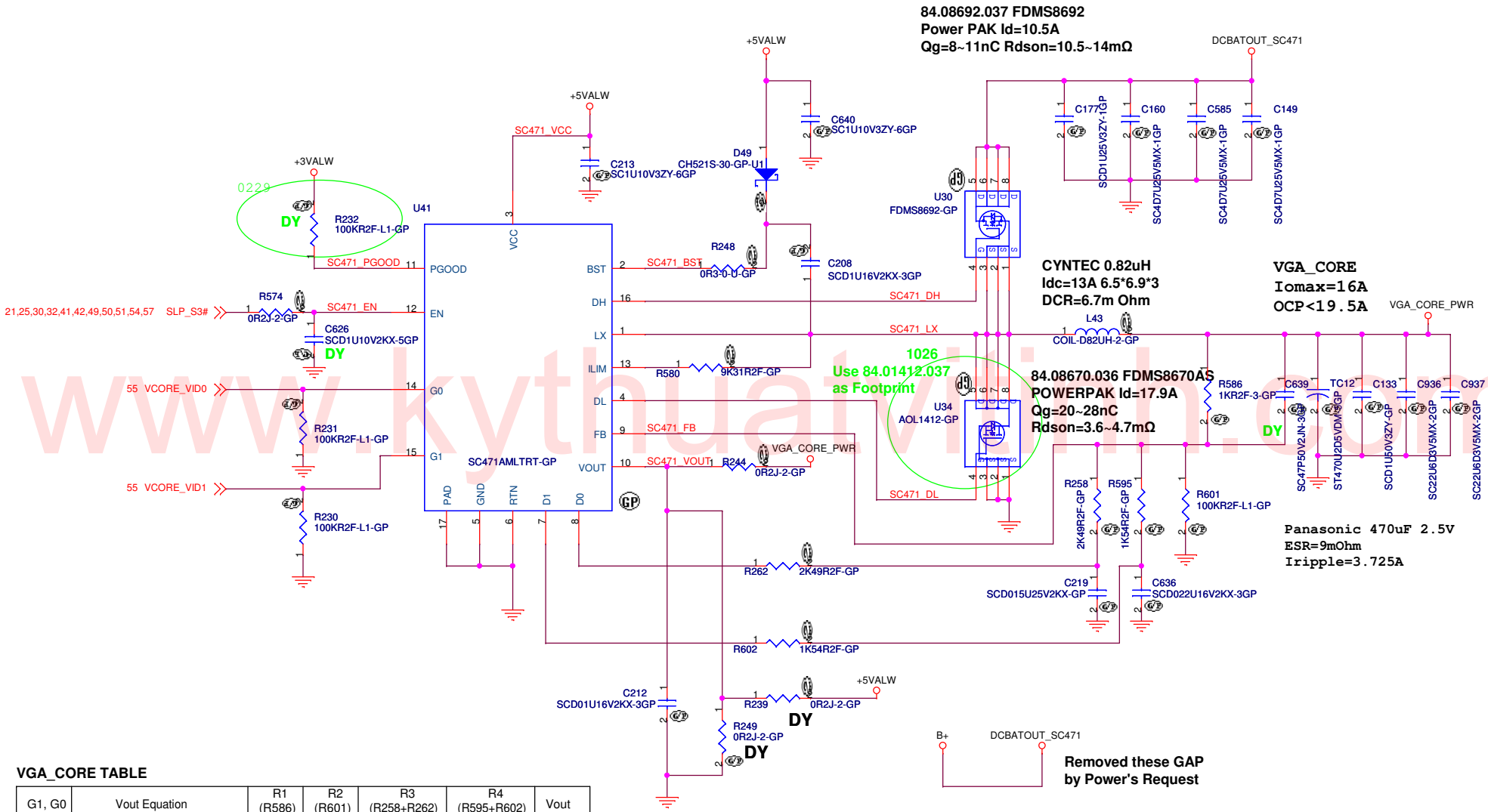
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL6266A_CPU_CORE(2/2)

Size: A3 | Document Number: KARIA - DISCRETE | Rev: SH

Date: Monday, May 19, 2008 | Sheet 44 of 58



VGA_CORE TABLE

G1, G0	Vout Equation	R1 (R586)	R2 (R601)	R3 (R258+R262)	R4 (R595+R602)	Vout
(0,0)	0.75*(1+R1/R2+R1/R3+R1/R4)	1K	100K	4.98K	3.82K	1.104V
(0,1)	0.75*(1+R1/R2+R1/R4)	1K	100K		3.08K	1.001V
(1,0)	0.75*(1+R1/R2+R1/R3)	1K	100K	4.98K		0.908V
(1,1)	0.75*(1+R1/R2)	1K	100K			0.758V

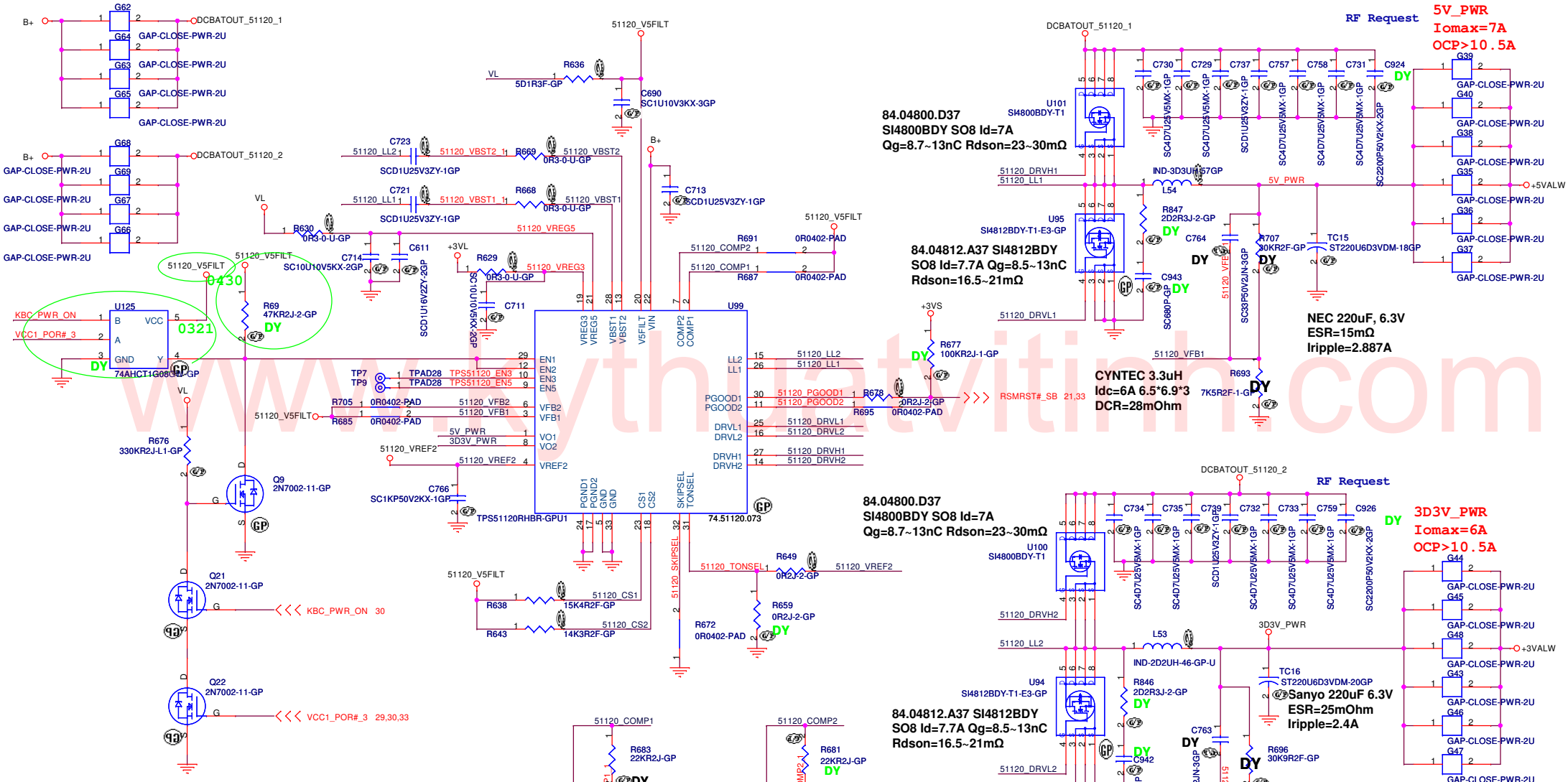
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **SC471A_VGA CORE**

Size: B | Document Number: **KARIA - DISCRETE** | Rev: SH

Date: Friday, May 16, 2008 | Sheet 45 of 58



	GND	VREF2	FLOAT	V5FILT
SKIPSEL	**AUTOSKIP**	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	**D-Cap MODE**
TONSEL	380k/CH1 580k/CH2	280k/CH1 430k/CH2	**220k/CH1 330k/CH2**	180k/CH1 280k/CH2
VFB1	Adjustable output (connect to the resistor divider)			**5V Fixed Output**
VFB2				**3.3V Fixed Output**
EN1,EN2	Switcher OFF		**Swithchr ON**	**Switcher ON**
EN3,EN5	LDO OFF	not use	**LDO ON**	VREG3 on (EN3 only)

For TPS51120,
Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.

Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

<Variant Name>

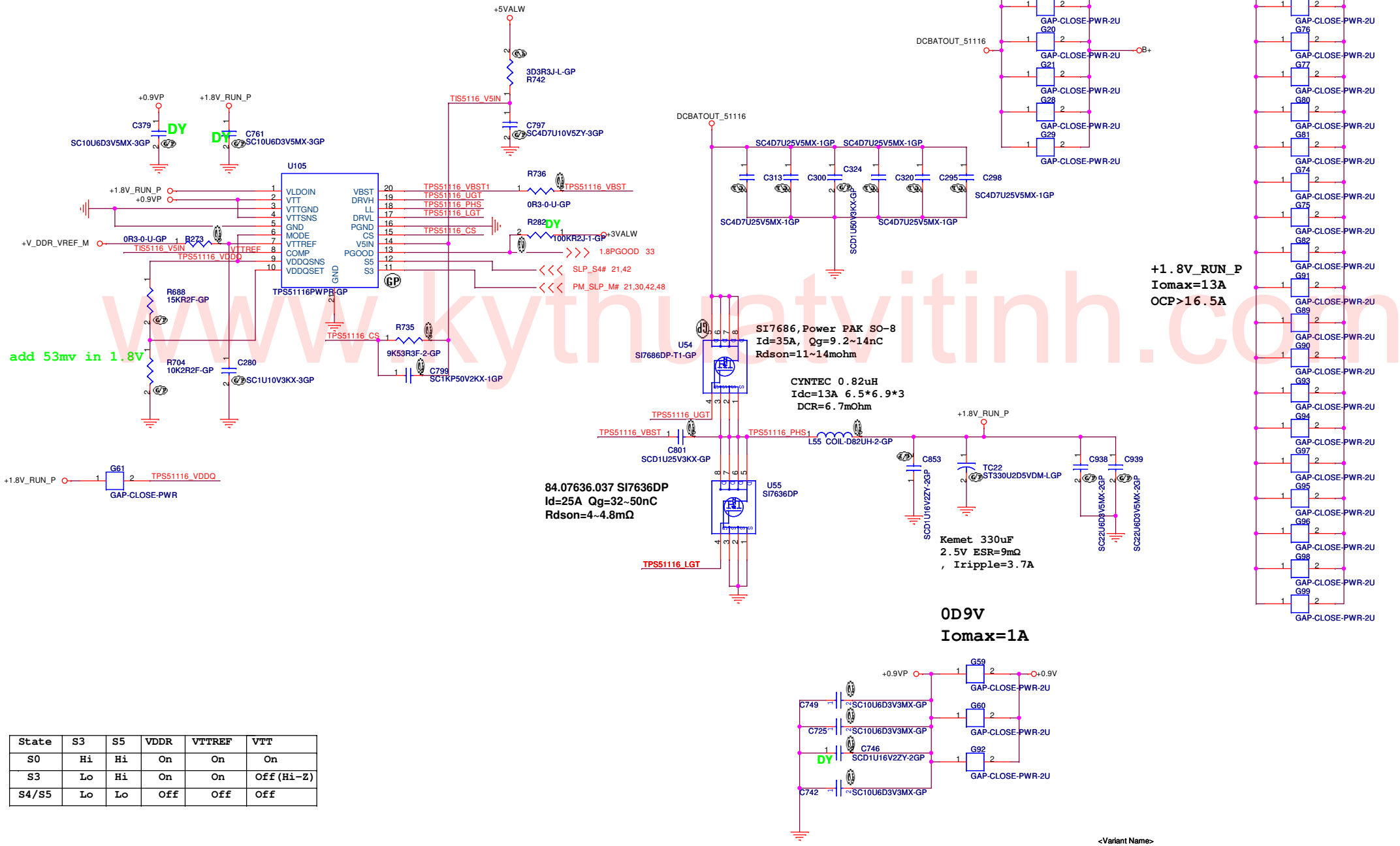
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPA51120 +5VALW +3VALW

Size: A3 | Document Number: KARIA - DISCRETE | Rev: SH

Date: Tuesday, May 20, 2008 | Sheet 46 of 58

TI TPS51116 for 1D8V and 0D9V



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

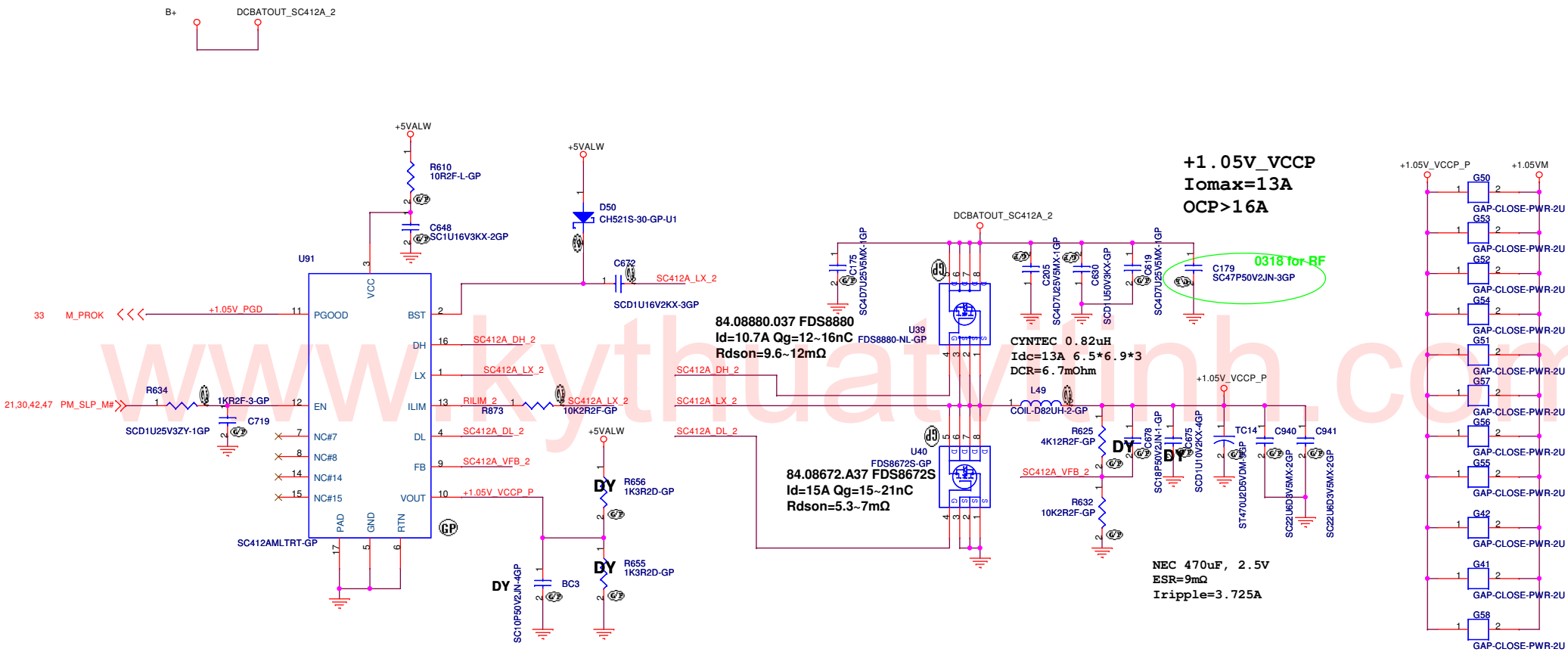
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51116 1D8V/0D9V

Size: A3 | Document Number: KARIA - DISCRETE | Rev: SH

Date: Friday, May 16, 2008 | Sheet 47 of 58



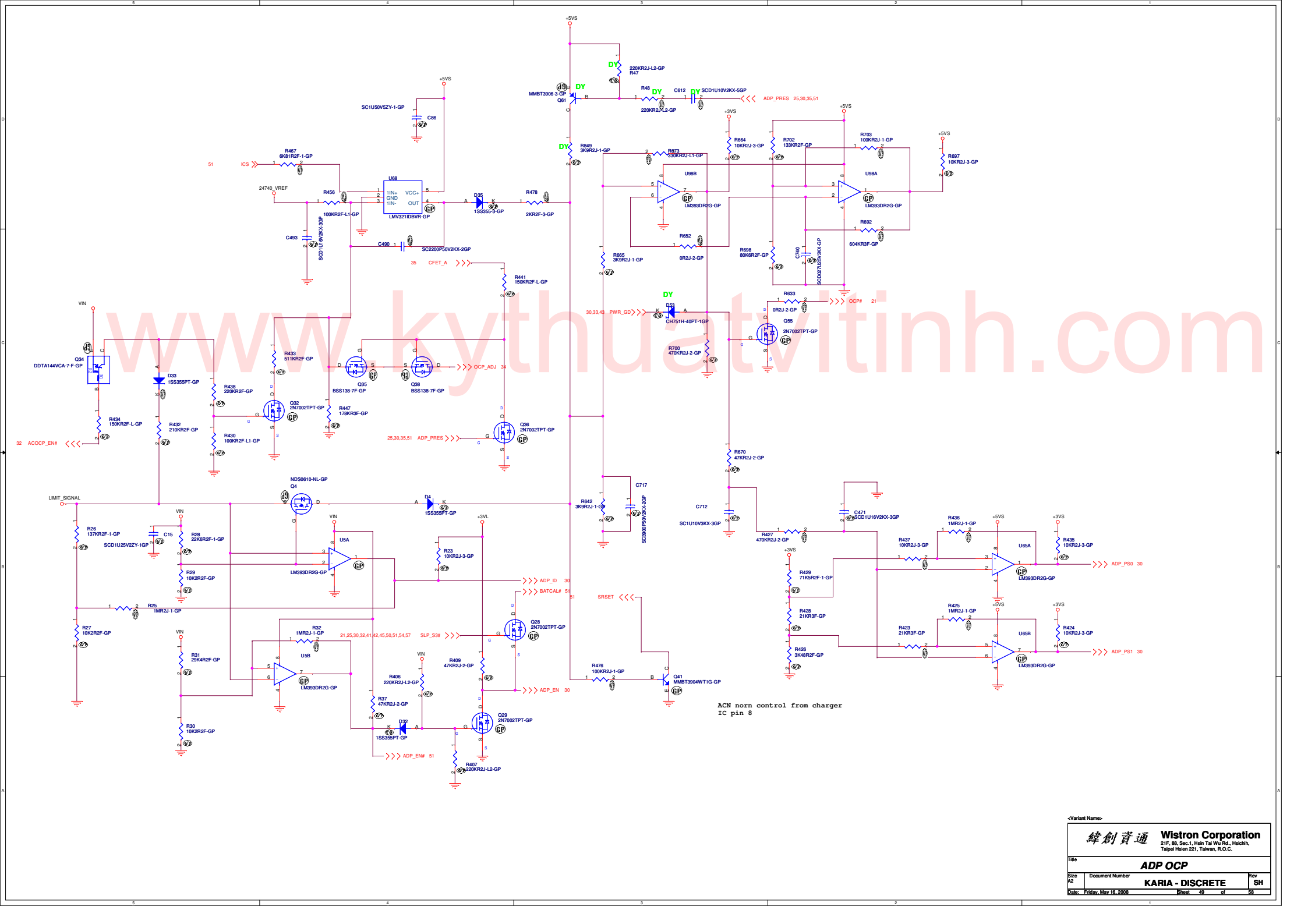
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SC412A +1.05VM

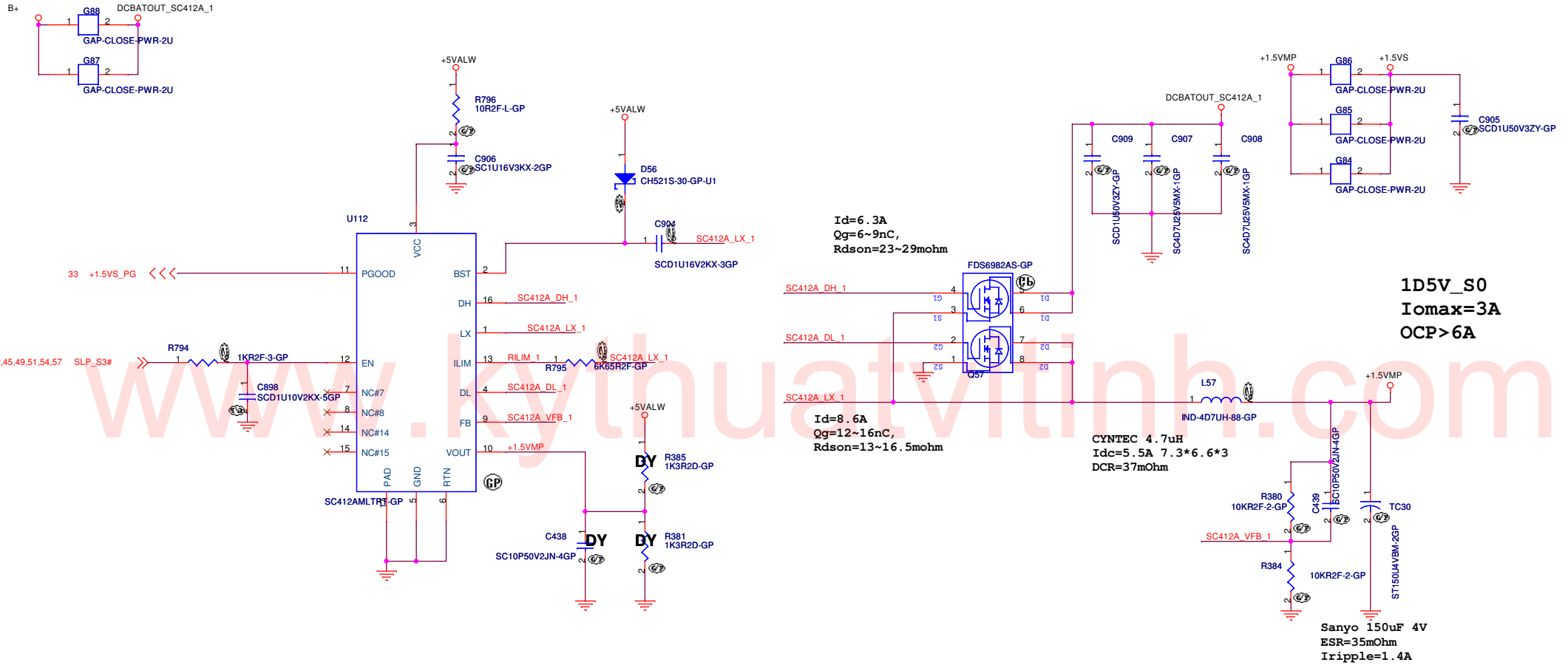
Size: A3 | Document Number: KARIA - DISCRETE | Rev: SH

Date: Friday, May 16, 2008 | Sheet 48 of 58



<Variant Name>

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	ADP OCP
Size: A2	Document Number: KARIA - DISCRETE
Rev	SH
Date: Friday, May 16, 2008	Sheet 49 of 58



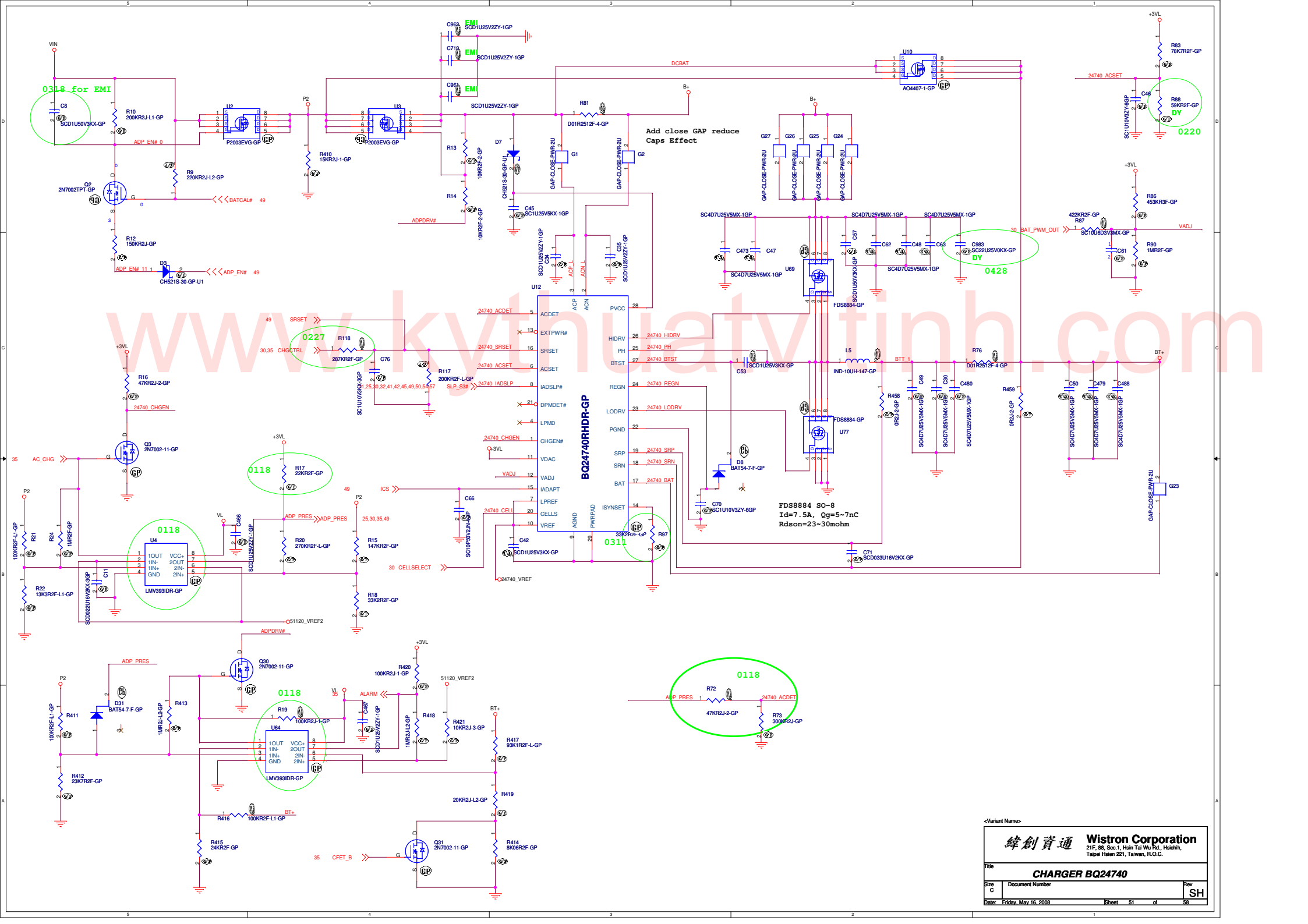
<Variant Name>

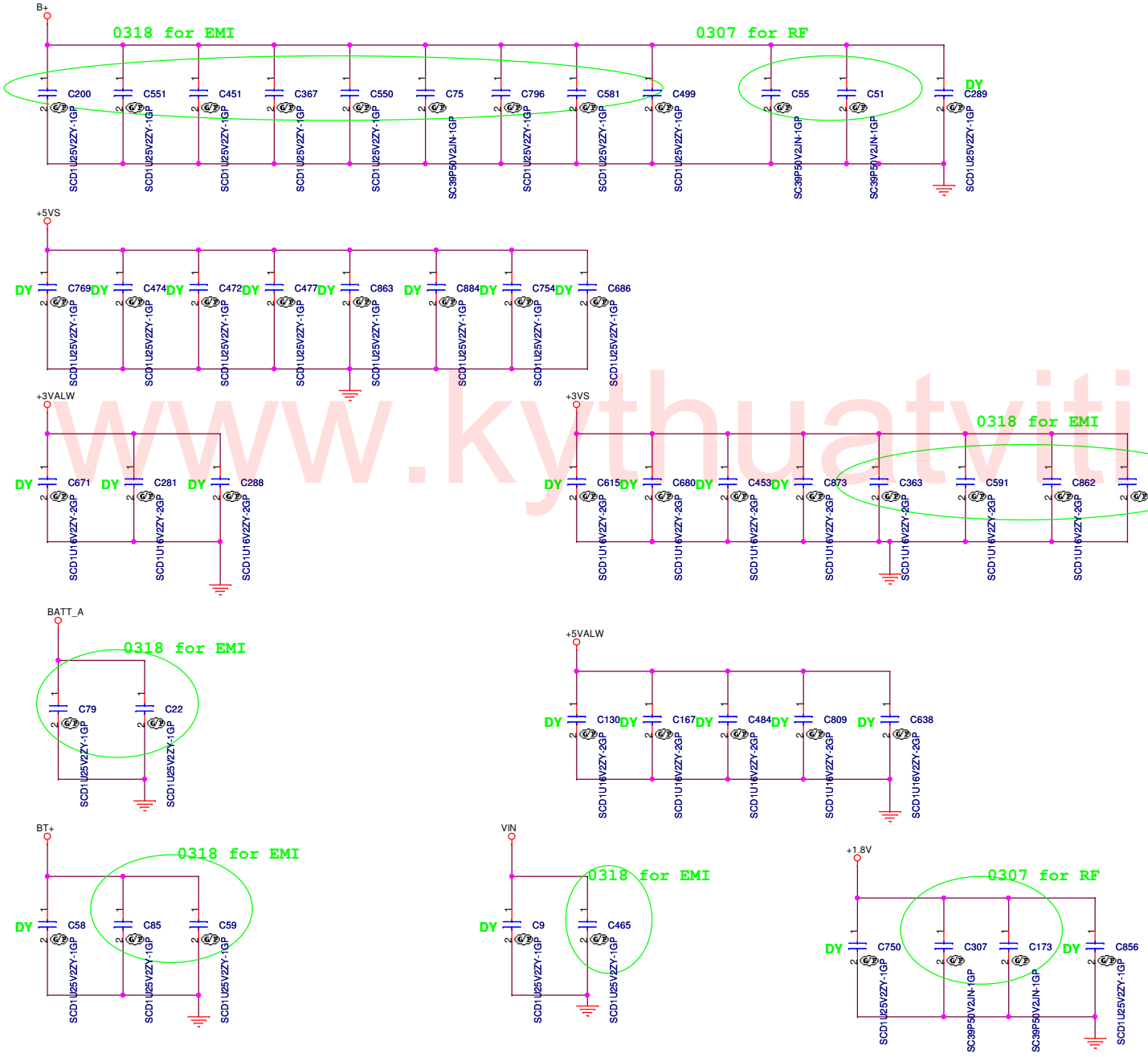
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SC412A_+1.5VS

Size: A3 | Document Number: KARIA - DISCRETE | Rev: SH

Date: Friday, May 16, 2008 | Sheet 50 of 58





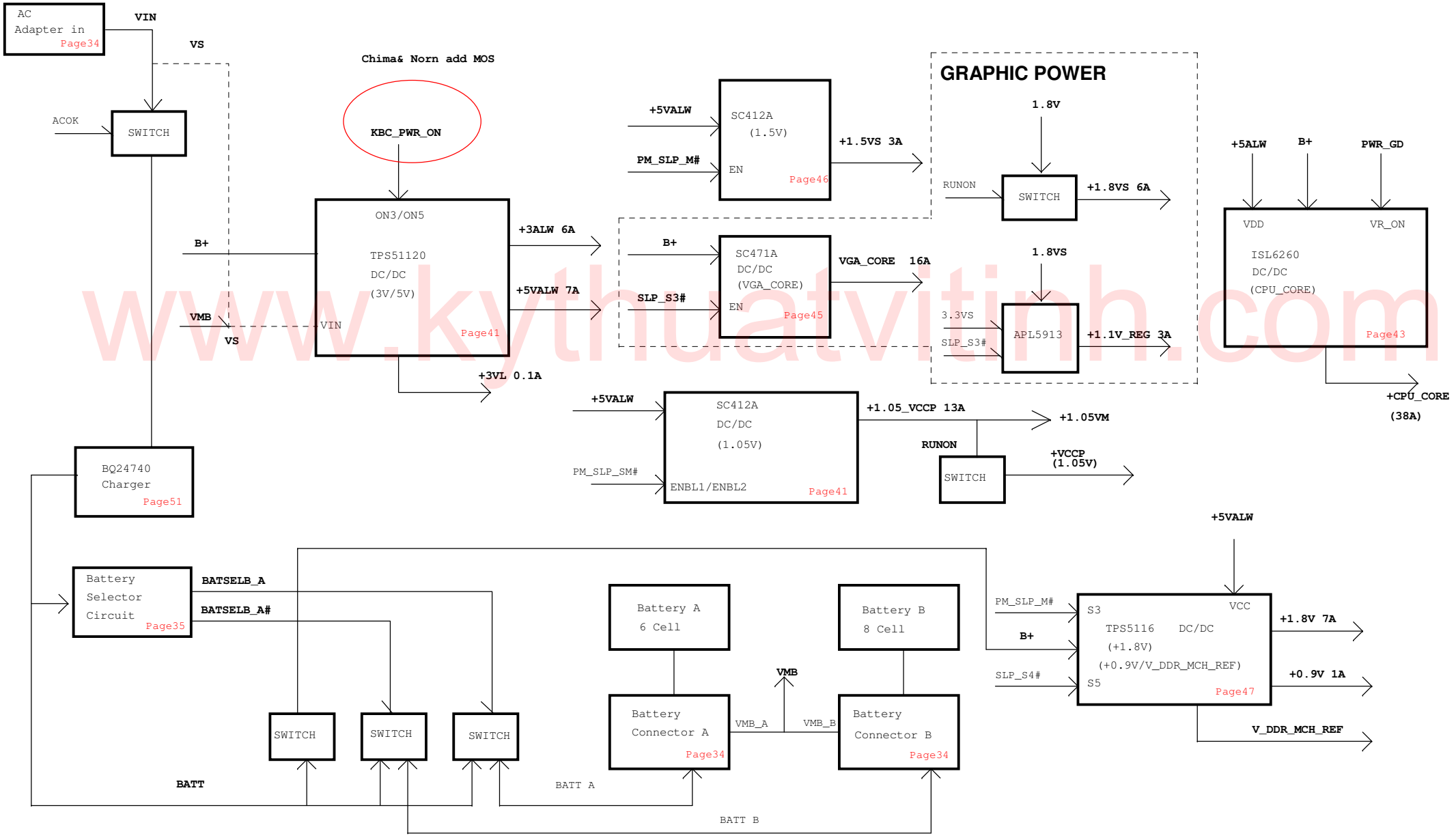
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***EMI CAPS***

Size	Document Number	Rev
A3		SH

Date: Friday, May 16, 2008 Sheet 52 of 58



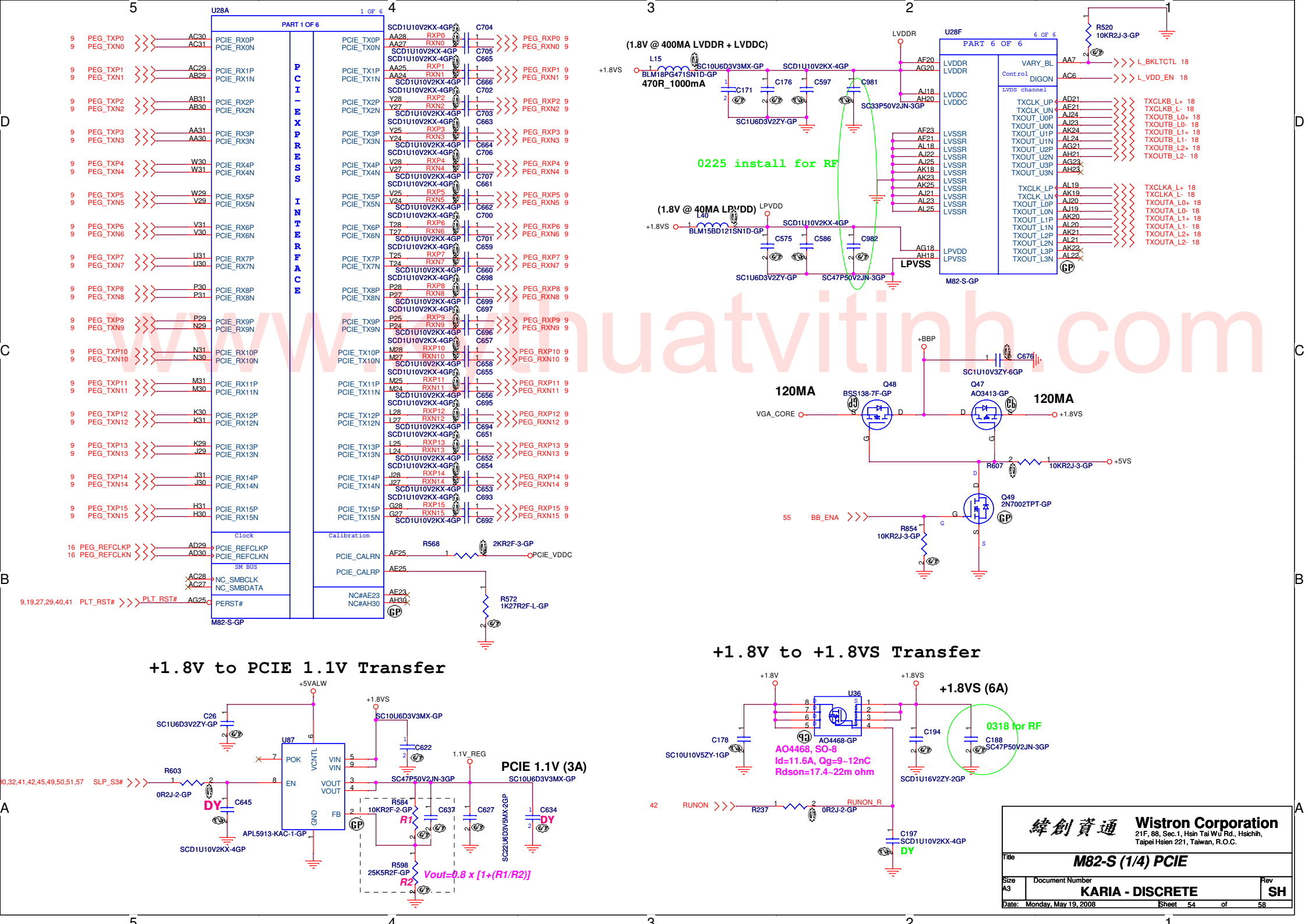
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Block Diagram

Size	Document Number	Rev
A3	KARIA - DISCRETE	SH

Date: Friday, May 16, 2008 Sheet 53 of 58



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

0 = DON'T INSTALL RES
1 = INSTALL 10K RES
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	M82-SCE
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	1
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS MUXED OUT	0
BIF_AUDIO_EN	GPIO8	ENABLE HD AUDIO (M8x)	1
BIF_GEN2_EN_A	GPIO5	ALLOW EITHER PCIE 2.5GT/s OR 5GT/s OPERATION	1
ROM ID CFG(3:0)	GPIO[13:11,9]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	X X X X
BIOS_ROM_EN	GPIO_22_ROMCSB	DISABLE EXTERNAL BIOS ROM	NA
VIP_DEVICE_STRAP_ENA	VSYNC	IGNORE VIP DEVICE STRAPS	0
BIF_VGA DIS	PSYNC	VGA ENABLED	0
BIF_HDMI_EN	HSYNC	HDMI ENABLE	1

VRID_[3..0]

GDDR3 64bit 0 0 0 0 / 0 1 0 1 / 1 0

00 -->8M*32
01 -->16M*32
10 -->32M*32

00 -->Qimonda
01 -->Samsung

VRAM Configuration	Install Resistors
Samsung 16x32MB	R134, R125, R119, R114 <-- Default
Samsung 32x32MB	R131, R121, R119, R114
Qimonda 16x32MB	R134, R125, R119, R113
Qimonda 32x32MB	R131, R121, R119, R113

VRAM ID

Aperture Config PIN	M82SCE GPIO	Strapping Resistor	64MB VRAM	128MB VRAM	256MB VRAM
CONFIG 0	GPIO_11	R597	0	0	1
CONFIG 1	GPIO_12	R831	1	0	0
CONFIG 2	GPIO_13	R832	0	0	0
CONFIG 3	GPIO_9	TP88	X	X	X

U28B PART 2 OF 6 (2 OF 6)

INTEGRATED TMDS/DP PORT

EXT TMDS DVO

DAC1 / CRT

DAC2 (TV/CRT2)

GENERAL PURPOSE I/O

SERIAL BUSES

PLL & XTAL

THERMAL

TEST

M82-S-GP

PLACE THESE CAPACITOR CLOSE TO CONNECTOR

PLACE THESE RESISTORS CLOSE TO DIFF. PAIRS AND AVOID STUBS TO ALL DIFF. TRACES.

MINIMIZE THE DISTANCE BETWEEN THESE RES. AND 100nF AC CAPS

(1.1V @ 400MA TPVDD)

CLOSE TO CONNECTOR

12MILS TO OTHER TRACE

5MILS TO EACH OTHER

Route RB, GB and BB as differential complement of R, G, and B signals to VGA connector and docking connector

CLOSE TO GPU

(1.8V @ 20MA TPVDD EACH)

(1.8V @ 65MA AVDD)

(1.8V @ 100MA VDD1DI,VDD2DI)

(3.3V @ 135MA A2VDD)

(1.8V @ 2MA A2VDDQ)

3.3V TO 5V LEVEL SHIFT LOGIC REQUIRED:
M82-S: DDC1 & 2 (DDC3 & 4 ARE 5V TOLERATNCE)

CRT

ICH

DVI

LVDS

Un-install to disable HD-Audio function

VREFG = VDDR4.5(1.8V) / 3=0.6V
PLACE VREF DIVIDER AND CAP CLOSE TO ASIC

VOLTAGE DIVIDER TO MAKE XTALIN VOLTAGE LEVEL OF 1.8V

3.3V => 147 ohm

PULLUP POWER RAIL MUST BE UP BEFORE CORE POWER RAIL

(1.8V @ 40MA DPLL_PVDD)

(1.8V @ 40MA PCIE_PVDD)

120 OHM 450MA

(.95V-1.1V @ 230MA MPVDD)

(DPLL_VDDC 1.1V @ 100 MA)

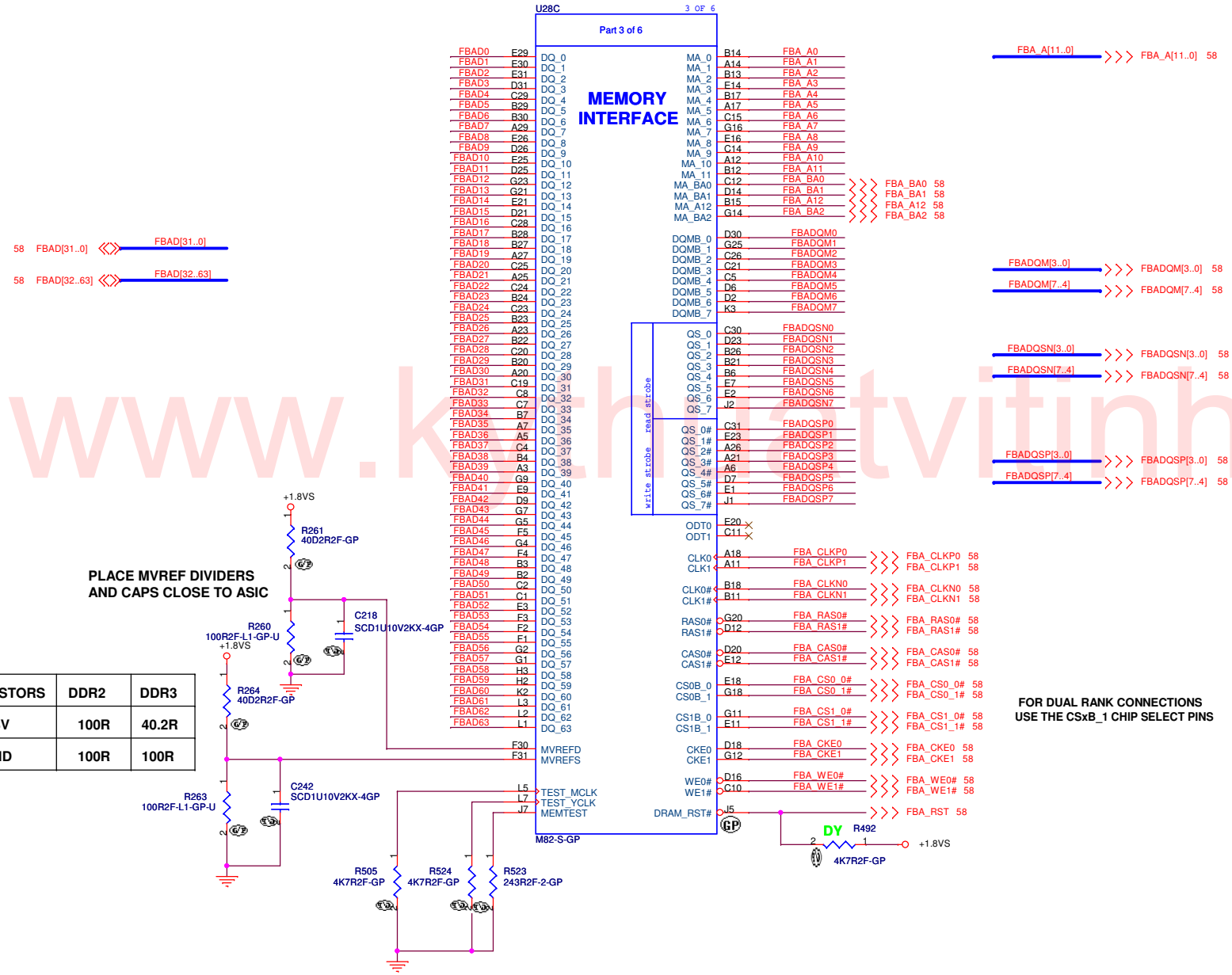
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: M82-S (2/4) I/O

Size: Custom | Document Number: KARIA - DISCRETE | Rev: SH

Date: Monday, May 19, 2008 | Sheet 55 of 58



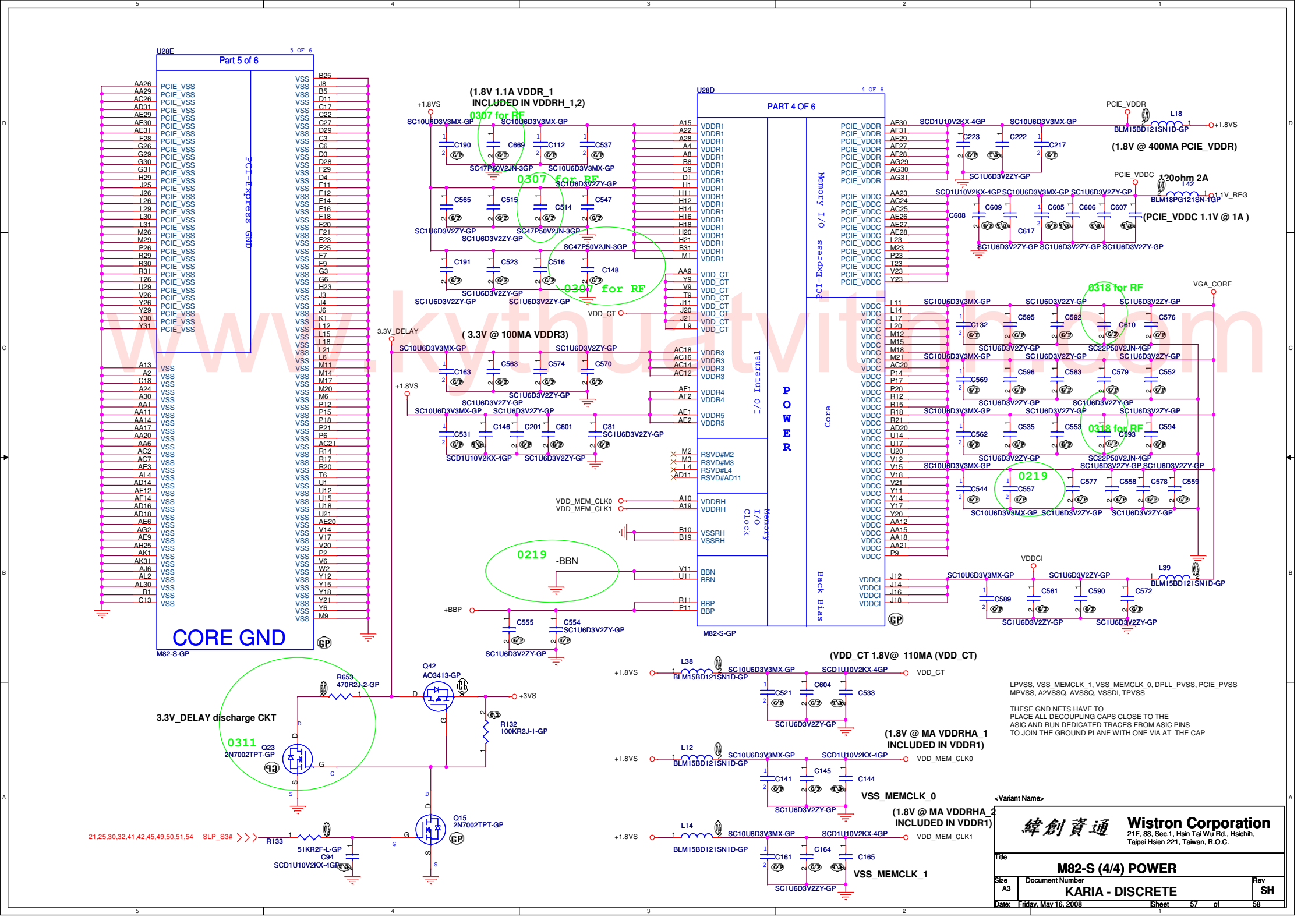
<Variant Name>

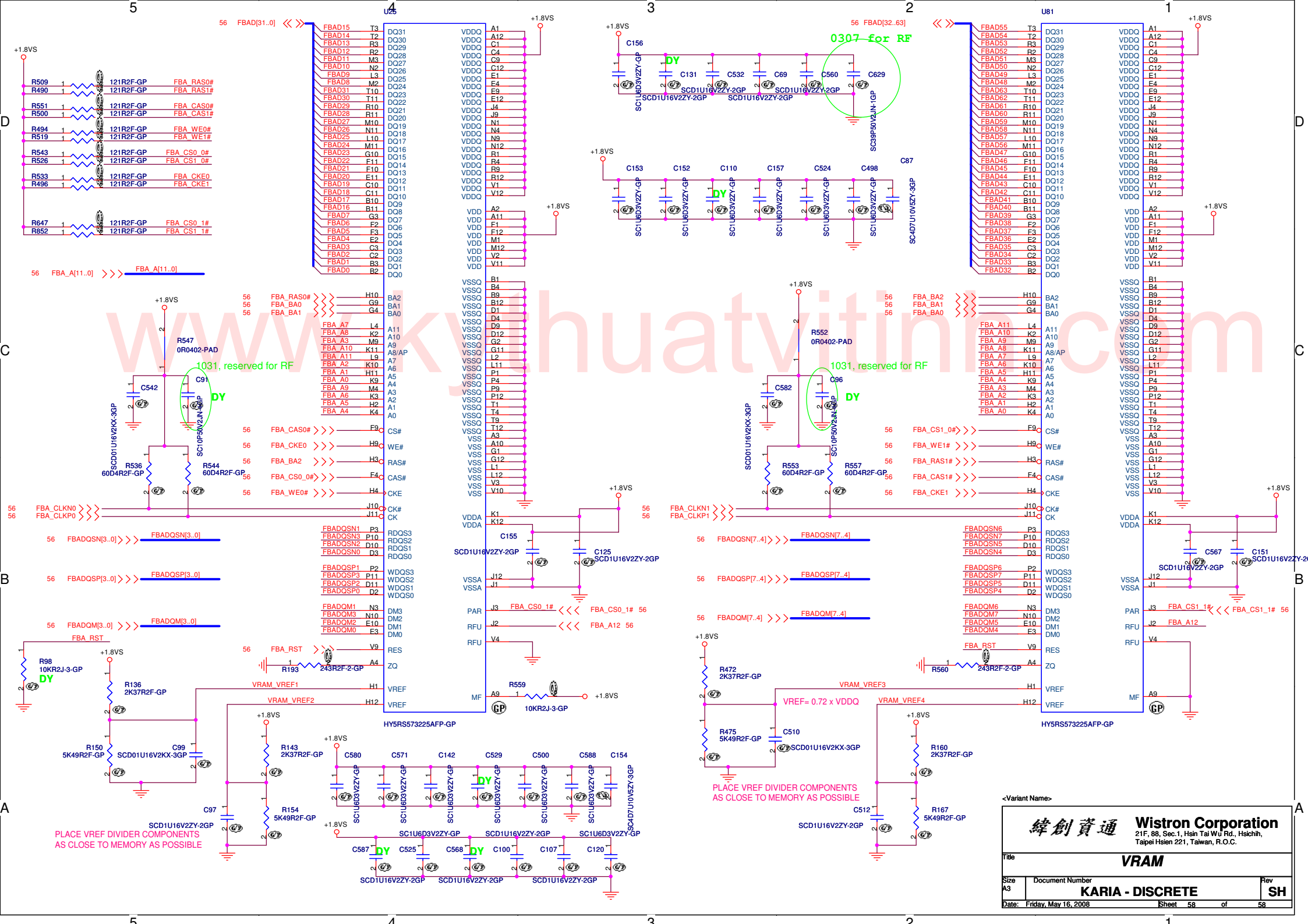
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: M82-S (3/4) VRAM Interface

Size: A3 | Document Number: KARIA - DISCRETE | Rev: SH

Date: Friday, May 16, 2008 | Sheet 56 of 58




U25
U81
HY5RS573225AFP-GP
0307 for RF
1031, reserved for RF
PLACE VREF DIVIDER COMPONENTS AS CLOSE TO MEMORY AS POSSIBLE
VREF= 0.72 x VDDQ
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
VRAM
Size A3
Document Number
KARIA - DISCRETE
Rev SH
Date: Friday, May 16, 2008
Sheet 58 of 58