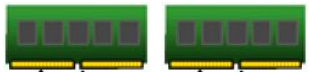
Compal Confidential

Model Name : Z5WAK



VRAM 1G/2G
64M16/128M16 x 8
page 23, 24

DDR3

AMD JET/OPAL
128Bit DDR3
uFCBGA-962
Page 13~19

PCIe x 8 Gen3

AMD Kaveri

AMD FP3 APU
Kaveri
Package
Page 5~10

Memory BUS
(DDR3/DDR3L)
Dual Channel

1.5V DDR3/DDR3L
fequence support :800~2133MHz

204pin DDRIII-SO-DIMM X2
BANK 0, 1, 2, 3
Page 11,12

APU HDMI
(UMA / Muxless)

DP2

DP1

DP0

P_GPP x 3
GEN2

DP x 4
(DP1 TXP/N 0~4)
ML for FCH VGA

UMI

HDMI Conn.
page 27

eDP Panel
page 25

UMA eDP

CRT Conn.
page 26

FCH CRT (VGA DAC)

FCH
BOLTON - M3

uFCBGA-656
Page 20~24

USB3.0
Port 0

USB30
M/B*1
page 36

USB20
Sub/B*2
page 36

CMOS
Camera
page 25

Touch
screen
page 25

Mini
Card 1
page 28

TP
Bridge
page 29

USB3.0

USB2.0
3.3V 48MHz

Port 0
Port 1

USB2.0
Port10

Port 2

Port 3

Port 4

Port 5

HD Audio 3.3V 24.576MHz/48Mhz

SATA Gen3

GPP0

GPP1

LAN(GbE)
Realtek
RTL8411B page 29

MINI Card 1
(Wireless LAN)
page 28

LPC BUS

port 0

port 1

SATA HDD
Conn. page 33

SATA ODD
Conn. page 33

HDA Codec
ALC283
page 34

D-MIC
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Speaker
page 34

LED
page 32

RTC CKT.
page 13

Power On/Off CKT.
page 32

Fan Control
page 31

DC/DC
Interface CKT
page 37

Power Circuit
page 38~52

RJ45 Conn
page 30

SD/MMC 2 IN 1
Card Reader
page 30

ENE
KB9012/KB9022
page 35

Touch Pad
page 36

Int.KBD
page 31

Sub board

LID SW - Power/B
page 32

USB20/B
-USB20 x2
page 36

BIOS ROM

SYS BIOS (8M)
page 14

Security Classification	Compal Secret Data		
Issued Date	2012/09/12	Deciphered Date	2015/07/08

Compal Electronics, Inc.	
Title	Block Diagrams
Size: Custom	Document Number: Z5WAK M/B LA-B221P
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Date: Wednesday, February 12, 2014	Sheet 2 of 52

Voltage Rails

Power Plane	Description	S0	S3	S4	S5
VIN	Adapter power supply (19V)	ON	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON
+CPU_CORE	Core voltage for APU	ON	OFF	OFF	OFF
+CPU_CORE_NB	Voltage for VDDNB	ON	OFF	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	DIS	OFF	OFF	OFF
+VDDCI	0.95-1.2V switched power rail	DIS	OFF	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF	OFF
+0.95VSDGPU	1.0V switched power rail for VGA	DIS	OFF	OFF	OFF
+1.1VALW	1.1V switched power rail for FCH	ON	ON	AC/DC	AC/DC
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF	OFF
+1.05VS	1.05VS switched power rail for APU	ON	OFF	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF	OFF
+1.5VS	1.5VS switched power rail	ON	OFF	OFF	OFF
+1.5VSDGPU	1.5V switched power rail for VGA	DIS	OFF	OFF	OFF
+1.8VSDGPU	1.8V switched power rail for VGA	DIS	OFF	OFF	OFF
+1.8VS	1.8VS for CPU_VDDA	ON	OFF	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON	ON
+3V_LAN	3.3V power rail for LAN	ON	ON	WOL	WOL
+3VS_WLAN	3.3V power rail for WLAN	ON	IOAC	IOAC	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON	ON

EC SM Bus1 address			EC SM Bus2 address		
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X	16H	SB-TSI (APU)	1001 100X	96H
			VGA Internal Thermal		

FCH SM Bus 0 address			FCH SM Bus 1 address		
Device	Address	HEX	Device	Address	HEX
DDR DIMM1	1010 000Xb	A0H			
DDR DIMM2	1010 001Xb	A2H			
MINI CARD					

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V				
Ra	100K +/- 1%				
Board ID	Rb	V min	V typ	V max	EC AD
0	0		0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V		0xE7 - 0xFF

ZZZ

PCB PCB@
DA60014Q000
LA-B221P REV0

BOARD ID Table

Board ID	PCB Revision
0	EVT
1	DVT
2	
3	
4	
5	
6	
7	

BOM Option Table

BOM Structure	Description
9022@	Use EC 9022
9012@	Use EC 9012
UMA@	Display output from APU (UMA only)
VGA@	Use VGA (PX or DIS only)
AL@	Use Auto load EC code function
AC@	Support AC Function
NOAC@	No Support AC Function
TPM@	Support D TPM function
CONN@	Connector (Control by ME)
HDT@	Debug Connector
EMC@	EMC Component
XEMC@	Reservec for EMC
TPSM@	Use APU SMBus for T/P
TPBRI@	Use USB to I2C IC for T/P
USBTP@	Use USB T/P
MOS@	Use MOSART soluation USB to I2C TP
X76@	VRAM ID Table (Load By X76J)
128@	VRAM x 8pcs
OPAL@	ATI OPAL VGA CONTROLLER
JET@	ATi JET VGA CONTROLLER
BL@	BACK LIGHT CIRCUIT
@	Unpop
X76@	VRAM type select

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: Notes List

Size: Custom | Document Number: Z5WAK M/B LA-B221P | Rev: 0.2

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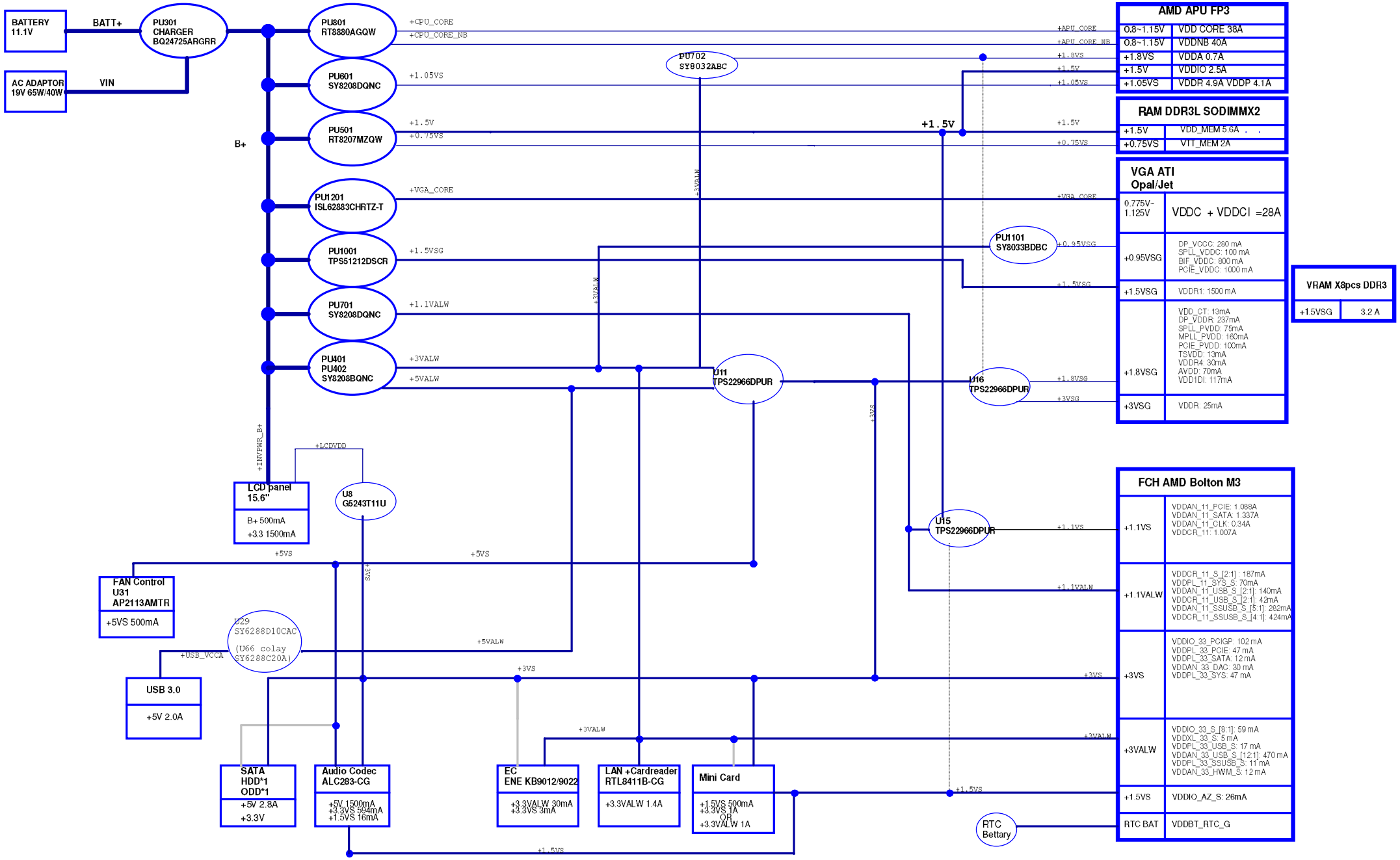
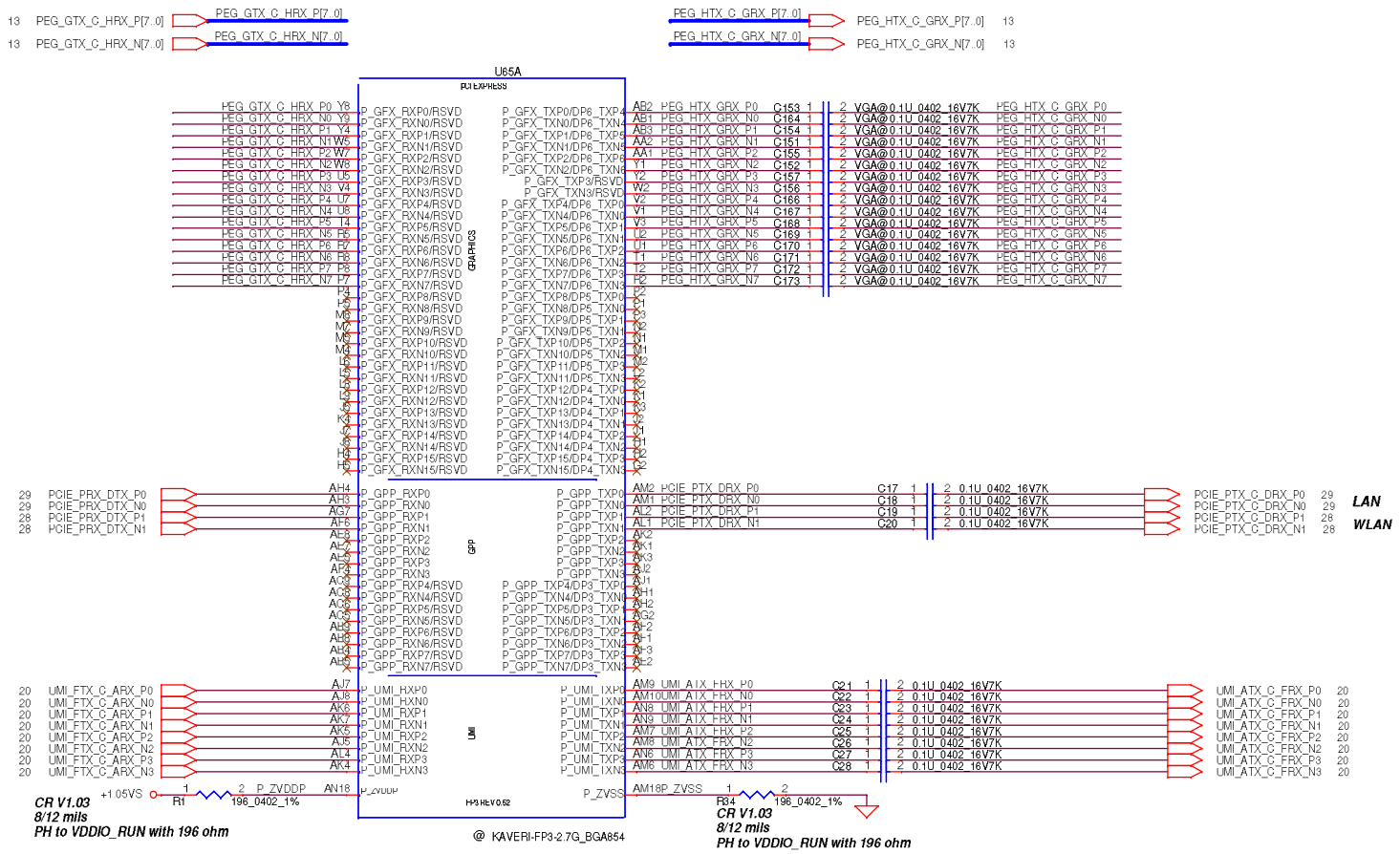


Security Classification	Compal Secret Data		
Issued Date	2011/07/08	Deciphered Date	2015/07/08

Title: POWER DELIVERY CHART

Size	Document Number	Rev
Custom	Z5WAK LA-B221P	0.2

Date: Wednesday, February 12, 2014 Sheet 4 of 52



U65 A10@ — SA00007S300 — A10-7300_854P_19W

U65 A8@ — SA00007S200 — A8-7100_854P_19W

U65 2367@ — SA00007D100 — KAVERI_1.8G BGA 854P

U65 4467@ — SA00007D000 — KAVERI_1.8G BGA 854P

Change to PC sample PN
02/11

Security Classification	Compal Secret Data		
Issued Date	2012/09/12	Deciphered Date	2012/07/29

Compal Electronics, Inc.

Title: FP3 PCIE/UMI

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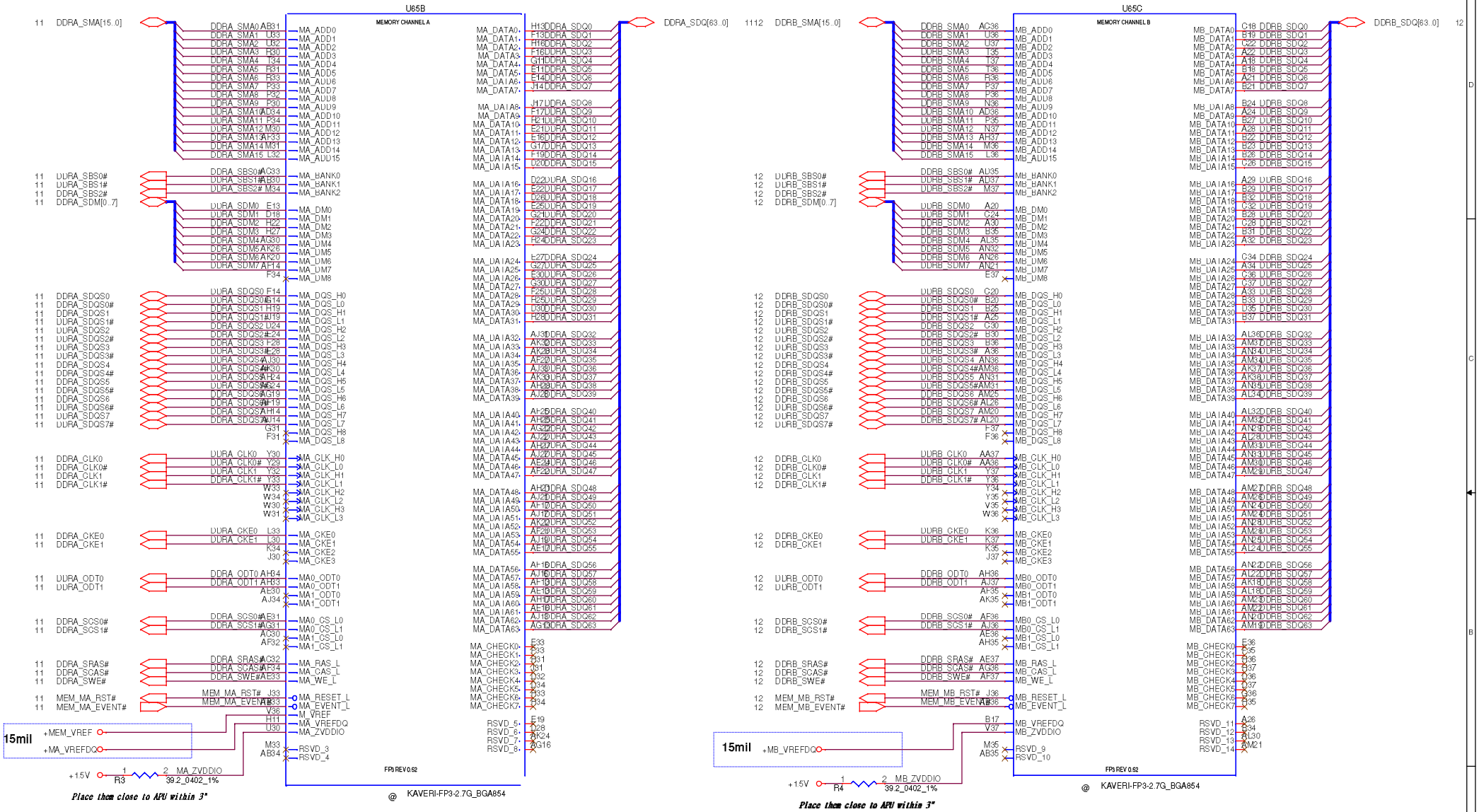
Date: Wednesday, February 12, 2014 | Sheet 5 of 52



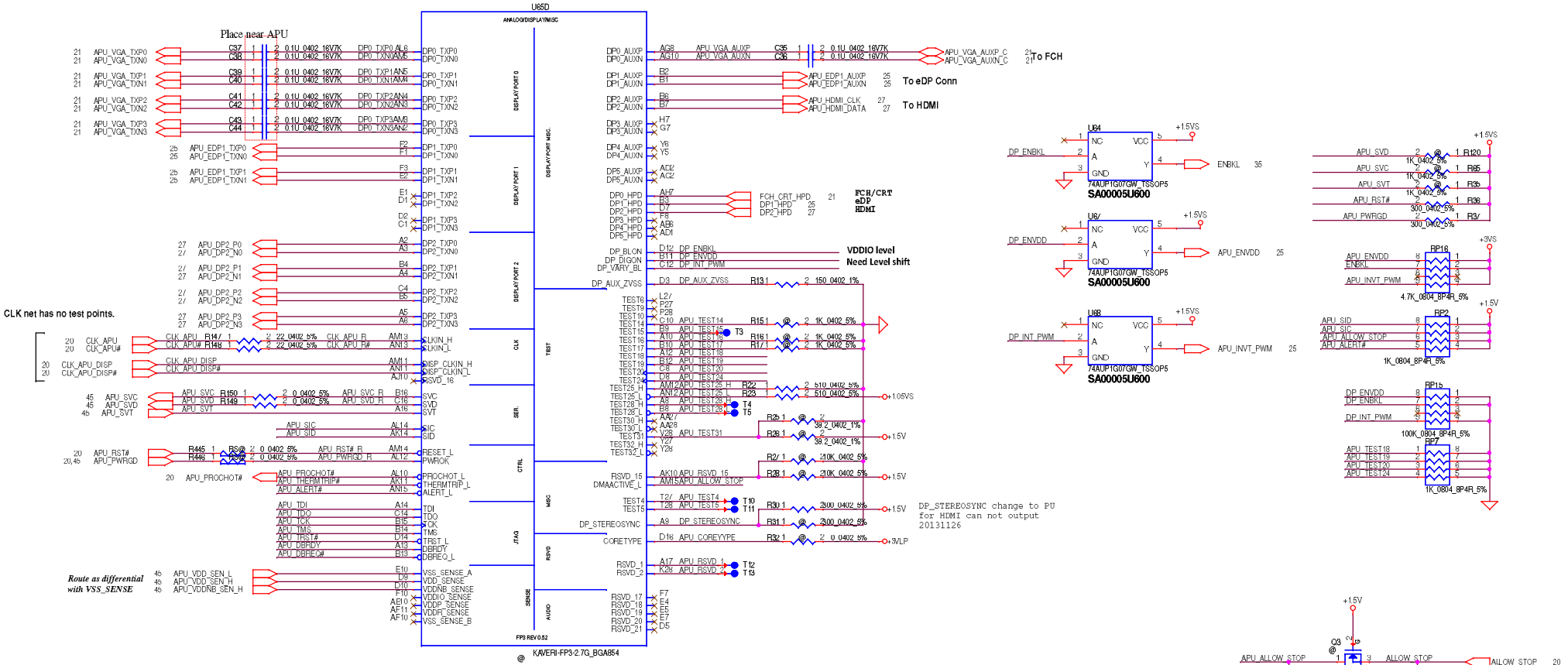
Security Classification	Compal Secret Data		
Issued Date	2012/09/12	Deciphered Date	2012/07/29

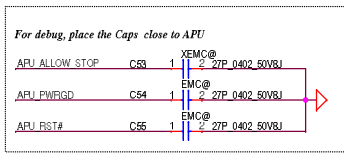
Compal Electronics, Inc.

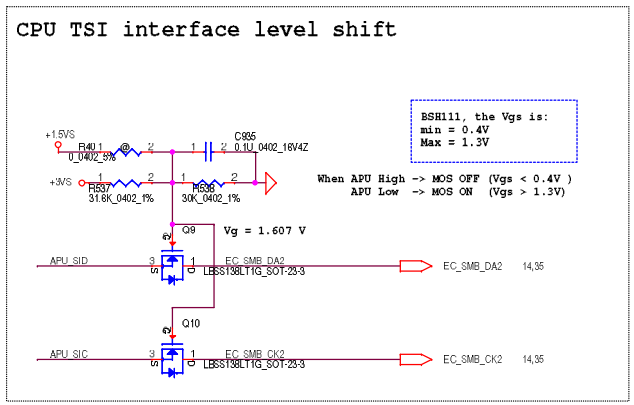
Title: FP3 DDRIII MEMORY I/F

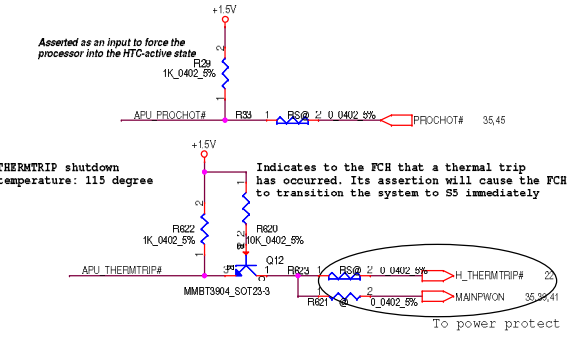
Size: Custom | Document Number: Z5WAK M/B LA-B221P | Rev: 0.2

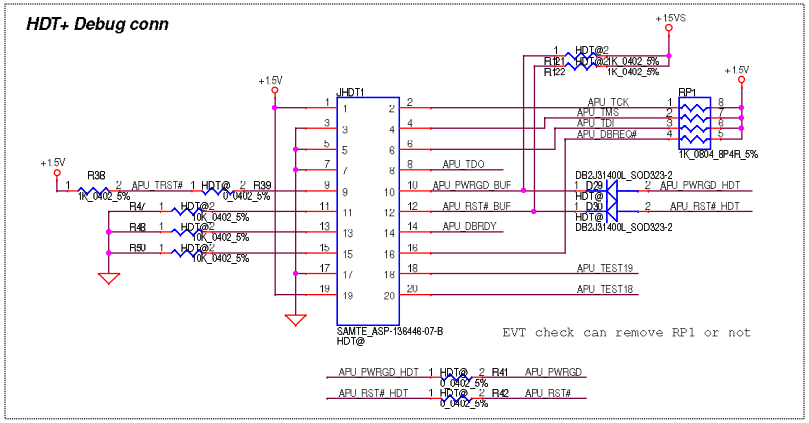
Date: Wednesday, February 12, 2014 | Sheet 6 of 52











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Issued Date	2012/09/12	Deciphered Date	2012/07/29

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Compal Electronics, Inc.

Title: FP3 Display/MISC/HDT

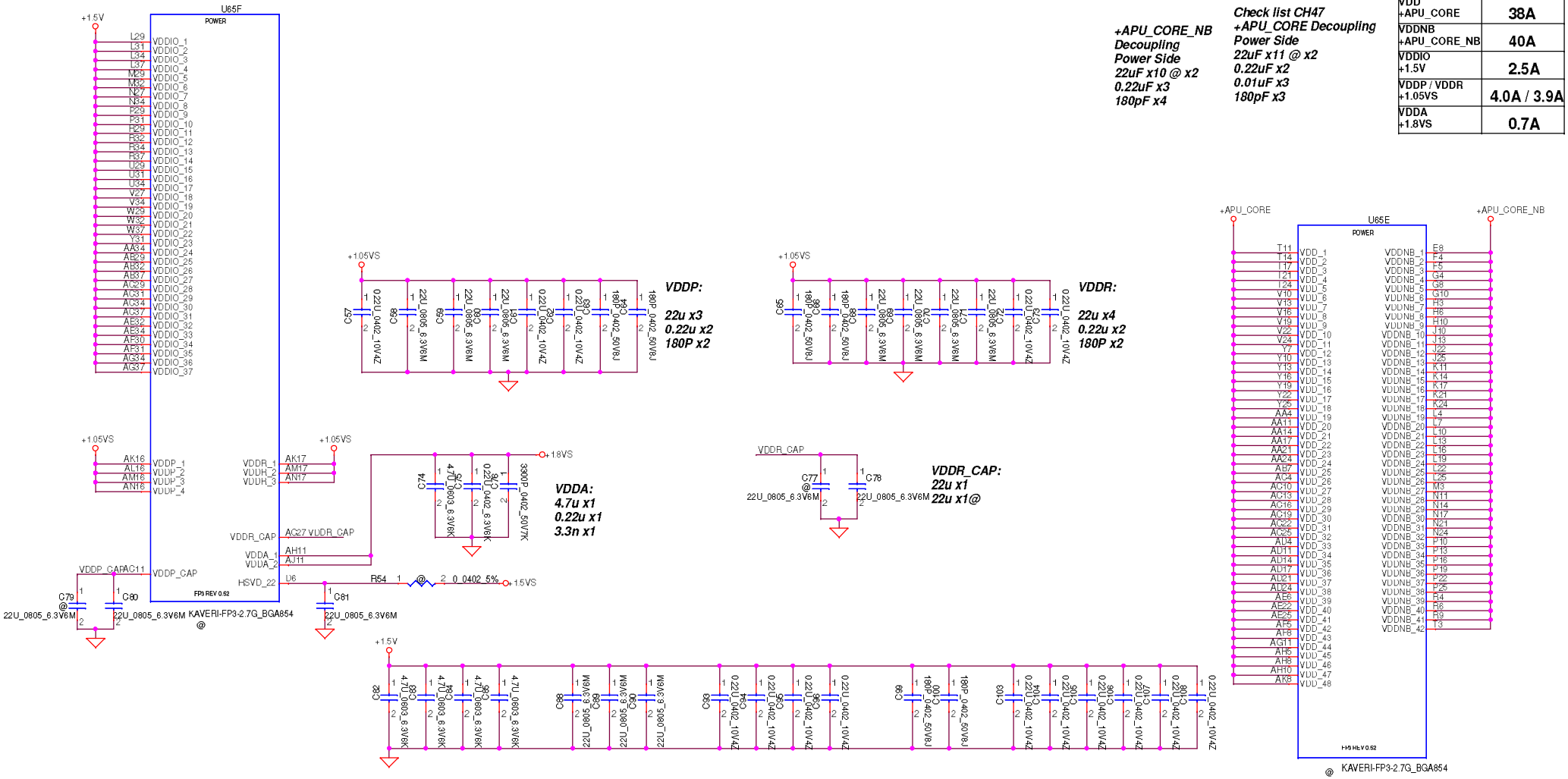
Size	Document Number	Rev
C	Z5WAK M/B LA-B221P	0.2

Date: Wednesday, February 12, 2014 Sheet 7 of 52

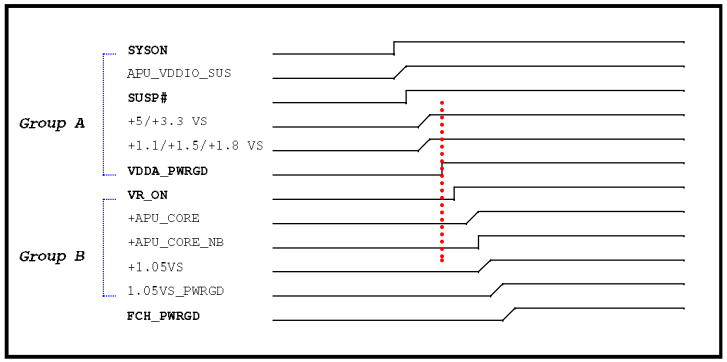
Power Name	Consumption
VDD +APU_CORE	38A
VDDNB +APU_CORE_NB	40A
VDDIO +1.5V	2.5A
VDDP / VDDR +1.05VS	4.0A / 3.9A
VDDA +1.8VS	0.7A

+APU_CORE_NB Decoupling Power Side
22uF x10 @ x2
0.22uF x3
180pF x4

Check list CH47
+APU_CORE Decoupling Power Side
22uF x11 @ x2
0.22uF x2
0.01uF x3
180pF x3



APU sequence : GROUP A need ramp before GROUP B



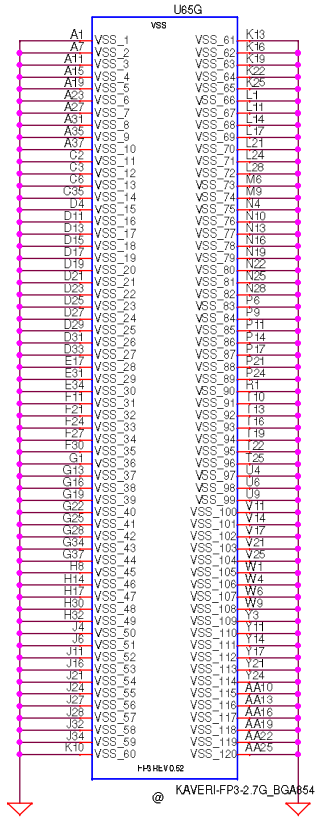
Security Classification	Compal Secret Data		
Issued Date	2012/09/12	Deciphered Date	2012/07/29

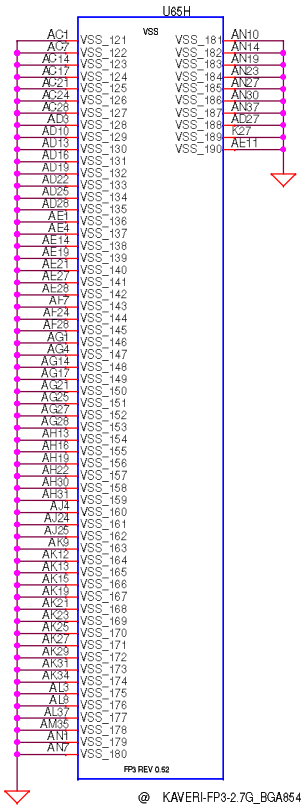
Compal Electronics, Inc.

Title: FP3 Power

Size: Custom | Document Number: Z5WAK M/B LA-B221P | Rev: 0.2

Date: Wednesday, February 12, 2014 | Sheet 8 of 52





Security Classification	Compal Secret Data		
Issued Date	2012/09/12	Deciphered Date	2012/07/29

Compal Electronics, Inc.

Title: FP3 GND

Size: Custom | Document Number: Z5WAK M/B LA-B221P | Rev: 0.2

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Panel ENBKL

Panel ENVDD

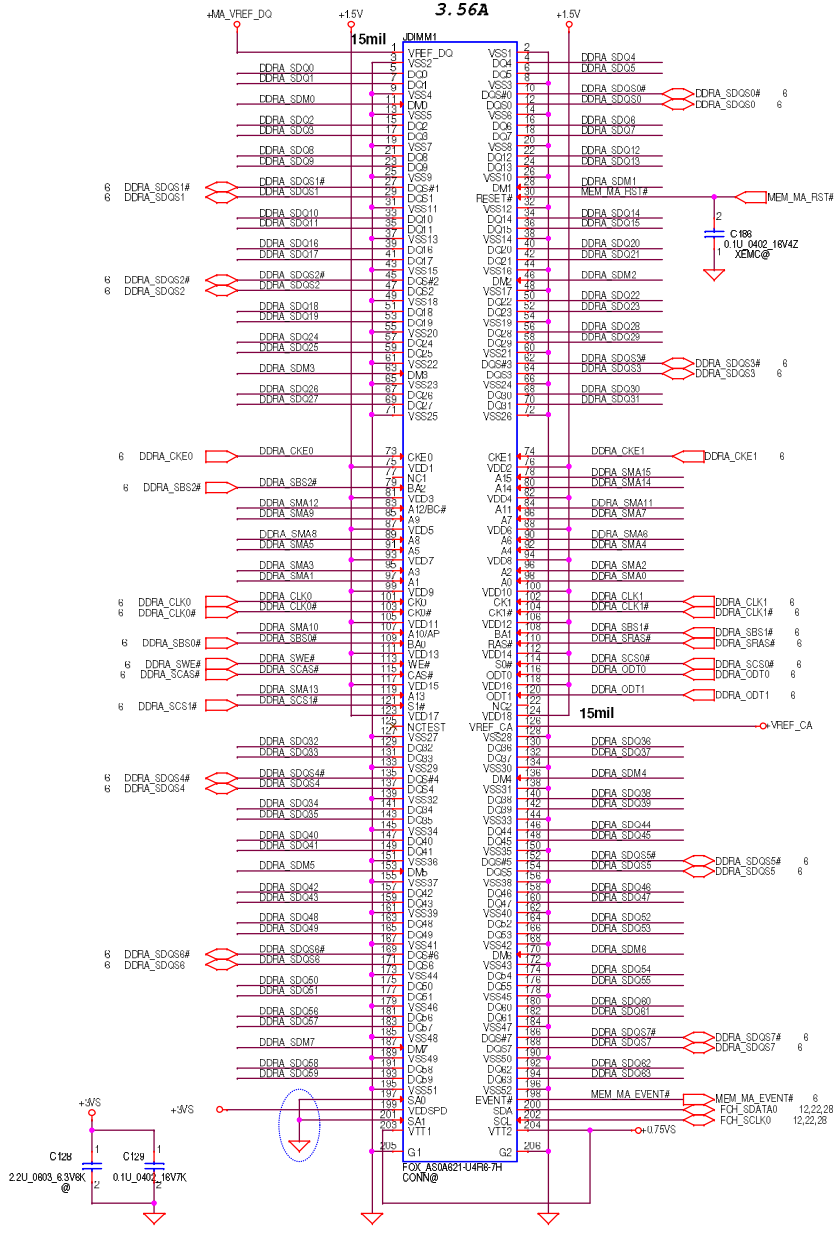
Panel PWM

Security Classification	Compal Secret Data		
Issued Date	2011/07/08	Deciphered Date	2015/07/08

Title: AMD FS1R2 Singal Level Shifter

Size: Custom | Document Number: Z5WAK M/B LA-B221P | Rev: 0.2

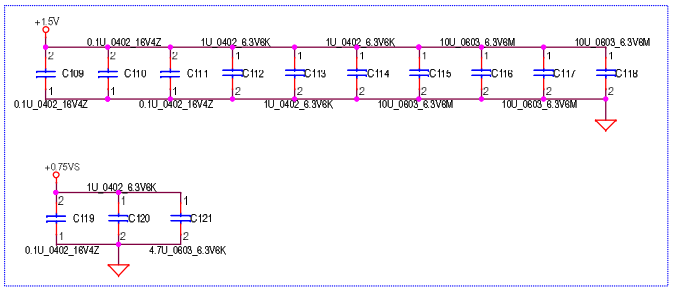
Date: Wednesday, February 12, 2014 | Sheet 10 of 52



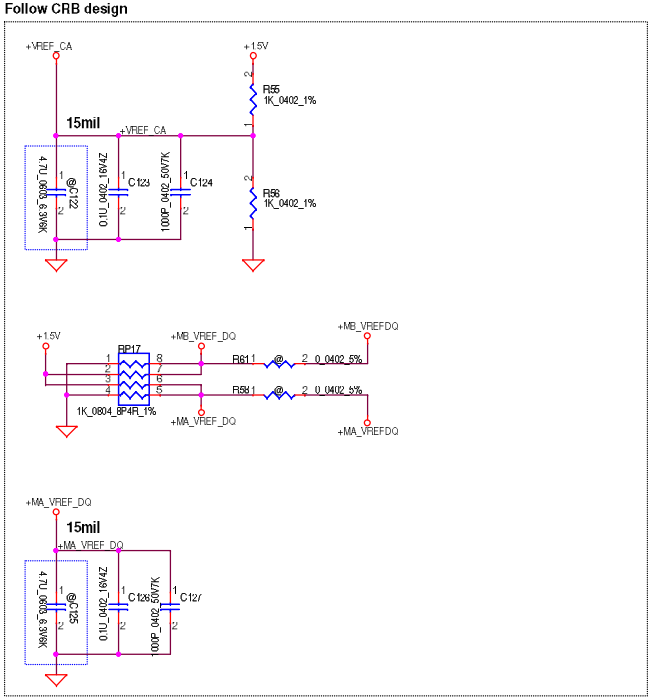
DIMM_A STD H:9.2mm

<Address: 00>

Place near DIMM1

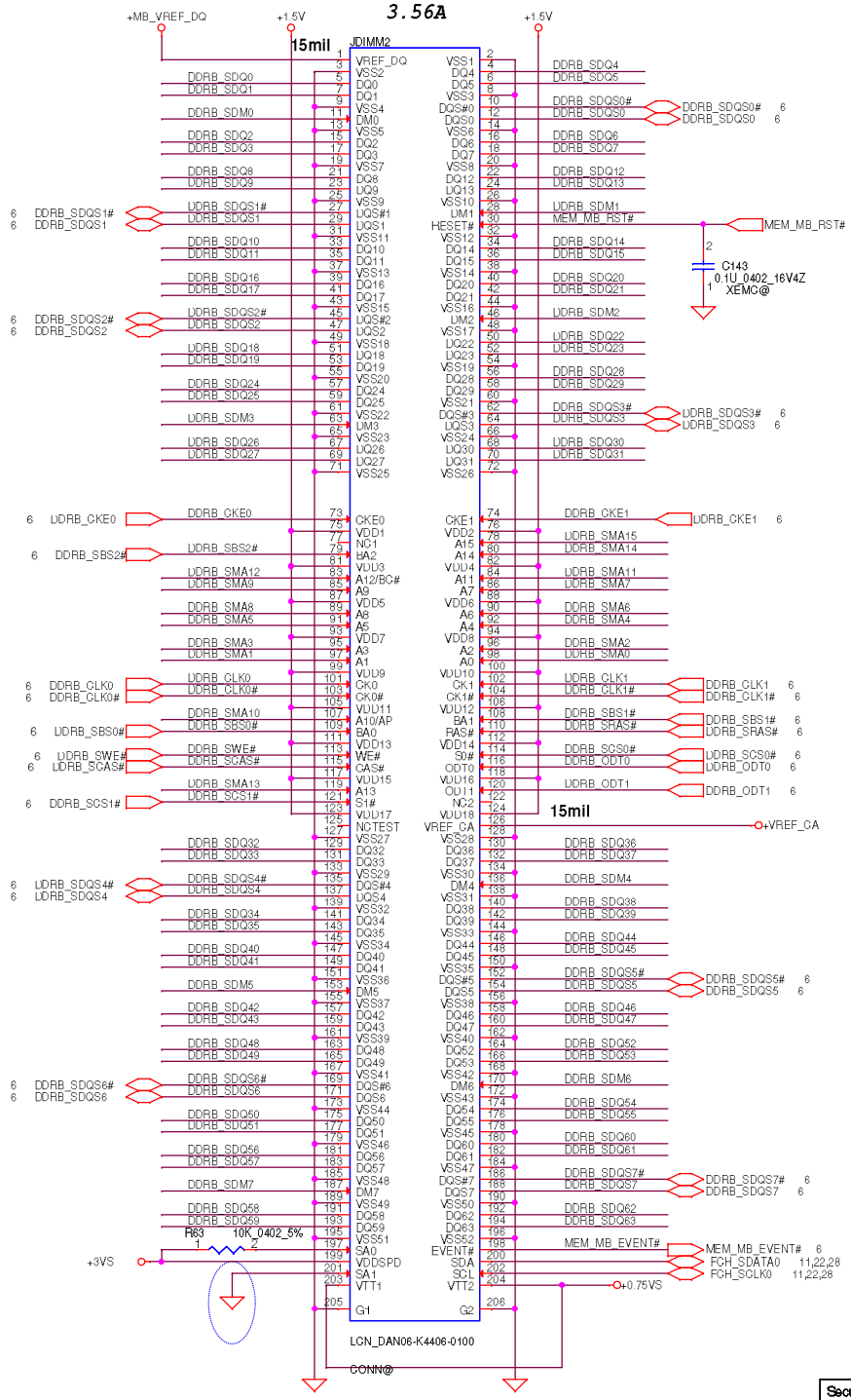


Follow CRB design



follow CRB design

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2012/09/12	Deciphered Date	2012/07/29	Title	DIMM_A
				Size C	Document Number Z5WAK M/B LA-B221P Rev 0.2
				Date: Wednesday, February 12, 2014	Sheet 11 of 52



DIMM_B STD H:5.2mm

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Issued Date	2012/09/12	Deciphered Date	2012/07/29

Compal Electronics, Inc.

Title: DIMM_B

Size: Custom | Document Number: Z5WAK M/B LA-B221P | Rev: 0.2

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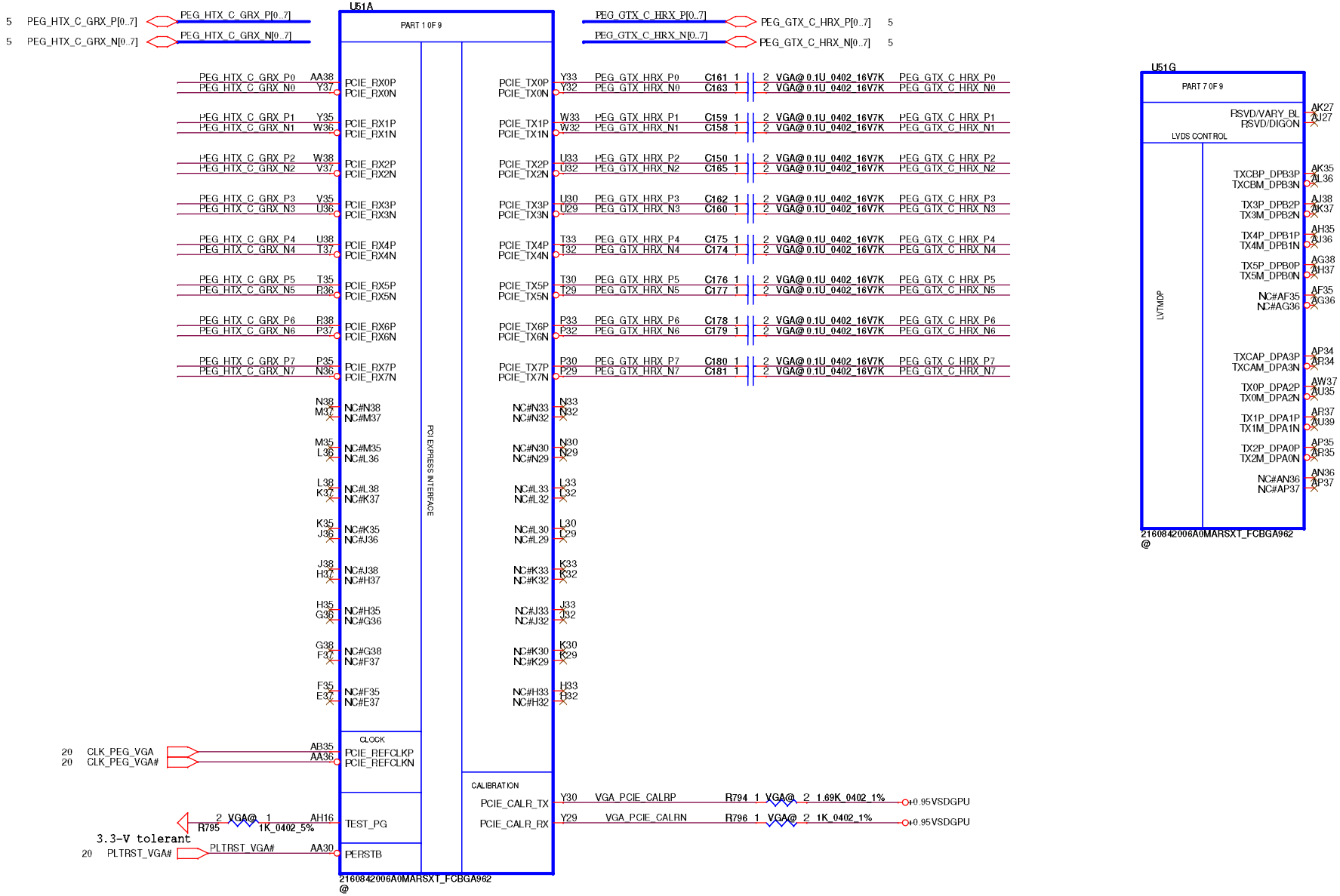
GFX PCIE LANE REVERSAL



U51
JET XT M2
JET@
SA000079000

U51
OPAL XT M2 FCBGA
OPAL@
SA000078V20
CHANGE TO R3 PN
02/11

Security Classification	Compal Secret Data		
Issued Date	2012/09/12	Deciphered Date	2013/07/10

Compal Electronics, Inc.

Title: OPAL-Pro_PCIE

Size: Custom | Document Number: Z5WAK M/B LA-B221P | Rev: 0.2

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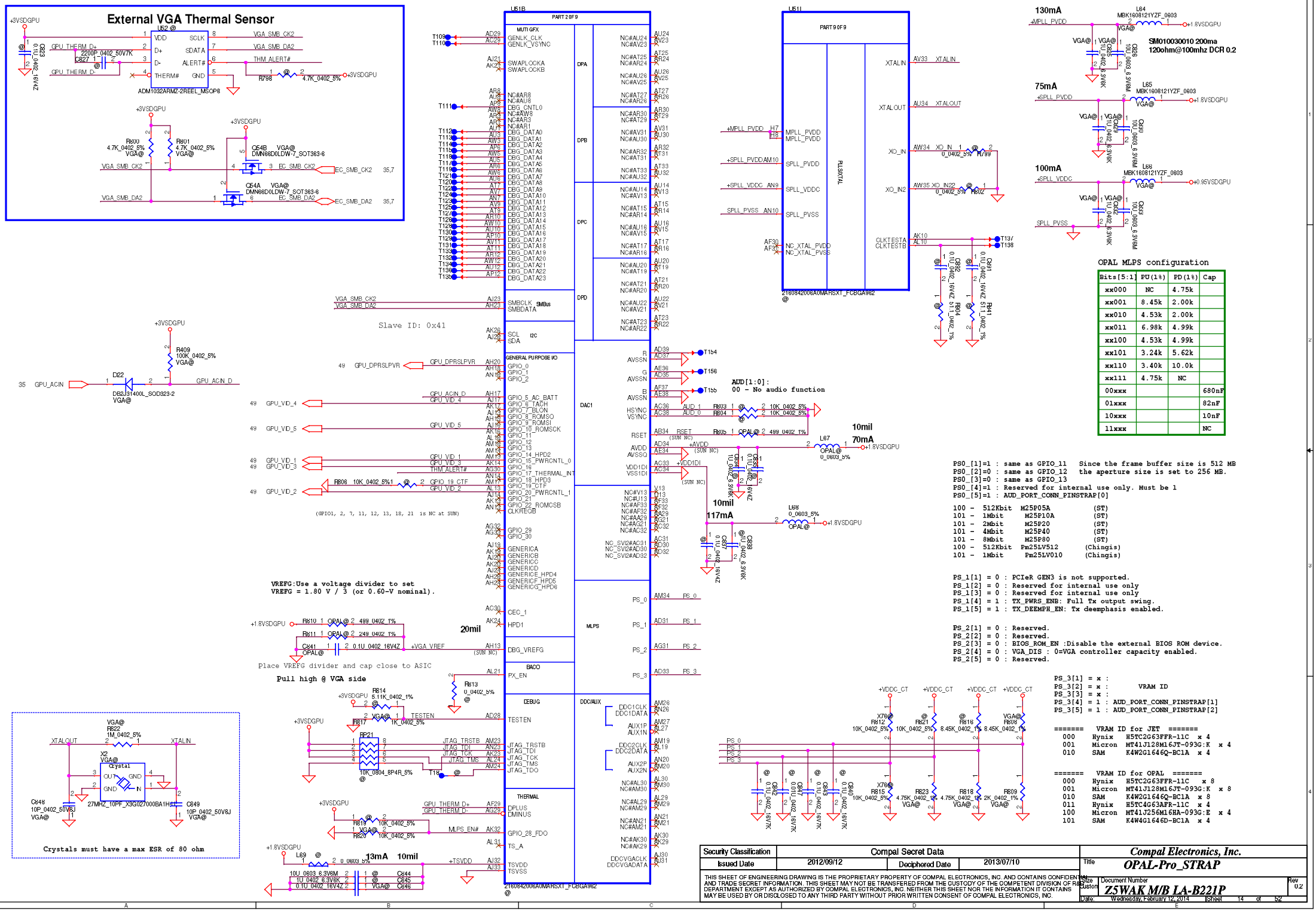
External VGA Thermal Sensor
ADM1032ARMZ-2REEL_MSOP8
Slave ID: 0x41
OPAL MLPS configuration
Bits[5:1] | PU(1%) | PD(1%) | Cap
xx000 | NC | 4.75k |
xx001 | 8.45k | 2.00k |
xx010 | 4.53k | 2.00k |
xx011 | 6.98k | 4.99k |
xx100 | 4.53k | 4.99k |
xx101 | 3.24k | 5.62k |
xx110 | 3.40k | 10.0k |
xx111 | 4.75k | NC |
00xxx | | | 680nF
01xxx | | | 82nF
10xxx | | | 10nF
11xxx | | | NC
AUD[1:0]:
00 - No audio function
PS0_[1]=1 : same as GPIO_11 Since the frame buffer size is 512 MB
PS0_[2]=0 : same as GPIO_12 the aperture size is set to 256 MB.
PS0_[3]=0 : same as GPIO_13
PS0_[4]=1 : Reserved for internal use only. Must be 1
PS0_[5]=1 : AUD_PORT_CONN_PINSTRAP[0]
100 - 512Kbit M25P05A (ST)
101 - 1Mbit M25P10A (ST)
101 - 2mbit M25P20 (ST)
101 - 4Mbit M25P40 (ST)
101 - 8Mbit M25P80 (ST)
100 - 512Kbit Pm25LV512 (Chingis)
101 - 1Mbit Pm25LV010 (Chingis)
PS_1[1] = 0 : PCIeR GEN3 is not supported.
PS_1[2] = 0 : Reserved for internal use only
PS_1[3] = 0 : Reserved for internal use only
PS_1[4] = 1 : TX_PWRS_ENB: Full Tx output swing.
PS_1[5] = 1 : TX_DEEMPH_EN: Tx deemphasis enabled.
PS_2[1] = 0 : Reserved.
PS_2[2] = 0 : Reserved.
PS_2[3] = 0 : BIOS_ROM_EN :Disable the external BIOS ROM device.
PS_2[4] = 0 : VGA_DIS : 0=VGA controller capacity enabled.
PS_2[5] = 0 : Reserved.
PS_3[1] = x :
PS_3[2] = x : VRAM ID
PS_3[3] = x :
PS_3[4] = 1 : AUD_PORT_CONN_PINSTRAP[1]
PS_3[5] = 1 : AUD_PORT_CONN_PINSTRAP[2]
======= VRAM ID for JET =======
000 Hynix H5TC2G63FFR-11C x 4
001 Micron MT41J128M16JT-093G:K x 4
010 SAM K4W2G1646Q-BC1A x 4
======= VRAM ID for OPAL =======
000 Hynix H5TC2G63FFR-11C x 8
001 Micron MT41J128M16JT-093G:K x 8
010 SAM K4W2G1646Q-BC1A x 8
011 Hynix H5TC4G63AFR-11C x 4
100 Micron MT41J256M16HA-093G:E x 4
101 SAM K4W4G1646D-BC1A x 4
VREFG:Use a voltage divider to set
VREFG = 1.80 V / 3 (or 0.60-V nominal).
Place VREFG divider and cap close to ASIC
Pull high @ VGA side
Crystals must have a max ESR of 80 ohm
130mA
75mA
100mA
SM010030010 200ma
120ohm@100mhz DCR 0.2
10mil
70mA
10mil
117mA
20mil
13mA
10mil
Security Classification
Compal Secret Data
Issued Date
2012/09/12
Deciphered Date
2013/07/10
Compal Electronics, Inc.
Title
OPAL-Pro_STRAP
Size
Document Number
Z5WAK M/B LA-B221P
Rev
0.2
Date: Wednesday, February 12, 2014
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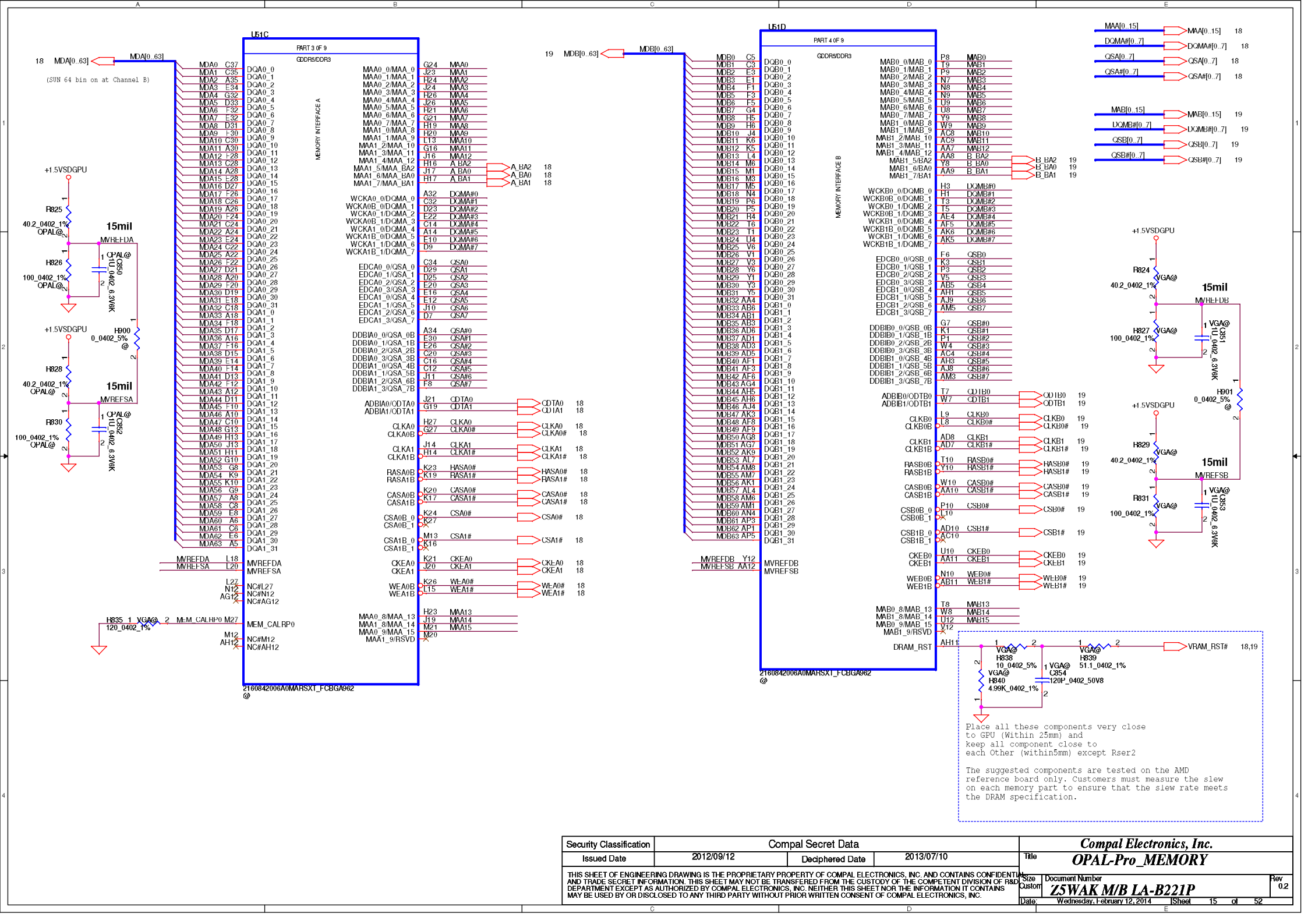
U51C
PART 3 OF 9
GDDR5/DDR3
MEMORY INTERFACE A
2160842006A0MARSXT_FCBGA962
U51D
PART 4 OF 9
GDDR5/DDR3
MEMORY INTERFACE B
2160842006A0MARSXT_FCBGA962
MDA[0..63]
MDB[0..63]
(SUN 64 bin on at Channel B)
+1.5VSDGPU
MVREFDA
MVREFSA
MEM_CALRP0
R825
R826
R828
R830
H900
H835
C350
C351
C352
C353
15mil
R824
R827
R829
R831
H901
H838
H839
H840
C354
VRAM_RST#
Place all these components very close
to GPU (Within 25mm) and
keep all component close to
each Other (within5mm) except Rser2
The suggested components are tested on the AMD
reference board only. Customers must measure the slew
on each memory part to ensure that the slew rate meets
the DRAM specification.
Security Classification
Compal Secret Data
Issued Date
2012/09/12
Deciphered Date
2013/07/10
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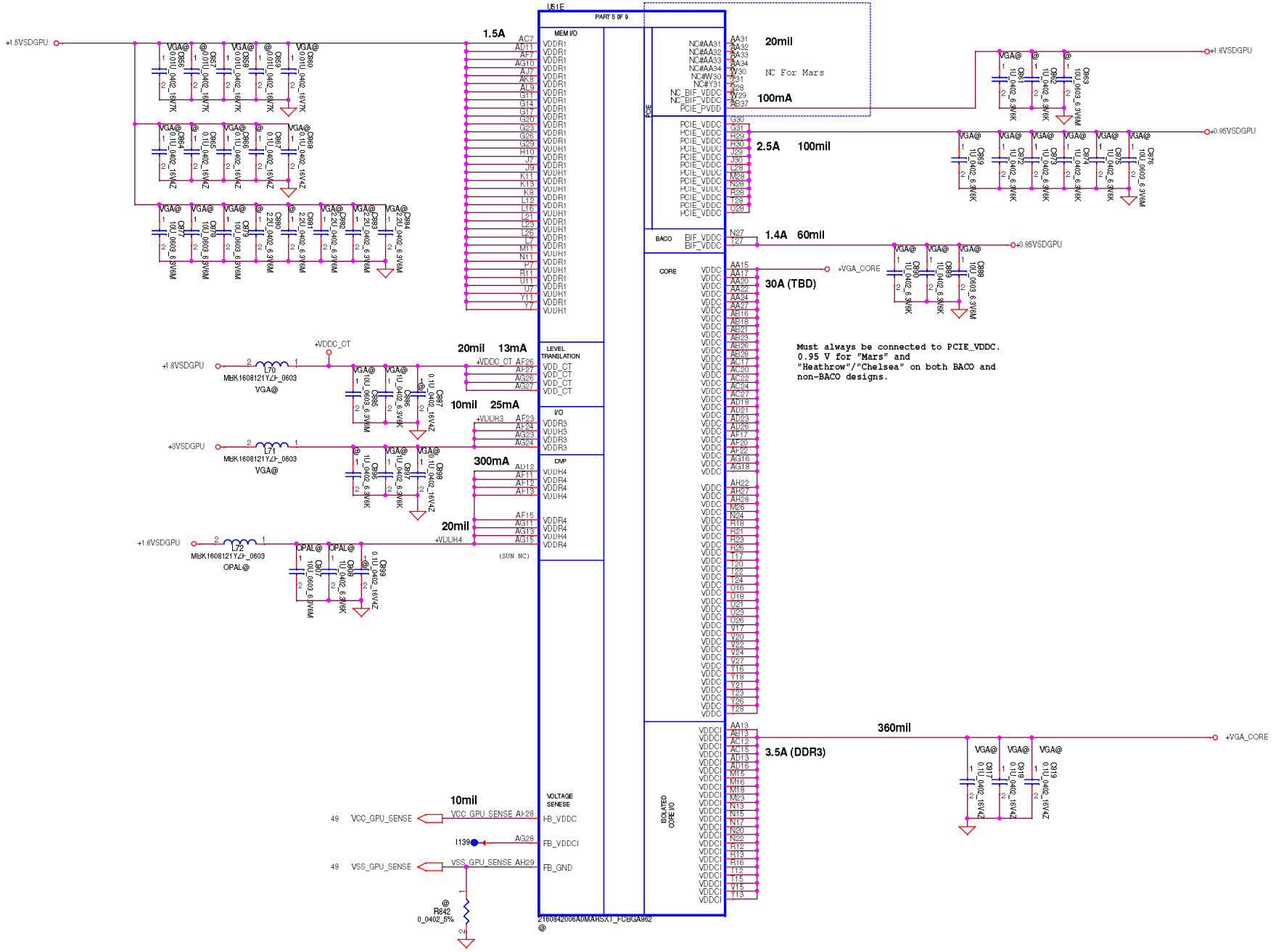
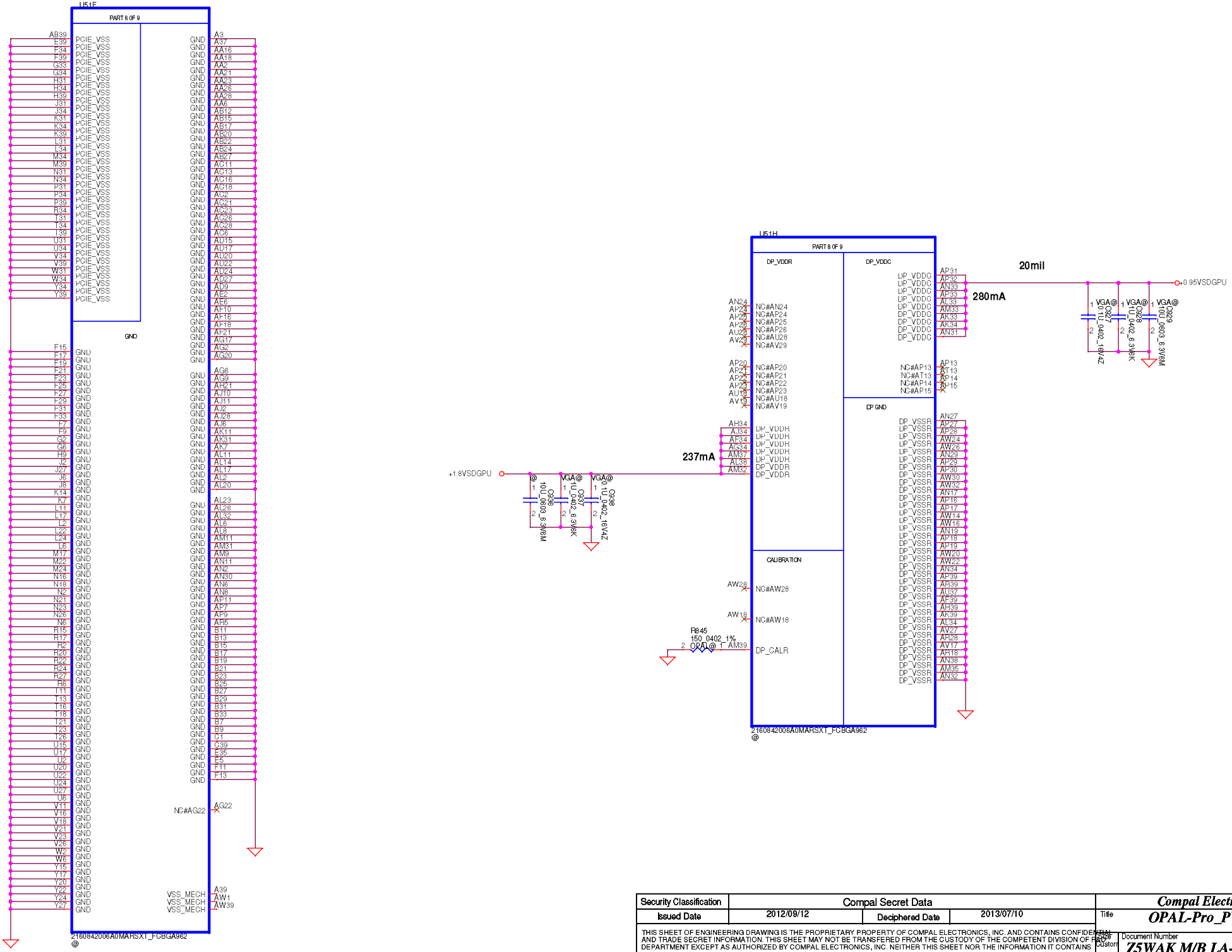
Compal Electronics, Inc.
Title
OPAL-Pro_MEMORY
Size
Custom
Document Number
Z5WAK M/B LA-B221P
Rev
0.2
Date:
Wednesday, February 12, 2014
Sheet
15
of
52



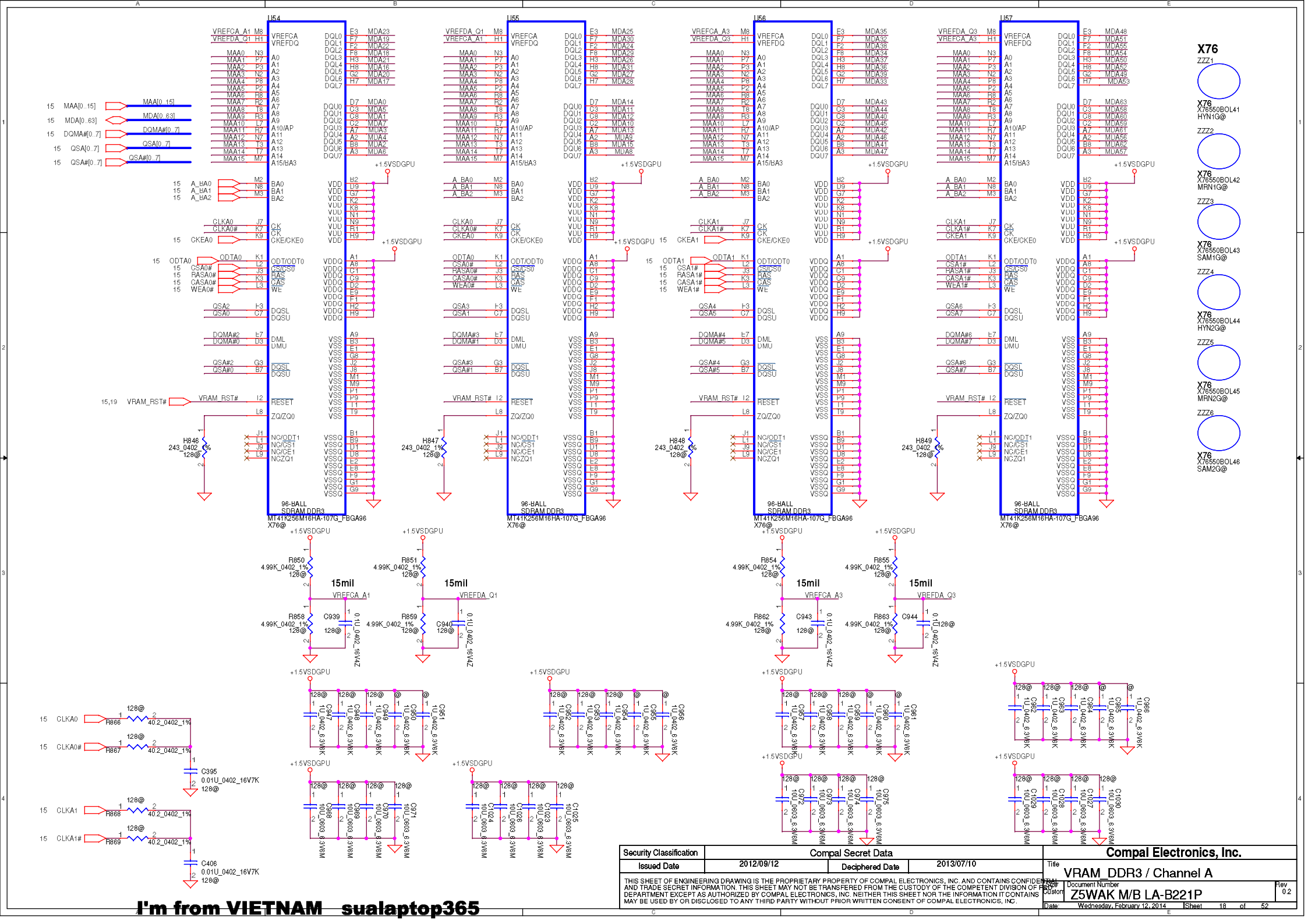
Security Classification	Compal Secret Data		
Issued Date	2012/09/12	Deciphered Date	2013/07/10

Compal Electronics, Inc.	
Title	OPAL-Pro_PWR/GND
Size: Custom	Document Number: Z5WAK M/B LA-B221P
Rev	0.2
Date: Wednesday, February 12, 2014	Sheet 16 of 52



Security Classification	Compal Secret Data		
Issued Date	2012/09/12	Deciphered Date	2013/07/10

Compal Electronics, Inc.			
Title	OPAL-Pro_PWR/GND		
Size: Custom	Document Number: Z5WAK M/B LA-B221P		Rev: 0.2
Date: Wednesday, February 12, 2014	Sheet 17 of 52		



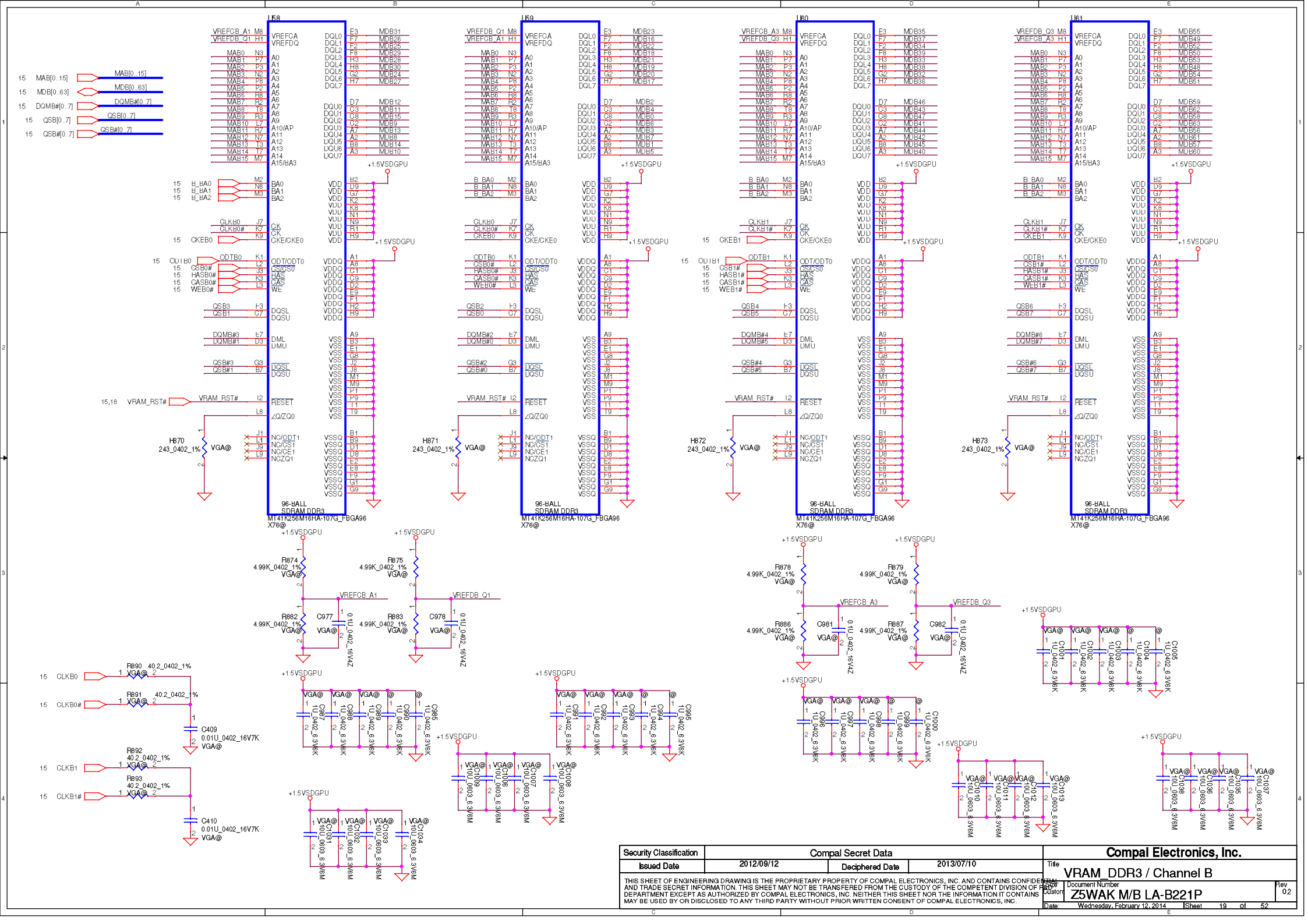
Security Classification	Compal Secret Data		
Issued Date	2012/09/12	Deciphered Date	2013/07/10

Compal Electronics, Inc.

Title: VRAM_DDR3 / Channel A

Size: Custom | Document Number: Z5WAK M/B LA-B221P | Rev: 0.2

Date: Wednesday, February 12, 2014 | Sheet 18 of 52



Security Classification	Compal Secret Data		
Issued Date	2012/09/12	Deciphered Date	2013/07/10

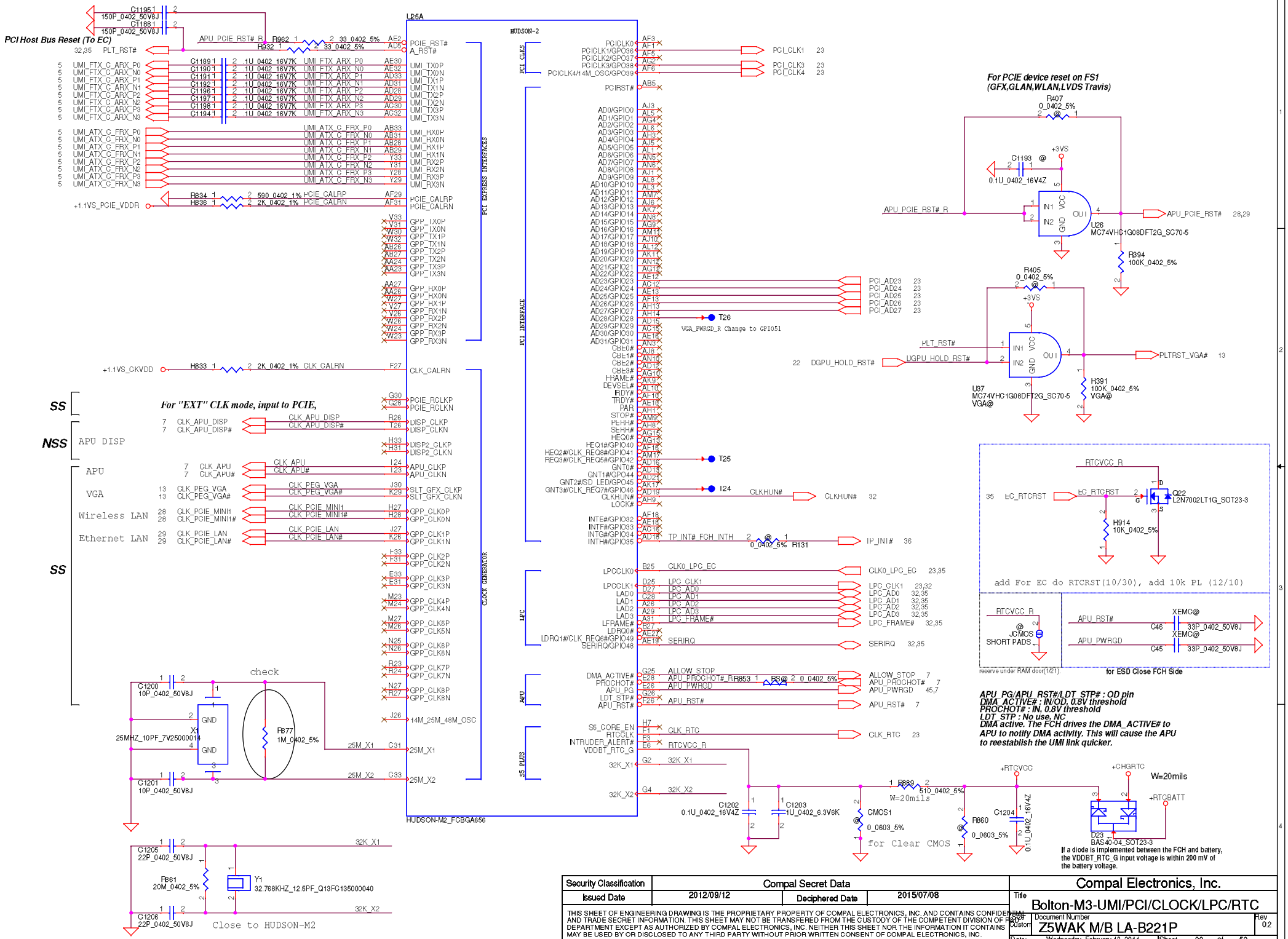
Compal Electronics, Inc.

Title: VRAM_DDR3 / Channel B

Document Number: Z5WAK M/B LA-B221P

Rev: 0.2

Date: Wednesday, February 12, 2014 Sheet 19 of 52



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/09/12	Deciphered Date 2015/07/08	Title: Bolton-M3-UMI/PCI/CLOCK/LPC/RTC
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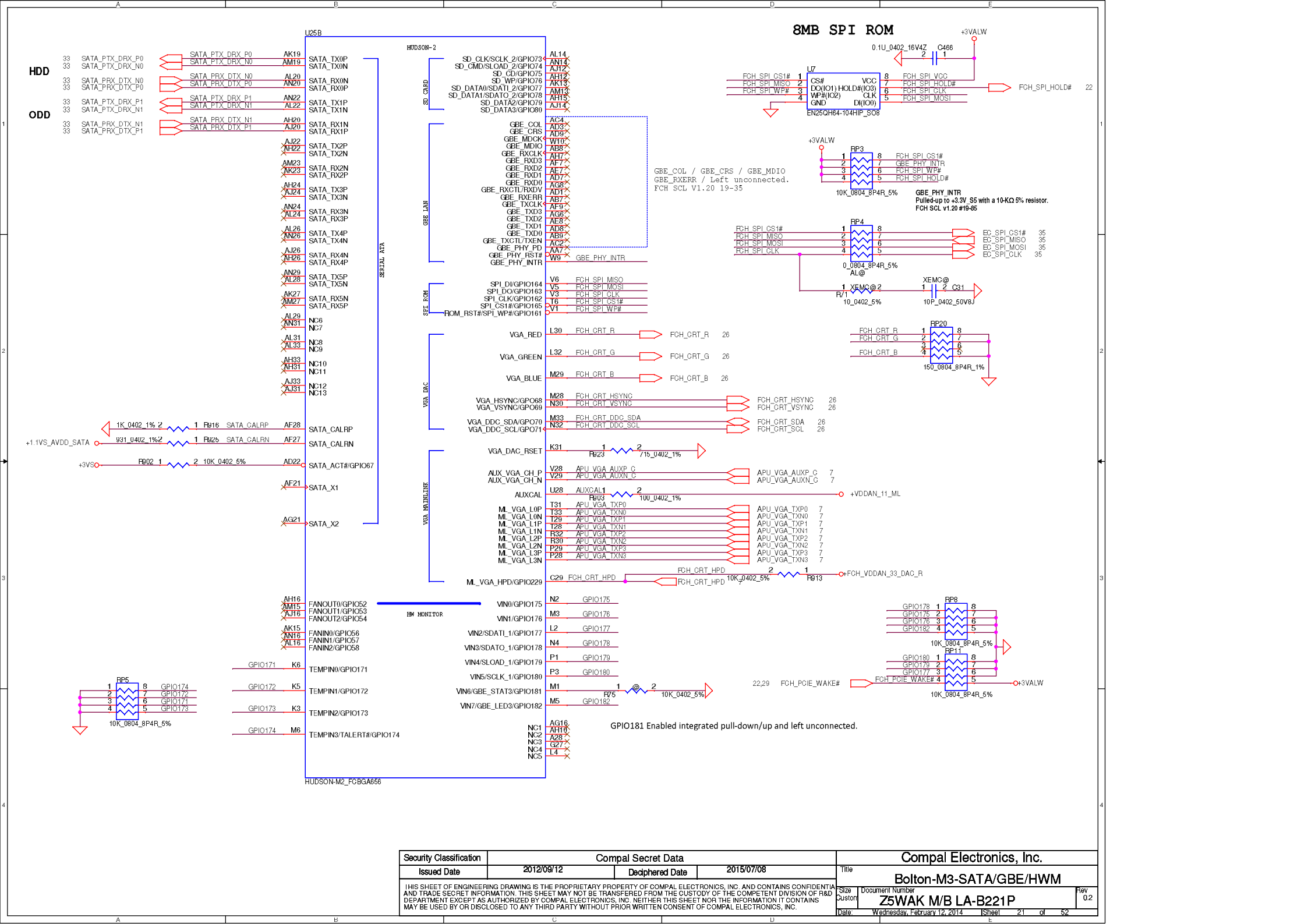
			Date: Wednesday, February 12, 2014; Sheet 20 of 52



Security Classification	Compal Secret Data		
Issued Date	2012/09/12	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: Bolton-M3-SATA/GBE/HWM

Size: Custom | Document Number: Z5WAK M/B LA-B221P | Rev: 0.2

Date: Wednesday, February 12, 2014 | Sheet 21 of 52

THERMTRIP:
Need level shift from +3VALW to +1.5V
Note: Ensure FCH internal pull-up resistor to +3.3V S5 is disabled to prevent leakage when APU is powered down.

SM bus 0-->S0 PWR domain
SM bus 1-->S5 PWR domain

PH on TP side

U25D
HUDSON-2

35	EC_LID_OUT#	AB6	PCIE_RST2#/PCI_PME#/GEVENT4#
		F25	R#/GEVENT22#
		W1	SPI_CS3#/GBE_STAT1/GEVENT21#
35	SLP_S3#	T3	SLP_S3#
35	SLP_S5#	W2	SLP_S5#
35	PBTN_OUT#	J3	PWR_BTN#
35	FCH_PWRGD	N7	PWR_GOOD
		T8	
		T15	TEST0
		T16	TEST1/TMS
		V3	TEST2
35	EC_GA20	AE22	GA20IN/GEVENT0#
35	EC_KBRST#	AG19	KBRST#/GEVENT1#
35	EC_SCI#	R3	LPC_PME#/GEVENT3#
35	EC_SMI#	C26	LPC_SMI#/GEVENT23#
32	LPCPD#	T5	LPC_PD#/GEVENT5#
	SYS_RESET#	U4	SYS_RESET#/GEVENT19#
	FCH_PCIE_WAKE#	K1	WAKE#/GEVENT8#
21,29	FCH_PCIE_WAKE#	V7	IR_RX1/GEVENT20#
35,36	TP_I2C_INT#	R10	THRMTRIP#/SMBALERT#/GEVENT2#
/	H_THERMTRIP#	AF19	WD_PWRGD
35	EC_RSMRST#	U2	RSMRST#
		AG24	CLK_REQ4#/SATA_IS0#/GPIO64
		AE24	CLK_REQ3#/SATA_IS1#/GPIO63
		AF25	SMARTVOLT1/SATA_IS2#/GPIO50
		AF22	CLK_REQ0#/SATA_IS3#/GPIO60
28	MINI1_CLKREQ#	AH17	SATA_IS4#/FANOUT3/GPIO65
		AG18	SATA_IS5#/FANIN3/GPIO69
34	FCH_SPKR	AF23	SPKR/GPIO66
11,12,28	FCH_SCLK0	AD26	SCL0/GPIO43
11,12,28	FCH_SDATA0	AD25	SDA0/GPIO47
36	FCH_SCLK1	T7	SCL1/GPIO227
36	FCH_SDATA1	R7	SDA1/GPIO228
		AG25	CLK_REQ2#/FANIN4/GPIO62
29	LAN_CLKREQ#	AG22	CLK_REQ1#/FANOUT4/GPIO61
		U6	IR_LED#/LLB#/GPIO184
3/,4/,48,49	VGA_PG	AG26	SMARTVOLT2/SHUTDOWN#/GPIO51
		V5	DDR3_RST#/GEVENT7#/VGA_PD
		W8	GBE_LED0/GPIO183
21	FCH_SPI_HOLD#	Y6	SPI_HOLD#/GBE_LED1/GEVENT9#
		V10	GBE_LED2/GEVENT10#
		AA8	GBE_STAT0/GEVENT11#
		AF26	CLK_REQG#/GPIO65/OSCIN/IDLEEXIT#
		M7	BLINK/USB_OC7#/GEVENT18#
		R8	USB_OC6#/IR_TX1/GEVENT6#
		T1	USB_OC5#/IR_TX0/GEVENT17#
		P6	USB_OC4#/IR_RX0/GEVENT16#
		T21	USB_OC3#/AC_PRES/TDO/GEVENT15#
		T22	USB_OC2#/TCK/GEVENT14#
		T23	USB_OC1#/TDI/GEVENT13#
36	USB_OC0#	T6	USB_OC0#/SPI_TPM_CS#/TRST#/GEVENT12#
		AB3	AZ_BITCLK
		AB1	AZ_SDOUT
34	HDA_SDIN0	AA2	AZ_SDIN0/GPIO167
		Y3	AZ_SDIN1/GPIO168
		Y1	AZ_SDIN2/GPIO169
		AD6	AZ_SYNC/GPIO170
		AE4	AZ_RST#
		K19	PS2_DAT/SDA4/GPIO187
		J19	PS2_CLK/CEC/SCL4/GPIO188
		U21	SPI_CS2#/GBE_STAT2/GPIO166
		D21	PS2KB_DAT/GPIO189
20	DGPU_HOLD_RST#	C20	PS2KB_CLK/GPIO190
37	VGA_ON	P23	PS2M_DAT/GPIO191
		C22	PS2M_CLK/GPIO192
		F21	
		K20	KSO_0/GPIO209
		F20	KSO_1/GPIO210
		A22	KSO_2/GPIO211
		E18	KSO_3/GPIO212
		A20	KSO_4/GPIO213
		J18	KSO_5/GPIO214
		H18	KSO_6/GPIO215
		C18	KSO_7/GPIO216
		B21	KSO_8/GPIO217
		K18	KSO_9/GPIO218
		D19	KSO_10/GPIO219
		K18	KSO_11/GPIO220
		C18	KSO_12/GPIO221
		B19	KSO_13/GPIO222
		E17	KSO_14/GPIO223
		A21	KSO_15/GPIO224
		C17	KSO_16/GPIO225
			KSO_17/GPIO226

HUDSON-M2_FCBGA656

USB MISC
USB 1.1
ACPI / WAKE UP EVENTS
GPIO
USB 2.0
USB OC
HD AUDIO
USB 3.0

		G8	USBCLK/14M_25M_48M_OSC
		B9	USB_RCOMP
		H1	USB_FSD1P/GPIO186
		H3	USB_FSD1N
		H6	USB_FSD0P/GPIO185
		H5	USB_FSD0N
		H10	USB_HSD13P
		G10	USB_HSD13N
		K10	USB_HSD12P
		J12	USB_HSD12N
		G12	USB_HSD11P
		F12	USB_HSD11N
		K12	USB_HSD10P
		K13	USB_HSD10N
		B11	USB_HSD9P
		D11	USB_HSD9N
		E10	USB_HSD8P
		F10	USB_HSD8N
		C10	USB_HSD7P
		A10	USB_HSD7N
		H9	USB_HSD6P
		G9	USB_HSD6N
		A8	USB_HSD5P
		C8	USB_HSD5N
		F8	USB_HSD4P
		E8	USB_HSD4N
		C6	USB_HSD3P
		A6	USB_HSD3N
		C5	USB_HSD2P
		A5	USB_HSD2N
		C1	USB_HSD1P
		C3	USB_HSD1N
		E1	USB_HSD0P
		E3	USB_HSD0N
		C16	USBSS_CALRP
		A16	USBSS_CALRN
		A14	USB_SS_TX3P
		C14	USB_SS_TX3N
		C12	USB_SS_RX3P
		A12	USB_SS_RX3N
		D15	USB_SS_TX2P
		B15	USB_SS_TX2N
		E14	USB_SS_RX2P
		F14	USB_SS_RX2N
		E15	USB_SS_TX1P
		G15	USB_SS_TX1N
		H13	USB_SS_RX1P
		G13	USB_SS_RX1N
		J16	USB_SS_TX0P
		H16	USB_SS_TX0N
		J15	USB_SS_RX0P
		K15	USB_SS_RX0N
		H19	SCL2/GPIO193
		G19	SDA2/GPIO194
		G22	SCL3_LV/GPIO195
		G21	SDA3_LV/GPIO196
		F22	
		H22	EC_PWM0/EC_TIMER0/GPIO197
		H21	EC_PWM1/EC_TIMER1/GPIO198
		J22	EC_PWM2/EC_TIMER2/WOL_EN/GPIO199
		J21	EC_PWM3/EC_TIMER3/GPIO200
		K21	
		K22	KSI_0/GPIO201
		F23	KSI_1/GPIO202
		F24	KSI_2/GPIO203
		E24	KSI_3/GPIO204
		D23	KSI_4/GPIO205
		C24	KSI_5/GPIO206
		F18	KSI_6/GPIO207
			KSI_7/GPIO208

USB20_P10 36 — USB20_N10 36 — For USB3.0 Port x1
USB20_P5 36 — USB20_N5 36 — USB to I2C bridge
USB20_P4 28 — USB20_N4 28 — Mini Card
USB20_P3 25 — USB20_N3 25 — TS
USB20_P2 25 — USB20_N2 25 — Camera
USB20_P1 36 — USB20_N1 36
USB20_P0 36 — USB20_N0 36 — For USB2.0 Port x2

RB94 1 — 2 11.8K_0402_1%
RB84 1 — 2 1K_0402_1%
RB85 1 — 2 1K_0402_1%
+FCH_VDD_11_SSUSB_S

USB3_TX0_P 36 — USB3_TX0_P
USB3_TX0_N 36 — USB3_TX0_N
USB3_RX0_P 36 — USB3_RX0_P
USB3_RX0_N 36 — USB3_RX0_N

RP8 10K_0804_8P4R_5%
FCH_GPIO196 1 — 8
FCH_GPIO194 2 — 7
FCH_GPIO193 3 — 6
FCH_GPIO195 4 — 5
FCH_GPIO199 — 23

For PCIE device reset on FS1 (GFX,GLAN,WLAN,LVDS Travis)

Hudson-M2/M3 OHCI CTL DEV 20, Fn 5 <Disable CTL>
Hudson-M3 xHCI CTL DEV 16, Fn 1 xHCI CTL DEV 16, Fn 0
Hudson-M2/M3 EHCI CTL DEV 19, Fn 2
Hudson-M2/M3 EHCI CTL DEV 18, Fn 2 <Support Wakeup>
Hudson-M3 xHCI CTL DEV 16, Fn 1 xHCI CTL DEV 16, Fn 0
On board USB Conn

RP10 33_0804_8P4R_5% EMC@
HDA_BITCLK — HDA_SDOUT — HDA_SDIN0 — HDA_SDIN1 — HDA_SDIN2 — HDA_SDIN3 — HDA_SYNC — HDA_RST#
34 HDA_SDIN0
34 HDA_SDOUT_AUDIO
34 HDA_BITCLK_AUDIO
34 HDA_SYNC_AUDIO
34 HDA_RST_AUDIO#

+3VALW
RH108 1 — 2 100K_0402_5% — USB_OC0#
RH980 1 — 2 10K_0402_5% — H_THERMTRIP#
RH881 1 @ 2 100K_0402_5% — EC_LID_OUT#
RH109 1 @ 2 10K_0402_5% — SYS_RESET#
RH957 1 @ 2 8.2K_0402_5% — LAN_CLKREQ#

+3VS
RH954 1 — 2 2.2K_0402_5% — FCH_SCLK0
RH885 1 — 2 2.2K_0402_5% — FCH_SDATA0
RH888 1 — 2 8.2K_0402_5% — MINI1_CLKREQ#
RH884 1 — 2 10K_0402_5% — WD_PWRGD
RH953 1 — 2 8.2K_0402_5% — LAN_CLKREQ#
RH948 1 — 2 2.2K_0402_5% — EC_RSMRST#
RH952 1 @ 2 10K_0402_5% — HDA_BITCLK

RP9 @ 10K_0804_8P4R_5%
HDA_SDIN0 — HDA_SDIN1 — HDA_SDIN2 — HDA_SDIN3

+3VALW
OPAL@ VGA@
RB83 2K_0402_5% — FCH_GPIO189
RB87 2K_0402_5% — FCH_GPIO190
RB88 2K_0402_5% — FCH_GPIO188
RB89 2K_0402_5% — FCH_GPIO187
RB90 2K_0402_5% — FCH_GPIO166
RB93 100K_0402_5% JET@
RB91 100K_0402_5% UMA@
RB94 100K_0402_5% JET@
RB95 100K_0402_5% UMA@

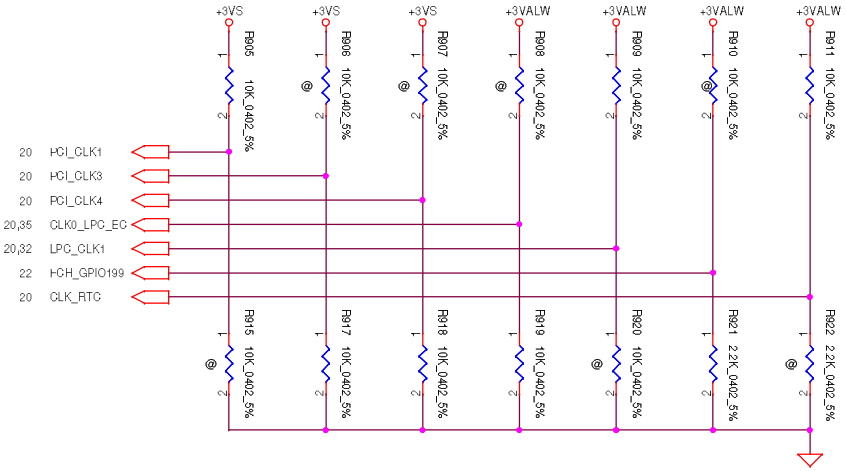
Project SKU ID	Value	
GPIO189 (use VGA)	Low (UMA)	High (VGA)
GPIO190	Low (JET)	High (OPAL)
GPIO188		
GPIO187		
GPIO166		

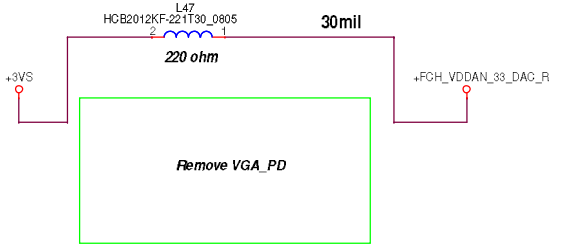
Security Classification	Compal Secret Data		
Issued Date	2012/09/12	Deciphered Date	2015/07/08

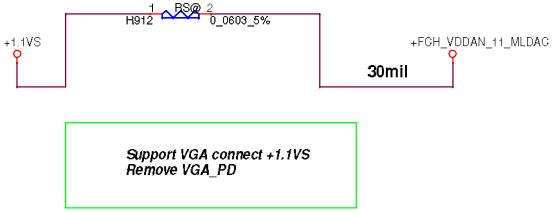
Compal Electronics, Inc.
Title: Bolton-M3-ACPI/USB/EC
Size: C | Document Number: Z5WAK M/B LA-B221P | Rev: 0.2
Date: Wednesday, February 12, 2014 | Sheet 22 of 52

STRAP PINS

	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	FCH_GPIO199	CLK_RTC
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	FCH EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	FCH EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED



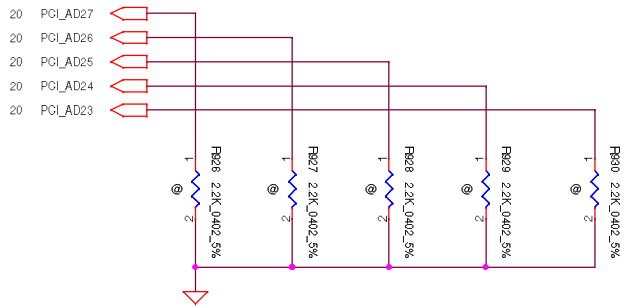




DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	RESERVED DEFAULT	NORMAL REFCLK TERMINATION DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	RESERVED	INVERT REFCLK TERMINATION	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



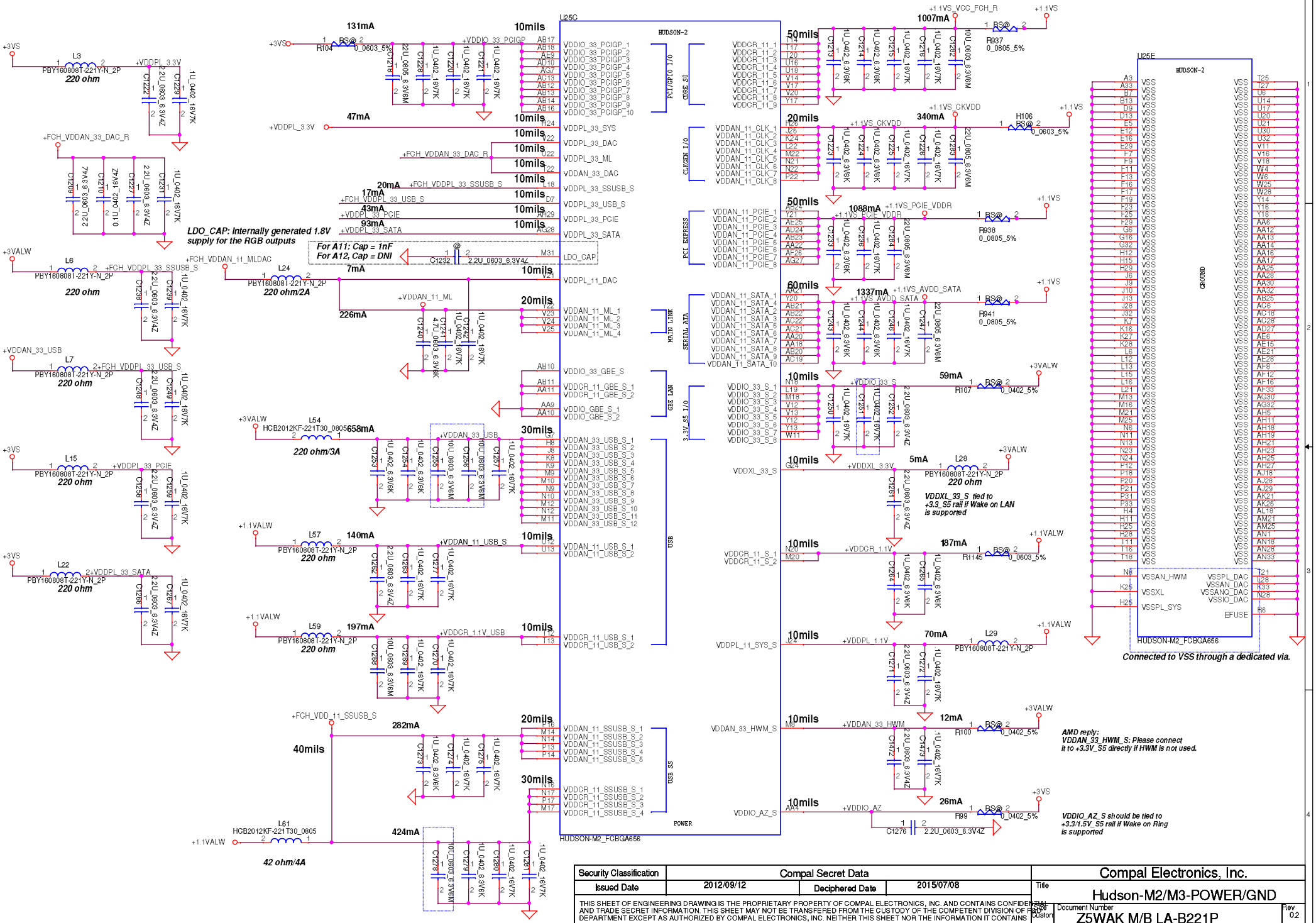
Security Classification	Compal Secret Data		
Issued Date	2012/09/12	Deciphered Date	2015/07/08

Compal Electronics, Inc.

Title: Bolton-M3-STRAP

Size: Custom | Document Number: Z5WAK M/B LA-B221P | Rev: 0.2

Date: Wednesday, February 12, 2014 | Sheet 23 of 52



Security Classification	Compal Secret Data		
Issued Date	2012/09/12	Deciphered Date	2015/07/08

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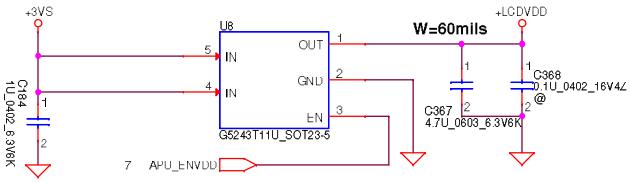
Compal Electronics, Inc.

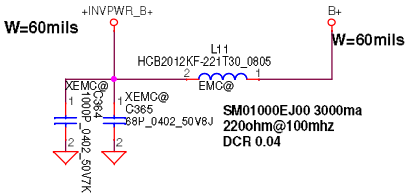
Title: Hudson-M2/M3-POWER/GND

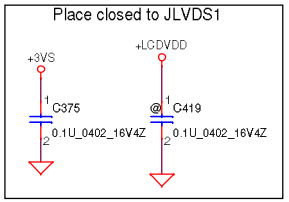
Size: B (Custom) | Document Number: Z5WAK M/B LA-B221P | Rev: 0.2

Date: Wednesday, February 12, 2014 | Sheet 24 of 52

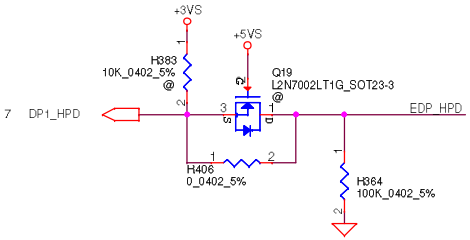
LCD POWER CIRCUIT

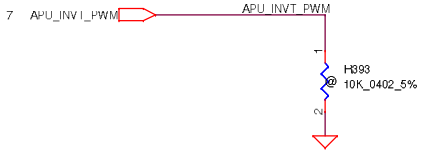


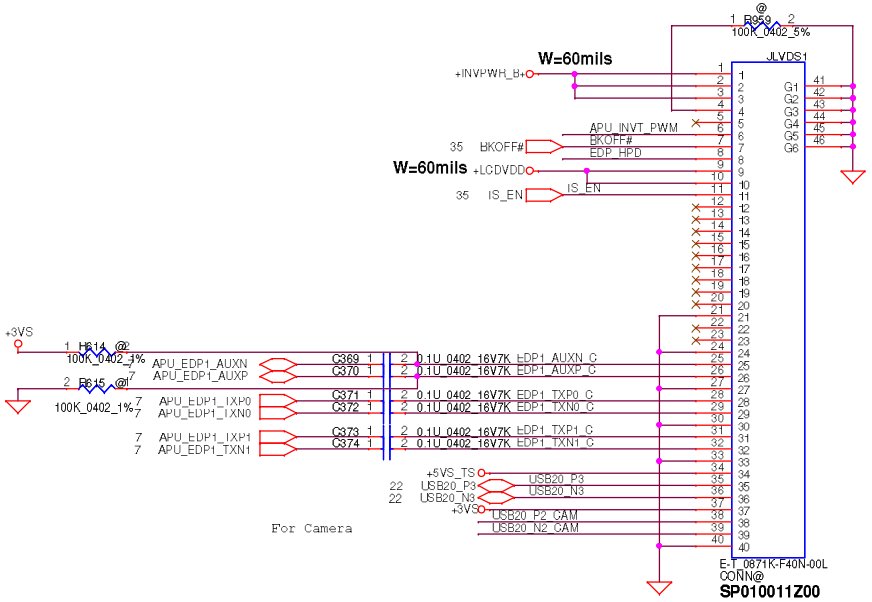


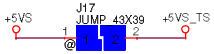


LCD/ LED PANEL Conn.

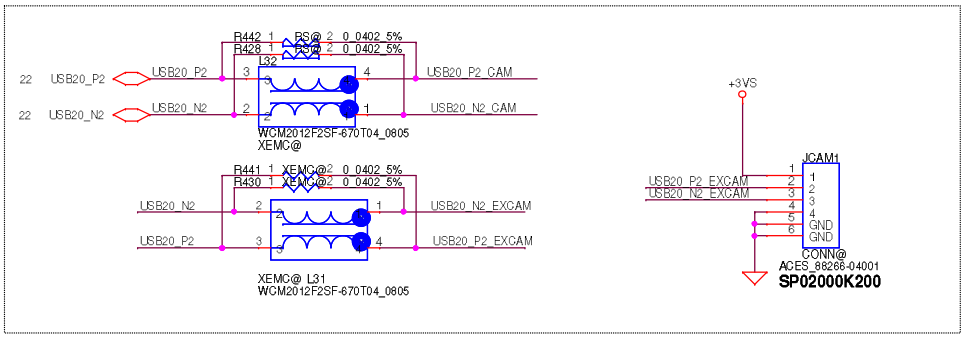








CMOS co-layout 4pin conn & eDP conn



Security Classification	Compal Secret Data		
Issued Date	2012/09/12	Deciphered Date	2012/07/29

Compal Electronics, Inc.	
Title	EDP CONN/Camera/TS
Size: Custom	Document Number: Z5WAK M/B LA-B221P
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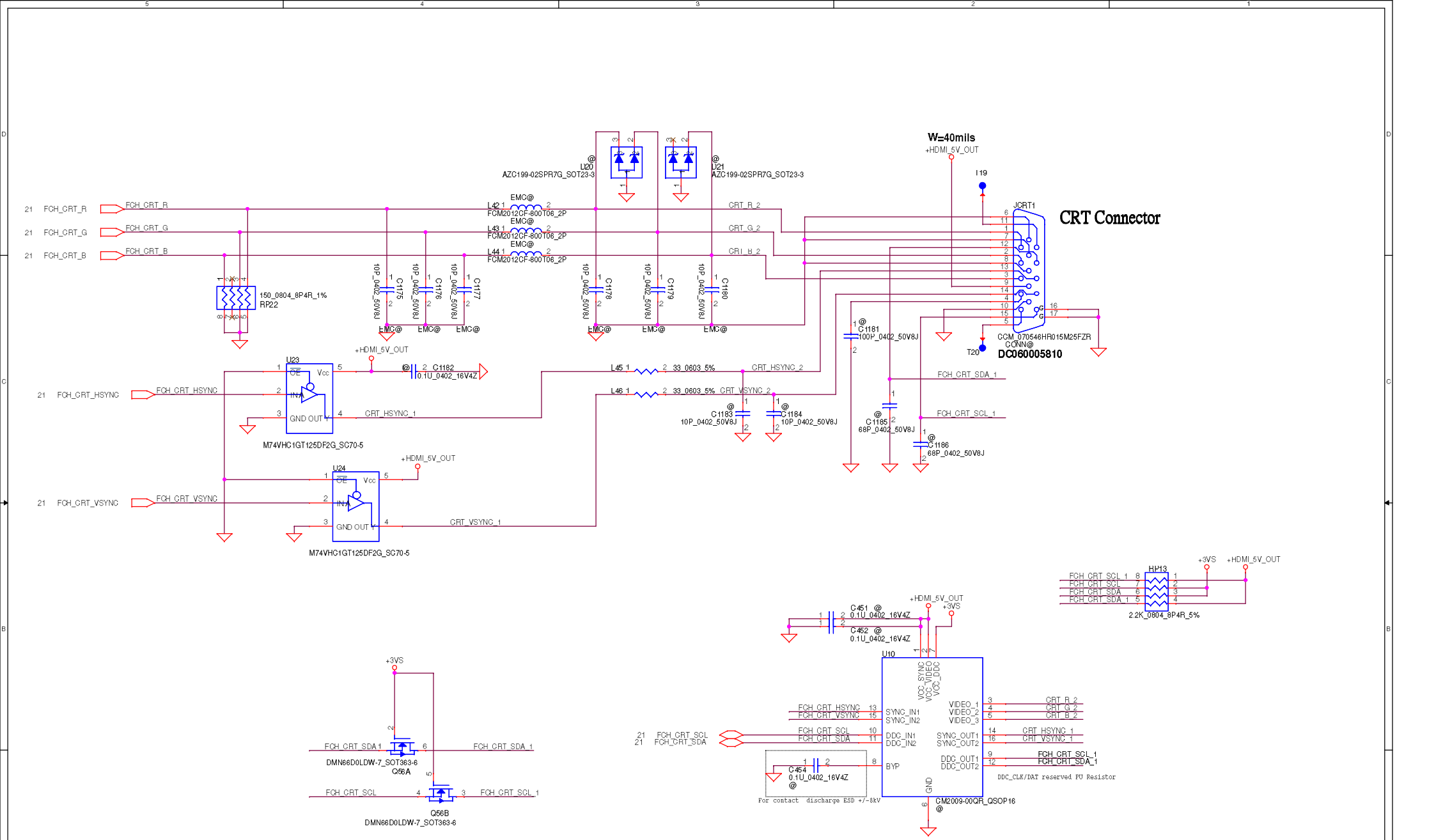
Date: Wednesday, February 12, 2014	Sheet 25 of 52



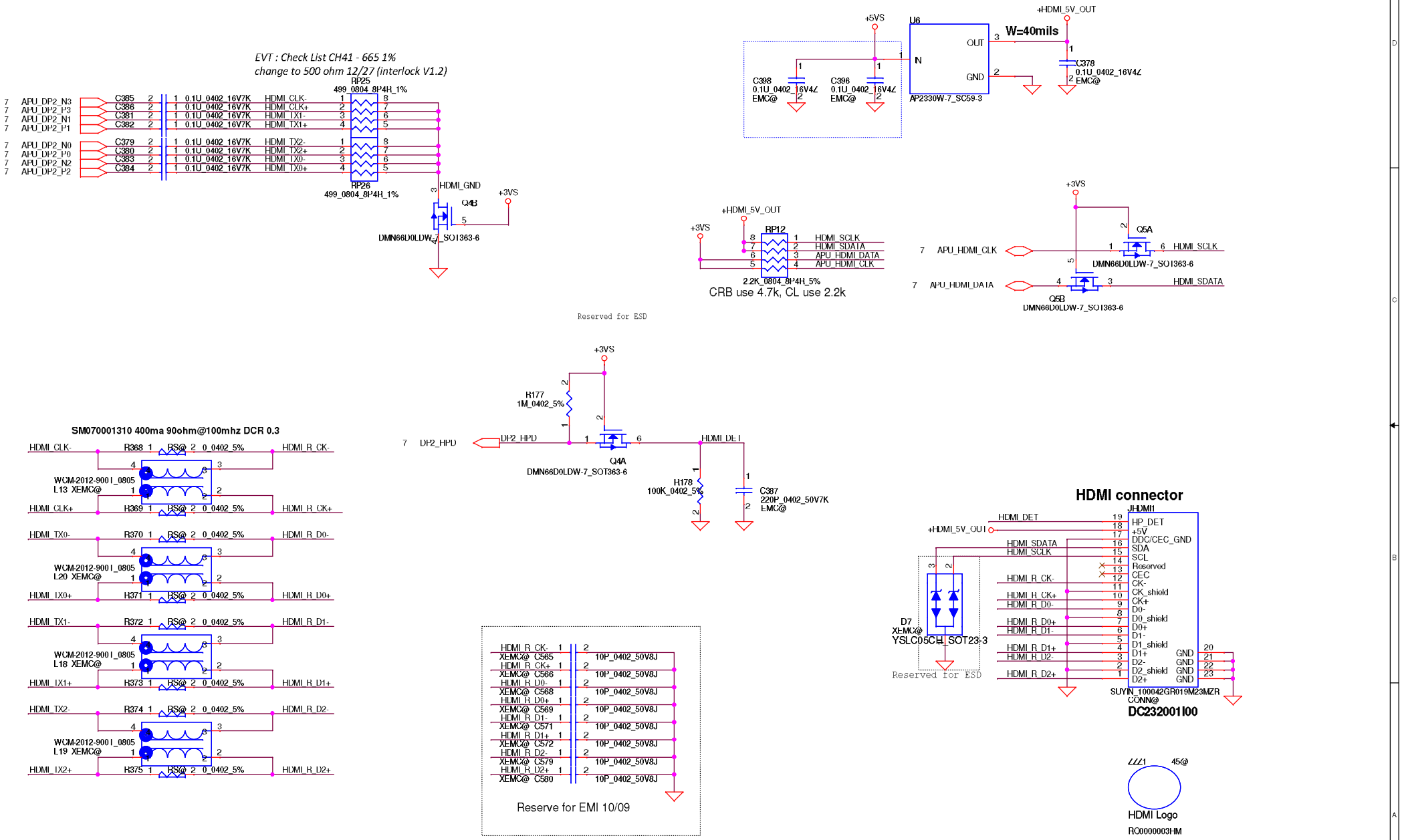
Security Classification	Compal Secret Data		
Issued Date	2012/09/12	Deciphered Date	2012/07/29

Compal Electronics, Inc.

Title: CRT Connector.

Size: Custom | Document Number: Z5WAK M/B LA-B221P | Rev: 0.2

Date: Wednesday, February 12, 2014 | Sheet 26 of 52



Security Classification	Compal Secret Data		
Issued Date	2012/09/12	Deciphered Date	2012/07/29

Compal Electronics, Inc.

Title: HDMI_CONN

Size: Custom | Document Number: Z5WAK M/B LA-B221P | Rev: 02

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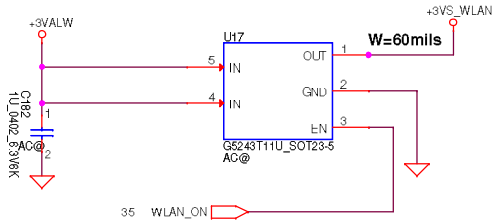
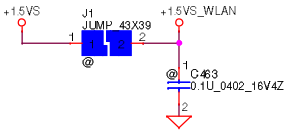
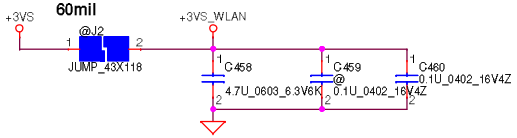
Mini-Express Card for WLAN/WiMAX(Half)

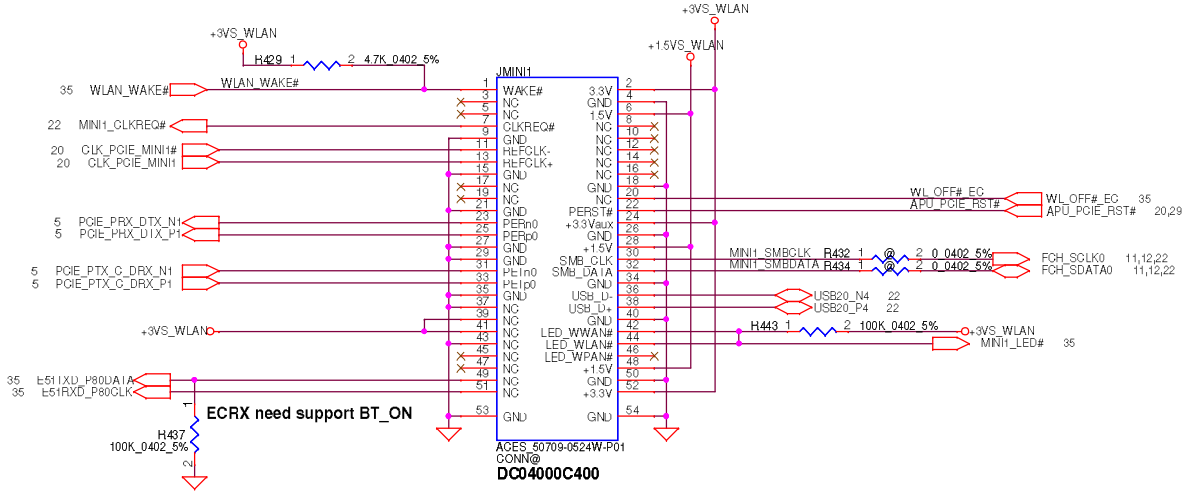






Mini-Express Card(WLAN)

Mini Card Power Rating



Security Classification	Compal Secret Data		
Issued Date	2012/09/12	Deciphered Date	2012/07/29

Compal Electronics, Inc.

Title: MINI Card

Size: Custom | Document Number: Z5WAK M/B LA-B221P | Rev: 0.2

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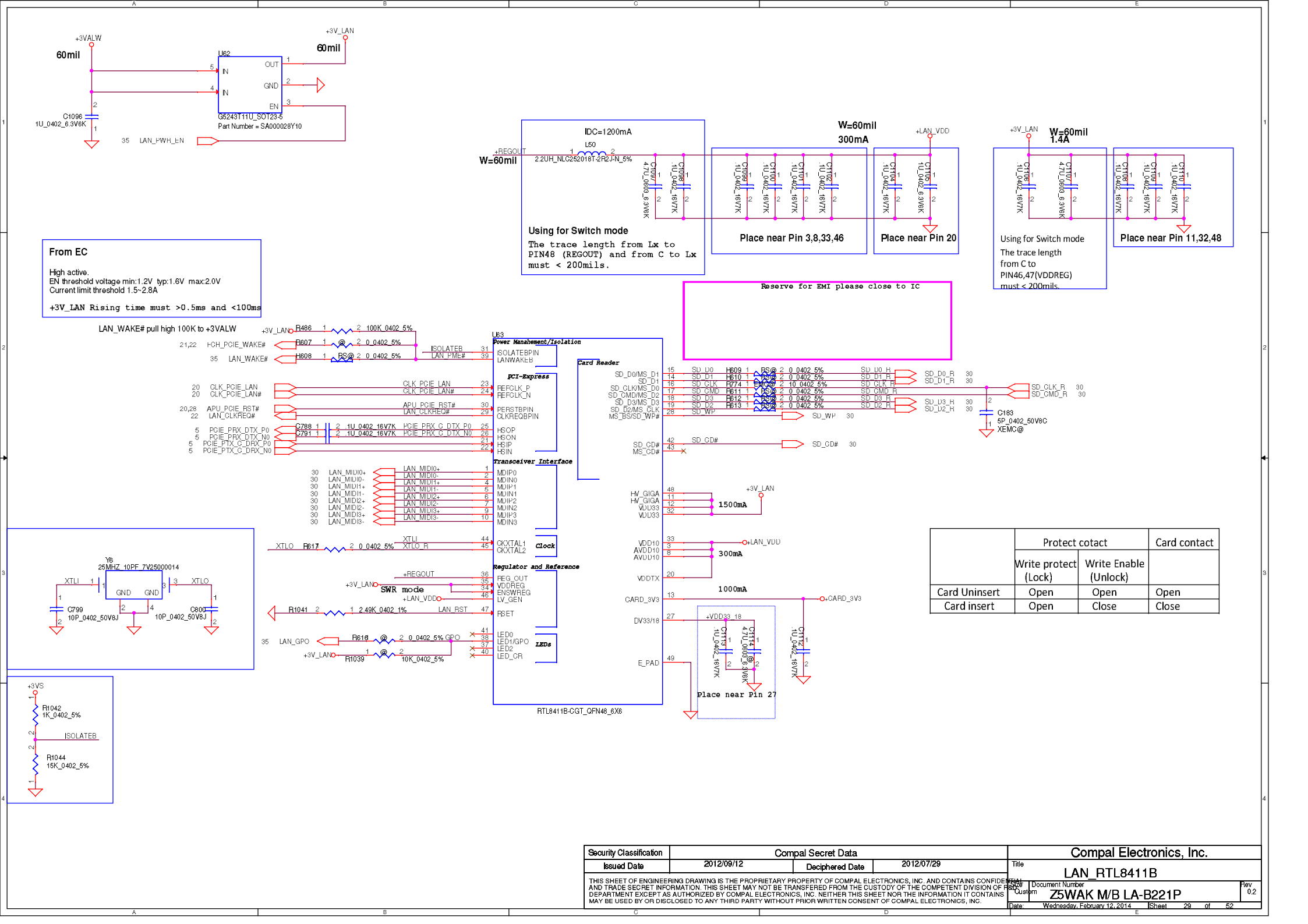

Security Classification	Compal Secret Data		
Issued Date	2012/09/12	Deciphered Date	2012/07/29

Compal Electronics, Inc.

Title: LAN_RTL8411B

Size: Custom | Document Number: Z5WAK M/B LA-B221P | Rev: 0.2

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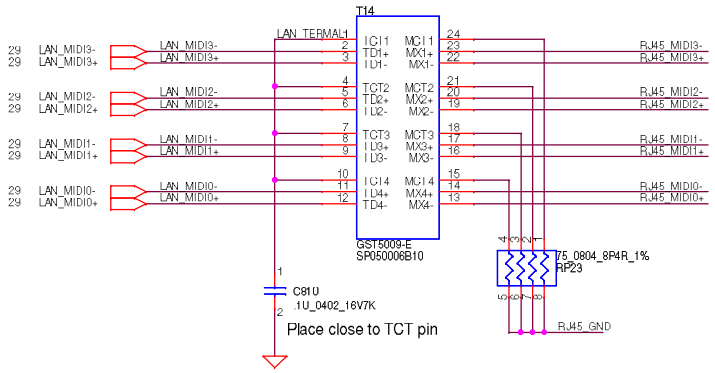
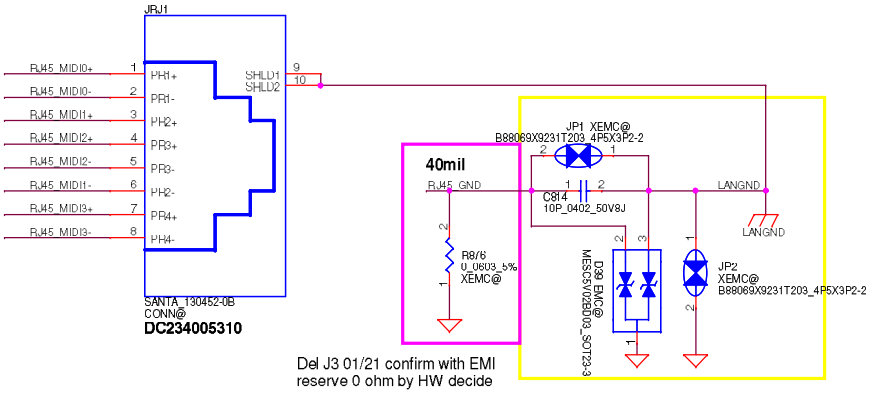
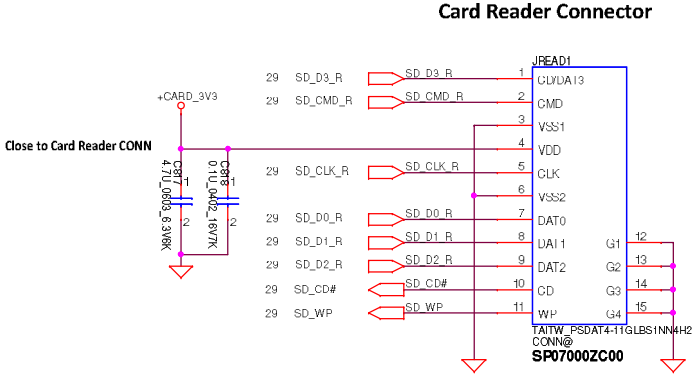


LAN Connector



Card Reader Connector



Security Classification	Compal Secret Data		
Issued Date	2012/09/12	Deciphered Date	2014/01/21

Compal Electronics, Inc.

Title: **Card Reader/LAN Conn**

Size	Document Number	Rev
Custom	Z5WAK M/B LA-B221P	0.2

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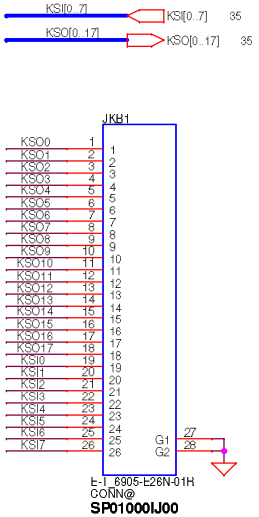
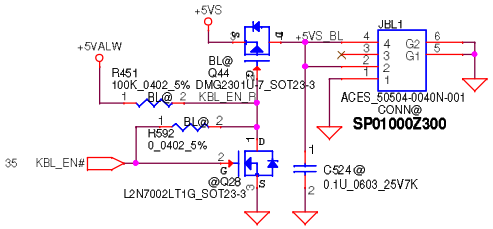
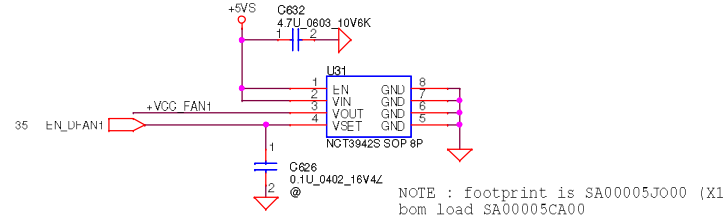
KB Conn.



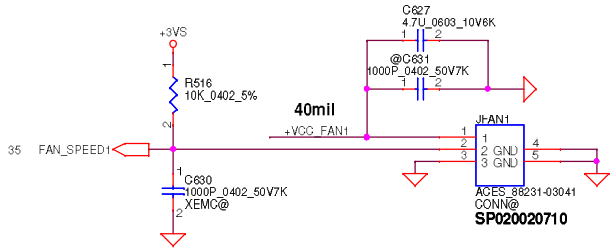
KB BackLight Conn. Reserve

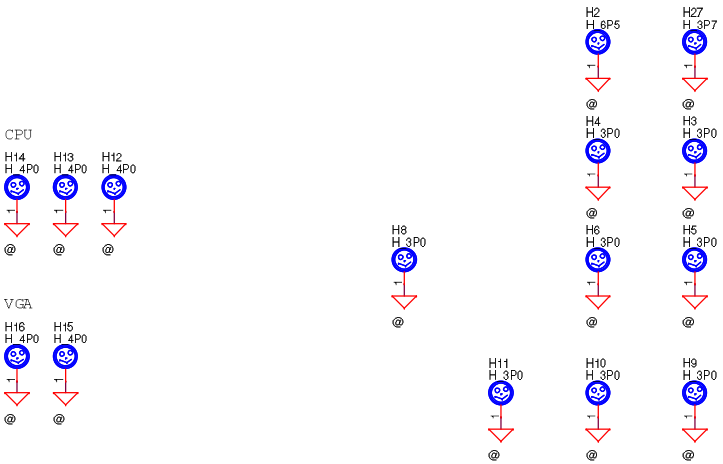


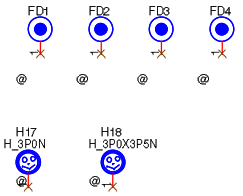
FAN1 Conn



NOTE : footprint is SA00005J000 (X1)
bom load SA00005CA00







Security Classification	Compal Secret Data		
Issued Date	2012/09/12	Deciphered Date	2012/07/29

Compal Electronics, Inc.

Title: FAN/screw/KB/KB BL

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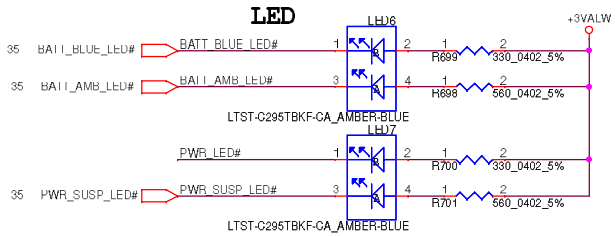
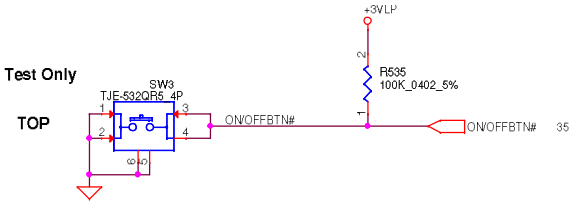
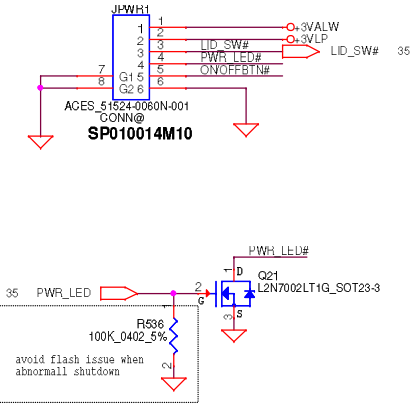
LED



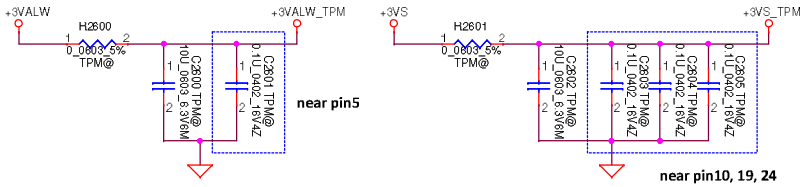
ON/OFF BTN



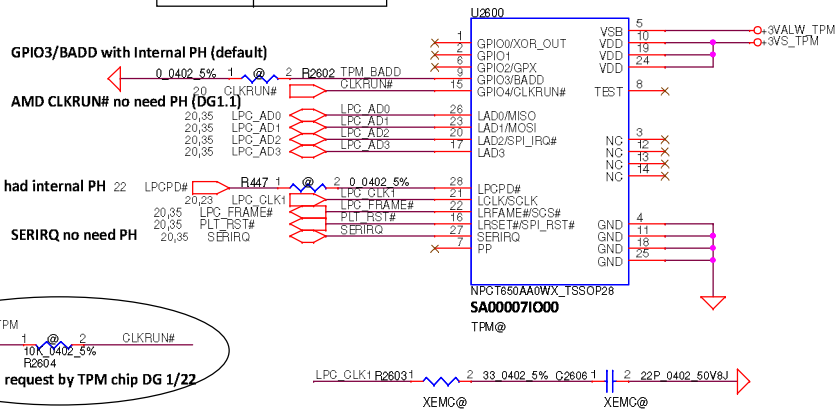
PWR/B



TPM Board



BADD	SELECTION
0	EEh - EFh
* 1	7Eh - 7Fh



G-sensor

Security Classification	Compal Secret Data		
Issued Date	2012/09/12	Deciphered Date	2012/07/29

Compal Electronics, Inc.

Title: PWR B/LED/TPM

Size: Custom | Document Number: Z5WAK M/B LA-B221P | Rev: 0.2

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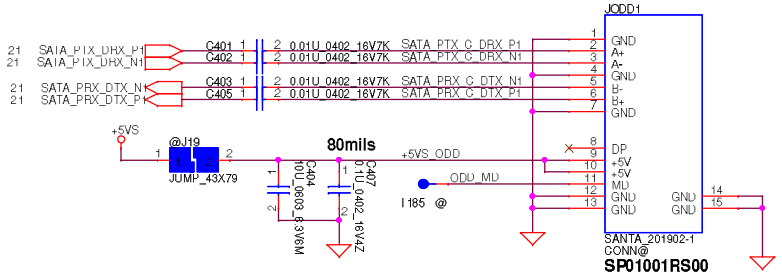
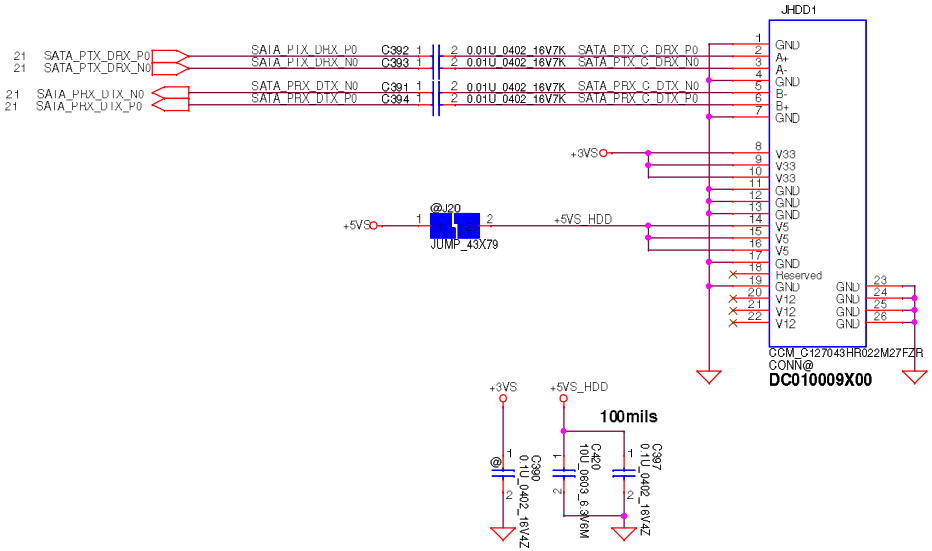
SATA ODD Conn.



SATA HDD Conn.



Security Classification	Compal Secret Data		
Issued Date	2012/09/12	Deciphered Date	2012/07/29

Compal Electronics, Inc.

Title: HDD/ODD Conn

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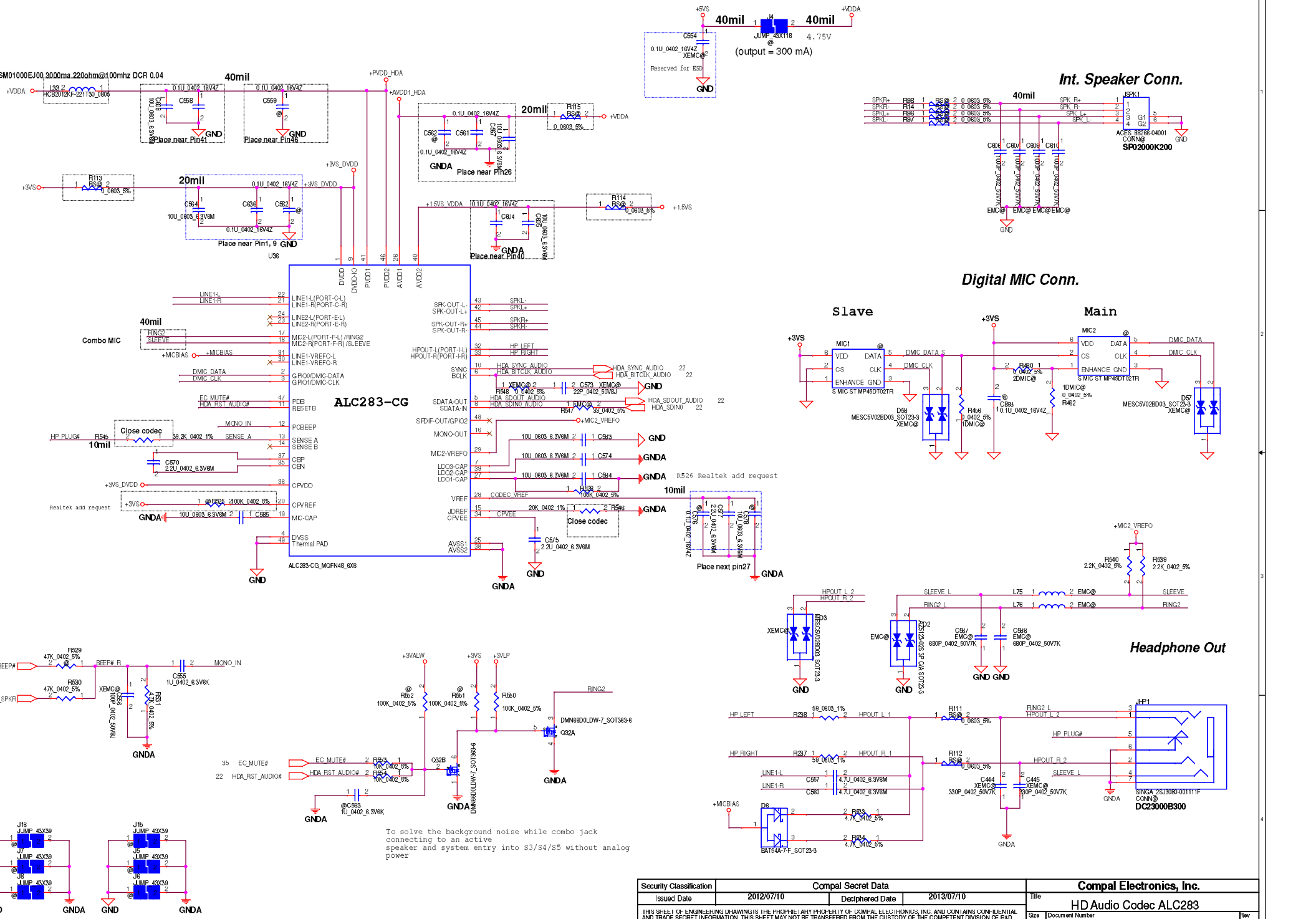
HD Audio Codec



Int. Speaker Conn.

Digital MIC Conn.

Headphone Out

Security Classification	Compal Secret Data		
Issued Date	2012/07/10	Deciphered Date	2013/07/10

Compal Electronics, Inc.			
Title	HD Audio Codec ALC283		
Size	Document Number		Rev
C	Z5WAK M/B LA-B221P		0.2
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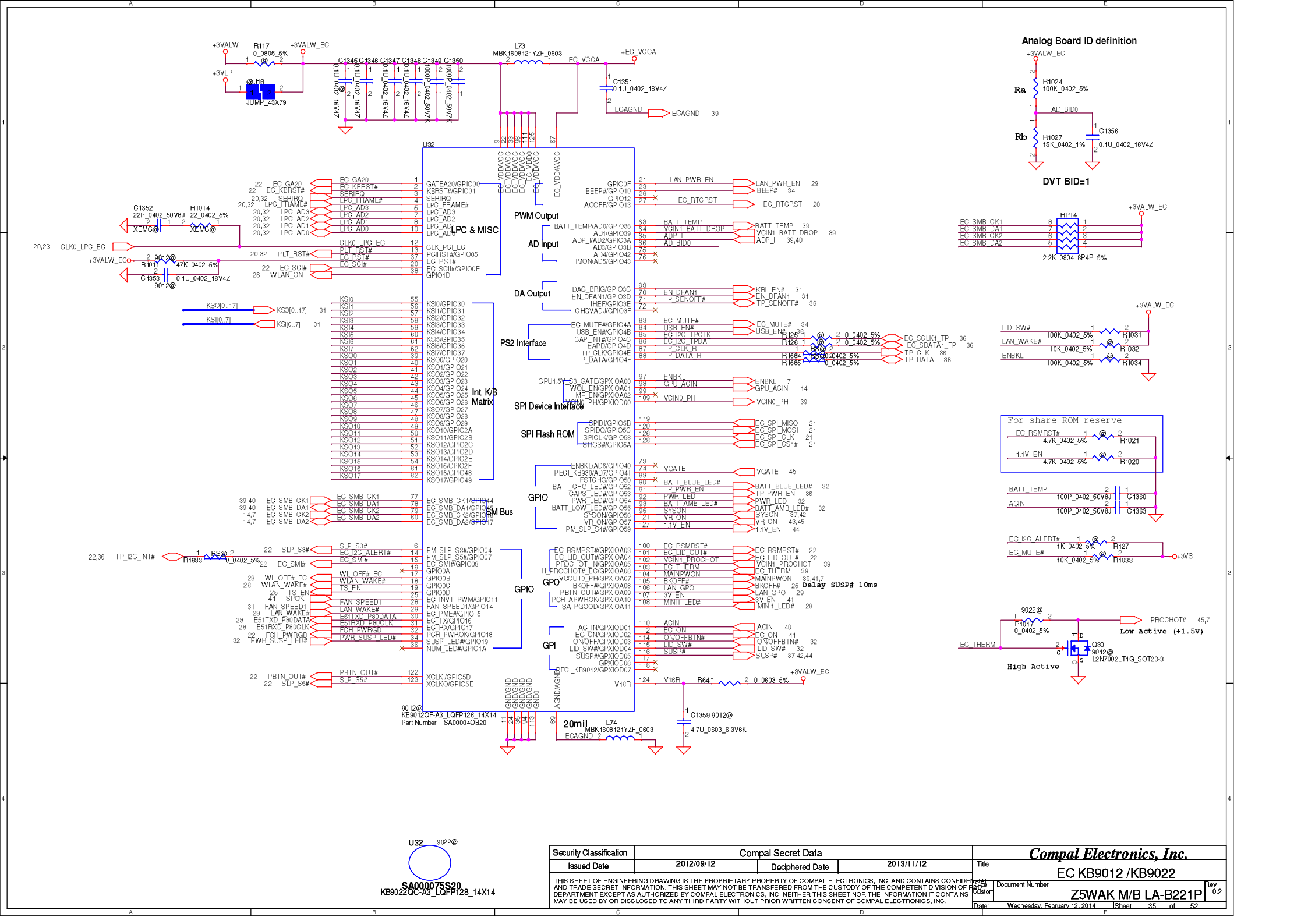

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Issued Date	2012/09/12	Deciphered Date	2013/11/12

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Compal Electronics, Inc.

Title: EC KB9012 /KB9022

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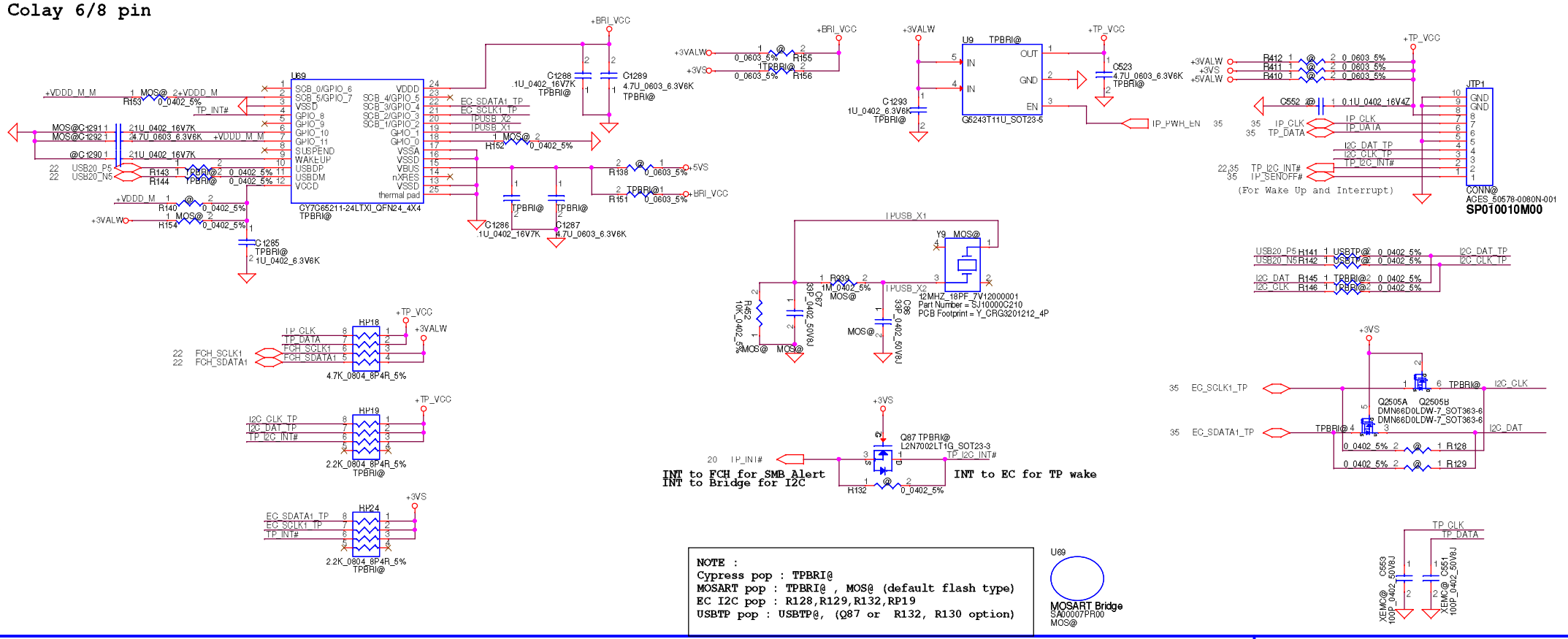
To TP/B Conn.

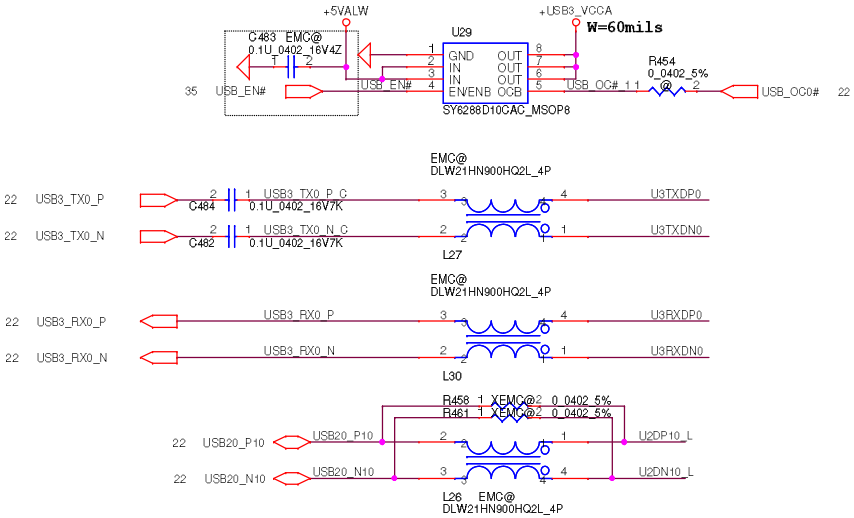
Colay 6/8 pin

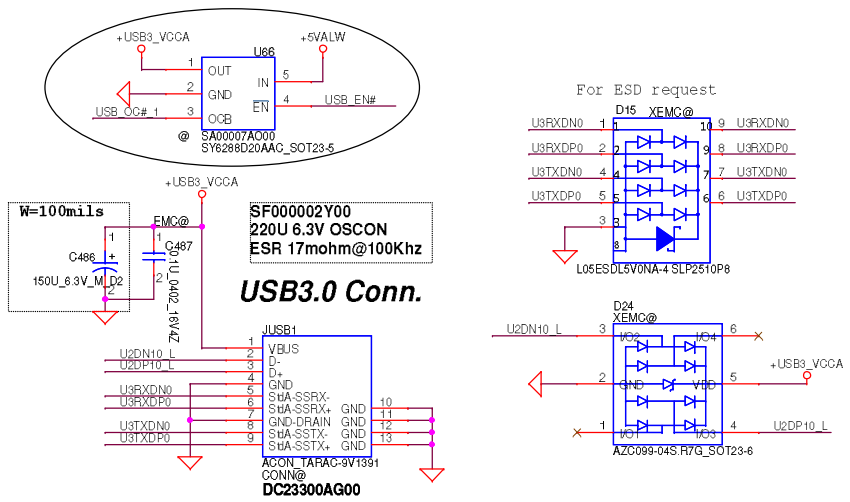


NOTE :
Cypress pop : TPBRI@
MOSART pop : TPBRI@ , MOS@ (default flash type)
EC I2C pop : R128,R129,R132,RP19
USBTP pop : USBTP@, (Q87 or R132, R130 option)

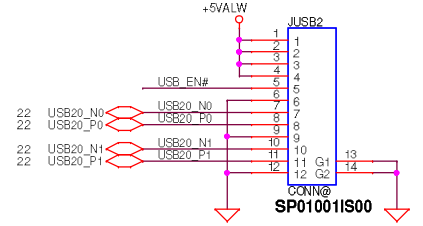
U69
MOSART Bridge
SA00007PR00
MOS@

USB3.0





USB2.0 CONN



Security Classification	Compal Secret Data		
Issued Date	2012/09/12	Deciphered Date	2013/11/12

Title: *USB3.0/ USB2.0 Ports/TP*

Size: Custom | Document Number: Z5WAK M/B LA-B221P | Rev: 0.2

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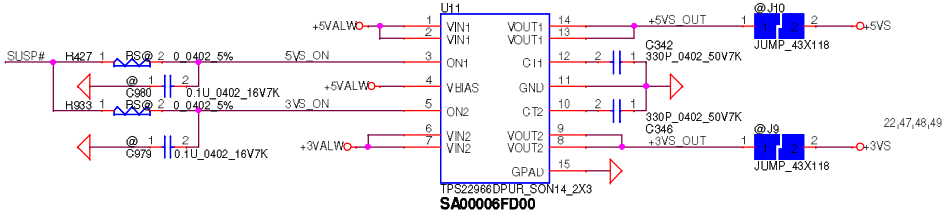
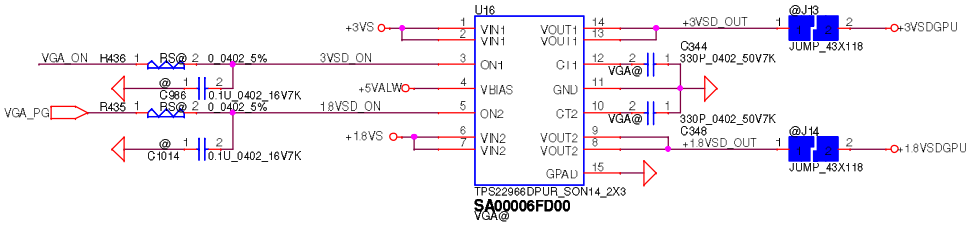
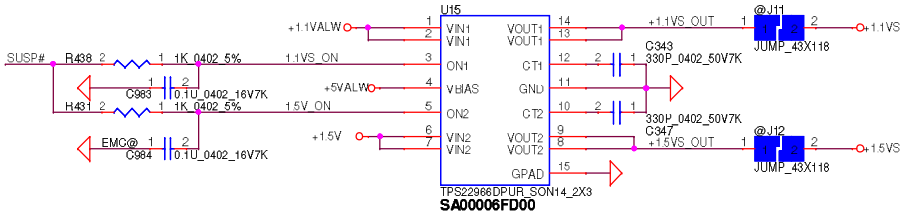
+5VALW to +5VS
+3VALW to +3VS

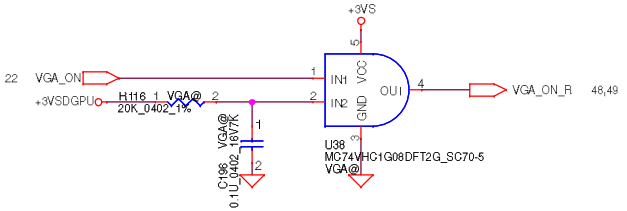


+3VS to +3VSDGPU
+1.8VS to +1.8VSDGPU

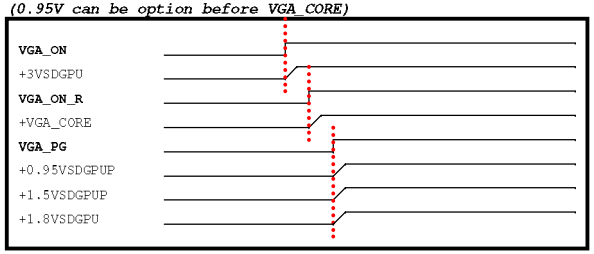


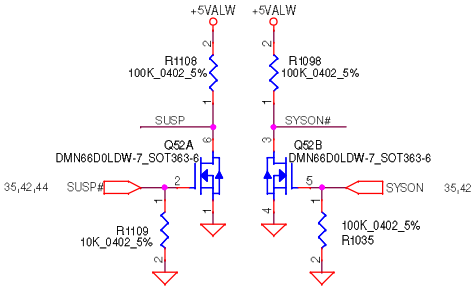
+1.1VALW to +1.1VS
+1.5V to +1.5VS

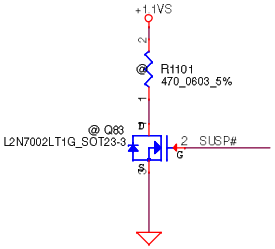


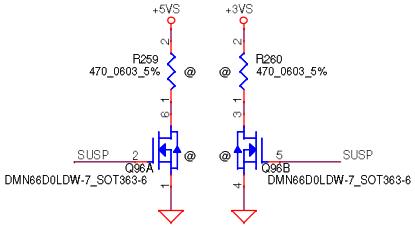


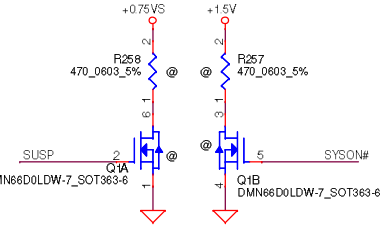
VGA sequence : default same as V5WE2
(0.95V can be option before VGA_CORE)

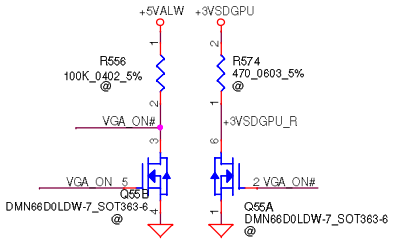


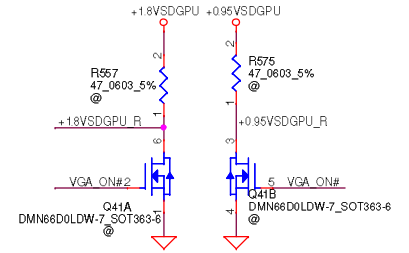


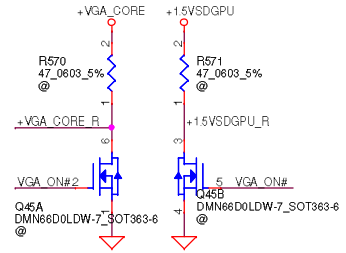












Security Classification	Compal Secret Data		
Issued Date	2012/09/12	Deciphered Date	2013/11/12

Compal Electronics, Inc.

Title: DC Interface

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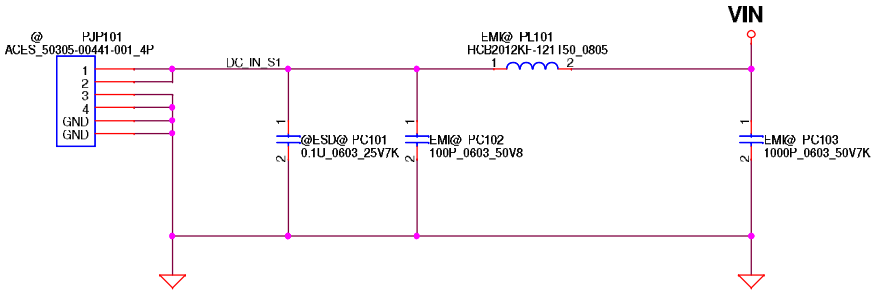

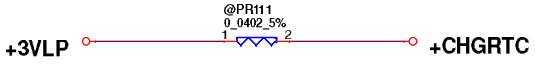

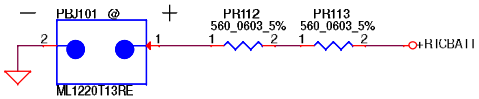

Compal Electronics, Inc.

Title: *DCIN*

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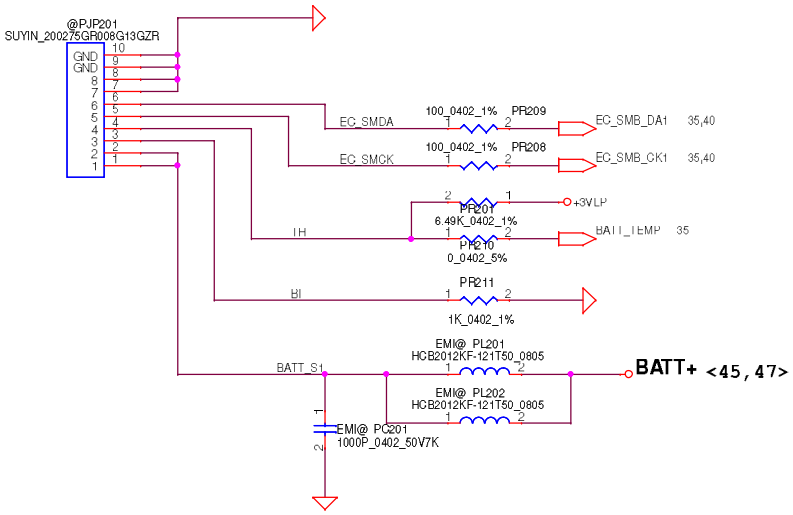
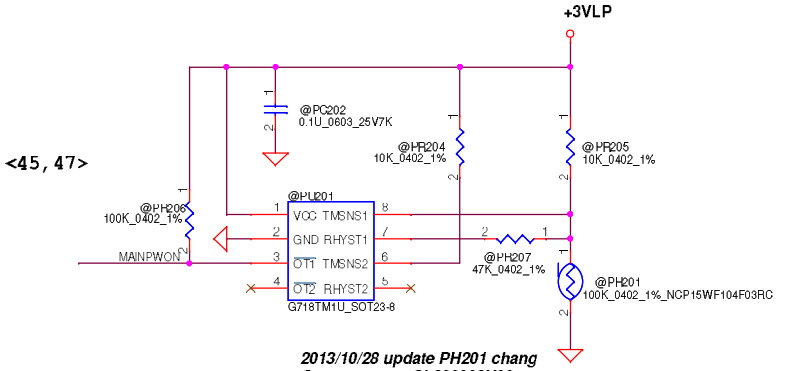




2013/10/28 update PH201 chang
Common part SL200002H00

```
---Battery_pin define---      ---Battery Con_pin define---
PIN1 GND                      PIN8 GND
PIN2 GND                      PIN7 GND
PIN3 SMD                      PIN6 SMD
PIN4 SMC                      PIN5 SMC
PIN5 TS                       PIN4 TS
PIN6 B/I                      PIN3 B/I
PIN7 Batt+                    PIN2 Batt+
PIN8 Batt+                    PIN1 Batt+
```

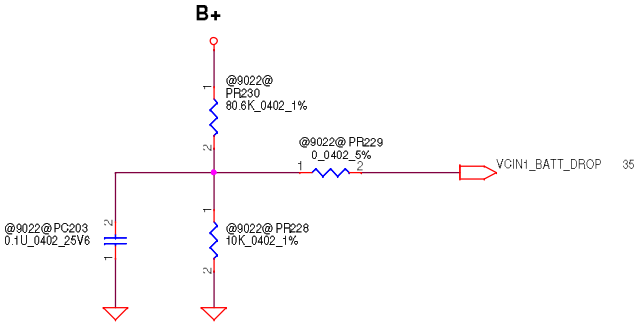
For KB9022 OTP	Active	Recovery
VCIN0_PH(V)	92C, 1V	56C, 2.044V
PH202(ohm)	6.99K	26.03K

For KB9012 sense 20mΩ	Active	Recovery
40W	42.8W, 0.73V	34.4W,0.59V
65W	69.55W, 0.73V	55.9W,0.59V

PH201 under CPU botten side :
CPU thermal protection at 92 degree C (shutdown)
Recovery at 56 degree C

2013/10/02
Add for ENE9022 Battery Voltage drop detection.
Connect to ENE9022 pin64 AD1.

Battery is 3-cell design.
B+=9V

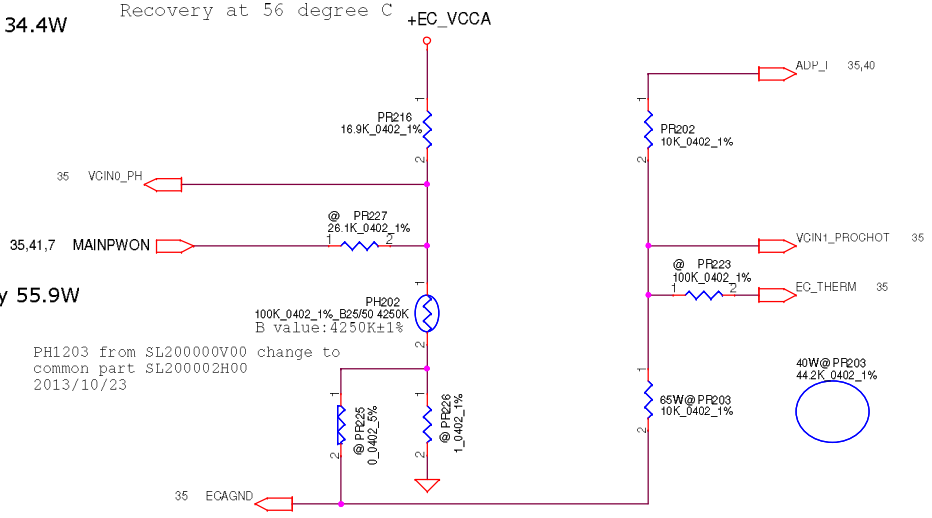


For 40W adapter==>action 42.8W , Recovery 34.4W
42.8W:
Iada= 0~2.253A (42.8W/19V=2.253A)
ADP_I=20*Iada*Rsense
ADP_I=20*2.253*0.02=0.901
34.4W:
Iada= 0~1.811A (34.4W/19V=1.811A)
ADP_I=20*Iada*Rsense
ADP_I=20*1.811*0.02=0.724

CP=40W*0.85=34W

For 65W adapter==>action 69.55W , Recovery 55.9W
69.55W:
Iada= 0~3.661A (69.55W/19V=3.661A)
ADP_I=20*Iada*Rsense
ADP_I=20*3.661*0.02=1.464
55.9W:
Iada= 0~2.942A (55.9W/19V=2.942A)
ADP_I=20*Iada*Rsense
ADP_I=20*2.942*0.02=1.177

CP=65W*0.85=55.25W



PH1203 from SL200000V00 change to
common part SL200002H00
2013/10/23

Security Classification	Compal Secret Data		
Issued Date	2012/07/10	Deciphered Date	2013/10/01

Compal Electronics, Inc.

Title: ***BATTERY CONN / OTP***

Size: Custom | Document Number | Rev: 0.3

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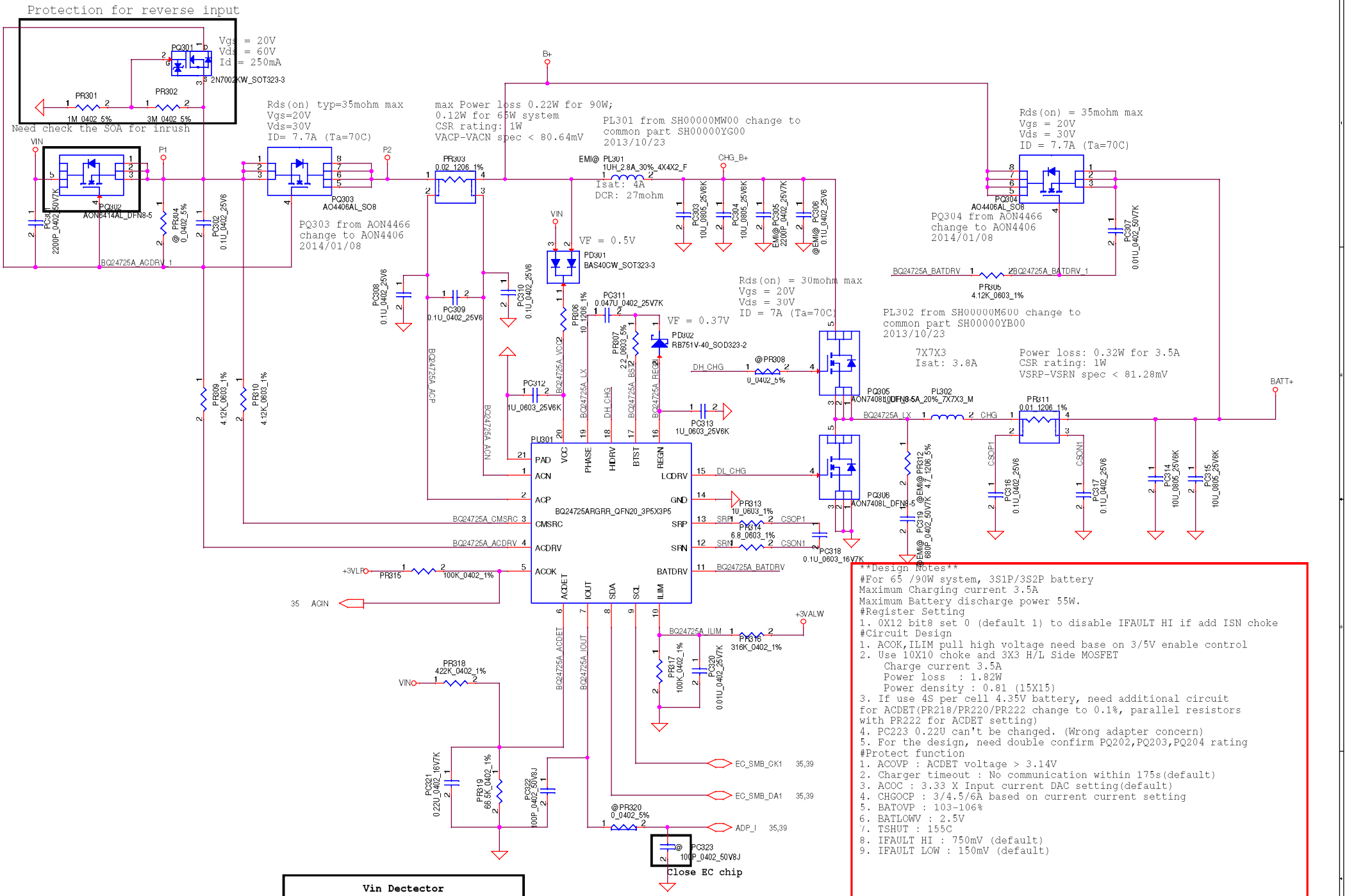


Security Classification	Compal Secret Data		
Issued Date	2014/07/02	Deciphered Date	2013/10/01

Compal Electronics, Inc.			
Title	CHARGER		
Size	Document Number		Rev 0.3
Date: Wednesday, February 12, 2014		Sheet 40 of 53	

Module model information

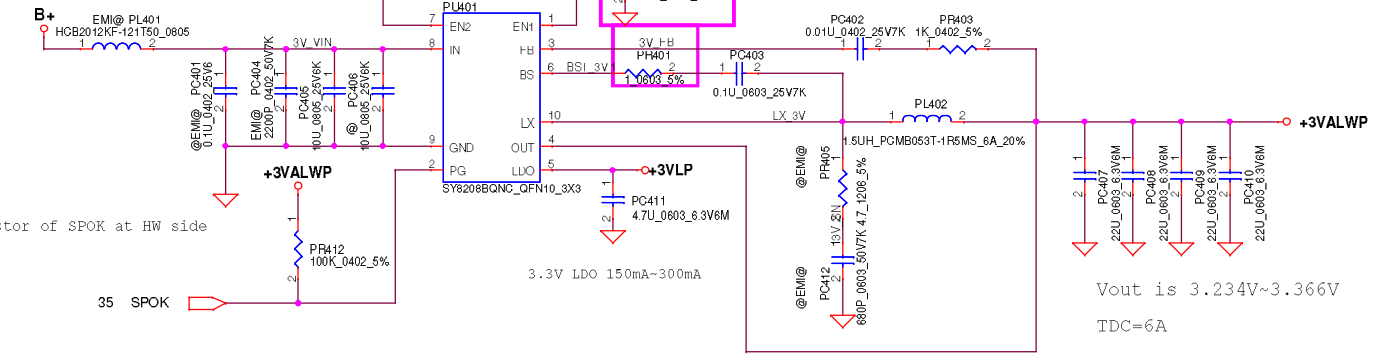
SY8208B_V2.mdd

SY8208C_V2.mdd

PR401 FAE review : change from 2.2_0603_5% to 1_0603_5%

HW request add PR413, and PC428-un-pop

EN1 and EN2 dont't floating

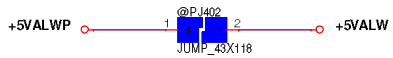


Check pull up resistor of SPOK at HW side

3.3V LDO 150mA~300mA

Vout is 3.234V~3.366V

TDC=6A

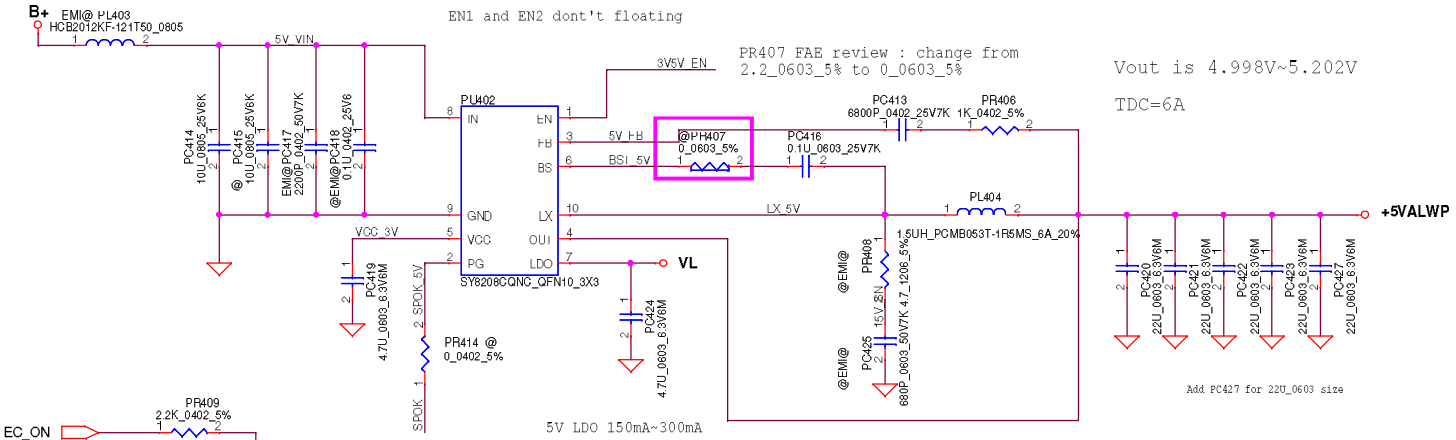


EN1 and EN2 dont't floating

PR407 FAE review : change from 2.2_0603_5% to 0_0603_5%

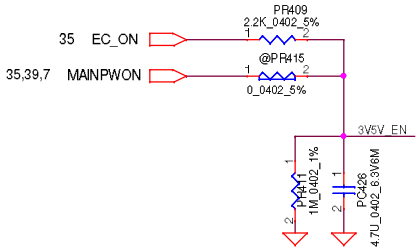
Vout is 4.998V~5.202V

TDC=6A



Add PC427 for 22U_0603 size

5V LDO 150mA~300mA



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2013/10/01

Compal Electronics, Inc.

Title: +3VALW/+5VALW

Size: Custom | Document Number | Rev: 0.3

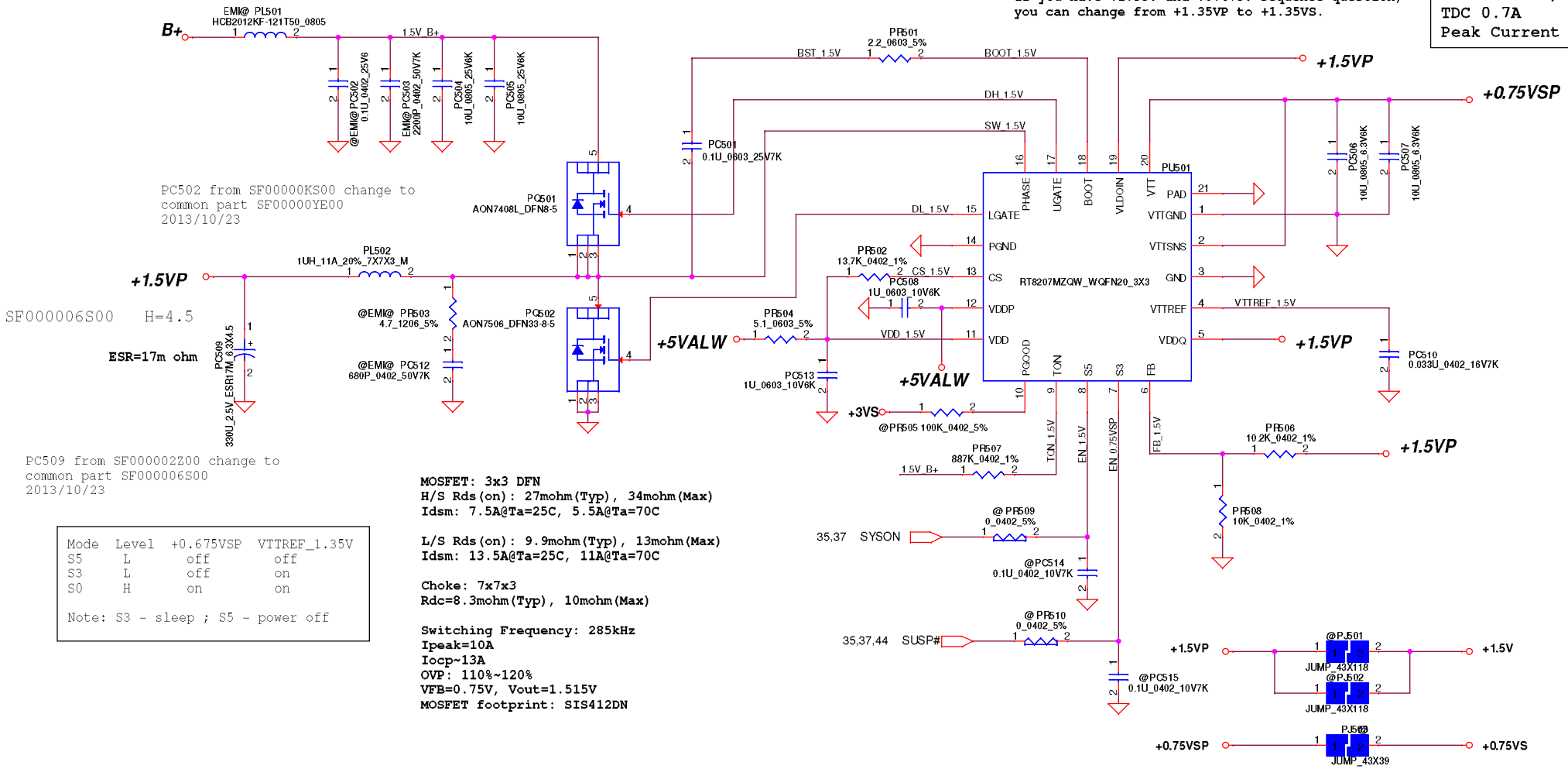
Date: Wednesday, February 12, 2014 | Sheet 41 of 53

Module model information

RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer

Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question,
you can change from +1.35VP to +1.35VS.

0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A



Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

MOSFET: 3x3 DFN
H/S Rds(on): 27mohm(Typ), 34mohm(Max)
Idsm: 7.5A@Ta=25C, 5.5A@Ta=70C

L/S Rds(on): 9.9mohm(Typ), 13mohm(Max)
Idsm: 13.5A@Ta=25C, 11A@Ta=70C

Choke: 7x7x3
Rdc=8.3mohm(Typ), 10mohm(Max)

Switching Frequency: 285kHz
Ipeak=10A
Iocp~13A
OVP: 110%~120%
VFB=0.75V, Vout=1.515V
MOSFET footprint: SIS412DN

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2013/10/01

Compal Electronics, Inc.

Title: +1.5VP/+0.75VSP

Size: Custom | Document Number | Rev: 0.3

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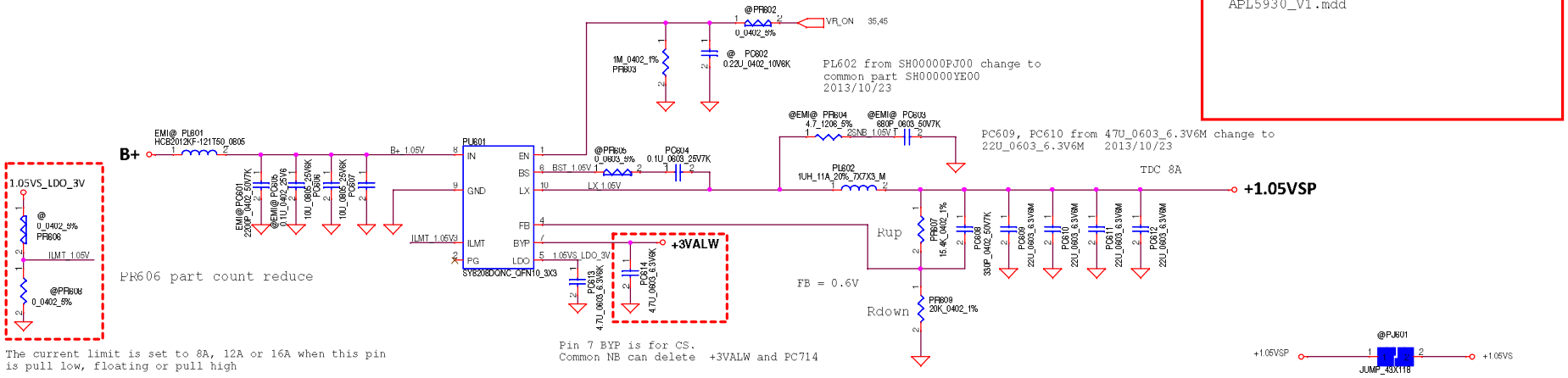
EN pin don't floating
If have pull down resistor at HW side, pls delete PR2

Module model information

SY8208D_V1.mdd
APL5930_V1.mdd

PL602 from SH00000PJ00 change to common part SH00000YE00 2013/10/23

PC609, PC610 from 47U_0603_6.3V6M change to 22U_0603_6.3V6M 2013/10/23



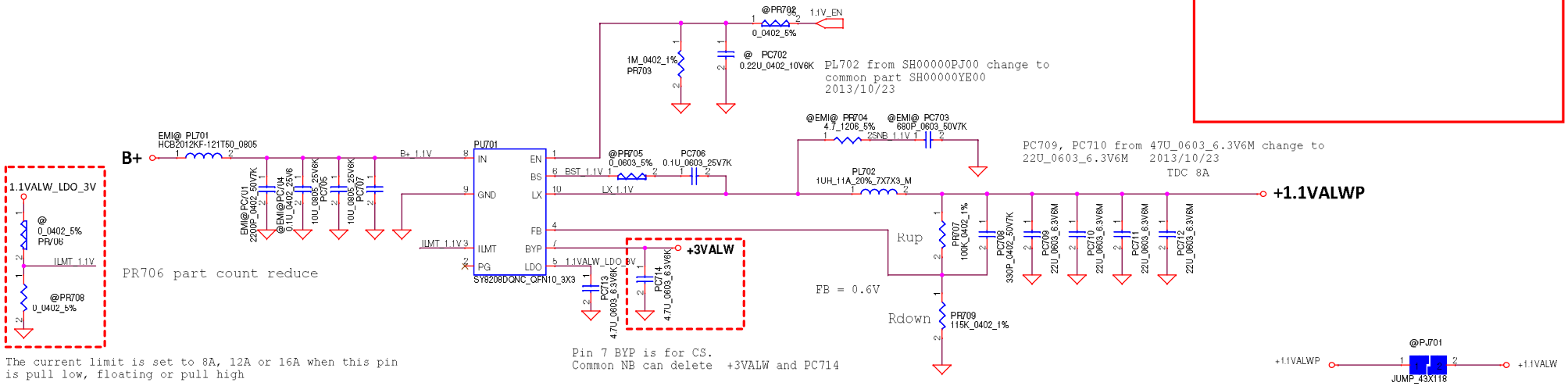
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/08/13	Deciphered Date	2013/10/01

Title	1.05VSP		
Size C	Document Number		Rev 0.3
Date: Wednesday, February 12, 2014		Sheet 43 of 53	

Module model information

SY8208D_V1.mdd

EN pin don't floating
If have pull down resistor at HW side, pls delete PR2

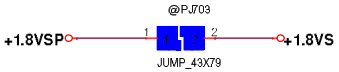


VFB=0.6V
Vout=0.6V* (1+Rup/Rdown)

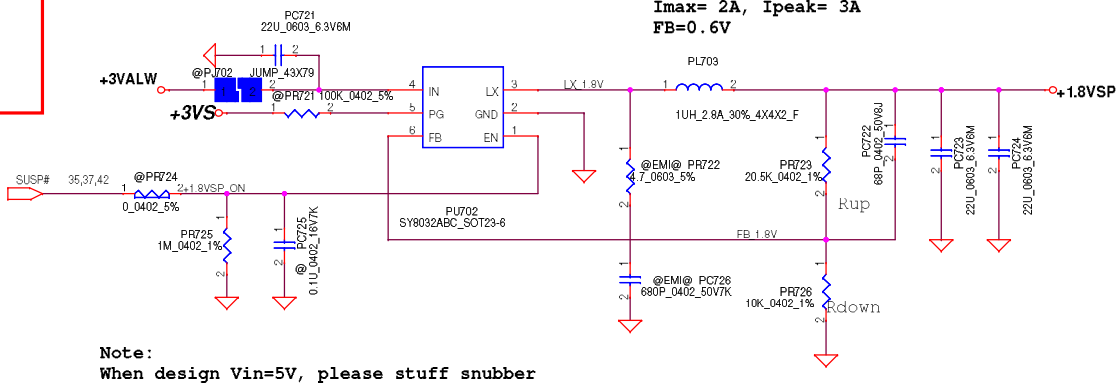
Vout=1.12V

Module model information

SY8032_V2.mdd



Imax= 2A, Ipeak= 3A
FB=0.6V



Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

Vout=0.6V* (1+Rup/Rdown)=1.83V

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2013/10/01

Title: **+1.1VALWP/+1.8VSP**

Size: Custom | Document Number | Rev: 0.3

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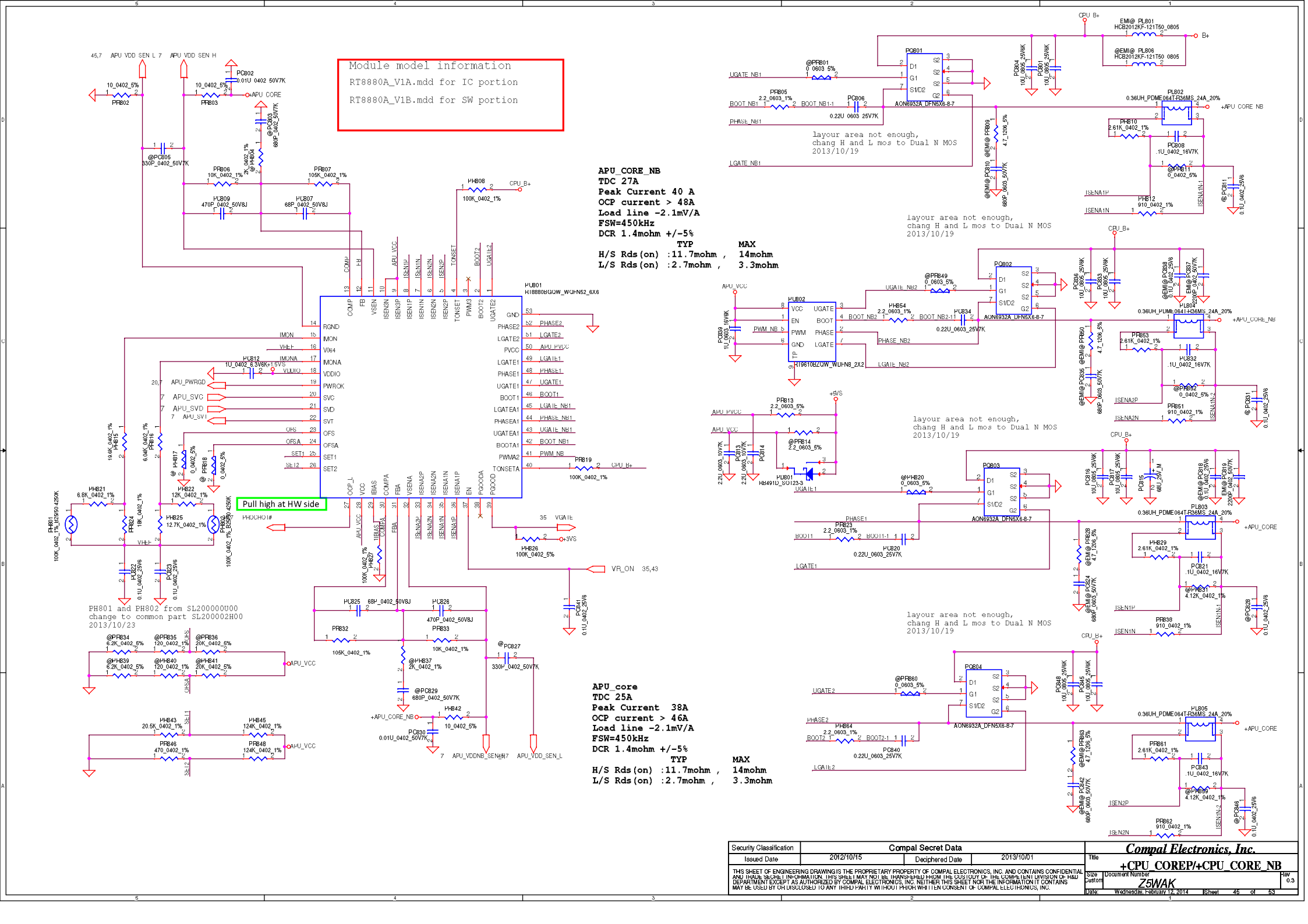
Module model information
RT8880A_V1A.mdd for IC portion
RT8880A_V1B.mdd for SW portion
APU_CORE_NB
TDC 27A
Peak Current 40 A
OCP current > 48A
Load line -2.1mV/A
FSW=450kHz
DCR 1.4mohm +/-5%
TYP MAX
H/S Rds(on) :11.7mohm , 14mohm
L/S Rds(on) :2.7mohm , 3.3mohm
APU_core
TDC 25A
Peak Current 38A
OCP current > 46A
Load line -2.1mV/A
FSW=450kHz
DCR 1.4mohm +/-5%
TYP MAX
H/S Rds(on) :11.7mohm , 14mohm
L/S Rds(on) :2.7mohm , 3.3mohm
Pull high at HW side
PH801 and PH802 from SL200000U00
change to common part SL200002H00
2013/10/23
layour area not enough,
chang H and L mos to Dual N MOS
2013/10/19
RT8880AGQW_WQHN52_6X6
RT9610BZQW_WUHN8_2X2
AON6932A_DFN5X6-8-7
HB491D_SOT23-3
Security Classification
Compal Secret Data
Issued Date
2012/10/15
Deciphered Date
2013/10/01
Compal Electronics, Inc.
+CPU_COREP/+CPU_CORE_NB
Z5WAK
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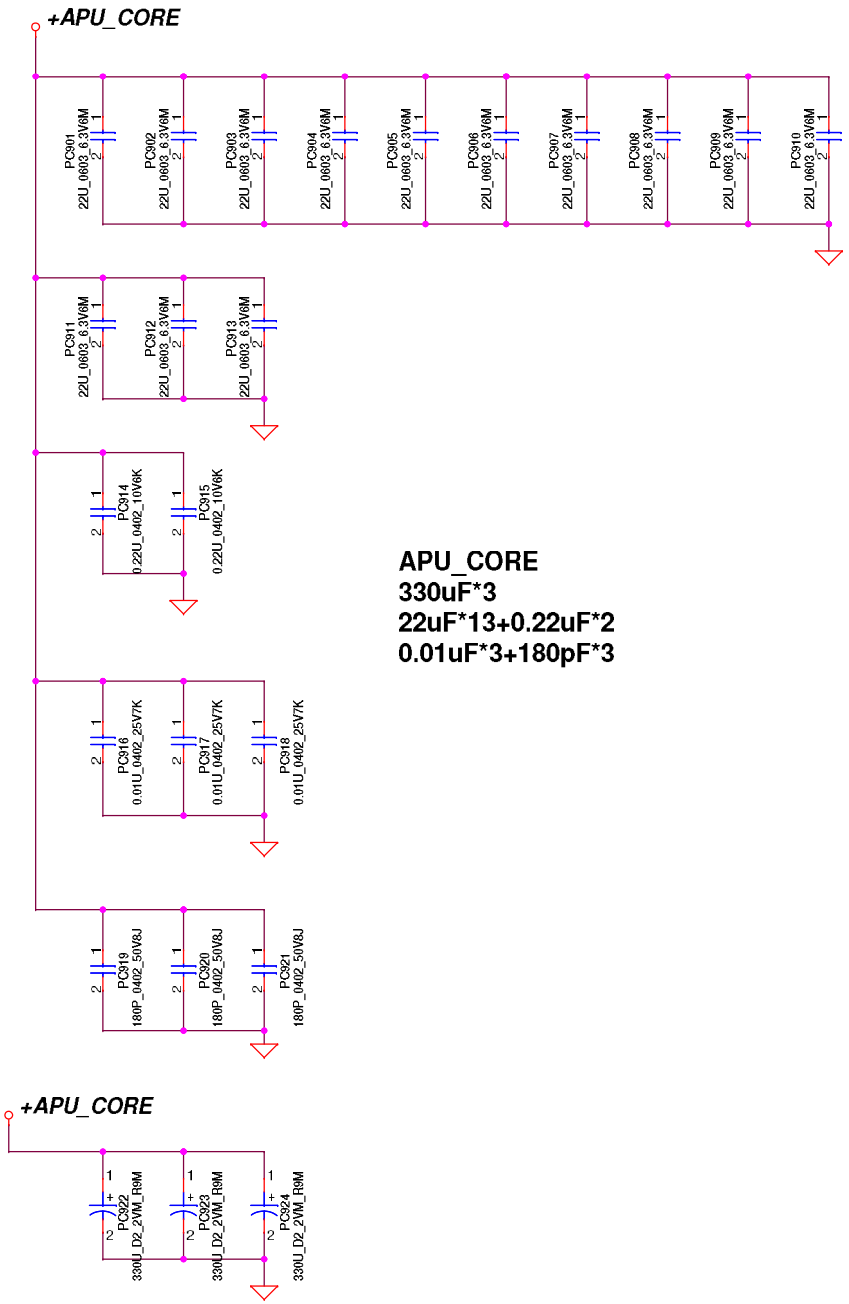
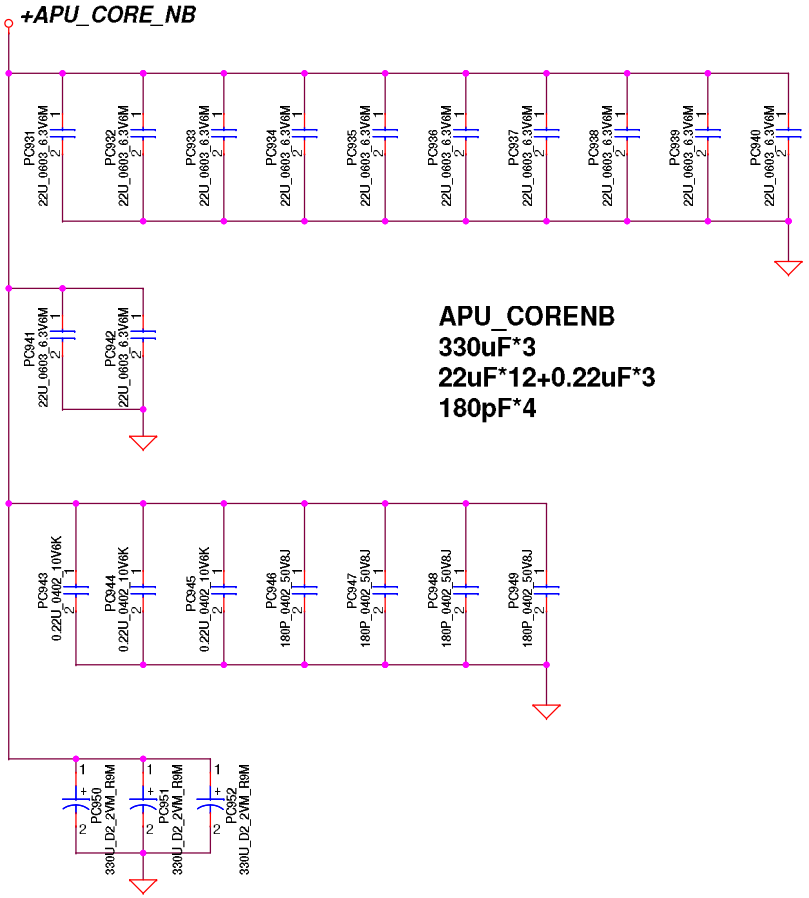
+APU_CORE



+APU_CORE_NB



Security Classification	Compal Secret Data		
Issued Date	2012/10/15	Deciphered Date	2013/10/01

Compal Electronics, Inc.

Title: Processor Decoupling

Size | Document Number: VS50_AMD | Rev: 0.3

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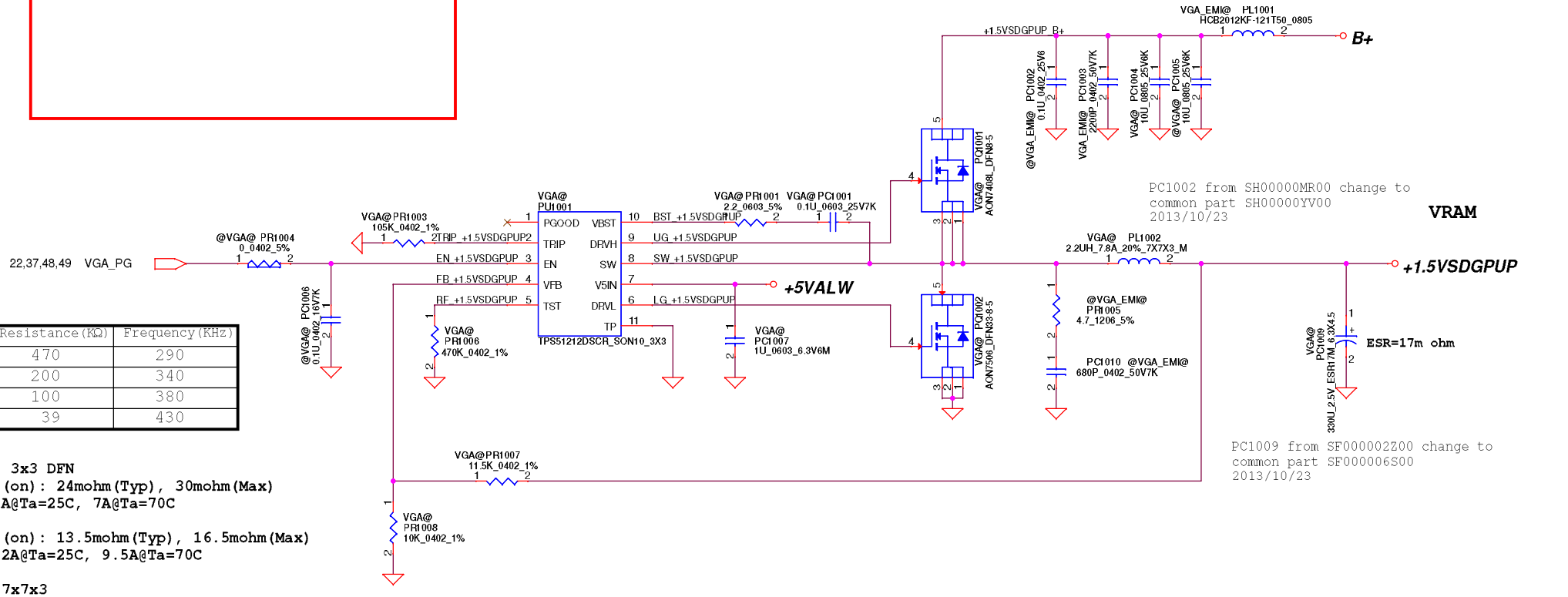
Module model information

'TPS51212_V1.mdd for Single layer
'TPS51212_V2.mdd for Dual layer



PC1002 from SH00000MR00 change to common part SH00000YV00
2013/10/23

VRAM

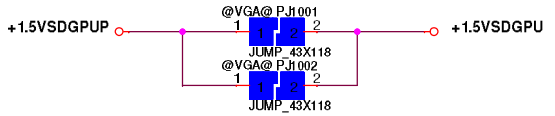
PC1009 from SF000002Z00 change to common part SF000006S00
2013/10/23

Resistance(KΩ)	Frequency(KHz)
470	290
200	340
100	380
39	430

MOSFET: 3x3 DFN
H/S Rds(on): 24mohm(Typ), 30mohm(Max)
Id: 8.7A@Ta=25C, 7A@Ta=70C

L/S Rds(on): 13.5mohm(Typ), 16.5mohm(Max)
Idsm: 12A@Ta=25C, 9.5A@Ta=70C

Choke: 7x7x3
Rdc=15.5mohm +/-15%



+1.2V

Switching Frequency: 290kHz
Imax=8A
OCP~10.5A
OVP: 120%~130%
VFB=0.704V, Vout=1.207V

+1.05V

Switching Frequency: 290kHz
Imax=5.4A
Ipeak=6.5A
Iocp=7.8A
OVP: 120%~130%
VFB=0.704V, Vout=1.055V

+1.5V

Switching Frequency: 290kHz
Imax=8A
OCP~10.5A
OVP: 120%~130%
VFB=0.704V, Vout=1.514V

Vout	PR1007	PR1008	PR1003
+1.2V	7.15K	10k	105K
+1.05V	4.99k	10k	93.1k
+1.5V	11.5K	10k	105K

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/07/29	Deciphered Date	Title: 1.5VSDGPUP

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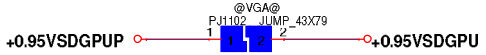
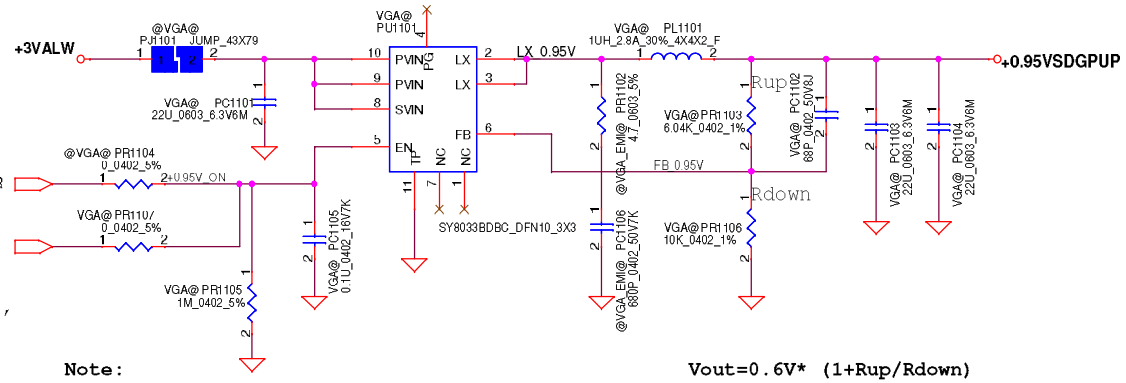
Module model information

SY8033_V1.mdd



FB=0.6V
Note:Iload(max)=3.5A

PC1101 from SH00000MN00 change to
common part SH00000YG00
2013/10/23



HW request Add PR1107,
and unpop PR1104

Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

Vout=0.6V* (1+Rup/Rdown)

Security Classification	Compal Secret Data		
Issued Date	2013/01/02	Deciphered Date	2013/10/01

Compal Electronics, Inc.

Title: **0.95VSDGPU**

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GPI021	GPI029	GPI030	GPI020	GPI015	
VID5	VID4	VID3	VID2	VID1	VDDC
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V
1	1	1	0	1	0.775V

Vboot

	AMD MARS series			LP: DDR3 Pro/XT/XTX: GDDR5	AMD SUN series		UL: DDR3 Pro/XT/XTX: GDDR5	Description
GPU	MARS XTX	MARS XT	MARS PRO	MARS LP	SUN UL	SUN PRO	SUN XT	NA
VDDC	0.775~1.175V	0.775~1.125V	0.775~1.050V	0.775~1.000V	0.775~1.125V	0.800~1.075V	0.800~1.150V	NA
TDC	32A (TDC)	25A (TDC)	21A (TDC)	17A (TDC)	16A (TDC)	19A (TDC)	25A (TDC)	NA
EDC	48A	37.5A	31.5A	26A	24A	28.5A	37.5A	NA
OCP	57.6A	45A	37.8A	31.2A	28.8A	34.2A	45A	NA
Vboot	0.85V	0.85V	0.85V	0.85V	0.9V	0.9V	0.9V	NA
Load line	1mohm	1mohm	1mohm	--------	--------	--------	1mohm	NA
Ri PR1248	1.13K Ohm	887 Ohm	750 Ohm	--------	--------	--------	887 Ohm	for OCP and LoadLine Setting
Rdroop PR1229	1.43K Ohm	1.13K Ohm	953 Ohm	--------	--------	--------	1.13K Ohm	for LoadLine Setting
PR1233	187K Ohm	147K Ohm	124K Ohm	--------	--------	--------	147K Ohm	for Compensation
PR1236	51.1K Ohm	51.1K Ohm	51.1K Ohm	--------	--------	--------	51.1K Ohm	for Positive offset

Remark: MARS LP/ SUN UL/ SUN PRO
don't use this 2-phase solution

H-side MOS:TPCA8065
Rds(on):
9.4mohm@Vgs=10V
11.7mohm@Vgs=4.5V
Id :16A@Ta=25 degC

L-side MOS:TPCA8057
Rds(on):
2.0mohm@Vgs=10V
2.6~3.2mohm@Vgs=4.5V
Id :42A@Ta=25 degC

Choke: 0.22uH (Size:7*7*4)
Rdc=0.98mohm +-5%
Heat Rating Current=28A
Saturation Current=28A

Remark:

1. PWM3 (Pin24) tie to 5V & CLK# (Pin40) external pull high
   => 2 phase GPU VR config
   PWM3 (Pin24) tie to 5V & CLK# (Pin40) tie to GND or floating
   => 2 phase GPU VR config

2. When 2 Phase GPU config
   a. DPSLPVR (Pin39)=0 PSI# (Pin2)=0
      =>1 phase CCM operation mode
   b. DPSLPVR (Pin39)=0 PSI# (Pin2)=1
      =>2 phase CCM operation mode
   c. DPSLPVR (Pin39)=1 PSI# (Pin2)=0 or 1
      =>1 phase DE operation mode

3. Rbias=147K =>overshoot reduction function disable
   Rbias=47k =>overshoot reduction function enable

4. Thermal throttling:
   Protect: (6.98K+Rth)*60uA=1.2V
   => Rth=13.02K
   =>Tp=110C (+-3C)
   Recovery:(6.98K+Rth)*56uA=1.24V
   => Rth=15.16K
   => Tr=105C (+-3C) 14 GPU_DPRSLPVR

PR1226=6.98K	PR1226=1.5K
protect T 110C +-3	protect T 100C +-3
Recovery I 105C +-3	Recovery I 96C +-3

5. Switching frequency set :
   Rfset(kohm)=[period(us)-0.29]*2.65
   =5.9Kohm
   fsw=1/period(us)=400KHZ

PH1201 from SL200000J00 change to common part SL200002E00 2013/10/23

Layout Note:
PH1201 should place near phase1 H-side MOS

Vboot regulation

Module model information:
ISL62883C_V1A for IC
ISL62883C_V1B for SW Choke/MOS on BTN
ISL62883C_V2B for SW Choke on BTN, MOS on TOP

+VGA_CORE
TDC 28A
Peak Current 40 A
OCP current > 48A
Load line 1mohm
FSW=400kHz
DCR 0.98mohm +/-5%

	TYP	MAX
H/S Rds(on)	:11.7mohm ,	14.5mohm
L/S Rds(on)	:2.6mohm ,	3.2mohm

PR1230 Pop:
for Loadline disable
PR1230 @:
for Loadline enable
and LL=1mohm

Transient response :
Rntcnet=(Rntcs+Rntc)*Rp/(Rntcs+Rntc+Rp)
Cn=L*(Rntcnet+Rsum/N)/[Rntcnet*DCR*(Rsum/N)]
N is the number of phases

Rdroop=Io*LL/Idroop

Layout Note:
PH1202 should place near Phase1 Choke

PH1202 from SL200000W00 change to common part SL200002F00 2013/10/23

Security Classification	Compal Secret Data		
Issued Date	2013/01/03	Deciphered Date	2013/10/01

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Compal Electronics, Inc.

Title: VGA_CORE

Size: Document Number: Rev: 0.3

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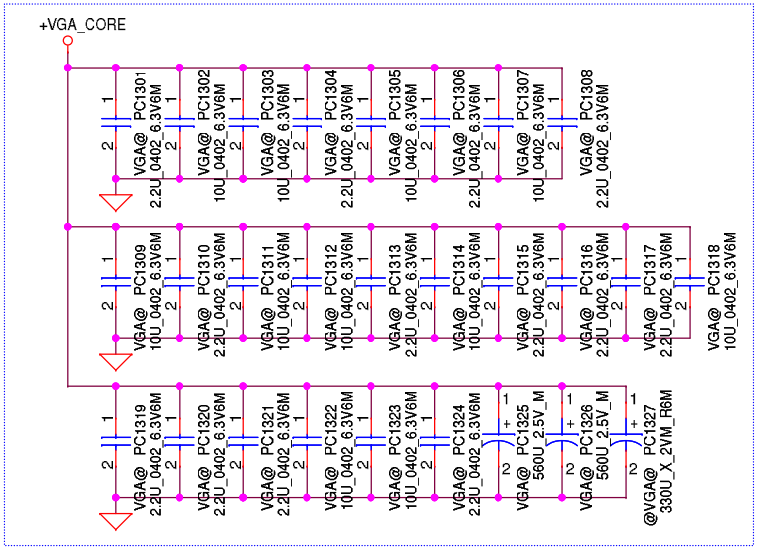
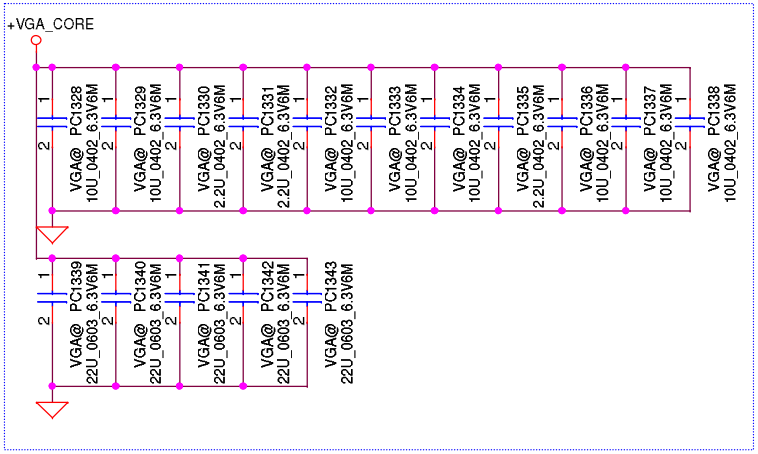


AMD MARS
GPU_CORE
560uF*2+330uF*1
10uF*11+2.2uF*13



AMD MARS
meet ripple
22uF*5+10uF*8+2.2uF*3

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Title: *VGA_CORE CAP*

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		layout area not enought		APU_CORE	PQ801;PQ803;PQ807;PQ808 FDMS7698 and PQ802;PQ804;PQ806;PQ809 MDU1511 change to Dual N AON6932A	10/09	EVT
2		EMI bead "HCB2012KF-121T50_0805" derating 5A, need 2pcs for APU_CORE and APU_CORENB		APU_CORE	Add PL806 EMI bead "HCB2012KF-121T50_0805" from 1pcs to 2pcs at B+, for APU_CORE and APU_CORENB	10/15	EVT
3		RT8880A FAE review		APU_CORE	PR813 from 0402 change to 0603, delete PR844, PR847	10/16	EVT
4		HW: EC share ROM, modify 3VALW and 1.1VALW enable net-name		3VALW 5VALW	change 3VALW enable net name from 3V5V_EN to 3V_EN change 1.1VALW enable net name from SUSP# to 1.1V_EN	10/17	EVT
5		Choke, OS-CON cap, Thermistor change to standard part				10/23	EVT
6		RT8880A vendor EOL, change to RT8880B		APU_CORE	CPU_CORE IC from RT8880A SA000066V00 change to RT8880B SA000066V10	10/23	EVT
7		Battery connector BATT+ bead, 1pcs for UMA, 2pcs for DIS.		BATT CONN	Add PL202 HCB2012KF-121T50_0805 for DIS only	10/28	EVT
8		22U_0603_6.3V6M cheaper than 47U_0603_6.3V6M		+1.05VS +1.1VALW	PC609, PC610 and PC709, PC710 from 47U_0603_6.3V6M change to 22U_0603_6.3V6M	10/30	EVT
9		HW request Add PR1107, and unpop PR1104, VGA_PG is default setting for VGA sequence control		+0.95V	Add location PR1107 0_0402_5%, and unpop PR1104 0_0402_5%	10/31	EVT
10		HW request add RC at 3VALW enable		+3VALW	Add PR413 0_0402_5%, and PC428 0.1U_0402_10V7K _ un-pop	10/31	EVT
11		adjust 1.05V output voltage		+1.05VSP	change PR607 from 100K ohm to 15.4K ohm, change PR609 from 133K ohm to 20K ohm, change 1.05V output from 1.05V to 1.062V	12/02	DVT
12		adjust 1.8VSP output voltage		+1.8VSP	change PR723 from 20K ohm to 20.5K ohm, change 1.05V output from 1.8V to 1.83V	12/10	DVT
13		adjust 1.1VALW output voltage		+1.1VALW	change PR709 from 118K ohm to 115K ohm, change 1.1VALW output from 1.108V to 1.121V	12/10	DVT
14		Part count reduce			change enable resistor PR413, PR602, PR702, PR724 from 0 ohm to R-Short, change EMI High side and Low side resistor PR308, PR407, PR605, PR705, PR801, PR820, PR849, PR860, PR1216, PR1232 from 0 ohm to R-Short.	12/10	DVT
15		adjust VGA Vboot voltage		VGA	change PR1205 from pop to un-pop, change PR1211 from un-pop to pop.	12/13	DVT
16		reserve PD801		CPU_CORE	reserve PD801 for AMD CPU lekage voltage from APU_SVD	12/13	DVT
17		delete VCIN0 and VCIN1 hysteresis		OTP	change PR216 from 22.6K to 16K, change PR227 from 26.1K to un-pop, change PR202 from UMA/10.5K and DIS/11.3K to 10K, change PR223 from UMA/162K and DIS/100K to un-pop.	12/24	DVT
18		ABO request BI pin short to GND		BATT CONN	change PR210 from 1k to 0 ohm.	12/26	DVT MEMO
19		65W and 40W VCIN0 set at the same voltage active and recovery		OTP	change UMA SKU PR203 from 10K to 44.2K Add PC426	12/26	DVT MEMO

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Issued Date	2012/07/10	Deciphered Date	2013/10/01

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
20		back to back damage, change to low Rds(on) Mos	0.3	Charger	PQ303, PQ304 change from AON4466 to AON4406	01/08	PVT
21		delete PD401 cost down	0.3	3VALW/ 5VALW	change PD301 to R-short PR415	01/08	PVT
22		change PD801 to low Vf diode	0.3	CPU_CORE	change PD801 from RB751V-40_SOD323-2 to RB491D_SOT23-3	01/20	PVT
23							

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Security Classification	Compal Secret Data		
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