MODEL NAME : *VAUB0*

PCB NO : *LA-9941P*
DAA0006W000

BOM P/N : *TBD*

Dell/Compal Confidential

Schematic Document

Phantom(Shark Bay)

Hasweill(BGA) + Lynx Point

DISCRETE VGA N14P(optimus) --- Testarossa
DISCRETE VGA N15P(optimus) --- Testarossa-P

2013-01-02

Rev: 0.1 (X00)

ZZZ PCB R1@

ZZZ PCB R3@

R3@U6 CPU

R3@U7 PCH

UV1 N15R3@ N15P-Q1

UV1 N14R3@ N14P-GT

R1@U6 CPU

R1@U7 PCH

UV1 N15R1@ N15P-Q1

UV1 N14R1@ N14P-GT

@ : Nopop Component
CONN@ : Connector Component
TPM@ : TPM function
DSP@ : DSP function
N14@ : DGPU N14P-GT
N15@ : DGPU N15P-Q1

Samsung 2G

UV5 K4G41325FC-HC04_FBGA170P~D VRAMSR3@

UV6 K4G41325FC-HC04_FBGA170P~D VRAMSR3@

UV9 K4G41325FC-HC04_FBGA170P~D VRAMSR3@

UV10 K4G41325FC-HC04_FBGA170P~D VRAMSR3@

Samsung 2G

UV5 K4G41325FC-HC04_FBGA170P~D VRAMSR1@

UV6 K4G41325FC-HC04_FBGA170P~D VRAMSR1@

UV9 K4G41325FC-HC04_FBGA170P~D VRAMSR1@

UV10 K4G41325FC-HC04_FBGA170P~D VRAMSR1@

Hynix 2G

UV5 H5GC4H24MFR-T2C_FBGA170P~D VRAMHR3@

UV6 H5GC4H24MFR-T2C_FBGA170P~D VRAMHR3@

UV9 H5GC4H24MFR-T2C_FBGA170P~D VRAMHR3@

UV10 H5GC4H24MFR-T2C_FBGA170P~D VRAMHR3@

Hynix 2G

UV5 H5GC4H24MFR-T2C_FBGA170P~D VRAMHR1@

UV6 H5GC4H24MFR-T2C_FBGA170P~D VRAMHR1@

UV9 H5GC4H24MFR-T2C_FBGA170P~D VRAMHR1@

UV10 H5GC4H24MFR-T2C_FBGA170P~D VRAMHR1@

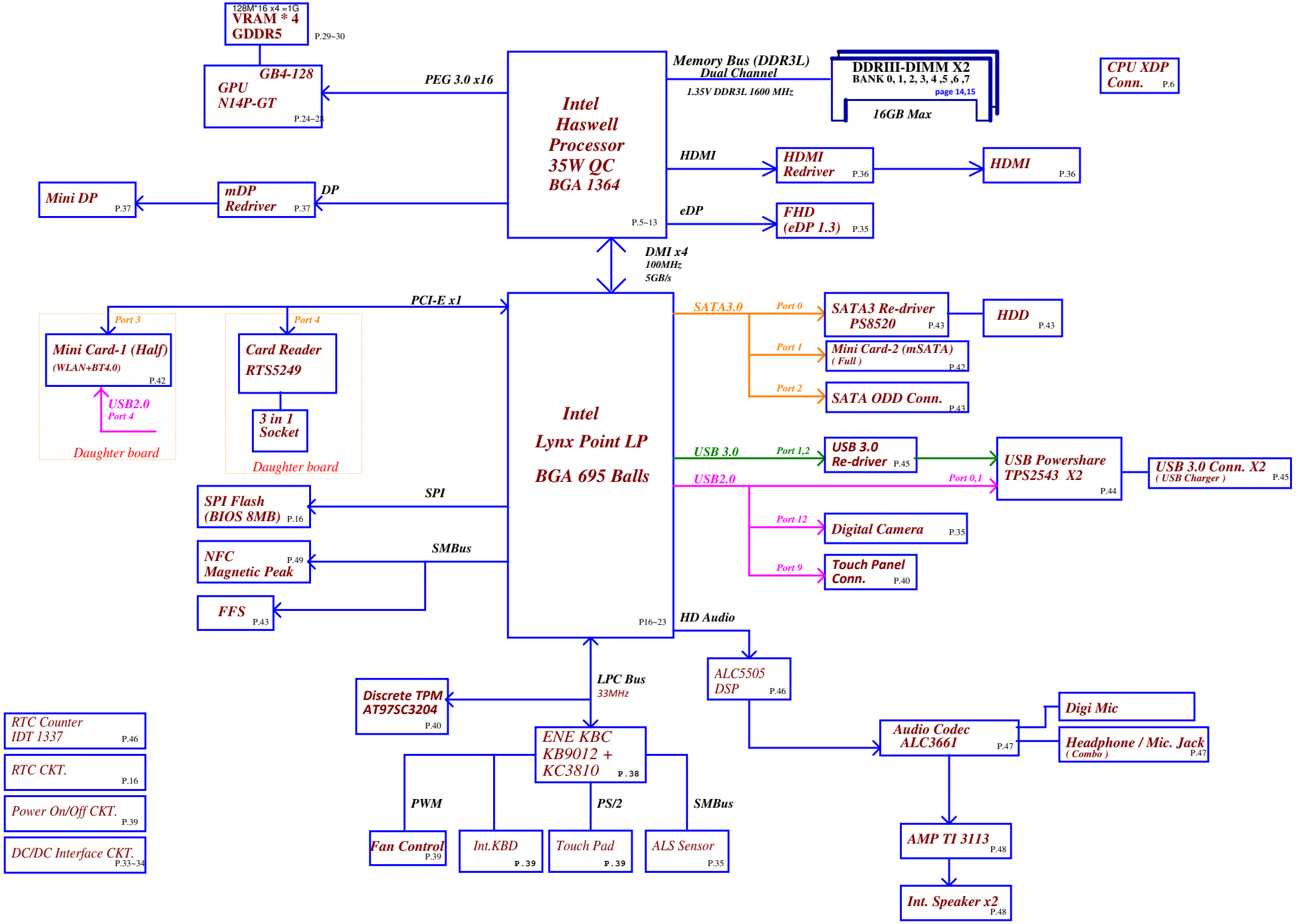
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: *Cover Page*

Size: | Document Number: *LA-9941P* | Rev: 0.1

Date: Wednesday, September 04, 2013 | Sheet 1 of 62

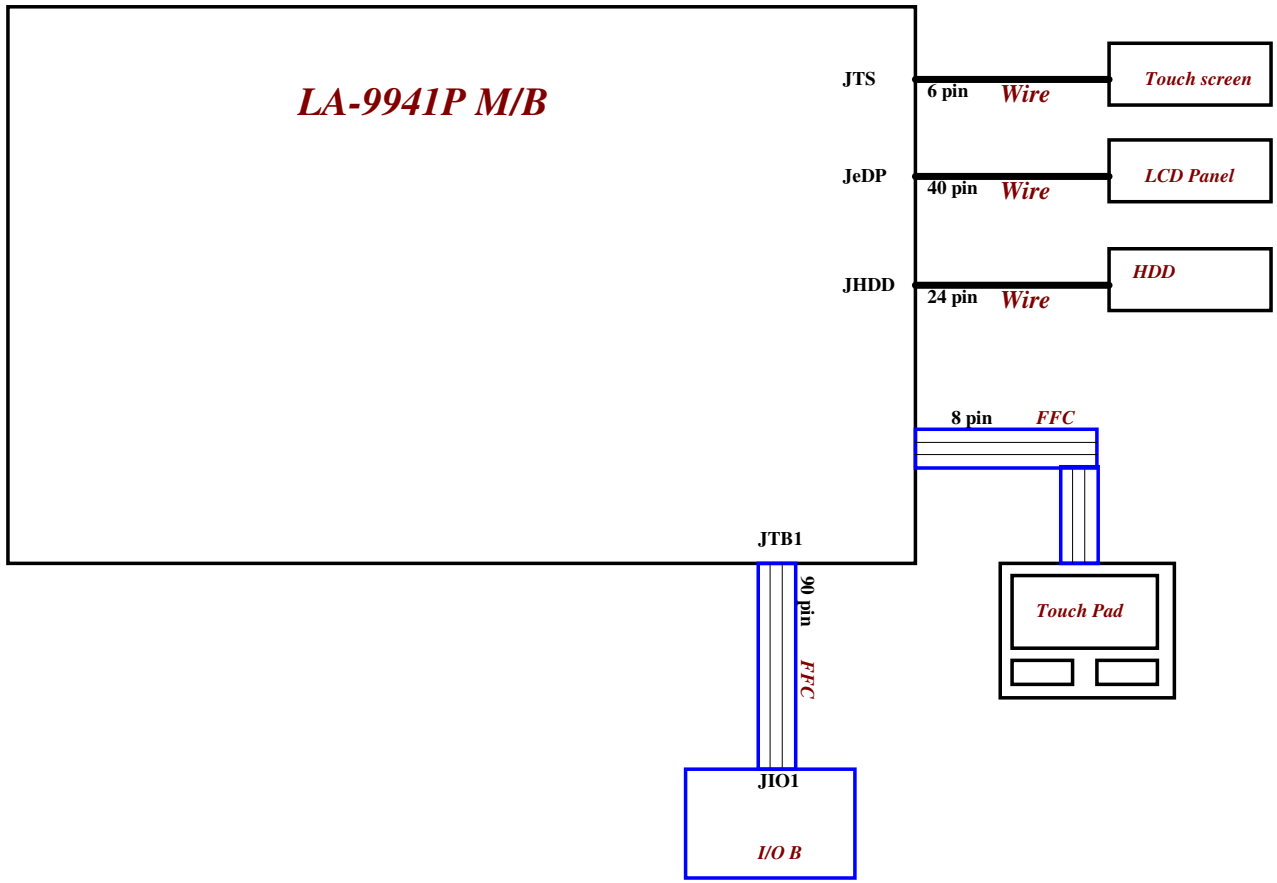


Security Classification	Compal Secret Data		Compal Electronics,Inc.
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Title			
Size C	Document Number		Rev 0.1
Date: Tuesday, September 03, 2013	Sheet 2	of 62	

Compal Confidential

Project Code : VAUB0
File Name : LA-9941P



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Title: **Block Diagram**

Size: B | Document Number | Rev: 0.1

Date: Tuesday, September 03, 2013 | Sheet 3 of 62

Vcc	3.3V	
Ra	100K +/- 1%	
Board ID	Rb	
0	0	
1	12K	+/- 1%
2	15K	+/- 1%
3	20K	+/- 1%
4	27K	+/- 1%
5	33K	+/- 1%
6	43K	+/- 1%
7	56K	+/- 1%
8	75K	+/- 1%
9	100K	+/- 1%
10	130K	+/- 1%
11	160K	+/- 1%
12	200K	+/- 1%
13	240K	+/- 1%
14	270K	+/- 1%
15	330K	+/- 1%
16	430K	+/- 1%
17	560K	+/- 1%
18	750K	+/- 1%
19	NC	

Board ID	PCB Revision
0	DIS 0.1
1	DIS 0.2
2	DIS 0.3
3	DIS 0.4
4	DIS 0.5
5	DIS 1.0
6	DIS-P 0.2
7	DIS-P 0.3
8	DIS-P 0.4
9	DIS-P 1.0
10	UMA 0.2
11	UMA 0.3
12	UMA 0.4
13	UMA 1.0
14	
15	
16	
17	
18	
19	

PCI EXPRESS	DESTINATION
Lane 1	None
Lane 2	None
Lane 3	MINI CARD-1 WLAN
Lane 4	CARD READER
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

SATA	DESTINATION
SATA0	HDD
SATA1	SSD
SATA2	None
SATA3	None
SATA4	None
SATA5	None

CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC LPC
PCI2	None
PCI3	None
PCI4	None

	USB PORT#	DESTINATION
PCH	0	USB Conn 1 (Power share)
	1	USB Conn 3 (Power share)
	2	USB Conn 2 (Power share)
	3	USB Conn 4 (Power share)
	4	JMINI1 (WLAN)
	5	None
	6	None
	7	None
	8	None
	9	Touch screen
	10	None
	11	None
	12	CAMERA
	13	None

USB3	DESTINATION
1	USB Conn 1 (Power share)
2	USB Conn 3 (Power share)
3	USB Conn 2 (Power share)
4	USB Conn 4 (Power share)

	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
CLK	CLKOUT_PCIE0	None	CLKOUTFLEX0	CLK_PCI_TPM
	CLKOUT_PCIE1	None	CLKOUTFLEX1	None
	CLKOUT_PCIE2	None	CLKOUTFLEX2	None
	CLKOUT_PCIE3	MINI CARD-1 WLAN	CLKOUTFLEX3	None
	CLKOUT_PCIE4	CARD READER		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

Symbol Note :

: means Digital Ground

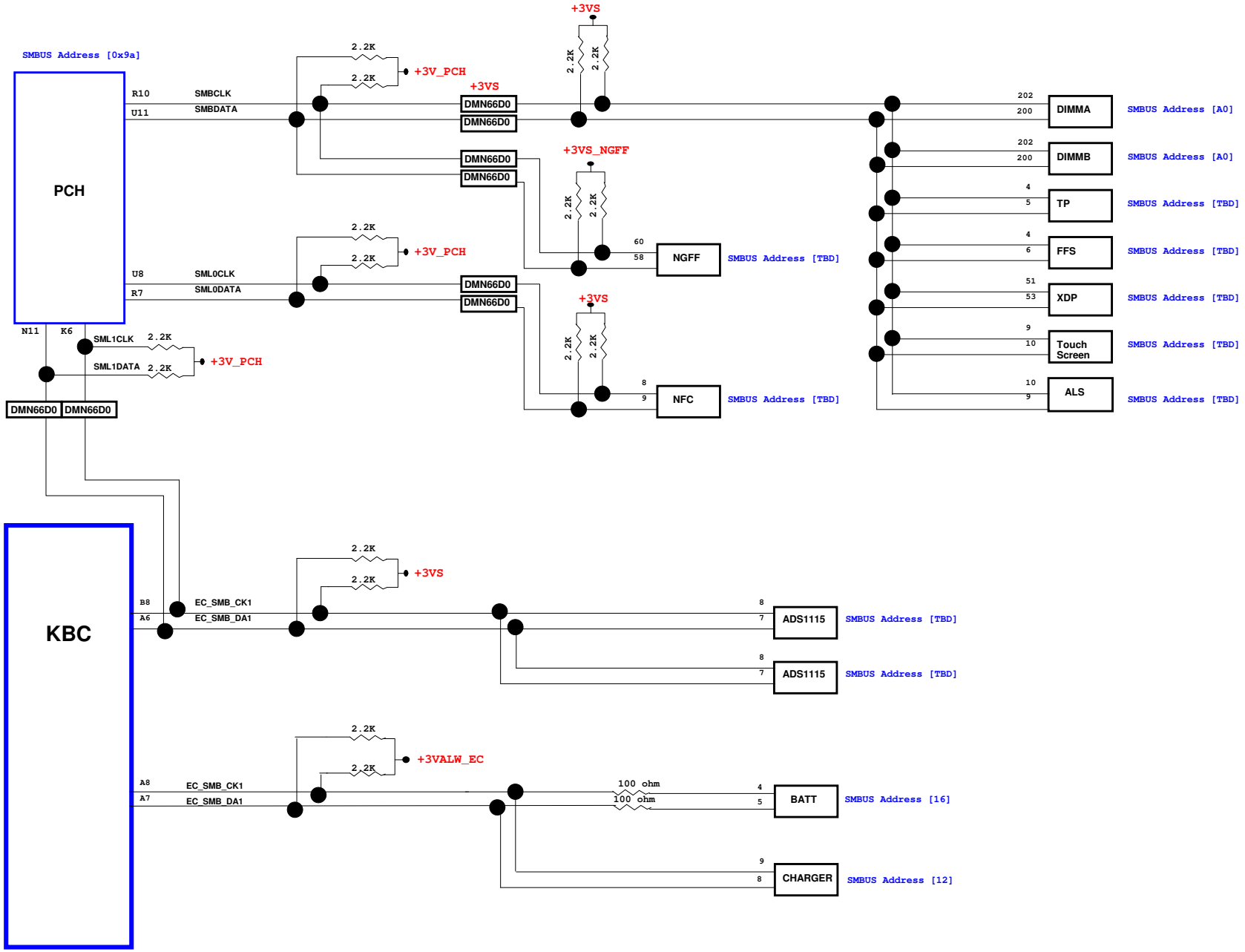
: means Analog Ground

Compal Electronics, Inc.

Title: Notes List

Size | Document Number: LA-9941P | Rev: 0.1

Date: Tuesday, September 03, 2013 | Sheet 4 of 62



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/15

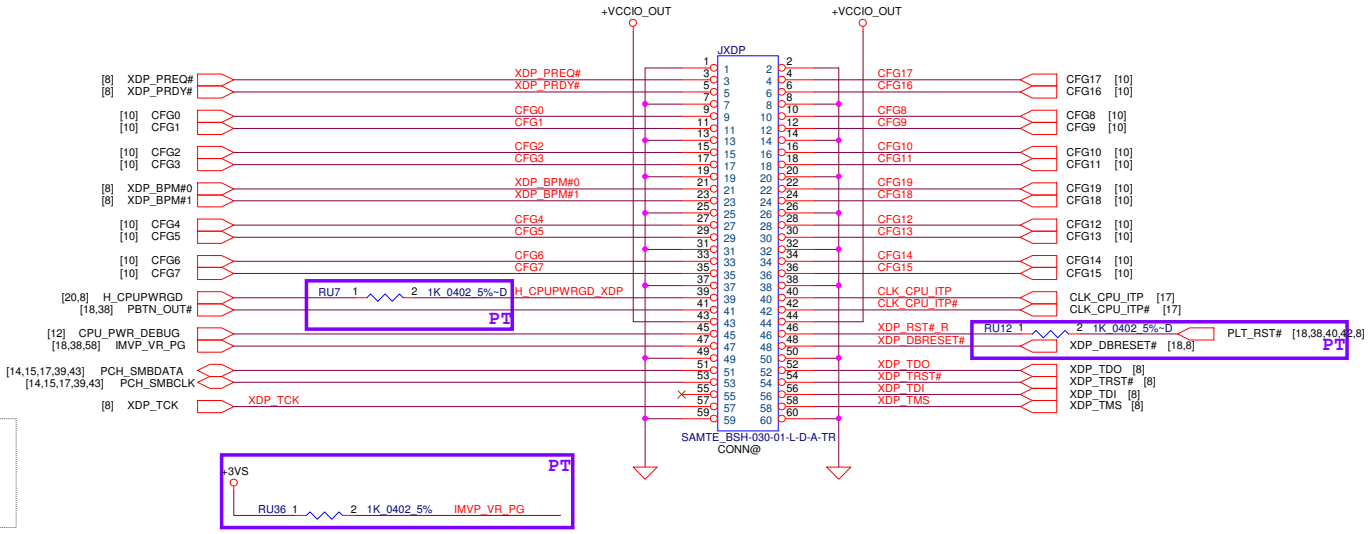
Compal Electronics, Inc.

Title: SMBus Block Diagram

Size	Document Number	Rev
Custom		0.1

Date: Tuesday, September 03, 2013 Sheet 5 of 62

XDP CONN



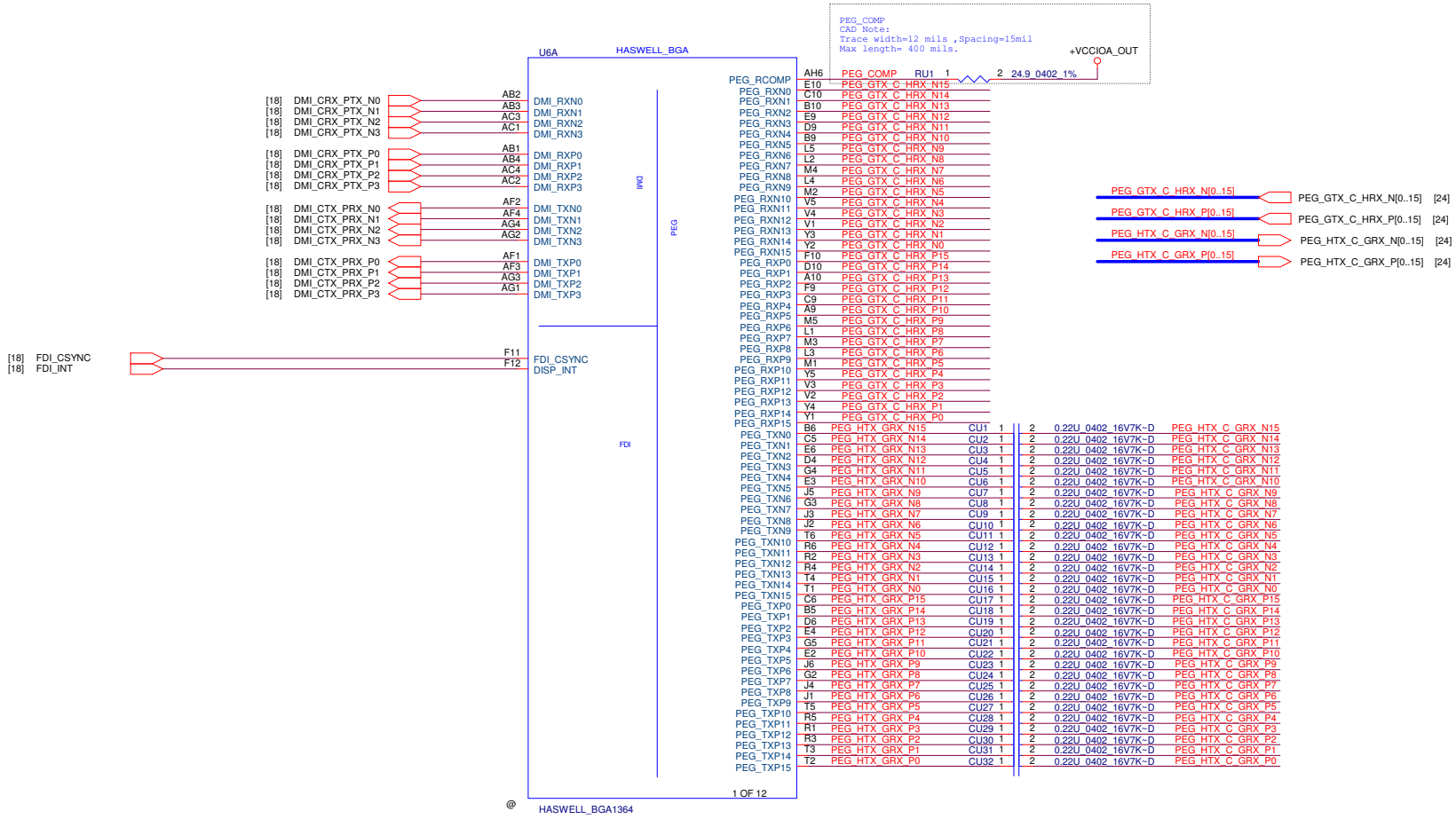
The resistor for HOOK2 should be placed such that the stub is very small on CFG0 net

Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **Block Diagram**

Size	Document Number	Rev 0.1
Date: Tuesday, September 03, 2013	Sheet 6 of 62	



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: PROCESSOR(1/7) DMI,FDI,PEG

Size	Document Number	Rev
Custom		0.1

Date: Tuesday, September 03, 2013 Sheet 7 of 62

Processor Pullups

+VCCIO_OUT

RU30 1 — 2 62_0402_5% — H_PROCHOT#

place RU33,RU30 near CPU

RU33 1 — 2 10K_0402_5%~D — H_CPUPWRGD

+VCCIO_OUT

@RU40 1 — 2 10K_0402_5%~D — CLK_CPU_SSC_DPLL

@RU44 1 — 2 10K_0402_5%~D — CLK_CPU_SSC_DPLL#

SSC CLOCK TERMINATION,
IF NOT USED, stuff RU40,RU44

U6B HASWELL_BGA

MISC: PROC_DETECT, CATERR, PECI, PROCHOT, THERMTRIP

THERMAL: DDR3L

DDR3L: SM_RCOMP0, SM_RCOMP1, SM_RCOMP2, SM_DRAMRST

JTAG: PRDY, PREQ, TCK, TMS, TRST, TDI, TDO, DBR

PWR: PM_SYNC, PWRGOOD, SM_DRAMPWROK, PLTRSTIN

CLOCK: DPLL_REF_CLKN, DPLL_REF_CLKP, SSC_DPLL_REF_CLKN, SSC_DPLL_REF_CLKP, BCLKN, BCLKP

BPM#0 BPM#1 BPM#2 BPM#3 BPM#4 BPM#5 BPM#6 BPM#7

2 OF 12

HASWELL_BGA1364

PT

[38] H_PECI

[38,53,58] H_PROCHOT# — RU32 1 — 2 56_0402_5% — H_PROCHOT# R

[20] H_THERMTRIP#

[18] H_PM_SYNC

[20,6] H_CPUPWRGD

[20] CPU_PLTRST# — @RU37 1 — 2 0_0402_5% — PM_SYS_PWRGD_BUF_R — BUF_CPU_RST#

ST

[17] DPLL_REF_CLK#

[17] DPLL_REF_CLK

[17] CLK_CPU_SSC_DPLL#

[17] CLK_CPU_SSC_DPLL

[17] CLK_CPU_DMI#

[17] CLK_CPU_DMI

CLK_CPU_SSC_DPLL#

CLK_CPU_SSC_DPLL

SM_RCOMP0 SM_RCOMP1 SM_RCOMP2 SM_DRAMRST

XDP_PRDY# XDP_PREQ# XDP_TCK XDP_TMS XDP_TRST# XDP_TDI XDP_TDO XDP_DBRESET# [18,6]

XDP_BPM#0 [6] XDP_BPM#1 [6]

For ESD concern, please put near CPU

DDR3L Compensation Signals

SM_RCOMP0 RU58 1 — 2 100_0402_1%~D

SM_RCOMP1 RU59 1 — 2 75_0402_1%~D

SM_RCOMP2 RU61 1 — 2 100_0402_1%~D

CAD Note:
Trace width=12~15 mil, Spcing=20 mils
Max trace length= 500 mil

PU/PD for JTAG signals

+VCCP

XDP_TDO RU66 1 — 2 51_0402_5%

XDP_TCK RU67 1 — 2 51_0402_5%

XDP_TRST# RU68 1 — 2 51_0402_5%

+3VS

XDP_DBRESET# RU35 1 — 2 1K_0402_5%~D

U6J HASWELL_BGA

DDIB_TXN0 DDIB_TXP0 DDIB_TXN1 DDIB_TXP1 DDIB_TXN2 DDIB_TXP2 DDIB_TXN3 DDIB_TXP3

[36] HDMI_A2N_VGA
[36] HDMI_A2P_VGA
[36] HDMI_A1N_VGA
[36] HDMI_A1P_VGA
[36] HDMI_A0N_VGA
[36] HDMI_A0P_VGA
[36] HDMI_A3N_VGA
[36] HDMI_A3P_VGA

[37] mDP_A0N_CPU
[37] mDP_A0P_CPU
[37] mDP_A1N_CPU
[37] mDP_A1P_CPU
[37] mDP_A2N_CPU
[37] mDP_A2P_CPU
[37] mDP_A3N_CPU
[37] mDP_A3P_CPU

DDIC_TXN0 DDIC_TXP0 DDIC_TXN1 DDIC_TXP1 DDIC_TXN2 DDIC_TXP2 DDIC_TXN3 DDIC_TXP3

DDID_TXN0 DDID_TXP0 DDID_TXN1 DDID_TXP1 DDID_TXN2 DDID_TXP2 DDID_TXN3 DDID_TXP3

EDP_AUXN EDP_AUXP EDP_HPD

EDP_TXN0 EDP_TXN1 EDP_TXP0 EDP_TXP1

EDP_RCOMP EDP_DISP_UTIL

FDI_TXN0 FDI_TXP0 FDI_TXN1 FDI_TXP1

EDP_AUXN [35] EDP_AUXP [35] EDP_HPD [35]

EDP_TXN0 [35] EDP_TXN1 [35] EDP_TXP0 [35] EDP_TXP1 [35]

+VCCIOA_OUT

AG6 EDP_COMP — RU2 1 — 2 24.9_0402_1%

EDP_COMP
CAD Note:Trace width=20 mils ,Spacing=25mil,
Max length=100 mils.

EDP_TXN2 [35] EDP_TXP2 [35] EDP_TXN3 [35] EDP_TXP3 [35]

10 OF 12

HASWELL_BGA1364

Buffered reset to CPU

CAD Note:
PLACE PULL-UP RESISTOR WITHIN 2 INCH OF THE CPU

+3VS — @RU42 75_0402_5% — +3VCP — RU13 1K_0402_5%~D

UU2 SN74LVC1G07DCKR_SC70-5

[18,38,40,42,6] PLT_RST# — PLT_RST# 2 — A

BUFO_CPU_RST# — @RU48 1 — 2 43_0402_1% — BUF_CPU_RST#

RU11 20K_0402_5%~D

+3VALW — ST — RU118 10K_0402_1%~D

[38] VCIN0_PH

HU101 100K_0402_1%_TSM0B104F4251RZ

close CPU chip

SM_DRAMPWROK

NOTE: S3 POWER REDUCTION IS NOT FOR
THIS CIRCUIT IS FOR INTERNAL TESTING PURPOSES ONLY.

PM_SYS_PWRGD_BUF — @RU56 — PM_SYS_PWRGD_BUF_R

QU7 BSS138-G_SOT23-3

[55] +1.35V_PWROK — @RU53 — ST

DRAMRST_CNTRL_S3 — @RU54 — 0_0402_5%~D

+3VALW — R23 100K_0402_5%~D

PT [38,56] +V1.05S_VCCP_PWRGOOD — @RU50 — 0_0402_5%~D — CPU1.5V_S3_GATE_R

[18] PM_DRAM_PWRGD — @RU51 — 0_0402_5%~D

UU3 74AHC1G09GW_TSSOP5

4PM_SYS_PWRGD_BUF

+1.35V_CPU_VDDQ — RU60 1.82K_0402_1%

R59 3.32K_0402_1%~D

@RU43 — PM_SYS_PWRGD_BUF_R — ST

+3VALW — RU76 — 200_0402_5%

S3 circuit:DRAM_RST# to memory should be high during S3

+1.35V — RU72 1K_0402_5%~D

H_DRAMRST# — RU74 4.99K_0402_1%~D

QU3 BSS138-G_SOT23-3

DDR3_DRAMRST# R — RU73 — 1K_0402_5%~D — DDR3_DRAMRST# [14,15]

DRAMRST_CNTRL_S3

[14,38] DRAMRST_CNTRL_S3 — RU62 — 100K_0402_5%~D

For deep S3

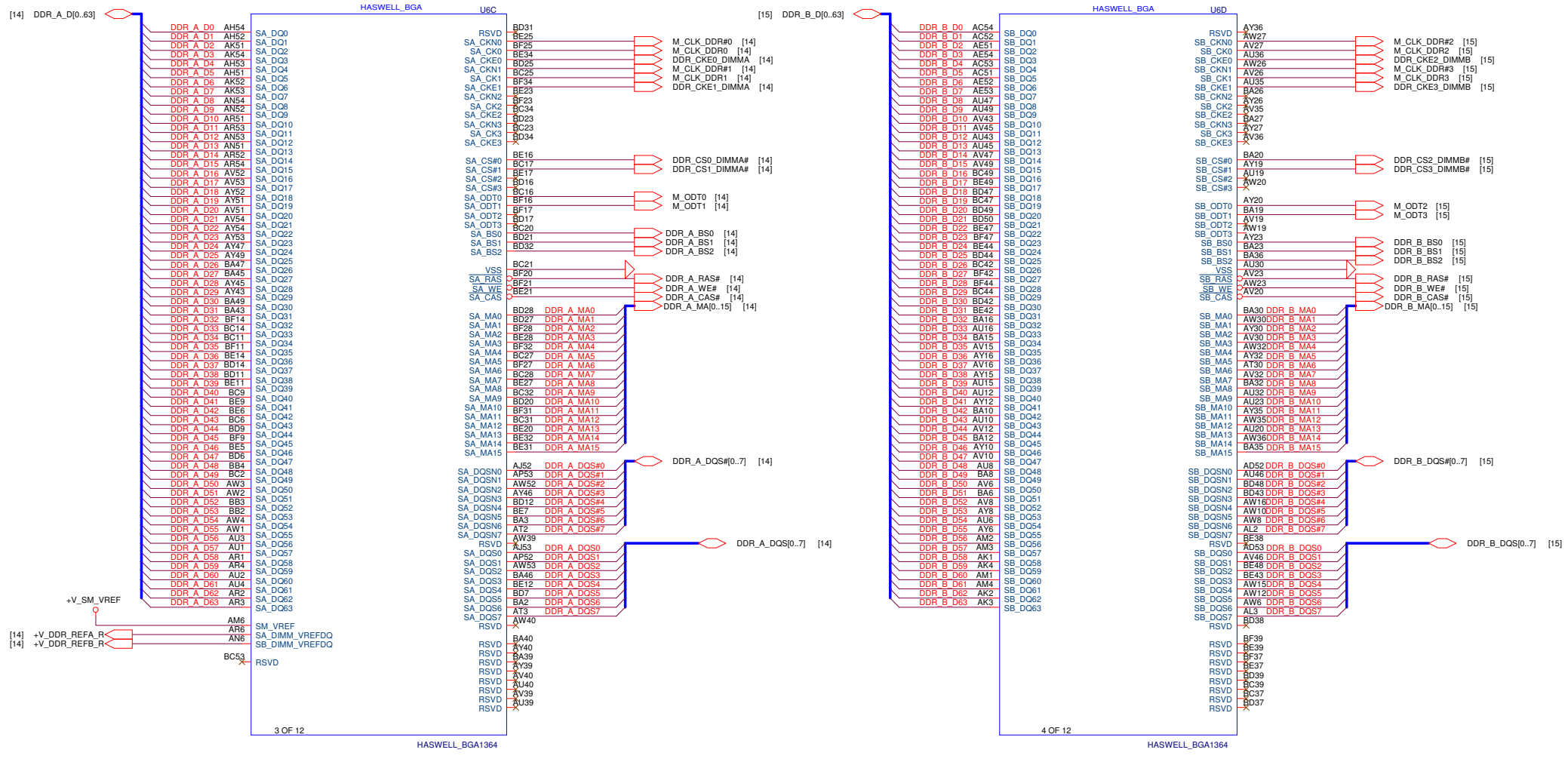
CU39 0.047U_0402_16V7K

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Title: PROCESSOR(2/7) PM,XDP,CLK

Size: Custom | Document Number | Rev: 0.1

Date: Tuesday, September 03, 2013 | Sheet 8 of 62



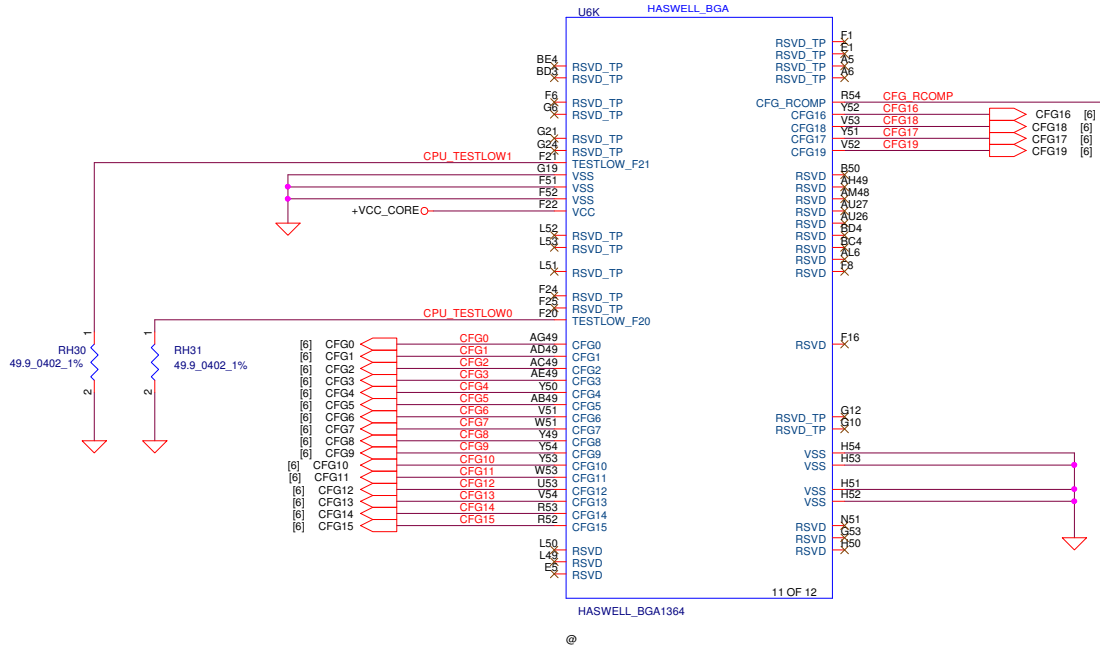
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

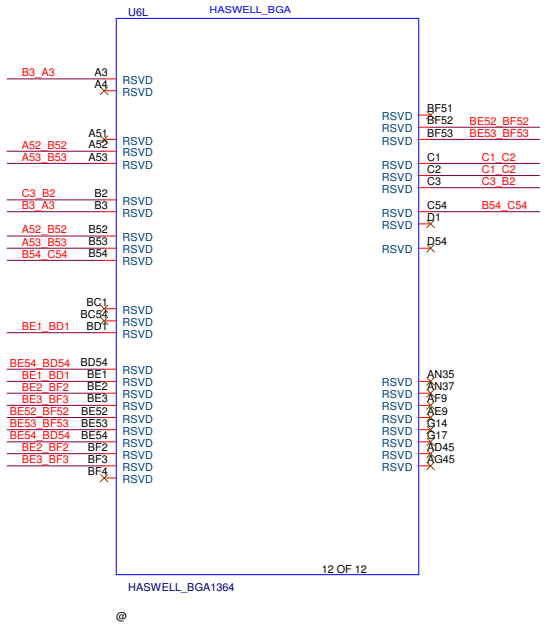
Compal Electronics, Inc.

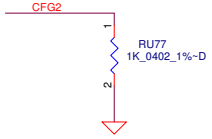
Title: PROCESSOR(3/7) DDRIII

Size: Custom	Document Number	Rev: 0.1
Date: Tuesday, September 03, 2013	Sheet 9 of 62	

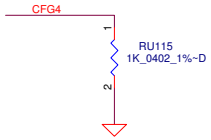
CFG Straps for Processor



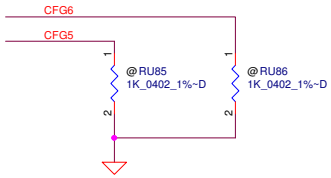




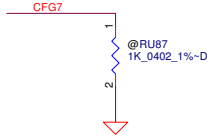
PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

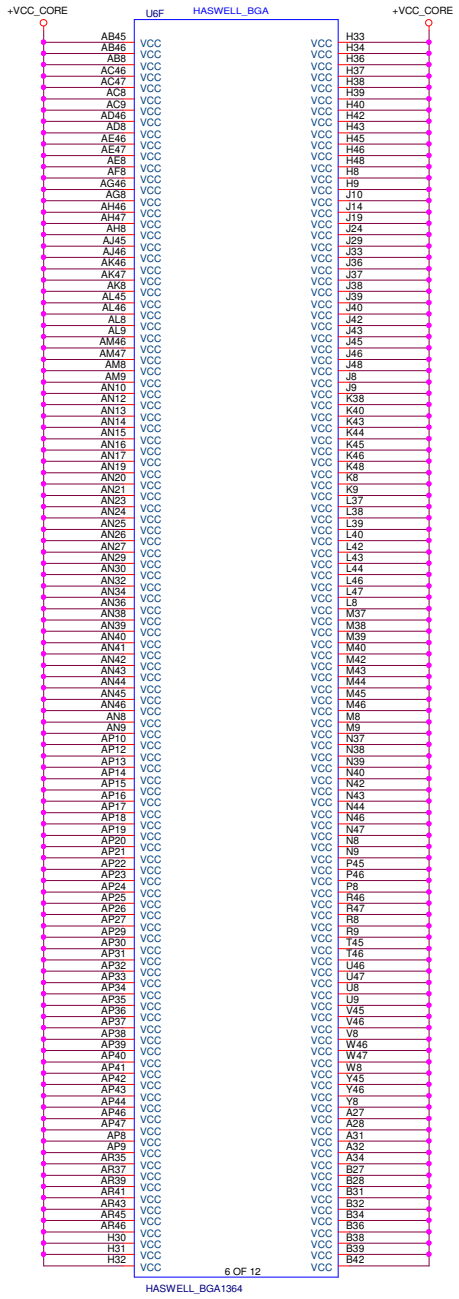
Compal Electronics, Inc.

Title: PROCESSOR(4/7) RSVD,CFG

Size: Custom | Document Number | Rev: 0.1

Date: Tuesday, September 03, 2013 | Sheet 10 of 62

55A



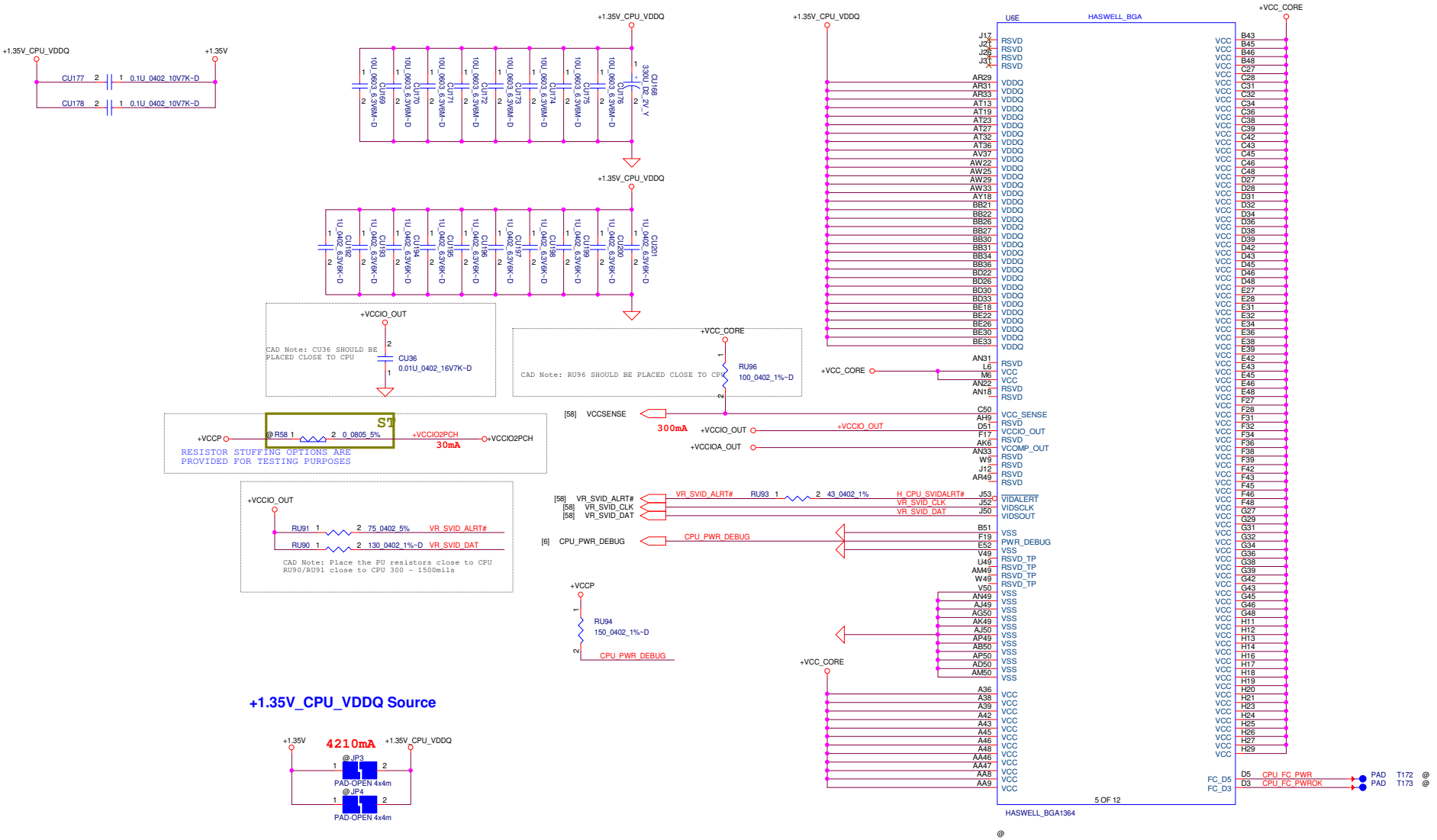
@

Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Title: ***PROCESSOR(5/7) PWR,BYPASS***

Size	Document Number	Rev
Custom		0.1

Date: Tuesday, September 03, 2013 Sheet 11 of 62



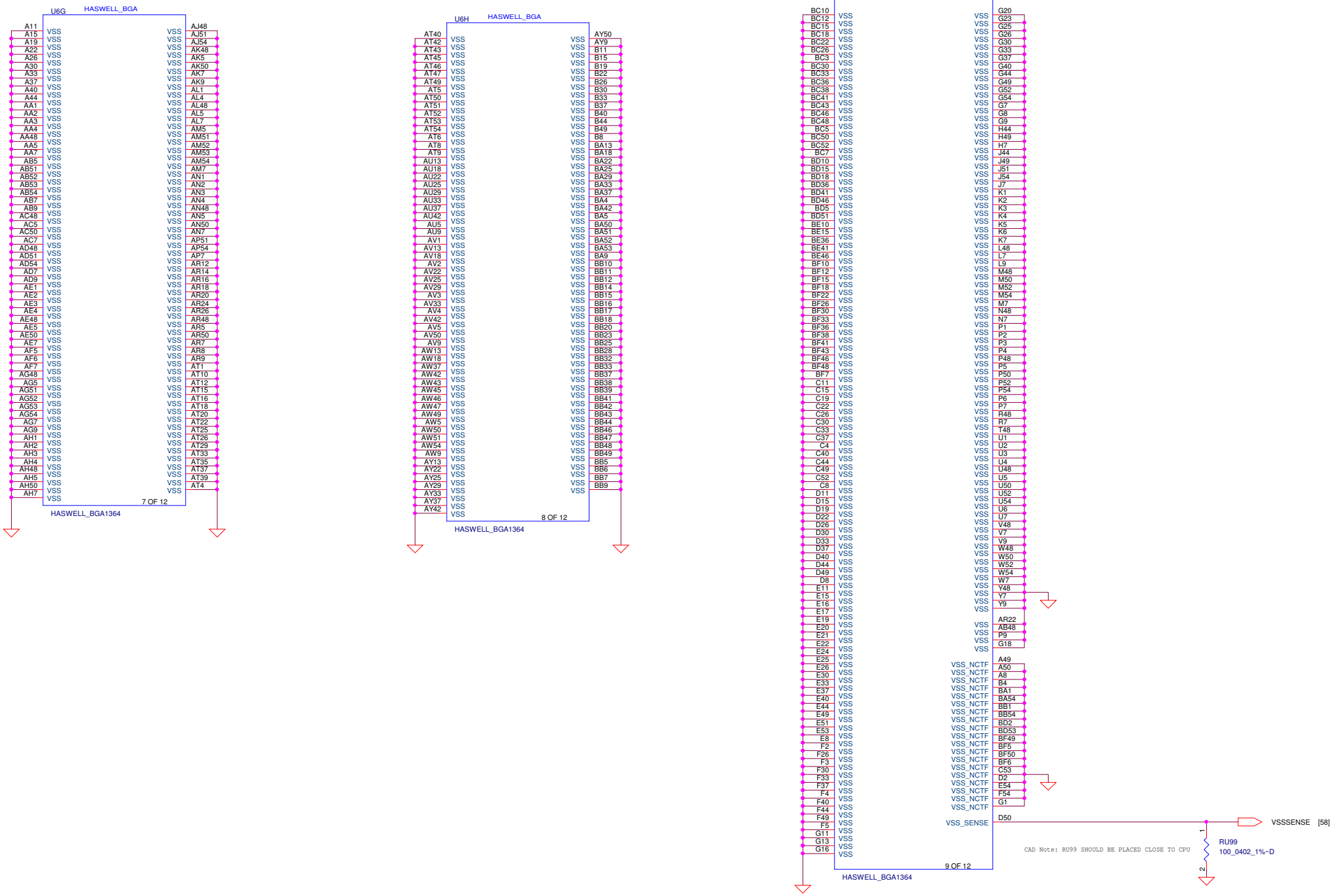
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: PROCESSOR(6/7) PWR

Size	Document Number	Rev
Custom		0.1

Date: Tuesday, September 03, 2013 Sheet 12 of 62



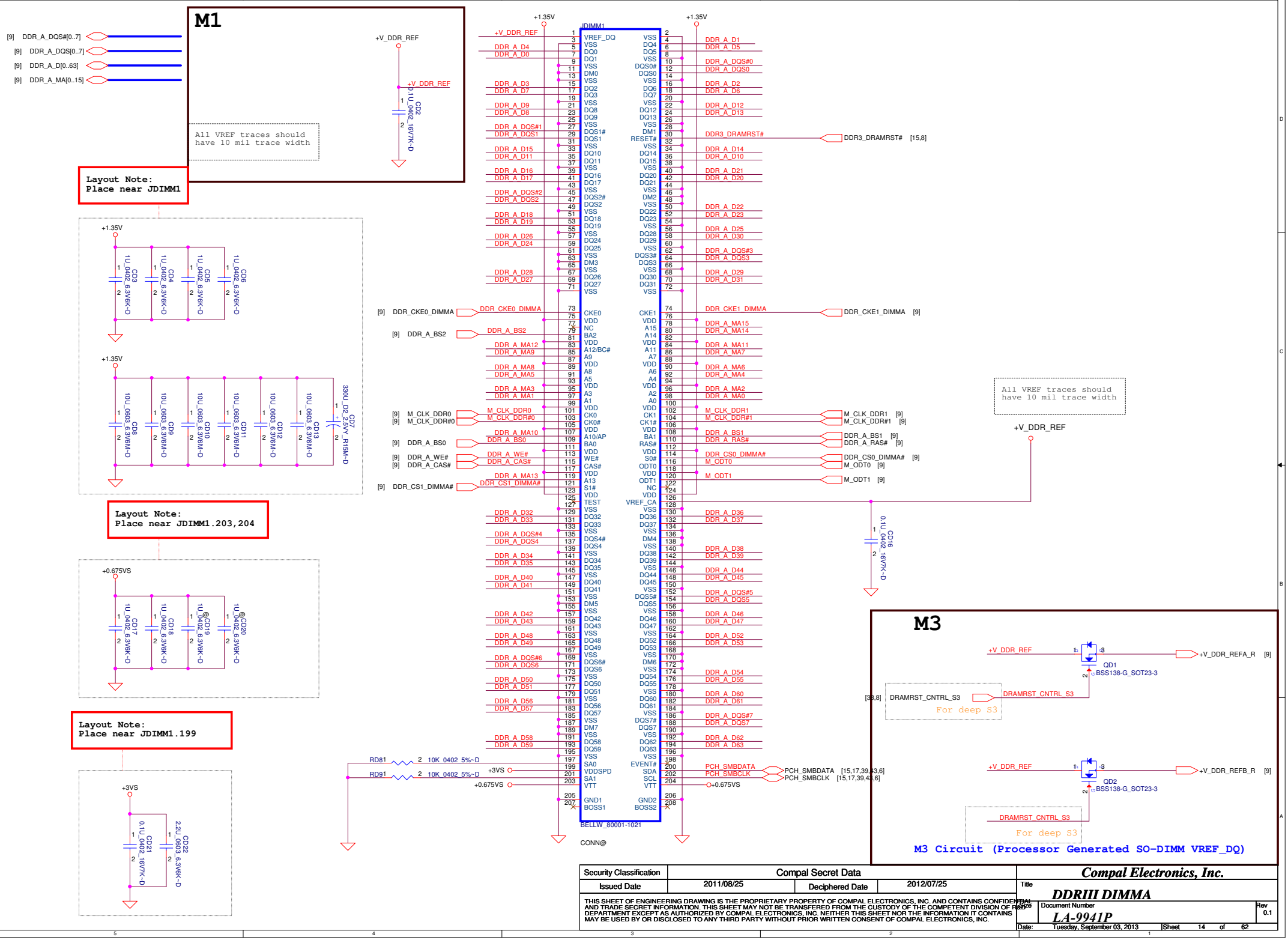
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: PROCESSOR(7/7) VSS

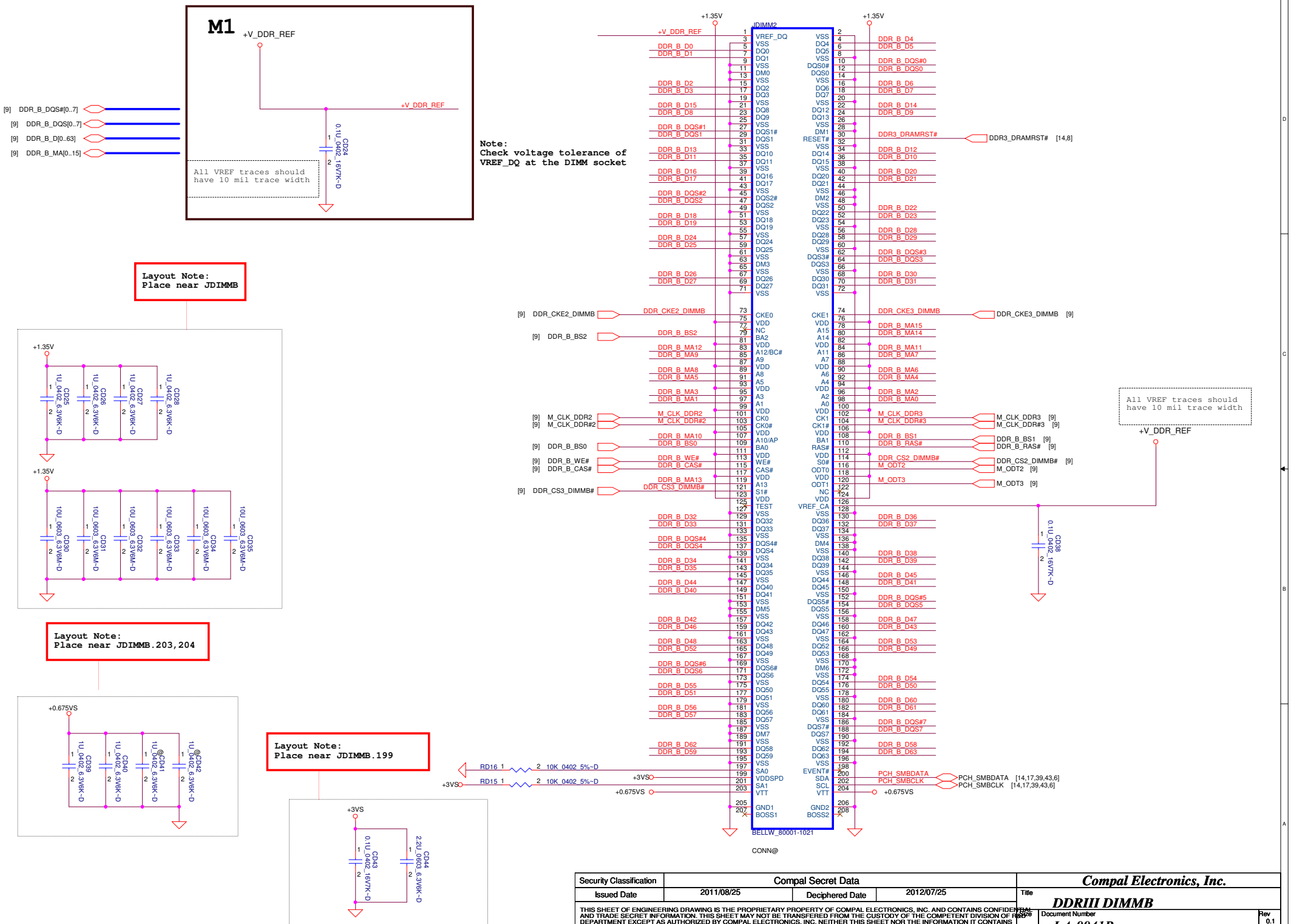
Size	Document Number	Rev
Custom		0.1

Date: Tuesday, September 03, 2013 Sheet 13 of 62



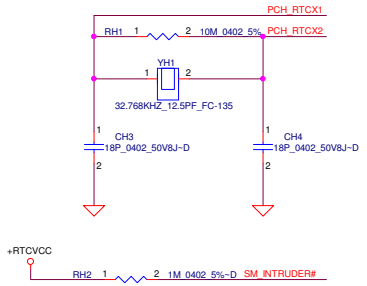
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.			
Title: DDRIII DIMMA			
Size	Document Number: LA-9941P		Rev: 0.1
Date: Tuesday, September 03, 2013	Sheet 14 of 62		



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/08/25	Deciphered Date	2012/07/25
Title	DDRIII DIMMB		
Size	Document Number		Rev
	LA-9941P		0.1
Date:	Tuesday, September 03, 2013	Sheet	15 of 62

RTC CRYSTAL

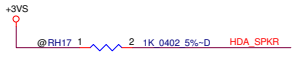


PCH Strap PIN

INTVRMEN Integrated 1.05V VRM Enable/Disable

* H : Integrated VRM enable
L : Integrated VRM disable

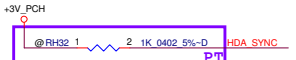
SPKR No Reboot



*LOW=Default
HIGH=No Reboot

If the signal is sampled high, this indicate that the system is strapped to the "No Reboot" mode

HDA_SYNC On-Die PLL Voltage Regulator Voltage Select



This signal has a weak internal pull-down
On Die PLL VR is supplied by
1.5V when smapled high
* 1.8V when sampled low
Needs to be pulled High for Huron River platfrom

HDA_SDO
Flash Descriptor Security Override/Intel ME Debug Mode

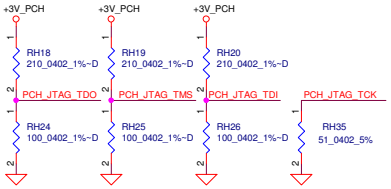
*Low = Disabled
High = Enabled

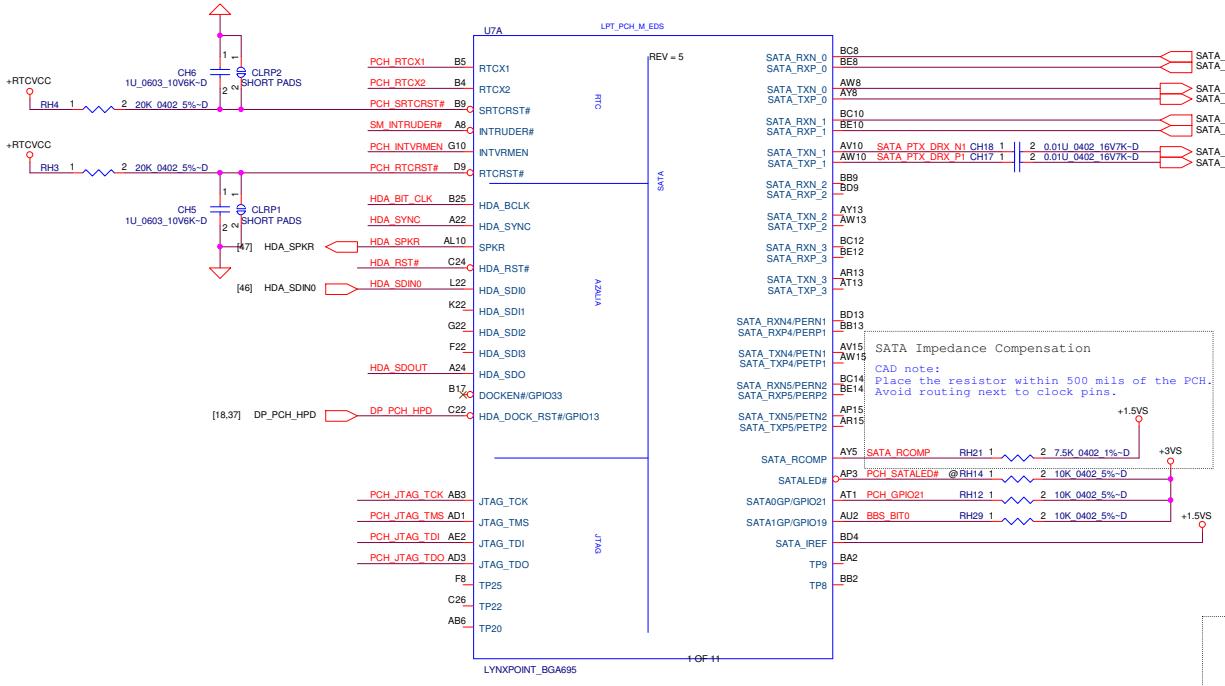
ME debug mode , this signal has a weak internal PD

L=>security measures defined in the Flash Descriptor will be in effect (default)

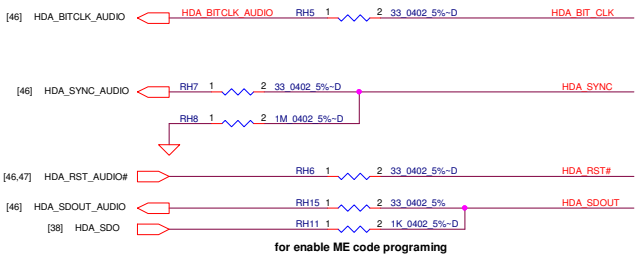
H=>Flash Descriptor Security will be overridden

JTAG



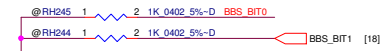


HD Audio



for enable ME code programing

Boot BIOS Strap

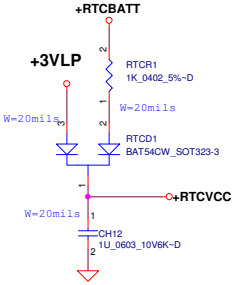


GPIO19 => BBS_BIT0
GPIO51 => BBS_BIT1

Boot BIOS Strap		
BBS_BIT[1]	BBS_BIT[0]	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

*

RTC Battery



Reserve for EMI

Reserve for RF please close to UH1

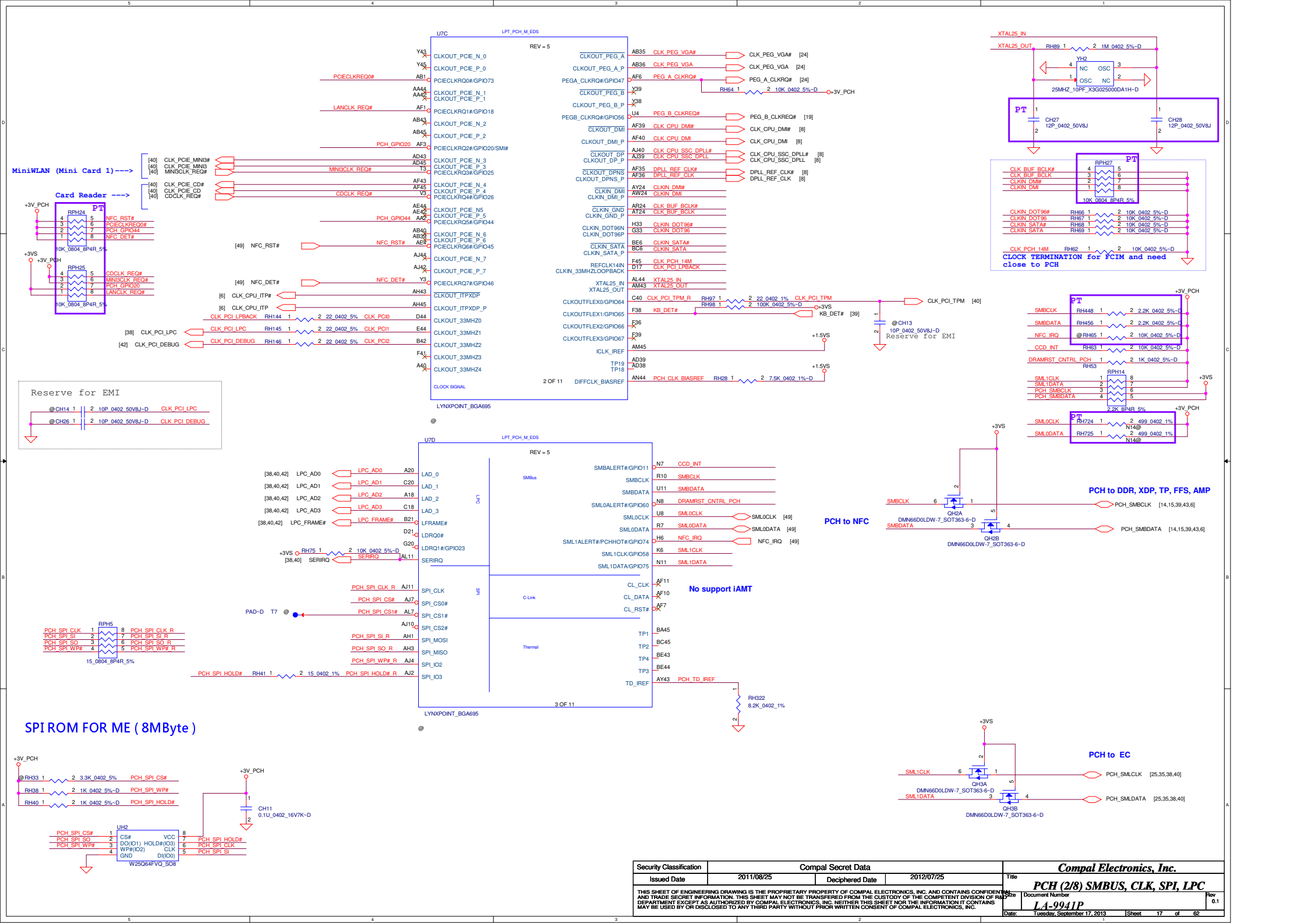
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: PCH (1/8) SATA,HDA

Size | Document Number: LA-9941P | Rev: 0.1

Date: Tuesday, September 03, 2013 | Sheet 16 of 62


U7C
LPT_PCH_M_EDS
REV = 5
LYNXPOINT_BGA695
2 OF 11
CLOCK SIGNAL
DIFFCLK_BIASREF
MiniWLAN (Mini Card 1)--->
Card Reader --->
CLOCK TERMINATION for FCIM and need close to PCH
Reserve for EMI
U7D
3 OF 11
SMBus
LPC
SPI
C-Link
Thermal
No support iAMT
PCH to NFC
PCH to DDR, XDP, TP, FFS, AMP
PCH to EC
SPI ROM FOR ME (8MByte)
W25Q64FVQ_SO8
Security Classification
Compal Secret Data
Issued Date
2011/08/25
Deciphered Date
2012/07/25
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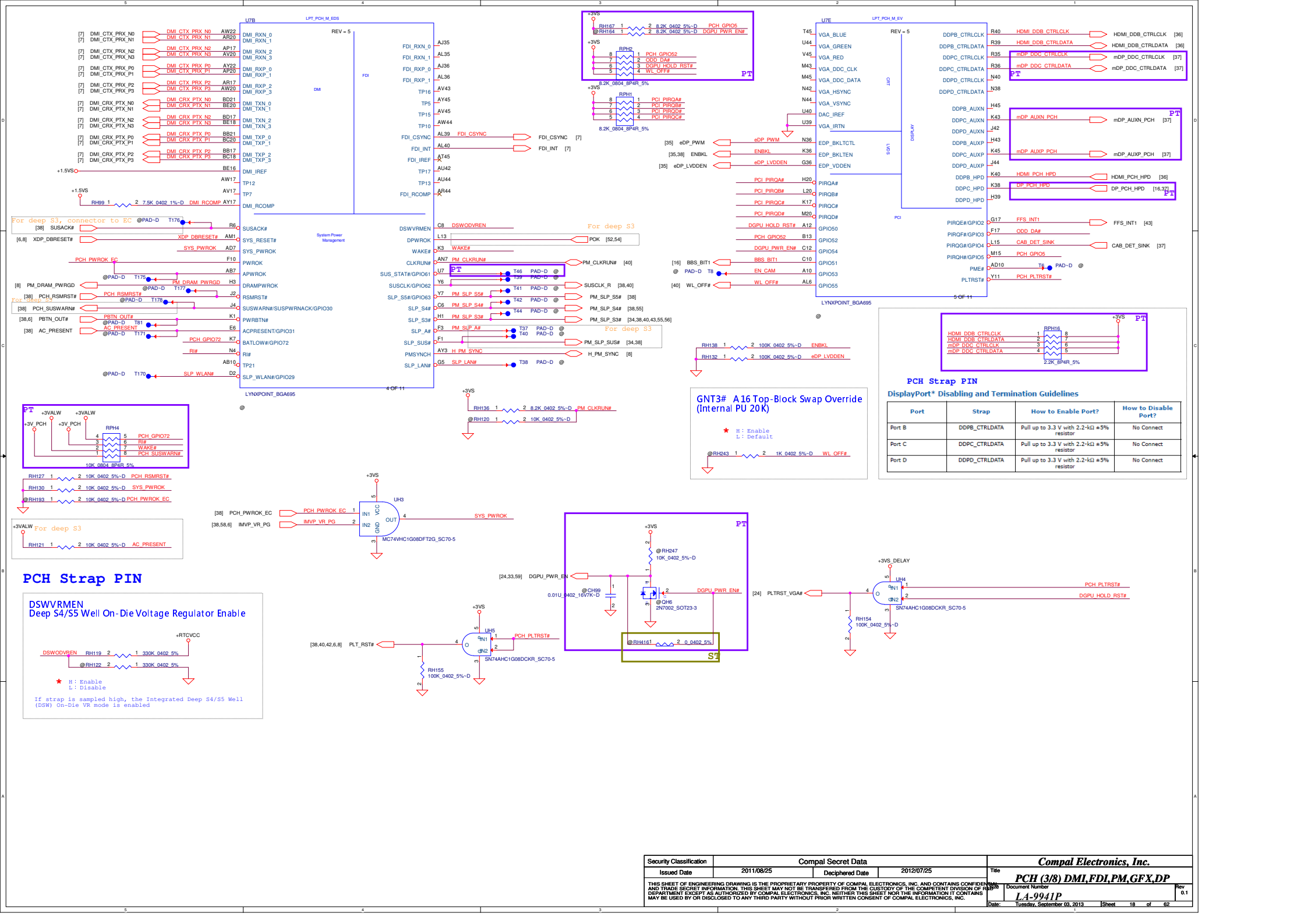
Compal Electronics, Inc.
Title
PCH (2/8) SMBUS, CLK, SPI, LPC
Size
Document Number
LA-9941P
Rev
0.1
Date: Tuesday, September 17, 2013
Sheet 17 of 62


U7B
LPT_PCH_M_EDS
REV = 5
DMI
FDI
System Power Management
LYNXPOINT_BGA695
4 OF 11
U7E
LPT_PCH_M_EV
CRT
DISPLAY
LVDS
PCI
LYNXPOINT_BGA695
5 OF 11
PCH Strap PIN
DSWVRMEN
Deep S4/S5 Well On-Die Voltage Regulator Enable
If strap is sampled high, the Integrated Deep S4/S5 Well (DSW) On-Die VR mode is enabled
PCH Strap PIN
DisplayPort* Disabling and Termination Guidelines
Port
Strap
How to Enable Port?
How to Disable Port?
Port B
DDPB_CTRLDATA
Pull up to 3.3 V with 2.2-kΩ ±5% resistor
No Connect
Port C
DDPC_CTRLDATA
Pull up to 3.3 V with 2.2-kΩ ±5% resistor
No Connect
Port D
DDPD_CTRLDATA
Pull up to 3.3 V with 2.2-kΩ ±5% resistor
No Connect
GNT3# A16 Top-Block Swap Override (Internal PU 20K)
H : Enable
L : Default
For deep S3
PT
ST
Security Classification
Compal Secret Data
Issued Date
2011/08/25
Deciphered Date
2012/07/25
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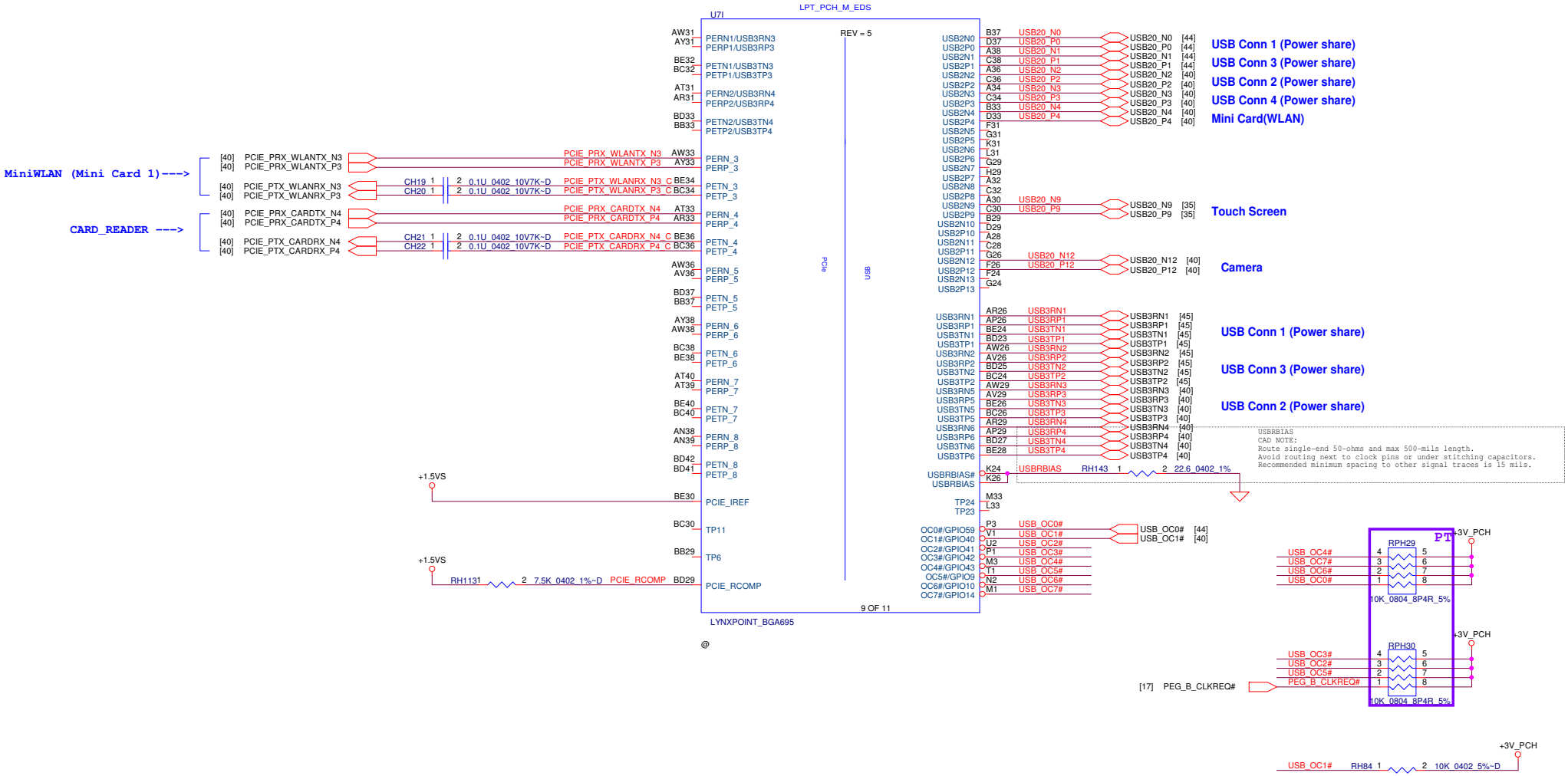
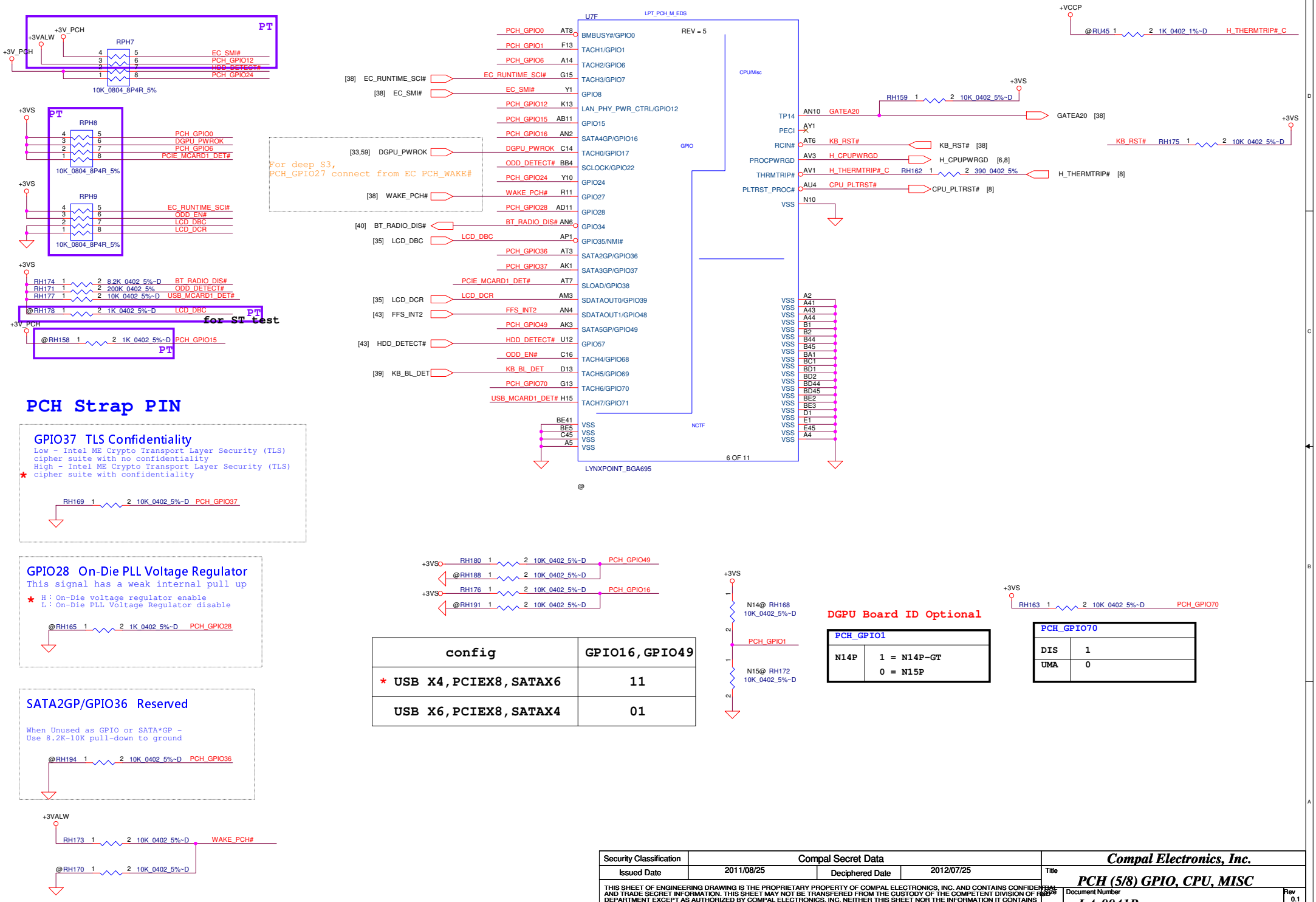
Compal Electronics, Inc.
Title
PCH (3/8) DMI,FDI,PM,GFX,DP
Size
Document Number
LA-9941P
Rev
0.1
Date:
Tuesday, September 03, 2013
Sheet
18
of
62



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.		
Title: PCH (4/8) PCI, USB		
Size	Document Number: LA-9941P	Rev: 0.1
Date: Tuesday, September 03, 2013	Sheet 19 of 62	



PCH Strap PIN

GPIO37 TLS Confidentiality

Low - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality
High - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality

★

RH169 1 2 10K_0402_5%~D PCH_GPIO37

GPIO28 On-Die PLL Voltage Regulator

This signal has a weak internal pull up

★ H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

@RH165 1 2 1K_0402_5%~D PCH_GPIO28

SATA2GP/GPIO36 Reserved

When Unused as GPIO or SATA*GP -
Use 8.2K-10K pull-down to ground

@RH194 1 2 10K_0402_5%~D PCH_GPIO36

+3VALW
RH173 1 2 10K_0402_5%~D WAKE_PCH#
@RH170 1 2 10K_0402_5%~D

+3VS
RH180 1 2 10K_0402_5%~D PCH_GPIO49
@RH188 1 2 10K_0402_5%~D
RH176 1 2 10K_0402_5%~D PCH_GPIO16
@RH191 1 2 10K_0402_5%~D

config	GPIO16,GPIO49
* USB X4,PCIEX8,SATAX6	11
USB X6,PCIEX8,SATAX4	01

+3VS
N14@ RH168 10K_0402_5%~D
PCH_GPIO1
N15@ RH172 10K_0402_5%~D

DGPU Board ID Optional

PCH_GPIO1	
N14P	1 = N14P-GT
	0 = N15P

+3VS
RH163 1 2 10K_0402_5%~D PCH_GPIO70

PCH_GPIO70	
DIS	1
UMA	0

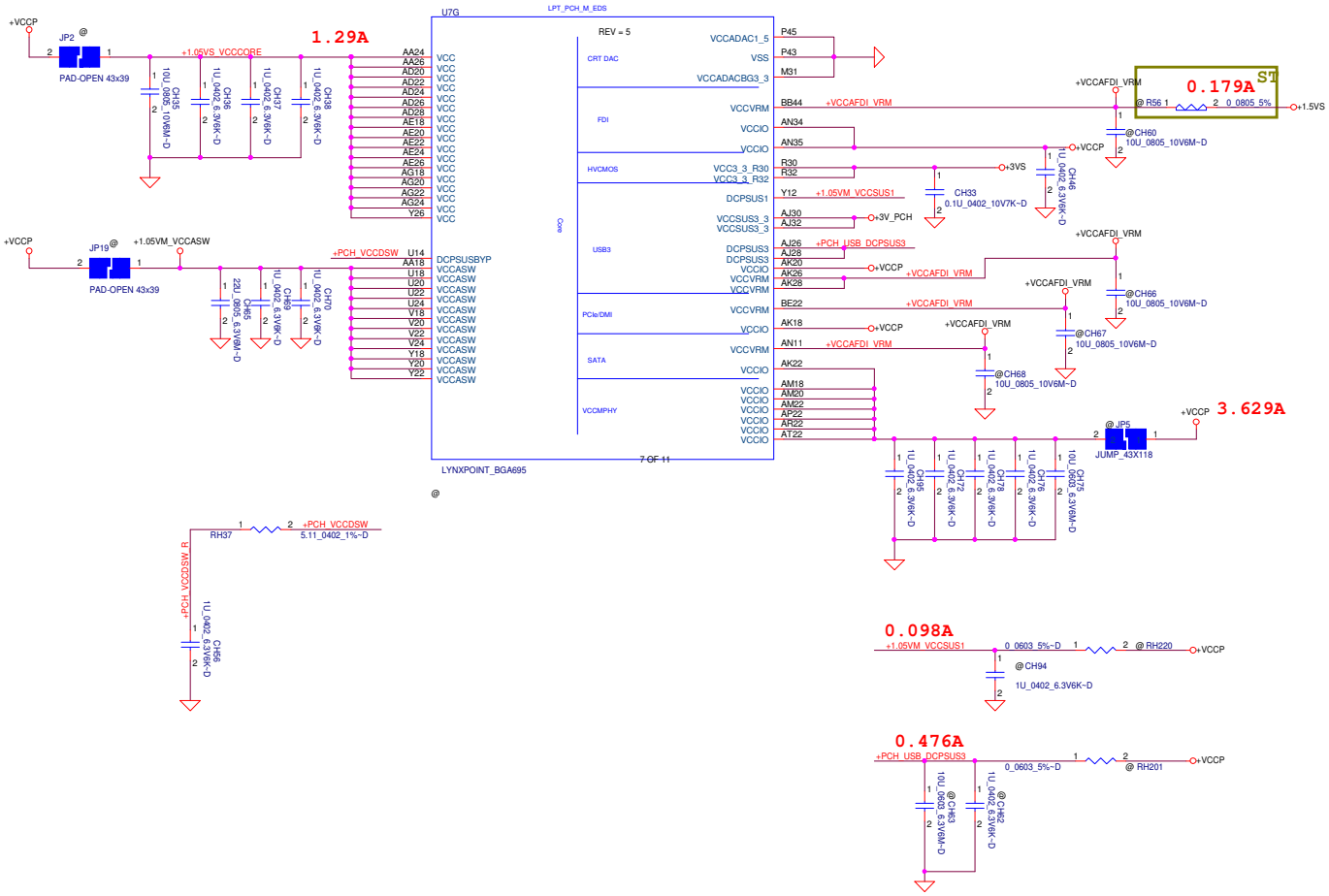
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: PCH (5/8) GPIO, CPU, MISC

Size: C | Document Number: LA-9941P | Rev: 0.1

Date: Tuesday, September 03, 2013 | Sheet 20 of 62



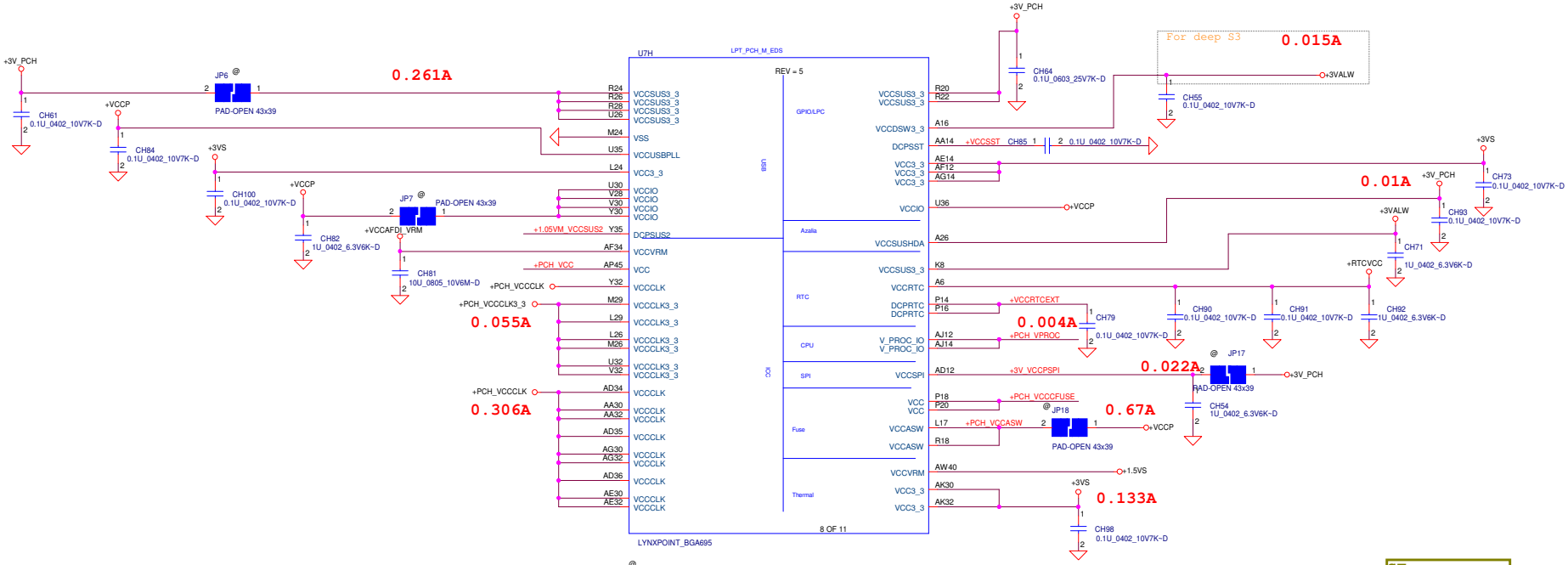
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

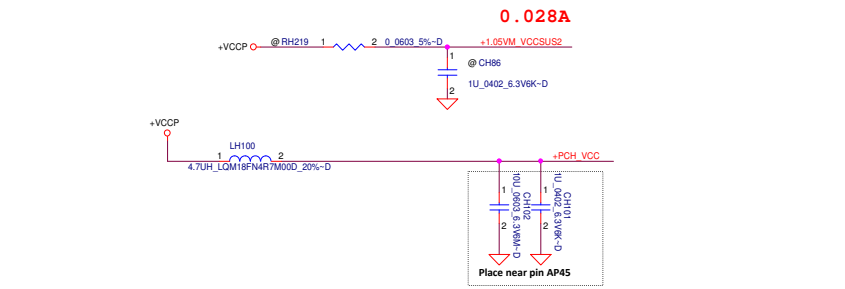
Compal Electronics, Inc.

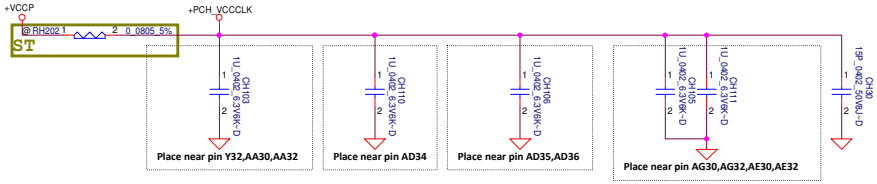
Title: **PCH (6/8) PWR**

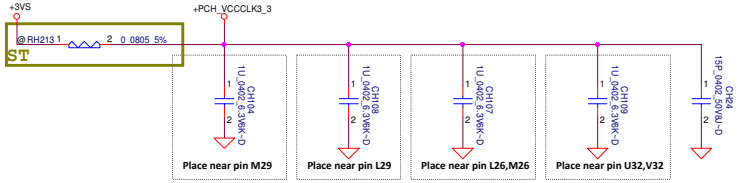
Size	Document Number	Rev
	LA-9941P	0.1

Date: Tuesday, September 03, 2013 | Sheet 21 of 62









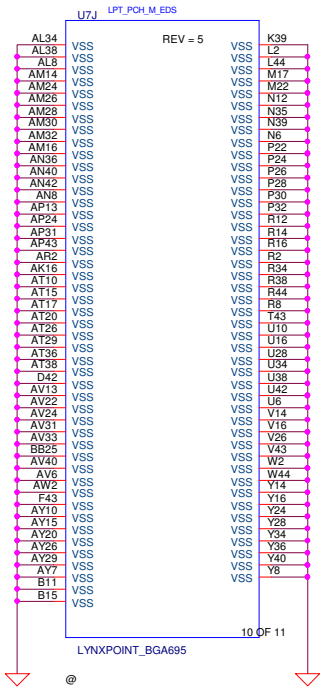
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

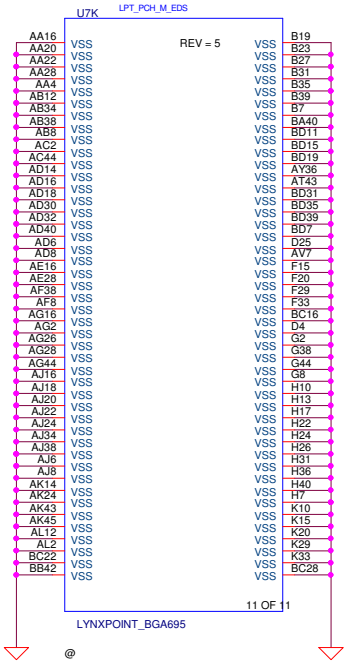
Compal Electronics, Inc.

Title: **PCH (7/8) PWR**

Size	Document Number	Rev
	LA-9941P	0.1

Date: Tuesday, September 03, 2013 | Sheet 22 of 62





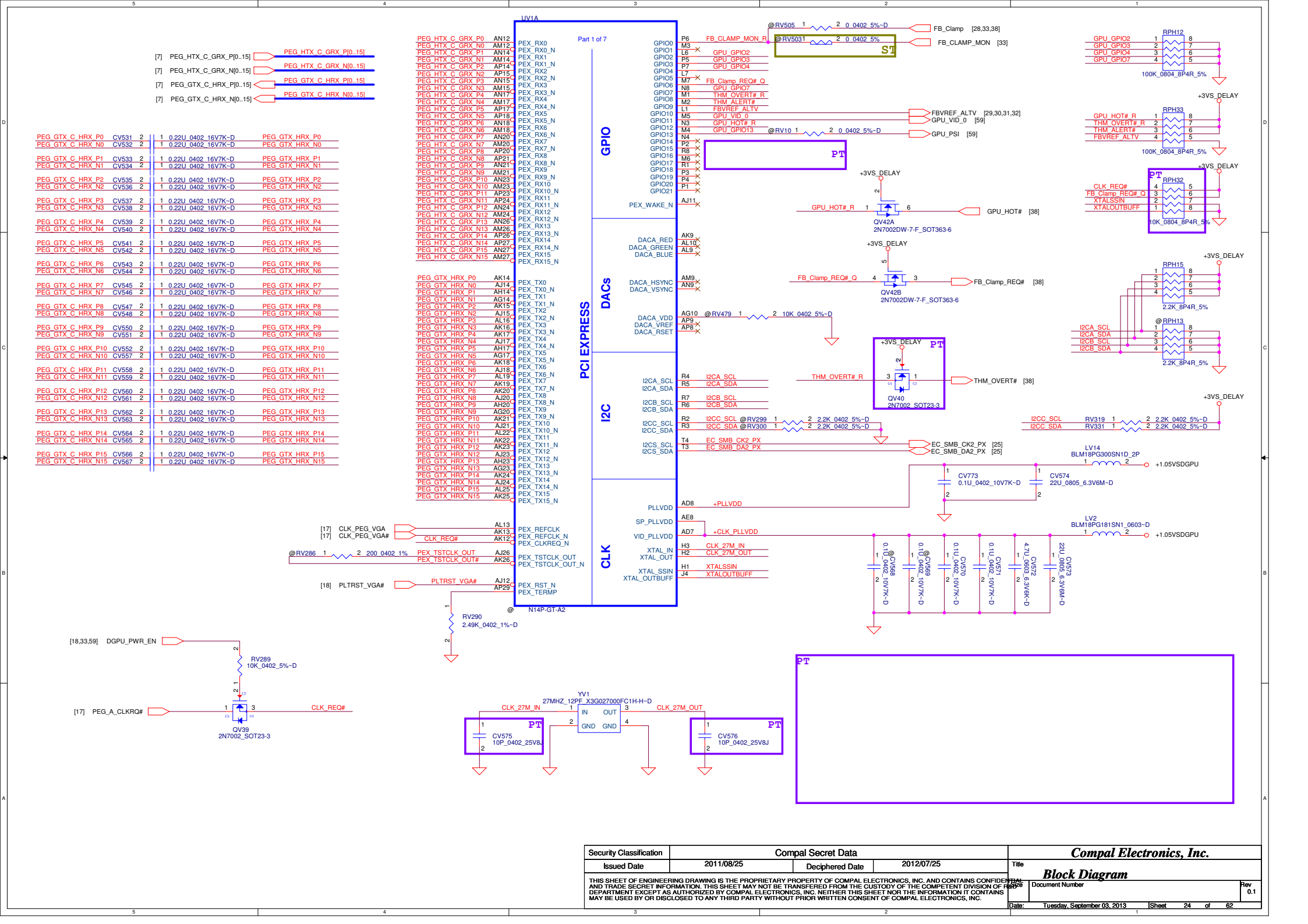
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **PCH (8/8) VSS**

Size	Document Number	Rev
	LA-9941P	0.1

Date: Tuesday, September 03, 2013 Sheet 23 of 62



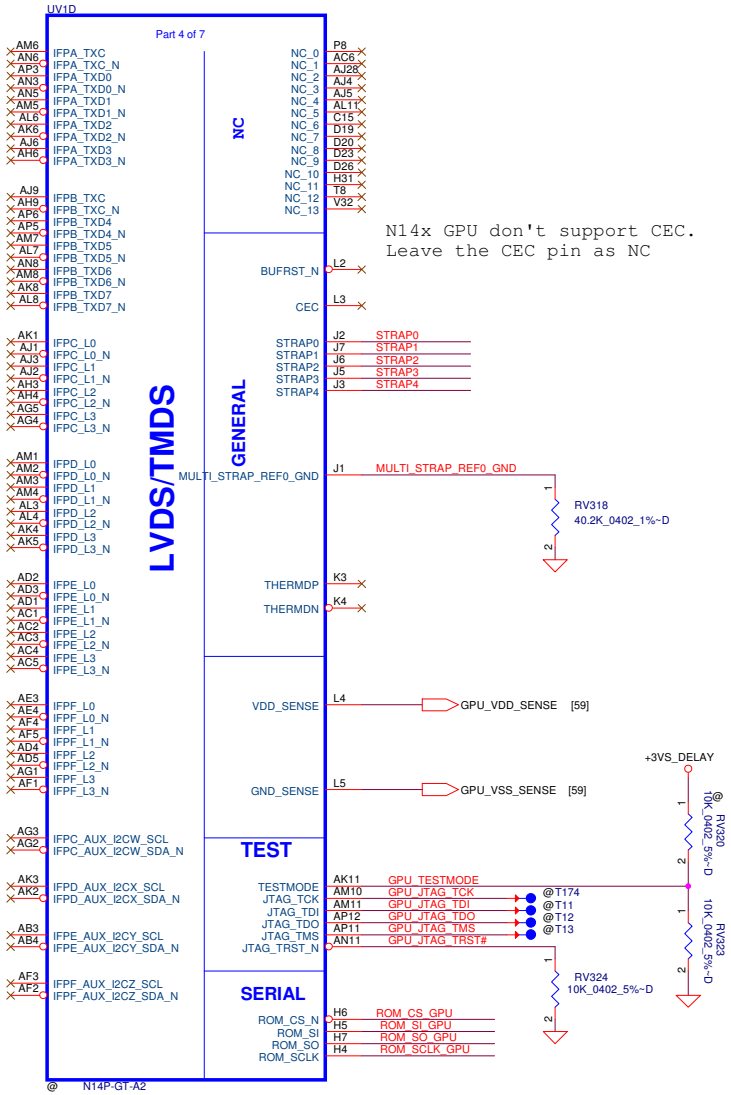
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **Block Diagram**

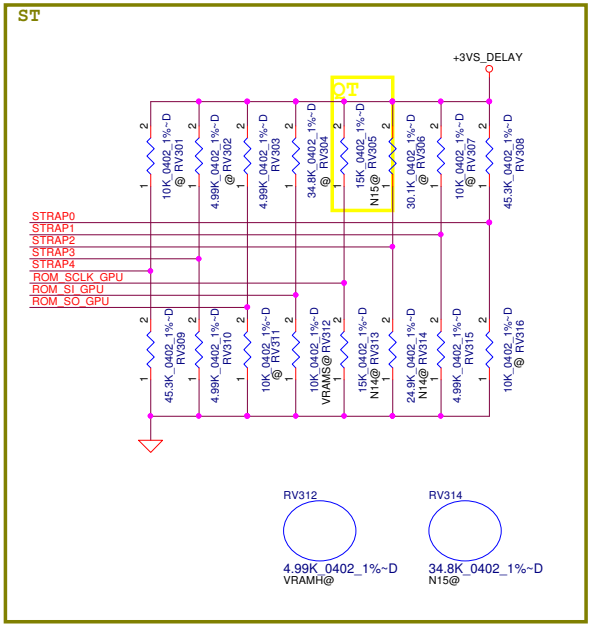
Size	Document Number	Rev
		0.1

Date: Tuesday, September 03, 2013 Sheet 24 of 62



N14x GPU don't support CEC.
Leave the CEC pin as NC

Straps

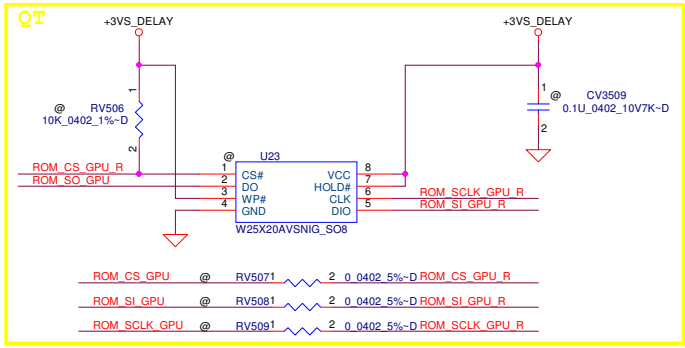


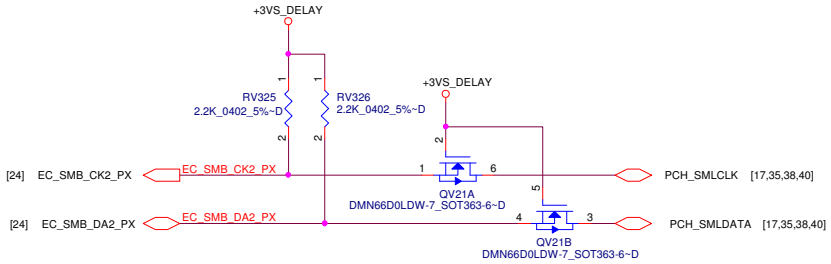
	N14P-GT	N15P-Q1
ROM_SCL	PD 15K	PU 15K
ROM_SI	PD 10K	
ROM_SO	PU 5K	
STRAP[0]	PU 45K	
STRAP[1]	PD 5K	
STRAP[2]	PD 24.9K	PD 35K
STRAP[3]	PD 5K	
STRAP[4]	PD 45K	

Change to PU35K in N15
for use ext ROM

Hynix "0". ROM_SI=PD 5K ohm
Samsung"1". ROM_SI=PD 10K ohm

SPI ROM for N14E-GL (2M bit/256K byte)





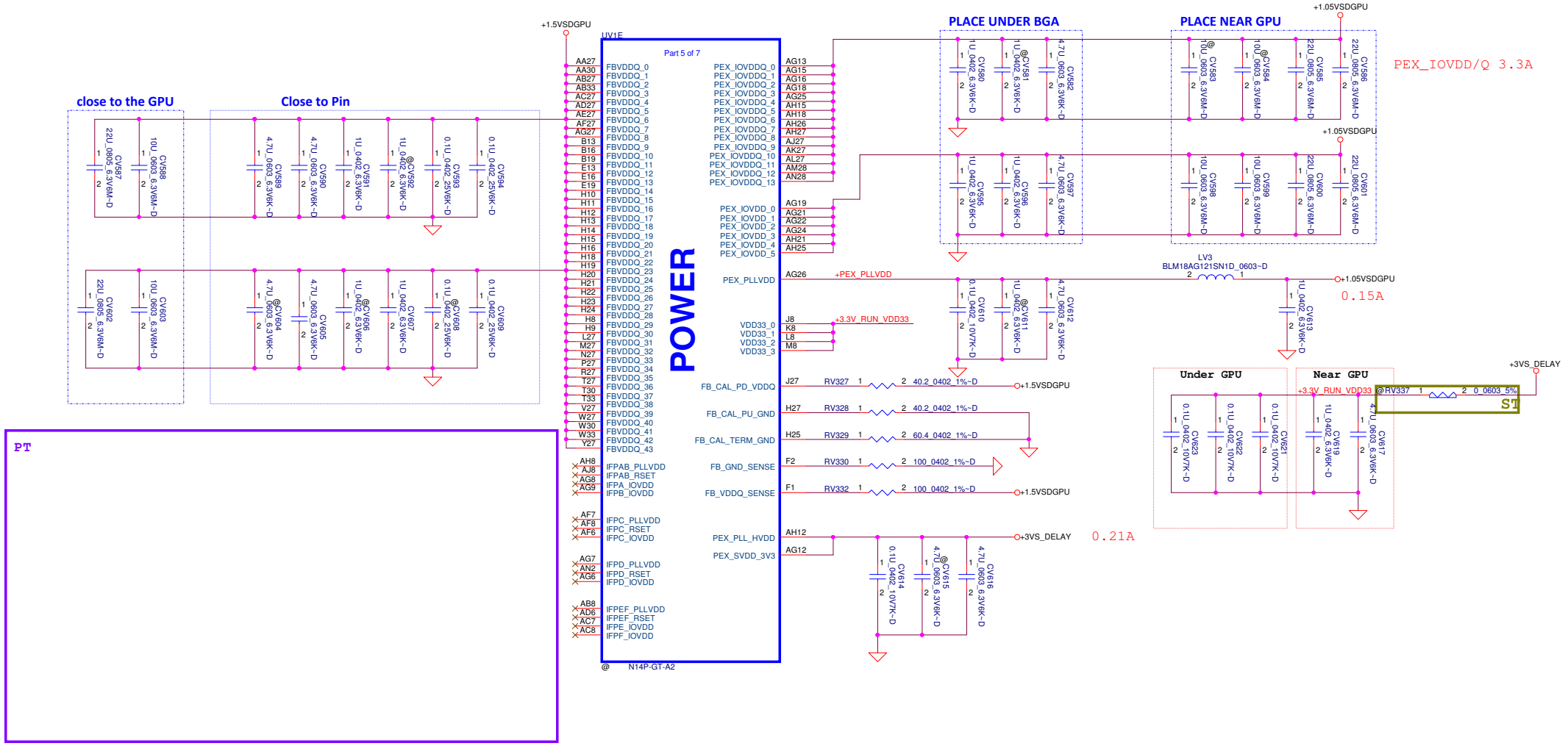
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

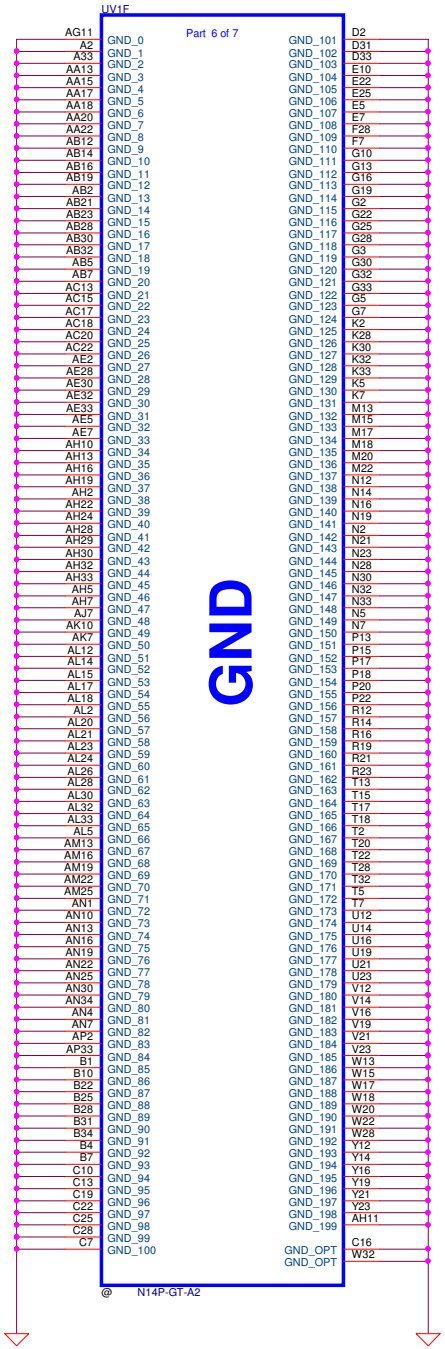
Title: Block Diagram

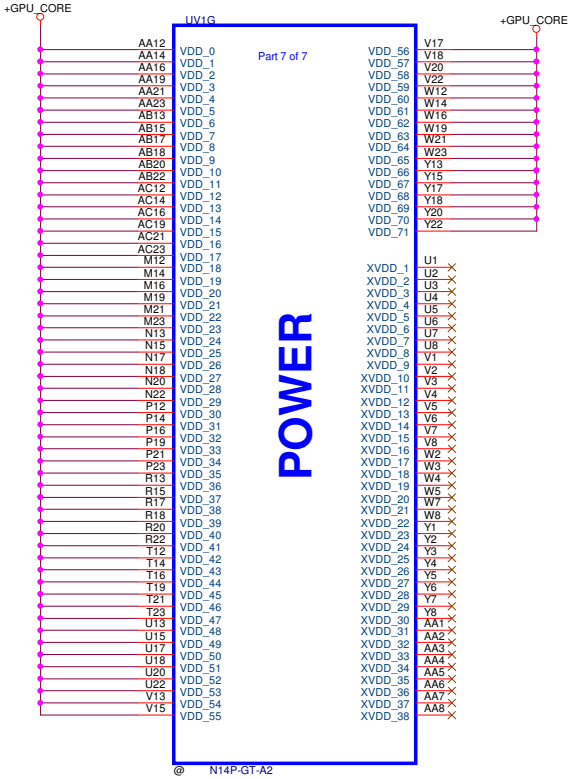
Size | Document Number | Rev 0.1

Date: Tuesday, September 03, 2013 | Sheet 25 of 62



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/08/25	Deciphered Date 2012/07/25	Title: Block Diagram
			Size: Document Number: Rev 0.1
			Date: Tuesday, September 03, 2013 Sheet 26 of 62





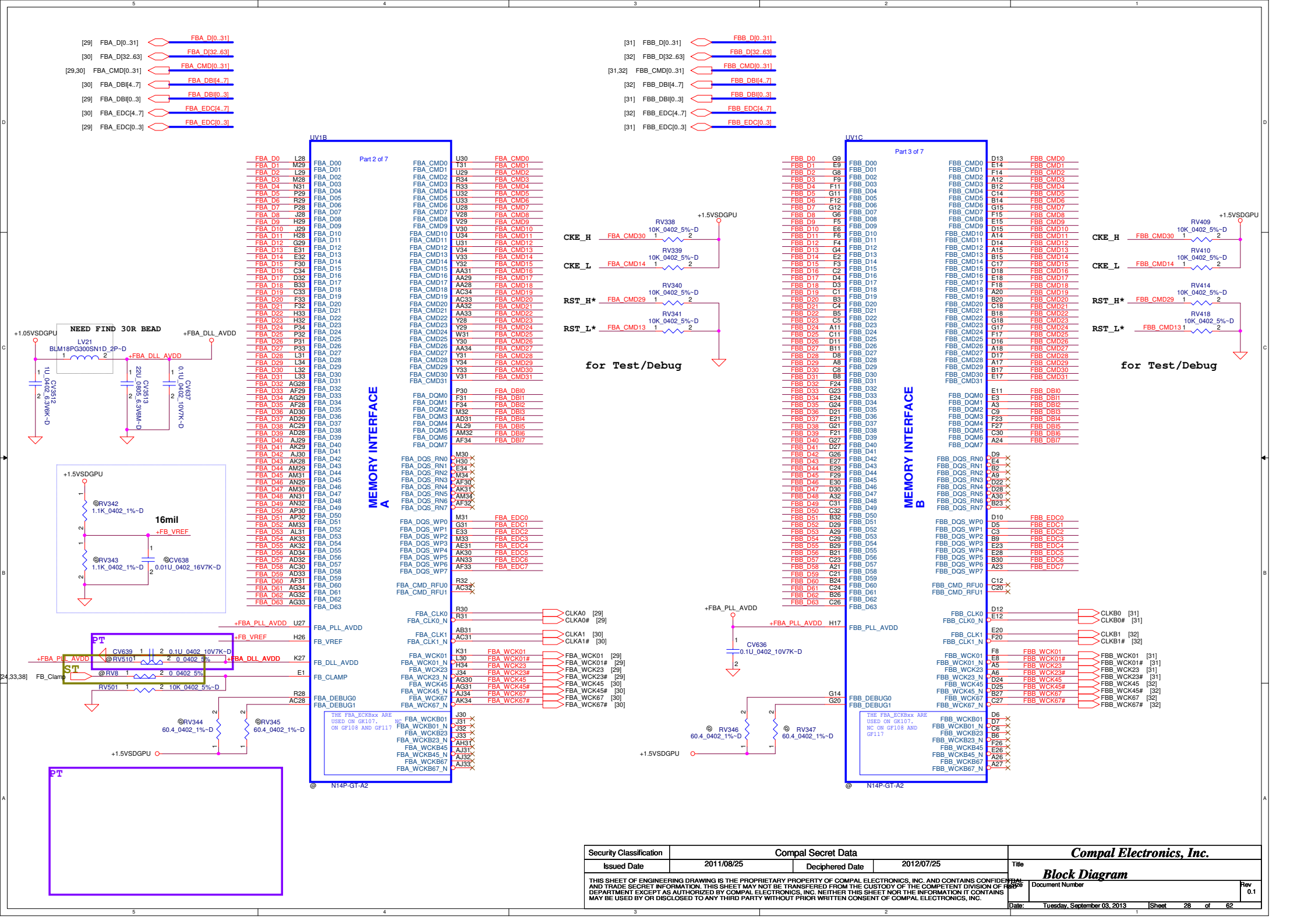
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **Block Diagram**

Size	Document Number	Rev
		0.1

Date: Tuesday, September 03, 2013 Sheet 27 of 62



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **Block Diagram**

Size	Document Number	Rev
		0.1

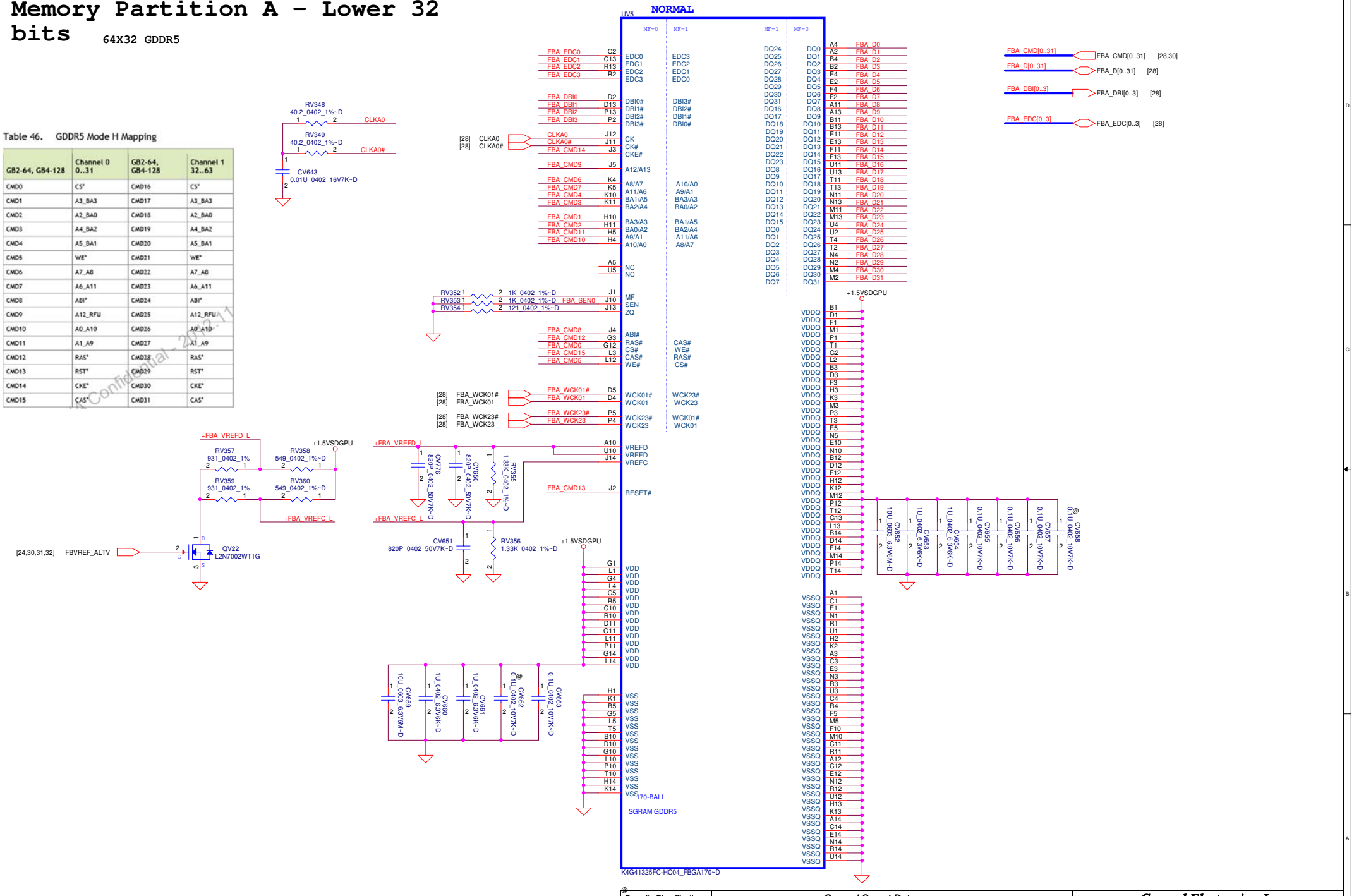
Date: Tuesday, September 03, 2013 Sheet 28 of 62

Memory Partition A – Lower 32 bits

64X32 GDDR5

Table 46. GDDR5 Mode H Mapping

GB2-64, GB4-128	Channel 0 0..31	GB2-64, GB4-128	Channel 1 32..63
CMD0	CS*	CMD16	CS*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	ABI*	CMD24	ABI*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **Block Diagram**

Size	Document Number	Rev
		0.1

Date: Tuesday, September 03, 2013 | Sheet 29 of 62

Memory Partition A – Upper 32 bits

Table 46. GDDR5 Mode H Mapping

GB2-64, GB4-128	Channel 0 0..31	GB2-64, GB4-128	Channel 1 32..63
CMD0	CS*	CMD16	CS*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	ABI*	CMD24	ABI*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*

NORMAL

UV6

K4G41325FC-HC04_FBGA170-D

170-BALL SGRAM GDDR5

@

Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: Block Diagram

Size	Document Number	Rev
		0.1

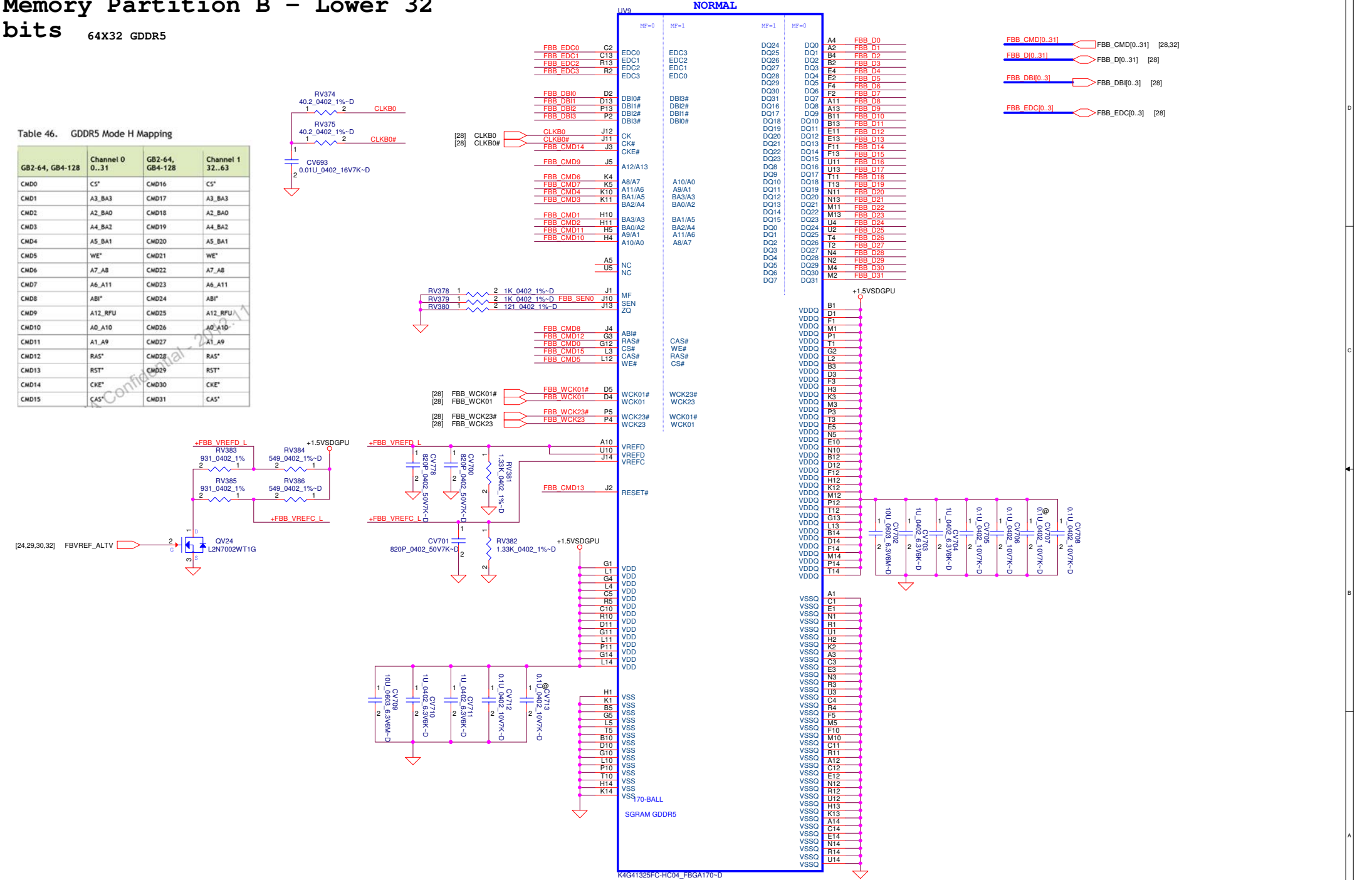
Date: Tuesday, September 17, 2013 Sheet 30 of 62

Memory Partition B – Lower 32 bits

64X32 GDDR5

Table 46. GDDR5 Mode H Mapping

GB2-64, GB4-128	Channel 0 0..31	GB2-64, GB4-128	Channel 1 32..63
CMD0	CS*	CMD16	CS*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	ABI*	CMD24	ABI*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: Block Diagram

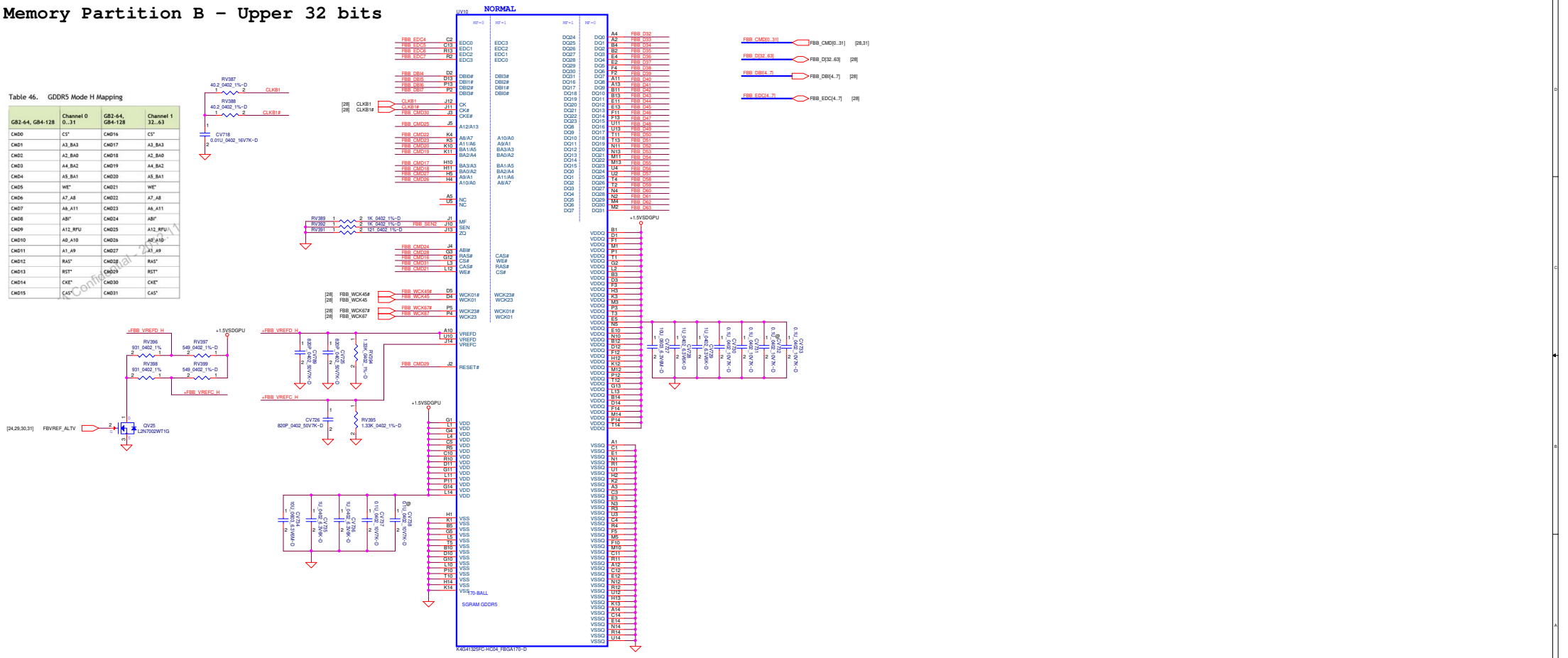
Size | Document Number | Rev 0.1

Date: Tuesday, September 03, 2013 | Sheet 31 of 62

Memory Partition B – Upper 32 bits

Table 46. GDDR5 Mode H Mapping

GB2-64, GB4-128	Channel 0 0..31	GB2-64, GB4-128	Channel 1 32..63
CMD0	CS*	CMD16	CS*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	ABI*	CMD24	ABI*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

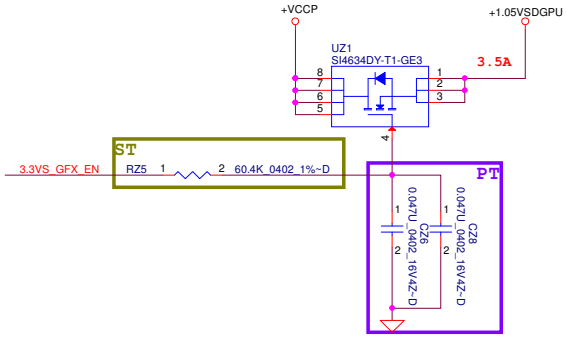
Compal Electronics, Inc.

Title: **Block Diagram**

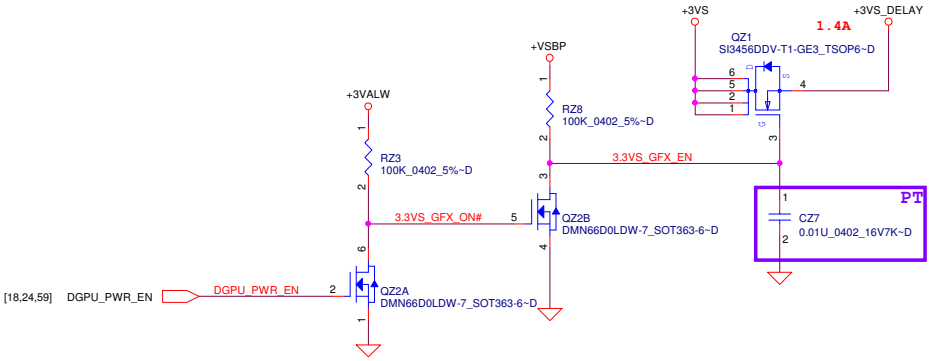
Size	Document Number	Rev
		0.1

Date: Tuesday, September 03, 2013 | Sheet 32 of 82

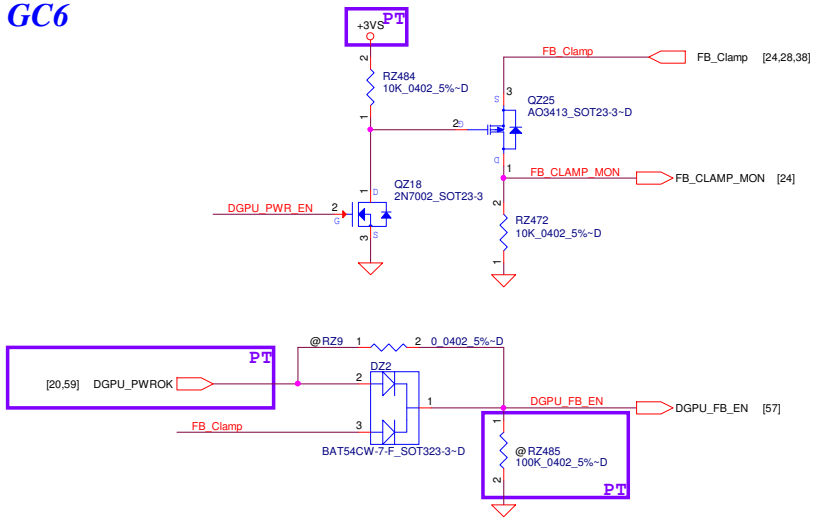
+1.05VS to +1.05VSDGPU



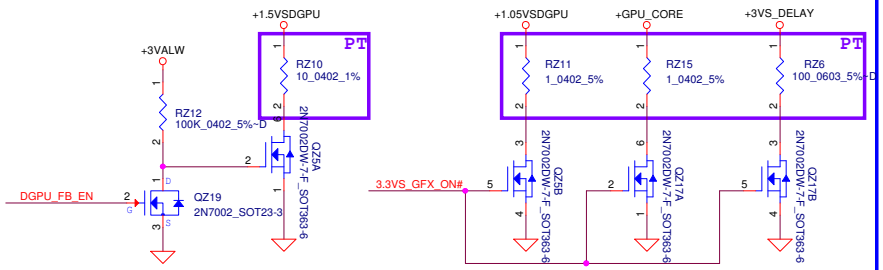
+3VS to +3VS_DELAY



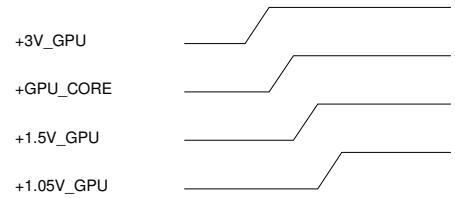
GC6



Discharge

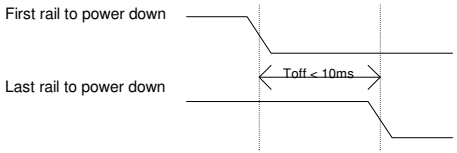


GPU Power Up Power Rail Sequence

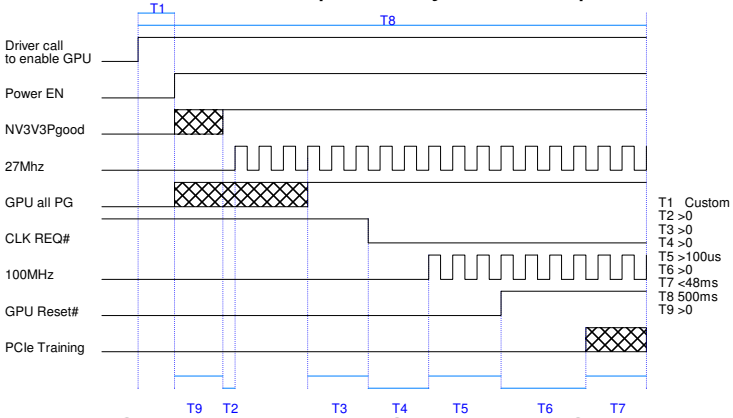


The ramp time for any rail must be more than 40us.

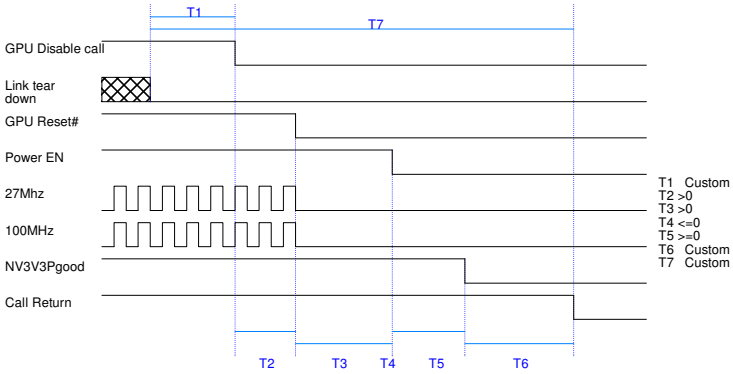
GPU Power Down Sequence



GPU Power Up Sub-system Sequence



GPU Power Down Sub-system Sequence



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

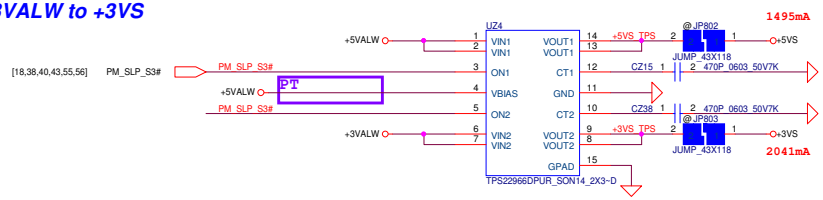
Compal Electronics, Inc.

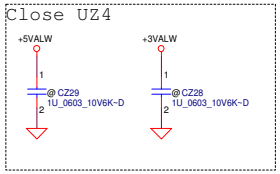
Title: **Block Diagram**

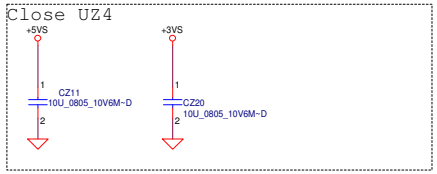
Size | Document Number | Rev 0.1

Date: Tuesday, September 03, 2013 | Sheet 33 of 62

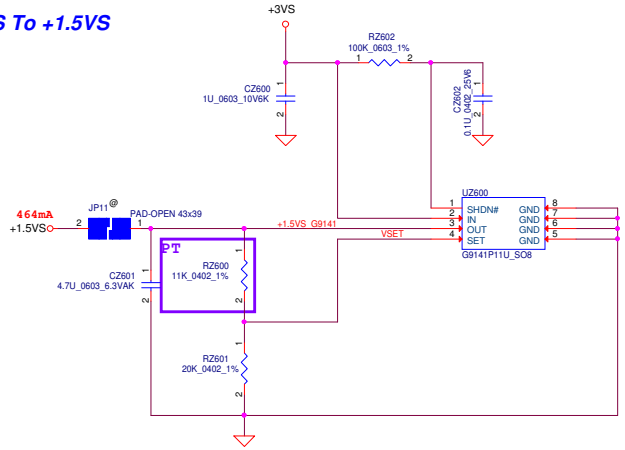
+5VALW to +5VS
+3VALW to +3VS



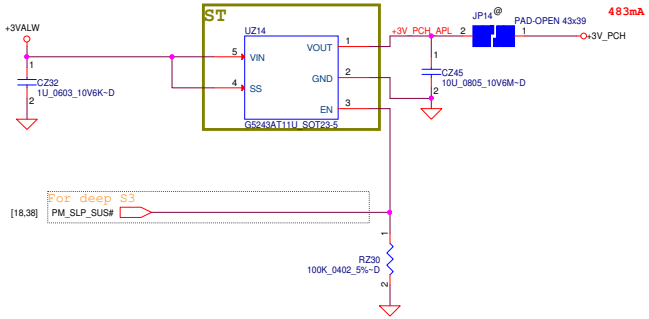




+3VS To +1.5VS



+3VALW to +3V_PCH



Discharge

Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: DC/DC Interface

Size	Document Number	Rev
	LA-9941P	0.1

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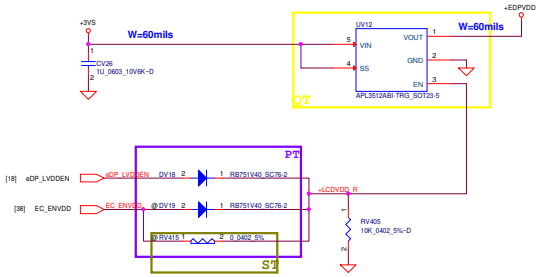
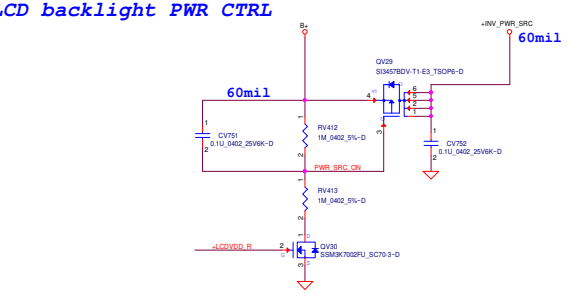
eDP Redriver

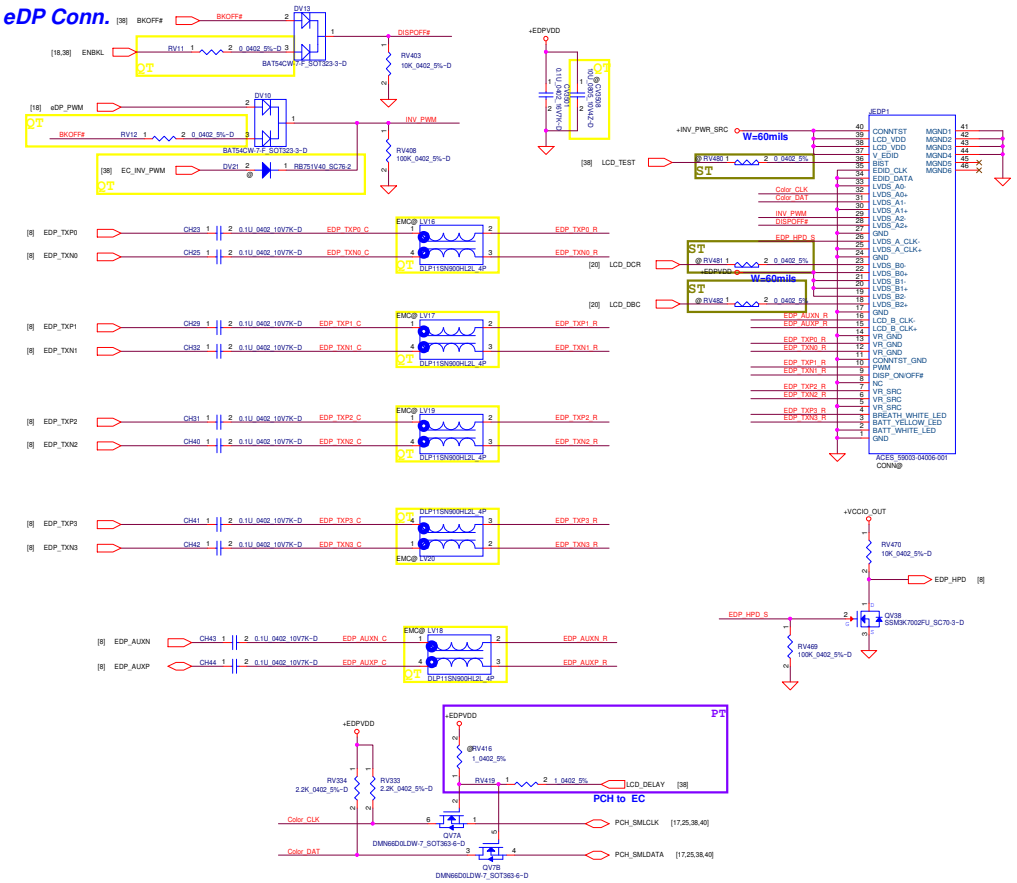
LCD PWR CTRL



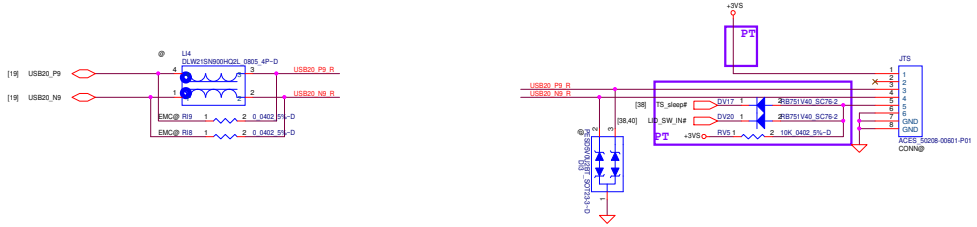
LCD backlight PWR CTRL



eDP Conn.



Touch Screen



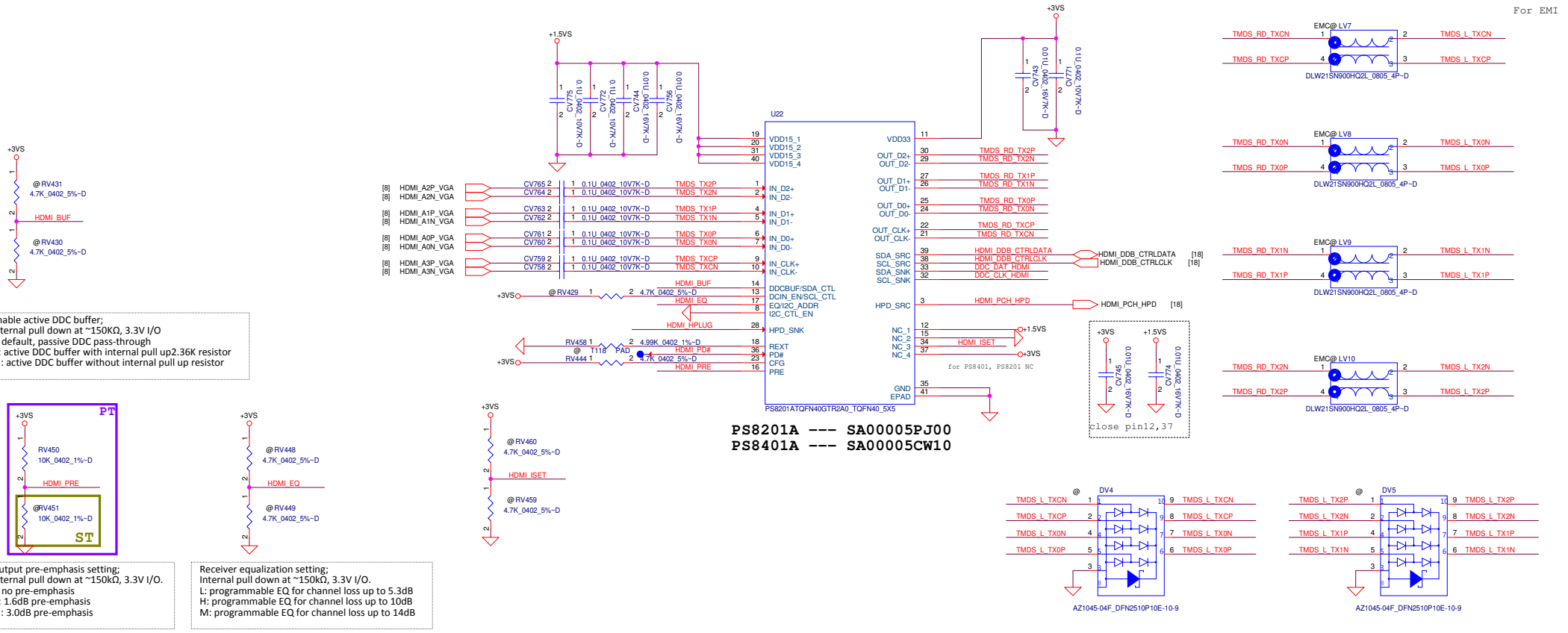
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.			
Title	eDP /camera conn.		
Size	Document Number		Rev
	LA-9911P		0.1
Date:	Wednesday, September 04, 2013	Sheet	35 of 62

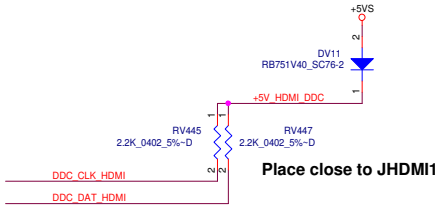
HDMI Active Level Shift(ALS type)

Place close to JHDMI1

For EMI



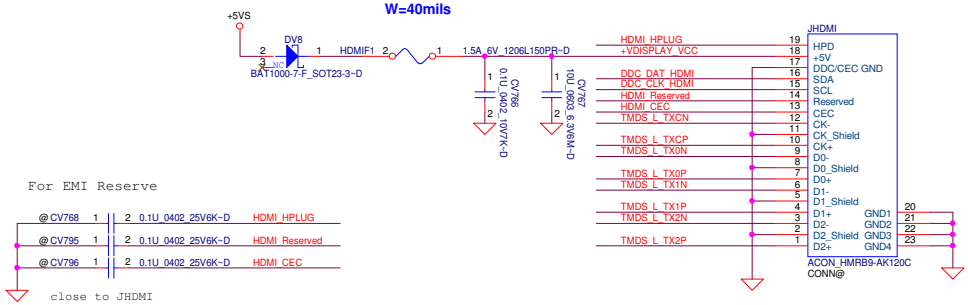
HDMI DDC



Place close to JHDMI1

HDMI conn

W=40mils



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: HDMI

Size	Document Number	Rev
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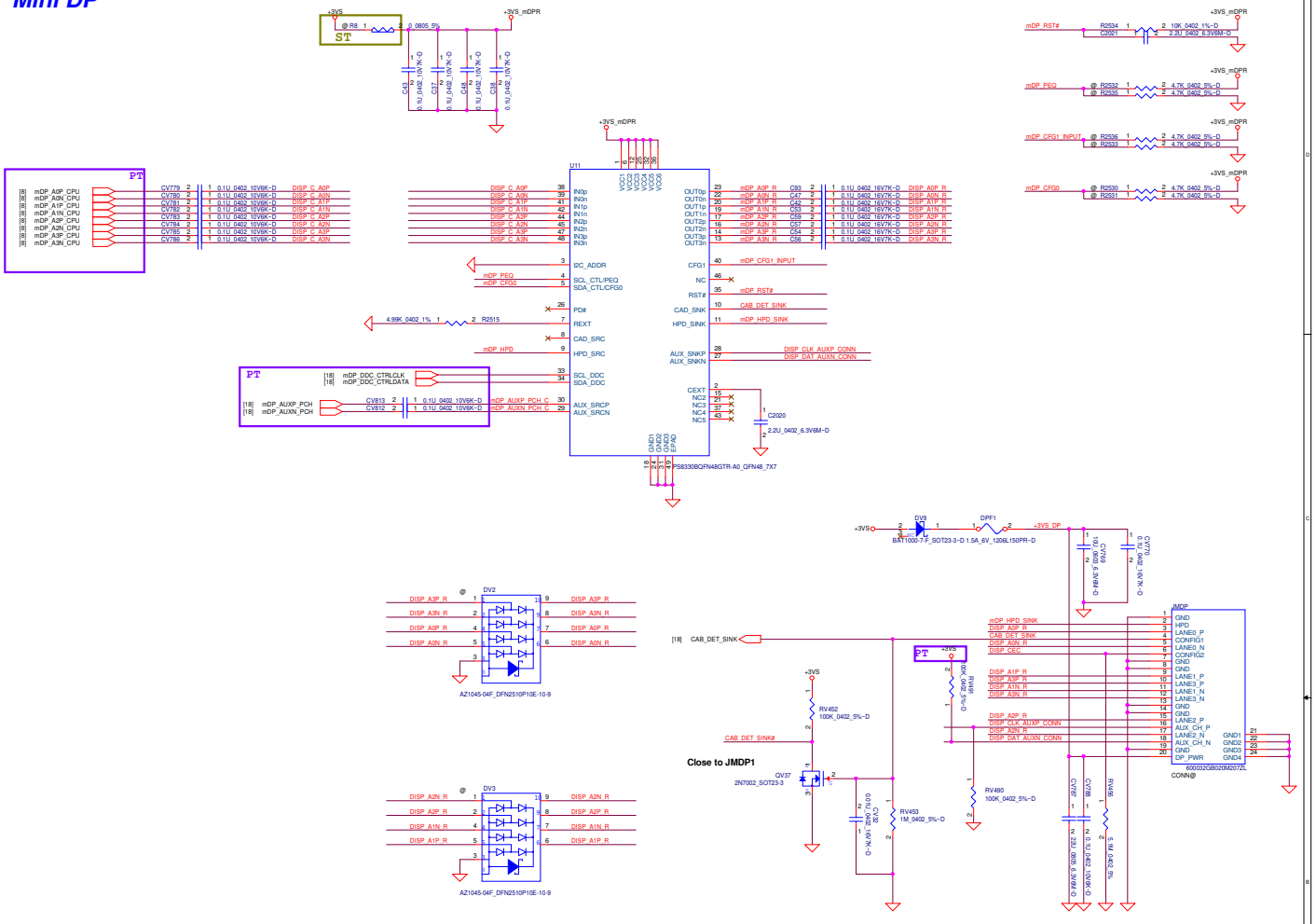
Mini DP

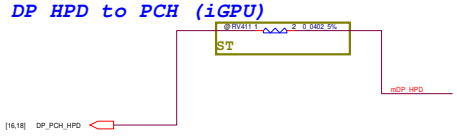
DP Re-Driver config



DDC Dongle SW for DP

PT

DP HPD to PCH (iGPU)

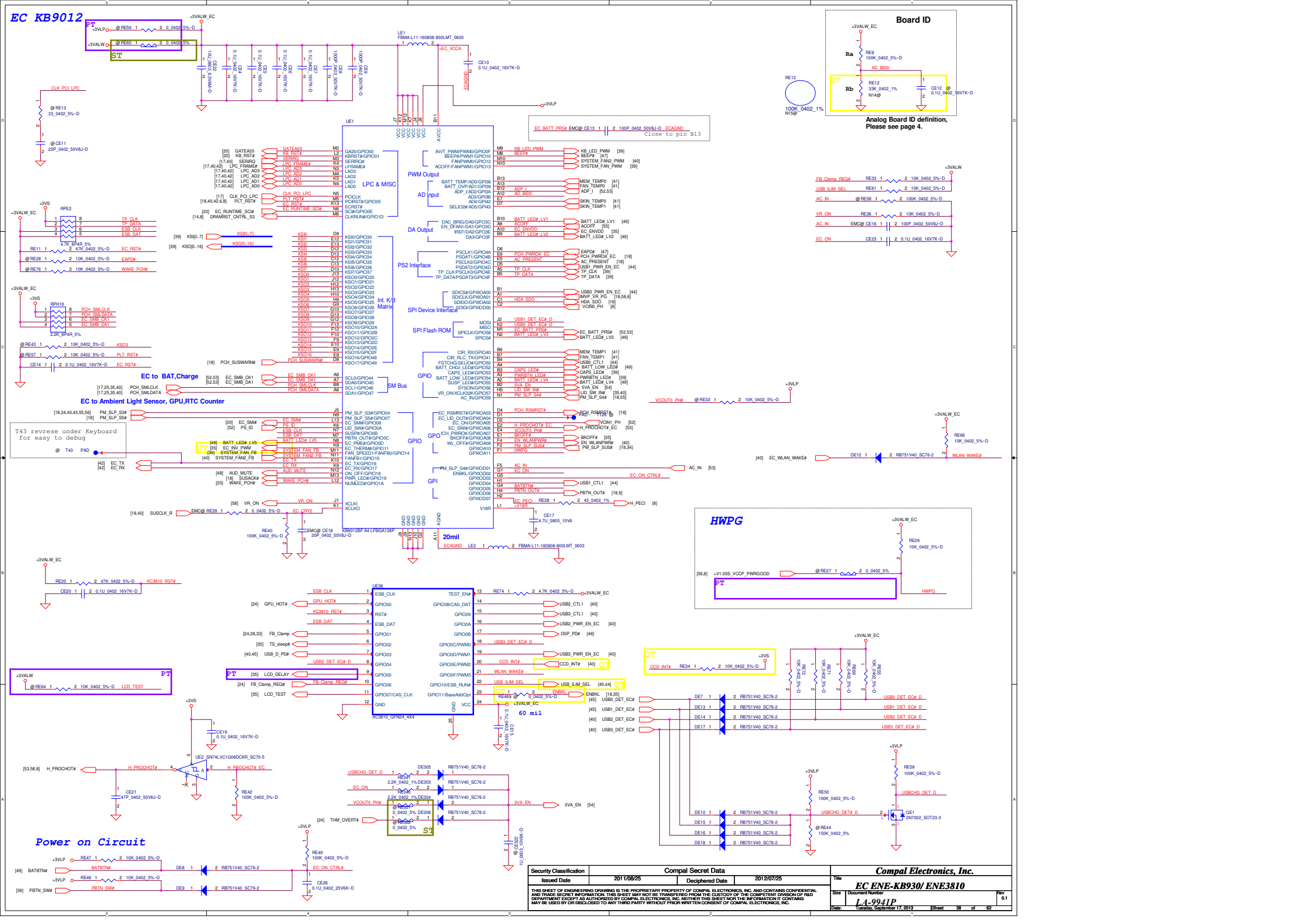


DP HPD for DGPU output (Optimus)

PT

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/08/25	Deciphered Date	2012/07/25
Title	Mini DP		
Size: Custom	Document Number: LA-9941P		Rev: 0.1
Date: Tuesday, September 03, 2013	Sheet 37 of 62		

EC KB9012


Board ID
Analog Board ID definition,
Please see page 4.
EC to BAT,Charge
EC to Ambient Light Sensor, GPU,RTC Counter
T43 revrese under Keyboard
for easy to debug
HWPG
Power on Circuit
20mil
60 mil
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
SPI Device Interface
SPI Flash ROM
Int. K/B Matrix
SM Bus
GPIO
GPO
GPI
Compal Electronics, Inc.
EC ENE-KB930/ ENE3810
LA-9941P
Security Classification: Compal Secret Data
Issued Date: 2011/08/25
Deciphered Date: 2012/07/25
Tuesday, September 17, 2013
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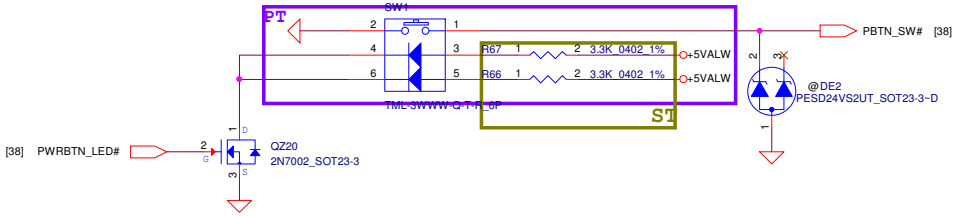
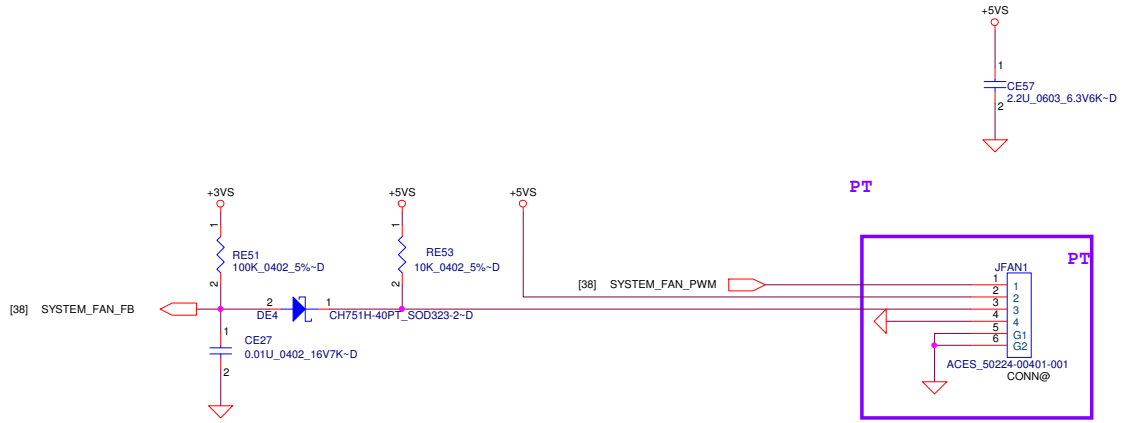
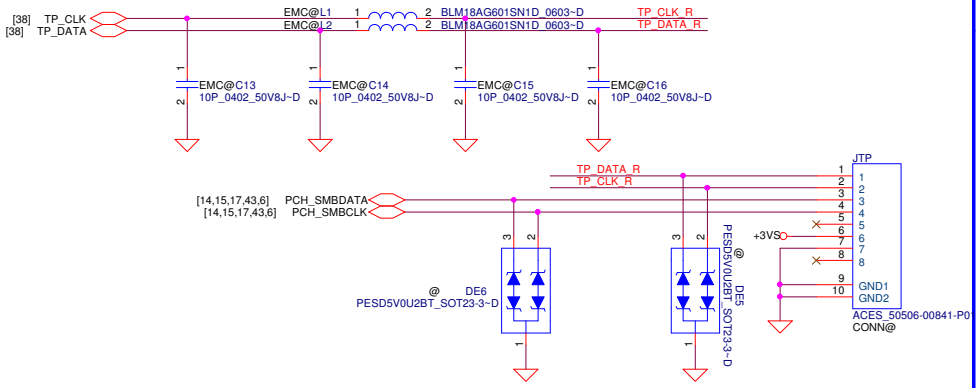
Power on Button



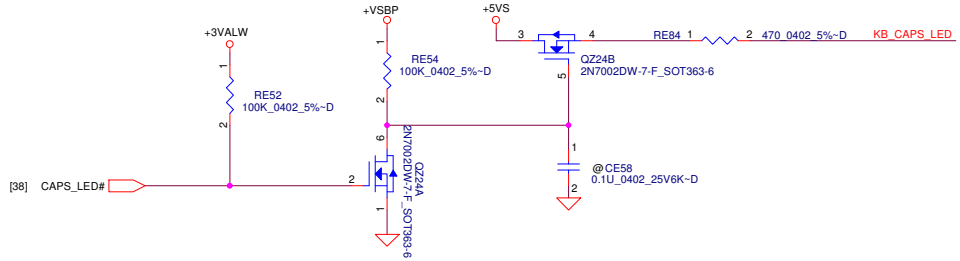
PWM FAN

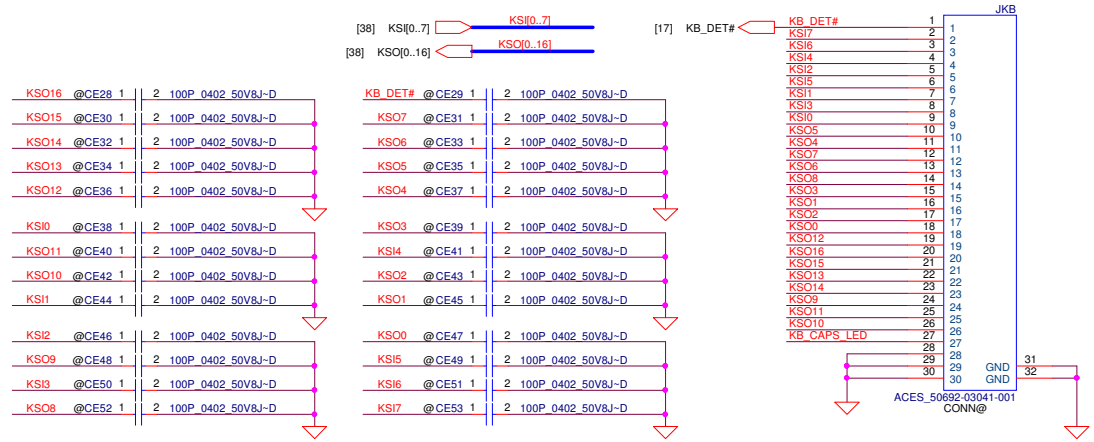


Touch pad

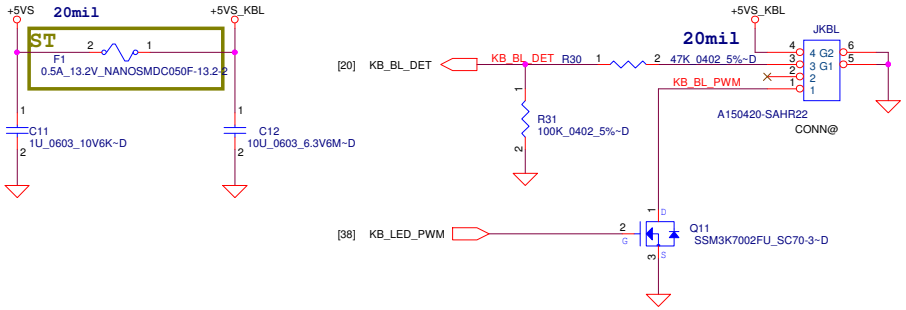


INT_KBD CONN





Keyboard back light



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.			
Title: SW/TP/SCREW			
Size: Custom	Document Number: LA-9941P		Rev: 0.1
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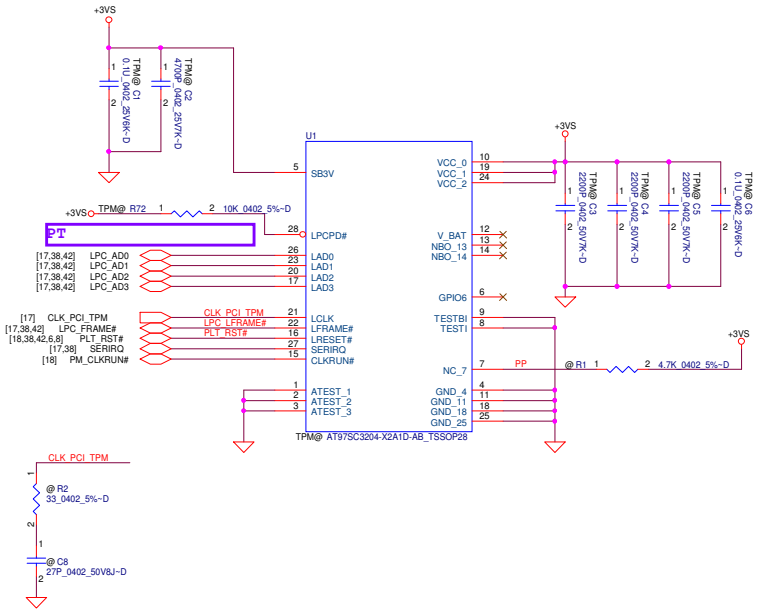
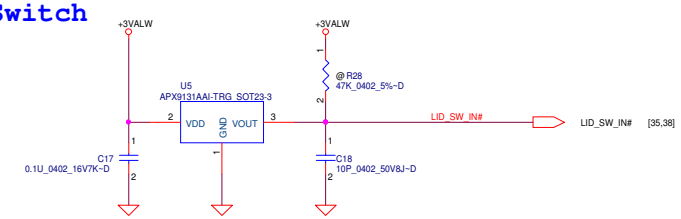
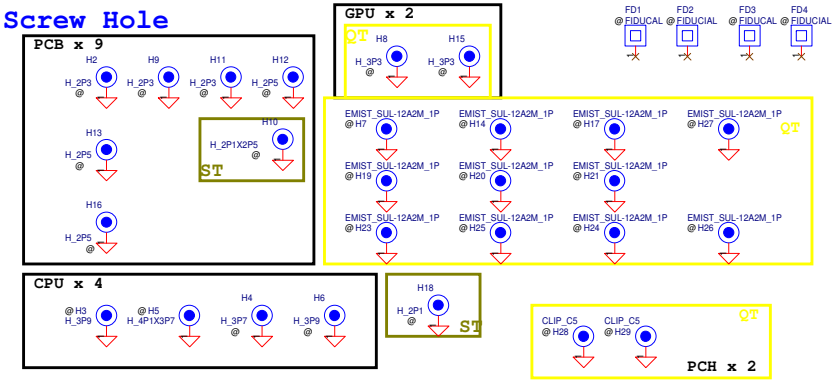
ATMEL TPM



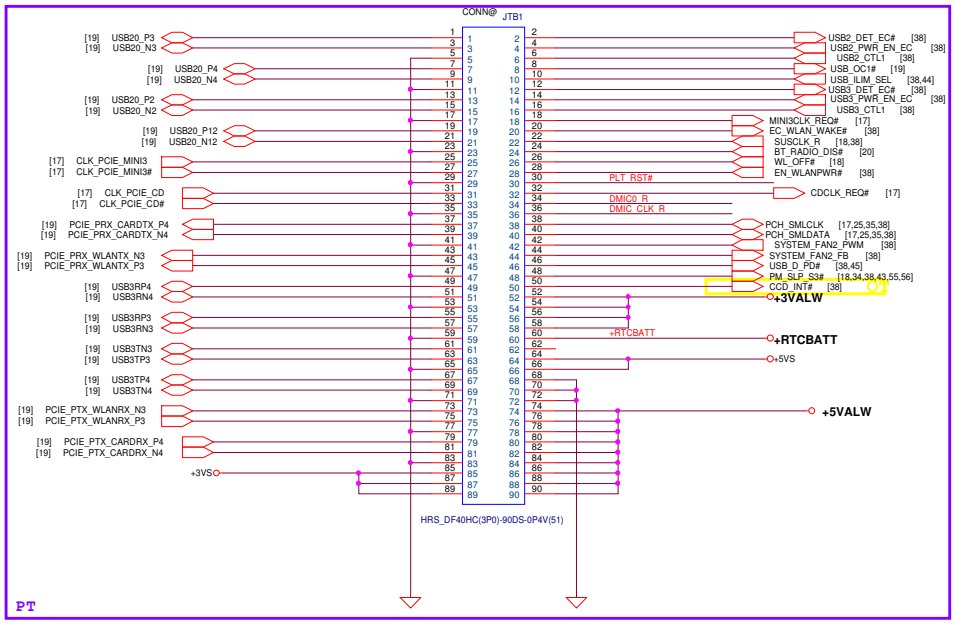
Lid Switch

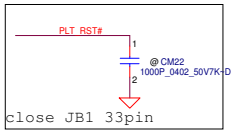


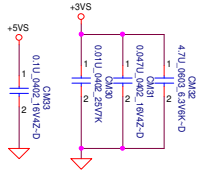
Screw Hole

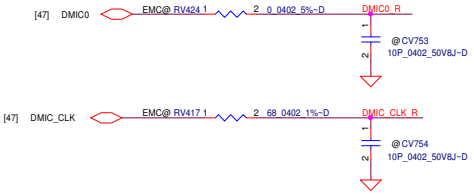


M/B to D/B conn.







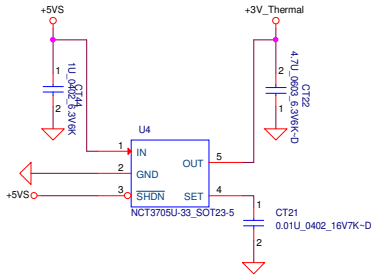


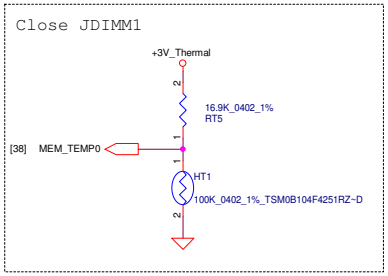
Wedcam PWR CTRL

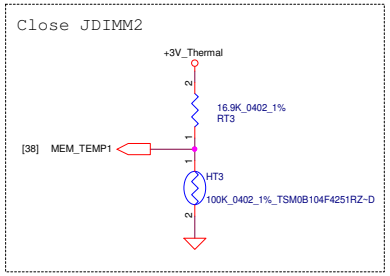
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

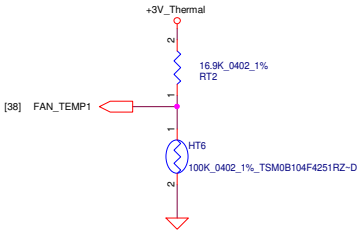
Compal Electronics, Inc.			
Title: CONN & LID			
Size	Document Number: LA-9941P		Rev: 0.1
Date: Thursday, September 05, 2013	Sheet 40 of 62		

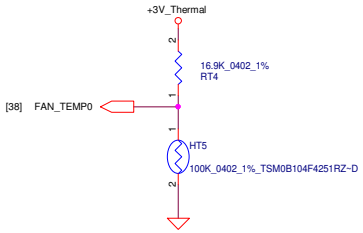
Thermal sensor

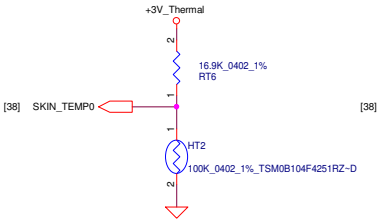


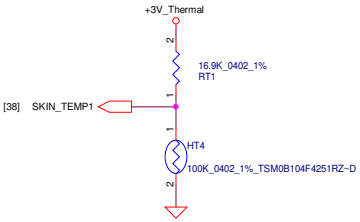












Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: Thermal Sensor EMC1412

Size	Document Number	Rev
Custom	LA-9941P	0.1

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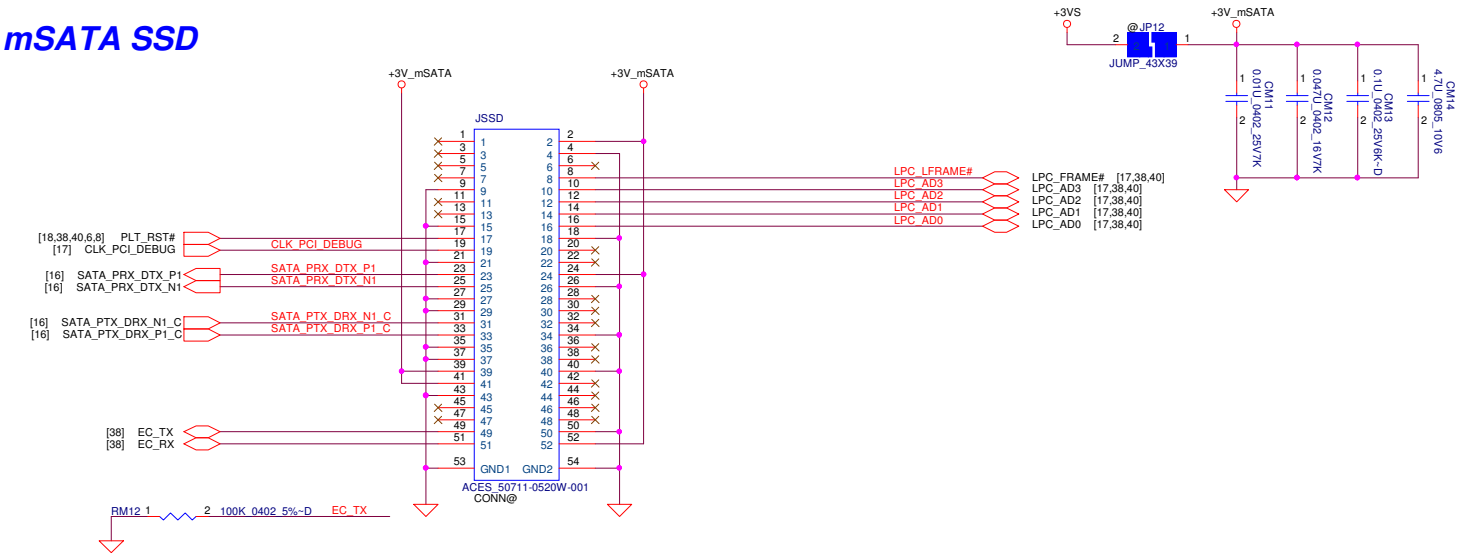
WLAN / BT4.0 PCIE Mini Card

Pin#	Assignment	Description	Pin#	Assignment	Description
1	N/A	N/A	27	GND	Return Current Path
2	+3.3V	3.3V source	28	N/A	N/A
3	N/A	N/A	29	GND	Return Current Path
4	GND	Return Current Path	30	N/A	N/A
5	N/A	N/A	31	-A (port 1)	SATA Differential RX- based on SSD
6	N/A	N/A	32	N/A	N/A
7	N/A	N/A	33	+A (port 1)	SATA Differential RX+ based on SSD
8	N/A	N/A	34	GND	Return Current Path
9	GND	Return Current Path	35	GND	Return Current Path
10	N/A	N/A	36	Reserved	No Connect
11	N/A	N/A	37	GND	Return Current Path
12	N/A	N/A	38	Reserved	No Connect
13	N/A	N/A	39	+3.3V	3.3V Source
14	N/A	N/A	40	GND	Return Current Path
15	GND	Return Current Path	41	+3.3V	3.3V Source
16	N/A	N/A	42	N/A	N/A
17	N/A	N/A	43	N/A	N/A
18	GND	Return Current Path	44	N/A	N/A
19	N/A	N/A	45	Reserved	N/A
20	N/A	N/A	46	N/A	N/A
21	GND	Return Current Path	47	Reserved	N/A
22	N/A	N/A	48	N/A	N/A
23	+B(port 1)	SATA Differential	49	DA/DSS	Device Activity / Disable Staggered Spin-up
24	+3.3V	3.3V Source	50	GND	Return Current Path
25	-B(port 1)	SATA Differential	51	Presence Detection	Shall be pulled to GND by device
26	GND	Return Current Path	52	+3.3V	3.3V Source

mSATA SSD



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

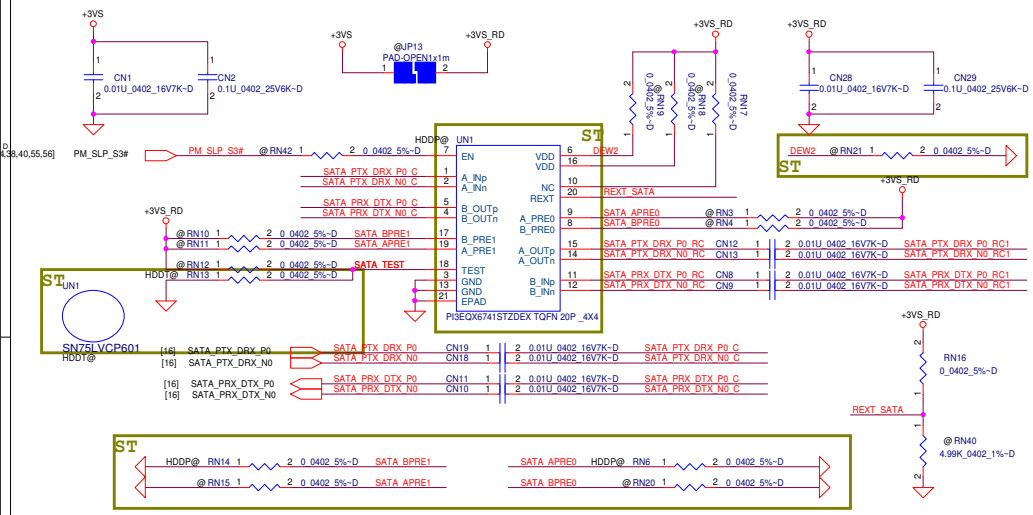
Compal Electronics, Inc.

Title: WLAN/WWAN/SIM/BT

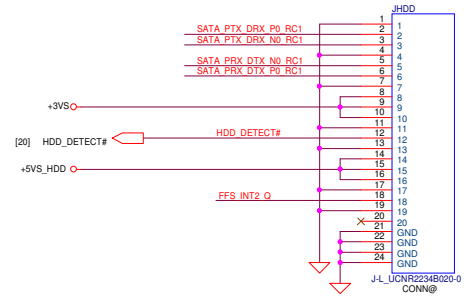
Size: Custom | Document Number: LA-9941P | Rev: 0.1

Date: Tuesday, September 03, 2013 | Sheet 42 of 62

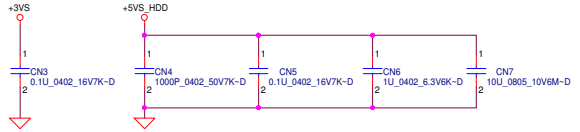
SATA III Re-driver for HDD



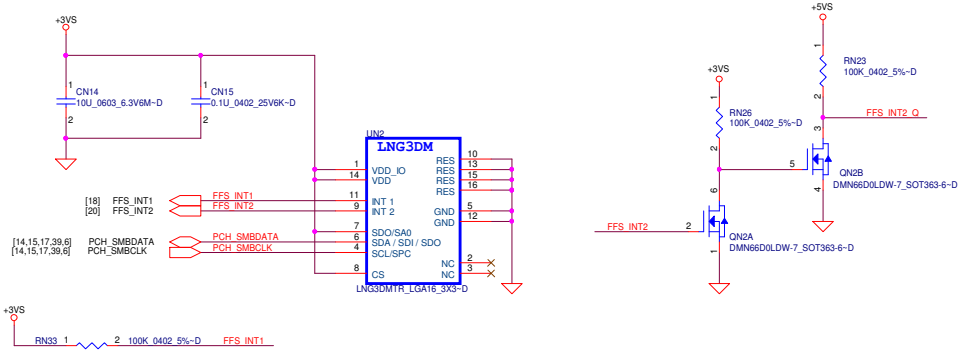
HDD CONN



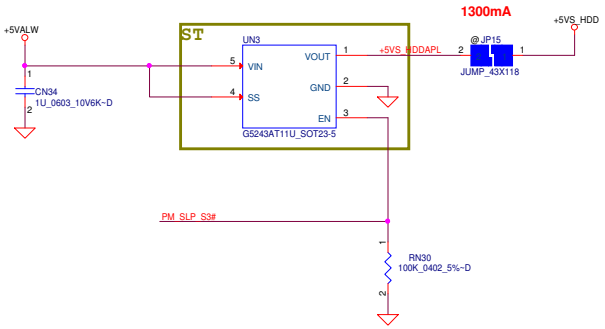
Place near HDD CONN (JHDD1)



Free Fall Sensor



HDD power control for AOAC



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **DC/DC INTERFACE**

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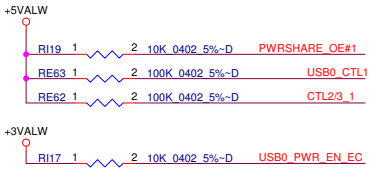
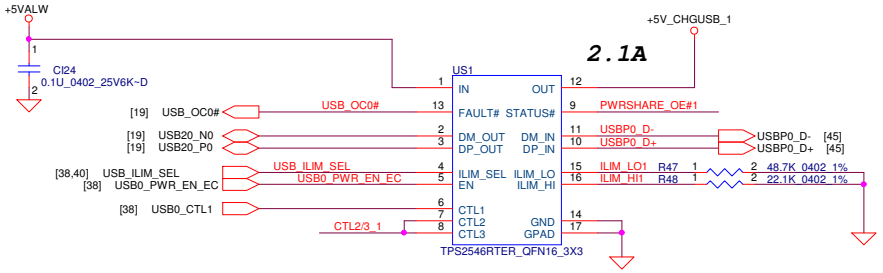
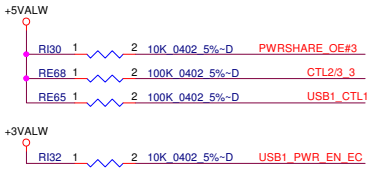
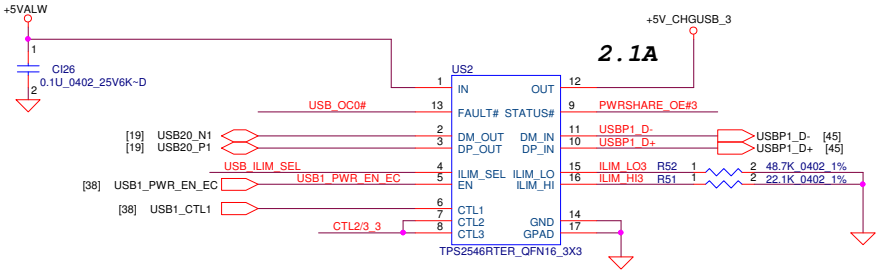
USB Powershare









Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Title	USB Powershare		
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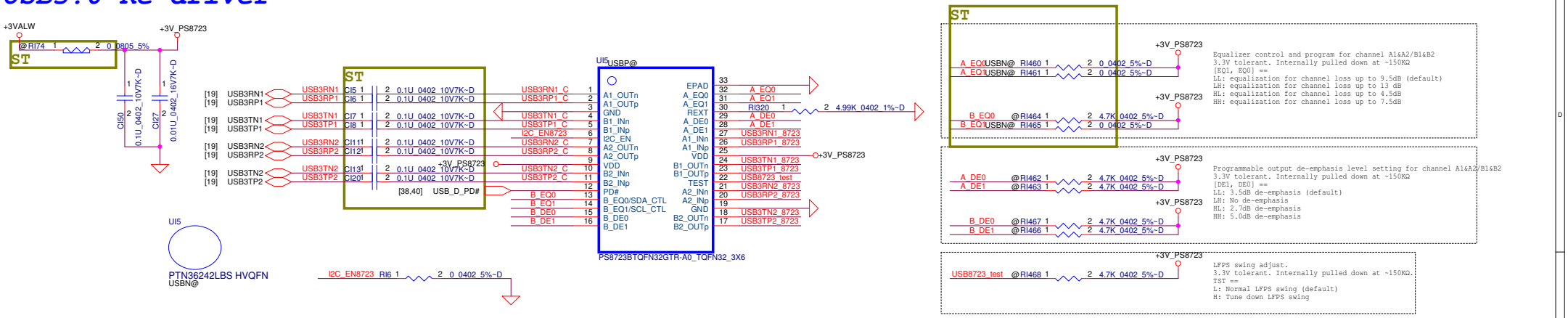
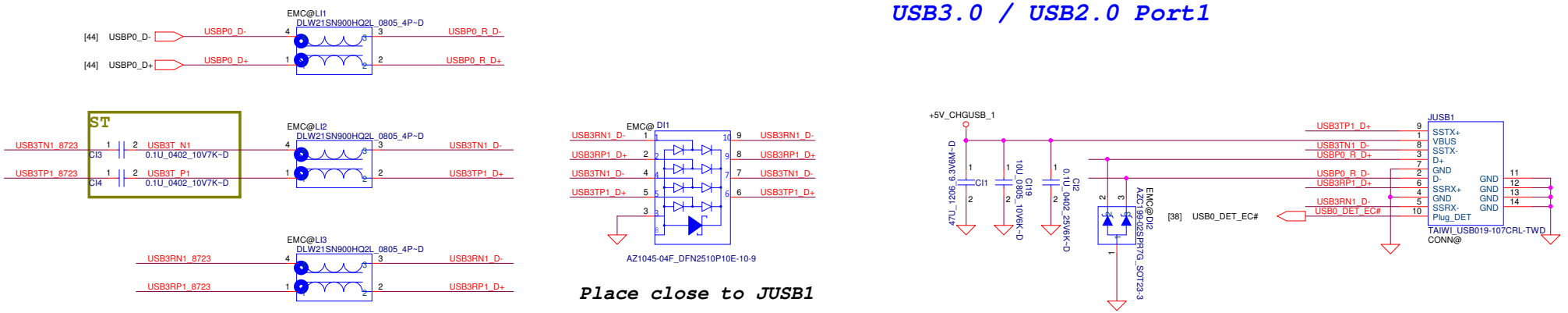
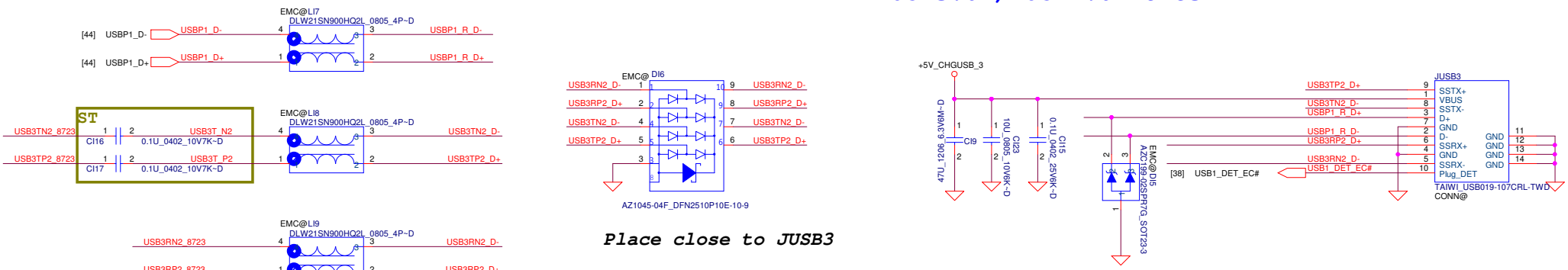
USB3.0 Re-driver



USB3.0 / USB2.0 Port1



USB3.0 / USB2.0 Port3



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Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.			
Title: USB conn.			
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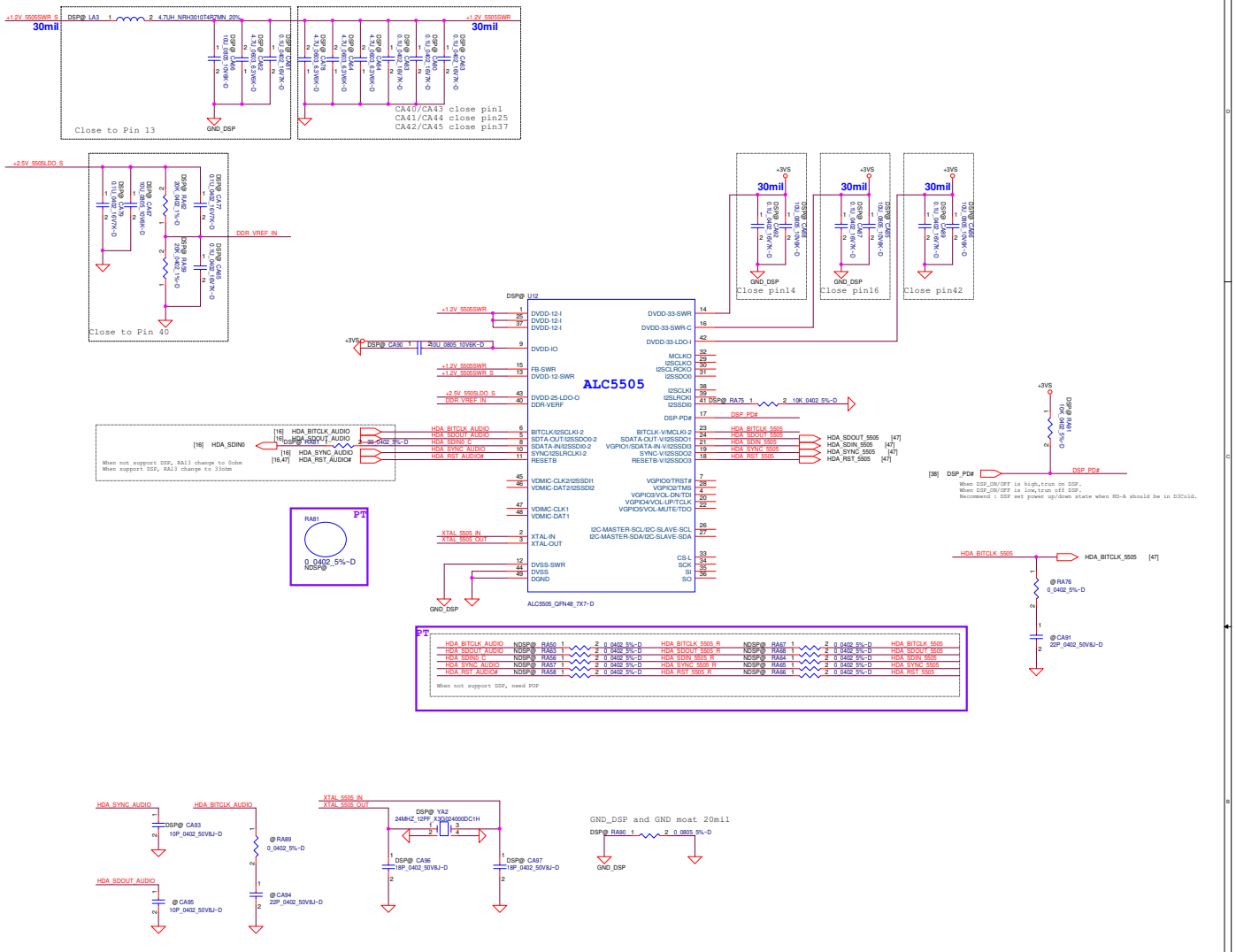
HD Audio DSP



Green Clock

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/08/25	Deciphered Date	2012/07/25
			Title: RTC Counter/Green Clock

Size: Custom	Document Number		Rev
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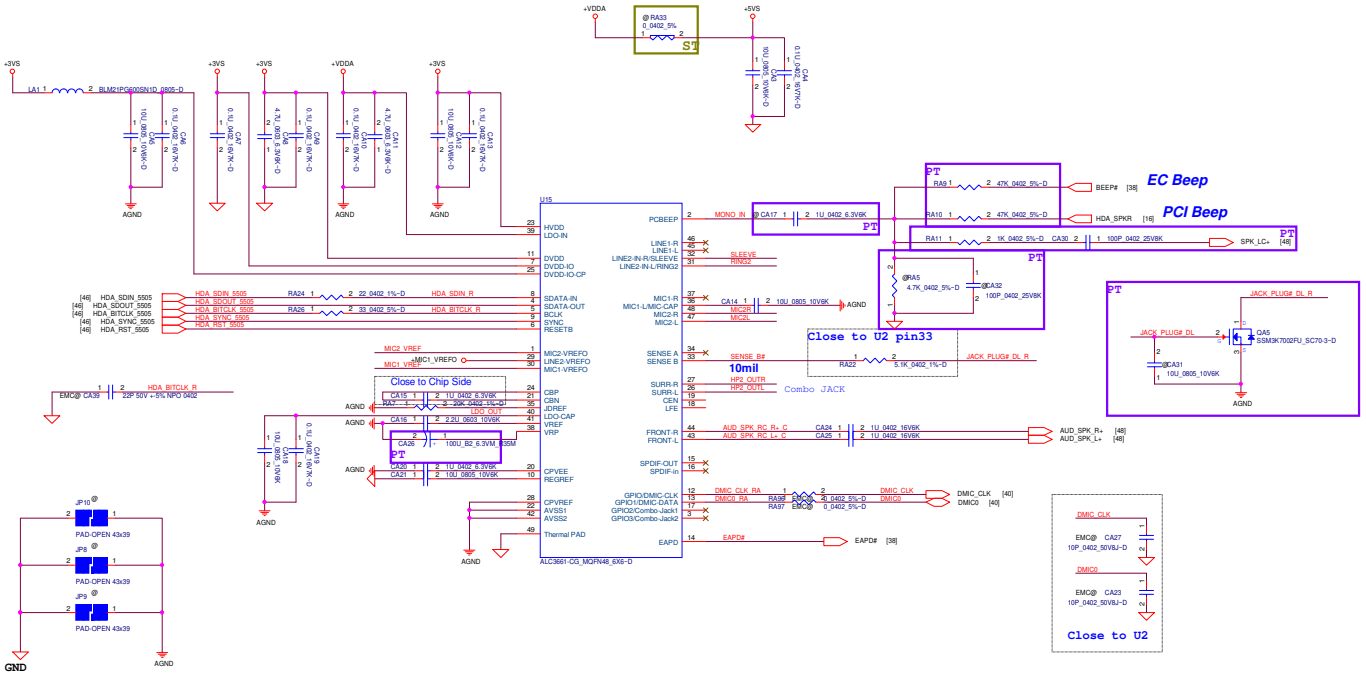
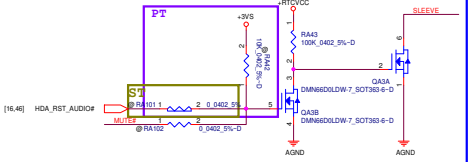
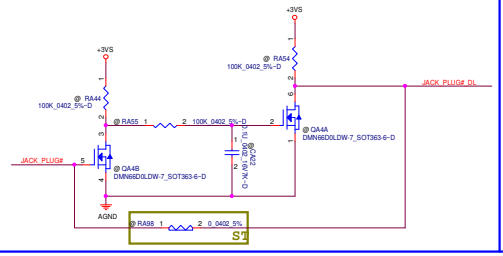
HDA_Audio Codec



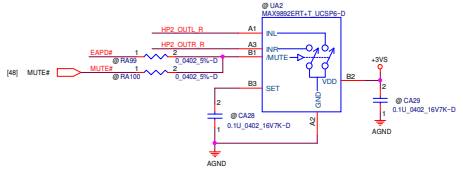
Prevent S3/S4/S5 Noise



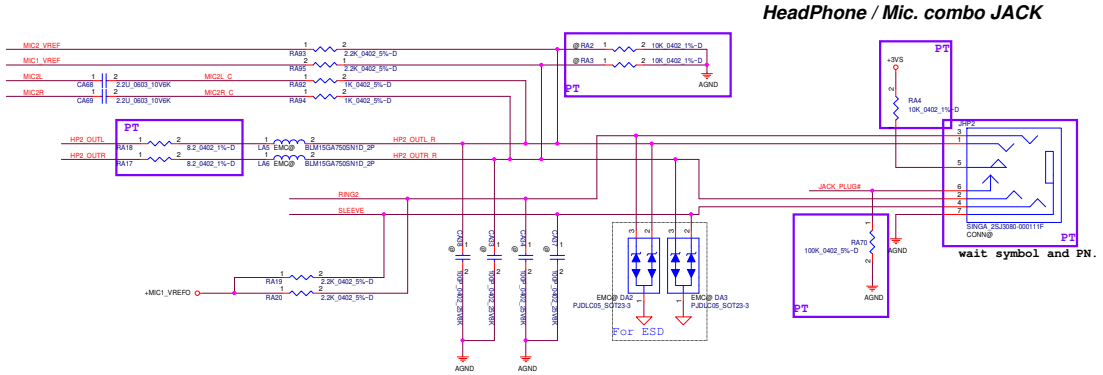
Reserved Delay Circuit



For De-pop noise



HeadPhone / Mic. combo JACK



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/08/25	Deciphered Date 2012/07/25	Title: HD Audio ALC275/Audio Jack

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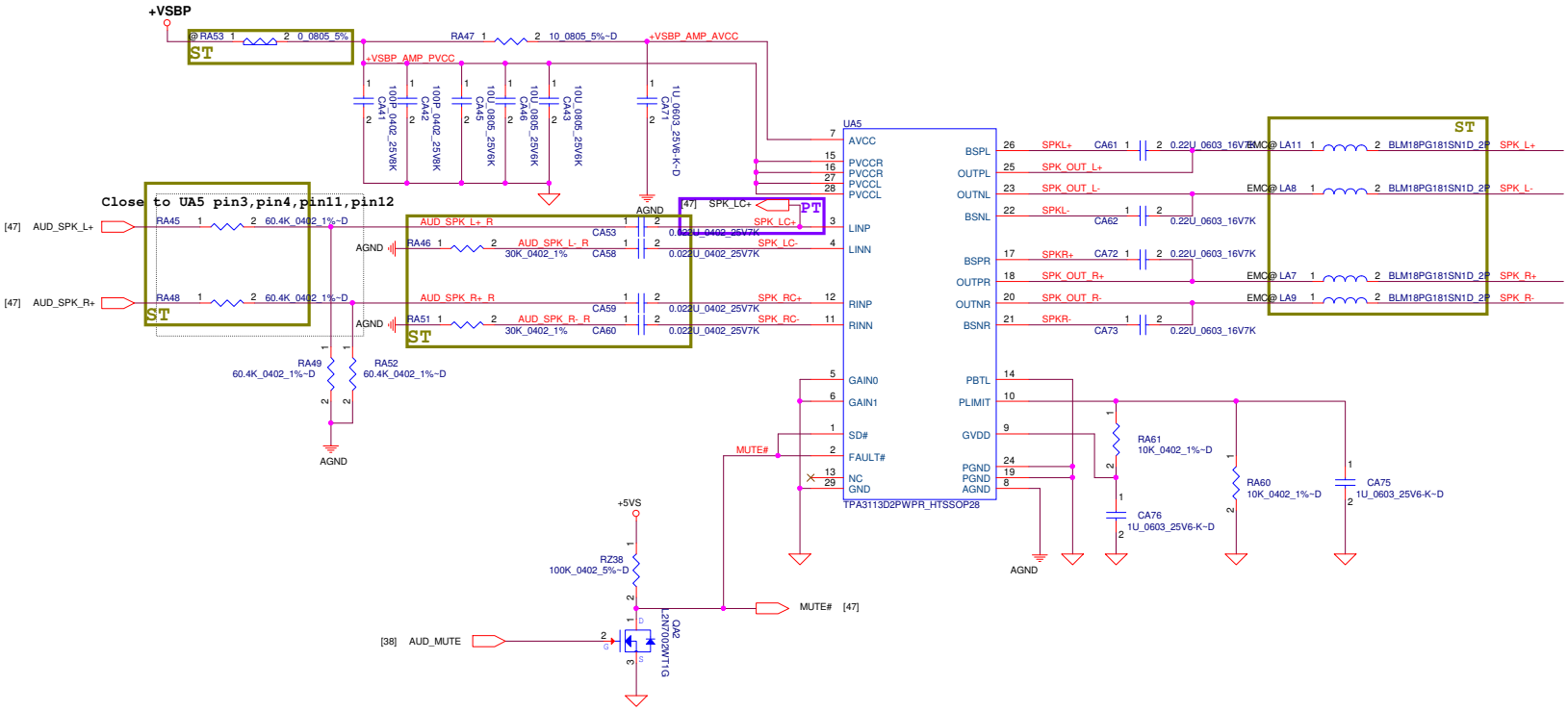
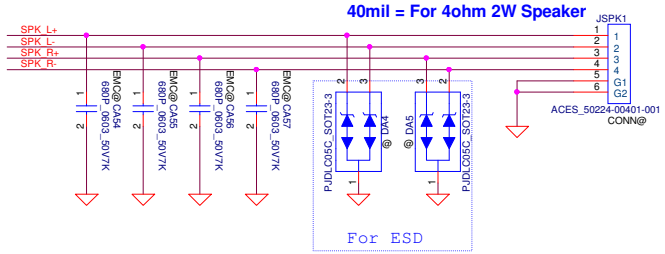
Audio AMP



Int. Speaker Conn.



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Issued Date	2011/08/25	Deciphered Date	2012/07/21

Compal Electronics, Inc.

Title: Speaker/Audio Jack

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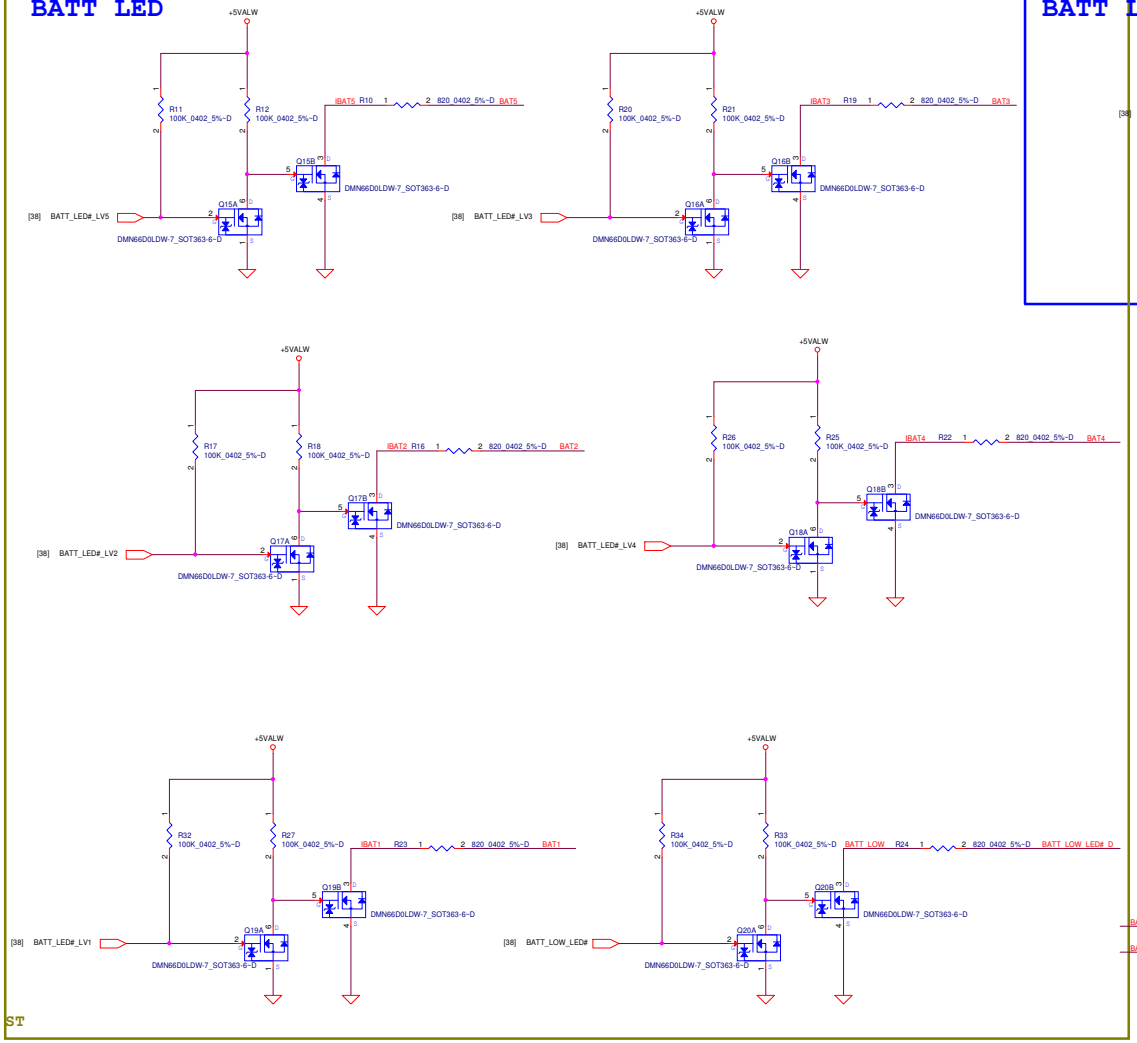
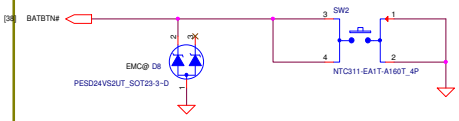
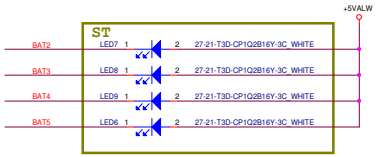
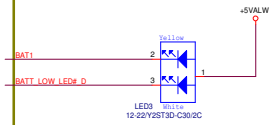
BATT LED

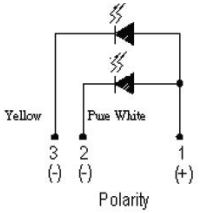


BATT LED Power Button

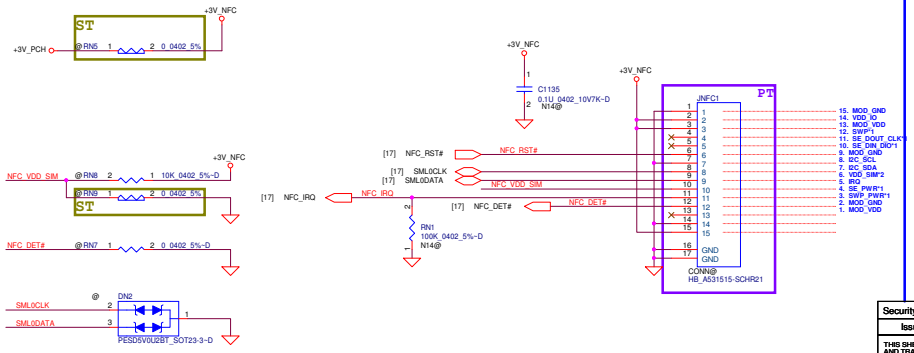








NFC Connector



RTC counter

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: Speaker/Audio Jack

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Module	REV	Change list	From	To
	X00	Remove Audio codec to DB --- page 47	X	X00
	X00	Add GC6 function for GPU N14P --- page 24/28/33	X	X00
	X00	Modify USB port detect pin to independent --- page 38 and page 45	X	X00
	X00	Follow GPIO table modify pin assign --- page 38	X	X00
	X00	Change to PWM FAN --- page 39	X	X00
	X00	Change mDP output from GPU --- page 25	X	X00
	X00	CCD connector change to 11 pin, add CCD_INT signal. --- page 35	X	X00
	X00	Change R45 PU to +3VALW for leakage current --- page 38	X	X00
	X00	Rmovie Audio DSP chip and add KC3801 --- page 46 and page 38	X	X00
	X00	Add RTC counter and add SSC chip for Audio bit clock --- page 46 and page 40	X	X00
	X00	Just support N14P-GS, so remove GPU board ID. --- page 20	X	X00
	X00	Co-layout Sata Re-driver PS8520B/C --- page 43	X	X00
	X00	EMC request add CM22 to close JTB1 pin17 --- page 40	X	X00
	X00	Buyer request Change YH2/YL1 to SJ10000DE00 --- page 17/41	X	X00
	X00	Buyer request Change YH1/Y4 to SJ10000DE00 --- page 16/46	X	X00
	X00	Change RH85 connector to +1.5VS --- page 17	X	X00
	X00	Change RPH1/RPH2/RPH3/RPH4/RPH5 tp single resister --- page 18/19	X	X00
	X00	Modify eDP connector pin define, remove +3VS --- page 35	X	X00
	X00	Modify support quad ROM, add RH10/RH41 --- page 17	X	X00
	X00	Change HDMI level shift to active --- page 36	X	X00
	X00	EMC request add CA36 --- page 40	X	X00
	X00	NFC SMBus change to PCH SMBus0 --- page 17	X	X00
	X00	CCD SMBus reserve connector to PCH, and CCD INT reserve connector to EC --- page 35	X	X00
	X00	Modify USB charger schematic, change RI17/RI31/RI32connect to +3VALW, and remove RI18/RI28 --- page 44	X	X00
	X00	Update VRAM PN --- page 1	X	X00
	X00	Remove NFC function --- page 49	X	X00
	X00	SWAP DA4 pin2 and pin3 --- page 48	X	X00
	X00	Use array resister to reduce component Change RH45/RH46/RH47/RH49 to array resister RPH11 --- page 17 Change RH50/RH51 to array resister RPH14 --- page 17 Change RH66/RH83/RH88/RH90 to array resister RPH24 --- page 17 Change RH69/RH74/RH77/RH81 to array resister RPH25 --- page 17 Change RH71/RH72 to array resister RPH15 --- page 17 Change RH137/RH139/RH140/RH141 to array resister RPH1 --- page 18 Change RH147/RH149/RH150/RH153 to array resister RPH2 --- page 18 Change RH116/RH117/RH118/RH124 to array resister RPH4 --- page 18 Change RH134/RH135/RH142/RH168/RH178/RH186/RH192/RH187 to array resister RPH26 --- page 19 Change RH189/RH183/RH179/RH181 to array resister RPH7 --- page 20 Change RH160/RH185/RH184/RH172 to array resister RPH8 --- page 20 Change RH190/RH178/RH177/RH182 to array resister RPH9 --- page 20 Change RV291/RV293/RV295/RV400 to array resister RPH12 --- page 24 Change RV292/RV294/RV296/RV297 to array resister RPH13 --- page 24 Change RV299/RV300 to array resister RPH16 --- page 24 Change RV325/RV326 to array resister RPH17 --- page 25 Change RV331/RV333/RV334/RV335 to array resiter RPH10 --- page 26 Change RH94/RH96 to array resister RPH27 --- page 35 Change RV445/RV447 to array resister RPH18 --- page 36 Change RE72/RE73 to array resister RPH20 --- page 38 Change RE17/RE18/RE36/RE37 to array resiter RPH19 --- page 38 Change RE14/RE15 to array resister RPH21 --- page 38 Change RH82/RH93 to array resister RPH22 --- page 42 Change R136/R137 to array resister RPH23 --- page 46	X	X00
	X00	Use dual MOSFET to reduce single MOSFET Change QZ15/QZ20 to dual MOS QZ23 --- page 34 Change QE4/QE6 to dual MOS QZ24 --- page 39	X	X00
	X00	Use Anpec APL3512 to reduce Component Remove RV401/RV402/QV26/QV28/RV404/CV745/QV27, Add CV26/CV28/UV12 --- page 35	X	X00
	X00	Use TI TPS22966 to reduce Component Remove RZ20/RZ14/QZ6/QZ10/CZ15/RZ17/QZ9/CZ38/QZ8/QZ7/RZ37, Add UZ4/RZ132/RZ133/CZ28/CZ29/QZ9/RZ17 --- page 34	X	X00
	X00	Add DV9 for display have leakage issue --- page 37	X	X00
	X00	Use Green Clock to reduce component Unstuff RH1/YH1/CH3/CH4, add RH96 --- page 16 Unstuff RH89/YH2/CH27/CH28, add RH102 --- page 17 Unstuff YV1/CV575/CV576, add RV13 --- page 24 Unstuff YL1/CL22/CL25, Stuff RL10 --- page 41 Add C28/C27/C26/C84/R67/R68/U3/C34/R91/Y5/C41/C32 --- page 46	X	X00
	X01	Remove DV7 for EMC component should close device connector side --- page 40	X00	X01
	X01	Remove +1.5V_PWROK and +1.35V_PWROK connect to HWPG for power good issue --- page 38	X00	X01
	X01	Change S3_DRAMPWRGD circuit, that change 1.5VPWRGD to +V1.05S_VCCP_PWRGOOD and un-stuff RU50 ---- page 8	X00	X01
	X01	Remove RZ13 for power value issue --- page 34	X00	X01
	X01	Remove RV471 for Touch screen power issue --- page 35	X00	X01
	X01	Un-stuff RE56 and stuff RE60 for EC power on issue --- page 38	X00	X01
	X01	Un-stuff RH32 for +3V backdrive --- page 16	X00	X01
	X01	Un-stuff RH158 for +3V backdrive --- page 20	X00	X01
	X01	Remove PCH control TPM PD pin for +3V backdrive --- page 40	X00	X01
	X01	Crete EC 3810 GPIO11 SUS_ON for DDR power enable --- page 38	X00	X01
	X01	Stuff RV450/RV451 10K ohm for HDMI EA measure issue --- page 36	X00	X01
	X01	Change RZ600 to 11K ohm for 1.5V power value issue --- page 34	X00	X01
	X01	For GPU power sequence issue Stuff CZ7 to 0.01u change CZ6 to 0.047u and add CZ8 0.047u cap for 1.05VDGPU delay --- page 33 Stuff RZ10 10 ohm, RZ11/RZ15 1 ohm, RZ6 100 ohm. change DZ2 enable pin2 to DGPU_PWROK and remove RZ485 Change RZ5 to 100k ohm	X00	X01
	X01	RZ484 change PU to +3VS for GPU GC6 function issue --- page 33	X00	X01
	X01	Remove RV504 and add QV40 for GPU thermal function --- page 24	X00	X01
	X01	Audio vendor suggest for Iphone Add RA11/CA30/RA2/RA3 Change CA26 to 100U Change RA18/RA17 to 8.2 ohm	X00	X01
	X01	Change PCH_GPIO72 and WAKE# PU to +3VALW for DSx issue --- page 18	X00	X01
	X01	Update power circuit Add +1.35V enable signal SUS_ON and rename PM_SLP_S5# to PM_SLP_S4#. Add 33uF*1 OS-CON for acoustic issue.	X00	X01
	X01	Un-stuff QZ26/QZ27 for EC multi SPI function --- page 17	X00	X01
	X01	SML0CLK/ SML0DATA PU to 499 ohm and reserve RH65 for NFC suggest --- page 17	X00	X01
	X01	Change RPH11 8P4R to RH448/RH456 single type --- page 17	X00	X01
	X01	Change DP from GPU output to Internal output	X00	X01
	X01	Add DSP bypass circuit --- page 46	X00	X01
	X01	Modify I/O connector JTB1 pin define --- page 40	X00	X01
	X01	Add DI15 for Touch screen function --- page 35	X00	X01
	X01	Add LCD_TEST RE64 PU to +EDPVDD --- page38	X00	X01
	X01	Power SW LED resistor R66 change to 560 ohm --- page39	X00	X01
	X01	Add JP802/JP803/JP11/JP14/JP15 for power measure	X00	X01
	X01	Add JRTC to MB --- page 16	X00	X01
	X01	Change JP5 size --- page 21	X00	X01
	X01	Change FAN connector --- page 39	X00	X01
	X01	PCH_GPIO12 change to PU +3VALW --- page 20	X00	X01
	X01	change CH27,CH28=12pF,CV575,CV576=10pF	X00	X01
	X01	Change LA7/LA8/LA9/LA11 to 180 ohm bead --- page 48	X00	X01
	X01	Remove JRTC --- page 16	X00	X01
	X01	Add RV411 for mDP voltage issue --- page 36	X00	X01
	X01	Add RF shielding EMIST_SUL-15A3M_1P footprint 12pcs --- page 40	X00	X01
	X01	Change ODD_DA# to RPH2, un-stuff RH164, and RH416 for GPU enable issue --- page 18	X00	X01
	X01	BIOS setting request PCH_GPIO70 for UMA/DIS, PCH_GPIO1 for GPU N14/N15 --- page 20	X00	X01
	X01	Change SW1 connector --- page 39	X00	X01
	X01	Change NFC connector --- page 49	X00	X01
	X01	Stuff RU7/RU12/RU36 --- page 6	X00	X01
	X01	Change Touch screen sleep circuit, remove DI5, add DV17/DV20/RV5 --- page 35	X00	X01
	X01	Un-stuff RV466--- page 37	X00	X01
	X01	Change DSP bypass circuit --- page 46	X00	X01
	X01	Update power circuit	X00	X01
	X01	Remove GPU DP HDP circuit --- page 24/37	X00	X01
	X01	Remove GPU DP port power --- page 26	X00	X01
	X01	Remove GPU VRAM power for N14E-GL --- page 28	X00	X01
	X01	Change JHP2 connector --- page 47	X00	X01
	X01	Add CV639 for vendor request --- page 28	X00	X01
	X01	Change SD302100280 to SD309100280 for EOL	X00	X01
	X01	CA17 un-stuff for pop issue	X00	X01
	X01	Remove DV16, add DV18/DV19/RV415 for LCD power control --- page 35 Add RV416/RV419 for EC control LCD SMBUS --- page 35	X00	X01
	X01	Remove RV483 and add RH178 for ST test --- page 20	X00	X01
	X02	RZ5 change to 60.4K ohm for GPU sequence --- page 33	X01	X02
	X02	USB3.0 CAP CI5,CI6,CI7,CI8,CI11,CI12,CI13,CI20,CI3,CI4,CI16,CI17 change to 0.1uF for USB3.0 issue --- page 45	X01	X02
	X02	modify eDP chock LV16-LV20 for footprint issue --- page 35	X01	X02
	X02	LA7/LA8/LA9/LA11 change footprint size --- page 48	X01	X02
	X02	CA53/CA58/CA59/CA60 change to 22nf for pop issue --- page 48	X01	X02
	X02	Hynix "0". ROM_SI=PD 5K ohm, Samsung"1". ROM_SI=PD 10K ohm for VRAM SETTING --- page 25	X01	X02
	X02	RA45/48 change to 60Kohm,RA46/51 changr to 30Kohm for Audio issue --- page 48	X01	X02
	X02	change F1 to SP040002400 --- page 39	X01	X02
	X02	Stuff RV460 and change RV458 to 4.7K ohm for HDMI EA issue --- page 36	X01	X02
	X02	Change CV677 to X6S --- page 30	X01	X02
	X02	Change UZ14 for G5243 for +3V_PCH issue --- page 34	X01	X02
	X02	Add TI HDD redriver co-layout --- page 43	X01	X02
	X02	Change LED footprint and change LED control circuit --- page 49	X01	X02
	X02	Add PD resistor for SATA redriver EA issue --- page 43	X01	X02
	X02	Change RU118 to 10K for OTP issue --- page 8	X01	X02
	X02	Change Board ID --- page38	X01	X02
	X02	Change H10/H18 footprint --- page 40	X01	X02
	X02	Reserve PD resistor for SATA redriver --- page 43	X01	X02
	X02	Change RA33/RA98/RA101/RE60/RE321/RE322/RN5/RN9/RU37/RU43/RU53/RV8/RV480/RV481/RV482/RV503/RV510/RH416 RV411/RV415/RV337/R8/R53/R54/R56/R58/RA53/RH202/RH213/RI74 to 0ohm short pad	X01	X02
	X02	Change UV12 and UN3 to GMT G5243	X01	X02
	A00	UV12 change to APL3512ABI-TRG_SOT23-5 for bring up issue --- page 35 Remove CV3508 for panel EA issue --- page 35 Add CCD_INT# pin --- page 38	X02	A00
	A00	EMI shielding clip footprint change to SOLUTION_ICSRC6510-015SFR-B_1P(H7/H14/H17/H27/H19/H20/H21/H23/H25/H24/H26) --- page 40 change SM070002000 to SM070002Q00 --- page 35	X02	A00
	A00	EMI shielding clip footprint change to EMIST_SUL-12A2M_1P(H7/H14/H17/H27/H19/H20/H21/H23/H25/H24/H26) --- page 40 Remove N15P external ROM and strap --- page 25	X02	A00
	A00	Remove eDP co-layout component, and add EC_INV_PWM conntrol PWM from EC --- page 35	X02	A00

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Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title: Block Diagram

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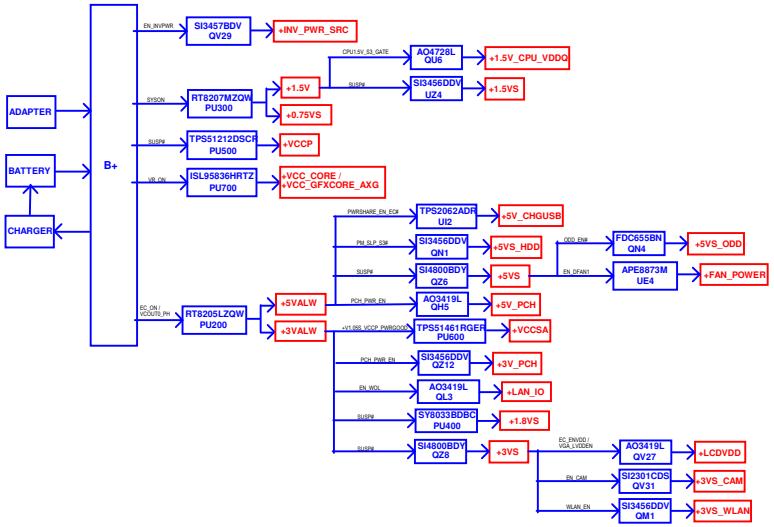
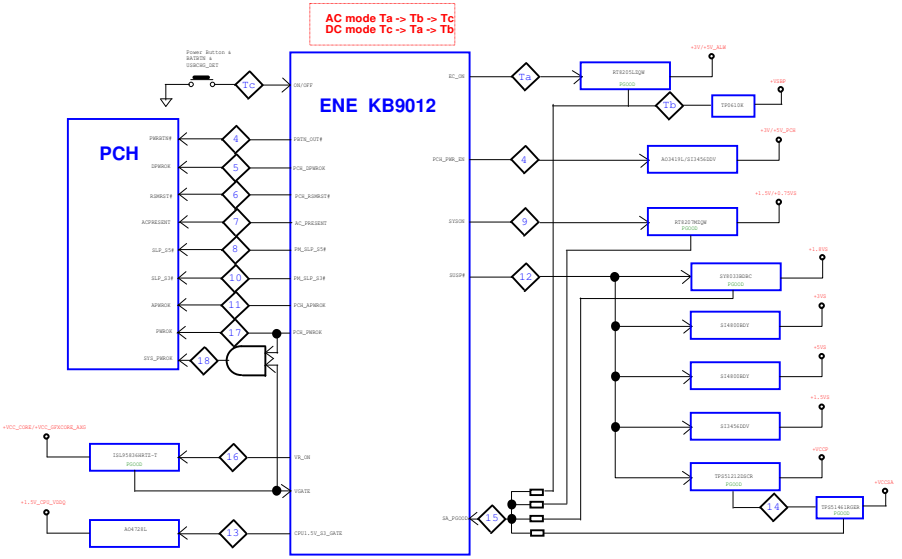
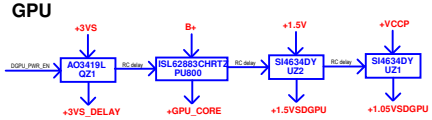
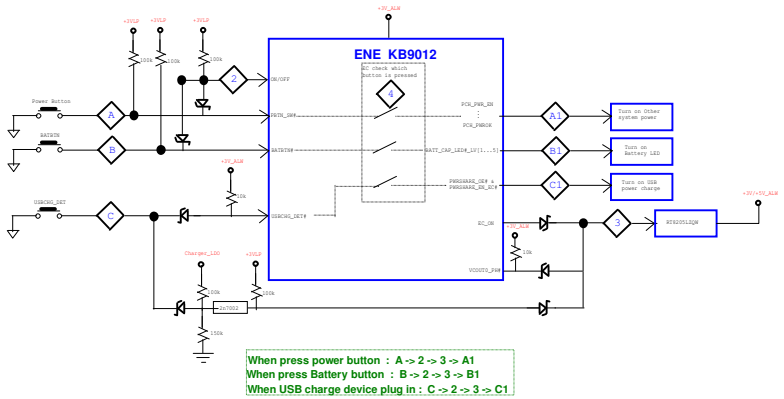




GPU





Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

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Title: Power Sequence

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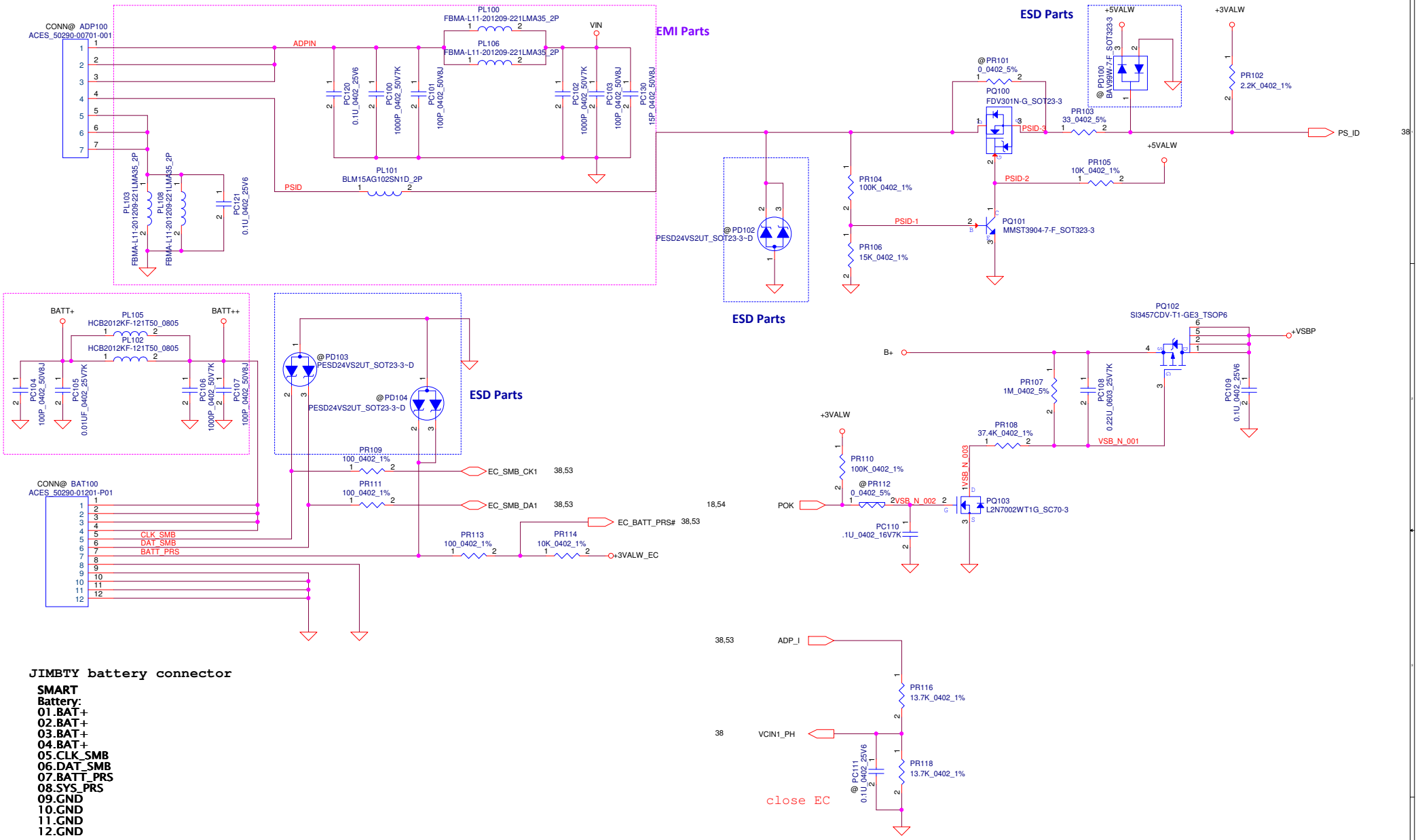

JIMBTY battery connector

SMART Battery:

01.BAT+
02.BAT+
03.BAT+
04.BAT+
05.CLK_SMB
06.DAT_SMB
07.BATT_PRS
08.SYS_PRS
09.GND
10.GND
11.GND
12.GND

Compal Electronics, Inc.

Title: PWR-DCIN / BATT CONN / OTP

Size | Document Number: LA-9941P | Rev: 0.1

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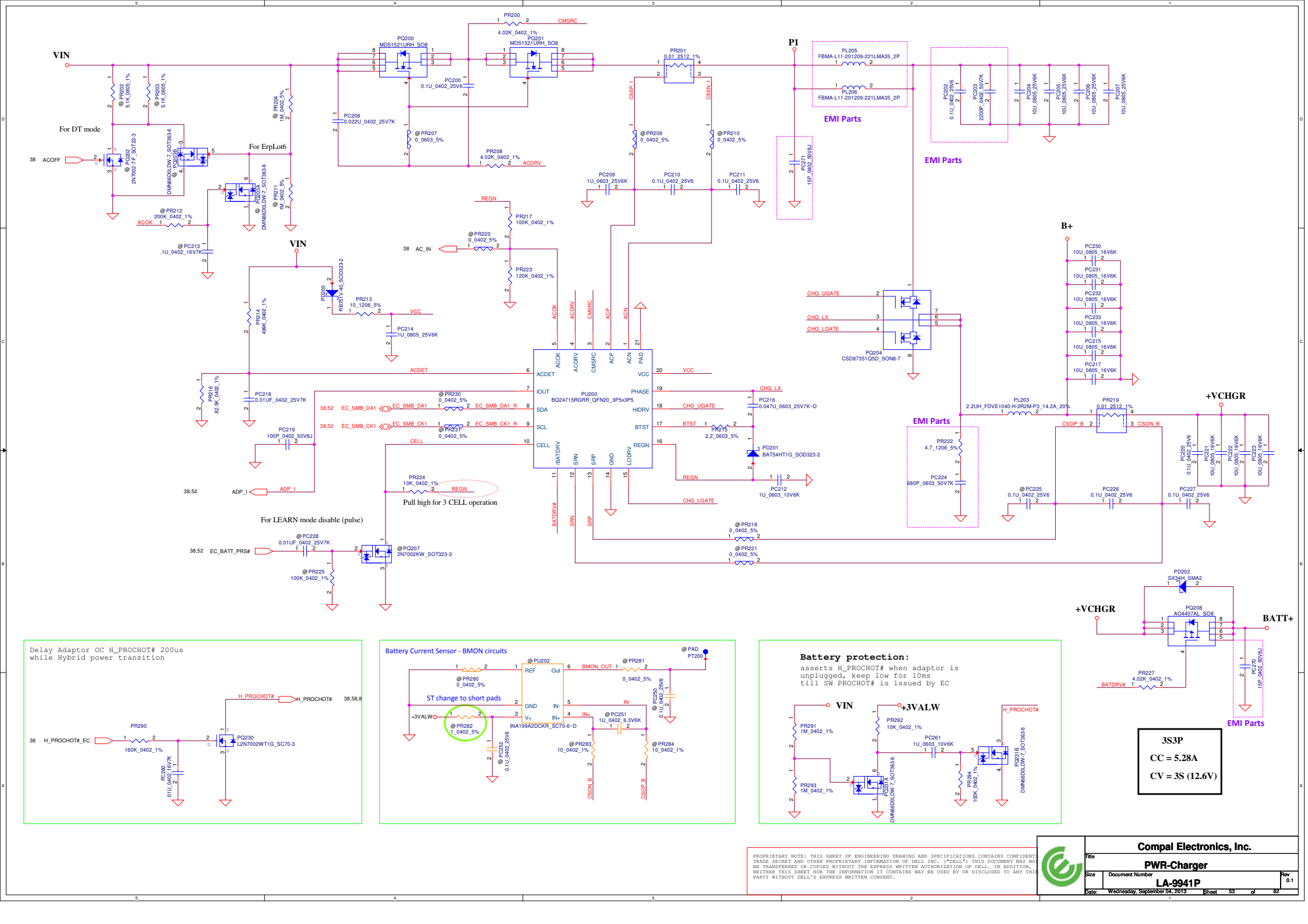

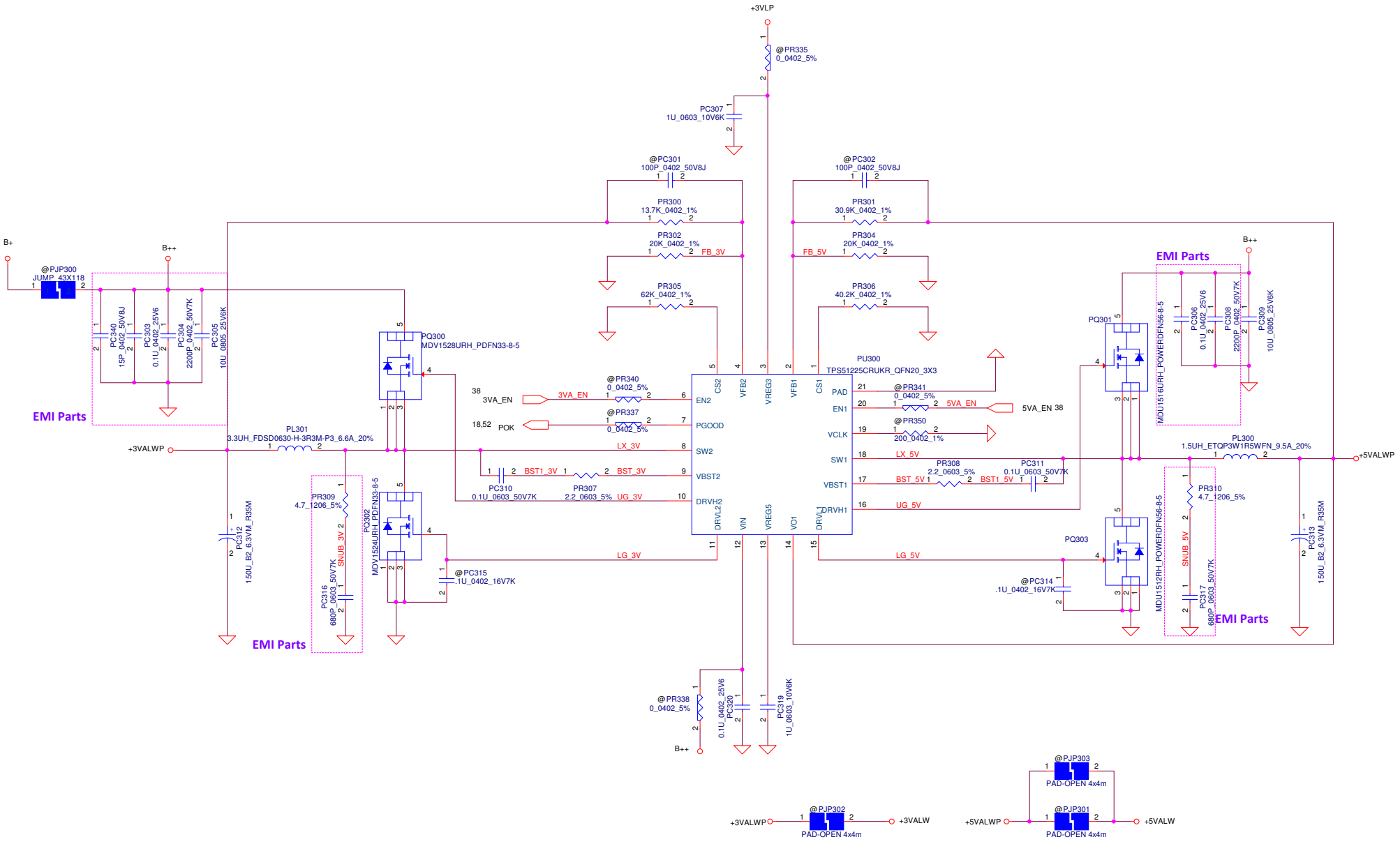

3.3VALWP
TDC 4.6A
Peak Current 6.5A
OCP current 7.8A

5VALWP
TDC 7.9A
Peak Current 11.3A
OCP current 13.4A

Compal Electronics, Inc.	
Title	PWR-3VALWP/5VALWP
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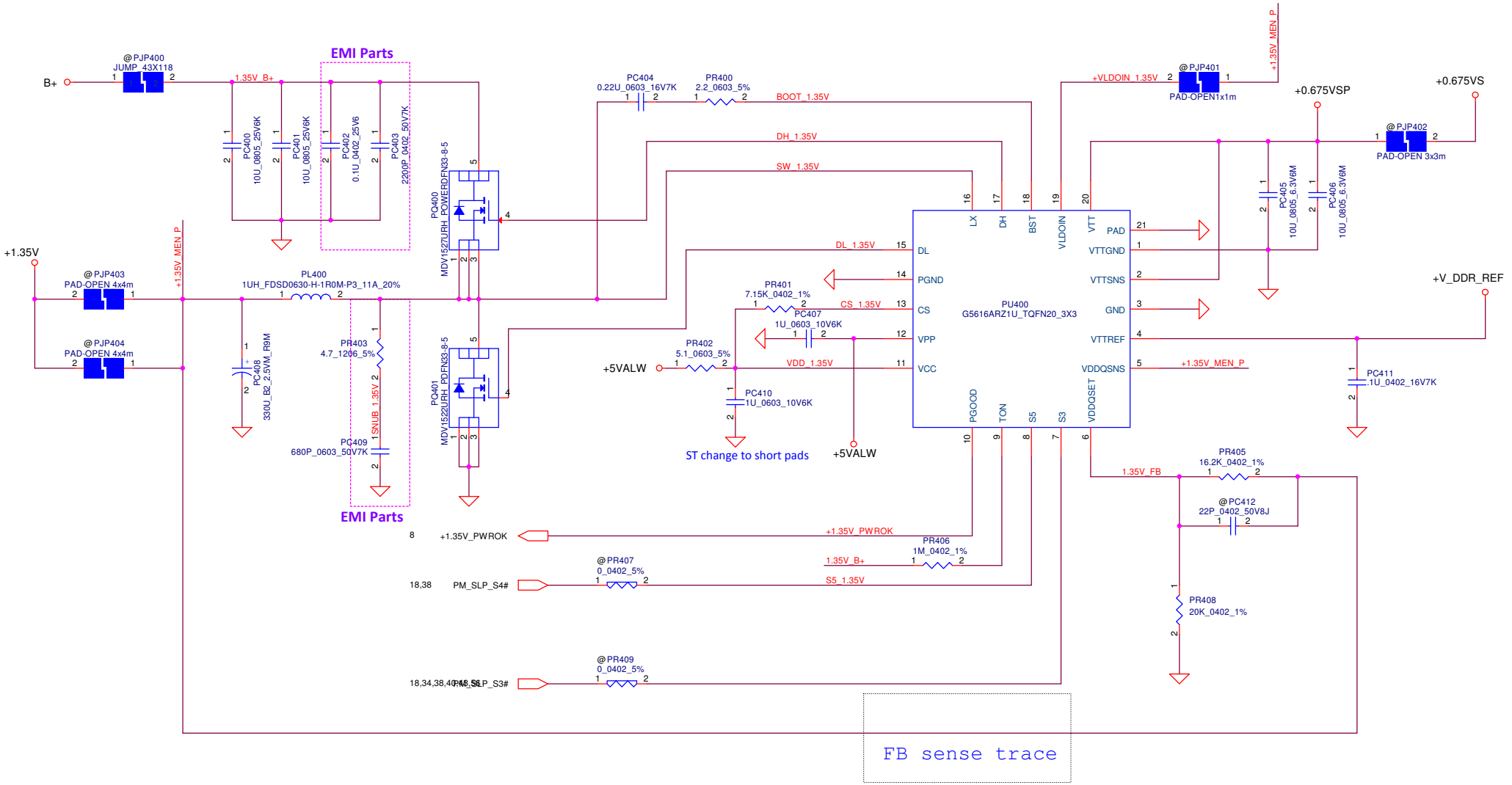
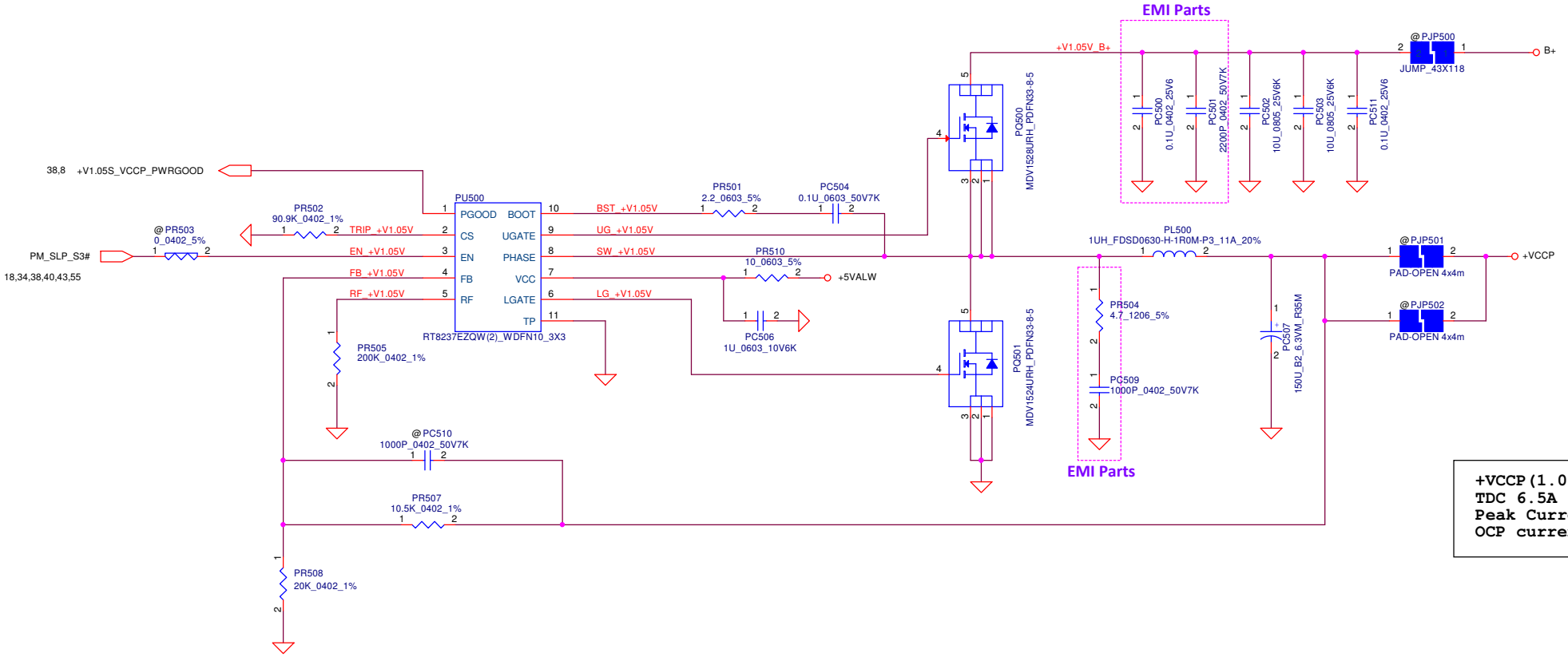


Compal Electronics, Inc.	
Title	+1.35V_MEN/+0.675V_DDR_VTT
Size	Document Number: LA-9941P
Rev	0.1
Date:	Thursday, September 05, 2013
Sheet	55 of 62



+VCCP(1.05V)
TDC 6.5A
Peak Current 9.2A
OCP current 11.1A

Compal Electronics, Inc.

Title: PWR-V1.05S_VCCPP

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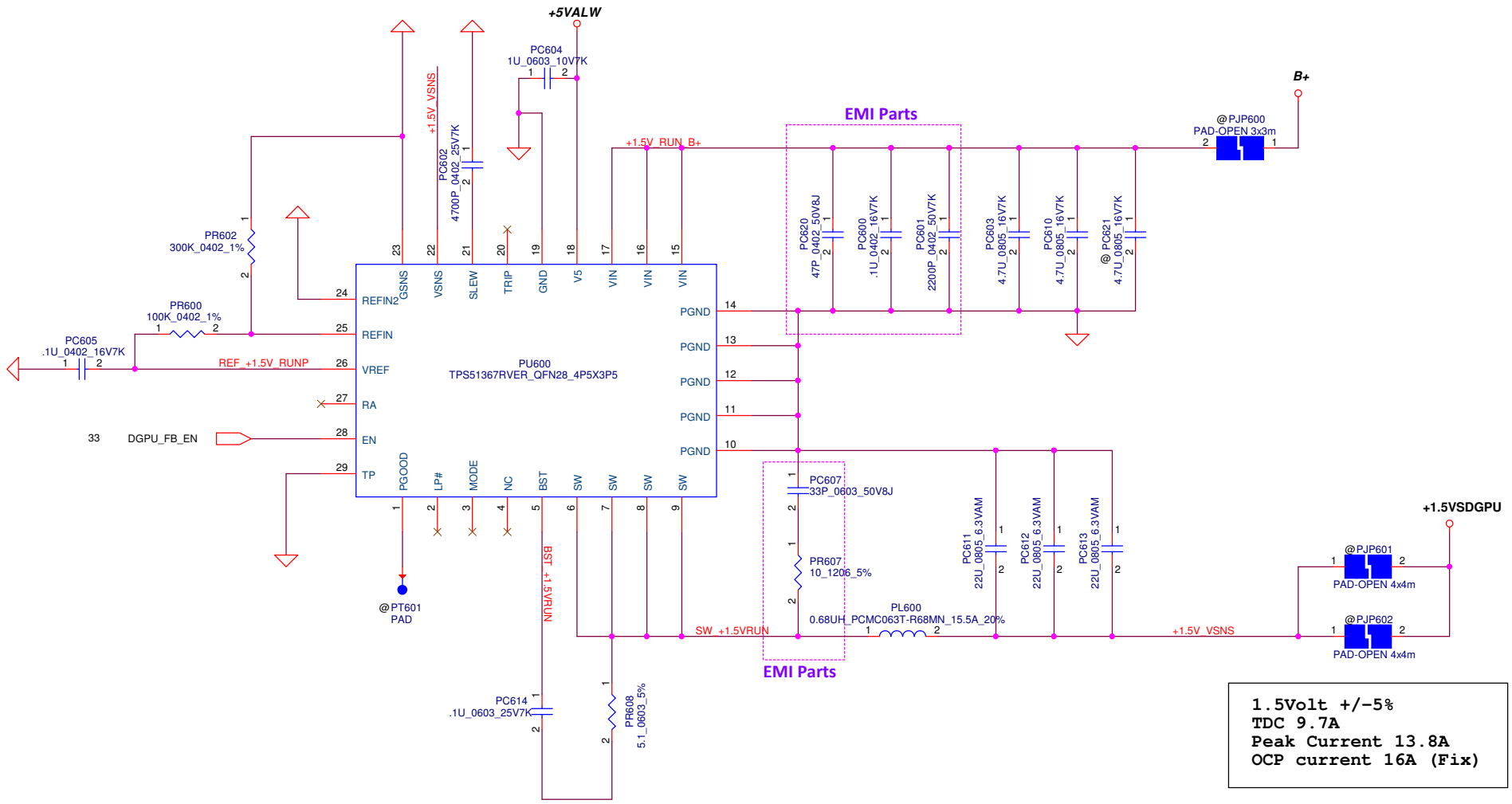

1.5Volt +/-5%
TDC 9.7A
Peak Current 13.8A
OCP current 16A (Fix)

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Compal Electronics, Inc.		
Title: PWR_+1.5VRUN		
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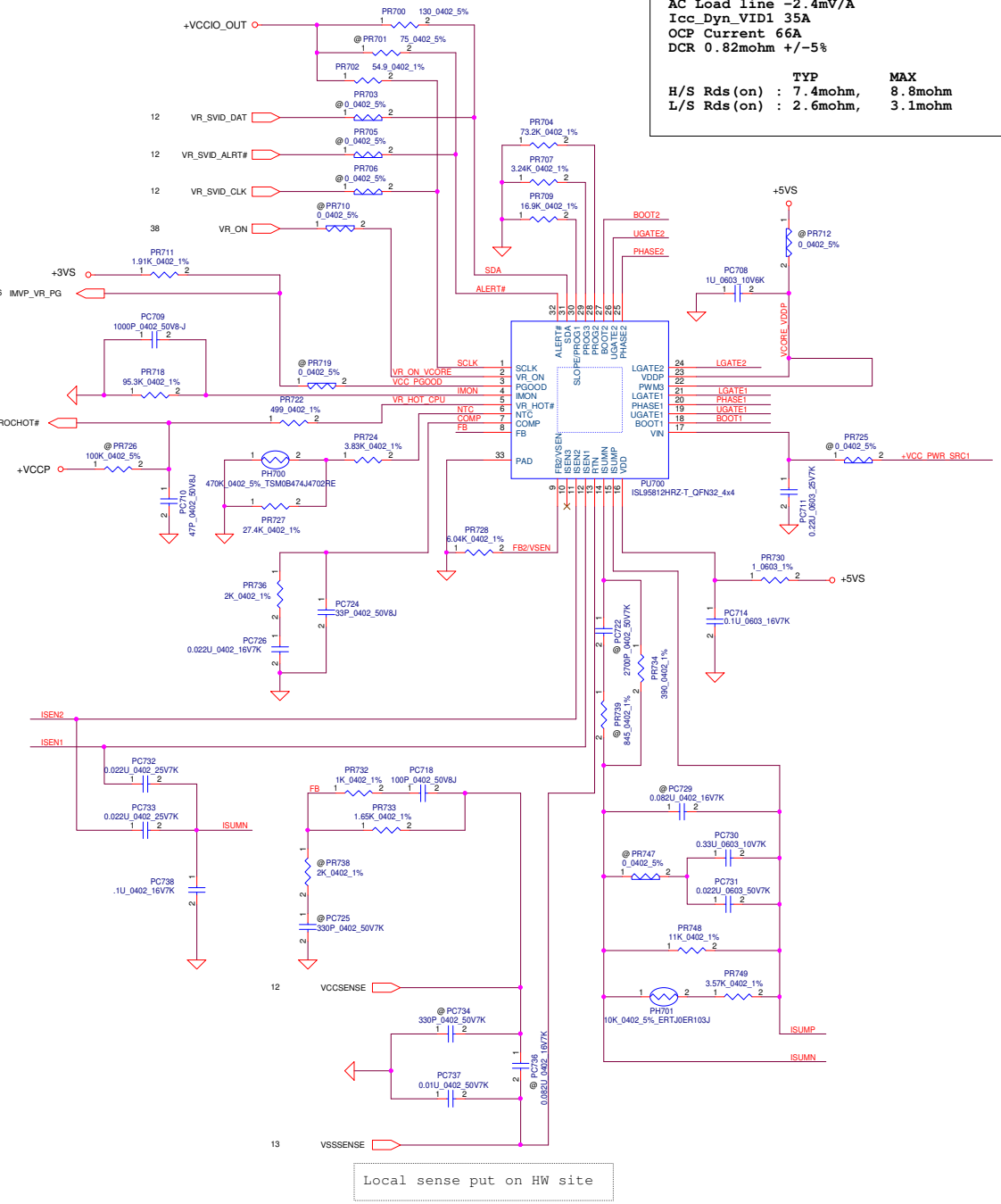
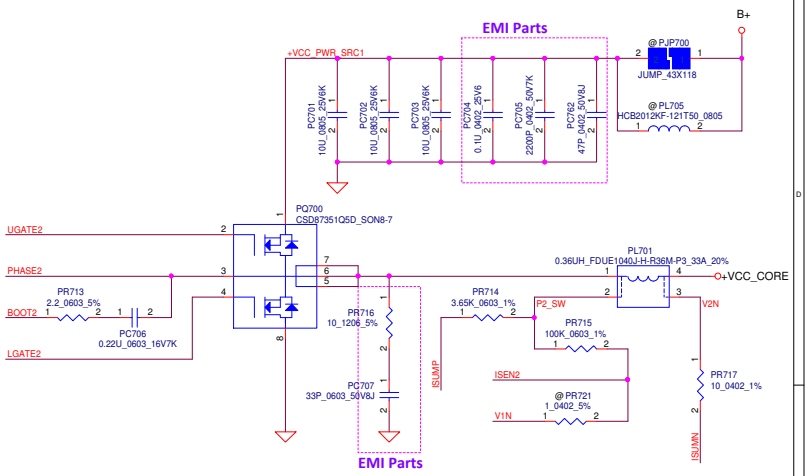
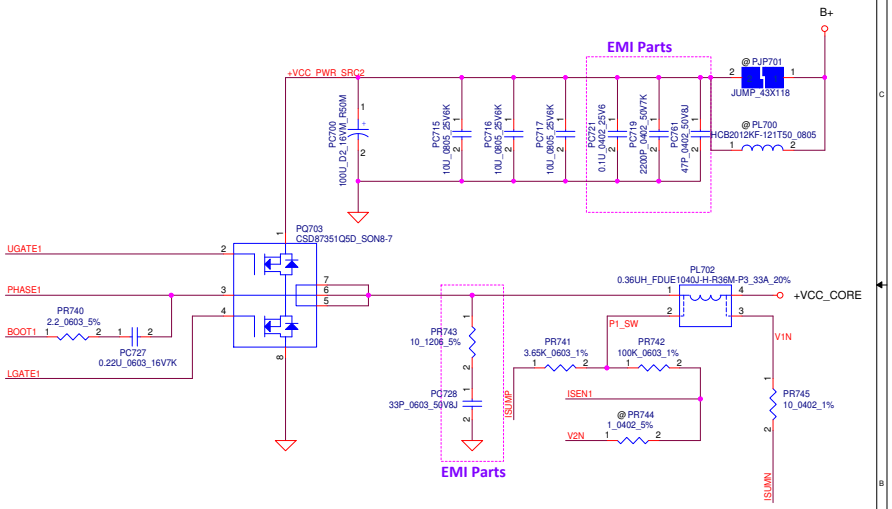
VCC_core (Base on PDDG rev 1.0) (1.8V)
TDC 21A
TDC PL2 (40Sec):26A
Peak Current 55A
DC Load line -1.5mV/A
AC Load line -2.4mV/A
Icc_Dyn_VID1 35A
OCP Current 66A
DCR 0.82mohm +/-5%

	TYP	MAX
H/S Rds(on) :	7.4mohm,	8.8mohm
L/S Rds(on) :	2.6mohm,	3.1mohm



Local sense put on HW site





Compal Electronics, Inc.

Title: +VCC_CORE

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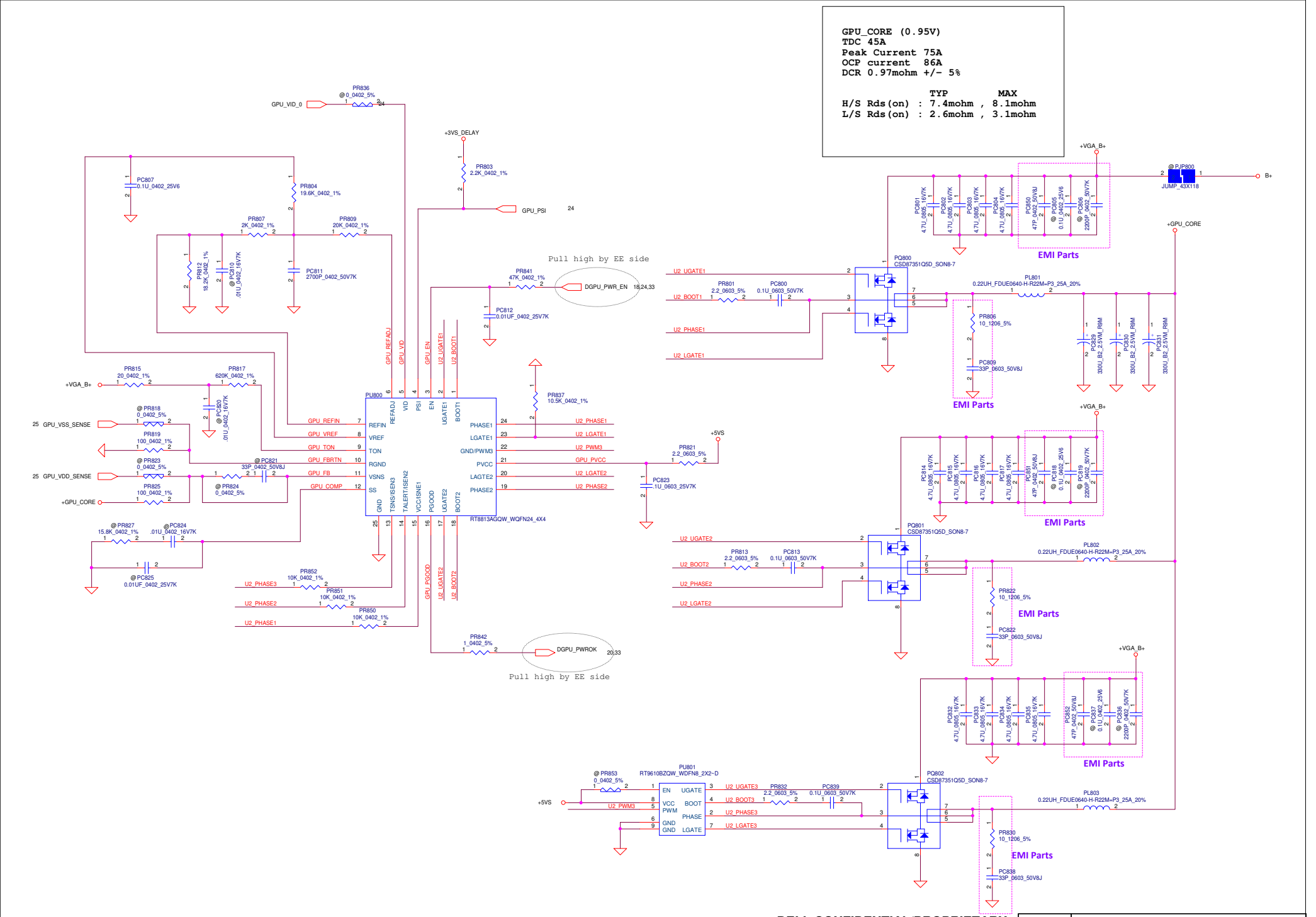
GPU_CORE (0.95V)
TDC 45A
Peak Current 75A
OCP current 86A
DCR 0.97mohm +/- 5%
TYP MAX
H/S Rds(on) : 7.4mohm , 8.1mohm
L/S Rds(on) : 2.6mohm , 3.1mohm
PU800
RT8813AGQW_WQFN24_4X4
PU801
RT9610BZQW_WDFN8_2X2-D
PQ800
PQ801
PQ802
CSD87351Q5D_SON8-7
PL801
PL802
PL803
0.22UH_FDUE0640-H-R22M=P3_25A_20%
EMI Parts
Pull high by EE side
Pull high by EE side
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Compal Electronics, Inc.
VGA_CORE
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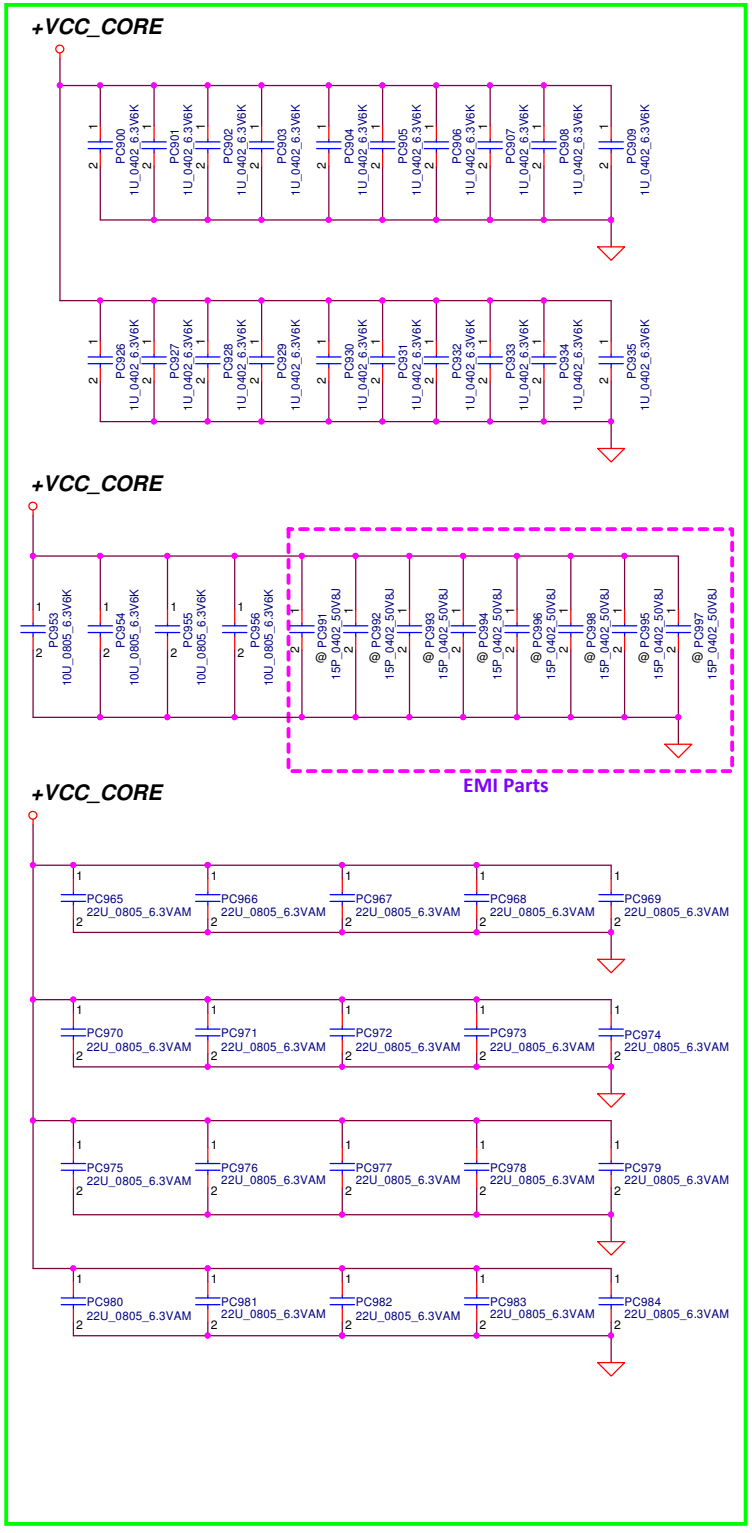
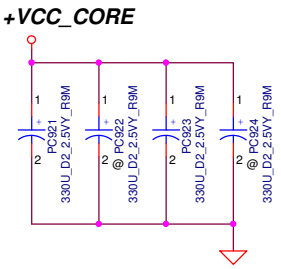
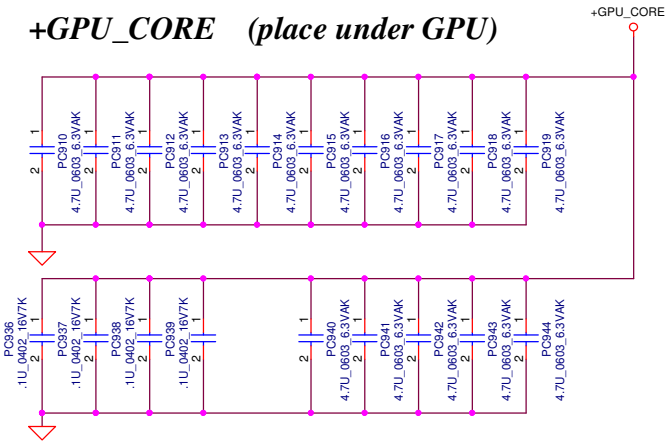
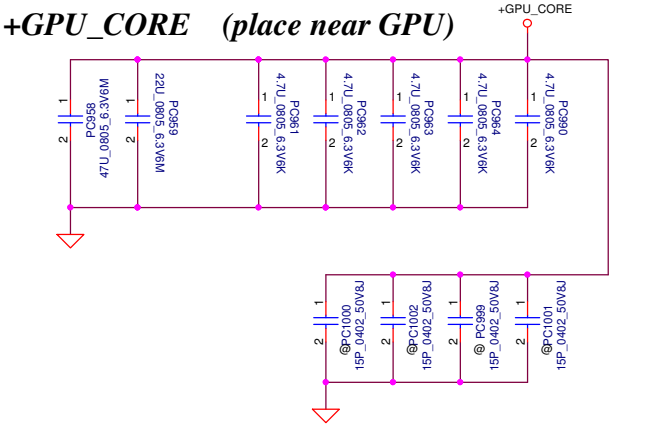




Based on PDDG rev 1.1 Table 5-2.

Design guilde:
+VCC_CORE
1. 470uF*4 (SGA0000420L)
2. 22uF*20 (SE000008L80)
3. 10uF*4 (SE160106M8L)
4. 1uF*20 (SE000000K8L)





Under:
1. 4.7uF*10 (SE000008L80)
2. 0.1uF*4 (SE160106M8L)
Near:
1. 4.7uF*5 (SE093475K80)
2. 22uF*1 (SE000001120)
3. 47uF*1 (SE00000PL0L)
4. 33uF*1 (SGA20331E10)

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Compal Electronics, Inc.		
Title: PROCESSOR DECOUPLING		
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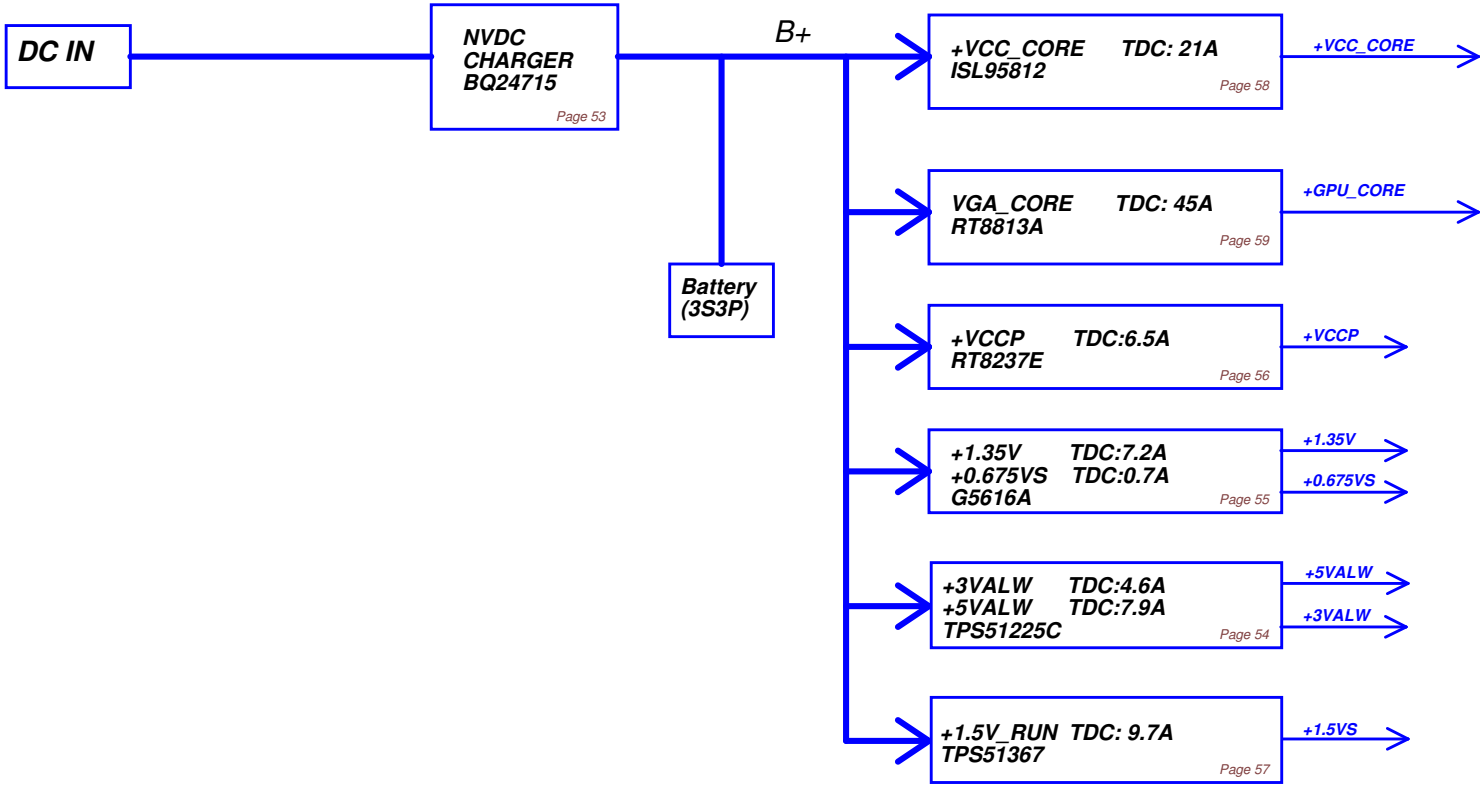

Compal Electronics, Inc.

Title: POWER BLOCK DIAGRAM

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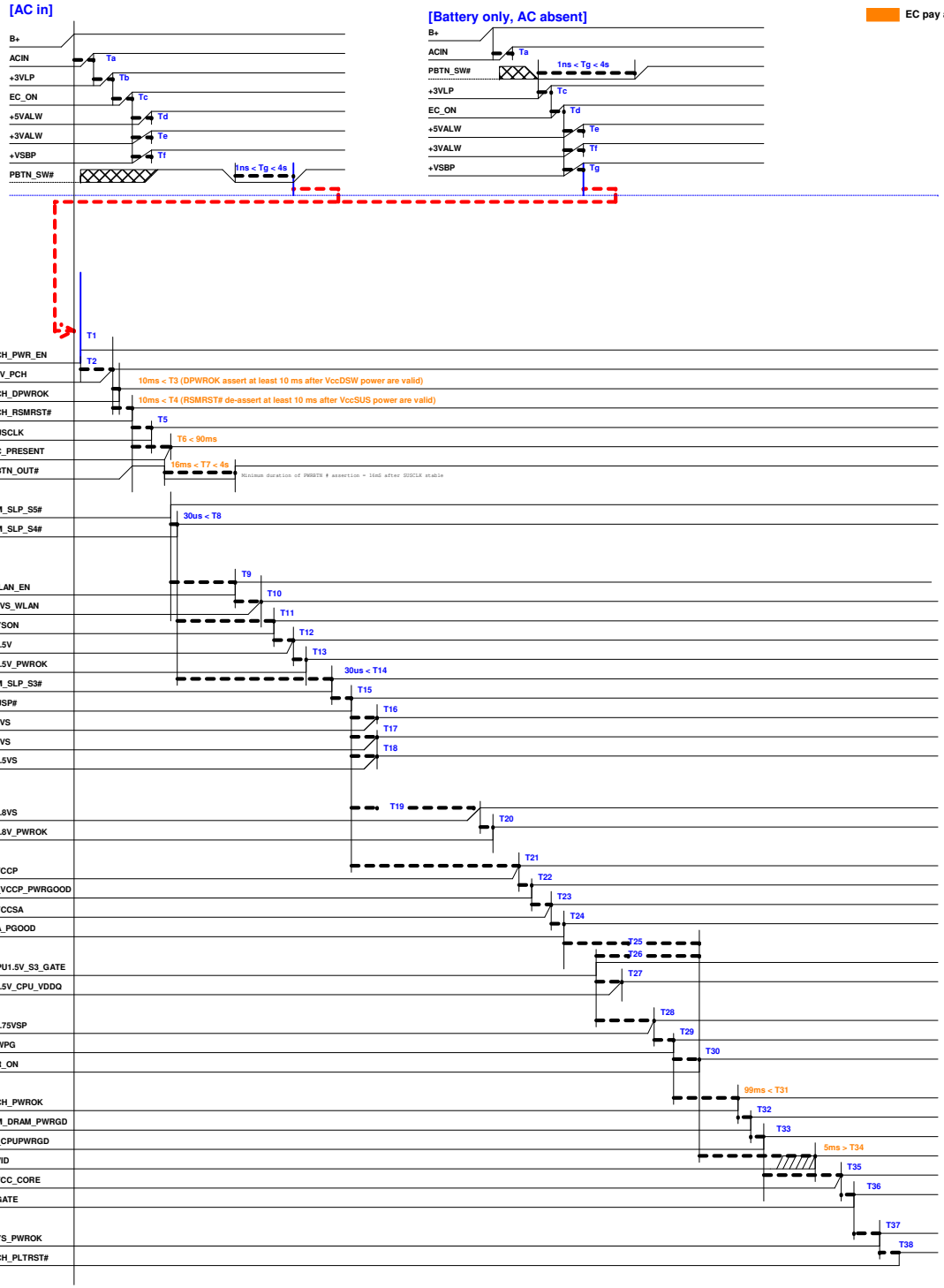
Discrete Power On Sequence

EC pay attention timing



[AC in]

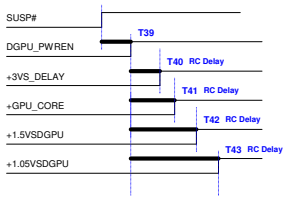
ITEM	Measure Point			Time
Ta	B+	To	ACIN	
Tb	ACIN	To	+3VLP	
Tc	+3VLP	To	EC_ON	
Td	EC_ON	To	+5VALW	
Te	EC_ON	To	+3VALW	
Tf	EC_ON	To	+VSBP	
Tg	PBTN_SW#		Low pluse width	N/A

[Battery only, AC absent]

ITEM	Measure Point			Time
Ta	B+	To	ACIN	
Tb	PBTN_SW#		Low pluse width	N/A
Tc	PBTN_SW#	To	+3VLP	
Td	+3VLP	To	EC_ON	
Te	EC_ON	To	+5VALW	
Tf	EC_ON	To	+3VALW	
Tg	EC_ON	To	+VSBP	

ITEM	Measure Point			Time
T1	PBTN_SW#	To	PCH_PWR_EN	
T2	PCH_PWR_EN	To	+3V_PCH	
T3	+3V_PCH	To	PCH_DPWROK	
T4	+3V_PCH	To	PCH_RSMRST#	
T5	PCH_RSMRST#	To	SUSCLK	
T6	PCH_RSMRST#	To	AC_PRESENT	
T7	PBTN_OUT#	To	Low pluse width	
T8	PM_SLP_S5#	To	PM_SLP_S4#	
T9	PM_SLP_S5#	To	WLAN_EN	
T10	WLAN_EN	To	+3VS_WLAN	
T11	PM_SLP_S4#	To	SYSON	
T12	SYSON	To	+1.5V	
T13	+1.5V	To	+1.5V_PWROK	
T14	PM_SLP_S4#	To	PM_SLP_S3#	
T15	PM_SLP_S3#	To	SUSP#	
T16	SUSP#	To	+5VS	
T17	SUSP#	To	+3VS	
T18	SUSP#	To	+1.5VS	
T19	SUSP#	To	+1.8VS	
T20	+1.8VS	To	+1.8V_PWROK	
T21	SUSP#	To	+VCCP	
T22	+VCCP	To	+V1.05S_VCCP_PWRGOOD	
T23	+V1.05S_VCCP_PWRGOOD	To	+VCCSA	
T24	+VCCSA	To	SA_PGOOD	
T25	SA_PGOOD	To	VR_ON	
T26	CPU1.5V_S3_GATE	To	VR_ON	
T27	CPU1.5V_S3_GATE	To	+1.5V_CPU_VDDQ	
T28	CPU1.5V_S3_GATE	To	+0.75VSP	
T29	+0.75VSP	To	HWPG	
T30	HWPG	To	VR_ON	
T31	HWPG	To	PCH_PWROK	
T32	PCH_PWROK	To	PM_DRAM_PWRGD	
T33	PM_DRAM_PWRGD	To	H_CPUPWRGD	
T34	VR_ON	To	SVID	
T35	H_CPUPWRGD	To	+VCC_CORE	
T36	+VCC_CORE	To	VGATE	
T37	VGATE	To	SYS_PWROK	
T38	SYS_PWROK	To	PCH_PLTRST#	
T39	DGPU_PWREN	To	+3VS_DELAY	
T40	DGPU_PWREN	To	+GPU_CORE	
T41	DGPU_PWREN	To	+1.5VSDGPU	
T42	DGPU_PWREN	To	+1.05VSDGPU	
T43	DGPU_PWREN	To	+1.05VSDGPU	

GPU power on sequence



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Issued Date	2011/08/25	Deciphered Date 2012/07/25	Title: Power Sequence

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