

Model Name: KAL80

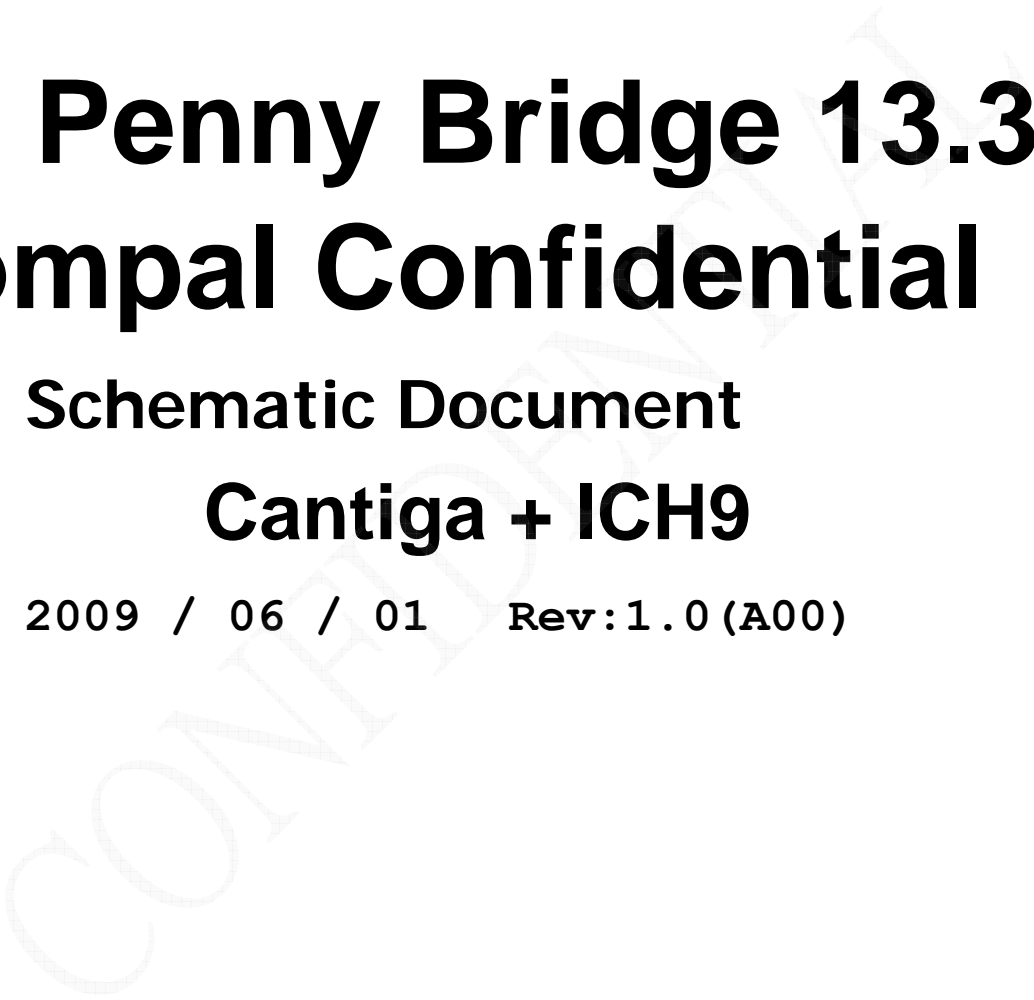
PCB NO: LA-4232P

BOM P/N:

Half Penny Bridge 13.3 Compal Confidential

Schematic Document Cantiga + ICH9

2009 / 06 / 01 Rev:1.0 (A00)



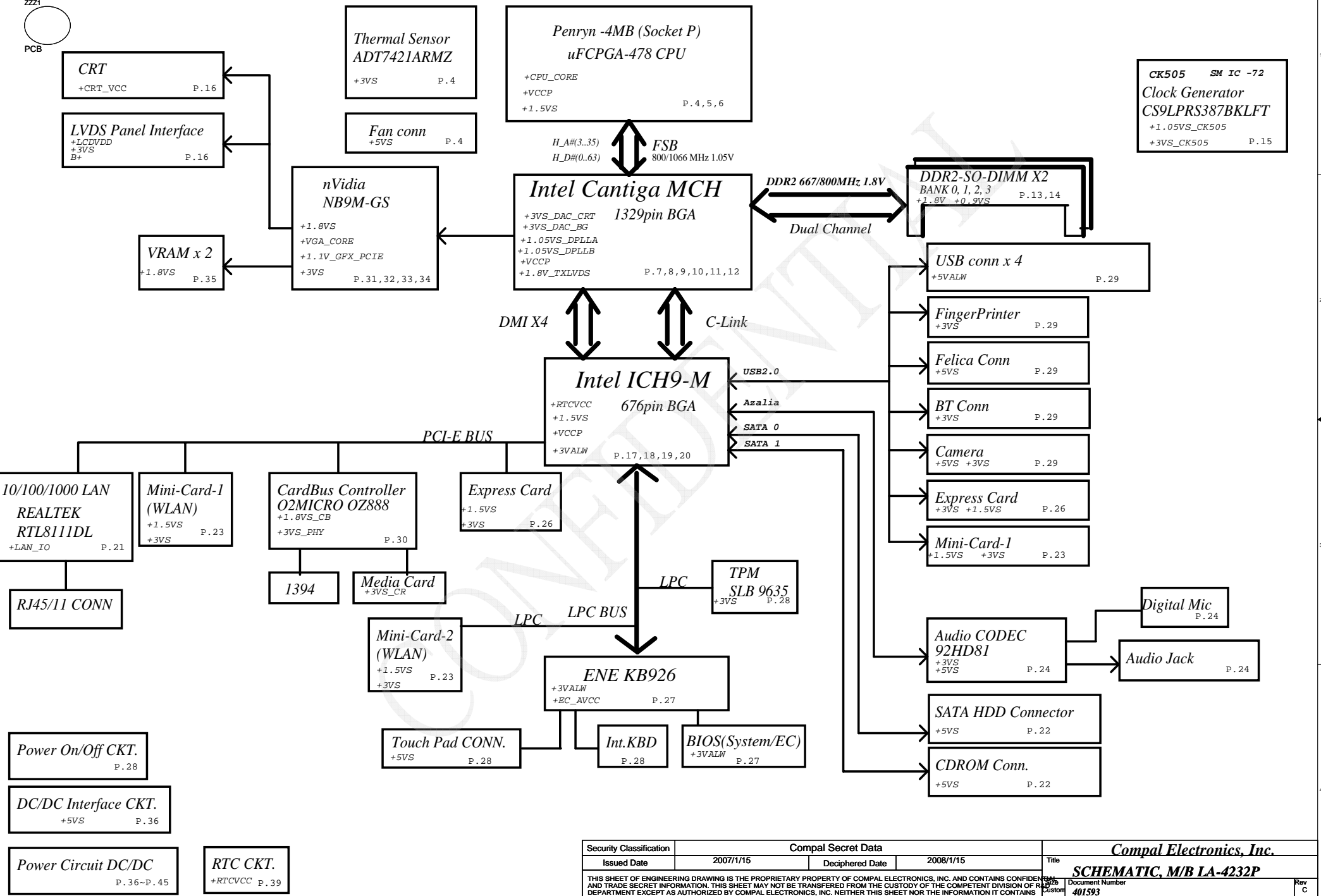
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Issued Date	2007/1/15	Deciphered Date	2008/1/15	Title	SCHEMATIC, M/B LA-4232P
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Half Penny Bridge 13.3

File Name : LA-4232P

zzz1

PCB




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Voltage Rails O MEANS ON X MEANS OFF

power plane	+B	+5VALW	+1.8V	+5VS
		+3VALW		+3VS
State				+1.5VS
				+0.9V
				+VCCP
				+CPU_CORE
				+VGA_CORE
				+1.8VS
				+1.1VS
				+0.9VGA
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build
 CONN@: connect
 VGA@: discrete component
 UMA@: uma component
 TPM@: TPM compoent

PCI EXPRESS	DESTINATION
Lane 1	NA
Lane 2	GLAN RTL8111DL
Lane 3	MINI CARD-2 WLAN
Lane 4	EXPRESS CARD
Lane 5	CARD READER OZ888
Lane 6	NA

SATA	DESTINATION
Lane 0	HDD
Lane 1	ODD
Lane 4	NA
Lane 5	NA

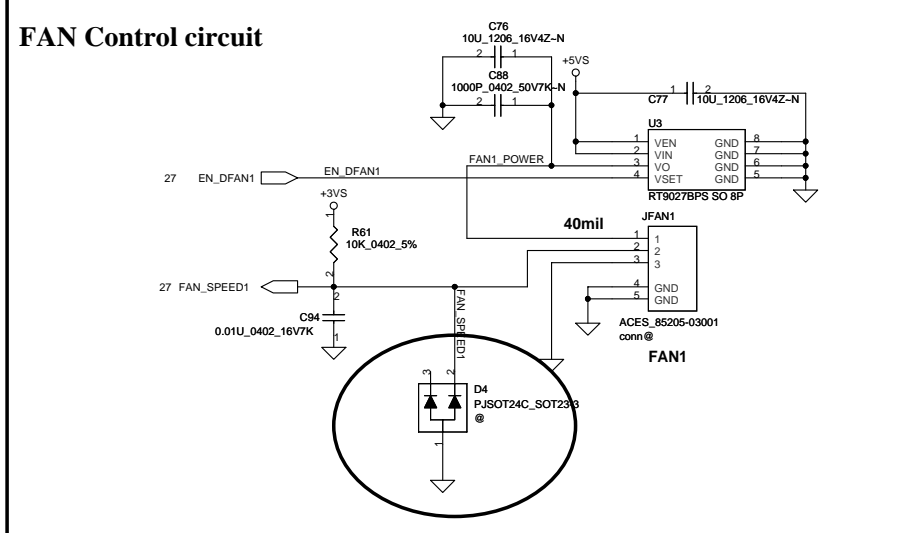
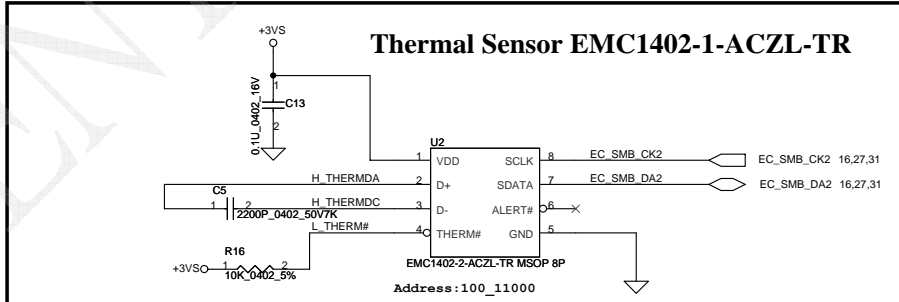
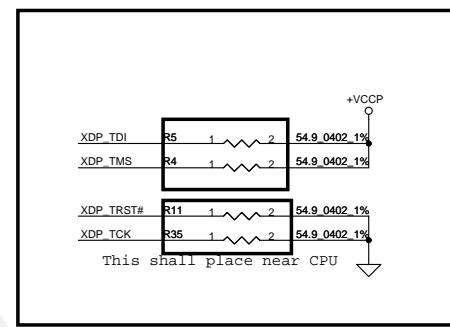
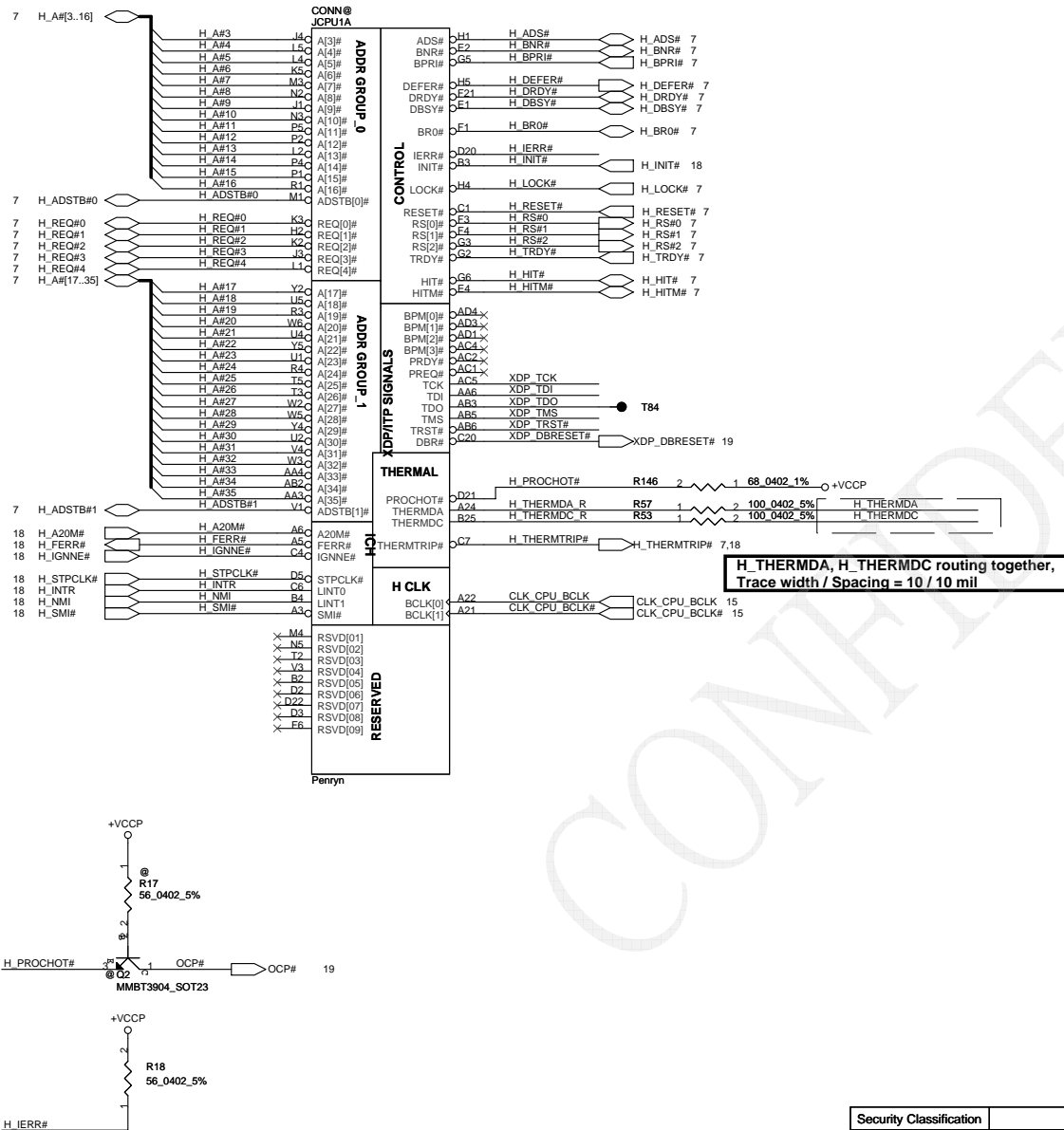
SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	X	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

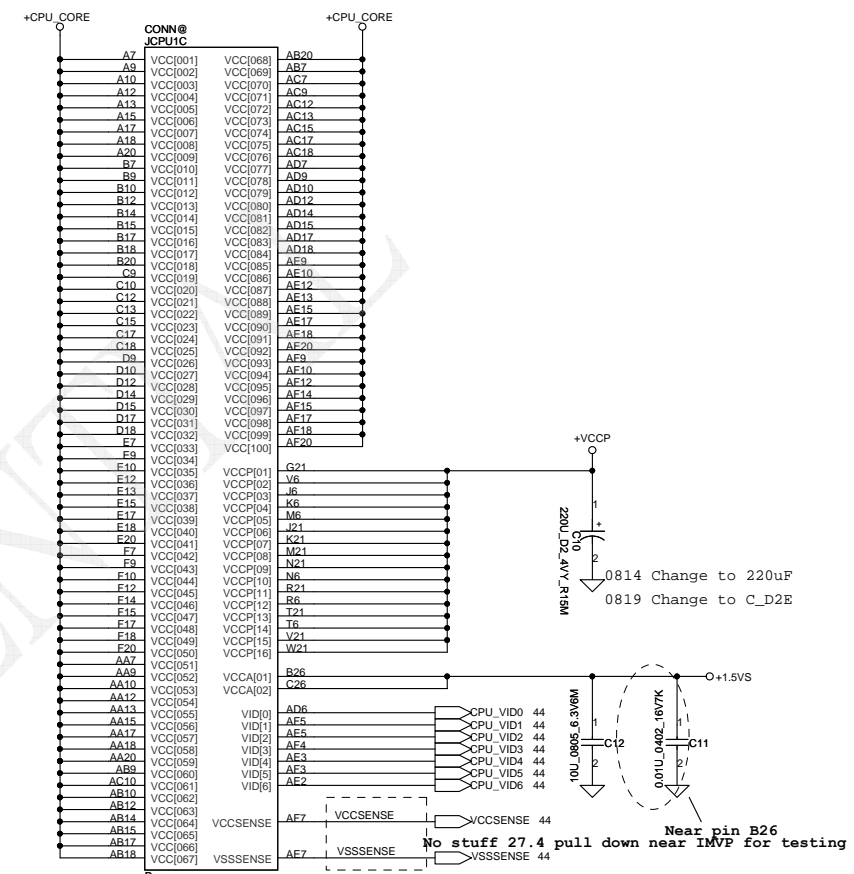
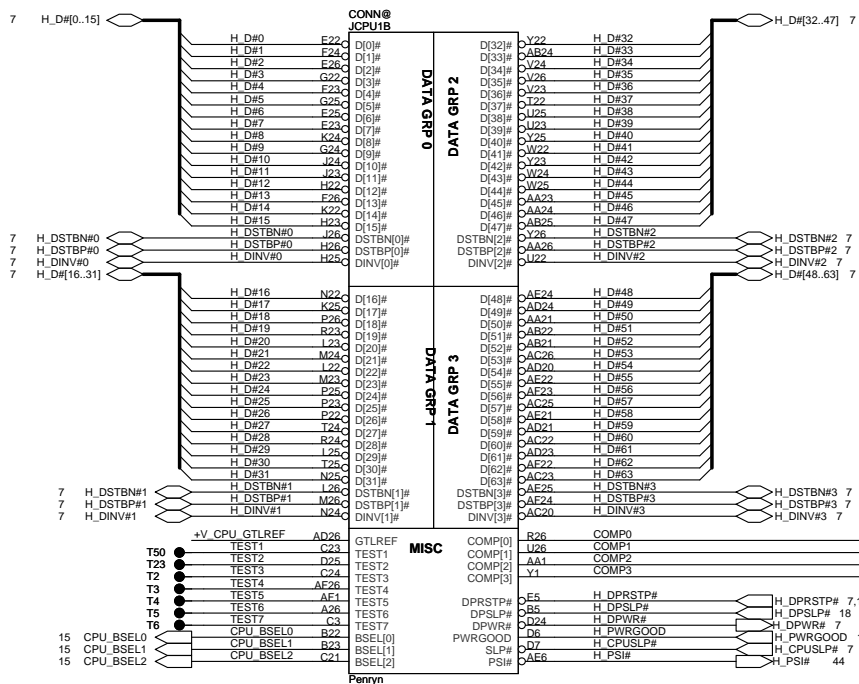
ICH9-M	USB PORT#	DESTINATION
	0	JUSBP1
	1	CAMERA
	2	JUSBP3(SINGLE)
	3	Felica
	4	Blue Tooth
	5	Finger Printer
	6	JMINI2-WLAN
	7	Express card
	8	JUSBP3(DUEL TOP)
	9	JUSBP3(DUEL BOTTOM)
	10	NA
11	NA	

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010



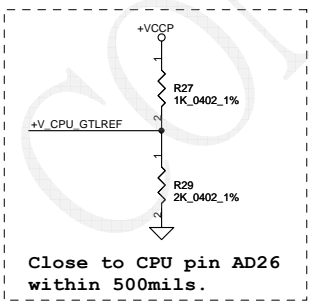
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layout note: Rout H_DPRSTP# from ICH9 to IMVP6 then to GMCH & CPU
 layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

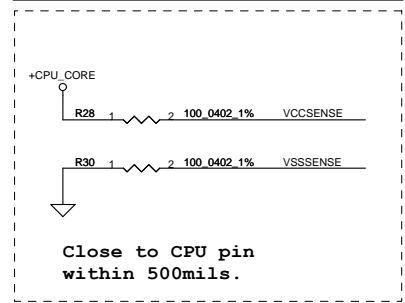
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 21 mils. COMP[1,3] trace width is 5



Close to CPU pin AD26 within 500mils.

Length match within 25 mils. The trace width/space/other is 20/7/25.

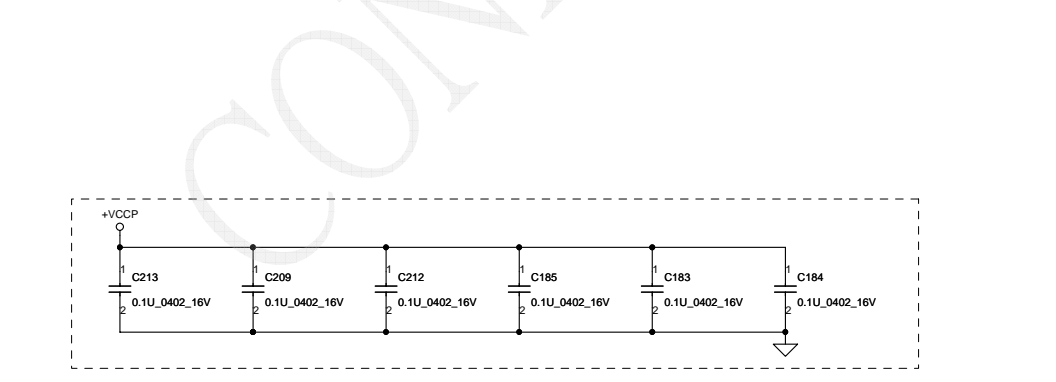
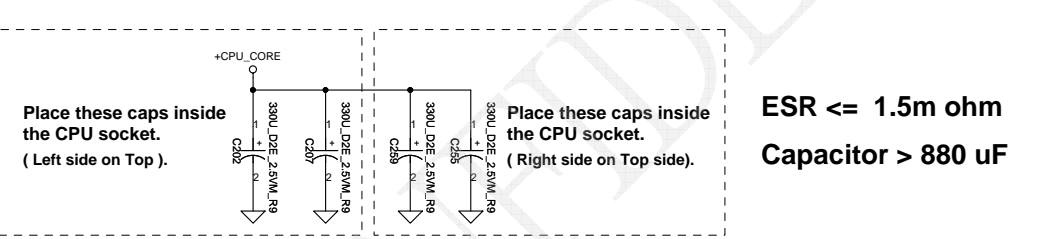
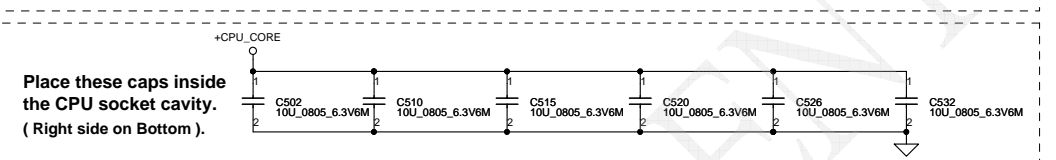
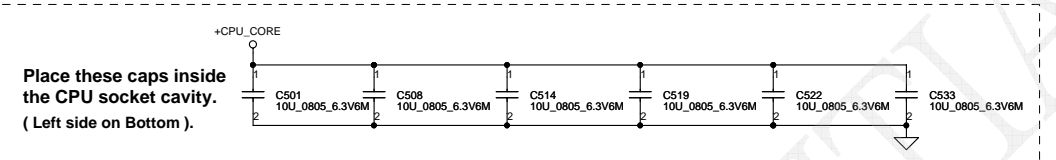
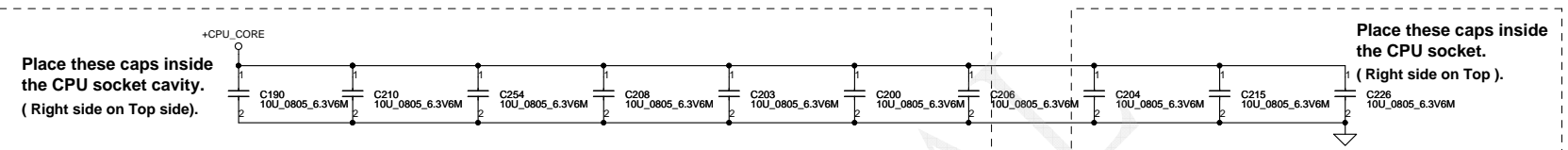
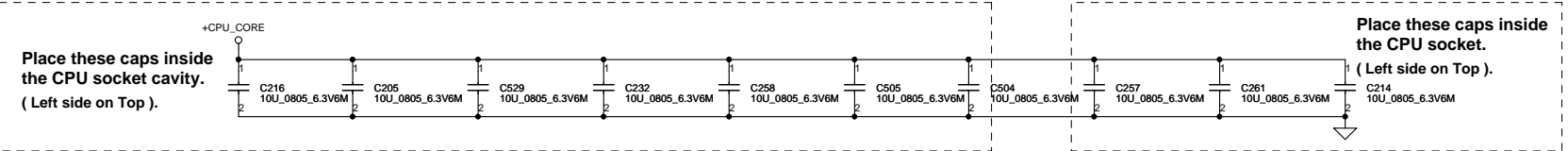


Close to CPU pin within 500mils.

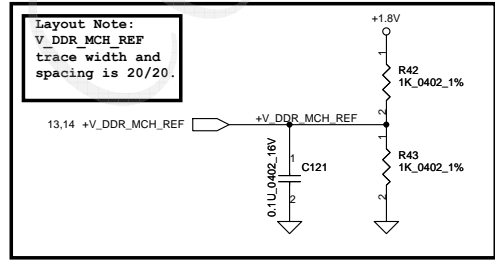
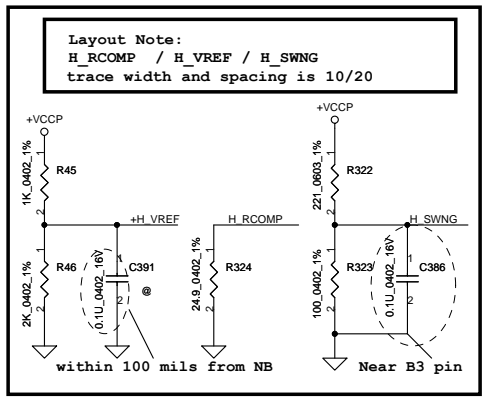
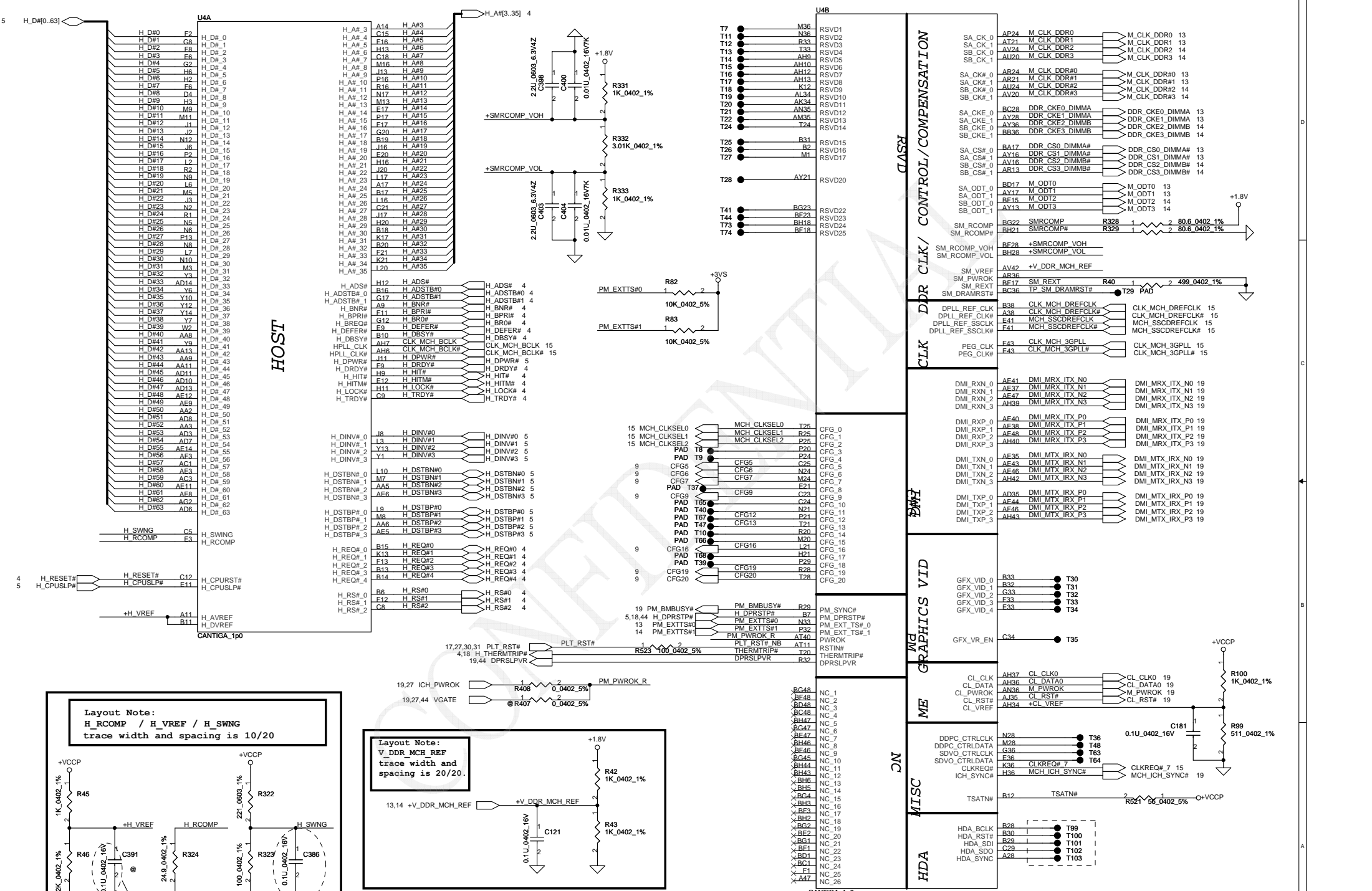
High Frequency Decoupling

10uF 0805 X5R -> 85 degree.

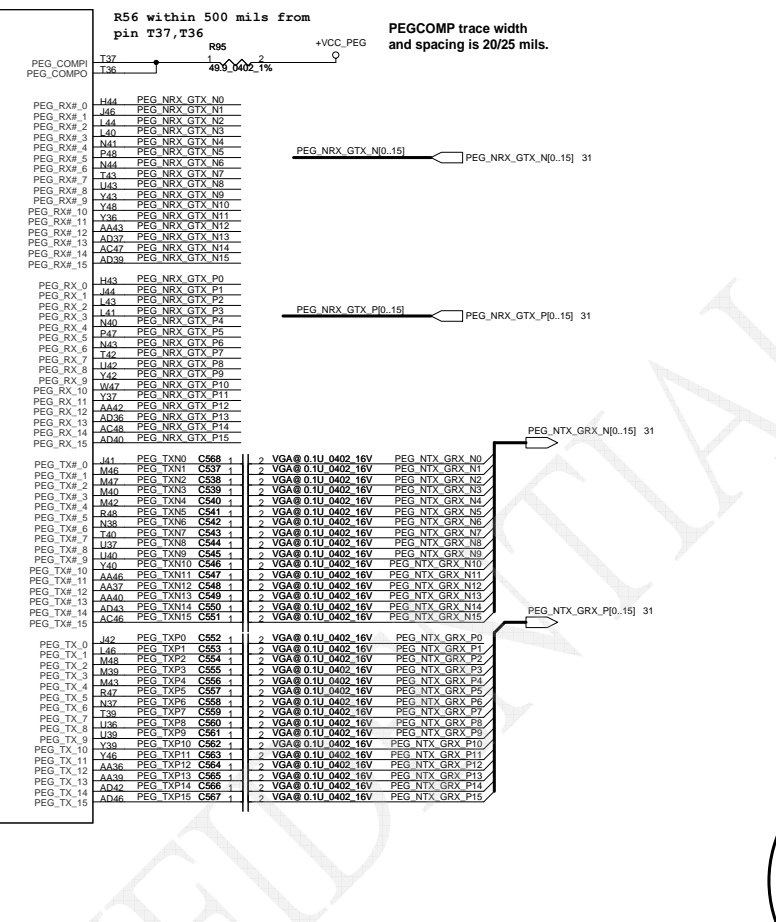
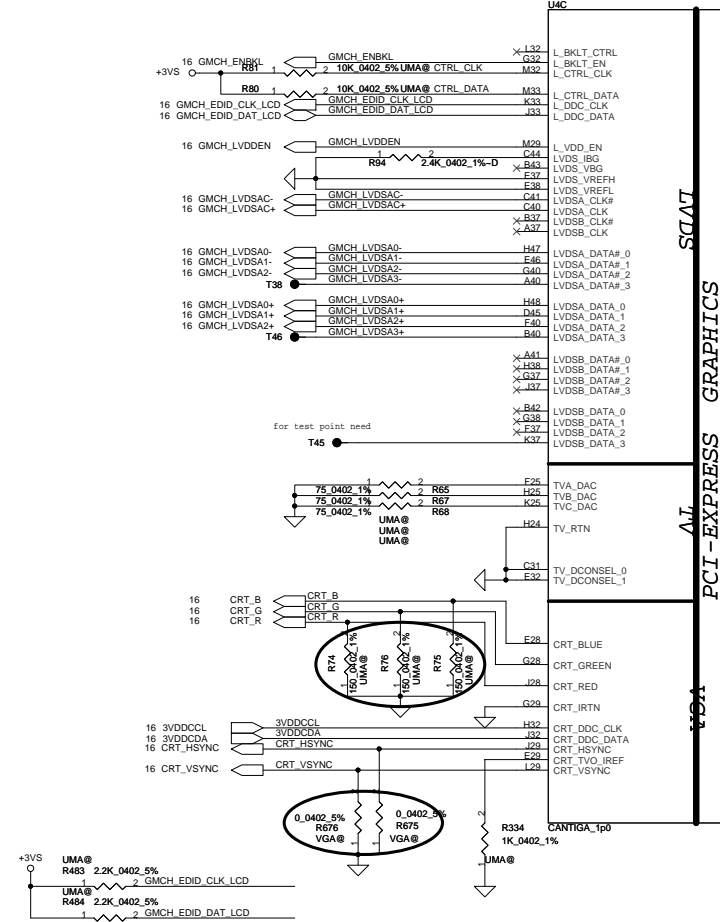
CONN#	ICPUID				
A4	VSS001	VSS082	P6		
A8	VSS002	VSS083	P21		
A11	VSS003	VSS084	P24		
A14	VSS004	VSS085	R5		
A16	VSS005	VSS086	R22		
A23	VSS007	VSS088	R25		
AE2	VSS008	VSS089	T1		
B6	VSS009	VSS090	T4		
B8	VSS010	VSS091	T23		
B11	VSS011	VSS092	T26		
B13	VSS012	VSS093	U3		
B16	VSS013	VSS094	U6		
B19	VSS014	VSS095	U21		
B21	VSS015	VSS096	U24		
B24	VSS016	VSS097	V5		
C5	VSS017	VSS098	V22		
C8	VSS018	VSS099	V25		
C11	VSS019	VSS100	W1		
C14	VSS020	VSS101	W4		
C16	VSS021	VSS102	W23		
C19	VSS022	VSS103	W26		
C2	VSS023	VSS104	Y3		
C22	VSS024	VSS105	Y6		
C25	VSS025	VSS106	Y21		
D1	VSS026	VSS107	Y24		
D4	VSS027	VSS108	AA2		
D8	VSS028	VSS109	AA5		
D11	VSS029	VSS110	AA8		
D16	VSS030	VSS111	AA11		
D19	VSS031	VSS112	AA14		
D23	VSS032	VSS113	AA17		
D26	VSS033	VSS114	AA19		
E3	VSS034	VSS115	AA22		
E6	VSS035	VSS116	AA25		
FR	VSS036	VSS117	AB1		
FR	VSS037	VSS118	AB4		
F11	VSS038	VSS119	AB8		
F14	VSS039	VSS120	AB11		
F16	VSS040	VSS121	AB13		
F19	VSS041	VSS122	AB16		
E21	VSS042	VSS123	AB19		
E24	VSS043	VSS124	AB23		
F6	VSS044	VSS125	AB26		
FR	VSS045	VSS126	AC3		
F11	VSS046	VSS127	AC6		
F16	VSS047	VSS128	AC8		
F19	VSS048	VSS129	AC11		
F22	VSS049	VSS130	AC14		
F25	VSS050	VSS131	AC16		
G4	VSS051	VSS132	AC19		
G1	VSS052	VSS133	AC21		
G23	VSS053	VSS134	AC24		
G26	VSS054	VSS135	AD2		
H3	VSS055	VSS136	AD5		
H3	VSS056	VSS137	AD8		
HR	VSS057	VSS138	AD11		
H21	VSS058	VSS139	AD13		
H24	VSS059	VSS140	AD16		
J2	VSS060	VSS141	AD19		
J5	VSS061	VSS142	AD22		
J22	VSS062	VSS143	AD25		
J26	VSS063	VSS144	AE1		
K1	VSS064	VSS145	AE4		
K4	VSS065	VSS146	AE8		
K23	VSS066	VSS147	AE11		
K26	VSS067	VSS148	AE14		
L3	VSS068	VSS149	AE16		
L6	VSS069	VSS150	AE19		
L21	VSS070	VSS151	AE23		
L24	VSS071	VSS152	AE26		
M2	VSS072	VSS153	A2		
M24	VSS073	VSS154	AE6		
M5	VSS074	VSS155	AE8		
M22	VSS075	VSS156	AE11		
M26	VSS076	VSS157	AE13		
N1	VSS077	VSS158	AE16		
N4	VSS078	VSS159	AE19		
N23	VSS079	VSS160	AE21		
N26	VSS080	VSS161	A25		
P3	VSS081	VSS162	AF25		
		VSS163			



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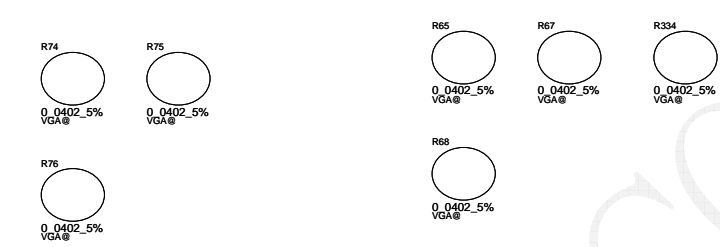
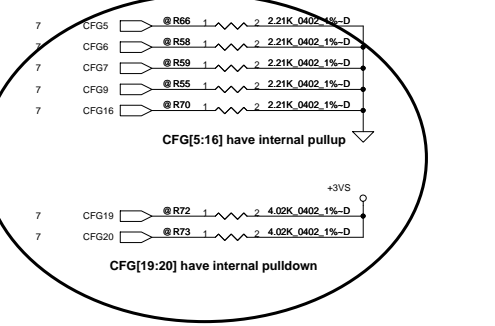


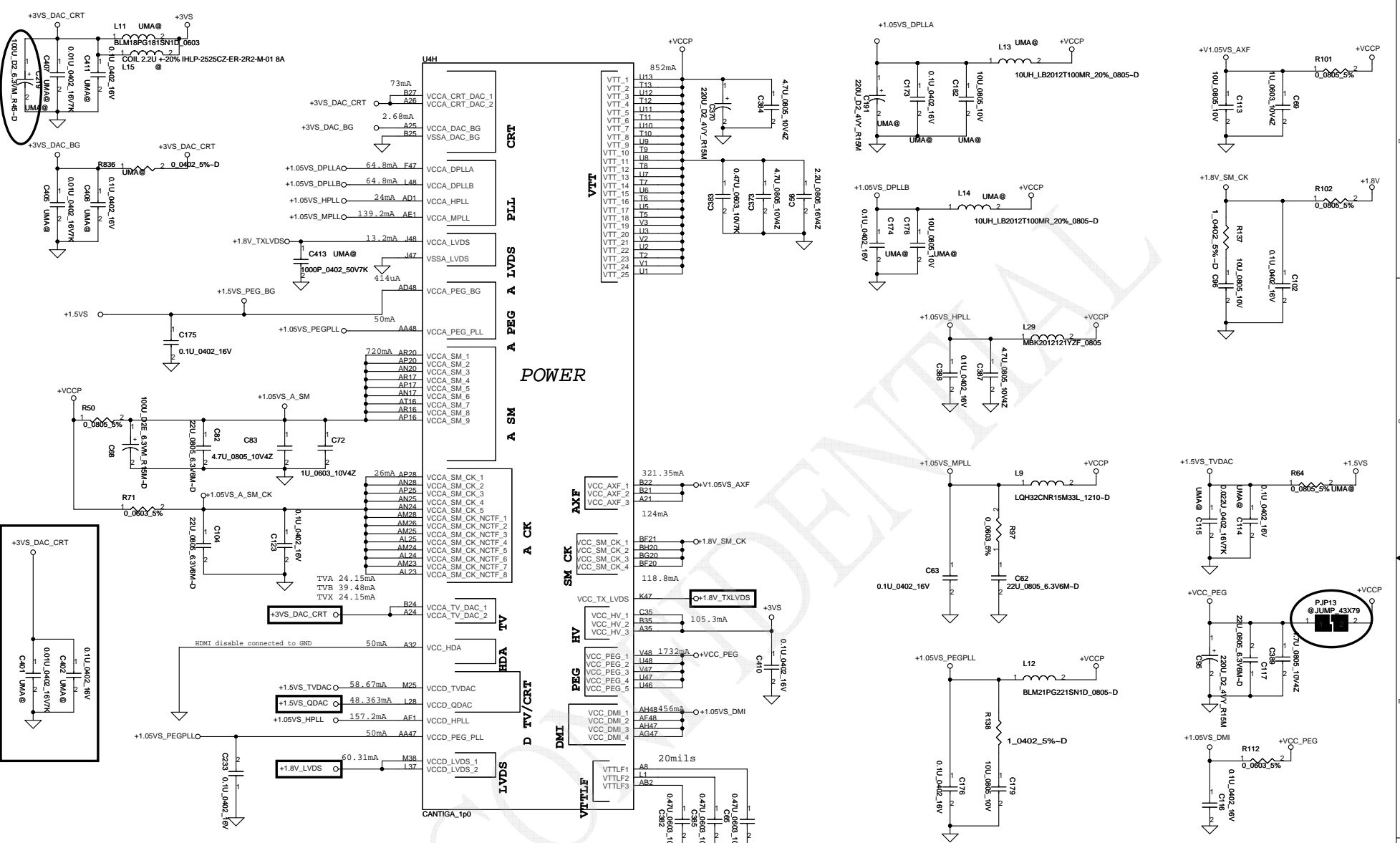
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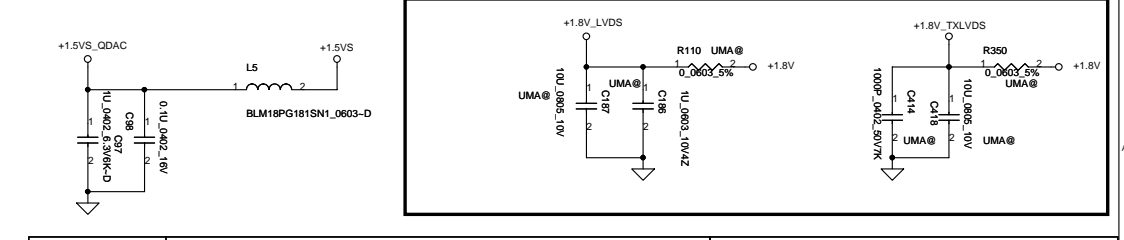
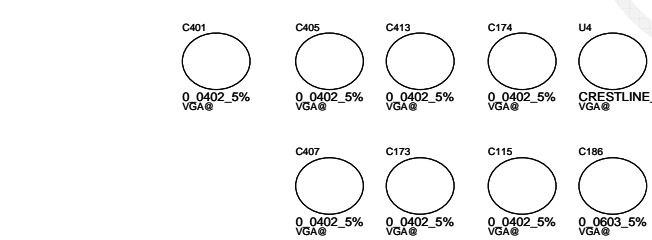
Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable * 1 = The iTPM Host Interface is disable
CFG7 (Intel Management Engine Crypto strap)	0 = (TLS)chiper suite with no confidentiality 1 = (TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation, Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.



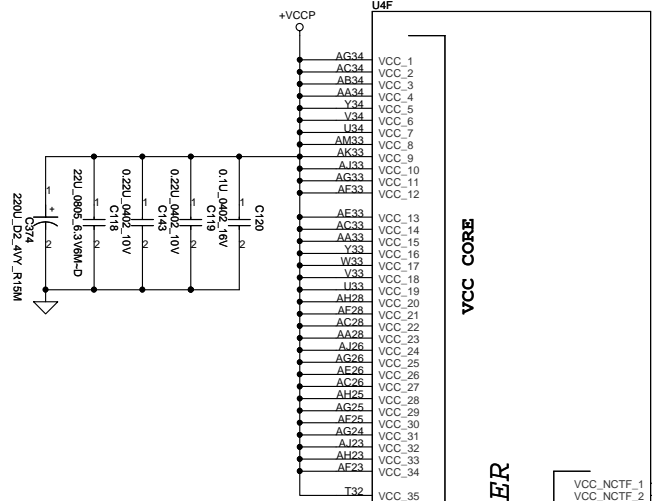


POWER



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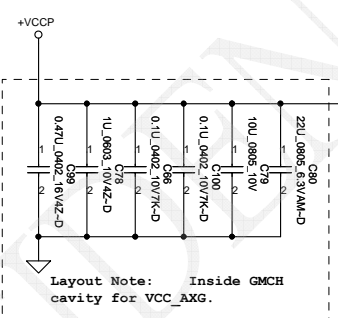
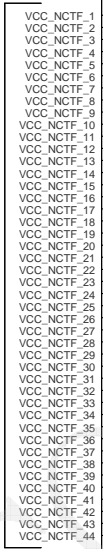
Extnal Graphic: 1210.34mA
 Integrated Graphic: 1930.4mA



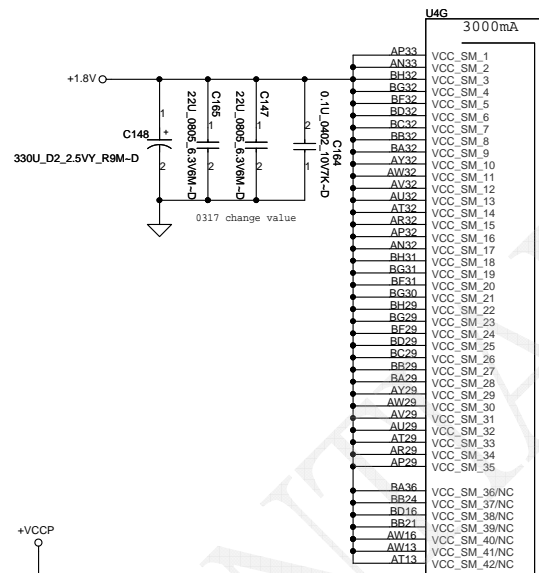
VCC CORE

POWER

VCC NCTF



Layout Note: Inside GMCH cavity for VCC_AXG.



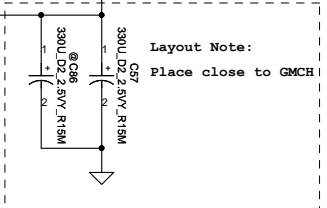
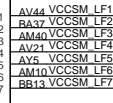
VCC SM

POWER

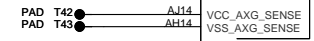
VCC GFX NCTF

VCC GFX

VCC SM LF

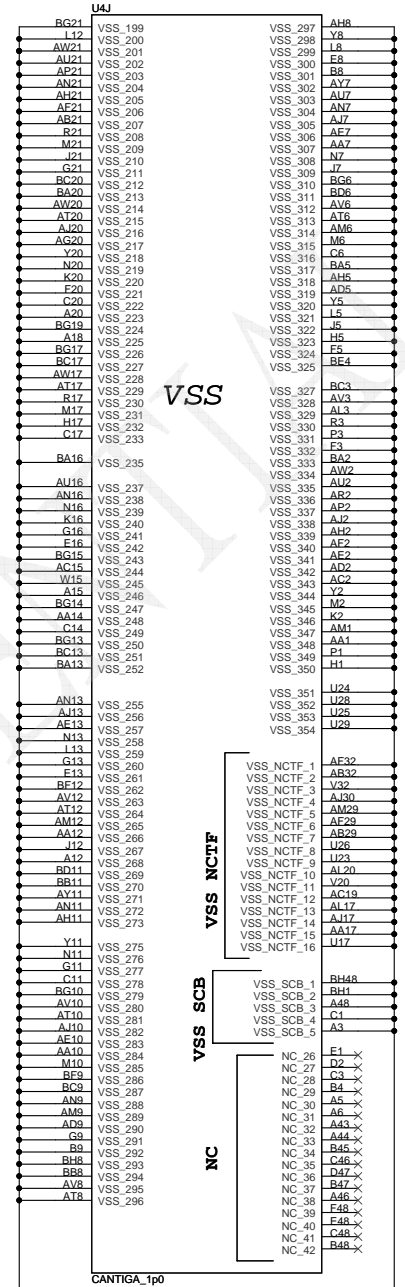
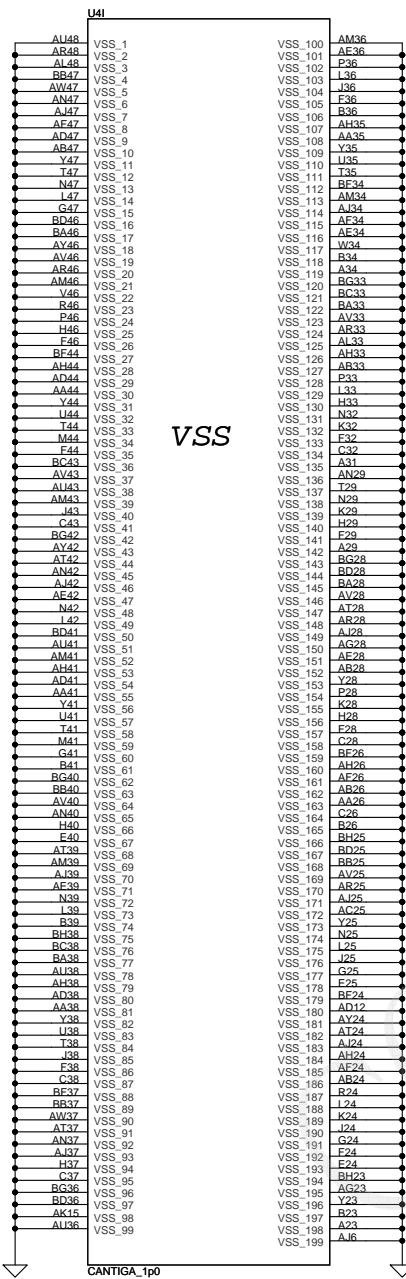


Layout Note:
Place close to GMCH



CANTIGA_1p0

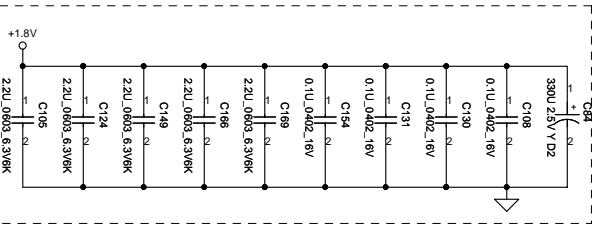
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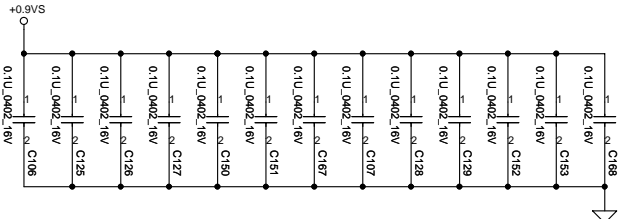
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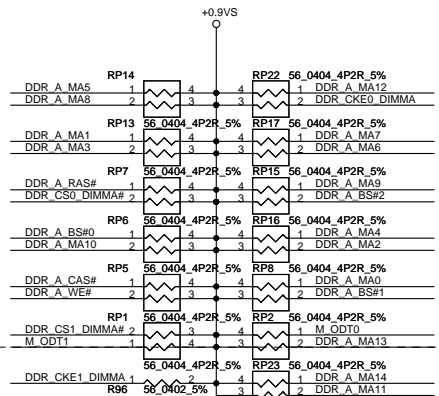
Layout Note:
Place near JDIM1



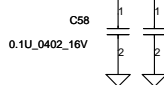
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V



Layout Note:
Place these resistor closely JP41, all trace length Max=1.5"



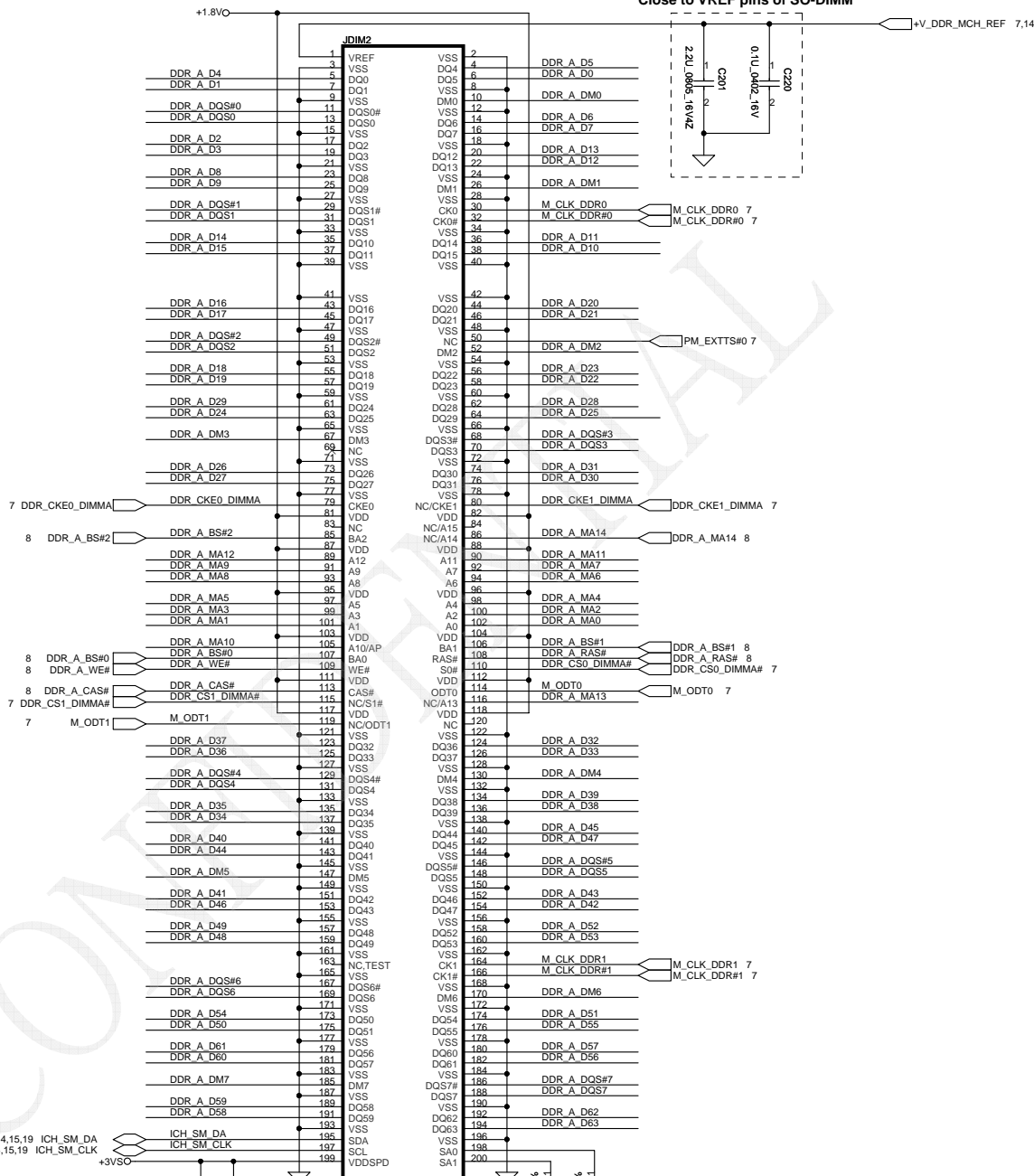
14,15,19 ICH_SM_DA
14,15,19 ICH_SM_CLK

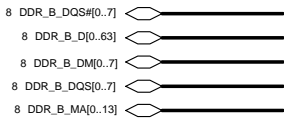


SO-DIMM A
REVERSE
Bottom side

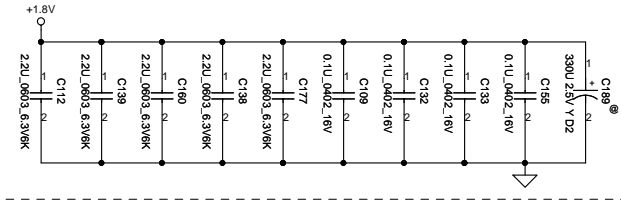
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/1/15	Deciphered Date	2008/1/15	Title	SCHEMATIC, M/B LA-4232P
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Close to VREF pins of SO-DIMM

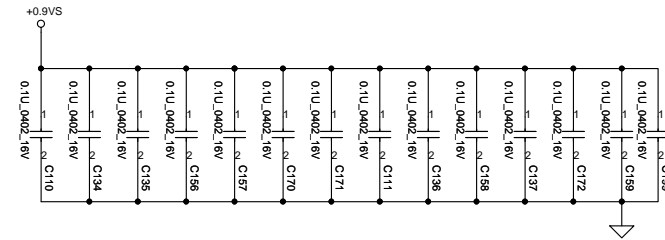




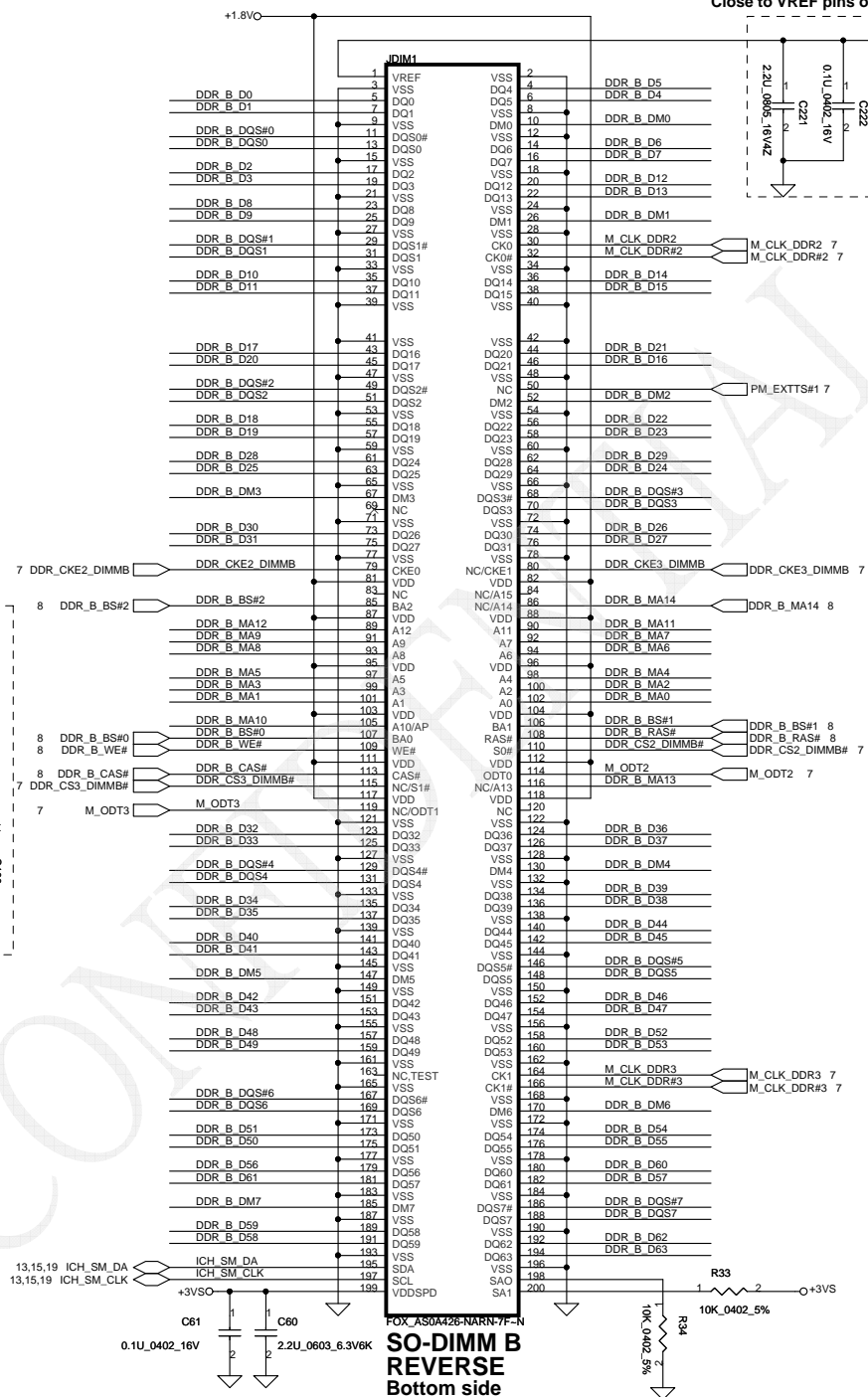
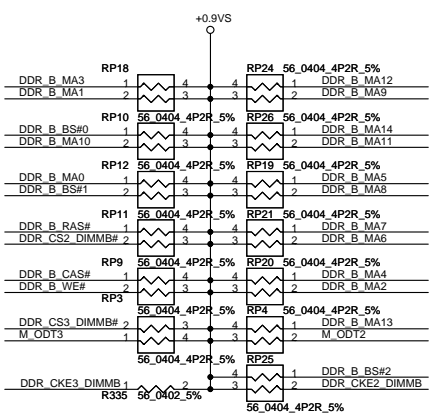
Layout Note:
Place near JDIM2



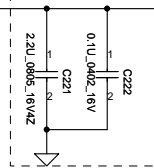
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistor closely JP42, all trace length Max=1.5"



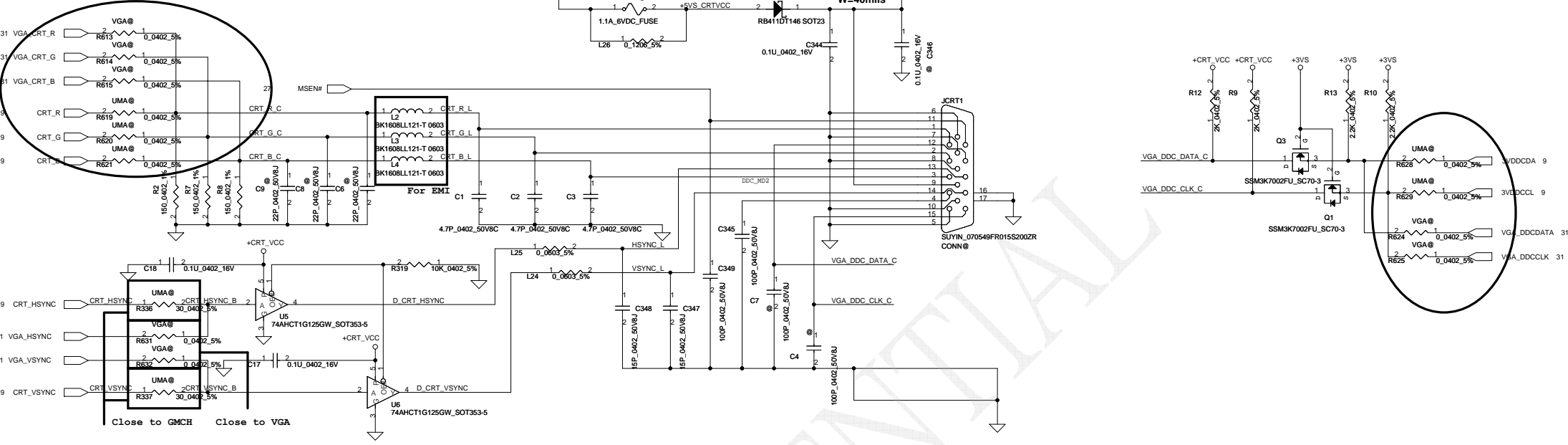
Close to VREF pins of SO-DIMM



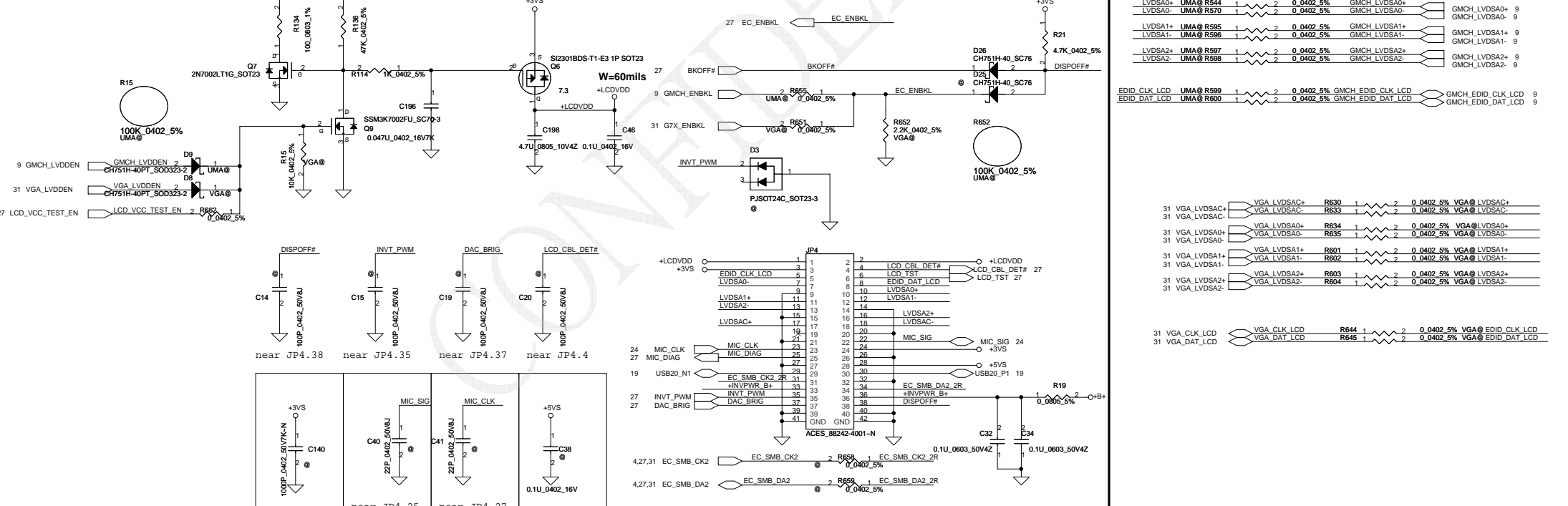
SO-DIMM B REVERSE Bottom side

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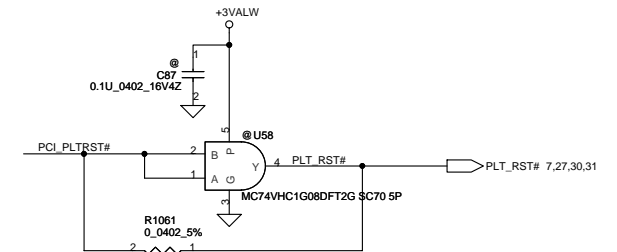
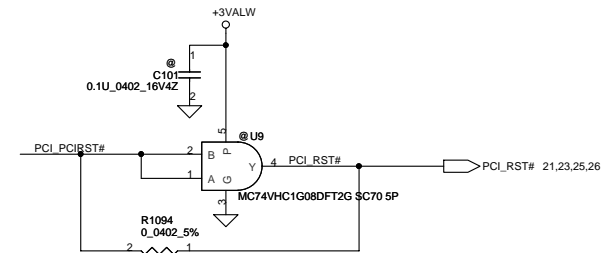
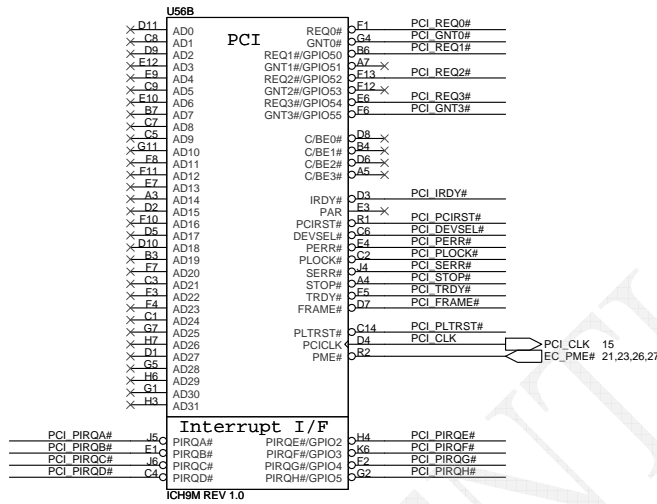
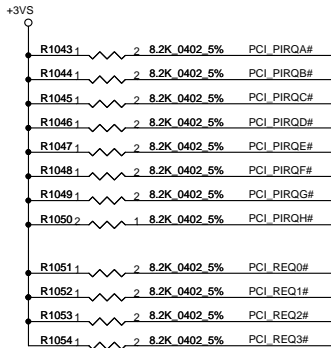
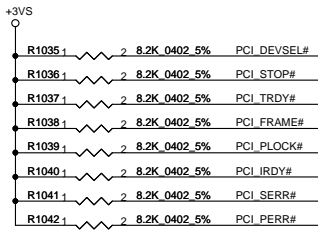
CRT



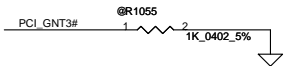
LCD



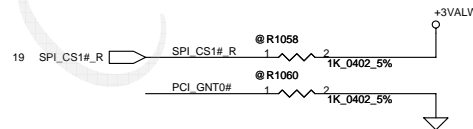
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Issued Date	2007/1/15	Deciphered Date	2008/1/15	Title	SCHMATIC, M/B LA-4232P
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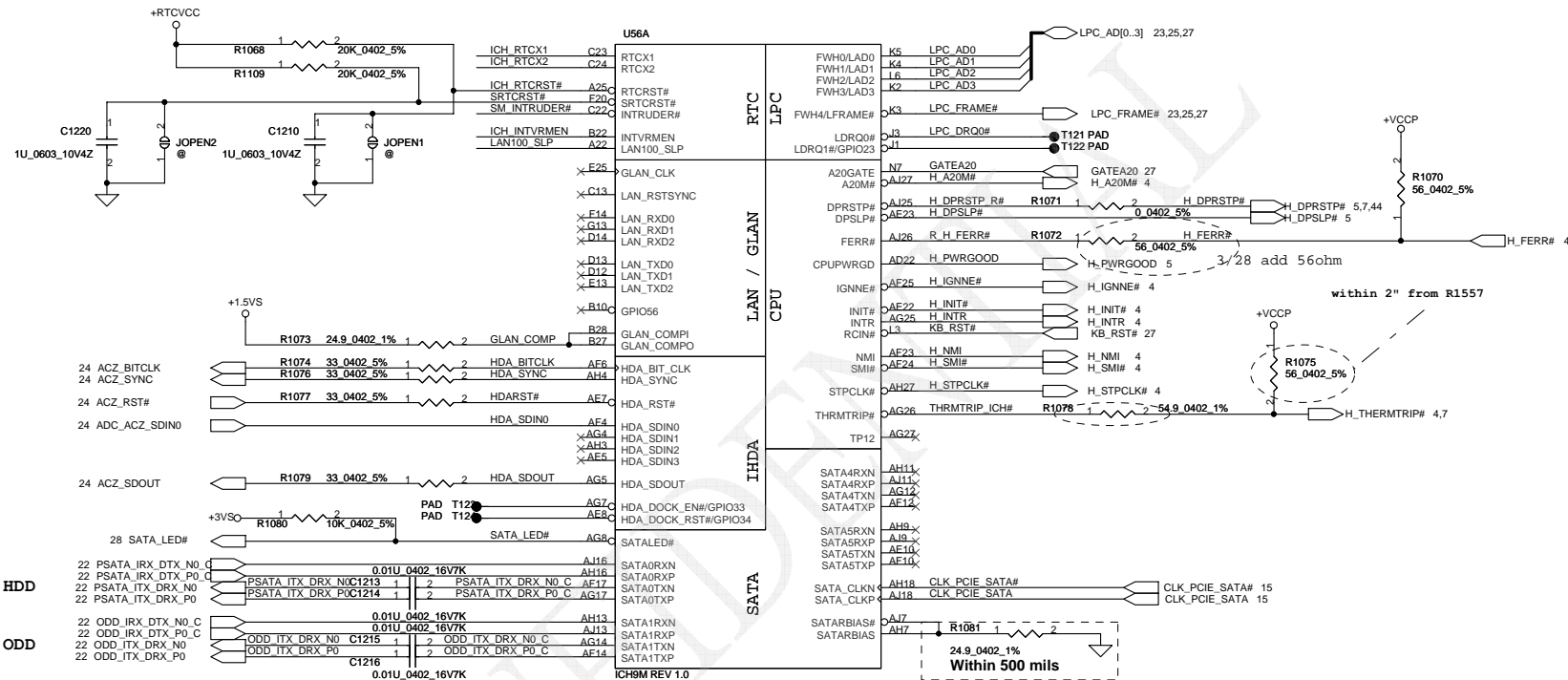
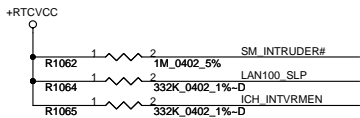


A16 swap override Strap
 Low= A16 swap override Enable
 High= Default*

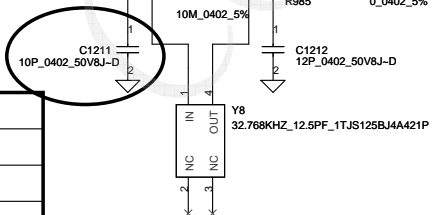
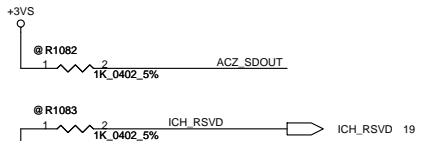


Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *





HDD
ODD

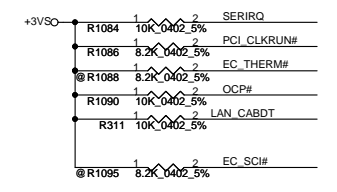


XOR CHAIN ENTRANCE STRAP:RSVD

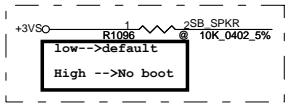
XOR Chain Entrance Strap		
ICH_RSVD_TP3	HDA SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1

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		2006/03/10
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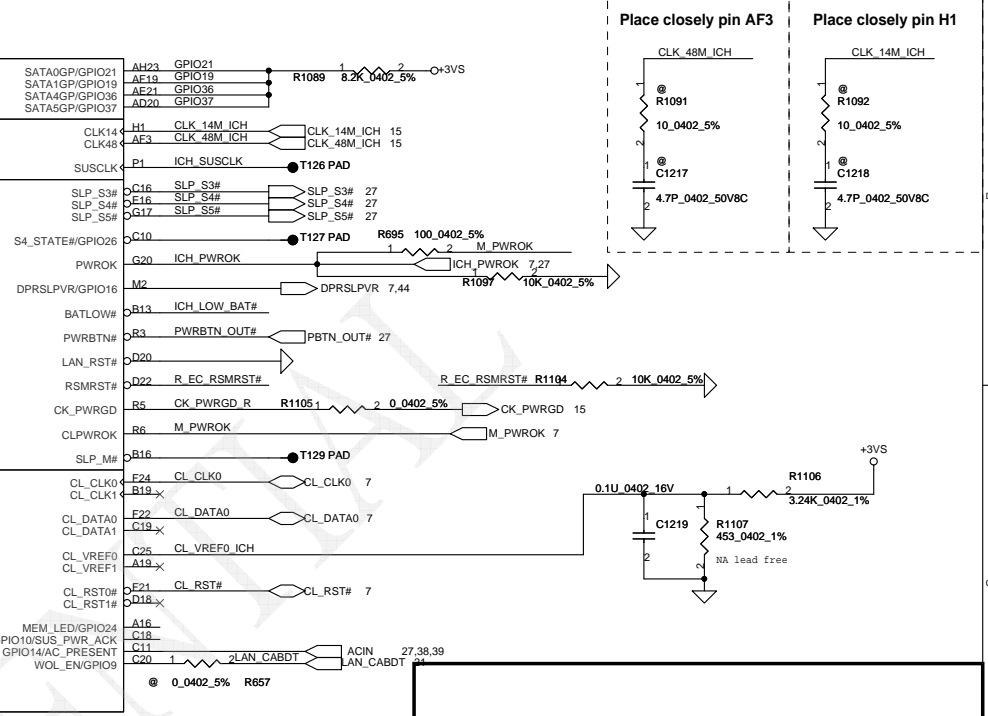
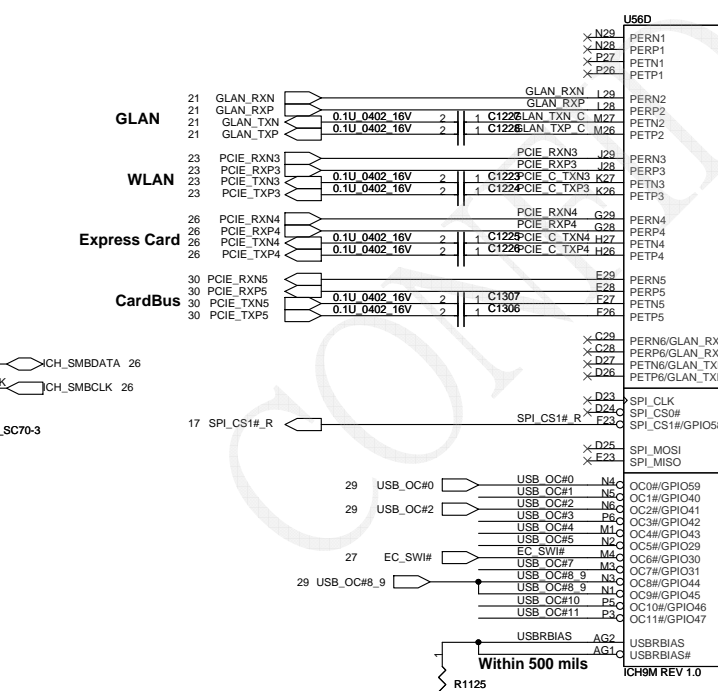
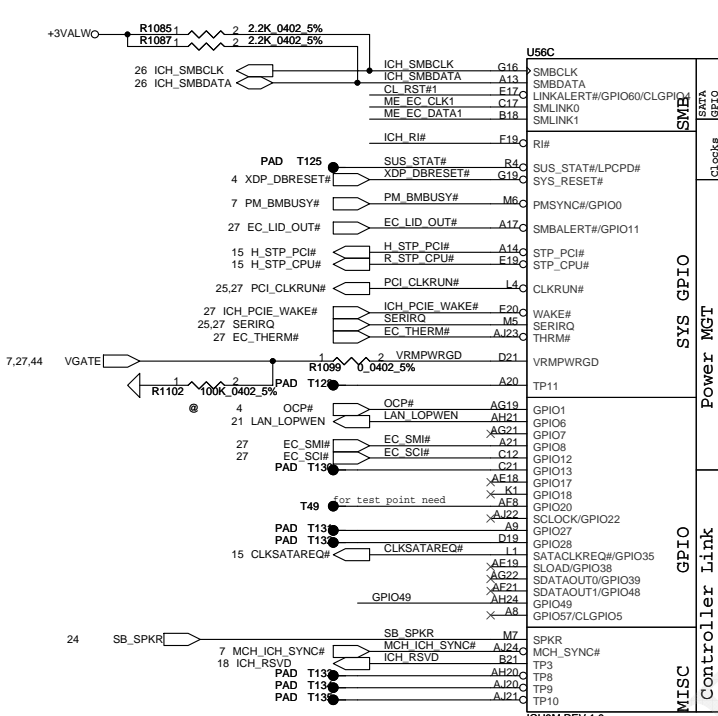
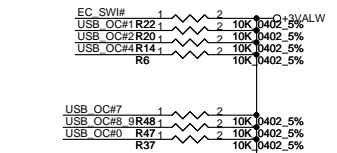
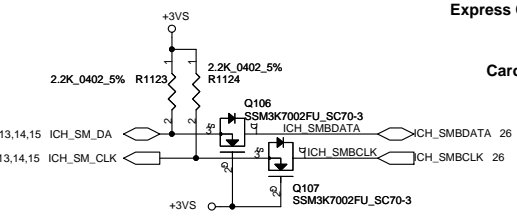
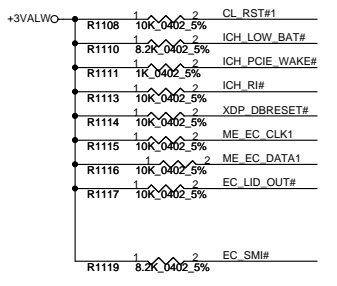
Title		Compal Electronics, Inc.	
SCHEMATIC, M/B LA-4232P		Document Number	401593
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ICH8 don't have

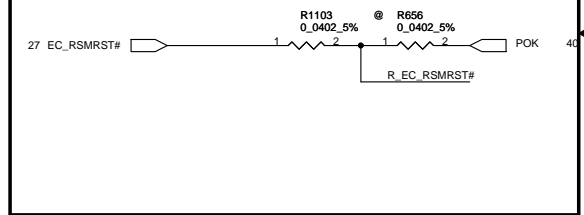


checklist pull hi

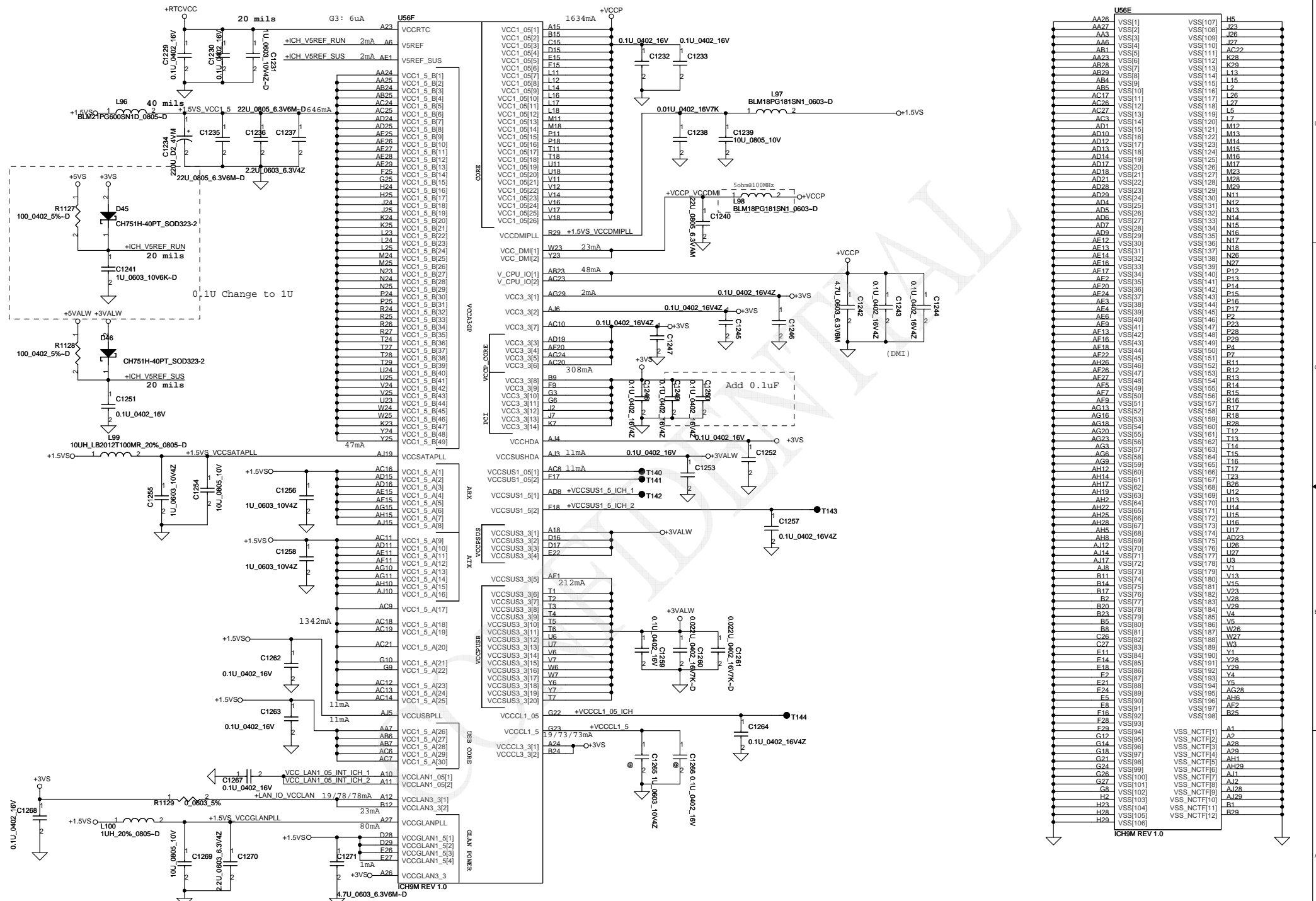


Place closely pin AF3 Place closely pin H1

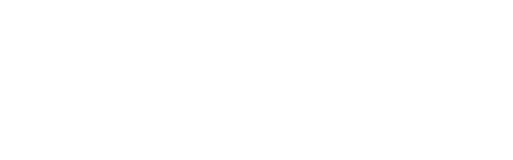
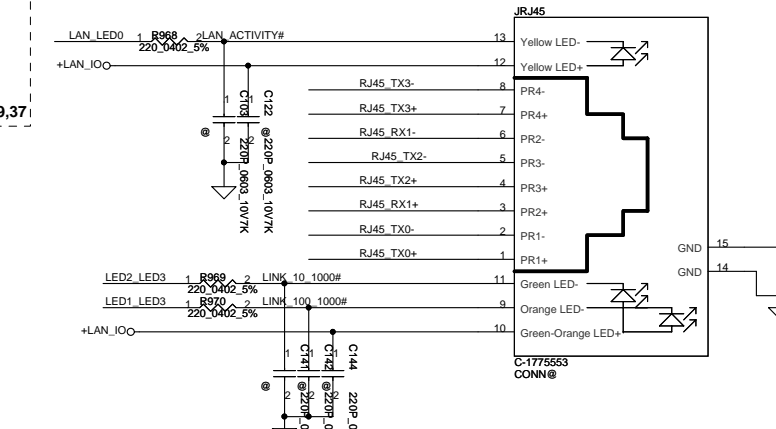
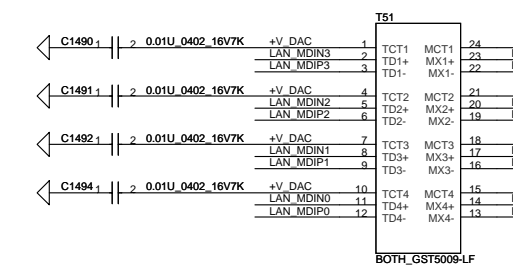
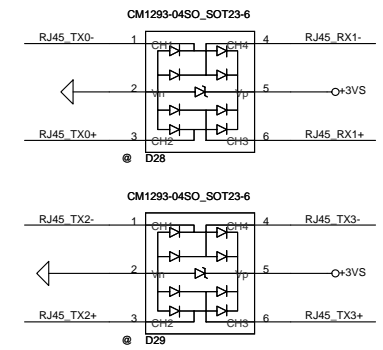
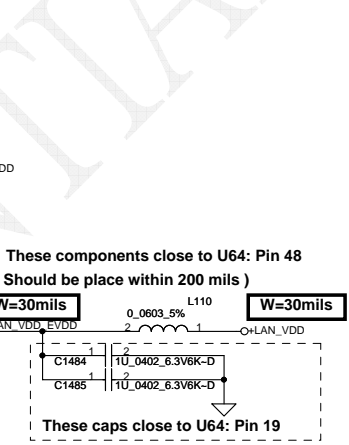
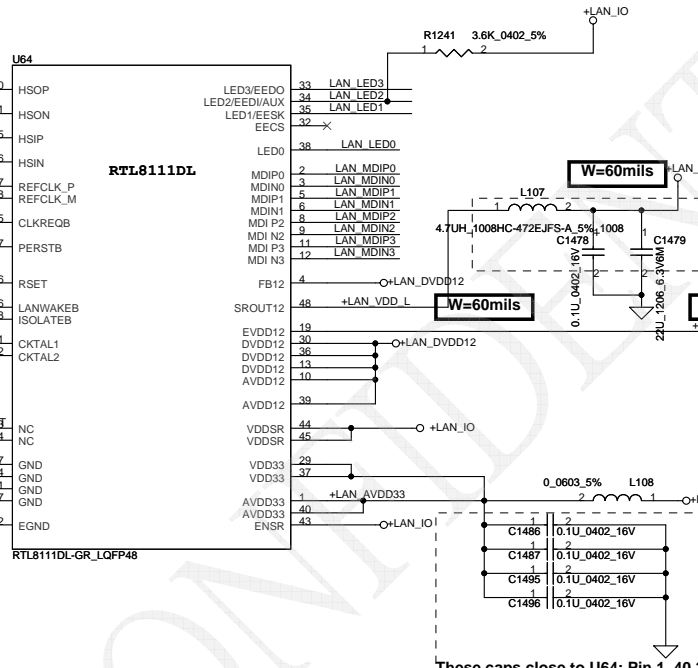
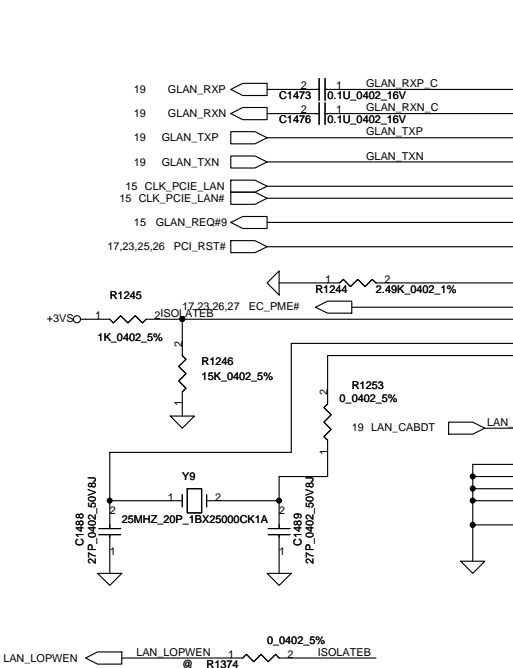
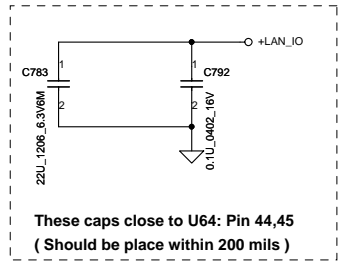
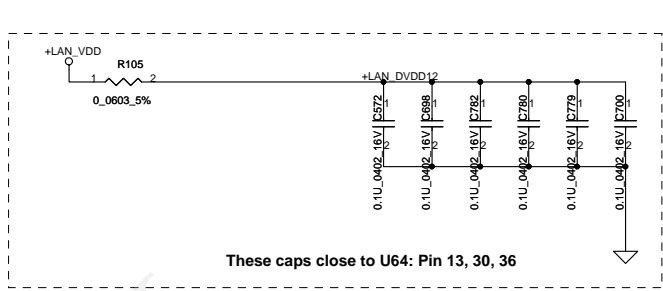
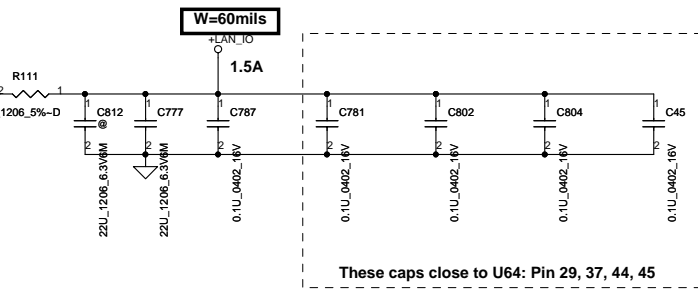
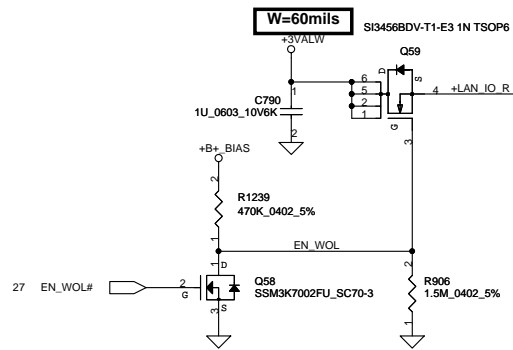
RSMRST circuit



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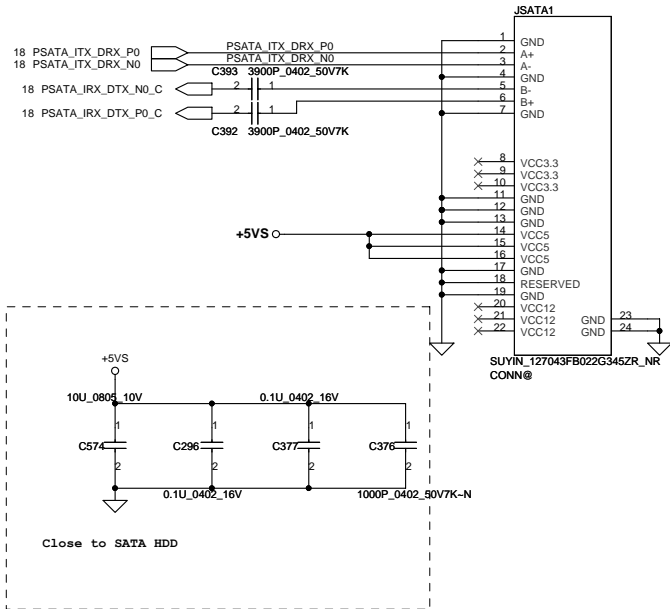


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AA27	VSS[2]
AA3	VSS[3]
AA4	VSS[4]
AA5	VSS[5]
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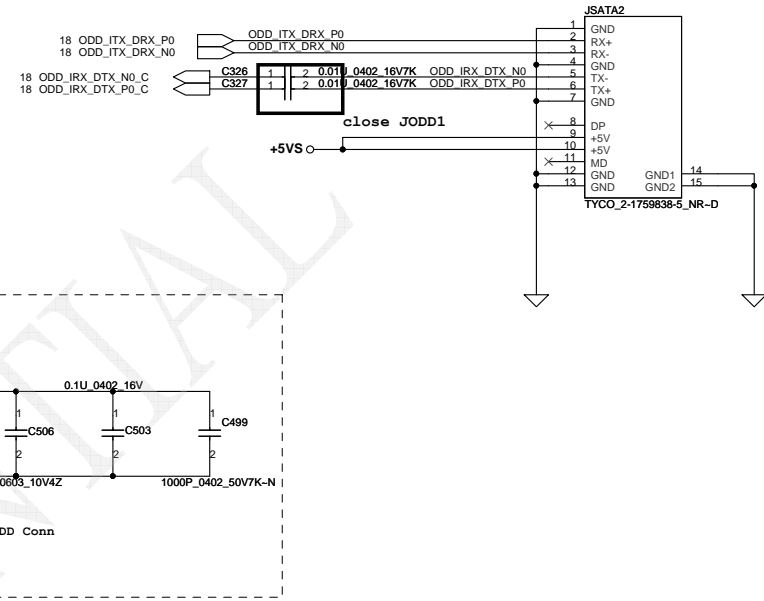


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SATA HDD CONN



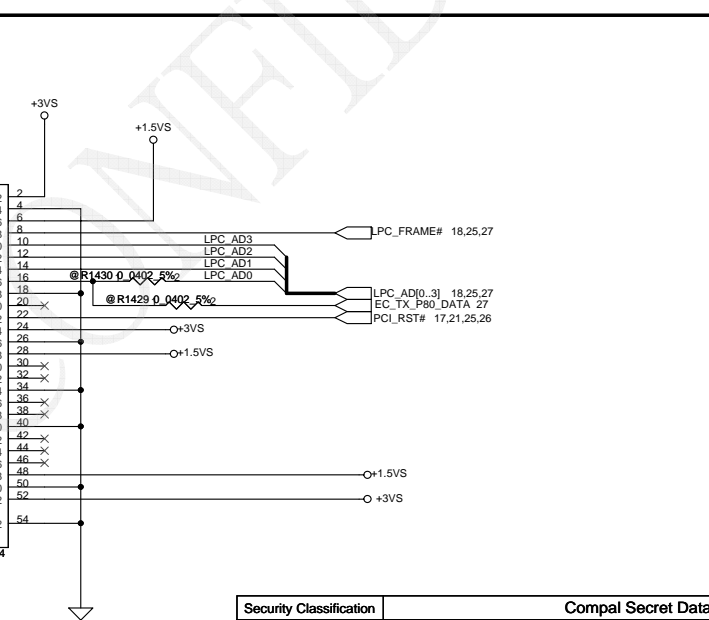
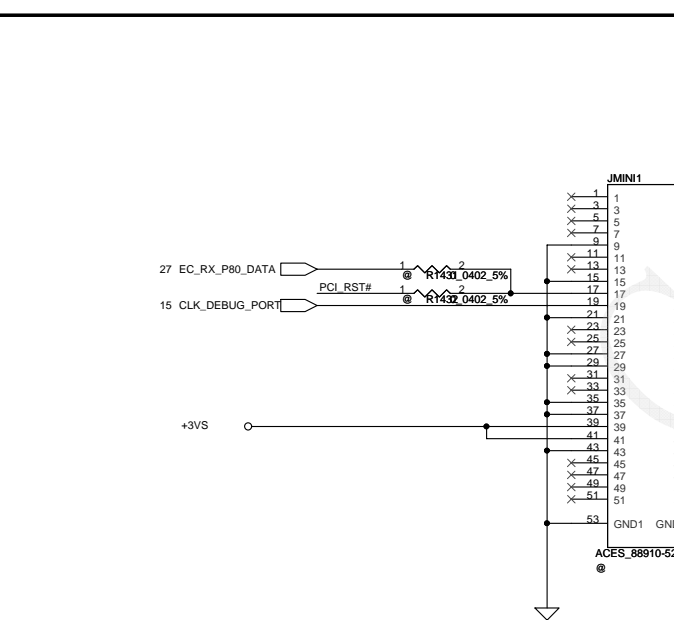
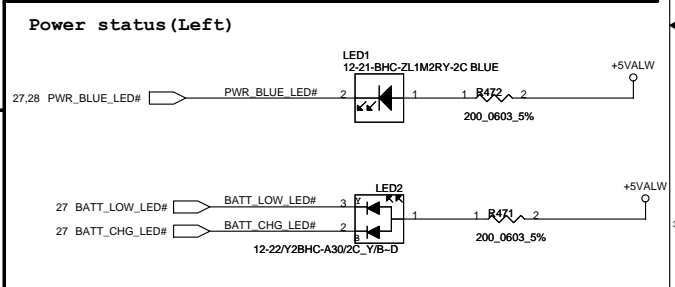
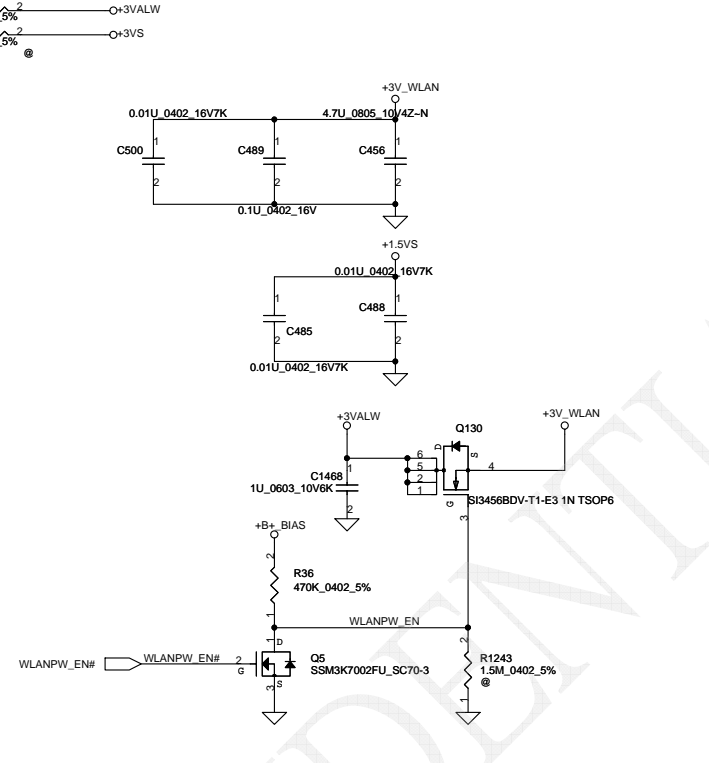
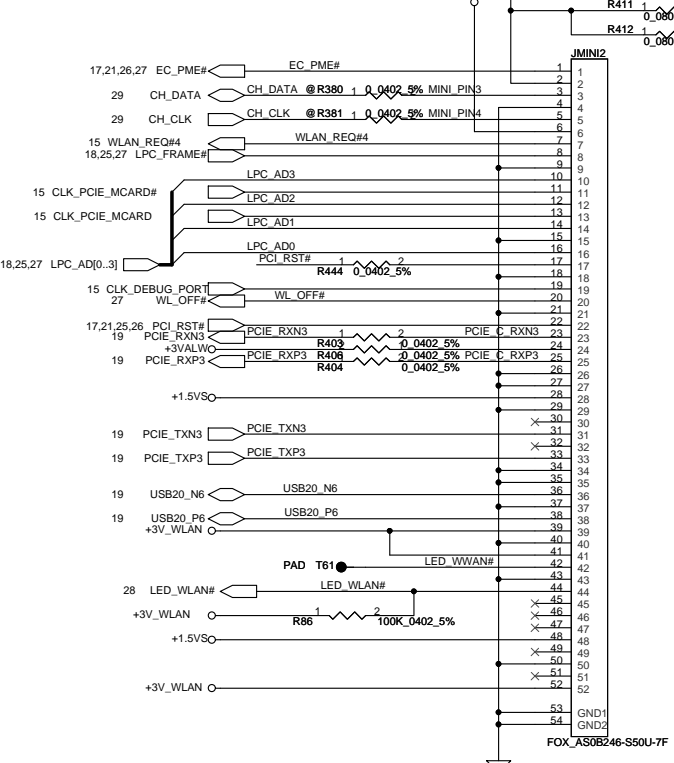
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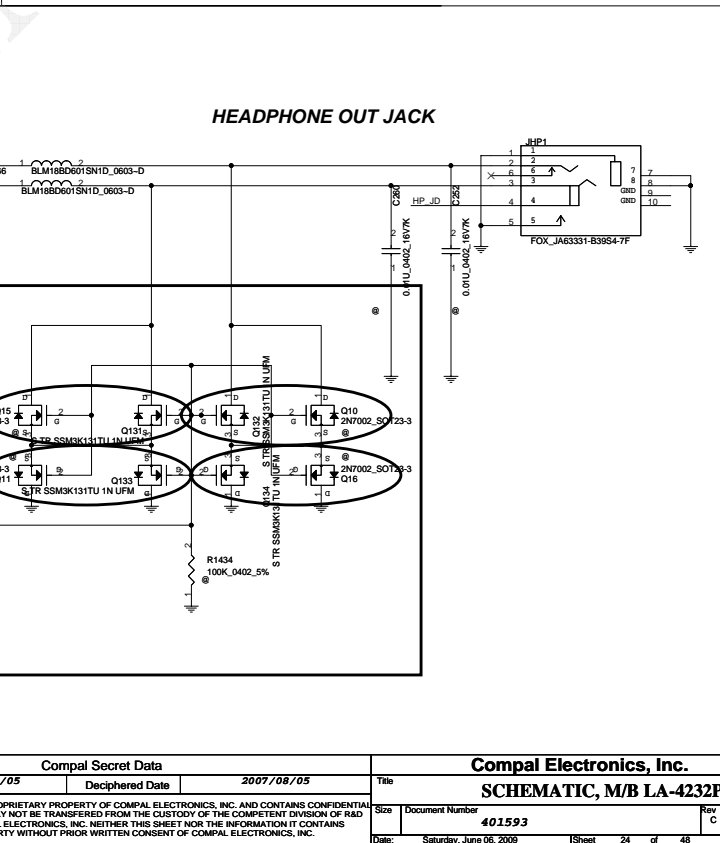
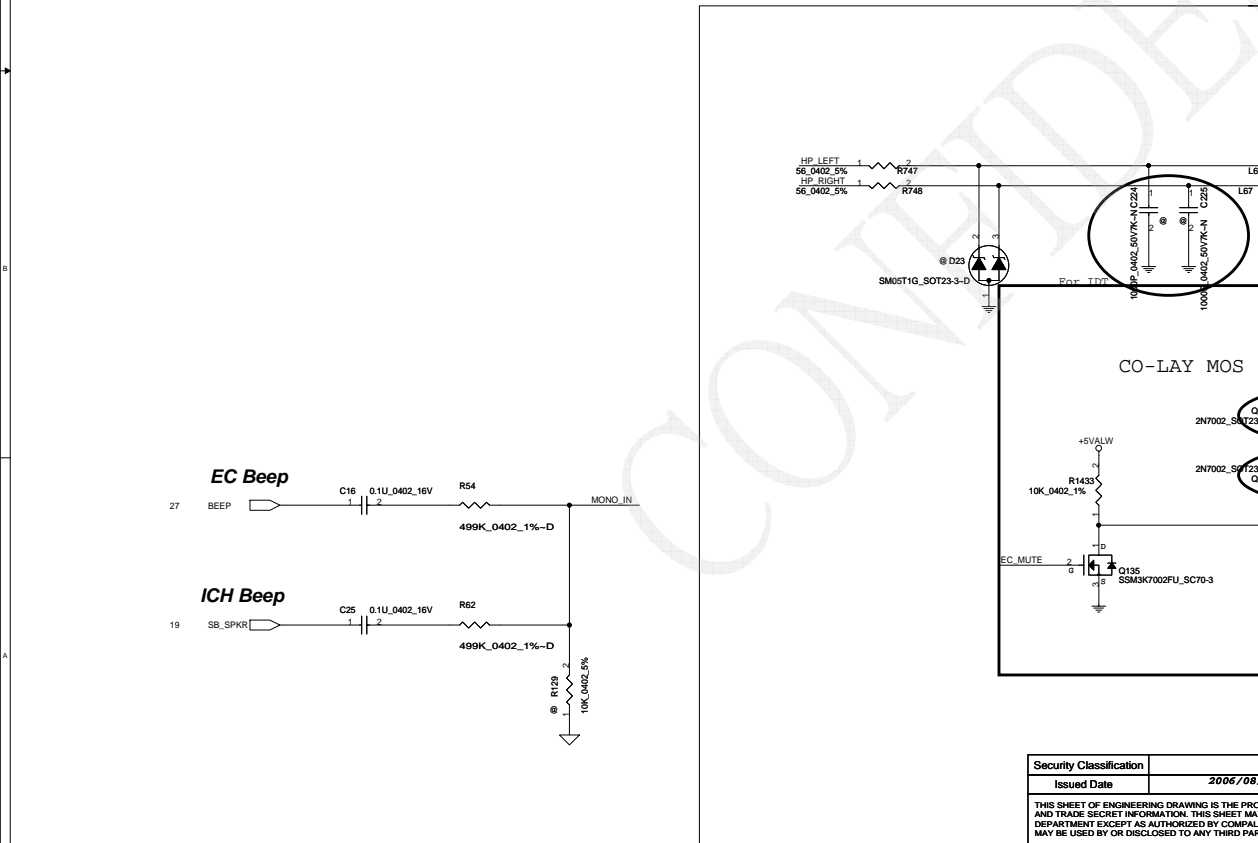
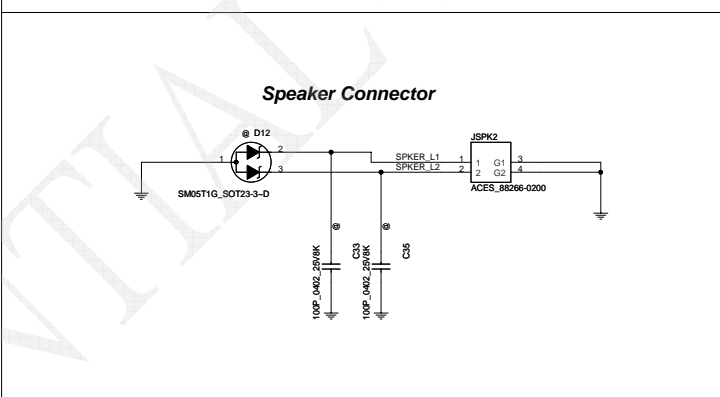
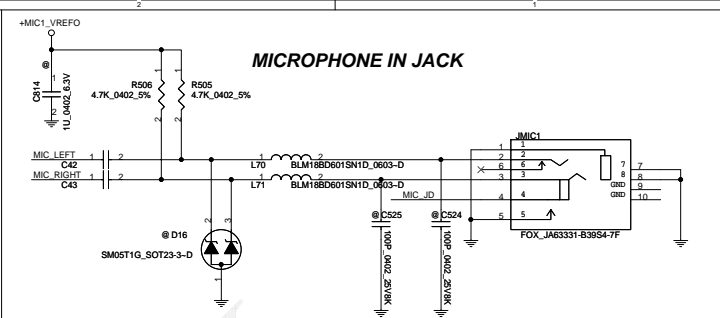
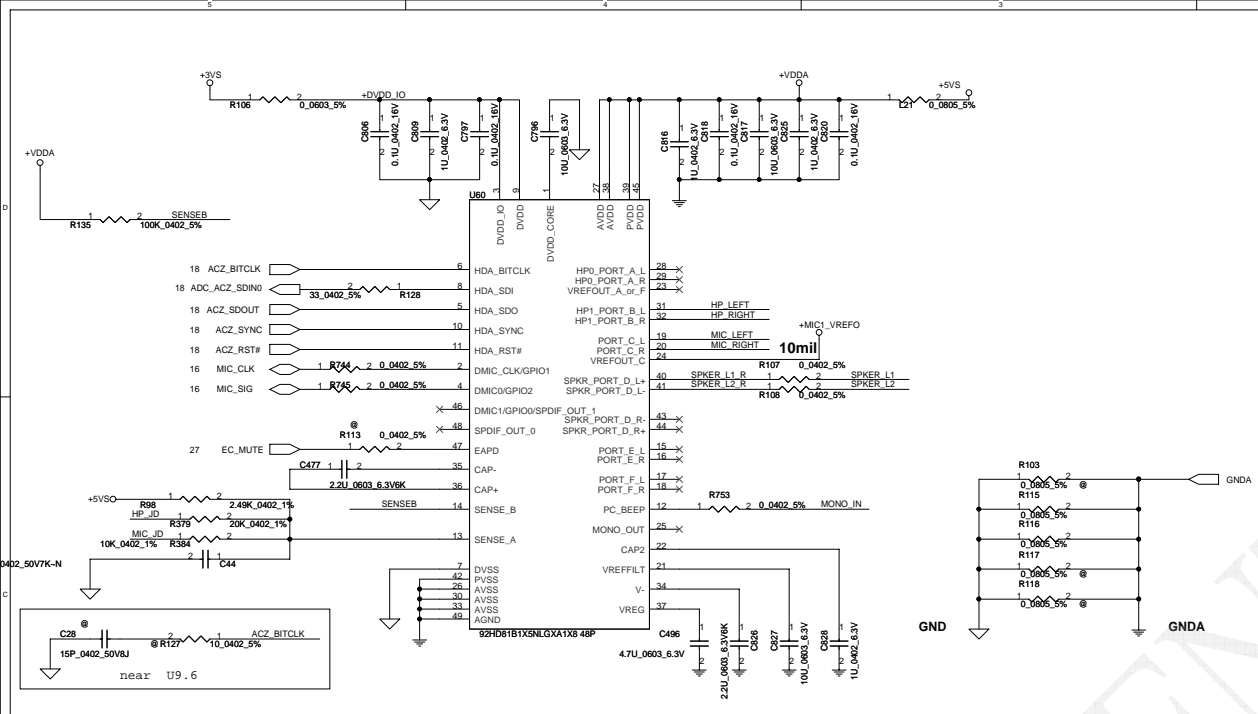
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Mini-Express Card---WLAN

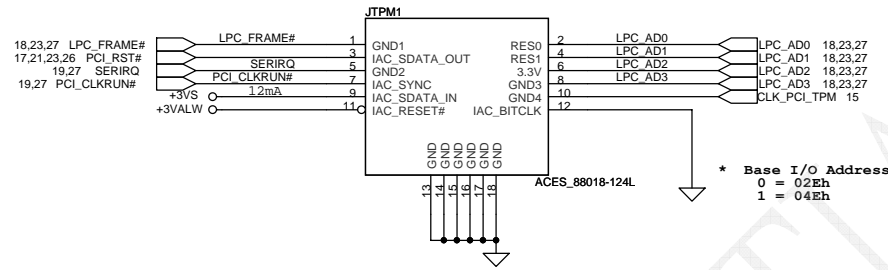


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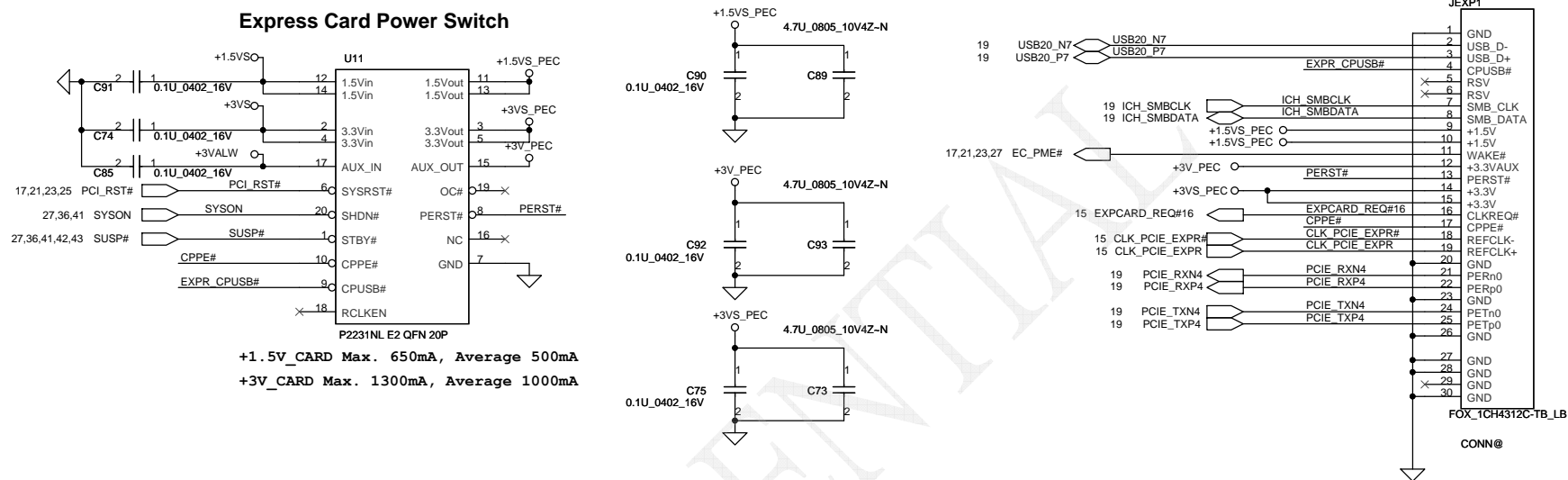
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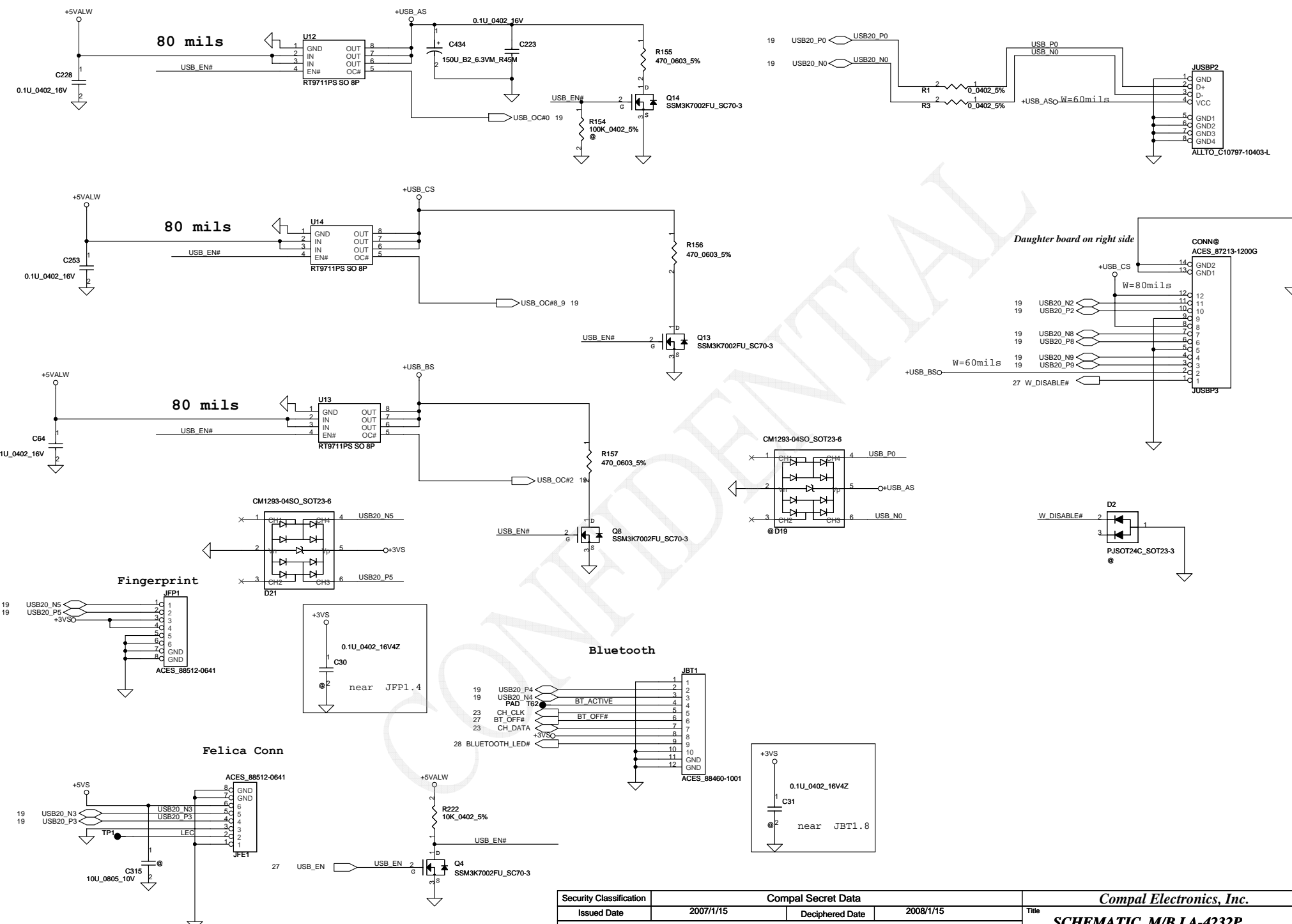
Express card



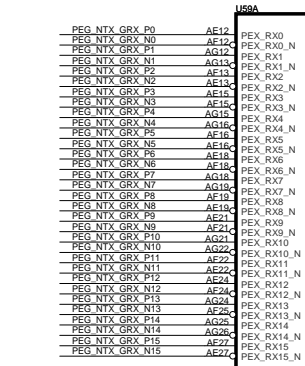
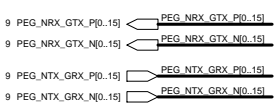
Express Card Power Switch

+1.5V_CARD Max. 650mA, Average 500mA
+3V_CARD Max. 1300mA, Average 1000mA

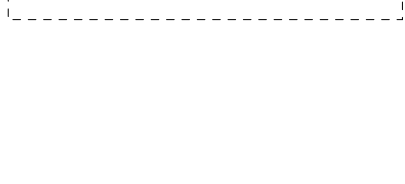
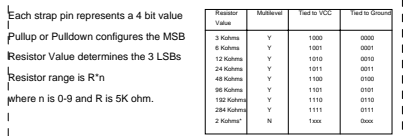
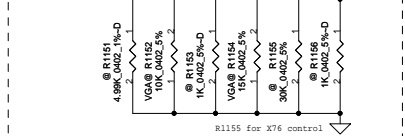
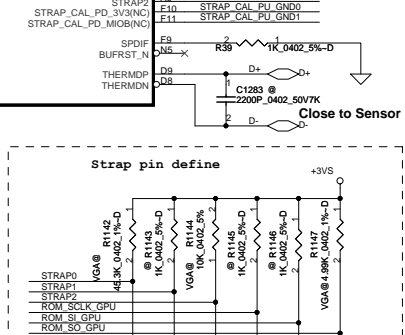
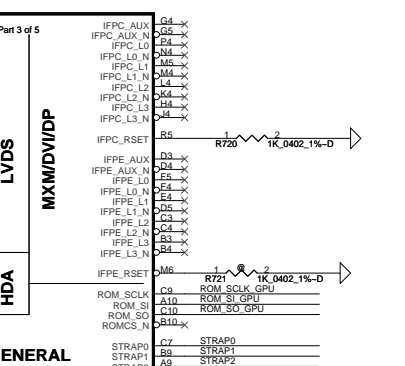
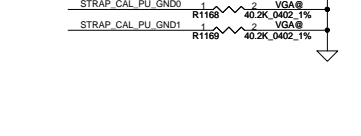
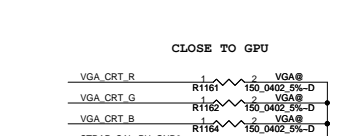
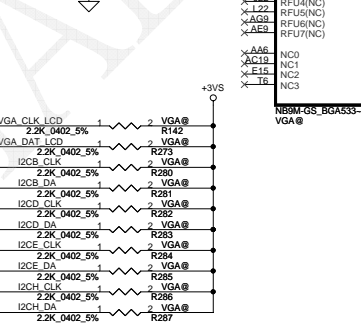
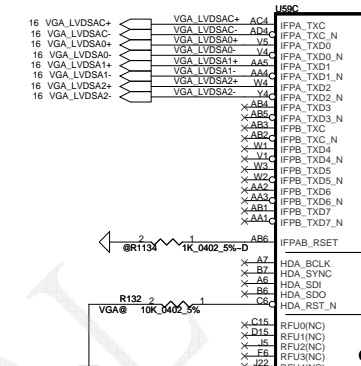
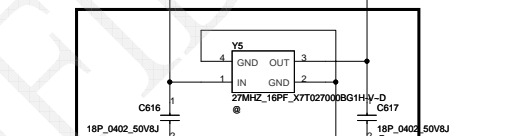
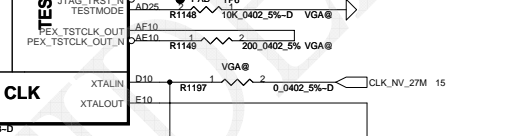
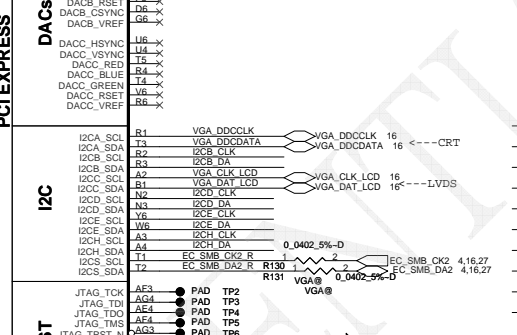
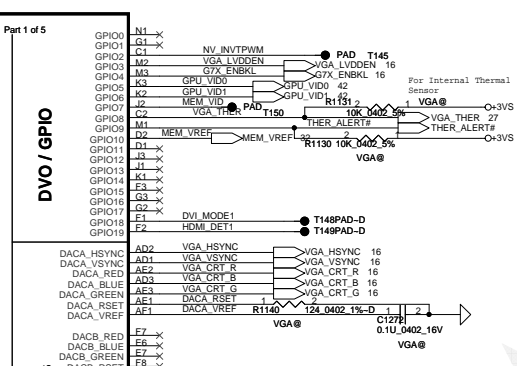
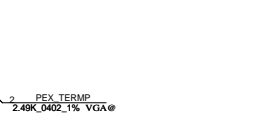
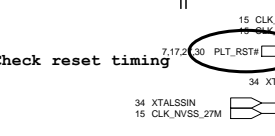
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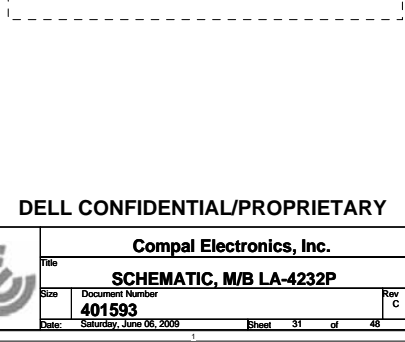
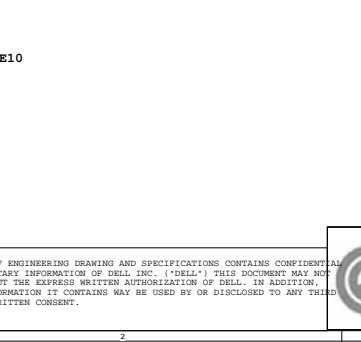
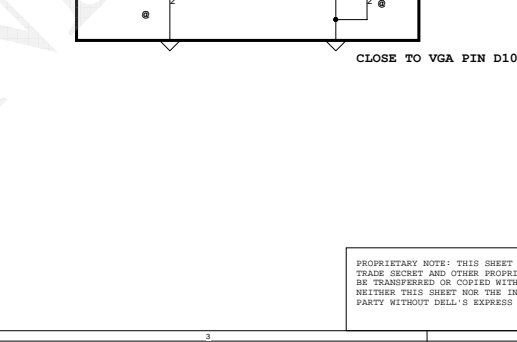
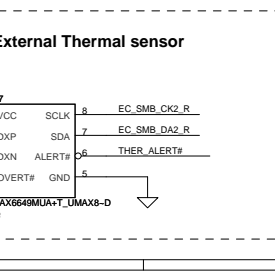


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Each strap pin represents a 4 bit value
Pullup or Pulldown configures the MSB
Resistor Value determines the 3 LSBs
Resistor range is R*n
where n is 0-9 and R is 5K ohm.

Resistor Value	Min/Max	Need to VCC	Need to Ground
3 KOhms	Y	1000	0000
4 KOhms	Y	1001	0001
5 KOhms	Y	1010	0010
6 KOhms	Y	1011	0011
7 KOhms	Y	1100	0100
8 KOhms	Y	1101	0101
9 KOhms	Y	1110	0110
10 KOhms	Y	1111	0111
2 KOhms	N	1xxx	0xxx



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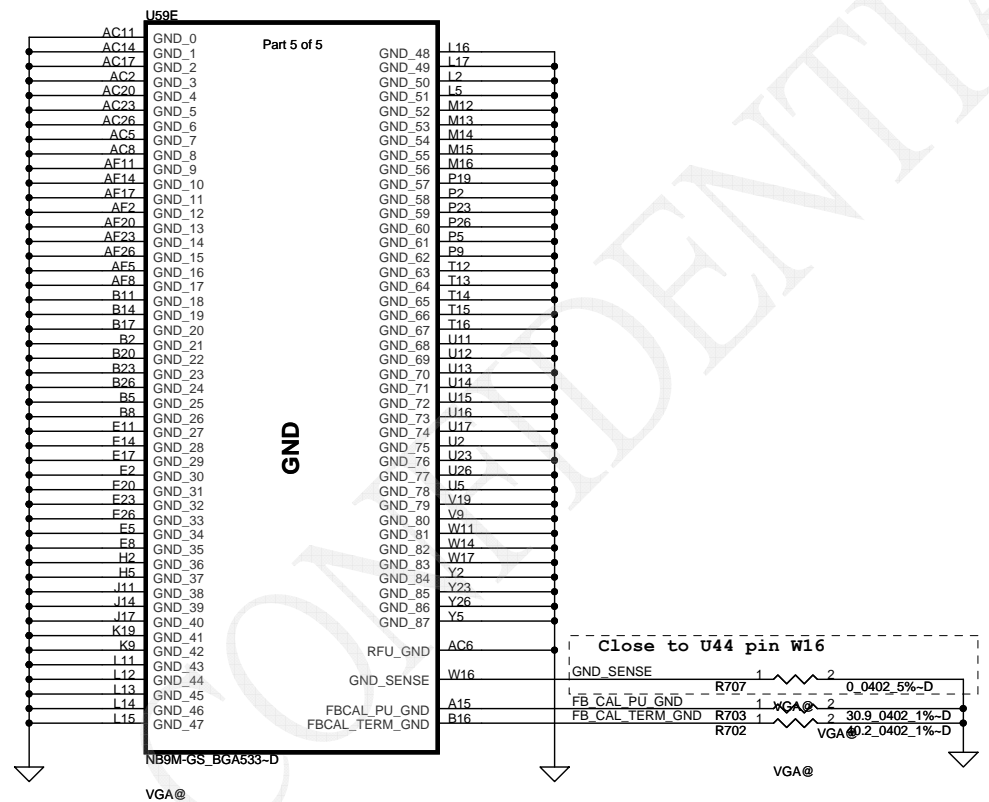
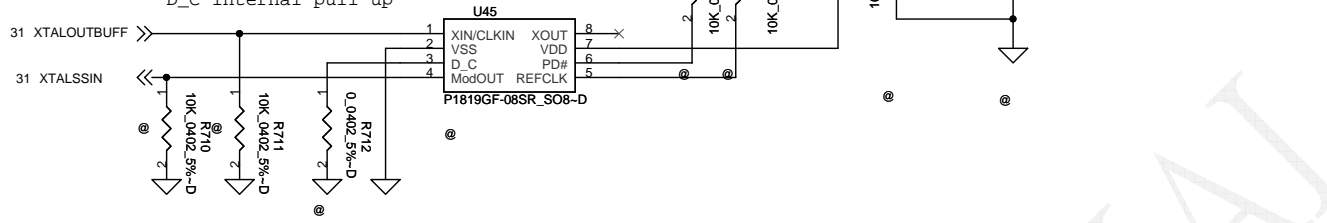
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 Date: Saturday, June 06, 2009
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	D_C
-1.75% (DOWN)	0
±0.875% (CENTER)	1

D_C Internal pull up



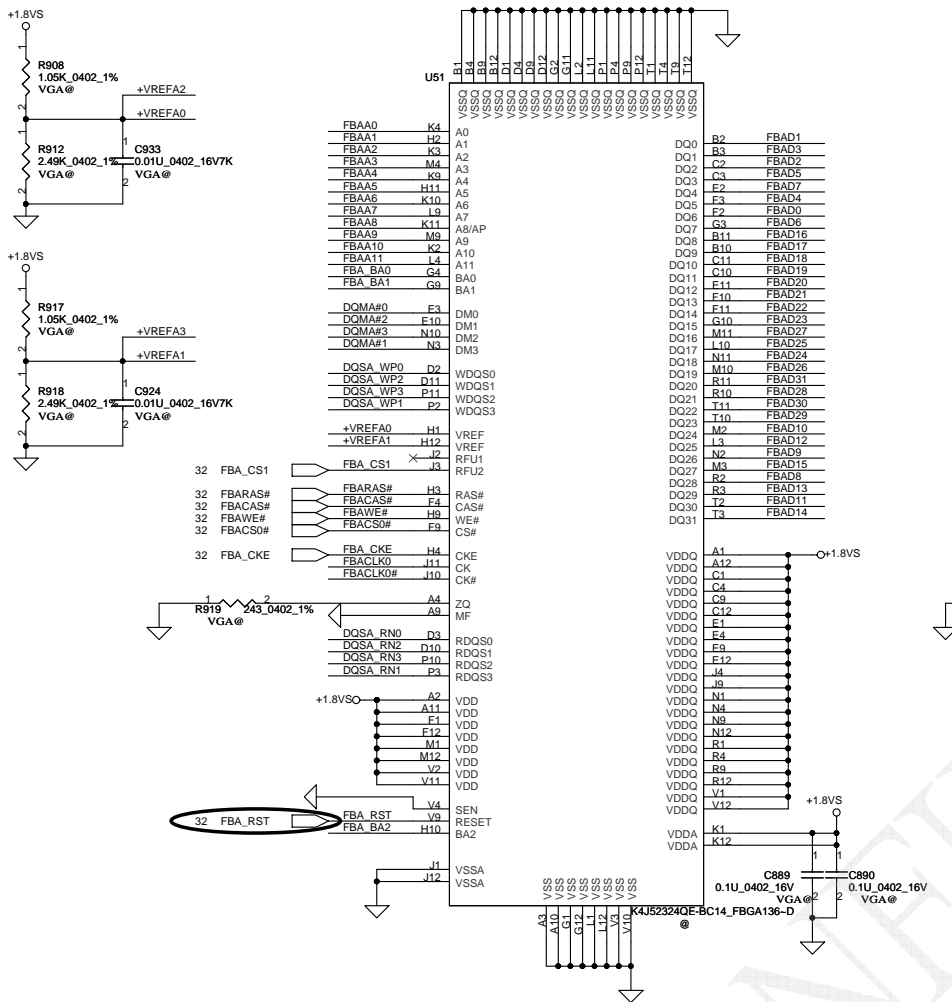
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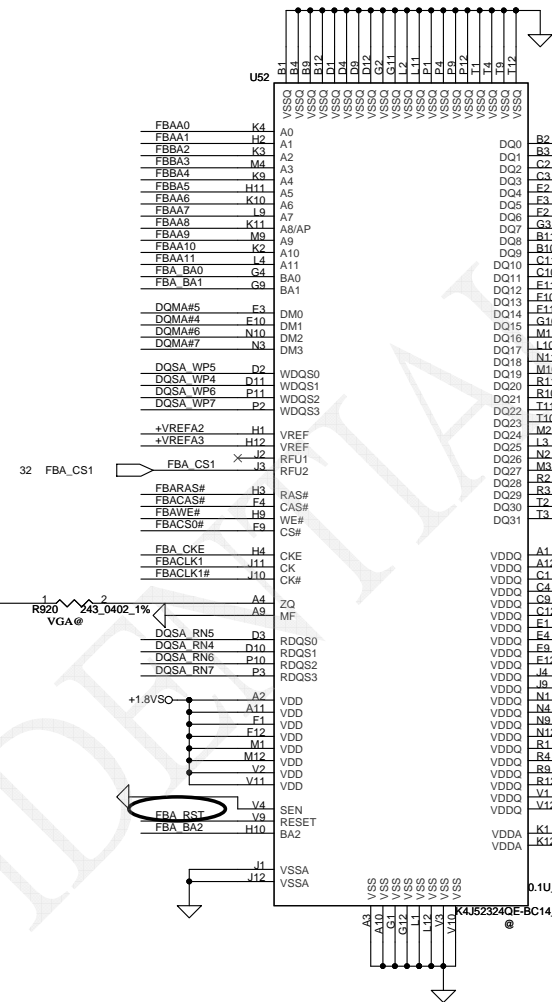
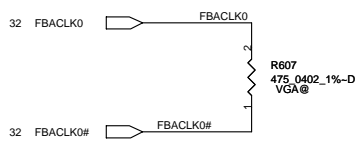
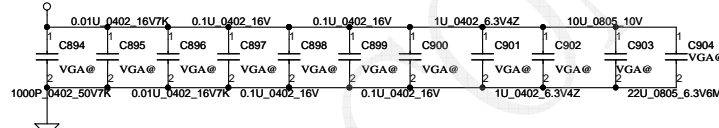
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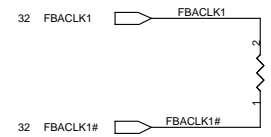
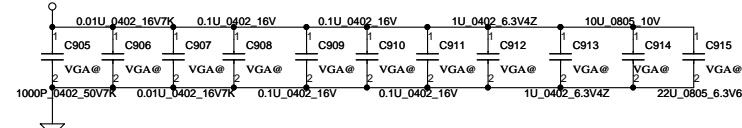
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GDDR3 BGA MEMORY

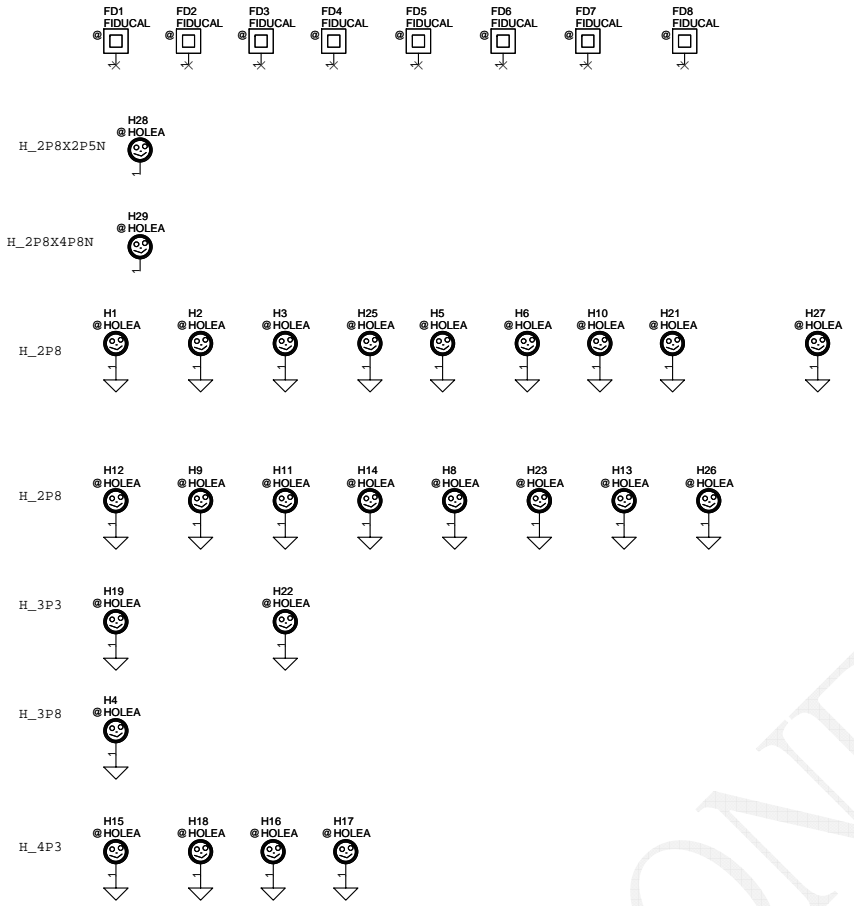


GDDR3 BGA MEMORY



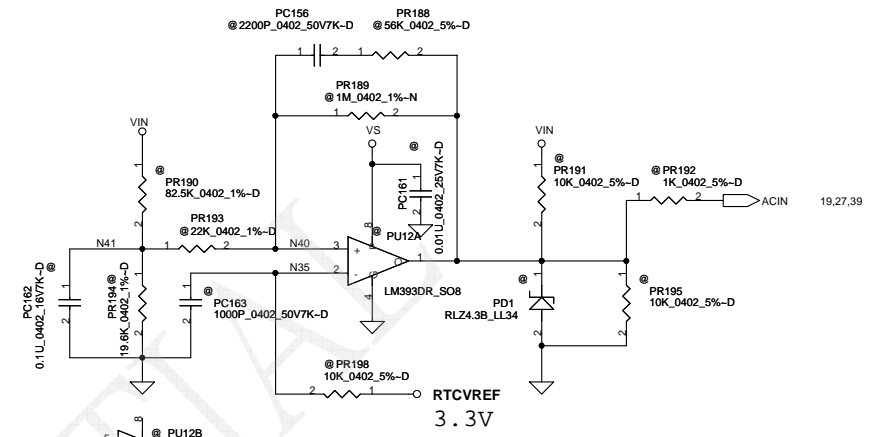
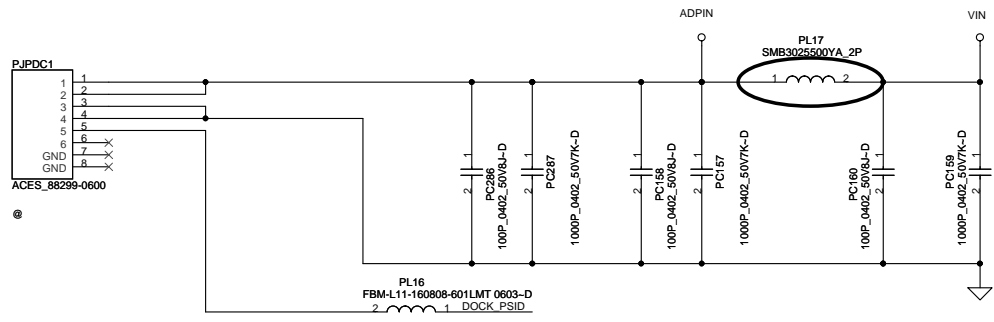
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- 32 DQMA#[0..7] DQMA#[0..7]
- 32 FBAA[0..11] FBAA[0..11]
- 32 FBAA[2..5] FBAA[2..5]
- 32 FBA_BA0 FBA_BA0
- 32 FBA_BA1 FBA_BA1
- 32 FBA_BA2 FBA_BA2

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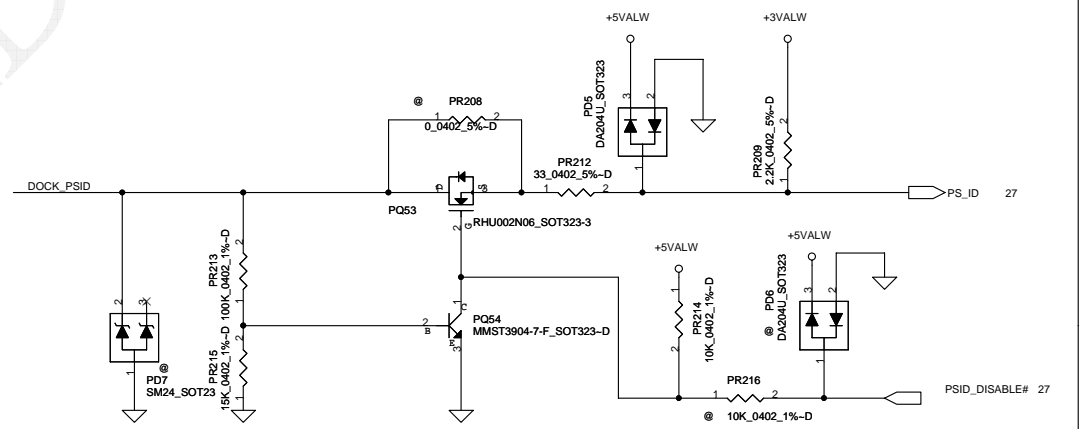
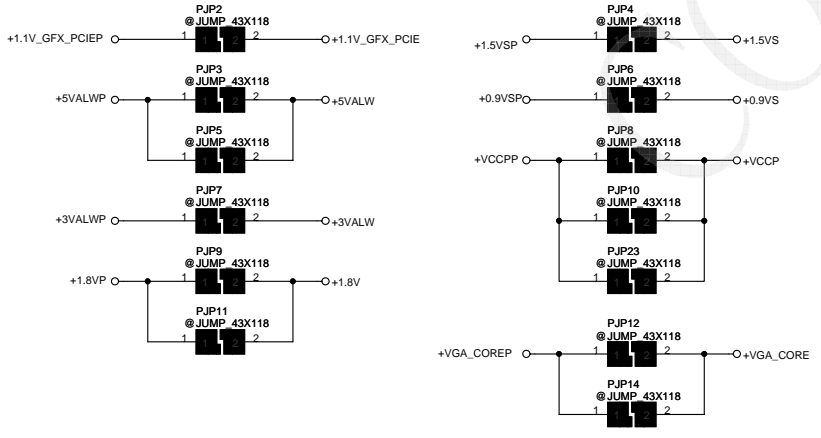
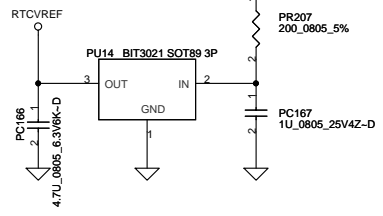
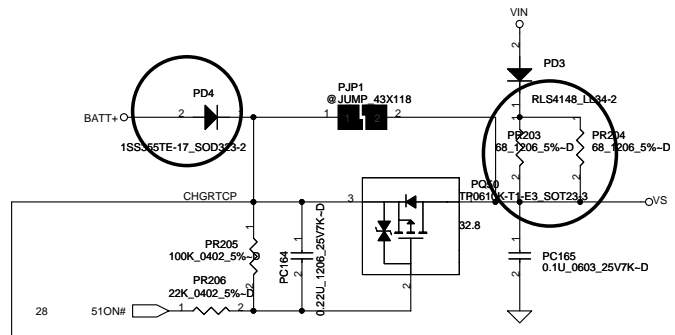


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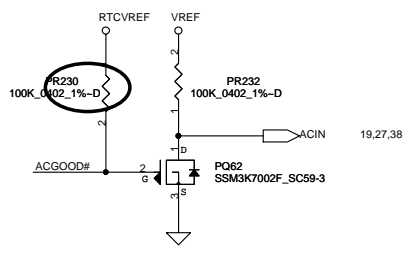
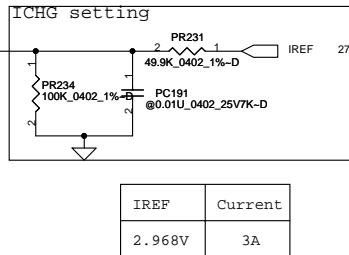
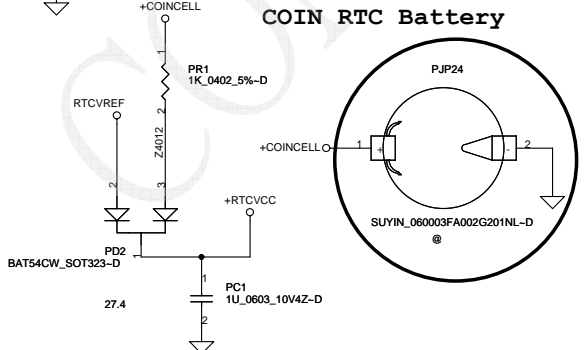
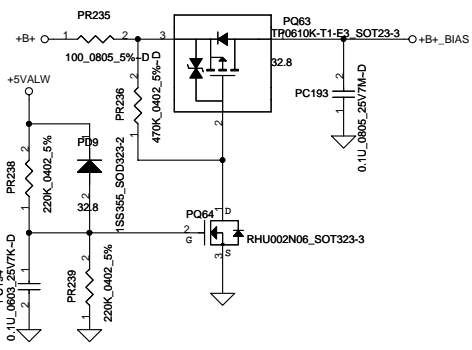
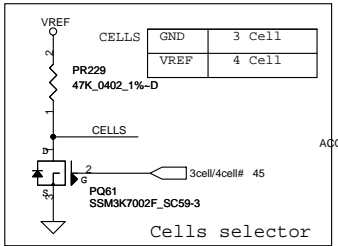


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H-->L	17.597	17.210	16.813

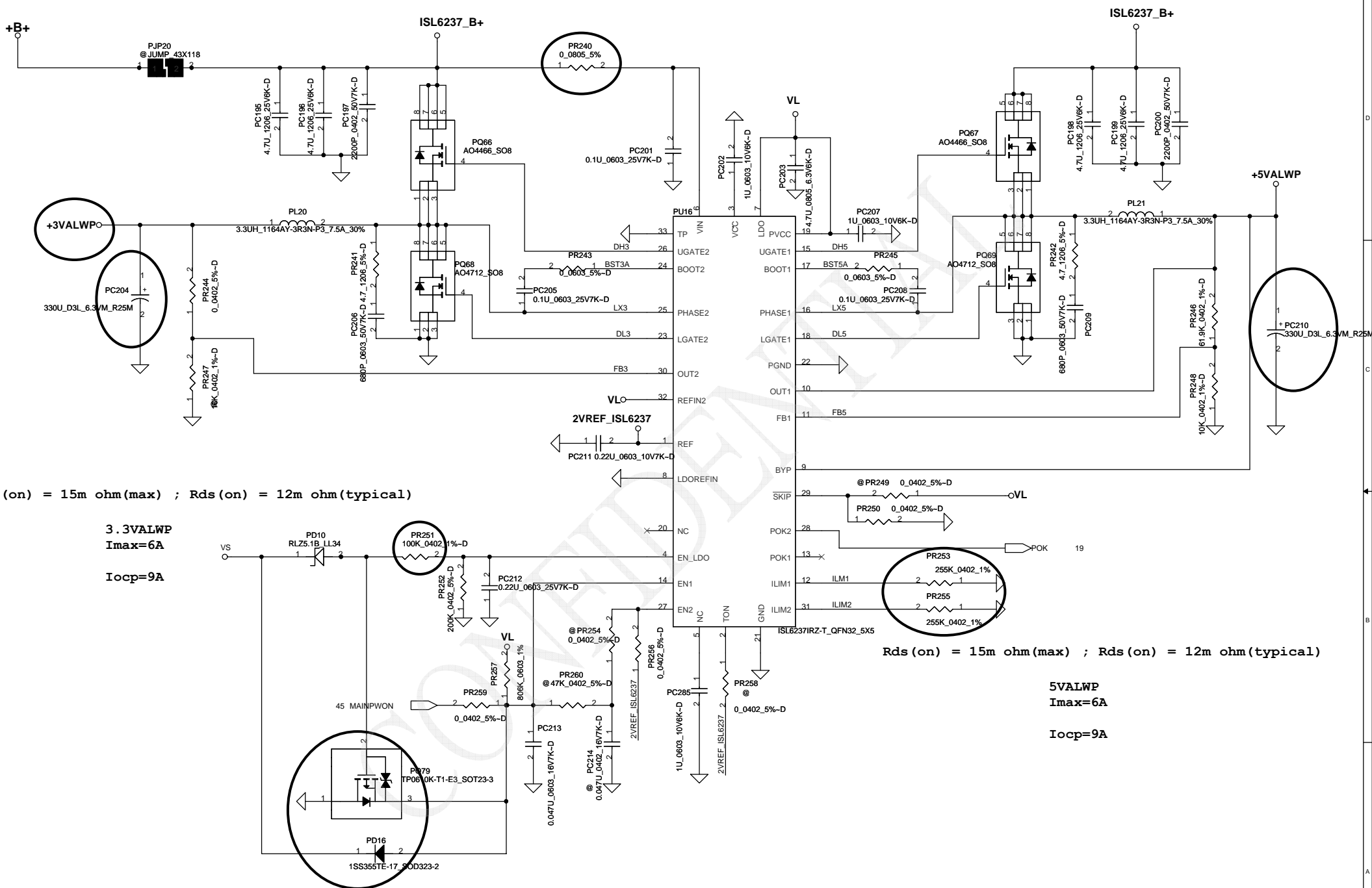


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90W adapter
 $I_{charge} = (V_{rsrset}/V_{vdac}) * (0.1/PR222) = 3.3A$
 $I_{adapter} = (V_{vacset}/V_{vdac}) * (0.1/PR217) = 3.1A$
 Input OVP : 22.3V
 Input UVP : 16.98V
 Fsw : 300KHz



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Rds(on) = 15m ohm(max) ; Rds(on) = 12m ohm(typical)

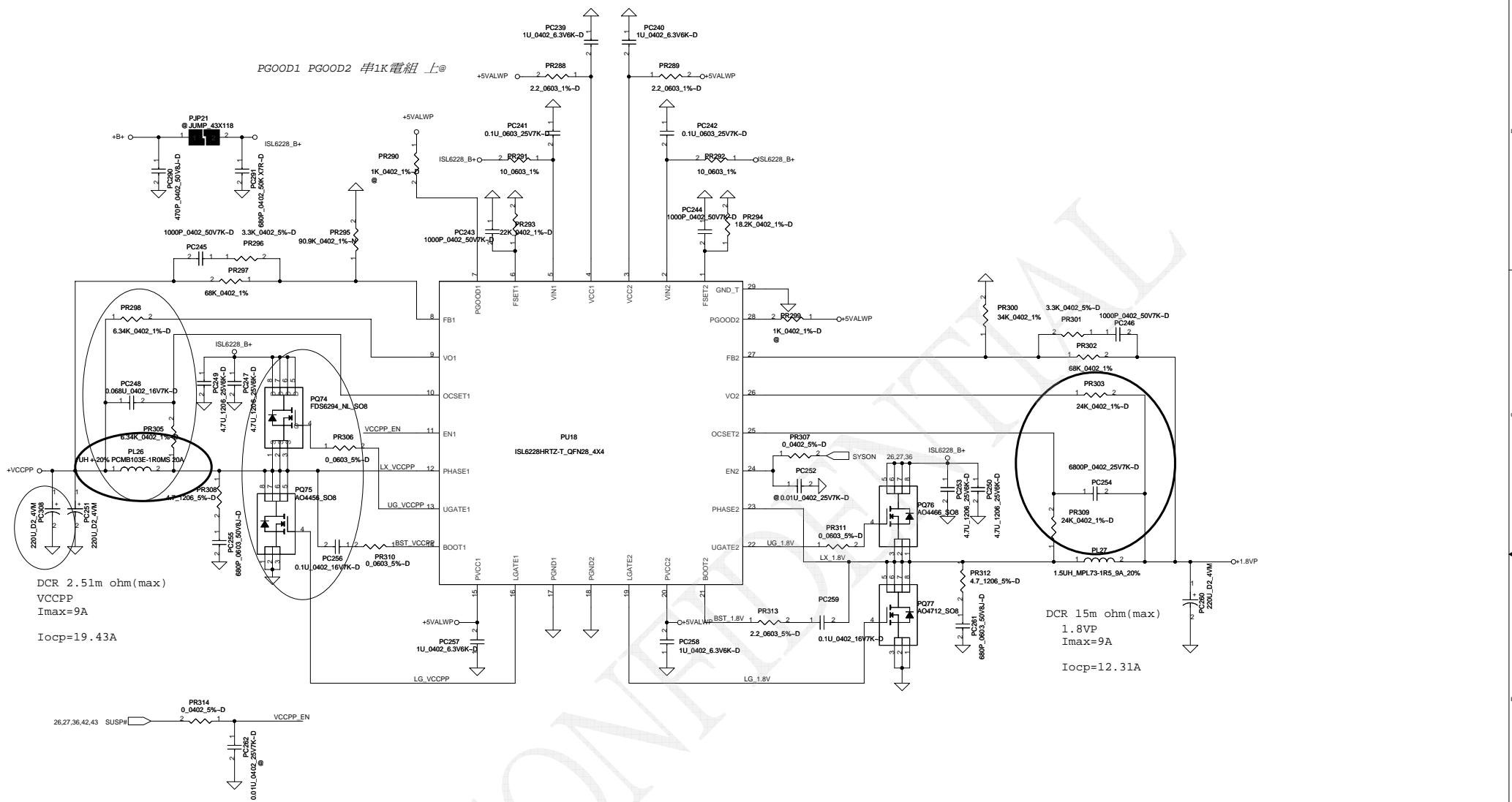
3.3VALWP
 I_{max}=6A
 I_{ocp}=9A

Rds(on) = 15m ohm(max) ; Rds(on) = 12m ohm(typical)

5VALWP
 I_{max}=6A
 I_{ocp}=9A

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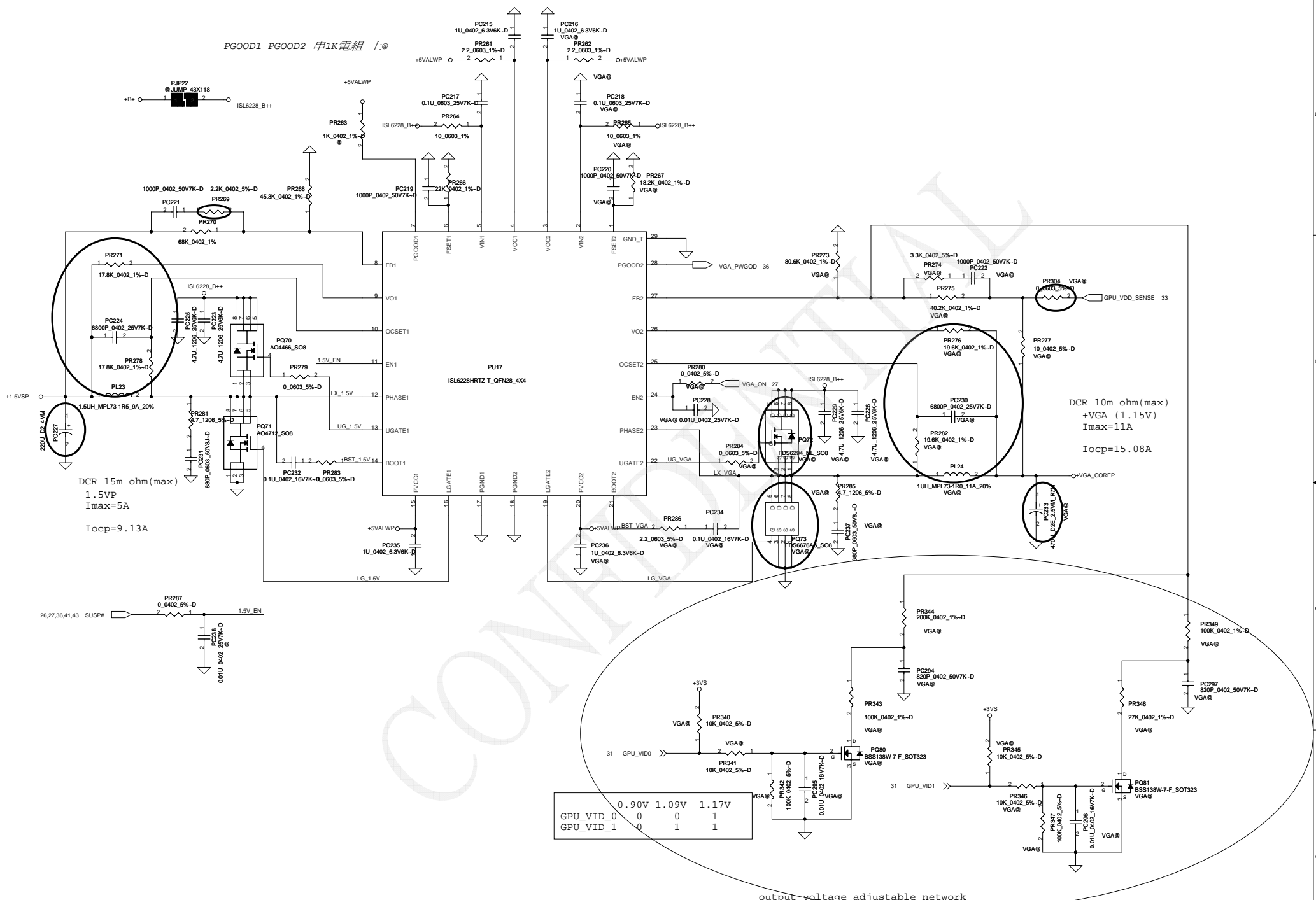


DCR 2.51m ohm(max)
 VCCPP
 I_{max}=9A
 I_{ocp}=19.43A

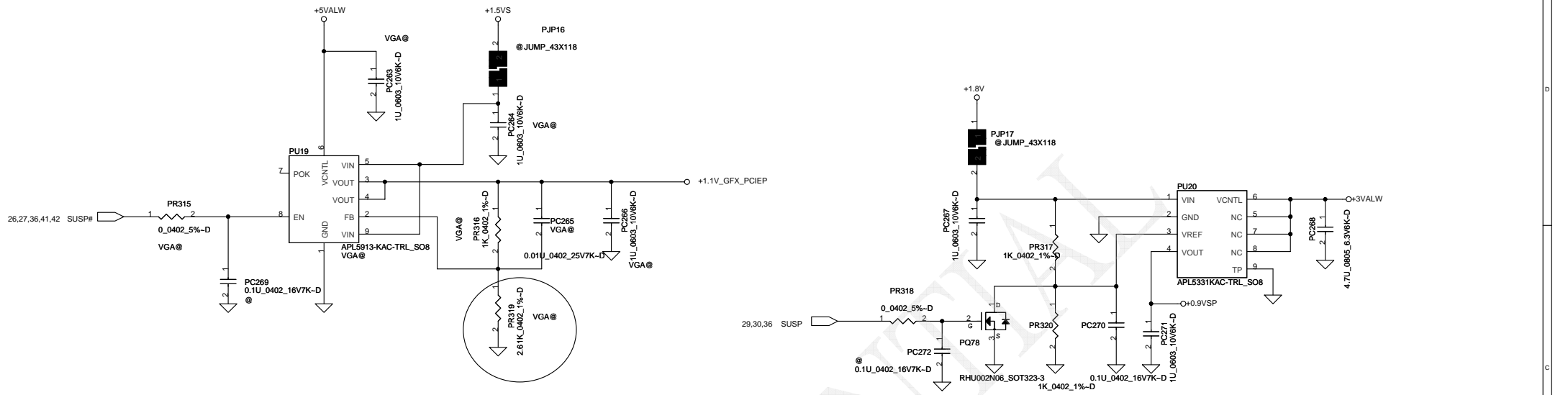
DCR 15m ohm(max)
 1.8VP
 I_{max}=9A
 I_{ocp}=12.31A

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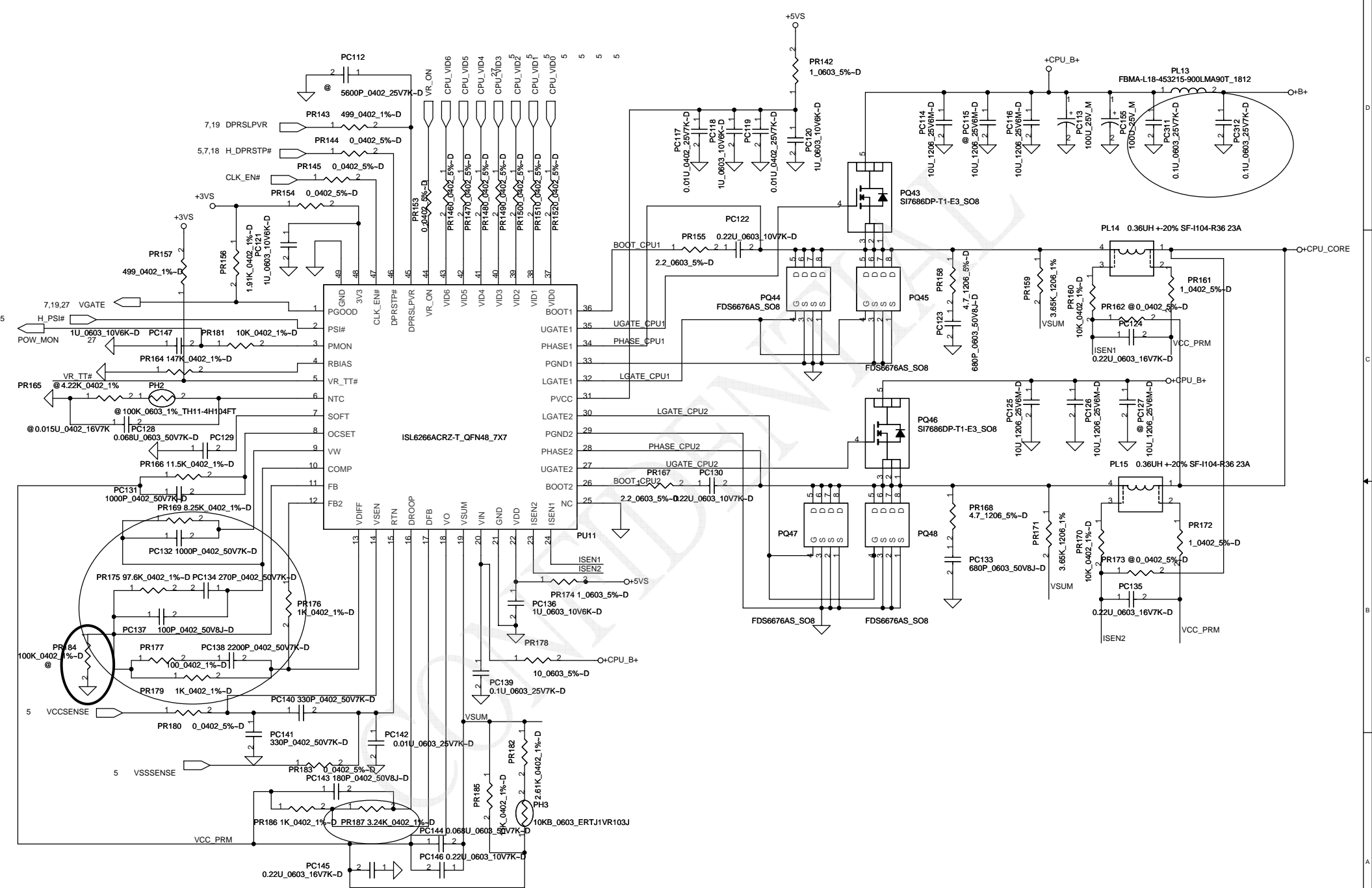


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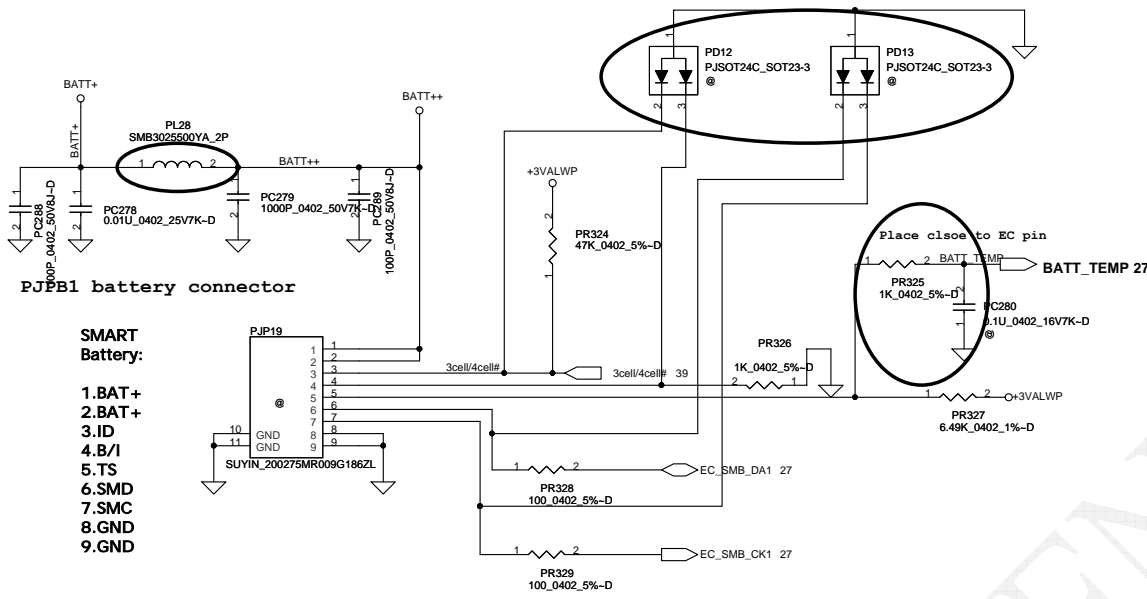
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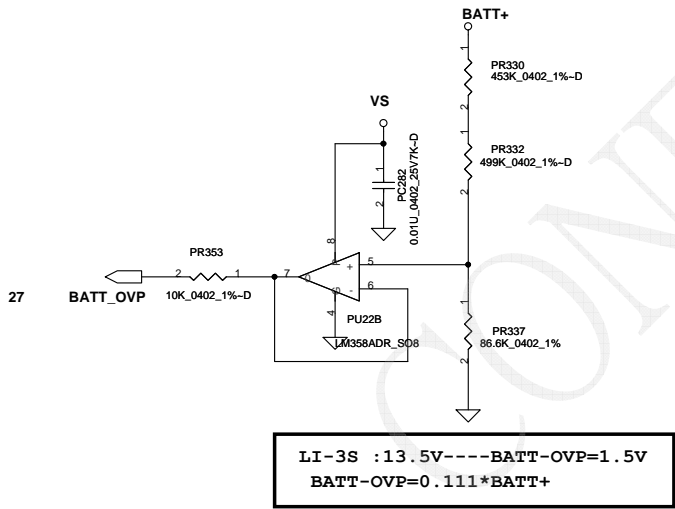


Battery Connect/OTP

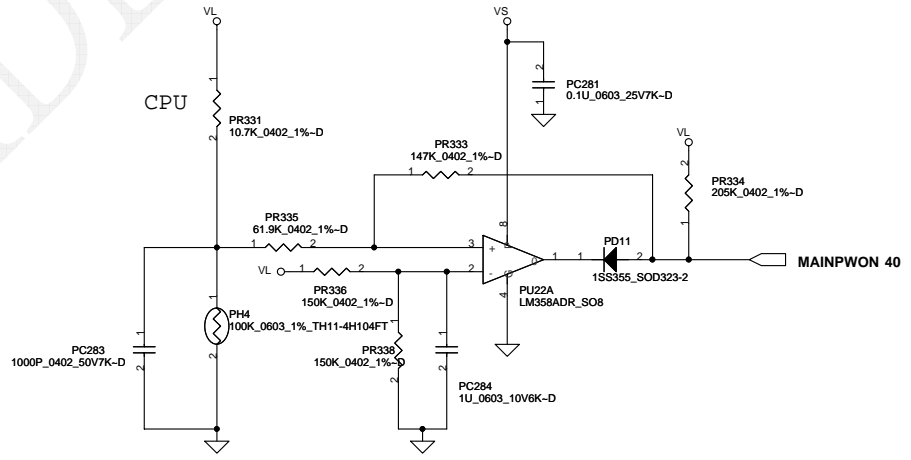
- SMART Battery:**
1. BATT+
 2. BATT+
 3. ID
 4. B/I
 5. TS
 6. SMD
 7. SMC
 8. GND
 9. GND

CPU

PH1 under CPU bottom side :
 CPU thermal protection at 90 +/-3 degree C
 Recovery at 50 +/-3 degree C



LI-3S : 13.5V --- BATT-OVP=1.5V
BATT-OVP=0.111*BATT+



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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	29	P29-EC KB926/REED SW/TPM1.2	07/10/30	compal	board rev update to 0.2	R231 change to 15K & R232 pop	0.2
2	40	P40-02129_Card Reader/1394	07/10/30	compal	CardBus vendor change	CardBus R5C833 change to 02129	0.2
3	29	P29-EC KB926/REED SW/TPM1.2	07/10/30	compal	Change pull up resistance	Change EC pin17,18 pull up to 4.7Kohm	0.2
4	29	P29-EC KB926/REED SW/TPM1.2	07/10/30	compal	Need pull up	NET MIC_DIAG pull up R to 10Kohm 3VS	0.2
5	13,14	DDR2 SODIMM-I,II Socket	07/10/30	compal	Change Capacitance	Change C84,C189 to SGA00002680 330U	0.2
6	29	P29-EC KB926/REED SW/TPM1.2	07/10/30	compal	EC update rev	EC change to 926C	0.2
7	28	P28-Express card	07/10/30	compal	Express card can't detect	POWER IC(U11) ADD PIN10 CPUSB# PIN9 EXPR_CPUSB#S	0.2
8	32	P32-USB/ Bluetooth/ FP/ Felica	07/10/30	compal	Bluetooth can't detect	BLUETOOTH CONN USB+- change	0.2
9	42	P42-Screws	07/10/30	compal	FIDUCAL no enough	ADD FIDUCAL*4	0.2
10	41	P41-DC/DC Interface	07/10/30	compal	Need pull down	SYSON pull down 10K ohm	0.2
11	41	P41-DC/DC Interface	07/11/12	compal	USB can't detect	SUSP change to 5VALW(Q32)	0.2
12	06	P06-Merom(3/3)-GND/Bypass	07/11/12	compal	Change CPU High Frequency Decoupling Capacitance	C195 change to C1150-C1181	0.2
13	41	P41-DC/DC Interface	07/11/13	compal	+1.8VS Discharge error	+1.8VS Discharge circuit Q65 net change to VGA_PWGOD#	0.2
14	41	P41-DC/DC Interface	07/11/16	compal	Delete	Remove SIM card connector	0.2
15	42	P42-Screws	07/11/16	compal	Change Holea size	Change Holea size 2.5 to 2.8, change 3.5 to 3.8	0.2
16	31	P31-PWR_OK/ BTN/ KB / TouchPad	07/11/21	compal	Change Touch PAD/B connector	Touch PAD/B connector change net	0.2
17	15	P15-CRT Conn.& LCD Conn.	07/11/21	compal	Add LCD control pin	Add LCD control pin LCD_CBL_DET# & LCD_TST & LCD_VCC_TEST_EN	0.2
18	20	P20-ICH9(4/4)_POWER&GND	08/04/22	compal	+5VS & +3VS have leakage	Change VCCCL3[1] [2] & VCCLAN3_3[1] [2] power source to +LAN_IO	
19	20	P09-Cantiga(3/6)-VGA/LVDS/TV	08/04/22	compal	Can't boot to OS	Add BOM Structure @	

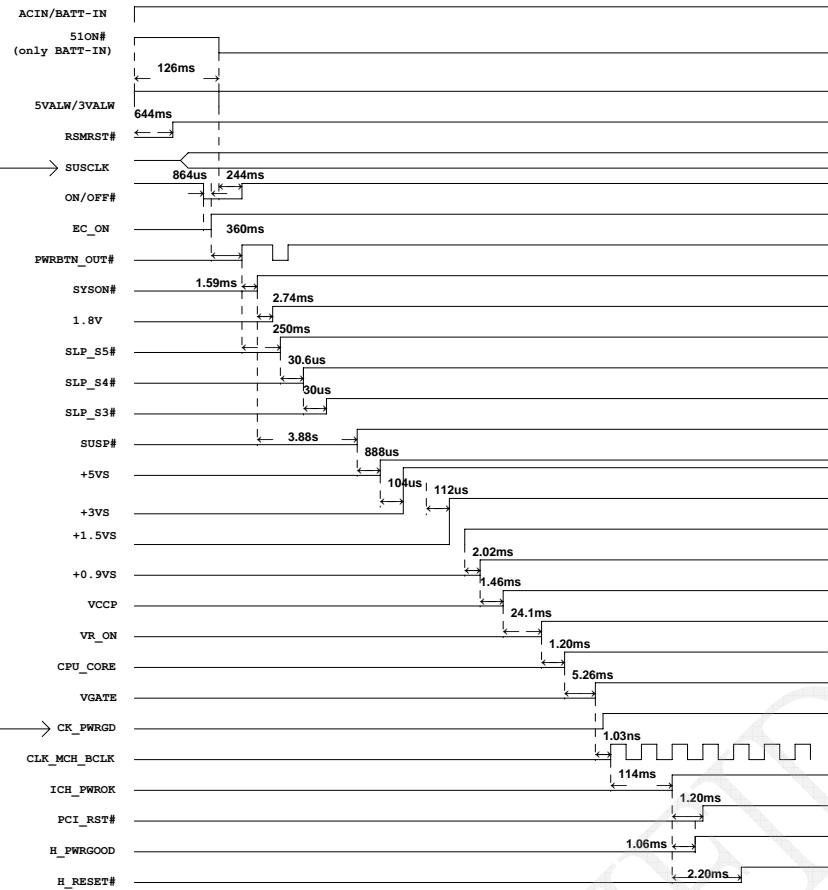
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	41	1.8VP/+VCCPP	08/10/22	COMPAL	adjust +VCCP OCP set	Change PC248 from 0.033u to 0.068u	0.2
2	42	1.5VSP/+VGA_CORE	08/10/22	COMPAL	ripple voltage fail	Change PC227 from SF22001M300 to SGA20221150	0.2
3	42	1.5VSP/+VGA_CORE	08/10/22	COMPAL	convenient test	Add PR304	0.2
4	44	CPU_CORE	08/10/22	COMPAL	load line fail	Change PR187 from 2.21K to 3.24K	0.2
5	38	DCIN / Precharge	08/10/22	COMPAL	modify MLCC part number	change part number N0 to 8L	0.2
6	39	Charger	08/10/22	COMPAL	modify MLCC part number	change part number N0 to 8L	0.2
7	40	+3VALWP/+5VALWP	08/10/22	COMPAL	modify MLCC part number	change part number N0 to 8L	0.2
8	41	1.8VP/+VCCPP	08/10/22	COMPAL	modify MLCC part number	change part number N0 to 8L	0.2
9	42	1.5VSP/+VGA_CORE	08/10/22	COMPAL	modify MLCC part number	change part number N0 to 8L	0.2
10	43	+0.9VSP/+1.1V_GFX_PCIEP	08/10/22	COMPAL	modify MLCC part number	change part number N0 to 8L	0.2
11	44	CPU_CORE	08/10/22	COMPAL	modify MLCC part number	change part number N0 to 8L	0.2
12	45	BATTERY CONN	08/10/22	COMPAL	modify MLCC part number	change part number N0 to 8L	0.2
13	40	+3VALWP/+5VALWP	08/10/24	COMPAL	boost choke current rating	change PL20 PL21 from SH000006380 to SH00000AY00	0.2
14	45	BATTERY CONN	08/10/30	COMPAL	delete diode for EMD request	del PD14 PD15	0.2
15	45	BATTERY CONN	08/10/30	COMPAL	change diode for EMD request	change PD12 PD13 from SC1A204U00L to SCA00000E00	0.2
16	39	Charger	08/10/31	COMPAL	design modify	add PR372 PR373	0.2
17	41	1.8VP/+VCCPP	08/11/03	COMPAL	dynamic fail	change PC233 from SGA20221150 to SGA00001U80	0.2
18	44	CPU_CORE	08/12/08	COMPAL	cost down	change PU11 from SA00001HU80 to SA000031W00 and interrelated components	0.3
19	38	DCIN / Precharge	08/12/08	COMPAL	common circuit design modify	change PR203 from 33 to 68 and add PR204 to 68	0.3
20	39	Charger	08/12/08	COMPAL	vendor FAE suggest	change PR272 PR339 from 1 to 3.3	0.3
21	38	DCIN / Precharge	08/12/08	COMPAL	design modify	change PL17 from SM010018880 to SM010008E10	0.3
22	45	BATTERY CONN	08/12/08	COMPAL	design modify	change PL28 from SM010018210 to SM010008E10	0.3
23	39	Charger	08/12/15	COMPAL	change component for EMD request	change PJP15 to PL19 SM010016410	0.3
24	39	Charger	08/12/15	COMPAL	add capacitor for EMD request	add PC274 0.1u	0.3
25	42	1.5VSP/+VGA_CORE	09/01/19	COMPAL	adjust VGA_CORE OCP set	change PQ72 from SB00000CG00 to SB562940080	0.4
26						change PQ73 from SB00000AJ00 to SB000003W00	0.4
27						change PL24 from SH000008700 to SH000005400	0.4
28						change PR276 PR282 from 24K to 19.6K	0.4
29						change PC230 from 0.022u to 6800p	0.4
30					consumption adjust	change PR269 from 3.3K to 2.2K	0.4
31	44	CPU_CORE	09/01/19	COMPAL	vendor FAE suggest	add PC141 330p	0.4
32	45	BATTERY CONN	09/02/18	COMPAL	delete diode for ESD request	del PD12 PD13	0.4

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KAL80 POWER UP SEQUENCE



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