

IM3 (Jolie) Discrete 256M & UMA Block Diagram VER : 3A

POWER

AC/BATT CONNECTOR PG 55

BATT CHARGER PG 48

HybridSLI POWER

VGA Core
+1.1V_GFX PG 53

REGULATOR For GDDR3
+1.8V_RUN PG 50

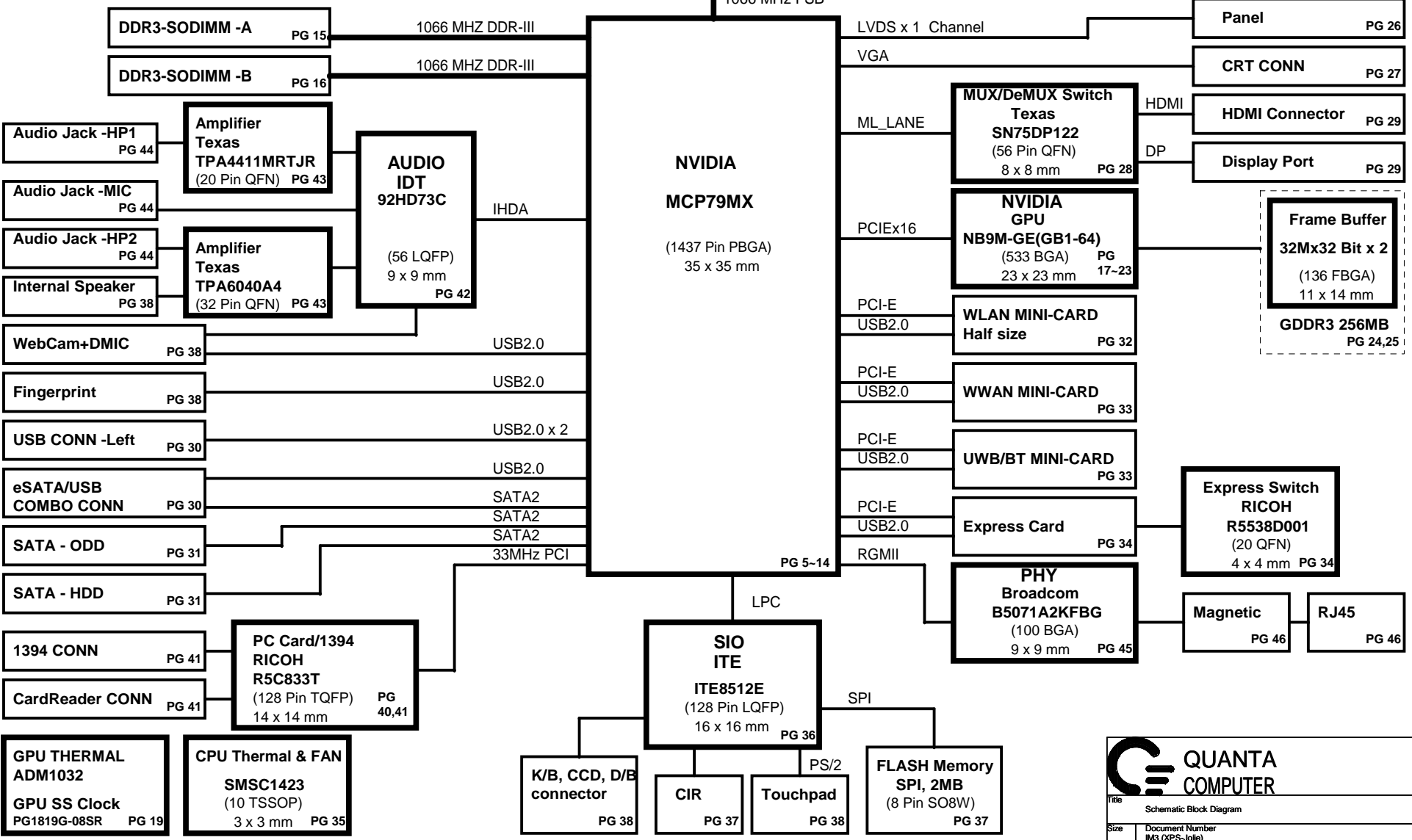
HybridSLI SW
+3.3V_NB9X/+1.8V_FBVDDQ/
+1.1V GFX_PCIE PG 23

Dual Core CPU Intel Penryn (25W)

(478 Micro-FCPGA)
35 x 35 mm PG 3,4

SYSTEM POWER

MCP VR +MCP_CORE PG 50	CPU VR +VCC_CORE/ +1.05V_VCCP PG 49,54	
REGULATOR For DDR3 +1.5V_DDR/ +0.75V_DDR_VTT PG 51	REGULATOR +3.3V_ALW/+5V_SRC/ +15V_ALW PG 52	
RUN/SUS POWER SW +5V/+3.3V/+1.5V_RUN +3.3V_SUS PG 56	LDO +1.1V_SUS PG 53	LDO +1.1V_RUN PG 51




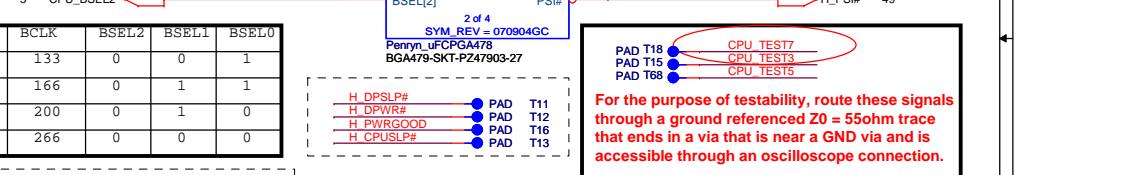
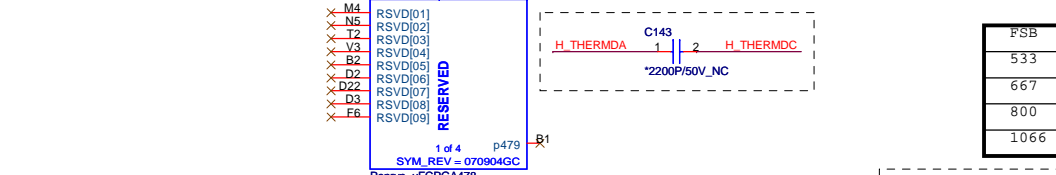
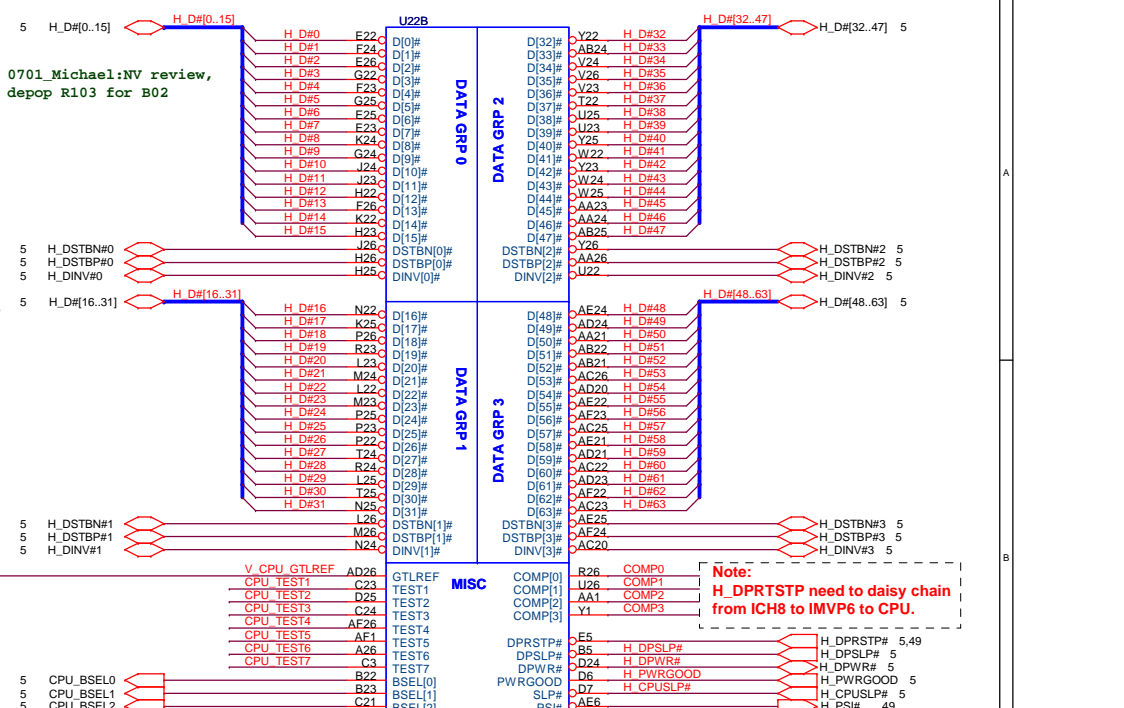
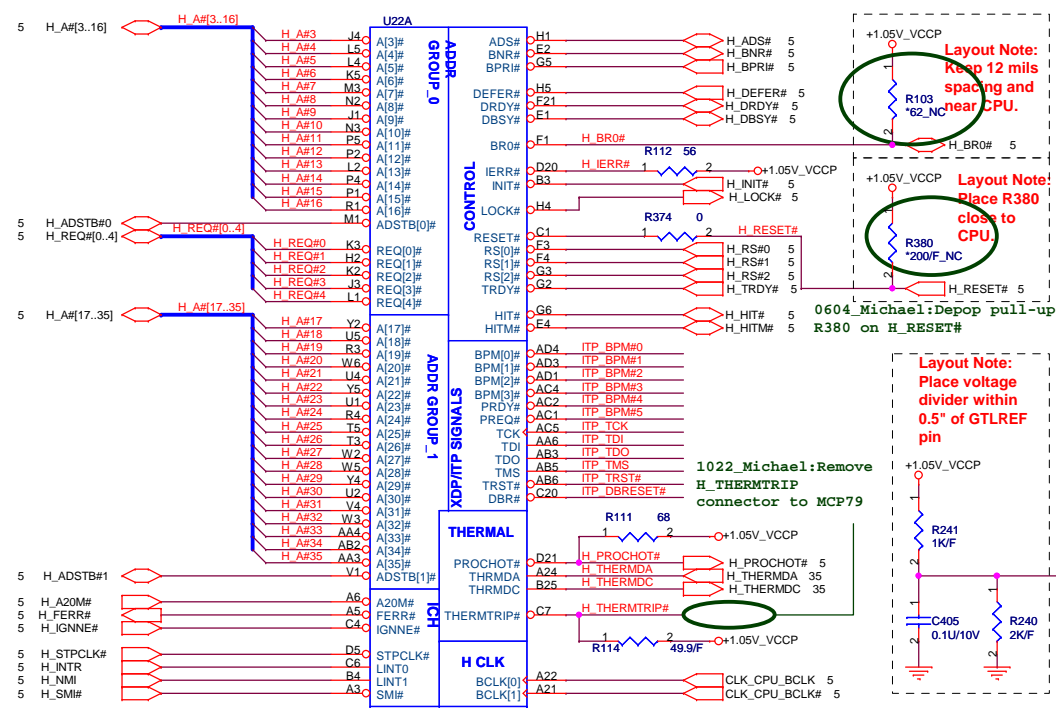
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27	CRT CONN
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55	DCIN,Batt
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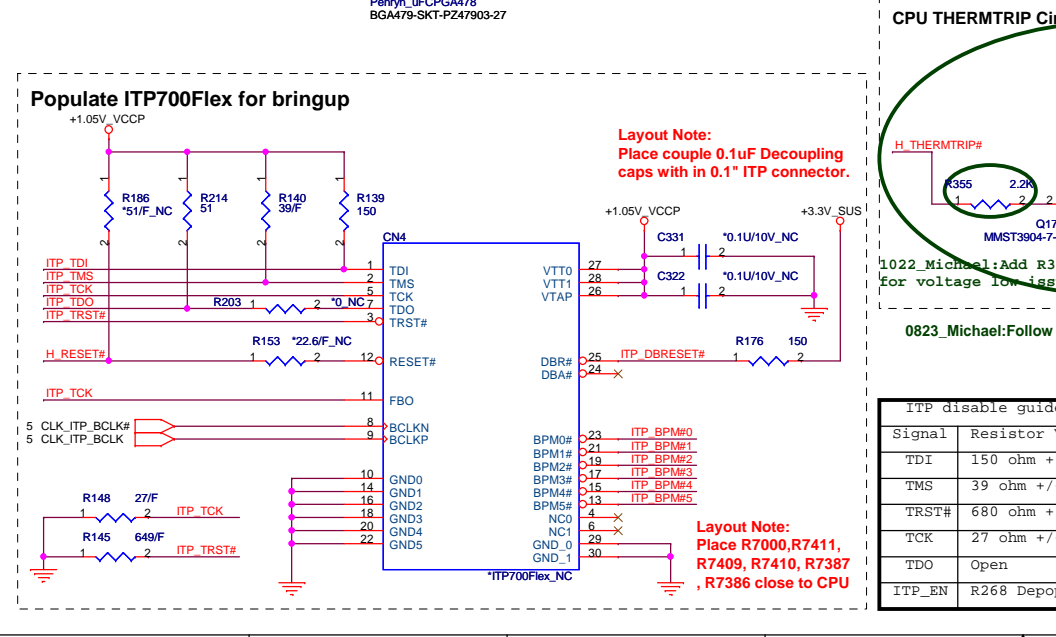
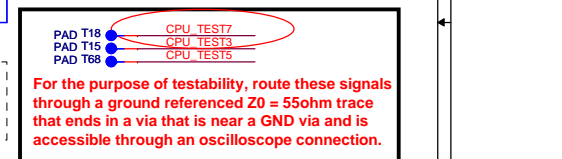
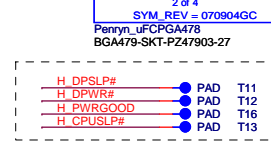
Power States

Power Rail	Control Signal	S0	S3	S4	S5	G3
+PWR_SRC	N/A	V	V	V	V	
+0.75V_DDR_VTT	RUN_ON	V				
+1.05V_VCCP	CPUVDD_EN	V				
+1.1V_GFX	+3.3V_NB9X	V				
+1.1V_GFX_PCIE	MXM_PWR_EN	V				
+1.1V_RMGT	SLP_RMGT#	V	V			
+1.1V_RUN	RUN_ON	V				
+1.1V_SUS	+3.3V_SUS	V	V			
+1.5V_RUN	RUN_ON	V				
+1.5V_DDR	SIO_SLP_S5#	V	V			
+1.8V_FBDDQ	NB9_CORE_PWRGD	V				
+1.8V_RUN	RUN_ON	V				
+15V_ALW	+5V_ALW	V	V			
+3.3V_ALW	+5V_ALW2	V	V	V	V	
+3.3V_NB9X	MXM_PWR_EN	V				
+3.3V_RMGT	SLP_RMGT#	V	V			
+3.3V_RUN	RUN_ON	V				
+3.3V_SUS	SUS_ON	V	V			
+5V_ALW	5V_ALW_ON	V	V			
+5V_ALW2	+PWR_SRC	V	V	V	V	
+5V_HDD	HDCC_EN	V				
+5V_MOD	MODC_EN	V				
+5V_RUN	RUN_ON	V				
+GFX_PWR_SRC	RUN_ON	V				
+LCDVCC	EN_LCDVCC	V				
+MCP_CORE	RUN_ON	V				
+NB9_CORE	+3.3V_NB9X	V				
+RTC_CELL	N/A	V	V	V	V	V
+VCC_CORE	1.05V_VCCP_PWRGD	V				
+USB_RIGHT_PWR	USB_SIDE_EN#	V	V			
+USB_LEFT_PWR	USB_BACK_EN#	V	V			

		
QUANTA COMPUTER		
Title Index & Power Status		
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FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1066	266	0	0	0



0823_Michael:Follow RM2 to change CPU THERMTRIP circuit

Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the ITP
TMS	39 ohm +/- 5%	VTT	Within 2.0" of the ITP
TRST#	680 ohm +/- 5%	GND	Within 2.0" of the ITP
TCK	27 ohm +/- 5%	GND	Within 2.0" of the ITP
TDO	Open	VTT	Within 2.0" of the ITP
ITP_EN	R268 Depop	+3VRUN	Close to CK410M Pin8

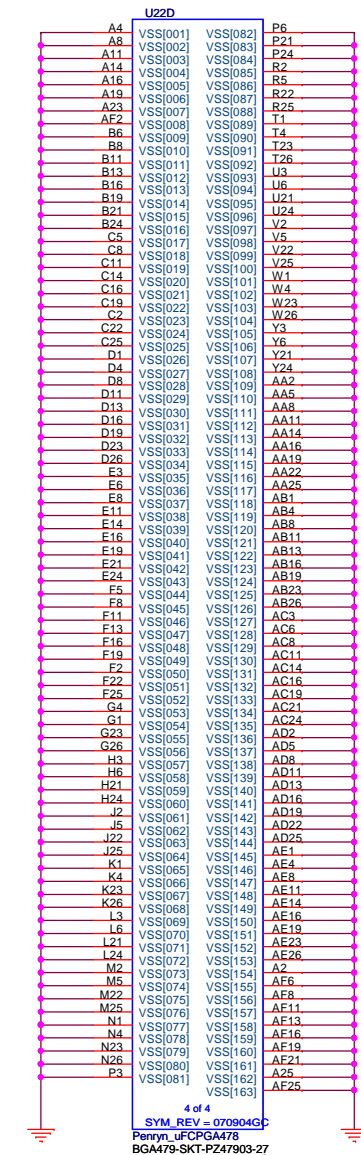
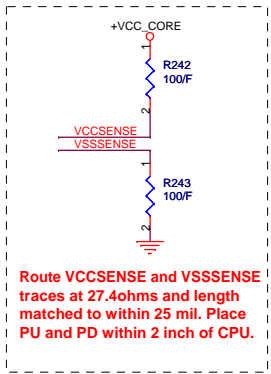
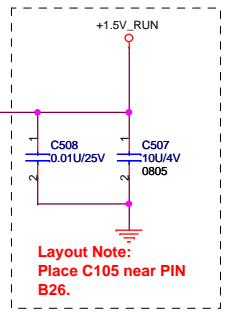
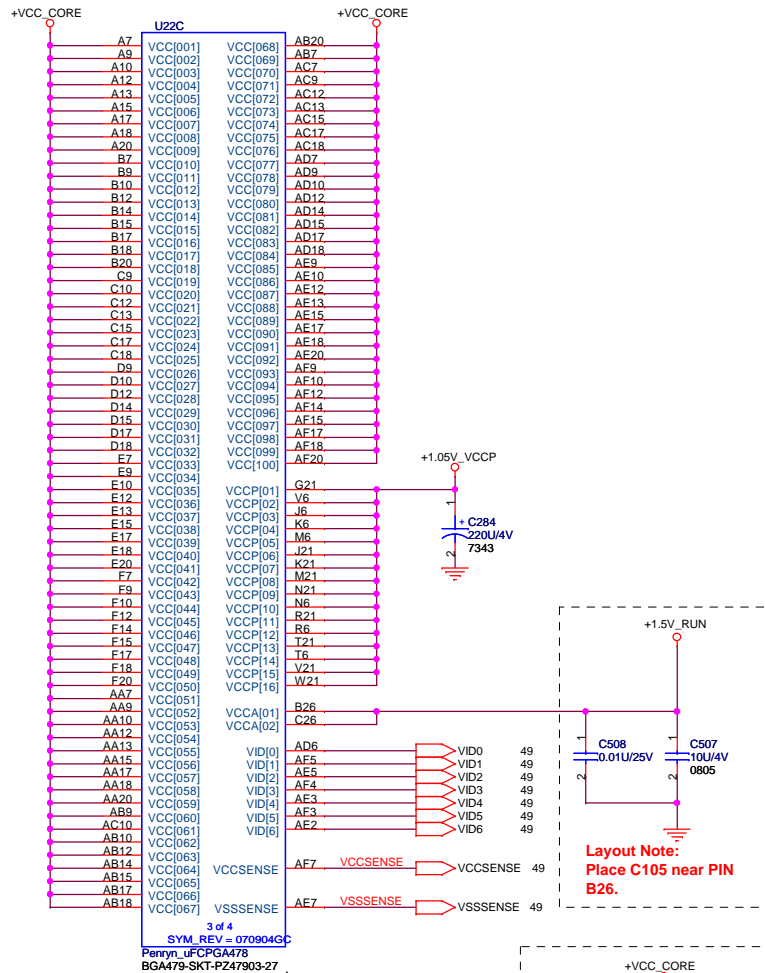
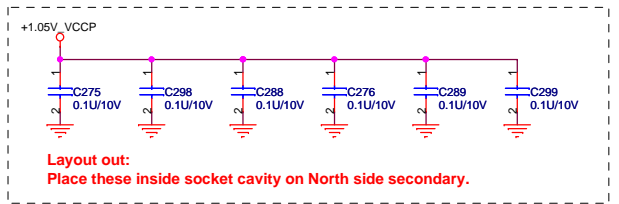
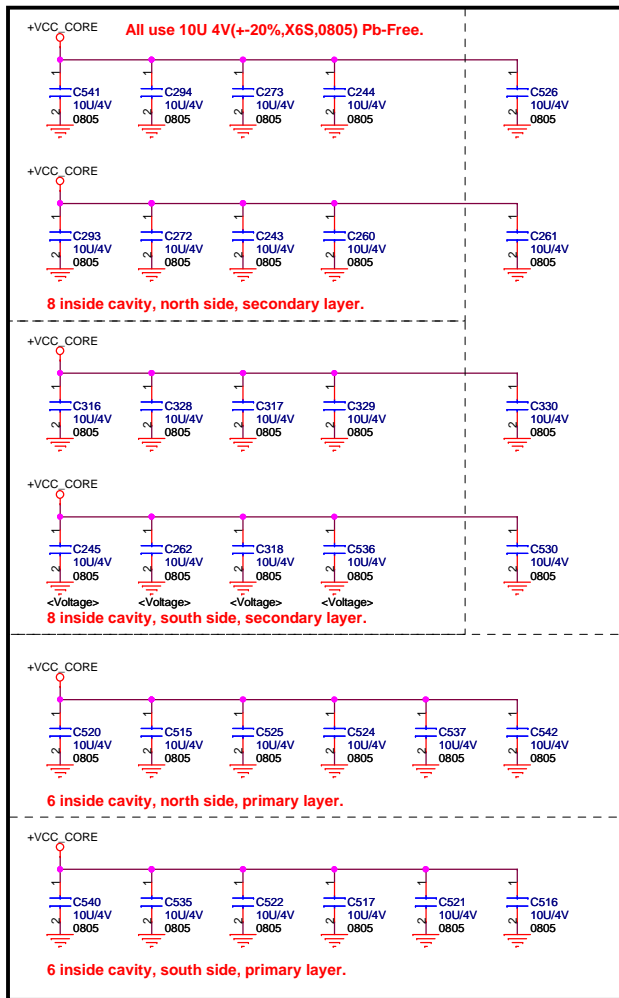
Comp0,2 connect with Zo=27.4ohm, Comp1,3 connect with Zo=55ohm, make those traces length shorter than 0.5". Trace should be at least 25 mils away from any other toggling signal.

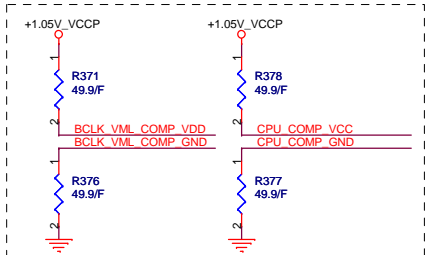
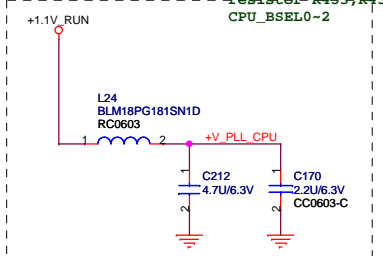
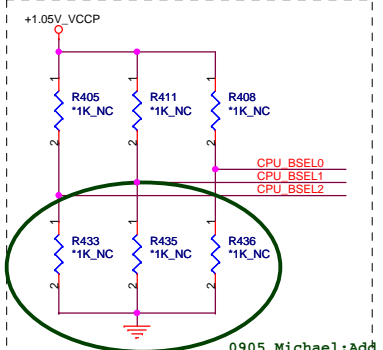
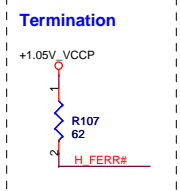
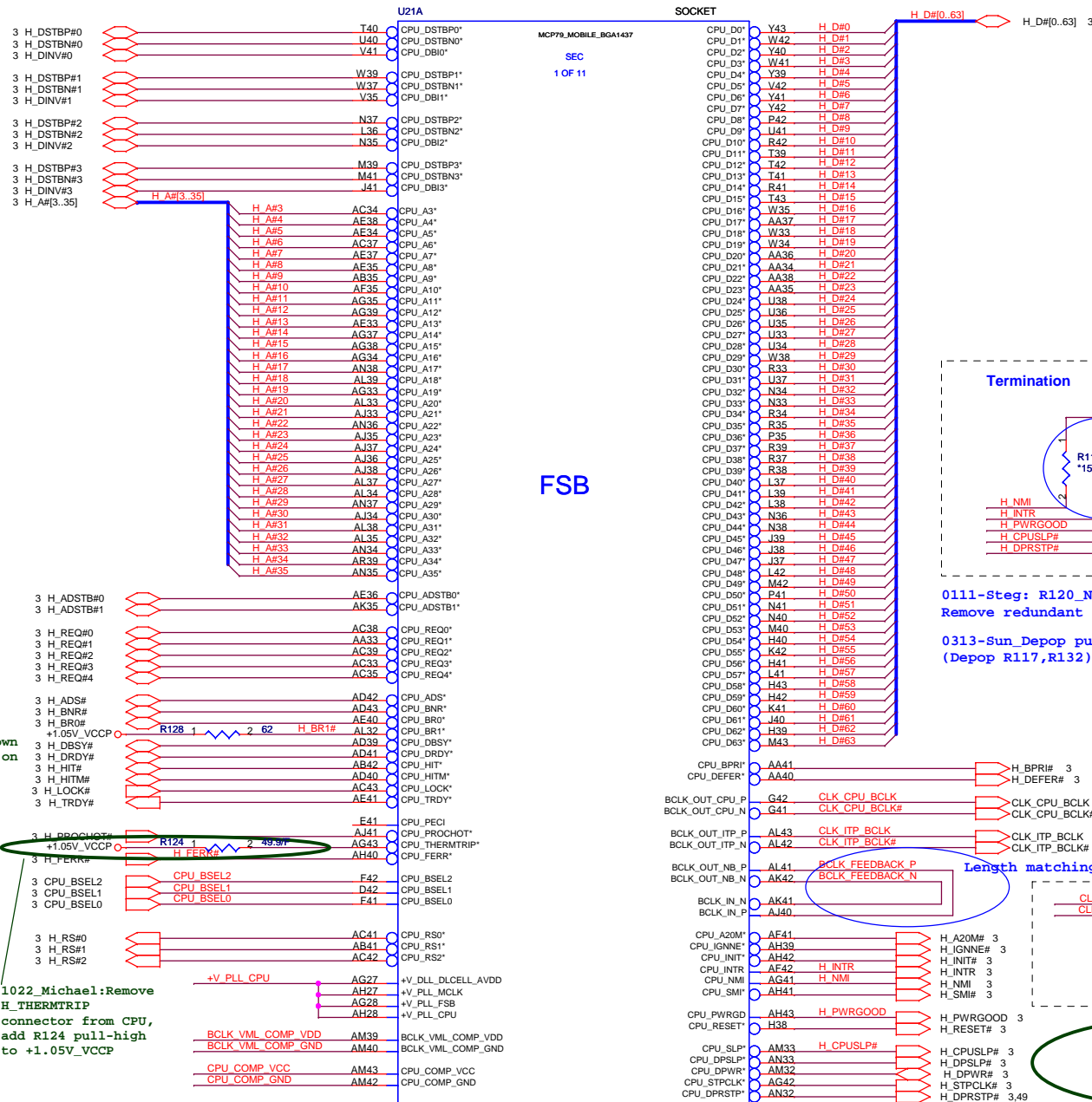
QUANTA COMPUTER

Title: Penryn Processor (HOST BUS)

Size: Document Number IM3 (XPS-Jolie) Rev 2A

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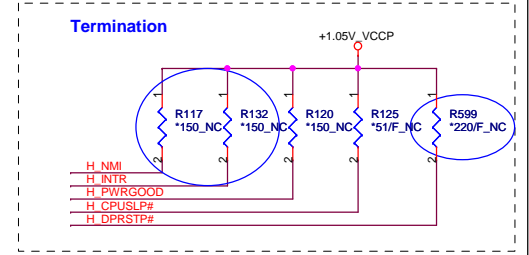


1. Route at normal impedance and 8 mils spacing to resistor.
 2. 49.9 ohm to GND or VTT_CPU less than 1 inch from MCP79.

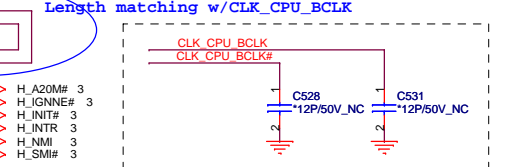
1022_Michael: Remove H_THERMTRIP connector from CPU, add R124 pull-high to +1.05V_VCCP

- | | | | |
|--|--|---|---|
| +V_DLL_DLCELL_AVDD
150mA with RUN rail
1 x ferrite bead
1 x 4.7uF X5R ceramic
1 x 2.2uF X7R ceramic | +V_PLL_MCLK
20mA with RUN rail
1 x ferrite bead
1 x 1uF X5R ceramic
1 x 2.2uF X7R ceramic | +V_PLL_FSB
29mA with RUN rail
1 x ferrite bead
1 x 4.7uF X5R ceramic
1 x 2.2uF X7R ceramic | +V_PLL_CPU
15mA with RUN rail
1 x ferrite bead
1 x 4.7uF X5R ceramic
1 x 2.2uF X7R ceramic |
|--|--|---|---|

0313-Sun_Add pull-up 220 ohm to +1.05V_VCCP on H_DPRSTP#



0111-Steig: R120_NC. Remove redundant pull-up R120 on H_PWRGOOD
 0313-Sun_Depop pull-up on H_NMI & H_INTR. (Depop R117, R132)



0605_Michael: NV review, remove pull-down C509 on CLK_ITP_BCLK & C510 on CLK_ITP_BCLK#

QUANTA COMPUTER

Title: MCP79 (HOST)

Size: Document Number IM3 (XPS-Jolie)

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Layout Notice:

- Memory Data Signal Group**
MCP79 BGA Breakout (<175ps): Route at 50 ohm impedance and 1.5x dielectric height spacing.
After Breakout: Route at 40 ohm impedance and 4x(Microstrip) or 3x(Stripline) dielectric spacing.
DIMM Fan-in (<90ps): Route at 40 ohm impedance and 1.5x dielectric height spacing.

- Memory Data Strobes**
Route strobes differentially at 66 ohm impedance (42 ohm SE) and 5x dielectric height spacing to other signals.

- Memory Clock Signal Group**
MCP79 BGA Breakout (<90ps): Route at 50 ohm SE / 100 ohm differential impedance.
After Breakout: Route at 40 ohm SE / 66 ohm differential impedance and 5x dielectric height spacing to other signals.

- Memory Address/Command/Control Signal Group**
MCP79 BGA Breakout (<90ps): Route at 50 ohm impedance and 1.5x dielectric height spacing.
After Breakout: Route at 40 ohm impedance and 2x dielectric height to other signals and 3x dielectric spacing to other non-associated signals.
DIMM Fan-in (<90ps): Route at 40 ohm impedance and 1.5x dielectric height spacing.



Title MCP79 (DDR3)		
Size	Document Number IMS (XPS-Jolie)	Rev 2A
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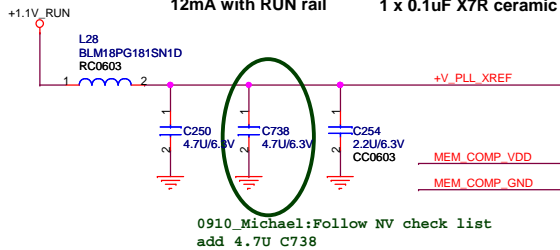
+V_VPLL
39mA with RUN rail

+V_PLL_XREF_XS
17mA with RUN rail

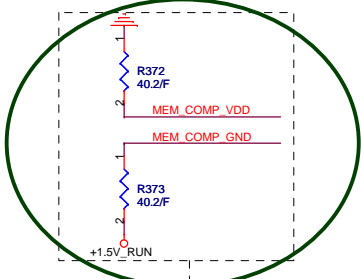
+V_PLL_CORE
19mA with RUN rail

+V_PLL_DP
12mA with RUN rail

1 x ferrite bead
1 x 4.7uF X5R ceramic
1 x 0.1uF X7R ceramic

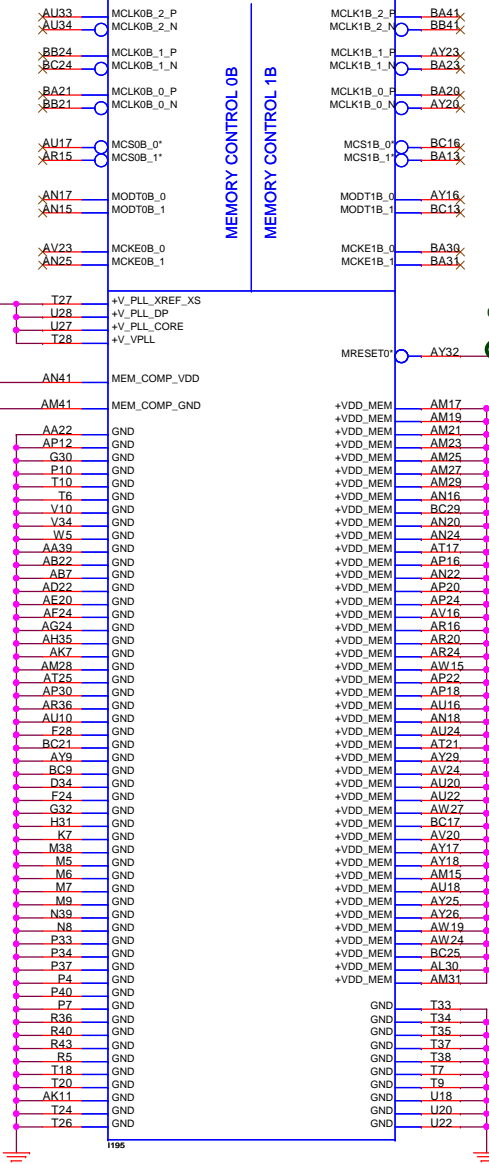


0102-Sun_Change MEM_COMP_VDD & MEM_COMP_GND setting
MEM_COMP_VDD from +1.5V_RUN to GND & MEM_COMP_GND from GND to +1.5V_RUN



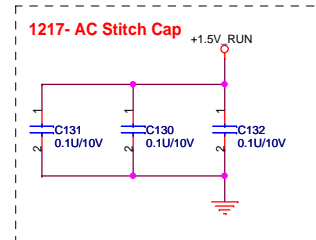
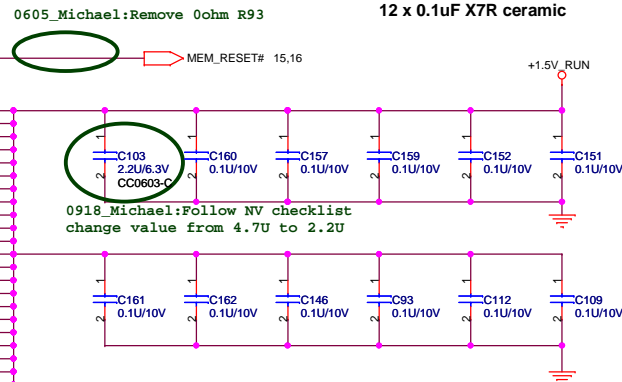
Layout Notice:
1. 40.2 +/-1% ohm to +1.5V_SUS less than 1 inch from MCP79 for DDR3.
2. Route with 7 mils trace width and 8 mils spacing to termination resistor.

U21D SOCKET
MCP79_MOBILE_BGA1437
SEC 4 OF 11



4.3A with ALW rail for S0
318mA for S0 Idle

1 x 2.2uF ceramic
12 x 0.1uF X7R ceramic



QUANTA COMPUTER

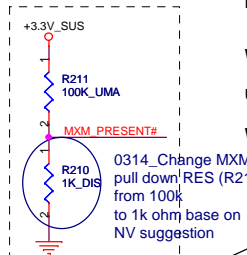
Title: MCP79 (MEM POWER)

Size: Document Number IM3 (XPS-Jolie) Rev 2A

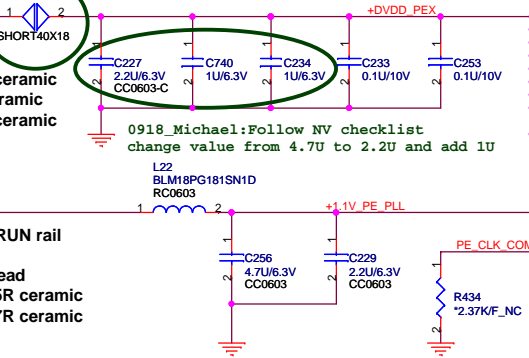
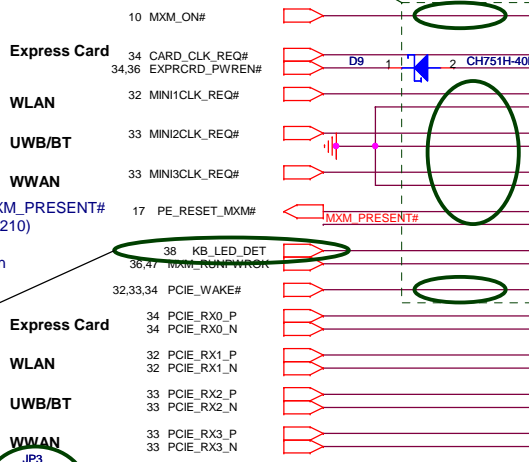
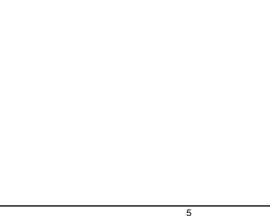
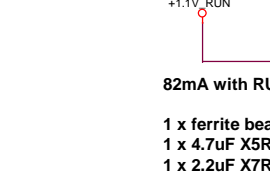
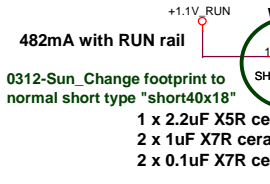
Date: Friday, September 19, 2008 Sheet 7 of 59

PCIe Layout Notice:
MCP79 BGA Breakout (<27ps):
Route at 50 ohm impedance and 1.5x dielectric height spacing.
After Breakout:
Route at 50 Signal end and 90 ohm differential.
Inter-pair spacing 4x (Microstrip) dielectric height spacing 3x (Stripline) dielectric height spacing.

0605_Michael:Remove 0ohm
 R185 on MXM_ON#
 R433,R435,168 pull-down to GND
 R177 on PE_RESET_MXM#
 R458 on PCIe_WAKE#



0825_Michael:Add KB detect function
 0918_Michael:Remove KB detect function
 0920_Michael:Add KB detect function



U21E MCP79_MOBILE_BGA1437

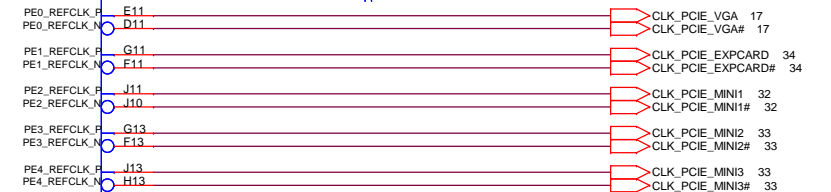
SEC 5 OF 11

PCIe

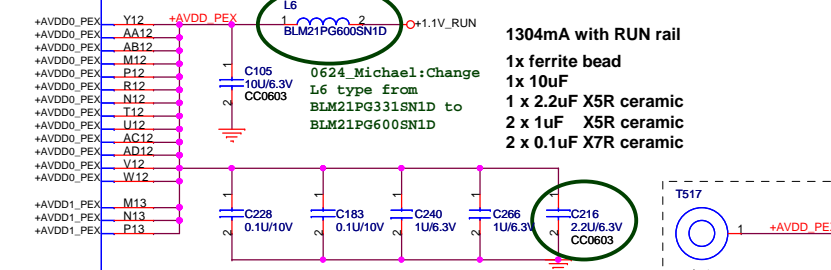
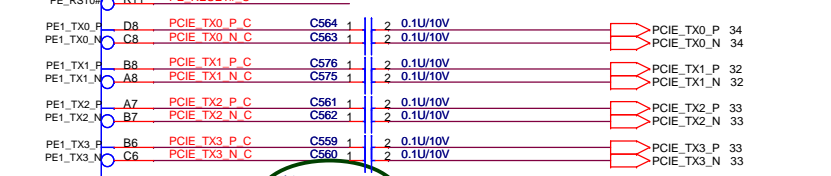
PCIe MRX GTX P0	E7	PE0_RX0_P
PCIe MRX GTX N0	E7	PE0_RX0_N
PCIe MRX GTX P1	D7	PE0_RX1_P
PCIe MRX GTX N1	C7	PE0_RX1_N
PCIe MRX GTX P2	E6	PE0_RX2_P
PCIe MRX GTX N2	E6	PE0_RX2_N
PCIe MRX GTX P3	E6	PE0_RX3_P
PCIe MRX GTX N3	F5	PE0_RX3_N
PCIe MRX GTX P4	E4	PE0_RX4_P
PCIe MRX GTX N4	E3	PE0_RX4_N
PCIe MRX GTX P5	C3	PE0_RX5_P
PCIe MRX GTX N5	D3	PE0_RX5_N
PCIe MRX GTX P6	G5	PE0_RX6_P
PCIe MRX GTX N6	H5	PE0_RX6_N
PCIe MRX GTX P7	J7	PE0_RX7_P
PCIe MRX GTX N7	J6	PE0_RX7_N
PCIe MRX GTX P8	J5	PE0_RX8_P
PCIe MRX GTX N8	J4	PE0_RX8_N
PCIe MRX GTX P9	L11	PE0_RX9_P
PCIe MRX GTX N9	L10	PE0_RX9_N
PCIe MRX GTX P10	L9	PE0_RX10_P
PCIe MRX GTX N10	L8	PE0_RX10_N
PCIe MRX GTX P11	L7	PE0_RX11_P
PCIe MRX GTX N11	L6	PE0_RX11_N
PCIe MRX GTX P12	N11	PE0_RX12_P
PCIe MRX GTX N12	N10	PE0_RX12_N
PCIe MRX GTX P13	N9	PE0_RX13_P
PCIe MRX GTX N13	N7	PE0_RX13_N
PCIe MRX GTX P14	N7	PE0_RX14_P
PCIe MRX GTX N14	N6	PE0_RX14_N
PCIe MRX GTX P15	N5	PE0_RX15_P
PCIe MRX GTX N15	N4	PE0_RX15_N

SOCKET

PE0_TX0_P	C5	PCIe MTX GRX C P0	C347	1	2	0.1U/10V DIS	PCIe MTX GRX P0
PE0_TX0_N	D4	PCIe MTX GRX C N0	C340	1	2	0.1U/10V DIS	PCIe MTX GRX N0
PE0_TX1_P	C4	PCIe MTX GRX C P1	C373	1	2	0.1U/10V DIS	PCIe MTX GRX P1
PE0_TX1_N	B4	PCIe MTX GRX C N1	C384	1	2	0.1U/10V DIS	PCIe MTX GRX N1
PE0_TX2_P	A4	PCIe MTX GRX C P2	C566	1	2	0.1U/10V DIS	PCIe MTX GRX P2
PE0_TX2_N	B3	PCIe MTX GRX C N2	C565	1	2	0.1U/10V DIS	PCIe MTX GRX N2
PE0_TX3_P	B2	PCIe MTX GRX C P3	C552	1	2	0.1U/10V DIS	PCIe MTX GRX P3
PE0_TX3_N	B2	PCIe MTX GRX C N3	C548	1	2	0.1U/10V DIS	PCIe MTX GRX N3
PE0_TX4_P	C1	PCIe MTX GRX C P4	C358	1	2	0.1U/10V DIS	PCIe MTX GRX P4
PE0_TX4_N	D1	PCIe MTX GRX C N4	C367	1	2	0.1U/10V DIS	PCIe MTX GRX N4
PE0_TX5_P	D2	PCIe MTX GRX C P5	C333	1	2	0.1U/10V DIS	PCIe MTX GRX P5
PE0_TX5_N	E1	PCIe MTX GRX C N5	C323	1	2	0.1U/10V DIS	PCIe MTX GRX N5
PE0_TX6_P	E2	PCIe MTX GRX C P6	C547	1	2	0.1U/10V DIS	PCIe MTX GRX P6
PE0_TX6_N	F2	PCIe MTX GRX C N6	C544	1	2	0.1U/10V DIS	PCIe MTX GRX N6
PE0_TX7_P	F3	PCIe MTX GRX C P7	C543	1	2	0.1U/10V DIS	PCIe MTX GRX P7
PE0_TX7_N	F4	PCIe MTX GRX C N7	C539	1	2	0.1U/10V DIS	PCIe MTX GRX N7
PE0_TX8_P	G3	PCIe MTX GRX C P8	C311	1	2	0.1U/10V DIS	PCIe MTX GRX P8
PE0_TX8_N	H4	PCIe MTX GRX C N8	C319	1	2	0.1U/10V DIS	PCIe MTX GRX N8
PE0_TX9_P	H3	PCIe MTX GRX C P9	C534	1	2	0.1U/10V DIS	PCIe MTX GRX P9
PE0_TX9_N	H2	PCIe MTX GRX C N9	C538	1	2	0.1U/10V DIS	PCIe MTX GRX N9
PE0_TX10_P	H1	PCIe MTX GRX C P10	C297	1	2	0.1U/10V DIS	PCIe MTX GRX P10
PE0_TX10_N	J1	PCIe MTX GRX C N10	C307	1	2	0.1U/10V DIS	PCIe MTX GRX N10
PE0_TX11_P	J2	PCIe MTX GRX C P11	C291	1	2	0.1U/10V DIS	PCIe MTX GRX P11
PE0_TX11_N	J3	PCIe MTX GRX C N11	C280	1	2	0.1U/10V DIS	PCIe MTX GRX N11
PE0_TX12_P	K2	PCIe MTX GRX C P12	C532	1	2	0.1U/10V DIS	PCIe MTX GRX P12
PE0_TX12_N	K3	PCIe MTX GRX C N12	C529	1	2	0.1U/10V DIS	PCIe MTX GRX N12
PE0_TX13_P	L4	PCIe MTX GRX C P13	C523	1	2	0.1U/10V DIS	PCIe MTX GRX P13
PE0_TX13_N	L3	PCIe MTX GRX C N13	C527	1	2	0.1U/10V DIS	PCIe MTX GRX N13
PE0_TX14_P	M4	PCIe MTX GRX C P14	C263	1	2	0.1U/10V DIS	PCIe MTX GRX P14
PE0_TX14_N	M3	PCIe MTX GRX C N14	C267	1	2	0.1U/10V DIS	PCIe MTX GRX N14
PE0_TX15_P	M2	PCIe MTX GRX C P15	C519	1	2	0.1U/10V DIS	PCIe MTX GRX P15
PE0_TX15_N	M1	PCIe MTX GRX C N15	C518	1	2	0.1U/10V DIS	PCIe MTX GRX N15



0605_Michael:Remove Test pad
 T21,T22,T28,T30



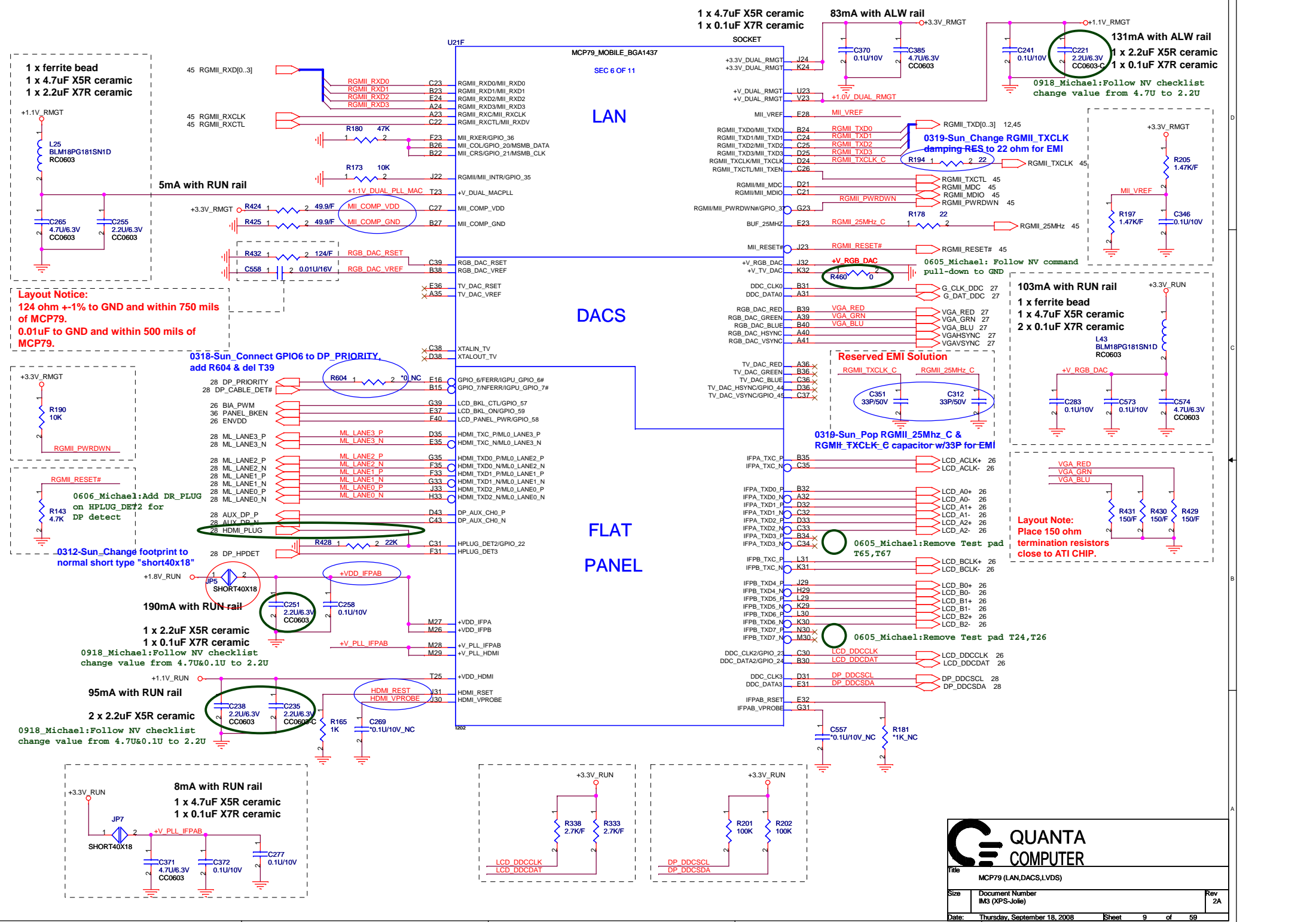
0918_Michael:Follow NV checklist
 change value from 4.7u to 2.2u

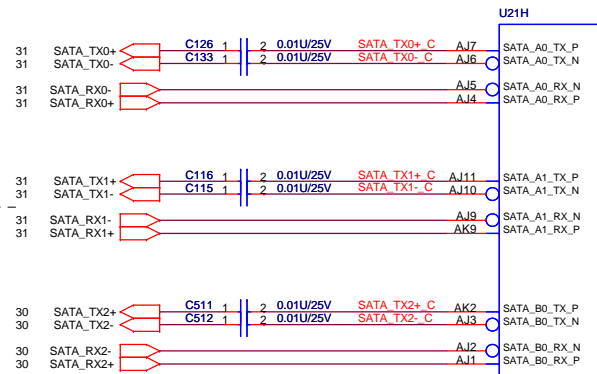
QUANTA COMPUTER

Title: MCP79 (PCIe)

Size	Document Number	Rev
	IM3 (XPS-Jolie)	2A

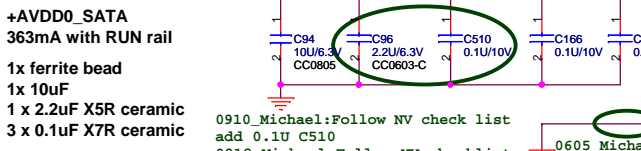
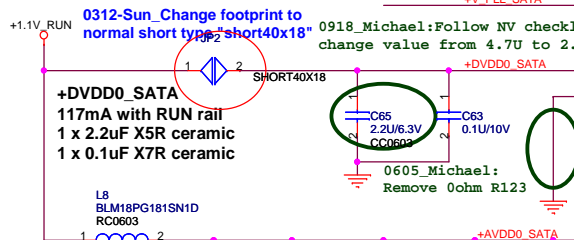
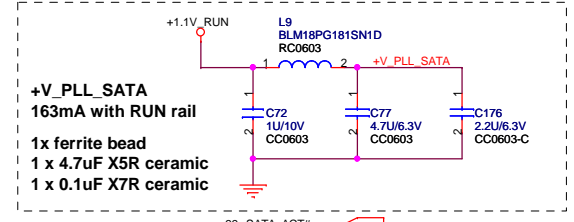
Date: Saturday, September 20, 2008 Sheet 8 of 59



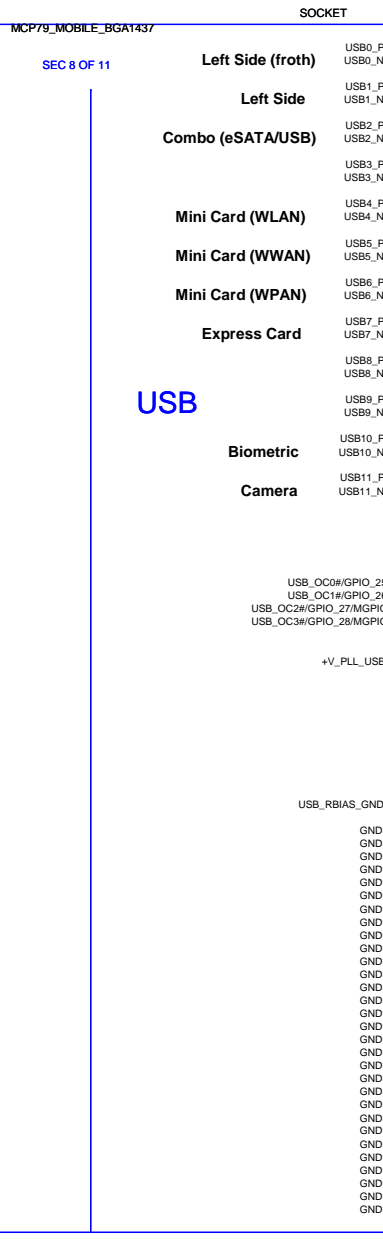
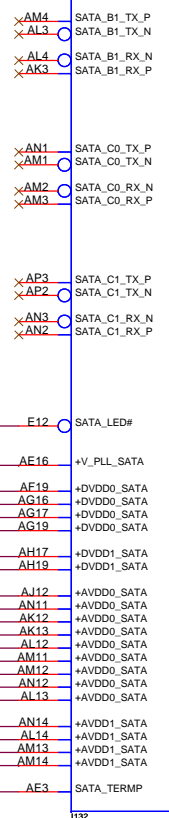


SATA

SATA Layout Notice:
BGA Breakout:
 Route differentially at normal impedance and 4 mils within pair and 6 mils to other signals. Maximum breakout distance is 400 mils of MCP79.
BGA Fan-out:
 Route differentially at normal impedance and 4 mils within pair and 10 mils to other signals. Maximum BGA breakout plus Fan-out distance is 500 mils.
After Brackout:
 Route at 100 ohm differential impedance (50 ohm SE) and 3x dielectric height spacing to other signals.
TX and RX intra-pair skew for a differential pair is 5 mils.

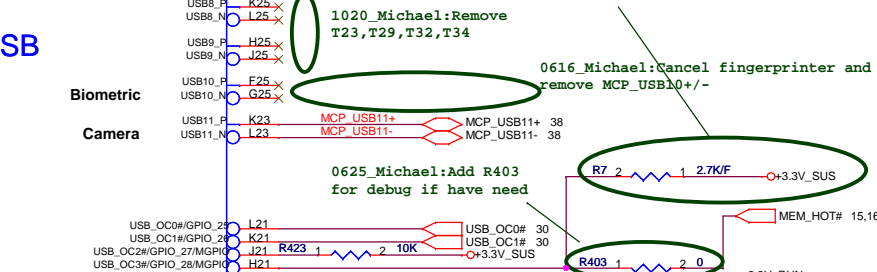
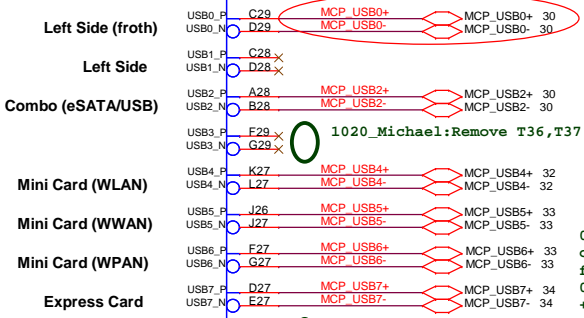


Layout Notice:
 2.49K ohm to GND within 500 mils of MCP79.
 Routing 8 mils spacing to resistor.



USB

0318-Sun_change left USB port from port1 to port0 for NV remote SW debug.



Layout Notice:
 909 ohm +-1% to GND within 1000 mil of MCP79.
 Routing trace at least 8 mil wide to resistor.

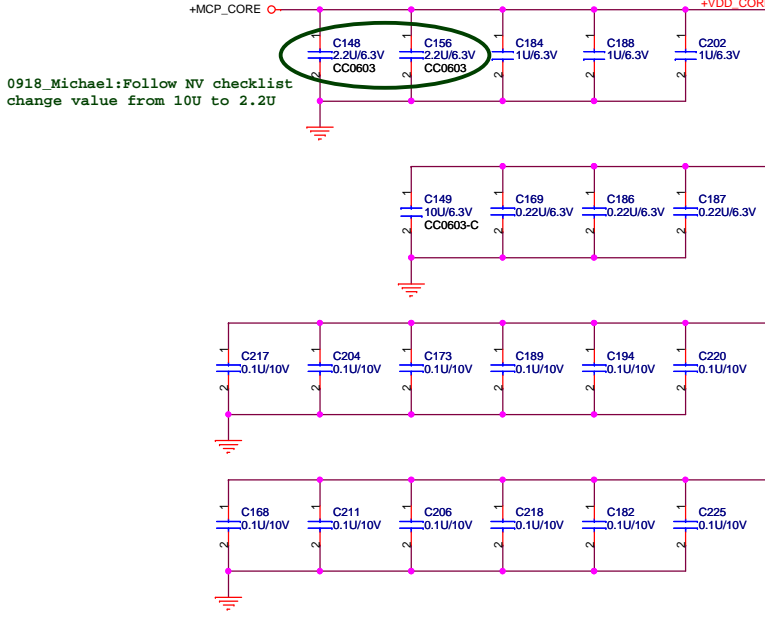
USB Layout Notice:
BGA Breakout:
 Route differentially at normal impedance and 4 mils within pair and 6 mils to other signals. Maximum breakout distance is 300 mils of MCP79.
BGA Fan-out:
 Route differentially at normal impedance and 4 mils within pair and 10 mils to other signals. Maximum BGA breakout plus Fan-out distance is 400 mils.
After Brackout:
 Route at 100 ohm differential impedance (50 ohm SE) and 4x dielectric height spacing (Microstrip) or 2x dielectric height spacing (Stripline) to other signals.
 Each USB pair must be length matched to within 50 mil.



Title MCP79 (SATA,USB)		
Size	Document Number IM3 (XPS-Jolie)	Rev 2A
Date:	Monday, October 20, 2008	Sheet 11 of 59

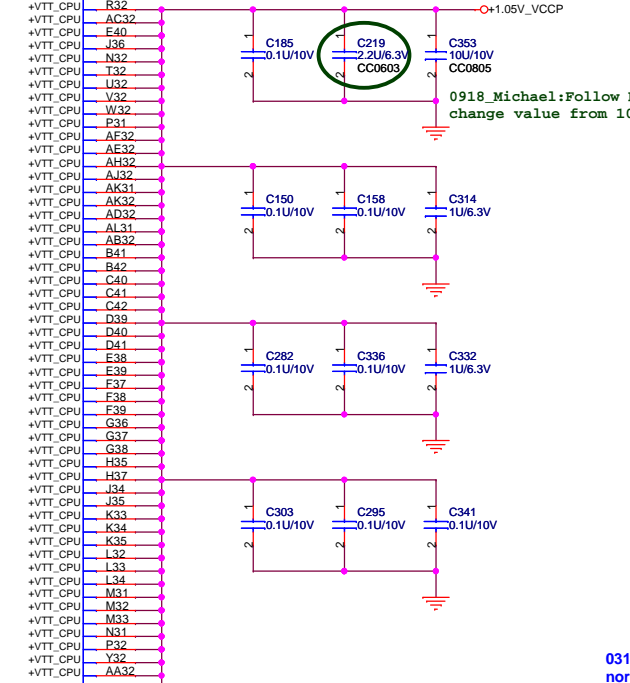
1 x 10uF ceramic
 2 x 2.2uF X5R ceramic
 3 x 1uF X5R ceramic
 3 x 0.22uF X5R ceramic
 12 x 0.1uF X7R ceramic

17.756A with RUN rail for S0
 2850mA for S0 Idle

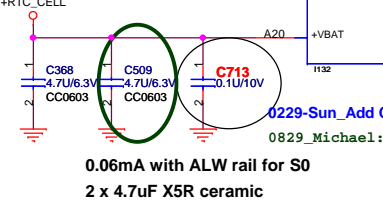
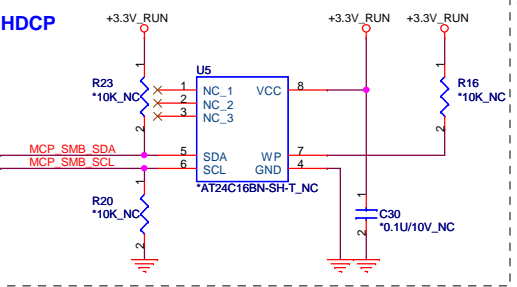
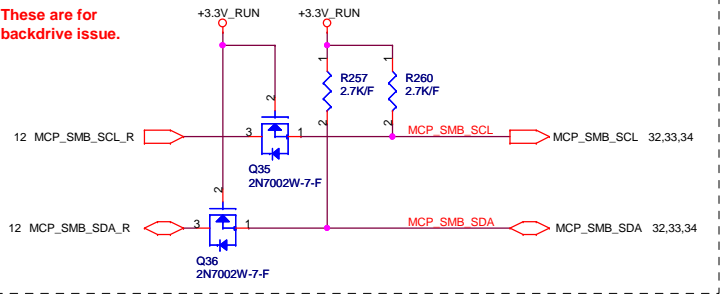


+VTT_CPU
 1139mA for ALW rail
 +VTT_CPUCLK
 43mA for ALW rail

1 x 10uF ceramic
 1 x 2.2uF X5R ceramic
 3 x 0.1uF X7R ceramic



POWER

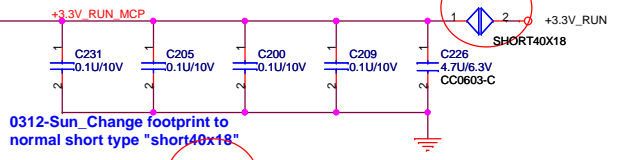


0229-Sun_Add C713 with 0.1U on +VBAT of MCP79
 0829_Michael:Follow NV new DG add C509 on +RTC_CELL of MCP79

0.06mA with ALW rail for S0
 2 x 4.7uF X5R ceramic

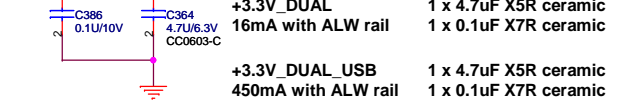
+3.3V_RUN_MCP
 450mA with RUN rail

1 x 4.7uF X5R ceramic
 4 x 0.1uF X7R ceramic



+3.3V_DUAL
 16mA with ALW rail

1 x 4.7uF X5R ceramic
 1 x 0.1uF X7R ceramic



+3.3V_DUAL_USB
 450mA with ALW rail

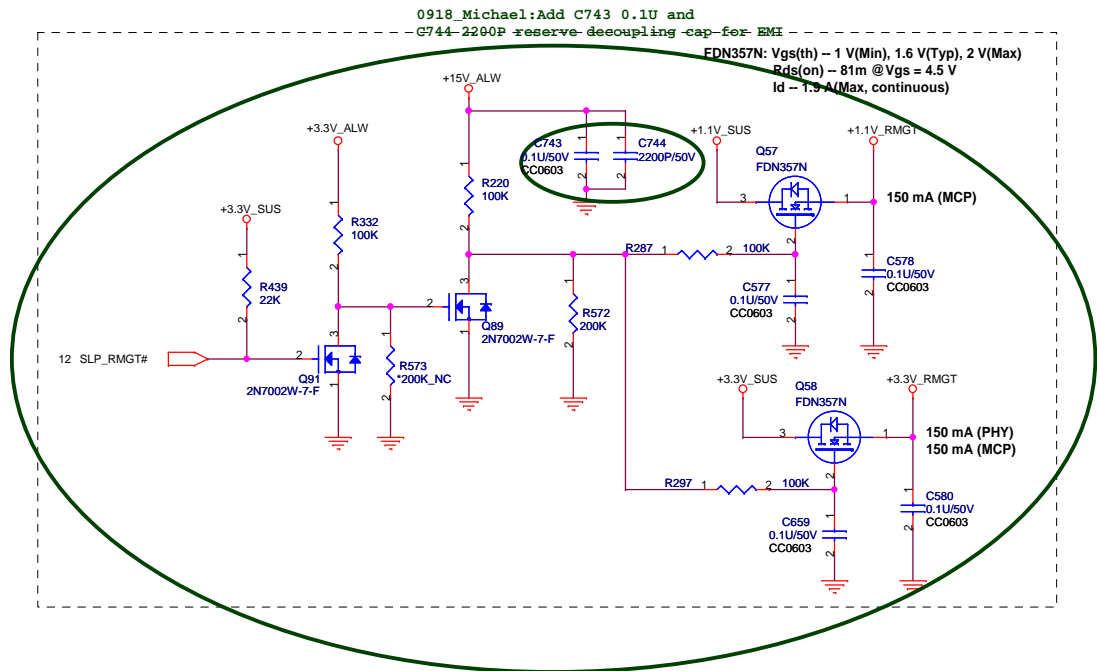
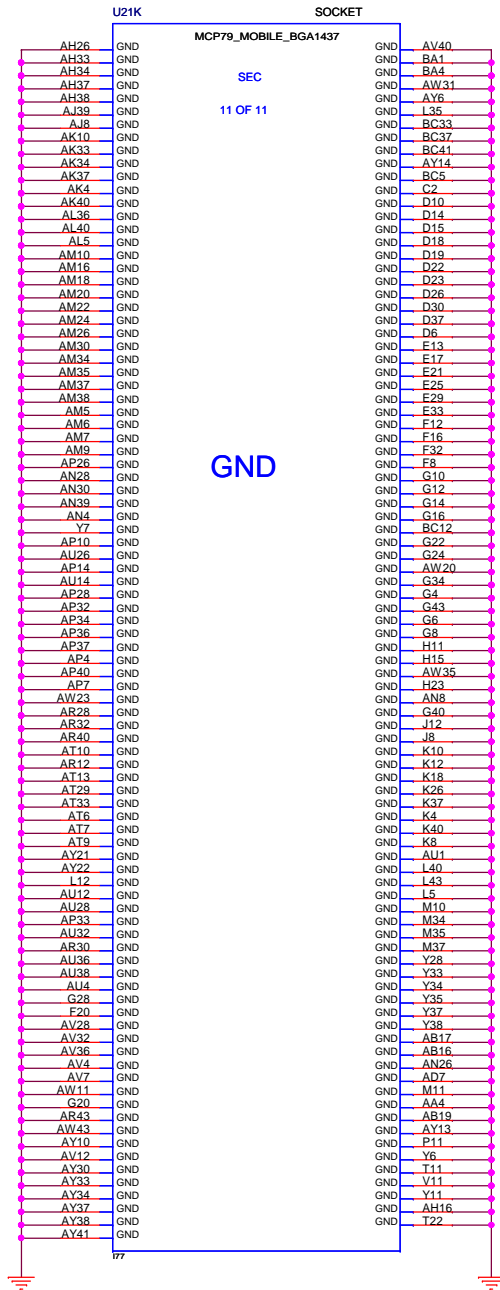
1 x 4.7uF X5R ceramic
 1 x 0.1uF X7R ceramic

+VDD_AUXC
 105mA with ALW rail

2 x 0.1uF X7R ceramic



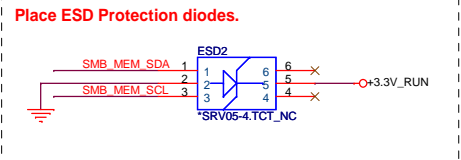
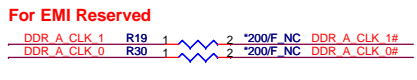
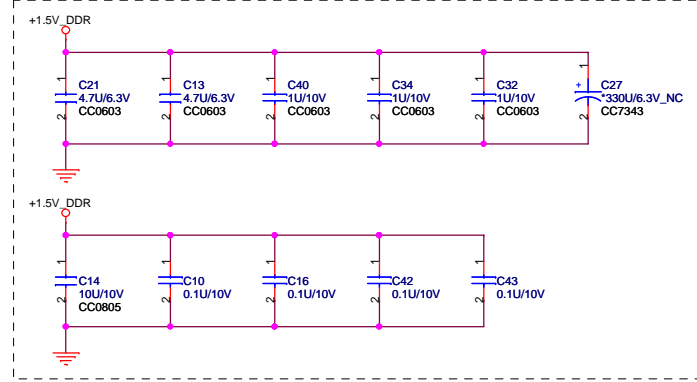
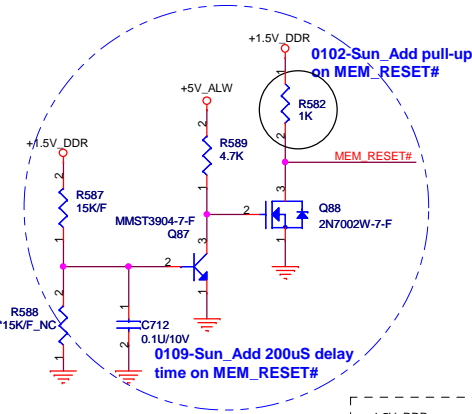
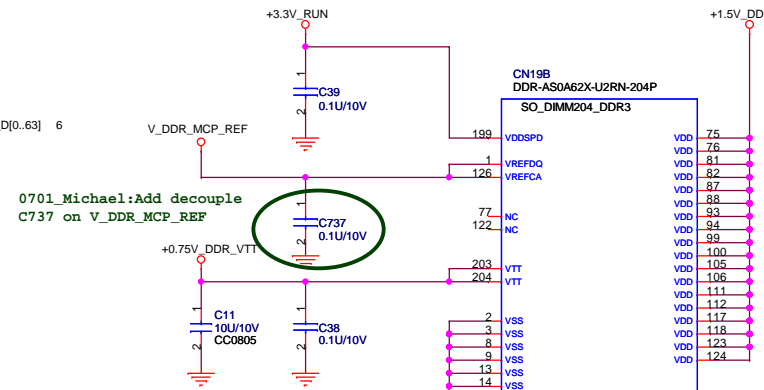
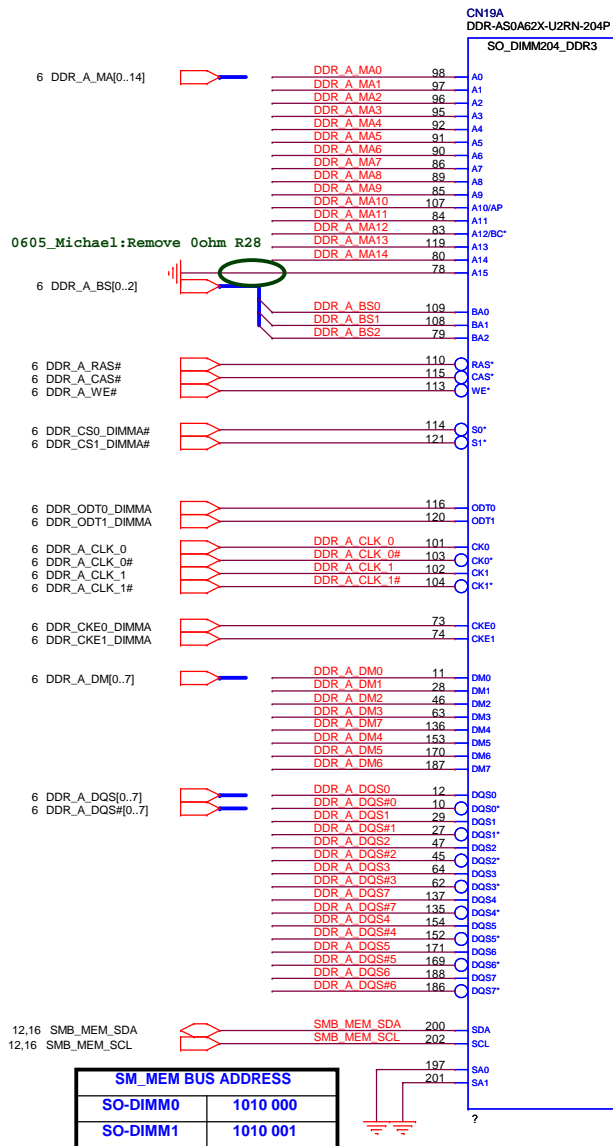
Title MCP79 (POWER)		
Size	Document Number IM3 (XPS-Jolie)	Rev 2A
Date:	Friday, September 19, 2008	Sheet 13 of 59



0229-Sun 1.1V_RMGT & +3.3V_RMGT MOSFET Vgs aren't enough issue, modify circuit reference NV CRB (Del JP11,JP12)
 Change Q57 from SI2304BDS-T1-E3 to FDN357N, Q58 from SI2304BDS-T1-E3 to SI2301BDS-T1-E3
 Add Q89 with 2N7002, R591 with 10K)
 0825_Michael:Change Q58 type from SI2301BDS to FDN357N and add MOS 2N7002W-7-F,R&C for +1.1V_RMGT and +3.3V_RMGT power low issue



Title MCP79 (GND)		
Size	Document Number IM3 (XPS-Jolie)	Rev 2A
Date:	Friday, September 19, 2008	Sheet 14 of 59

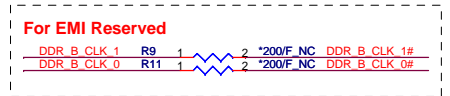
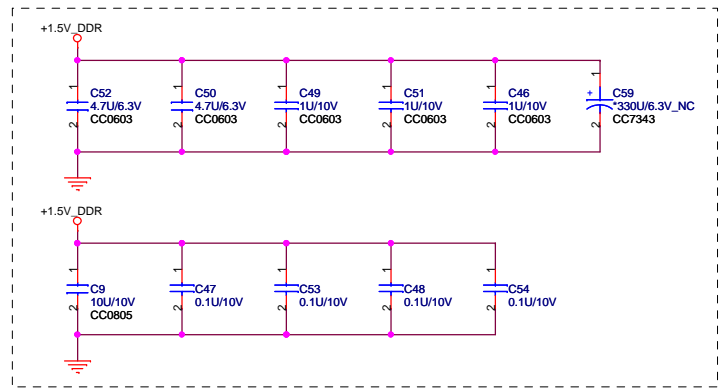
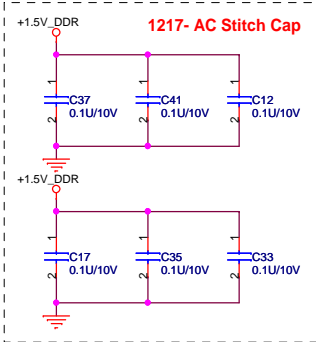
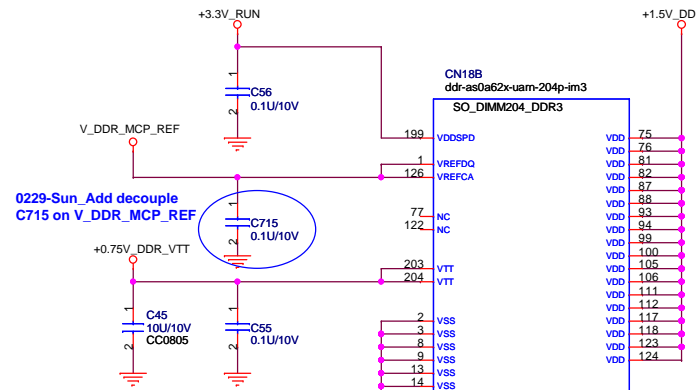
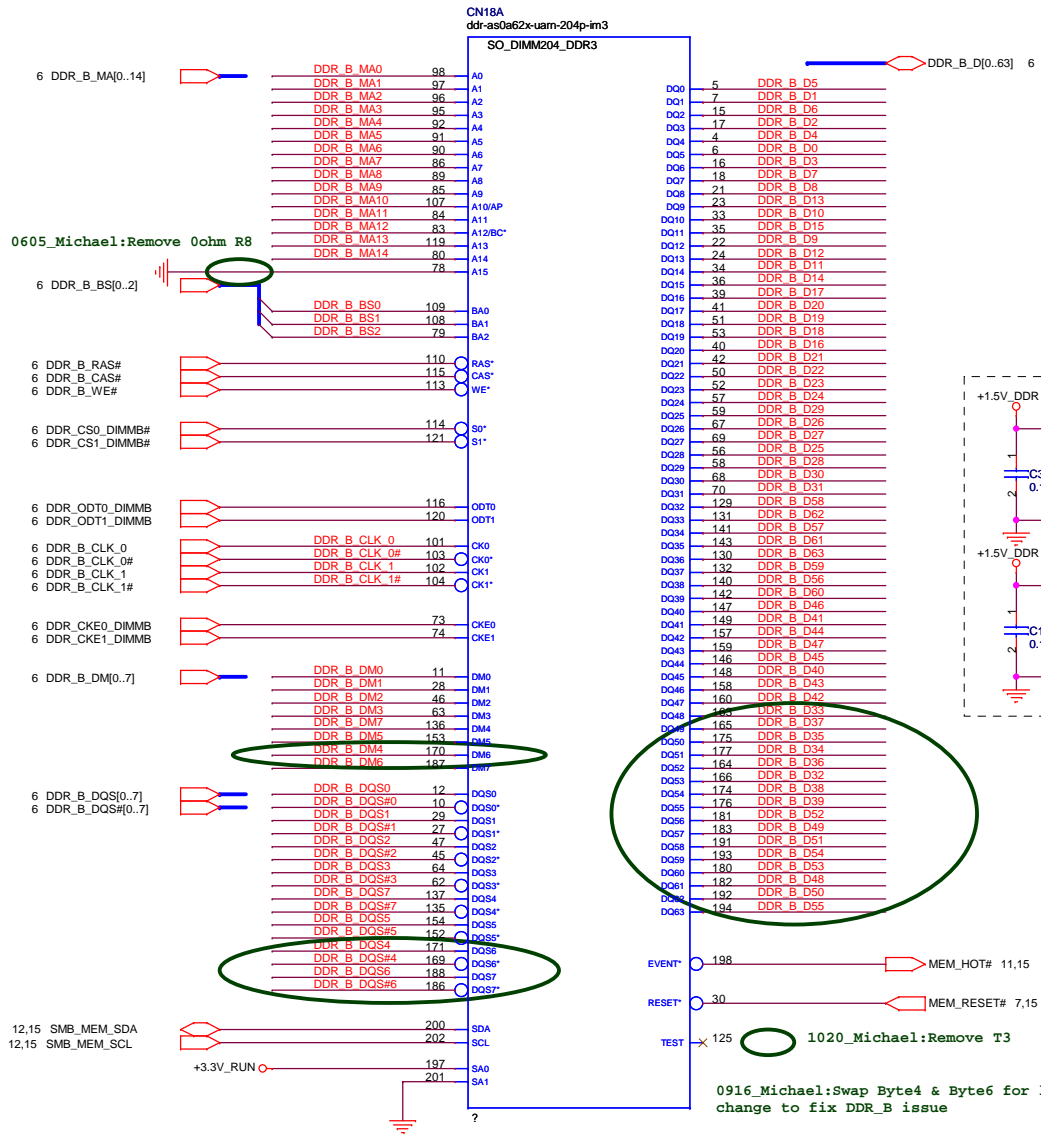


QUANTA COMPUTER

Title: DDR3 SO-DIMM (204P)

Size: Document Number IM3 (XPS-Jolie) Rev 2A

Date: Monday, October 20, 2008 Sheet 15 of 59



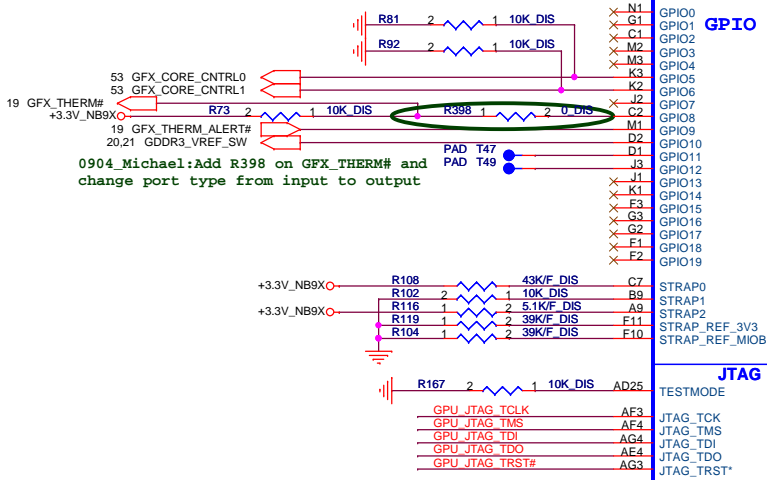
Title DDR3 SO-DIMM (204P)		
Size	Document Number IM3 (XPS-Jolie)	Rev 2A
Date:	Monday, October 20, 2008	Sheet 16 of 59

8 PCIE_MTX_GRX_P[0..15]
8 PCIE_MTX_GRX_N[0..15]

1113-Sun_Swap PEG for routing smooth.

1115-Sun_Follow NV's command to swap PEG for routing

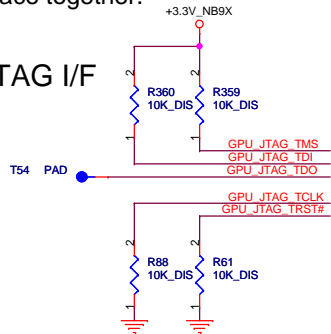
8 CLK_PCIE_VGA
8 CLK_PCIE_VGA#
8,32,33,34,36 PE_RESET#
8 PE_RESET_MXM#



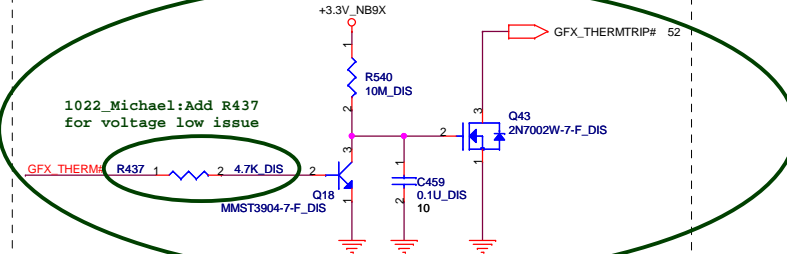
0904_Michael: Add R398 on GFX_THERM# and change port type from input to output

Place together.

JTAG I/F



GPU THERMTRIP Circuit



1022_Michael: Add R437 for voltage low issue

0825_Michael: Modify THERMTRIP circuit, add MOS and CAP

U20A PART 1 OF 5

PCIE_MTX_GRX_P15	AE12	PEX_RX0
PCIE_MTX_GRX_N15	AF12	PEX_RX0*
PCIE_MTX_GRX_P14	AG12	PEX_RX1
PCIE_MTX_GRX_N14	AG13	PEX_RX1*
PCIE_MTX_GRX_P13	AF13	PEX_RX2
PCIE_MTX_GRX_N13	AE13	PEX_RX2*
PCIE_MTX_GRX_P12	AE15	PEX_RX3
PCIE_MTX_GRX_N12	AF15	PEX_RX3*
PCIE_MTX_GRX_P11	AG15	PEX_RX4
PCIE_MTX_GRX_N11	AG16	PEX_RX4*
PCIE_MTX_GRX_P10	AE16	PEX_RX5
PCIE_MTX_GRX_N10	AE16	PEX_RX5*
PCIE_MTX_GRX_P9	AE18	PEX_RX6
PCIE_MTX_GRX_N9	AF18	PEX_RX6*
PCIE_MTX_GRX_P8	AG18	PEX_RX7
PCIE_MTX_GRX_N8	AG19	PEX_RX7*
PCIE_MTX_GRX_P7	AF19	PEX_RX8
PCIE_MTX_GRX_N7	AE19	PEX_RX8*
PCIE_MTX_GRX_P6	AE21	PEX_RX9
PCIE_MTX_GRX_N6	AF21	PEX_RX9*
PCIE_MTX_GRX_P5	AG21	PEX_RX9*
PCIE_MTX_GRX_N5	AG22	PEX_RX10
PCIE_MTX_GRX_P4	AE22	PEX_RX10*
PCIE_MTX_GRX_N4	AE22	PEX_RX11
PCIE_MTX_GRX_P3	AE24	PEX_RX12
PCIE_MTX_GRX_N3	AF24	PEX_RX12*
PCIE_MTX_GRX_P2	AG24	PEX_RX12*
PCIE_MTX_GRX_N2	AE25	PEX_RX13
PCIE_MTX_GRX_P1	AG25	PEX_RX14
PCIE_MTX_GRX_N1	AG26	PEX_RX14*
PCIE_MTX_GRX_P0	AE27	PEX_RX15
PCIE_MTX_GRX_N0	AE27	PEX_RX15*

GPIO

ROM_CS*
ROM_SI
ROM_SO
ROM_SCLK
I2CH_SCL
I2CH_SDA
BUFRST*

JTAG

TESTMODE
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_TRST*

NB9M_DIS
PBGAs33-NVIDIA-GEFORCE6250
Footprint: BGA533-NVIDIA-NB9M-GS

GPIO0
GPIO1
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8
GPIO9
GPIO10
GPIO11
GPIO12
GPIO13
GPIO14
GPIO15
GPIO16
GPIO17
GPIO18
GPIO19

STRAP0
STRAP1
STRAP2
STRAP_REF_3V3
STRAP_REF_MIOB

NC_01
NC_02
NC_03
NC_04
NC_05
NC_06
NC_07
NC_08
NC_09
NC_10

C15
D15
E15
J6
J5
T6
AA6
AC19
AE9
AG9

ROM_CS*
ROM_SI
ROM_SO
ROM_SCLK
I2CH_SCL
I2CH_SDA
BUFRST*

STRAP0
STRAP1
STRAP2
STRAP_REF_3V3
STRAP_REF_MIOB

NC_01
NC_02
NC_03
NC_04
NC_05
NC_06
NC_07
NC_08
NC_09
NC_10

C15
D15
E15
J6
J5
T6
AA6
AC19
AE9
AG9

ROM_CS*
ROM_SI
ROM_SO
ROM_SCLK
I2CH_SCL
I2CH_SDA
BUFRST*

STRAP0
STRAP1
STRAP2
STRAP_REF_3V3
STRAP_REF_MIOB

NC_01
NC_02
NC_03
NC_04
NC_05
NC_06
NC_07
NC_08
NC_09
NC_10

C15
D15
E15
J6
J5
T6
AA6
AC19
AE9
AG9

ROM_CS*
ROM_SI
ROM_SO
ROM_SCLK
I2CH_SCL
I2CH_SDA
BUFRST*

STRAP0
STRAP1
STRAP2
STRAP_REF_3V3
STRAP_REF_MIOB

NC_01
NC_02
NC_03
NC_04
NC_05
NC_06
NC_07
NC_08
NC_09
NC_10

C15
D15
E15
J6
J5
T6
AA6
AC19
AE9
AG9

ROM_CS*
ROM_SI
ROM_SO
ROM_SCLK
I2CH_SCL
I2CH_SDA
BUFRST*

STRAP0
STRAP1
STRAP2
STRAP_REF_3V3
STRAP_REF_MIOB

NC_01
NC_02
NC_03
NC_04
NC_05
NC_06
NC_07
NC_08
NC_09
NC_10

C15
D15
E15
J6
J5
T6
AA6
AC19
AE9
AG9

ROM_CS*
ROM_SI
ROM_SO
ROM_SCLK
I2CH_SCL
I2CH_SDA
BUFRST*

STRAP0
STRAP1
STRAP2
STRAP_REF_3V3
STRAP_REF_MIOB

NC_01
NC_02
NC_03
NC_04
NC_05
NC_06
NC_07
NC_08
NC_09
NC_10

C15
D15
E15
J6
J5
T6
AA6
AC19
AE9
AG9

ROM_CS*
ROM_SI
ROM_SO
ROM_SCLK
I2CH_SCL
I2CH_SDA
BUFRST*

STRAP0
STRAP1
STRAP2
STRAP_REF_3V3
STRAP_REF_MIOB

NC_01
NC_02
NC_03
NC_04
NC_05
NC_06
NC_07
NC_08
NC_09
NC_10

C15
D15
E15
J6
J5
T6
AA6
AC19
AE9
AG9

ROM_CS*
ROM_SI
ROM_SO
ROM_SCLK
I2CH_SCL
I2CH_SDA
BUFRST*

STRAP0
STRAP1
STRAP2
STRAP_REF_3V3
STRAP_REF_MIOB

NC_01
NC_02
NC_03
NC_04
NC_05
NC_06
NC_07
NC_08
NC_09
NC_10

C15
D15
E15
J6
J5
T6
AA6
AC19
AE9
AG9

ROM_CS*
ROM_SI
ROM_SO
ROM_SCLK
I2CH_SCL
I2CH_SDA
BUFRST*

STRAP0
STRAP1
STRAP2
STRAP_REF_3V3
STRAP_REF_MIOB

NC_01
NC_02
NC_03
NC_04
NC_05
NC_06
NC_07
NC_08
NC_09
NC_10

C15
D15
E15
J6
J5
T6
AA6
AC19
AE9
AG9

ROM_CS*
ROM_SI
ROM_SO
ROM_SCLK
I2CH_SCL
I2CH_SDA
BUFRST*

STRAP0
STRAP1
STRAP2
STRAP_REF_3V3
STRAP_REF_MIOB

NC_01
NC_02
NC_03
NC_04
NC_05
NC_06
NC_07
NC_08
NC_09
NC_10

C15
D15
E15
J6
J5
T6
AA6
AC19
AE9
AG9

ROM_CS*
ROM_SI
ROM_SO
ROM_SCLK
I2CH_SCL
I2CH_SDA
BUFRST*

STRAP0
STRAP1
STRAP2
STRAP_REF_3V3
STRAP_REF_MIOB

NC_01
NC_02
NC_03
NC_04
NC_05
NC_06
NC_07
NC_08
NC_09
NC_10

C15
D15
E15
J6
J5
T6
AA6
AC19
AE9
AG9

ROM_CS*
ROM_SI
ROM_SO
ROM_SCLK
I2CH_SCL
I2CH_SDA
BUFRST*

STRAP0
STRAP1
STRAP2
STRAP_REF_3V3
STRAP_REF_MIOB

NC_01
NC_02
NC_03
NC_04
NC_05
NC_06
NC_07
NC_08
NC_09
NC_10

C15
D15
E15
J6
J5
T6
AA6
AC19
AE9
AG9

ROM_CS*
ROM_SI
ROM_SO
ROM_SCLK
I2CH_SCL
I2CH_SDA
BUFRST*

STRAP0
STRAP1
STRAP2
STRAP_REF_3V3
STRAP_REF_MIOB

NC_01
NC_02
NC_03
NC_04
NC_05
NC_06
NC_07
NC_08
NC_09
NC_10

C15
D15
E15
J6
J5
T6
AA6
AC19
AE9
AG9

ROM_CS*
ROM_SI
ROM_SO
ROM_SCLK
I2CH_SCL
I2CH_SDA
BUFRST*

STRAP0
STRAP1
STRAP2
STRAP_REF_3V3
STRAP_REF_MIOB

NC_01
NC_02
NC_03
NC_04
NC_05
NC_06
NC_07
NC_08
NC_09
NC_10

C15
D15
E15
J6
J5
T6
AA6
AC19
AE9
AG9

ROM_CS*
ROM_SI
ROM_SO
ROM_SCLK
I2CH_SCL
I2CH_SDA
BUFRST*

STRAP0
STRAP1
STRAP2
STRAP_REF_3V3
STRAP_REF_MIOB

NC_01
NC_02
NC_03
NC_04
NC_05
NC_06
NC_07
NC_08
NC_09
NC_10

C15
D15
E15
J6
J5
T6
AA6
AC19
AE9
AG9

ROM_CS*
ROM_SI
ROM_SO
ROM_SCLK
I2CH_SCL
I2CH_SDA
BUFRST*

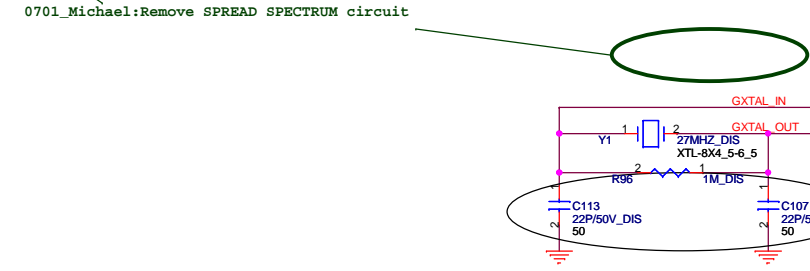
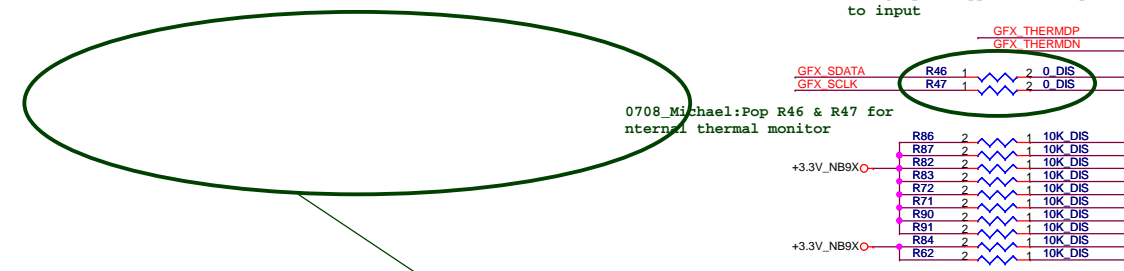
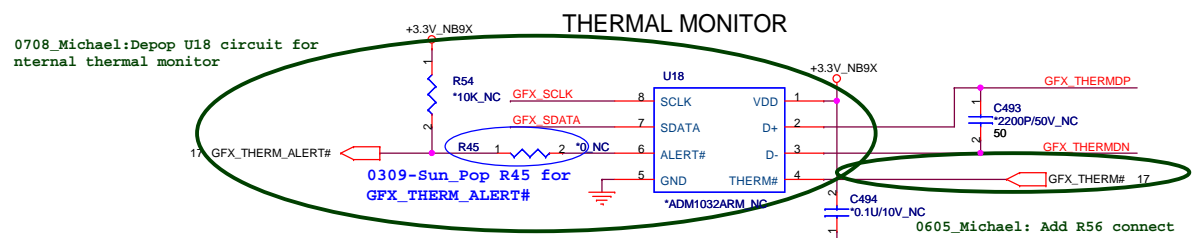
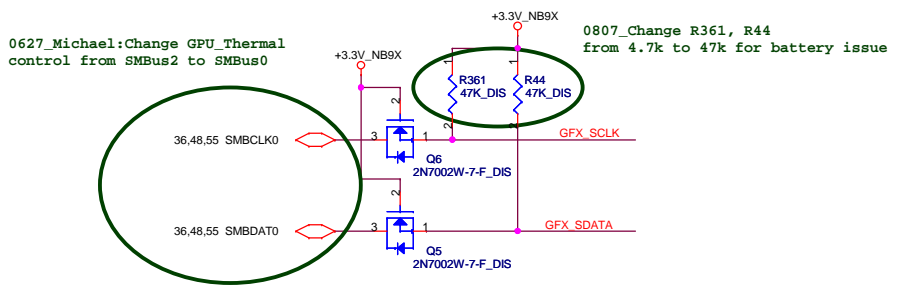
STRAP0
STRAP1
STRAP2
STRAP_REF_3V3
STRAP_REF_MIOB

NC_01
NC_02
NC_03
NC_04
NC_05
NC_06
NC_07
NC_08
NC_09
NC_10

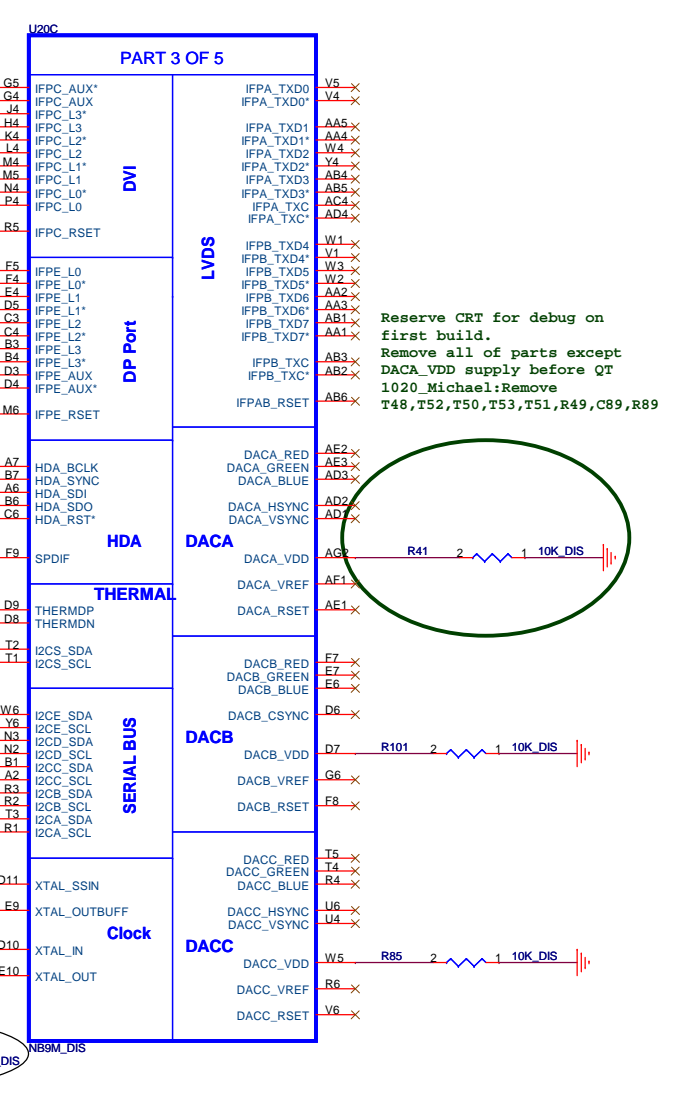
C15
D15
E15
J6
J5
T6
AA6
AC19
AE9
AG9

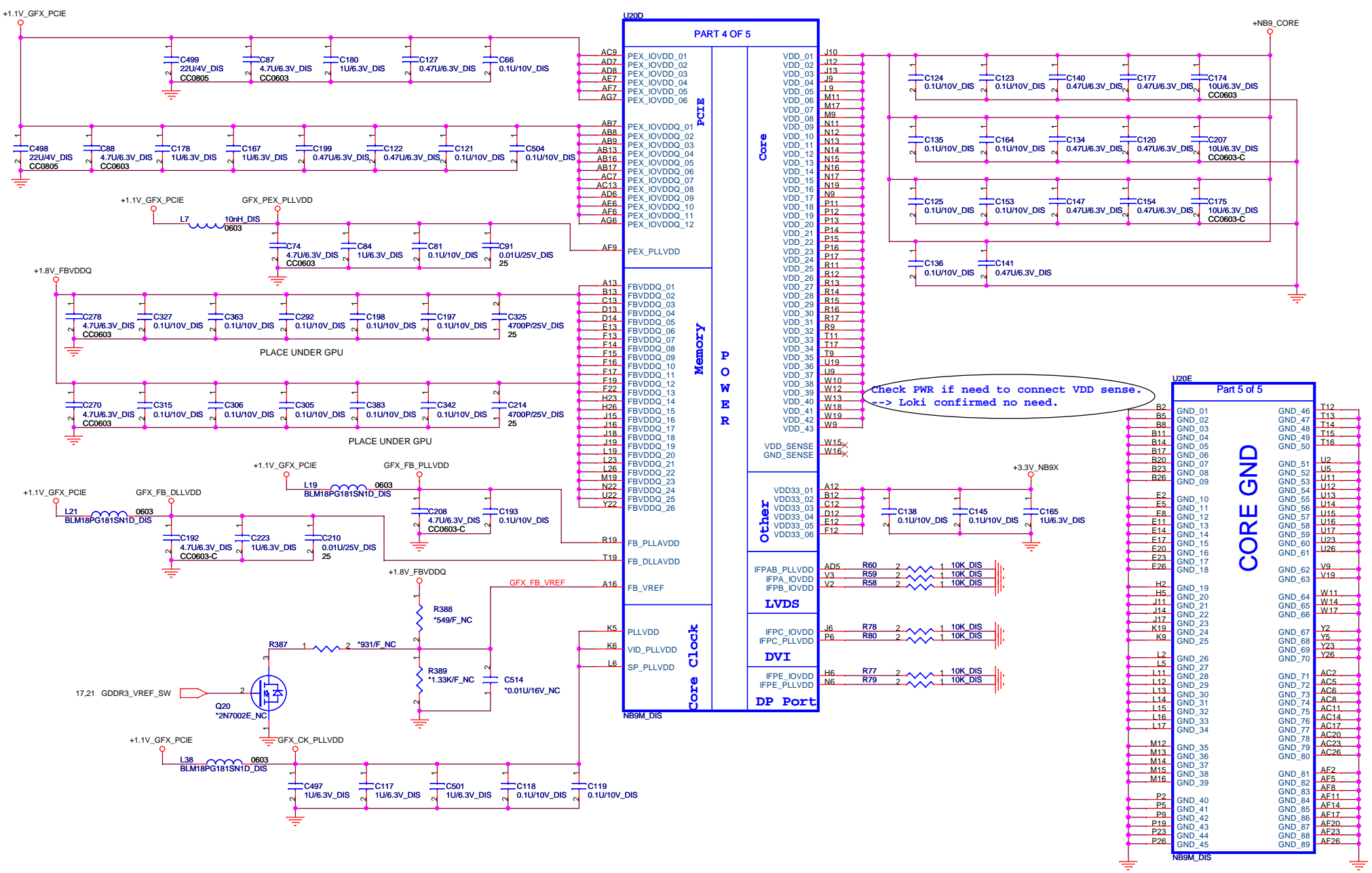
ROM_CS*
ROM_SI
ROM_SO
ROM_SCLK
I2CH_SCL
I2CH_SDA
BUFRST*


STRAP0
STRAP1
STR



0709-Steg: Change CAP Value from 18p to 22p



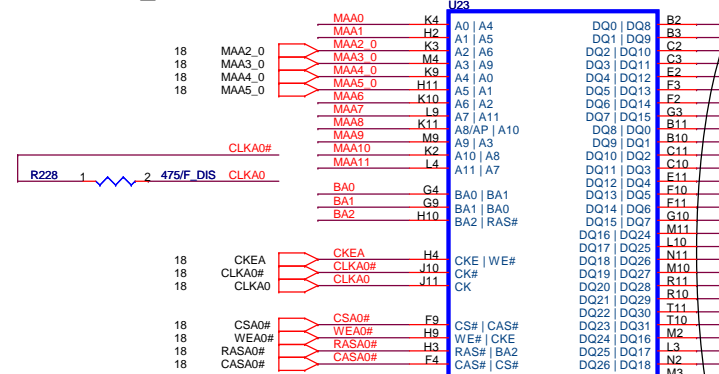




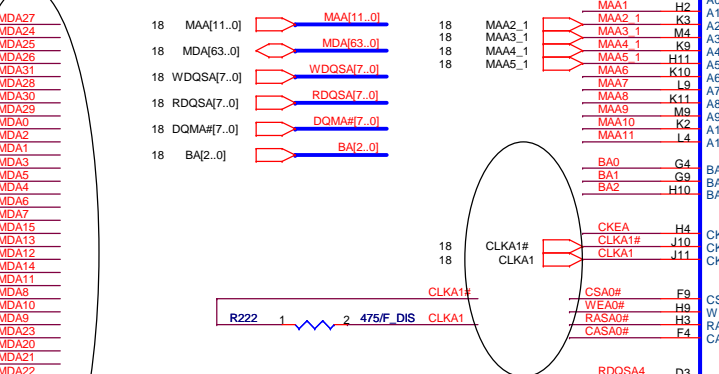
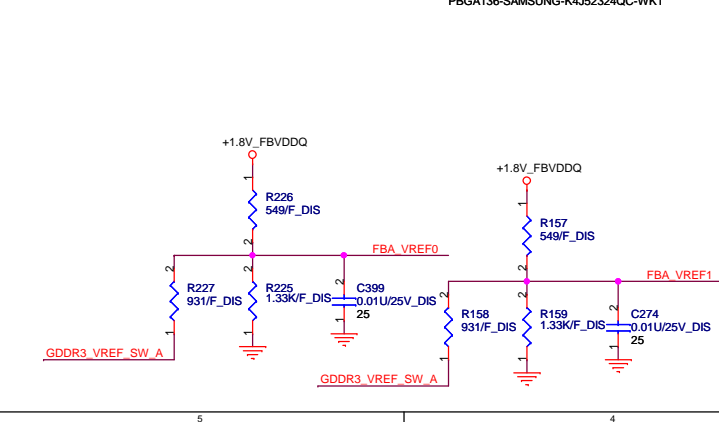
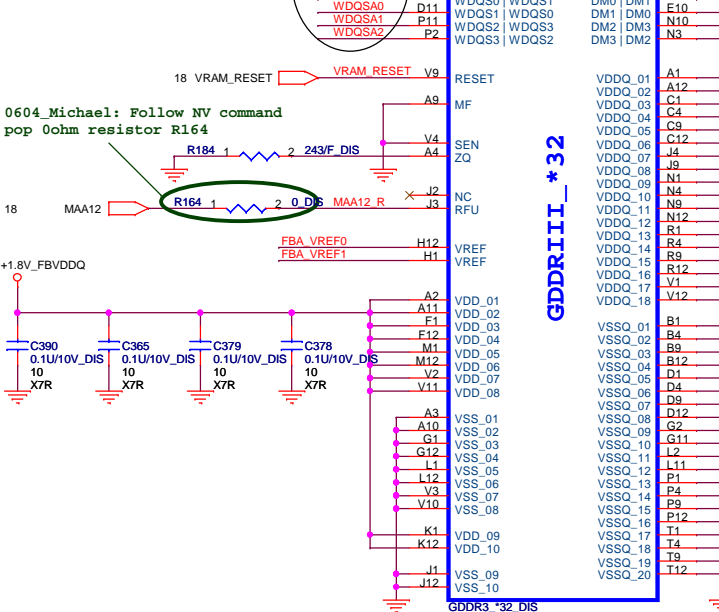
QUANTA COMPUTER

Title		
VGA-NB9X GB1-64 (POWER,GND)		
Size	Document Number	Rev
	IMS (XPS-Jolie)	2A
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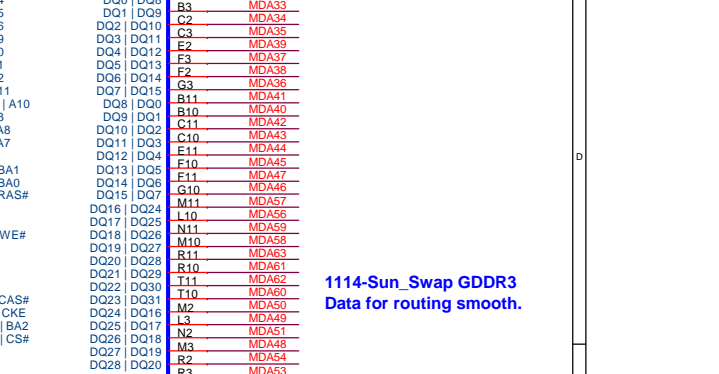
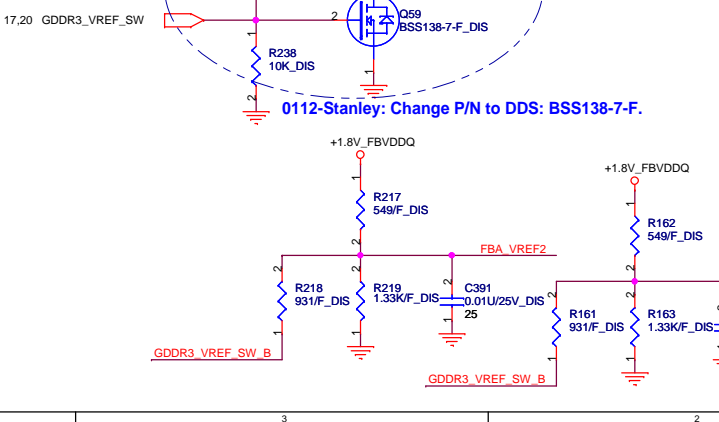
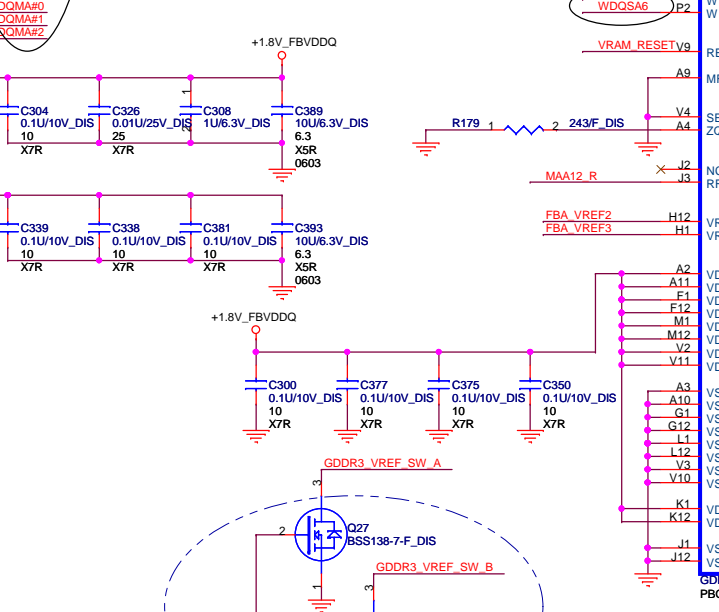
GDDR3_M*32



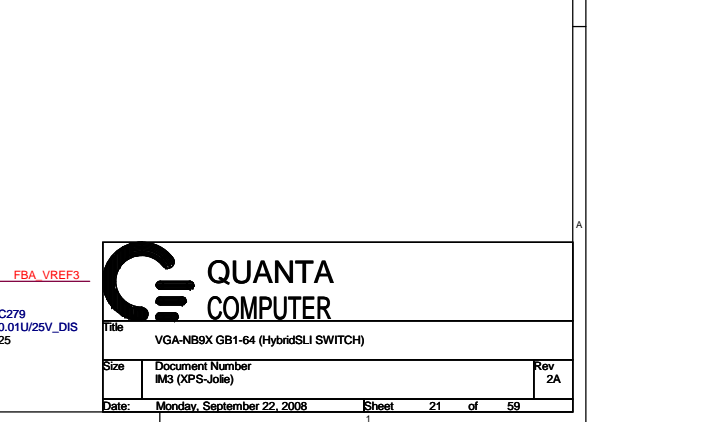
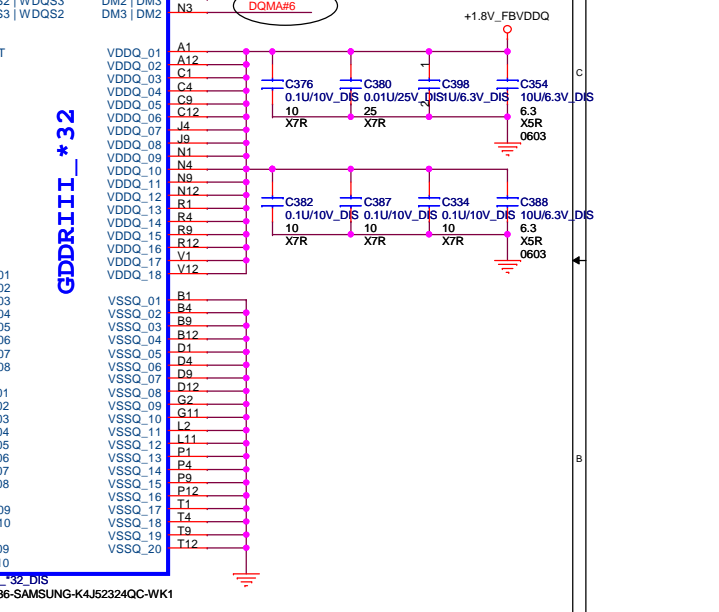
1114-Sun_Swap GDDR3
Data for routing smooth.



1114-Sun_Swap GDDR3
Data for routing smooth.



1114-Sun_Swap GDDR3
Data for routing smooth.




QUANTA COMPUTER

Title: VGA-NB9X GB1-64 (HybridSLI SWITCH)

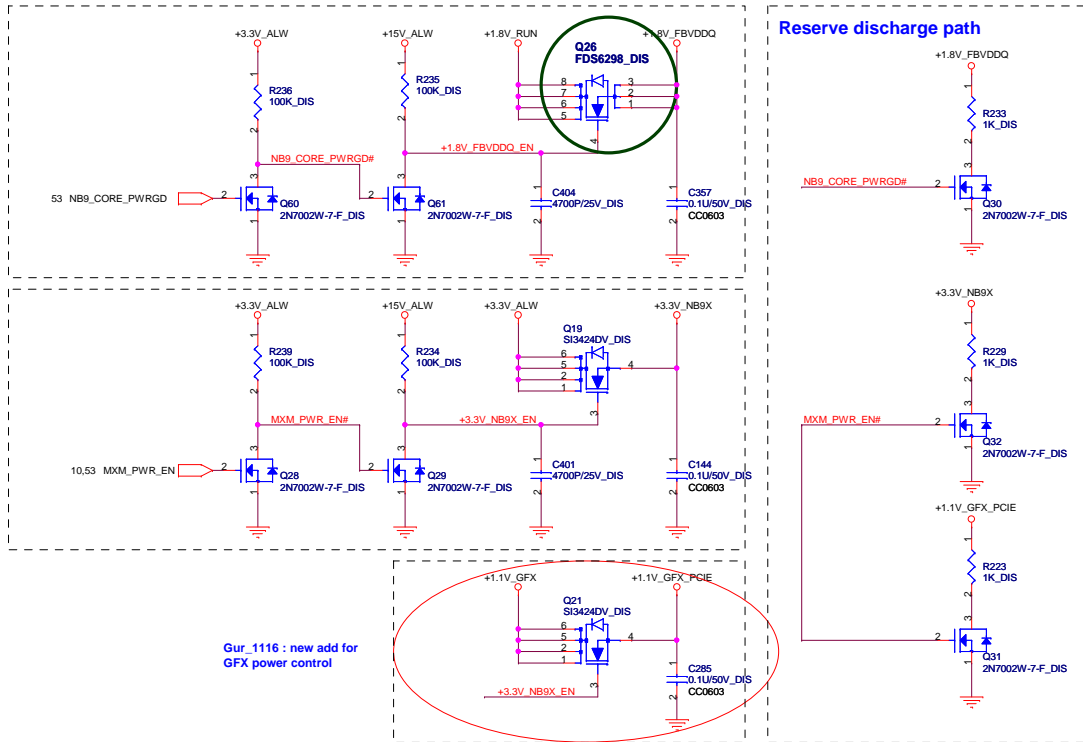
Size: Document Number IM3 (XP-S-Jolie) Rev 2A

Date: Monday, September 22, 2008 Sheet 21 of 59


**BLANK PAGE FOR PAGE
NUMBER SAME AS DISCRETE**

 QUANTA COMPUTER		
Title		
Size	Document Number IMS (XPS-Jolie)	Rev 2A
Date:	Friday, September 05, 2008	Sheet 22 of 59


1225-Sun_Change Q26 from SI4812BDY to SI4800BDY-T1-E3
 1022_Michael:Change Q26 from SI4800BDY-T1-E3 to BAM62980005



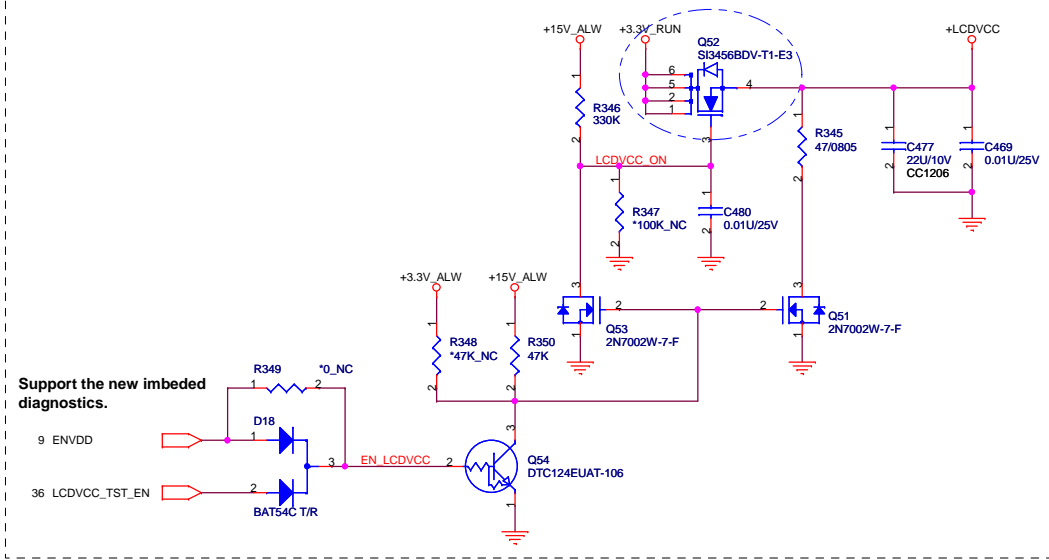
**BLANK PAGE FOR PAGE
NUMBER SAME AS DISCRETE**

 QUANTA COMPUTER		
Title		
Size	Document Number IMS (XPS-Jolie)	Rev 2A
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**BLANK PAGE FOR PAGE
NUMBER SAME AS DISCRETE**

 QUANTA COMPUTER		
Title		
Size	Document Number IMS (XPS-Jolie)	Rev 2A
Date:	Friday, September 05, 2008	Sheet 25 of 59

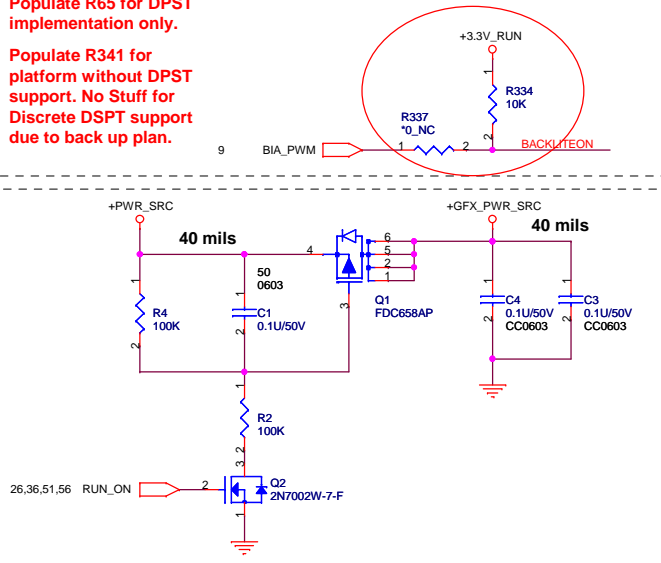
0112-Stanley: Change BOM for EOL issue (SI3456BDV).



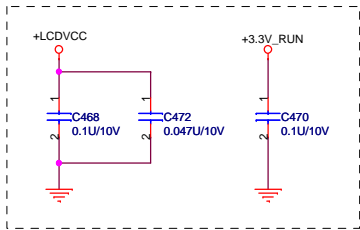
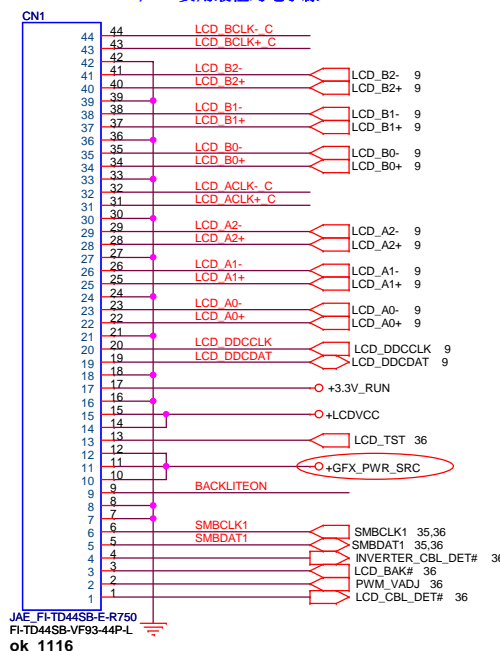
Support the new imbedded diagnostics.

Populate R65 for DPST implementation only.

Populate R341 for platform without DPST support. No Stuff for Discrete DSPT support due to back up plan.



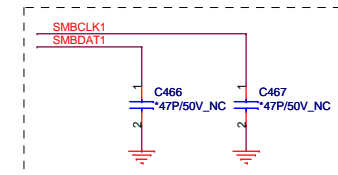
GND,VCC要用最粗的電子線



WXGA 1280*800=>70 MHz
 WXGA+ 1440*900=>108 MHz
 WSXGA+ 1680*1050=>120MHz
 WUXGA 1920*1200=>166 MHz

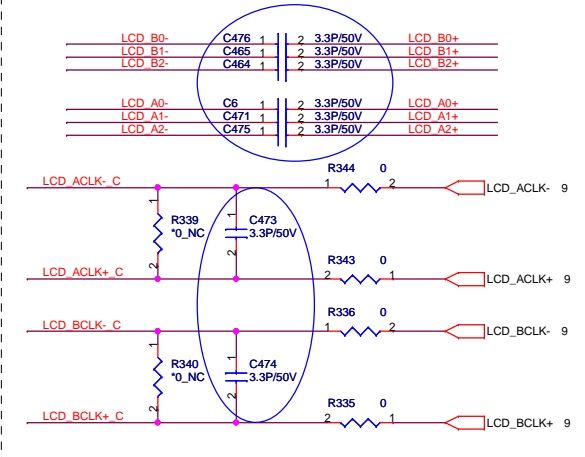
Address : A9H --Contrast
 AAH --Backlight

MBRAI specification of antenna gain is
 10dBi@474MHz, -7dBi@698MHz,
 -5dBi@858MHz.

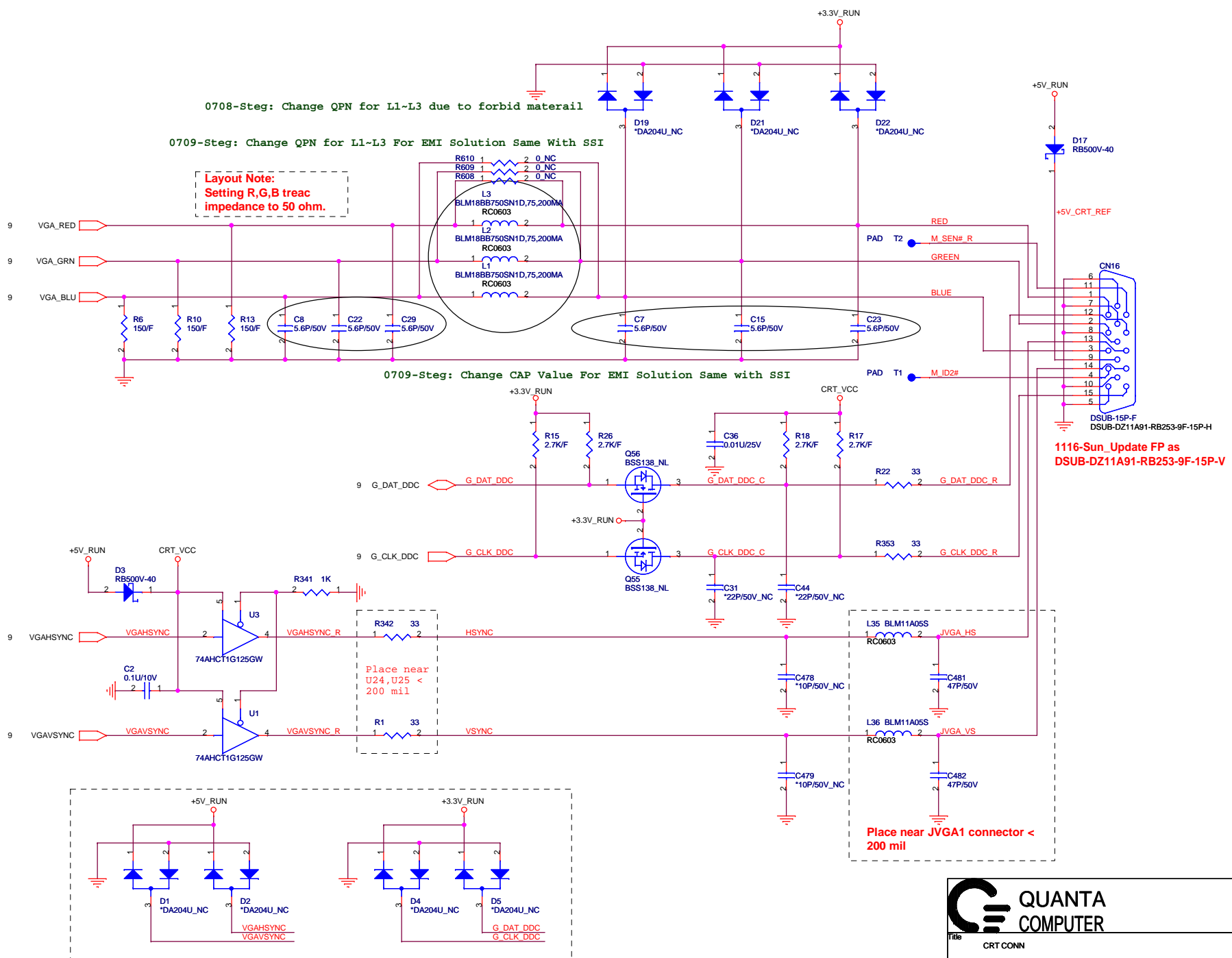


0319-Sun_Pop 3.3P on LVDS bus for COMM team demand

Shunt capacitors on LVDS for improving WWAN.



Title LCD CONN		
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Layout Note:
Setting R,G,B treac
impedance to 50 ohm.

0709-Step: Change CAP Value For EMI Solution Same with SSI

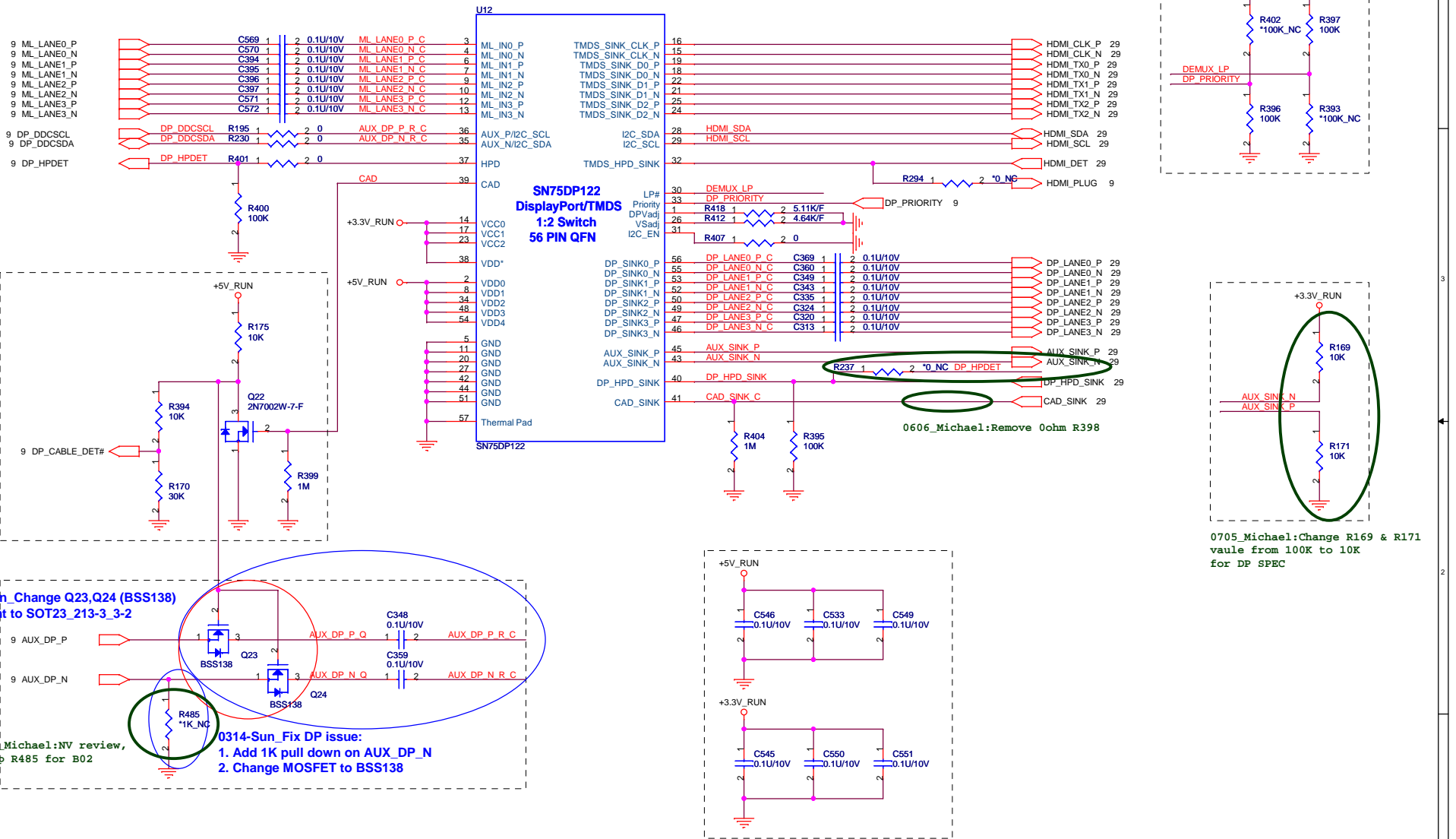
Place near
U24, U25 <
200 mil

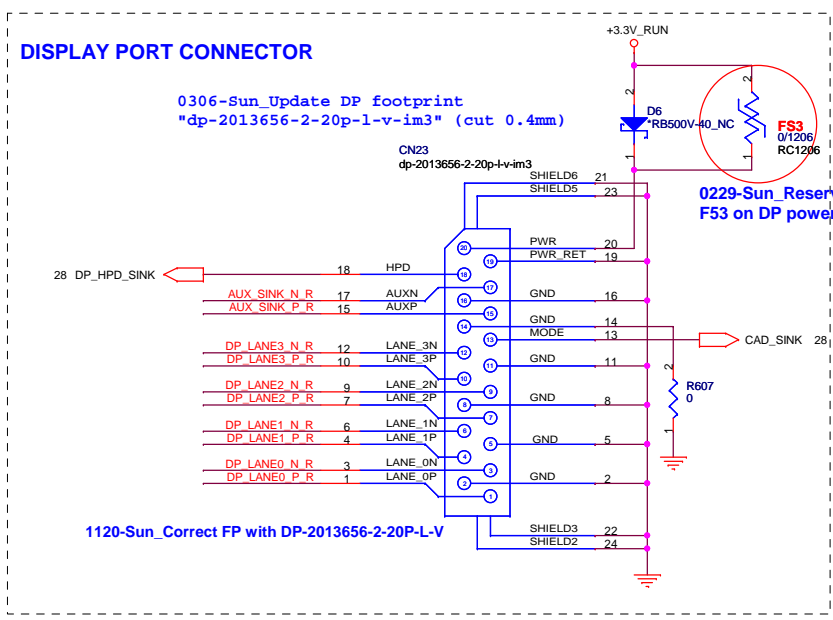
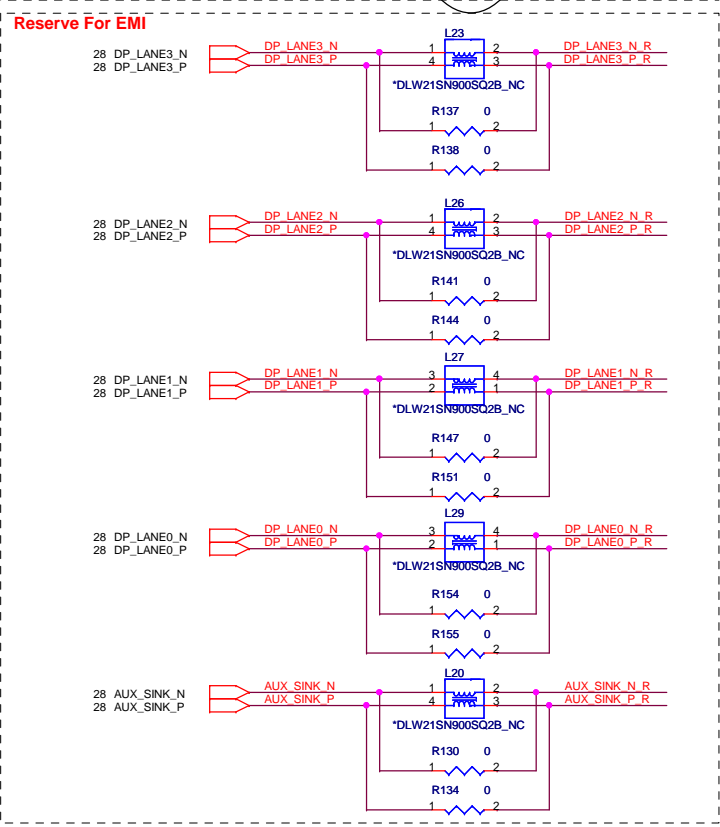
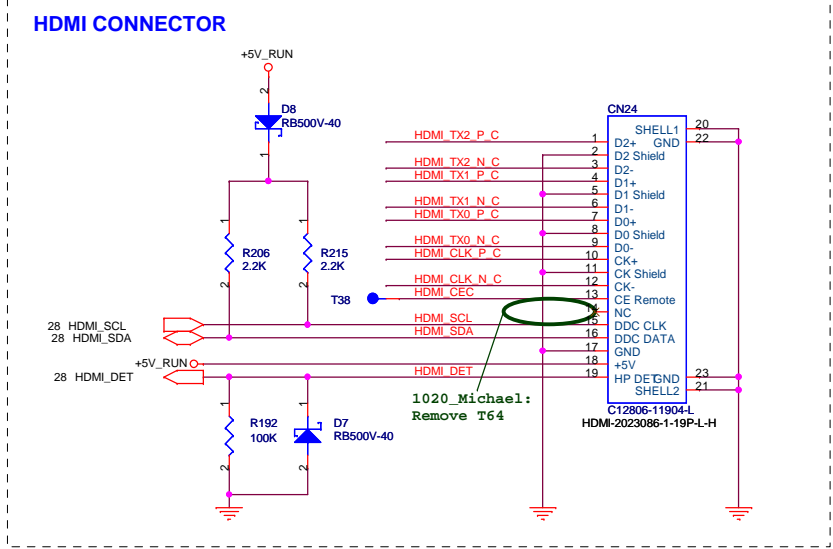
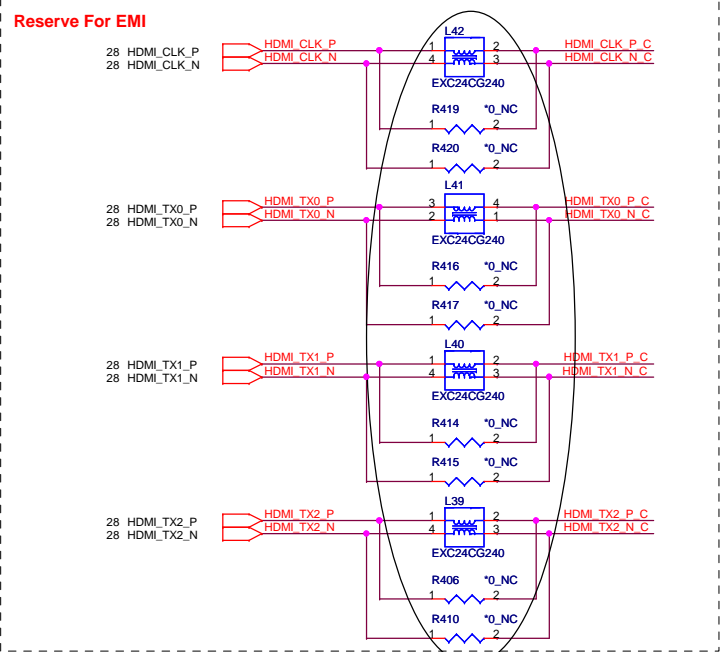
Place near JVG1 connector <
200 mil

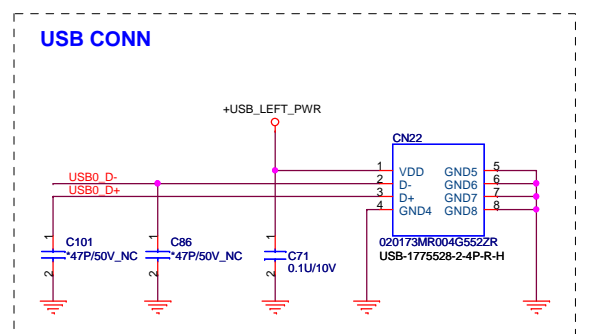
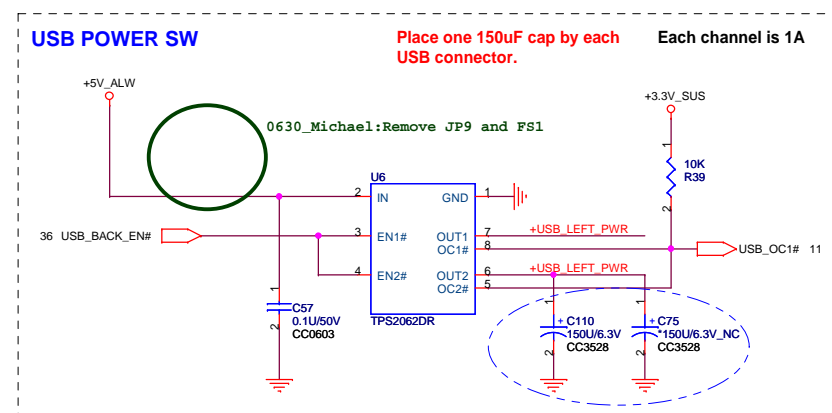
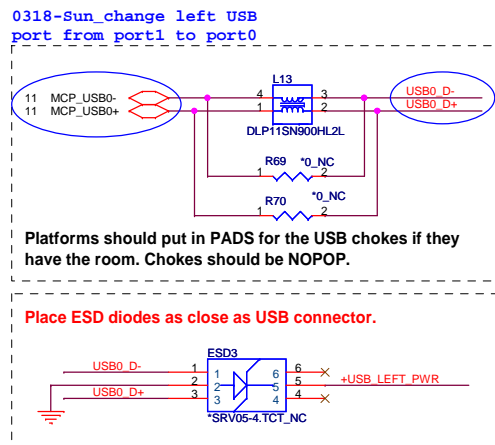
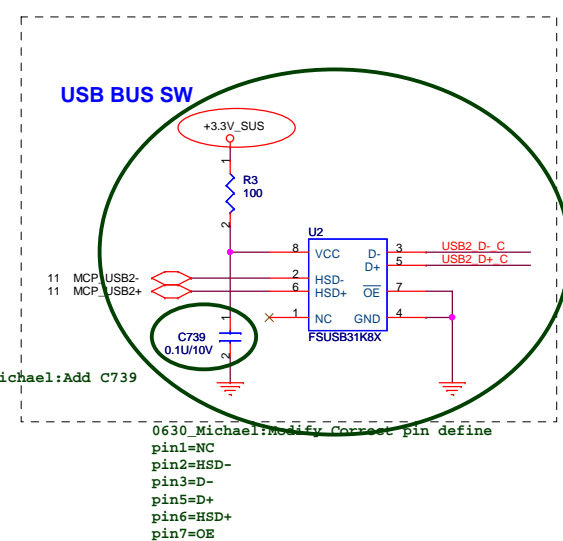
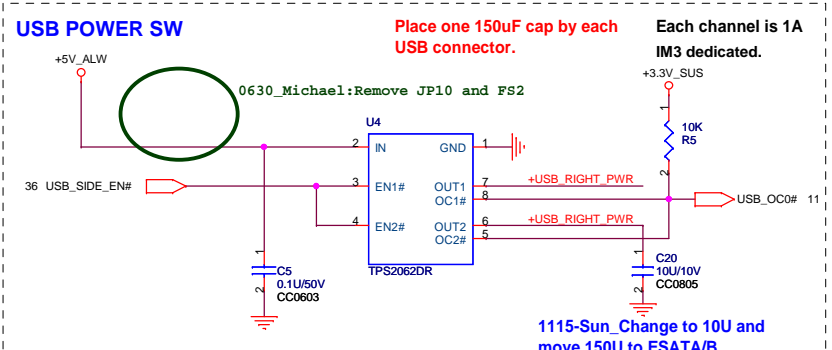
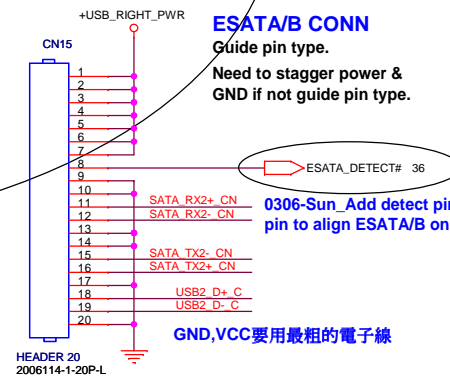
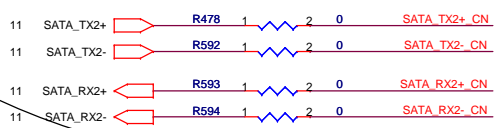
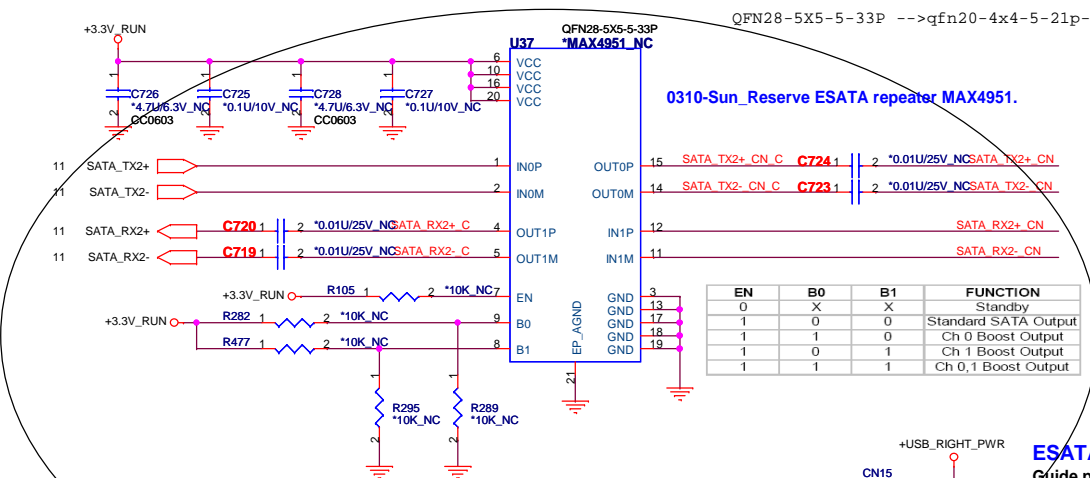
1116-Sun_Update FP as
DSUB-DZ11A91-RB253-9F-15P-H



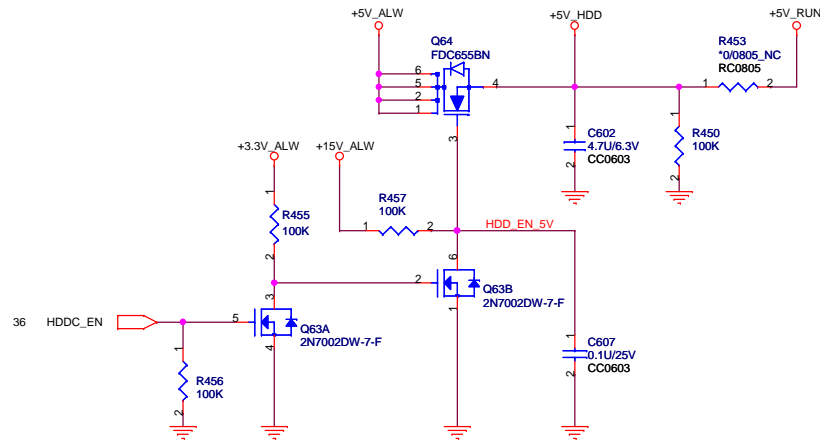
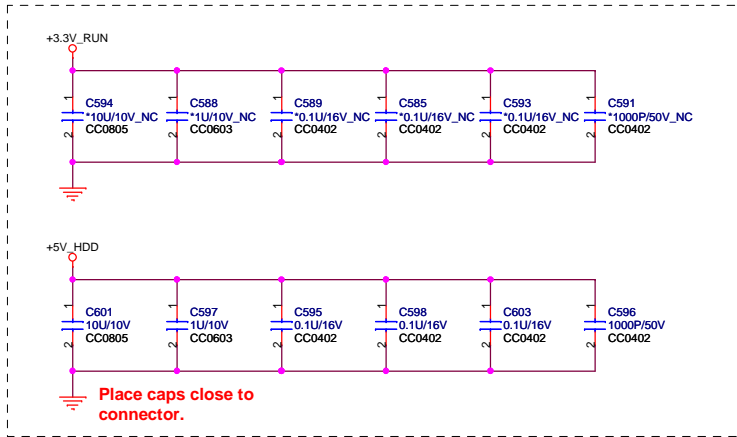
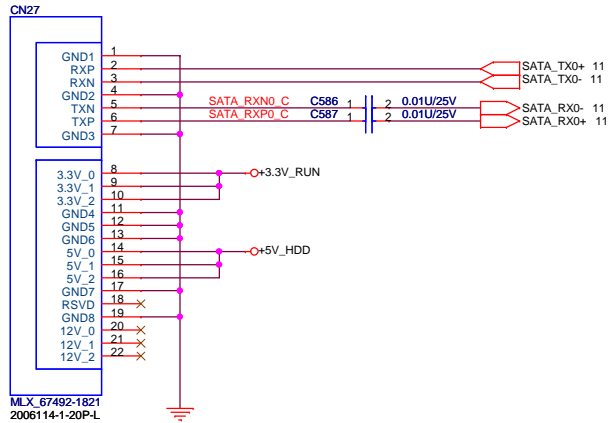
Title CRT CONN		
Size	Document Number IM3 (XPS-Jolie)	Rev 2A
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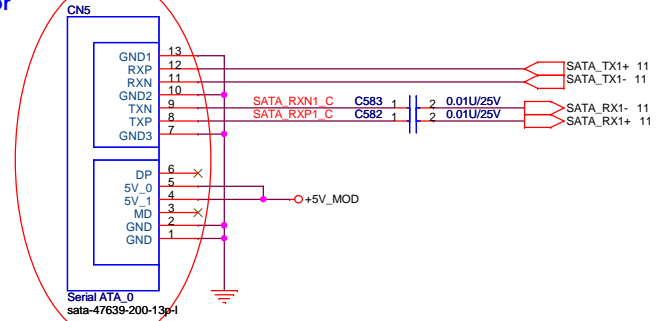




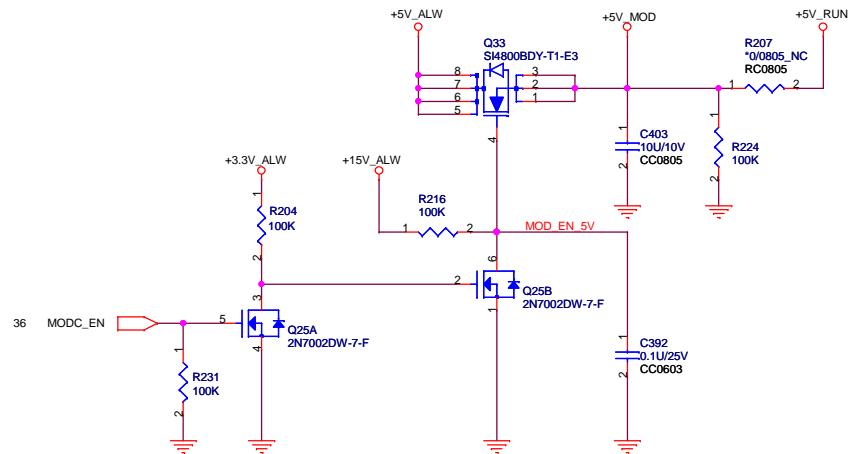
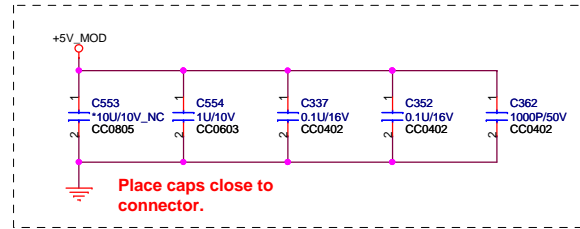
SATA HDD Connector



SATA ODD Connector

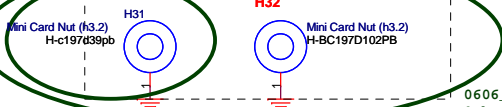


0306-Sun_Change to new footprint_sata-47639-200-13p-1
 0407-Sun_Swap pin assignment due to pin direction is reversed

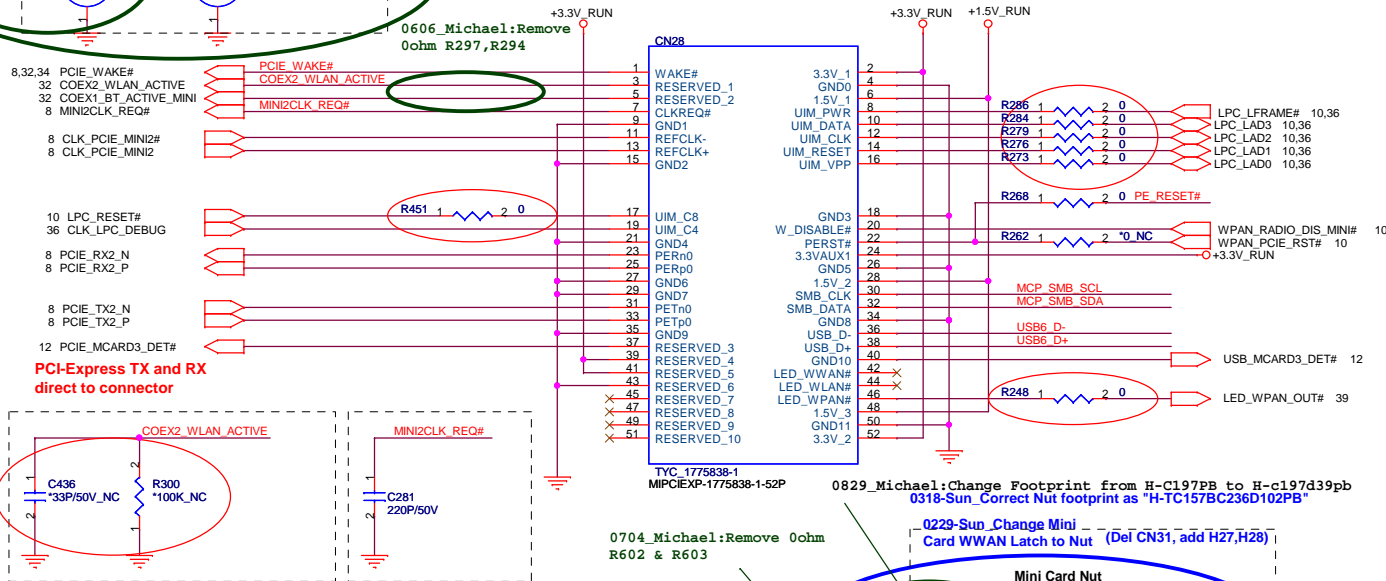


0829_Michael:Change Footprint from H-c1197PB to H-c197d39pb
 0605_Michael: Del MiniCard WPAN latch add Nut H31,H32

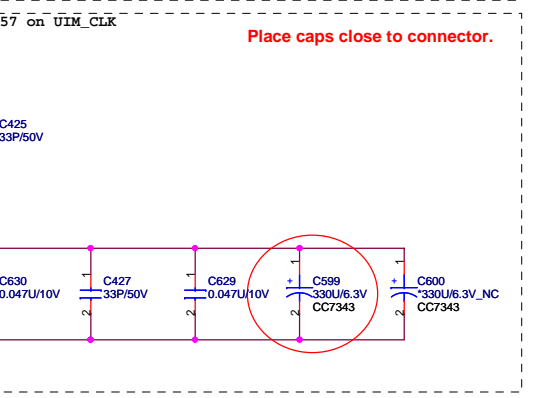
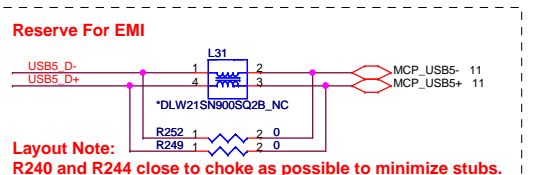
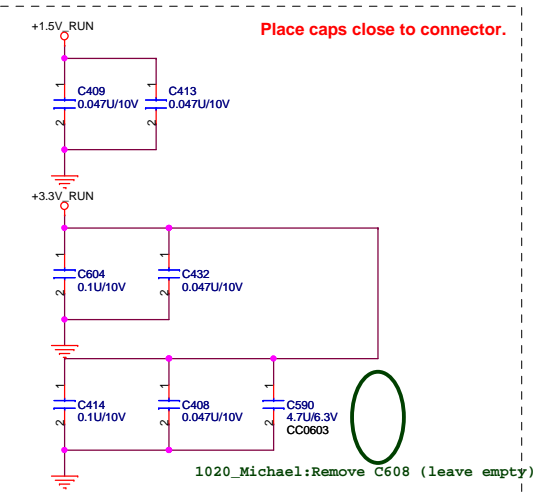
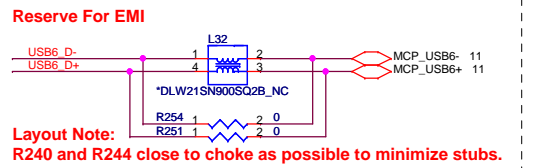
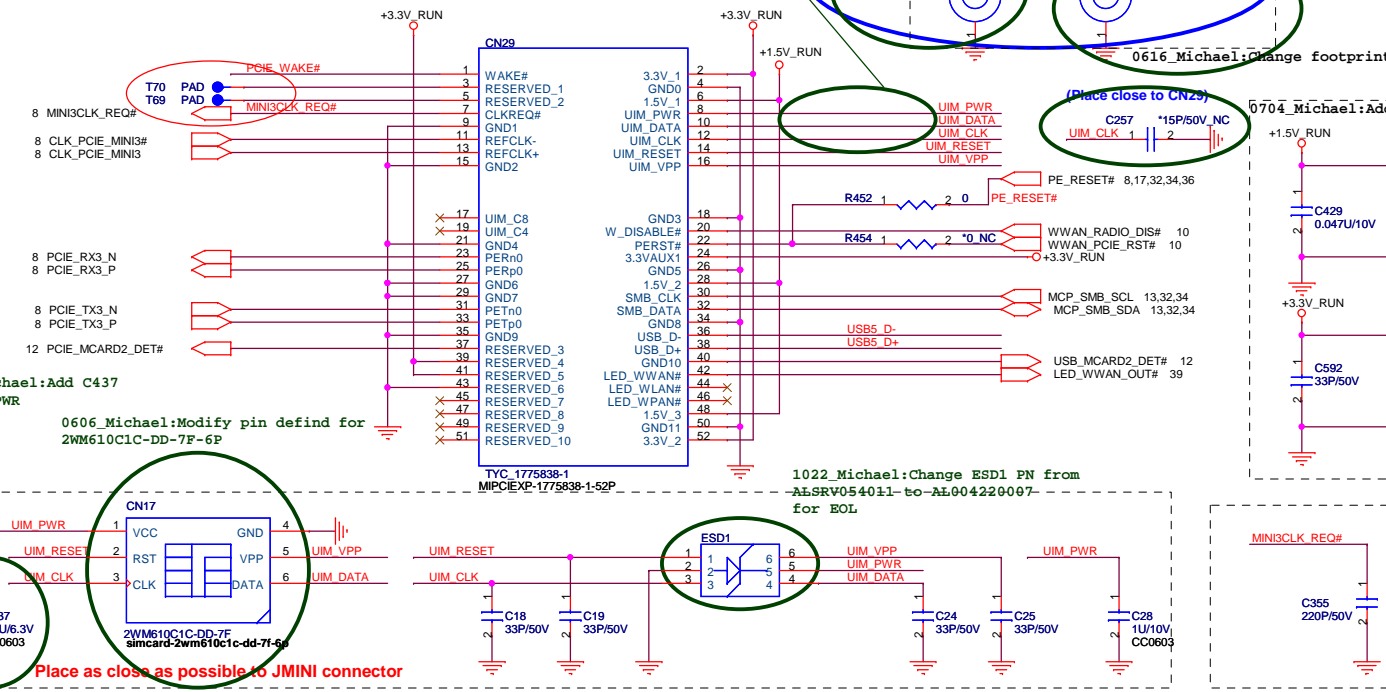
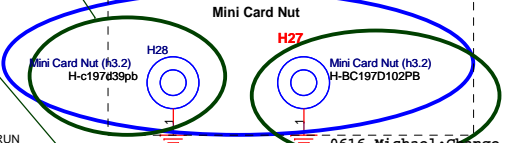
Mini Card Nut



MiniCard Robson, BT. UWB Connector



MiniCard WWAN Connector



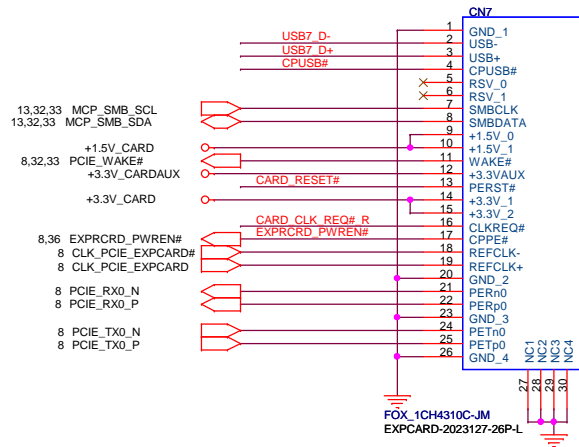
QUANTA COMPUTER

Title: MINI-CARD (WWAN,WPAN)

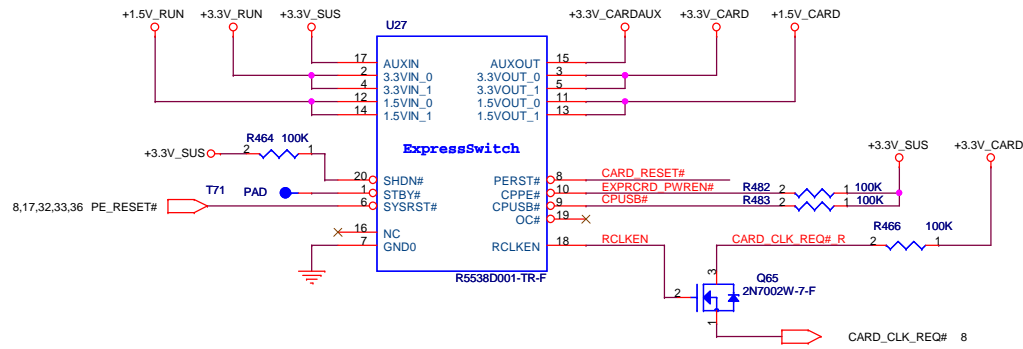
Size: Document Number IM3 (XPS-Jolie) Rev 2A

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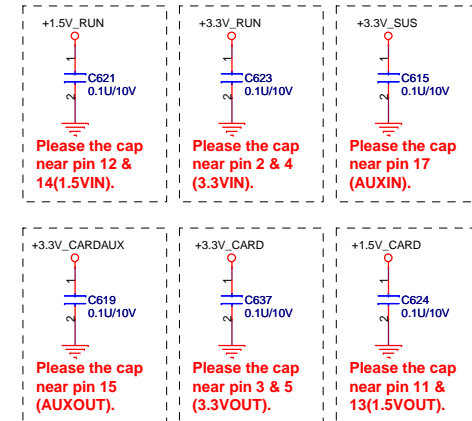
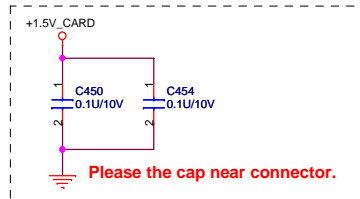
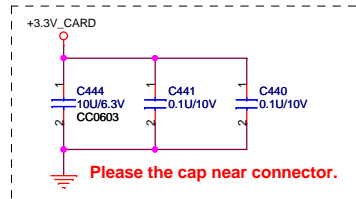
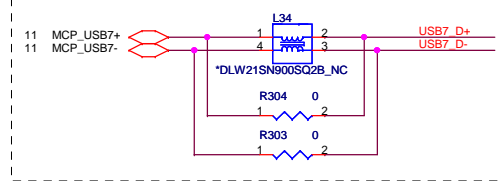
Express Card

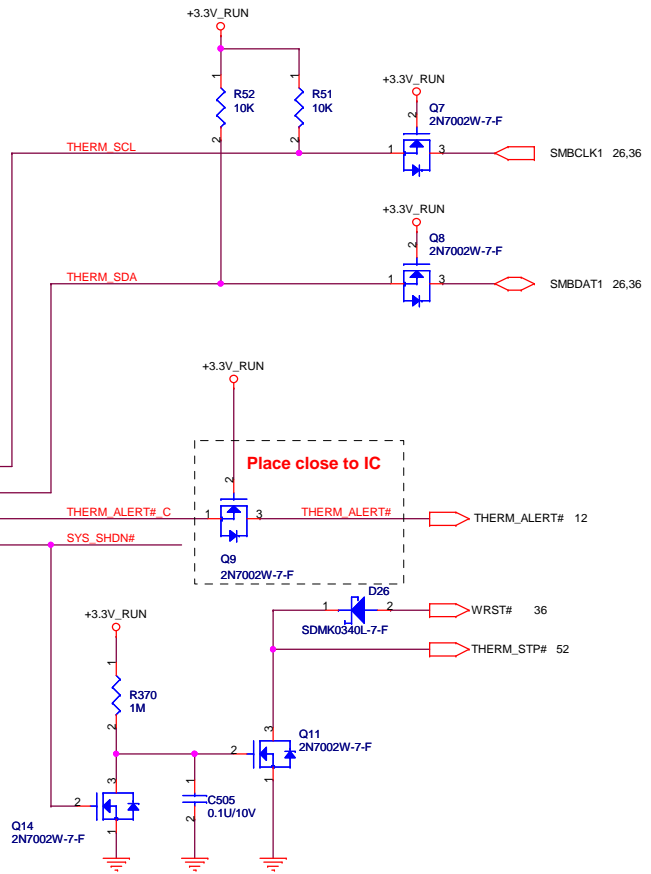
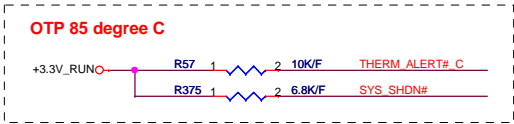
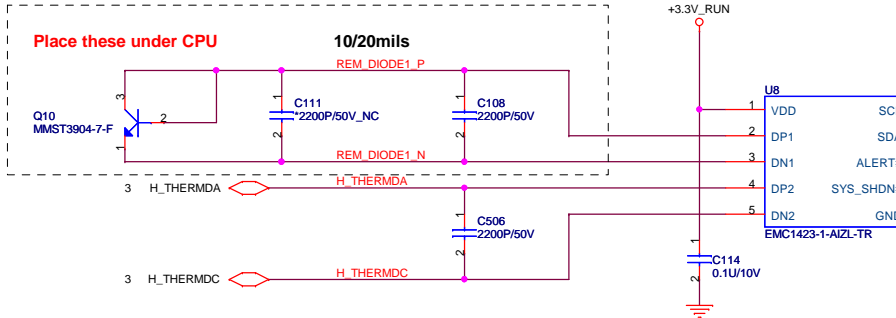
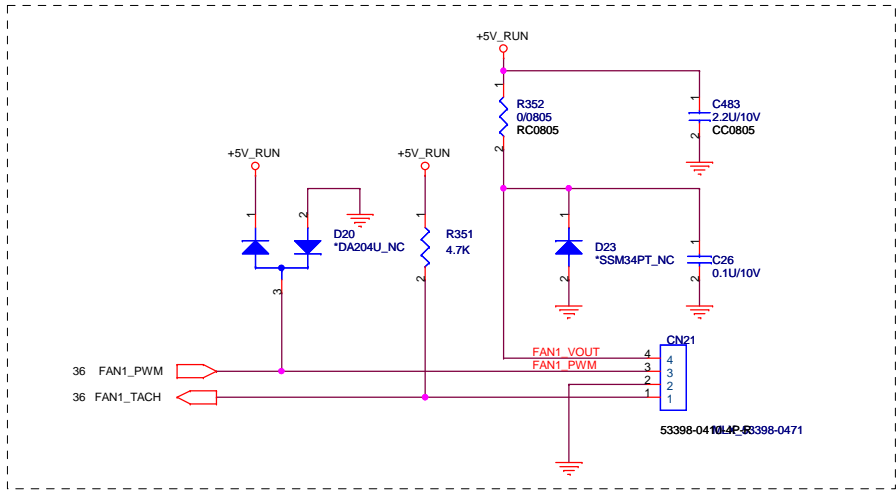


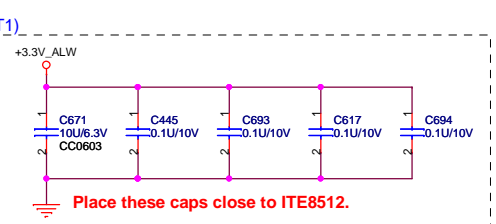
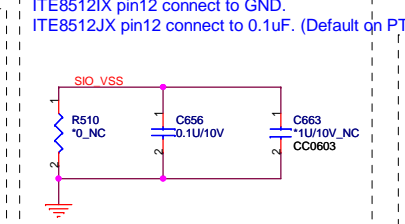
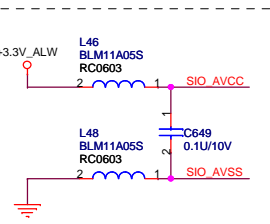
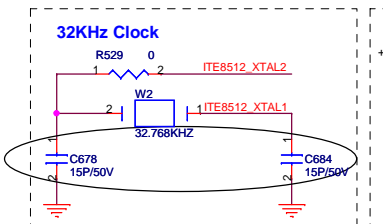
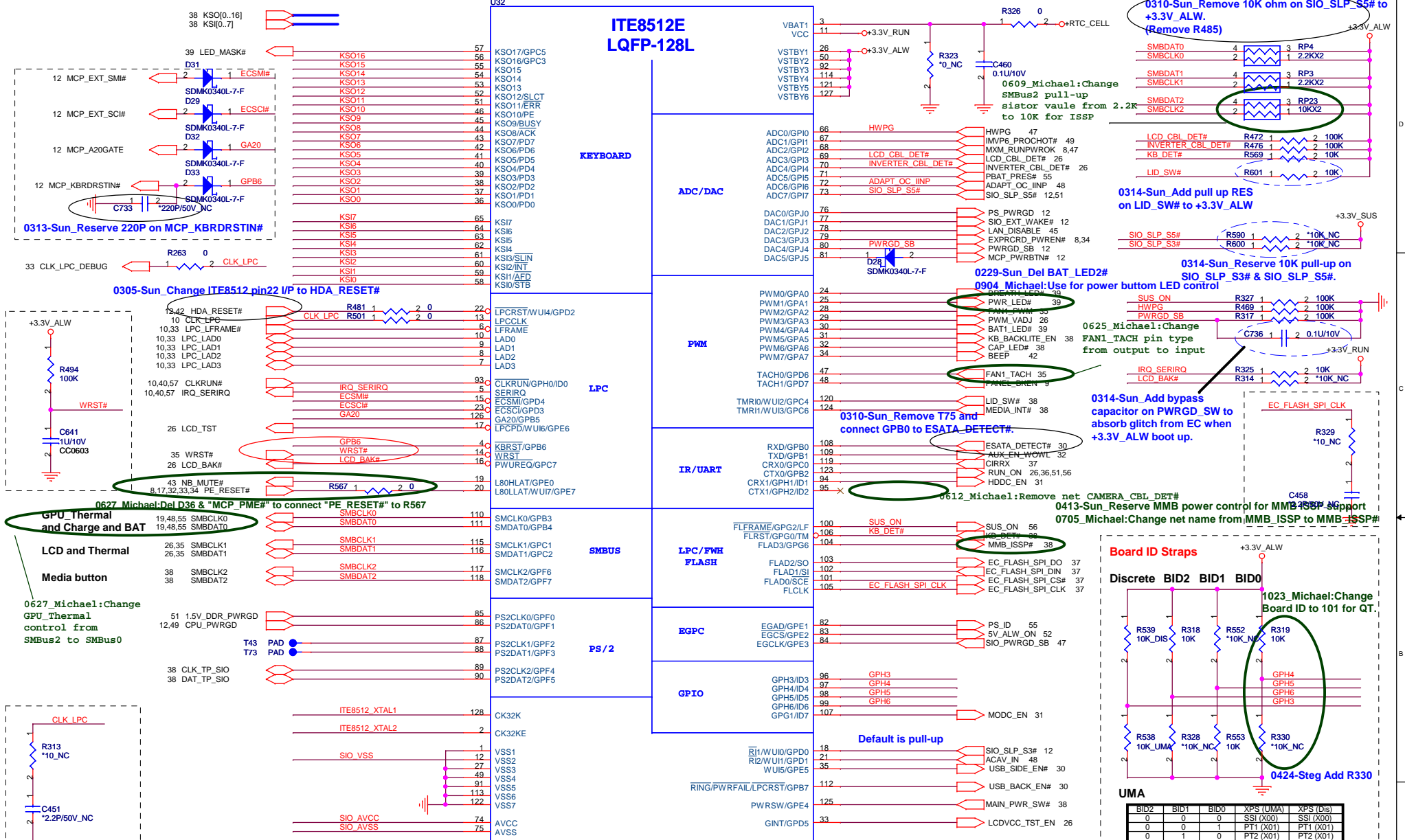
+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.



PCI-Express TX and RX direct to connector.







0709-Steig: Change CAP value from 10p to 15p

QUANTA COMPUTER

Title: SIO(ITE8512)

Size: Document Number IM3 (XPS-Joie)

Date: Thursday, October 23, 2008

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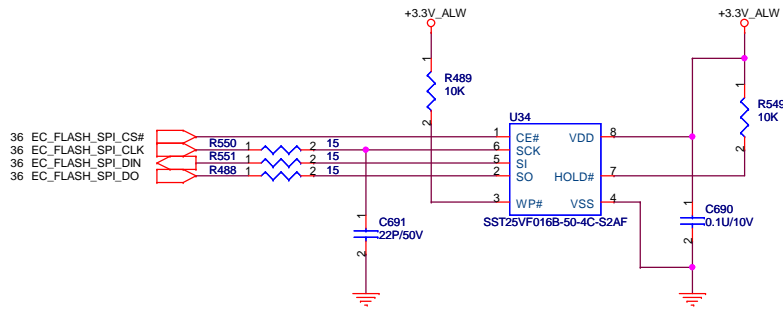
Rev: 2A

UMA

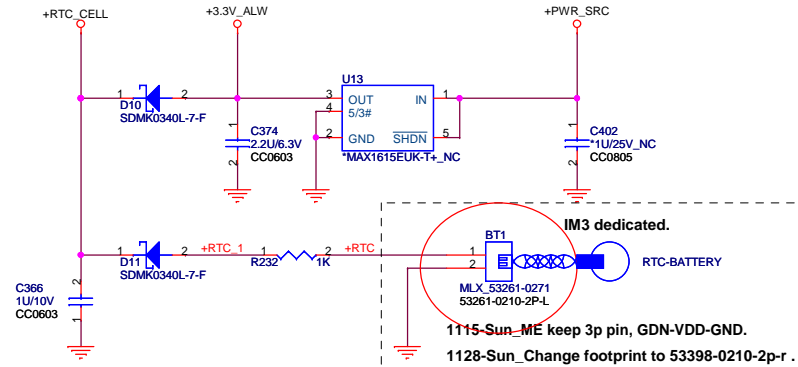
BID2	BID1	BID0	XPS (UMA)	XPS (DS)
0	0	0	SSI (X01)	SSI (X01)
0	0	1	PT1 (X01)	PT1 (X01)
0	1	0	PT2 (X01)	PT2 (X01)
0	1	1	ST (X02)	ST (X02)
1	0	0	ST2 (X02)	ST2 (X02)
1	0	1	QT (A00)	QT (A01)

VGA_IDENTIFY : USB_SIDE_EN#
1 = Discrete Gfx / 0 = UMA

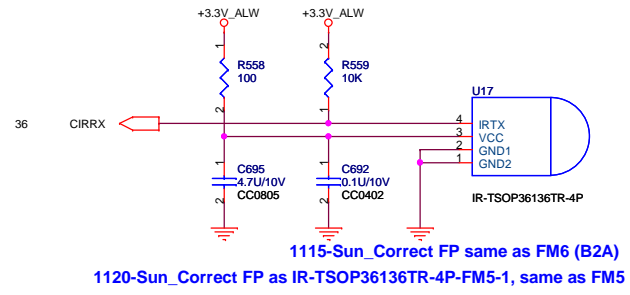
16Mbit (2M Byte), SPI



RTC BATTERY



Consumer IR



0605_Michael: Change CN6 from 32pin to 28pin but need to check footprint and PN

BREATH_PWRLED_BOT:

Solid = System On, Normal Activity; "Breathing" = System in Standby; Off = System Off (or in Hibernate)

0920_Michael: Add KB detect function
 1023_Michael: Disable KB_LED function
 depop R722 and change R723 from 200K to 0 ohm

Power Button

Speaker

KB LED

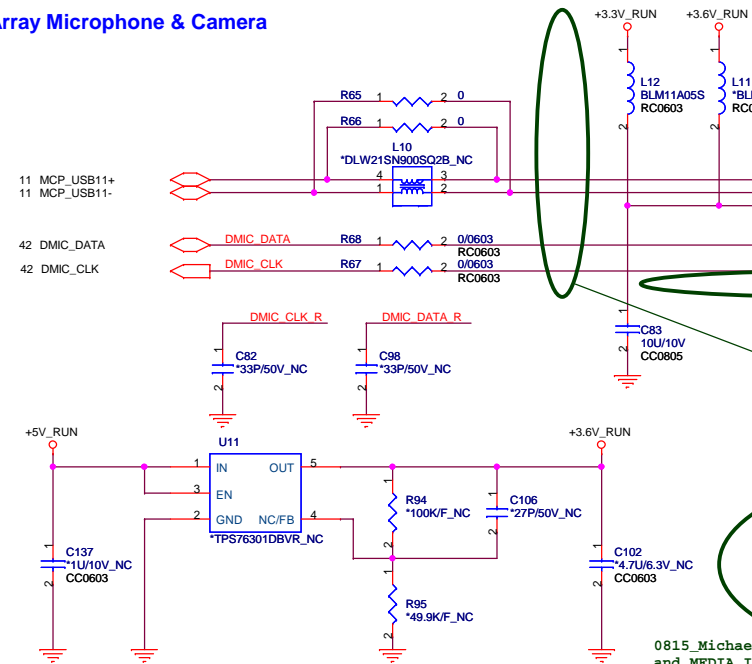
Touch Pad

Media Button

0624_Michael: Change net name from +5V_ALW2 to +MMB_PWR
 0704_Michael: Swap SMBCLK2 and +MMB_PWR for Ass'y issue

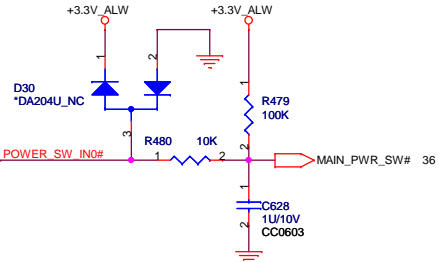
0825_Michael: Add KB detect function
 0911_Michael: Change pin from 16 to 8
 0918_Michael: Return to LID_SW#

Array Microphone & Camera

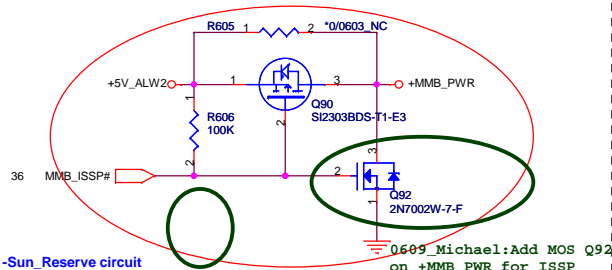


0815_Michael: Add Hall Switch circuit and MEDIA_INT# pull-high at MB side

Power Button



0909_Michael: Remove LID_SW# and connector to GND



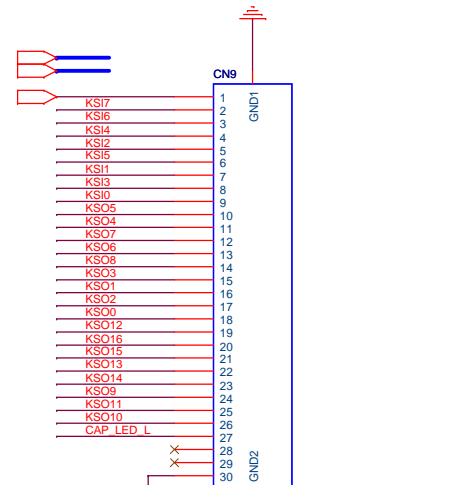
0411-Sun_ Reserve circuit for MMB ISSP support
 0414-Sun_ Change MOSFET control voltage level

0609_Michael: Add MOS Q92 on +MMB_PWR for ISSP

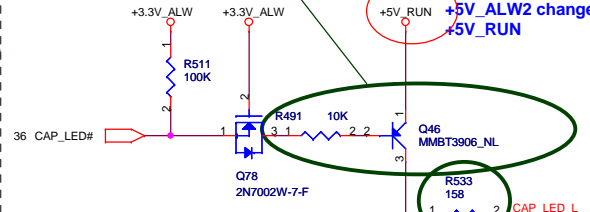
0701_Michael: Remove Q91 for ISSP

KEYBOARD CONNECTOR

36 KSI0[0..16]
 36 KSI0[0..7]



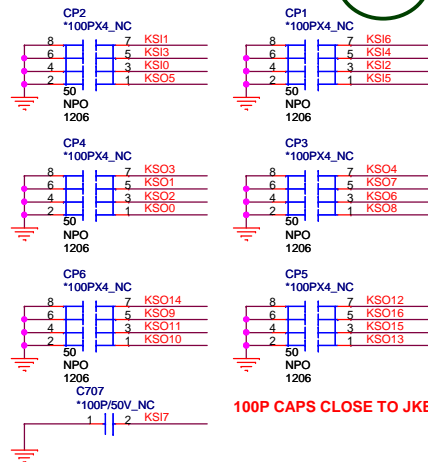
0701_Michael: Remove Q80 and add Q46 & R491 for leakage issue on S3



0310-Sun_CAP_LED +5V_ALW2 change to +5V_RUN

R533 158

1022_Michael: Change R533 from 2.49K to 158ohm for LED brightness



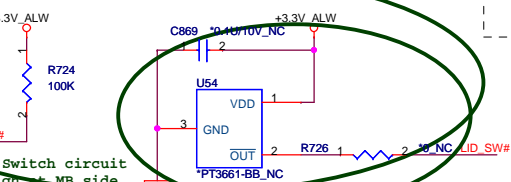
100P CAPS CLOSE TO JKB1

GND,VCC要用最粗的电子线

0306-Sun_Change CCD connector to 10pin

0612_Michael: Remove CAMERA DET circuit, R64 pull-up to +3.3V_RUN and connector to U32 pin95

Hall Switch



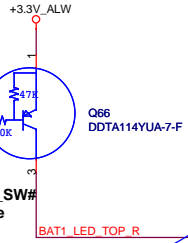
1023_Michael: Depop LID_Switch function on MB side



Title USER INTERFACE/ CIR		
Size	Document Number IM3 (XPS-Jolie)	Rev 2A
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Battery status

0313-Sun_Change battery LED to Amber (3.3V drive) (Remove Q68, R462, R460)



0606_Michael:Add R462 connect to CN2 on BAT1_LED

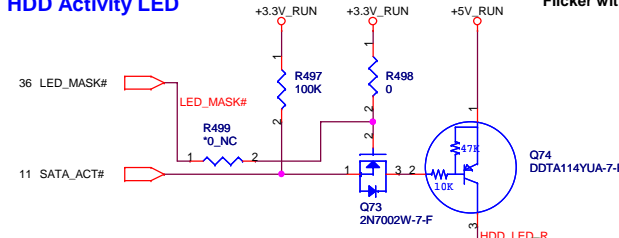


0922_Michael:Remove BAT1_AMB_LED function

0229-Sun_Del BAT_LED2 [Del R295,Q48,Q43 (2N7002) and Q46,Q47 (DDTA114YUA)]

HDD Activity LED

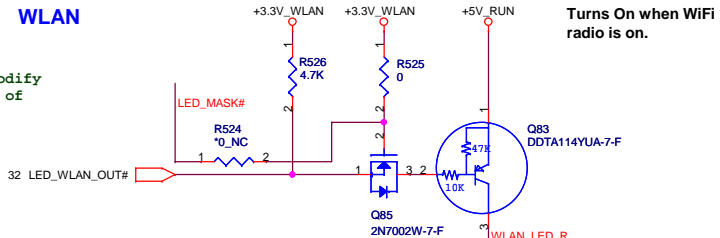
Flicker with HDD activity.



1022_Michael:Change R500 from 2.49K to 169ohm for LED brightness

WLAN

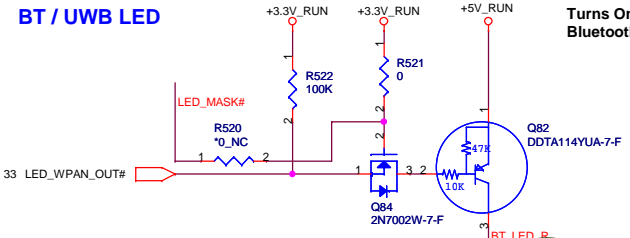
Turns On when WiFi radio is on.



1022_Michael:Change R523 from 2.49K to 169ohm for LED brightness

BT / UWB LED

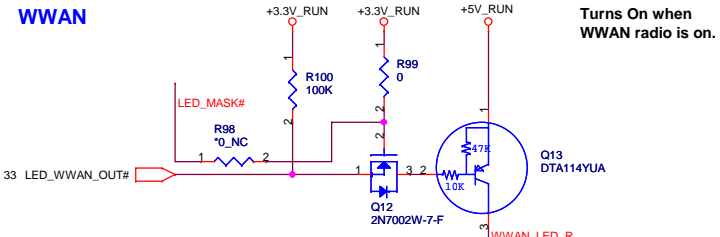
Turns On when Bluetooth radio is on.



1022_Michael:Change R519 from 2.49K to 169ohm for LED brightness

WWAN

Turns On when WWAN radio is on.



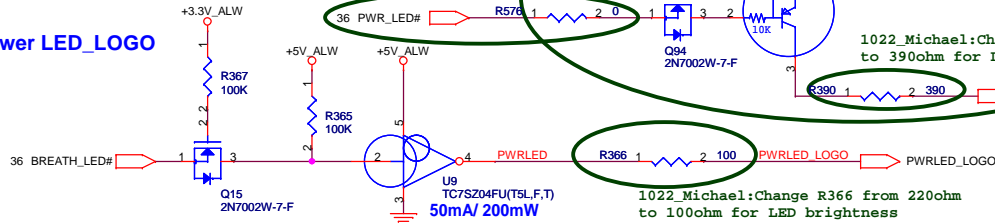
1022_Michael:Change R97 from 2.49K to 169ohm for LED brightness

0229-Sun_Remove BAT_LED controlled by LID_SW# [Del Q69 (2N7002), Q67 (DDTA114YUA); change R462 from 220 to 10K]

Power LED_LOGO

0229-Sun_Change PWRLED_SW control same as PWRLED_LOGO [Del U10 (TC7S204F), Q16 (2N7002)]

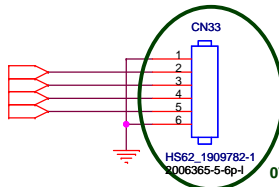
0904_Michael:Add R576 and onnector to PWR_LED# from ITE8512



1022_Michael:Change R366 from 220ohm to 100ohm for LED brightness

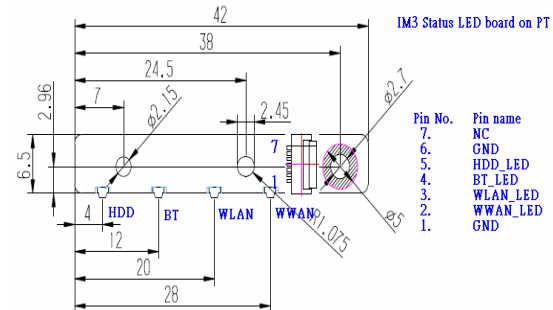
0618_Michael:Follow DELL command modify circuit to change the LED behavior of Power button

1022_Michael:Change R390 from 1K to 390ohm for LED brightness



0704_Michael:Change CN33 pin number from 7pin to 6pin and also change type from HEADER7 to HS62_1909782-1 for cost down

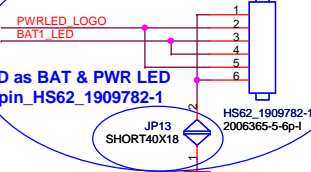
0229-Sun_Remove LED control by LID_SW# (Del R478,R477,Q75)



IM3 Status LED board on PT

Pin No.	Pin name
7.	NC
6.	GND
5.	HDD_LED
4.	BT_LED
3.	WLAN_LED
2.	WWAN_LED
1.	GND

Logo LED/B connector



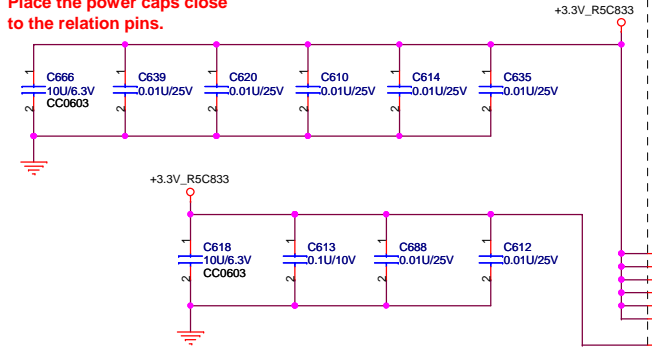
0306-Sun_Change Logo LED as BAT & PWR LED and change connector to 6pin_HS62_1909782-1

0314-Sun_Add short pad on GND of Logo LED/B connector for EMI request.

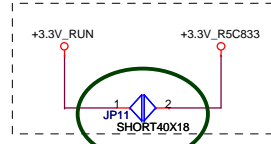
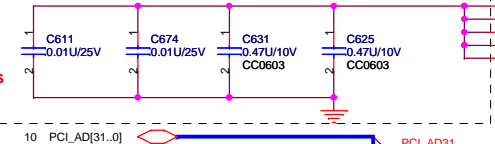


Title		LED
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	IM3 (XPS-Jolie)	2A
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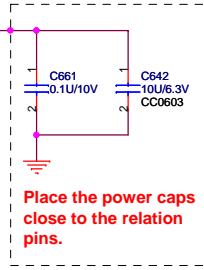
Place the power caps close to the relation pins.



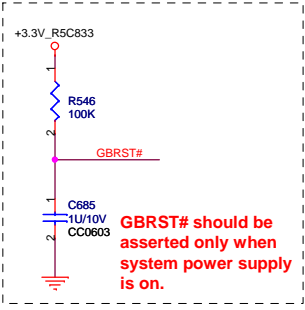
Please place capacitors for VCC_ROUTx as close to R5C833 as possible.



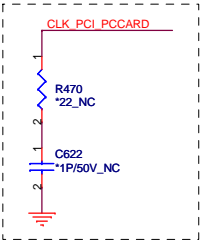
0606_Michael:Change footprint from 0ohm R468 to normal short type JP11 (short40x18)



Place the power caps close to the relation pins.



GBRST# should be asserted only when system power supply is on.



- 10 PCI_PAR
- 10 PCI_C_BE3#
- 10 PCI_C_BE2#
- 10 PCI_C_BE1#
- 10 PCI_C_BE0#

- 10 PCI_REQ0#
- 10 PCI_GNT0#
- 10 PCI_FRAME#
- 10 PCI_IRDY#
- 10 PCI_TRDY#
- 10 PCI_DEVSEL#
- 10 PCI_STOP#
- 10 PCI_PERR#
- 10 PCI_SERR#

- 10 PCI_RST#
- 10 CLK_PCI_PCCARD
- 10 PCI_PME#
- 10,36 CLKRUN#

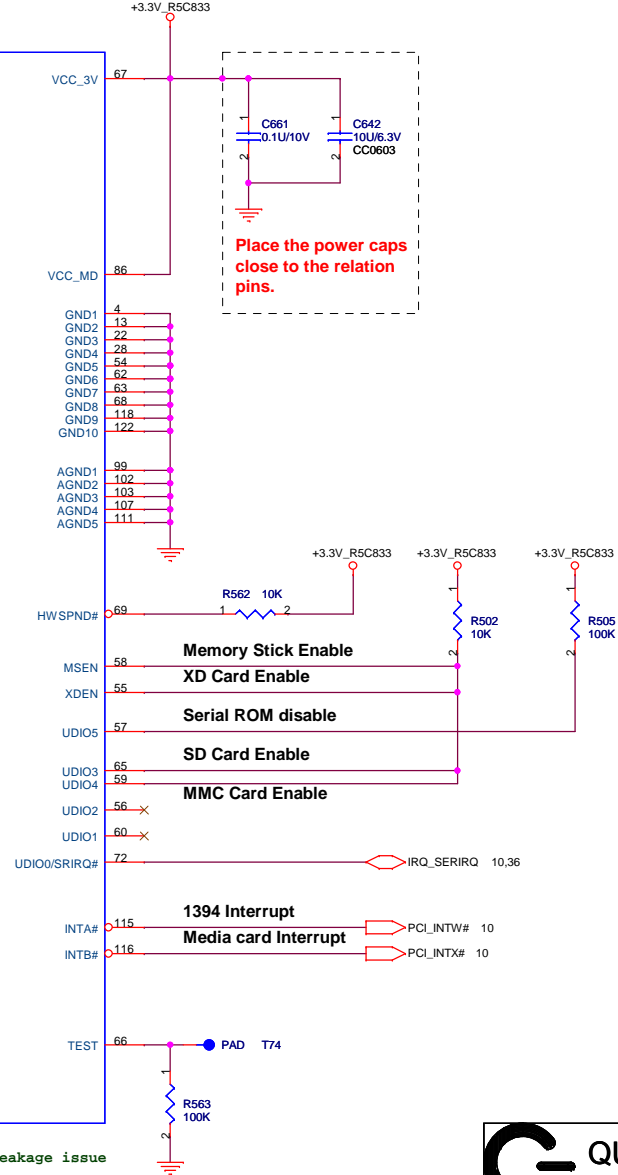
- PCI AD31 125 AD31
- PCI AD30 126 AD30
- PCI AD29 127 AD29
- PCI AD28 1 AD28
- PCI AD27 2 AD27
- PCI AD26 3 AD26
- PCI AD25 5 AD25
- PCI AD24 6 AD24
- PCI AD23 9 AD23
- PCI AD22 11 AD22
- PCI AD21 12 AD21
- PCI AD20 14 AD20
- PCI AD19 15 AD19
- PCI AD18 17 AD18
- PCI AD17 18 AD17
- PCI AD16 19 AD16
- PCI AD15 36 AD15
- PCI AD14 37 AD14
- PCI AD13 38 AD13
- PCI AD12 39 AD12
- PCI AD11 40 AD11
- PCI AD10 42 AD10
- PCI AD9 43 AD9
- PCI AD8 44 AD8
- PCI AD7 46 AD7
- PCI AD6 47 AD6
- PCI AD5 48 AD5
- PCI AD4 49 AD4
- PCI AD3 50 AD3
- PCI AD2 51 AD2
- PCI AD1 52 AD1
- PCI AD0 53 AD0

- PAR 33 PAR
- C/BE3# 7 C/BE3#
- C/BE2# 21 C/BE2#
- C/BE1# 35 C/BE1#
- C/BE0# 45 C/BE0#
- IDSEL 8 IDSEL

- REQ# 124 REQ#
- GNT# 123 GNT#
- FRAME# 23 FRAME#
- IRDY# 24 IRDY#
- TRDY# 25 TRDY#
- DEVSEL# 26 DEVSEL#
- STOP# 29 STOP#
- PERR# 30 PERR#
- SERR# 31 SERR#

- GBRST# 71 GBRST#
- PCIRST# 119 PCIRST#
- PCICLK 121 PCICLK
- PME# 70 PME#
- CLKRUN# 117 CLKRUN#

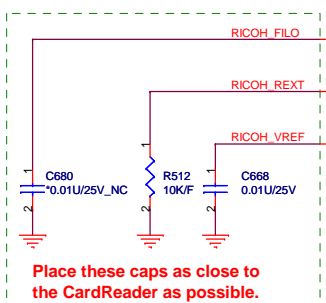
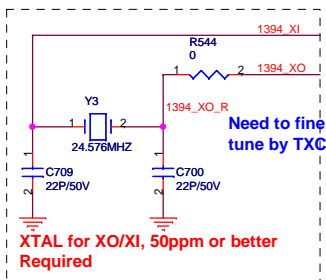
PCI / OTHER



0630_Michael:Remove Mini PCI CN8 and circuit

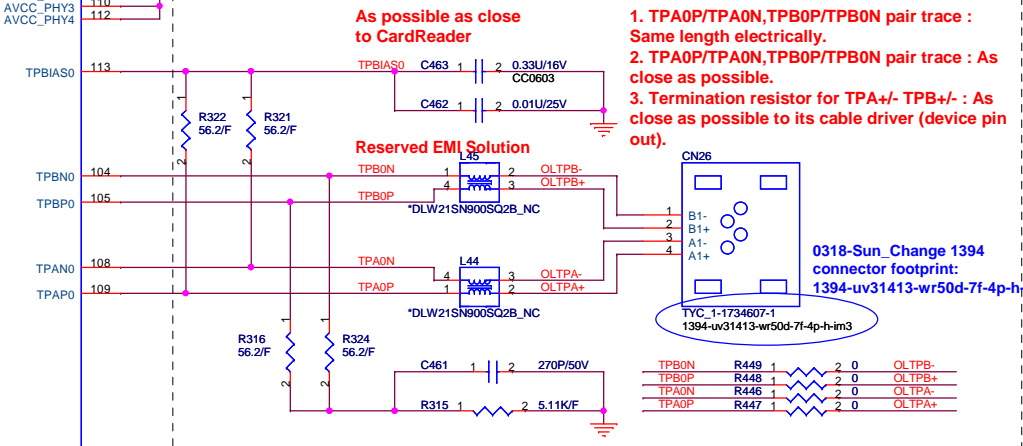
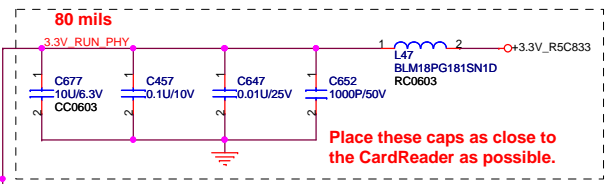
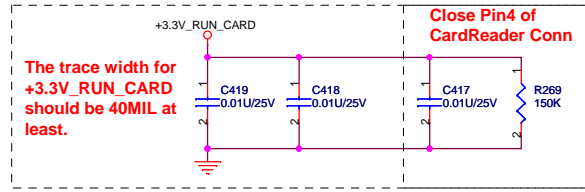
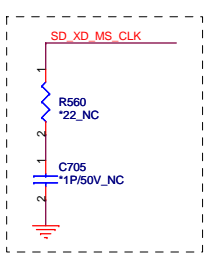
0707_Michael:Depop R561 for leakage issue





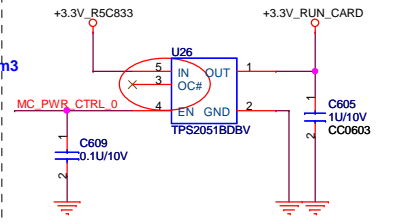
Card Reader interface signal mapping

PIN	SD	MMC	MS	XD
MDIO00	SD_CD#	MMC_CD#		XD_CD#
MDIO01			MS_CDR#	XD_CD1#
MDIO02	SD_WP#			XD_CER#
MDIO03	SD_PWR0	MMC_PWR	MS_PWR	XD_ER/B#
MDIO04	SD_PWR1			XD_WP#
MDIO05	SD_LED#	MMC_LED#	MS_LED#	XD_LED#
MDIO07	MTEST			
MDIO08	SD_CMD	MMC_CMD	MS_BS	XD_WE#
MDIO09	SD_CLK	MMC_CLK	MS_CLK	XD_RE#
MDIO10	SD_D0	MMC_D0	MS_D0	XD_D0
MDIO11	SD_D1	MMC_D1	MS_D1	XD_D1
MDIO12	SD_D2	MMC_D2	MS_D2	XD_D2
MDIO13	SD_D3	MMC_D3	MS_D3	XD_D3
MDIO14		MMC_D4		XD_D4
MDIO15		MMC_D5		XD_D5
MDIO16		MMC_D6		XD_D6
MDIO17		MMC_D7		XD_D7
MDIO18				XD_CLE
MDIO19				XD_ALE

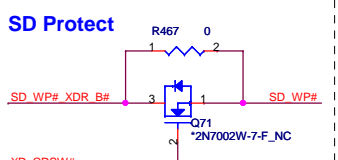
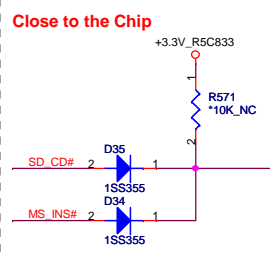
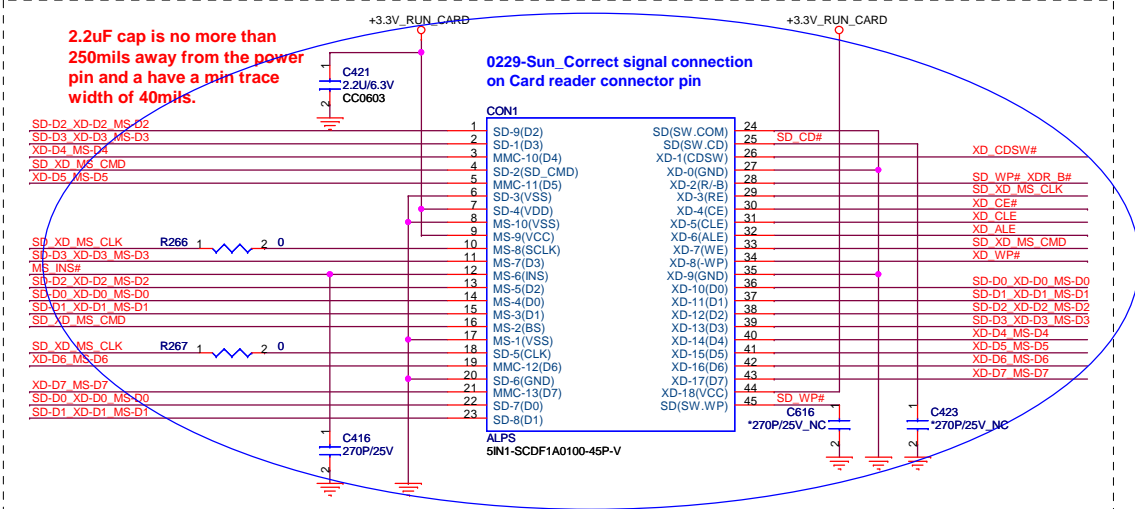


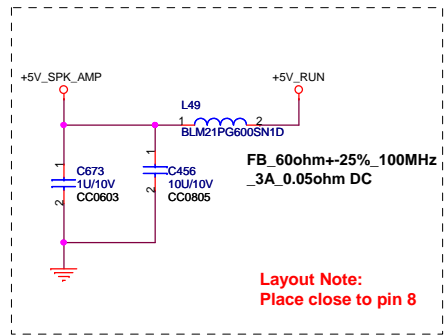
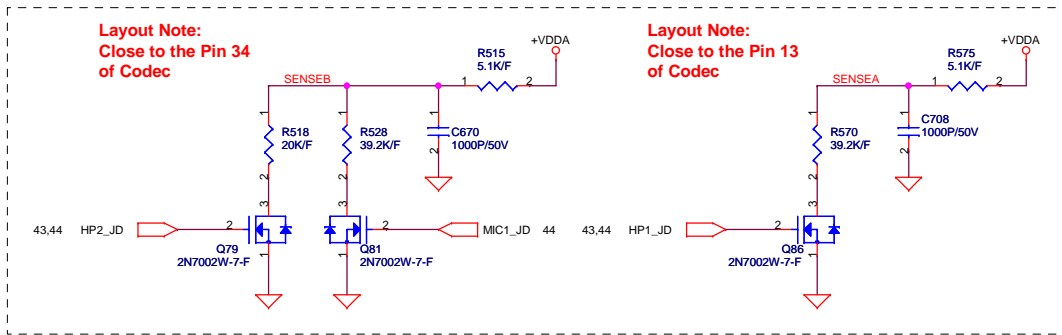
Layout Note:

- 1). The distance between Media Card Power Switch and Media Socket should be less than 2-inches.
- 2). The trace width for +3.3V_RUN_CARD should be 40MIL at least.
- 3). The GND trace for Media Card Socket should be 40MIL at least.

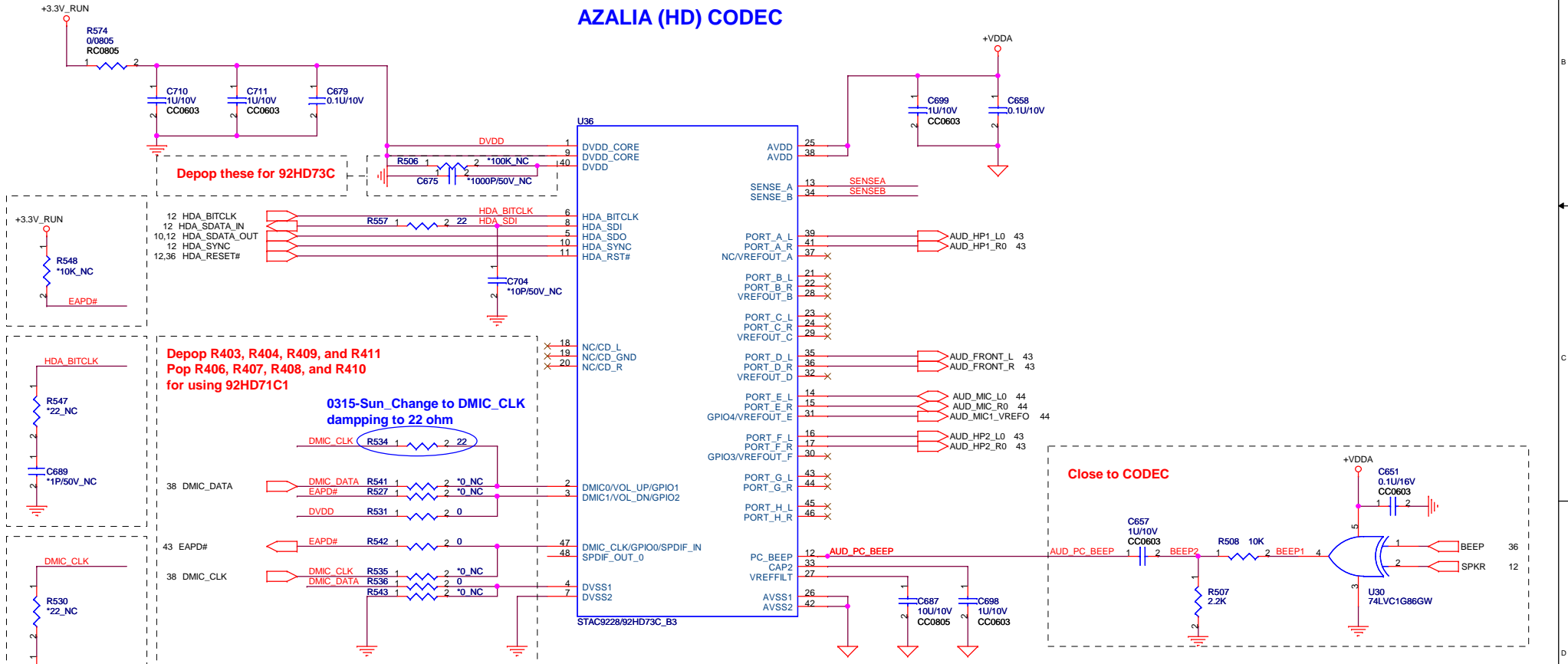


- MDIO17 XD-D7 MS-D7
- MDIO16 XD-D6 MS-D6
- MDIO15 XD-D5 MS-D5
- MDIO14 XD-D4 MS-D4
- MDIO13 SD-D3 XD-D3 MS-D3
- MDIO12 SD-D2 XD-D2 MS-D2
- MDIO11 SD-D1 XD-D1 MS-D1
- MDIO10 SD-D0 XD-D0 MS-D0
- MDIO05 XD_WP#
- MDIO08 SD_XD_MS_CMD
- MDIO19 XD_ALE
- MDIO02 XD_CE#
- MDIO03 SD_WP# XDR_B#
- MDIO00 SD_CD#
- MDIO01 MS_INS#
- MDIO09 SD_XD_MS_CLK
- MDIO04 MC_PWR_CTRL_0
- MDIO06 T44 PAD
- MDIO07 R5C833T_V00





AZALIA (HD) CODEC



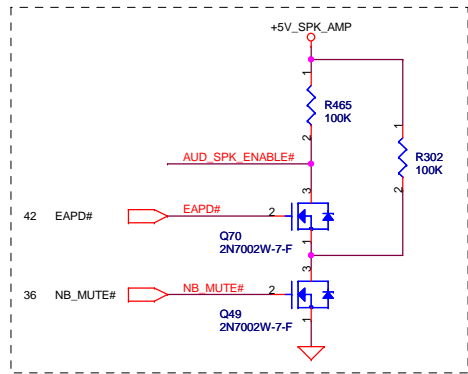
**QUANTA
COMPUTER**

Title: Azalia CODEC

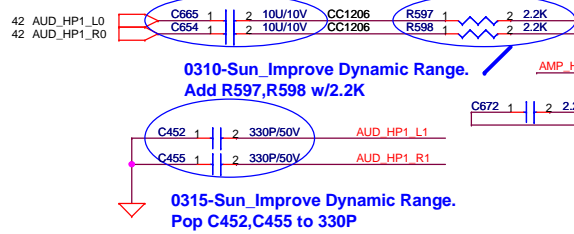
Size: Document Number IM3 (XPS-Jolie) Rev 2A

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INTERNAL SPEAKER AMP

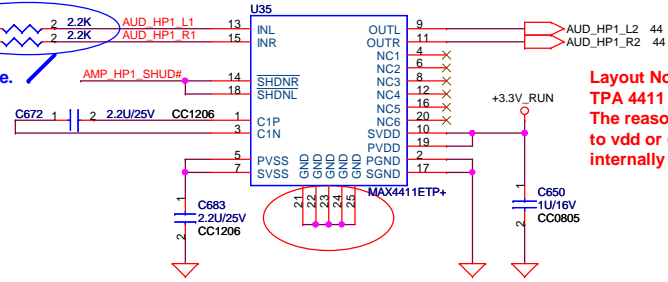


0315-Sun_Improve Dynamic Range.
0320-StegChange AC coupling to 10U/10V

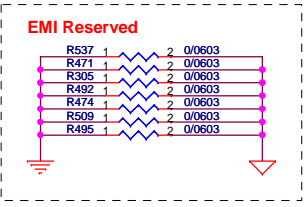
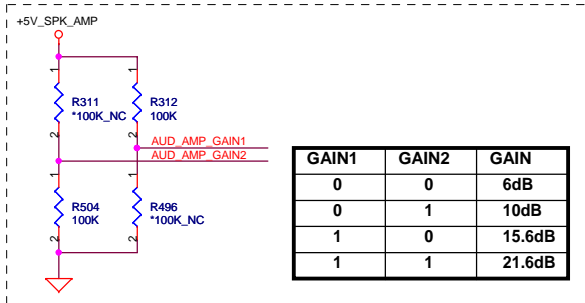
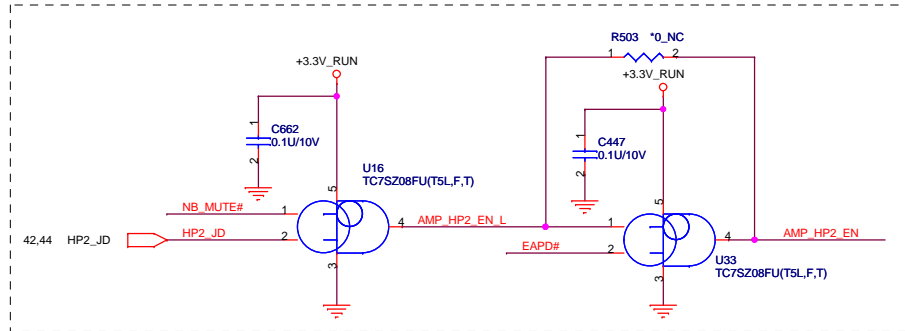
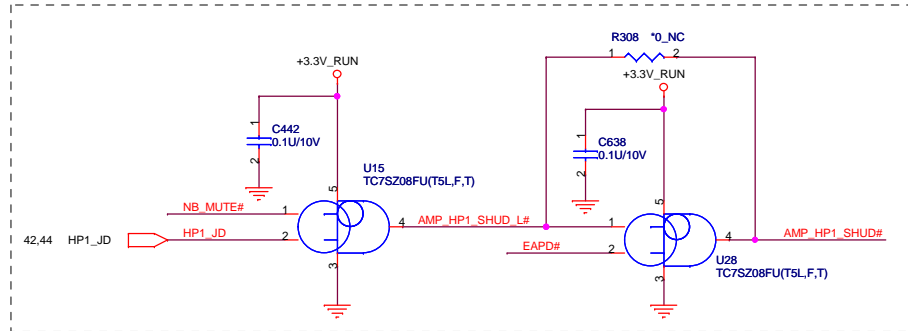


0310-Sun_Improve Dynamic Range.
Add R597,R598 w/2.2K

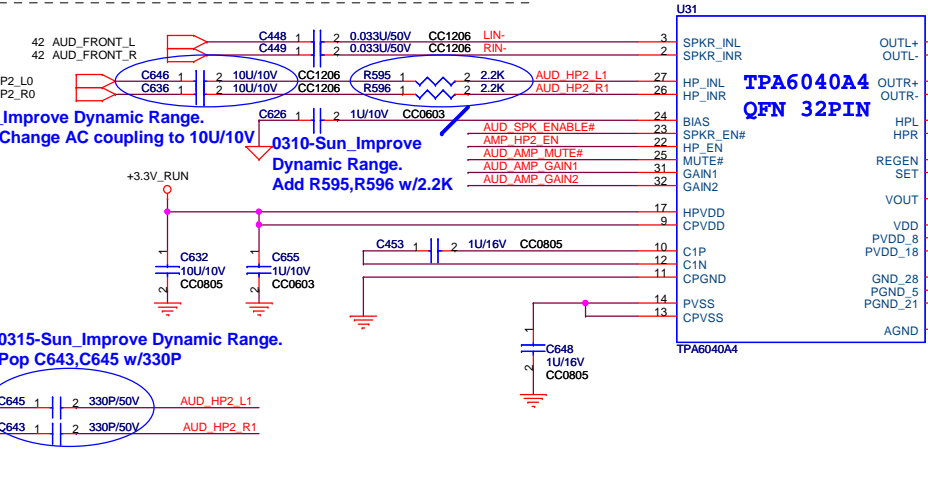
0315-Sun_Improve Dynamic Range.
Pop C452,C455 to 330P



Layout Note:
TPA 4411 : cannot connect EP to GND.
The reason that we can't solder the pad to vdd or ground is because it is internally connected to VSS.



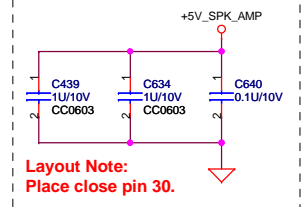
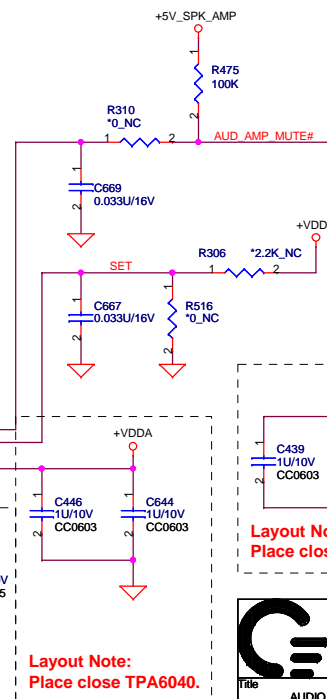
Layout Note:
MAX9789A/TPA6040A : need to connect EP (exposed paddle) to GND.
TPA 4411 : cannot connect EP to GND.
MAX 4411: can connect EP to GND.



TPA6040A QFN 32PIN

0315-Sun_Improve Dynamic Range.
0320-StegChange AC coupling to 10U/10V
0310-Sun_Improve Dynamic Range.
Add R595,R596 w/2.2K

0315-Sun_Improve Dynamic Range.
Pop C643,C645 w/330P



Layout Note:
Place close pin 30.

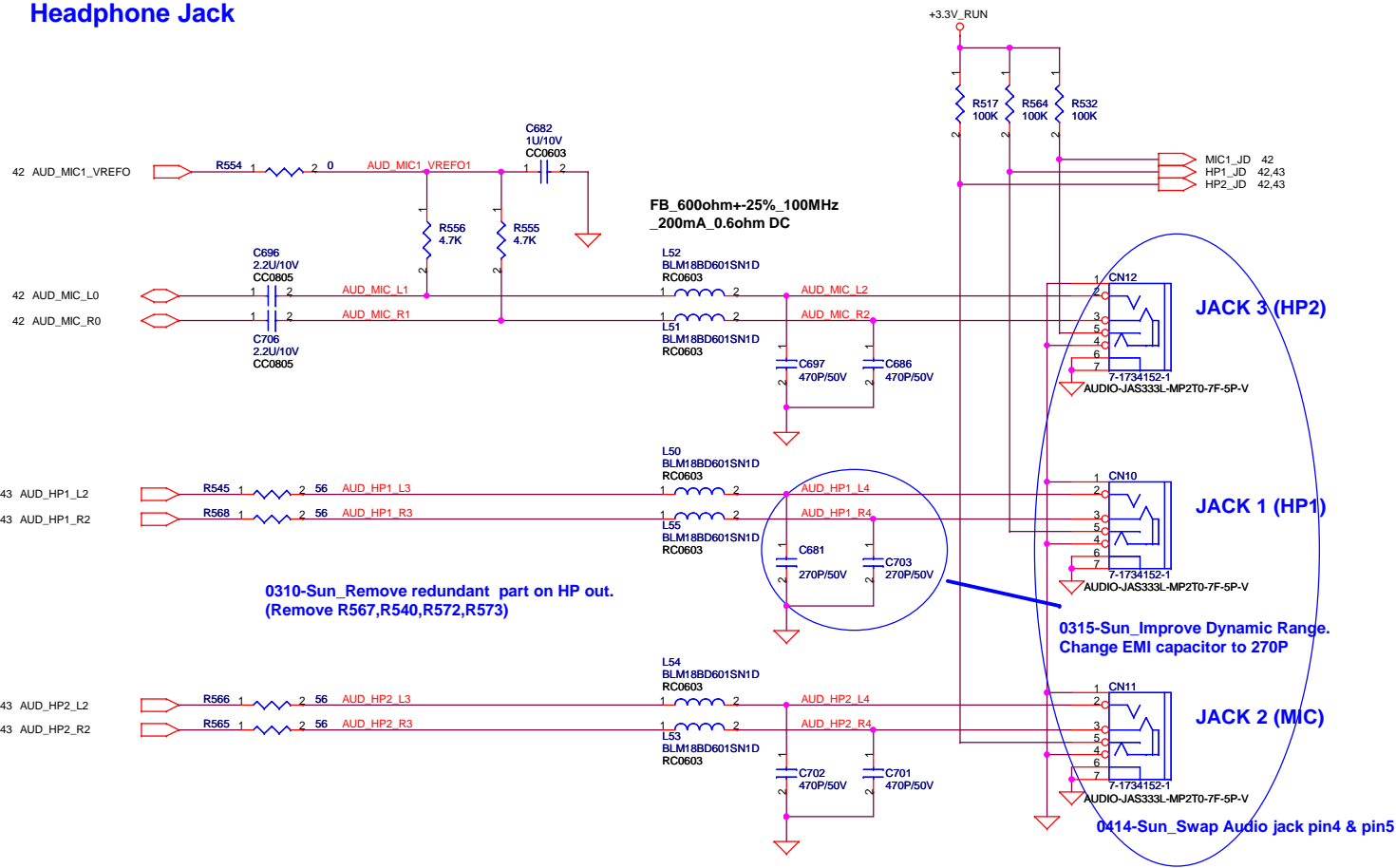
Layout Note:
Place close to pin 18.

Layout Note:
Place close TPA6040.

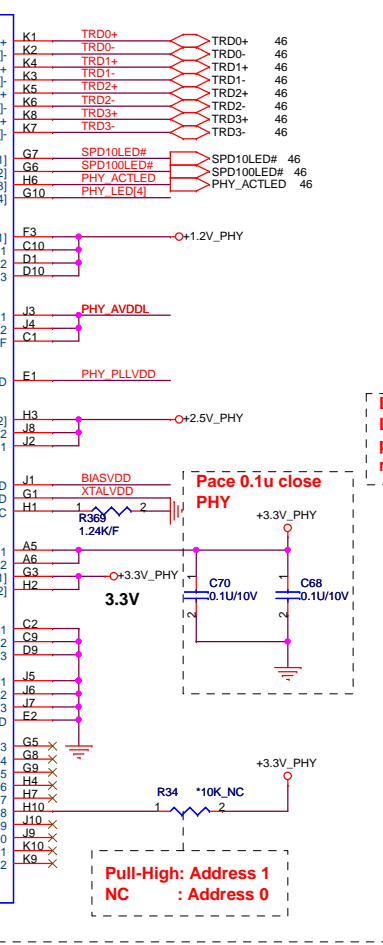
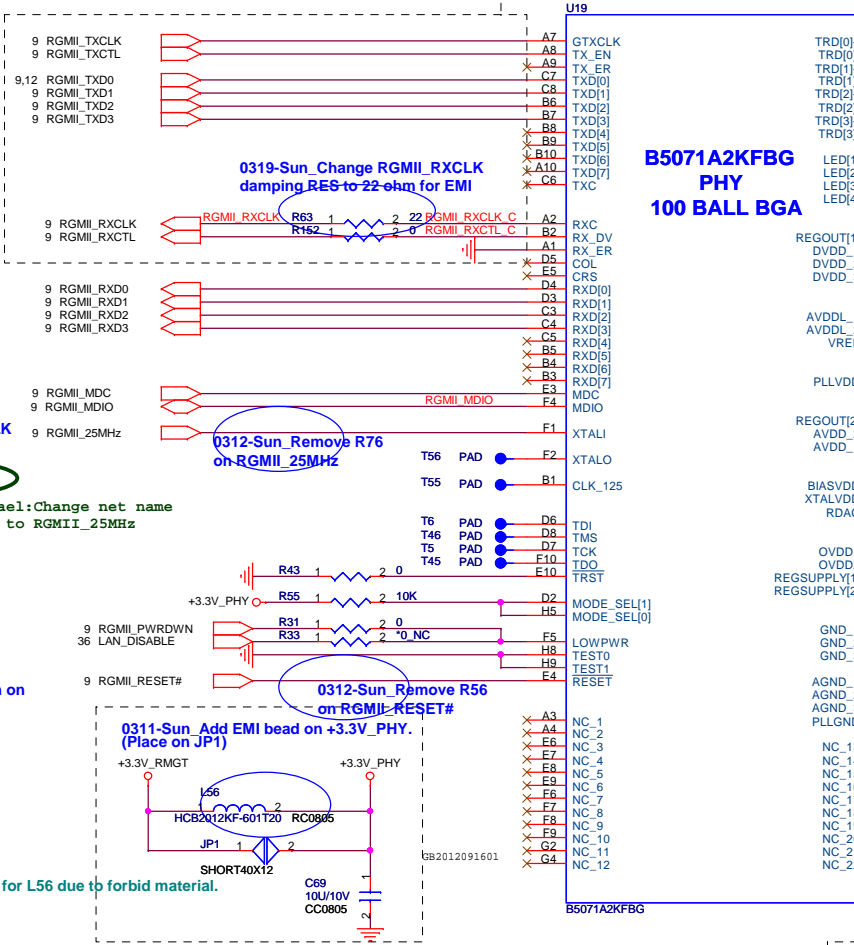
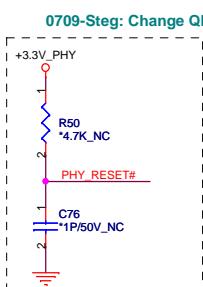
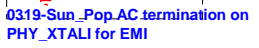
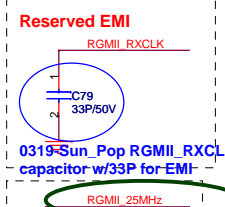
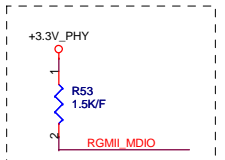
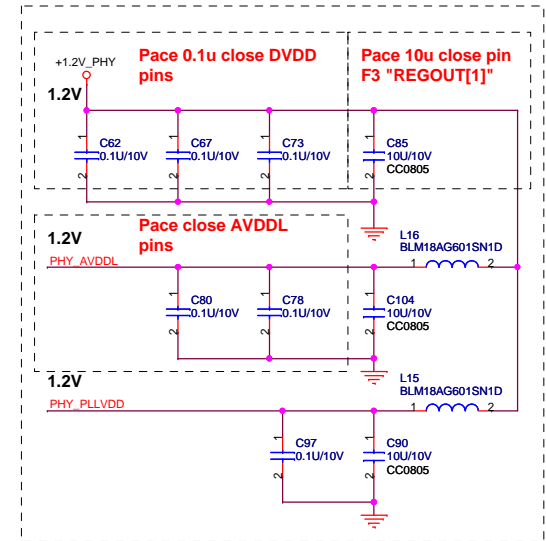
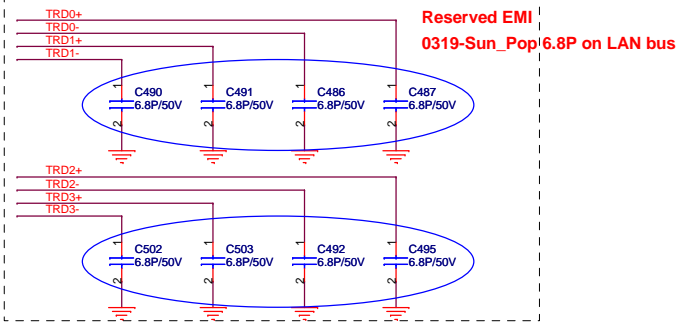
**QUANTA
COMPUTER**

Title: AUDIO AMP		
Size:	Document Number: IMS (XPS-Jolie)	Rev: 2A
Date: Friday, September 05, 2008	Sheet: 43	of 59

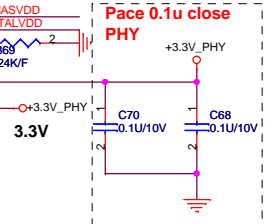
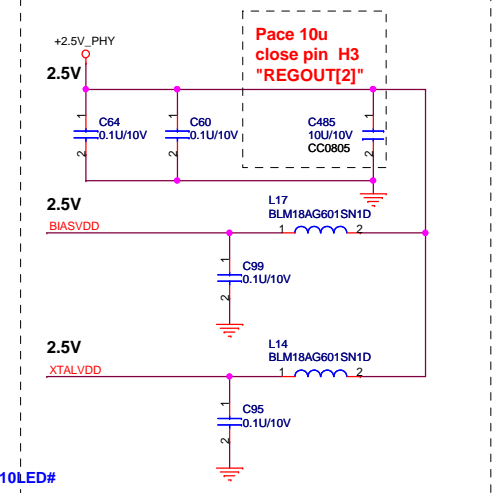
Headphone Jack



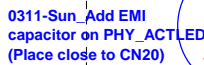
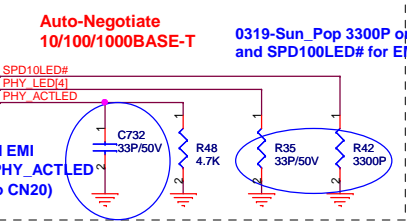
Layout Note:
 1. Use 50 ohm impedance for all trace.
 2. Trace length matched to a tolerance of 9.8mm in order to keep the skew between signals less than 0.07ns.
 3. The receive and transmit signals kept away from each other and other analog and clock signals to reduce crosstalk.



Layout Note:
 Locate the RDAC resistor as close to the RDAC pin as possible and keep the trace between the pin and resistor and short and wide as possible.



Pull-High: Address 1 NC : Address 0



QUANTA COMPUTER

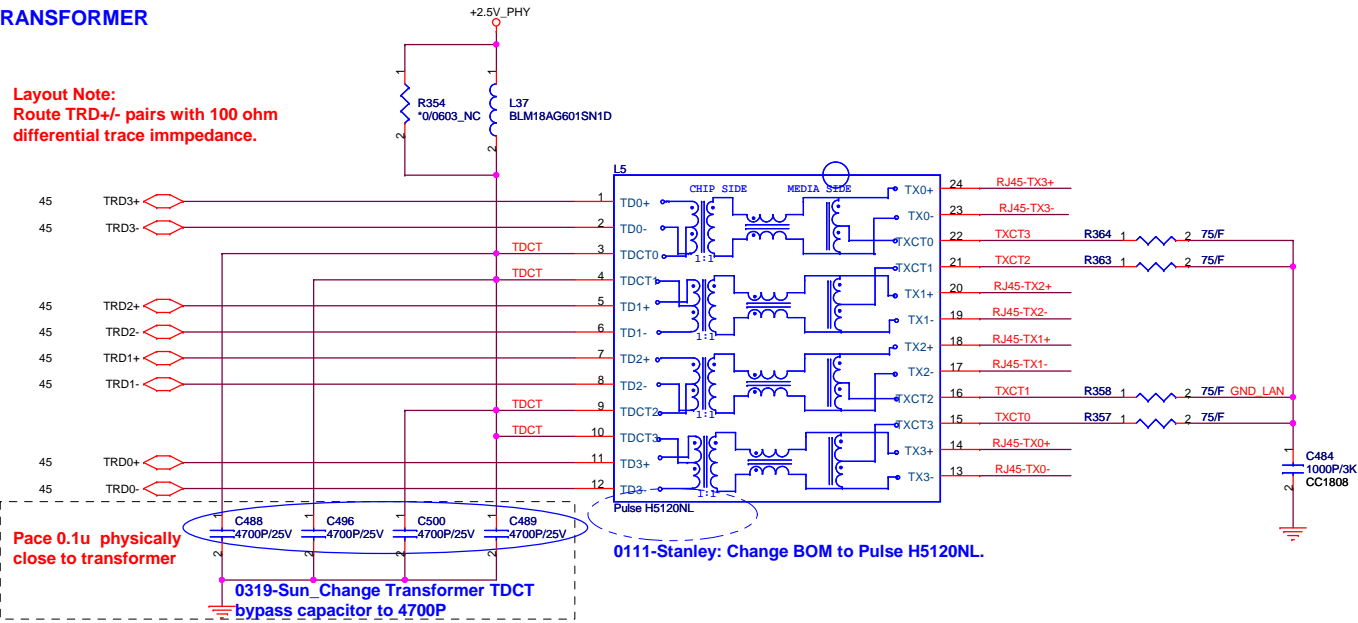
Title: LAN Broadcom PHY B5071

Size: Document Number IM3 (XPS-Jolie) Rev 2A

Date: Friday, September 05, 2008 Sheet 45 of 59

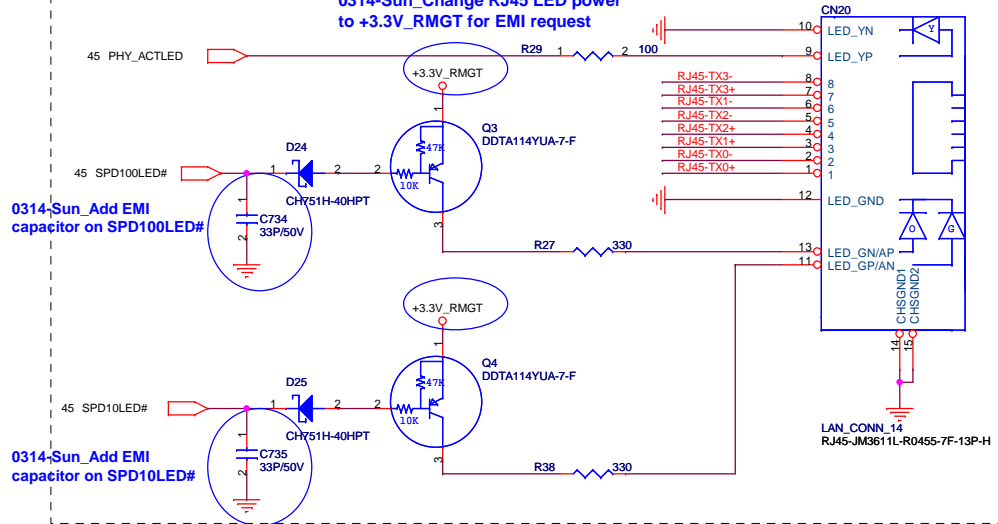
TRANSFORMER

Layout Note:
Route TRD+/- pairs with 100 ohm differential trace impedance.

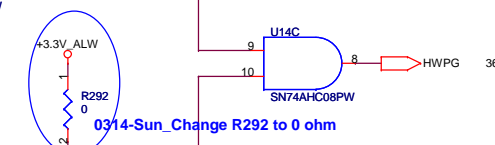
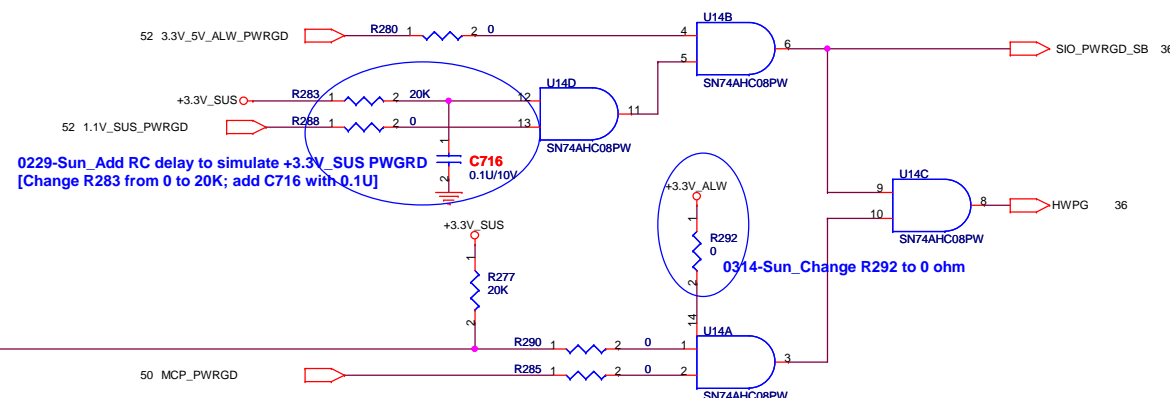
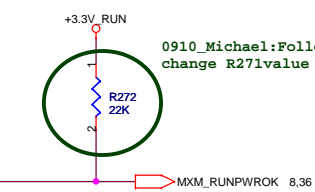
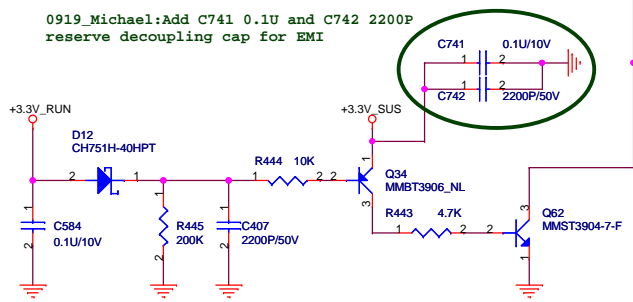
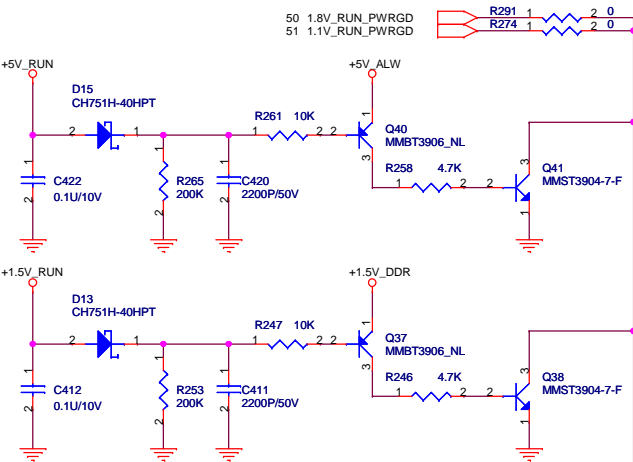
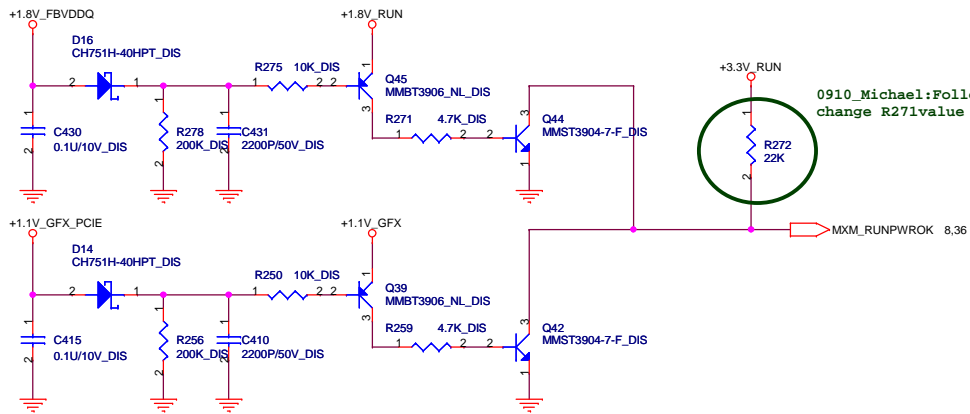


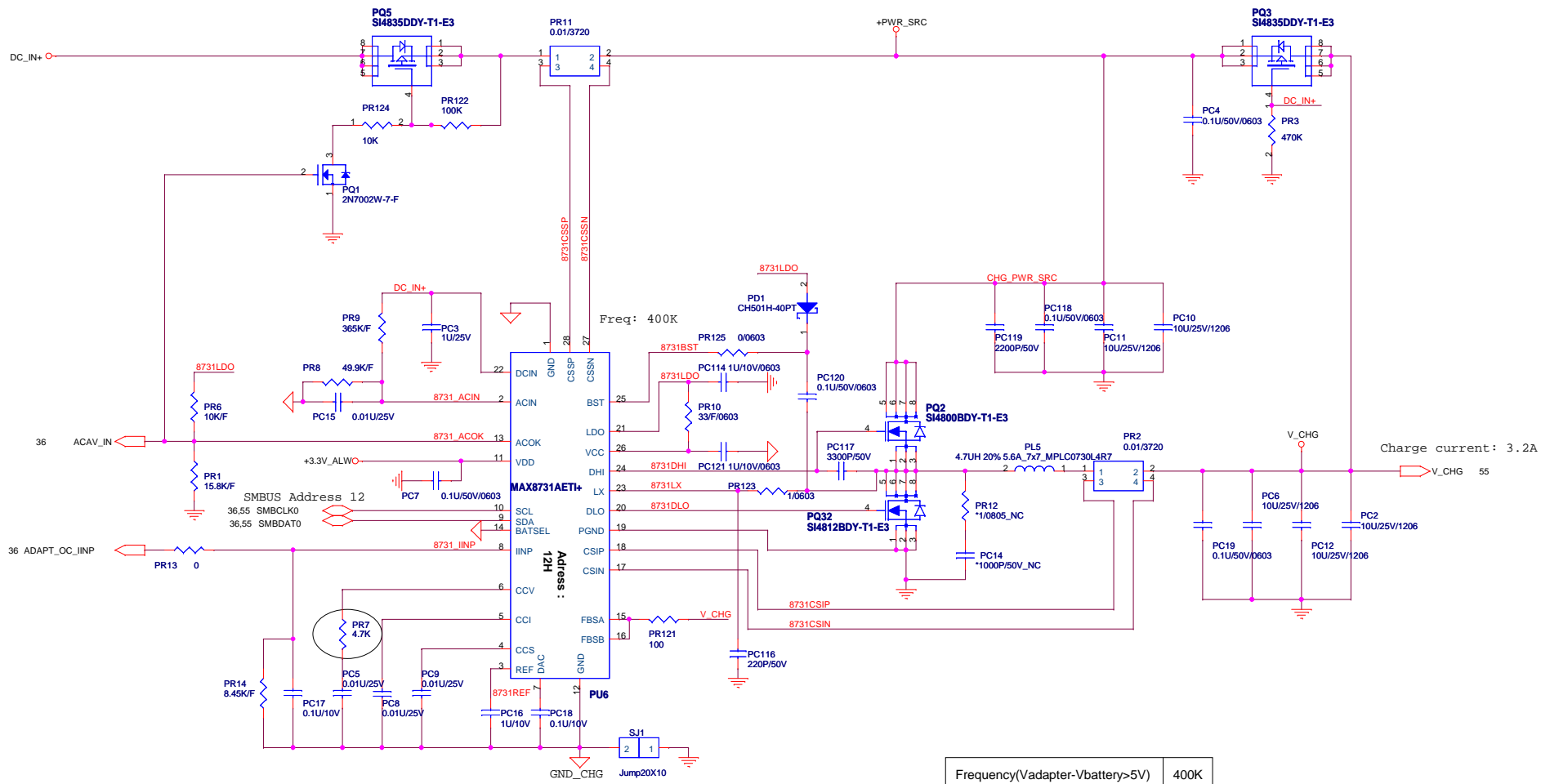
RJ-45 Connector

0314-Sun_Change RJ45 LED power to +3.3V_RMGT for EMI request



Title LAN SWITCH		
Size	Document Number IM3 (XPS-Jolie)	Rev 2A
Date:	Friday, September 05, 2008	Sheet 46 of 59



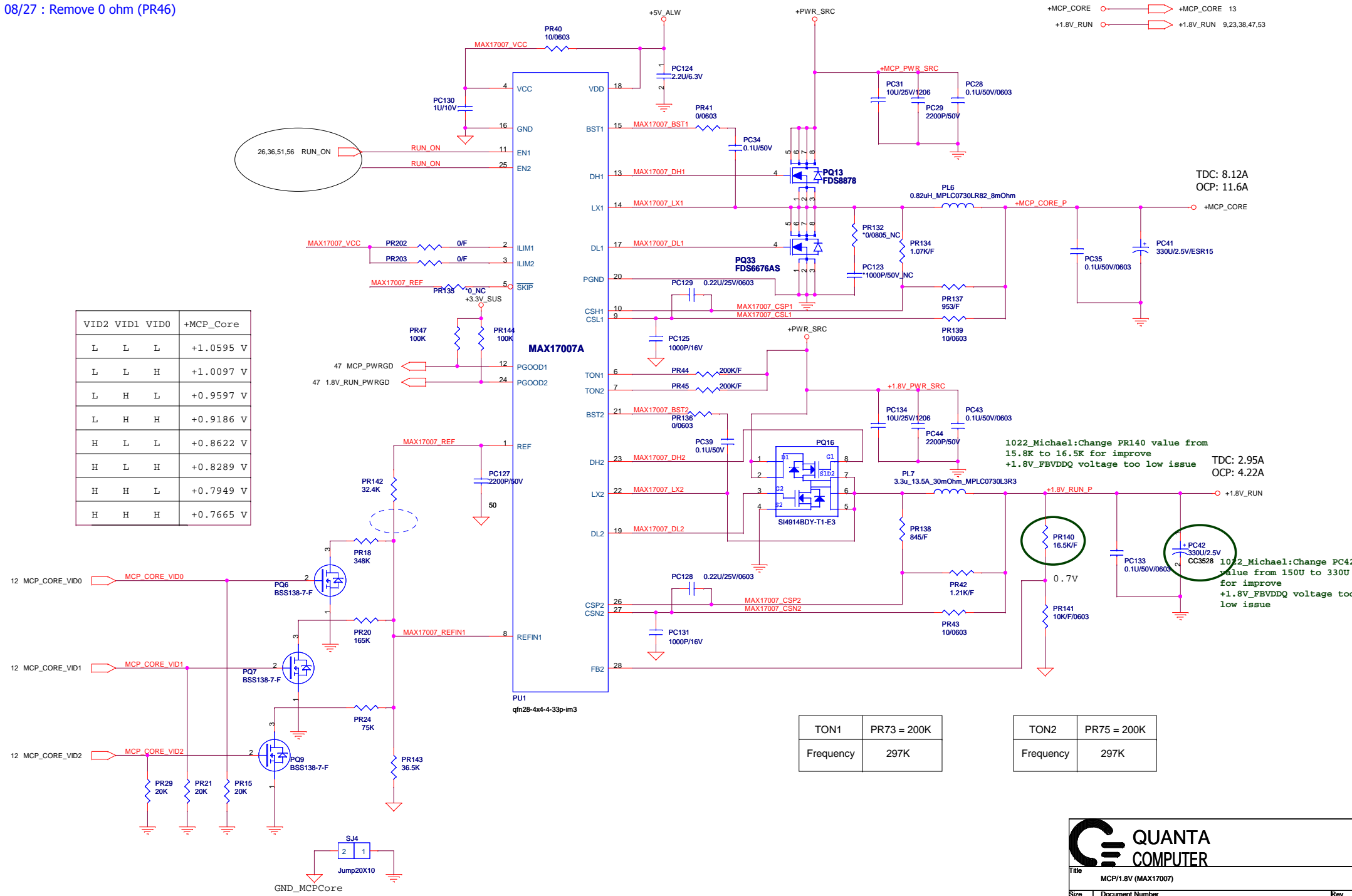


08/27 : Remove 0 ohm (PR46)

+MCP_CORE +MCP_CORE 13
 +1.8V_RUN +1.8V_RUN 9,23,38,47,53

26,36,51,56 RUN_ON

VID2	VID1	VID0	+MCP_Core
L	L	L	+1.0595 V
L	L	H	+1.0097 V
L	H	L	+0.9597 V
L	H	H	+0.9186 V
H	L	L	+0.8622 V
H	L	H	+0.8289 V
H	H	L	+0.7949 V
H	H	H	+0.7665 V



TDC: 8.12A
 OCP: 11.6A

1022_Michael:Change PR140 value from 15.8K to 16.5K for improve +1.8V_FBVDQ voltage too low issue
 TDC: 2.95A
 OCP: 4.22A

1022_Michael:Change PC42 value from 150U to 330U for improve +1.8V_FBVDQ voltage too low issue

TON1	PR73 = 200K
Frequency	297K

TON2	PR75 = 200K
Frequency	297K

QUANTA COMPUTER

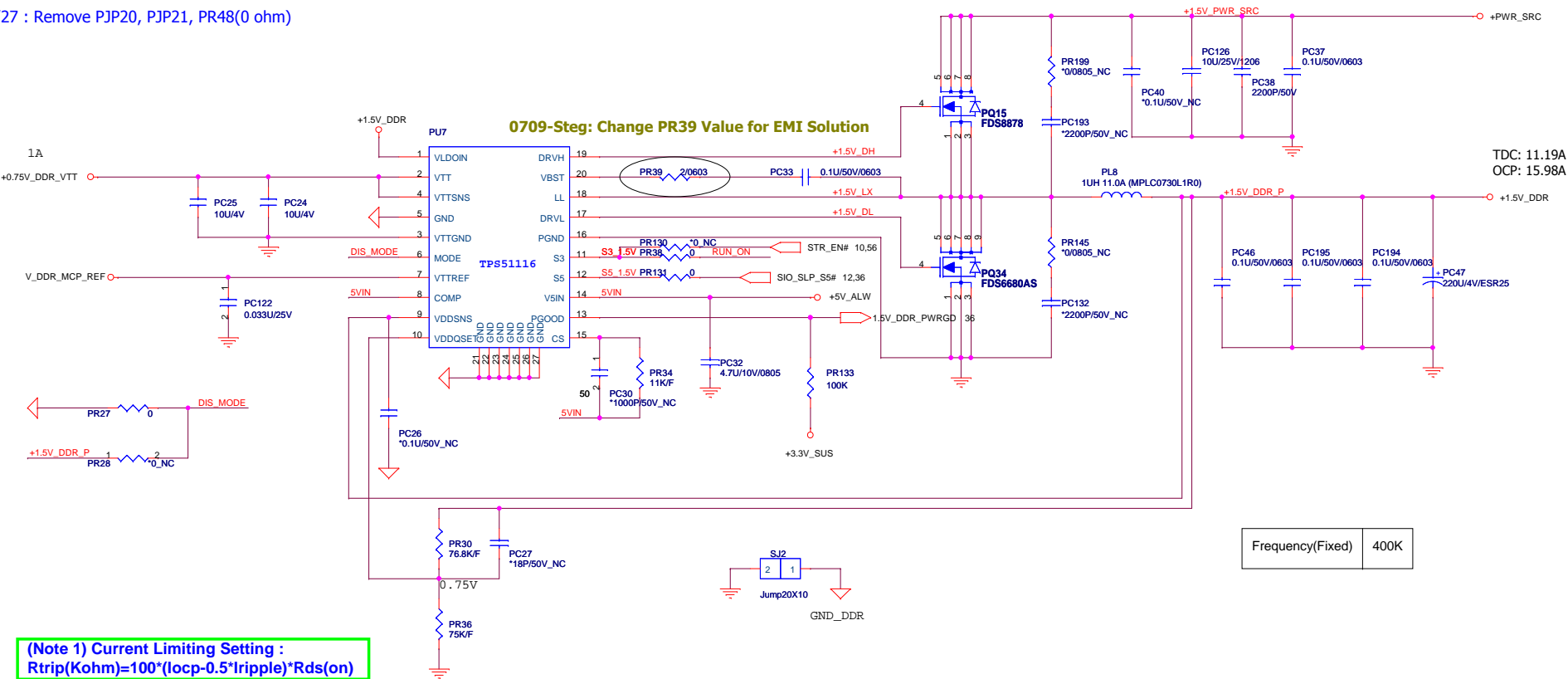
Title: MCP/1.8V (MAX17007)

Size: Document Number IM3 (XPS-Jolie) Rev 1B

Date: Thursday, October 23, 2008 Sheet 50 of 59

- +1.5V_DDR ○ → +1.5V_DDR 15,16,47,56
- +0.75V_DDR_VTT ○ → +0.75V_DDR_VTT 15,16,56
- +1.1V_RUN ○ → +1.1V_RUN 5,7,8,9,11,12
- V_DDR_MCP_REF ○ → V_DDR_MCP_REF 15,16

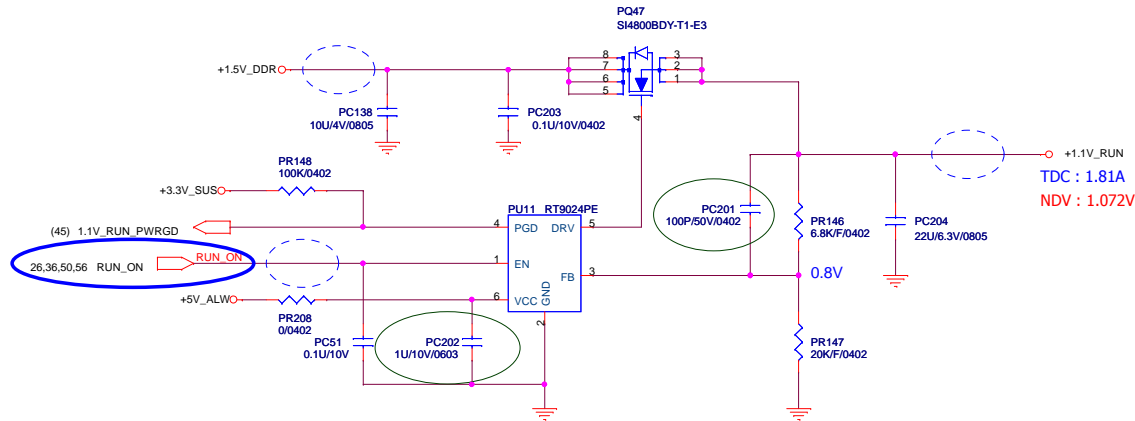
08/27 : Remove PJP20, PJP21, PR48(0 ohm)



TDC: 11.19A
OCP: 15.98A

Frequency(Fixed)	400K
------------------	------

(Note 1) Current Limiting Setting :
 $R_{trip}(Kohm) = 100 * (I_{ocp} - 0.5 * I_{ripple}) * R_{ds(on)}$



TDC : 1.81A
NDV : 1.072V

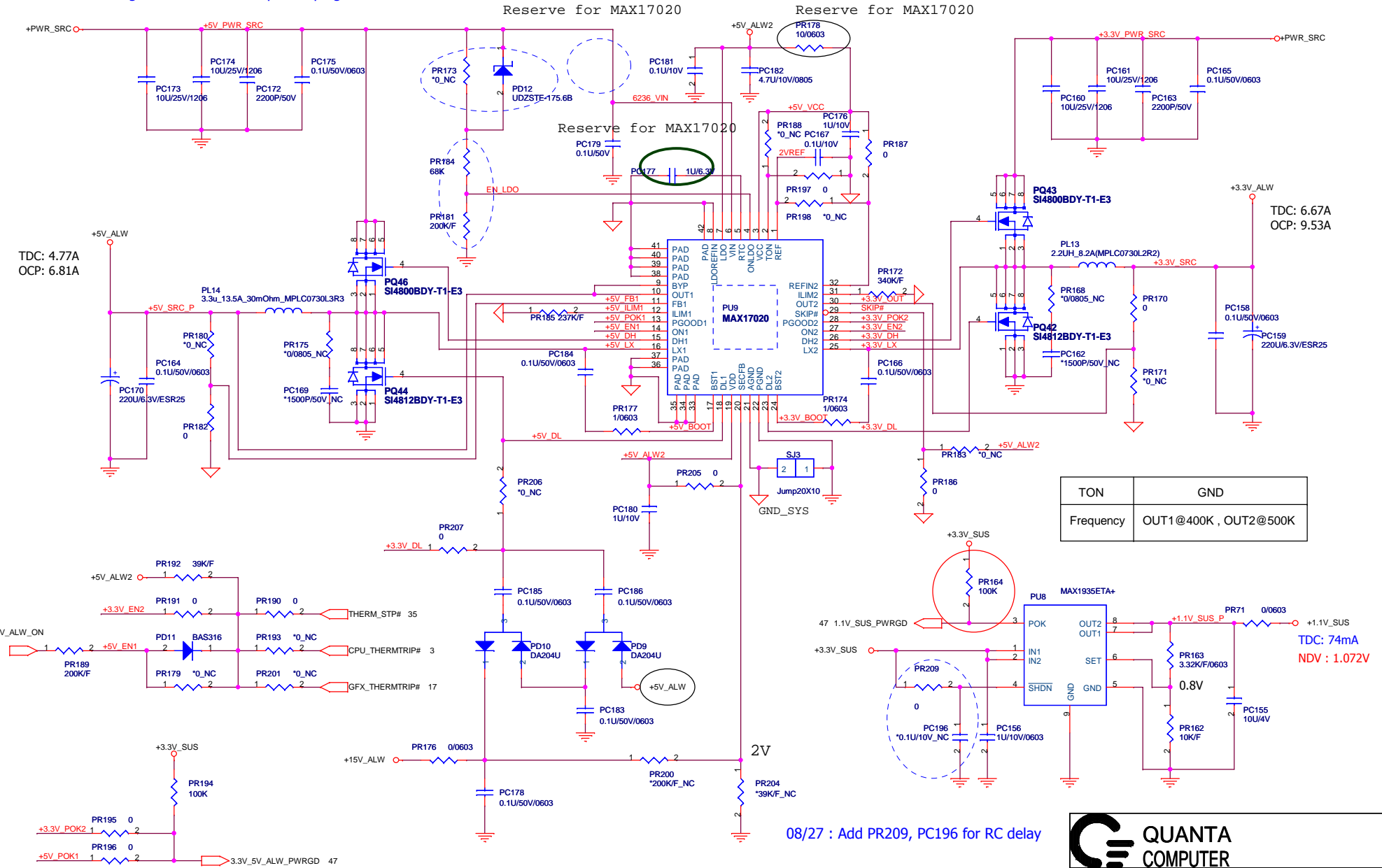


- +1.1V_SUS  +1.1V_SUS 13,14
- +5V_ALW  +5V_ALW 15,30,31,38,39,47,50,51,53,54,56
- +3.3V_ALW  +3.3V_ALW 23,26,31,32,36,37,38,39,47,48,55,56

08/27 : Remove PR169, PR173 (0 ohm)

08/27 : Add Zener Diode (PD12), PR173 and change PR184=68K, PR181=200K to fix +3.3V_ALW glitch issue when adapter unplug

0916_Rick:Change PC177 value from 0.1u to 1u



TON	GND
Frequency	OUT1@400K , OUT2@500K

QUANTA COMPUTER

Title: SYS 5V/3V(MAX17020)

Size: Document Number IM3 (XPS-Jolie) Rev 1A

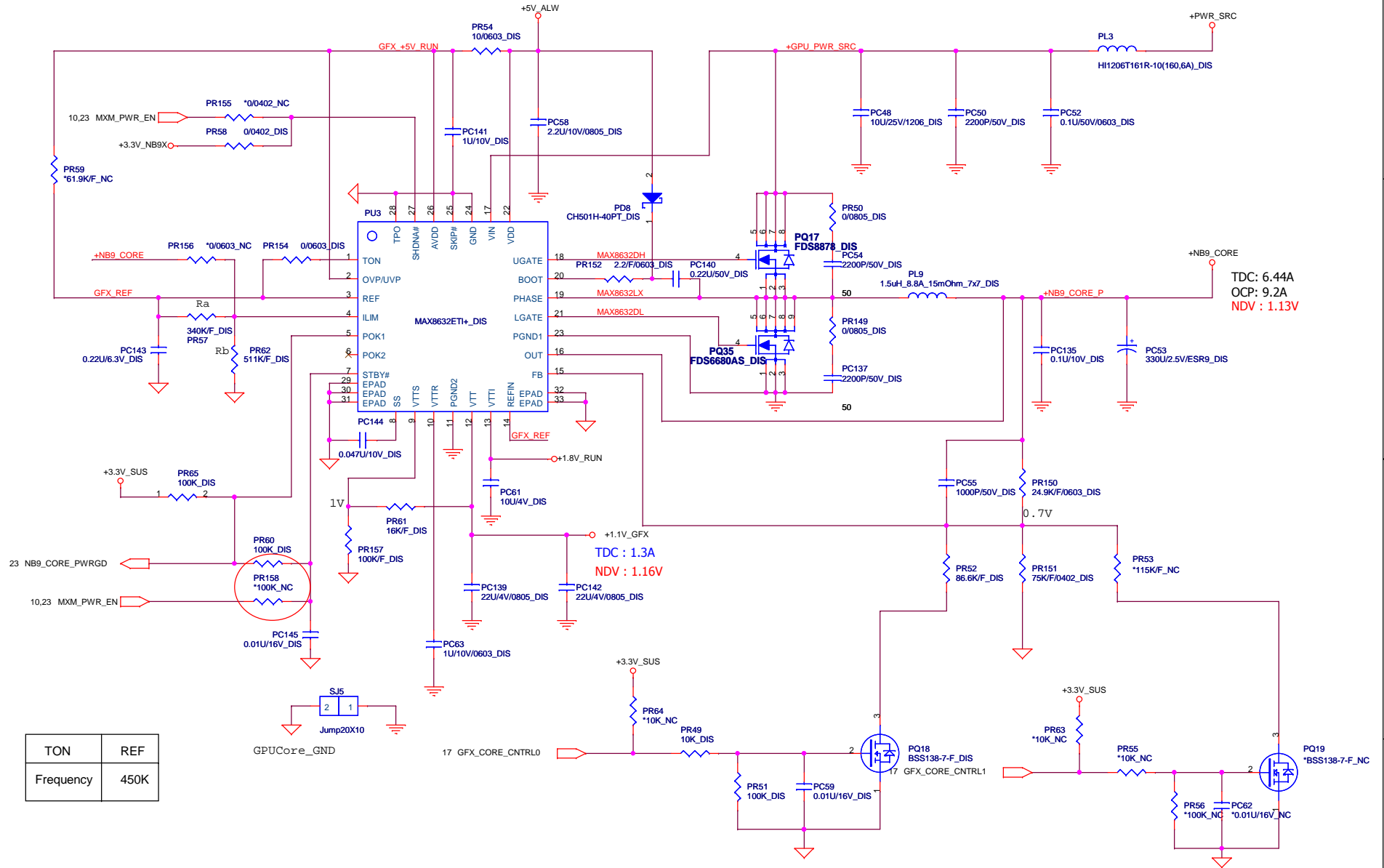
Date: Wednesday, September 17, 2008 Sheet 52 of 59

08/27 : Add PR209, PC196 for RC delay

TDC: 6.67A
OCP: 9.53A

TDC: 74mA
NDV : 1.072V

+NB9_CORE 20
+1.1V_GFX 23.47



TDC: 6.44A
OCP: 9.2A
NDV: 1.13V

TDC: 1.3A
NDV: 1.16V

TON	REF
Frequency	450K

ILIM	$I_{ovp} = (2 * (R_b / (R_a + R_b)) * 0.1 * (1 / RDSON)) + (I_{DELTA} / 2)$
SKIP#	AVDD = Low-noise, forced-PWM mode. GND = Pulse-skipping operation.
OVP/UVFP	The overvoltage limit is 116% of Vout. The undervoltage limit is 70% of Vout.

GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	+NB9_CORE
LOW	LOW	0.9
HIGH	LOW	0.9
HIGH	HIGH	1.1V

QUANTA COMPUTER

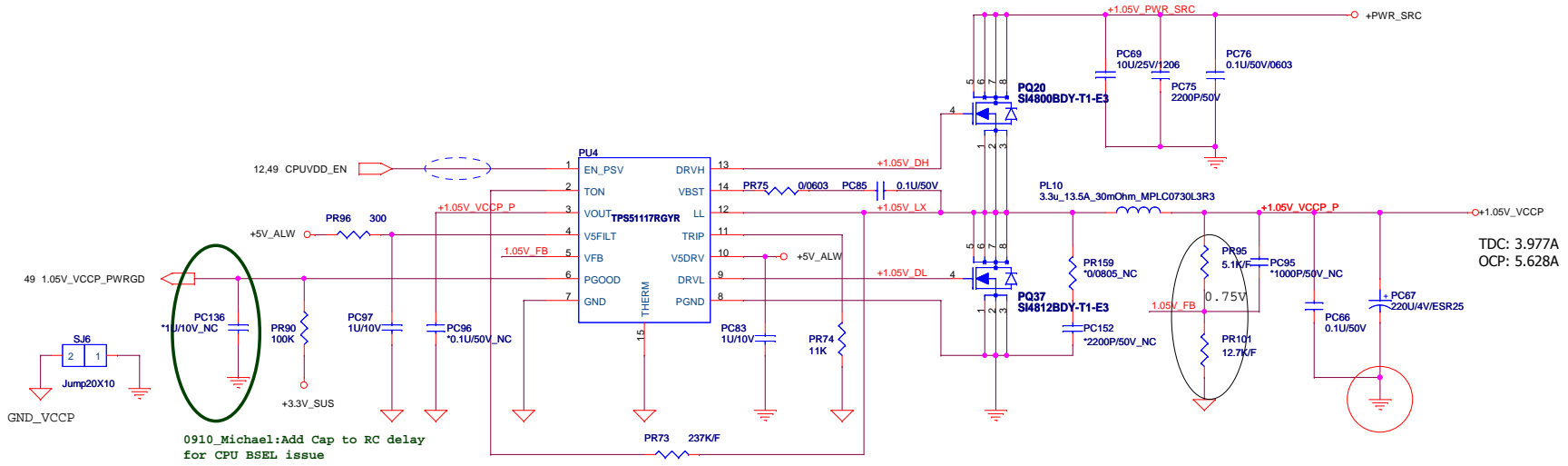
Title: VGA DC/DC

Size: Document Number: IMS (XPS-Jolie) Rev: 1A

Date: Wednesday, September 17, 2008 Sheet: 53 of 59

+1.05V_VCCP +1.05V_VCCP 3,4,5,13

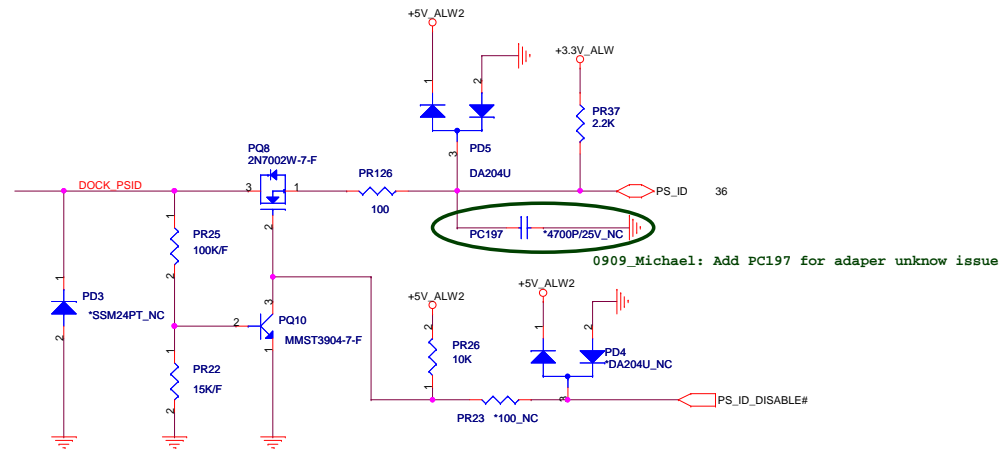
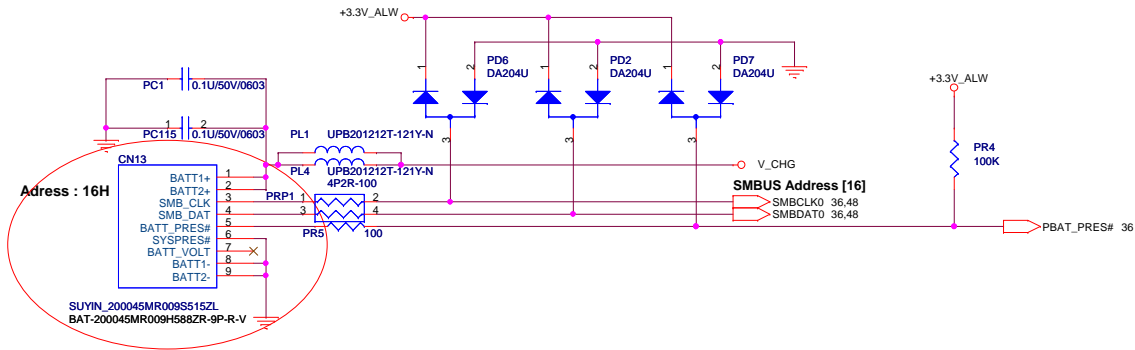
08/27 : Remove 0 ohm (PR79)



TON	PR185=237K
Frequency	300K

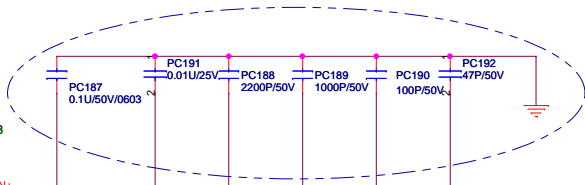
**QUANTA
COMPUTER**

Title		CPUVTT_Core (TPS51117)	
Size	Document Number	Rev	
	IM3 (XPS-Jolie)	1A	
Date:	Thursday, September 11, 2008	Sheet	54 of 59

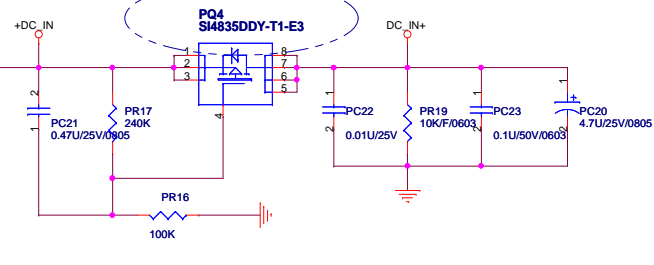


0909_Michael: Add PC197 for adaper unknow issue

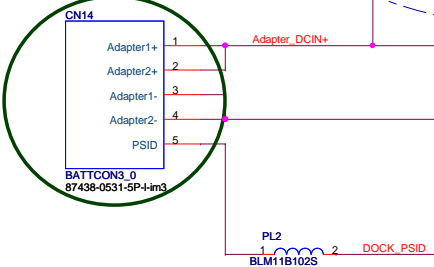
0311-Rick: Add PC187-PC192 for EMC



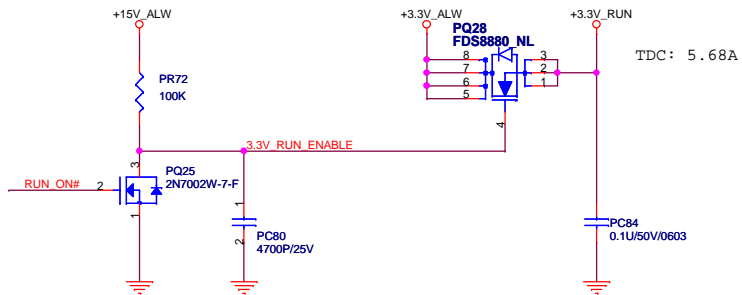
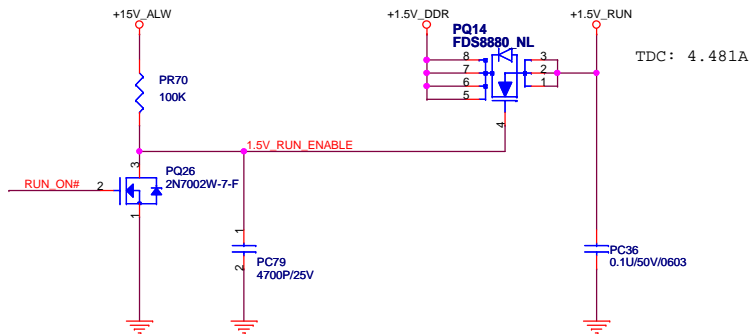
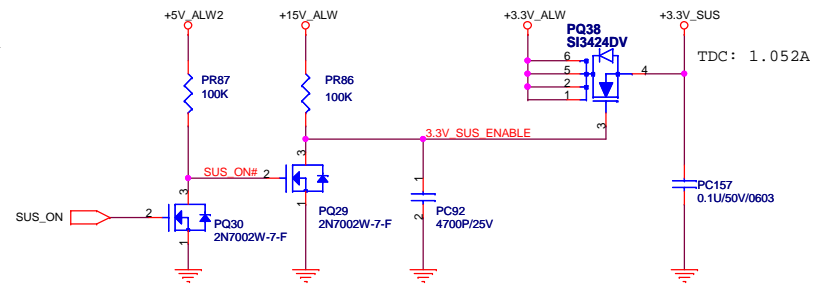
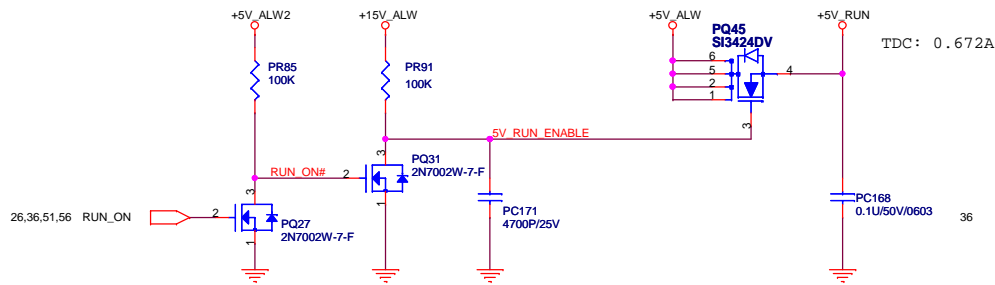
0709-Rick: Change PQ4 Value



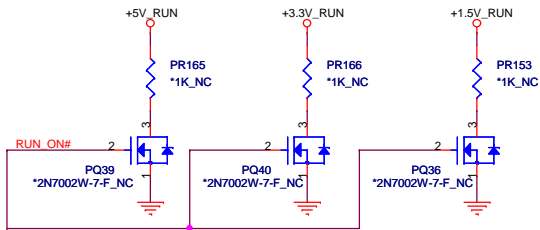
0823_Michael: Change Footprint from 87438-0531-5p-L to 87438-0531-5p-1-im3



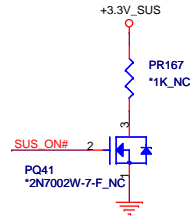
Title		DCIN,Batt
Size	Document Number	Rev
	IM3 (XPS-Jolie)	1A
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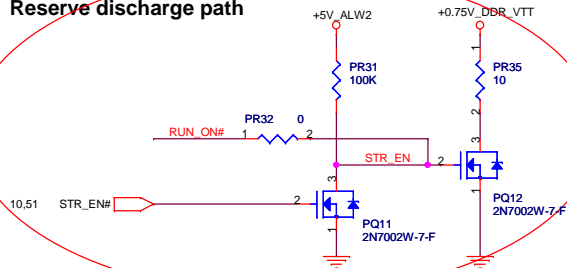
Reserve discharge path



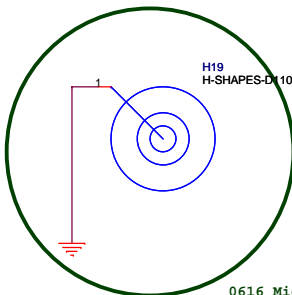
Reserve discharge path



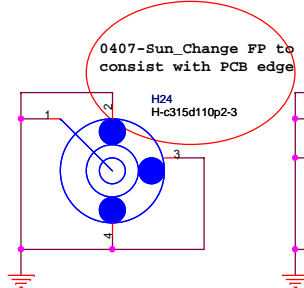
Reserve discharge path



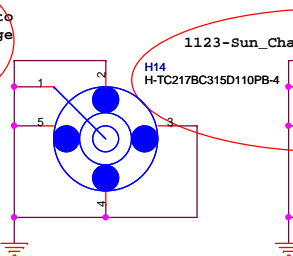
Title RUN POWER SW		
Size	Document Number IM3 (XPS-Jolie)	Rev 1A
Date:	Tuesday, September 09, 2008	Sheet 56 of 59



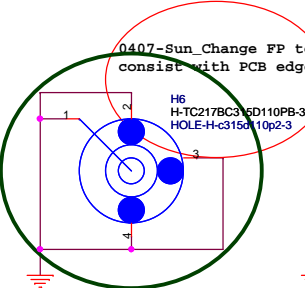
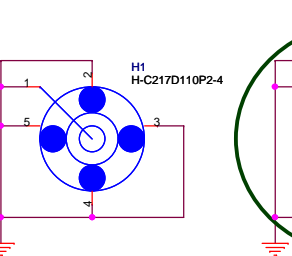
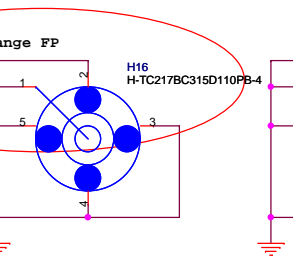
0616_Michael:Change footprint



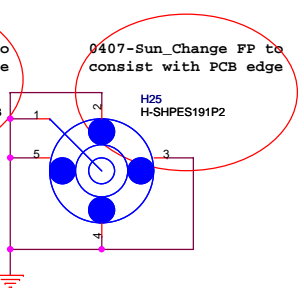
0407-Sun_Change FP to consist with PCB edge



1123-Sun_Change FP

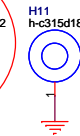
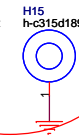
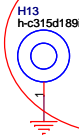
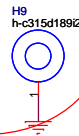
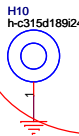
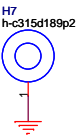


0407-Sun_Change FP to consist with PCB edge

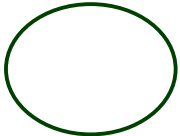
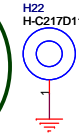
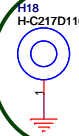
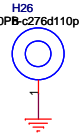
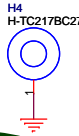
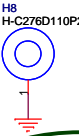


0407-Sun_Change FP to consist with PCB edge

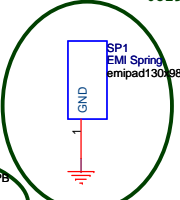
0616_Michael:Change footprint



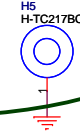
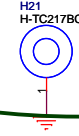
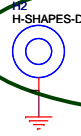
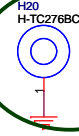
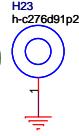
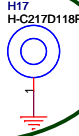
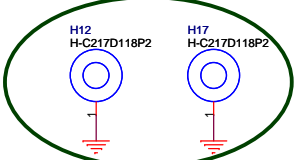
1123-Sun_Change FP



0829_Michael:Remove H3



0411-Sun_Add SP1
0605_Michael: Add connect to GND



0616_Michael:Change footprint



Title		
SCREW PAD		
Size	Document Number	Rev
	IMS (XPS-Jolie)	2A
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