

FM9 XXXX Intel Discrete GFX

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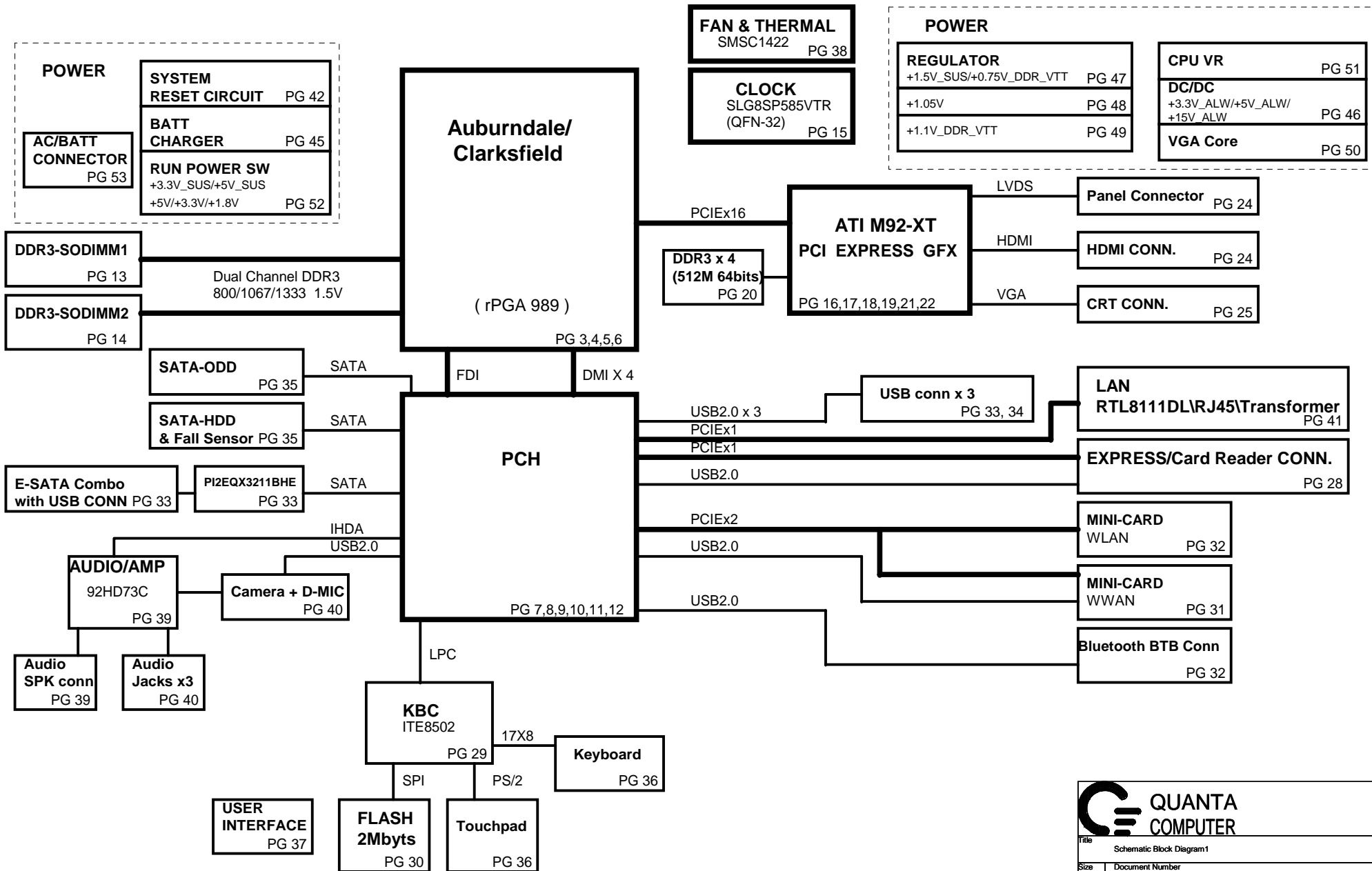









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Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	24,30,45,46,47,48,49,50,51	MAIN POWER		S0-S5
+RTC_CELL	+3.0V~+3.3V	08,11,29,30	RTC		S0-S5
+3.3V_ALW	+3.3V	08,29,30,35,36,37,42,44,45,46,47,52,53	8051 POWER	ALWON	S0-S5
+5V_ALW2	+5V	37,46,53	LARGE POWER	RUN_ON	S0-S5
+3.3V_LAN	+3.3V	41	LAN POWER	AUX_ON	
+5V_SUS	+5V	11,33,34,35,37,51,52	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	7,09,10,11,13,14,19,24,26,28,29,37,41,42,44,48,49,50,51,52	SLP_S5# CTRLD POWER	SUS_ON	
+1.5V_SUS	+1.8V	03,05,13,14,47,50,52	SODIMM POWER	SUS_ON	
+0.75V_DDR_VTT	+0.9V	13,14,47,52	SODIMM POWER	RUN_ON	
+5V_RUN	+5V	11,18,24,25,35,36,38,39,40,52	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,7,8,9,10,11,13,14,15,17,24,25,26,28,29,30,31,32,33,35,37,38,39,40,41,42,46,51,52,59	SLP_S3# CTRLD POWER	RUN_ON	
+1.8V_RUN	+1.8V	05,11,26,44,52	SDVO POWER	RUN_ON	
+1.5V_RUN	+1.5V	11,18,19,20,28,31,32,52	CALISTOGA/ICH9 POWER	RUN_ON	
+1.8V_RUN_GFX	+1.25V	17,18,21,22,44,52	VGA POWER	RUN_ON	
+VCC_GFX_CORE	+0.9V~+1.2V	18,21,50	VGA POWER	RUN_ON	
+1.05V_PCH	+1.05V	08,09,11,15,48	CPU/CALISTOGA/ICH8 POWER	1.05V_RUN_ON	
+VCC_CORE	+0.7V~+1.77V	05,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	26	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	36	Module Power	MODC_EN	
+5V_HDD	+5V	36	HDD Power	HDDC_EN	
+1.1V_VTT	+1.1V	03,05,10,11,49,59			
+1.1V_GFX_PCIE	+1.1V	18,50			

GND PLANE	PAGE	DESCRIPTION
 GND_CHG	46	
 GND_1.05V	47	
 GND_VGA	50	
 GND_SIGNAL	51	
 AGND_DC/DC	52	
 GND	ALL	



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Title: Index & Power Status

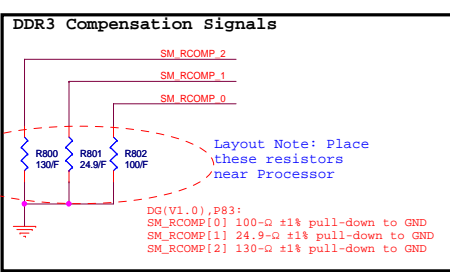
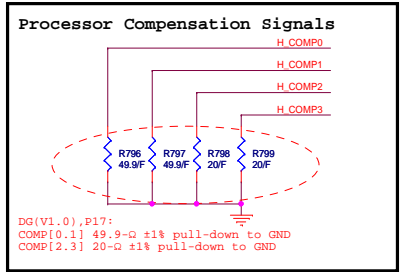
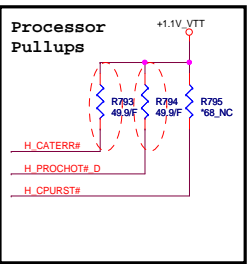
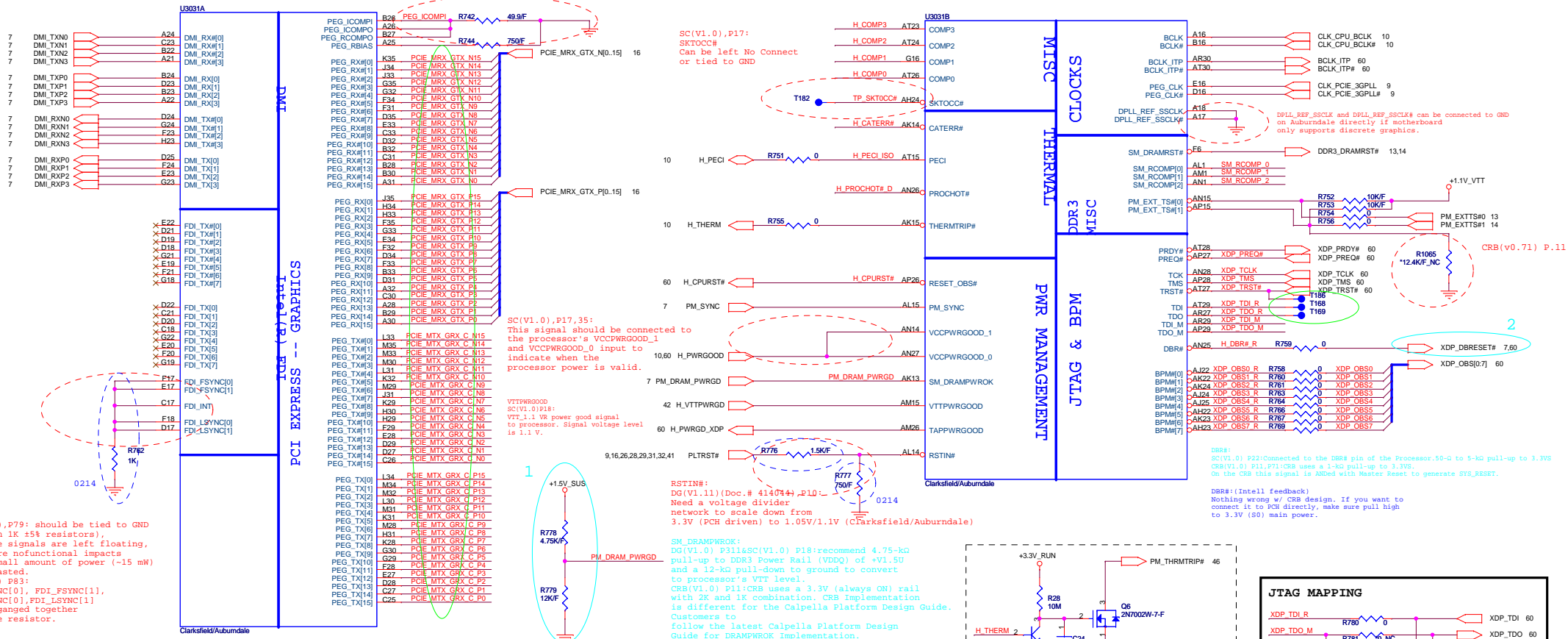
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AUBURNDALE/CLARKSFIELD PROCESSOR (DMI, PEG, FDI)

AUBURNDALE/CLARKSFIELD PROCESSOR (CLK, MISC, JTAG)

SC(V1.0),P11: Should be shorted at the pins and then routed to one end of the 49.9-Q ±1% resistor, pulled-down to GND on the board.

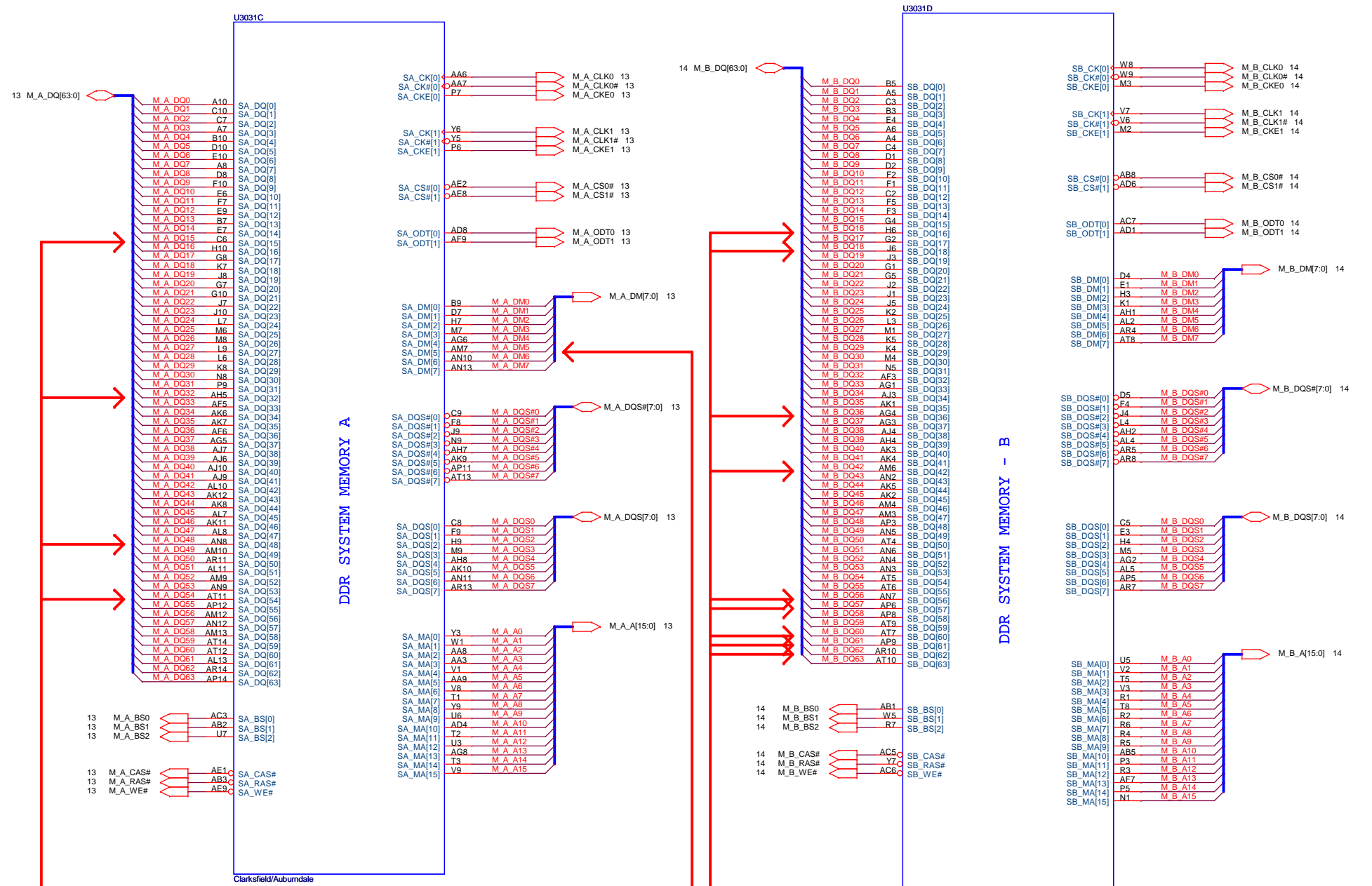


JTAG MAPPING

XDP_TDI_R	R780	0	XDP_TDI	60
XDP_TDO_M	R781	0	XDP_TDO	60
XDP_TDI_M	R785	0	XDP_TRST#	51
XDP_TDO_R	R786	0		


Sea# Chain (Default)	STUFF -> R780, R783, R786 NO STUFF -> R781, R785
CPU Only	STUFF -> R780, R781 NO STUFF -> R783, R785, R786
GMCH Only	STUFF -> R785, R786 NO STUFF -> R780, R781, R783

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



Channel A DQ[15,32,48,54], DM[5]
Requires minimum 12mils spacing
with all other signals, including data signals.

Channel B DQ[16,18,36,42,56,57,60,61,62]
Requires minimum 12mils spacing
with all other signals, including data signals.



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AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)

CPU Core Power

- AG35 VCC1
- AG34 VCC2
- AG33 VCC3
- AG32 VCC4
- AG31 VCC5
- AG30 VCC6
- AG29 VCC7
- AG28 VCC8
- AG27 VCC9
- AG26 VCC10
- AF35 VCC11
- AF34 VCC12
- AF33 VCC13
- AF32 VCC14
- AF31 VCC15
- AF30 VCC16
- AF29 VCC17
- AF28 VCC18
- AF27 VCC19
- AF26 VCC20
- AD35 VCC21
- AD34 VCC22
- AD33 VCC23
- AD32 VCC24
- AD31 VCC25
- AD30 VCC26
- AD29 VCC27
- AD28 VCC28
- AD27 VCC29
- AD26 VCC30
- AC35 VCC31
- AC34 VCC32
- AC33 VCC33
- AC32 VCC34
- AC31 VCC35
- AC30 VCC36
- AC29 VCC37
- AC28 VCC38
- AC27 VCC39
- AC26 VCC40
- AA35 VCC41
- AA34 VCC42
- AA33 VCC43
- AA32 VCC44
- AA31 VCC45
- AA30 VCC46
- AA29 VCC47
- AA28 VCC48
- AA27 VCC49
- AA26 VCC50
- Y35 VCC51
- Y34 VCC52
- Y33 VCC53
- Y32 VCC54
- Y31 VCC55
- Y30 VCC56
- Y29 VCC57
- Y28 VCC58
- Y27 VCC59
- Y26 VCC60
- VCC61
- VCC62
- VCC63
- V31 VCC64
- V30 VCC65
- V29 VCC66
- V28 VCC67
- V27 VCC68
- V26 VCC69
- V25 VCC70
- VCC71
- VCC72
- VCC73
- VCC74
- VCC75
- VCC76
- VCC77
- VCC78
- VCC79
- VCC80
- R35 VCC81
- R34 VCC82
- R33 VCC83
- R32 VCC84
- R31 VCC85
- R30 VCC86
- R29 VCC87
- R28 VCC88
- R27 VCC89
- R26 VCC90
- P35 VCC91
- P34 VCC92
- P33 VCC93
- P32 VCC94
- P31 VCC95
- P30 VCC96
- P29 VCC97
- P28 VCC98
- P27 VCC99
- P26 VCC100

AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)

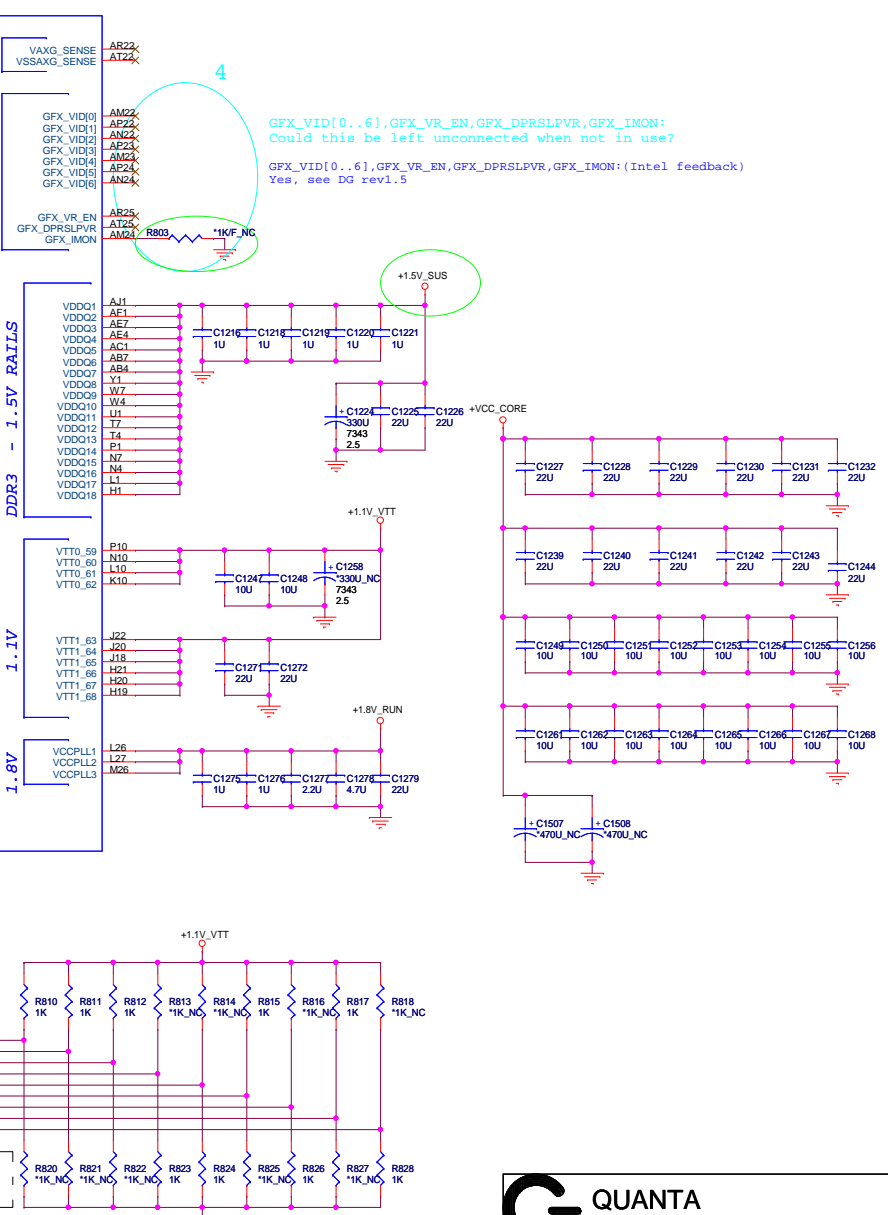
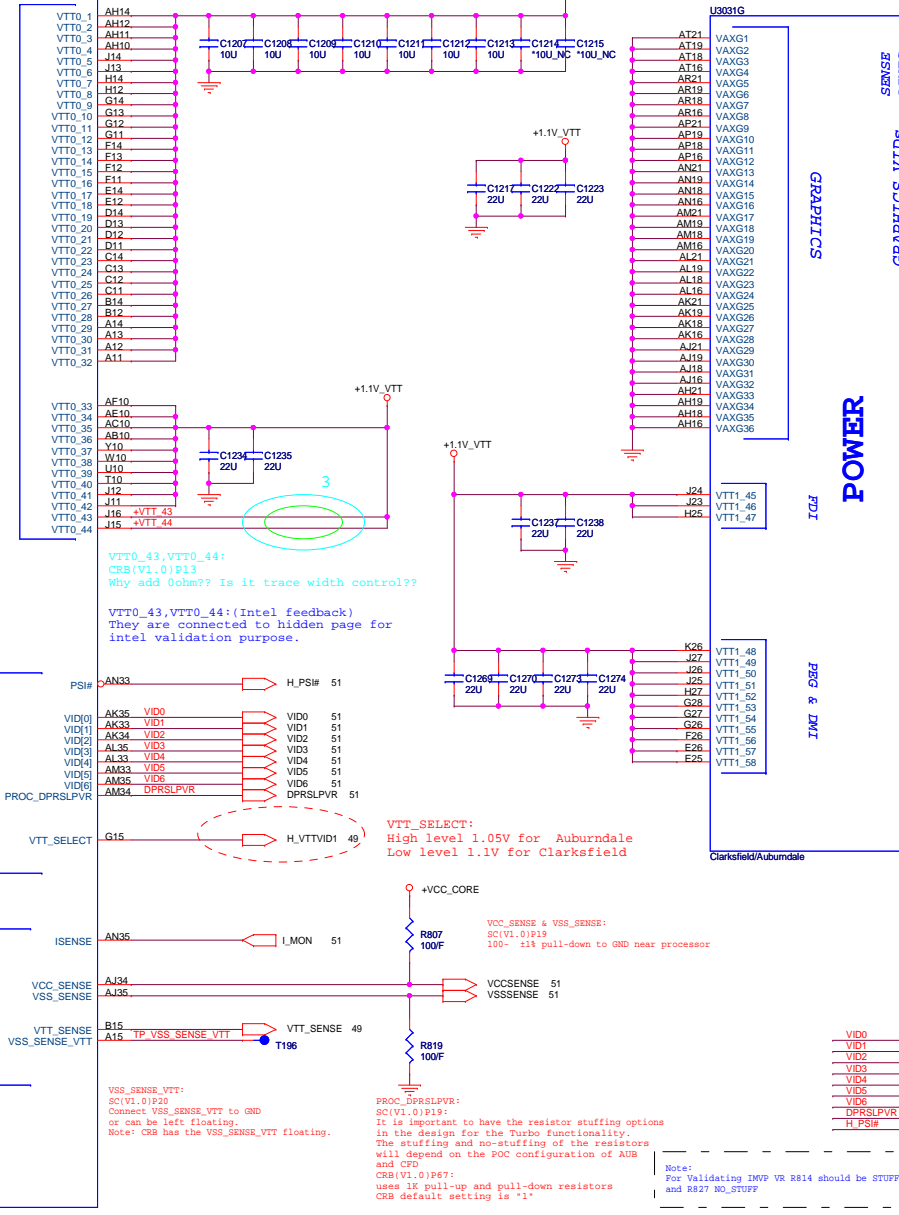
1.1V RAIL POWER

CPU CORE SUPPLY

CPU VIDS

POWER

SENSE VIDS



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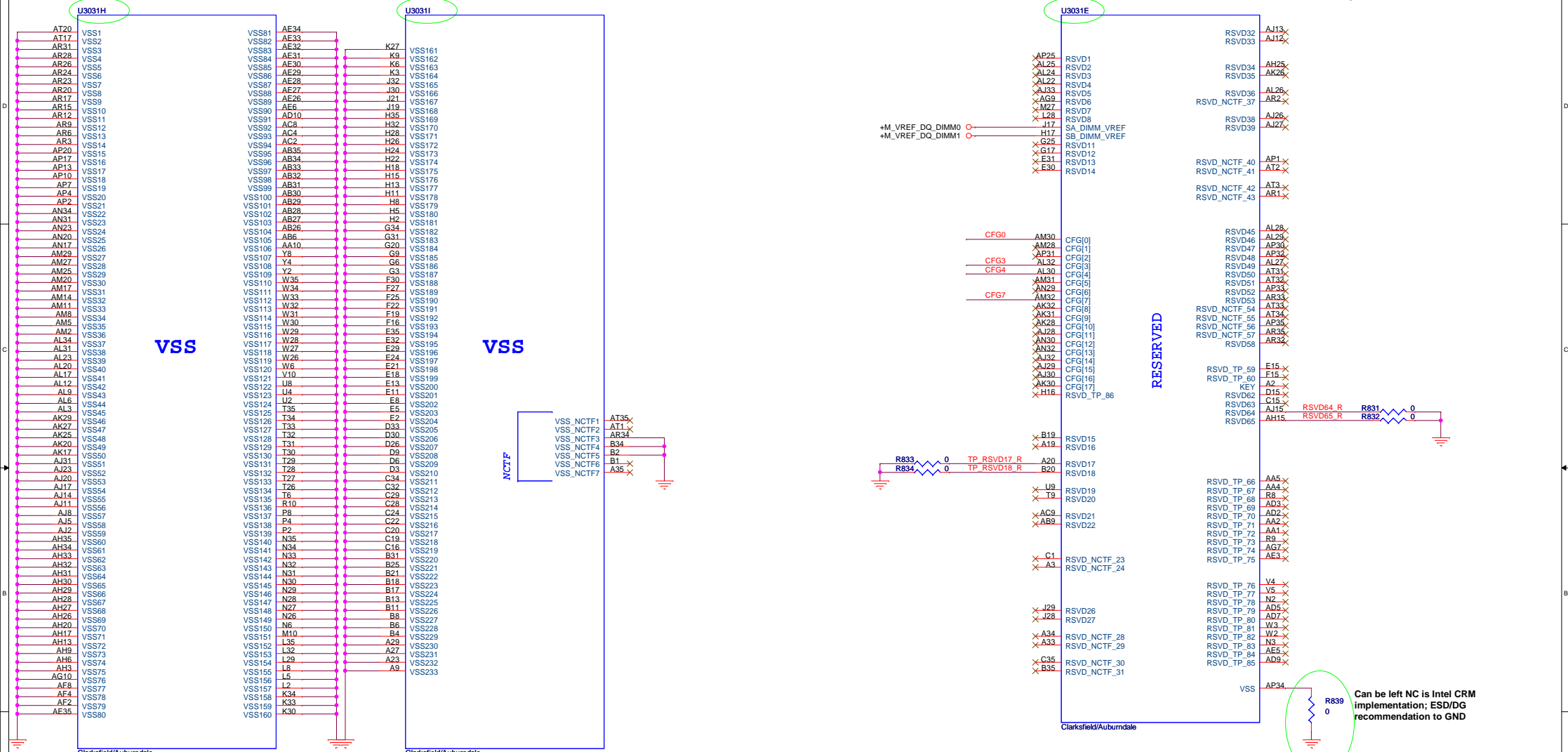
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AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

AUBURNDALE/CLARKSFIELD PROCESSOR (RESERVED, CFG)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.



PCIE LANE is Lane Numbers Reversed

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

QUANTA COMPUTER

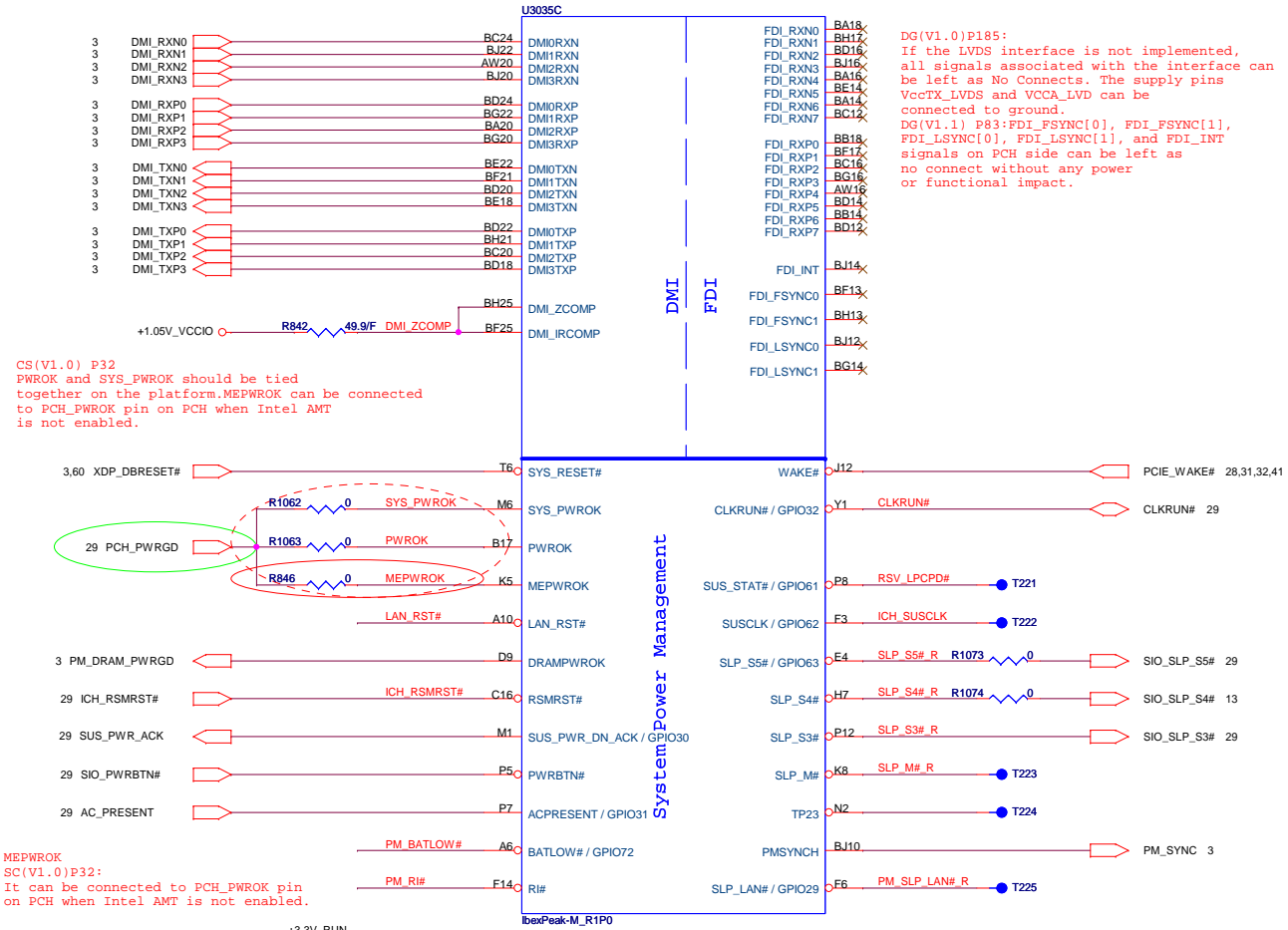
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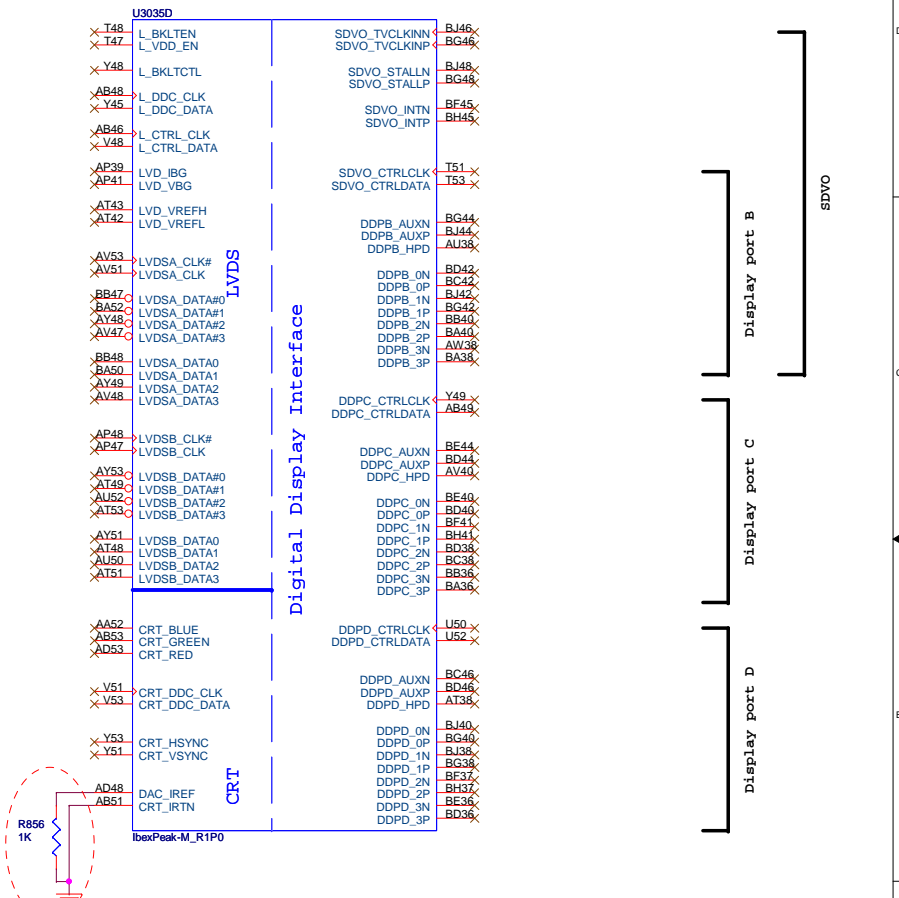
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IBEX PEAK-M (DMI, FDI, GPIO)

IBEX PEAK-M (LVDS, DDI)



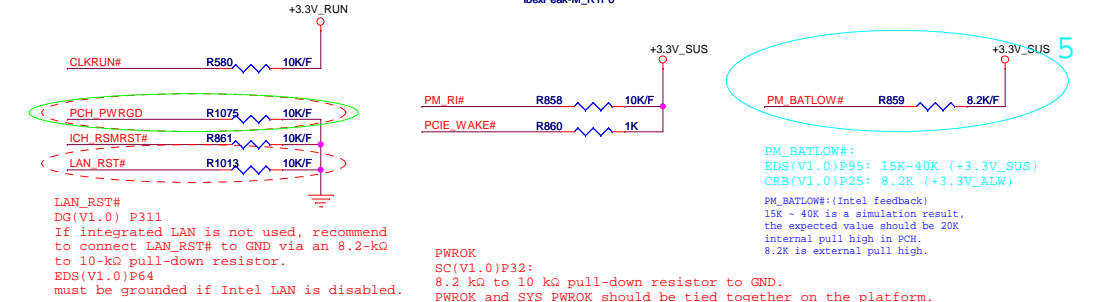
DG(V1.0)P185:
If the LVDS interface is not implemented, all signals associated with the interface can be left as No Connects. The supply pins VccTX_LVDS and VCCA_LVD can be connected to ground.
DG(V1.1) P83: FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT signals on PCH side can be left as no connect without any power or functional impact.



CS(V1.0) P32
PWROK and SYS_PWROK should be tied together on the platform. MEPWROK can be connected to PCH_PWROK pin on PCH when Intel AMT is not enabled.

MEPWROK
SC(V1.0)P32:
It can be connected to PCH_PWROK pin on PCH when Intel AMT is not enabled.

DG(V1.0)P189:
If the CRT interface is not implemented, all signals associated with the interface can be left as No Connects. The pins CRT_IRTN Connect this signals to GND and DAC_IREF Connect to GND via a 1.0 k \pm 0.5% pull-down resistor



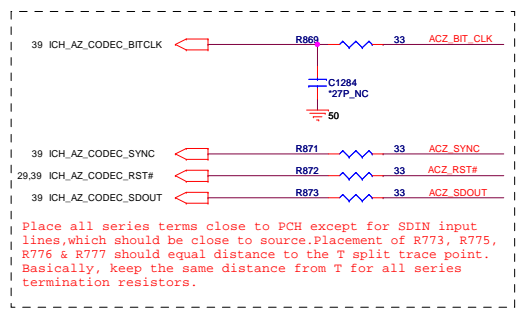
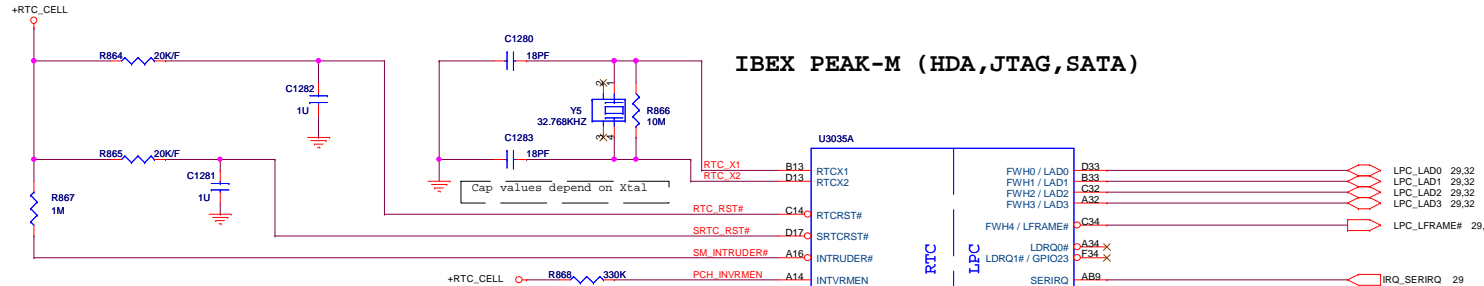
QUANTA COMPUTER

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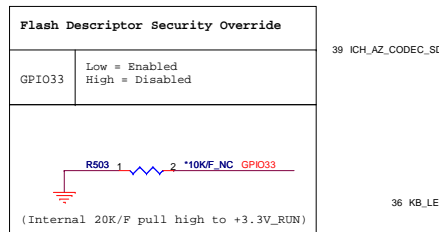
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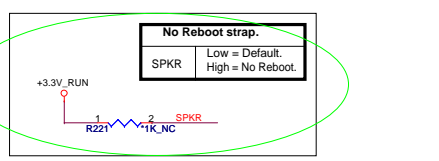
IBEX PEAK-M (HDA, JTAG, SATA)



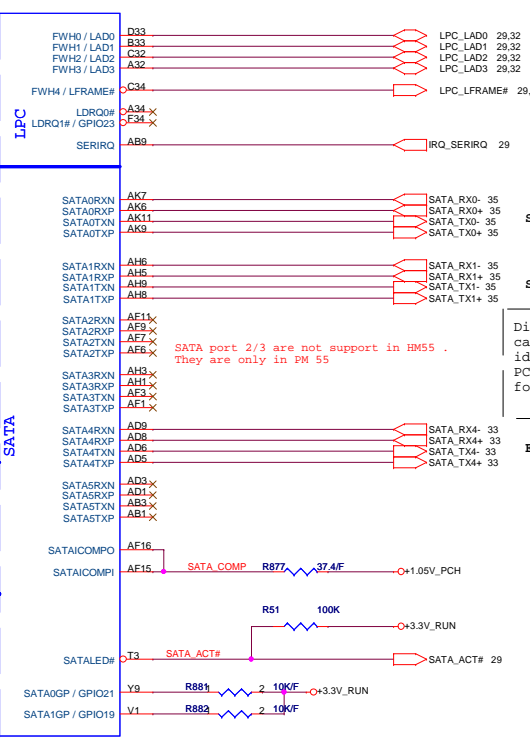
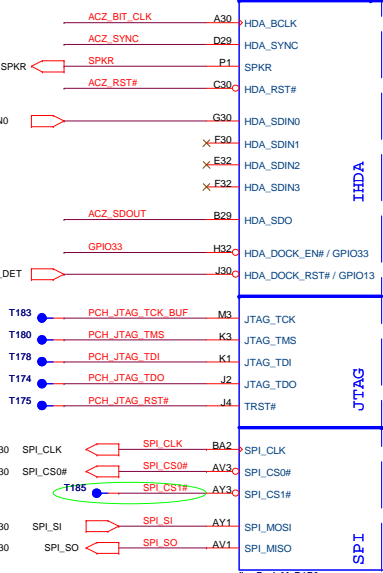
INTVRMEN (Internal Voltage Regulator Enable) :
This signal enables the internal 1.05 V regulators. This signal must be always pulled-up to VccRTC.



Note : GPIO33 is a signal used for Flash Descriptor Security Override/ME Debug Mode. This signal should be only asserted low through an external pull-down in manufacturing or debug environments ONLY.



JTAG
Test Pads are need to put on the same side of mother board.



SATA port 2/3 are not support in HM55 . They are only in PM 55

Distance between the PCH and cap on the "P" signal should be identical distance between the PCH and cap on the "N" signal for the same pair.

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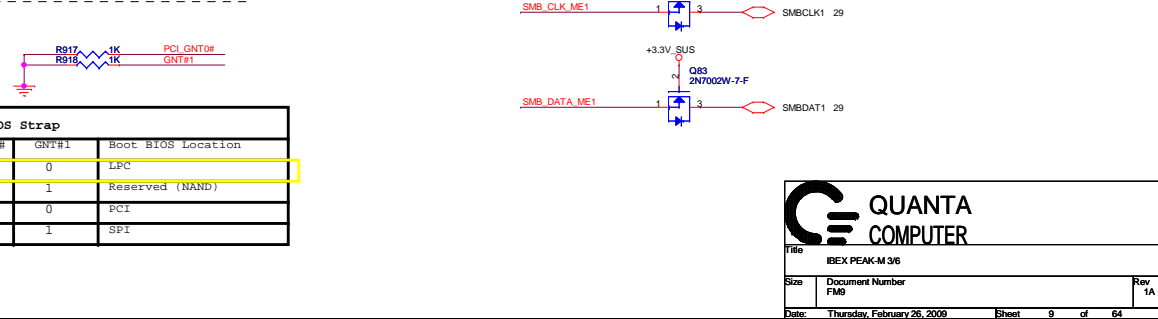
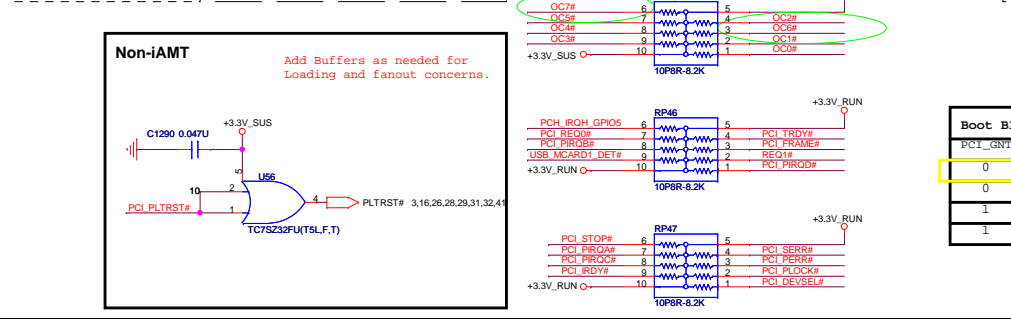
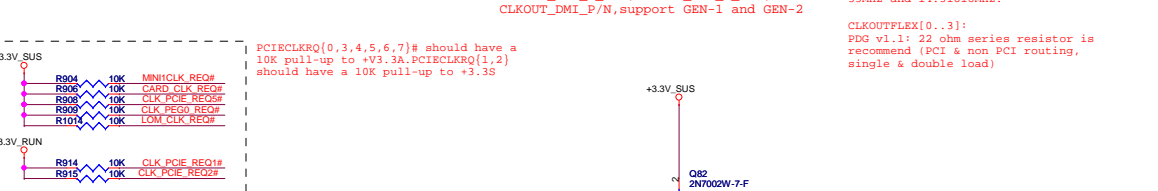
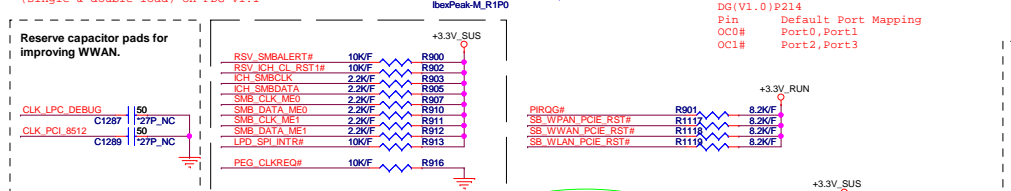
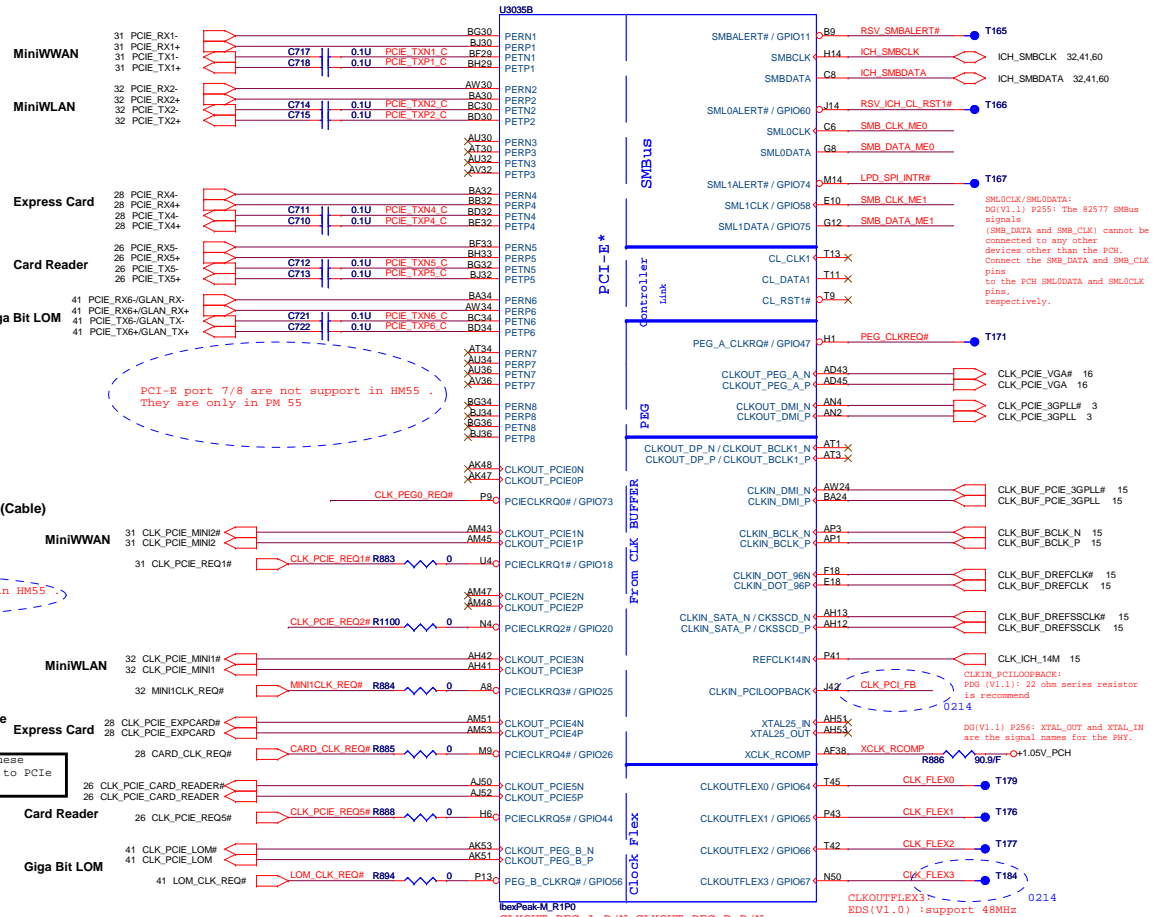
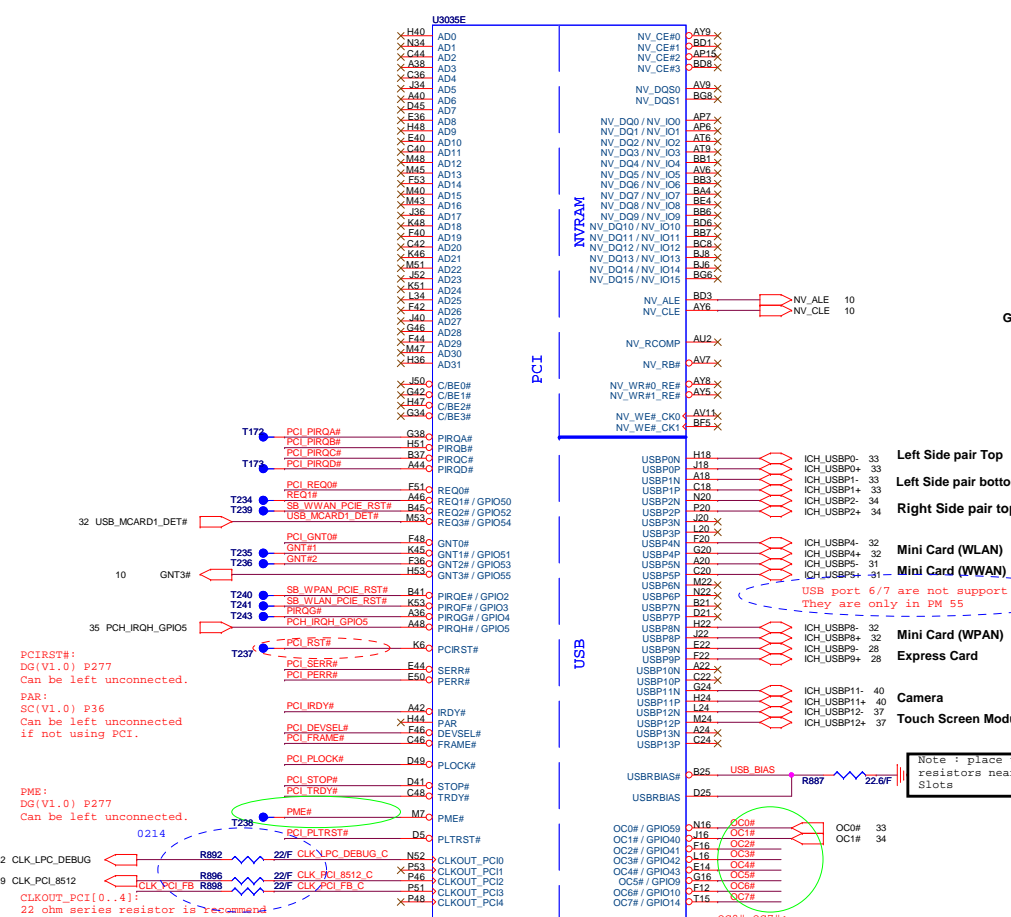
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IBEX PEAK-M (PCI,USB,NVRAM)

IBEX PEAK-M (PCI-E,SMBUS,CLK)

Place TX DC blocking caps close PCH.



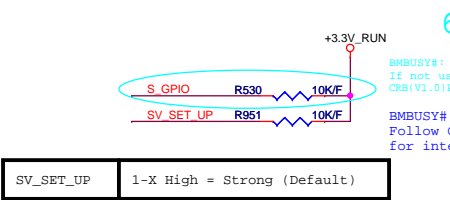
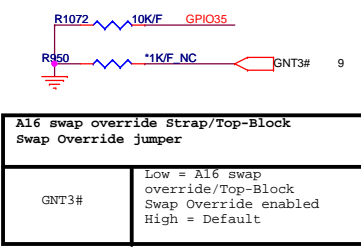
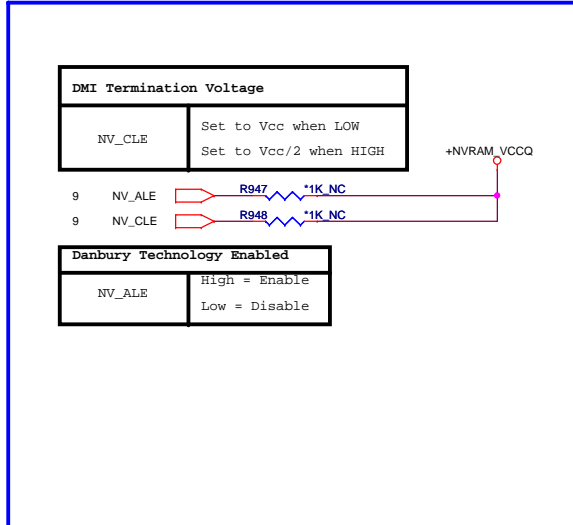
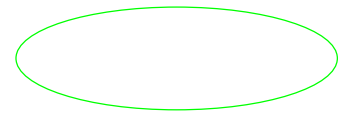
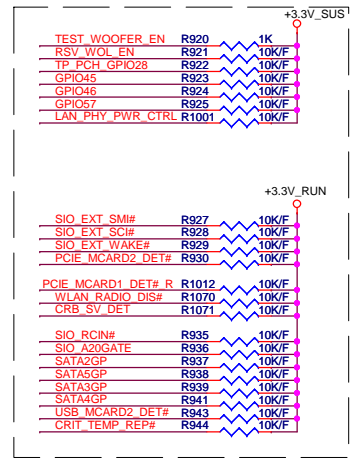
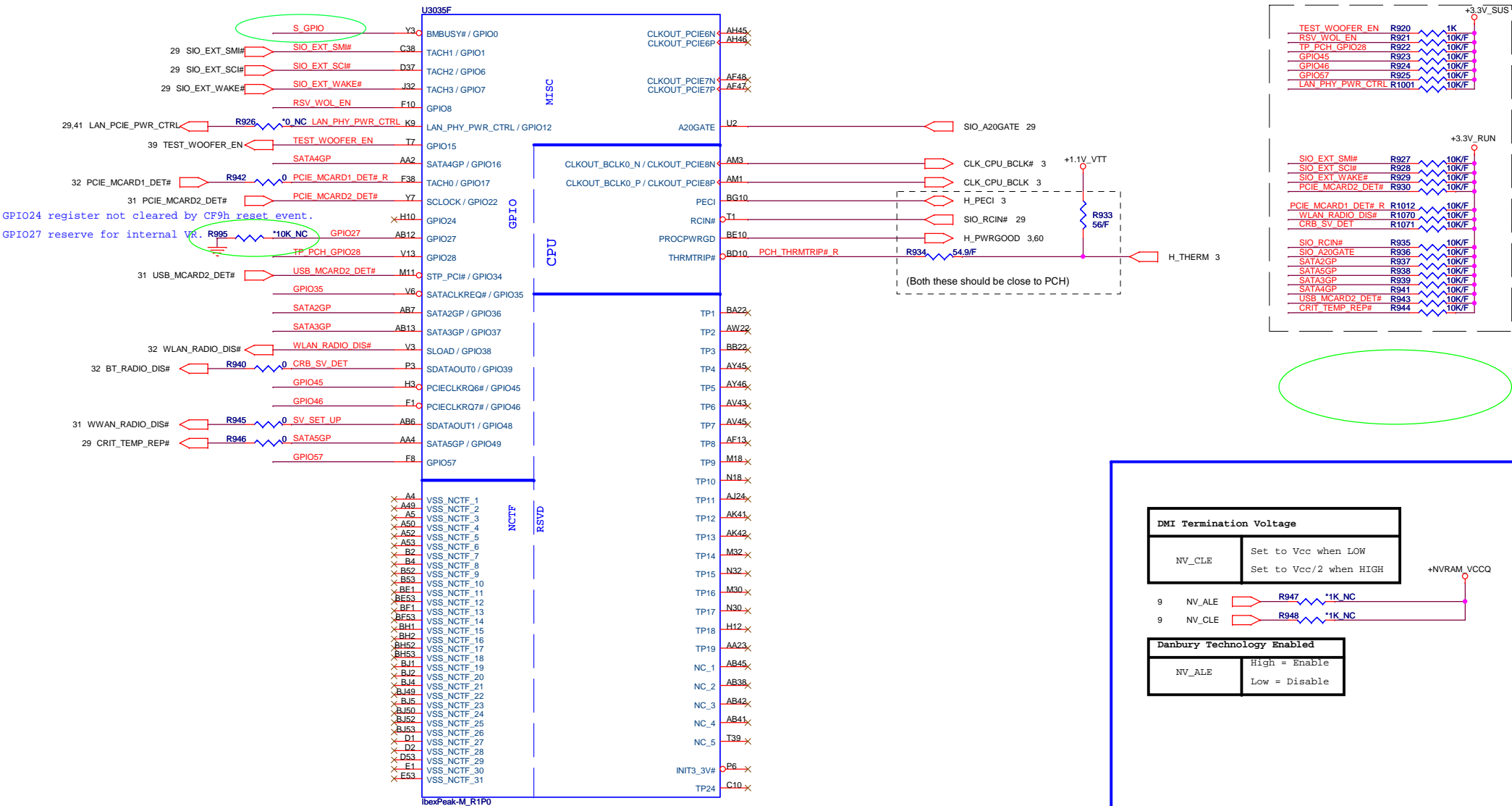
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IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



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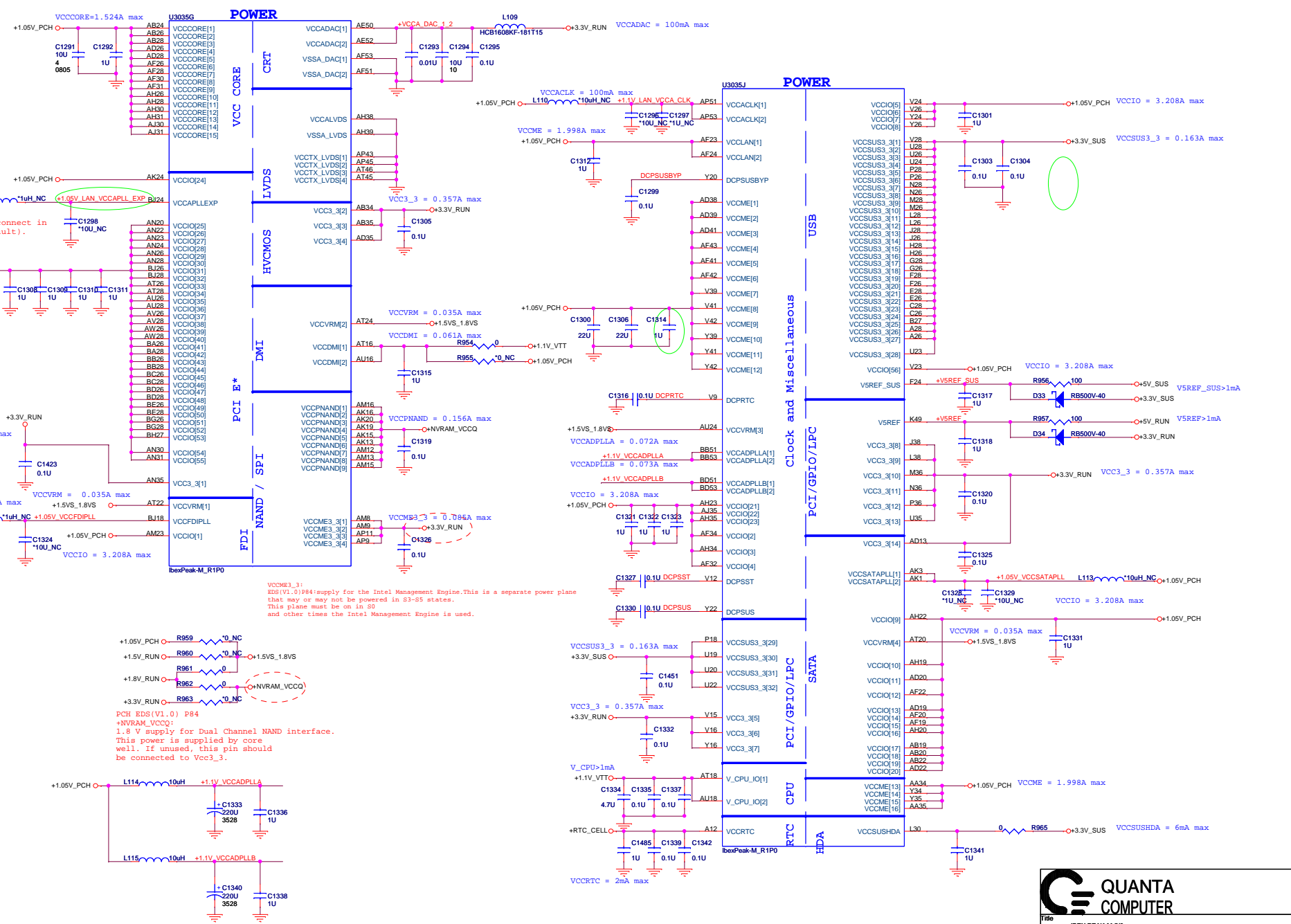
BMBUSY#:
If not used, require a weak pull-up (8.2- KΩ to 10 kΩ) to Vcc3.3.
CRB(V1.0)P28: it has 1K PU and 100 ohm on this net for validation purpose.

BMBUSY#:(Intel feedback)
Follow CRB checklist, 1K is for intel BIOS validation purpose.

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IBEX PEAK-M (POWER)



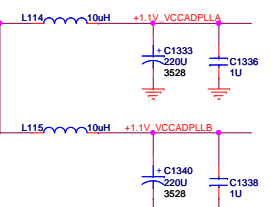
VCCAPLEXP = 100mA max
 This pin can be left as no connect in On-Die VR enabled mode (default).

VCCIO = 3.208A max
 VCCIO[24] AK24
 VCCIO[25] AN20
 VCCIO[26] AN22
 VCCIO[27] AN23
 VCCIO[28] AN26
 VCCIO[29] AN28
 VCCIO[30] BI26
 VCCIO[31] BI28
 VCCIO[32] AT26
 VCCIO[33] AU28
 VCCIO[34] AU28
 VCCIO[35] AU28
 VCCIO[36] AU28
 VCCIO[37] AV26
 VCCIO[38] AV28
 VCCIO[39] AW26
 VCCIO[40] AW28
 VCCIO[41] BA26
 VCCIO[42] BA28
 VCCIO[43] BC26
 VCCIO[44] BC28
 VCCIO[45] BD26
 VCCIO[46] BD28
 VCCIO[47] BE26
 VCCIO[48] BE28
 VCCIO[49] BG26
 VCCIO[50] BG28
 VCCIO[51] BH27
 VCCIO[52] AN30
 VCCIO[54] AN31
 VCCIO[55] AN31

VCCM3_3:
 EDS(V1.0)P84 supply for the Intel Management Engine. This is a separate power plane that may or may not be powered in S3-S5 states. This plane must be on in S0 and other times the Intel Management Engine is used.

VCCVCRM = 0.035A max
 VCCFDIPLL = 100mA max
 VCCSUS3_3 = 0.163A max
 VCCME = 1.998A max
 VCCSUS_HDA = 6mA max

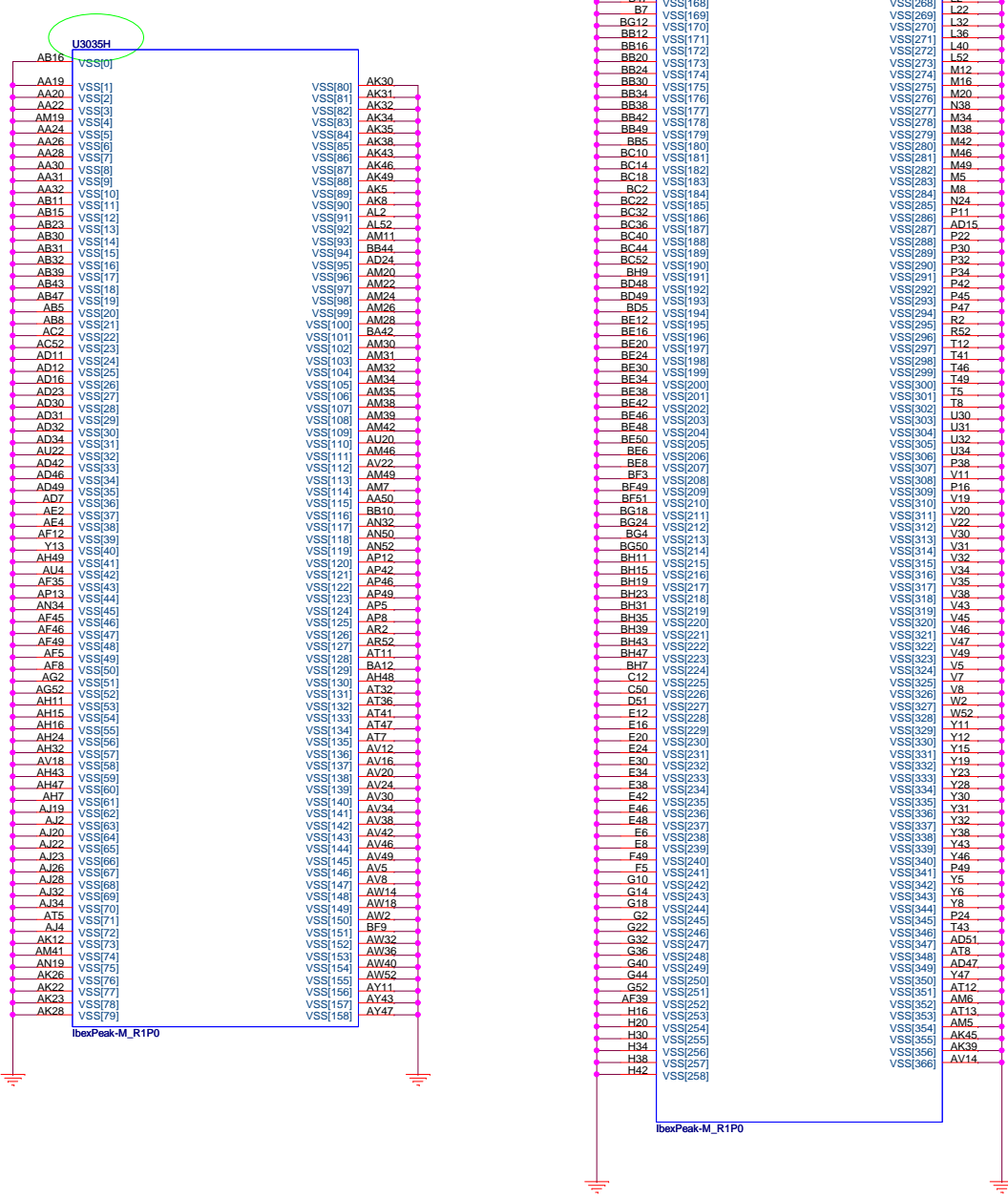
PCH EDS(V1.0) P84
 +NVRAM_VCCQ:
 1.8 V supply for Dual Channel NAND interface. This power is supplied by core well. If unused, this pin should be connected to Vcc3_3.



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IBEX PEAK-M (GND)

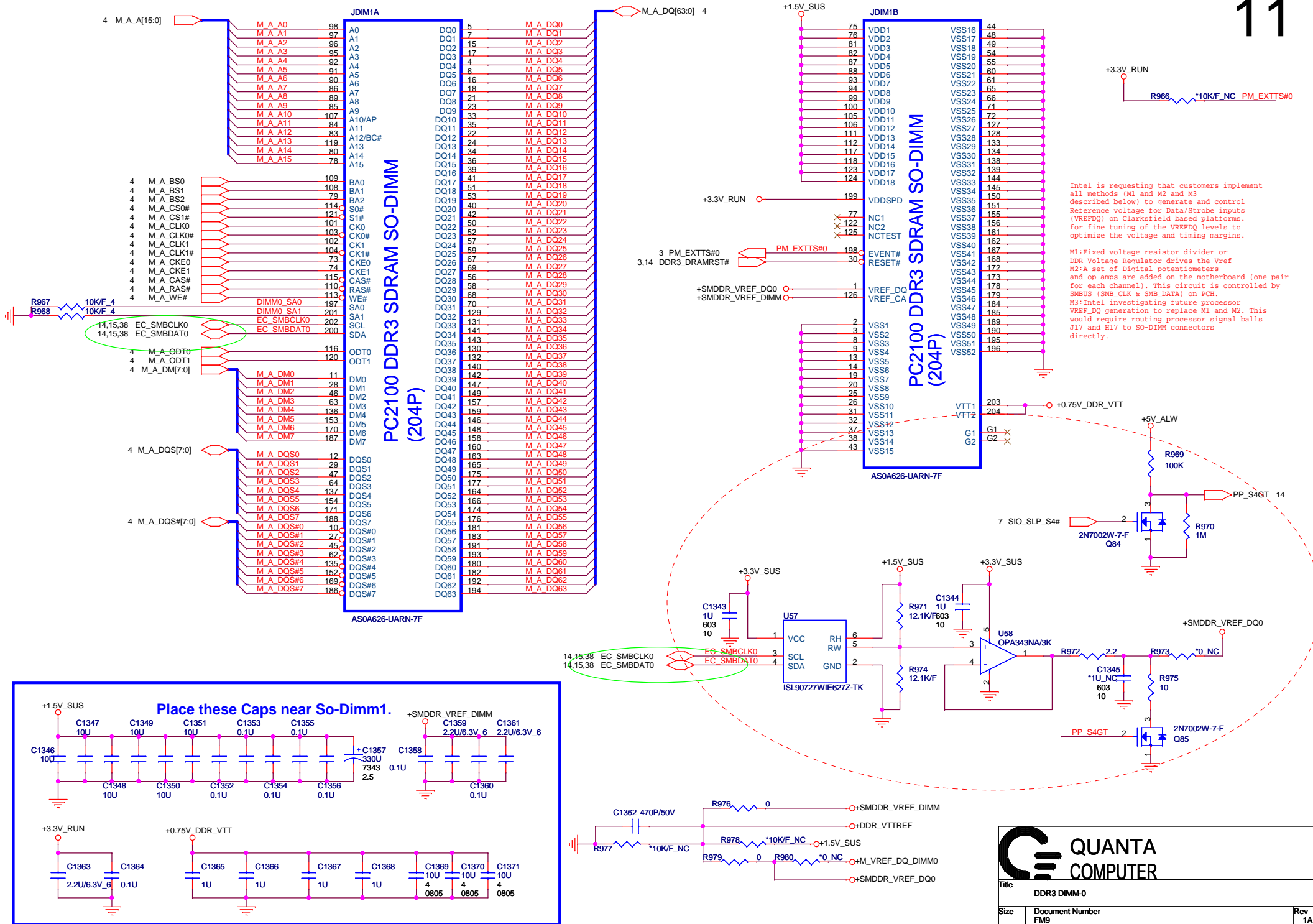


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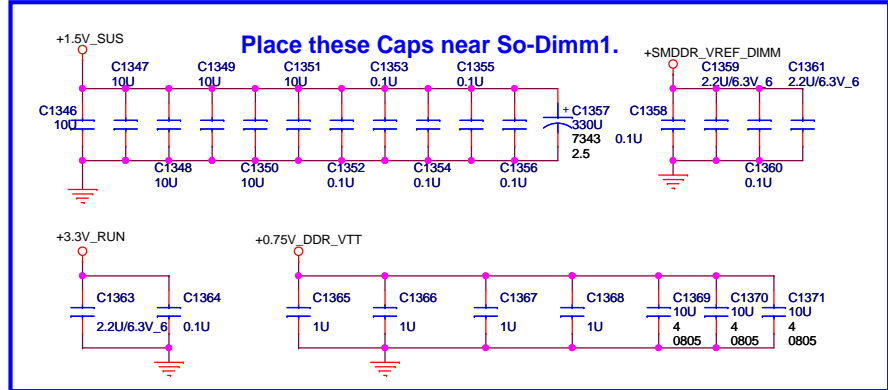
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Intel is requesting that customers implement all methods (M1 and M2 and M3 described below) to generate and control Reference voltage for Data/Strobe inputs (VREFPQ) on Clarksfield based platforms. for fine tuning of the VREFPQ levels to optimize the voltage and timing margins.

M1: Fixed voltage resistor divider or DDR Voltage Regulator drives the Vref
M2: A set of Digital potentiometers and op amps are added on the motherboard (one pair for each channel). This circuit is controlled by SMBUS (SMB_CLK & SMB_DATA) on PCB.
M3: Intel investigating future processor VREFPQ generation to replace M1 and M2. This would require routing processor signal balls J17 and H17 to SO-DIMM connectors directly.

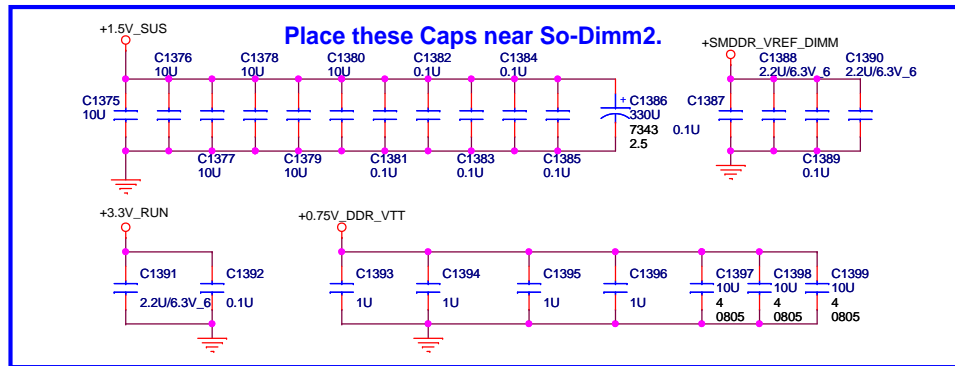
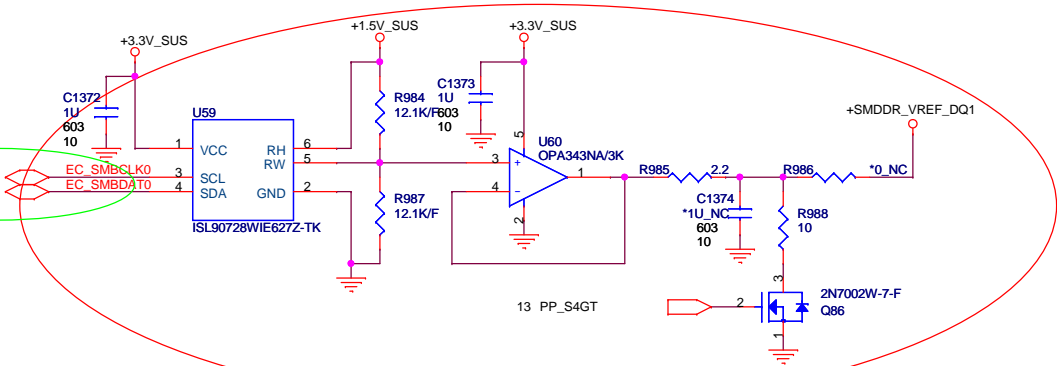
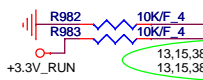
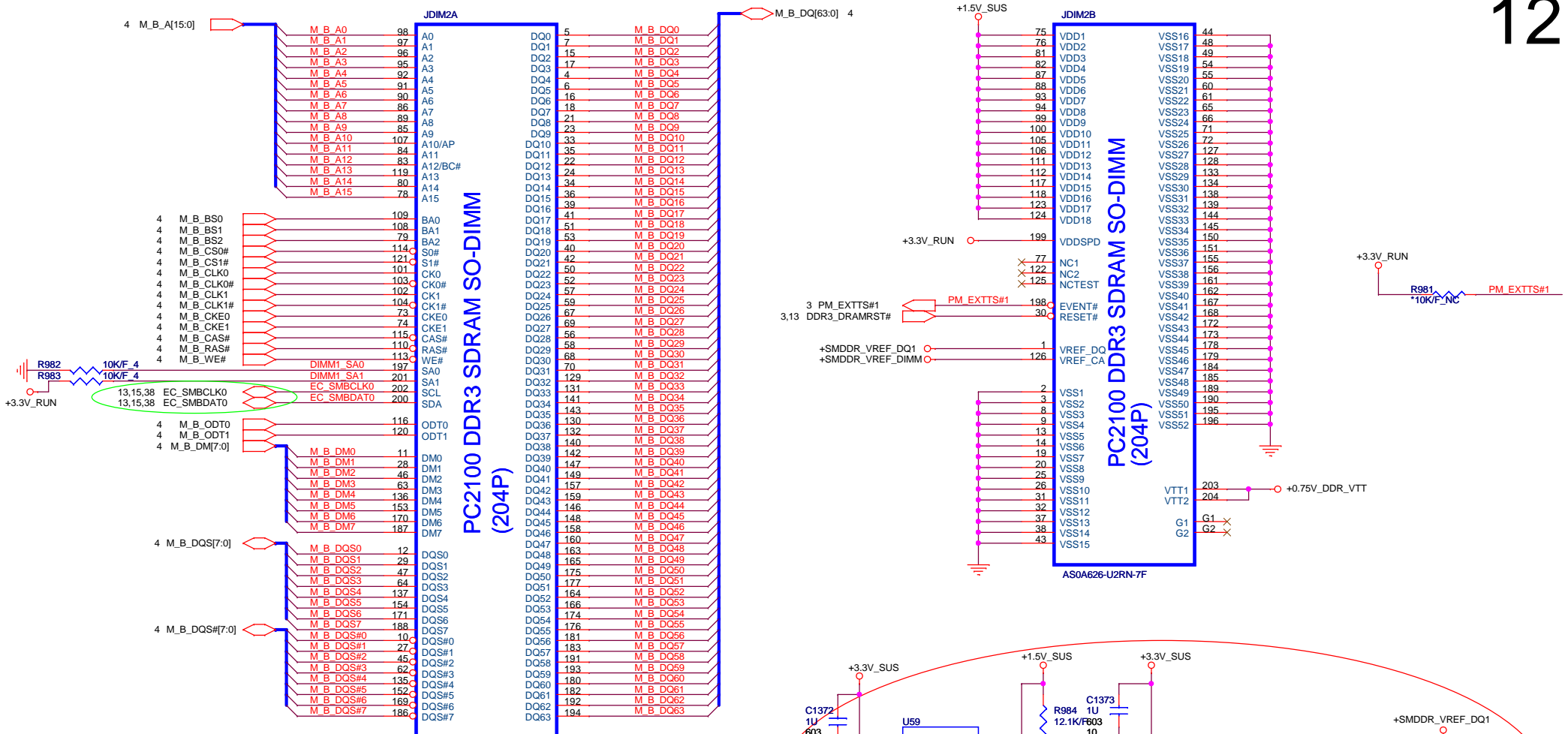


QUANTA COMPUTER

Title: DDR3 DIMM-0

Size	Document Number FM9	Rev 1A
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Date: Thursday, February 26, 2009 Sheet 13 of 64



QUANTA COMPUTER

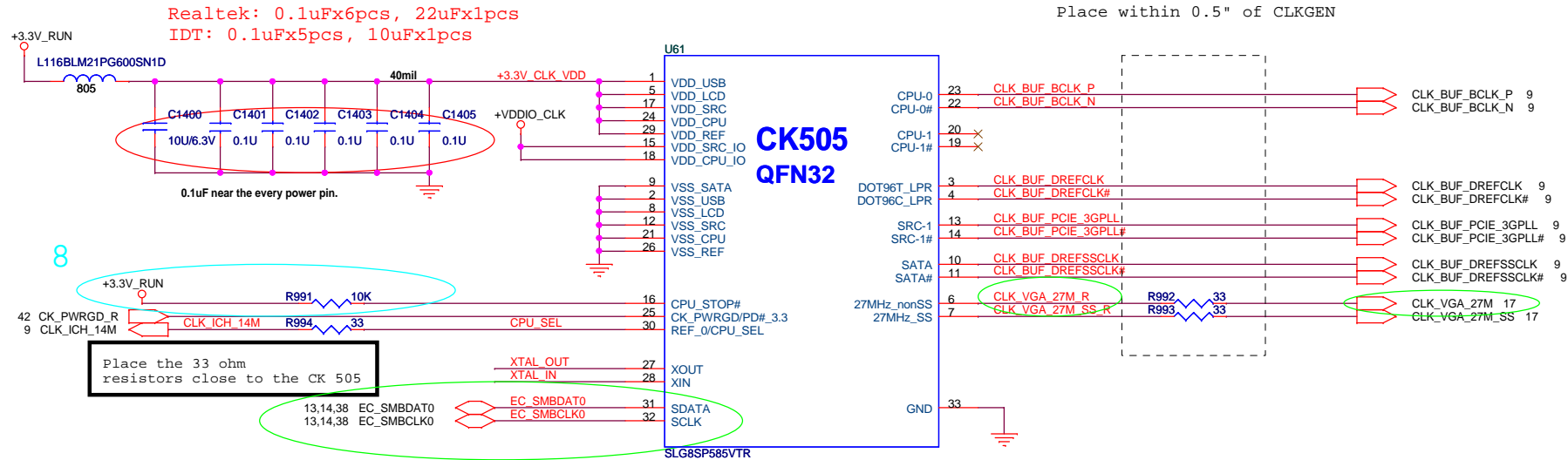
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Size: Document Number FM9

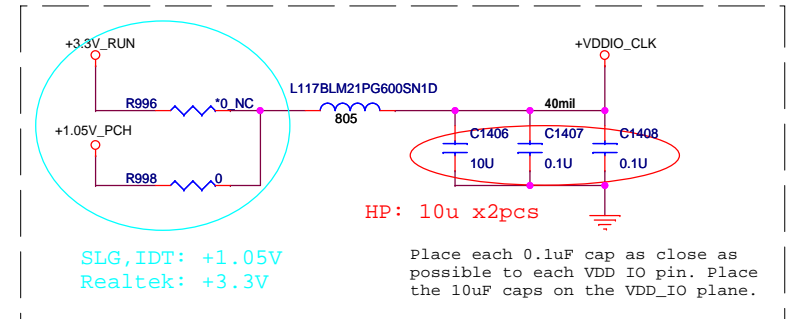
Date: Thursday, February 26, 2009

Sheet: 14 of 64

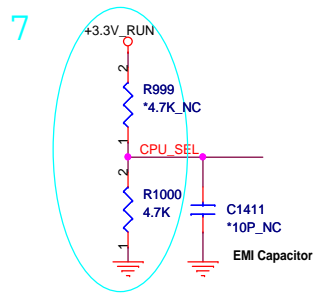
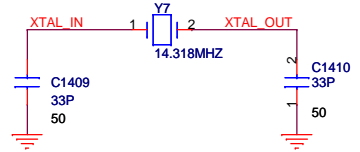
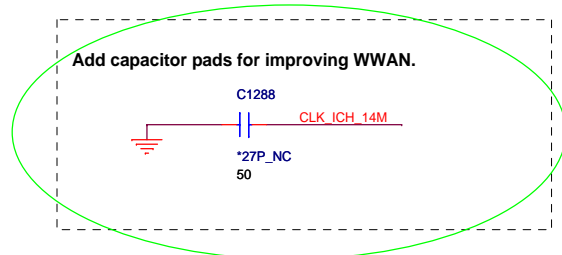
Rev: 1A



Realtex: 0.1uF x 3 pcs, 22uF x 1 pcs
 IDT: 0.1uF x 2 pcs, 10uF x 1 pcs



+VDDIO_CLK:
 SLG date sheet (V0.2) P15: Min 1.05V, Max 3.465V.
 Realtex date sheet (V1.2) P11: Min 1.05V, Max 3.3V.
 IDT date sheet (V0.7) P10: Min 0.9975V, Max 3.465V.



PIN 30	CPU_0	CPU_1
0 (default)	133MHz	133MHz
1 (0.7V-1.5V)	100MHz	100MHz

CPU_SEL:
 SLG date sheet (V0.2) P15:
 High Voltage: Min 0.7V, Max 1.5V.
 Low Voltage: Min Vss-0.3V, Max 0.35V.
 Realtex date sheet (V1.2) P11:
 High Voltage: Min 0.7V, Max 1.5V.
 Low Voltage: Min Vss-0.3V, Max 0.35V.
 IDT date sheet (V0.7) P10:
 High Voltage: Min 0.7V, Max 1.5V.
 Low Voltage: Min Vss-0.3V, Max 0.35V.

3 PCIE_MTX_GRX_P[0..15]
3 PCIE_MTX_GRX_N[0..15]

3 PCIE_MRX_GTX_P[0..15]
3 PCIE_MRX_GTX_N[0..15]

U32A

PART 1 OF 10

PCI-EXPRESS INTERFACE

PCIE_MTX_GRX_P0	AF30	PCIE_RX0P
PCIE_MTX_GRX_N0	AE31	PCIE_RX0N
PCIE_MTX_GRX_P1	AE29	PCIE_RX1P
PCIE_MTX_GRX_N1	AD28	PCIE_RX1N
PCIE_MTX_GRX_P2	AD30	PCIE_RX2P
PCIE_MTX_GRX_N2	AC31	PCIE_RX2N
PCIE_MTX_GRX_P3	AC29	PCIE_RX3P
PCIE_MTX_GRX_N3	AB28	PCIE_RX3N
PCIE_MTX_GRX_P4	AB30	PCIE_RX4P
PCIE_MTX_GRX_N4	AA31	PCIE_RX4N
PCIE_MTX_GRX_P5	AA29	PCIE_RX5P
PCIE_MTX_GRX_N5	Y28	PCIE_RX5N
PCIE_MTX_GRX_P6	Y30	PCIE_RX6P
PCIE_MTX_GRX_N6	W31	PCIE_RX6N
PCIE_MTX_GRX_P7	W29	PCIE_RX7P
PCIE_MTX_GRX_N7	V28	PCIE_RX7N
PCIE_MTX_GRX_P8	V30	PCIE_RX8P
PCIE_MTX_GRX_N8	U31	PCIE_RX8N
PCIE_MTX_GRX_P9	U29	PCIE_RX9P
PCIE_MTX_GRX_N9	T28	PCIE_RX9N
PCIE_MTX_GRX_P10	T30	PCIE_RX10P
PCIE_MTX_GRX_N10	R31	PCIE_RX10N
PCIE_MTX_GRX_P11	R29	PCIE_RX11P
PCIE_MTX_GRX_N11	P28	PCIE_RX11N
PCIE_MTX_GRX_P12	P30	PCIE_RX12P
PCIE_MTX_GRX_N12	N31	PCIE_RX12N
PCIE_MTX_GRX_P13	N29	PCIE_RX13P
PCIE_MTX_GRX_N13	M28	PCIE_RX13N
PCIE_MTX_GRX_P14	M30	PCIE_RX14P
PCIE_MTX_GRX_N14	L31	PCIE_RX14N
PCIE_MTX_GRX_P15	L29	PCIE_RX15P
PCIE_MTX_GRX_N15	K30	PCIE_RX15N

PCIE_TX0P	AH30	PCIE_MRX_GTX_C_P0
PCIE_TX0N	AG31	PCIE_MRX_GTX_C_N0
PCIE_TX1P	AG29	PCIE_MRX_GTX_C_P1
PCIE_TX1N	AF28	PCIE_MRX_GTX_C_N1
PCIE_TX2P	AF27	PCIE_MRX_GTX_C_P2
PCIE_TX2N	AF26	PCIE_MRX_GTX_C_N2
PCIE_TX3P	AD27	PCIE_MRX_GTX_C_P3
PCIE_TX3N	AD26	PCIE_MRX_GTX_C_N3
PCIE_TX4P	AC25	PCIE_MRX_GTX_C_P4
PCIE_TX4N	AB25	PCIE_MRX_GTX_C_N4
PCIE_TX5P	Y23	PCIE_MRX_GTX_C_P5
PCIE_TX5N	Y24	PCIE_MRX_GTX_C_N5
PCIE_TX6P	AB27	PCIE_MRX_GTX_C_P6
PCIE_TX6N	AB26	PCIE_MRX_GTX_C_N6
PCIE_TX7P	Y27	PCIE_MRX_GTX_C_P7
PCIE_TX7N	Y26	PCIE_MRX_GTX_C_N7
PCIE_TX8P	W24	PCIE_MRX_GTX_C_P8
PCIE_TX8N	W23	PCIE_MRX_GTX_C_N8
PCIE_TX9P	V27	PCIE_MRX_GTX_C_P9
PCIE_TX9N	U26	PCIE_MRX_GTX_C_N9
PCIE_TX10P	U24	PCIE_MRX_GTX_C_P10
PCIE_TX10N	U23	PCIE_MRX_GTX_C_N10
PCIE_TX11P	T26	PCIE_MRX_GTX_C_P11
PCIE_TX11N	T27	PCIE_MRX_GTX_C_N11
PCIE_TX12P	T24	PCIE_MRX_GTX_C_P12
PCIE_TX12N	T23	PCIE_MRX_GTX_C_N12
PCIE_TX13P	P27	PCIE_MRX_GTX_C_P13
PCIE_TX13N	P26	PCIE_MRX_GTX_C_N13
PCIE_TX14P	P24	PCIE_MRX_GTX_C_P14
PCIE_TX14N	P23	PCIE_MRX_GTX_C_N14
PCIE_TX15P	M27	PCIE_MRX_GTX_C_P15
PCIE_TX15N	N26	PCIE_MRX_GTX_C_N15

PCIE_MRX_GTX_P0	0.1U	2	1	C814	10	PCIE_MRX_GTX_C_P0
PCIE_MRX_GTX_P1	0.1U	2	1	C815	10	PCIE_MRX_GTX_C_P1
PCIE_MRX_GTX_P2	0.1U	2	1	C816	10	PCIE_MRX_GTX_C_P2
PCIE_MRX_GTX_P3	0.1U	2	1	C817	10	PCIE_MRX_GTX_C_P3
PCIE_MRX_GTX_P4	0.1U	2	1	C818	10	PCIE_MRX_GTX_C_P4
PCIE_MRX_GTX_P5	0.1U	2	1	C819	10	PCIE_MRX_GTX_C_P5
PCIE_MRX_GTX_P6	0.1U	2	1	C820	10	PCIE_MRX_GTX_C_P6
PCIE_MRX_GTX_P7	0.1U	2	1	C821	10	PCIE_MRX_GTX_C_P7
PCIE_MRX_GTX_P8	0.1U	2	1	C822	10	PCIE_MRX_GTX_C_P8
PCIE_MRX_GTX_P9	0.1U	2	1	C823	10	PCIE_MRX_GTX_C_P9
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PCIE_MRX_GTX_N0	0.1U	2	1	C830	10	PCIE_MRX_GTX_C_N0
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PCIE_MRX_GTX_N8	0.1U	2	1	C838	10	PCIE_MRX_GTX_C_N8
PCIE_MRX_GTX_N9	0.1U	2	1	C839	10	PCIE_MRX_GTX_C_N9
PCIE_MRX_GTX_N10	0.1U	2	1	C840	10	PCIE_MRX_GTX_C_N10
PCIE_MRX_GTX_N11	0.1U	2	1	C841	10	PCIE_MRX_GTX_C_N11
PCIE_MRX_GTX_N12	0.1U	2	1	C842	10	PCIE_MRX_GTX_C_N12
PCIE_MRX_GTX_N13	0.1U	2	1	C843	10	PCIE_MRX_GTX_C_N13
PCIE_MRX_GTX_N14	0.1U	2	1	C844	10	PCIE_MRX_GTX_C_N14
PCIE_MRX_GTX_N15	0.1U	2	1	C845	10	PCIE_MRX_GTX_C_N15

100 MHz (+/-300 ppm) input frequency, 0-0.7 V single-ended swing.
clock must be provided less than 400ns
after CLKREQ# is asserted

9 CLK_PCIE_VGA AK30
9 CLK_PCIE_VGA# AK32

9, 26, 28, 29, 31, 32, 41 PLTRST# A27

M92-S2M92-XT

PCIE_CALRN AA22 PCIE_CALRN 2.0K R591
PCIE_CALRP Y22 PCIE_CALRP 1.27K R592

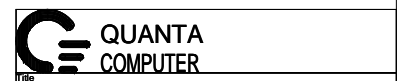
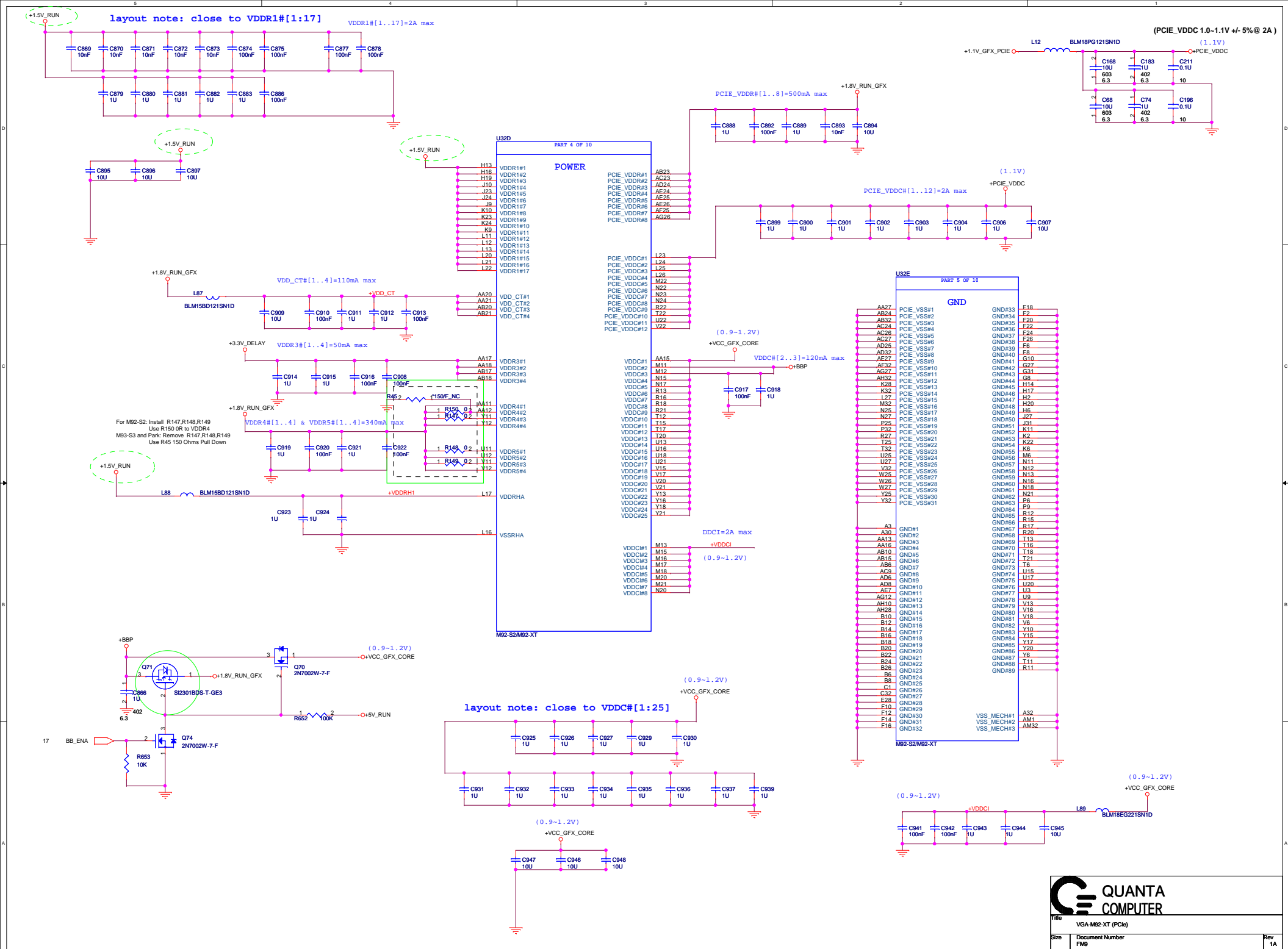
(1.1V)

+PCIE_VDDC

M92-S2 XT AJ072800T04 100-CG1675(216-0728004)
M92-S2 AJ072800T03 100-CG1643(216-0728003)



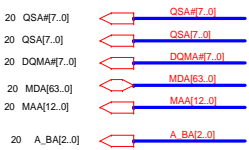
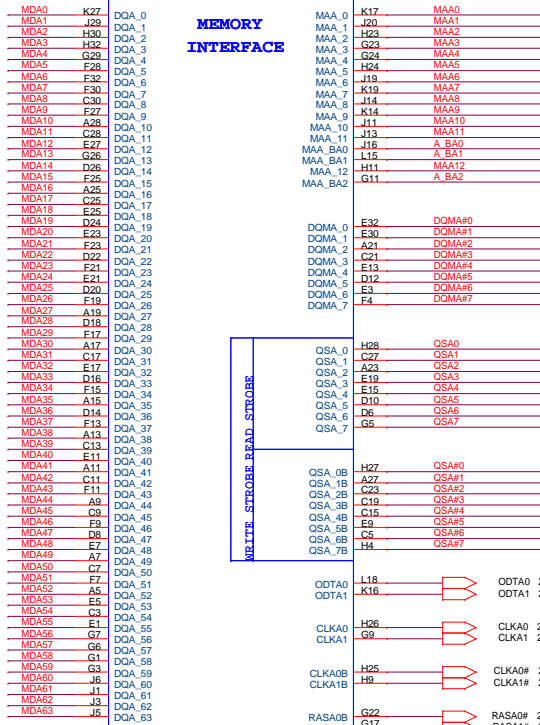
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VGA-M92-XT (PCIe)			1A
Size	Document Number		
	FM9		
Date:	Thursday, February 26, 2009	Sheet	16 of 64



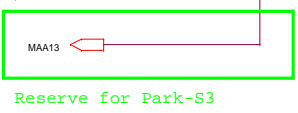
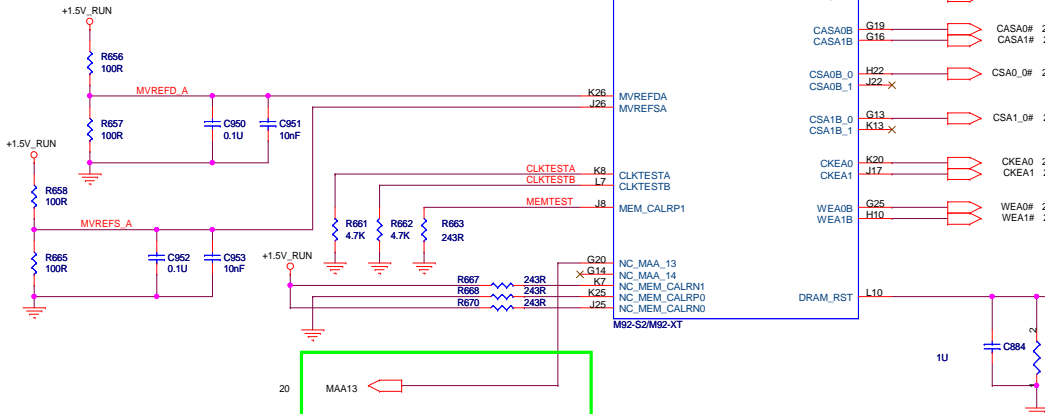
MEMORY INTERFACE

U32C

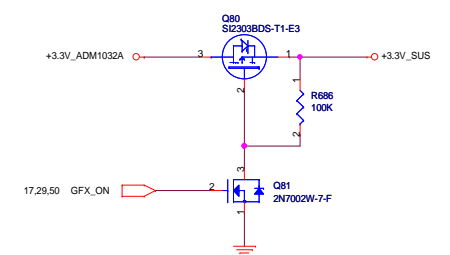
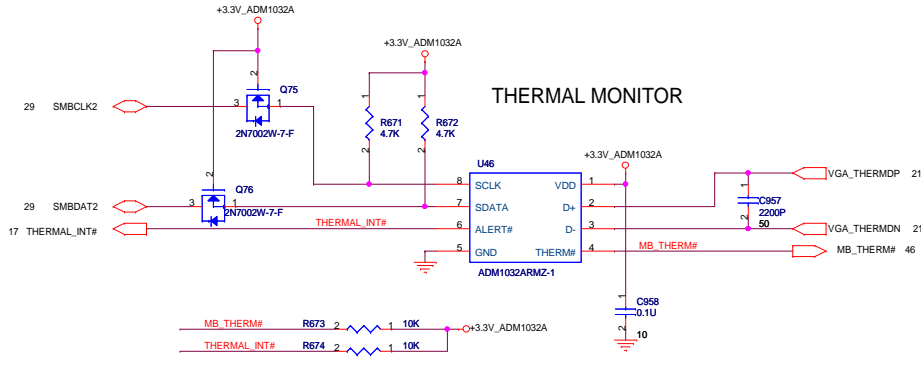
MEMORY INTERFACE



DIVIDER RESISTORS	DDR3
MVREF TO 1.5V	100R
MVREF TO GND	100R



WRITE STROBE PALL STROBE

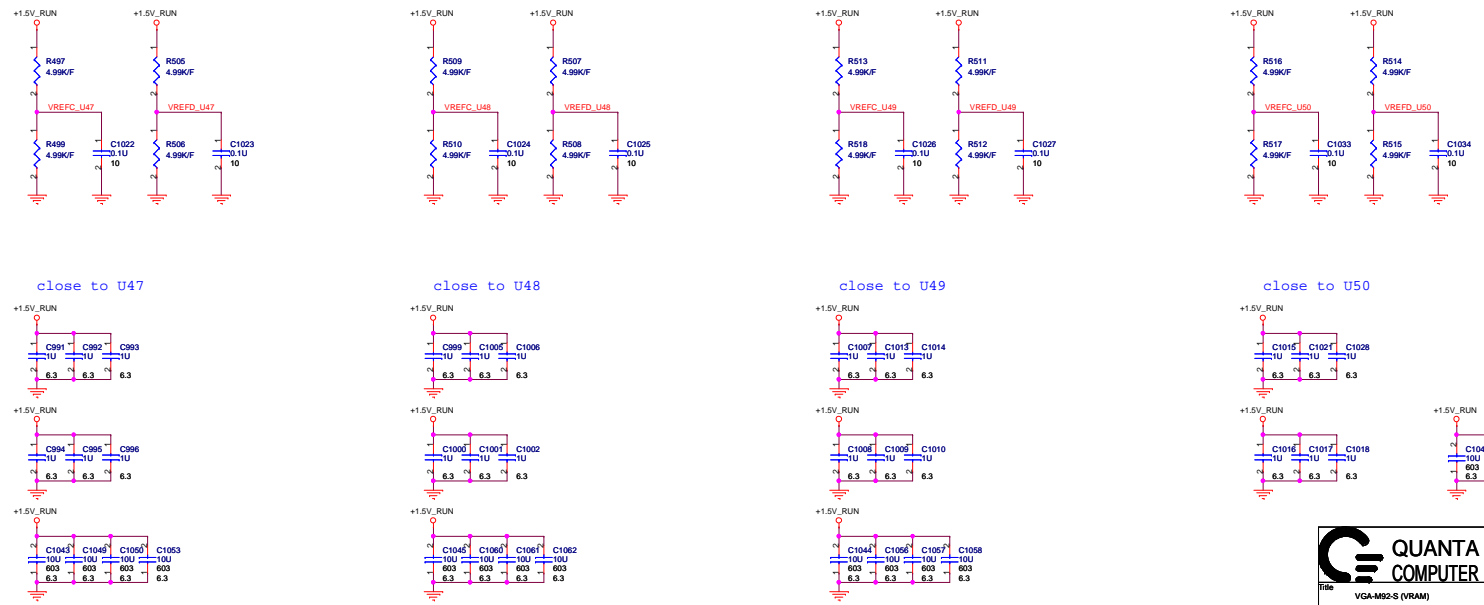
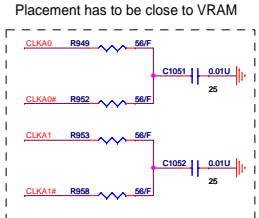
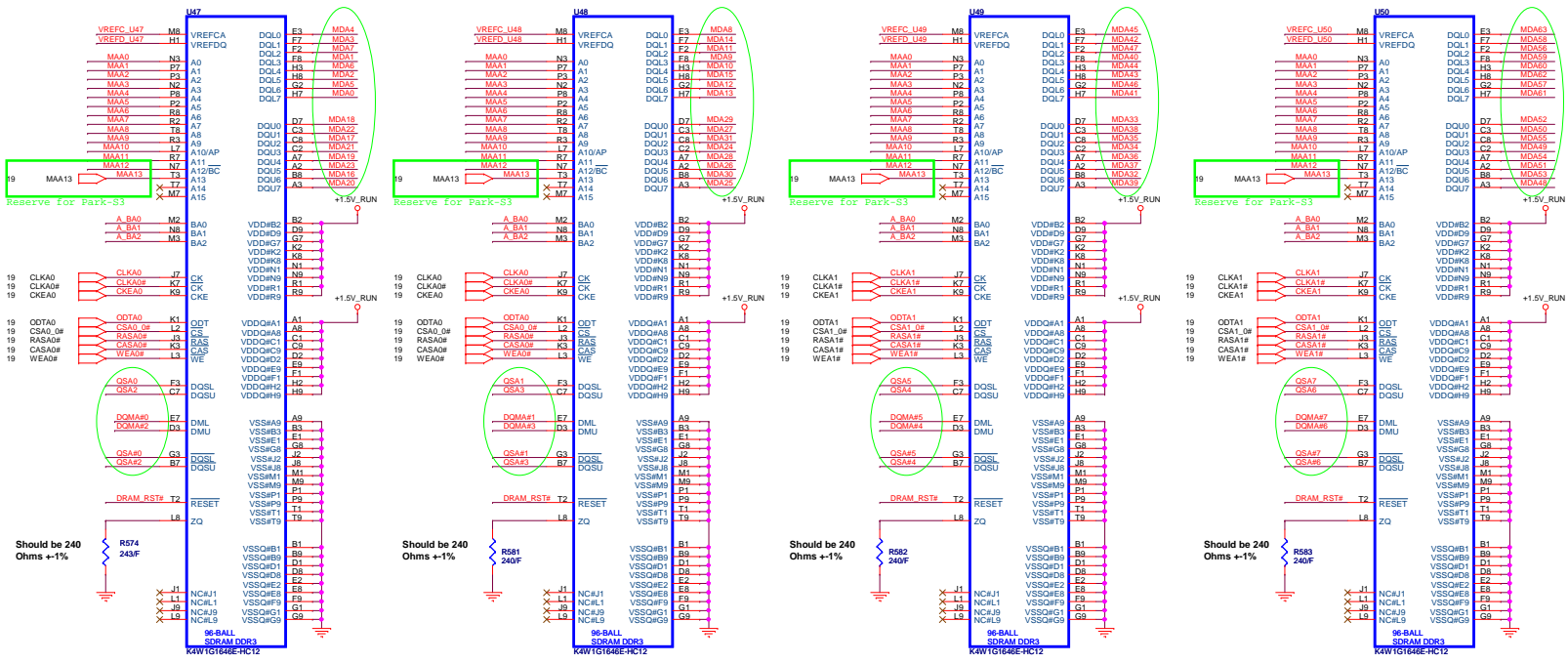


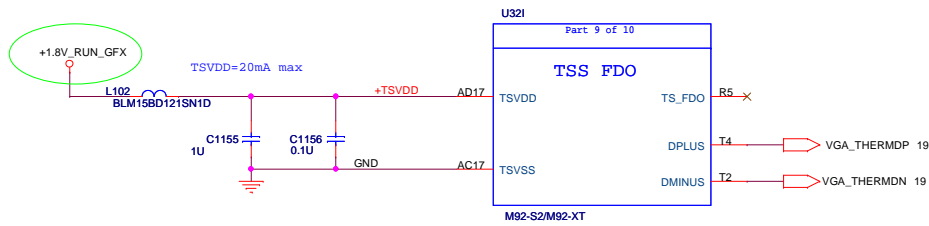
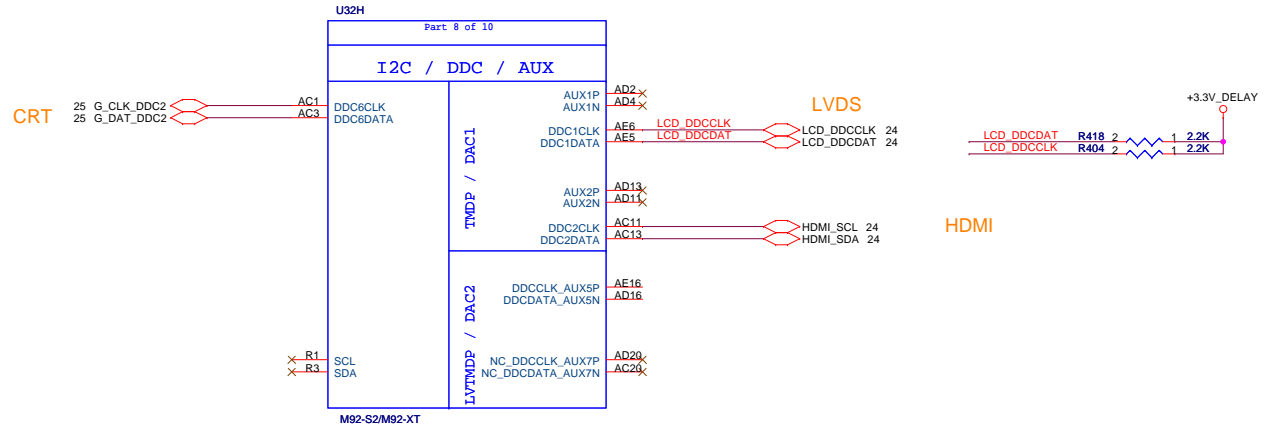
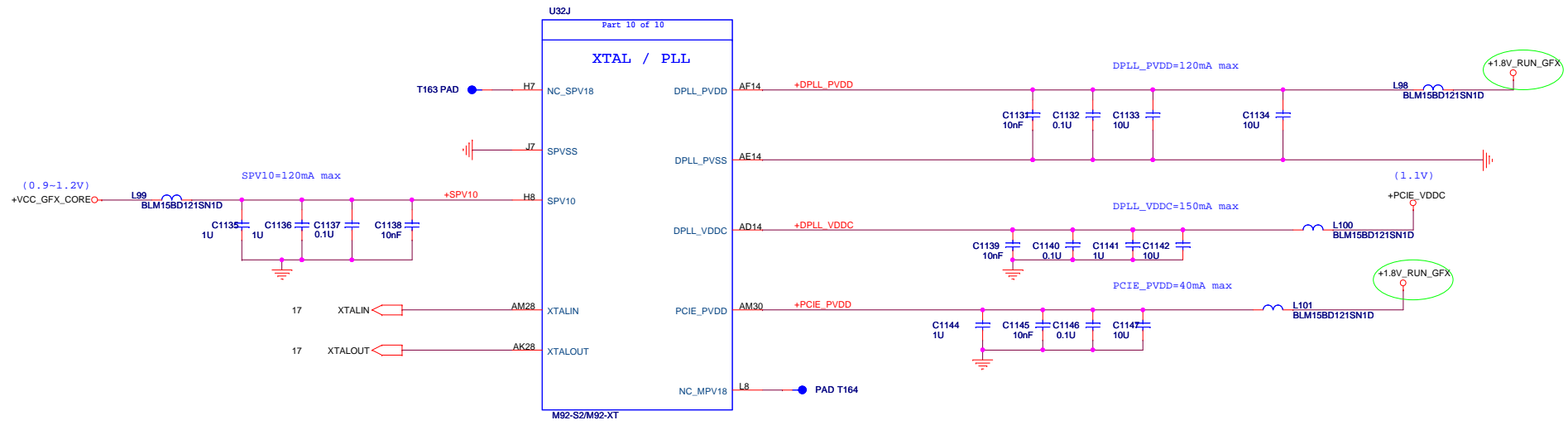
**QUANTA
COMPUTER**

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Size: F1M0	Document Number: F1M0	
Date: Thursday, February 26, 2009	Sheet: 19	of 64

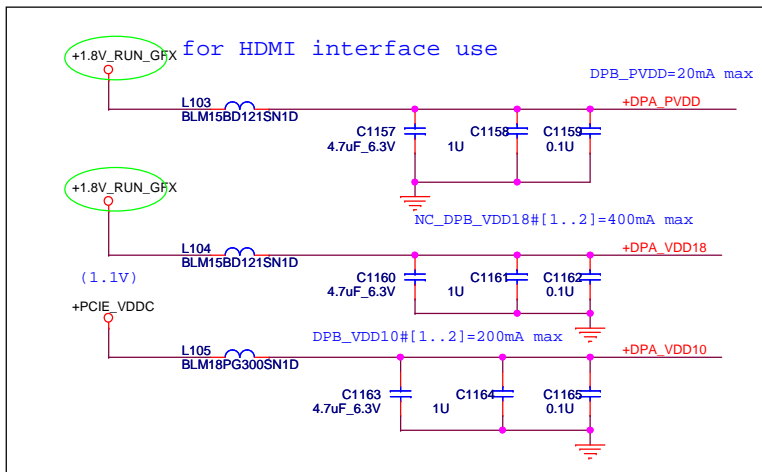
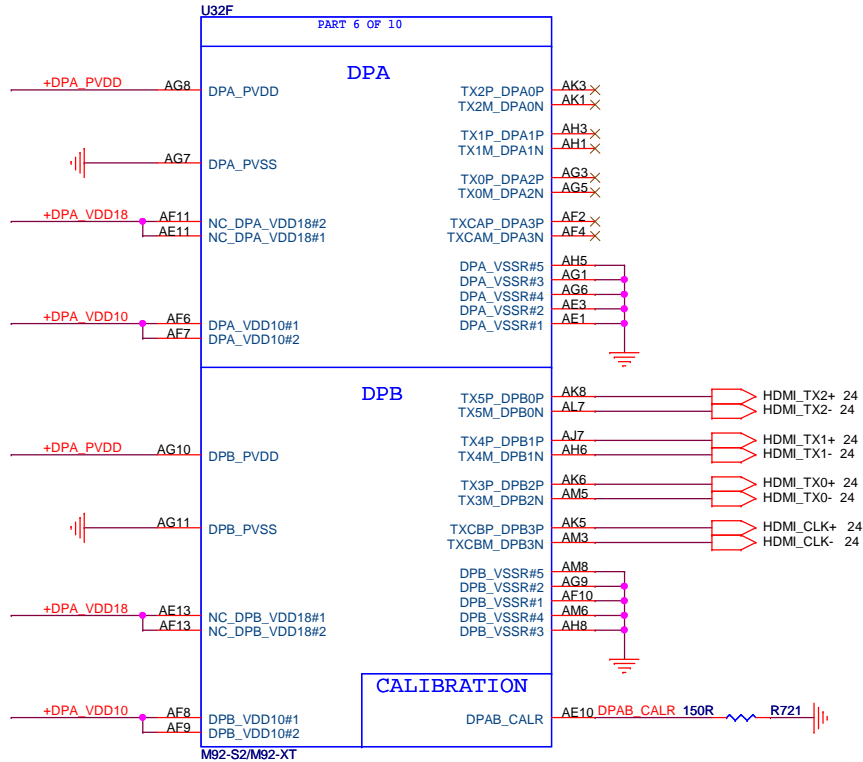
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- 19 MAA#(12..0) MAA#(12..0)
- 19 QSA#(7..0) QSA#(7..0)
- 19 QSA#(7..0) QSA#(7..0)
- 19 QMA#(7..0) QMA#(7..0)
- 19 DRAM_RST# DRAM_RST#
- 19 A_BA[2..0] A_BA[2..0]

DDR3

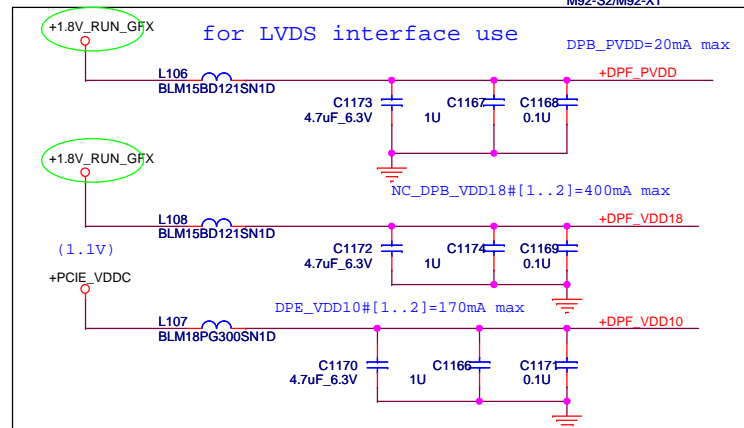
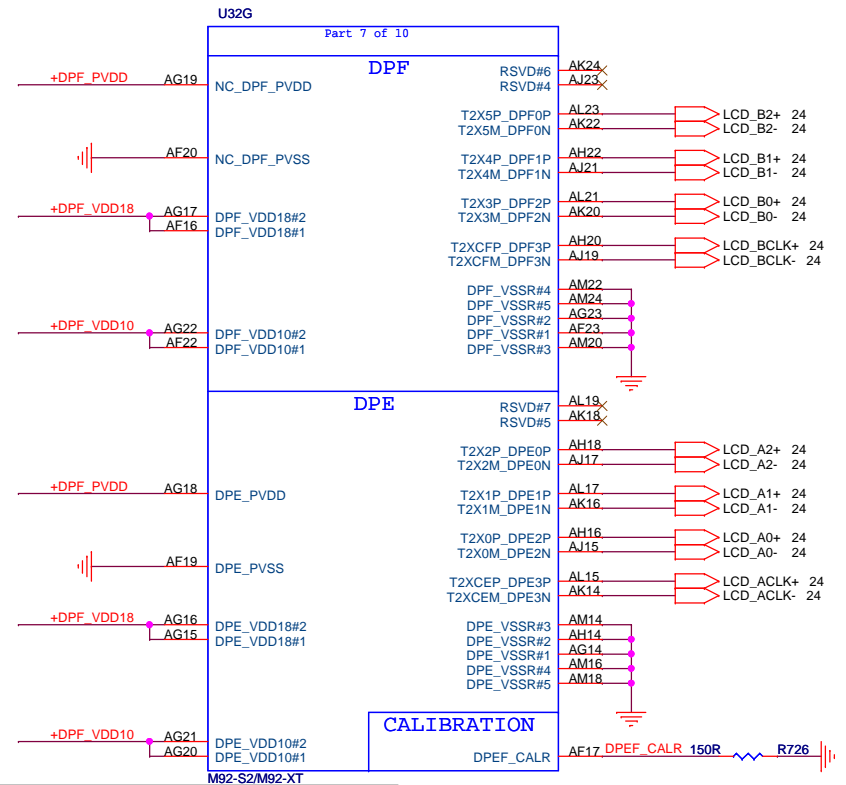




TMDP(HDMI) INTERFACE



LVDS INTERFACE



Title		
VGA-M92-XT (PCIe)		
Size	Document Number	Rev
	F9M9	1A
Date:	Thursday, February 26, 2009	Sheet 22 of 64

5

4

3

2

1

D

D

C

C

B

B

A

A



File		VGA-M82-S (PCIe)	
Size	Document Number	Rev	
	FMS	1A	
Date:	Thursday, February 26, 2009	Sheet	23 of 64

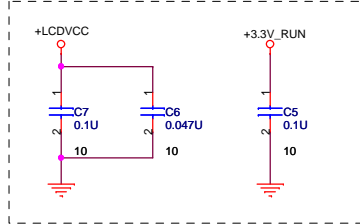
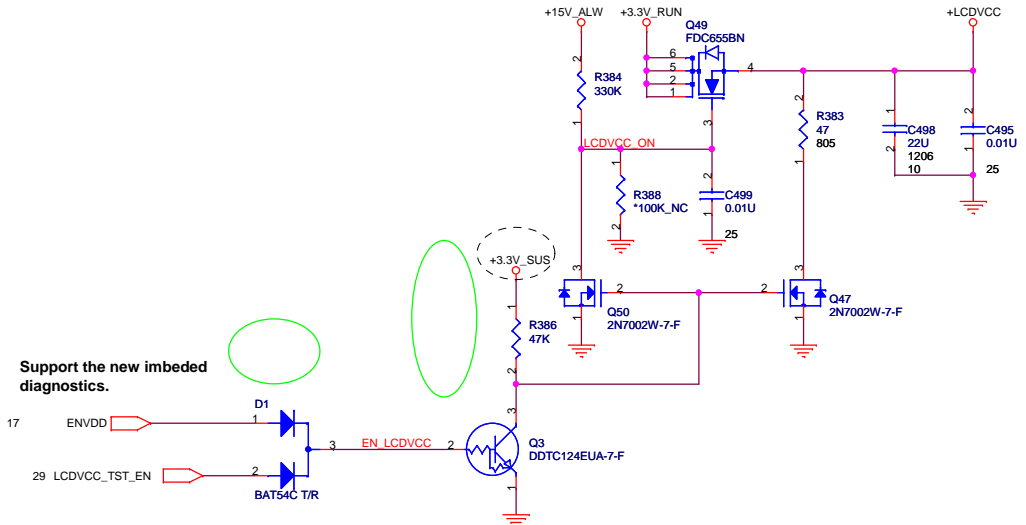
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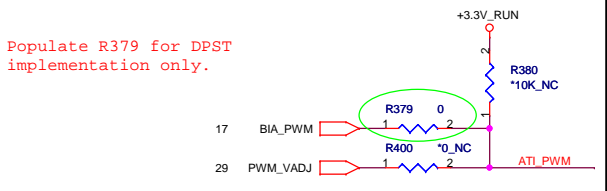
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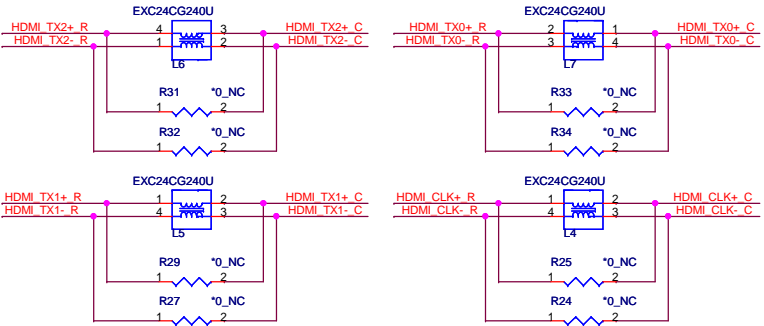
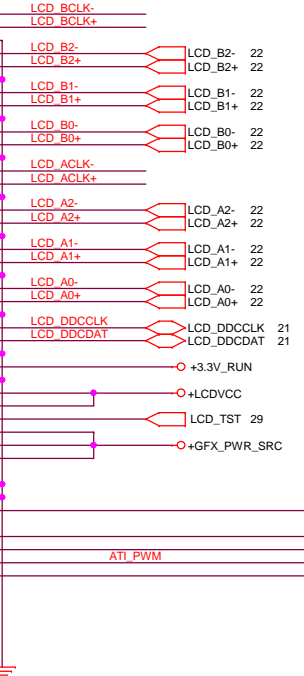
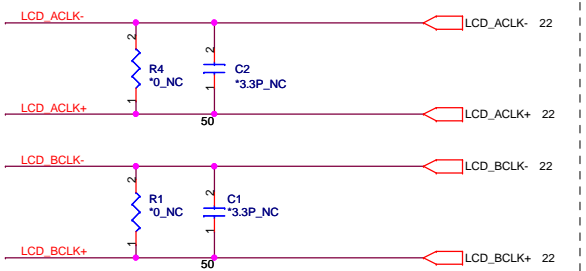


Address : A9H --Contrast
AAH --Backlight

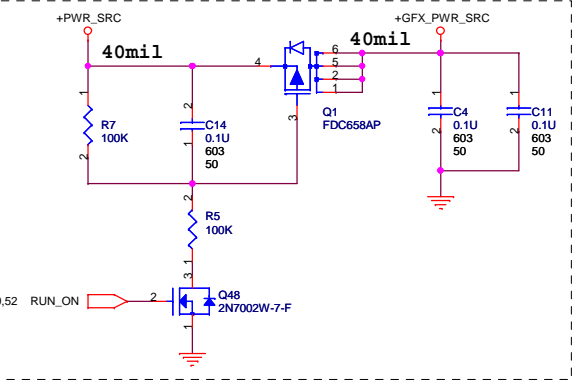


Shunt capacitors on LVDS for improving WWAN.

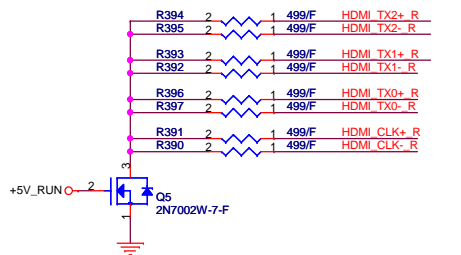
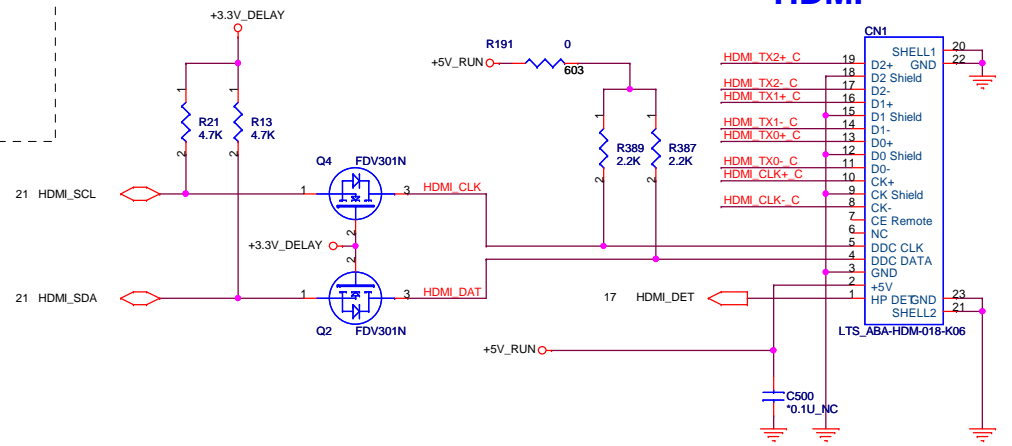
LCD B0-	C16	1	2	*3.3P	NC	50	LCD B0+
LCD B1-	C10	1	2	*3.3P	NC	50	LCD B1+
LCD B2-	C15	1	2	*3.3P	NC	50	LCD B2+
LCD A0-	C13	1	2	*3.3P	NC	50	LCD A0+
LCD A1-	C12	1	2	*3.3P	NC	50	LCD A1+
LCD A2-	C3	1	2	*3.3P	NC	50	LCD A2+



HDMI



HDMI_TX2+	C25	0.1U/10V/X7R	HDMI_TX2+ R
HDMI_TX2-	C26	0.1U/10V/X7R	HDMI_TX2- R
HDMI_TX1+	C23	0.1U/10V/X7R	HDMI_TX1+ R
HDMI_TX1-	C22	0.1U/10V/X7R	HDMI_TX1- R
HDMI_TX0+	C27	0.1U/10V/X7R	HDMI_TX0+ R
HDMI_TX0-	C30	0.1U/10V/X7R	HDMI_TX0- R
HDMI_CLK+	C21	0.1U/10V/X7R	HDMI_CLK+ R
HDMI_CLK-	C20	0.1U/10V/X7R	HDMI_CLK- R

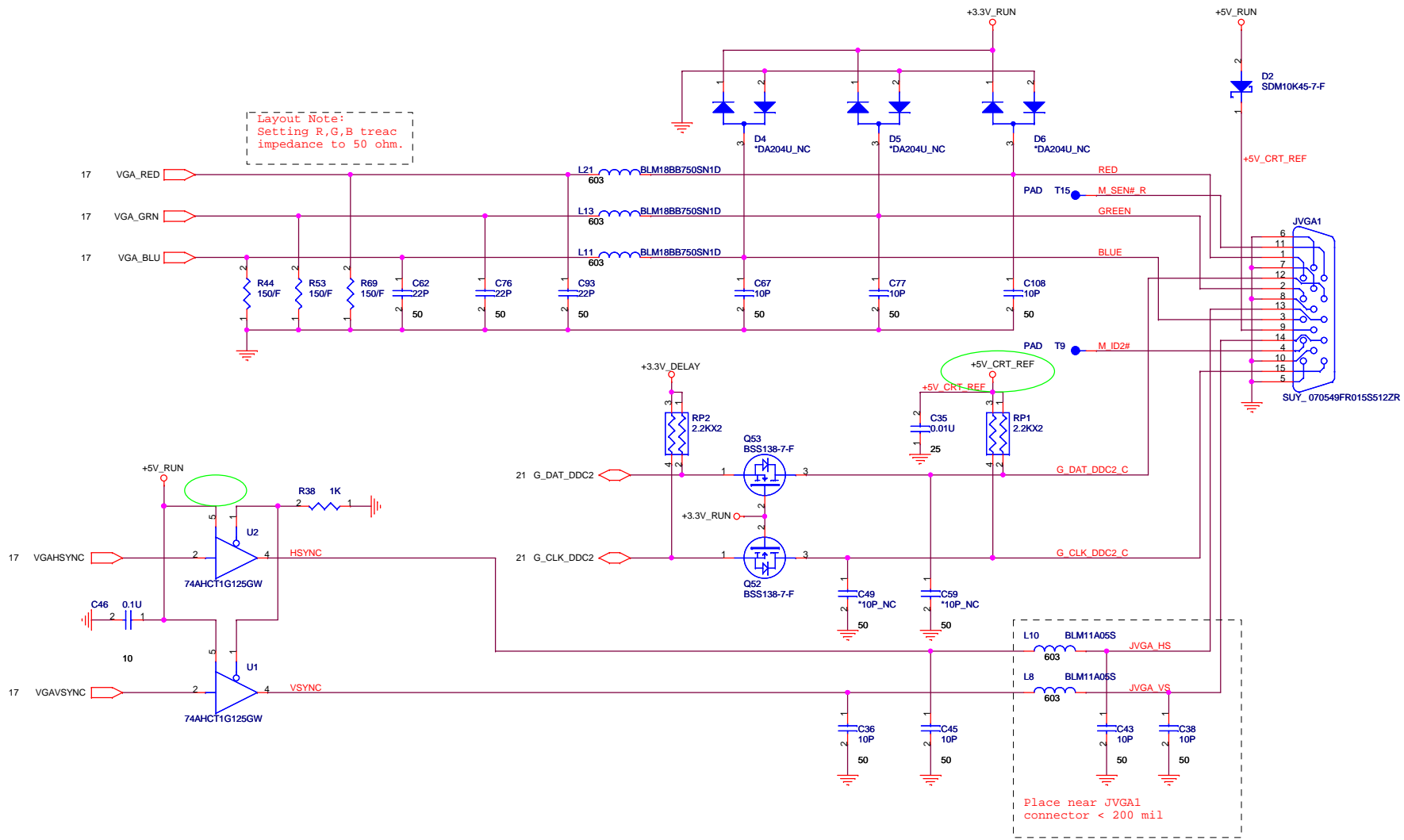


QUANTA COMPUTER

Title: LCD CONN & CK-SSCD

Size: Document Number FMG Rev 1A

Date: Thursday, February 26, 2009 Sheet 24 of 64

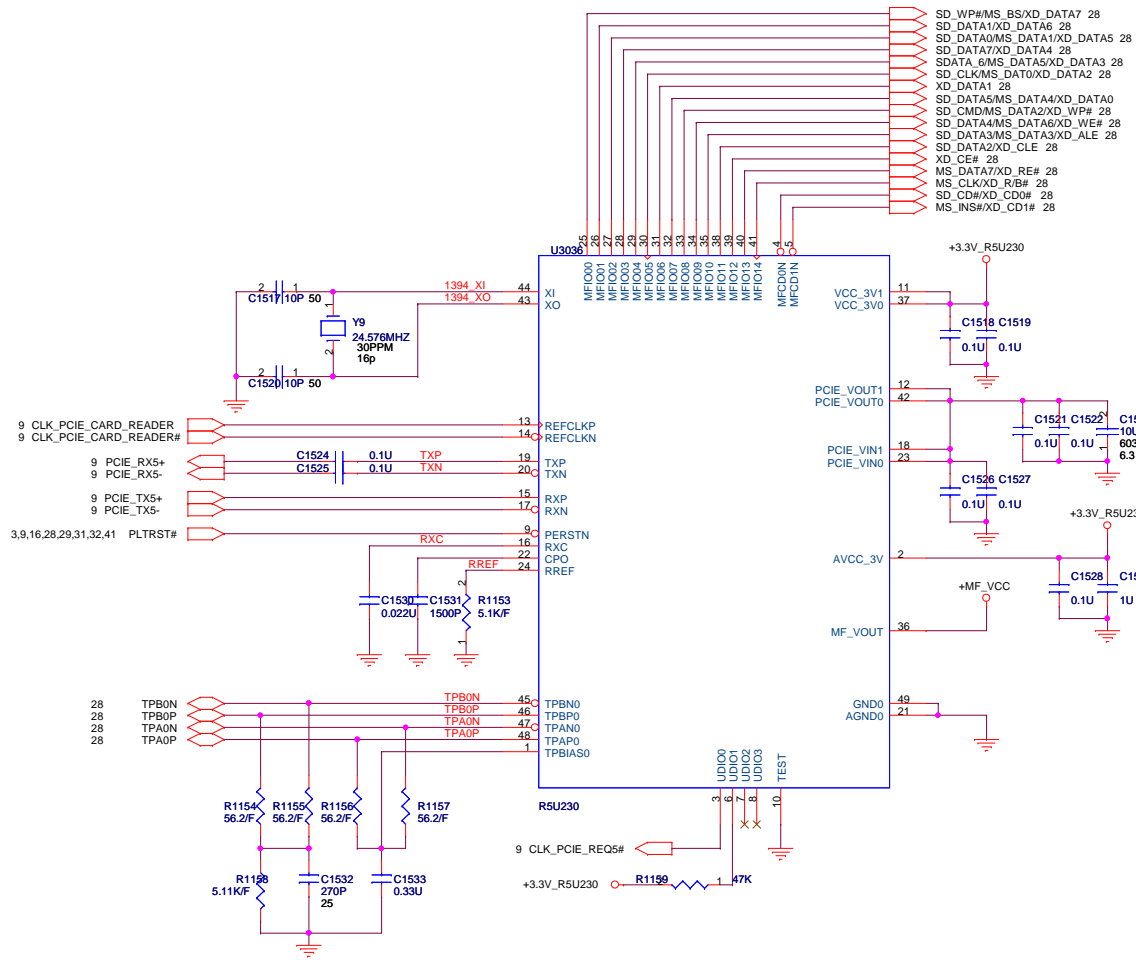


Layout Note:
Setting R,G,B trace
impedance to 50 ohm.

Place near JVGA1
connector < 200 mil

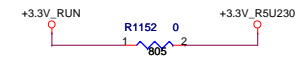


Title		CRT&TV CONN
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MFIO Pin Assignment Table

MFIO	SD8	MS8	XD
00	WP	BS	D7
01	D1	-	D6
02	D0	D1	D5
03	D7	-	D4
04	D6	D5	D3
05	CLK	D0	D2
06	-	-	D1
07	D5	D4	D0
08	CMD	D2	WP#
09	D4	D6	WE#
10	D3	D3	ALE
11	D2	-	CLE
12	-	-	CE#
13	-	D7	RE#
14	-	CLK	R/B#



A

B

C

D

E

1

1

2


2

3

3

4

4

 QUANTA COMPUTER		
Title: IEEE 1394		
Size: FM9	Document Number: FM9	Rev: 1A
Date: Thursday, February 26, 2009		
Sheet 27 of 64		

A

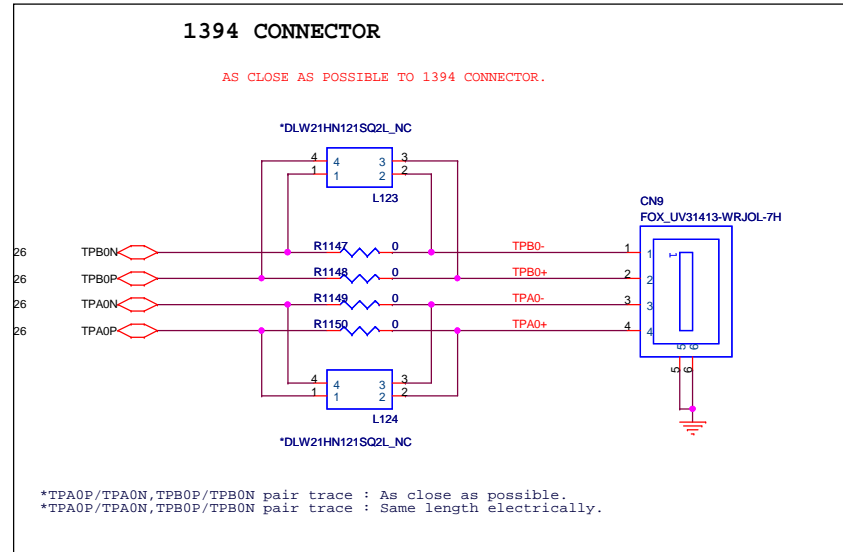
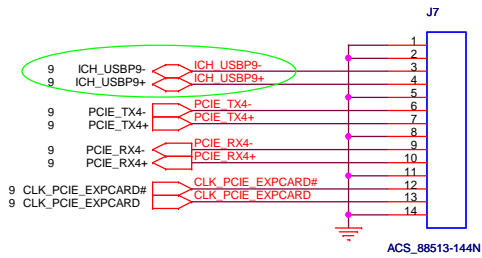
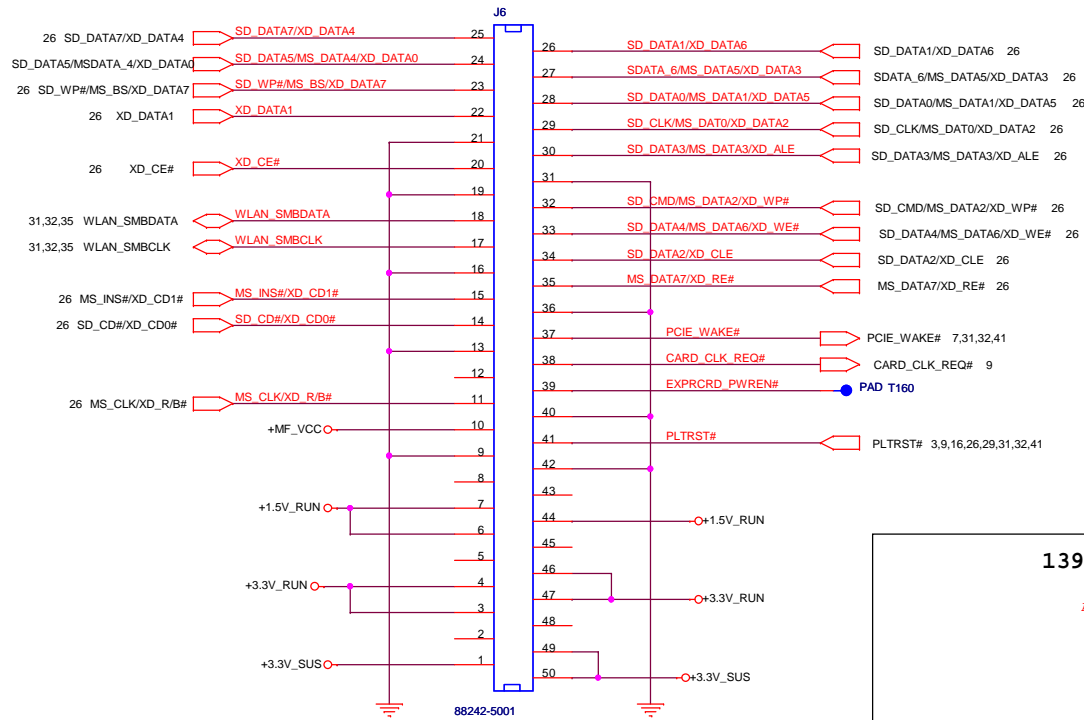
B

C

D

E

Express Card/CARD READER



*TPA0P/TPA0N,TPB0P/TPB0N pair trace : As close as possible.
 *TPA0P/TPA0N,TPB0P/TPB0N pair trace : Same length electrically.

QUANTA COMPUTER

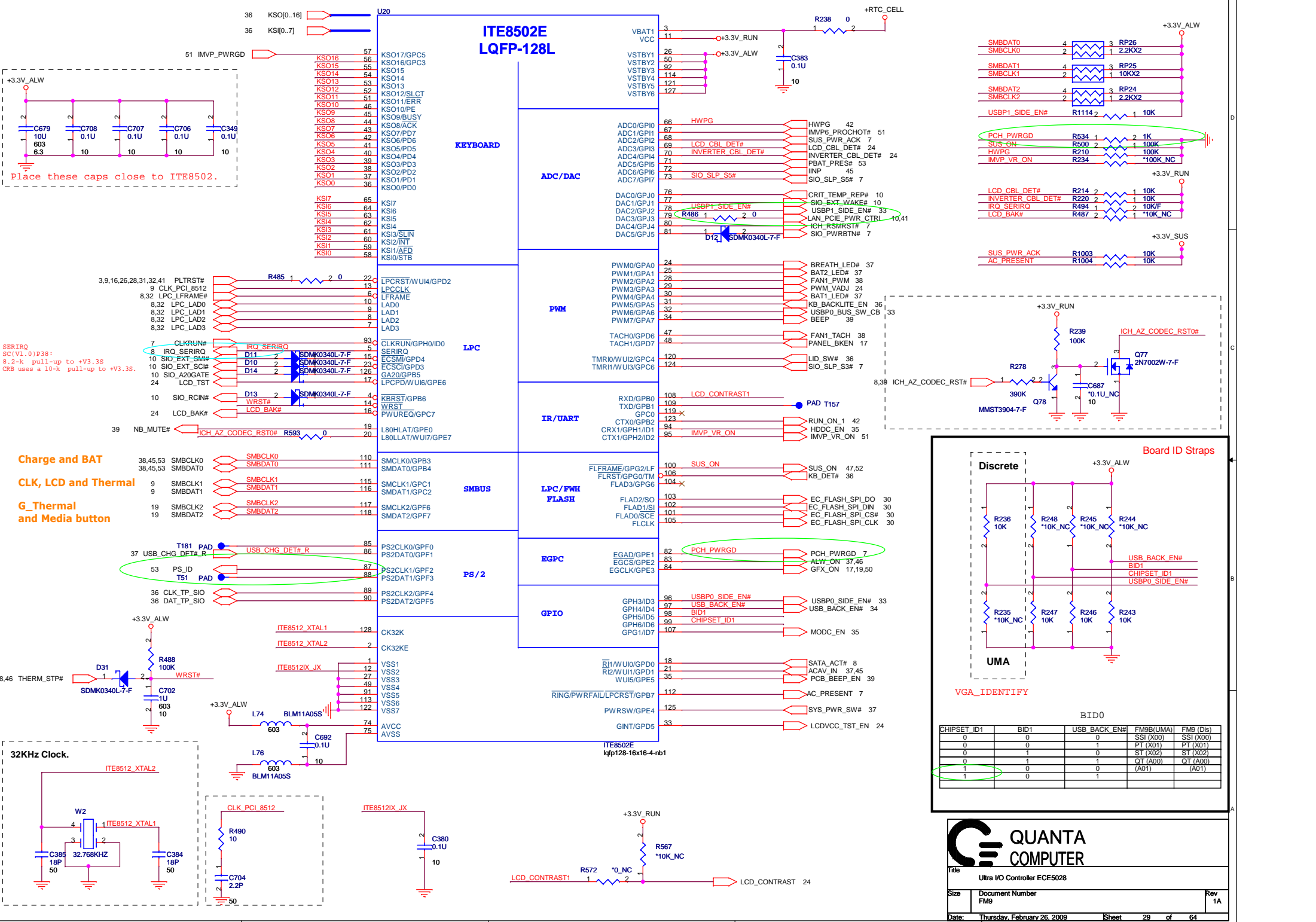
Title: ExpressCard/SmartCard

Size: Document Number
FMG

Rev: 1A

Date: Thursday, February 26, 2009

Sheet: 28 of 64

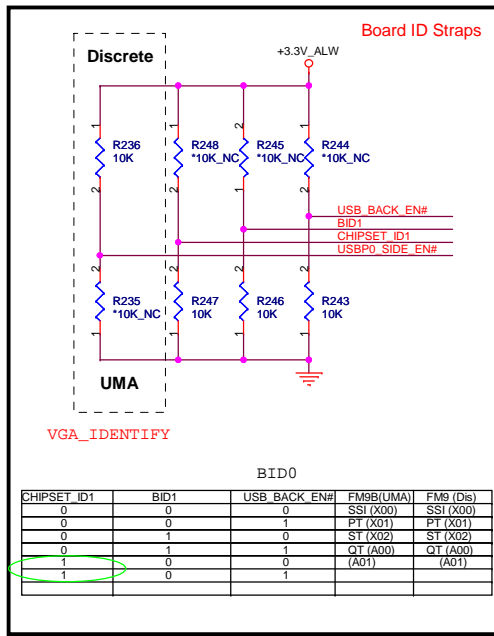
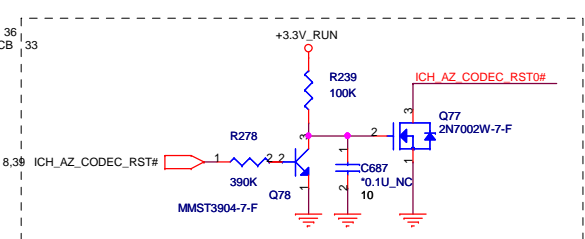
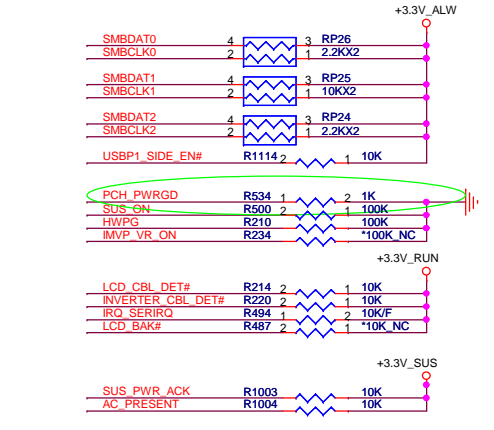


Place these caps close to ITE8502.

SERIRQ SC(V1_0)P38: 8.2-k pull-up to +V3_3S CRB uses a 10-k pull-up to +V3_3S.

Charge and BAT
CLK, LCD and Thermal
G_Thermal and Media button

32KHz Clock.



QUANTA COMPUTER

Ultra I/O Controller ECE5028

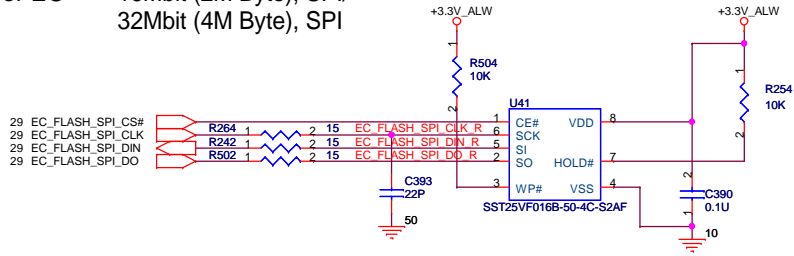
CHIPSET ID1	BID1	USB_BACK_EN#	FM9B(UMA)	FM9(Ds)
0	0	0	SSI (X00)	SSI (X00)
0	0	1	PT (X01)	PT (X01)
0	1	0	ST (X02)	ST (X02)
0	1	1	QT (A00)	QT (A00)
1	0	0	(A01)	(A01)
1	0	1		

File: Ultra I/O Controller ECE5028

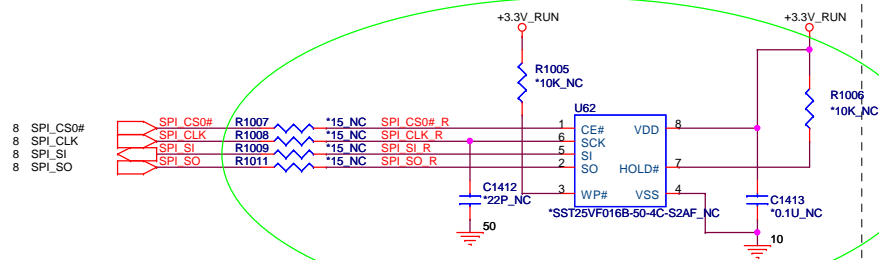
Size: Document Number FM9 Rev 1A

Date: Thursday, February 26, 2009 Sheet 29 of 64

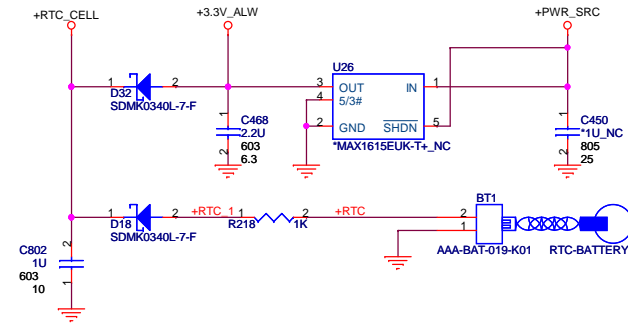
For EC 16Mbit (2M Byte), SPI/
32Mbit (4M Byte), SPI



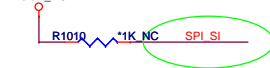
For PCH 16Mbit (2M Byte), SPI/
32Mbit (4M Byte), SPI



RTC BATTERY



iTPM ENABLE/DISABLE



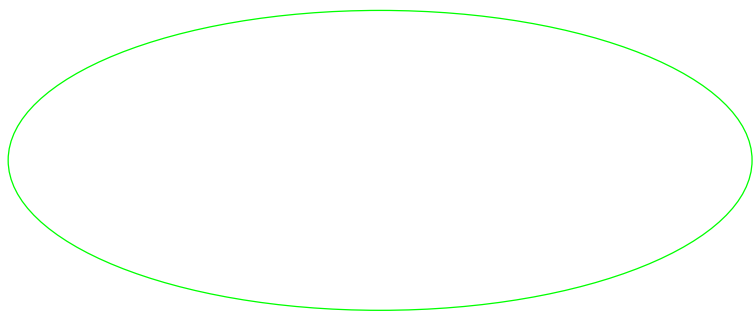
TPM Function	R712
Enable	Mount
Disable	NC (Default)



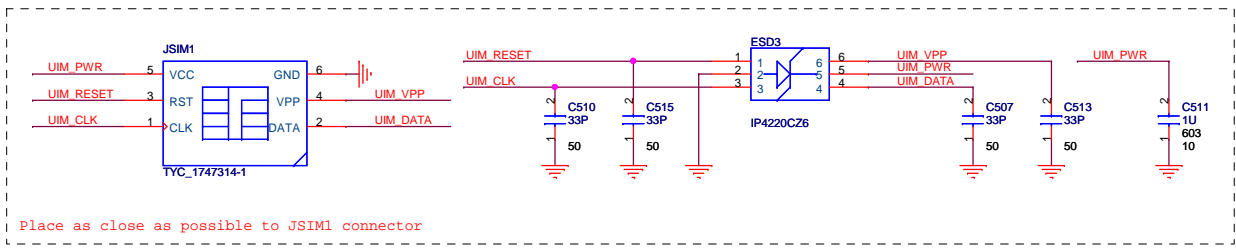
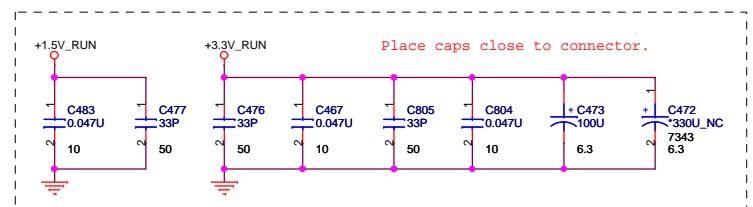
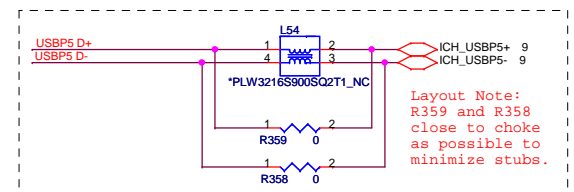
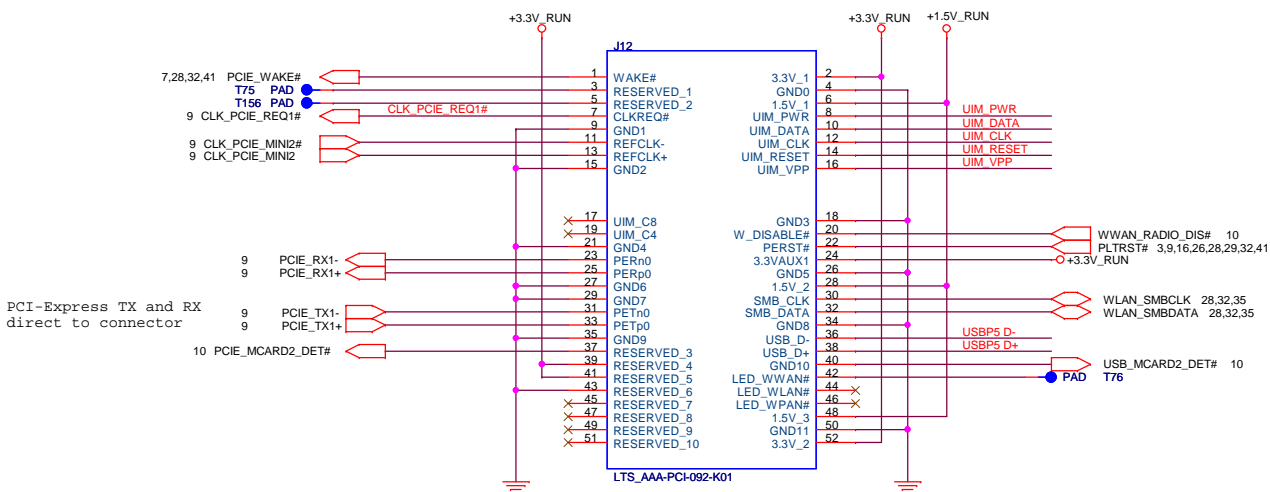
Title Ultra I/O Controller ECE5028

Size Document Number
FMG

Rev 1A

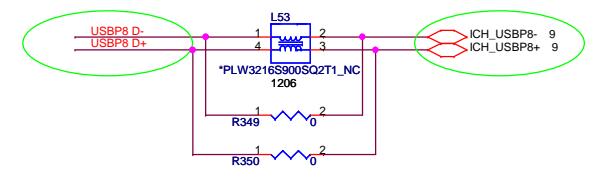
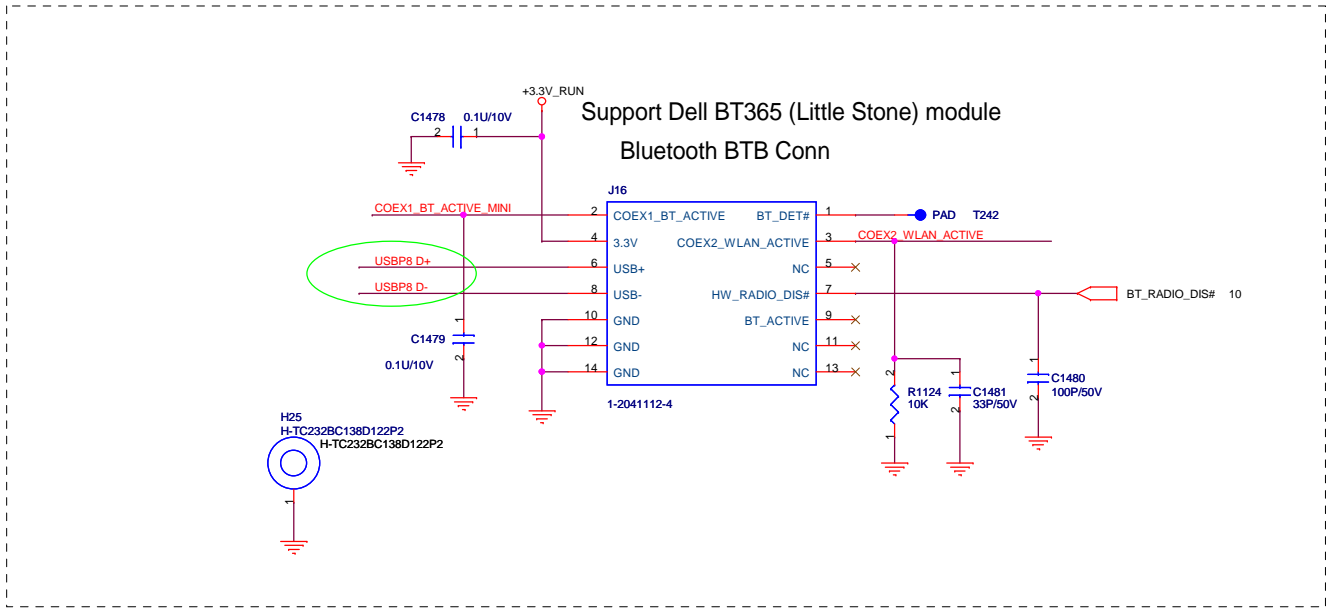
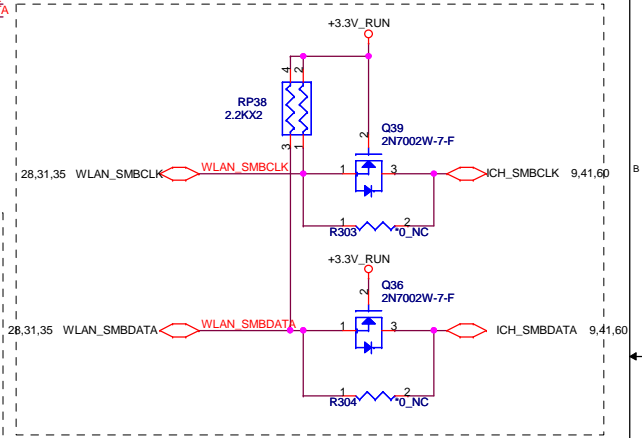
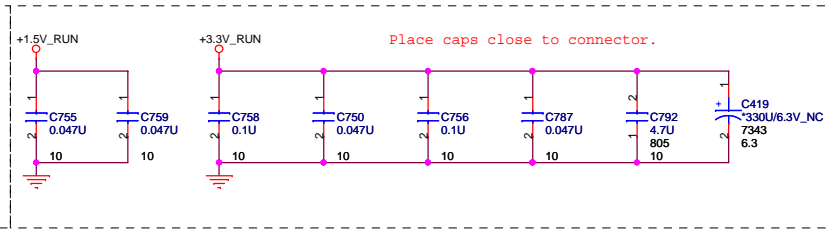
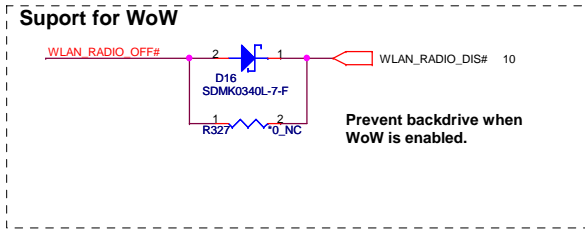
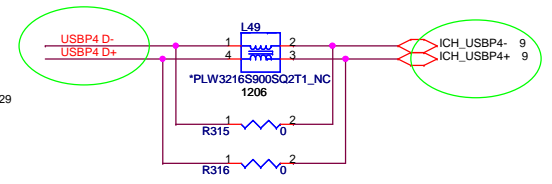
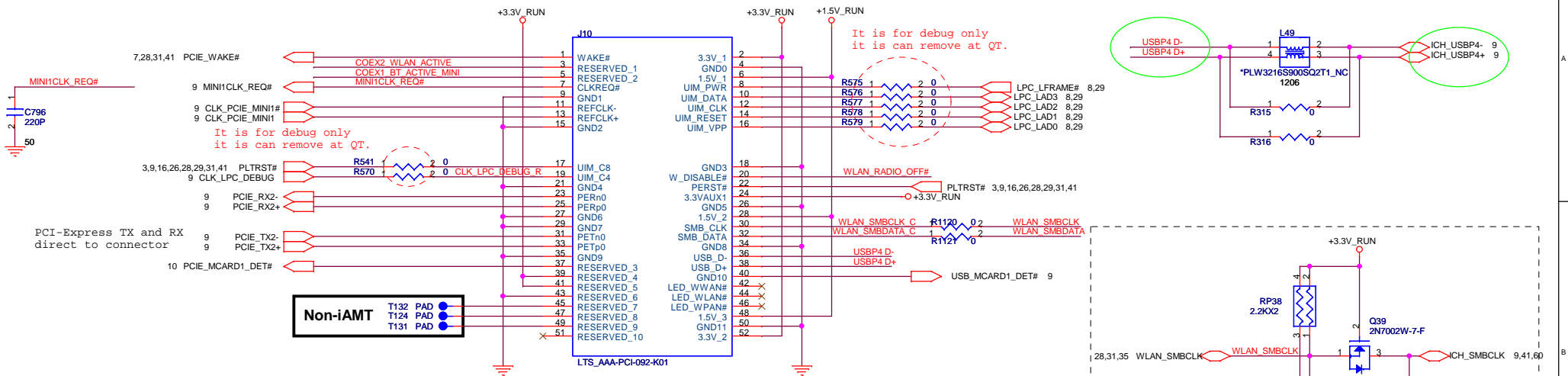


MiniCard WWAN connector



Title		MINI-PCI
Size	Document Number	Rev
	FMG	1A
Date:	Thursday, February 26, 2009	Sheet 31 of 64

MiniCard WLAN connector



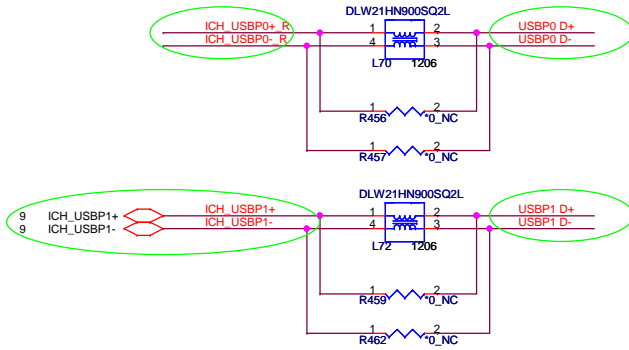
QUANTA COMPUTER

Title: MDC CONN.

Size: Document Number: Rev 1A

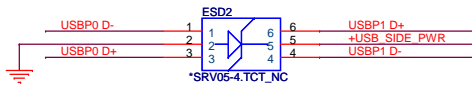
Date: Thursday, February 26, 2009 Sheet 32 of 64

External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently



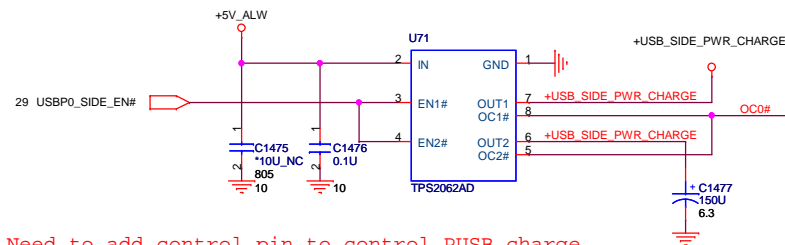
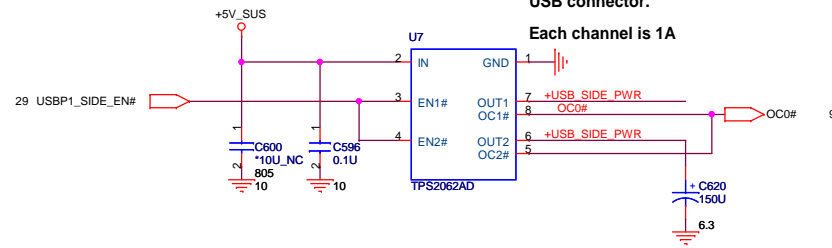
Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

Place ESD diodes as close as USB connector.



Place one 150uF cap by each USB connector.

Each channel is 1A

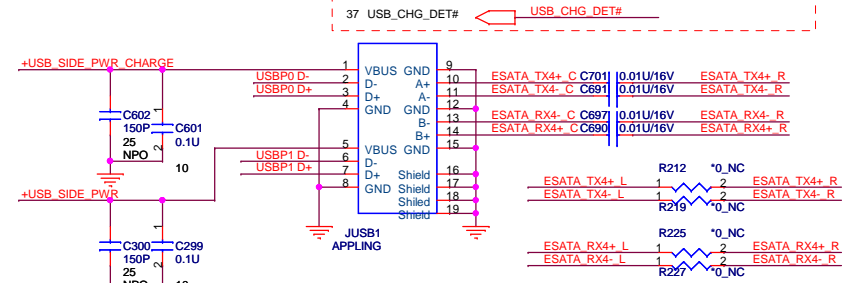


Need to add control pin to control PUSB charge

Support USBP1 charge function.
JUSB1 need to add USB_CHG_DET# pin wire to EC GPIO to detect USB device.

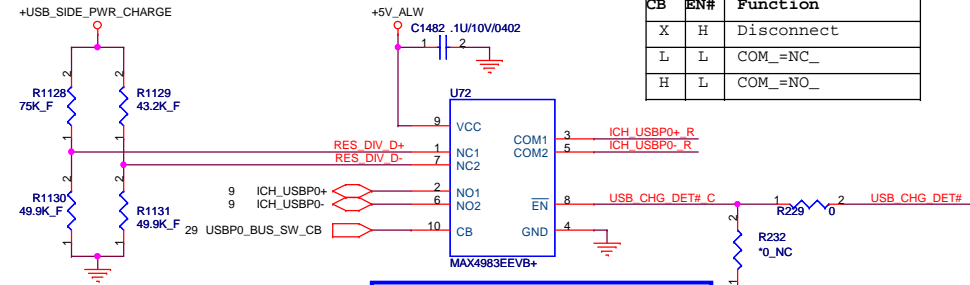
Side External USBX2

For USPI USB PWR CHARGE, JUSB1 need add USB_CHG_DET#



Please put those on the same side of MB PCB
USBx2 & ESATA COMBO & PWR CHARGE

USB BUS SW



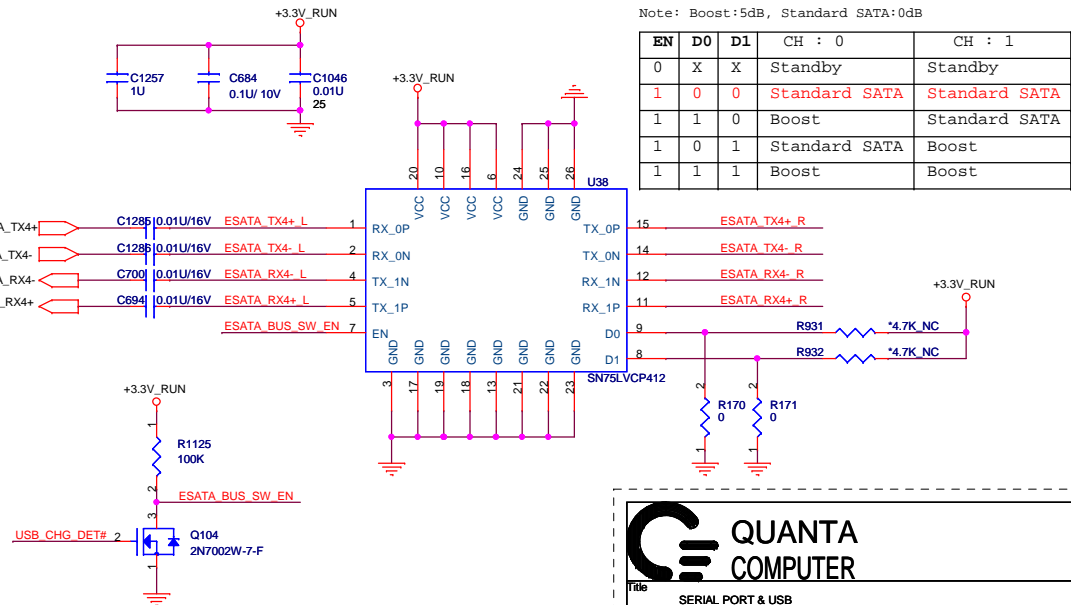
(5V)-43.2K-(D-)-49.9K-GND (about 2.68V)
(5V)-75.0K-(D+)-49.9K-GND (about 2.00V)

CB	EN#	Function
X	H	Disconnect
L	L	COM_=NC_
H	L	COM_=NO_

E-SATA Re-driver

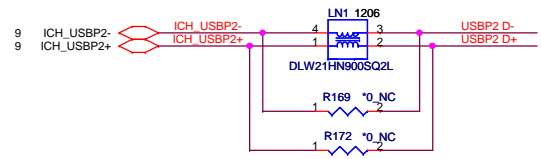
Please put those on the same side of MB PCB

Note: Boost:5dB, Standard SATA:0dB

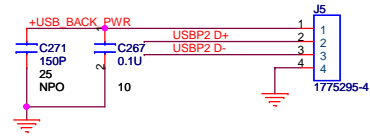
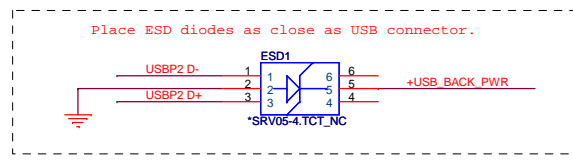
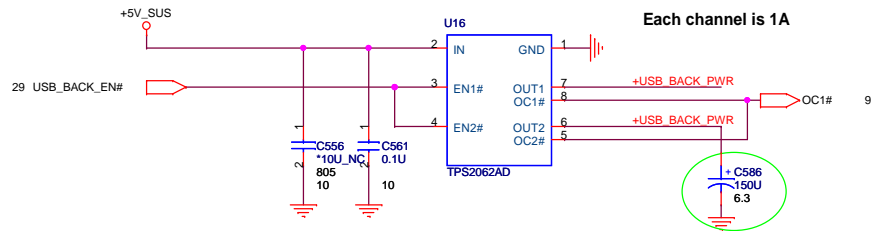


EN	D0	D1	CH : 0	CH : 1
0	X	X	Standby	Standby
1	0	0	Standard SATA	Standard SATA
1	1	0	Boost	Standard SATA
1	0	1	Standard SATA	Boost
1	1	1	Boost	Boost

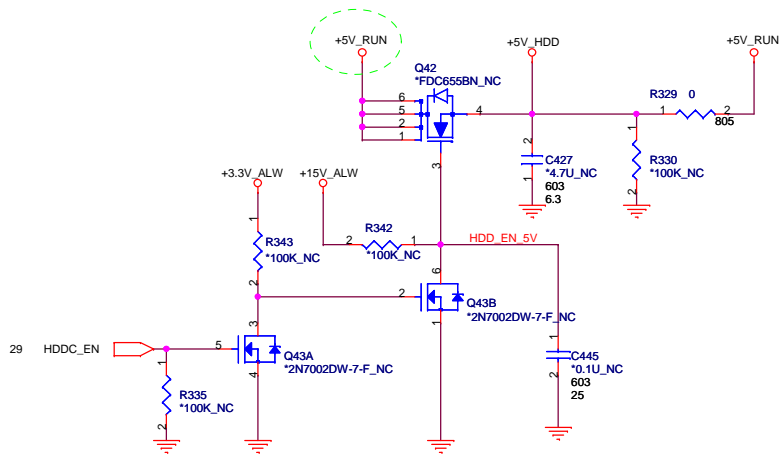
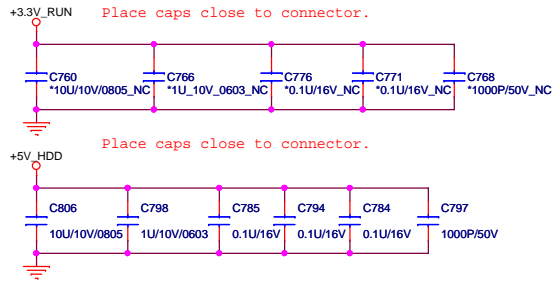
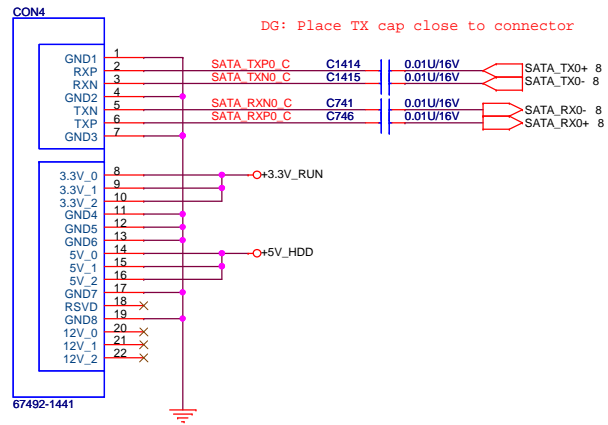




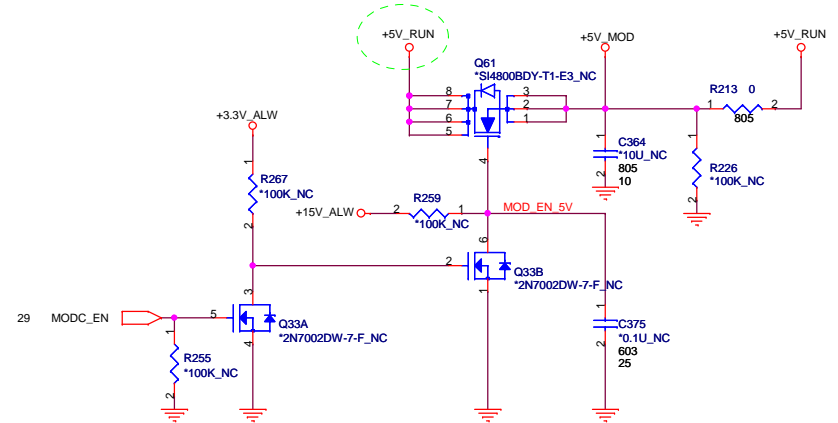
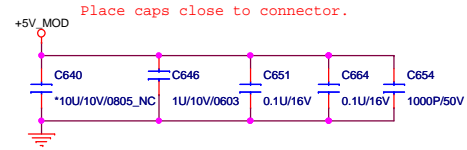
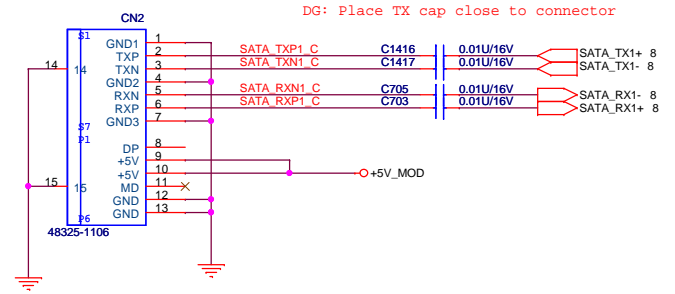
Place one 150uF cap by each USB connector.
Each channel is 1A



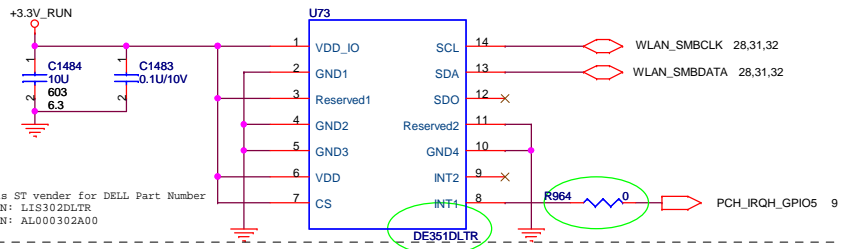
SATA Connector.



ODD Connector



3-axis Fall Sensor (HDD data protector)

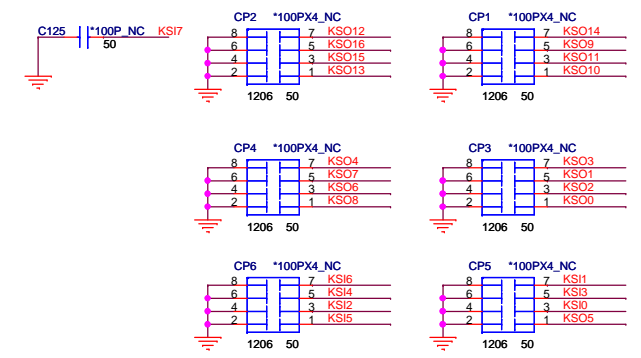
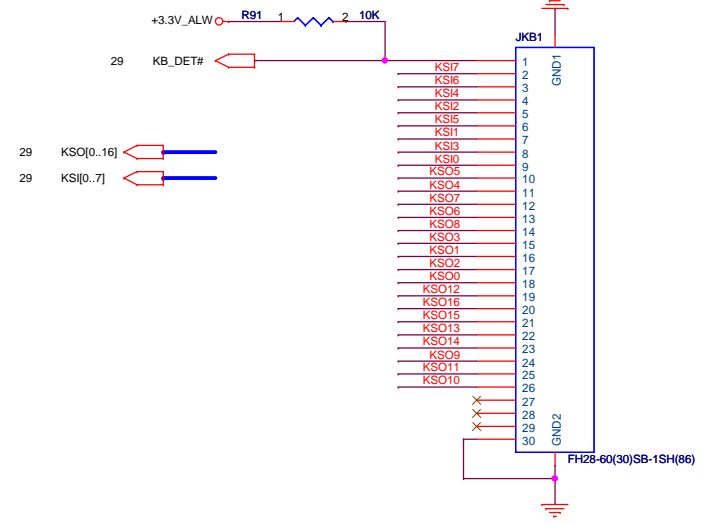


DE351DL is ST vendor for DELL Part Number
 Vendor PN: L1S302DLTR
 Quanta PN: AL000302A00



Title		SATA (HDD&CD_ROM)
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	FMG	1A
Date:	Thursday, February 26, 2009	Sheet 35 of 64

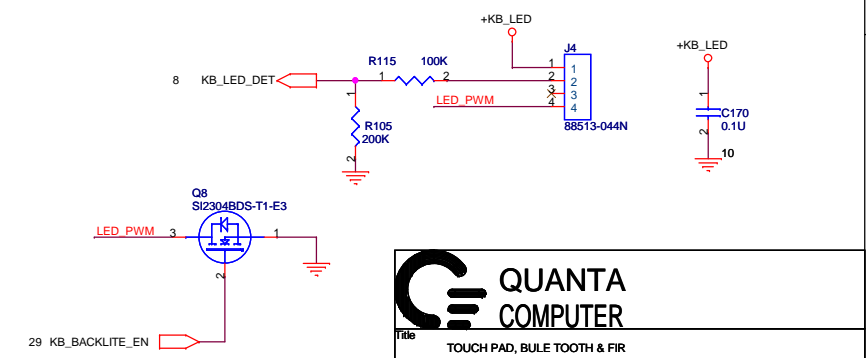
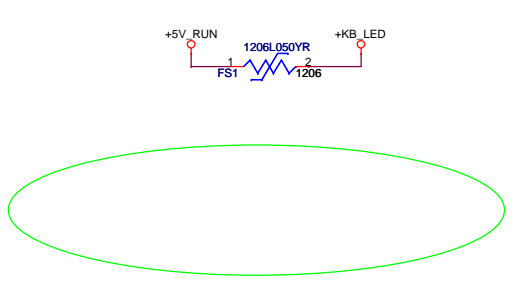
KEYBOARD CONNECTOR



100P CAPS CLOSE TO JKB1

Key board illumination

+KB_LED power trace width >10 mil



**QUANTA
COMPUTER**

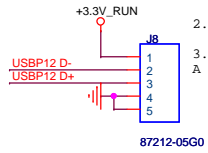
Title: TOUCH PAD, BULE TOOTH & FIR

Size	Document Number	Rev
	FMG	1A

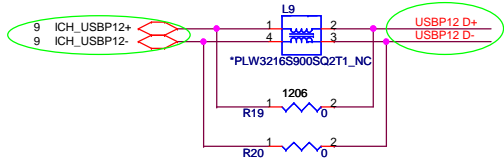
Date: Thursday, February 26, 2009 Sheet 36 of 64

Touch Screen Module

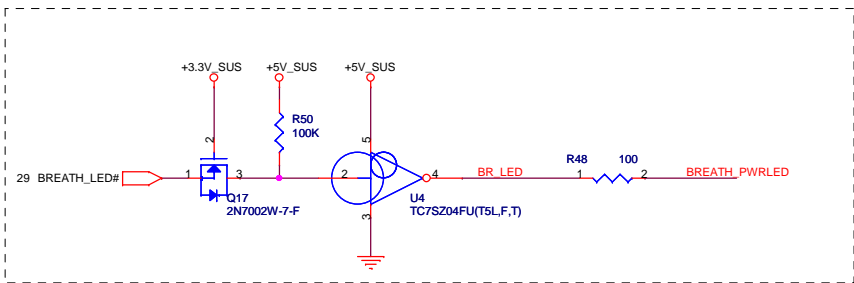
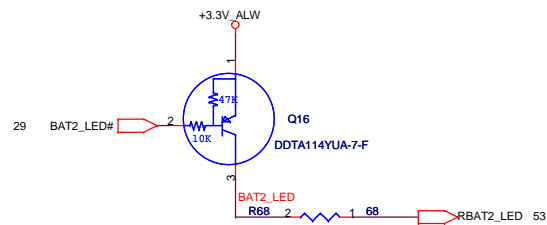
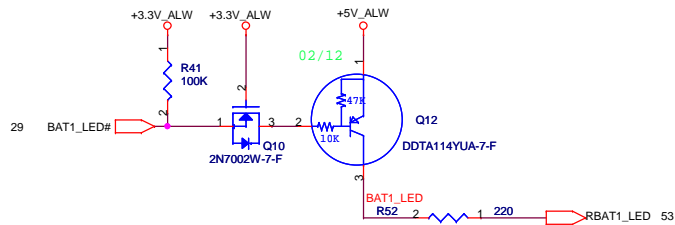
- Note:
1. VBUS IND:VBUS indication should be supplied to single the DuoSense to connect According to the USB 2.0 specification. A GND voltage from the host should indicate a connection.
 2. Maximum cable resistance on VCC, GND should be 150m ohm.
 3. FPC cable should support 12MHz USB singles. A tri-state should indicate no connection.



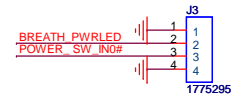
Need check the connector footprint and symbol.



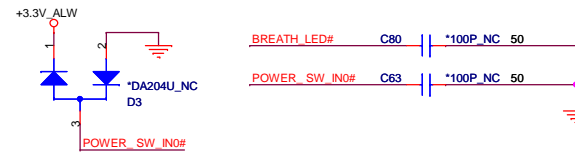
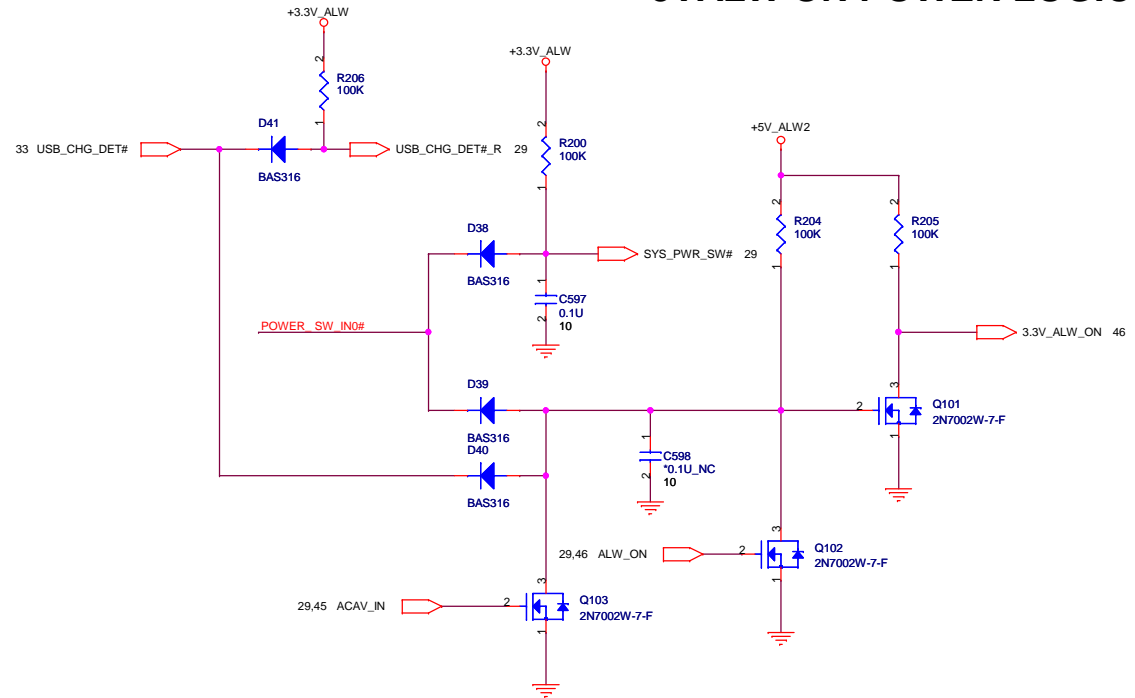
Battery status.



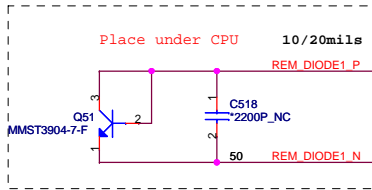
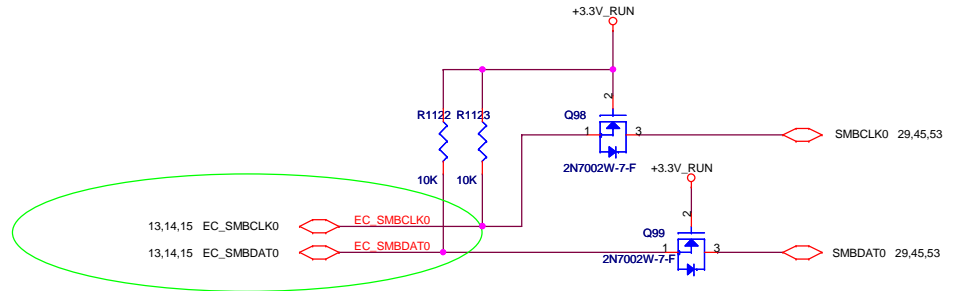
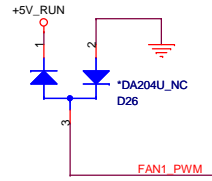
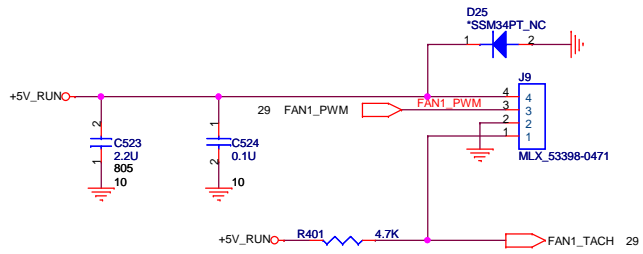
Power button Cable



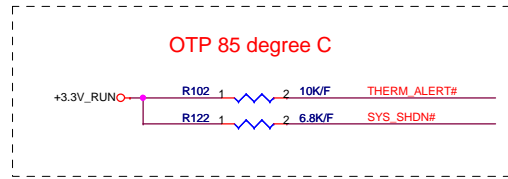
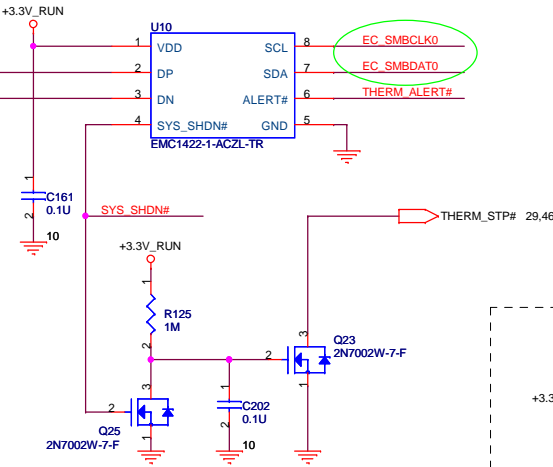
3VALW ON POWER LOGIC

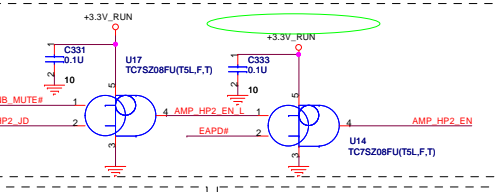
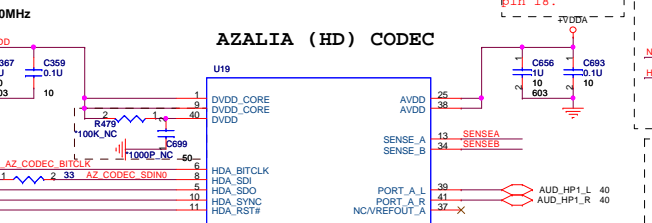
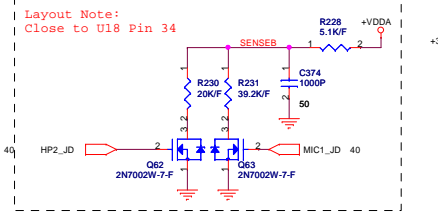
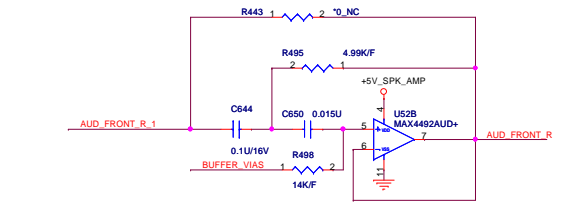
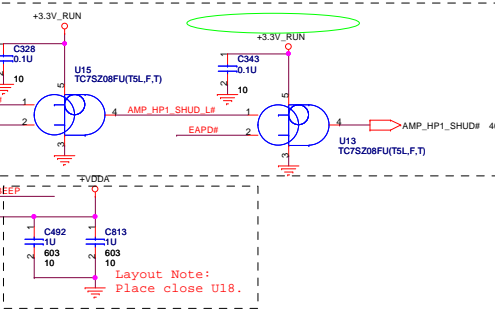
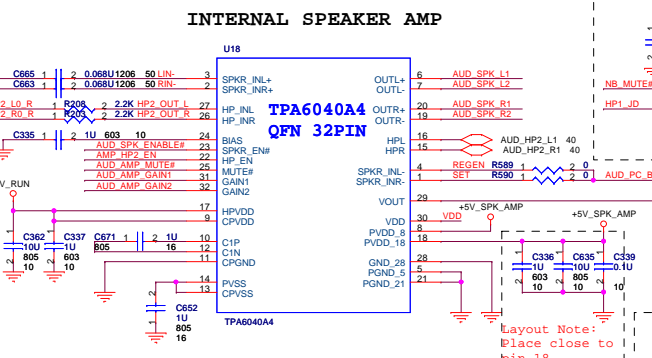
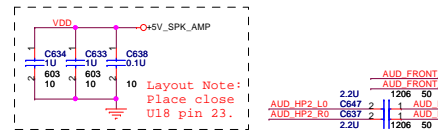
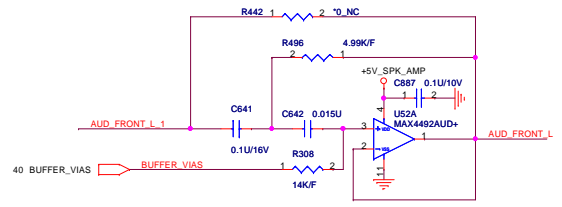
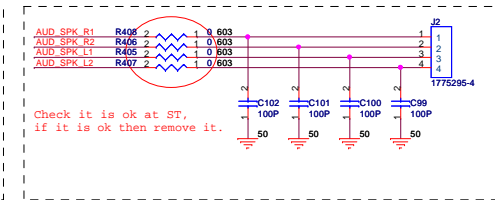
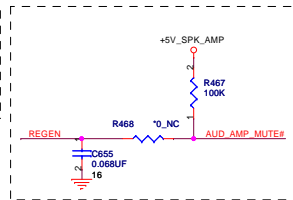
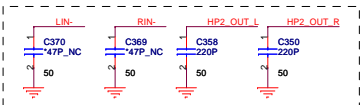
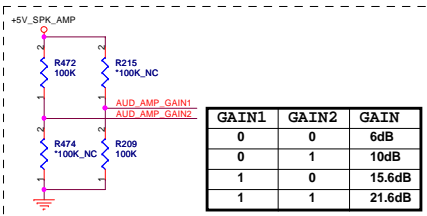


Title SWITCH, KEYBOARD & LED&Touch Screen Module		
Size FMG	Document Number FMG	Rev 1A
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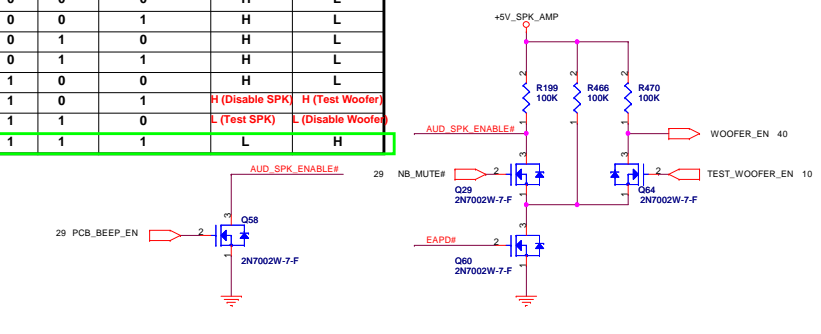


1. Place C160 close to EMC1422
 2. Place C518 to be close to Q51
- Total capacitance between D+/D- is 2200pF(max)
if use 2200pF for C160, then C518 should be dummy

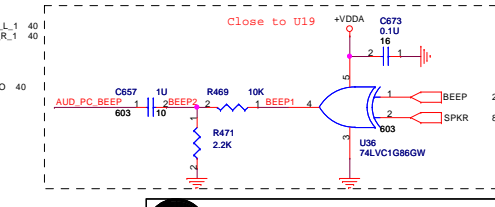
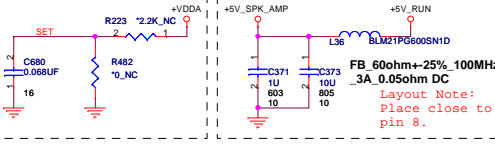
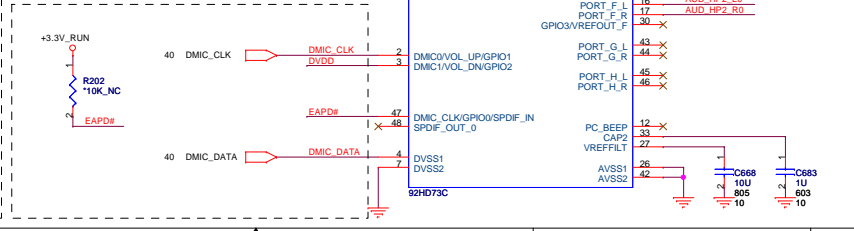




EAPD#	NB_MUTE#	TEST_WOOFER_EN	AUD_SPK_ENABLE#	WOOFER_EN
0	0	0	H	L
0	0	1	H	L
0	1	0	H	L
0	1	1	H	L
1	0	0	H	L
1	0	1	H (Disable SPK)	H (Test Woofers)
1	1	0	L (Test SPK)	L (Disable Woofers)
1	1	1	L	H



Depop R477, R478, R484, R473
Pop R476, R480, R483, R475
for using 92HD73C
R476, R483 close to U19, Let DVDD width be 10-mils

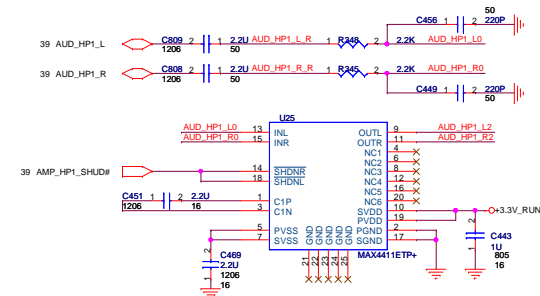
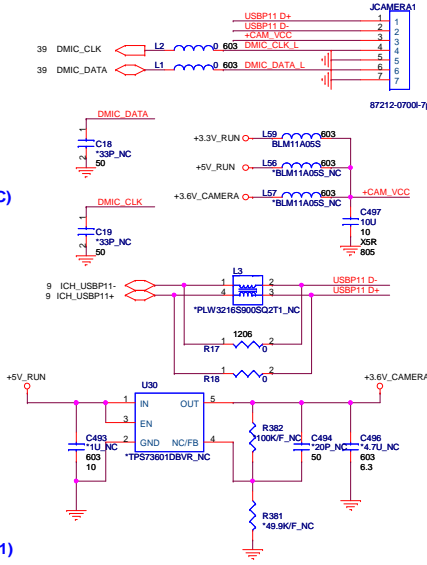
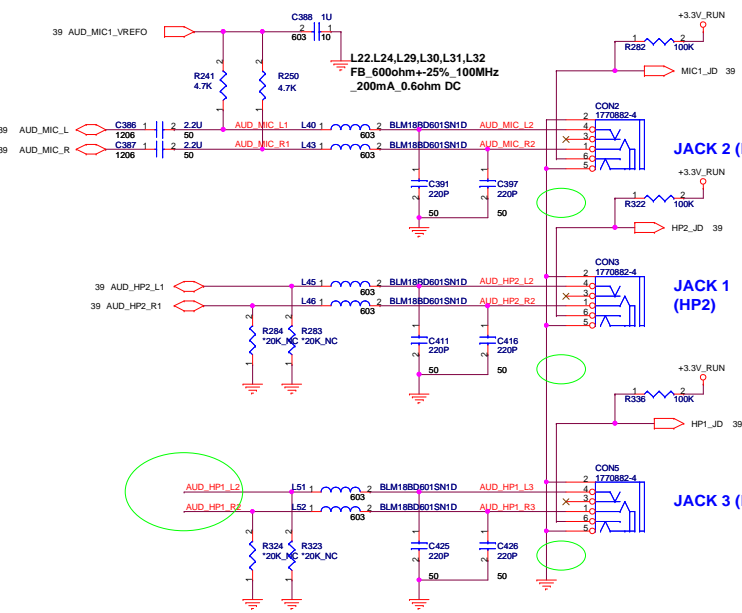


QUANTA COMPUTER

File: Azelia CODEC
 Size: Document Number FM6
 Date: Thursday, February 26, 2009
 Sheet: 39 of 64
 Rev: 1A

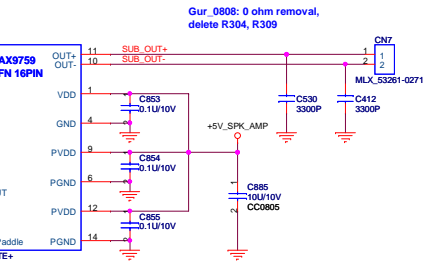
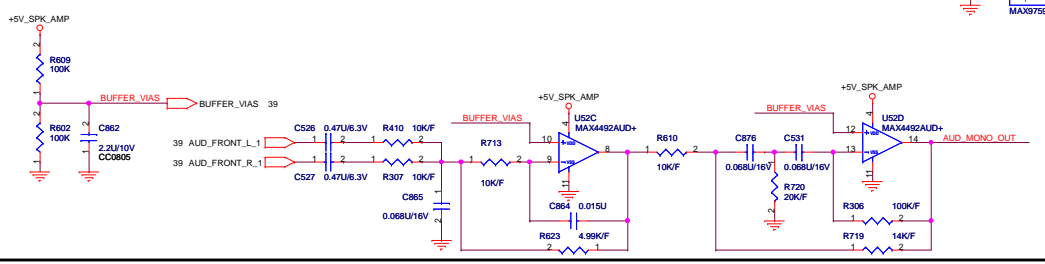
Headphone Jack Stereo MIC Jack

Array Microphone & Camera

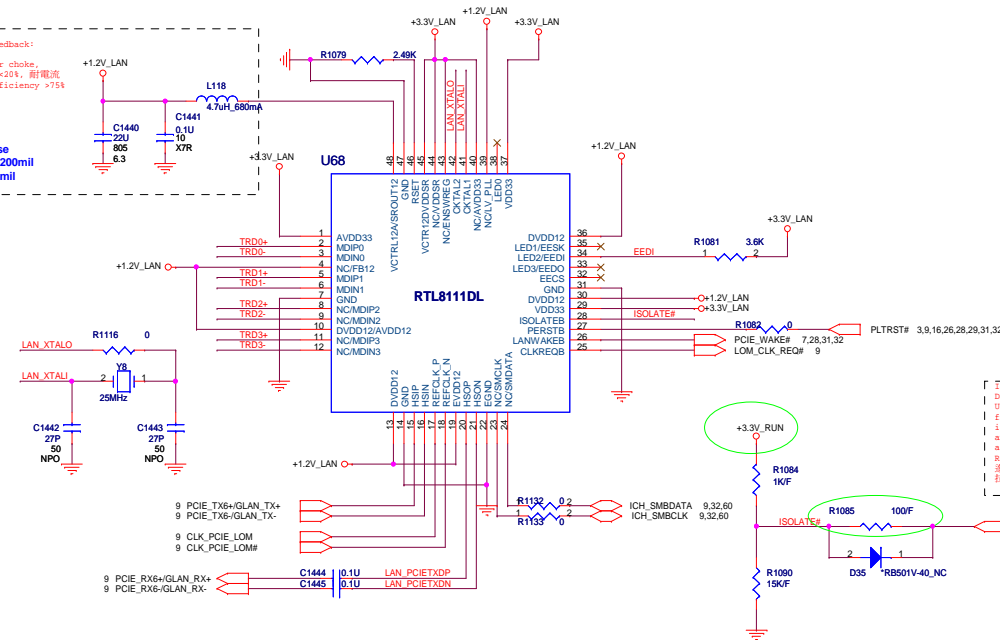
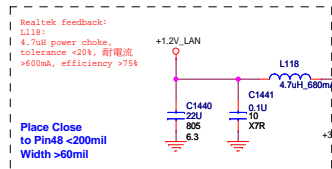
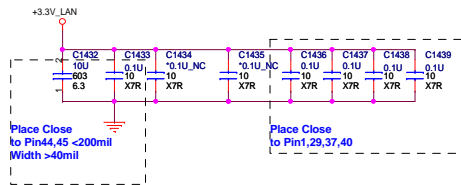
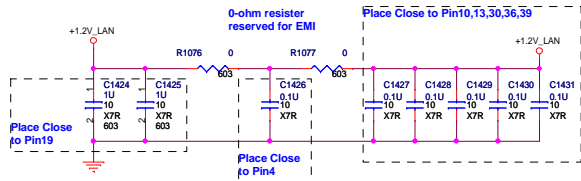


INTERNAL SUBWOOFER AMP

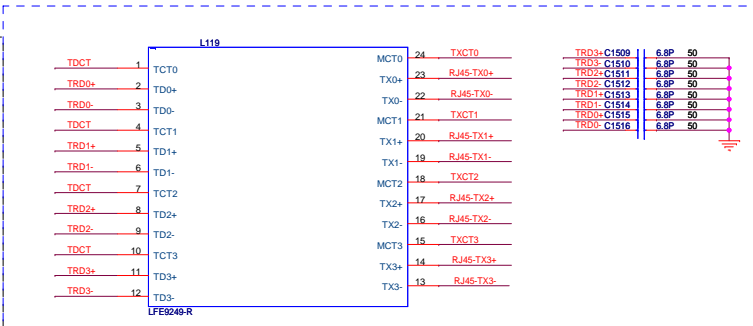
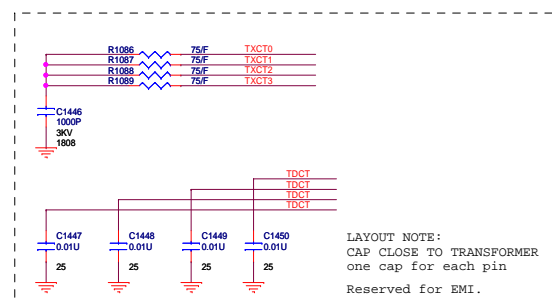
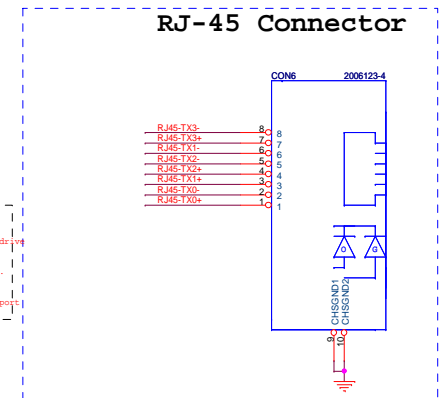
SYNC	Condition
VDD	Spread-spectrum mode with fS = 1200kHz ±70kHz.
GND	Fixed-frequency mode with fS = 1100kHz.
FLOAT	Fixed-frequency mode with fS = 1500kHz.
Clocked	Fixed-frequency mode with fS = external clock frequency.

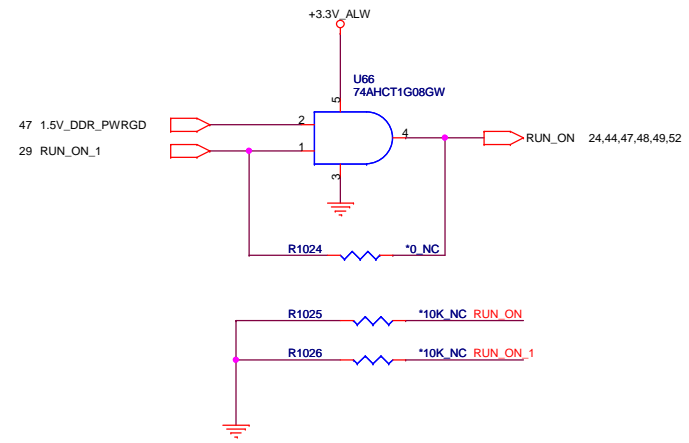
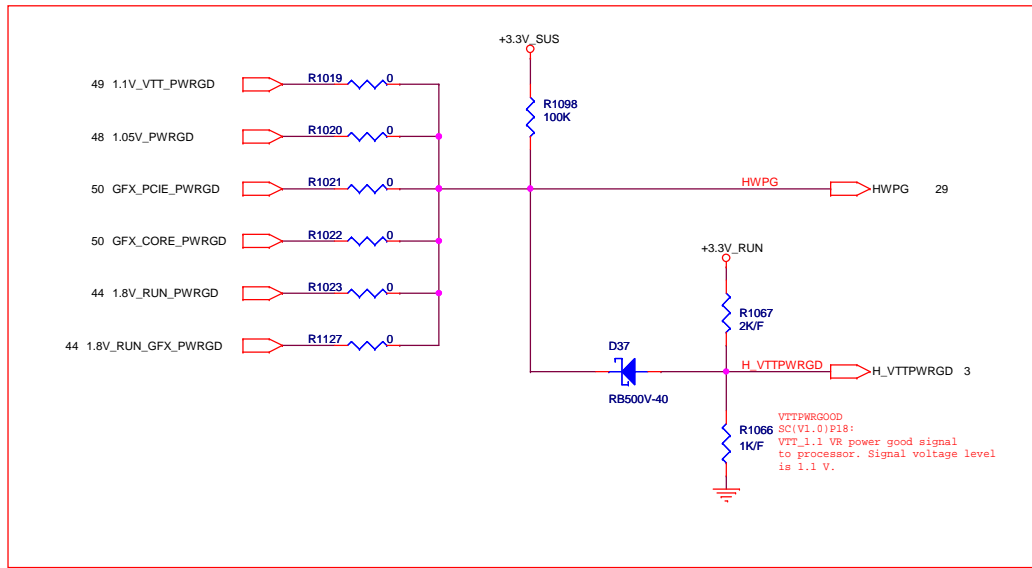
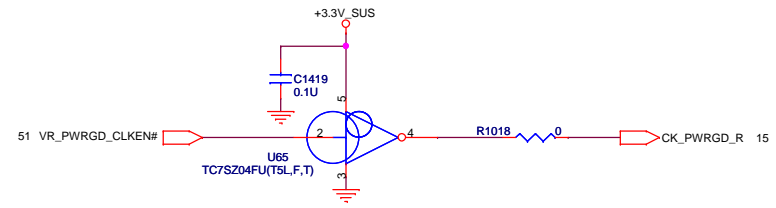
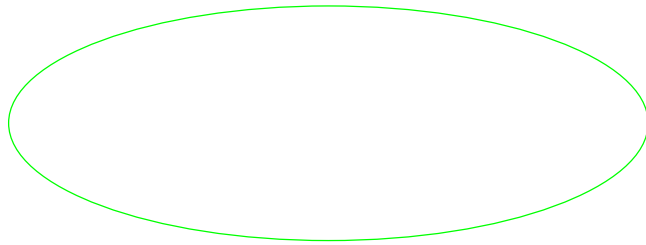


GAIN1	GAIN2	GAIN
0	0	24dB
0	1	18dB
1	0	12dB
1	1	6dB



ISOLATE#
Database(V1.419):
Used to isolate the rtl8111dl
from the PCI-E bus. RTL8111DL will not drive
its PCI-E outputs (excluding LANWAKE#)
and will not sample its PCI-E input
as long as the isolate pin is asserted.
Realtek feedback:
低电平 禁用S3,S4,S5 驱动High for WOL support





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D

 QUANTA COMPUTER		
Title Battery Selector		
Size	Document Number FM9	Rev 1A
Date:	Thursday, February 26, 2009	Sheet 43 of 64

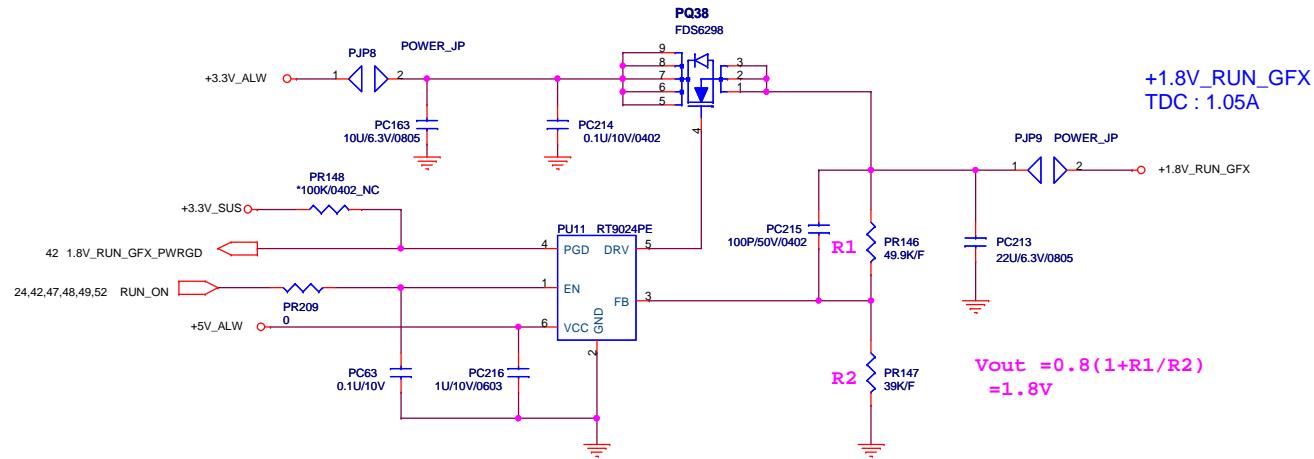
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2

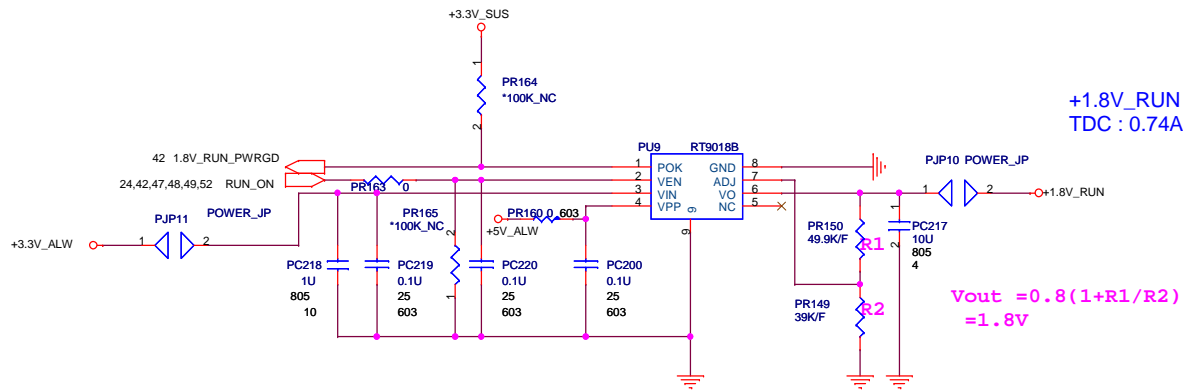
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4

5



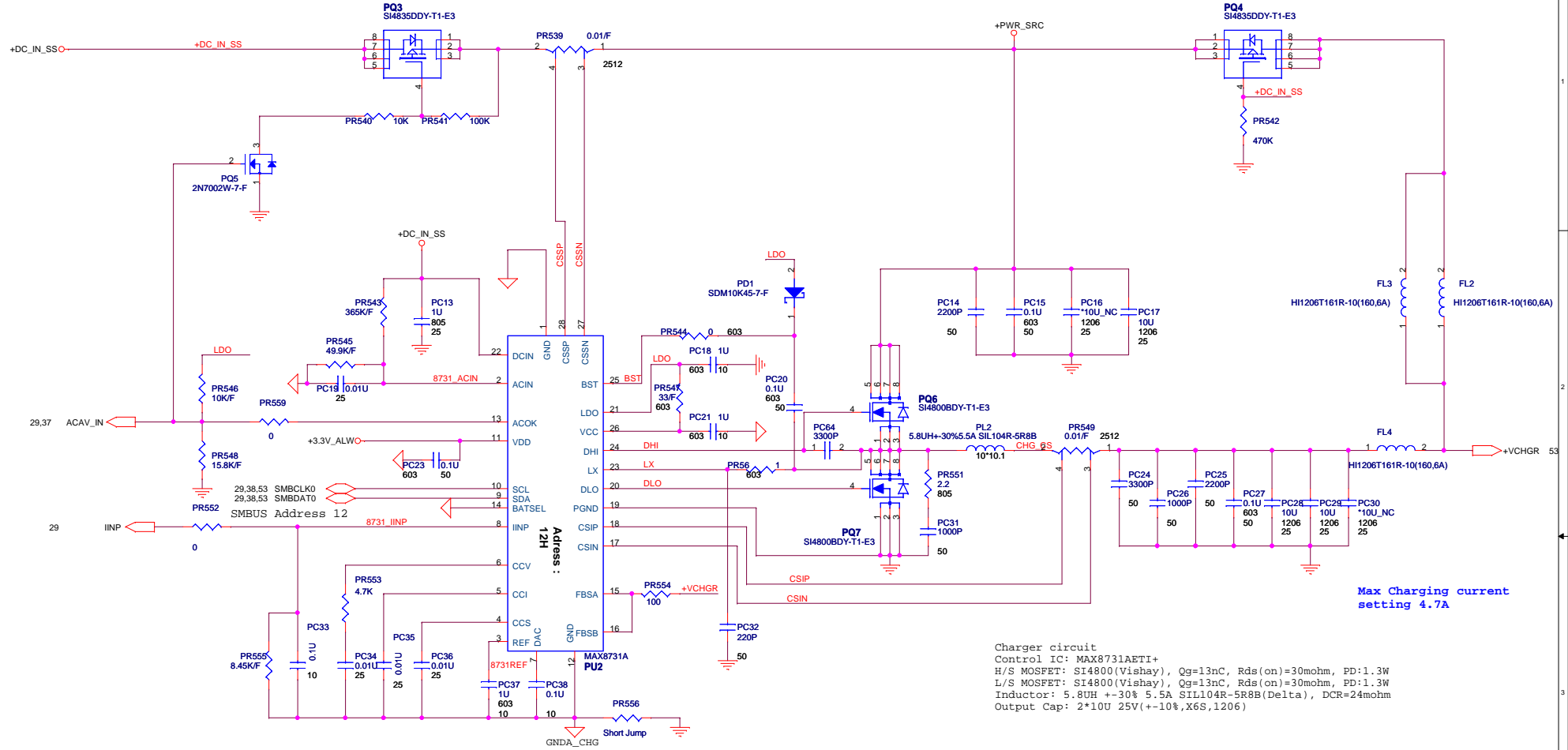
+1.8V_RUN_GFX for VGA 1.8V
+1.8V_RUN for CPU and PCH 1.8V



Title		
+1.8V_RUN_GFX (RT9024PE) & +1.8V_RUN(RT9018B)		
Size	Document Number	Rev
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Date:	Thursday, February 26, 2009	Sheet 44 of 64

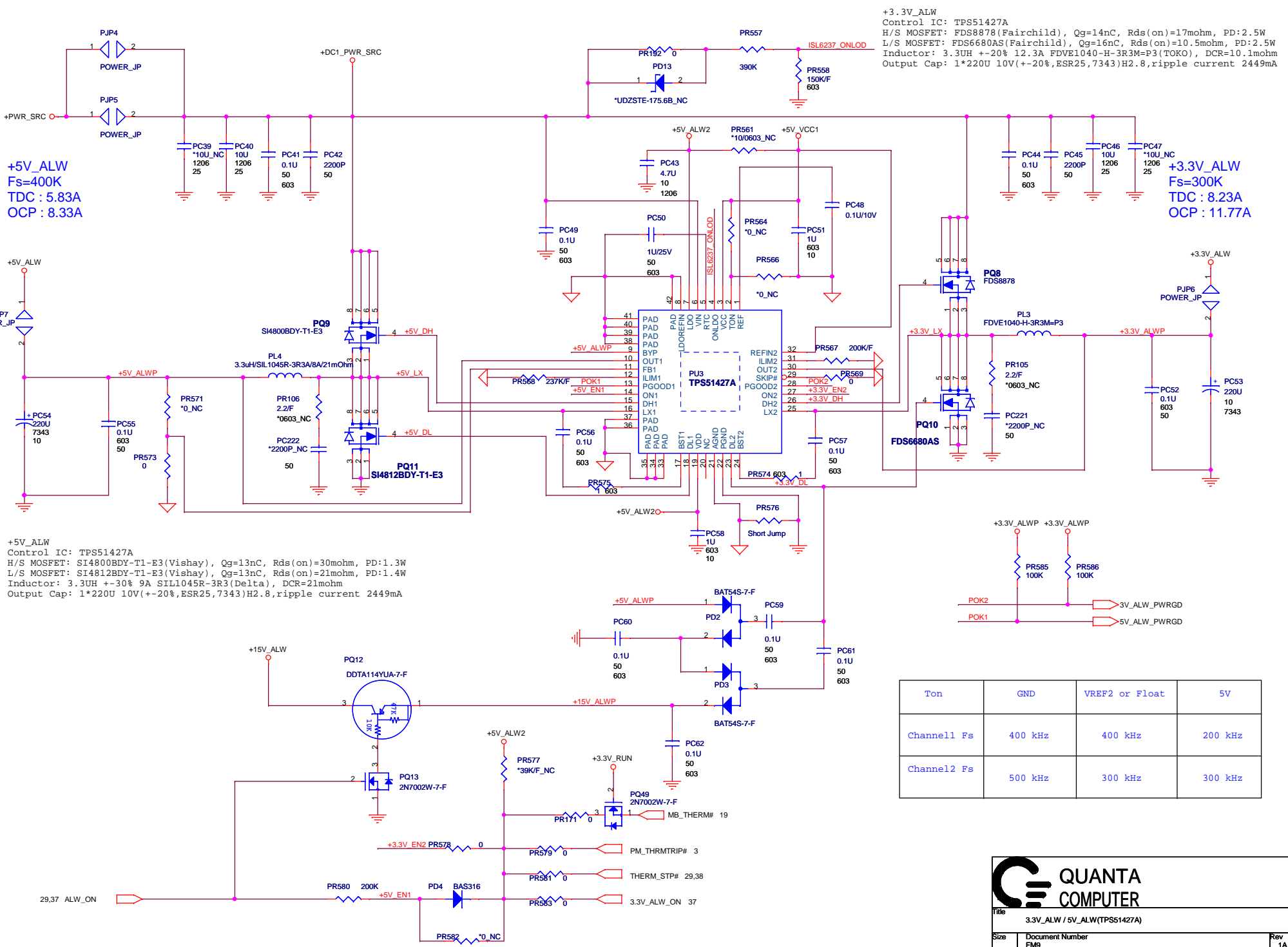
Continuous current : 13A
Rds(on) : 18mohm

Continuous current : 13A
Rds(on) : 18mohm



Max Charging current setting 4.7A

Charger circuit
Control IC: MAX8731AETI+
H/S MOSFET: SI4800(Vishay), Qg=13nC, Rds(on)=30mohm, PD=1.3W
L/S MOSFET: SI4800(Vishay), Qg=13nC, Rds(on)=30mohm, PD=1.3W
Inductor: 5.8uH +/-30% 5.5A SILL104R-5R8B(Delta), DCR=24mohm
Output Cap: 2*10u 25V(+/-10%,X6S,1206)

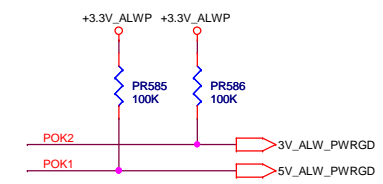


+3.3V_ALW
 Control IC: TPS51427A
 H/S MOSFET: FDS8878 (Fairchild), Qg=14nC, Rds(on)=17mohm, PD:2.5W
 L/S MOSFET: FDS6680AS (Fairchild), Qg=16nC, Rds(on)=10.5mohm, PD:2.5W
 Inductor: 3.3uH +/-20% 12.3A FDVE1040-H-3R3M-P3 (TOKO), DCR=10.1mohm
 Output Cap: 1*220U 10V(+/-20%,ESR25,7343)H2.8,ripple current 2449mA

+5V_ALW
 Fs=400K
 TDC : 5.83A
 OCP : 8.33A

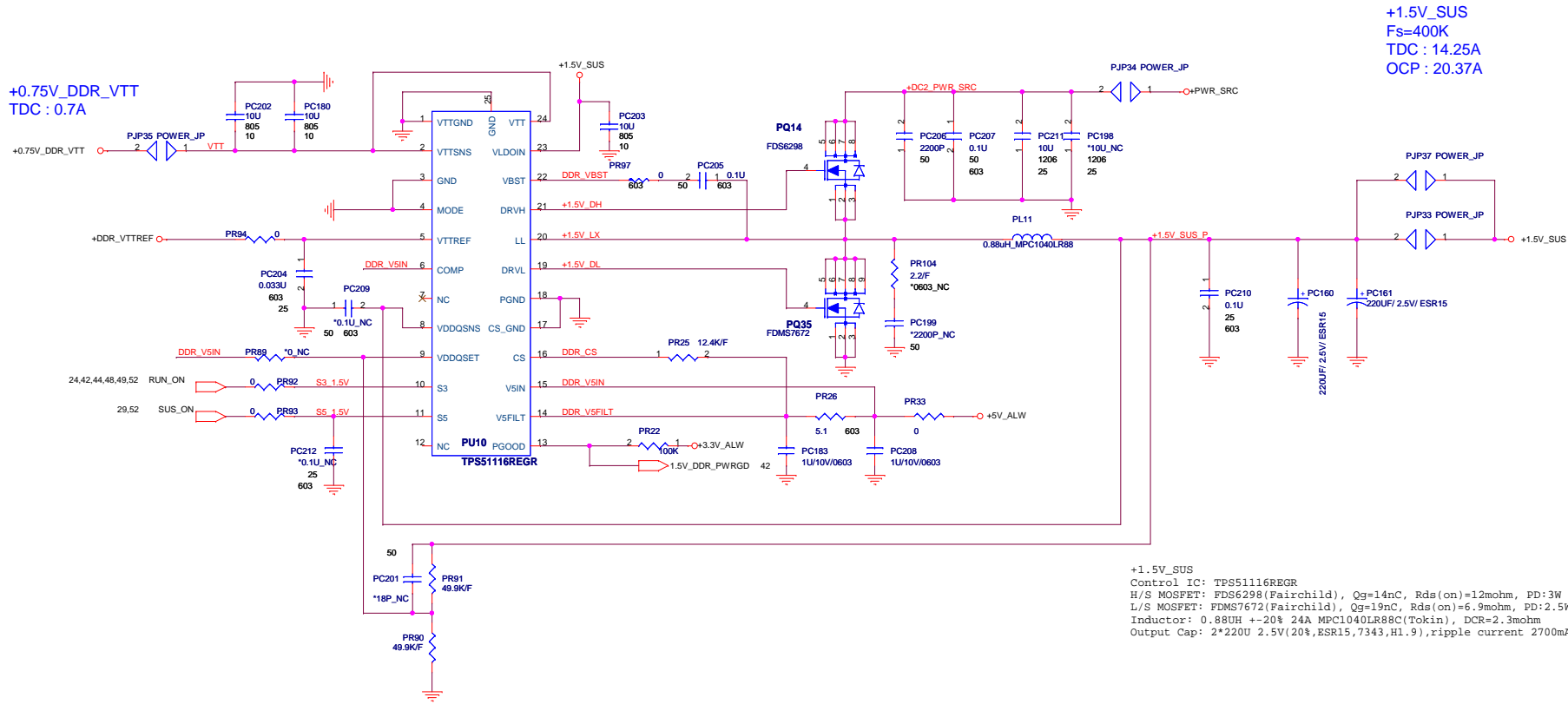
+3.3V_ALW
 Fs=300K
 TDC : 8.23A
 OCP : 11.77A

+5V_ALW
 Control IC: TPS51427A
 H/S MOSFET: SI4800BDY-T1-E3 (Vishay), Qg=13nC, Rds(on)=30mohm, PD:1.3W
 L/S MOSFET: SI4812BDY-T1-E3 (Vishay), Qg=13nC, Rds(on)=21mohm, PD:1.4W
 Inductor: 3.3uH +/-30% 9A SIL1045R-3R3 (Delta), DCR=21mohm
 Output Cap: 1*220U 10V(+/-20%,ESR25,7343)H2.8,ripple current 2449mA



Ton	GND	VREF2 or Float	5V
Channel1 Fs	400 kHz	400 kHz	200 kHz
Channel2 Fs	500 kHz	300 kHz	300 kHz





+1.5V_SUS
 Fs=400K
 TDC : 14.25A
 OCP : 20.37A

+1.5V_SUS
 Control IC: TPS51116REGR
 H/S MOSFET: FDS6298 (Fairchild), Qg=14nC, Rds(on)=12mohm, PD:3W
 L/S MOSFET: FDMS7672 (Fairchild), Qg=19nC, Rds(on)=6.9mohm, PD:2.5W
 Inductor: 0.88uH +-20% 24A MPC1040LR88C (Tokin), DCR=2.3mohm
 Output Cap: 2*220U 2.5V(20%, ESR15, 7343, H1.9), ripple current 2700mA

VDDQ and VTT discharge control

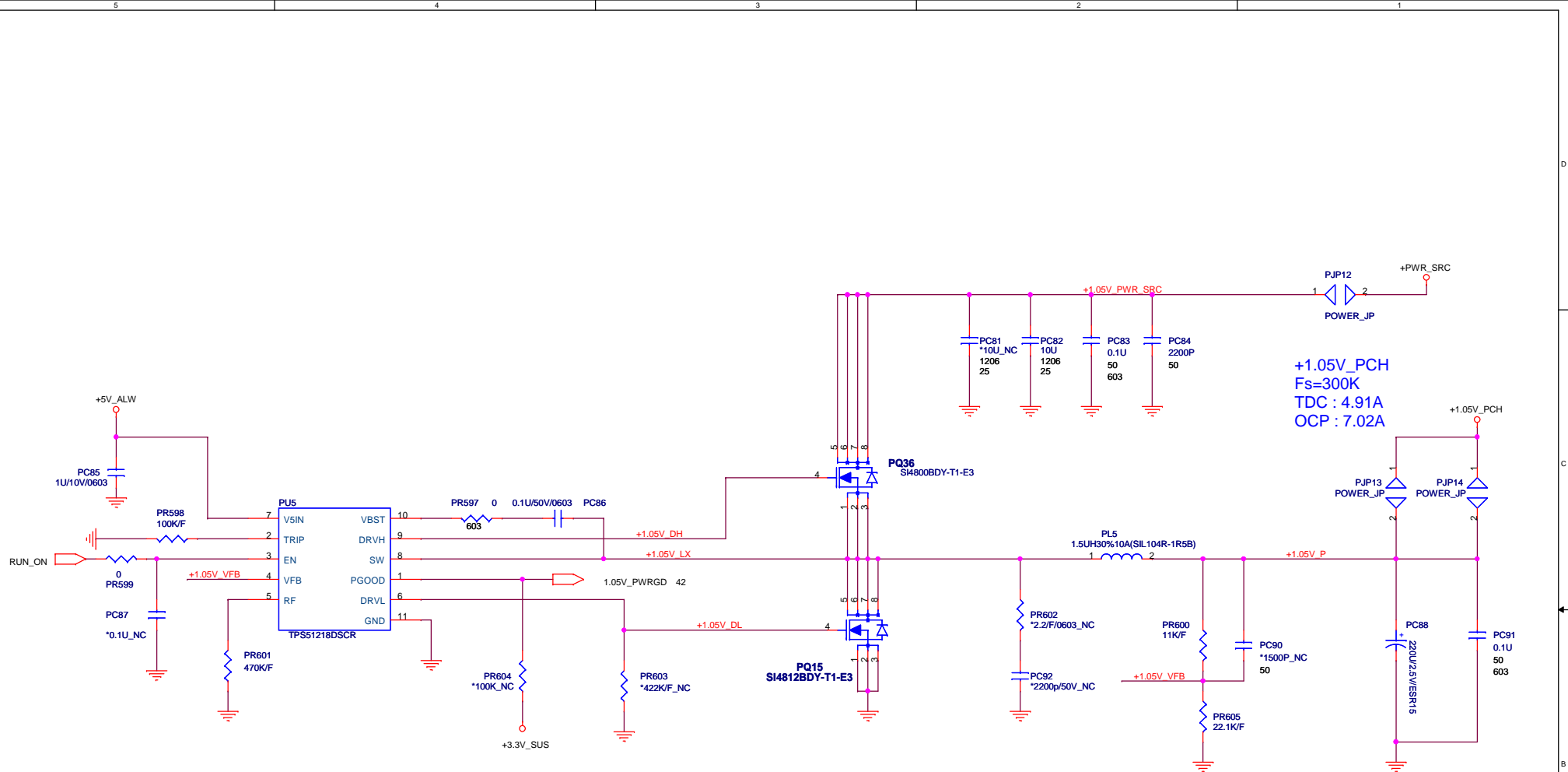
MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

VDDQ output voltage selection

VDDQSET	VDDQ(V)	VTTREF and VTT	NOTE
GND	2.5V	VDDQSNS/2	DDR
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)

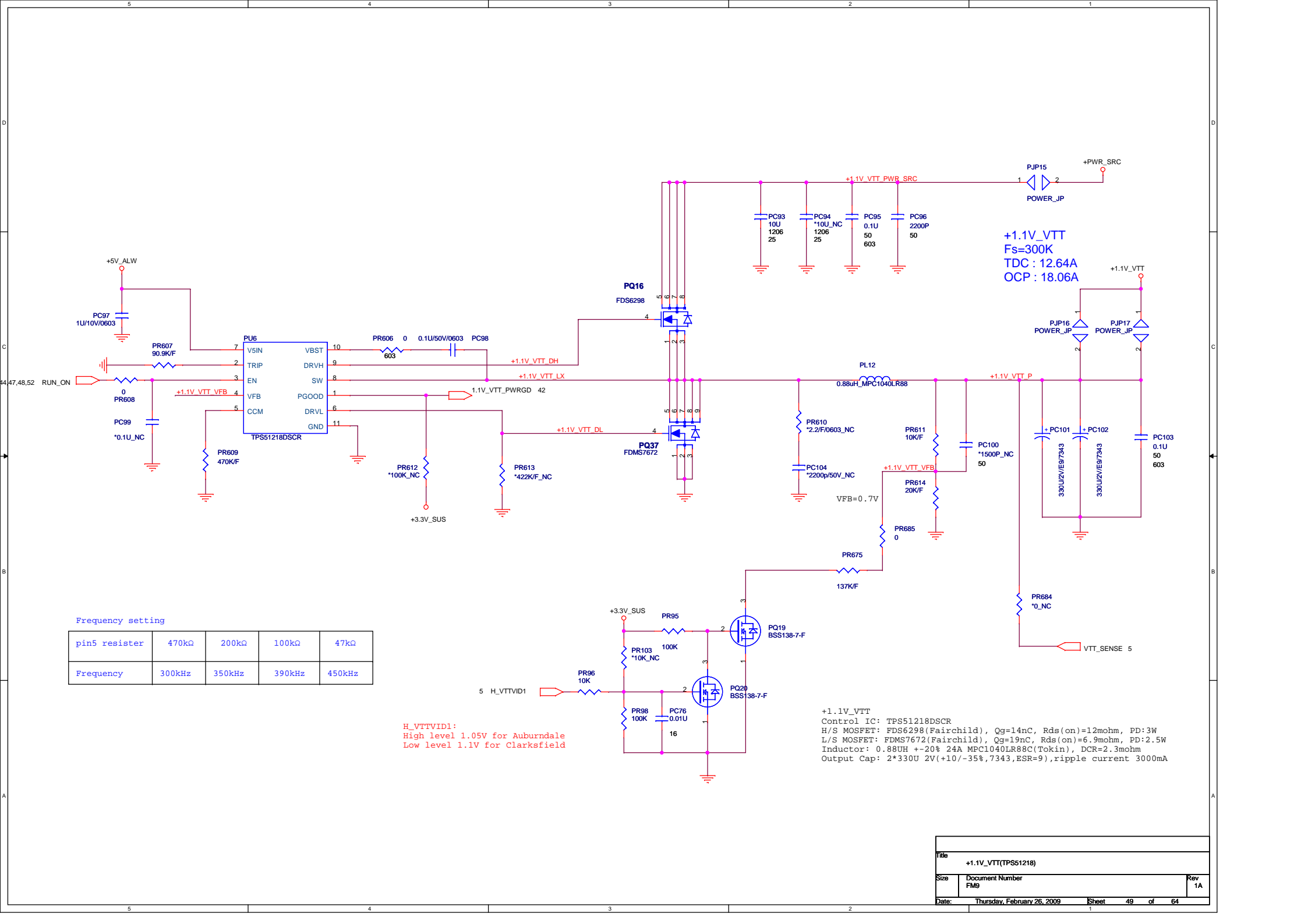


+1.05V_PCH
 Fs=300K
 TDC : 4.91A
 OCP : 7.02A

Frequency setting

pin5 resistor	470kΩ	200kΩ	100kΩ	47kΩ
Frequency	300kHz	350kHz	390kHz	450kHz

+1.05V_PCH
 Control IC: TPS51218DSCR
 H/S MOSFET: SI4800BDY-T1-E3(Vishay), Qg=13nC, Rds(on)=30mohm, PD:1.3W
 L/S MOSFET: SI4812BDY-T1-E3(Vishay), Qg=13nC, Rds(on)=21mohm, PD:1.4W
 Inductor: 1.5uH +-30% 10A SIL104R-1R5B(Delta), DCR=8.1mohm
 Output Cap: 1*220u 2.5V(20%,ESR15,7343,H1.9),ripple current 2700mA



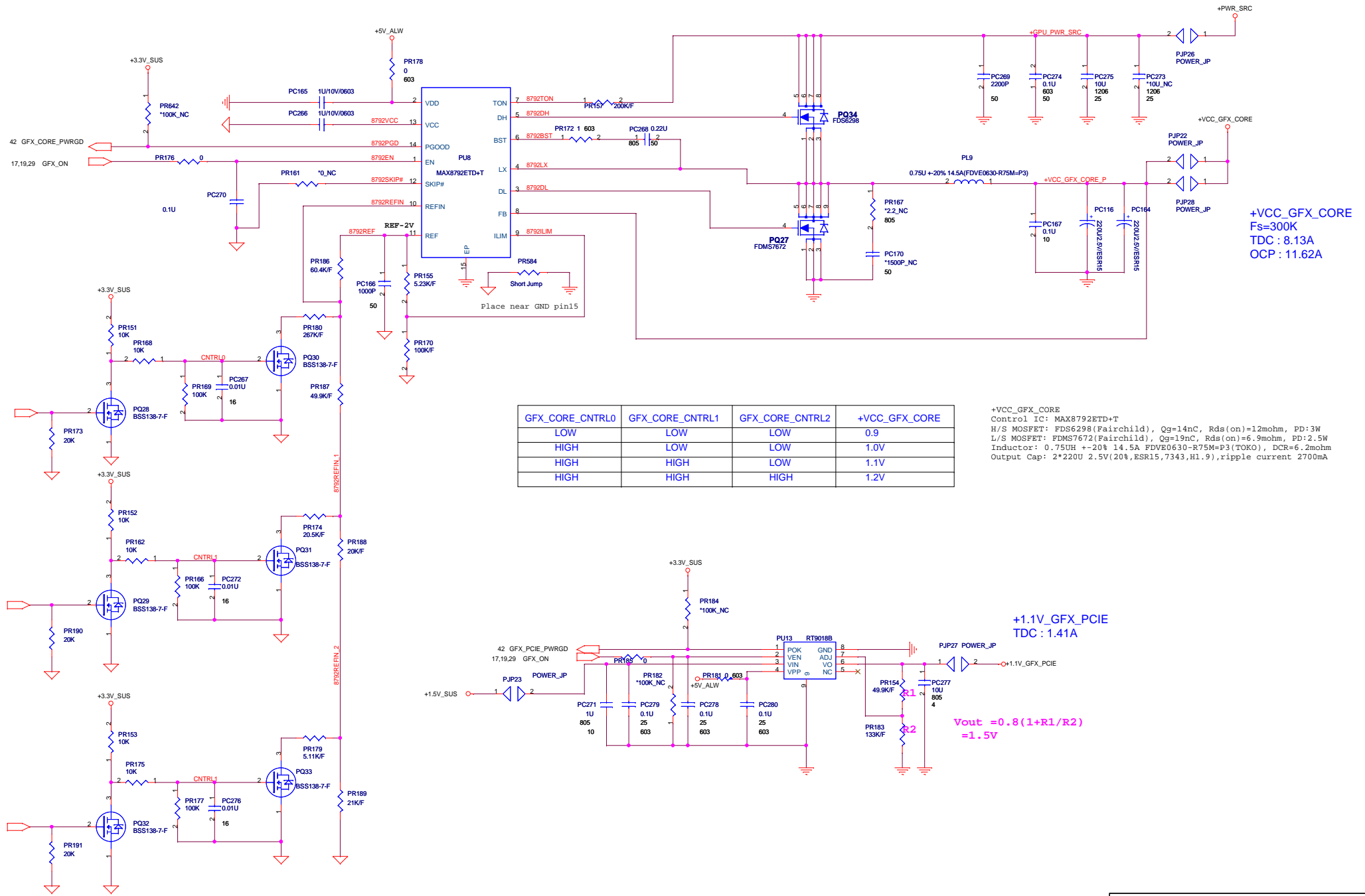
+1.1V_VTT
 Fs=300K
 TDC : 12.64A
 OCP : 18.06A

Frequency setting

pin5 resistor	470kΩ	200kΩ	100kΩ	47kΩ
Frequency	300kHz	350kHz	390kHz	450kHz

H_VTVID1:
 High level 1.05V for Auburndale
 Low level 1.1V for Clarksfield

+1.1V_VTT
 Control IC: TPS51218DSCR
 H/S MOSFET: FDS6298(Fairchild), Qg=14nC, Rds(on)=12mohm, PD:3W
 L/S MOSFET: FDMS7672(Fairchild), Qg=19nC, Rds(on)=6.9mohm, PD:2.5W
 Inductor: 0.88uH +-20% 24A MPC1040LR88C(Tokin), DCR=2.3mohm
 Output Cap: 2*330U 2V(+10/-35%,7343,ESR=9),ripple current 3000mA



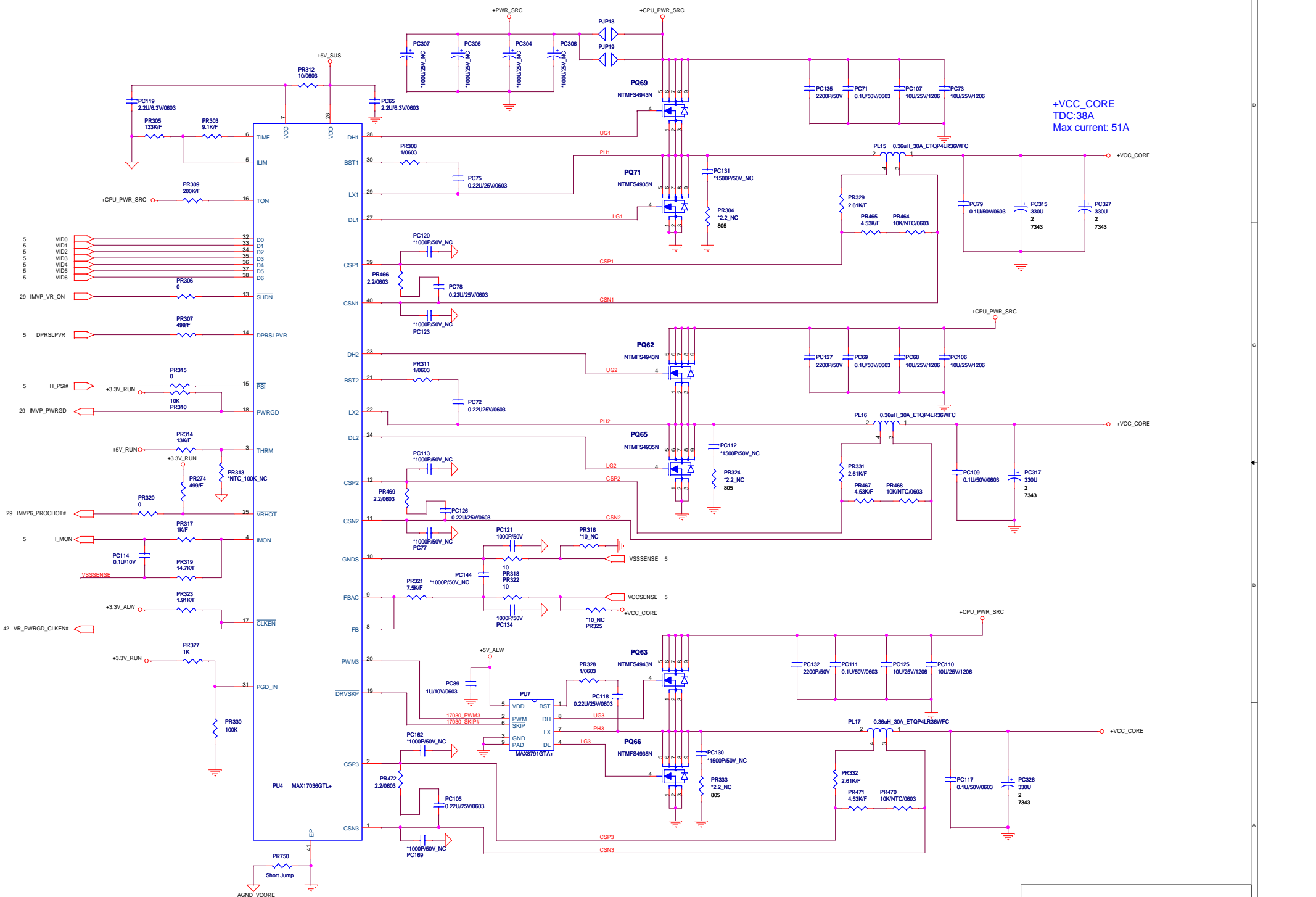
+VCC_GFX_CORE
 Fs=300K
 TDC : 8.13A
 OCP : 11.62A

GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	GFX_CORE_CNTRL2	+VCC_GFX_CORE
LOW	LOW	LOW	0.9
HIGH	LOW	LOW	1.0V
HIGH	HIGH	LOW	1.1V
HIGH	HIGH	HIGH	1.2V

+VCC_GFX_CORE
 Control IC: MAX8792ETD+T
 H/S MOSFET: FDS6298 (Fairchild), Qg=14nC, Rds(on)=12mohm, PD:3W
 L/S MOSFET: FDS57672 (Fairchild), Qg=19nC, Rds(on)=6.9mohm, PD:2.5W
 Inductor: 0.75uH +/-20% 14.5A FDVE0630-R75M-P3 (TOKO), DCR=6.2mohm
 Output Cap: 2*220u 2.5V(20%,ESR15,7343,H1.9), ripple current 2700mA

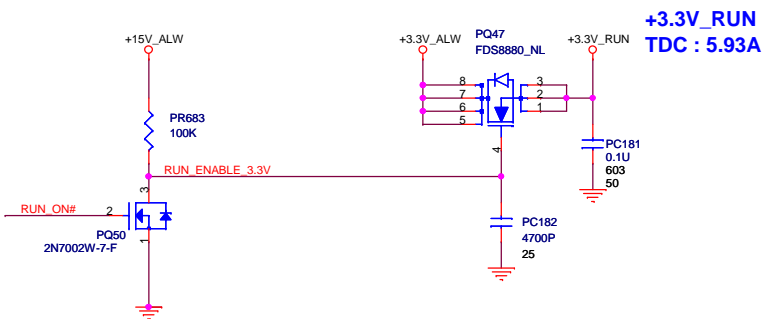
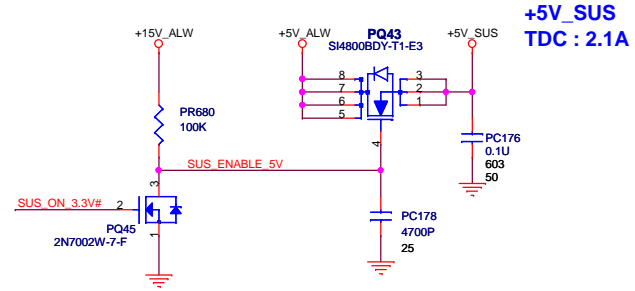
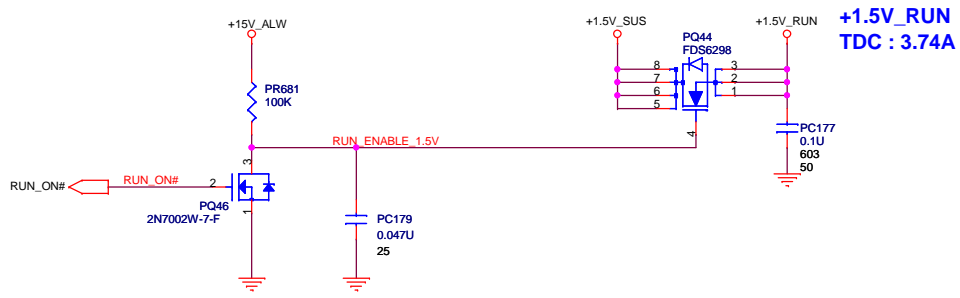
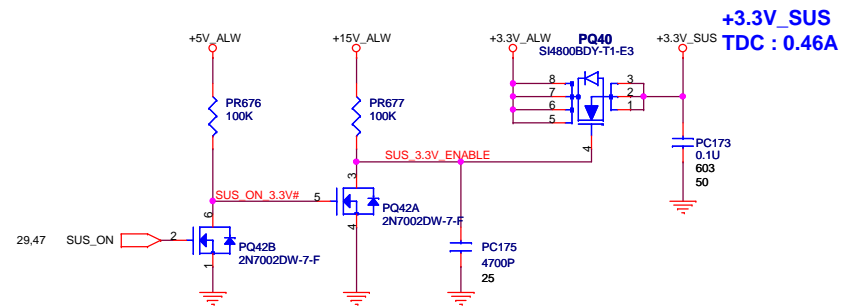
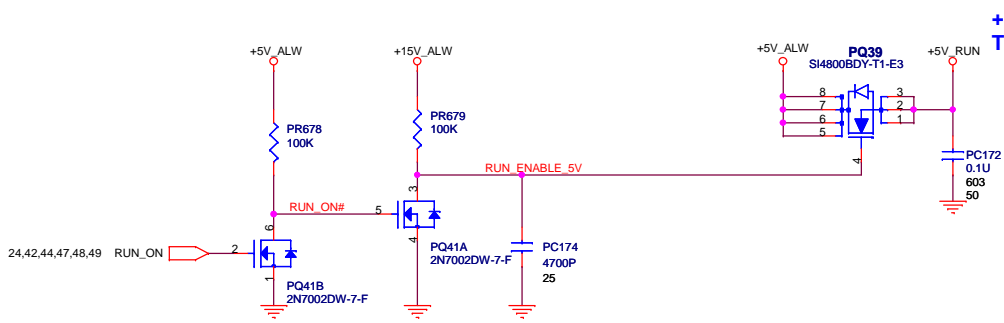
+1.1V_GFX_PCIE
 TDC : 1.41A

$V_{out} = 0.8(1 + R1/R2) = 1.5V$

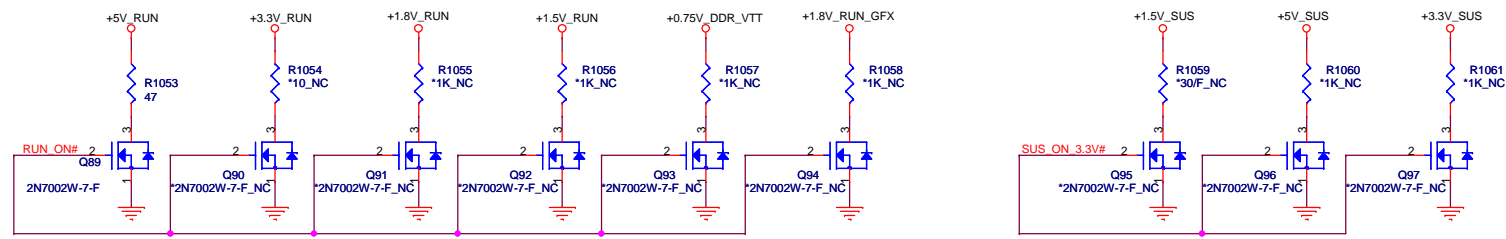


+VCC_CORE
TDC:38A
Max current: 51A

Title		CPU core (MAX17036)		Rev	
Size	Document Number	FM9		Rev	<Rev Code>
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Reserve discharge path

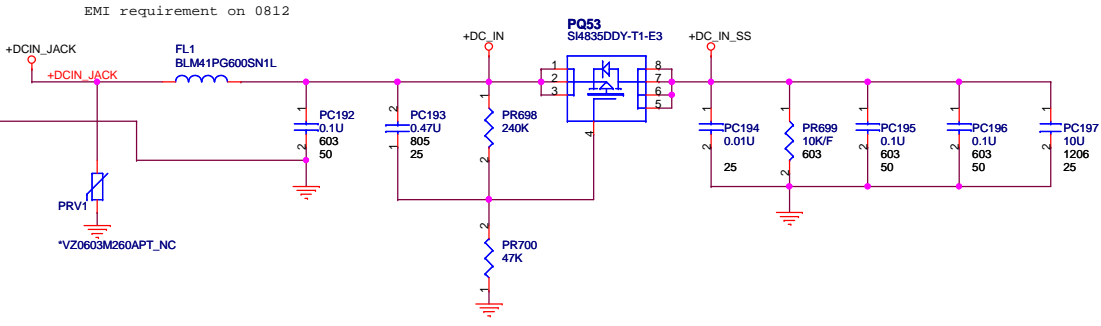
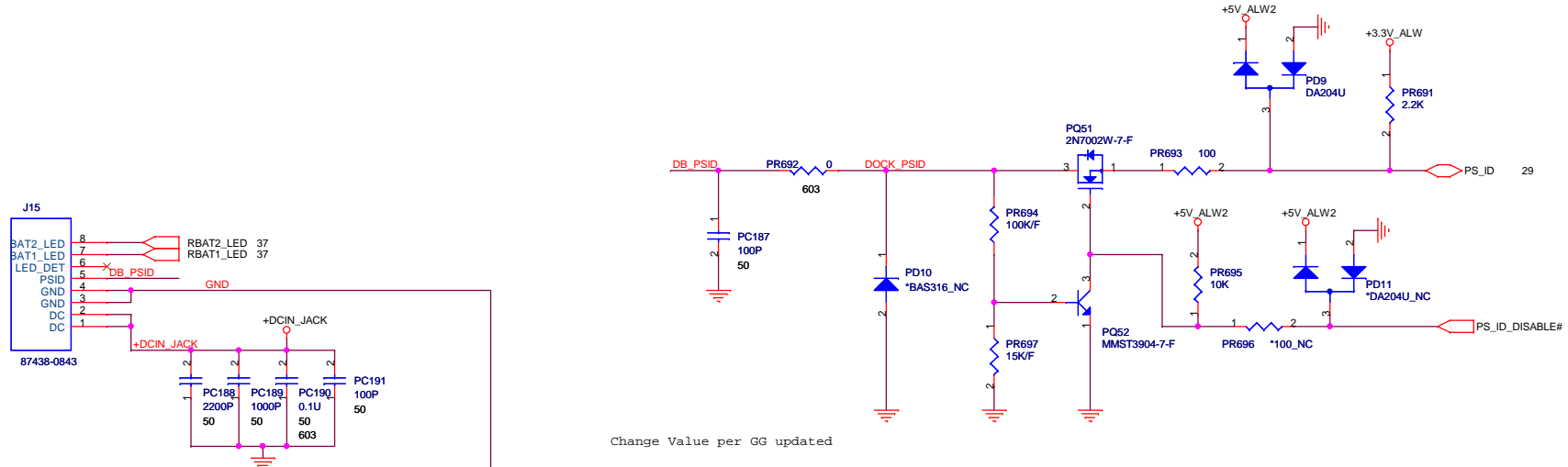
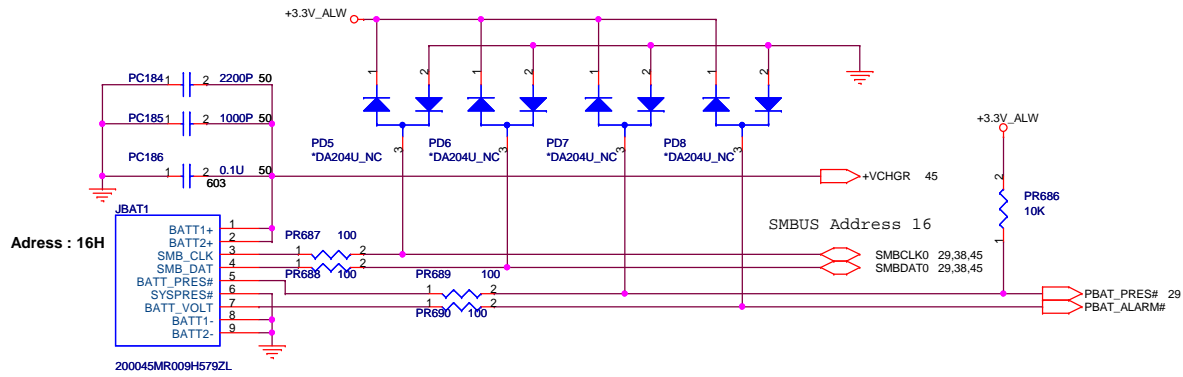


**QUANTA
COMPUTER**

Title: RUN / SUS POWER SW

Size	Document Number	Rev
	FMG	1A

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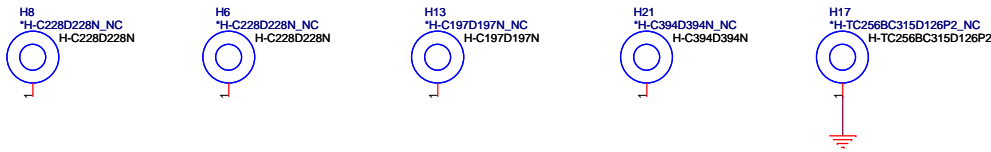
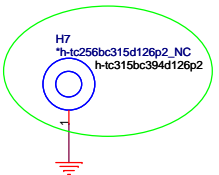
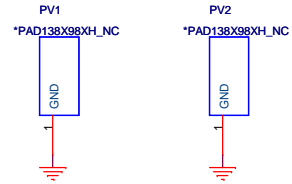
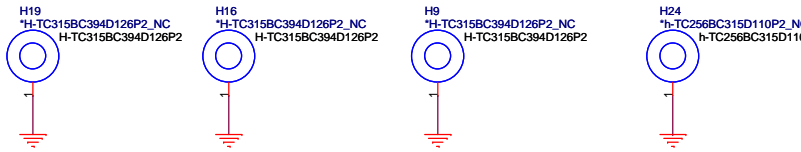
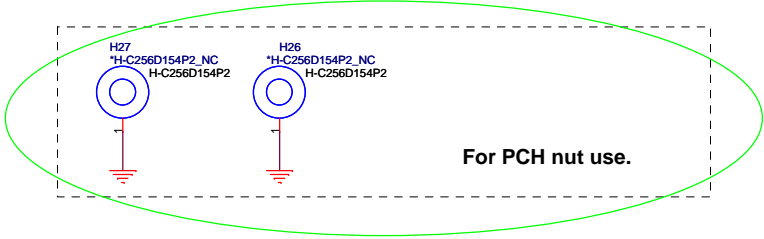
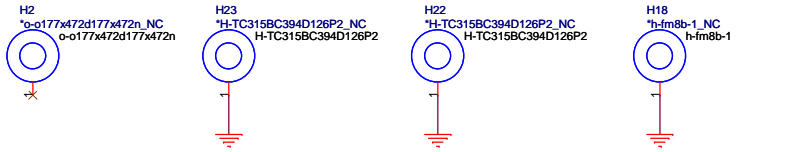
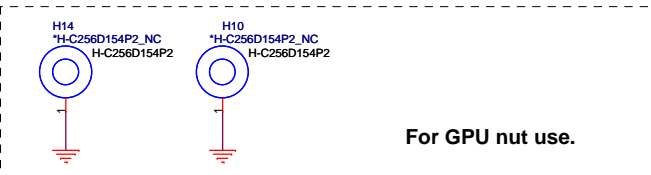
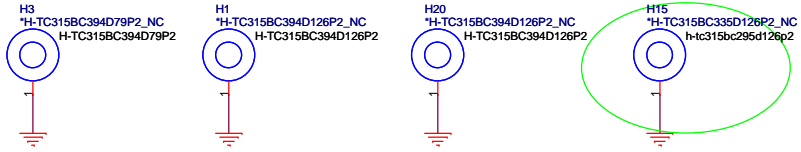
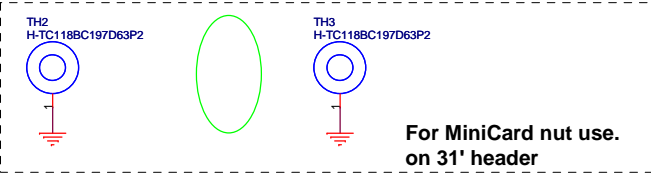
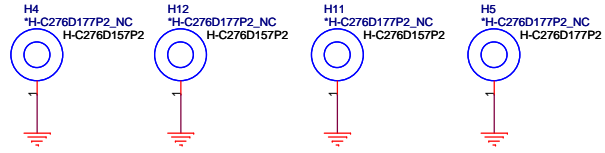
QUANTA COMPUTER

Title: DCIN,BATT CONNECTOR

Size: F19	Document Number: F19	Rev: 1A
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FOR CPU use



Title			SCREW PAD
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Reserved for EMI.

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 QUANTA COMPUTER		
Title EMI CAP		
Size	Document Number FM9	Rev 1A
Date: Thursday, February 26, 2009		
Sheet 55 of 64		1

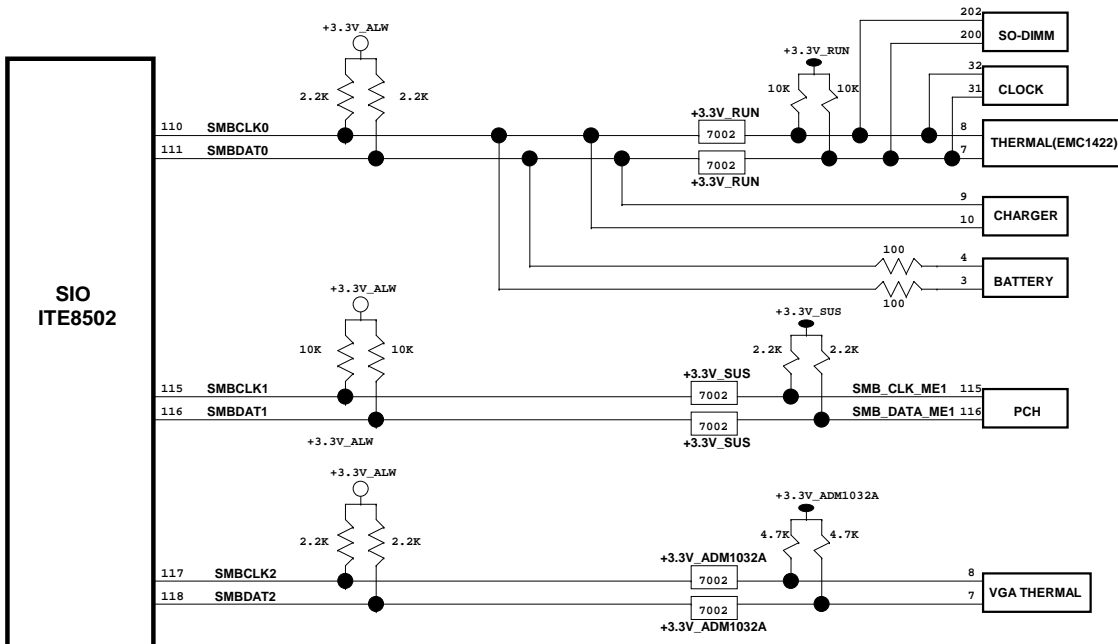
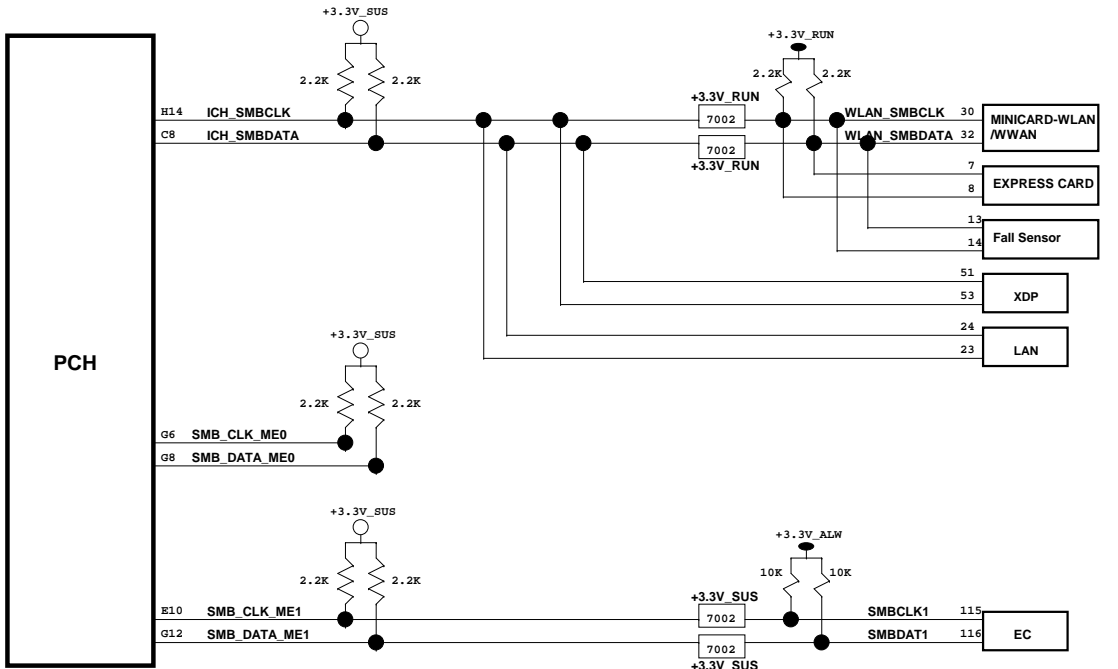
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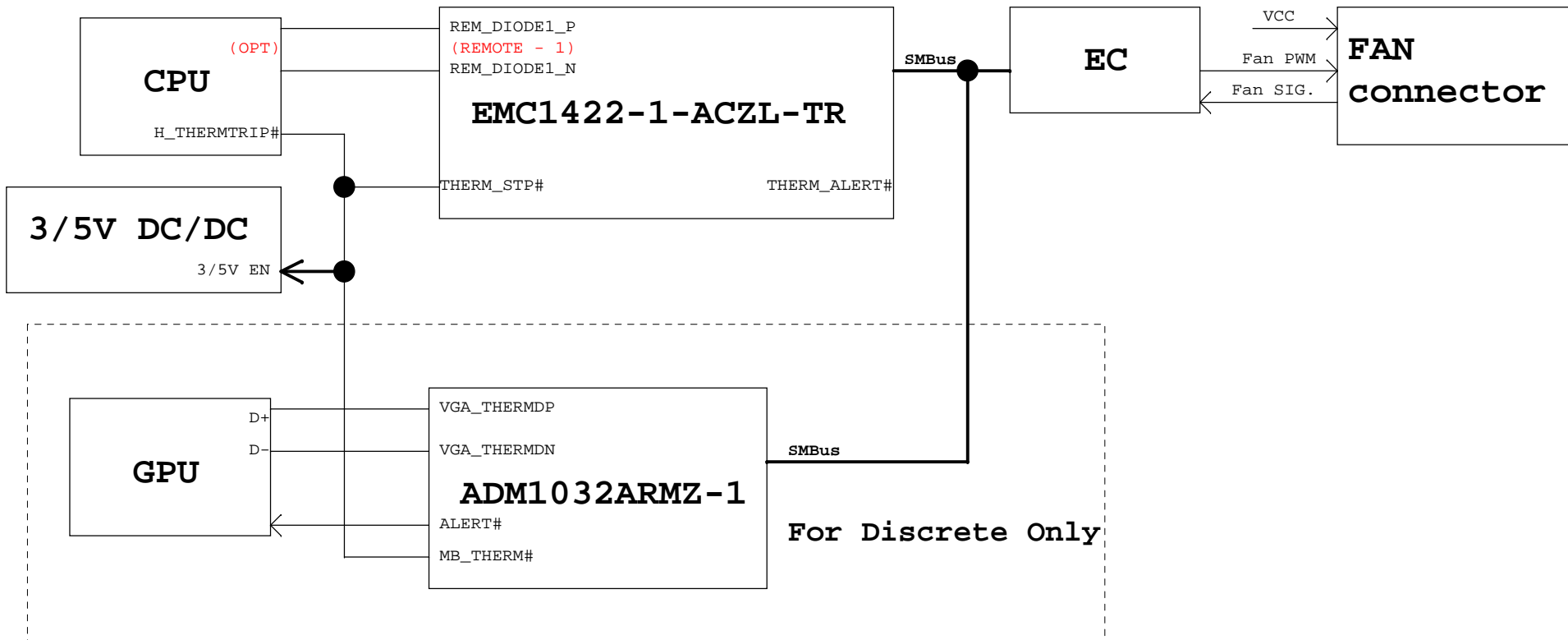
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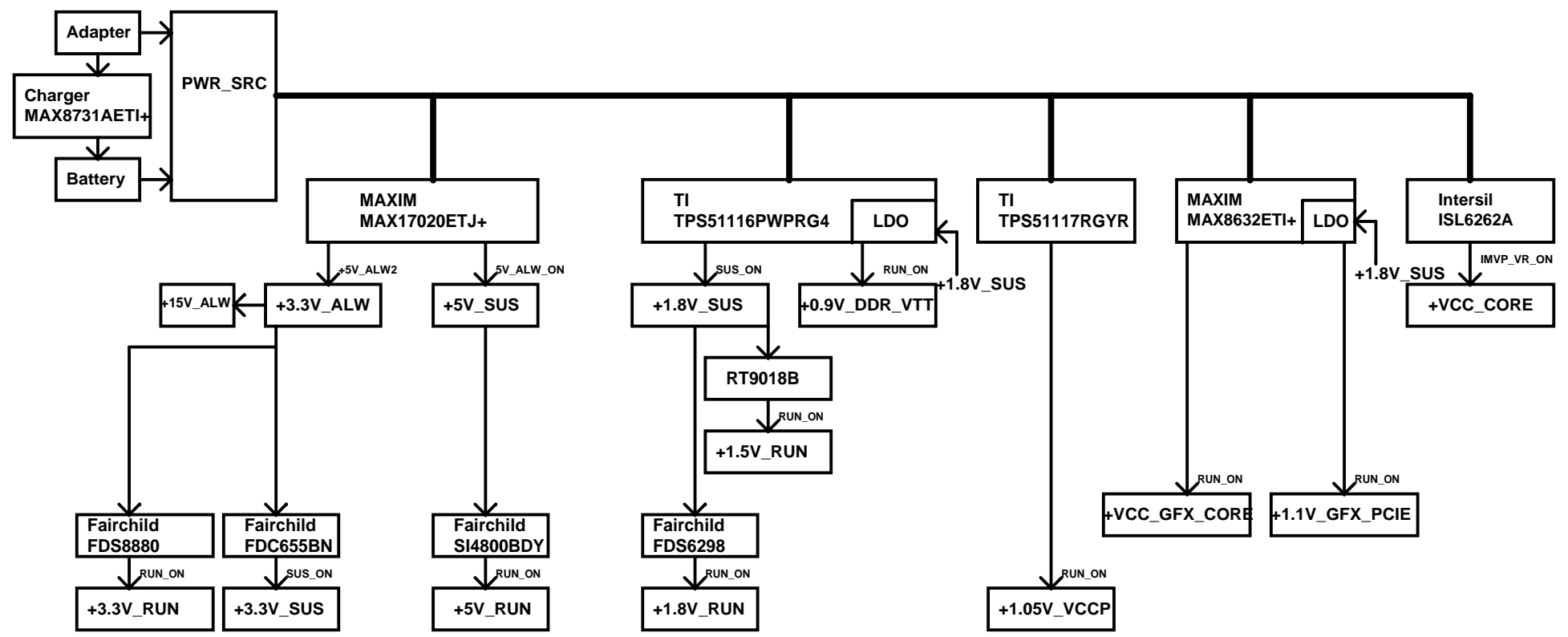
3

2

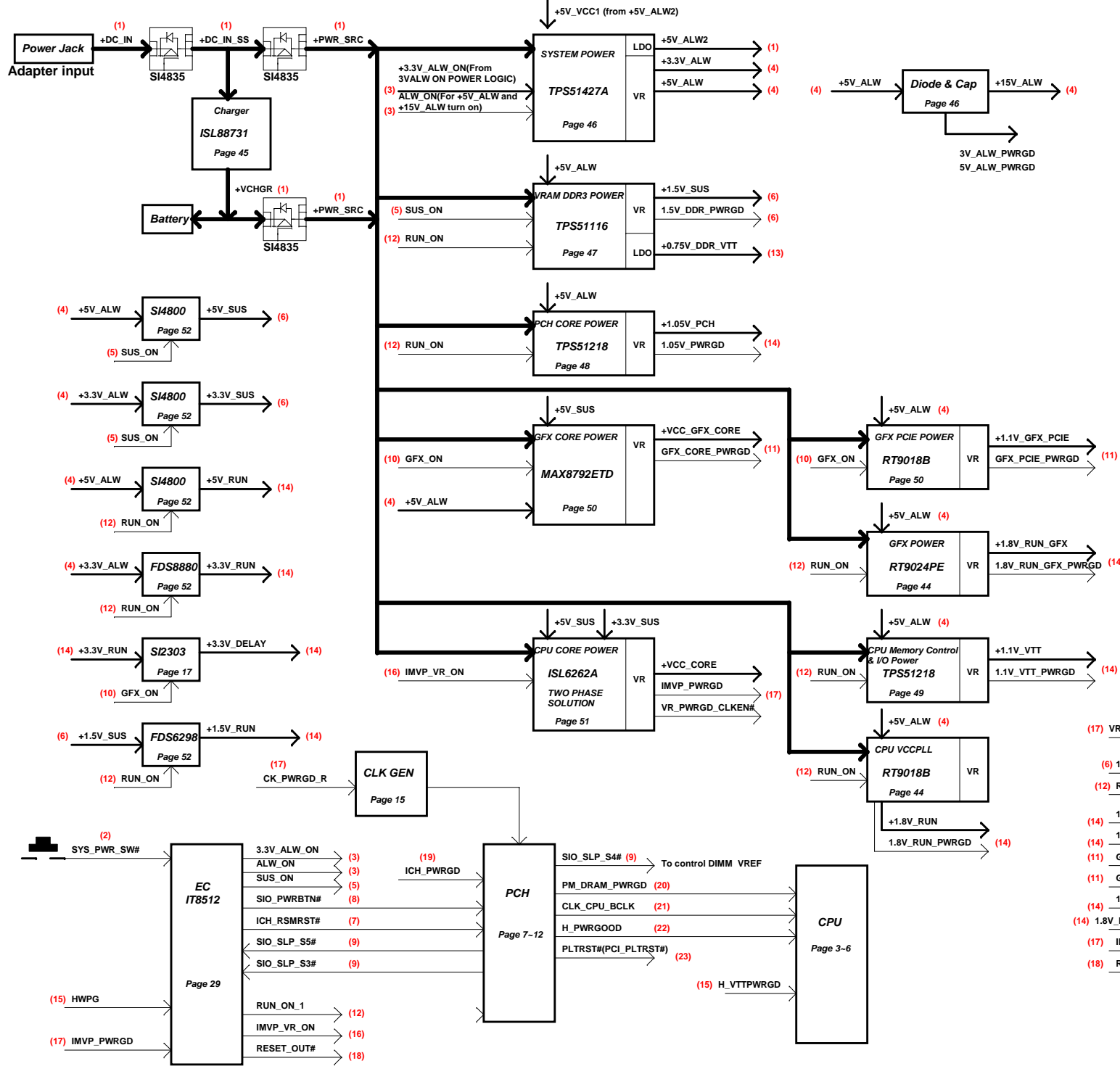
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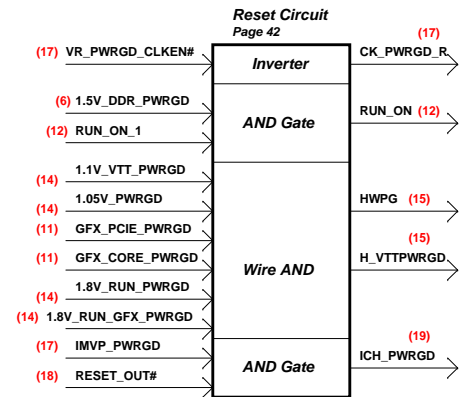


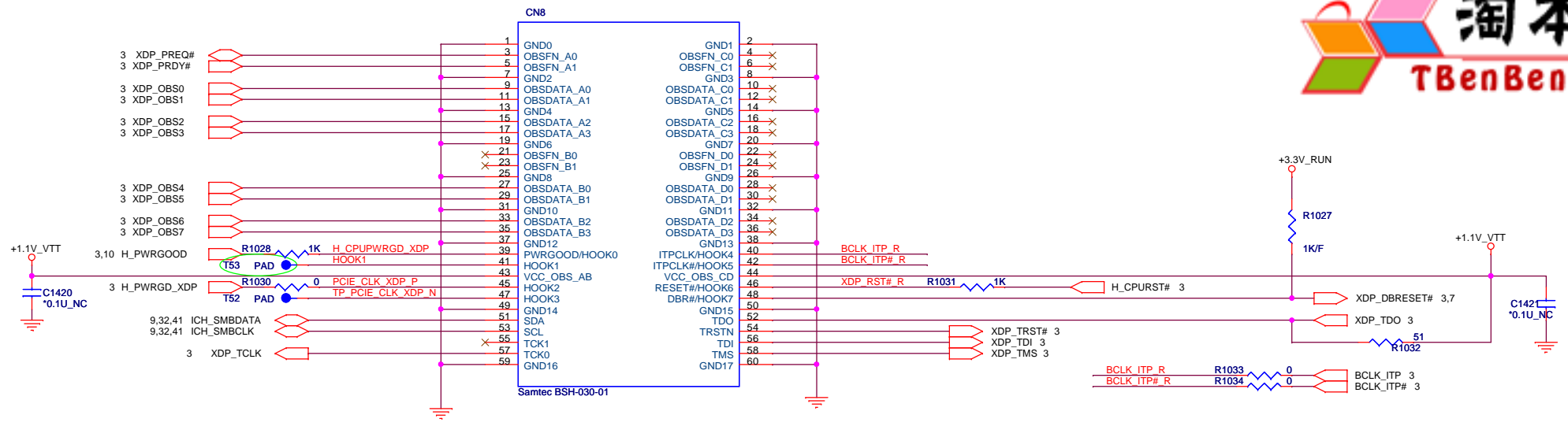



FM9 Power Design Block Diagram 2009/02/25



- (1) AC : DC_IN -> DC_IN_SS -> +PWR_SRC
Bat : +VCHGR -> +PWR_SRC, +5V_ALW2, SYS_PWR_SW#
- (2) SYS_PWR_SW#
- (3) 3.3V_ALW_ON, ALW_ON
- (4) +3.3V_ALW, +5V_ALW, +15V_ALW
- (5) SUS_ON
- (6) +5V_SUS, +3.3V_SUS, +1.5V_SUS, 1.5V_DDR_PWRGD
- (7) ICH_RSMRST#
- (8) SIO_PWRBTN#
- (9) SIO_SLP_S5#, SIO_SLP_S4#, SIO_SLP_S3#
- (10) GFX_ON
- (11) +VCC_GFX_CORE, +1.1V_GFX_PCIE and PWRGD
- (12) RUN_ON_1(RUN_ON)
- (13) +0.75V_DDR_VTT
- (14) +5V_RUN, +3.3V_RUN, +3.3V_DELAY, +1.8V_RUN_GFX, +1.5V_RUN, +1.1V_VTT, +1.05V_PCH ad PWRGD
- (16) IMVP_VR_ON
- (17) +VCC_CORE, IMVP_PWRGD
- (18) RESET_OUT#
- (19) ICH_PWRGD
- (20) PM_DRAM_PWRGD
- (21) CLK_CPU_BCLK(PCH to CPU)
- (22) H_PWRGOOD
- (23) PLTRST#(PCI_PLTRST#)



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Title		Rev
SMBUS BLOCK		1A
Size	Document Number	
	FM9	
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