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Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	4,26,32,34,46,48,49,51,52,56	MAIN POWER		S0-S5
+RTC_CELL	+3.0V~+3.3V	11,14,31,32	RTC		S0-S5
+3.3V_ALW	+3.3V	3,31,32,34,36,37,38,44,46,49,52,53,54	8051 POWER	ALWON	S0-S5
+5V_ALW	+5V	35,36,46,48,49,52,53,54,56	LCD/CHARGE POWER	ALWON	S0-S5
+15V_ALW	+15V	26,36,37,52,53	LARGE POWER	+5V_ALW	S0-S5
+3.3V_LAN	+3.3V	42,43	LAN POWER	AUX_ON	
+5V_SUS	+5V	14,38,51,53	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	3,11,12,13,14,26,30,37,38,43,48,49,51,53	SLP_S5# CTRLD POWER	3.3V_SUS_ON	
+1.8V_SUS	+1.8V	6,8,9,15,48,49,53	SODIMM POWER	DDR_ON	
+0.9V_DDR_VTT	+0.9V	16,49,53	SODIMM POWER	0.9V_DDR_VTT_ON	
+5V_RUN	+5V	14,18,27,36,37,38,39,40,41,53	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	14,18,27,36,37,38,39,40,41,53	SLP_S3# CTRLD POWER	3.3V_RUN_ON	
+1.8V_RUN	+1.8V	18,38,53	SDVO POWER	RUN_ON	
+1.5V_RUN	+1.5V	4,9,14,30,33,34,48,53,56	CALISTOGA/ICH8 POWER	1.5V_RUN_ON	
+1.25V_RUN	+1.25V	6,9,14,49,53	CALISTOGA/ICH8 POWER	1.25V_RUN_ON	
+1.05V_VCCP	+1.05V	3,4,5,6,8,9,11,14,48,56	CPU/CALISTOGA/ICH8 POWER	1.05V_RUN_ON	
+VCC_CORE	+0.7V~+1.77V	4,51,56	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	26	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	36	Module Power	MODC_EN#	
+5V_HDD	+5V	36	HDD Power	HDDC_EN#	
+PBATT	+10V~+17V		MAIN BATTERY	CHG_PBATT	
+SBATT	+10V~+17V		SECOND BATTERY	CHG_SBATT	

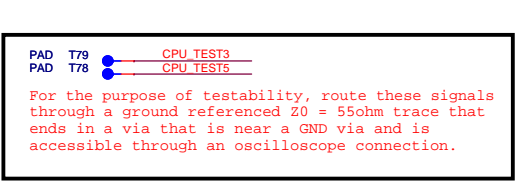
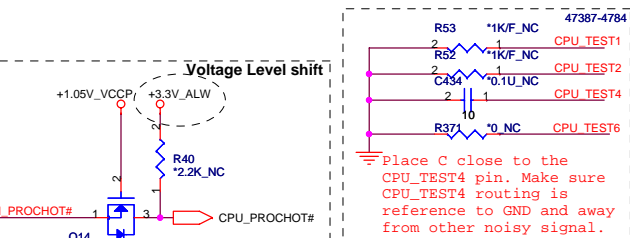
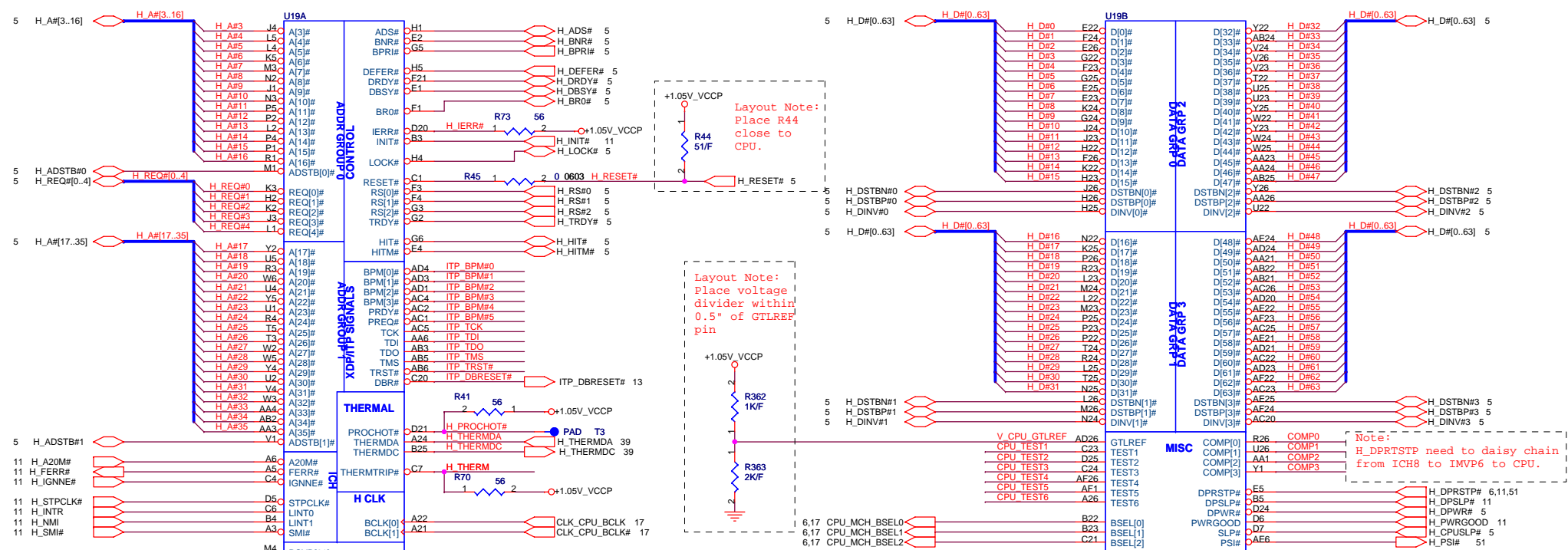
GND PLANE	PAGE	DESCRIPTION
⏚ 8731AGND	46	
⏚ AGND_0.9V	49	
⏚ AGND_DC/DC	52	
⏚ AGND_DC2	48	
⏚ AGND_DDR	49	
⏚ AGND_ISL6260	51	
⏚ GND	ALL	



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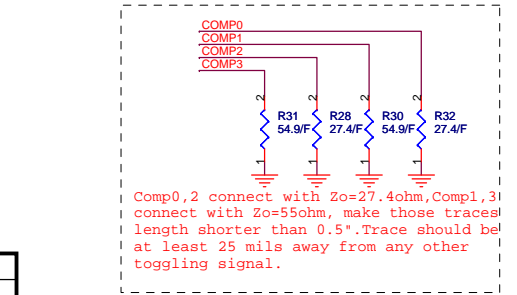
Title: Index & Power Status

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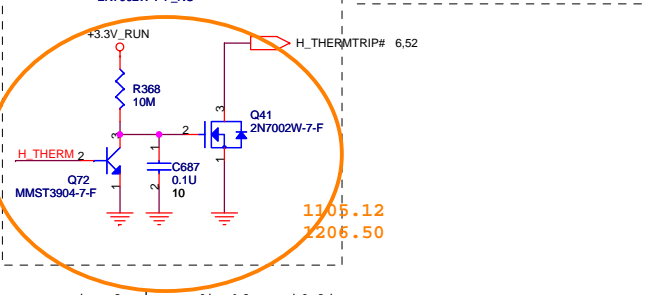
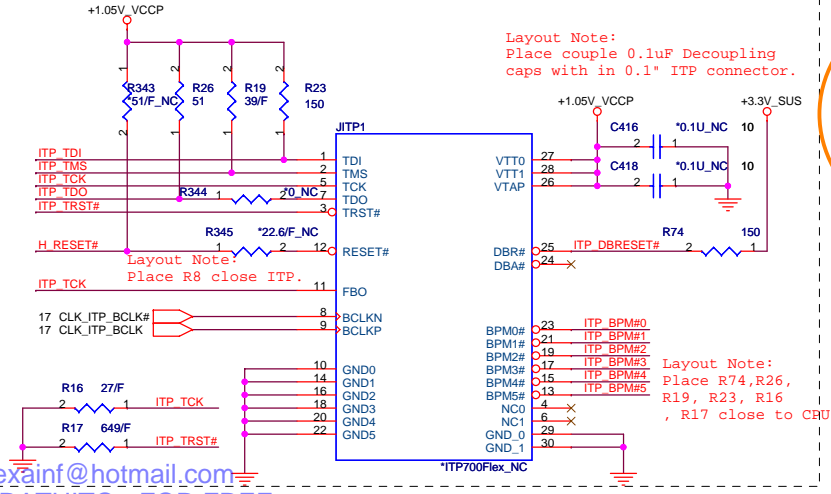


PAD	T79	CPU TEST3
COMP0 <td>R26</td> <td>COMP0</td>	R26	COMP0
COMP1 <td>U26</td> <td>COMP1</td>	U26	COMP1
COMP2 <td>AA1</td> <td>COMP2</td>	AA1	COMP2
COMP3 <td>Y1</td> <td>COMP3</td>	Y1	COMP3

For the purpose of testability, route these signals through a ground referenced Z0 = 55ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.



Populate ITP700Flex for bringup



Signal	ITP disable guidelines
TDI	Resistor Value
TMS	150 ohm +/- 5%
TRST#	39 ohm +/- 5%
TCK	680 ohm +/- 5%
TDO	0±5ohm +/- 5%
ITP_EN	

Connect To	Resistor Placement
VTT	Within 2.0" of the ITP
GND	Within 2.0" of the ITP
VTT	Within 2.0" of the ITP
+3VVRUN	Close to CK410M Pin8

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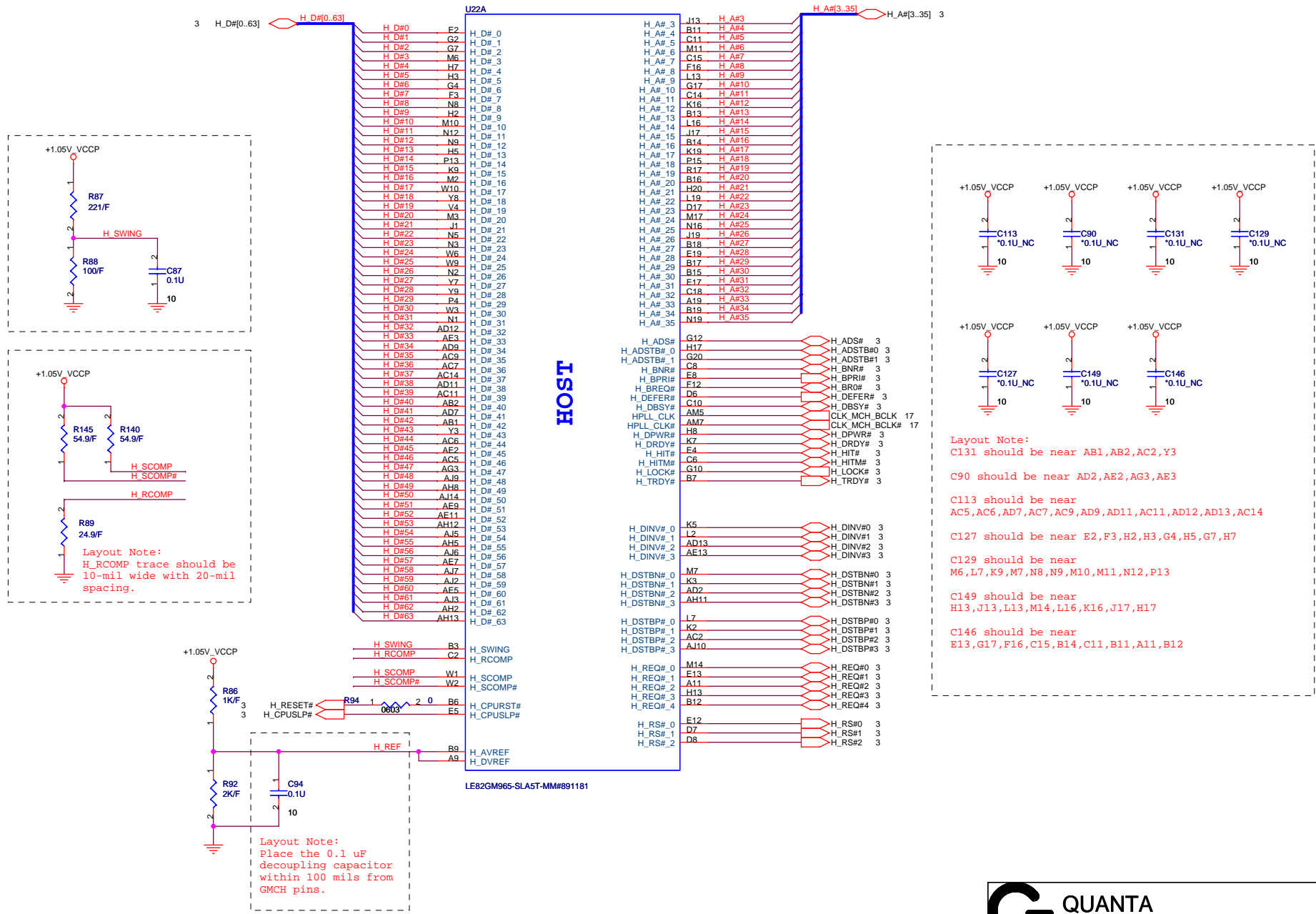
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Size: Document Number FM6B

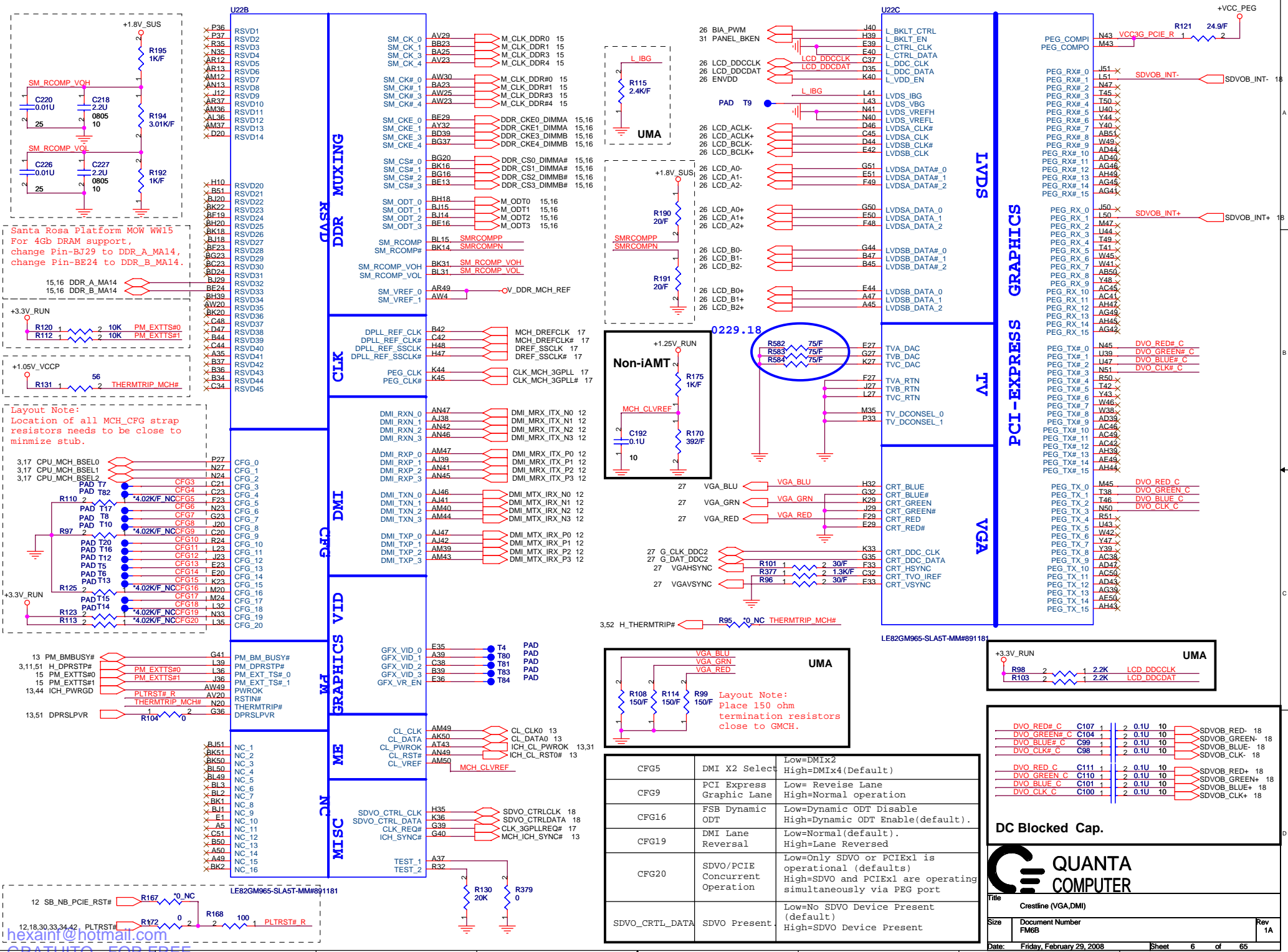
Date: Monday, February 25, 2008

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Title Crestline (HOST)		
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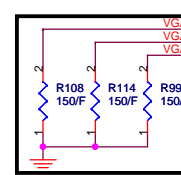
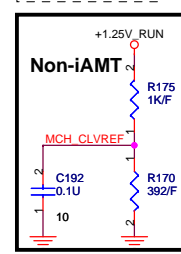


Santa Rosa Platform MOW WW15
For 4Gb DRAM support,
change Pin-BJ29 to DDR_A_MA14,
change Pin-BE24 to DDR_B_MA14.

Layout Note:
Location of all MCH_CFG strap
resistors needs to be close to
minimize stub.

13 PM_BMBUSY#
3,11,51 H_DPRSTP#
15 PM_EXTTSS#0
15 PM_EXTTSS#1
13,44 ICH_PWRGD
13,51 DPRSLPVR

12 SB_NB_PCIE_RST#
12,18,30,33,34,42 PLTRST#_R

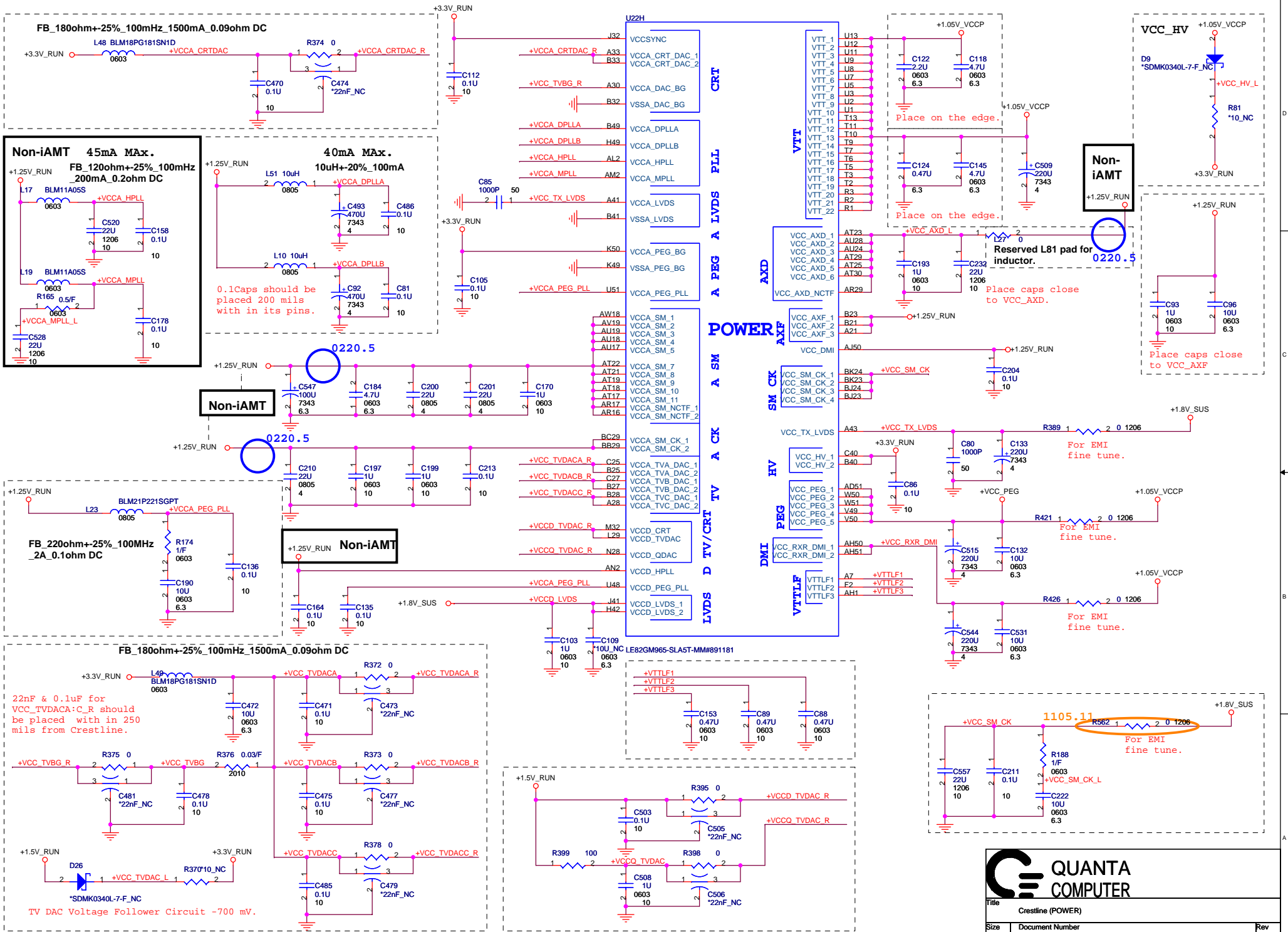


CFG5	DMI X2 Select	Low=DMIx2 High=DMIx4(Default)
CFG9	PCI Express Graphic Lane	Low= Reverse Lane High=Normal operation
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable(default).
CFG19	DMI Lane Reversal	Low=Normal(default). High=Lane Reversed
CFG20	SDVO/PCIE Concurrent Operation	Low=Only SDVO or PCIeI1 is operational (defaults) High=SDVO and PCIeI1 are operating simultaneously via PEG port
SDVO_CTRL_DATA	SDVO Present	Low=No SDVO Device Present (default) High=SDVO Device Present

DVO RED# C	C107	1	2	0.1U	10	SDVOB_RED-	18
DVO GREEN# C	C104	1	2	0.1U	10	SDVOB_GREEN-	18
DVO BLUE# C	C99	1	2	0.1U	10	SDVOB_BLUE-	18
DVO CLK# C	C98	1	2	0.1U	10	SDVOB_CLK-	18
DVO RED+ C	C111	1	2	0.1U	10	SDVOB_RED+	18
DVO GREEN+ C	C110	1	2	0.1U	10	SDVOB_GREEN+	18
DVO BLUE+ C	C101	1	2	0.1U	10	SDVOB_BLUE+	18
DVO CLK+ C	C100	1	2	0.1U	10	SDVOB_CLK+	18

DC Blocked Cap.



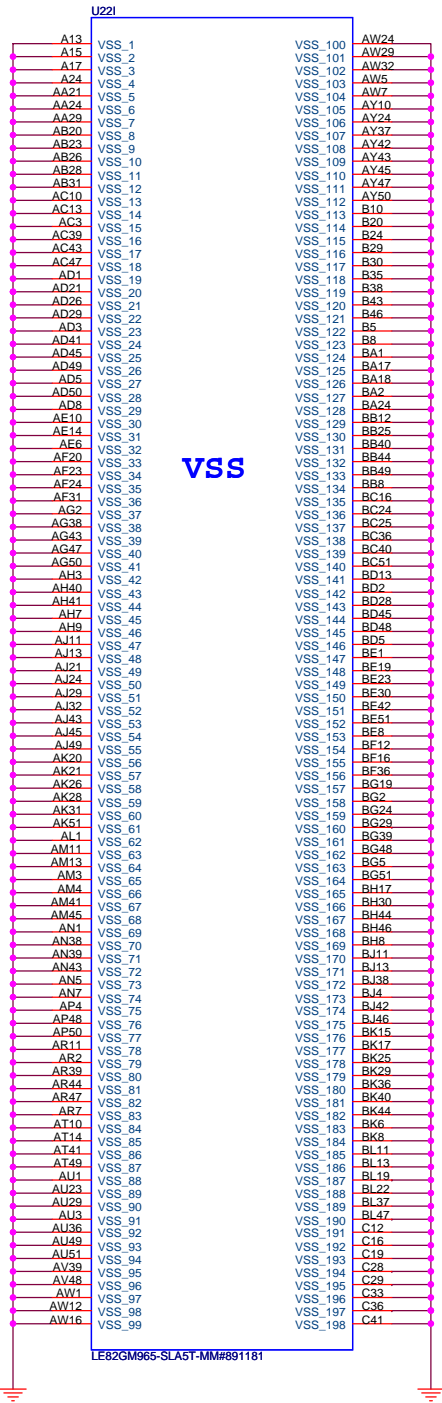


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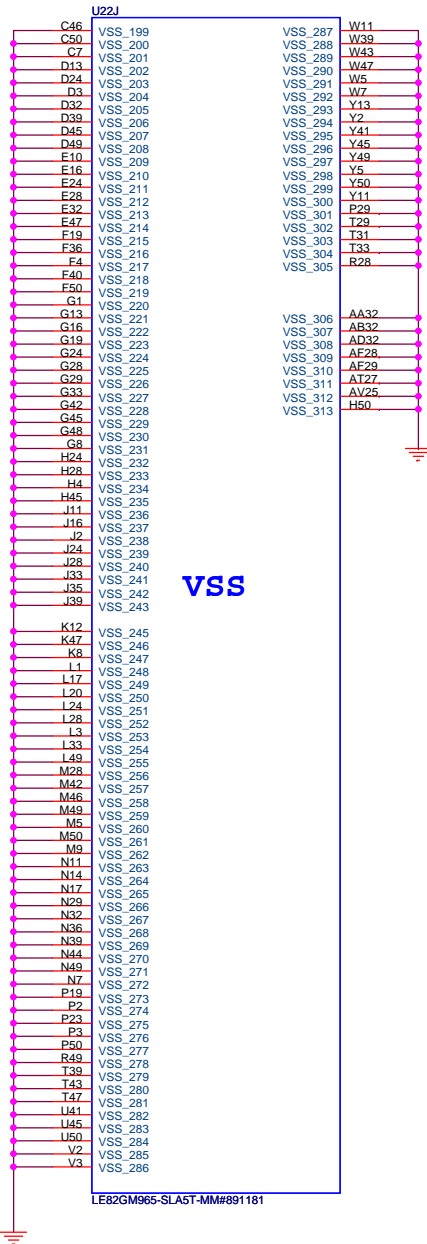
Title: Crestline (POWER)

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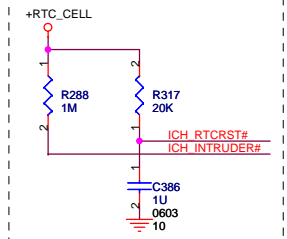
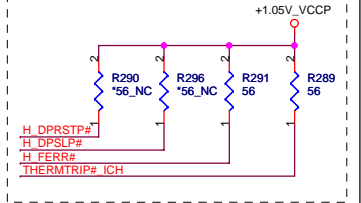
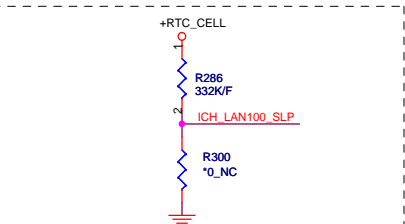
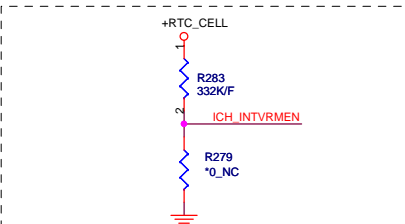
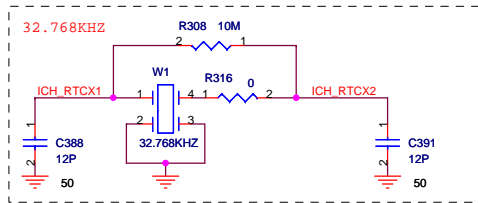
VSS



VSS



Title		
Crestline (VSS)		
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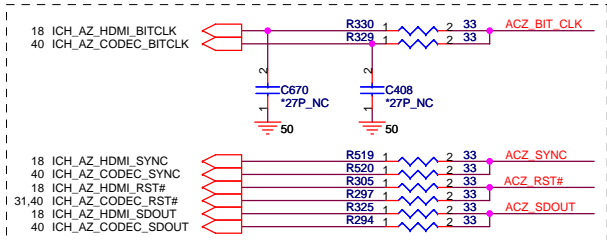
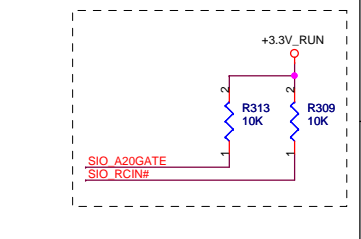


ICH8M Internal VR Enable Strap
(Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)

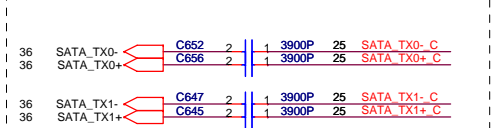
ICH_INTVRMEN	Low = Internal VR Disabled
	High = Internal VR Enabled(Default)

ICH8M LAN100 SLP Strap
(Internal VR for VccLAN1.05 and VccCL1.05)

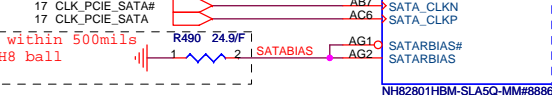
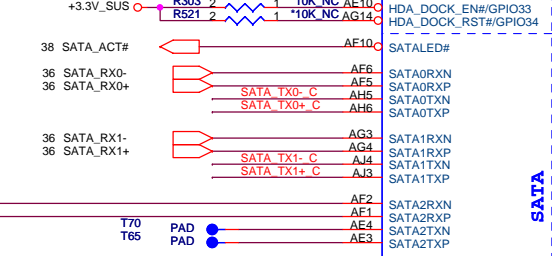
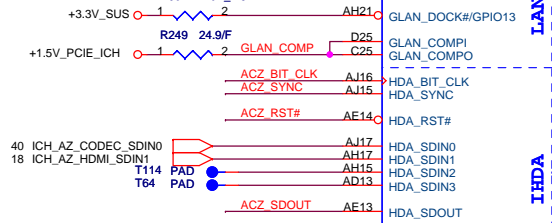
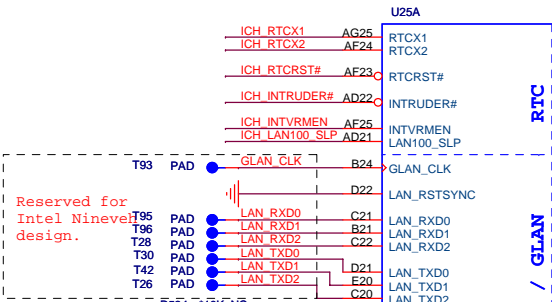
ICH_LAN100_SLP	Low = Internal VR Disabled
	High = Internal VR Enabled(Default)



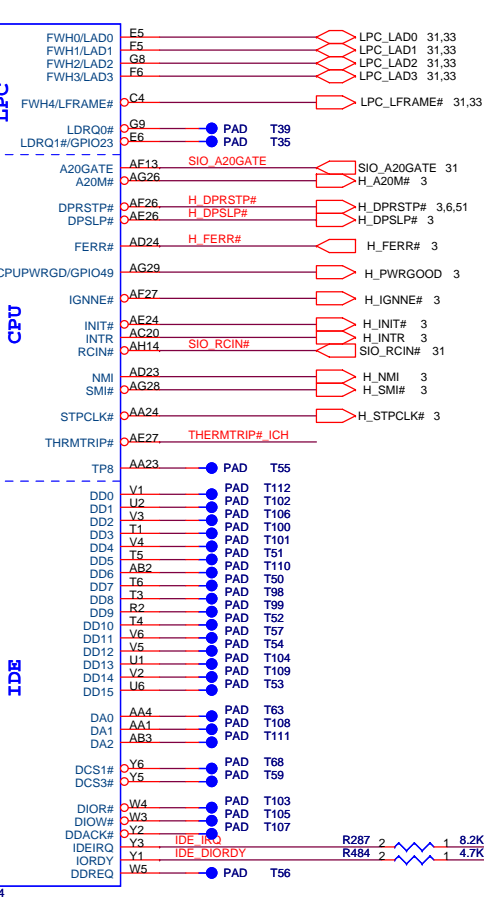
Place all series terms close to ICH8 except for SDIN input lines, which should be close to source. Placement of R330, R519, R305 & R325 should equal distance to the T split trace point as R329, R520, R297 & R294 respective. Basically, keep the same distance from T for all series termination resistors.



Distance between the ICH-8 M and cap on the "P" signal should be identical distance between the ICH-8 M and cap on the "N" signal for same pair.



Place within 500mills of ICH8 ball

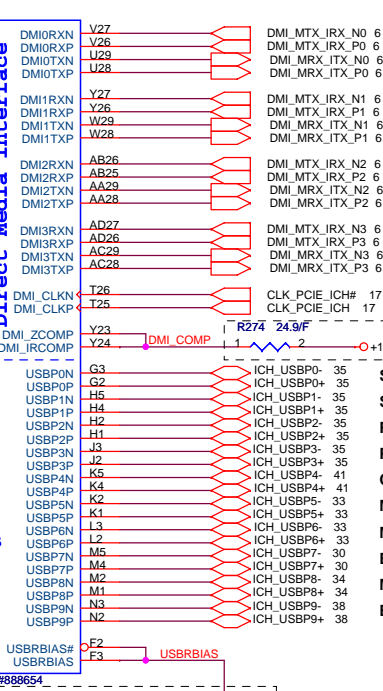
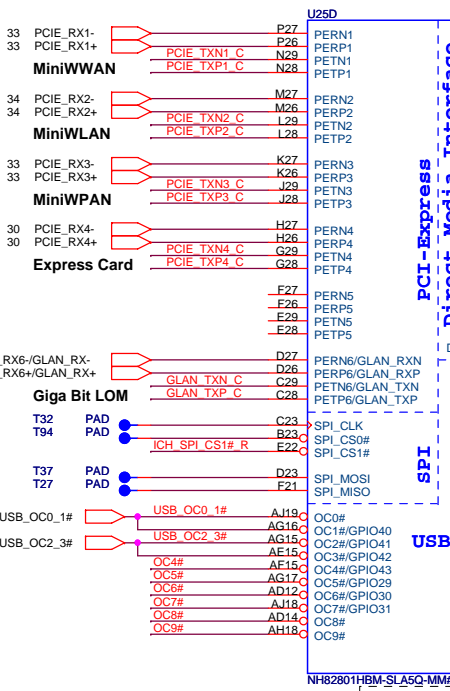
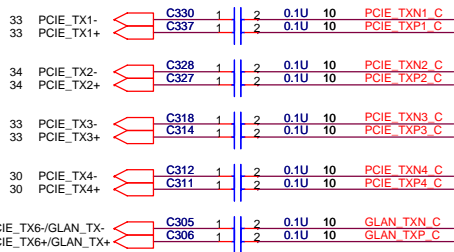


XOR Chain Entrance Strap

ICH_RSVD	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1

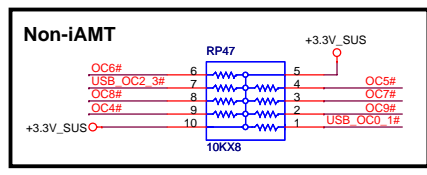
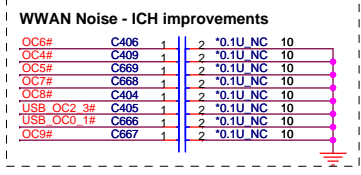
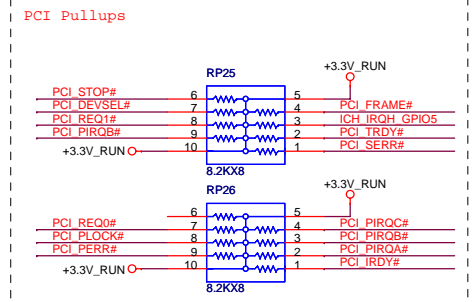
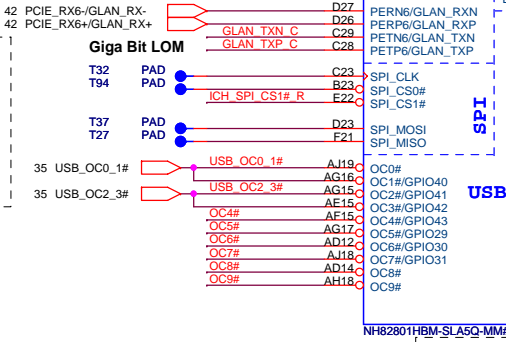
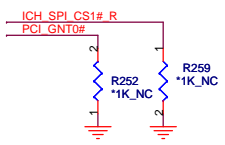


Place TX DC blocking caps close ICH8.

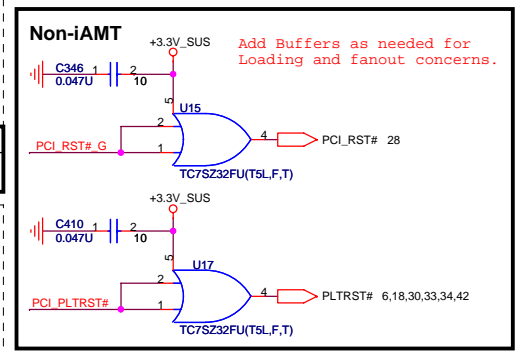
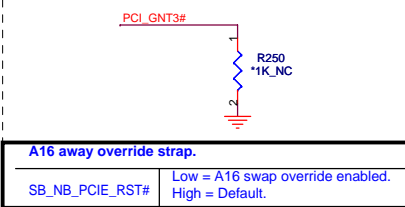
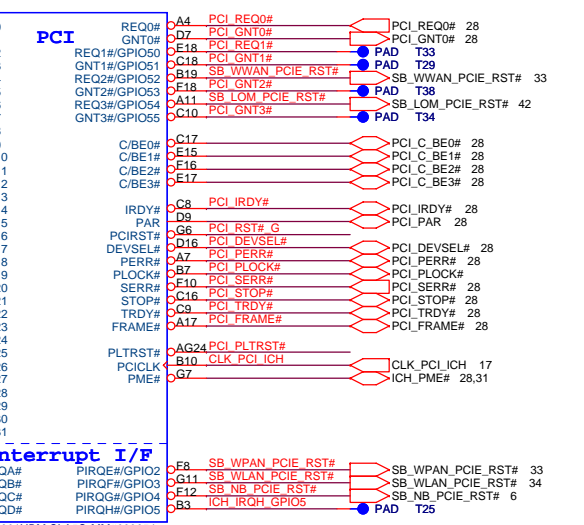
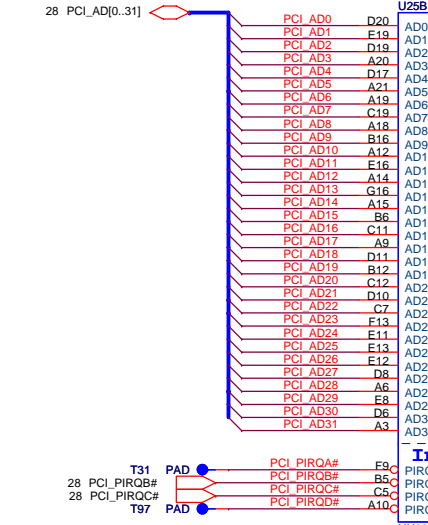


- Side pair Top / left
- Side pair bottom / right
- Pair 1 top / left
- Pair 1 bottom / right
- Camera
- Mini Card (WWAN)
- Mini Card (WPAN)
- Express Card
- Mini Card (WLAN)
- Biometric

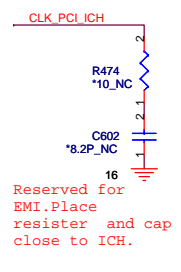
Boot BIOS Strap			
	LPC	GNT0#	SPI_CS1#
ICH_SPI_CS1# R	11	No stuff	No stuff
PCI_GNT0#	10	No stuff	Stuff
SPI	01	Stuff	No stuff



Short F2 and F3 at the package and keep length to less than 500mils. Trace Impedance should be 60ohms +/- 15%.



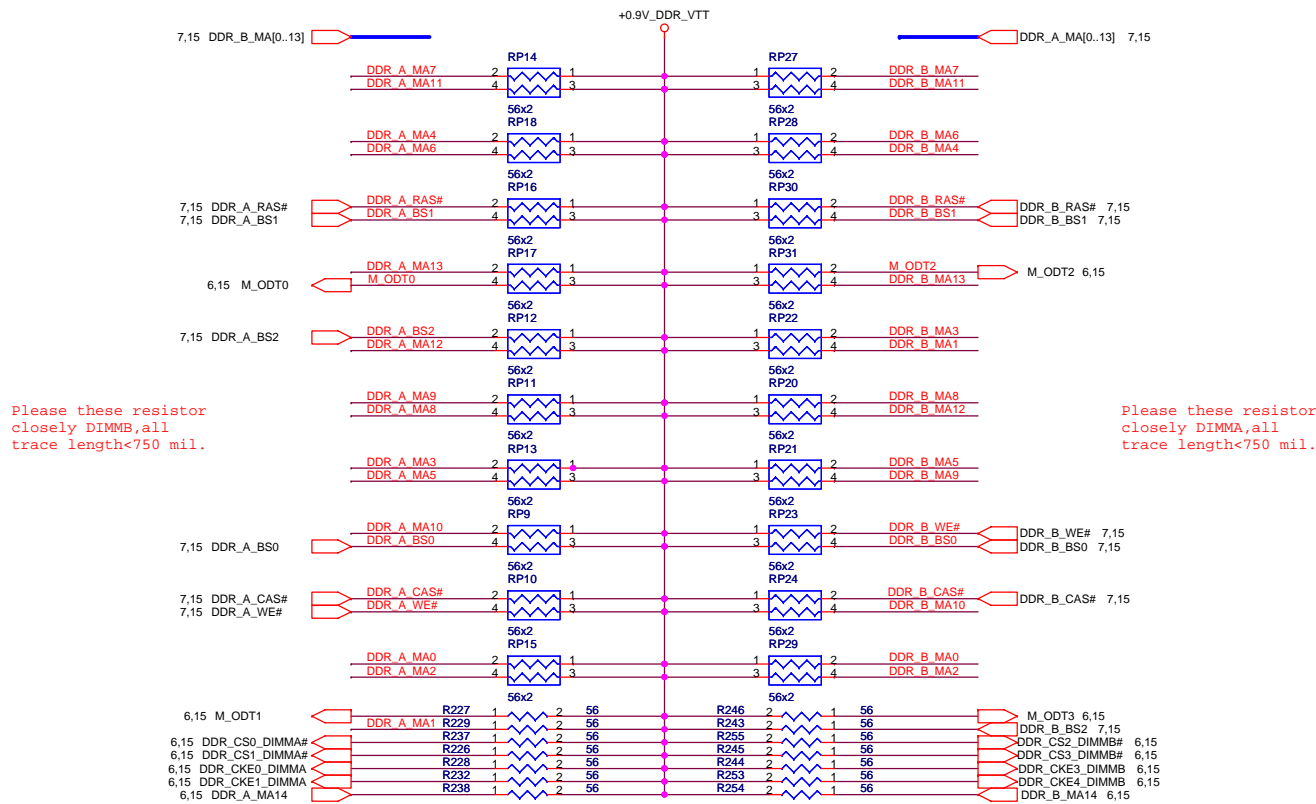
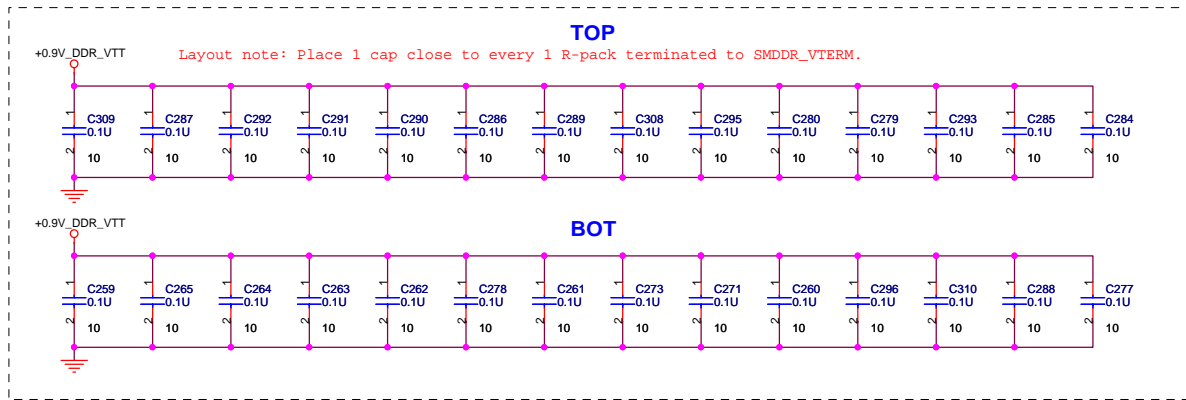
BIOS should not enable the internal GPIO pull up resistor.



Reserved for EMI. Place resistor and cap close to ICH.

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Title: ICH8-M (USB,DMI,PCIE,PCI)
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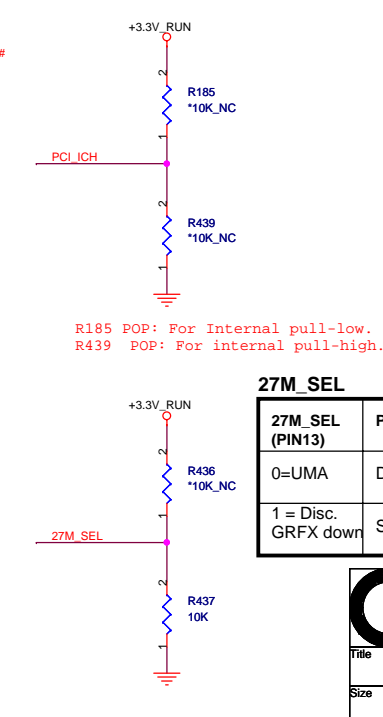
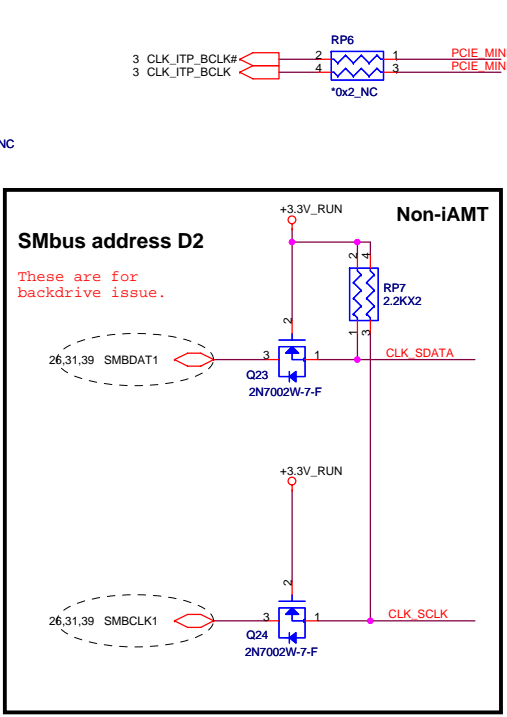
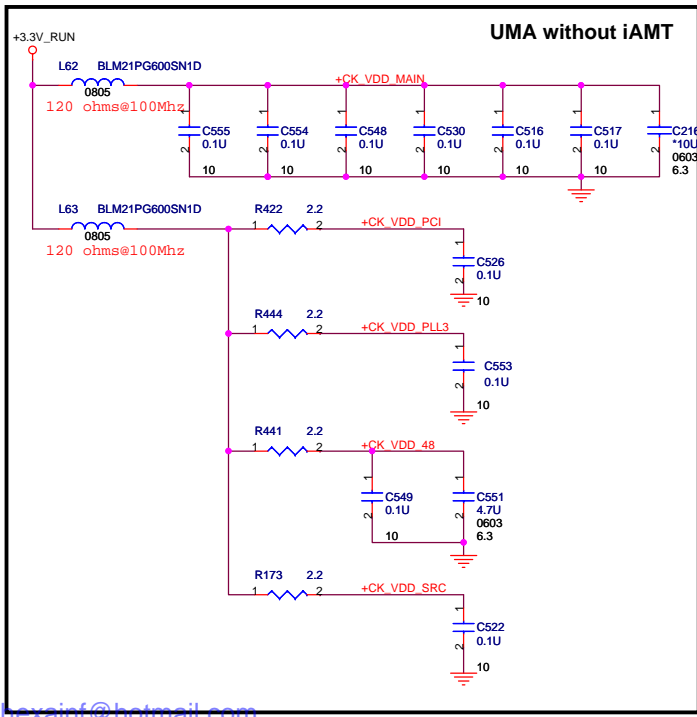
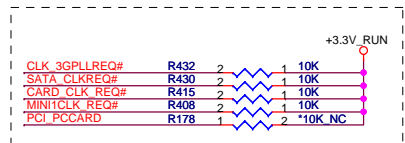
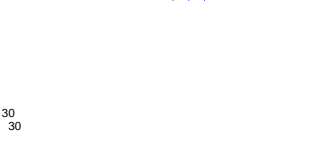
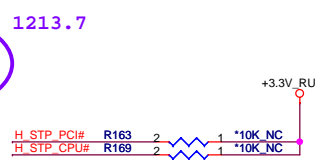
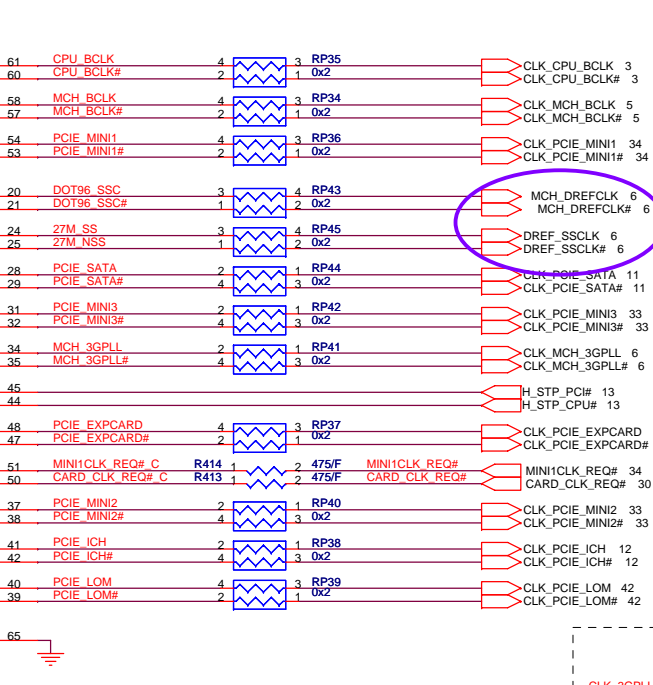
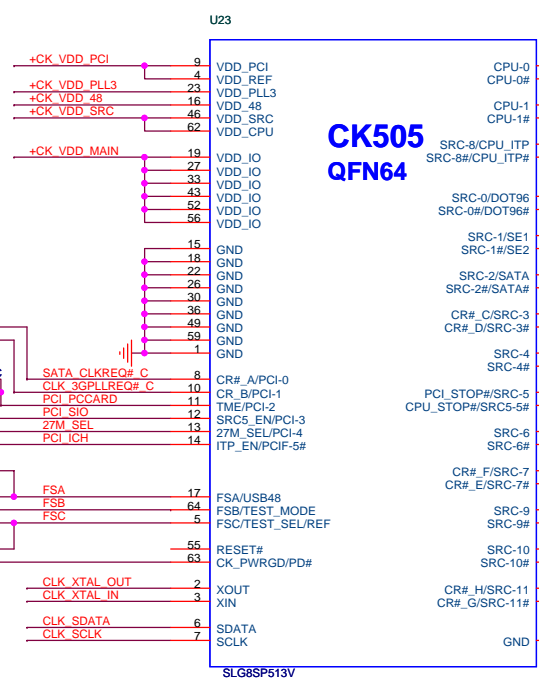
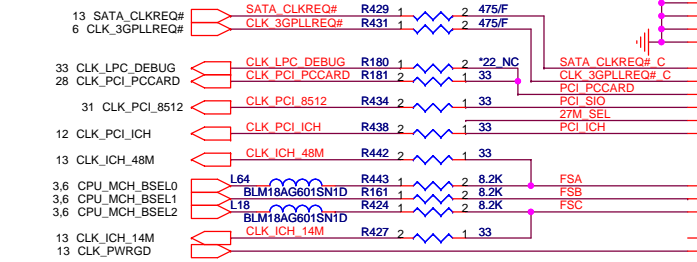
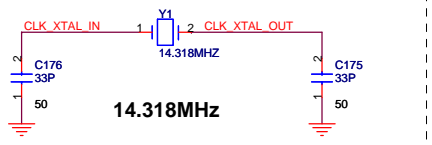
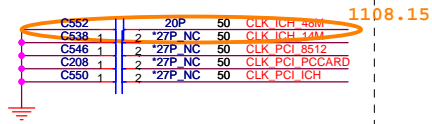
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Title: **DDR2 RES ARRAY**

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Add capacitor pads for improving WWAN.




FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33


27M_SEL (PIN13)	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	96/100M_T	96/100M_C
1 = Disc. GRFX down	SRCT0	SRCC0	27Mout	27MSSout




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Title		
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Title: FLASH, RTC & KC		
Size: FM6B	Document Number: FM6B	Rev: 1A
Date: Friday, February 22, 2008	Sheet: 23	of 65

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4

5

A

A

B

B


C

C

D

D

hexainf@hotmail.com
GRATUITO - FOR FREE


 QUANTA COMPUTER		
Title		
Battery Selector		
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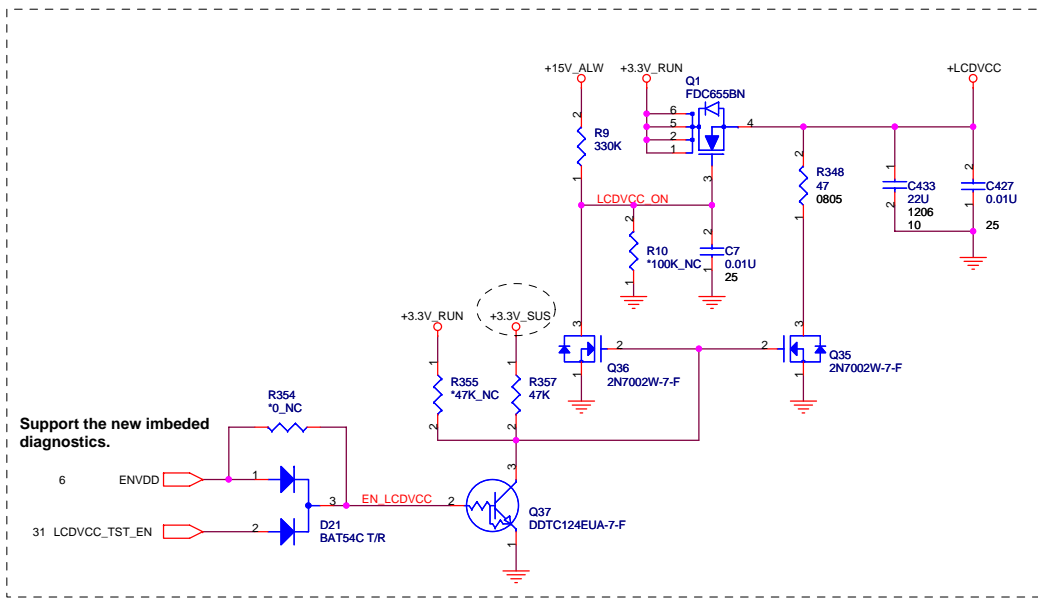
2

3

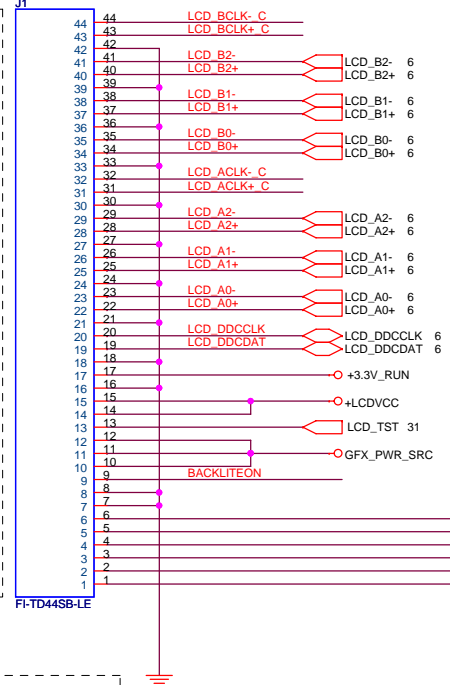
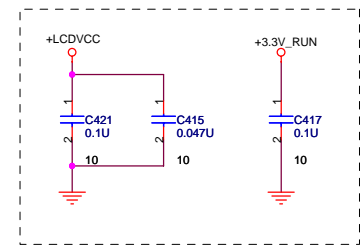
4

5

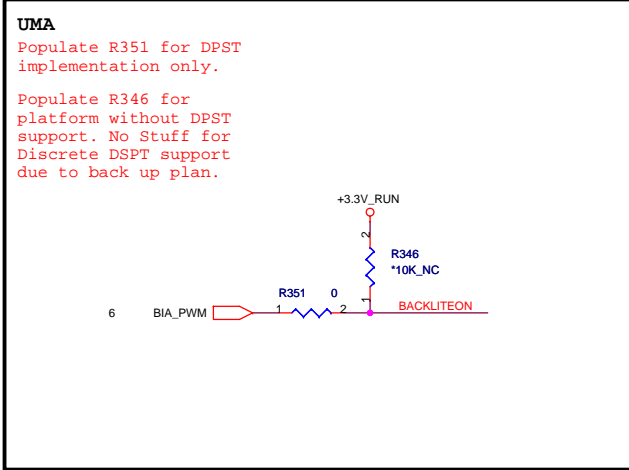
 QUANTA COMPUTER		
Title: Docking Station CONN.		
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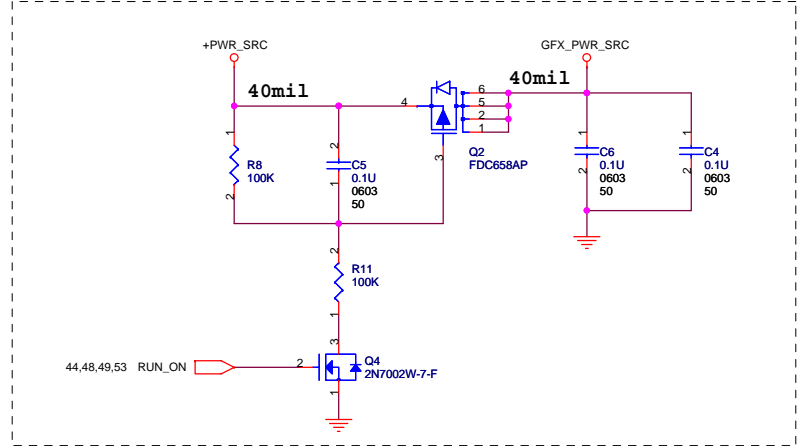
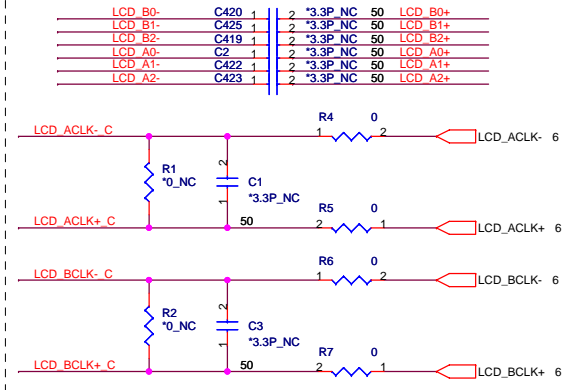
Support the new imbedded diagnostics.



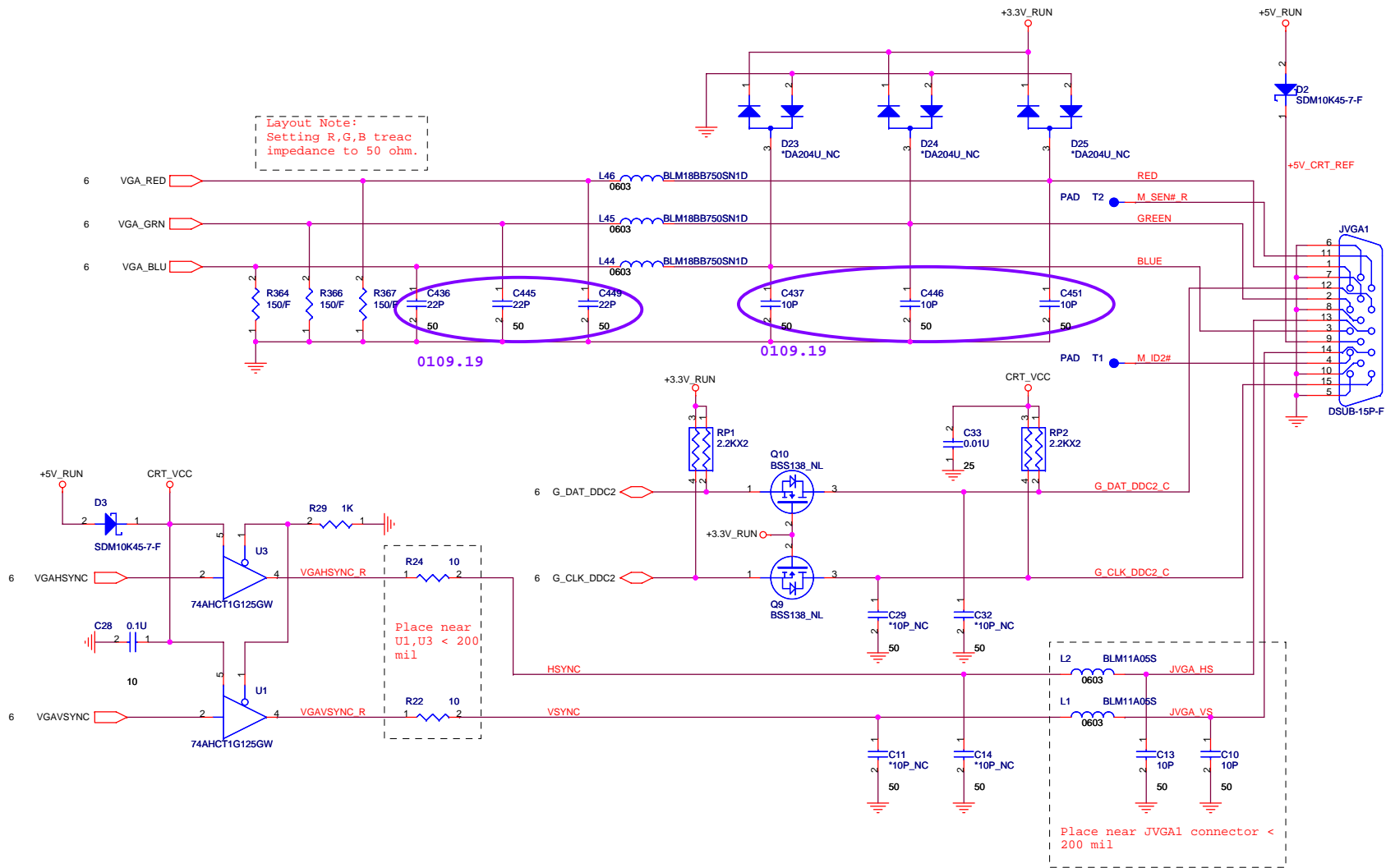
Address : A9H --Contrast
AAH --Backlight



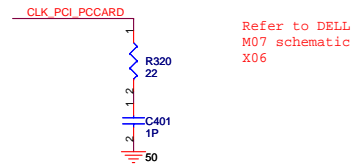
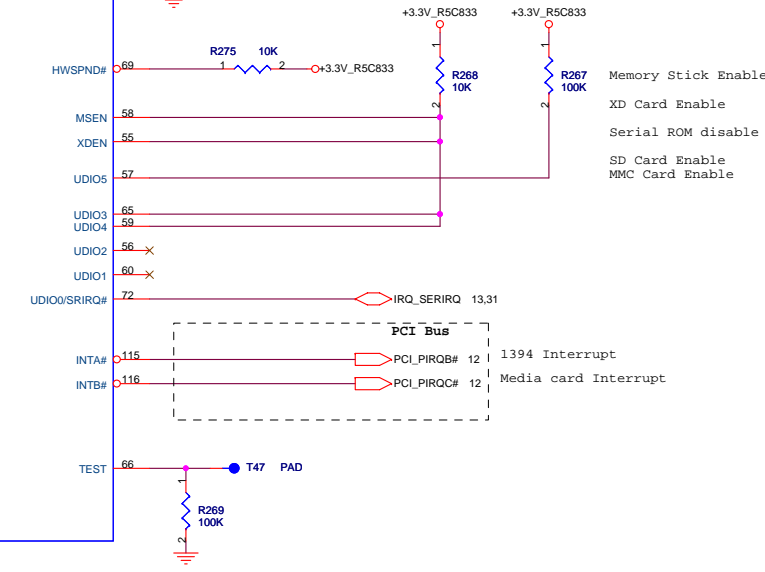
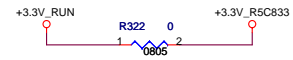
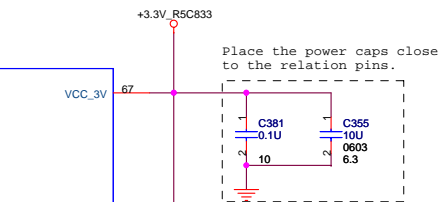
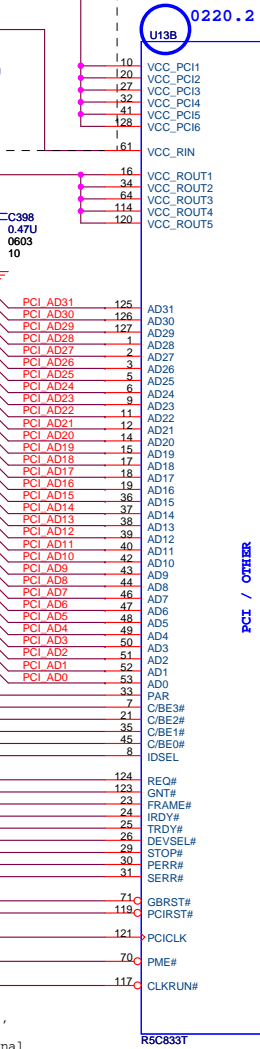
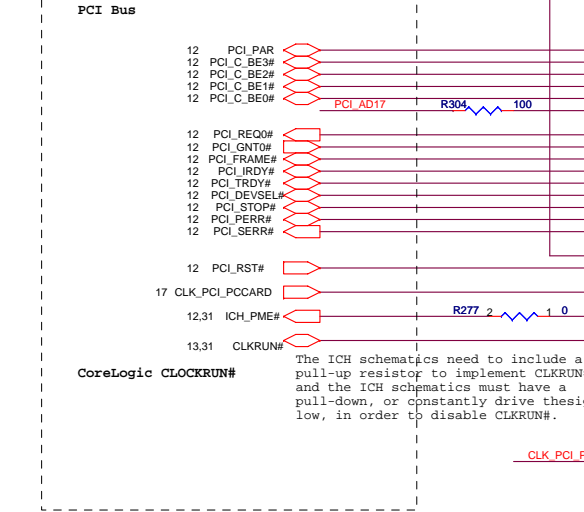
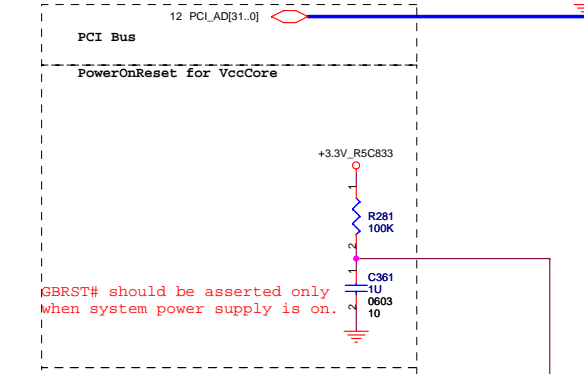
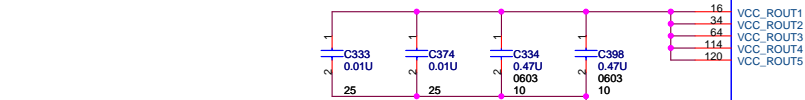
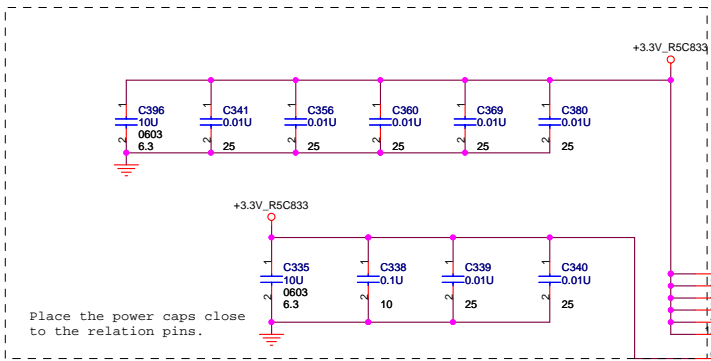
Shunt capacitors on LVDS for improving WWAN.



Title		LCD CONN & CK-SSCD
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Title		CRT&TV CONN
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0220.2

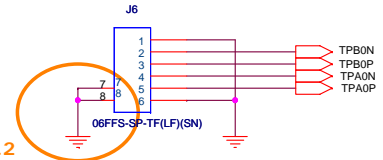
AVCC_PHY1
AVCC_PHY2
AVCC_PHY3
AVCC_PHY4

Place these caps as close to the R5C833 as possible.

AS CLOSE AS POSSIBLE TO R5C833

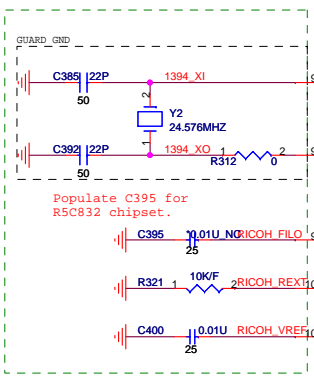
Circuit area : As small as possible.

1029.2



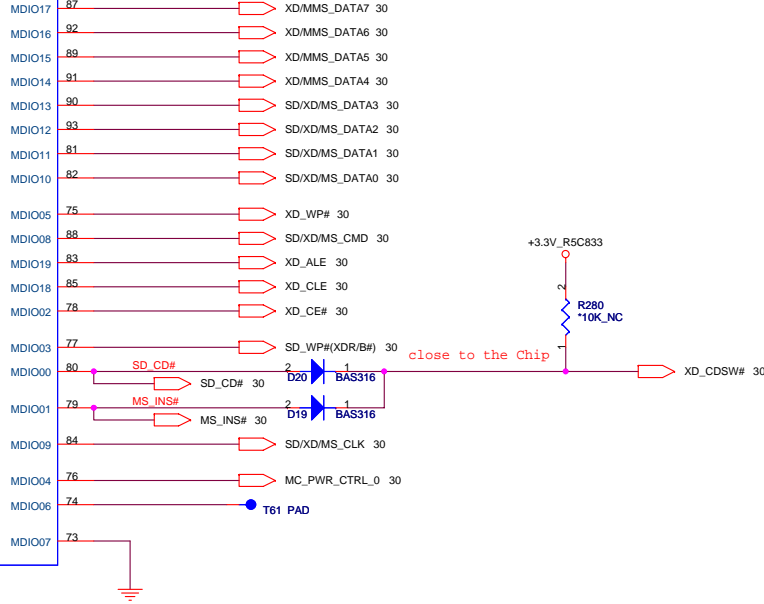
TPBON
TPBOP
TPAON
TPAOP

- *TPAOP/TPAON, TPBOP/TPBON pair trace : As close as possible.
- *TPAOP/TPAON, TPBOP/TPBON pair trace : Same length electrically.
- *Termination resistor for TPA+/- TPB+/- : As close as possible to its cable driver (device pin out).



Populate C395 for R5C833 chipset.

Place these caps as close to the U26 as possible.



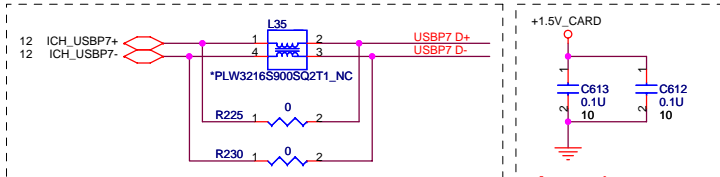
QUANTA COMPUTER

Title: IEEE 1394

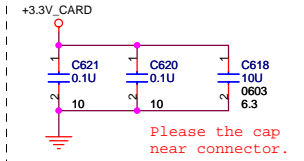
Size: Document Number FM6B Rev 1A

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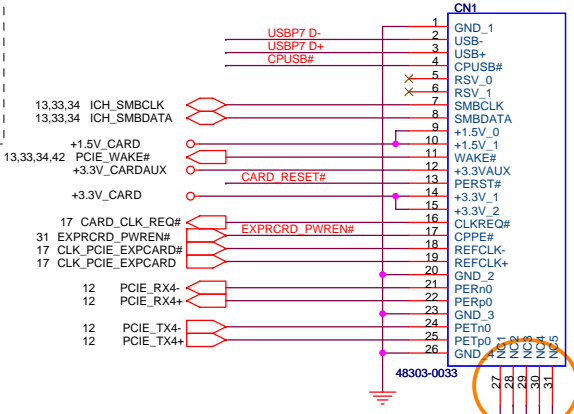
Express Card



Please the cap near connector.



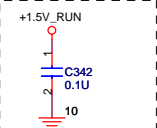
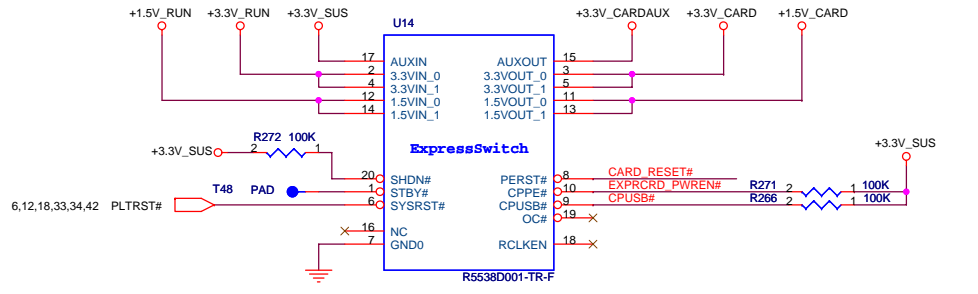
Please the cap near connector.



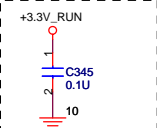
JAE PX10FS16PH-26P

PCI-Express TX and RX direct to connector.

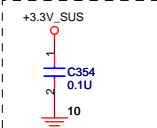
+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.



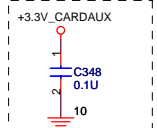
Please the cap near pin 12 & 14 (1.5VIN).



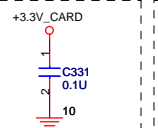
Please the cap near pin 2 & 4 (3.3VIN).



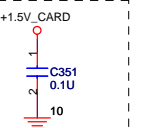
Please the cap near pin 17 (AUXIN).



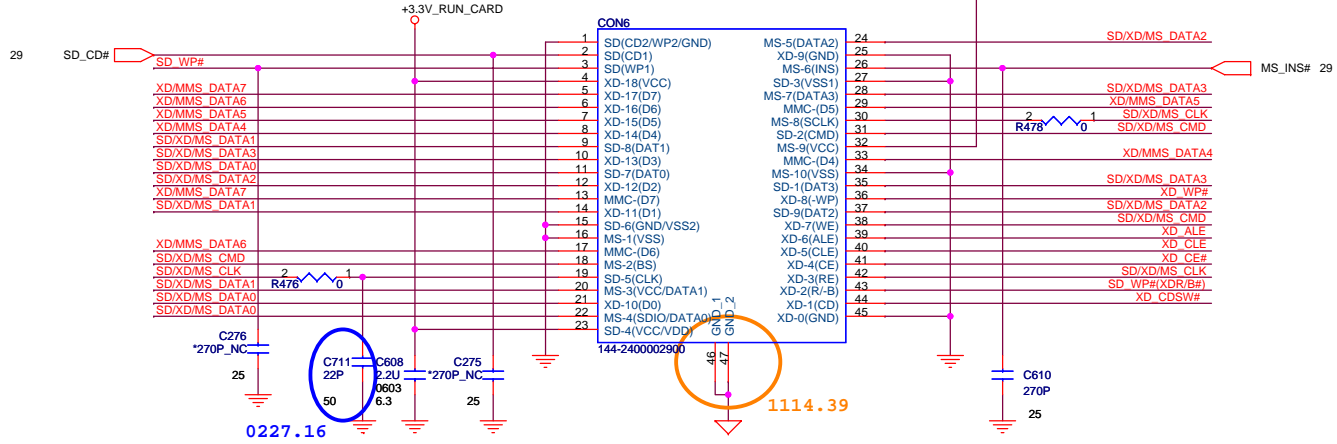
Please the cap near pin 15 (AUXOUT).



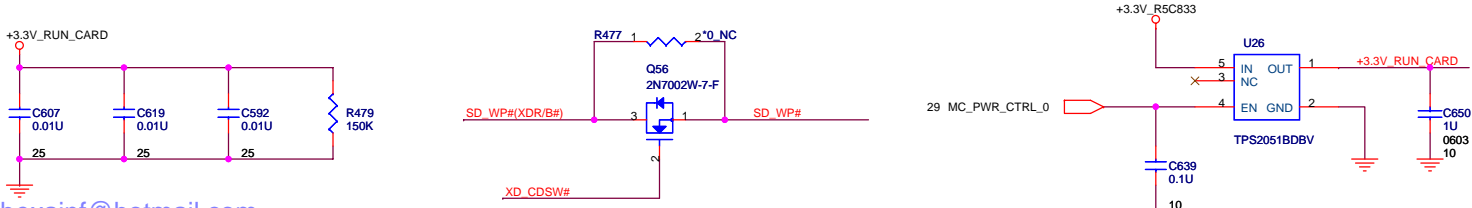
Please the cap near pin 3 & 5 (3.3VOUT).



Please the cap near pin 11 & 13 (1.5VOUT).



8 IN1 CARD READER



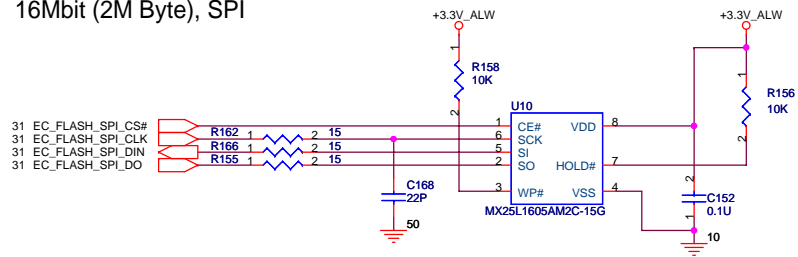
**QUANTA
COMPUTER**

Title: ExpressCard/SmartCard

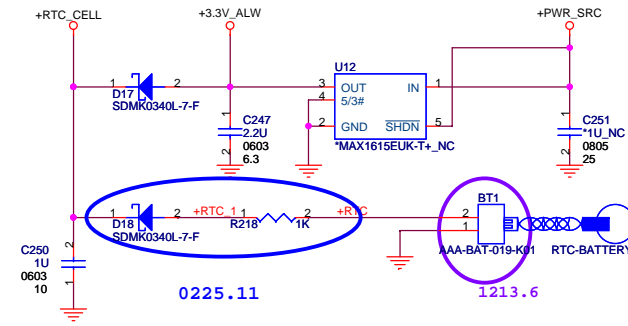
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16Mbit (2M Byte), SPI

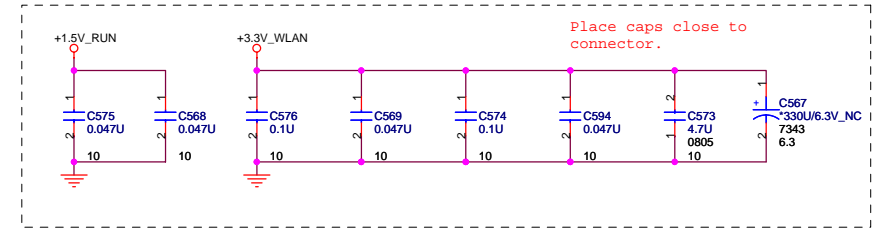
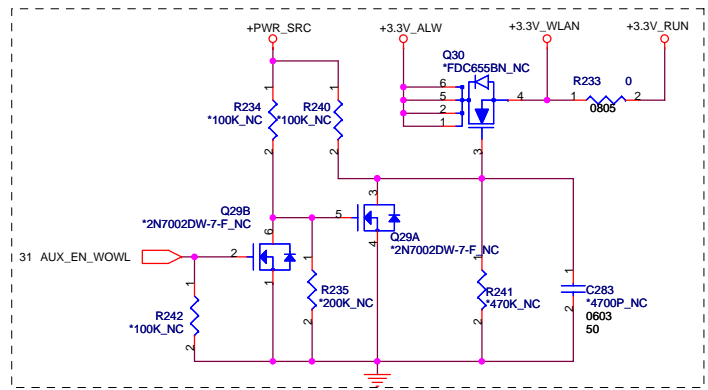
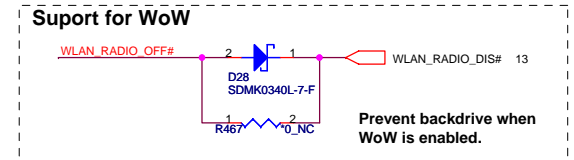
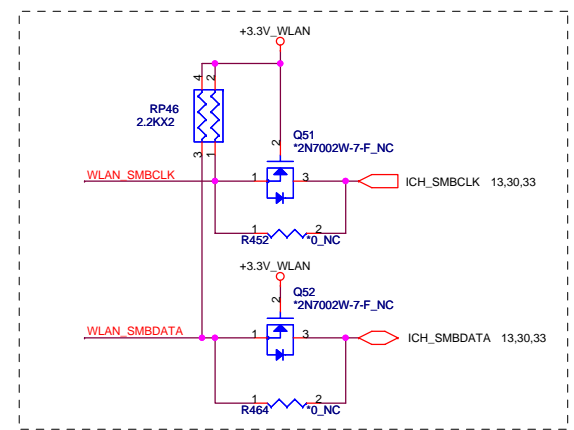
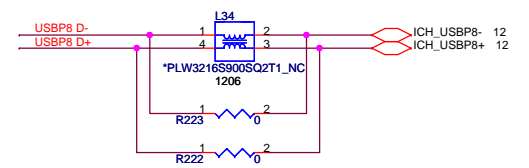
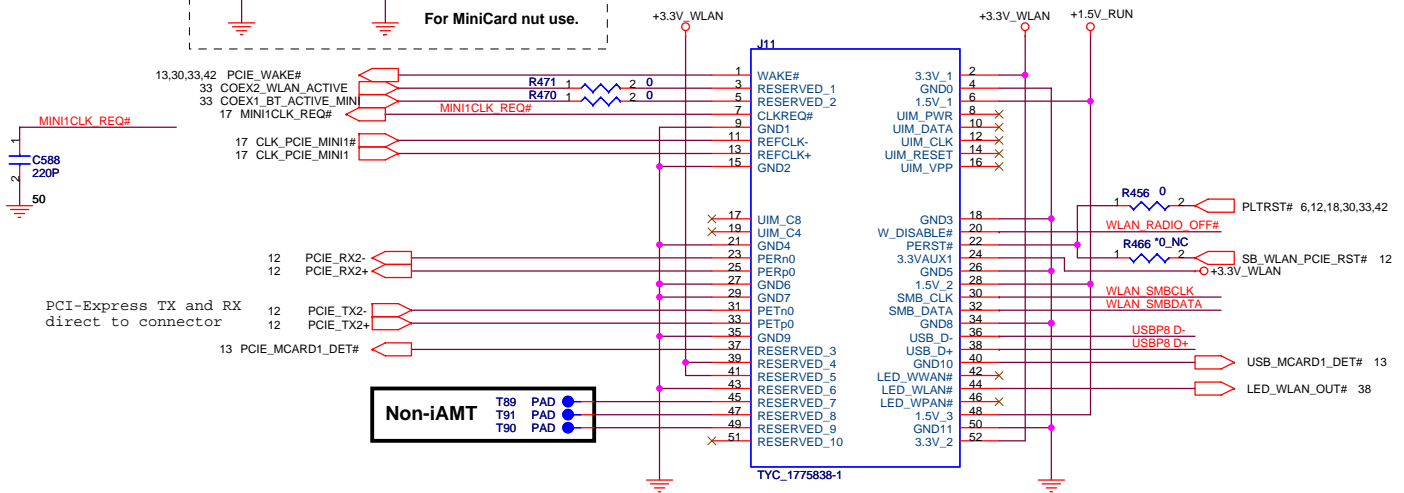
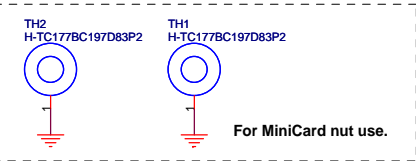


RTC BATTERY

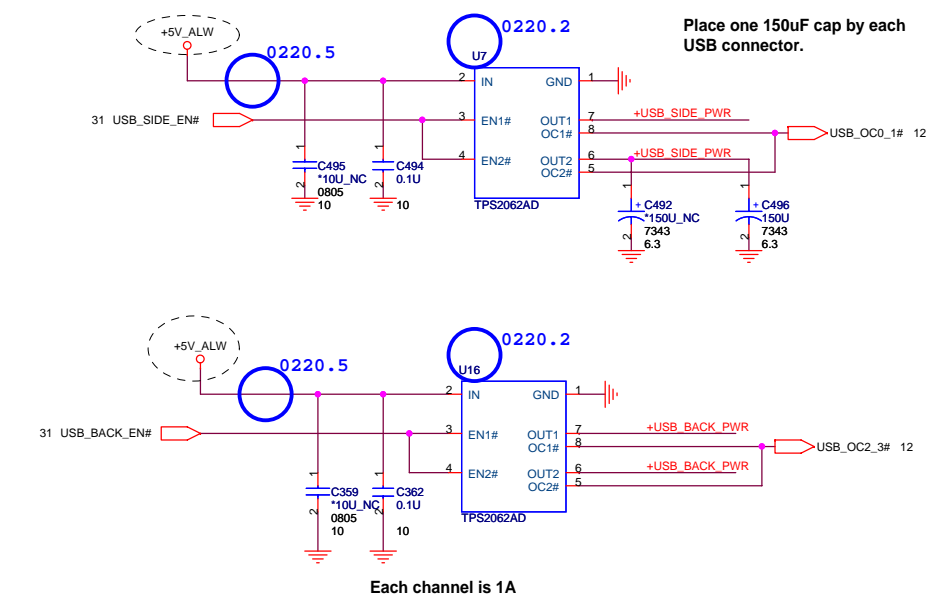
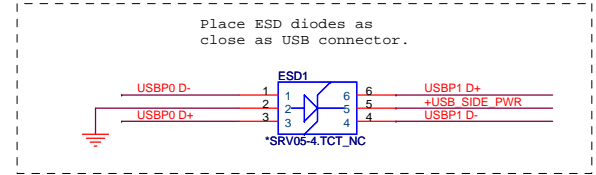
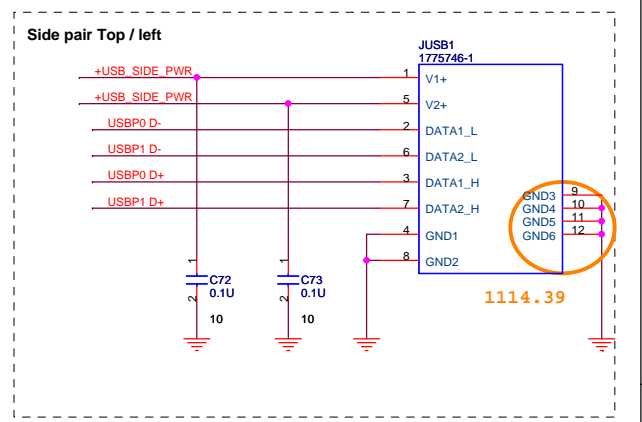
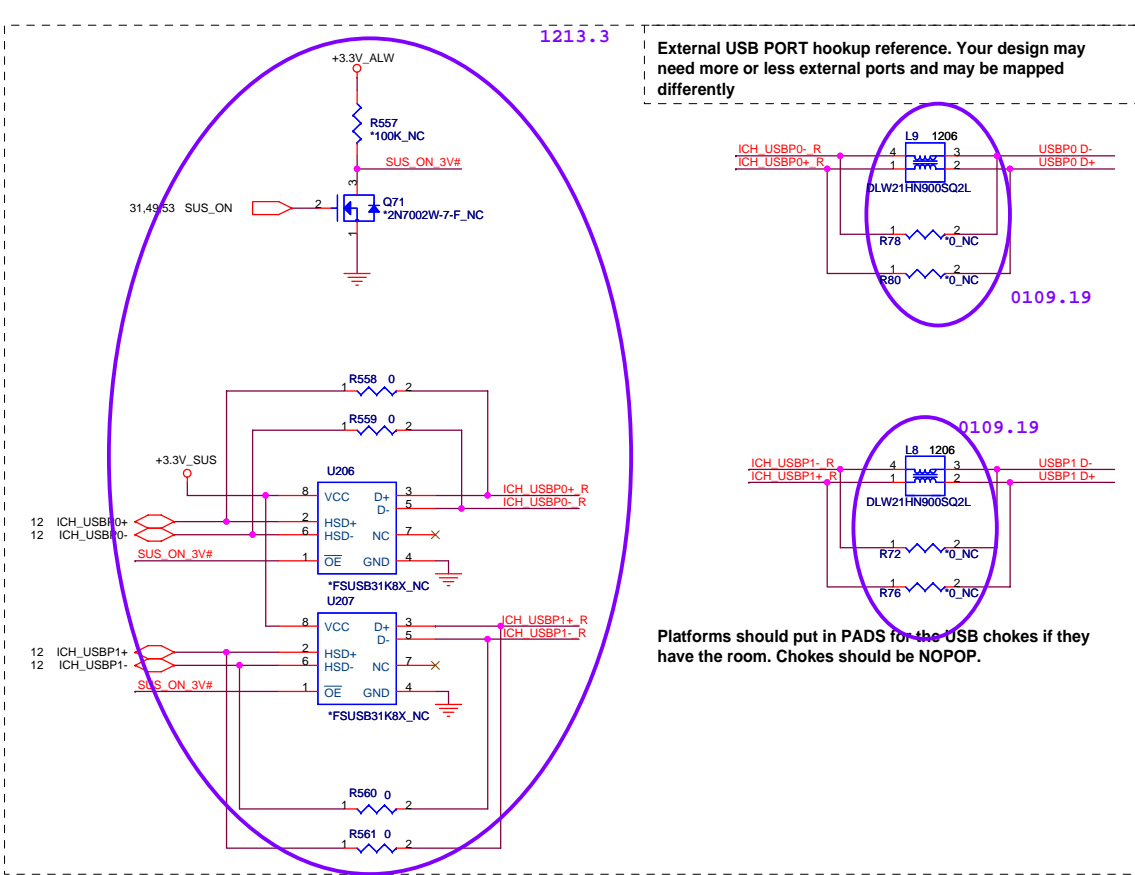


Title		
Ultra I/O Controller ECE5028		
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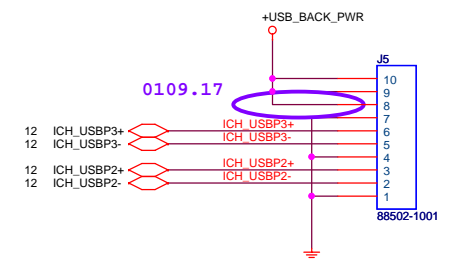
MiniCard WLAN connector



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MB side

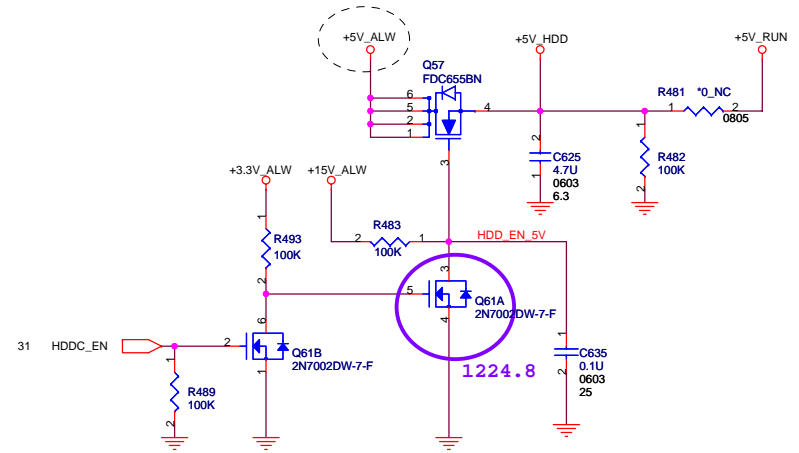
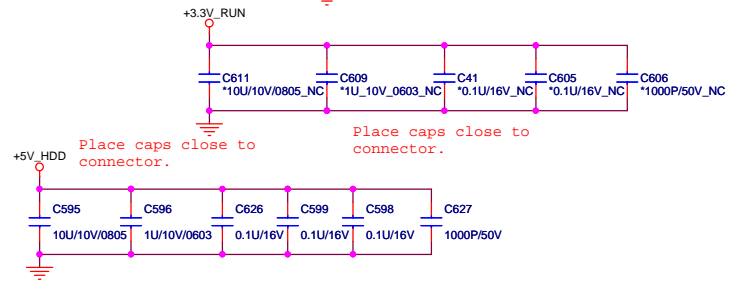
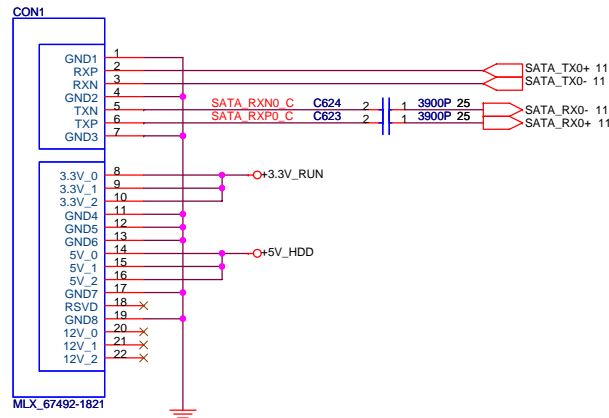


QUANTA COMPUTER

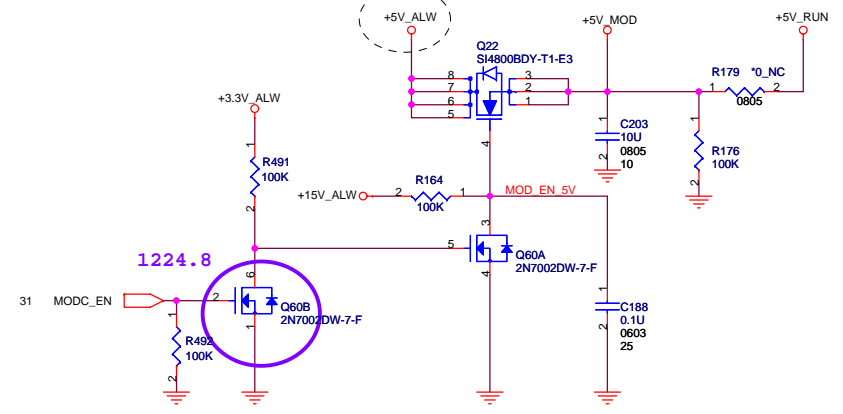
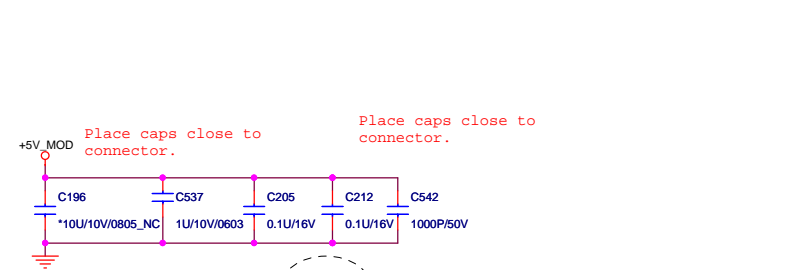
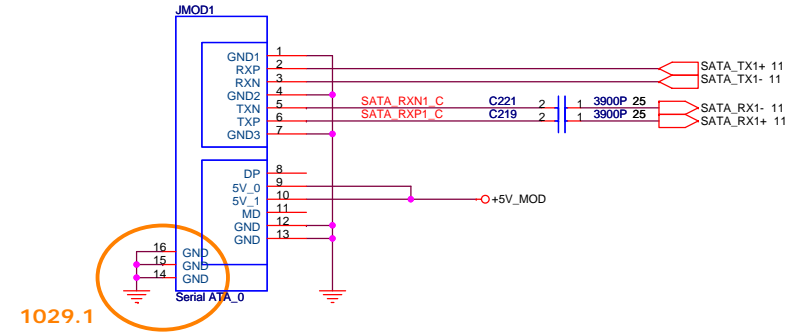
Title SERIAL PORT & USB

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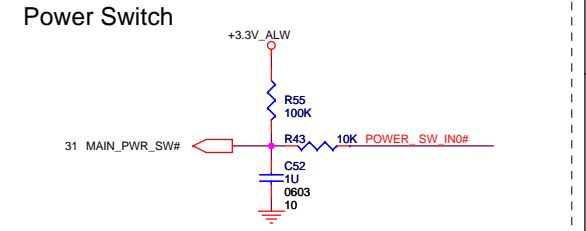
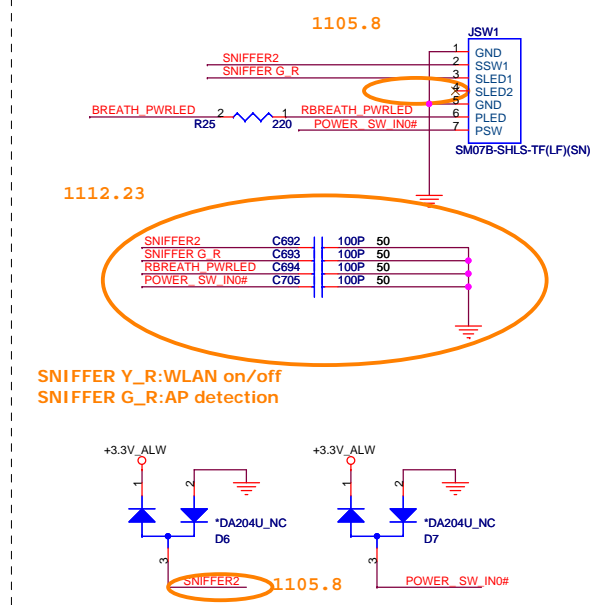
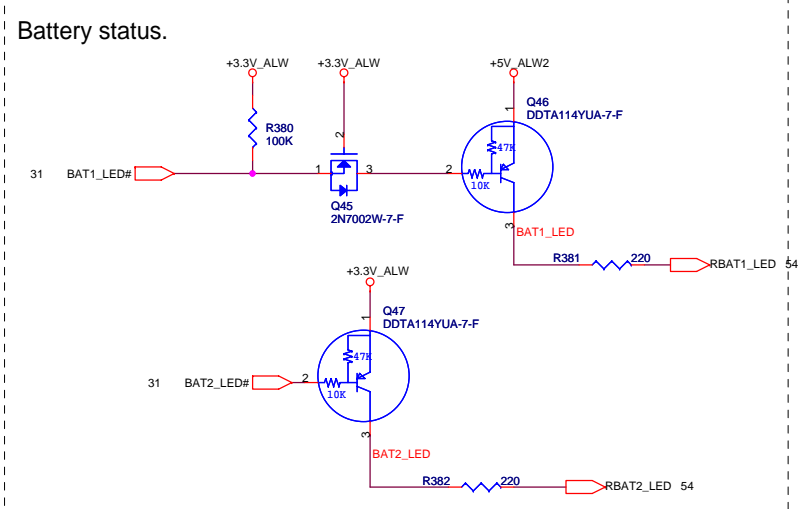
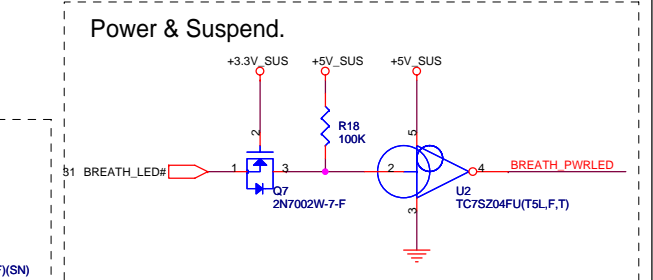
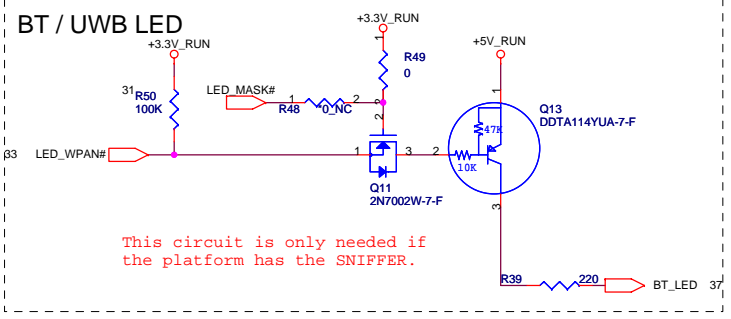
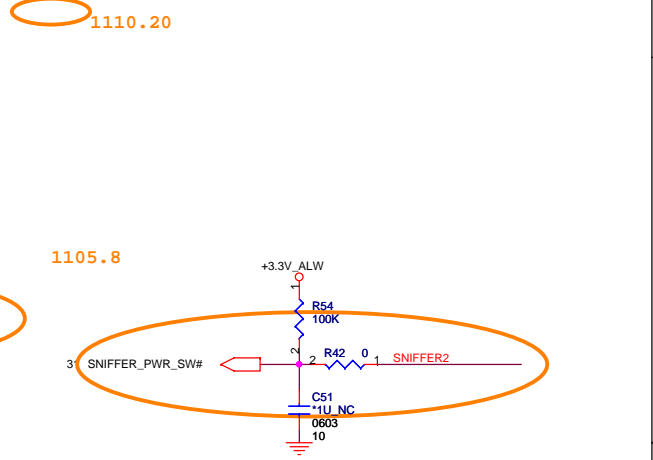
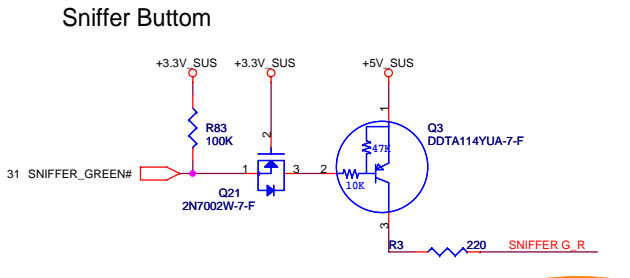
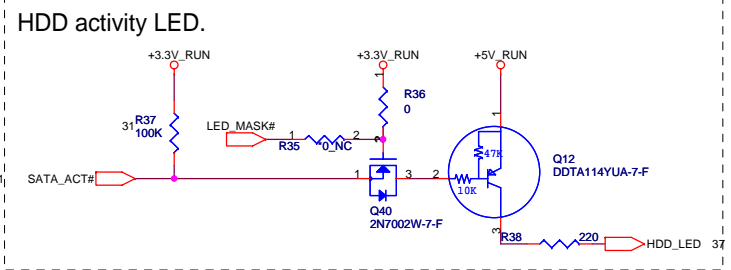
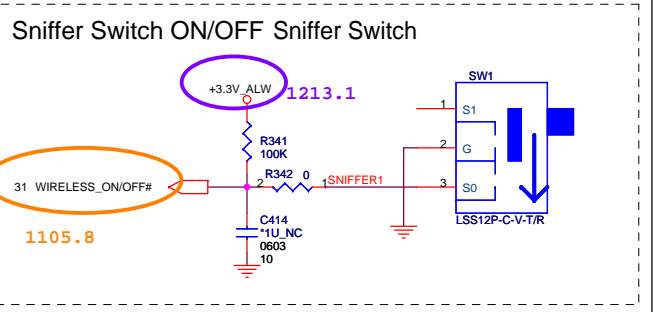
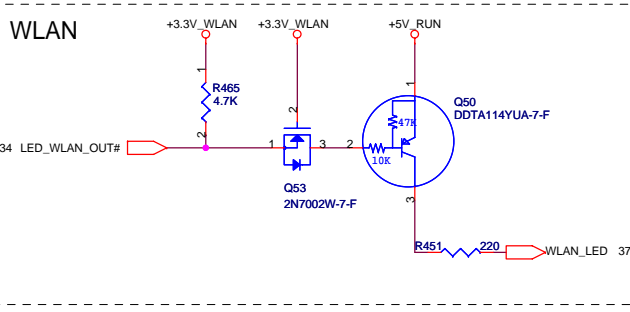
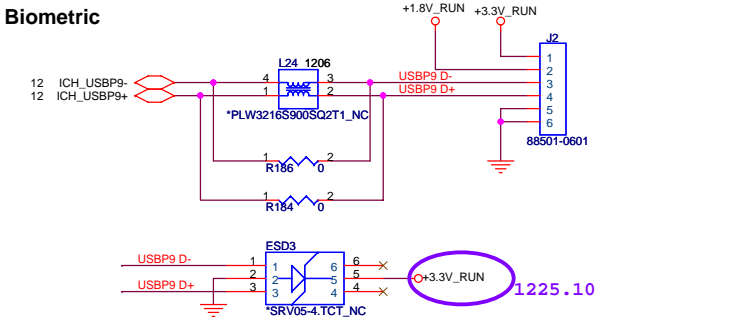
SATA Connector.



ODD Connector



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SATA (HDD&CD_ROM)		
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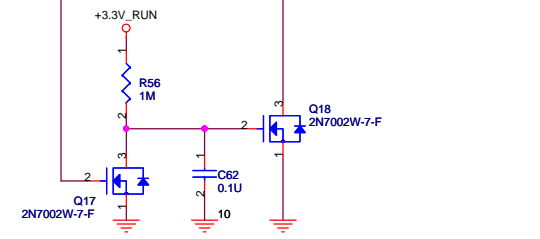
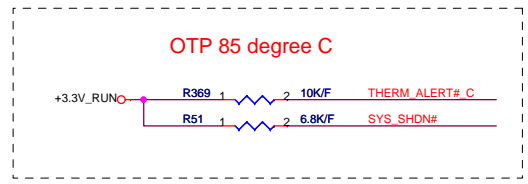
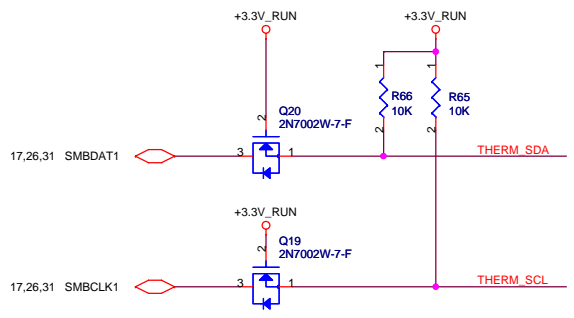
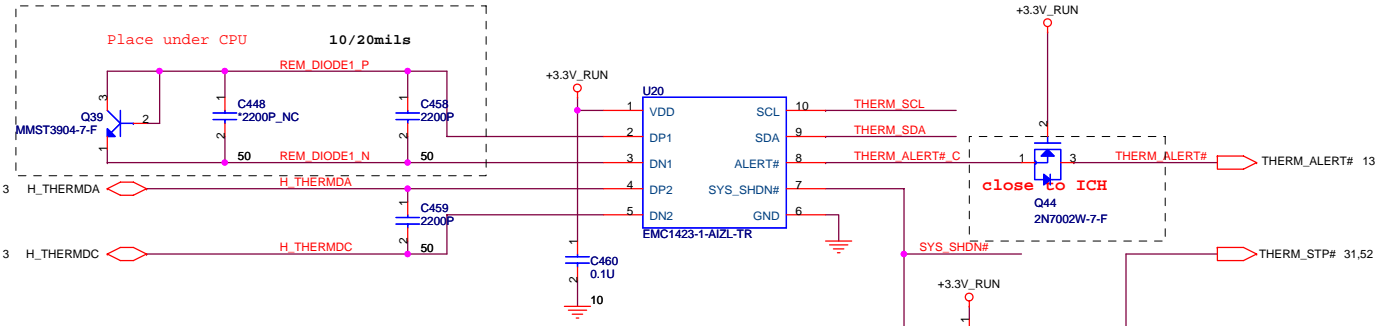
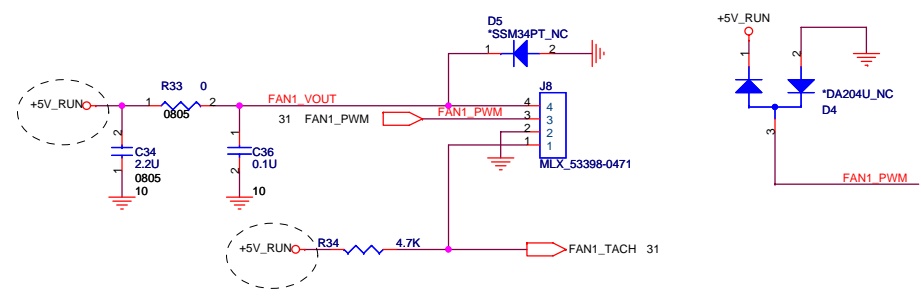
Title: SWITCH, KEYBOARD & LED

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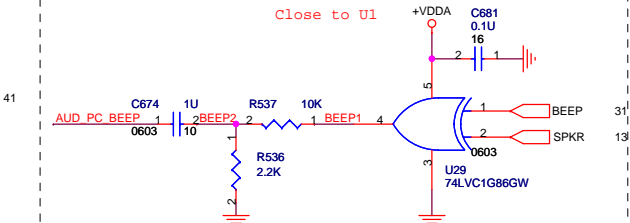
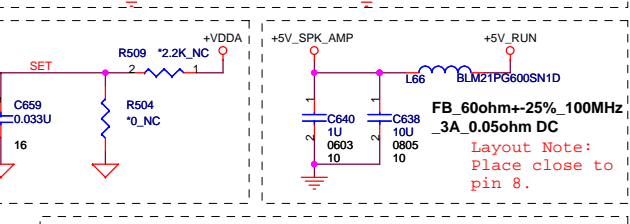
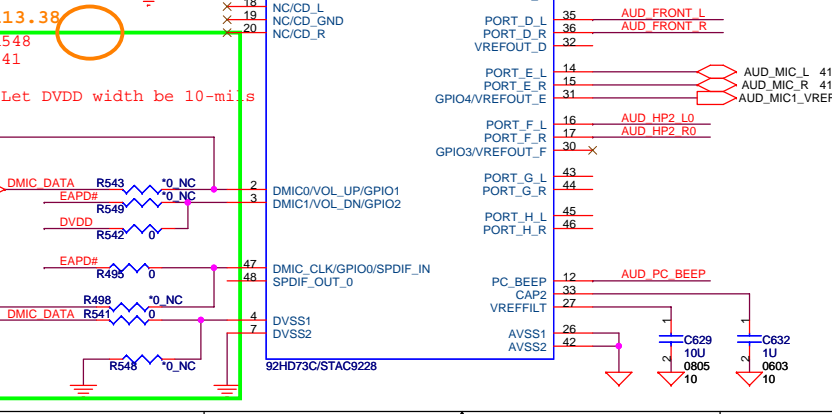
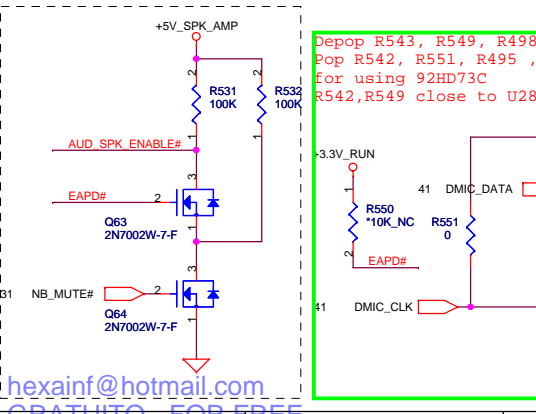
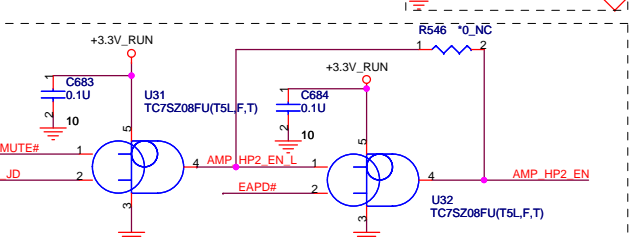
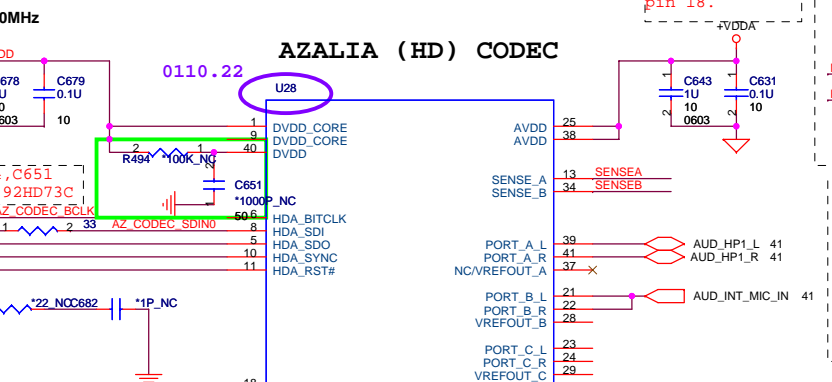
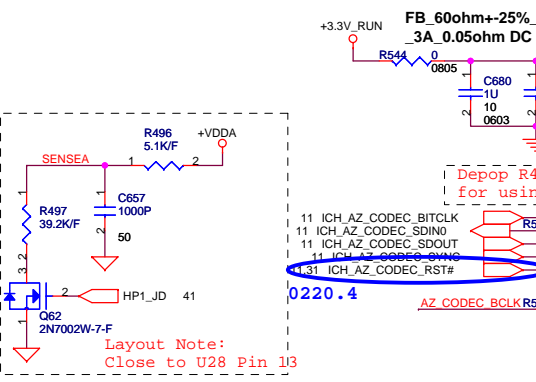
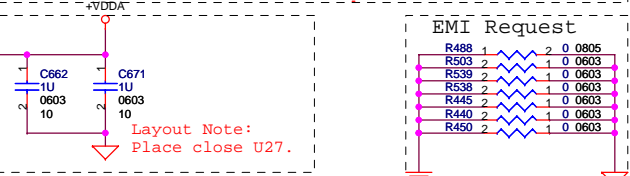
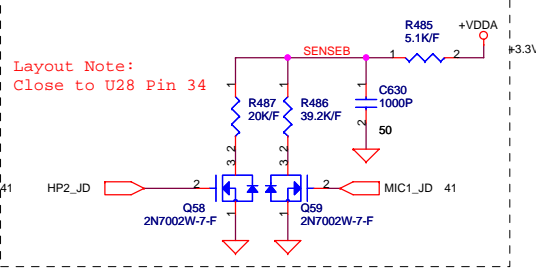
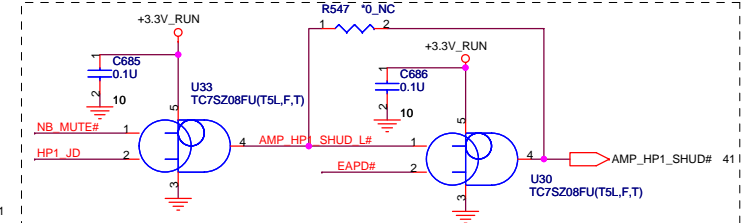
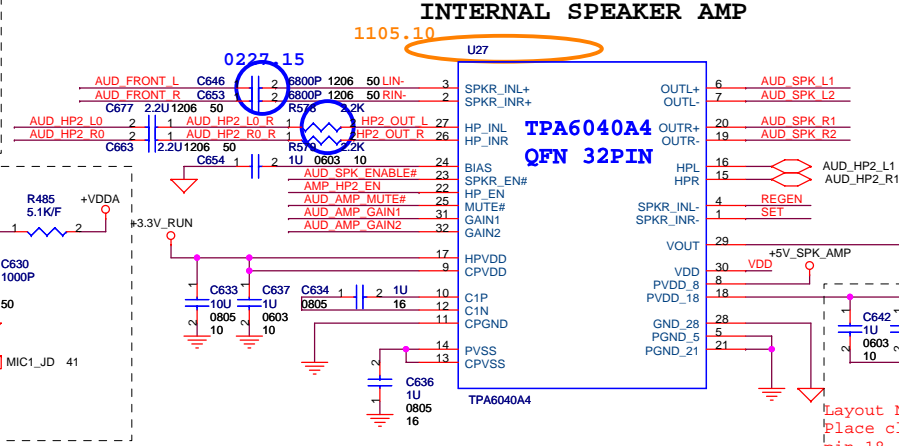
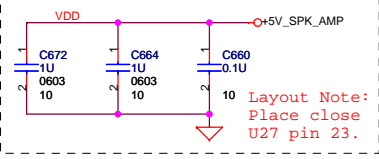
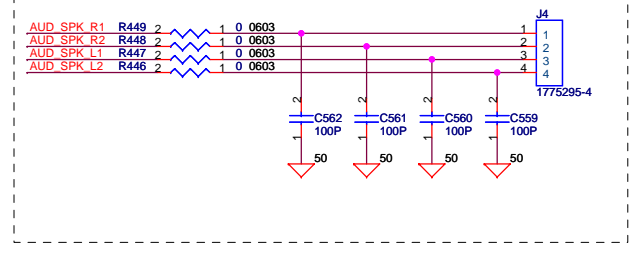
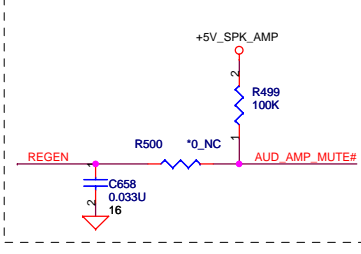
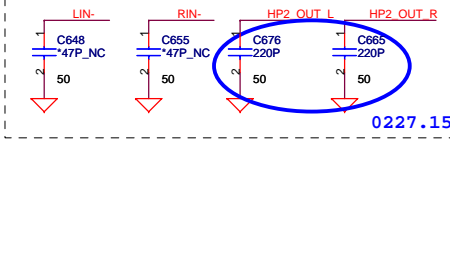
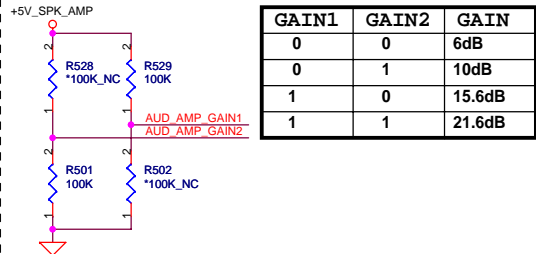


QUANTA COMPUTER

Title: FAN & THERMAL

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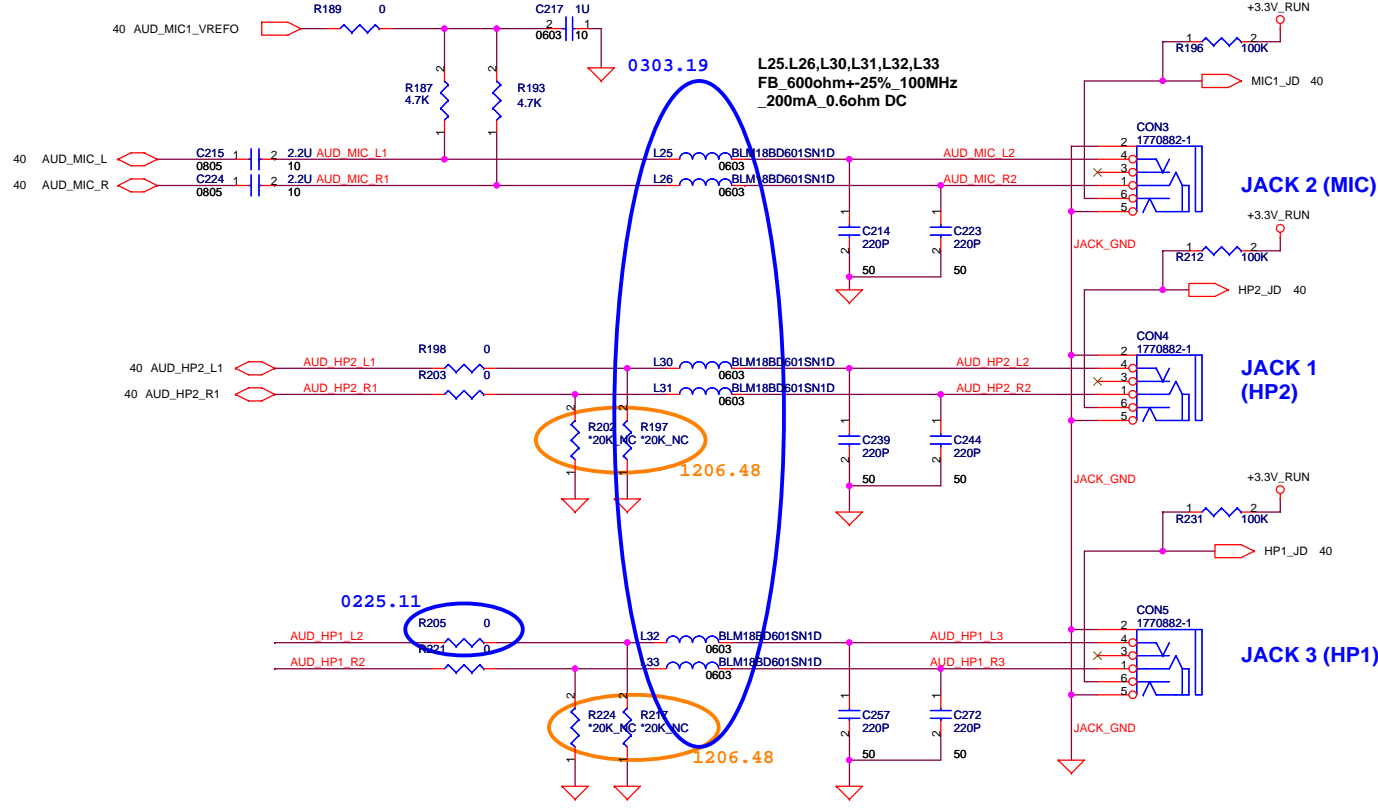


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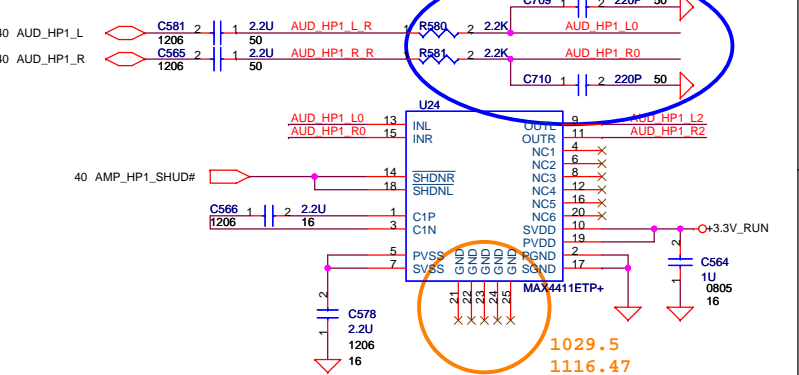
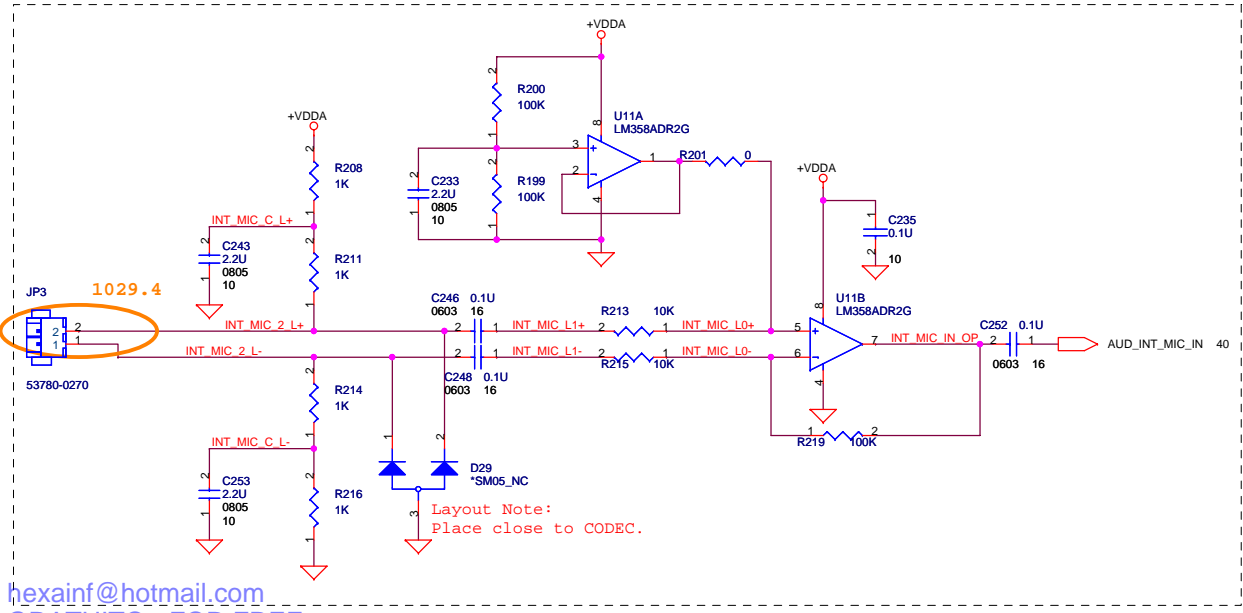
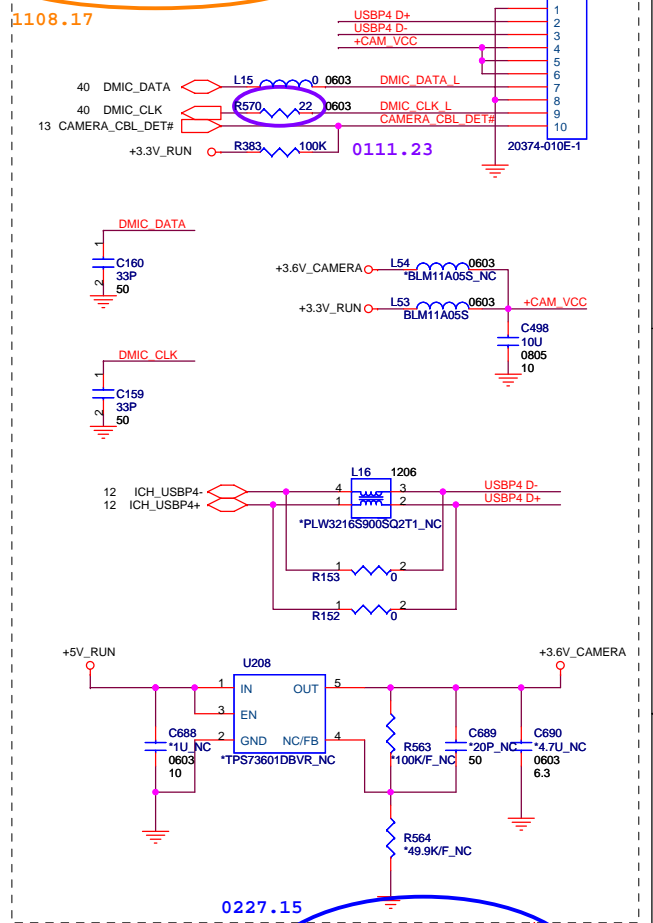
QUANTA COMPUTER

Title: Azelia CODEC
 Size: Document Number FM6B
 Date: Friday, February 29, 2008 Sheet 40 of 65 Rev 1A

Headphone Jack Stereo MIC Jack



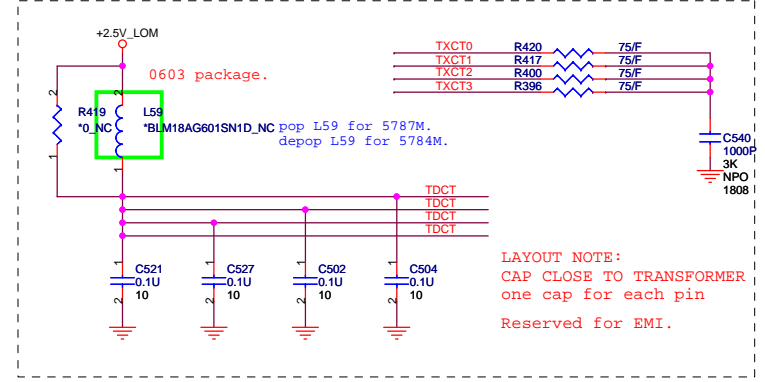
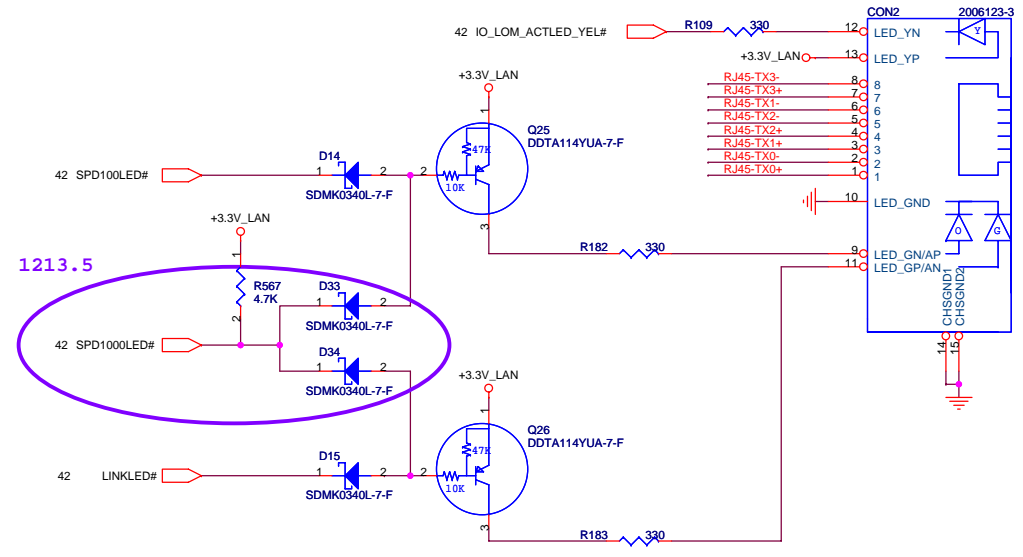
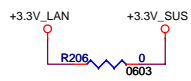
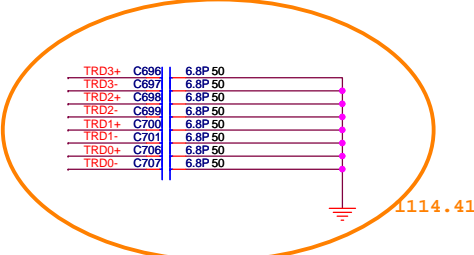
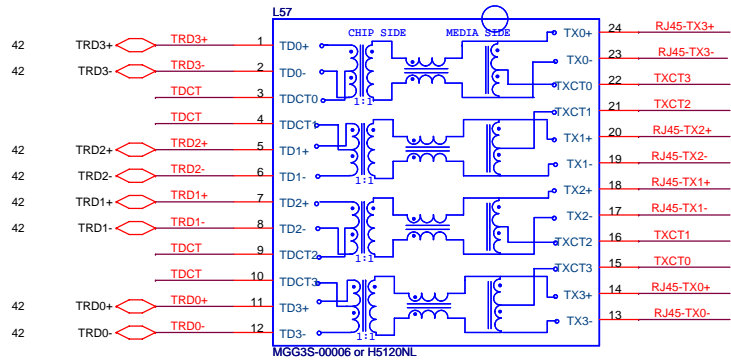
Array Microphone & Camera



Title AUDIO CONN		
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TRANSFORM

TRANSFORM



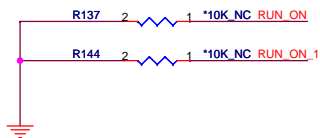
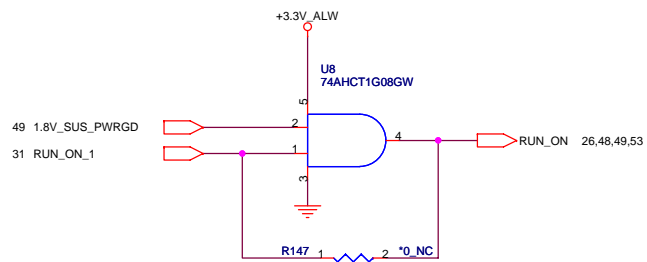
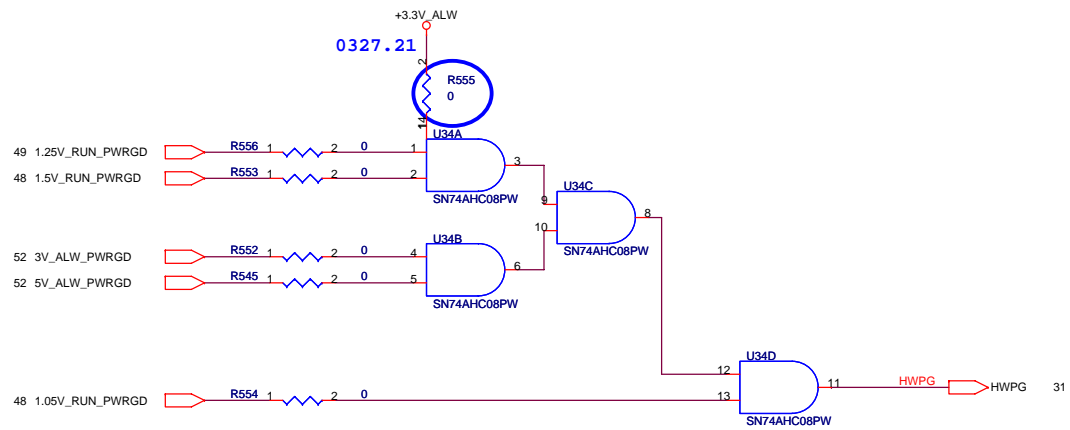
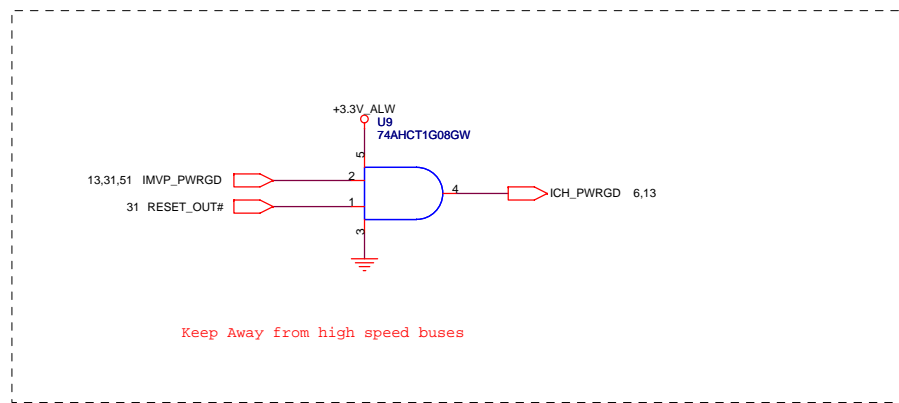
RJ-45 Connector

QUANTA
COMPUTER


Title: LAN SWITCH

Size: Document Number FM6B Rev 1A

Date: Friday, February 22, 2008 Sheet 43 of 65



			Title System Reset Circuit
Size Document Number FM6B	Date: Thursday, March 27, 2008		Rev 1A
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 QUANTA COMPUTER		
Title: Docking Q-SWITCH		
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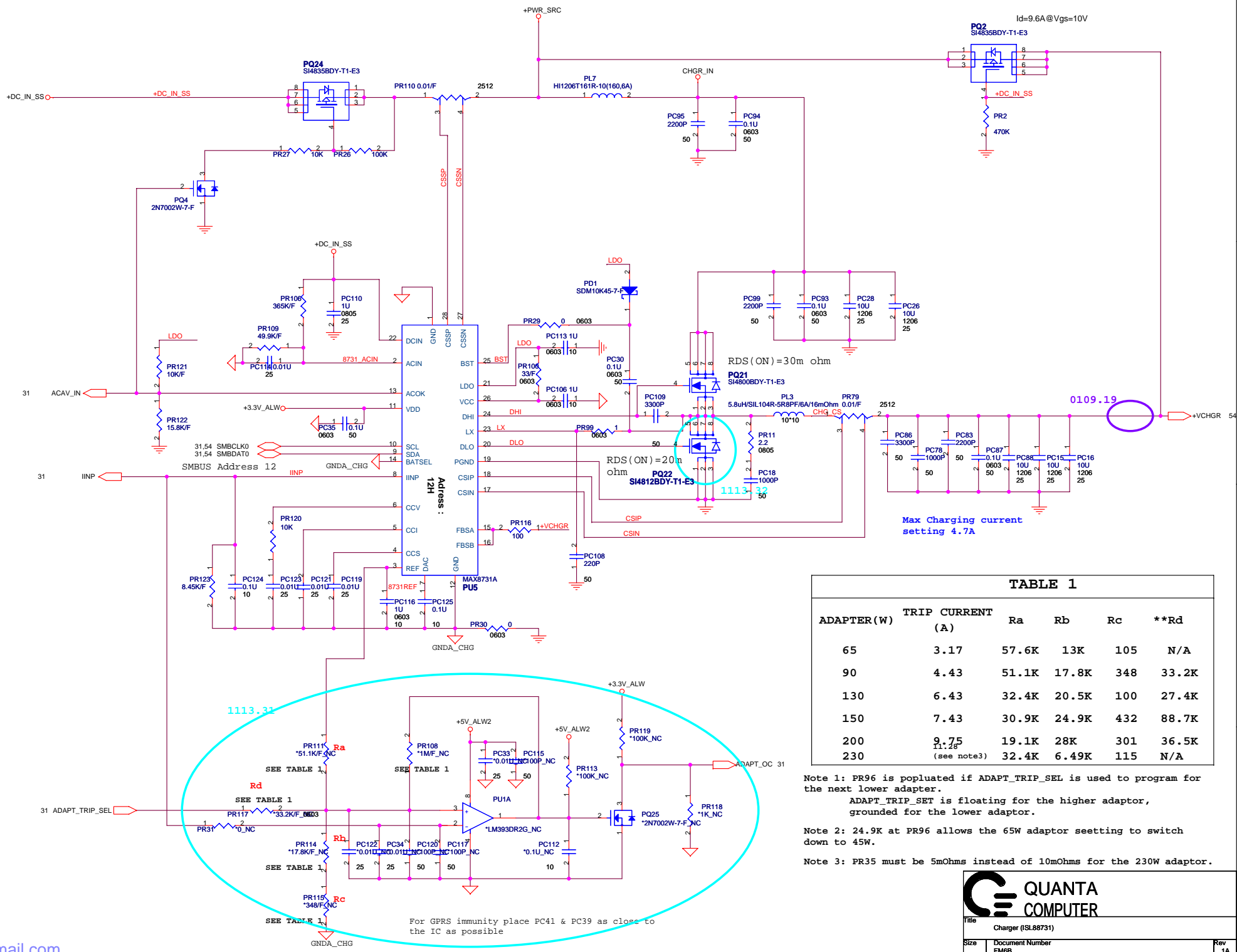


TABLE 1

ADAPTER (W)	TRIP CURRENT (A)	Ra	Rb	Rc	**Rd
65	3.17	57.6K	13K	105	N/A
90	4.43	51.1K	17.8K	348	33.2K
130	6.43	32.4K	20.5K	100	27.4K
150	7.43	30.9K	24.9K	432	88.7K
200	9.75	19.1K	28K	301	36.5K
230	11.28 (see note3)	32.4K	6.49K	115	N/A

Note 1: PR96 is populated if ADAPT_TRIP_SEL is used to program for the next lower adaptor.
 ADAPT_TRIP_SET is floating for the higher adaptor, grounded for the lower adaptor.

Note 2: 24.9K at PR96 allows the 65W adaptor setting to switch down to 45W.

Note 3: PR35 must be 5mOhms instead of 10mOhms for the 230W adaptor.


QUANTA COMPUTER

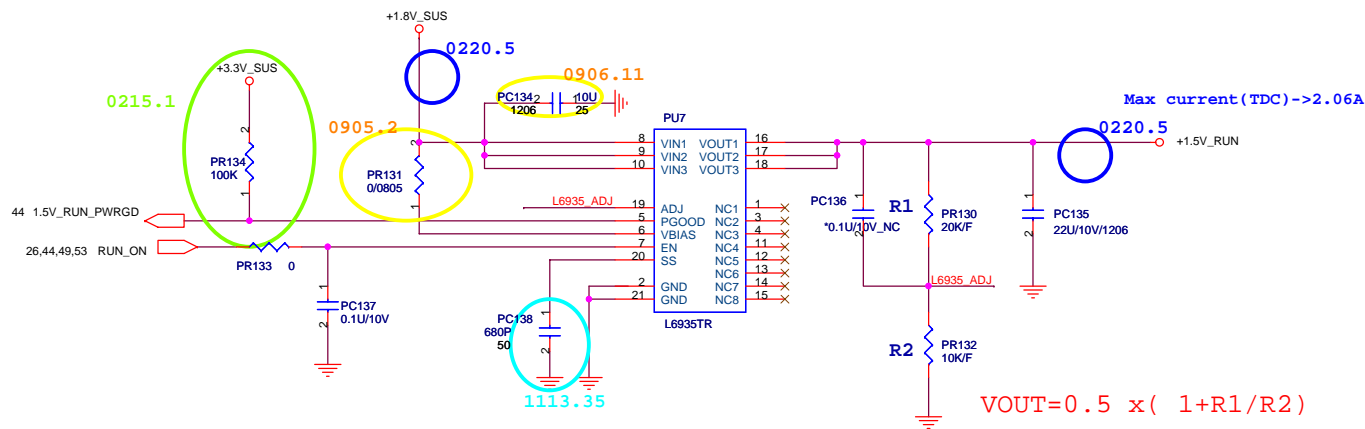
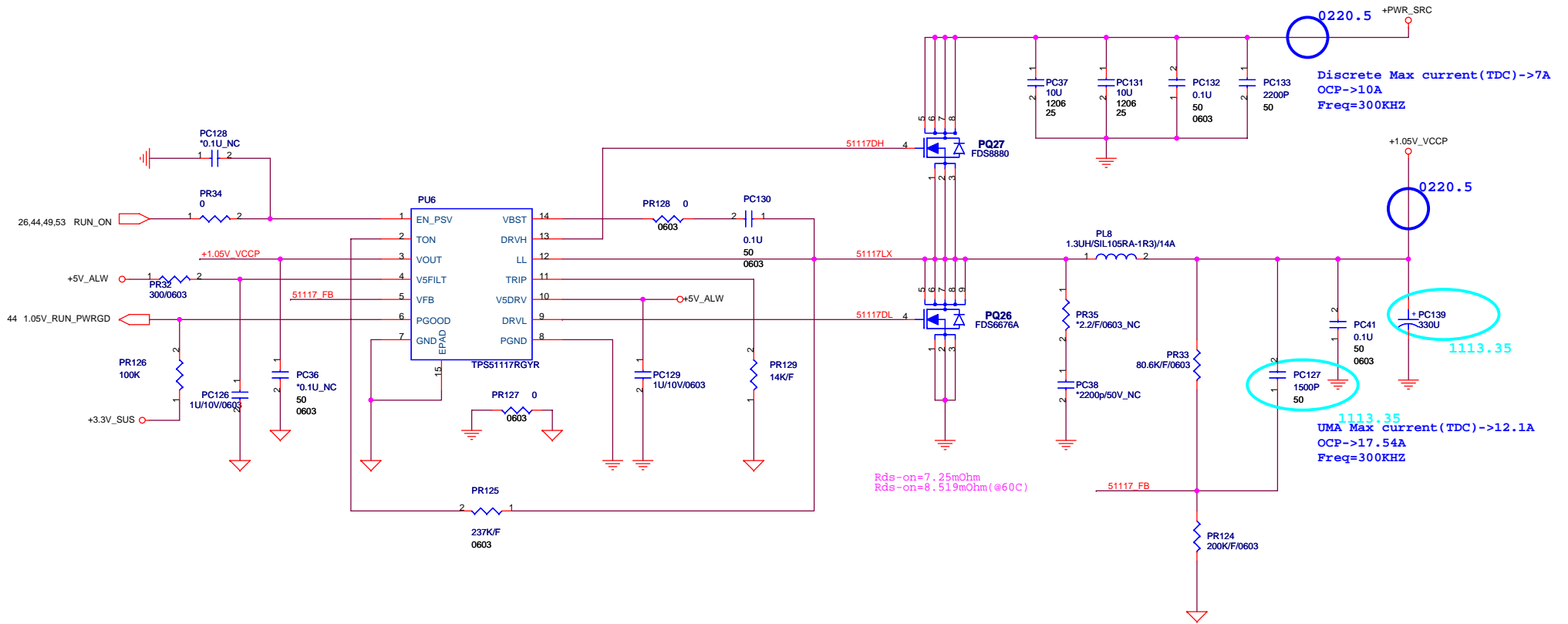
Title: Charger (ISL8731)

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For GPRS immunity place PC41 & PC39 as close to the IC as possible

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	UMA(12.1A)	Discrete(7A)
PQ22	FDS8880_NL (BAM88800012)	FDS8878 (BAM88780020)
PQ25	FDS6676AS_NL (BAM66760026)	FDS6680AS (BAM66800061)
PL25	SIL105RA-1R5-R (CV-15F0MZ08)	SIL104R-1R5PF (DC-15A00010)
PR452		


QUANTA COMPUTER

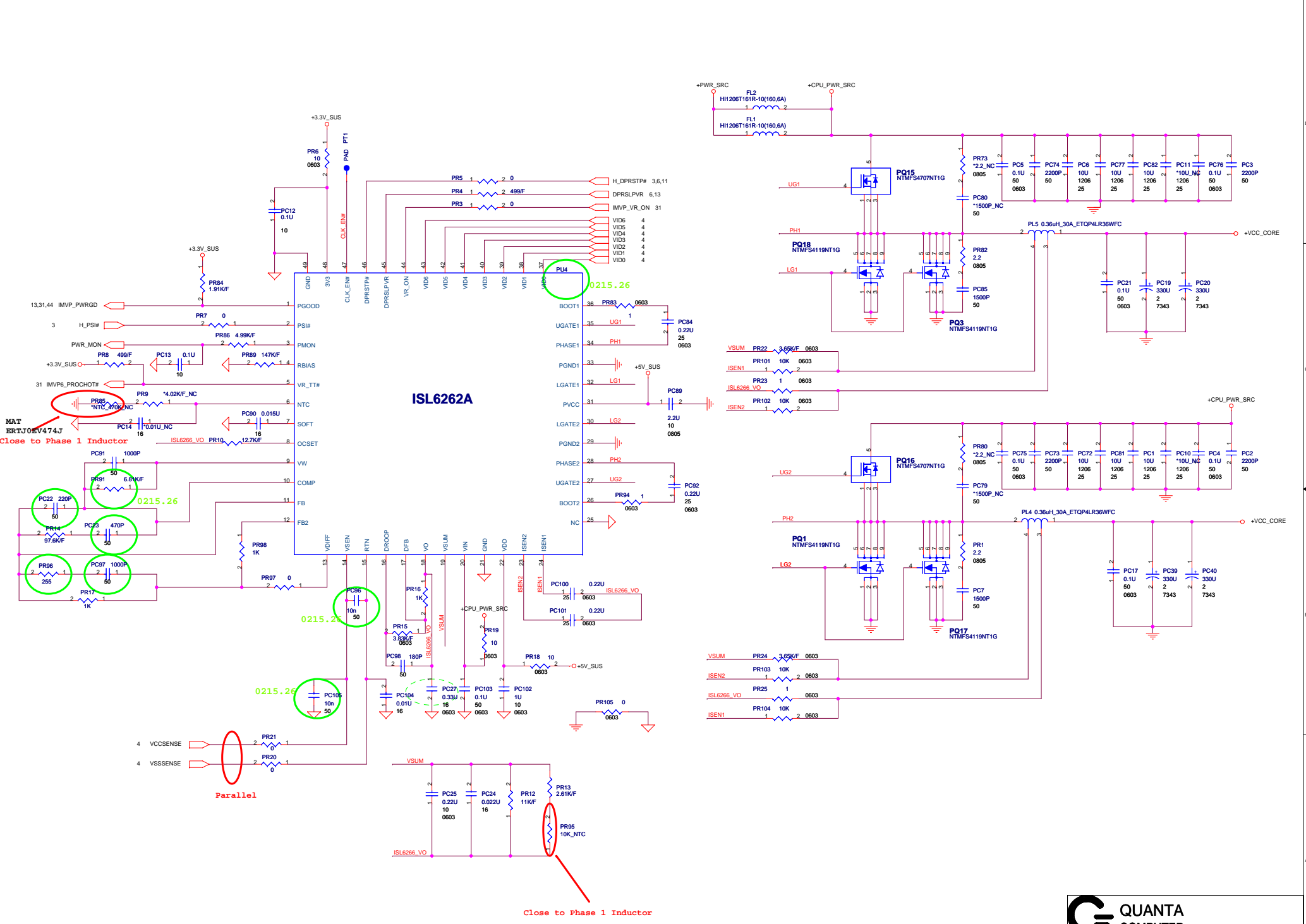
File: 1.05_VCCP & 1.5V_RUN

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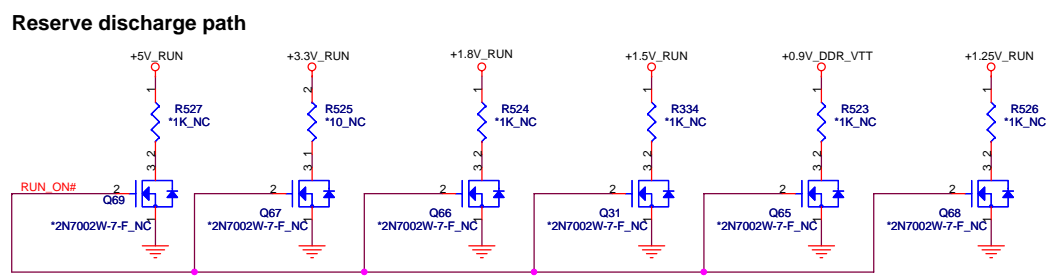
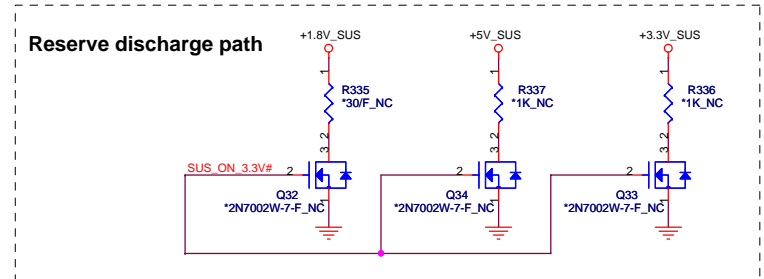
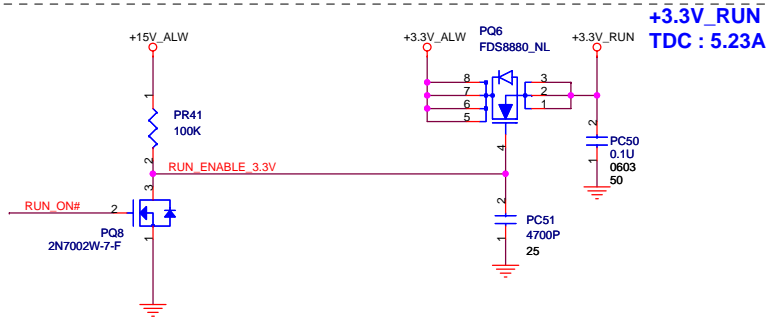
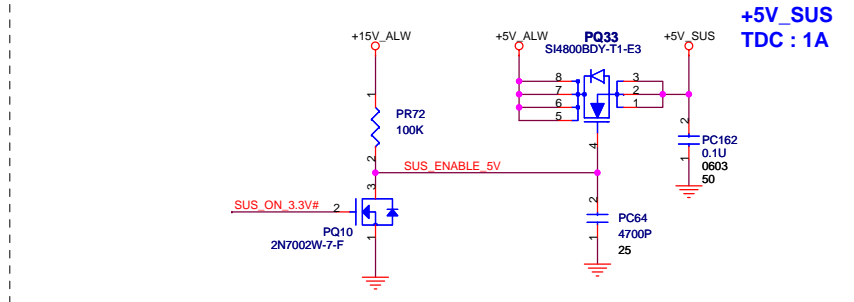
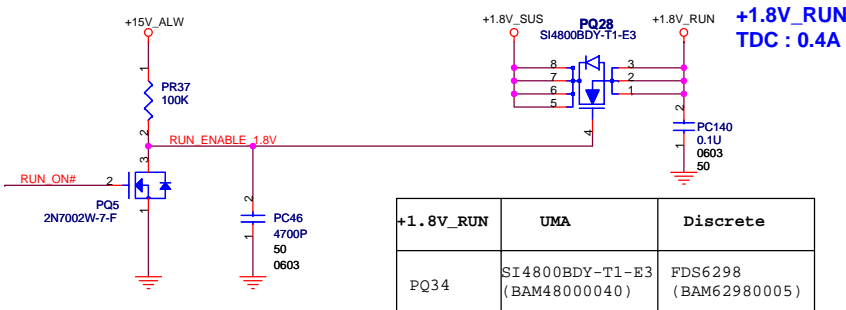
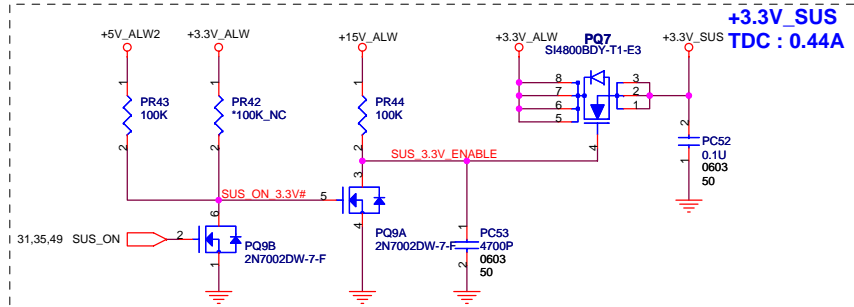
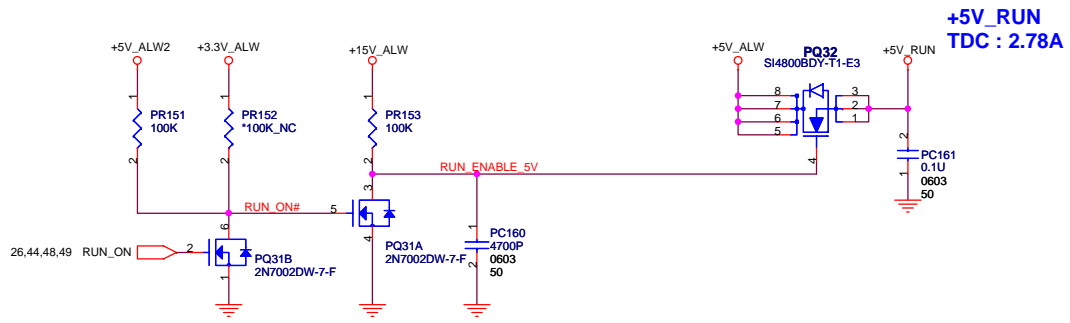
 QUANTA COMPUTER		
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Close to Phase 1 Inductor

Parallel

Close to Phase 1 Inductor

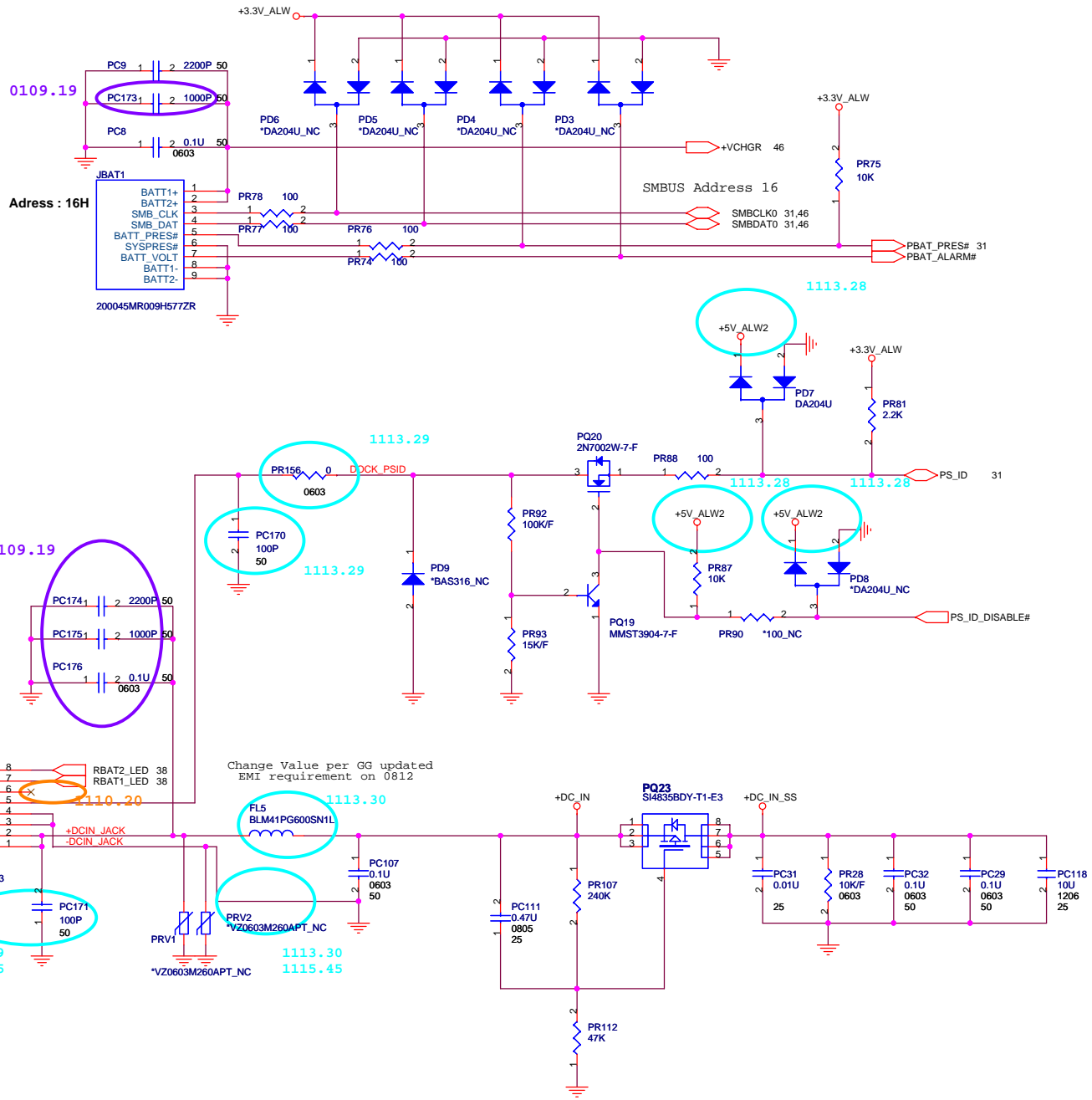


QUANTA COMPUTER

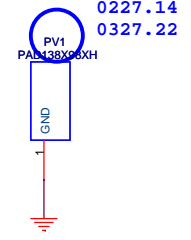
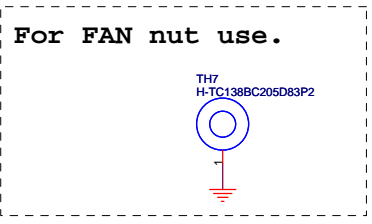
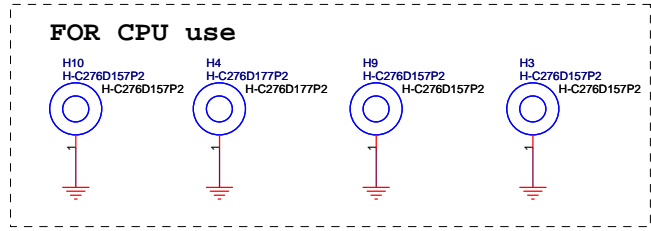
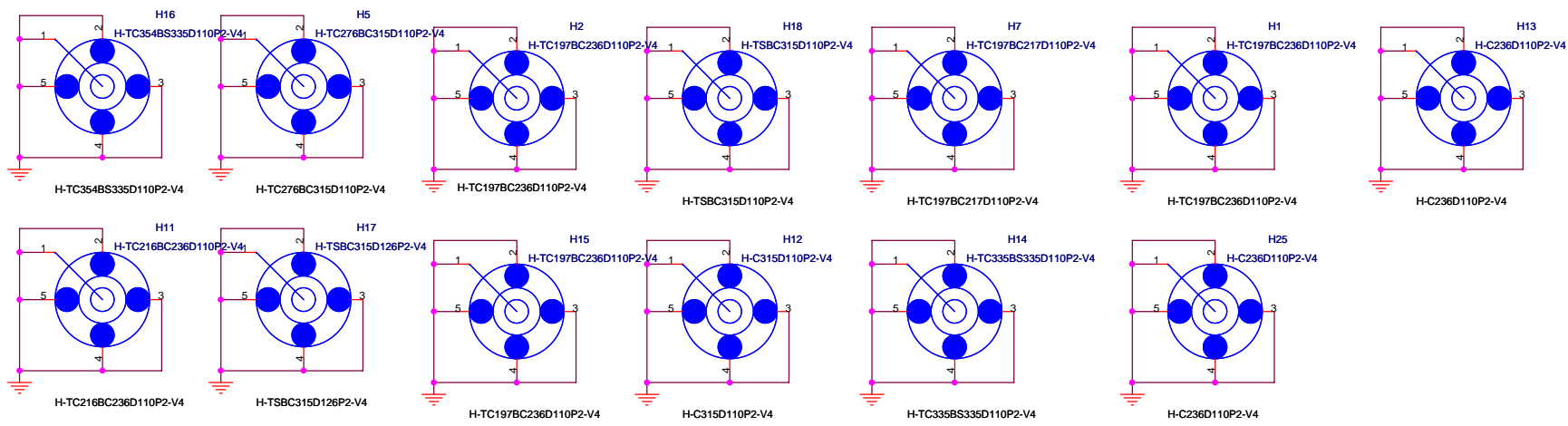
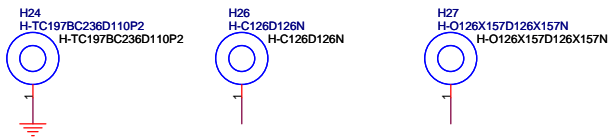
Title: RUN POWER SW

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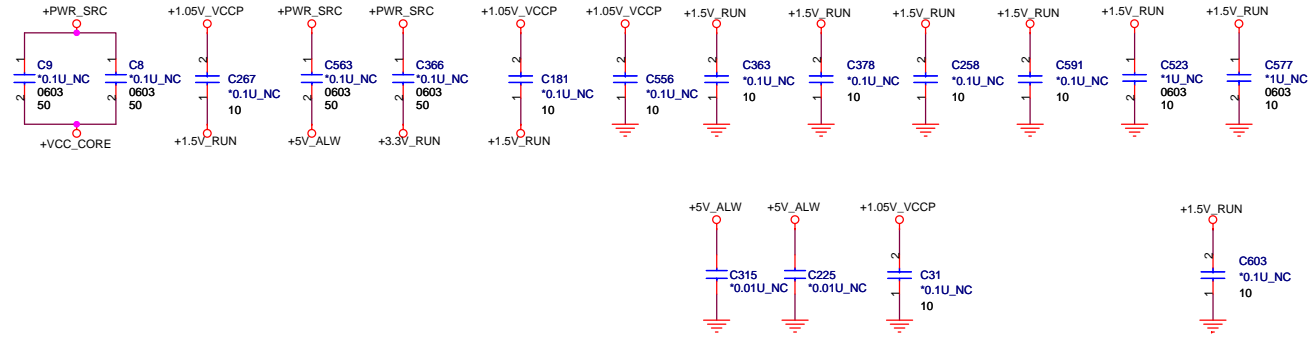
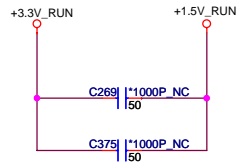
Title DCIN, BATT CONNECTOR		
Size FM6B	Document Number FM6B	Rev 1A
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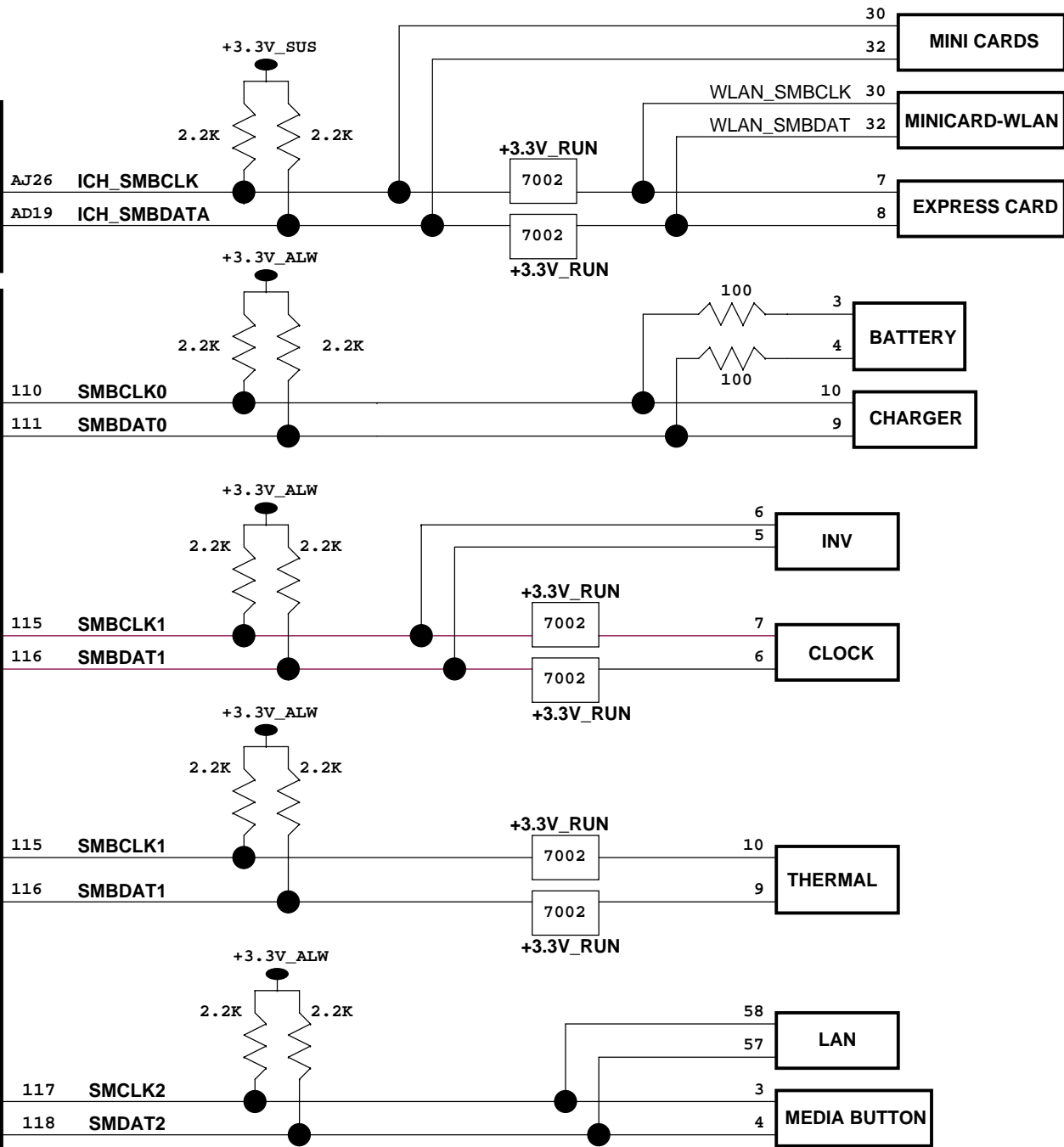
Title: SCREW PAD		
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Reserved for EMI.

Stitching caps.

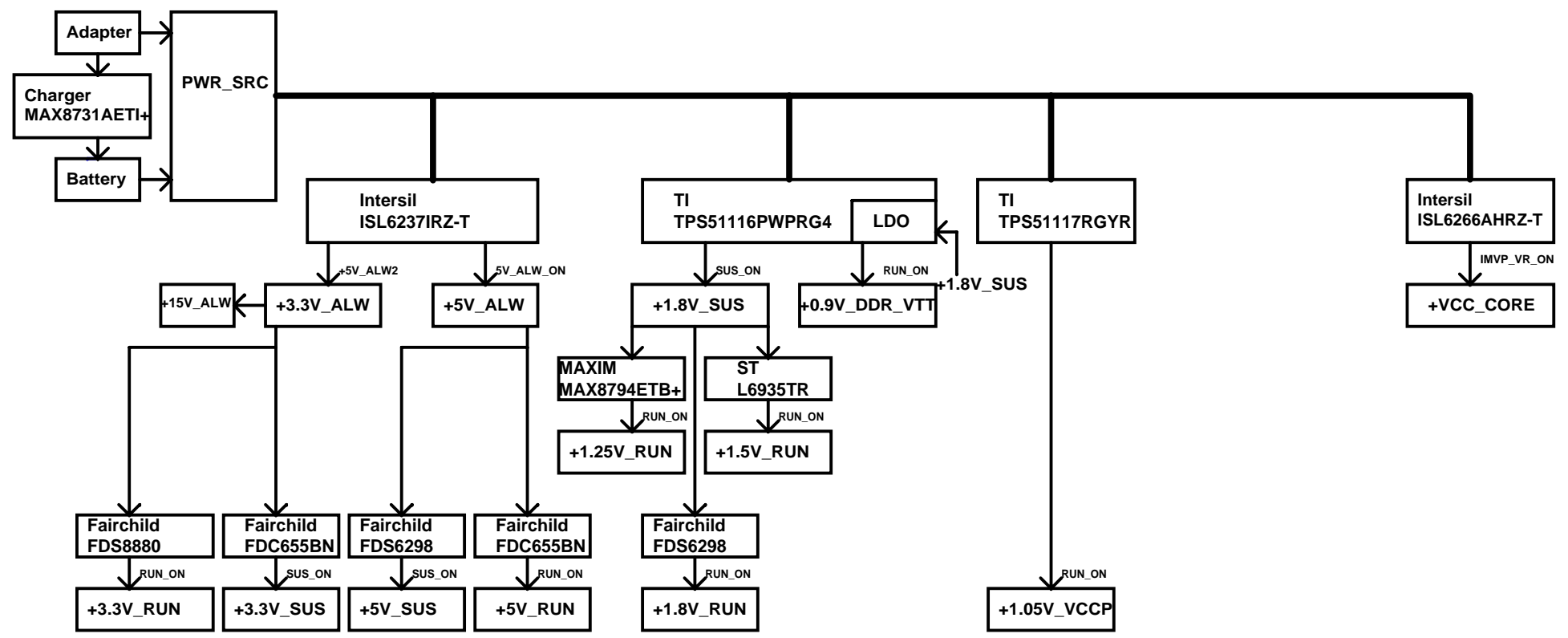


 QUANTA COMPUTER		
Title: EMI CAP		
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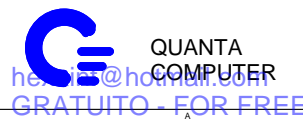
QUANTA
COMPUTER

Title SMBUS BLOCK		
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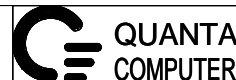
Title Schematic Block Diagram1		
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MODEL	REV	CHANGE LIST	Model	FM6 MB	
			Page	FM	TO
FM6B MB	1A	Refer to ECN No.	1	2A	3A
			2	1A	
			3	2A	
			4	1A	
			5	1A	
			6	1A	
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			9	2A	
			10	1A	
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			55	2A	



PROJECT : FM6B	DOC. NO.	REV:	ASSY:	
APPROVED BY : Kevin Chang	CHECKED BY: Kevin Yu	DRAWN BY : Kevin Yu	DATE :	SHEET 1 OF 1

Model	Item	Page	Date	ECN Number	Item Id	Rev.	Issue Description	Solution Description
FM6B	1	36	29.Oct.07				Modify "JMOD1" symbol	Done.
	2	29	29.Oct.07				Add 2 ground pin on J6 symbol	Done.
	3	55	29.Oct.07				Modify symbol UMA: H2,H5,H7,H8,H16,H18,H19	Done.
	4	41	29.Oct.07				Remove M1.	Done.
	5	41	29.Oct.07				Add 4 analog ground pins for U24	Done.
	6	42	29.Oct.07				change SUPER_IDDQ resistor setting R497 from "*39K_NC" to "*20K_NC" (At this moment this function not support).	Done.
	7	31 37	05.Nov.07				modify LED Key board Illumination schematic	1, Remove EC pin 68 2, Depop R204,Q27,R209,Q28,C245,C242,R210 pop R207, add Q70 and Q70.2 connect "KB_BACKLITE_EN" and remove "KB_BACKLITE_SET" on J3, and add "LED_PWM" between Q70.3 and J3.4
	8	38	05.Nov.07				Depop SNIFFER_YELLOW LED circuit. and Swap WIRELESS_ON/OFF#, SNIFFER_PWR_SW# circuit.	1, Depop R365, Q38, Q8, R27 2, Swap R341, R54 signals
	9	35	05.Nov.07				Added USB charge co-lay circuit for prevent leakage.	1, Reserve Q71,R557,U206,U207 for NC. 2, Add R558,R559,R560,R561 for Co-lay.
	10	40	05.Nov.07				change TPA6040A4 symbol design to meet SPEC definition	Done.
	11	9	05.Nov.07				Add one 0ohm between +1.8V_SUS and "+VCC_SM_CK" for EMI fine tune.	Add R562, Done.
	12	3 52	05.Nov.07				Modify H_THERMTRIP# Voltage Level shift circuit.	1, Add Q72, C687. 2, Pop PR52,PR53.
	13	33	05.Nov.07				Modify JSIM1 connector.	Done.
	14	13	08.Nov.07				Can not enter S3 mode.	change,"USB_MCARD1_DET#", the power rail of pull up circuit from "+3.3V_RUN" to "+3.3V_SUS".
	15	17	08.Nov.07				To match EA spec for "CLK_ICH_48M" item.	change C552 from "27P_NC" to "20p".
	16	31 42	08.Nov.07				To match the frequency stability of oscillation circuit. (By TXC test and Recommend).	1, Adjust C125,C143 from "10pF" to "18pF". 2, Adjust C536 from "27pF" to "22pF".
	17	41	08.Nov.07				Added +3.6V_CAMERA Camera power circuit	1, Added U208,C688,R563,R564,C689,C690 2, Remove C499 and Pop C159,C160. 3, Modify JCAMERA1 pin define and L54 power rail.
	18	31	08.Nov.07				Adjust "NUM_LED#" and "KB_BACKLITE_EN" and "5V_ALW_ON" position.	1, U6.31 for "KB_BACKLITE_EN" 2, U6.98 for "5V_ALW_ON" 3, U6.88 for "NUM_LED#"
	19	18	08.Nov.07				when plug-in HDMI signal, there are no HDMI option inside Windows Vista.	1, change AVCC33V working voltage from +1.8V_RUN to +3.3V_RUN. 2, Change SDVO_CTRLCLK/ SDVO_CTRLDATA pull-high resistors from 3.3K to 3.9K
	20	31 38 54	10.Nov.07				Remove DC IN LED circuit and change signal name DCIN_DETECT_LED# to CHIPSET_ID1.	Remove R12,Q6,Q5,R13




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Model	Item	Page	Date	ECN Number	Item Id	Rev.	Issue Description	Solution Description									
FM6B	21	31	10.Nov.07				Move "5V_ALW_ON" from U8.98 to U8.83 and add BID1 to EC pin98.	Done.									
	22	31	10.Nov.07				Board ID implementation needs to be updated. Update UMA Board ID Straps table to reflect the following: <table border="1"> <tr> <td>BID1</td> <td>BID0</td> <td>Board Rev</td> </tr> <tr> <td>0</td> <td>0</td> <td>X00</td> </tr> <tr> <td>0</td> <td>1</td> <td>X01</td> </tr> </table>	BID1	BID0	Board Rev	0	0	X00	0	1	X01	Pop R127 and depop R128.
	BID1	BID0	Board Rev														
	0	0	X00														
	0	1	X01														
	23	38	12.Nov.07				EMI Solution: Create five capacitances 100pF at the 2, 3, 4, 6, 7 pin separately for JSW1 Connector	Done.									
	24	37	12.Nov.07				EMI Solution: Create two capacitances 100pF at the 1, 10 pin separately for JP1 connector.	Done.									
	25	35	12.Nov.07				EMI Solution: Remove R72, R76, R78, R80 and add L9, L8	Done.									
	26	41	12.Nov.07				Reserve +3.6V_CAMERA for camera module first.	Depop U208,C688,R563,R564.									
	27	13	12.Nov.07				"THERM_ALERT#" should change the power rail from ""+3.3V_SUS" to "+3.3V_RUN" according datasheet.	Done.									
	28	54	13.Nov.07				Change PD7,PD8,PR87 connection to connect +5V_ALW2	Done.									
	29	54	13.Nov.07				Add PR156,PC170,PC171,PR157 for EMI	Done.									
	30	54	13.Nov.07				Change FL5 to BLM41PG600SN1L and del FL4(add PJP21)	Done.									
	31	46	13.Nov.07				Depop PR117 ,PR31 ,PR111 ,PR114 ,PR115 ,PC122 ,PC34 ,PC120 ,PC117 ,PR108 ,PC33 ,PC115 ,PU1 ,PC112 ,PR113 ,PR119 ,PR118 and PR25	Done.									
	32	46	13.Nov.07				Change PQ22 to SI4812BDY	Done.									
	33	52	13.Nov.07				Change PL1 ,PL2 to CV-3380TZ00 and PQ13 ,PQ14 to SI4812BDY	Done.									
	34	49	13.Nov.07				1. Change PC157 ,PC158 to 220U/2.5V/ESR15 and PL9 to 1.3UH/SIL1045RA-1R3 and PQ30 to FDS6676A 2. Pop PR150,PC154 3. Add PR155, PC172	Done.									
	35	48	13.Nov.07				1. Change PR134 to connect RUN_ON and PC138 to 680PF 2. Pop PC127 to 1500PF 3. Change PC139 to 330U/2V/ESR12	Done.									
36	51	13.Nov.07				Change PU4 footprint	Done.										
37	31	13.Nov.07				Connect "THERM_STP#" with ITE8512.	Done.										
38	40	13.Nov.07				Change Codec IC from STAC9228 to 92HD73C.	1, Depop R494,C651. 2, Depop R543, R549, R498,R548 and pop R542, R551, R495 ,R541.										



Title			
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Model	Item	Page	Date	ECN Number	Item Id	Rev.	Issue Description	Solution Description
FM6B	39	30 35	14.Nov.07				EMI Solution: 1, Define Card Reader shielding into Analog GND. 2, Define express card reader shielding into Digital GND. 3, Define USB connector shielding into Digital GND.	Done.
	40	18	14.Nov.07				EMI Solution: Add L40, L41, L42, L43 and depop R360,R361,R359,R358, R347,R349,R356,R353.	Done.
	41	43	14.Nov.07				EMI Solution: Create 8 capacitances 6.8pF between the TRD3+, TRD3-, TRD2+, TRD2-, TRD1+, TRD1-, TRD0+, TRD0- (1, 2, 5, 6, 7, 8, 11, 12pin) and GND separately.	Done.
	42	18	14.Nov.07				when plug-in HDMI signal, there are no HDMI option inside Windows Vista.	Change SDVO_CTRLCLK/ SDVO_CTRLDATA pull-high resistors from 3.3K to 5.6K
	43	37	14.Nov.07				Change R207 to FS3 for "Key board Illumination" circuit.	Done.
	44	13	14.Nov.07				Reserve 0ohm for GPIO18 of ICH8M for PCIE_MCARD1_DET# debug.	Done.
	45	54	15.Nov.07				Remove PR157 and PJP21 to fulfill EMI request.	Done.
	46	40 41	15.Nov.07				Change C677,C663,C581 and C565 to 2.2u for batter Audio precision. (per IDT suggestion)	Done.
	47	41	16.Nov.07				Leave U24.pin 21,22,23,24,25 unconnected by FAE suggestion.	Done.
	48	41	06.Dec.07				Remove these 20K ohm resistors because it is for desktop design or codec internal headphone amplifier.	Depop R197, R202, R217, R224, done.
	49	42	06.Dec.07				Change BCM5787M to BCM5784M.	Done.
50	3	06.Dec.07				Modify H_THERMTRIP# Voltage Level shift circuit.	Adjust R368 from 1Mohm to 10Mohm,done.	
51	31	06.Dec.07				Change SMBDAT1/SMBCLK1 pull-up resistors with 10Kohm from 2.2Kohm.	Done.	



**QUANTA
COMPUTER**

Title: Change List

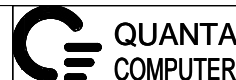
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Model	Item	Page	Date	ECN Number	Item Id	Rev.	Issue Description	Solution Description									
FM6B	1	38	13.Dec.07				Sniffer should be during S5.Dell define our Sniffer switch need to stay 'ON' after the WiFi can be enable.	change R341 to +3.3V_ALW.									
	2	31	13.Dec.07				Follow ITE feedback to reserve caps for ITE8512JX.	Add C704,R566 to U6 pin.12.									
	3	35	13.Dec.07				Change USB Q-switch power rail from +3.3V_RUN to +3.3V_SUS.	Change U206 pin.8, U207 pin.8 from +3.3V_RUN to +3.3V_SUS, Q71 pin.2 from RUN_ON to SUS_ON.									
	4	31	13.Dec.07				Sniffer power switch needs to wake up EC, when battery only. So it needs to use WUI pin.	Swap U6.108 SNIFFER_PWR_SW# and U6.35 WIRELESS_ON/OFF#									
	5	42 43	13.Dec.07				Modify LAN 1000 LED circuit to solve BCM5784M LED issue.	Add D33,D34,R567 to solve BCM5784M 1000 LED issue.									
	6	32	13.Dec.07				BT1 connector pin define is different before.	Change BT1 pin.1 to GND, pin.2 to +RTC.									
	7	17	13.Dec.07				MCH DPLL clock trace connection is not correct.	MCH_DREFCLK connect with U23 Pin.20 MCH_DREFCLK# connect with U23 Pin.21 DREF_SSCLK connect with U23 Pin.24 DREF_SSCLK# connect with U23 Pin.25									
	8	36	24.Dec.07				Exchange Q61A and Q60B position inside schematic.	Done.									
	9	18	25.Dec.07				Setup SDSCL/SDSDA pull up voltage more achieve spec.	Add R568,R569 and change R69, R71 to get 2.52V pull up voltage.									
	10	38	25.Dec.07				Change ESD3 power rail from +3.3V_ALW to +3.3V_RUN.	Done.									
	11	37	31.Dec.07				1, Change MMB LED power source from ALW plane to RUN plane for power saving .added one 5V_ALW2 power plane for PAID diag used. 2, Change the Media board power from 3V_ALW to 5V_ALW2 to solve LED flash issue when AC/Bat plug in.	Done.									
	12	37	31.Dec.07				WLAN and BT LED need to show function at factory side.	Change power supply of Cap and Num LED from 5V_ALW2 to 5V_RUN.									
	13	37	31.Dec.07				Avoid system can enter S3 mode but wake up fail problem.	Change the lid switch IC power source from 3.3V_SUS to 3.3V_ALW.									
	14	31	31.Dec.07				Board ID implementation needs to be updated. Update UMA Board ID Straps table to reflect the following: <table border="1" style="margin-left: 20px;"> <tr> <td>BID1</td> <td>BID0</td> <td>Board Rev</td> </tr> <tr> <td>0</td> <td>1</td> <td>X01</td> </tr> <tr> <td>1</td> <td>0</td> <td>X02</td> </tr> </table>	BID1	BID0	Board Rev	0	1	X01	1	0	X02	Pop R128 and depop R127. Pop R133 and depop R134.
	BID1	BID0	Board Rev														
	0	1	X01														
	1	0	X02														
	15	37	7.Jan.08				MMB vendor will change F/W to fix the issue that LED flash issue when AC/Bat plug in. So change the circuit back to original.	Done.									
	16	37	7.Jan.08				Prevent the leakage from +3.3V_ALW to +5V_RUN inside Num/Cap LED circuit.	Change Q15.pin2, Q16.pin2, R57 and R58 from +3.3V_ALW to +3.3V_RUN.									
17	35	9.Jan.08				Fulfill Reliability team request.	Connect J5.Pin8 to +USB_BACK_PWR.										
18	49	9.Jan.08				Change PJP18 to FL6, According POWER team request.	Done.										
19	35 46	9.Jan.08				Fulfill EMI team request. FI3 change to short-circuit USB CONN.: use Murata Common mode Choke (P/N: DL W 21 S N 900 H Q 2 L) L8 , L9 , LN1 , LN2	Done.										



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Model	Item	Page	Date	ECN Number	Item Id	Rev.	Issue Description	Solution Description									
FM6B	1	48	15.Feb.08				Solve 1.5V PWRGD issue.	change to pull high PR154 to +3.3V_SUS.									
	2	28,29 35,42	20.Feb.08				Fulfill safety team request, change USB control IC (TPS2062) location of UMA same as Discrete platform.	ORINIGAL U5, U13 -> TPS2062AD U7-> 24LC02BT-I/STG in P.42 U16-> R5C833 in P.28,29 AFTER SAFETY TEAM REQUEST, U7, U16 -> TPS2062AD U5-> 24LC02BT-I/STG in P.42 U13-> R5C833 in P.28,29									
	3	18	20.Feb.08				Fulfill EMI team request, change common choke for HDMI CONN.: use Panasonic Common mode Choke (P/N: EXC24CG900U) L40 , L41 , L42 , L43	Done.									
	4	31	20.Feb.08				Use ITE8512 pin 22 detect ICH_AZ_CODEC_RST# to mute speaker pop noise.	Connect ICH_AZ_CODEC_RST# and U6 pin 22.									
	5	9,18 35,48 49,52	20.Feb.08				Delete all debug power jump.	Done.									
	6	31	20.Feb.08				Board ID implementation needs to be updated. Update UMA Board ID Straps table to reflect the following: <table border="1"> <tr> <td>BID1</td> <td>BID0</td> <td>Board Rev</td> </tr> <tr> <td>1</td> <td>0</td> <td>X02</td> </tr> <tr> <td>1</td> <td>1</td> <td>A00</td> </tr> </table>	BID1	BID0	Board Rev	1	0	X02	1	1	A00	Depop R128 and pop R127.
	BID1	BID0	Board Rev														
	1	0	X02														
	1	1	A00														
	7	18	20.Feb.08				DDC Capacitance over spec 50pf. We will add level shift circuit to reduce Capacitance.	Add level shift Q73, Q74 2N7002 to reduce the DDC Capacitance.									
	8	4	20.Feb.08				Acoustic team suggest to resolve Acoustic issue.	Pop C438 and C450.									
	9	18	25.Feb.08				Update HDMI level shift circuit.	Add R572,R573,R576,R577.									
	10	13 37	25.Feb.08				Install LED keyboard detect pin between GPIO17 of ICH8 and J3.pin3	Done.									
	11	14,32 41	25.Feb.08				Fulfill safety team request, change RTC resistor and diode location of UMA same as Discrete platform.	Swap D18 and D16, R218 and R205.									
	12	3,6 7,12	25.Feb.08				Delete all EA test pad.	Delete ET1 ~ET68.									
	13	18	26.Feb.08				Update HDMI level shift circuit.	Change Q73,Q74 from 2N7002 to FDV301N.									
	14	55	27.Feb.08				Fulfill EMI team request, add one EMI SPRING near sniffer switch area.	Install PV1, done.									
	15	40,41	27.Feb.08				Need to meet WLP4.0 1, Add 2.2K-ohm resistors to prevent amplifier clipping. 2, Add 220PF capacitors to allow proper dynamic range measurent.	1. Add 2.2K series resistance (R578,R579,R580,R581) between the codec and the headphone amplifier inputs. 2. Add 220pF capacitors (C665,C676,C709,C710) to ground on the headphone amplifier inputs. 3. Change cap from 0.0033U to 6800p for AUD_FRONT_L/AUD_FRONT_R.									
16	30	27.Feb.08				Fulfill EMI team request, add a 22p capacitor in mini SD circuit.	Install C711, done.										
17	13	27.Feb.08				Update ICH_RSMRST# Pd resister	Done.										
18	6	29.Feb.08				Follow Intel design guide, TVA_DAC, TVB_DAC, TVC_DAC connect 75 ohm to GND.	Done.										



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