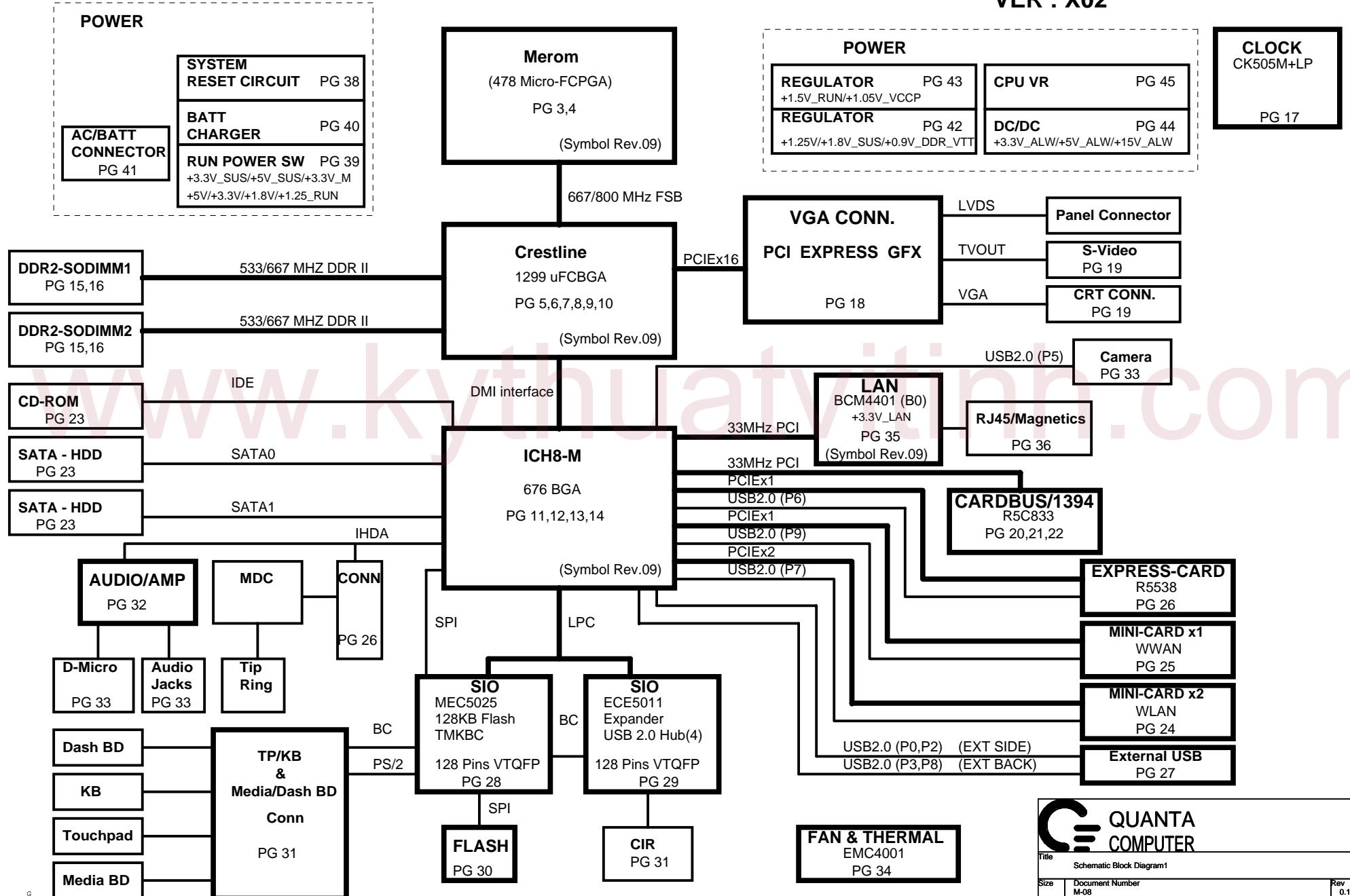


Corsica\Gilligan - DISCRETE

VER : X02



QUANTA COMPUTER

Title: Schematic Block Diagram 1

Size: Document Number M-08 Rev 0.1

Date: Tuesday, March 06, 2007 Sheet 1 of 51

C 31PM5MB0011 31GM2MB0004
G 41PM5SS0017 41GM2SS0000

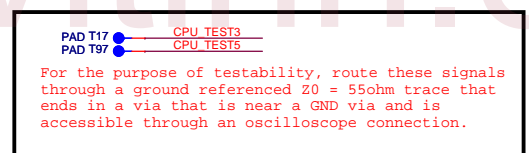
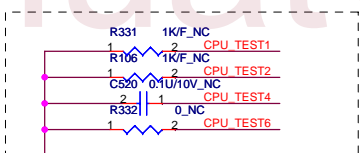
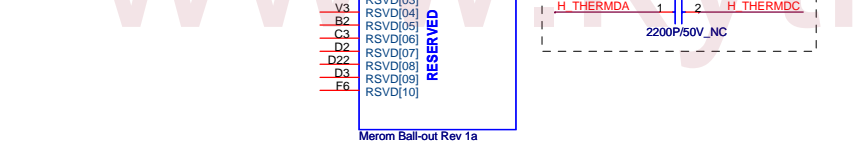
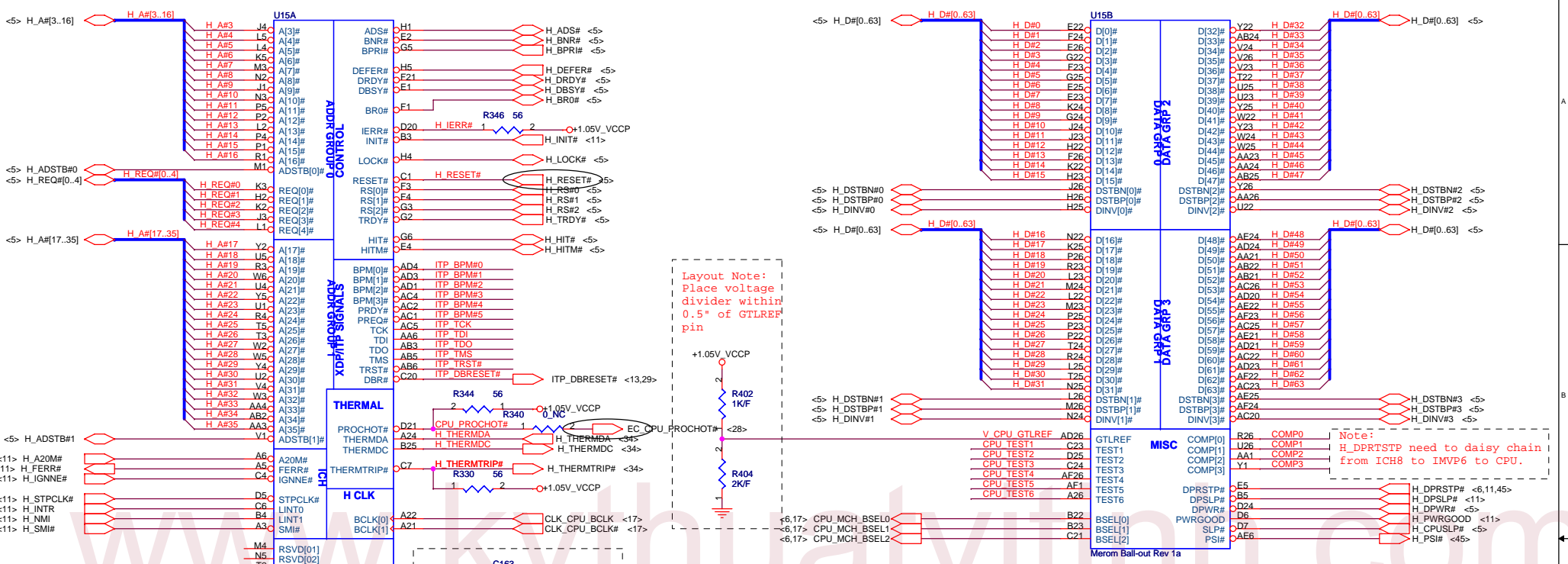
INDEX

Pg#	Description	DNI LIST
1	Schematic Block Diagram	
2	Front Page	
3-4	Merom	
5-10	Crestline	
11-14	ICH8M	
15-16	DDRII SO-DIMM(200P)	
17	Clock Generator	
18-21	VGA	
22	LCD Conn. & SSP	
23	CRT Conn	
24	SATA & IDE Conn	
25	PCCARD/Conn & 1394	
26	Express Card & Smart Card	
27	Mini Card	
28	MDC Conn.	
29	SIO (MEC5004)	
30	SIO (MEC5018)	
31	SERIAL PORT & USB	
32	Flash ROM	
33	TP,BT & FIR	
34	Switch,Keyboard & LED	
35	FAN & Thermal	
36-37	Audio CODEC(STAC9200)/Phone Jack	
38-39	LOM (BCM5752)/Switch	
40-41	Docking Conn/Q-Switch	
42	System Reset Circuit	
43-44	Battery Selector & Charger	
45	DDR2_1.8VSUS, 0.9V	
46	1.5VSUS,1.05V(VTT)	
47	1.25V,1.05VM	
48	CPU_MAX8786(3phase)	
49	D/D Power	
50	RUN Power Switch	
51	VGA DC/DC	
52	DCIN/Batt Conn.	
53	PAD& SCREW	
54	EMI CAP	

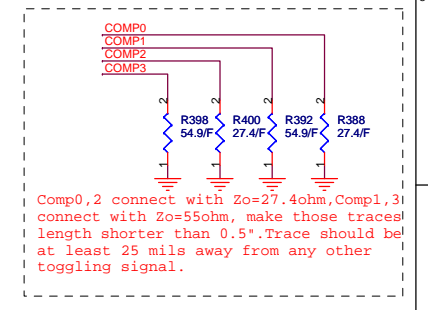
Power & Ground

Label	Pg#	Description	Control Signal
DC_IN+		AC ADAPTER (19V)	
PBATT+		MAIN BATTERY + (10~17V)	
PBATT+		SECOND BATTERY + (10~17V)	
PWR_SRC		MAIN POWER (10~19V)	
RTC_PWR3_3V		RTC & +3.3V_RTC_LDO(3.3V)	
+VCC_CORE		CPU CORE POWER (1.5V)	RUNPWROK
+15V_ALW		LARGE POWER (15V)	SUS_ON
+3.3V_RUN		SLP_S3# CTRLD POWER	RUN_ON
+3.3V_SUS		SLP_S5# CTRLD POWER	SUS_ENABLE
+3.3V_ALW		8051 POWER (3.3V)	ALWON/THERM_STP#
+5V_RUN		SLP_S3# CTRLD POWER	RUN_ON
+5V_SUS		SLP_S5# CTRLD POWER	SUS_ON
+5V_HDD		HDD POWER (5V)	+5V_RUN
+5V_MOD		MODULE POWER (5V)	HDDC_EN
+5V_ALW		LCD/CHARGE POWER (5V)	
+VDDA		AUDIO ANALOG POWER (5V)	AUDIO_AVDD_ON
+1.5V_RUN		CALISTOGA/ICH7 POWER	RUN_ON
+1.05V_VCCP		CPU/CALISTOGA/ICH7 POWER	RUN_ON
+1.8V_SUS		SODIMM POWER	SUSPWROK_5V
+1.8V_RUN		SDVO POWER	RUN_ON
+0.9V_DDR_VTT		SODIMM POWER	RUN_ON
+3.3V_LAN		LAN POWER	AUX_EN
 GND	ALL PAGES	DIGITAL GROUND	
 AGND_ISL6260		CPU GND	
 AGND_TPS51120		DC/DC POWER GND	
 AGND1		VTT POWER GND	
 AGND2		VTT POWER GND	
 8731AGND		CHARGER GND	



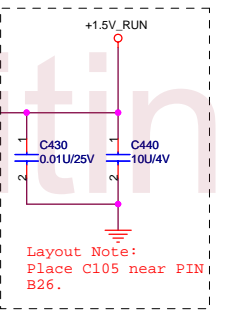
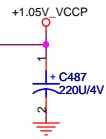
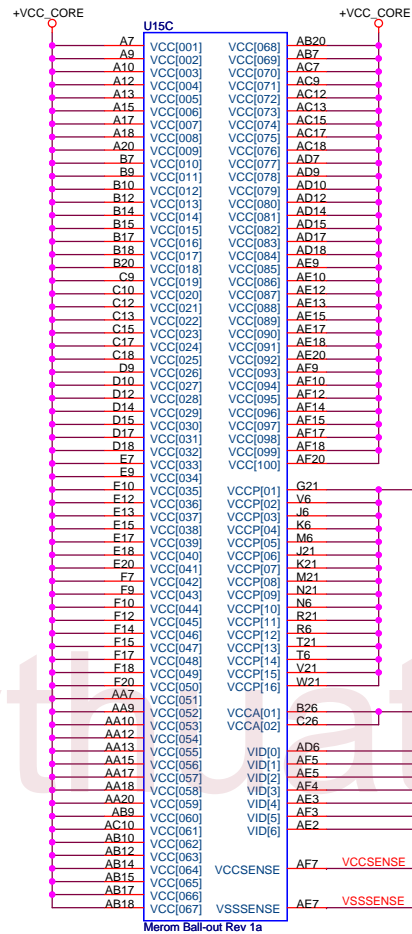
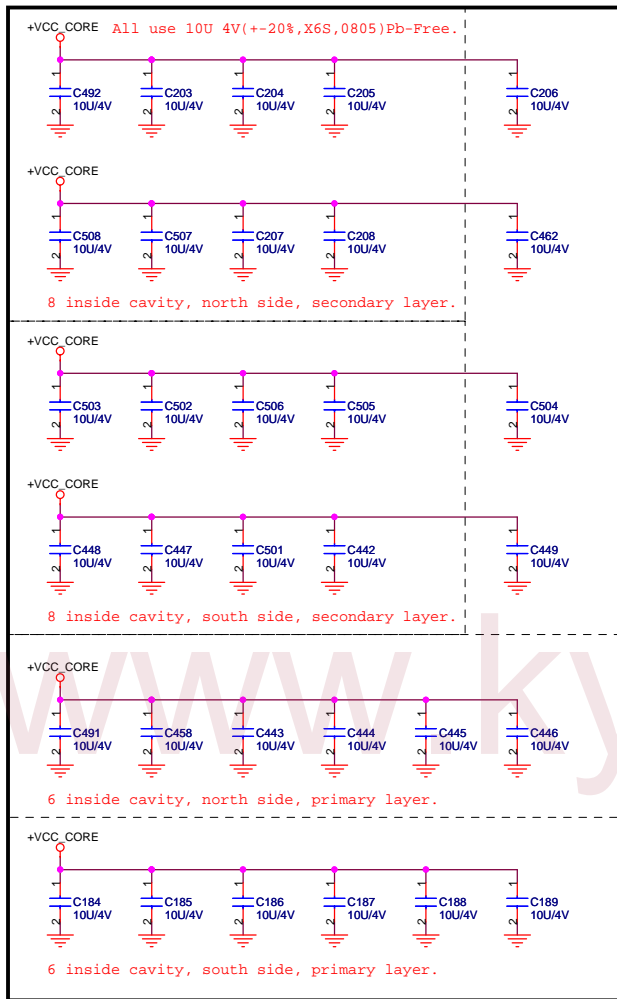


FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

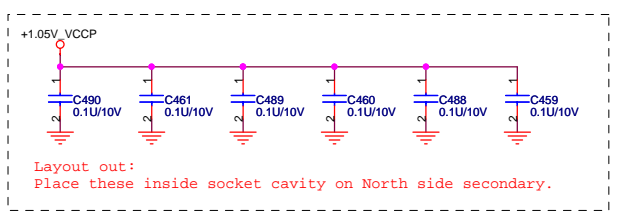


ITP700 layout guidelines

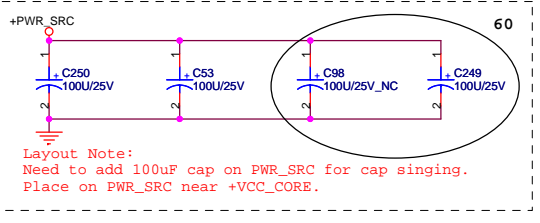
Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm ± 5%	VCCP	Place the pull-up near CPU
TMS	39 ohm ± 1%	VCCP	Within 200ps of ITP connector
TRST#	500 to 680 ohm ± 5%	GND	Place the pull-down near CPU
TCK	27 ohm ± 1%	GND	Connect to TCK pin of CPU and then connect it to FBO pin of ITP connector in daisy chain. Place the pull-down near TCK0 pin of ITP connector
TDO	51 ohm ± 5%	VCCP	Place the pull-up near ITP
RESET#	22.6 ohm ± 1% series resistor and pullup 51 ohm ± 1%.	VCCP	Connect to CPURST# pin of GMCH through the series resistor placed within 200ps of ITP connector. Place the pull-up after the series resistor from ITP connector.



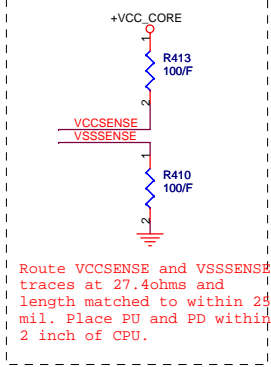
Layout Note:
Place C105 near PIN B26.



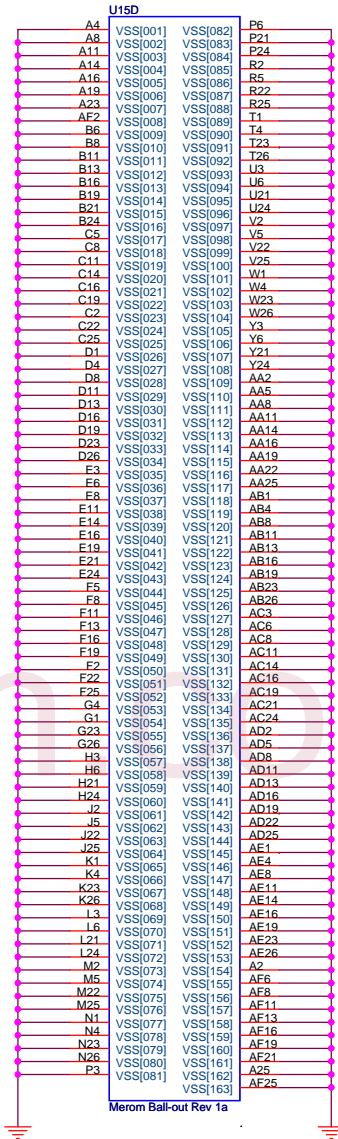
Layout out:
Place these inside socket cavity on North side secondary.

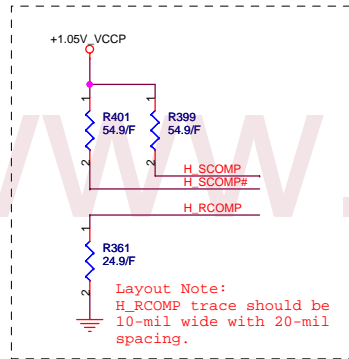
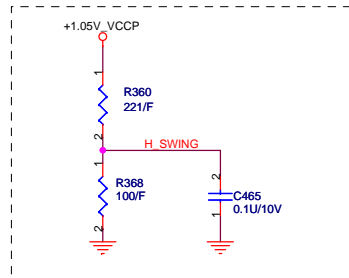


Layout Note:
Need to add 100uF cap on PWR_SRC for cap singing.
Place on PWR_SRC near +VCC_CORE.

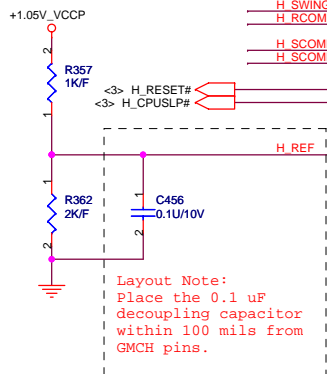


Route VCCSENSE and VSSSENSE traces at 27.4ohms and length matched to within 25 mil. Place PU and PD within 2 inch of CPU.

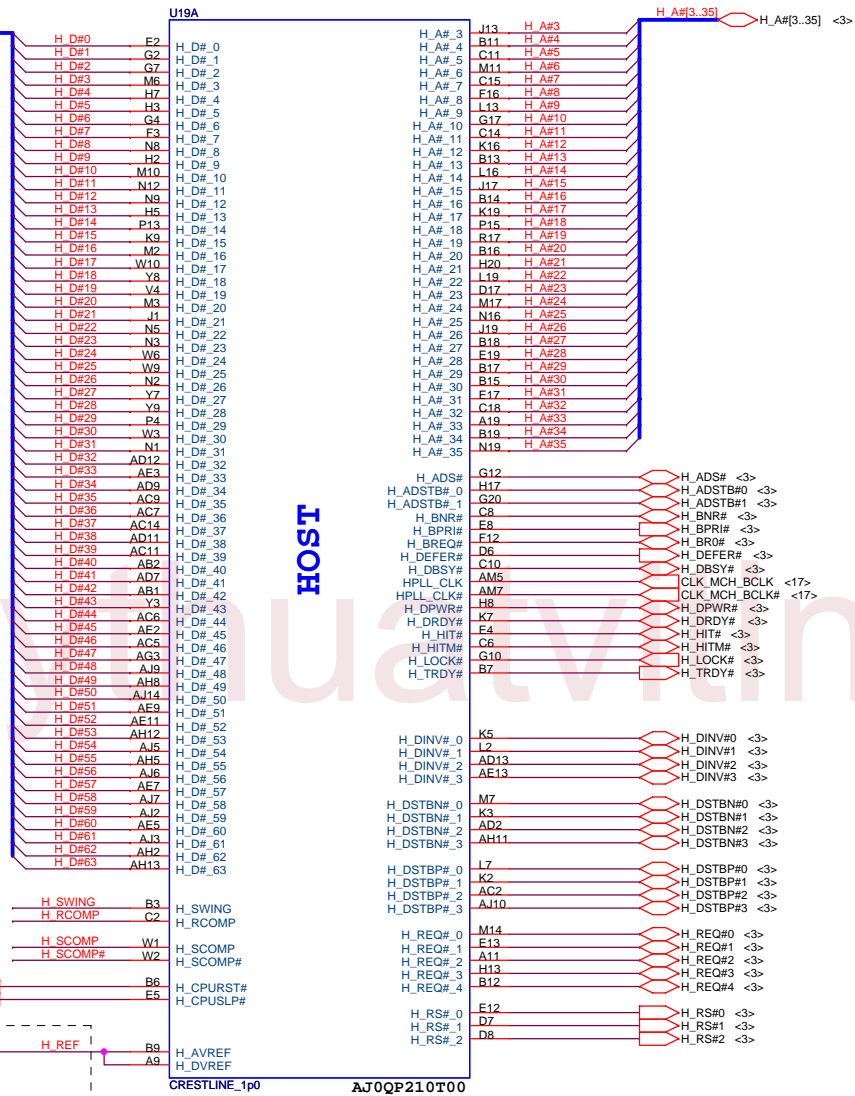


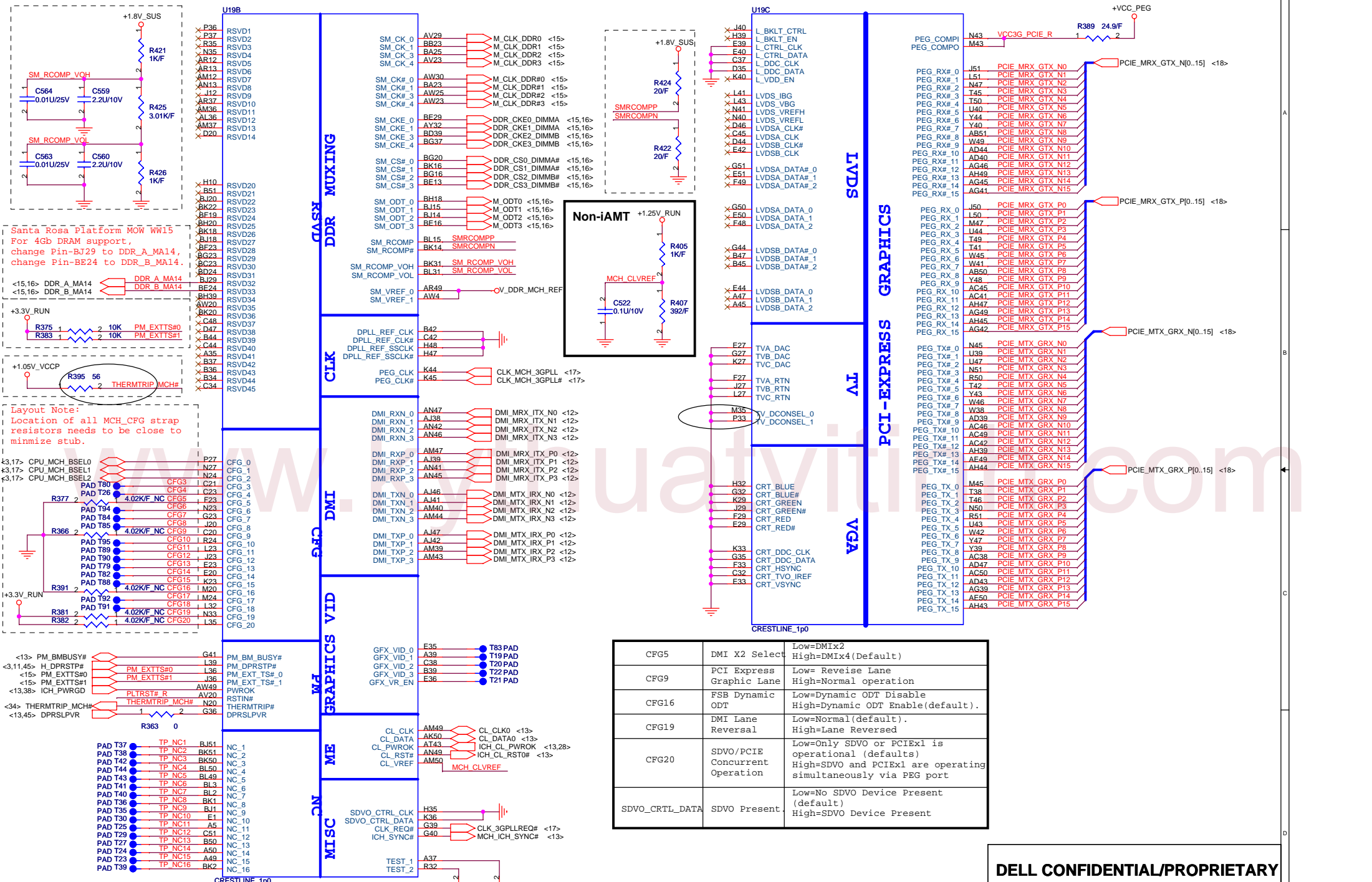


Layout Note:
H_RCOMP trace should be 10-mil wide with 20-mil spacing.



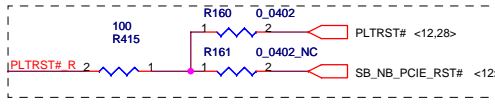
Layout Note:
Place the 0.1 uF decoupling capacitor within 100 mils from GMCH pins.



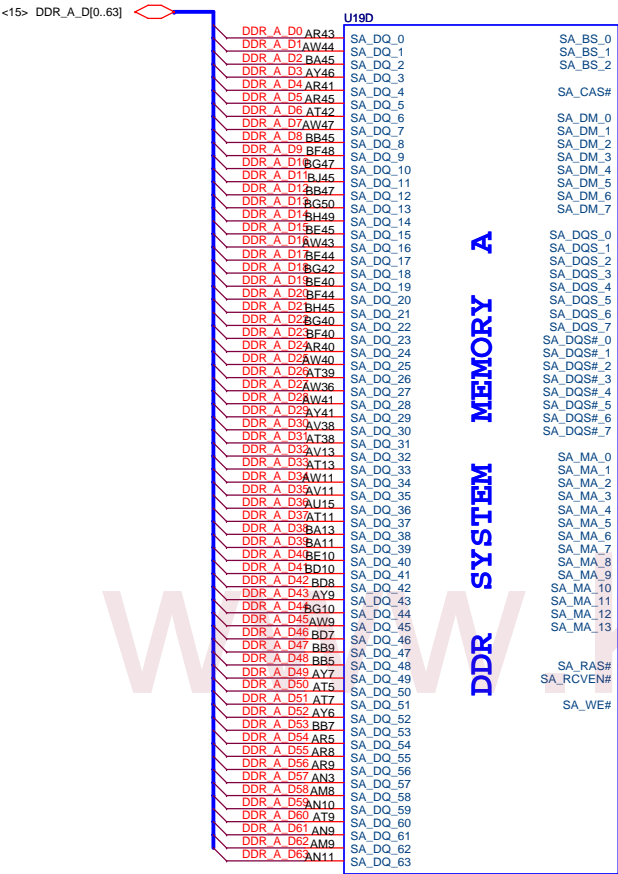


CFG5	DMI X2 Select	Low=DMIx2 High=DMIx4(Default)
CFG9	PCI Express Graphic Lane	Low= Reverse Lane High=Normal operation
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable(default).
CFG19	DMI Lane Reversal	Low=Normal(default). High=Lane Reversed
CFG20	SDVO/PCIE Concurrent Operation	Low=Only SDVO or PCIeEx1 is operational (defaults) High=SDVO and PCIeEx1 are operating simultaneously via PEG port
SDVO_CTRL_DATA	SDVO Present	Low=No SDVO Device Present (default) High=SDVO Device Present

DELL CONFIDENTIAL/PROPRIETARY

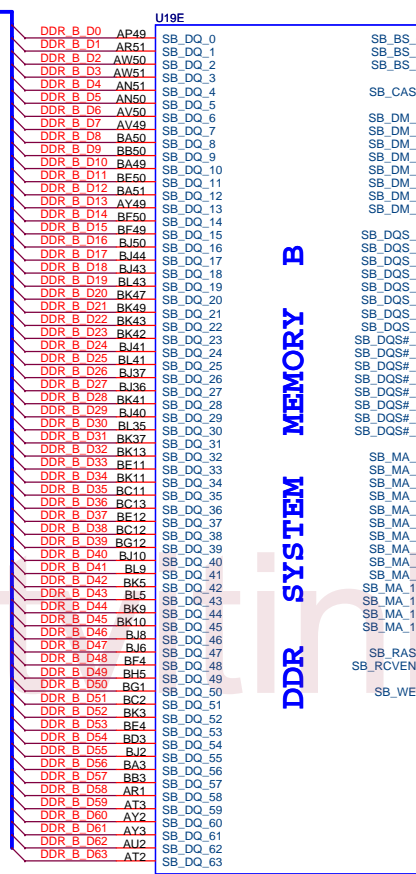


<15> DDR_A_D[0..63]

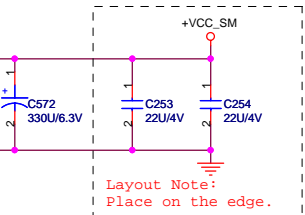
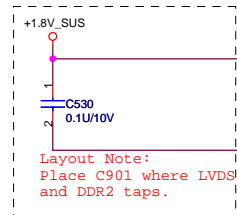
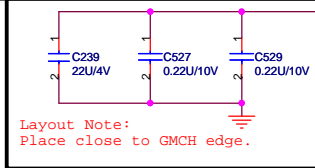
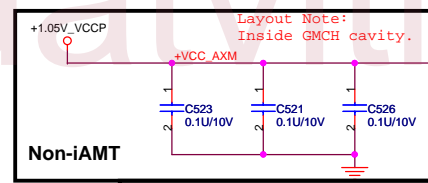
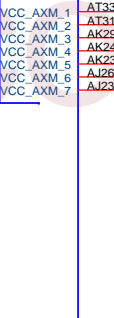
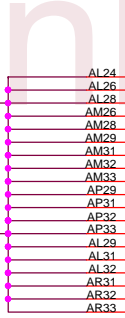
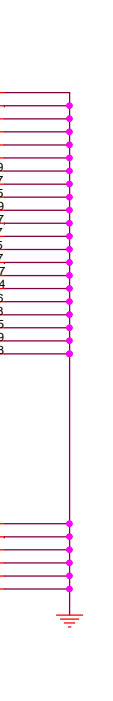
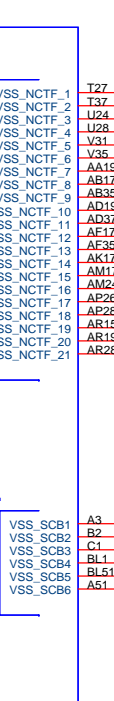
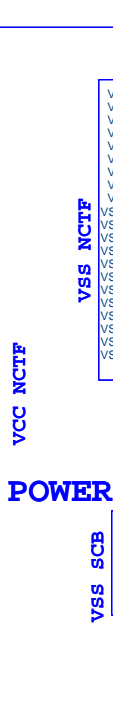
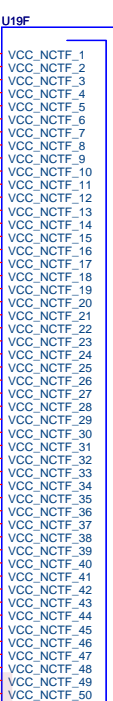
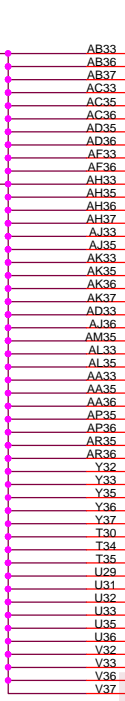
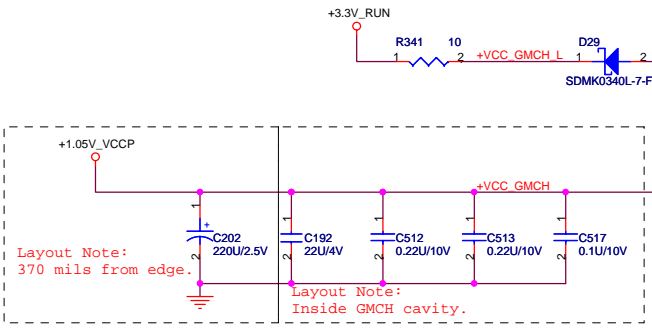
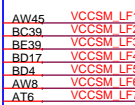
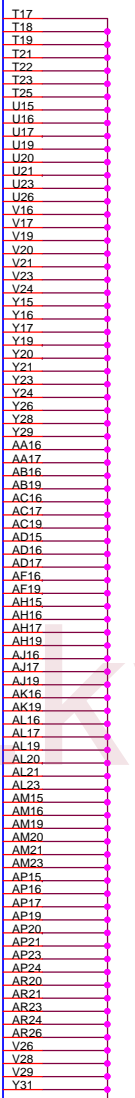
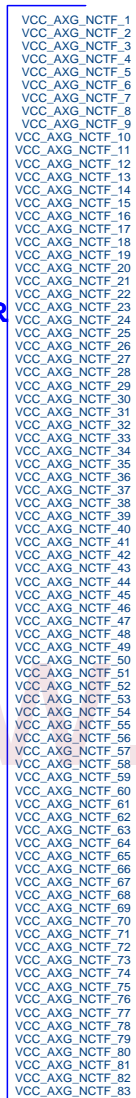
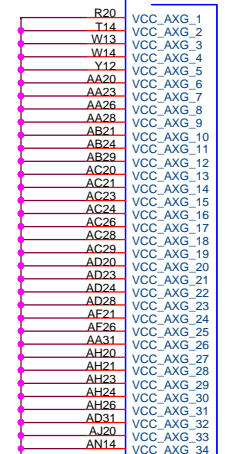
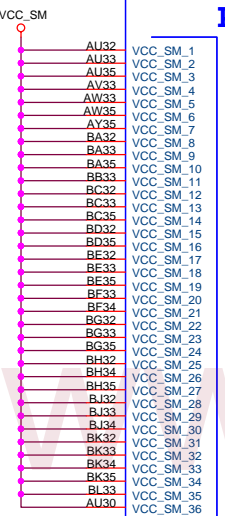
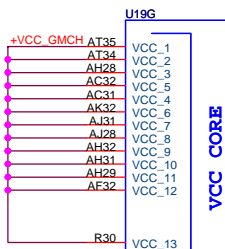


CRESTLINE_1p0

<15> DDR_B_D[0..63]



CRESTLINE_1p0



DELL CONFIDENTIAL/PROPRIETARY

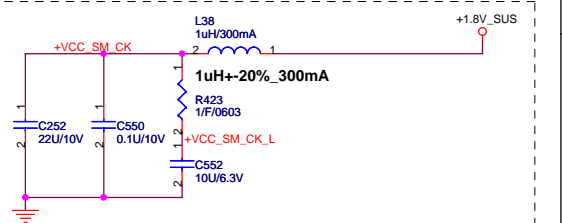
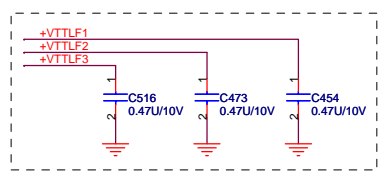
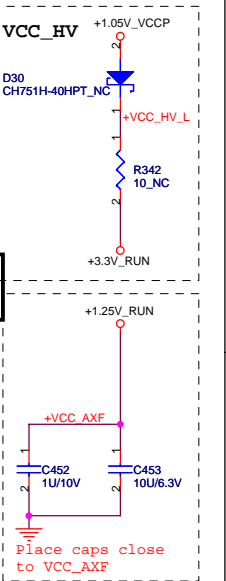
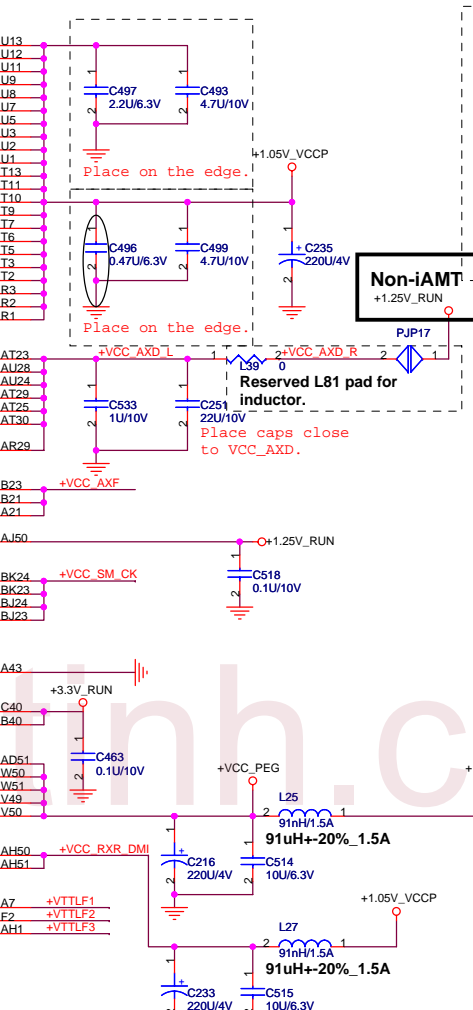
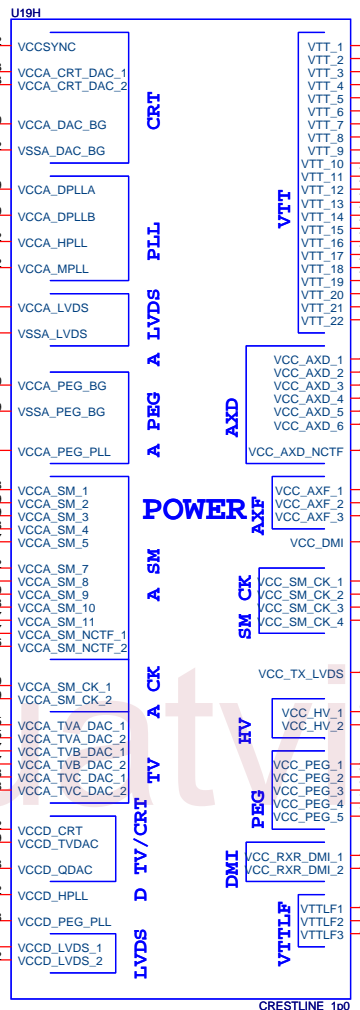
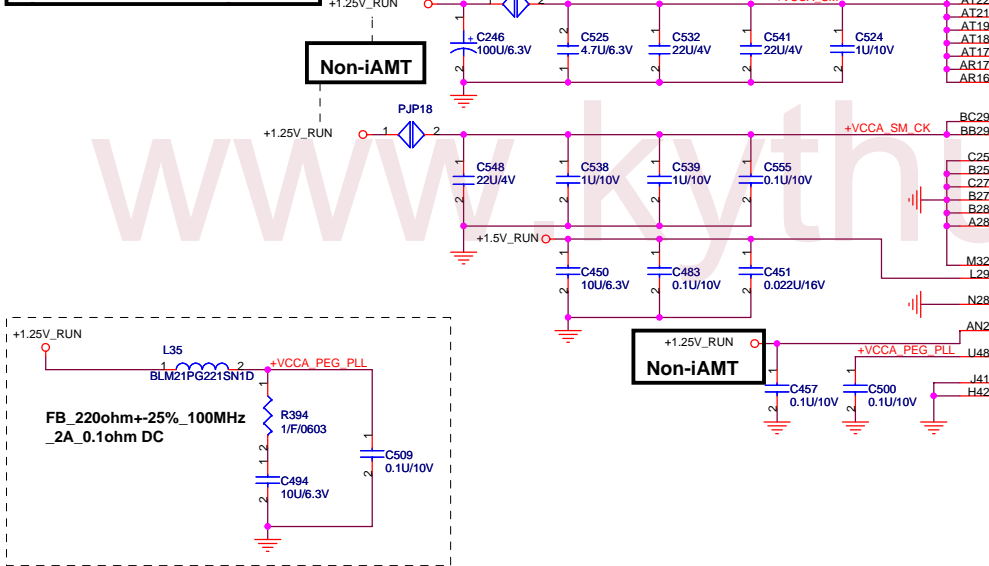
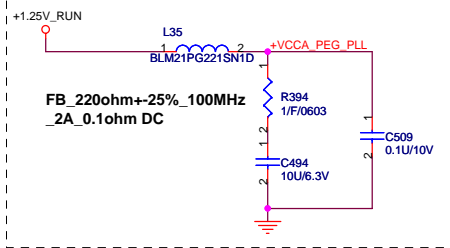
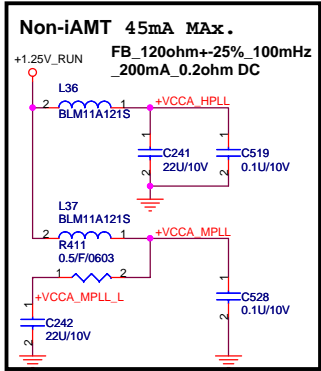
Title
 Crestline (VCC,NCTF)

Size
 Document Number
 M-08

Date
 Monday, March 05, 2007

Rev
 0.1

Sheet
 8 of 51



DELL CONFIDENTIAL/PROPRIETARY		
Title Crestline (POWER)		
Size	Document Number M-08	Rev 0.1
Date:	Monday, March 05, 2007	Sheet 9 of 51

U19I		
A13	VSS_1	VSS_100
A15	VSS_2	VSS_101
A17	VSS_3	VSS_102
A24	VSS_4	VSS_103
AA21	VSS_5	VSS_104
AA24	VSS_6	VSS_105
AA29	VSS_7	VSS_106
AB20	VSS_8	VSS_107
AB23	VSS_9	VSS_108
AB26	VSS_10	VSS_109
AB28	VSS_11	VSS_110
AB31	VSS_12	VSS_111
AC10	VSS_13	VSS_112
AC13	VSS_14	VSS_113
AC3	VSS_15	VSS_114
AC39	VSS_16	VSS_115
AC43	VSS_17	VSS_116
AC47	VSS_18	VSS_117
AD1	VSS_19	VSS_118
AD21	VSS_20	VSS_119
AD26	VSS_21	VSS_120
AD29	VSS_22	VSS_121
AD3	VSS_23	VSS_122
AD41	VSS_24	VSS_123
AD45	VSS_25	VSS_124
AD49	VSS_26	VSS_125
AD5	VSS_27	VSS_126
AD50	VSS_28	VSS_127
AD8	VSS_29	VSS_128
AE10	VSS_30	VSS_129
AE14	VSS_31	VSS_130
AE6	VSS_32	VSS_131
AF20	VSS_33	VSS_132
AF23	VSS_34	VSS_133
AF24	VSS_35	VSS_134
AF31	VSS_36	VSS_135
AG2	VSS_37	VSS_136
AG38	VSS_38	VSS_137
AG43	VSS_39	VSS_138
AG47	VSS_40	VSS_139
AG50	VSS_41	VSS_140
AH3	VSS_42	VSS_141
AH40	VSS_43	VSS_142
AH41	VSS_44	VSS_143
AH7	VSS_45	VSS_144
AH9	VSS_46	VSS_145
AJ11	VSS_47	VSS_146
AJ13	VSS_48	VSS_147
AJ21	VSS_49	VSS_148
AJ24	VSS_50	VSS_149
AJ29	VSS_51	VSS_150
AJ32	VSS_52	VSS_151
AJ34	VSS_53	VSS_152
AJ45	VSS_54	VSS_153
AJ49	VSS_55	VSS_154
AK20	VSS_56	VSS_155
AK21	VSS_57	VSS_156
AK28	VSS_58	VSS_157
AK28	VSS_59	VSS_158
AK31	VSS_60	VSS_159
AK51	VSS_61	VSS_160
AL1	VSS_62	VSS_161
AM11	VSS_63	VSS_162
AM13	VSS_64	VSS_163
AM3	VSS_65	VSS_164
AM4	VSS_66	VSS_165
AM41	VSS_67	VSS_166
AM45	VSS_68	VSS_167
AN1	VSS_69	VSS_168
AN38	VSS_70	VSS_169
AN39	VSS_71	VSS_170
AN43	VSS_72	VSS_171
AN5	VSS_73	VSS_172
AN7	VSS_74	VSS_173
AP4	VSS_75	VSS_174
AP48	VSS_76	VSS_175
AP50	VSS_77	VSS_176
AR11	VSS_78	VSS_177
AR2	VSS_79	VSS_178
AR39	VSS_80	VSS_179
AR44	VSS_81	VSS_180
AR47	VSS_82	VSS_181
AR7	VSS_83	VSS_182
AT10	VSS_84	VSS_183
AT14	VSS_85	VSS_184
AT41	VSS_86	VSS_185
AT49	VSS_87	VSS_186
AU1	VSS_88	VSS_187
AU23	VSS_89	VSS_188
AU29	VSS_90	VSS_189
AU32	VSS_91	VSS_190
AU38	VSS_92	VSS_191
AU49	VSS_93	VSS_192
AU51	VSS_94	VSS_193
AV39	VSS_95	VSS_194
AV48	VSS_96	VSS_195
AW1	VSS_97	VSS_196
AW12	VSS_98	VSS_197
AW16	VSS_99	VSS_198

VSS

CRESTLINE_1p0

U19J		
C46	VSS_199	VSS_287
C50	VSS_200	VSS_288
G7	VSS_201	VSS_289
D13	VSS_202	VSS_290
D24	VSS_203	VSS_291
D3	VSS_204	VSS_292
D32	VSS_205	VSS_293
D38	VSS_206	VSS_294
D45	VSS_207	VSS_295
D49	VSS_208	VSS_296
E10	VSS_209	VSS_297
E16	VSS_210	VSS_298
E24	VSS_211	VSS_299
E28	VSS_212	VSS_300
E32	VSS_213	VSS_301
E47	VSS_214	VSS_302
F19	VSS_215	VSS_303
F36	VSS_216	VSS_304
F4	VSS_217	VSS_305
F40	VSS_218	
F50	VSS_219	
G1	VSS_220	
G13	VSS_221	VSS_306
G16	VSS_222	VSS_307
G19	VSS_223	VSS_308
G24	VSS_224	VSS_309
G28	VSS_225	VSS_310
G29	VSS_226	VSS_311
G33	VSS_227	VSS_312
G42	VSS_228	VSS_313
G45	VSS_229	
G48	VSS_230	
G8	VSS_231	
H24	VSS_232	
H28	VSS_233	
H4	VSS_234	
H45	VSS_235	
H11	VSS_236	
J16	VSS_237	
J2	VSS_238	
J24	VSS_239	
J28	VSS_240	
J33	VSS_241	
J35	VSS_242	
J39	VSS_243	
K12	VSS_245	
K47	VSS_246	
K8	VSS_247	
L1	VSS_248	
L17	VSS_249	
L20	VSS_250	
L24	VSS_251	
L28	VSS_252	
L3	VSS_253	
L33	VSS_254	
L49	VSS_255	
M28	VSS_256	
M42	VSS_257	
M46	VSS_258	
M49	VSS_259	
M5	VSS_260	
M50	VSS_261	
M9	VSS_262	
N11	VSS_263	
N14	VSS_264	
N17	VSS_265	
N29	VSS_266	
N32	VSS_267	
N36	VSS_268	
N39	VSS_269	
N44	VSS_270	
N49	VSS_271	
N7	VSS_272	
P19	VSS_273	
P2	VSS_274	
P23	VSS_275	
P3	VSS_276	
P50	VSS_277	
R49	VSS_278	
T38	VSS_279	
T43	VSS_280	
T47	VSS_281	
U41	VSS_282	
U45	VSS_283	
U50	VSS_284	
VL11	VSS_285	
V2	VSS_286	
V3	VSS_286	

VSS

CRESTLINE_1p0

W11	VSS_287
W39	VSS_288
W43	VSS_289
W47	VSS_290
W5	VSS_291
W7	VSS_292
Y13	VSS_293
Y2	VSS_294
Y41	VSS_295
Y45	VSS_296
Y49	VSS_297
Y5	VSS_298
Y50	VSS_299
Y11	VSS_300
P29	VSS_301
T29	VSS_302
T31	VSS_303
T33	VSS_304
R28	VSS_305
AA32	VSS_306
AB32	VSS_307
AD32	VSS_308
AE28	VSS_309
AF29	VSS_310
AT27	VSS_311
AV25	VSS_312
H50	VSS_313

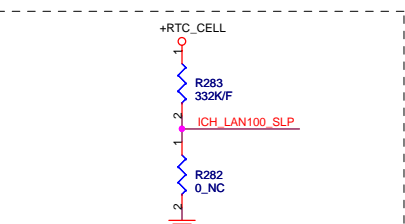
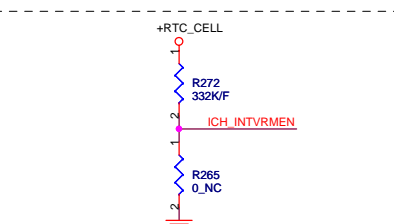
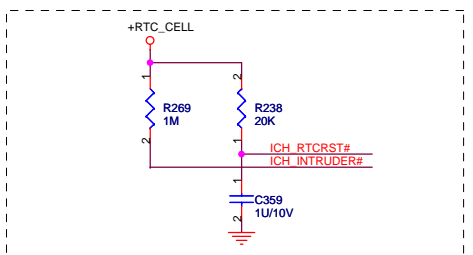
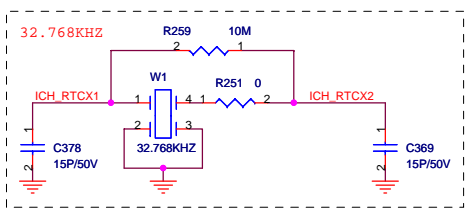


DELL CONFIDENTIAL/PROPRIETARY

Title: Crestline (VSS)

Size: Document Number M-08 Rev 0.1

Date: Monday, March 05, 2007 Sheet 10 of 51

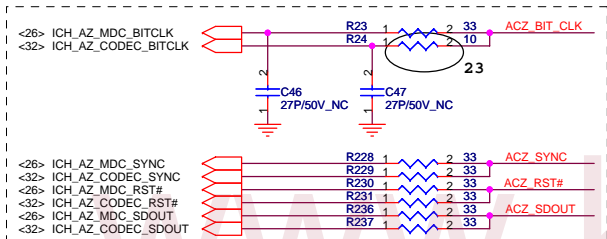


ICH8M Internal VR Enable Strap
(Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)

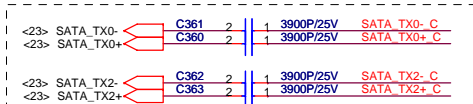
ICH_INTVRMEN	Low = Internal VR Disabled
	High = Internal VR Enabled(Default)

ICH8M LAN100 SLP Strap
(Internal VR for VccLAN1.05 and VccCL1.05)

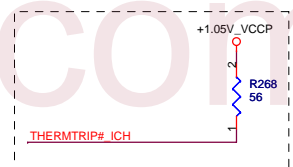
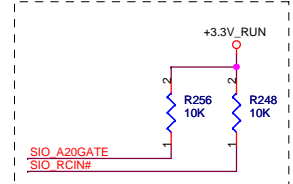
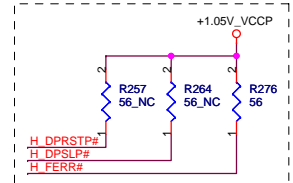
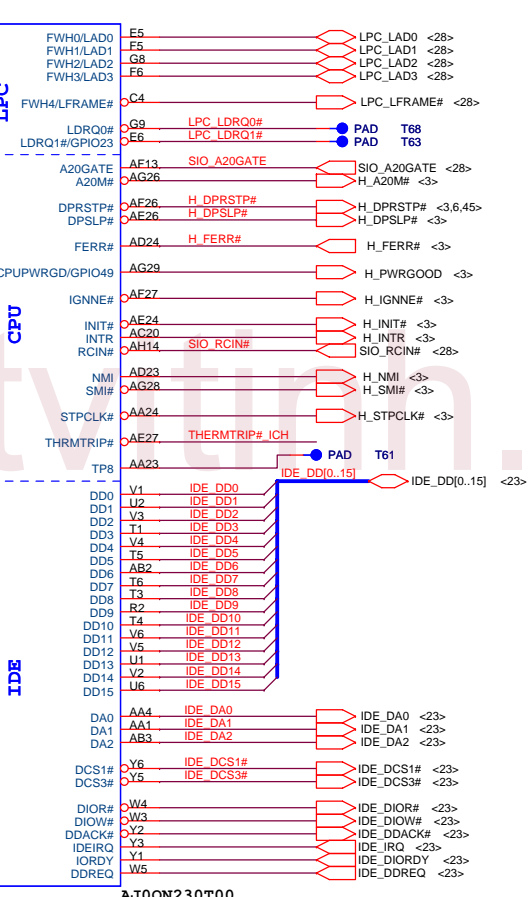
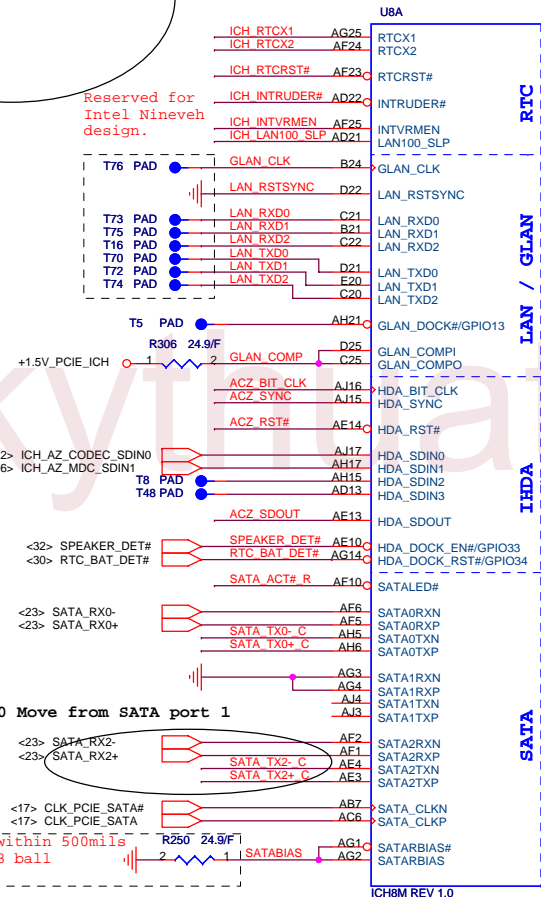
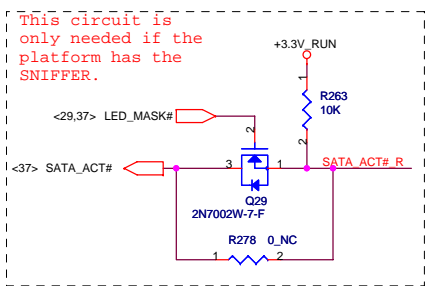
ICH_LAN100_SLP	Low = Internal VR Disabled
	High = Internal VR Enabled(Default)



Place all series terms close to ICH8 except for SDIN input lines, which should be close to source. Placement of R23, R228, R230 & R236 should equal distance to the T split trace point as R24, R229, R231 & R237 respective. Basically, keep the same distance from T for all series termination resistors.



Distance between the ICH-8 M and cap on the "P" signal should be identical distance between the ICH-6 M and cap on the "N" signal for same pair.



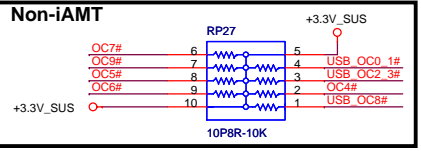
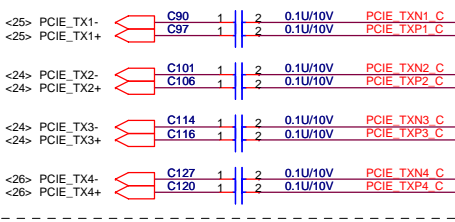
9/20 Move from SATA port 1

Place within 500mils of ICH8 ball

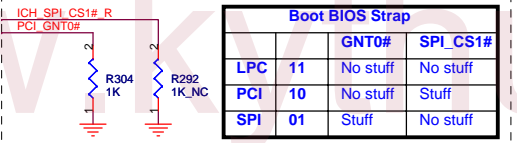
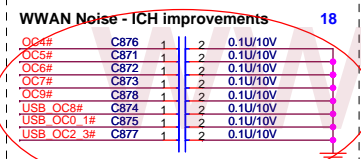
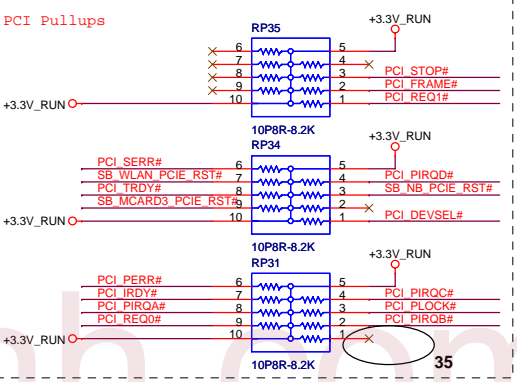
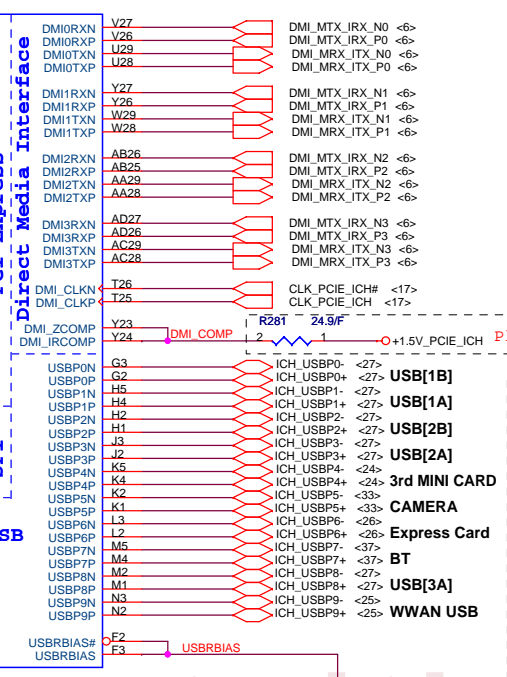
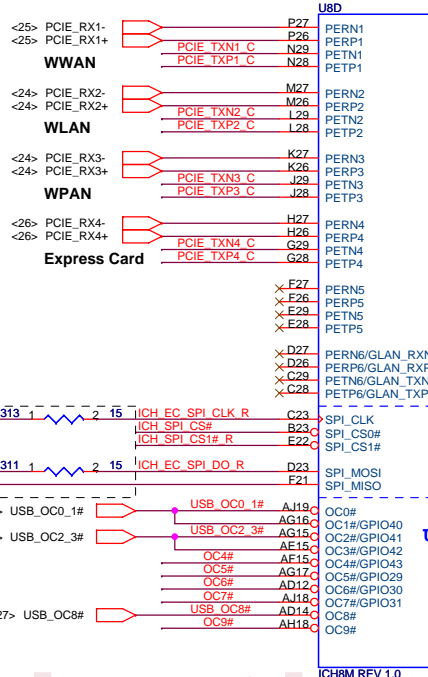
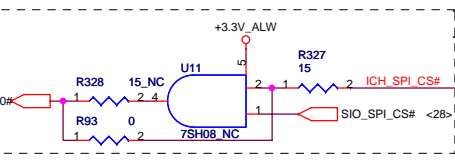
XOR Chain Entrance Strap

ICH_RSVD	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1

Place TX DC blocking caps close ICH8.



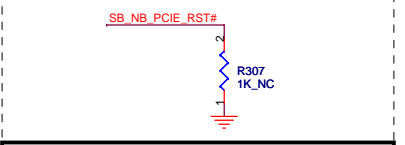
Layout Note:
Place R313, R311 and R327 within 500 mils from ICH8.



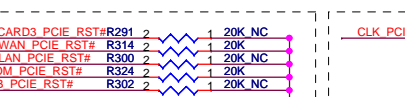
Boot BIOS Strap			
	GNT0#	SPI_CS1#	
LPC	11	No stuff	No stuff
PCI	10	No stuff	Stuff
SPI	01	Stuff	No stuff

Short F2 and F3 at the package and keep length to less than 500mils. Trace Impedance should be 60ohms +/- 15%.

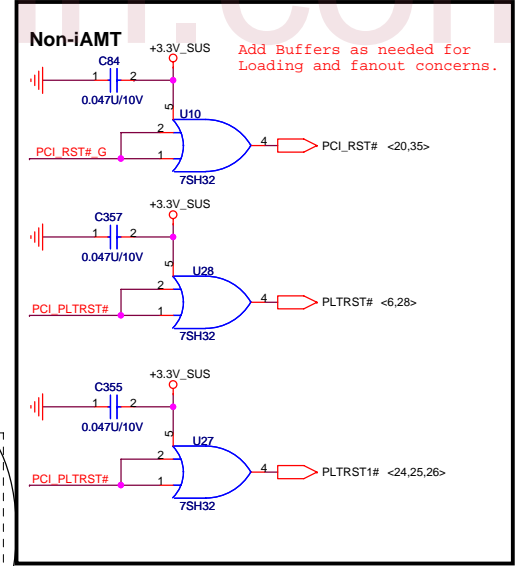
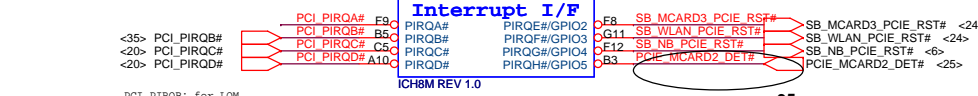
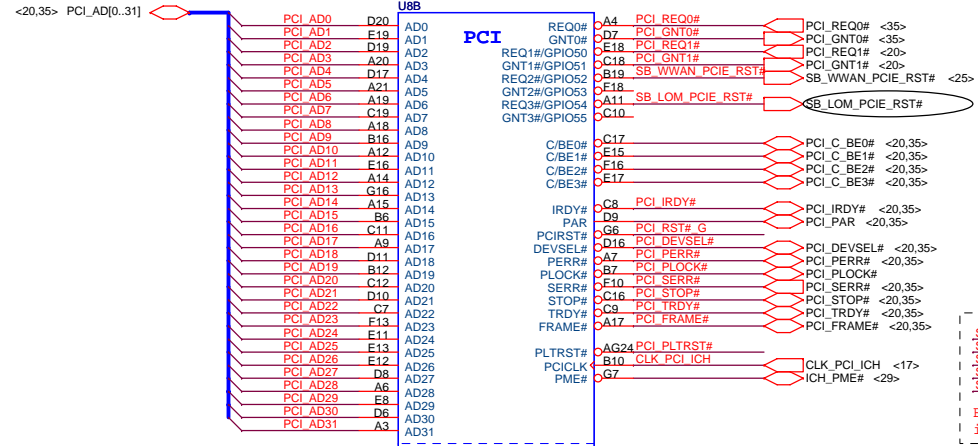
LOM	REQ0	GNT0	PIRQB
1394/MediaCard	REQ1	GNT1	PIRQC



A16 away override strap.
Low = A16 swap override enabled.
High = Default.



BIOS should not enable the internal GPIO pull up resistor.

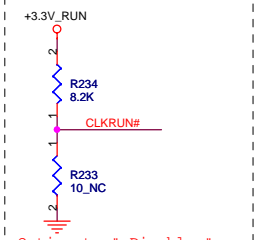
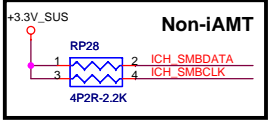
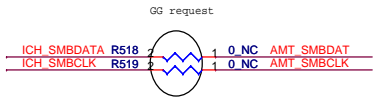


Reserved for EMV. Place resistors and cap close to ICH8.

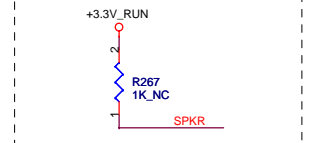
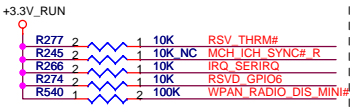
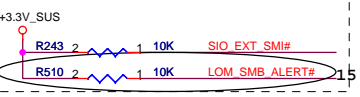
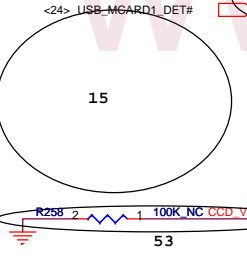
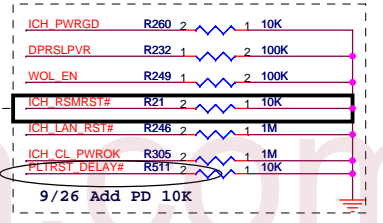
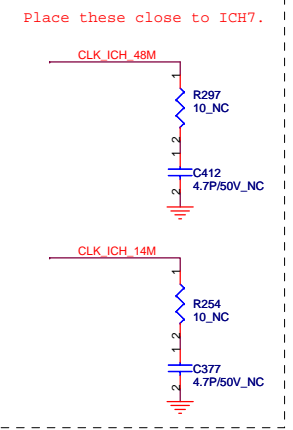
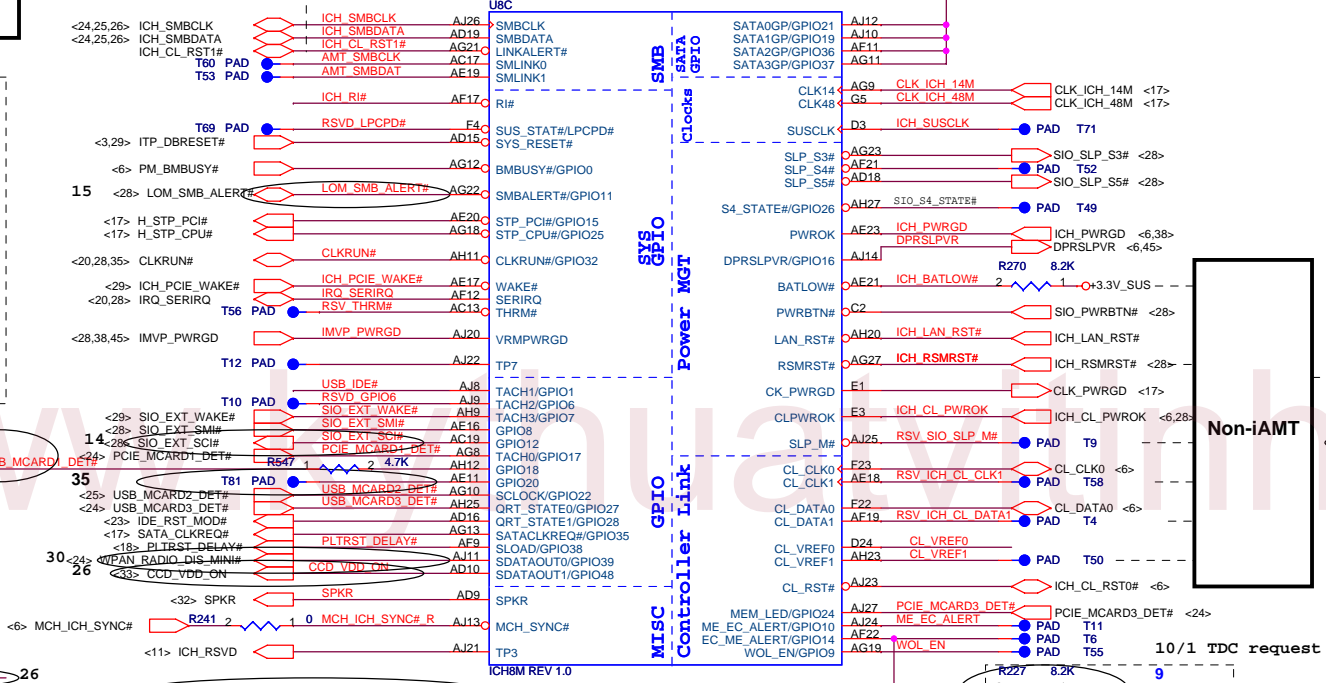
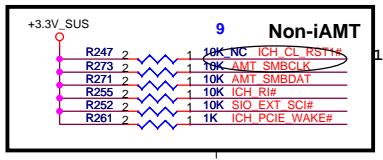
PCI_PIRQB: for LOM
PCI_PIRQC: for Media Card
PCI_PIRQD: for 1394

DELL CONFIDENTIAL/PROPRIETARY

Title ICH8-M (USB,DMI,PCIE,PCI)		
Size	Document Number M-08	Rev 0.1
Date:	Tuesday, March 06, 2007	Sheet 12 of 51

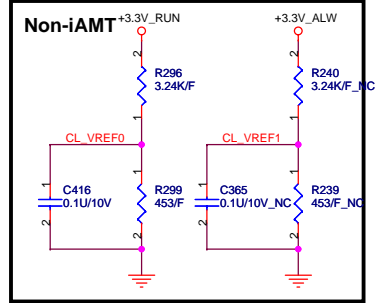
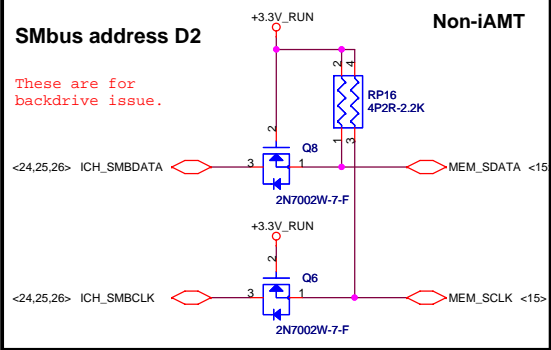


Option to "Disable" clkrun. Pulling it down will keep the clks running.



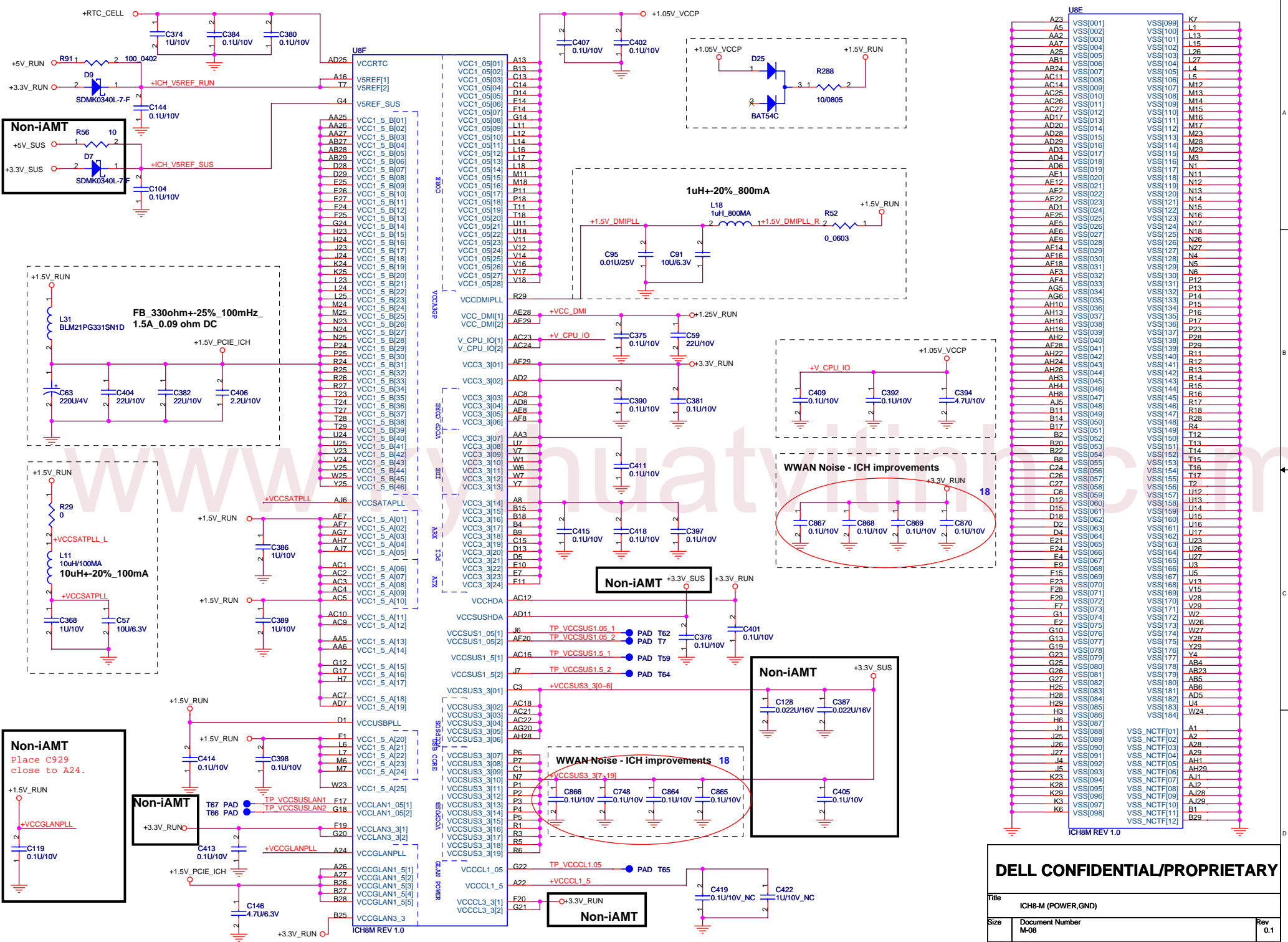
No Reboot strap.
SPKR Low = Default. High = No Reboot.

9/20 Delete R258



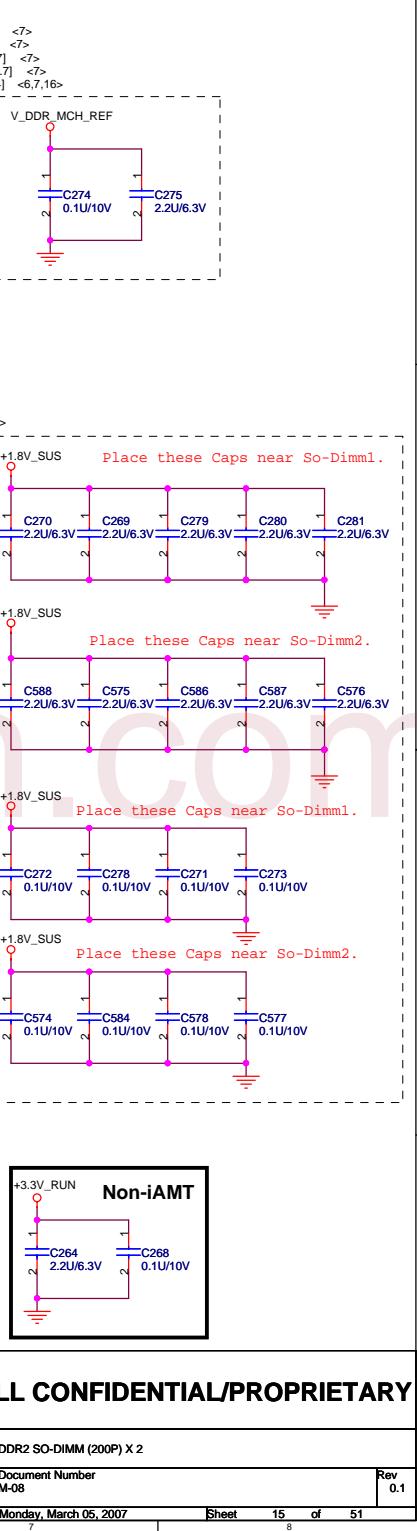
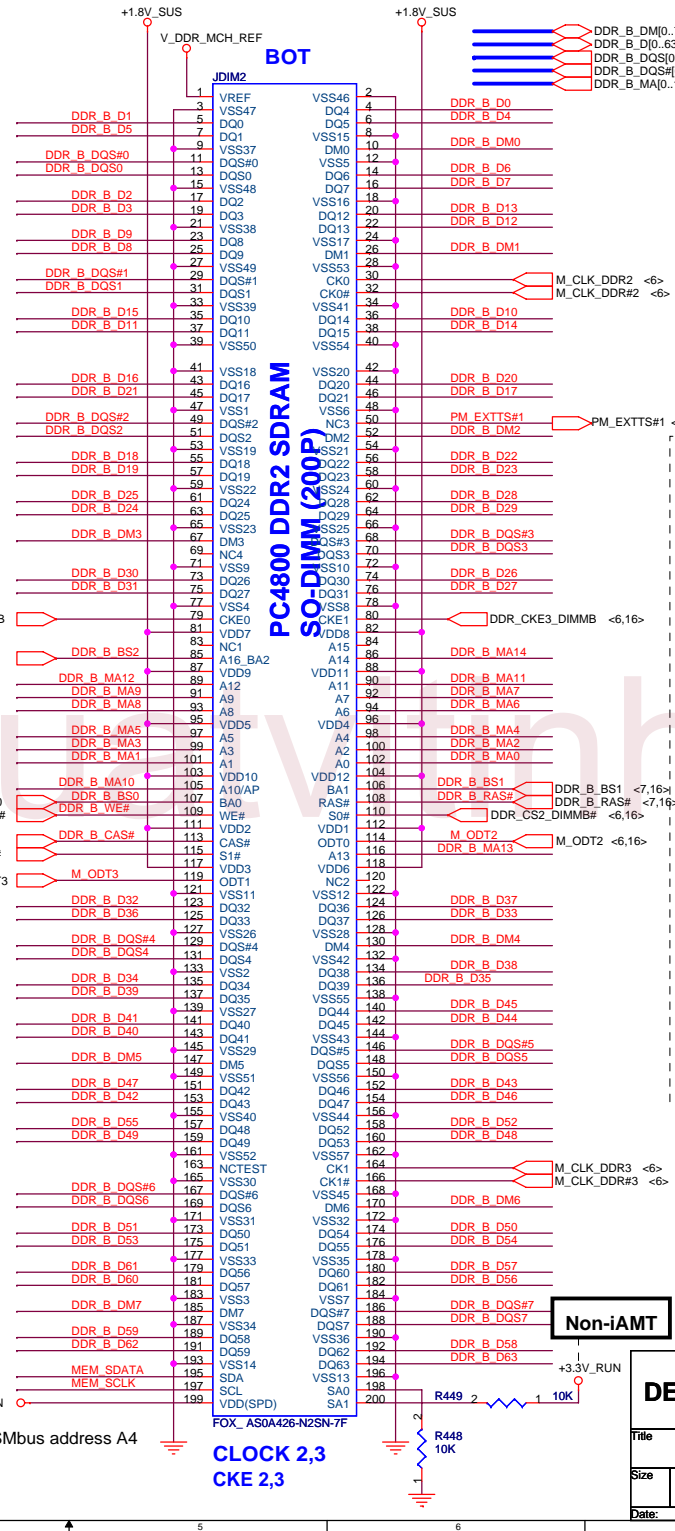
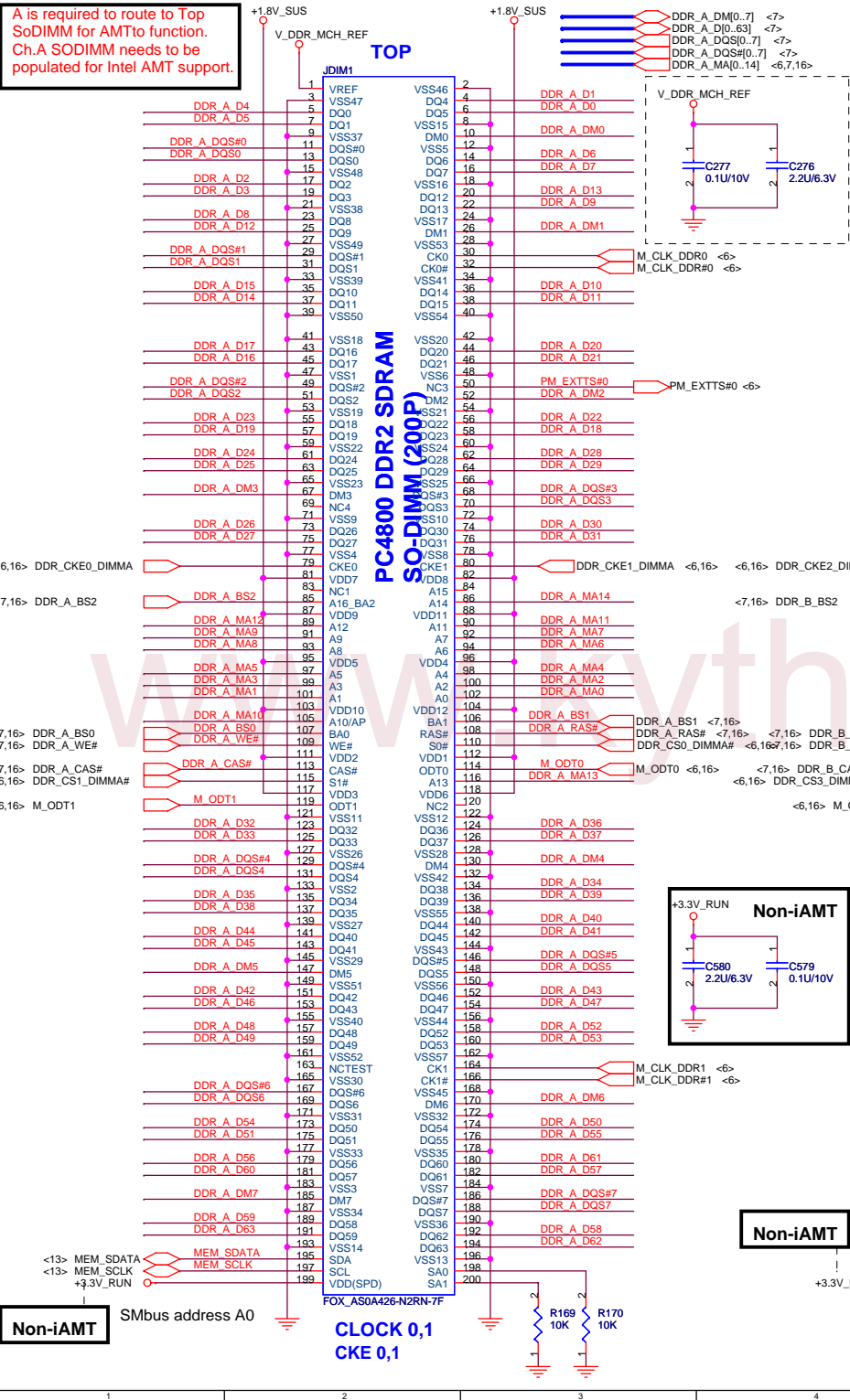
DELL CONFIDENTIAL/PROPRIETARY

Title		
ICH8-M (PM,GPIO,SMB,CL)		
Size	Document Number	Rev
M-08		0.1
Date:	Tuesday, March 06, 2007	Sheet 13 of 51

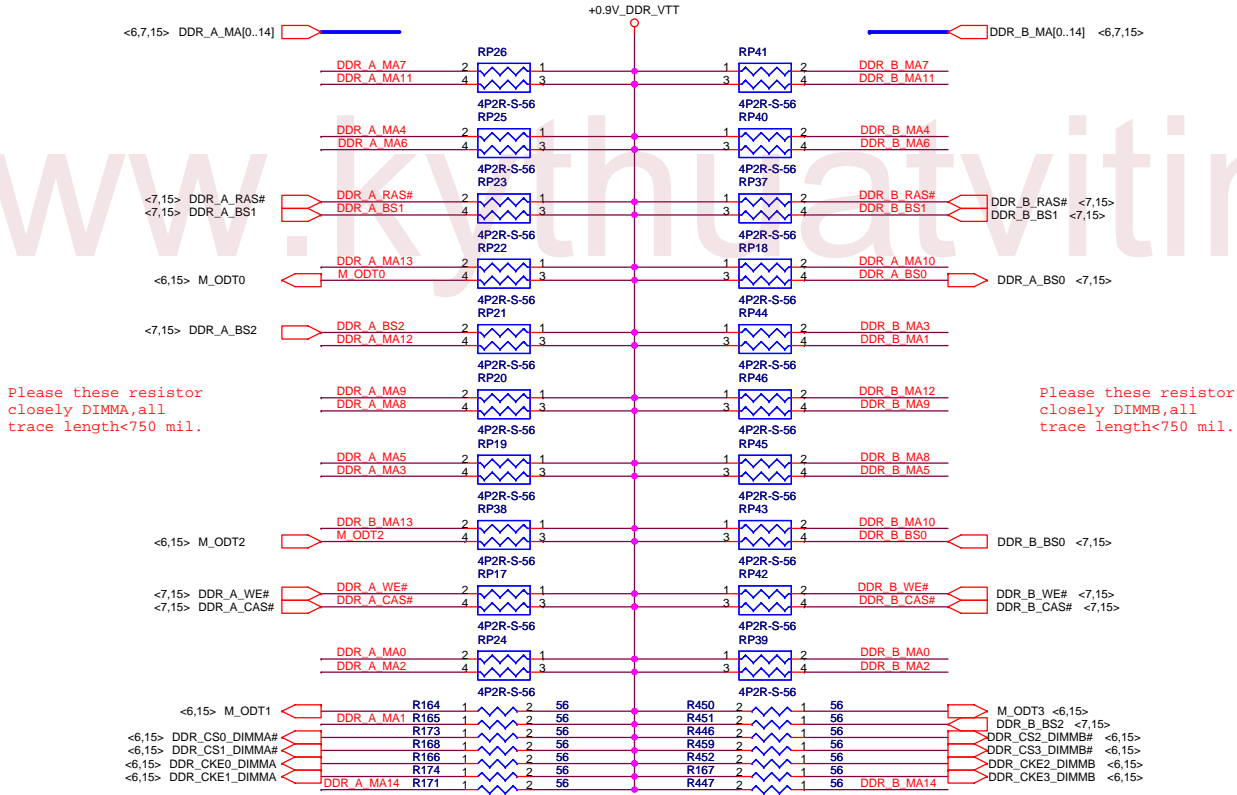
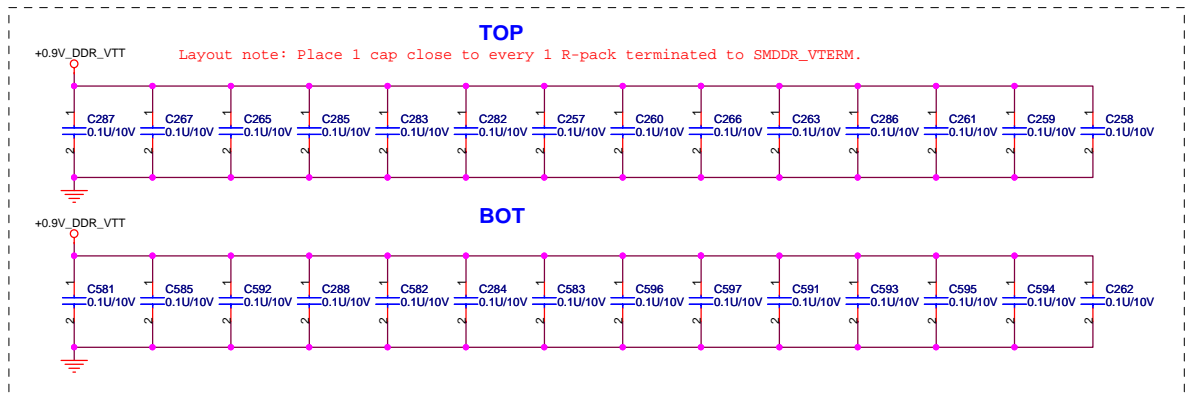


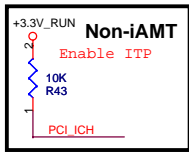
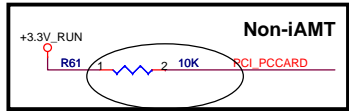
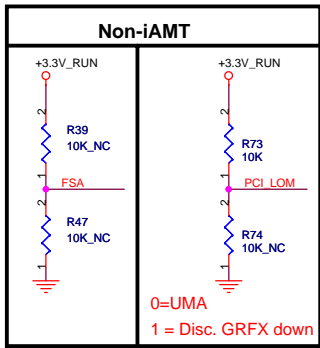
U8E		
A23	VSS[001]	VSS[099]
A5	VSS[002]	VSS[100]
AA2	VSS[003]	VSS[101]
AA7	VSS[004]	VSS[102]
A25	VSS[005]	VSS[103]
AB1	VSS[006]	VSS[104]
AB24	VSS[007]	VSS[105]
AC11	VSS[008]	VSS[106]
AC14	VSS[009]	VSS[107]
AC25	VSS[010]	VSS[108]
AC26	VSS[011]	VSS[109]
AC27	VSS[012]	VSS[110]
AD17	VSS[013]	VSS[111]
AD20	VSS[014]	VSS[112]
AD28	VSS[015]	VSS[113]
AD29	VSS[016]	VSS[114]
AD3	VSS[017]	VSS[115]
AD4	VSS[018]	VSS[116]
AD6	VSS[019]	VSS[117]
AE1	VSS[020]	VSS[118]
AE12	VSS[021]	VSS[119]
AE2	VSS[022]	VSS[120]
AE22	VSS[023]	VSS[121]
AD1	VSS[024]	VSS[122]
AE25	VSS[025]	VSS[123]
AE5	VSS[026]	VSS[124]
AE6	VSS[027]	VSS[125]
AE9	VSS[028]	VSS[126]
AF14	VSS[029]	VSS[127]
AF16	VSS[030]	VSS[128]
AF18	VSS[031]	VSS[129]
AF3	VSS[032]	VSS[130]
AF4	VSS[033]	VSS[131]
AG5	VSS[034]	VSS[132]
AG6	VSS[035]	VSS[133]
AH10	VSS[036]	VSS[134]
AH13	VSS[037]	VSS[135]
AH16	VSS[038]	VSS[136]
AH19	VSS[039]	VSS[137]
AH2	VSS[040]	VSS[138]
AE28	VSS[041]	VSS[139]
AH22	VSS[042]	VSS[140]
AH24	VSS[043]	VSS[141]
AH26	VSS[044]	VSS[142]
AH3	VSS[045]	VSS[143]
AH4	VSS[046]	VSS[144]
AH8	VSS[047]	VSS[145]
AJ5	VSS[048]	VSS[146]
B11	VSS[049]	VSS[147]
B14	VSS[050]	VSS[148]
B17	VSS[051]	VSS[149]
B2	VSS[052]	VSS[150]
B20	VSS[053]	VSS[151]
B22	VSS[054]	VSS[152]
B8	VSS[055]	VSS[153]
C24	VSS[056]	VSS[154]
C26	VSS[057]	VSS[155]
C27	VSS[058]	VSS[156]
C6	VSS[059]	VSS[157]
D12	VSS[060]	VSS[158]
D18	VSS[061]	VSS[159]
D2	VSS[062]	VSS[160]
D4	VSS[063]	VSS[161]
D18	VSS[064]	VSS[162]
E21	VSS[065]	VSS[163]
E24	VSS[066]	VSS[164]
E4	VSS[067]	VSS[165]
E9	VSS[068]	VSS[166]
F15	VSS[069]	VSS[167]
F23	VSS[070]	VSS[168]
F28	VSS[071]	VSS[169]
F29	VSS[072]	VSS[170]
F7	VSS[073]	VSS[171]
G1	VSS[074]	VSS[172]
G2	VSS[075]	VSS[173]
G10	VSS[076]	VSS[174]
G13	VSS[077]	VSS[175]
G19	VSS[078]	VSS[176]
G23	VSS[079]	VSS[177]
G25	VSS[080]	VSS[178]
G26	VSS[081]	VSS[179]
G27	VSS[082]	VSS[180]
H25	VSS[083]	VSS[181]
H28	VSS[084]	VSS[182]
H29	VSS[085]	VSS[183]
H3	VSS[086]	VSS[184]
H6	VSS[087]	VSS[185]
J1	VSS[088]	VSS[186]
J25	VSS[089]	VSS[187]
J26	VSS[090]	VSS[188]
J27	VSS[091]	VSS[189]
J4	VSS[092]	VSS[190]
J5	VSS[093]	VSS[191]
K23	VSS[094]	VSS[192]
K28	VSS[095]	VSS[193]
K29	VSS[096]	VSS[194]
K3	VSS[097]	VSS[195]
K6	VSS[098]	VSS[196]
K7	VSS[099]	VSS[197]
L1	VSS[100]	VSS[198]
L13	VSS[101]	VSS[199]
L15	VSS[102]	VSS[200]
L26	VSS[103]	VSS[201]
L7	VSS[104]	VSS[202]
L4	VSS[105]	VSS[203]
L5	VSS[106]	VSS[204]
M12	VSS[107]	VSS[205]
M13	VSS[108]	VSS[206]
M14	VSS[109]	VSS[207]
M15	VSS[110]	VSS[208]
M16	VSS[111]	VSS[209]
M17	VSS[112]	VSS[210]
M23	VSS[113]	VSS[211]
M28	VSS[114]	VSS[212]
M29	VSS[115]	VSS[213]
M3	VSS[116]	VSS[214]
N1	VSS[117]	VSS[215]
N11	VSS[118]	VSS[216]
N12	VSS[119]	VSS[217]
N13	VSS[120]	VSS[218]
N14	VSS[121]	VSS[219]
N15	VSS[122]	VSS[220]
N16	VSS[123]	VSS[221]
N17	VSS[124]	VSS[222]
N18	VSS[125]	VSS[223]
N26	VSS[126]	VSS[224]
N27	VSS[127]	VSS[225]
N4	VSS[128]	VSS[226]
N5	VSS[129]	VSS[227]
N6	VSS[130]	VSS[228]
P12	VSS[131]	VSS[229]
P14	VSS[132]	VSS[230]
P15	VSS[133]	VSS[231]
P16	VSS[134]	VSS[232]
P17	VSS[135]	VSS[233]
P23	VSS[136]	VSS[234]
P28	VSS[137]	VSS[235]
P29	VSS[138]	VSS[236]
R11	VSS[139]	VSS[237]
R12	VSS[140]	VSS[238]
R13	VSS[141]	VSS[239]
R14	VSS[142]	VSS[240]
R15	VSS[143]	VSS[241]
R16	VSS[144]	VSS[242]
R17	VSS[145]	VSS[243]
R18	VSS[146]	VSS[244]
R28	VSS[147]	VSS[245]
R4	VSS[148]	VSS[246]
T12	VSS[149]	VSS[247]
T13	VSS[150]	VSS[248]
T14	VSS[151]	VSS[249]
T15	VSS[152]	VSS[250]
T16	VSS[153]	VSS[251]
T17	VSS[154]	VSS[252]
T2	VSS[155]	VSS[253]
U12	VSS[156]	VSS[254]
U13	VSS[157]	VSS[255]
U14	VSS[158]	VSS[256]
U15	VSS[159]	VSS[257]
U16	VSS[160]	VSS[258]
U17	VSS[161]	VSS[259]
U23	VSS[162]	VSS[260]
U26	VSS[163]	VSS[261]
U27	VSS[164]	VSS[262]
U3	VSS[165]	VSS[263]
U5	VSS[166]	VSS[264]
U13	VSS[167]	VSS[265]
V15	VSS[168]	VSS[266]
V28	VSS[169]	VSS[267]
W2	VSS[170]	VSS[268]
W2	VSS[171]	VSS[269]
W26	VSS[172]	VSS[270]
W27	VSS[173]	VSS[271]
W28	VSS[174]	VSS[272]
W29	VSS[175]	VSS[273]
W2	VSS[176]	VSS[274]
Y4	VSS[177]	VSS[275]
AB4	VSS[178]	VSS[276]
AB23	VSS[179]	VSS[277]
AB5	VSS[180]	VSS[278]
AB6	VSS[181]	VSS[279]
AD5	VSS[182]	VSS[280]
U4	VSS[183]	VSS[281]
W24	VSS[184]	VSS[282]
A1	VSS[185]	VSS[283]
A2	VSS[186]	VSS[284]
A29	VSS[187]	VSS[285]
AH1	VSS[188]	VSS[286]
AH29	VSS[189]	VSS[287]
A11	VSS[190]	VSS[288]
A12	VSS[191]	VSS[289]
A28	VSS[192]	VSS[290]
A29	VSS[193]	VSS[291]
B1	VSS[194]	VSS[292]
B29	VSS[195]	VSS[293]

A is required to route to Top SoDIMM for AMTto function. Ch.A SODIMM needs to be populated for Intel AMT support.

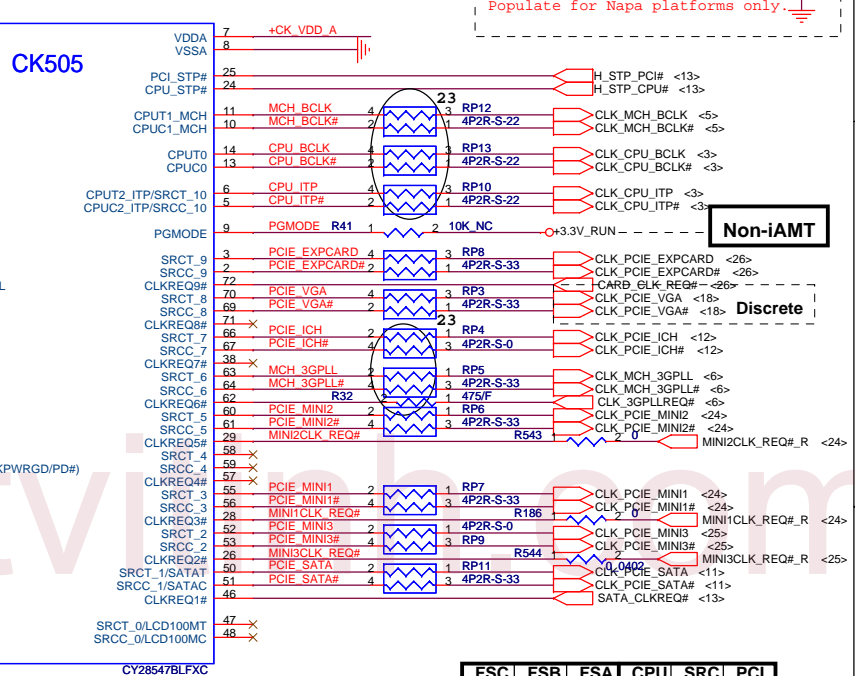
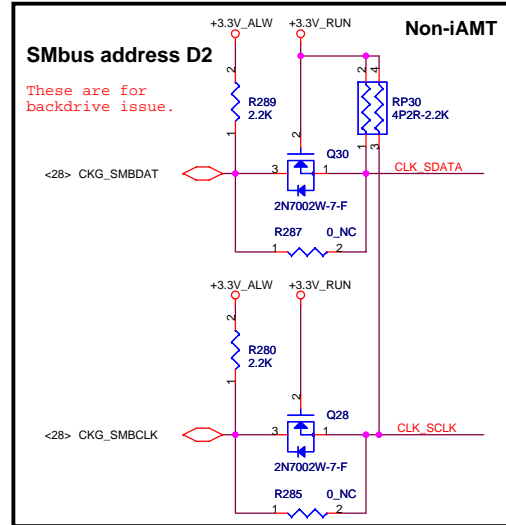
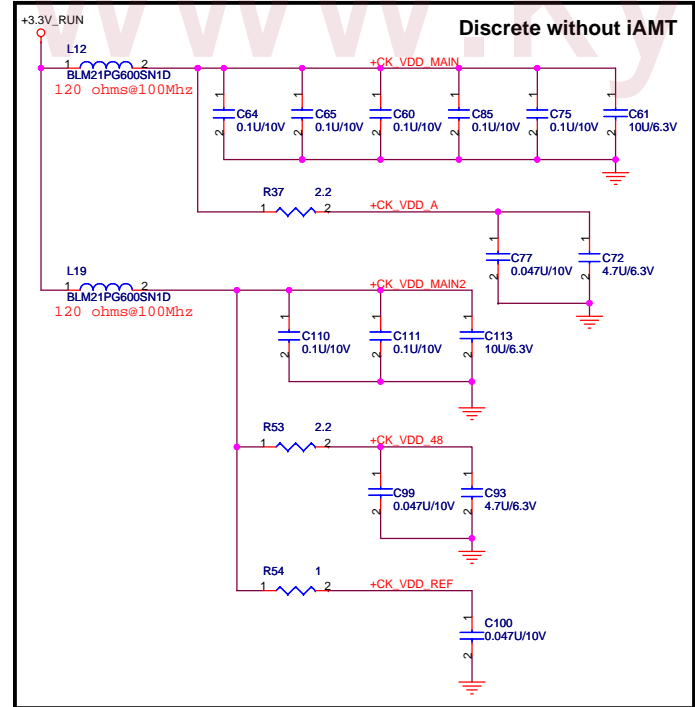
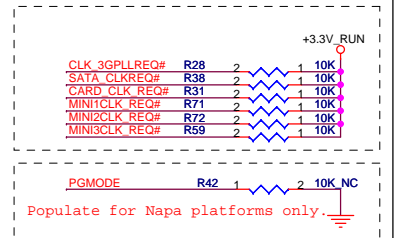
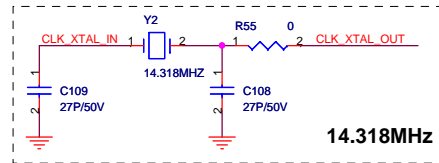
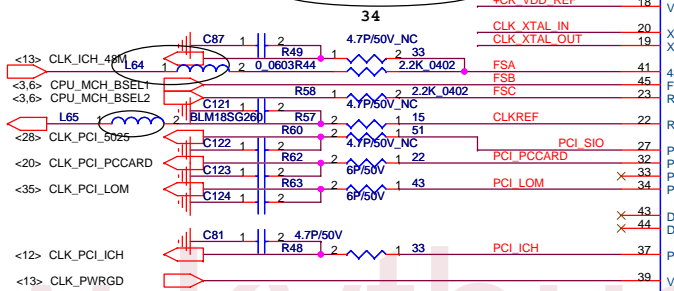


DELL CONFIDENTIAL/PROPRIETARY		
Title	DDR2 SO-DIMM (200P) X 2	
Size	Document Number	Rev
	M-08	0.1
Date:	Monday, March 05, 2007	Sheet 15 of 51





<3,6> CPU_MCH_BSEL0
<3,6> CPU_MCH_BSEL1
<3,6> CPU_MCH_BSEL2
<13> CLK_ICH_14M
<13> CLK_ICH_14M
BK1005LL330
CX5LL330000



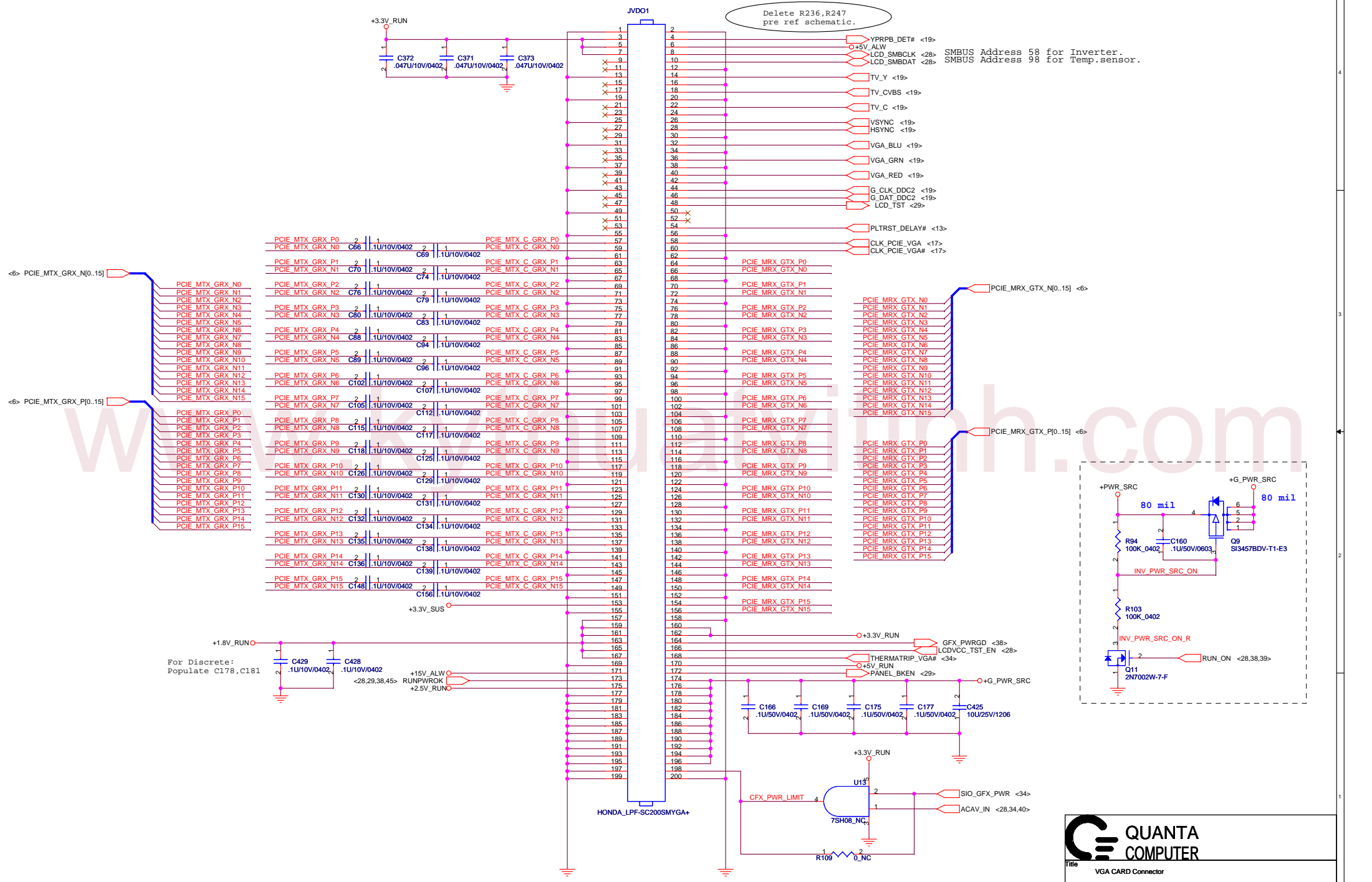
FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

PCI_LOM = FCTSEL1

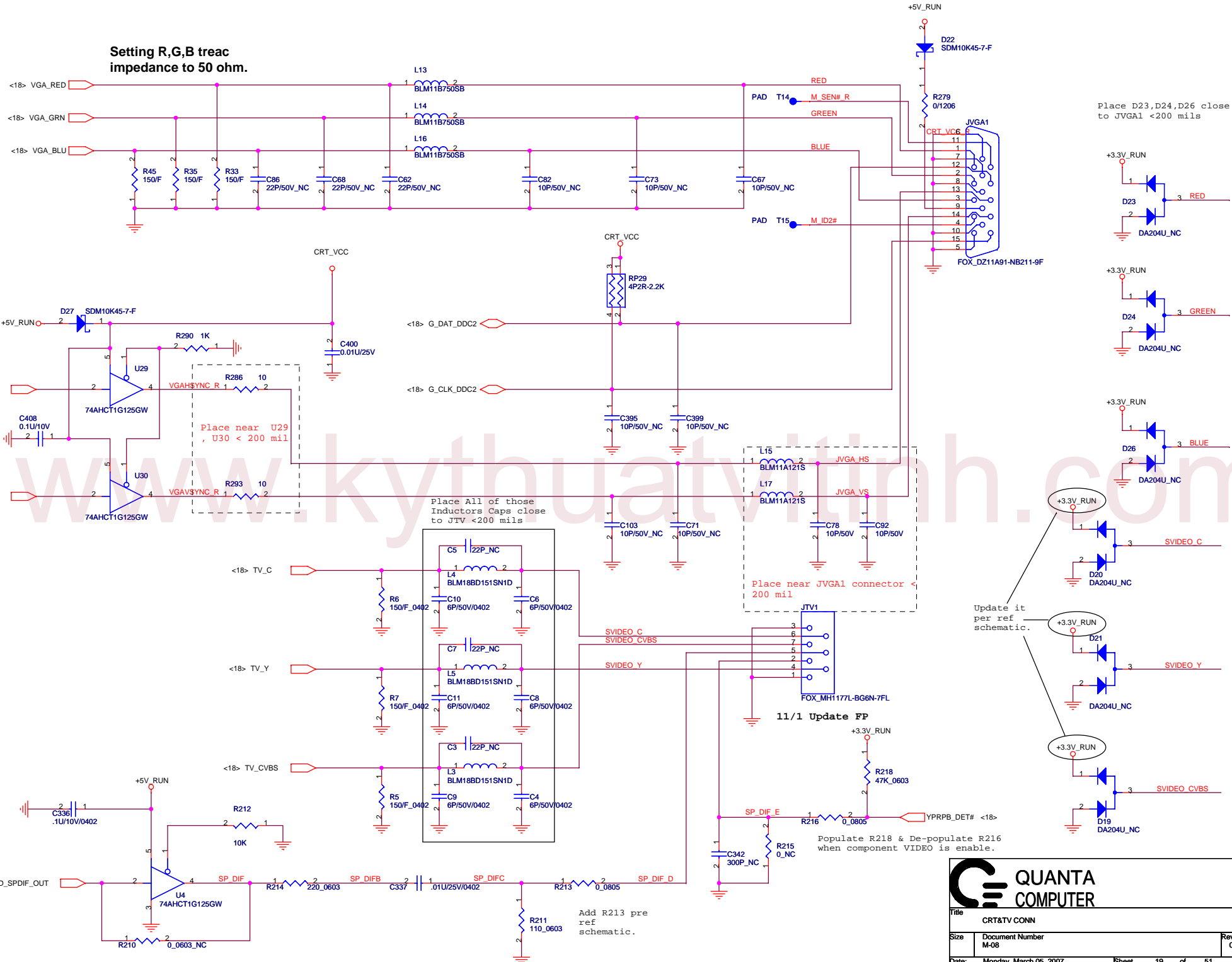
FCTSEL1 (PIN34)	PIN43	PIN44	PIN47	PIN48
0=UMA	DOT96T	DOT96C	96/100M_T	96/100M_C
1 = Disc. GRFX down	27Mout	27MSSout	SRCT0	SRCC0

YPRPB_DET: SIGNAL FROM SVIDEO CONNECTOR,
TO SWITCH TO COMPONENT OUT.

Delete R236,R247
pre ref schematic.



Setting R,G,B treac impedance to 50 ohm.



Place D23,D24,D26 close to JVG A1 <200 mils

Place near U29 , U30 < 200 mil

Place All of those Inductors Caps close to JTV <200 mils

Place near JVG A1 connector < 200 mil

Update it per ref schematic.

Populate R218 & De-populate R216 when component VIDEO is enable.

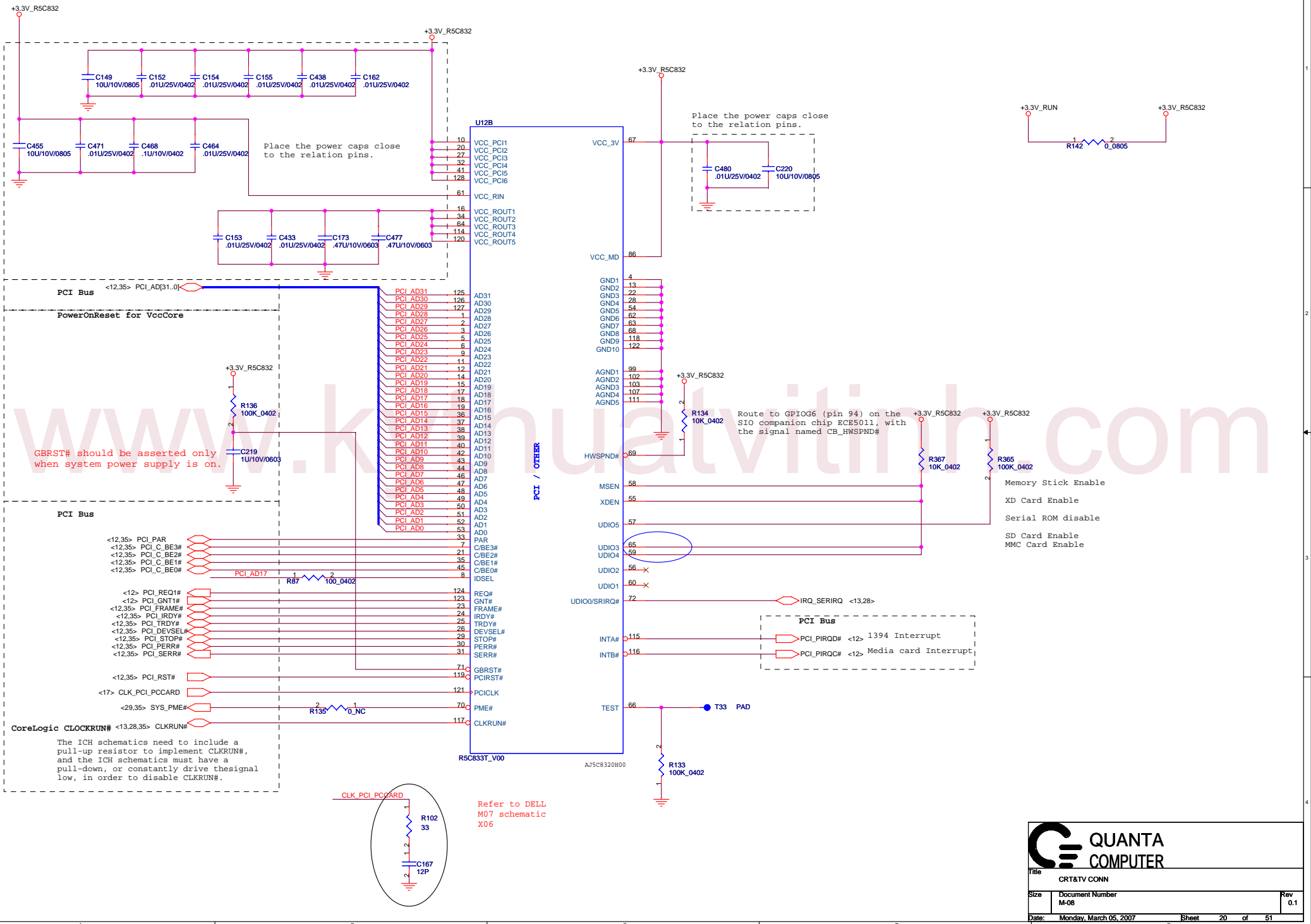
Add R213 pre ref schematic.

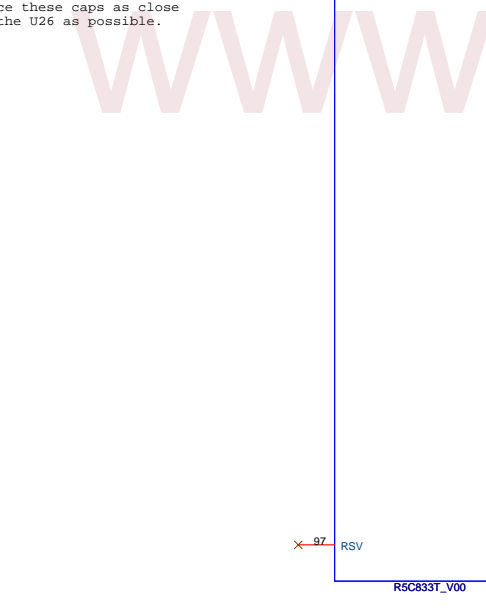
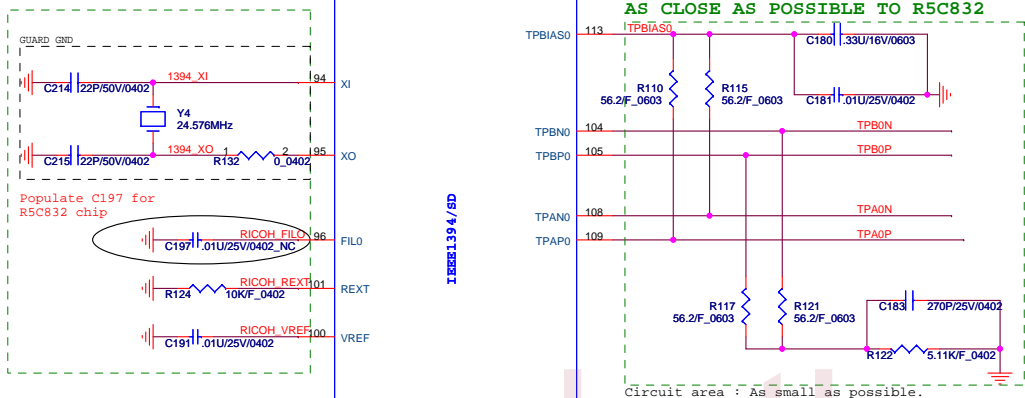
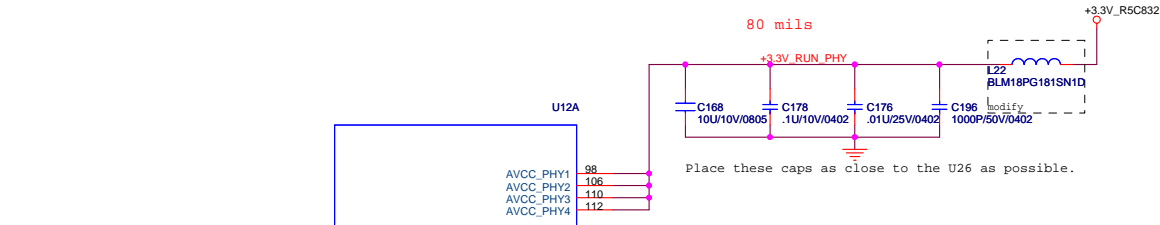
QUANTA COMPUTER

Title: CRT&TV CONN

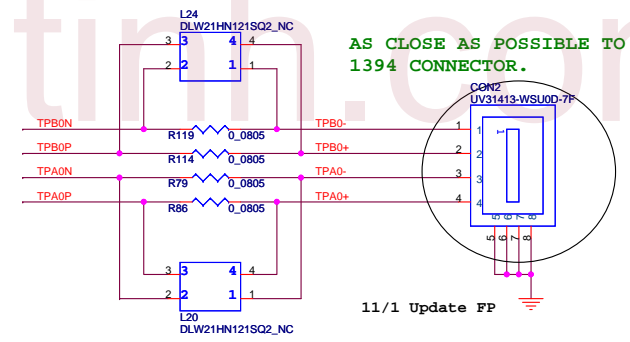
Size: M-08	Document Number: M-08	Rev: 0.1
------------	-----------------------	----------

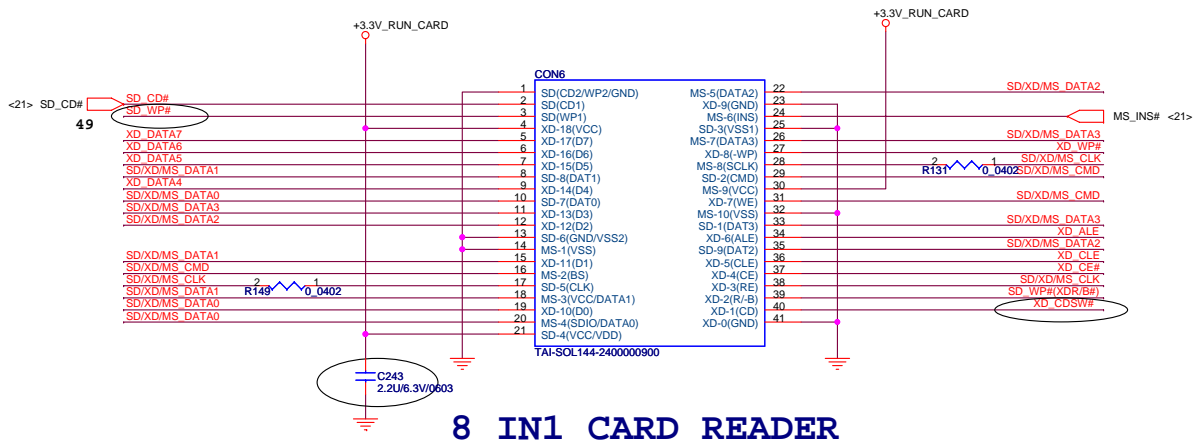
Date: Monday, March 05, 2007 Sheet 19 of 51



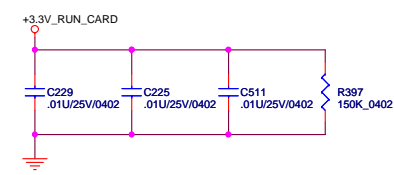


*TPA0P/TPA0N,TPB0P/TPB0N pair trace : As close as possible.
*TPA0P/TPA0N,TPB0P/TPB0N pair trace : Same length electrically.
*Termination resistor for TPA+/- TPB+/- : As close as possible to its cable driver (device pin out).

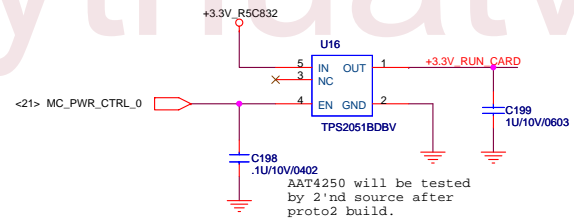




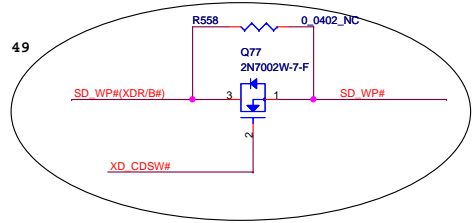
8 IN1 CARD READER



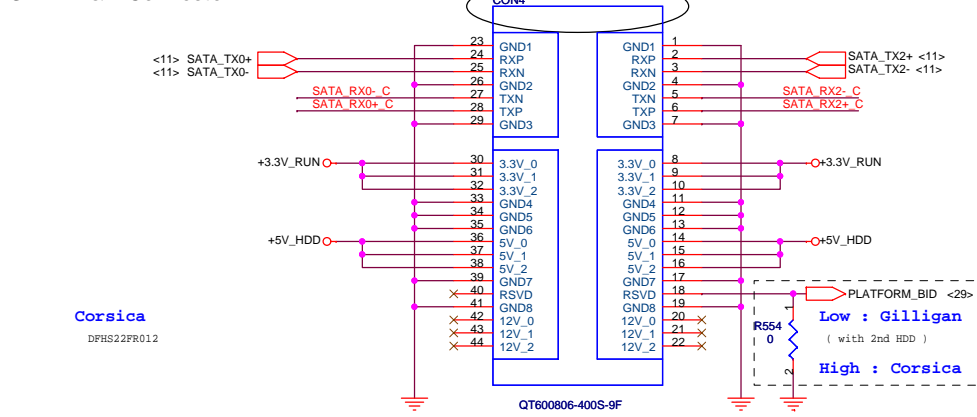
- <21> XD_CDSW#
- <21> SD_WP#(XDR/B#)
- <21> XD_DATA7
- <21> XD_DATA6
- <21> XD_DATA5
- <21> XD_DATA4
- <21> SD/XD/MS_DATA3
- <21> SD/XD/MS_DATA2
- <21> SD/XD/MS_DATA1
- <21> SD/XD/MS_DATA0
- <21> SD/XD/MS_CMD
- <21> XD_WP#
- <21> XD_ALE
- <21> XD_CLE
- <21> XD_CE#
- <21> SD/XD/MS_CLK



SD Protect

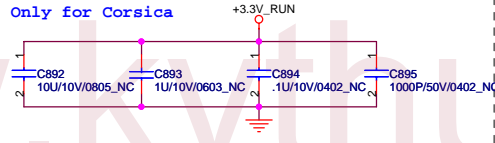
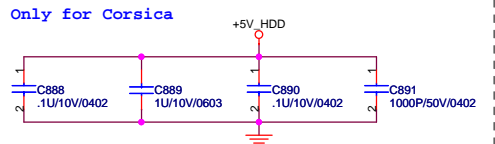
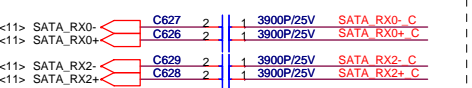


SATA 1 & 2 Connector.

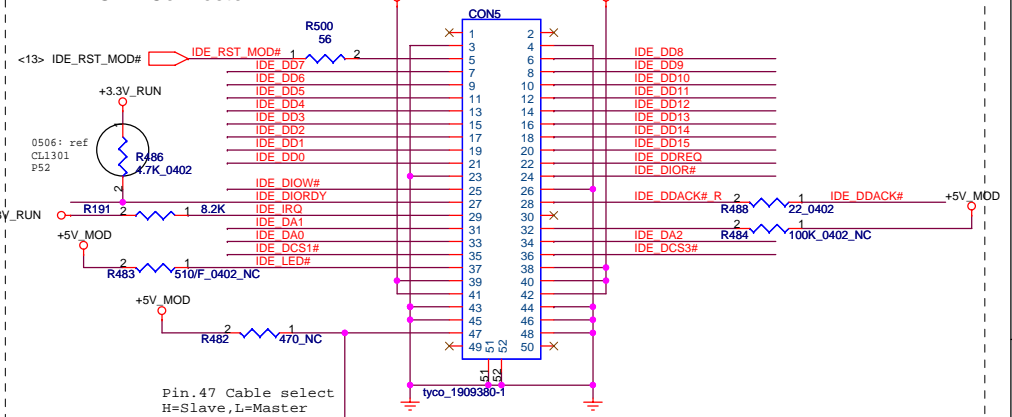


Place close to connector side

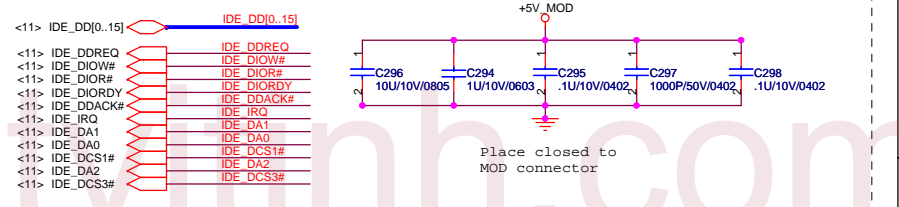
Locate caps C626, C627, C628, C629 near HDD Conn. Length match SATA_C_RX0- & SATA_C_RX0+ within 0 mils.



ODD Connector.

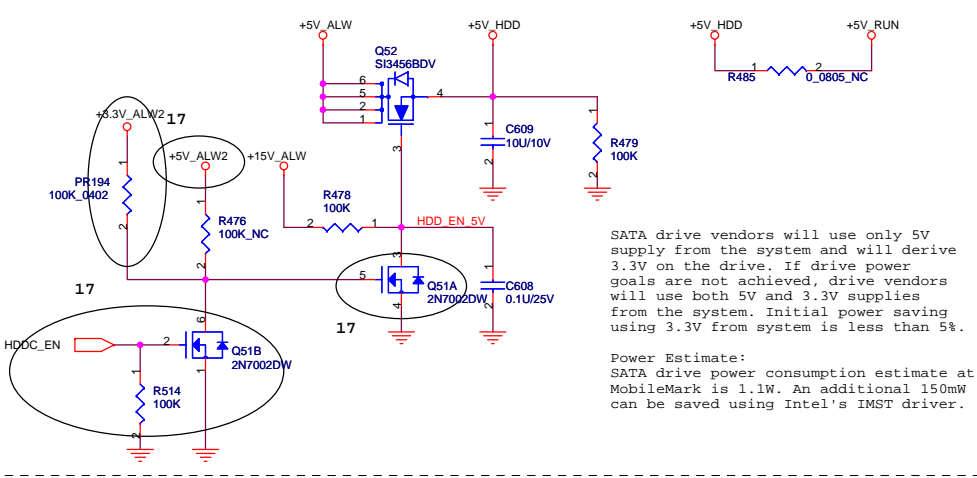


Pin.47 Cable select H=Slave,L=Master

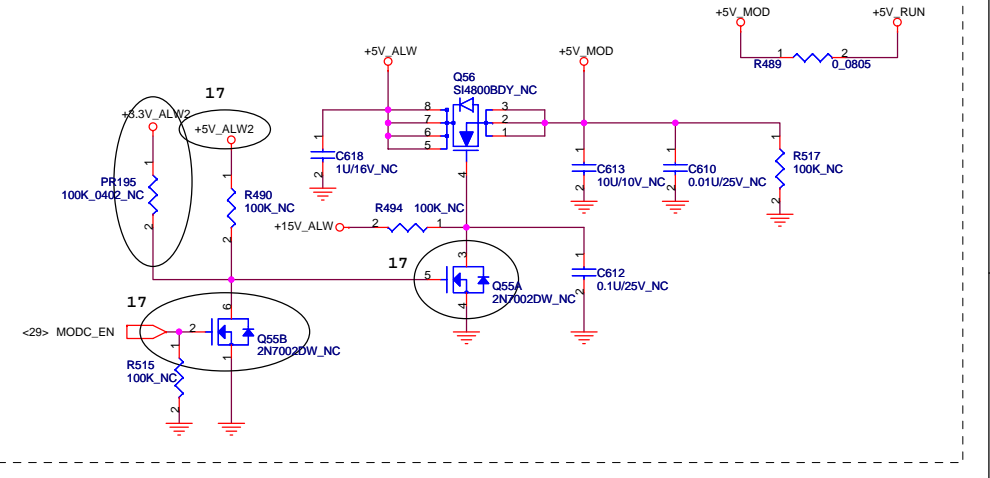


Place closed to MOD connector

SATA PWR

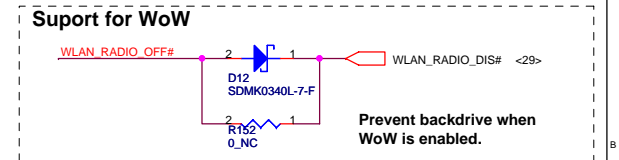
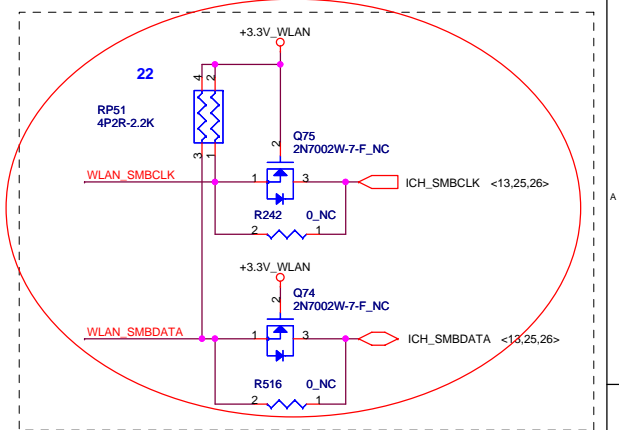
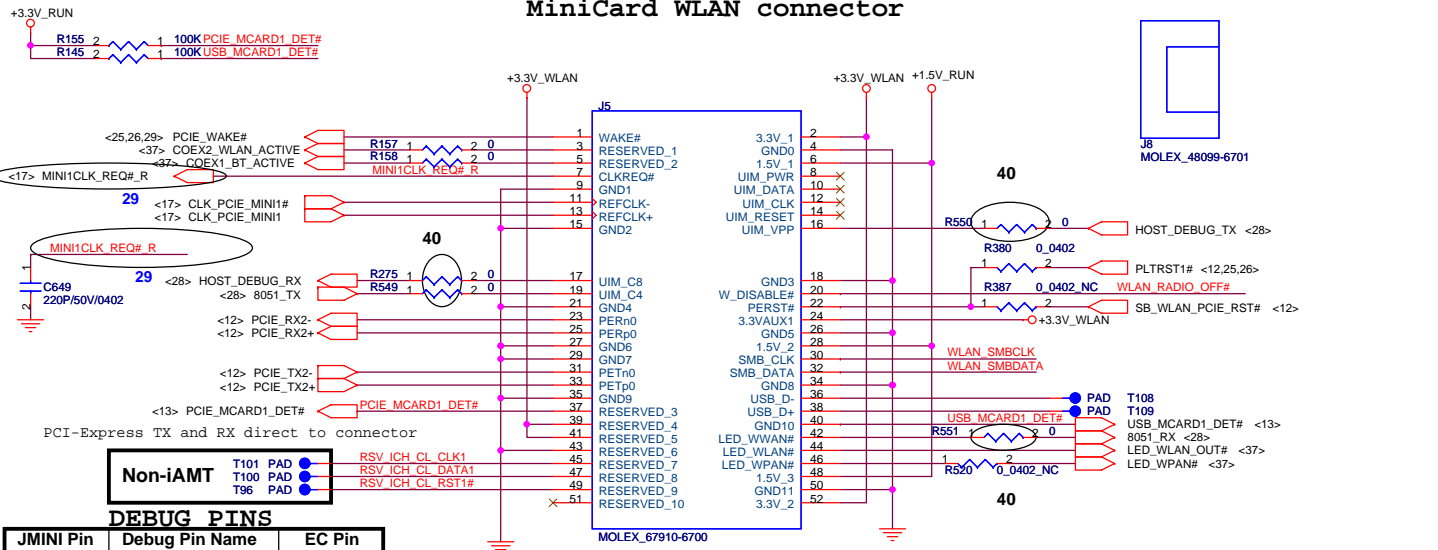


ODD PWR



Title SATA (HDD&CD_ROM)		
Size M-08	Document Number M-08	Rev 0.1
Date: Monday, March 05, 2007	Sheet 23	of 51

MiniCard WLAN connector

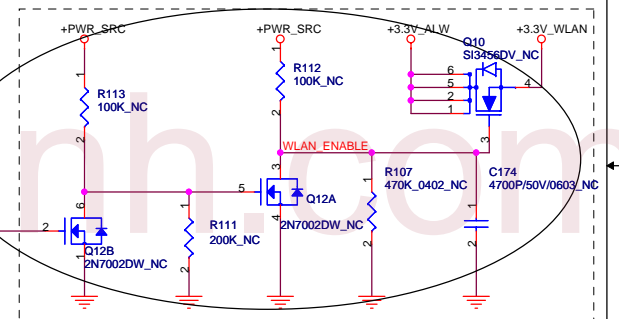
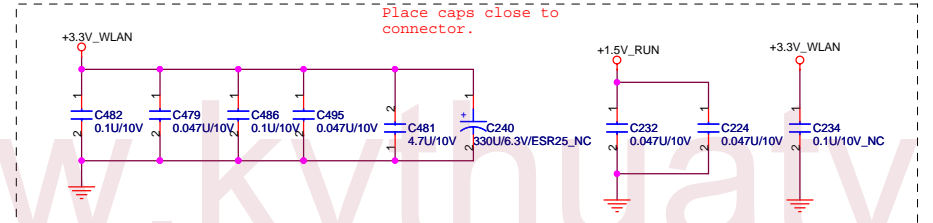


Non-iAMT

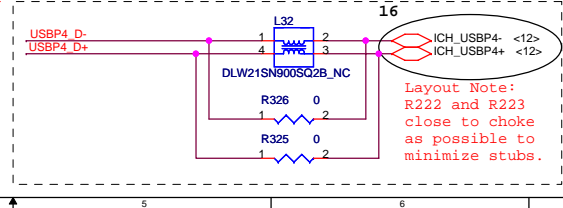
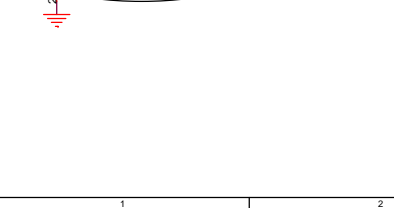
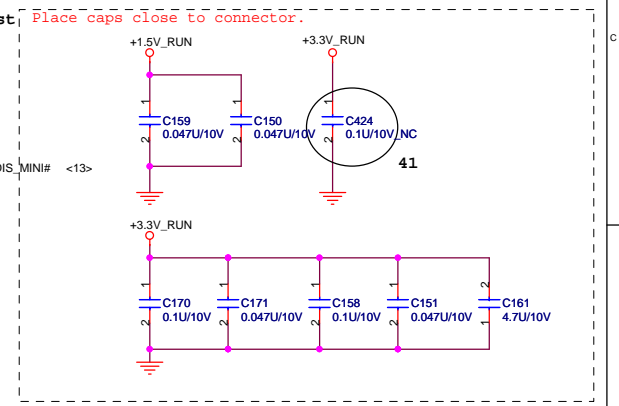
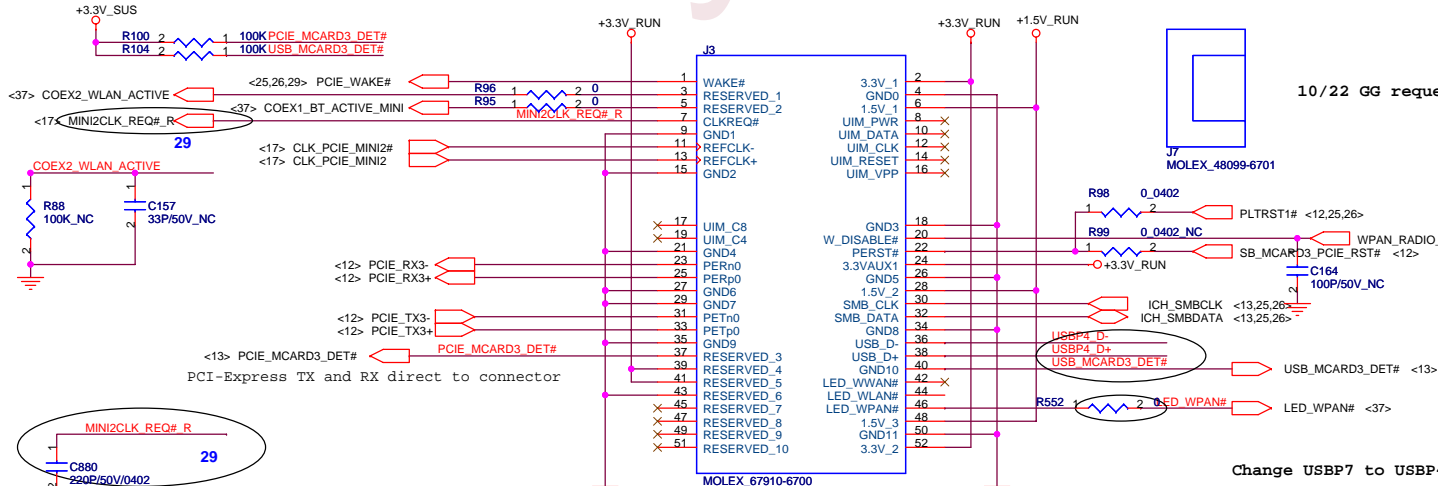
- T101 PAD
- T100 PAD
- T96 PAD

RSV ICH_CL_CLK1
RSV ICH_CL_DATA1
RSV ICH_CL_RST1#

JMINI Pin	Debug Pin Name	EC Pin
16	HOST_DEBUG_TX	70
17	HOST_DEBUG_RX	71
19	8051_TX	82
42	8051_RX	81



MiniCard WPAN connector



QUANTA COMPUTER

Title: MINI-PCI

Size: Document Number M-08

Date: Monday, March 05, 2007

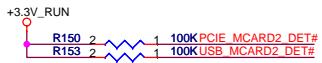
Sheet: 24 of 51

Rev: 0.1

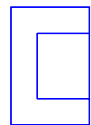
Layout Note:
R222 and R223
close to choke
as possible to
minimize stubs.

10/22 GG request:

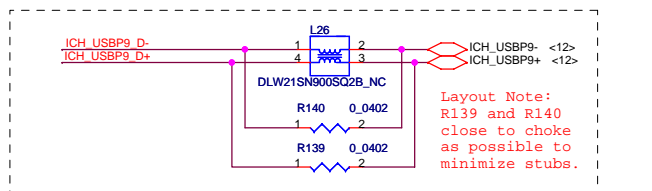
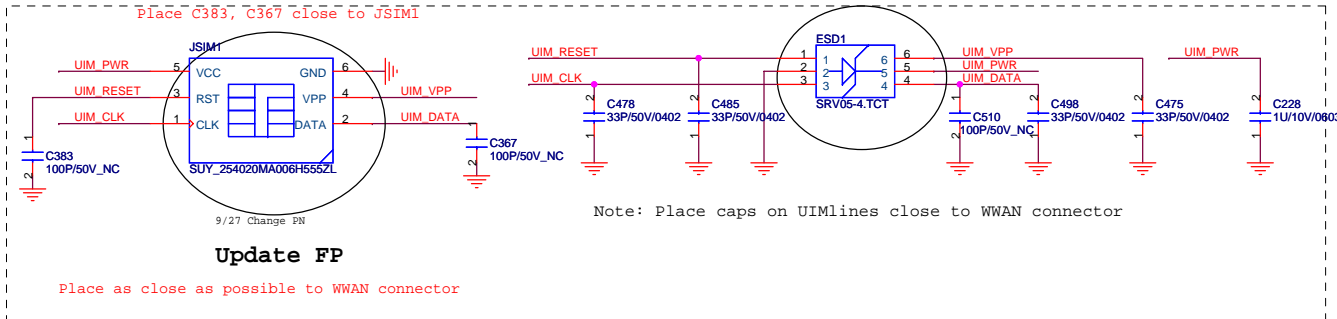
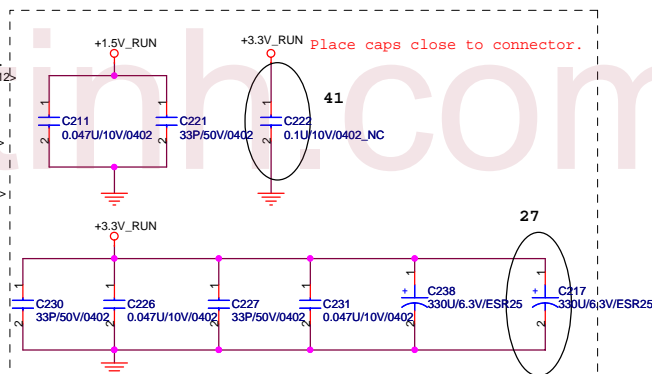
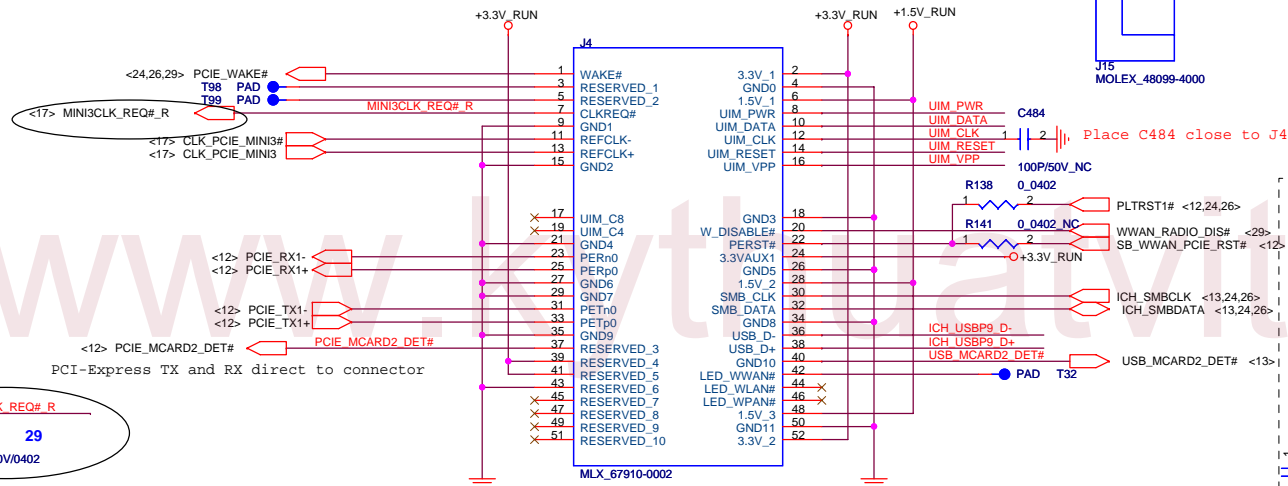
Place caps close to connector.



MiniCard WWAN connector



J15 MOLEX_48099-4000



Update FP

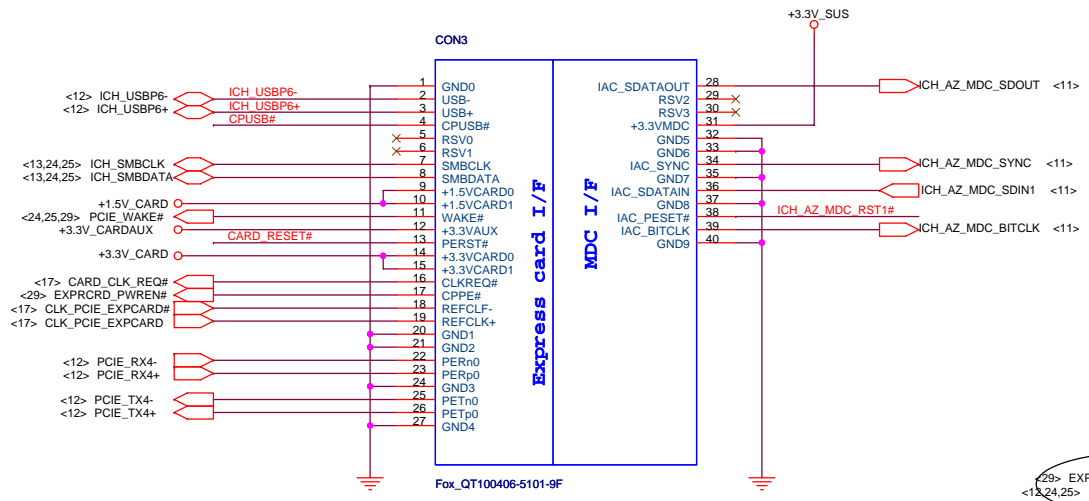
Place as close as possible to WWAN connector

Note: Place caps on UIMlines close to WWAN connector



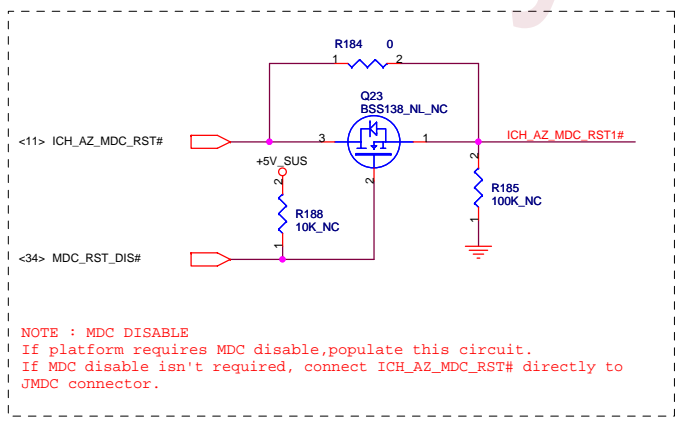
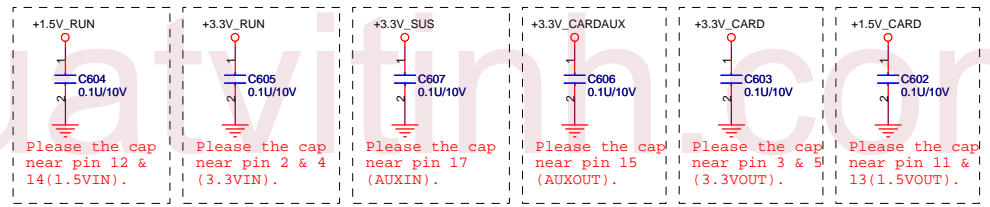
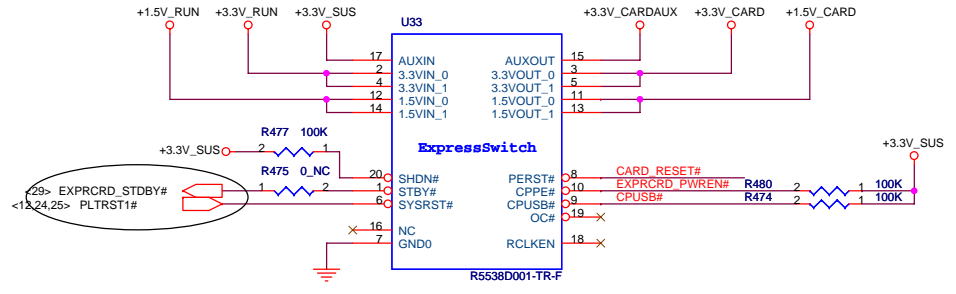
Title WWAN		
Size	Document Number VC-08B	Rev 0.1
Date:	Monday, March 05, 2007	Sheet 25 of 51

EXPRESS+MDC

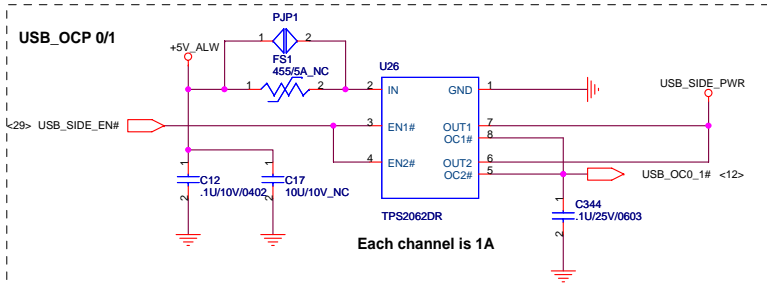


Update PN

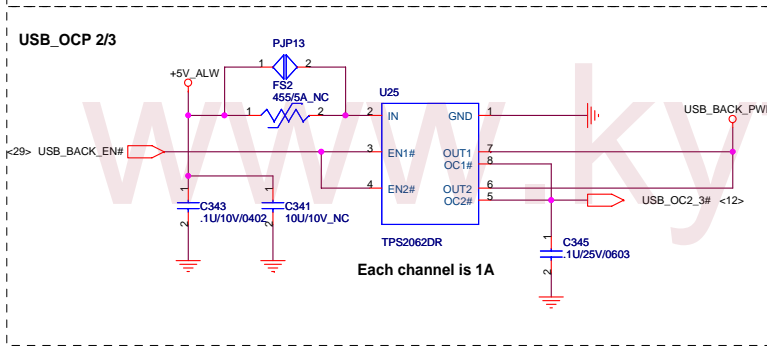
+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.



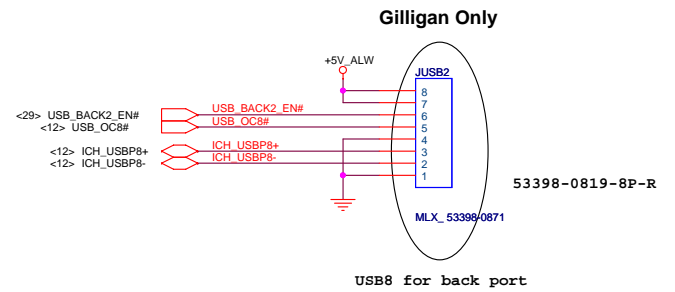
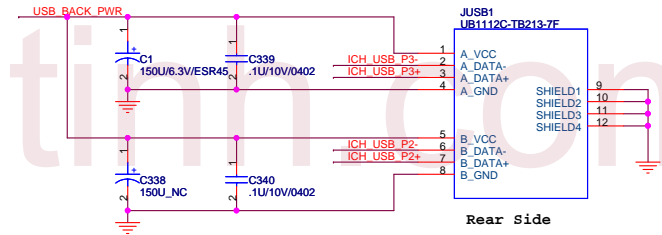
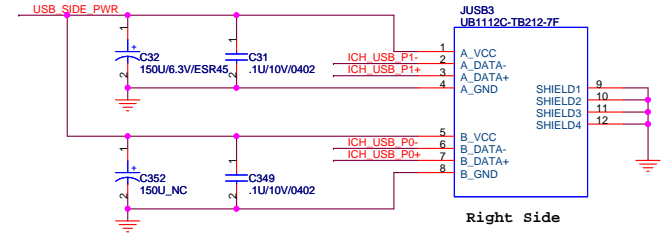
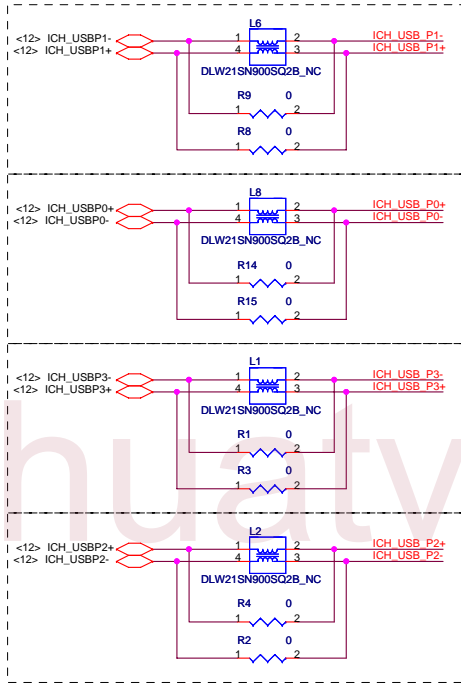
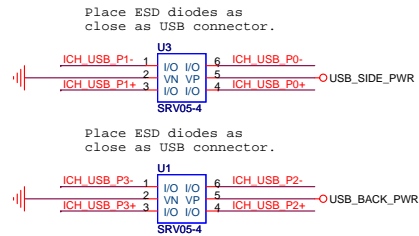
USB_OCP 0/1

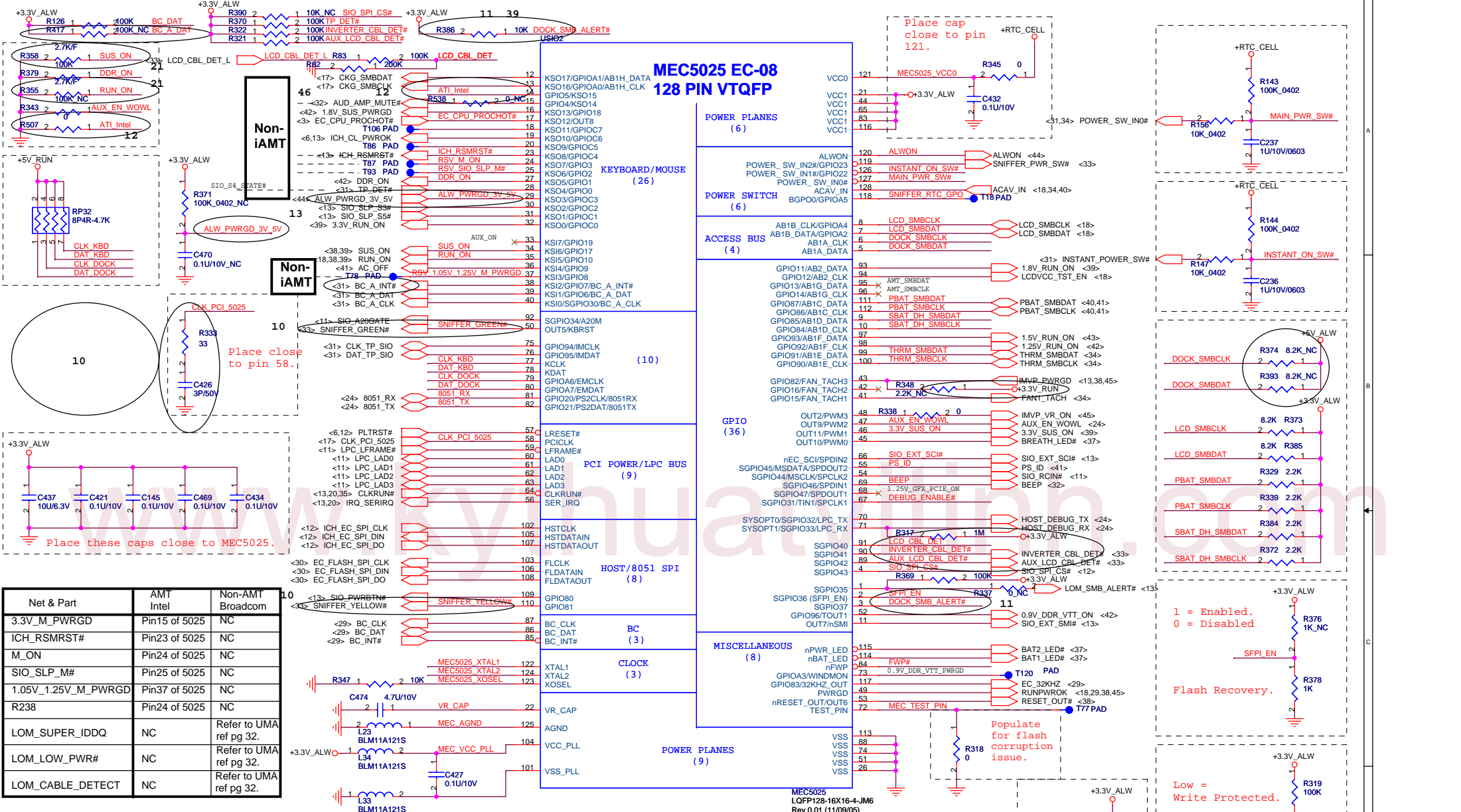


USB_OCP 2/3

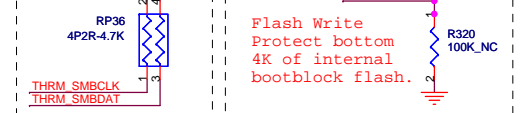
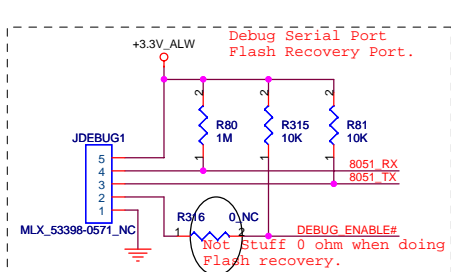
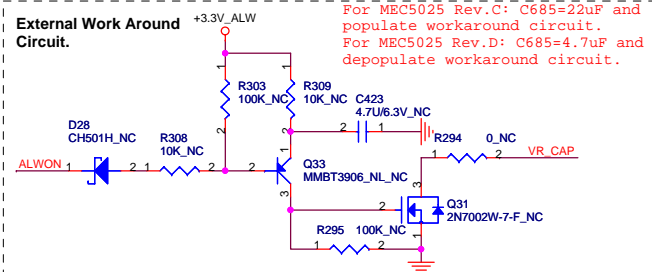
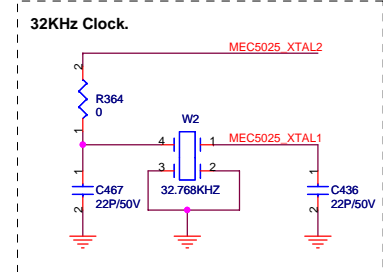


ESD Protect



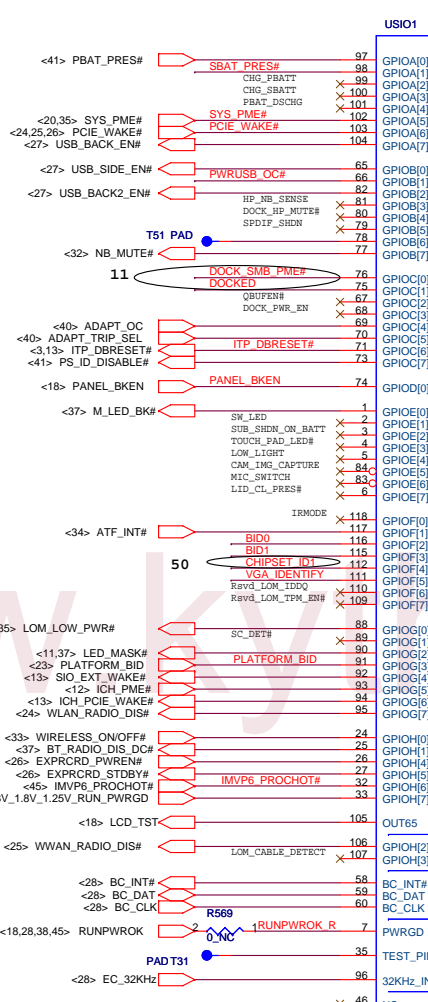
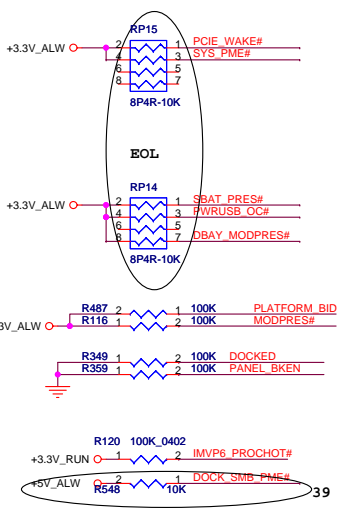


Net & Part	AMT Intel	Non-AMT Broadcom
3.3V_M_PWRGD	Pin15 of 5025	NC
ICH_RSMRST#	Pin23 of 5025	NC
M_ON	Pin24 of 5025	NC
SIO_SLP_M#	Pin25 of 5025	NC
1.05V_1.25V_M_PWRGD	Pin37 of 5025	NC
R238	Pin24 of 5025	NC
LOM_SUPER_IDDQ	NC	Refer to UMA ref pg 32.
LOM_LOW_PWR#	NC	Refer to UMA ref pg 32.
LOM_CABLE_DETECT	NC	Refer to UMA ref pg 32.



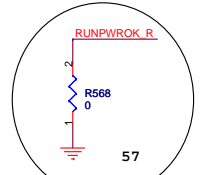
Update to 5021

Depopulate R529, R530, R531, R532, R533, R534, R535, R536, R92, R97, C142, C133, C137, C141, C179, C165, C172, L21
 Populate R537, C879.



VGA	BID2	BID1	BID0	Board Revision
1	0	0	0	SST (X00)
1	0	1	0	Pre-PT (X01)
1	0	1	0	PT (X02)
1	0	1	1	ST (X03)
1	0	0	0	Q1T(A00)
1	0	0	1	RAMP-2 (A01)

Reset BID



Update P/N

**ECE5021
 128 Pin
 V1QFP**

GPIOs

USB

CIRCC

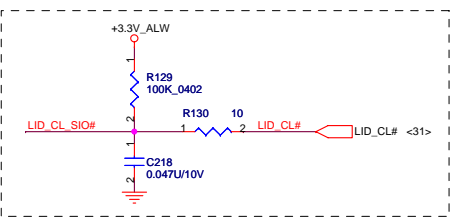
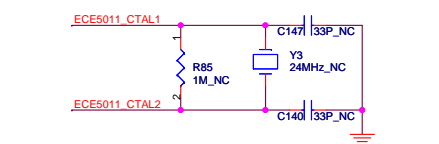
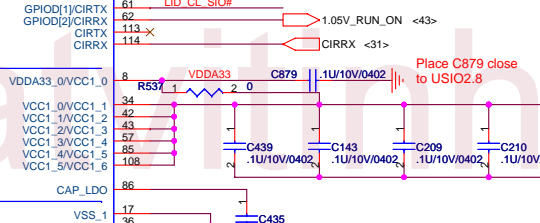
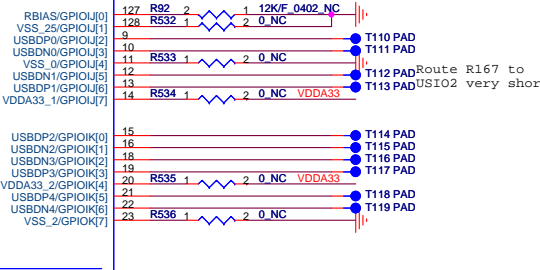
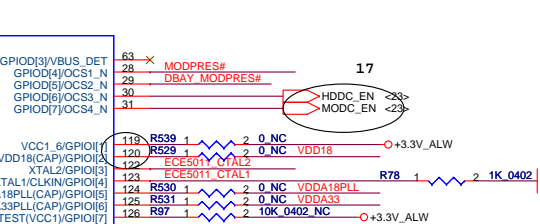
POWER

VSS

SIO Reset

BC

MISCELLANEOUS



QUANTA COMPUTER

Title: SIO (GPIO/BC/USB/CIRRX)

Size: Document Number FM1

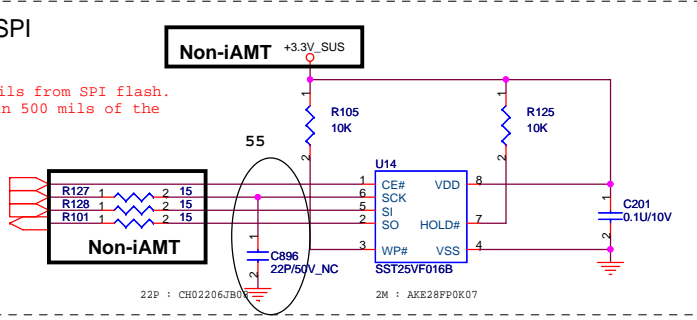
Date: Monday, March 05, 2007

Sheet 29 of 51

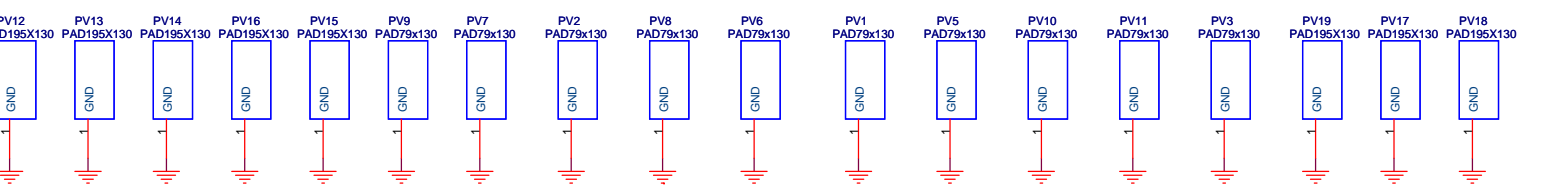
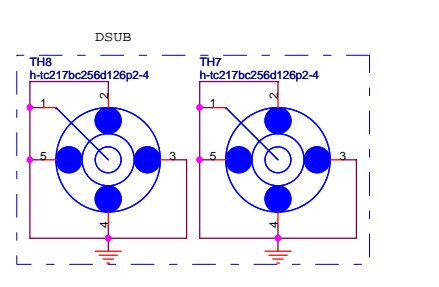
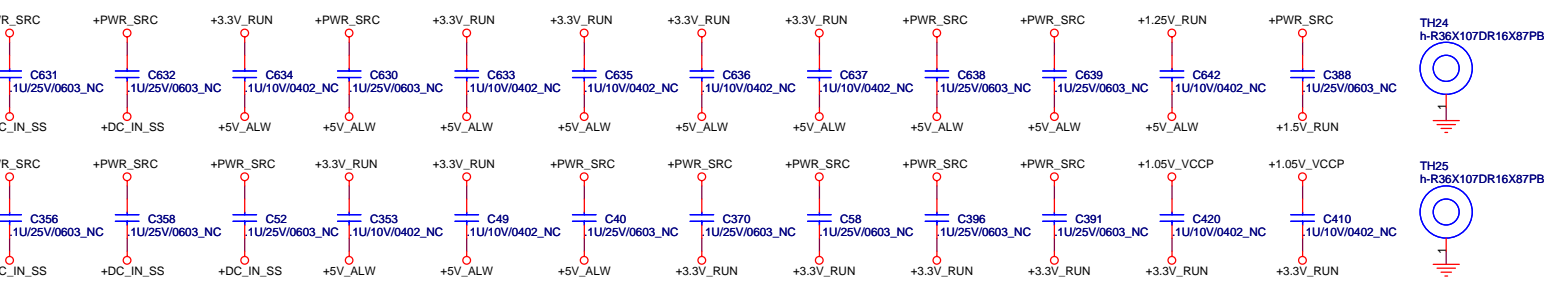
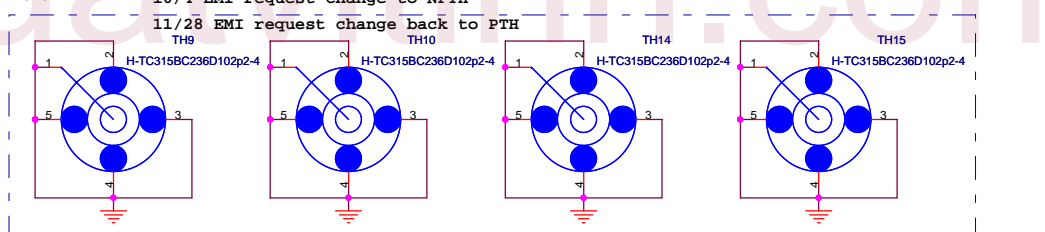
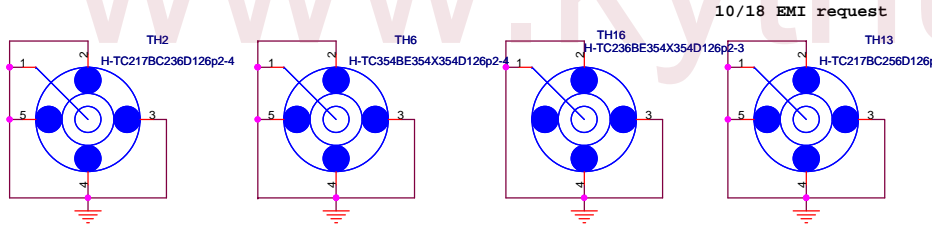
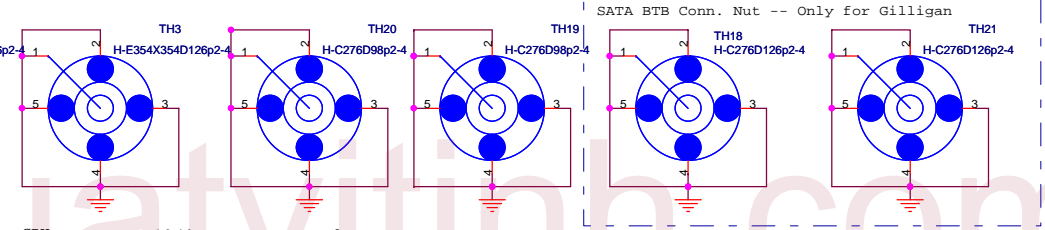
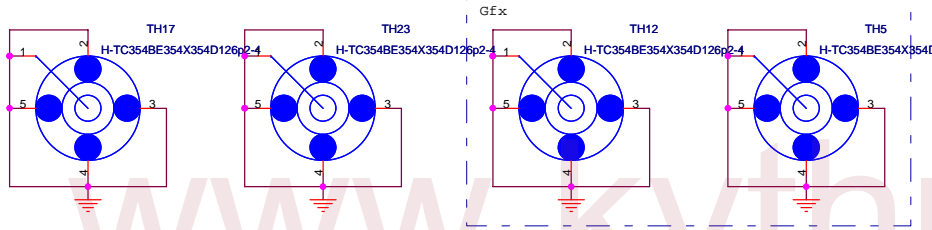
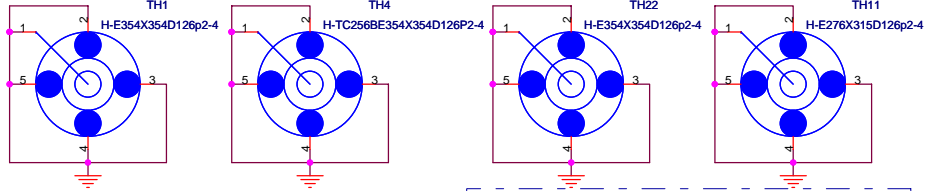
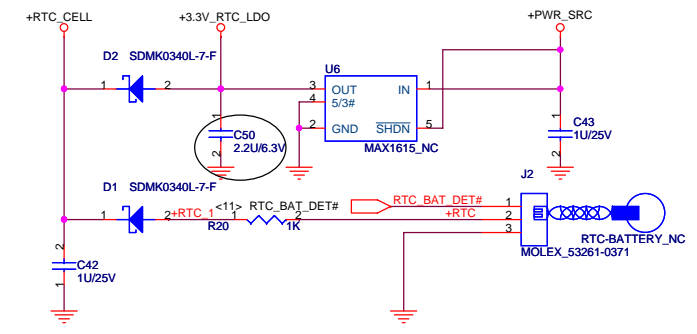
Rev 0.1


16Mbit (2M Byte), SPI

Layout Note:
Place R471 within 500 mils from SPI flash.
Place R498 & R534 within 500 mils of the
MBC5025.



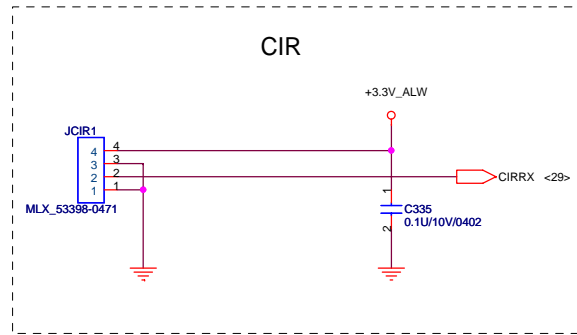
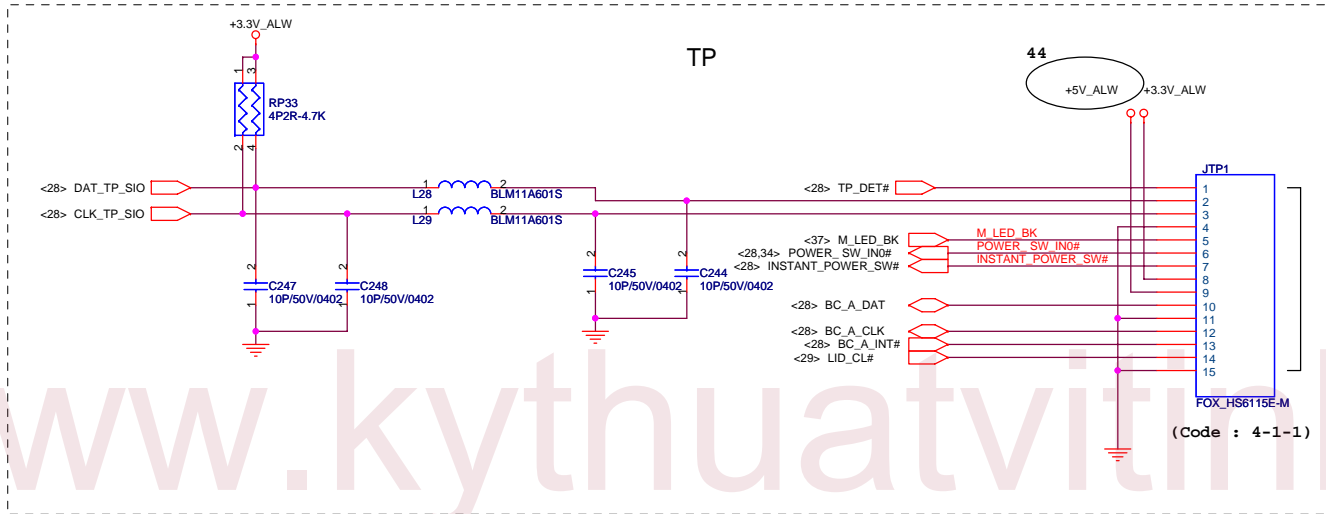
RTC BATTERY





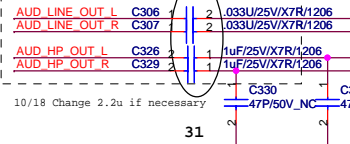
QUANTA COMPUTER

Title FLASH, RTC & KC		
Size M-08	Document Number M-08	Rev 0.1
Date: Monday, March 05, 2007	Sheet 30	of 51



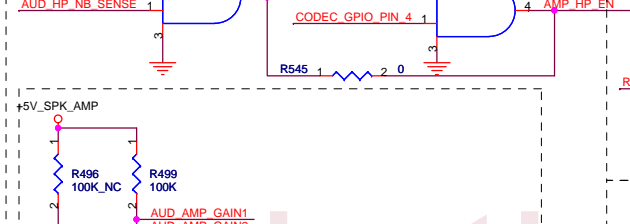
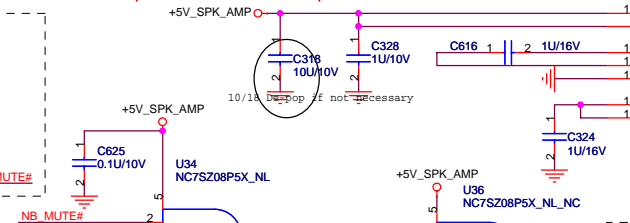
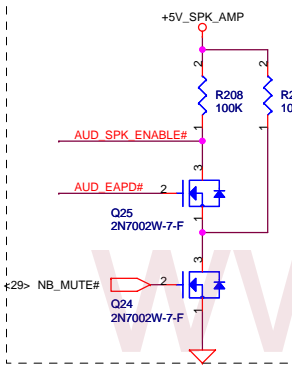
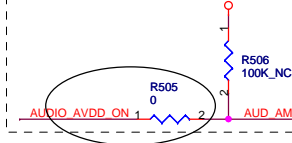
INTERNAL SPEAKER AMP Update PN

Package 1206 for THD+N performance for Vista Logo requirements.



10/18 Change 2.2u if necessary

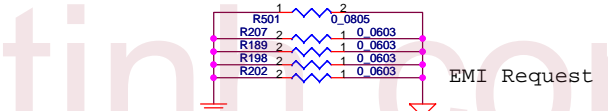
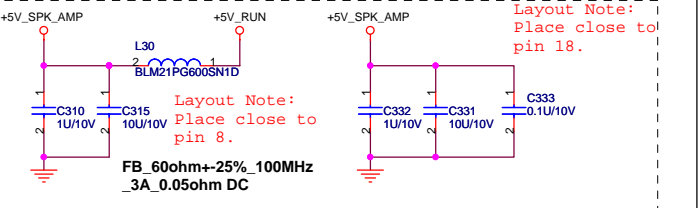
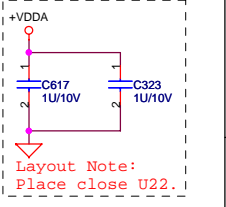
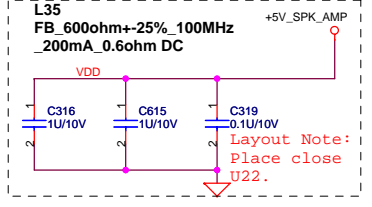
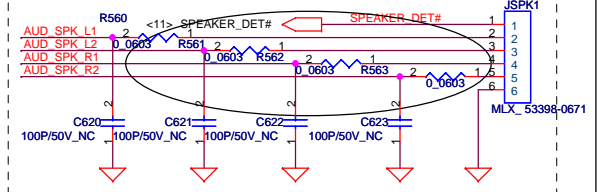
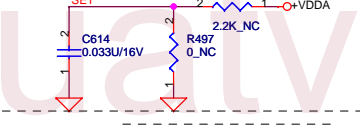
For MAX9789A, depop R505, pop R506.



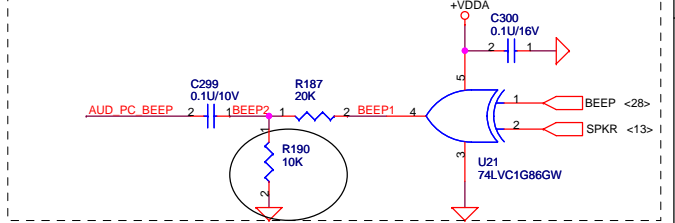
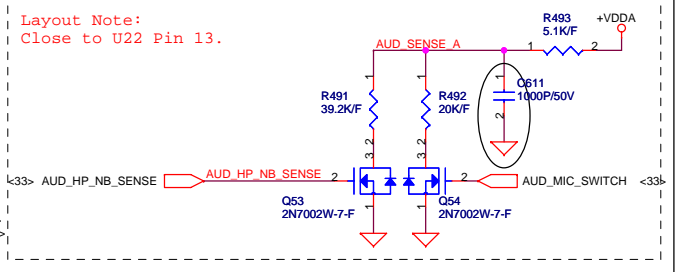
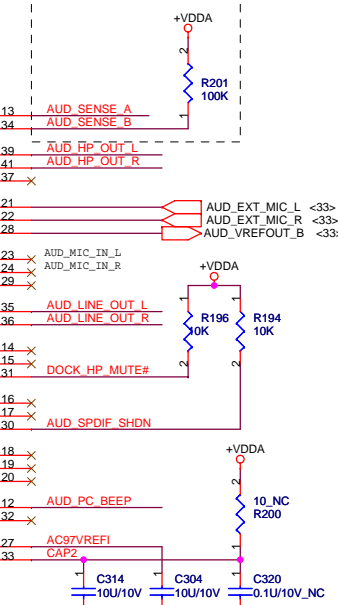
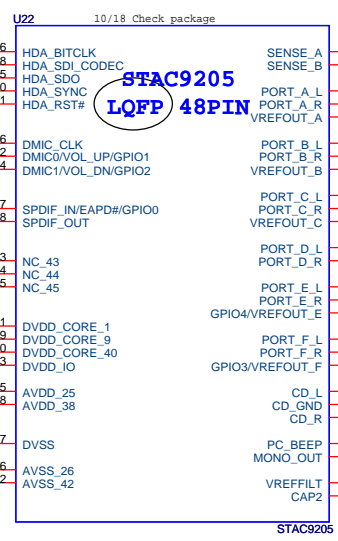
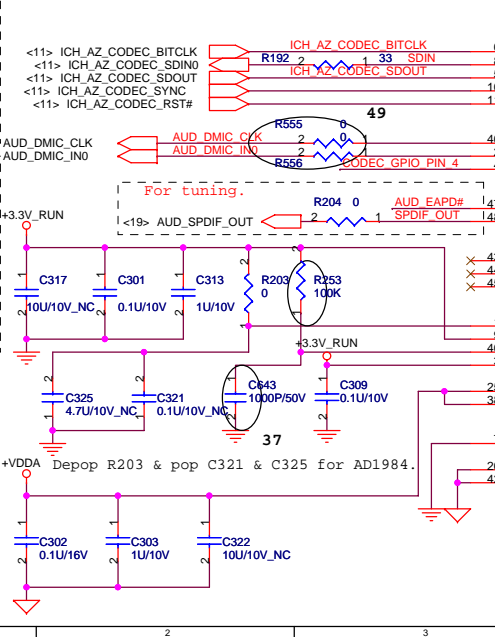
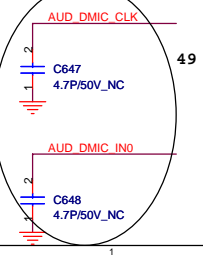
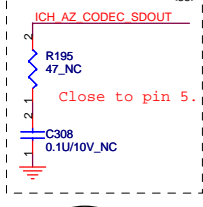
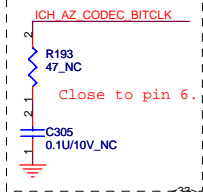
GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

C1425/C331 value need to match with C326/C290. This value be chosen in PT phase.

For MAX9789A, depop C614, pop R497.



AZALIA (HD) CODEC

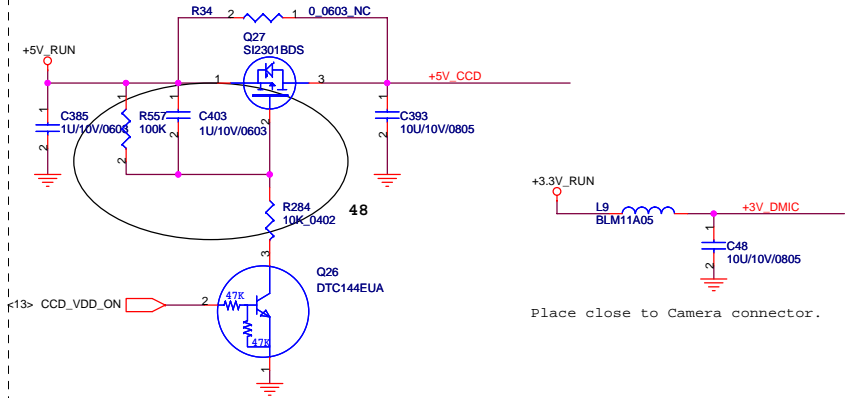


C304 must be 1U & Pop C320 & R200 for AD1984.

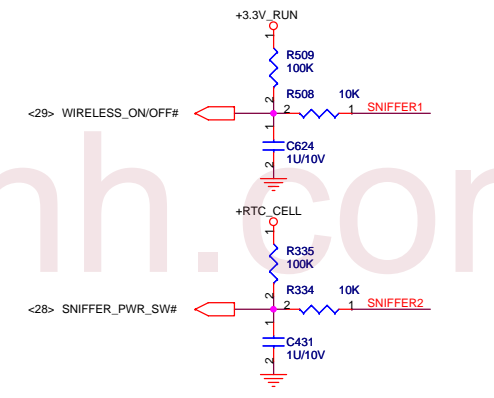
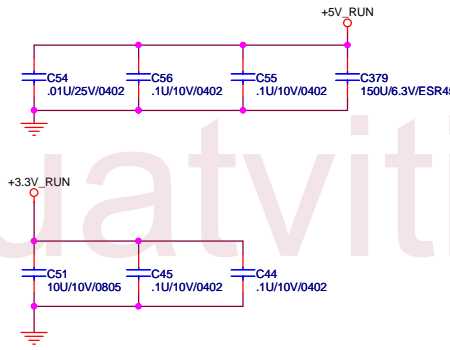
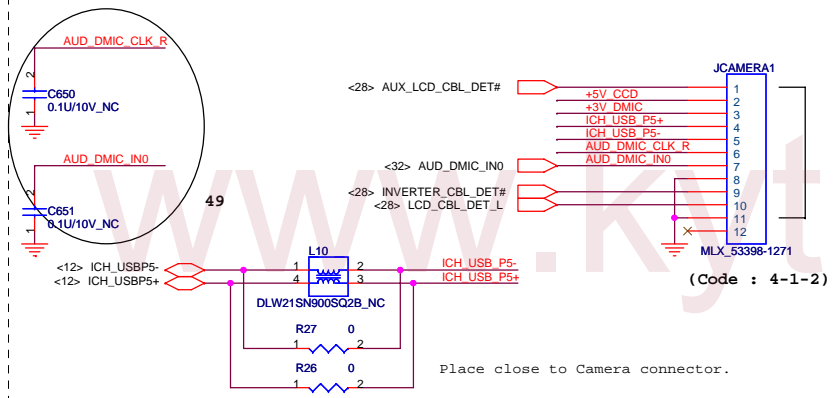
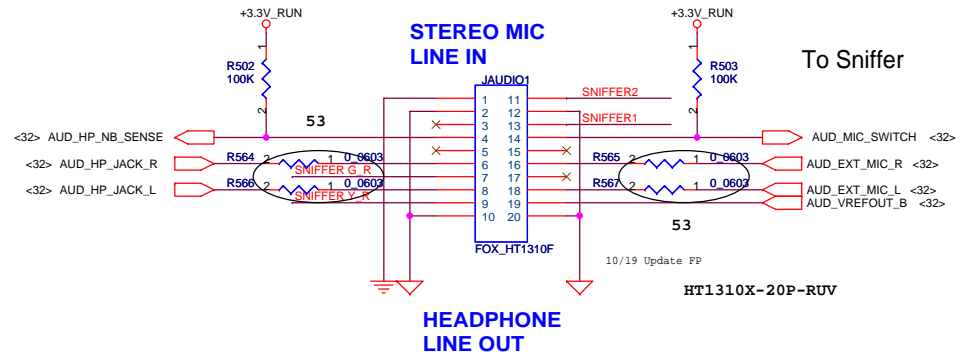
DELL CONFIDENTIAL/PROPRIETARY

Title: Azelia CODEC(STAC9205)		
Size: M-08	Document Number: M-08	Rev: 0.1
Date: Monday, March 05, 2007	Sheet: 32	of 51

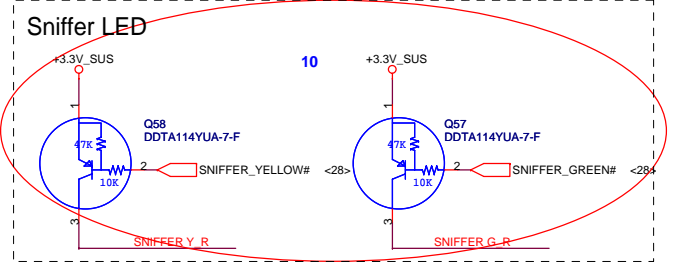
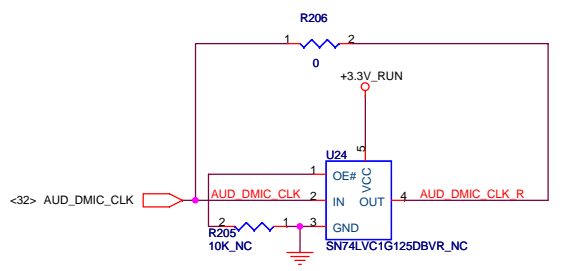
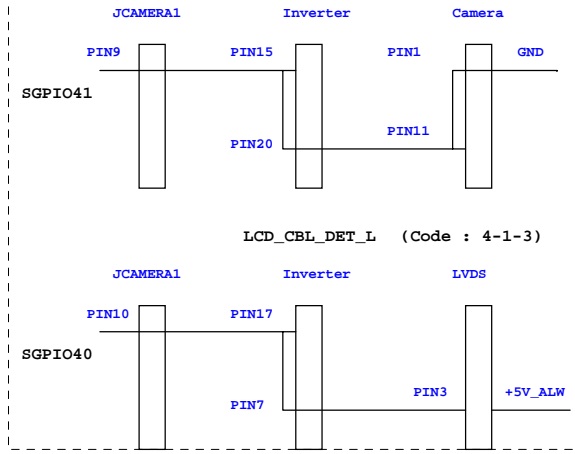
Digital Microphone & Camera



Update PN

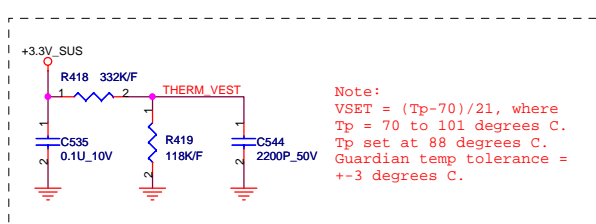
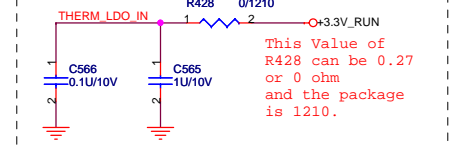
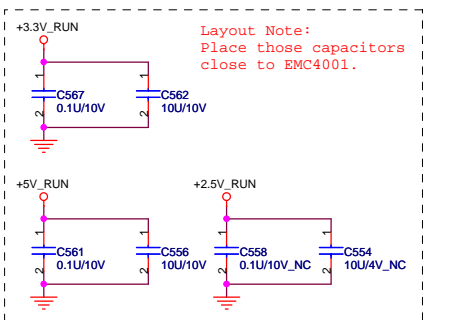
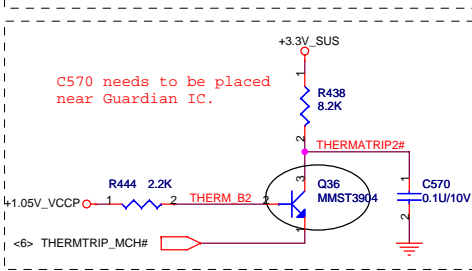
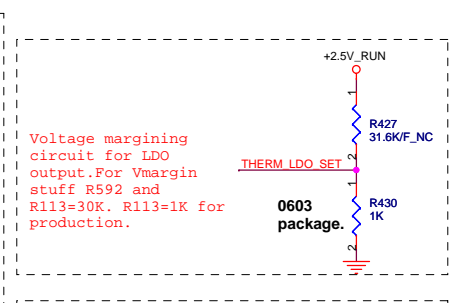
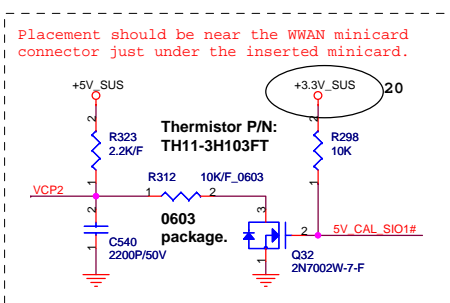
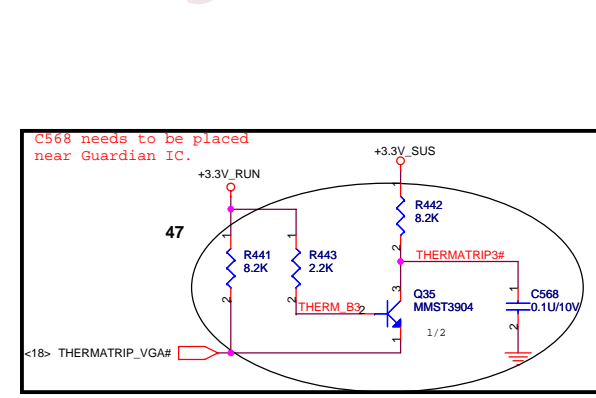
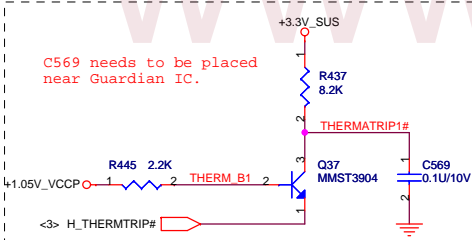
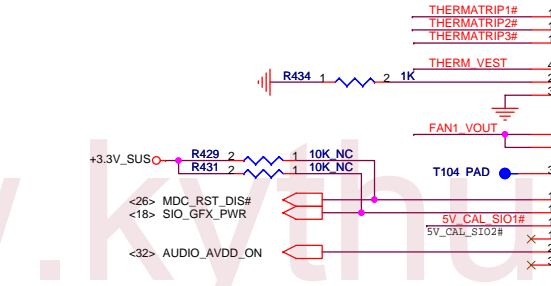
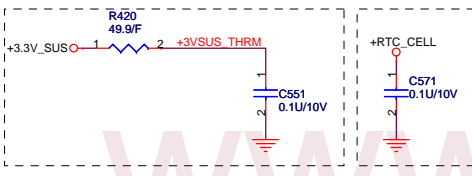
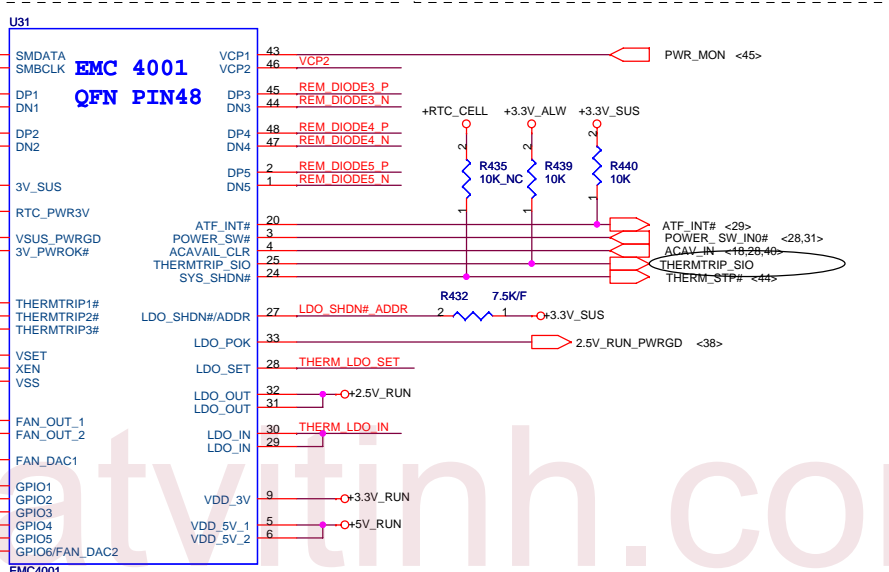
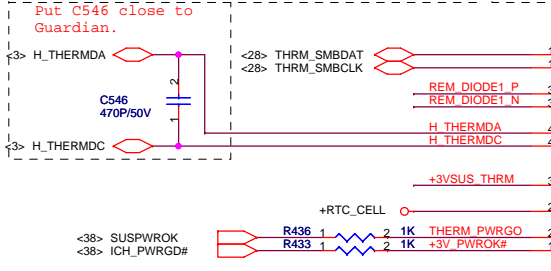
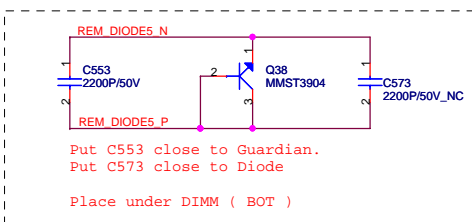
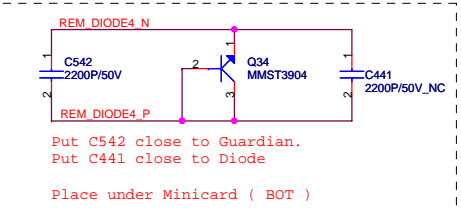
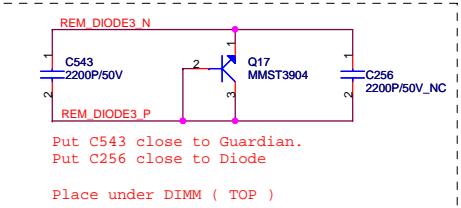
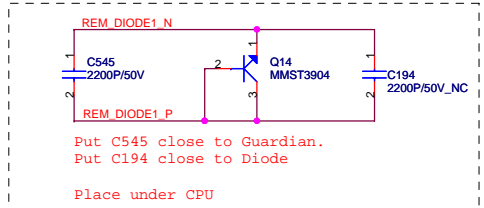
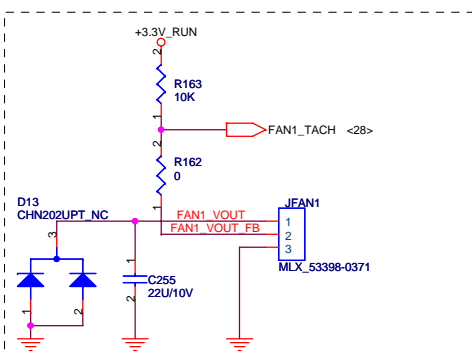


PAID INVERTER_CBL_DET# (Code : 4-1-4)

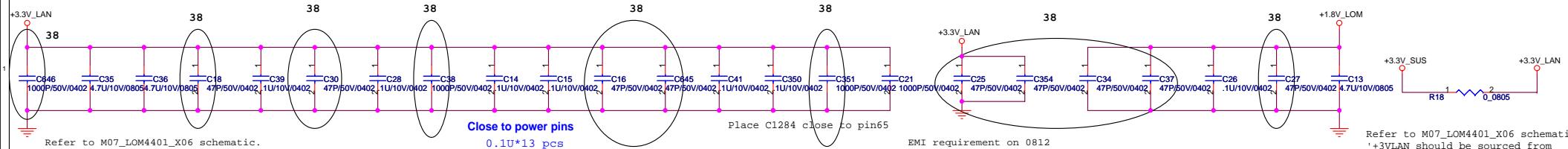


DELL CONFIDENTIAL/PROPRIETARY

Title		
AUDIO CONN		
Size	Document Number	Rev
M-08		0.1
Date:	Monday, March 05, 2007	Sheet 33 of 51



Refer to M07_LOM4401_X06 schematic.



Refer to M07_LOM4401_X06 schematic.

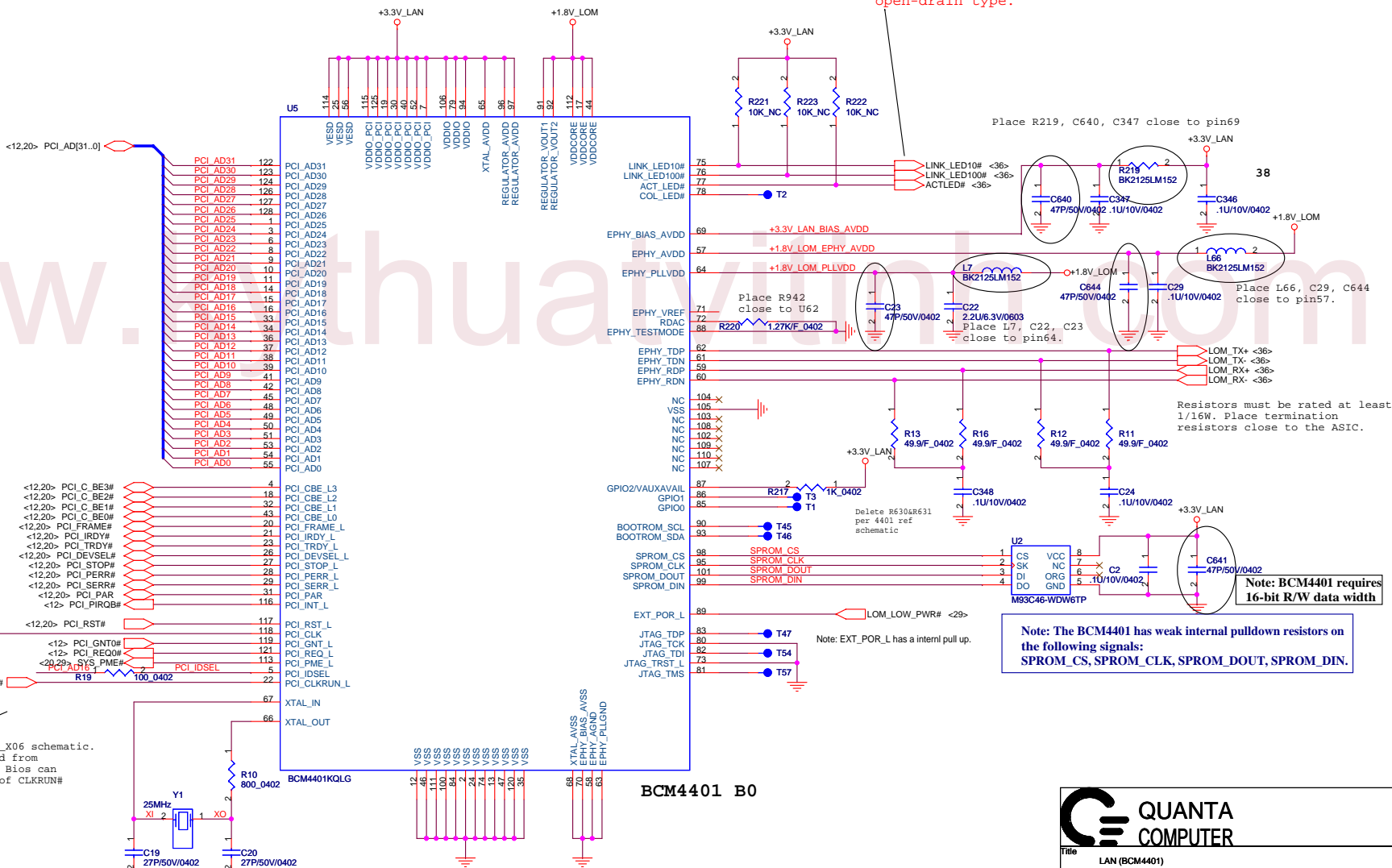
Close to power pins
0.1U*13 pcs

Place C1284 close to pin65

EMI requirement on 0812

Refer to M07_LOM4401_X06 schematic.
'+3VLAN should be sourced from +3VSUS instead of +3VSR since WOL is not supported on C/G.

These three pin
LINK_LED10#,
LINK_LED100#,
ACT_LED are
open-drain type.



www.thuam.com

Note: BCM4401 requires 16-bit R/W data width

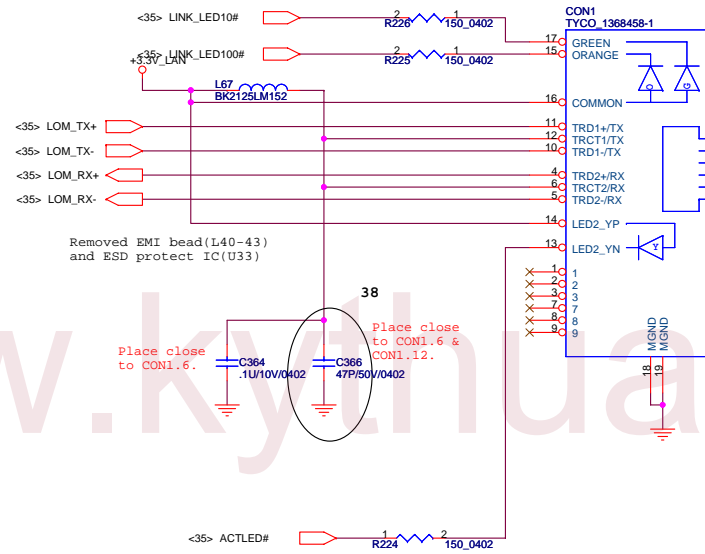
Note: The BCM4401 has weak internal pulldown resistors on the following signals:
SPROM_CS, SPROM_CLK, SPROM_DOUT, SPROM_DIN.

Note: EXT_POR_L has a internal pull up.

Refer to M07_LOM4401_X06 schematic.
R489 and R490 removed from schematic because of Bios can configure the state of CLKRUN# signal.

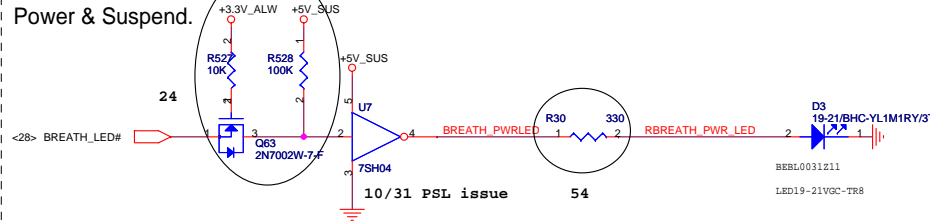
QUANTA COMPUTER

Title		LAN (BCM4401)	
Size	Document Number	Rev	
	FM1	0.1	
Date:	Monday, March 05, 2007	Sheet	35 of 51

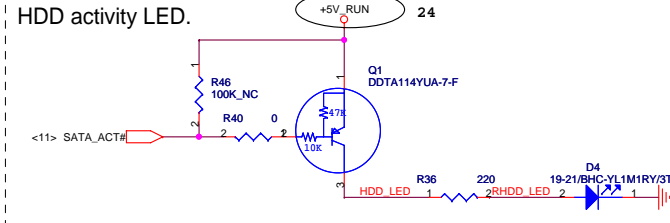


www.kyathuatvith.com

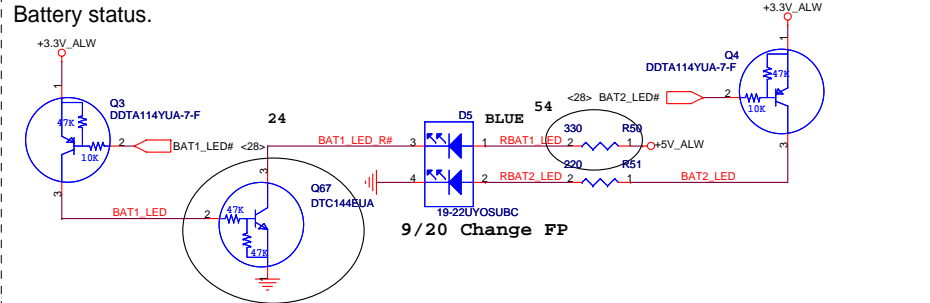
Power & Suspend.



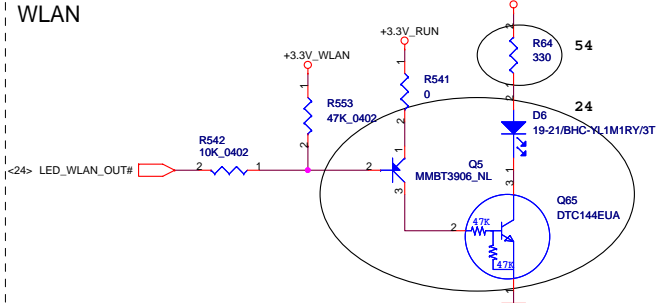
HDD activity LED.



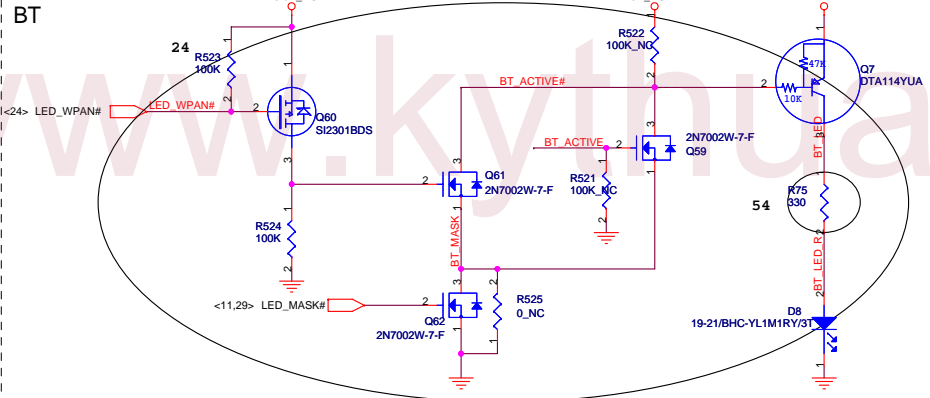
Battery status.



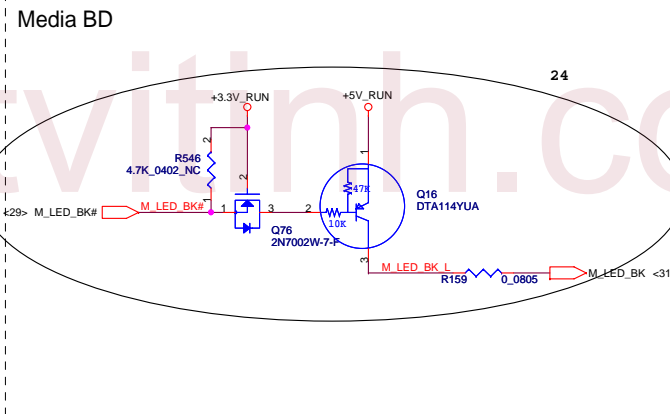
WLAN



BT

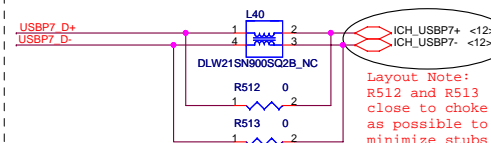
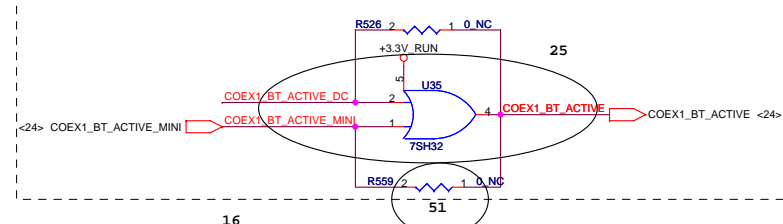
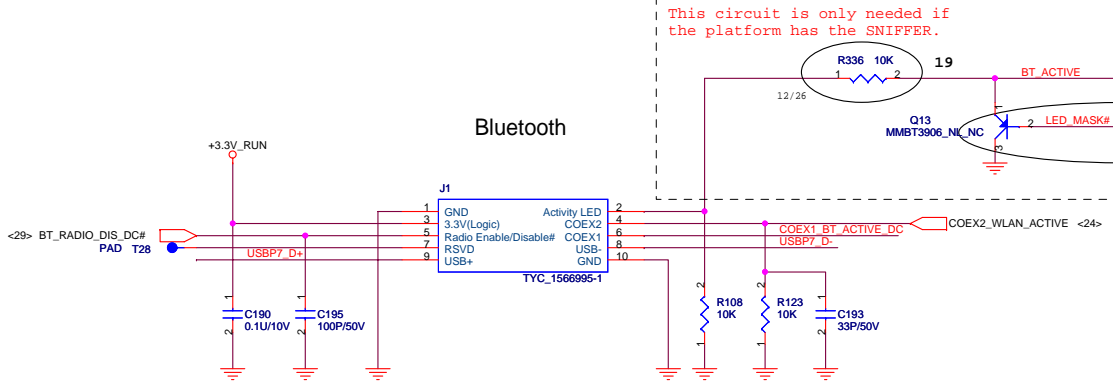


Media BD



This circuit is only needed if the platform has the SNIPPER.

Bluetooth



Layout Note:
R512 and R513
close to choke
as possible to
minimize stubs.

QUANTA COMPUTER

Title: SWITCH & LED

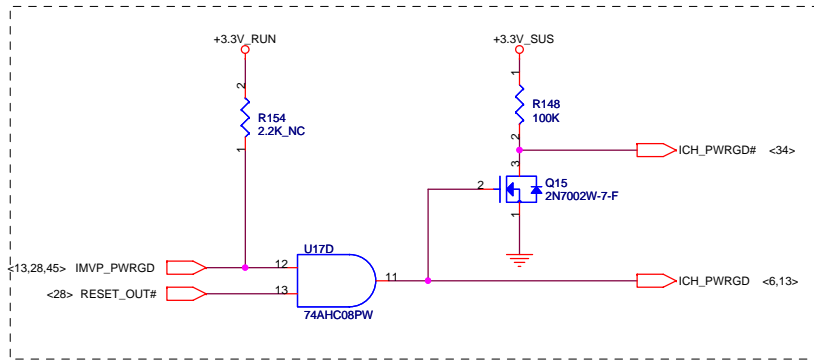
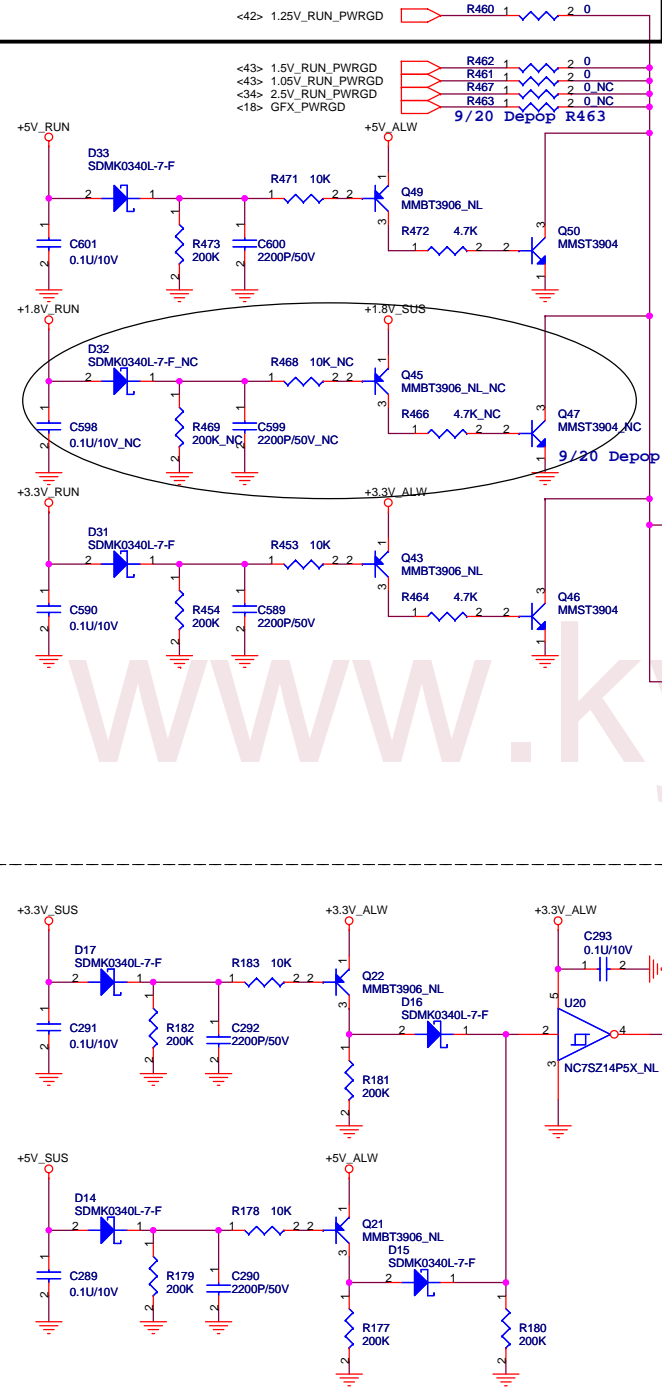
Size: Document Number FM1

Date: Monday, March 05, 2007

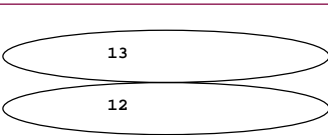
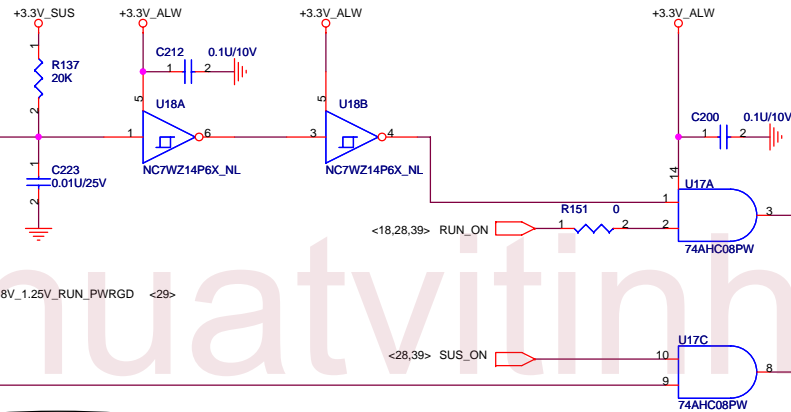
Sheet 37 of 51

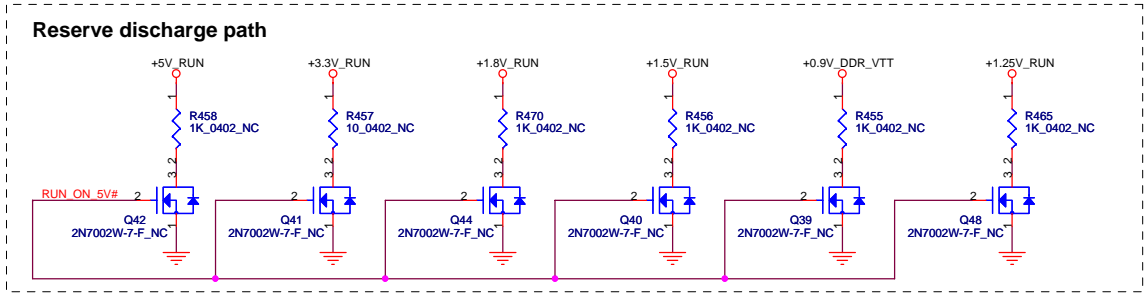
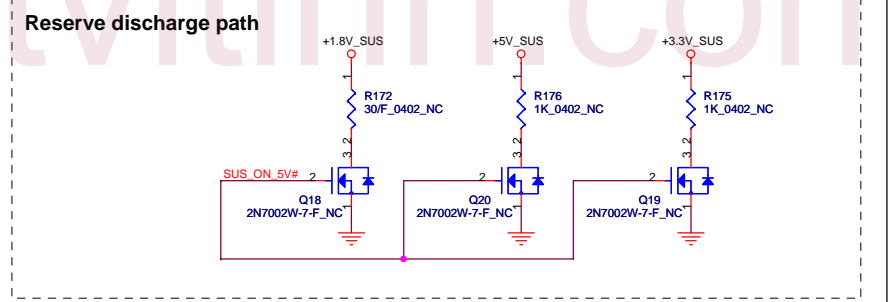
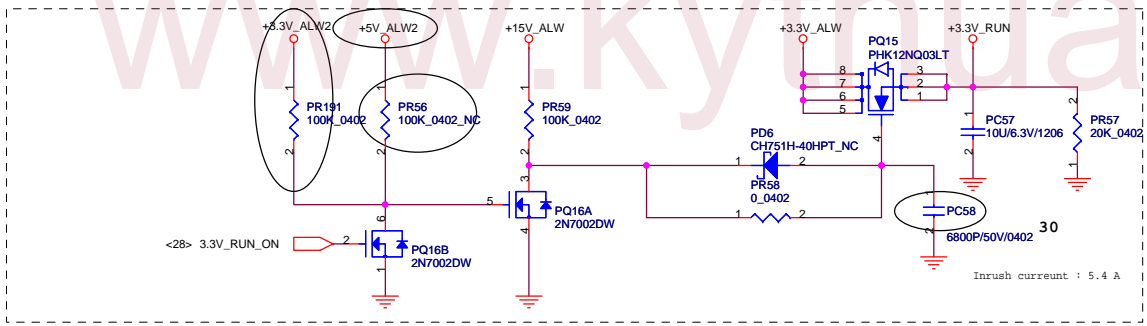
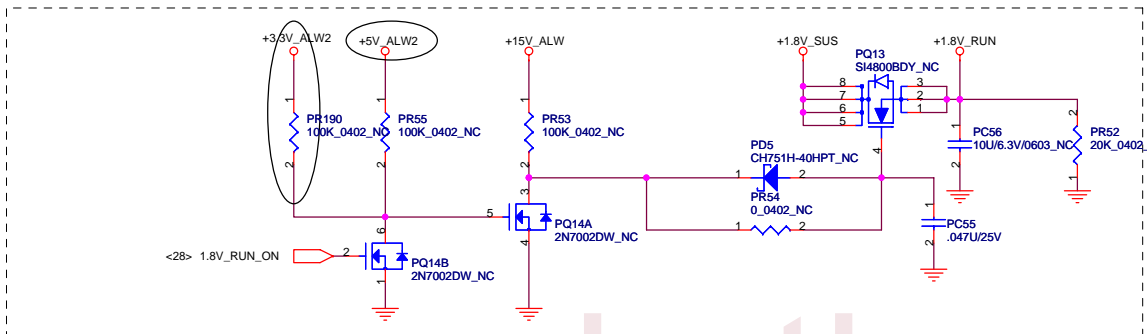
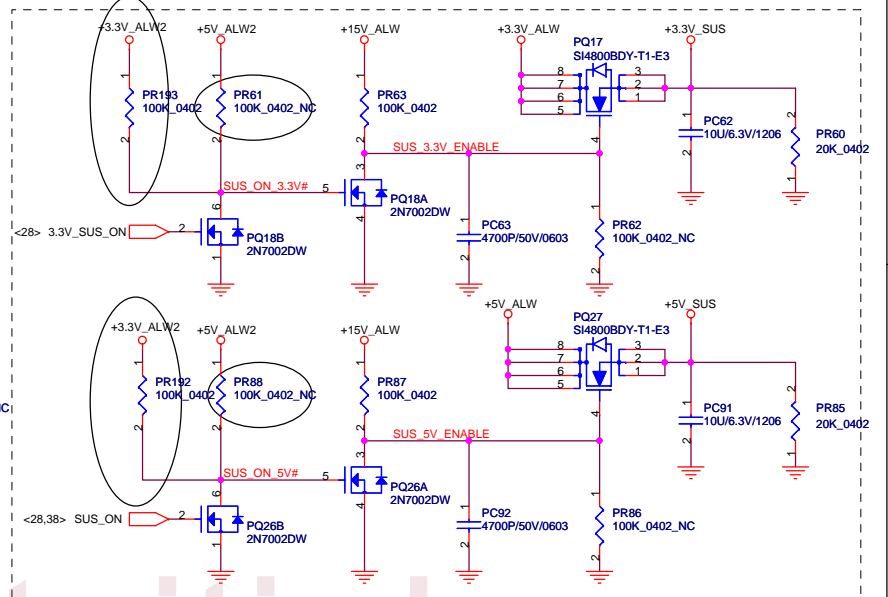
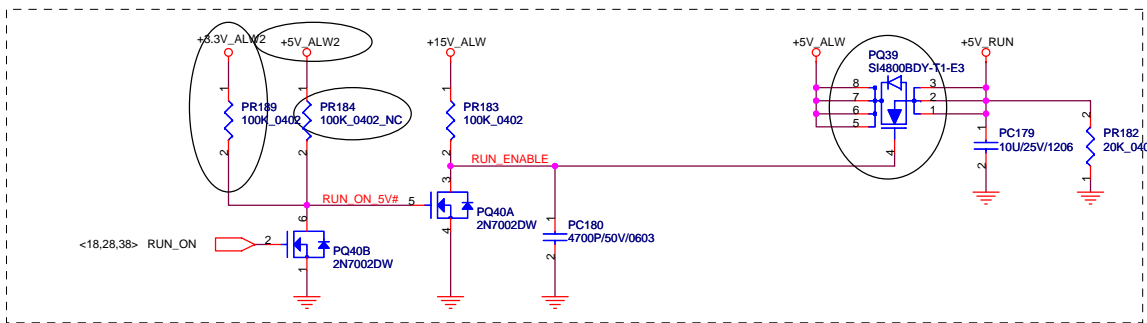
Rev 0.1

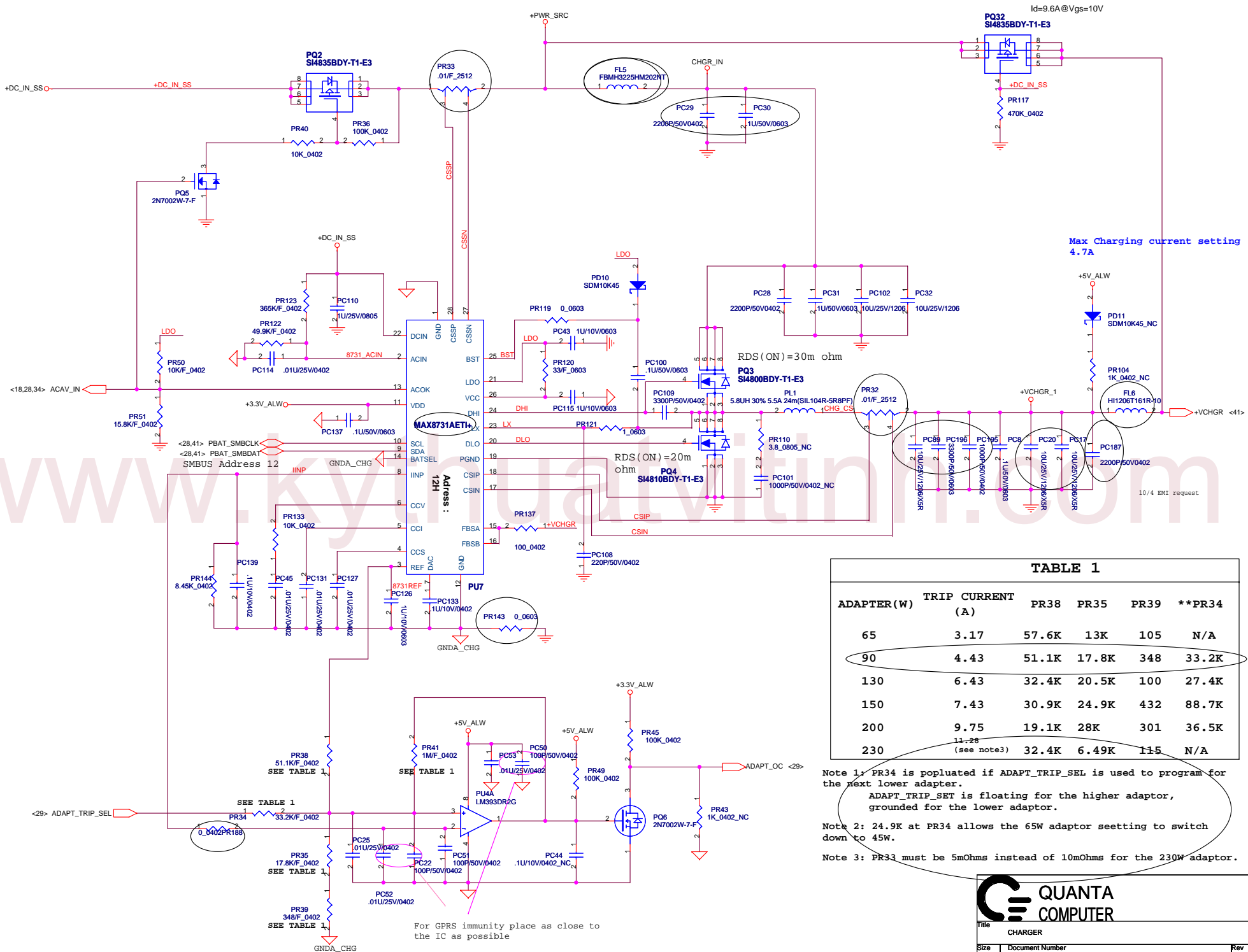
Non-iAMT



Keep Away from high speed buses







Max Charging current setting 4.7A

TABLE 1

ADAPTER (W)	TRIP CURRENT (A)	PR38	PR35	PR39	**PR34
65	3.17	57.6K	13K	105	N/A
90	4.43	51.1K	17.8K	348	33.2K
130	6.43	32.4K	20.5K	100	27.4K
150	7.43	30.9K	24.9K	432	88.7K
200	9.75	19.1K	28K	301	36.5K
230	11.28 (see note3)	32.4K	6.49K	115	N/A

Note 1: PR34 is populated if ADAPT_TRIP_SEL is used to program for the next lower adaptor.

ADAPT_TRIP_SET is floating for the higher adaptor, grounded for the lower adaptor.

Note 2: 24.9K at PR34 allows the 65W adaptor setting to switch down to 45W.

Note 3: PR33 must be 5mOhms instead of 10mOhms for the 230W adaptor.

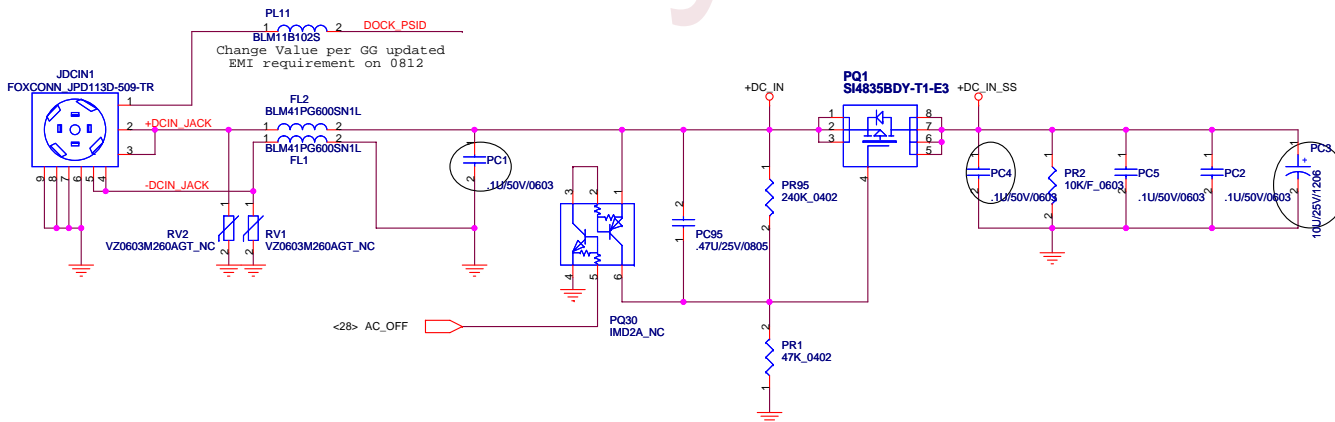
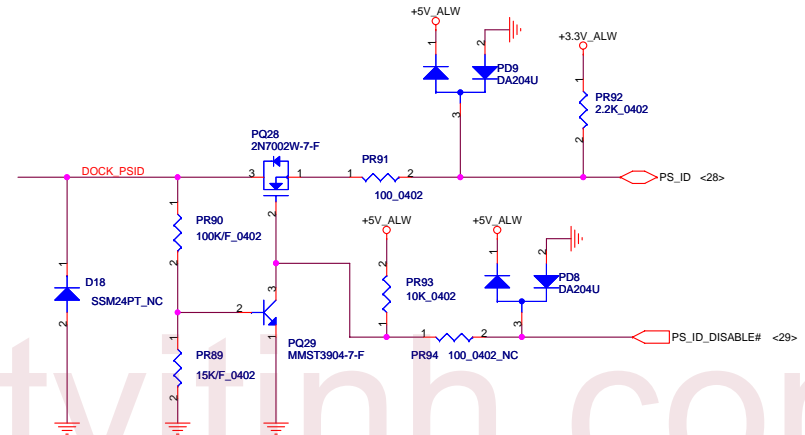
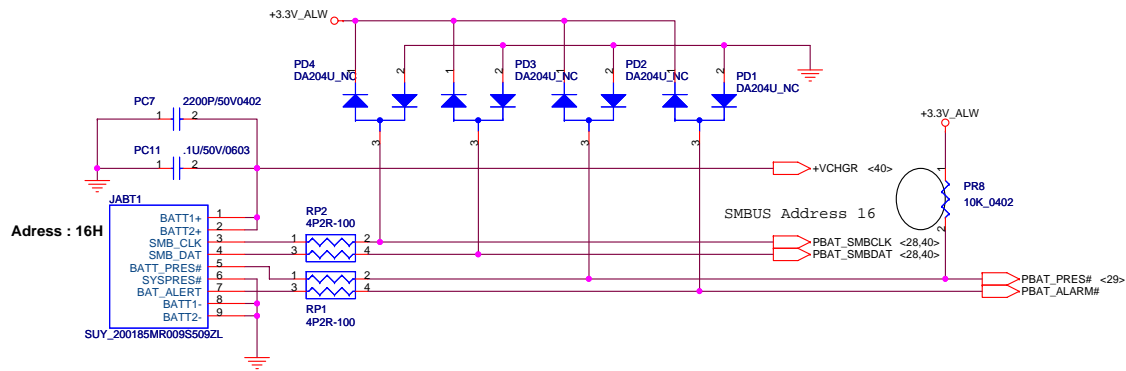
QUANTA COMPUTER

File: CHARGER

Size	Document Number	Rev
	FMS	0.1

Date: Monday, March 05, 2007 Sheet 40 of 51

For GPRS immunity place as close to the IC as possible

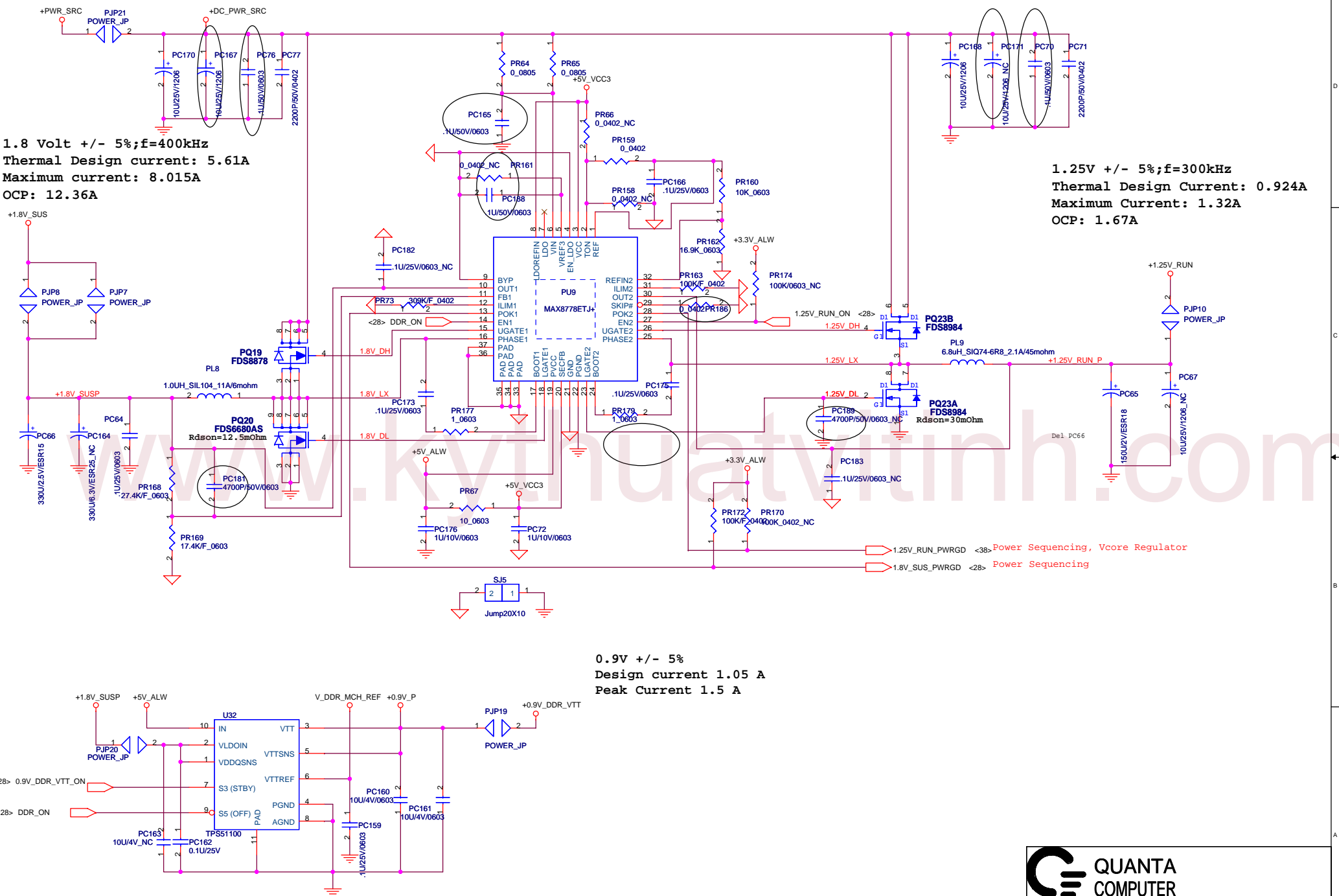


Title		
DCIN,BATT CONNECTOR		
Size	Document Number	Rev
FM5		0.1
Date:	Monday, March 05, 2007	Sheet 41 of 51

1.8 Volt +/- 5%; f=400kHz
 Thermal Design current: 5.61A
 Maximum current: 8.015A
 OCP: 12.36A

1.25V +/- 5%; f=300kHz
 Thermal Design Current: 0.924A
 Maximum Current: 1.32A
 OCP: 1.67A

0.9V +/- 5%
 Design current 1.05 A
 Peak Current 1.5 A



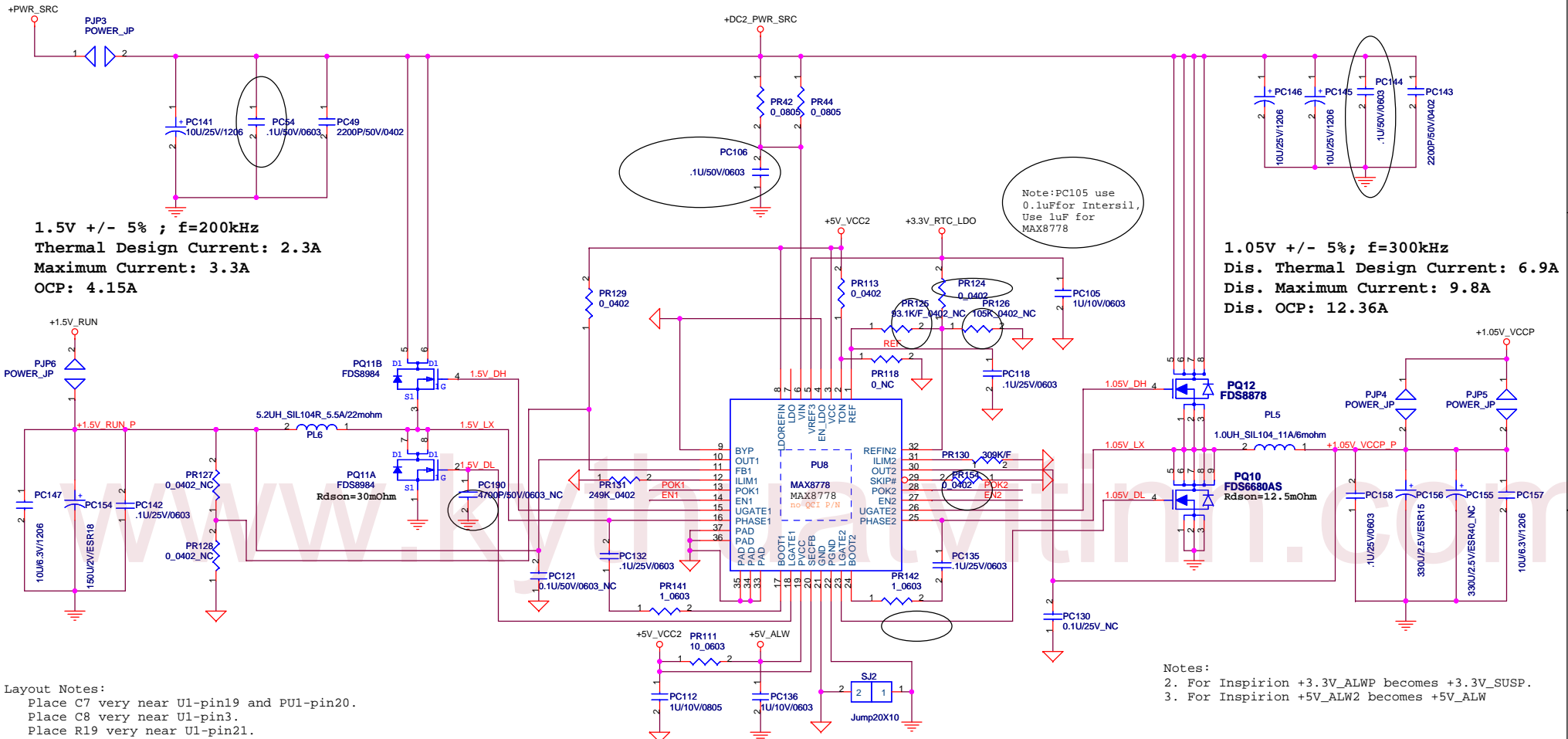
QUANTA COMPUTER

Title: 1.25V, 1.05V, 1.8V, 0.9V

Size: FMS	Document Number: FMS	Rev: 0.1
-----------	----------------------	----------

Date: Monday, March 05, 2007 Sheet 42 of 51

+1.5V_RUN / +1.05V_VCCP / +3.3V_ALW / +3.3_RTC_LDO



1.5V +/- 5% ; f=200kHz
Thermal Design Current: 2.3A
Maximum Current: 3.3A
OCP: 4.15A

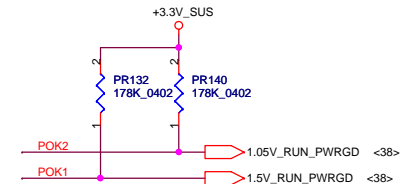
1.05V +/- 5% ; f=300kHz
Dis. Thermal Design Current: 6.9A
Dis. Maximum Current: 9.8A
Dis. OCP: 12.36A

Layout Notes:

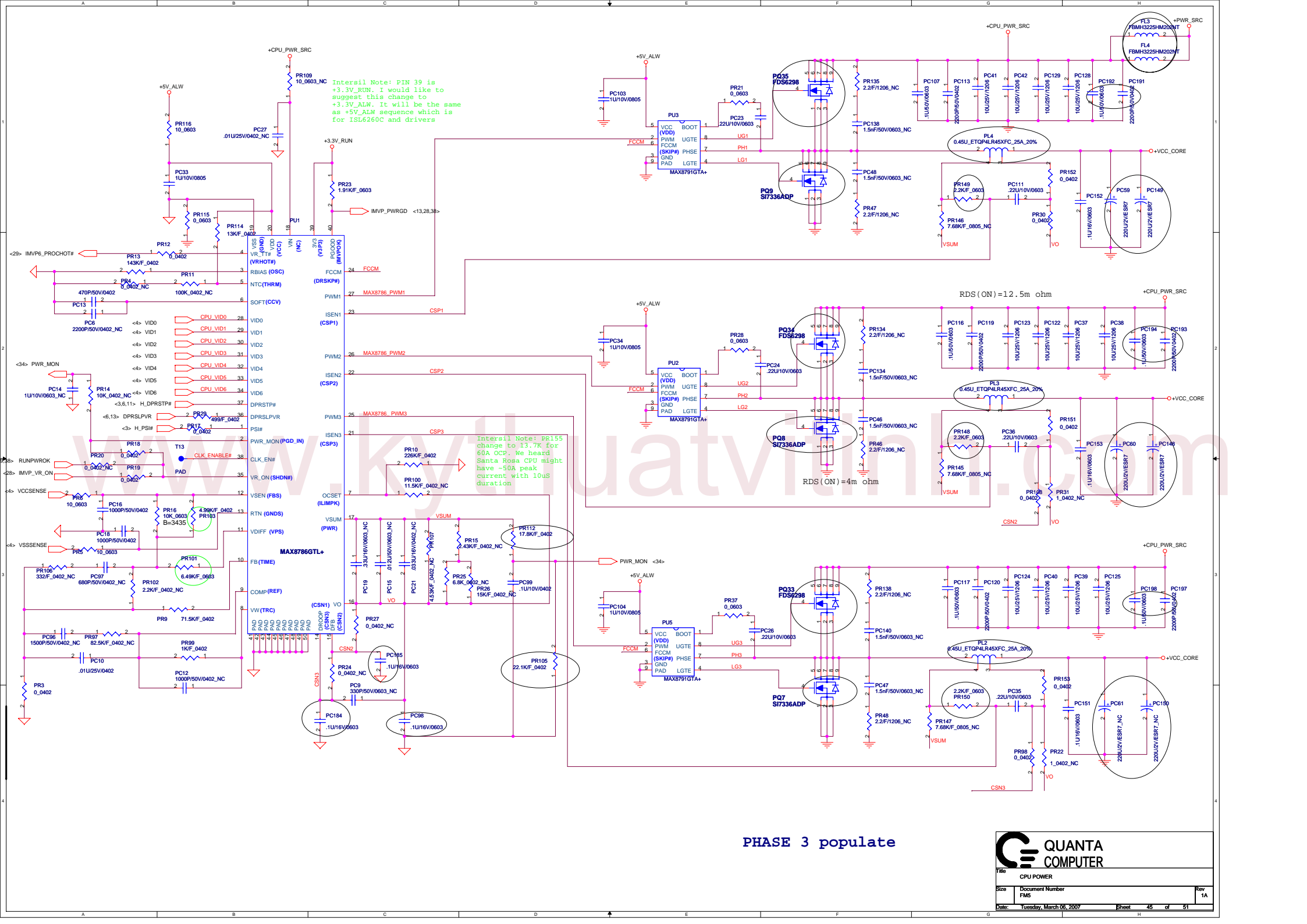
- Place C7 very near U1-pin19 and PU1-pin20.
- Place C8 very near U1-pin3.
- Place R19 very near U1-pin21.
- Minimize loop including Q4, L2, C11, C12 and R19.
- Minimize loop including Q2, L3, C17, C18, C19 and R19.
- Route GNDA_DC2 using at least 25 mil trace width.
- Minimize GNDA_DC2 trace length.
- Place C15 near U1-pin7.
- Place C20 near U1-pin5.
- Place R7 near U1-pin11.
- Place R12 near U1-pin31.
- Place R3, C10 near U1-pins 24 and 25.
- Place R2, C9 near U1-pins 16 and 17.
- Route +1.05V_BOOT, +1.05V_BOOST, +1.5V_BOOT, +1.5V_BOOST using 25mil trace width and minimize lengths.
- Connect large copper fill areas to PQ1, PQ2, PQ3 and Q4 signals for thermal improvement.
- Minimize length of +1.5V_RUN_PL and +1.05V_VCCP_PL.
- Place C1, C2, C3, C22 very near Q3-pins 5, 6, 7, 8.
- Place C4, C5, C6, C23 very near Q1-pins 5, 6, 7, 8.
- Route +DC2_PWR_SRC using 50 mil trace width and minimize length.
- Route OUT1 and OUT2 away from inductor and switch-node.
- Sense Vout directly at output bulk cap.

Notes:

- 2. For Inspirion +3.3V_ALWP becomes +3.3V_SUSP.
- 3. For Inspirion +5V_ALW2 becomes +5V_ALW



Title		
1.5V,1.05V		
Size	Document Number	Rev
FMS		1A
Date:	Monday, March 05, 2007	Sheet 43 of 51



Interisil Note: PIN 39 is +3.3V_RUN. I would like to suggest this change to +3.3V_ALW. It will be the same as +5V_ALW sequence which is for ISL6260C and drivers

Interisil Note: PR155 change to 13.7K for 60A OCP. We heard Santa Rosa CPU might have -50A peak current with 10uS duration

PHASE 3 populate

QUANTA COMPUTER

Title: CPU POWER

Size	Document Number	Rev
FMS		1A

Date: Tuesday, March 06, 2007 Sheet 45 of 51

POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	ON
S4 (Suspend to DISK) / M1	LOW	HIGH	HIGH	LOW	HIGH	ON	ON	ON	OFF	ON
S5 (SOFT OFF) / M1	LOW	HIGH	LOW	LOW	HIGH	ON	ON	ON	OFF	ON
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State \ power plane	+3.3V_ALW +3.3V_RTC_LDO +3.3V_WLAN +5V_ALW +15V_ALW	+1.8V_SUS +1.8V_LOM +3.3V_LAN +3.3V_SUS +5V_SUS	+0.9V_DDR_VTT +1.05V_VCCP +1.25V_RUN +1.5V_CARD +1.5V_RUN +3.3V_CARD +3.3V_CARDAUX +3.3V_R5C832 +3.3V_RUN	+3.3V_RUN_CARD +2.5V_RUN +5V_MOD +5V_RUN +5V_SPK_AMP +CPU_PWR_SRC +VCC_CORE +VDDA	+DC_IN +DC_IN_SS +PWR_SRC +RTC_CELL
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	OFF	ON
S5 S4/AC	ON	OFF	OFF	OFF	ON
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	ON

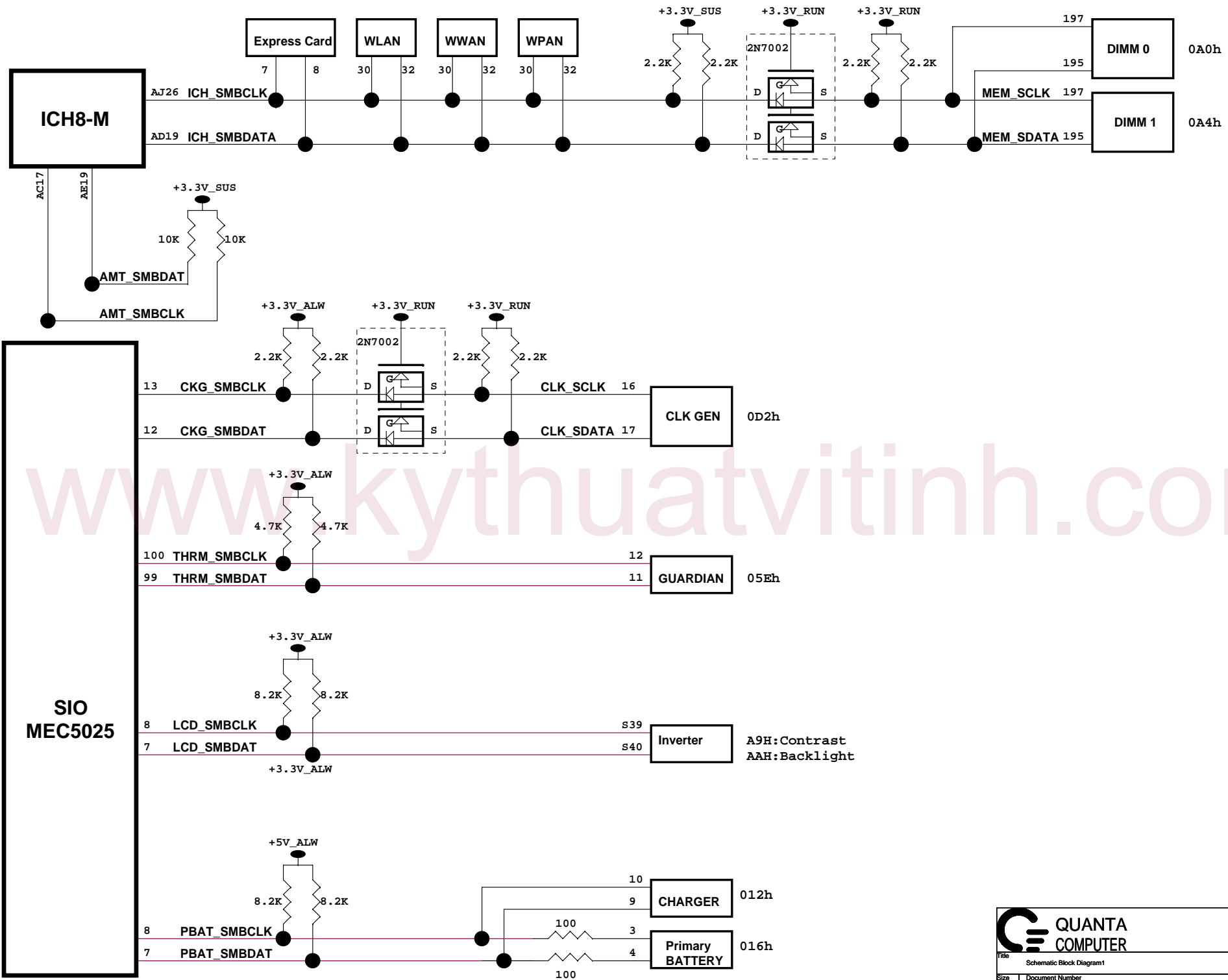
PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
BCM4401B	AD16	REQ#0 / GNT#0	PIRQB
R5C833	AD17	REQ#1 / GNT#1	PIRQC: Card reader PIEQD: 1394

ICH8-M	USB PORT#	DESTINATION
	0	Right Top
	1	Right Bottom
	2	Side TOP
	3	Side Bottom
	4	Ext. USB TOP
	5	Digital Camera
	6	Express Card
	7	WPAN/Bluetooth
	8	Ext. USB Bottom
ECE 5011	9	WWAN
	1	None
	2	None
	3	None
	4	None

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	MINI CARD-3 WPAN
Lane 4	Express Card
Lane 5	None
Lane 6	None





www.kythuatvithinh.com




Model	Item	Page	Date	ECN Number	Item Id	Rev.	Issue Description	Solution Description	
C/G DISCRETE	1	39-45	7/13/2006					Update PWR schematics	
	2	13,29	9/20/2006				S3 resume fail	Move PLTRST_DELAY# from EC to ICH8	
	3	11	9/20/2006				2nd SATA HDD can't recognize	Move 2nd SATA from port 1 to port 2	
	4	38	9/20/2006				Gfx card timing error	Disconnect GFX_PWRGD to system (Delete R463)	
	5	38	9/20/2006				Gfx card timing error	Disconnect +1.8V_RUN detect circuit to system (Delete Q47)	
	6	39-45	9/21/2006					Update PWR schematics	
	7	23	9/21/2006					Add +1.8V_RUN for SATA buffer test (CON4.20-21-22-42-43-44)	
	8	37	10/2/2006				Update WLAN LED implementation.With the current implementation, there is a possibility for backdrive from the WLAN LED control signal to +3.3V_RUN while in S3 / S4 / S5. With the voltage rail being +3.3V_WLAN, there is a high probability that the LED will be illuminated while in S3 / S4 / S5.	Please change the WLAN LED implementation to advice from Dell.	
	9	13	10/2/2006				Intel has advised that the pull-up on LINKALERT# be depopulated and that the pull-up on GPIO14 be 8.2k. Please update.	Depop R247 & change R227 from 10K ohm to 8.2K ohm	
	10	28,33	10/11/2006				In order to leverage the M07 implementation, the sniffer LED circuit needs to be modified. The MEC5025 pins are being changed from active high to active low.	Change back VC08 design, rename SNIFFER_YELLOW to SNIFFER_YELLOW#, SNIFFER_GREEN to SNIFFER_GREEN# and remove R507 and R510.	
	11	28,29	10/11/2006				Move DOCK_SMB_PME from MEC5025 SGPIO37 to ECE5018/5011 GPIOC0.Move DOCK_SMB_ALERT# from ECE5018/5011 GPIOC0 to MEC5025 SGPIO37	DOCK_SMB_PME# should be pulled up to +3.3V_ALW DOCK_SMB_ALERT# should be pulled up to +5V_ALW	
	12	28,38	10/11/2006				Add ATI_Intel to MEC5025 pin 14 and tie to GND.This connection should be labeled ATI_Intel.	Remove 3.3V_LAN_PWRGD circuit from page 38 Delete 3.3V_LAN_PWRGD from MEC5025 pin 14 Add a connection from the MEC5025 pin 14 and tie to GND.	
	13	28	10/11/2006					Move ALW_PWRGD_3V_5V from MEC5025 pin 18 to pin 29	
	14	13	10/11/2006					1) Move SIO_EXT_SC# from ICH pin AG22 to ICH pin AC19 2) Delete R242 (delete DOCKED# signal)	
	15	13	10/11/2006					Reserve LOM_SMBALERT# (ICH8 AG22) & PU resistor	
	16	24	10/16/2006					Change WPAN USB port from USBP7 to USBP4	
	17	23,29	10/18/2006				Modify HDDC_EN and MODC_EN Circuits to Resolve Glitch Issue. unintentionally for a brief moment.With the current Dawson design, it has been shown that the +15V_ALW rail comes up before the +3V_ALW rail on the original HDDC_EN and MODC_EN circuits. This can cause a momentary glitch at the gate of the power FET, which may cause the FET to turn on unintentionally for a brief moment.	To resolve this issue, please use the HDDC_EN and MODC_EN circuits that are attached below. These new circuits resemble closely our other load switch circuits, but require an additional FET and changes the sense of the HDDC_EN and MODC_EN signals to active high. Please note the use of +5V_ALW2 on these circuits. The +5V_ALW2 voltage comes directly from the LDO output on the 3V/5V switcher in your M08 design.	
	18	12,14	10/18/2006				WWAN Noise - ICH improvements. Add one .1 uF cap on each USB OC (over current) trace near the ICH. Add four .1uF caps in parellel to C813 close to the ICH pins. Add four .1uF caps in parellel to C825 close to the ICH pins.	Add C871-C878 for USB OC. Add C867-C870 in parellel to C825. Add C748,C864-C866 in parellel to C813.	
	19	37	10/23/2006					Use LED_MASK# to control BT LED to prevent leakage	Add R336 & change Q13 to BJT
	20	34	10/23/2006				Change pull-up rail on 5V_CAL_SIO1# to +3.3V_SUS. Feedback from SMSC has indicated that the pull-up rail on 5V_CAL_SIO1# needs to change from +5V_SUS to +3.3V_SUS.This is necessary because the GPIO on the EMC4001 is 3V tolerant, not 5V.	Pullup is at reference designator R298.	
	21	28	10/23/2006				Due to the power on defaults of the MEC5025, the pull-downs on the KSI lines of the MEC5025 need to be stronger, to avoid pulses from powering on certain power rails. Please do the following: 1. Change pull-down on SUS_ON to 2.7k 2. Change pull-down on RUN_ON to 2.7k	Change R355,R358 to 2.7K	
	22	24	10/23/2006				Add SMBus isolation circuitry for WLAN.Add isolation circuitry for SMBus on WLAN.		



Model	Item	Page	Date	ECN Number	Item Id	Rev.	Issue Description	Solution Description
C/G DISCRETE	23	17	10/26/2006				Chipset side spec. Differential CLK raise/fall slew rate is 2.5-8 V/ns, only express card and mini card is 0.6-4V/ns. BITCLK rise/fall slew rate in 1-3 V/ns &	Change serial resistors (PR4,PR5,PR10,PR12,PR13) to meet the CLK SPEC
	24	37	10/26/2006				Change LED control method	
	25	37	10/26/2006				Add OR gate for BT_ACTIVE	
	26	13	10/26/2006				M08 GPIO A14 update. Original EC5011 pin66 CCD_VDD_ON move to IC8 pinAD10 GPIO48 and add 100K ohm pull down.	Move CCD_VDD_ON from EC5011 pin66to IC8 pin AD10 GPIO48 and add 100K ohm pull down.
	27	25	10/26/2006				For Comm team suggestion (GG list), pop C217 for WWAN	
	28	39 - 45	10/31/2006				PWR team updat schematics - 10/23	

www.kythatvithinh.com



**QUANTA
COMPUTER**

Title: Change List

Size	Document Number	Rev
	JM7B	1A


Date: Monday, March 05, 2007 Sheet 50 of 1

Model	Item	Page	Date	ECN Number	Item Id	Rev.	Issue Description	
C/G DISCRETE	29	24 - 25	11/1/2006				For EMI request, add RC circuit for Mini card clk request	Add R543, C880, R186, C649, R544, C181
	30	39	11/1/2006				For +3.3V_RUN inrush current, it may over OCP (12.36 A)	Change PC58 from 470 pF to 6800 pF
	31	32	11/3/2006				For AP - THN+D fail, change C306, 307 to 0.033uF/16V/X7R/1206 & C326, C329 to 1uF/16V/X7R/1206	Change C306, 307 to 0.033uF/16V/X7R/1206 & C326, C329 to 1uF/16V/X7R/1207
	32	32	11/3/2006				'PO' noise in resume from S3,S4,S5	Reserved the AUD_AMP_MUTE# for 'PO' noise
	33	39 - 45	11/09/2006				PWR team updat schemtics - 11/08	
	34	17	11/09/2006				Change R44 to 2.2K per Intel recommend value.	
	35	12 - 13	11/21/2006				Due to Intel-ICH8 uses GPIO20 pin AE11 as an Internal Strapping at power up	Move PCIE_MCARD2_DET# from GPIO20 to ICH8 GPIO5/PIRQH# pin B3.
	36	13	11/21/2006				GPIO18 is default as an output at power up, it will drive 1Hz output at power up. Per Intel this GPIO could not be connected to GND	Add 4.7K series - R547 resistor to separate it
	37	32	11/22/2006				There is potential back drive from the codec DVdd back to the AVdd supply due to an internal ESD diode	add 100kohm resistor (R253) between pin 40 and +3.3V_RUN and a 1000pF cap (C643 below) from Pin 40 to ground
	38	35 - 36	11/28/2006				GG list -- COMM team request	1.Change capacitor for U5 pin 79, 94,106 (VDDIO) (C18, C16, C25) to 47pF. 2.Change those three capacitors (C27, C37,C34) to 47pF 3.Add C644 - 47pF capacitor by the pin 57 of U5 4.Change L7 to 0805 package -BK2125LM152. & C23 to 47 pF 5.Add Ferrite Bead BK1608LM152 on 1.8V to EPHY_AVDD pin 57
	39	28-29	11/28/2006				Move DOCK_SMB_PME from MEC5025 SGPIO37 to ECE5018/5011 GPIOC0.Move DOCK_SMB_ALERT# from ECE5018/5011 GPIOC0 to MEC5025 SGPIO37	DOCK_SMB_PME# should be pulled up to +5V_ALW DOCK_SMB_ALERT# should be pulled up to +3.3V_ALW
	40	24	12/01/2006				GG list -- Seperate debug port with MINI-PCI if not necessary	Add 4 0ohm resistors for these pins
	41	24 - 25	12/01/2006				GG list -- Delete decoupling cap	Delete C222 & C424
	42	39 - 45	12/04/2006				PWR team updat schemtics - 12/04	
	43	32	12/08/2006				GG List -- Change audio AMP to TI solution	1.Change codec to TPA9040A4 2.Pop R505, C619 & C614; depop R506, R504 & R497
	44	31	12/13/2006				GG List -- Change power source for LED of dash board	Change JTP1.9 from +3.3V_RUN to +5V_ALW
	45	39 - 45	12/19/2006				PWR team updat schemtics - 12/19	
	46	28	12/25/2006				GG List -- Remove EC5025 pin15 GPIO4 AUD_AMP_MUTE# circuit.	NC R538
47	34	12/25/2006				GG List -- Add THERMATRIP_VGA# function	Pop R441,442,443 and Q35, C568 for THERMATRIP_VGA# trip.	
48	33	12/28/2006				Modify CCD power control soft start function	Change C403 , R284 connect method	



Model	Item	Page	Date	ECN Number	Item Id	Rev.	Issue Description
C/G DISCRETE	49	22	1/11/2006				XD card detect function error
	50	29	1/11/2006				Base on A16 GPIO : Change net name from BID2 to CHIPSET_ID1
	51	37	1/24/2007				Add 0ohm_NC(R571) resistor pad connected from Coex1_BT_Active_MINI to Coex1_BT_Active
	52	32	1/24/2007				Audio solution for pass EMI 225MHz and 451MHz radiation emission test. Added R560, R561, R562 and R563 on AUD_SPK_L1, AUD_SPK_L2, AUD_SPK_R1, AUD_SPK_R2 trace
	52	33	1/24/2007				Audio solution for pass EMI 225MHz and 451MHz radiation emission test. Added R564, R565, R566 and R567 on AUD_LINE_OUT,AUD_HP_OUT
	53	13	1/24/2007				GG List -- CCD_ON pull down R258 100K NC.
	54	37	2/5/2007				Blue LED brightness is too high Change R30,R50,R75,R64 & R36 from 220 ohm to 330 ohm
	55	30	2/12/2007				Prevent SPI CLK overshoot/undershoot issue Add C896 for RC circuit but not pop it
	56	39 - 45	2/12/2007				PWR team updat schemtics - 2/12
	57	29	2/12/2007				GG List -- CIR function intermidiate issue ECE5021 pin7 PWRGD need to pull-down to GND with 0 ohm - Add R568 PD resistor & R569 series resistor (NC)
	58	44	3/1/2007				PWR team updat schemtics - 3/1
	59	17	3/2/2007				Per TDC COMM team request - Change L65 to Fine tune 14M CLK - Change R57 from 33 to 15 ohm & L65 to BLM18SG260
	60	04	3/2/2007				Per reliability issue - Move C98 to C249 De-pop C98 & pop C249

www.kythuatchinh.com

 QUANTA COMPUTER		
Title EMI & Screw hole		
Size	Document Number C & G UMA	Rev 2A
Date: Wednesday, March 07, 2007 Sheet 51 of 51		