

COMPAL CONFIDENTIAL

MODEL NAME : *QXW10*
PCB NO : *LA-7902P (DA60000PV00)*
BOM P/N : *4319F831L01*
GPIO MAP: E4_VC_GPIO_map_rev_1.1

Korbel 15 UMA

Ivy/Sandy Bridge + Panther POINT(HM77 w/o Vpro,/QM77 w/Vpro)

2012-03-07

REV : 1.0 (A00)

@ : Nopop Component


CONN@ : Connector Component

	MB Type	BOM P/N	
*	TPM(R1)	4319F831L01	1@ 3@ 5@
	TPM DIS(R1)	4319F831L02	2@ 3@
	TPM(R3)	4319F831L03	1@ 3@ 5@
	TPM DIS(R3)	4319F831L04	2@ 3@
*	HM77 w/o Vpro		
	QM77 w/ Vpro		
	PCH XDP		PXDP@
	HDMI LOGO		46@

Part Number	Description
DA60000PV00	PCB 0LH LA-7902P REV0 M/B UMA

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POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

USB 3.0 PORT#	Connetion
1	NA
2	JUSB1 (Left side)
3	JESA1 (Left side)
4	MLK DOCK

PCH	USB PORT#	DESTINATION
	0	JUSB (Right side-IO/B)
	1	JUSB1 (Left side)
	2	JESA1 (Left side ESATA)
	3	DOCKING
	4	WLAN
	5	WWAN
	*1 6	JMINI3(Flash)-for w/ Vpro
	*1 7	DOCKING
	8	NA
	9	JUSB (Right side-Audio/B)
	10	Express card
	11	Bluetooth
12	Camera	
13	BIO	

*1: HM76 don't support port 6,7

PM TABLE

power plane State	+15V_ALW +5V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_CORE +1.05V_RUN_VTT +1.05V_RUN	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF


need to update Power Status and PM Table

SATA	DESTINATION
SATA 0	HDD
SATA 1	ODD/ E3 Module Bay
SATA 2	NA
SATA 3	NA
SATA 4	ESATA
SATA 5	Dock

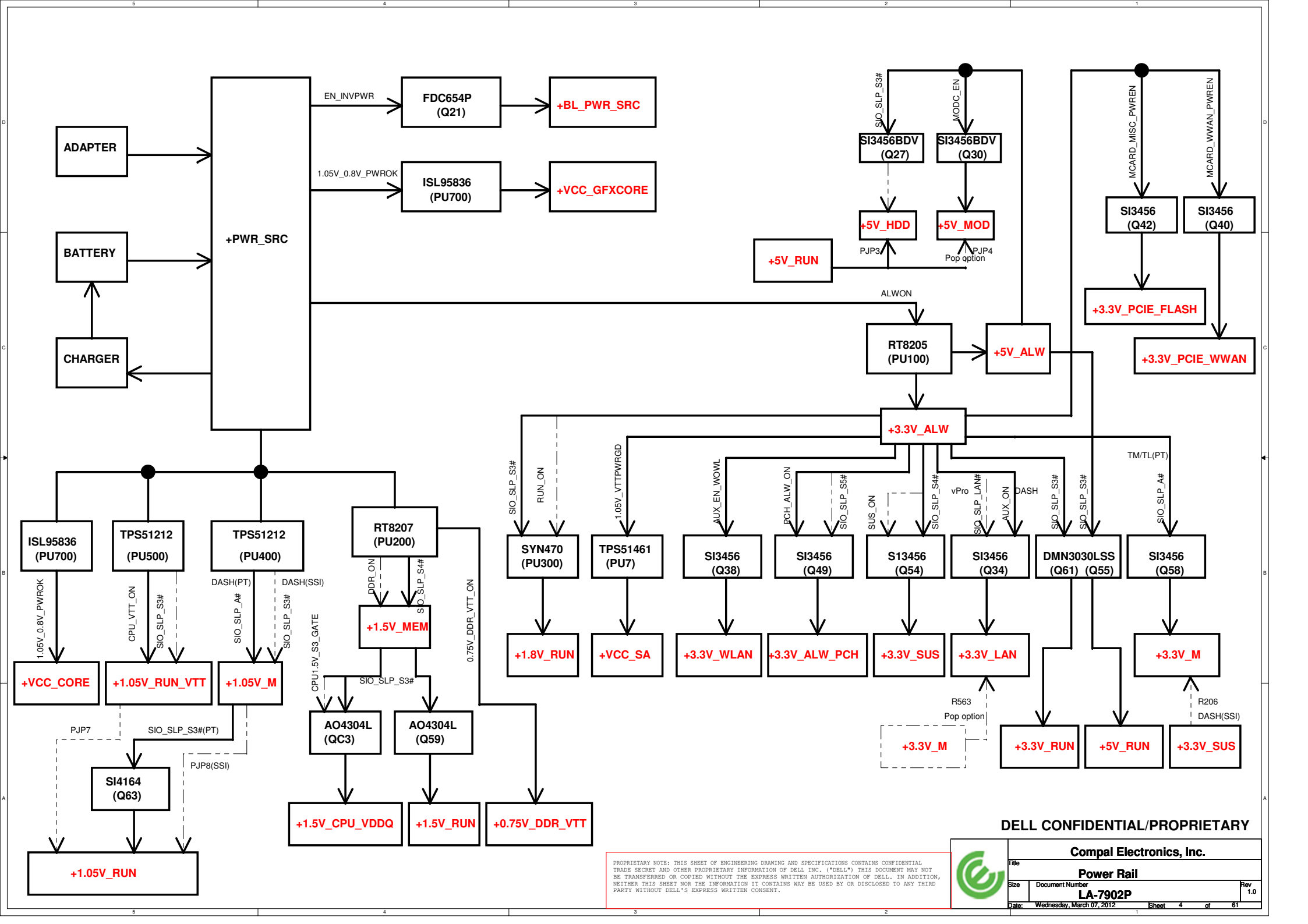
UMA DP/HDMI Port	Connetion
Port B	MB HDMI Conn
Port C	Dock DP port 2
Port D	Dock DP port 1

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	Express card
Lane 4	None
Lane 5	1/2vMINI CARD-3 PCIE
Lane 6	MMI
Lane 7	10/100/1G LOM
Lane 8	None

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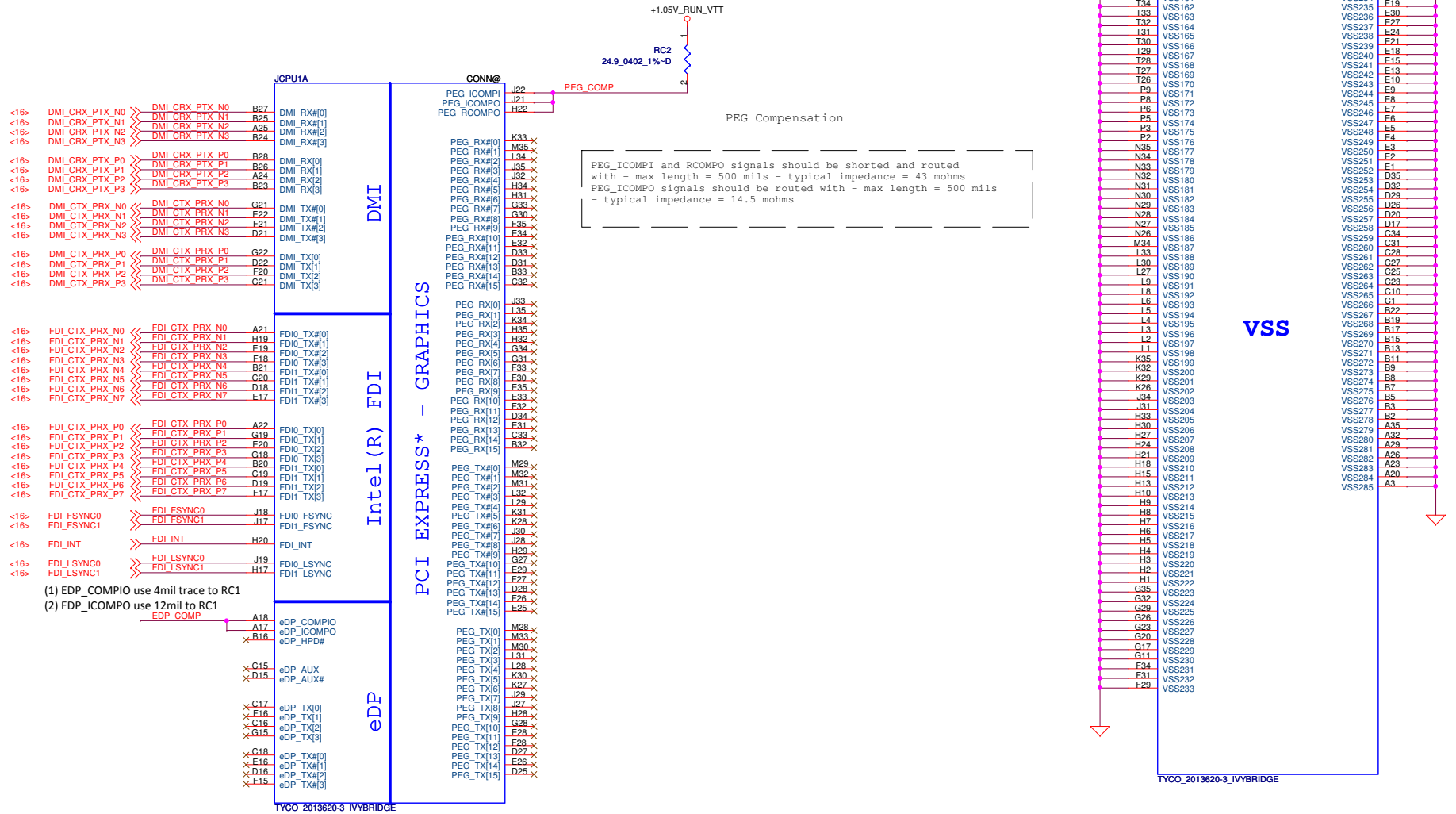
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Power Rail

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- (1) PEG_RCOMPO (H22) use 4mil connect to PEG_ICOMPI, then use 4mil connect to RC2.
- (2) PEG_ICOMPO use 12mil connect to RC2



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Ivy/Sandt Bridge (1/6)

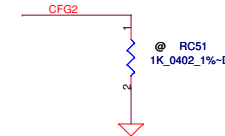
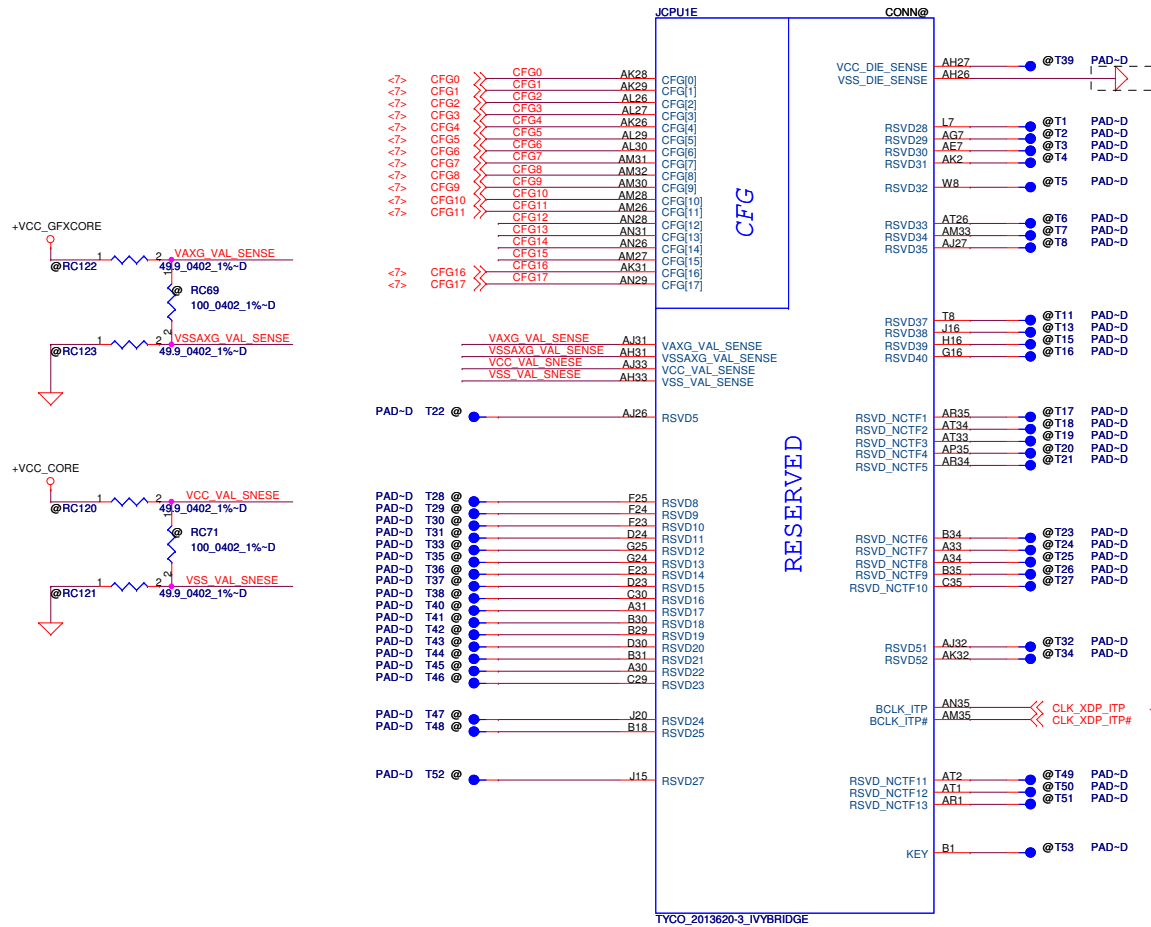
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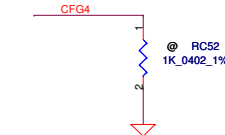
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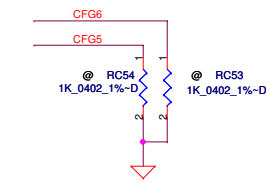
CFG Straps for Processor



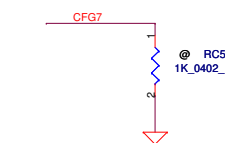
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: (Default) Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

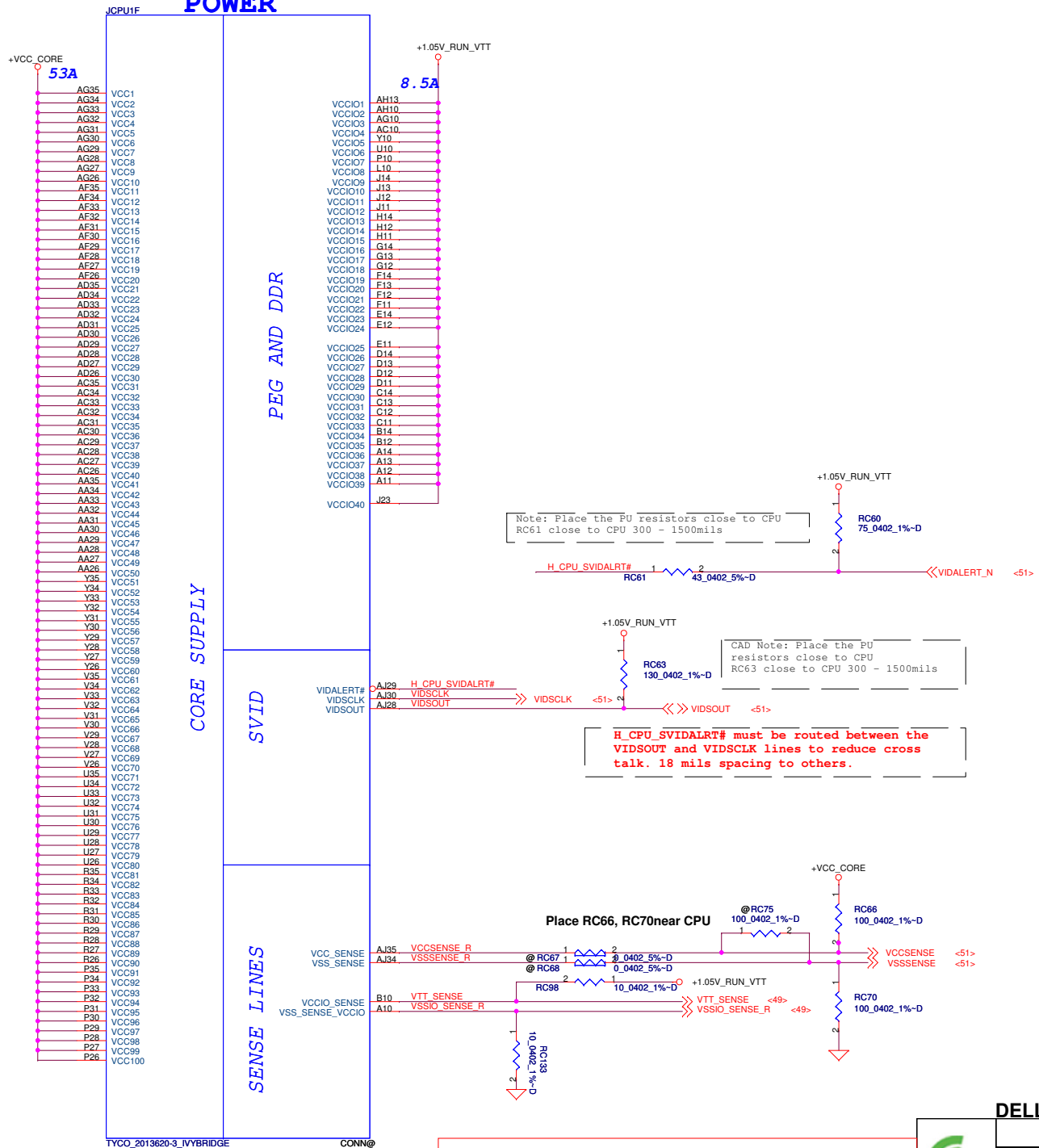
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POWER



Iccmax current changed for PDDG Rev0.7

CPU Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	0.65-1.3	53
VCCIO	1.05	8.5
VAXG	0.0-1.1	26
VCCPLL	1.8	3
VDDQ	1.5	5
VCCSA	0.65-0.9	6
+1.5V_MEM	1.5	12-16 *

*** Description**

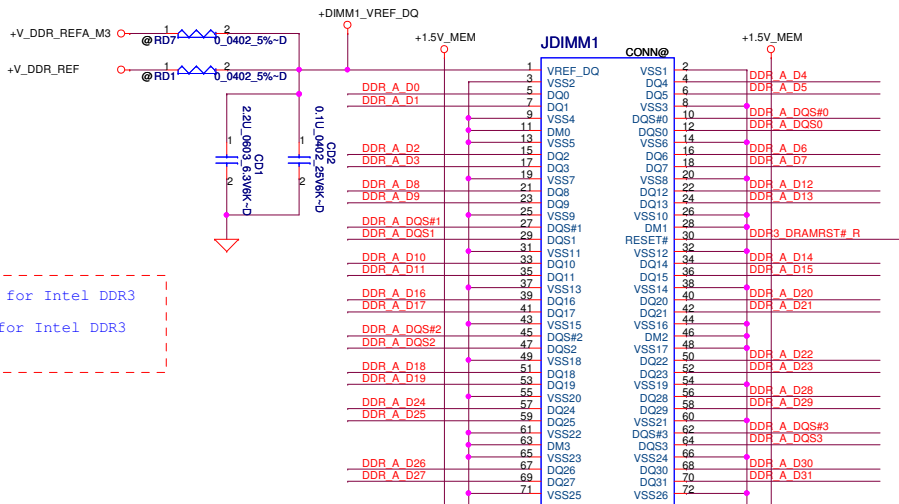
- 5A to Mem controller(+1.5V_CPU_VDDQ)
- 5-6A to 2 DIMMs/channel
- 2-5A to +1.5V_RUN & +0.75V_DDR_VTT

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2-3A to 1 DIMMs/channel

JDIMM1 H=8

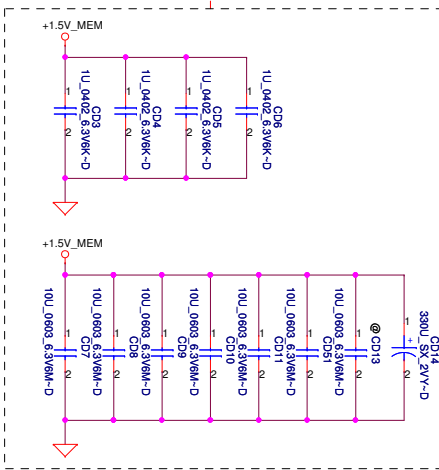
Follow CONN List_0609A

Populate RD1, De-Populate RD7 for Intel DDR3 VREFDQ multiple methods M1
 Populate RD7, De-Populate RD1 for Intel DDR3 VREFDQ multiple methods M3

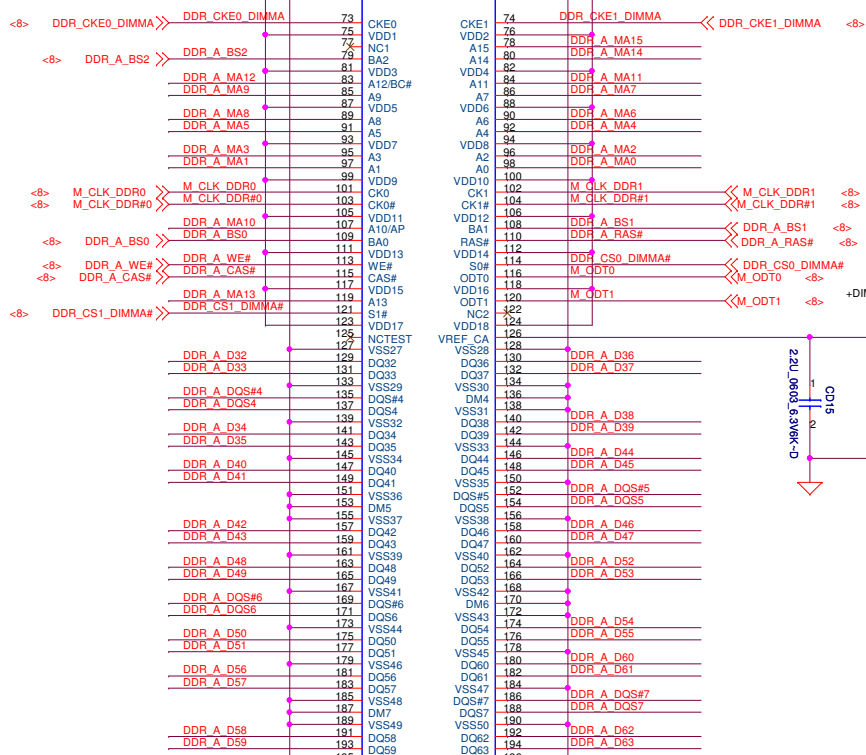
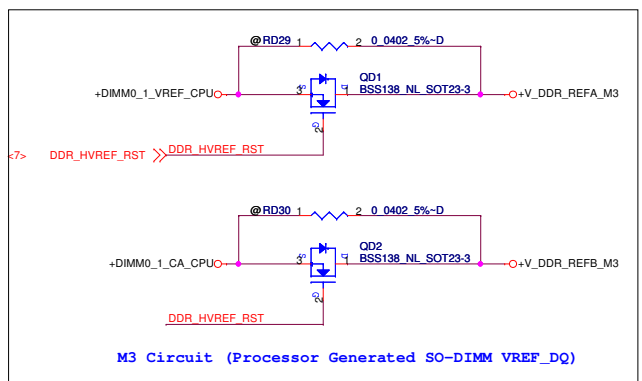
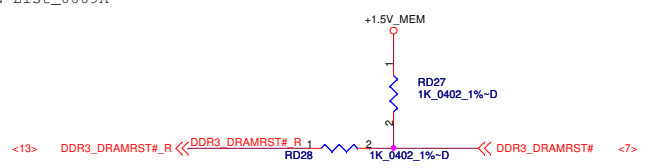
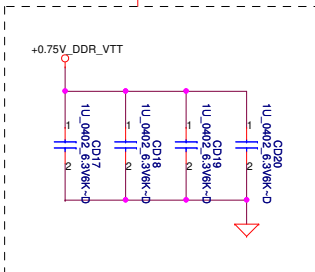
All VREF traces should have 10 mil trace width



Layout Note:
Place near JDIMM1



Layout Note:
Place near JDIMM1.203,204

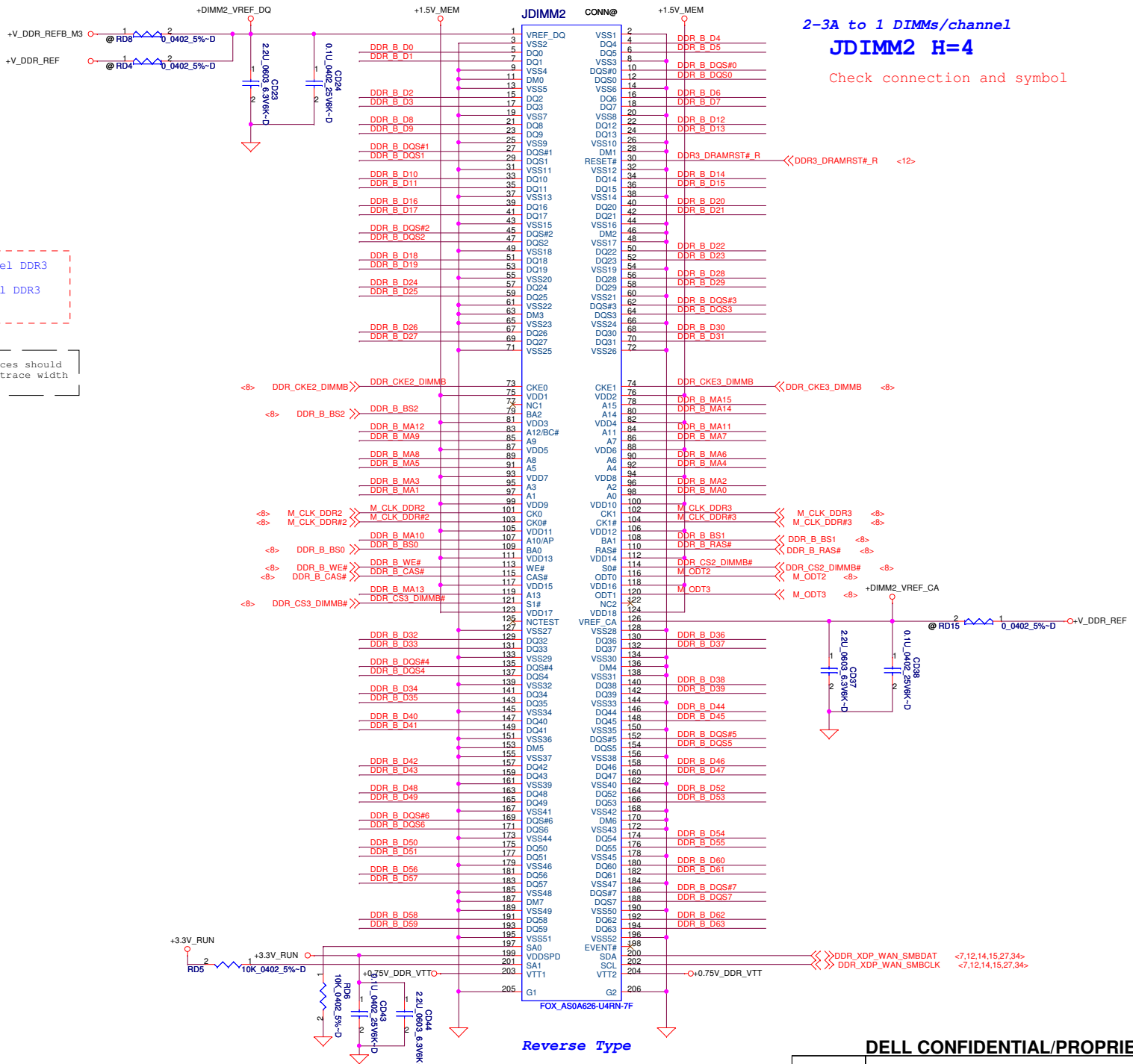


Reverse Type

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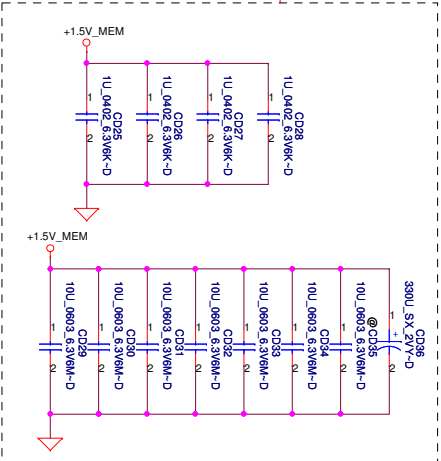


Populate RD4, De-Populate RD8 for Intel DDR3
 VREFDQ multiple methods M1
 Populate RD8, De-Populate RD4 for Intel DDR3
 VREFDQ multiple methods M3

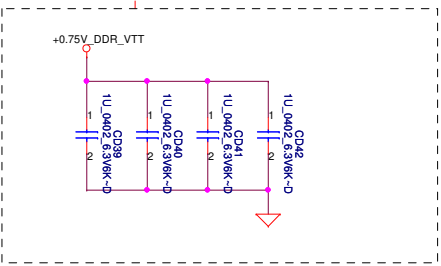
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 <8> DDR_B_DQ[0..63] <<>>
 <8> DDR_B_DQS#[0..7] <<>>
 <8> DDR_B_MA[0..15] <<>>

All VREF traces should have 10 mil trace width

Layout Note:
 Place near JDIMM2



Layout Note:
 Place near JDIMM2.203, 204

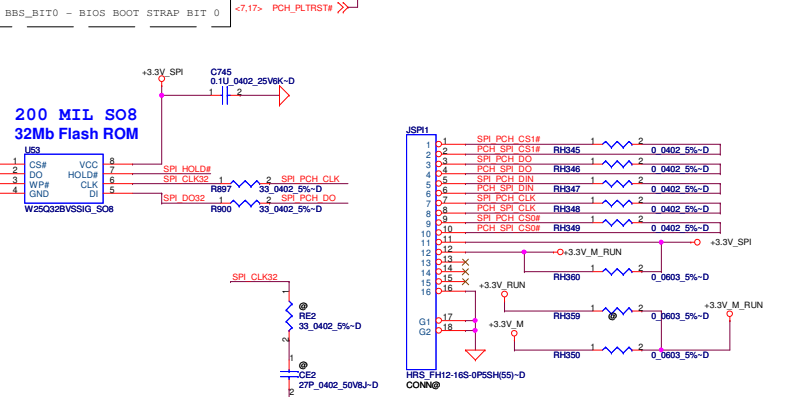
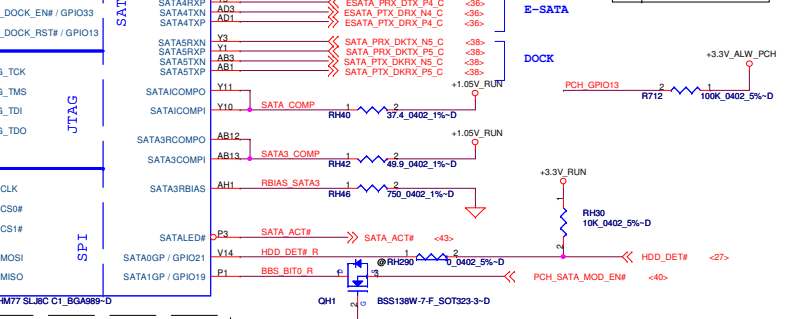
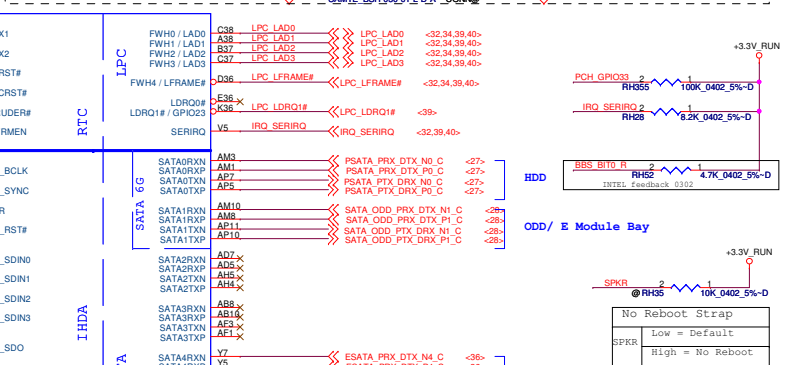
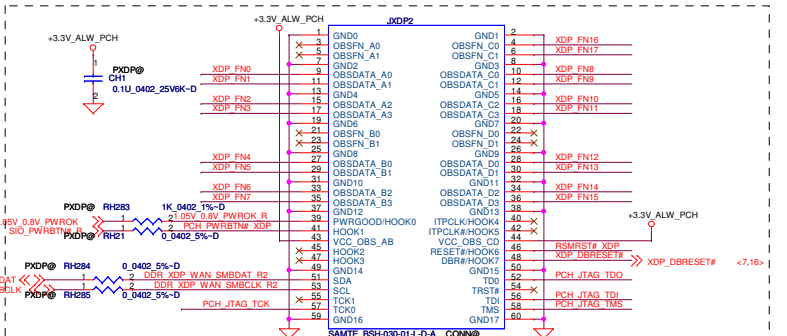
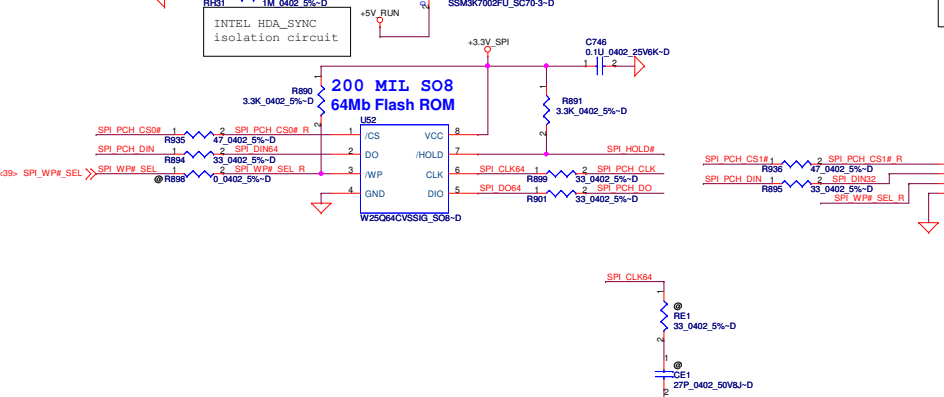
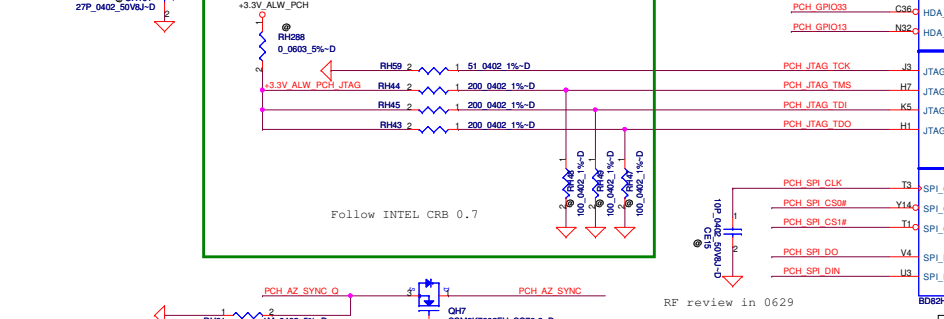
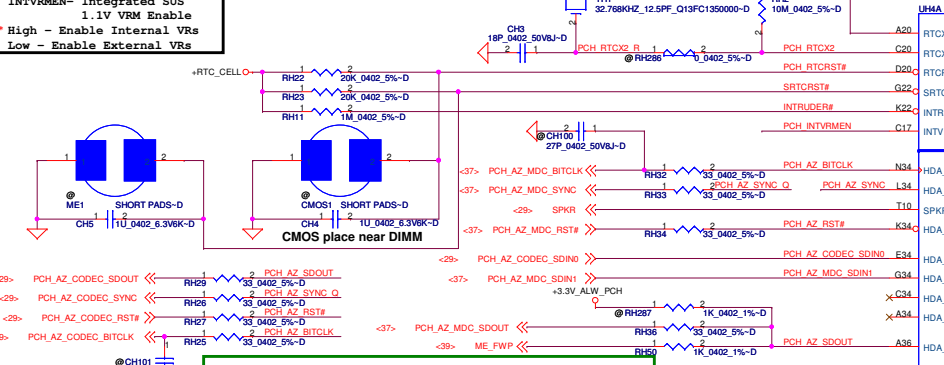
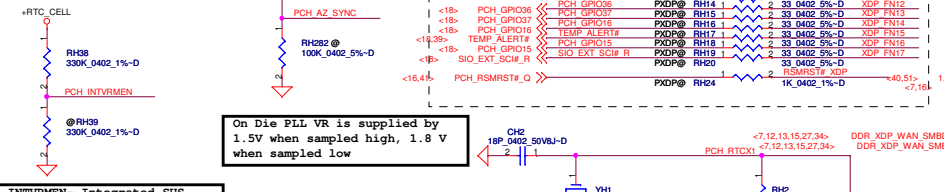


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CMOS CLR1		CMOS setting	
Shunt	Clear CMOS	Open	Keep CMOS
ME CLR1		TPM setting	
Shunt	Clear ME RTC Registers	Open	Keep ME RTC Registers



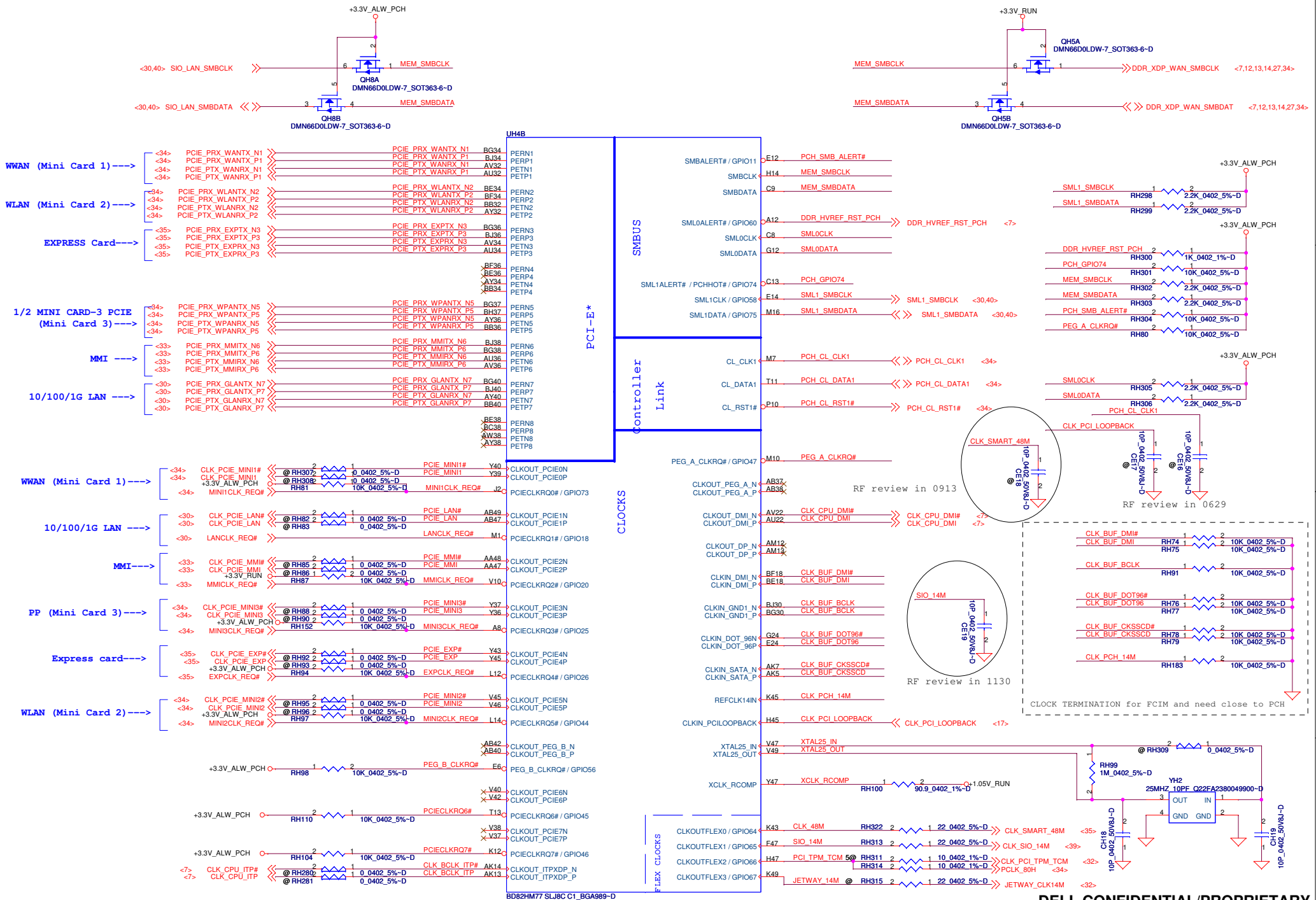
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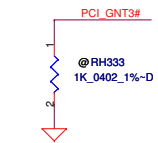
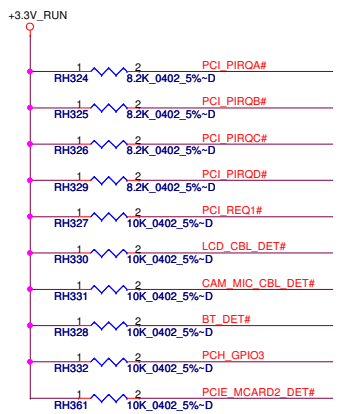
PCIE REQ power rail:
suspend: 0 3 4 5 6 7
core: 1 2

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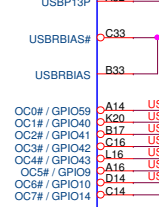
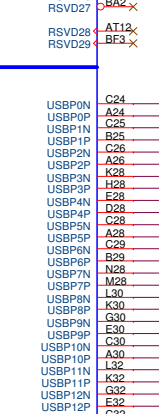
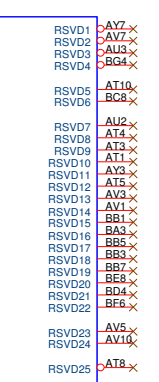
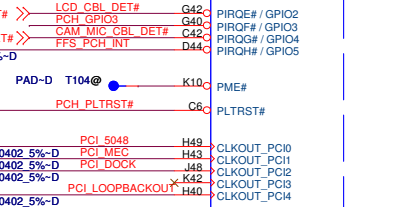
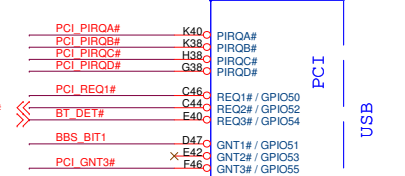
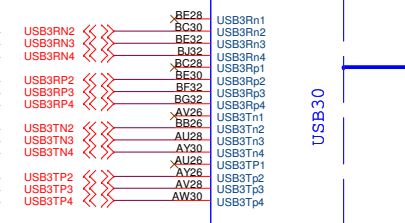
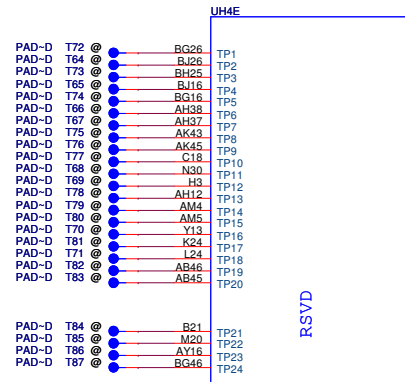
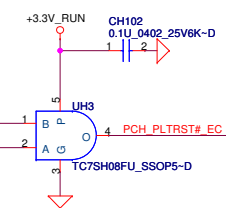
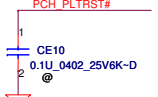
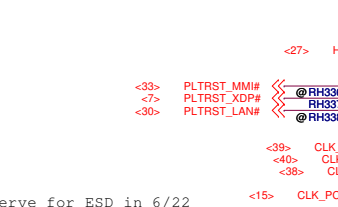


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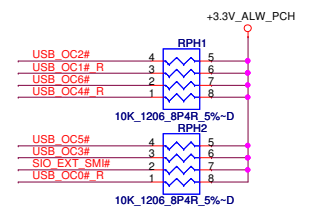


A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap High = Default

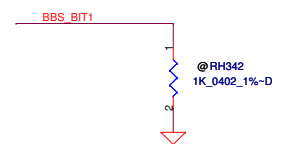


- >Back Right--JIO1
- >Left Side
- >Left side JESA1
- >MLK DOCK
- >WLAN/WIMAX
- >WWAN/UWB
- >Flash
- >DOCK
- >Non used
- >Right side--JAUD1
- >Express Card
- >Blue Tooth
- >Camera
- >BIO

Route single-end 50-ohms and max 500-mils length. Minimum spacing to other signals: 15 mils

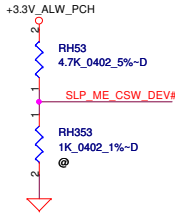


BBS_BIT1	SATA_SLPD (BBS_BIT0)	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI



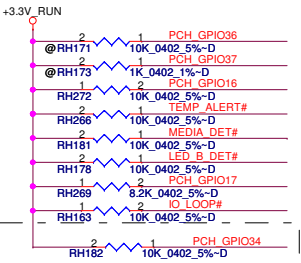
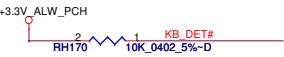
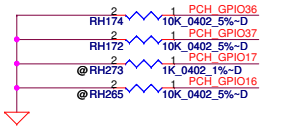
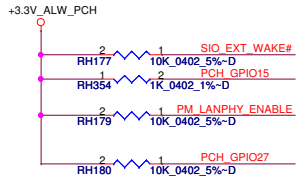
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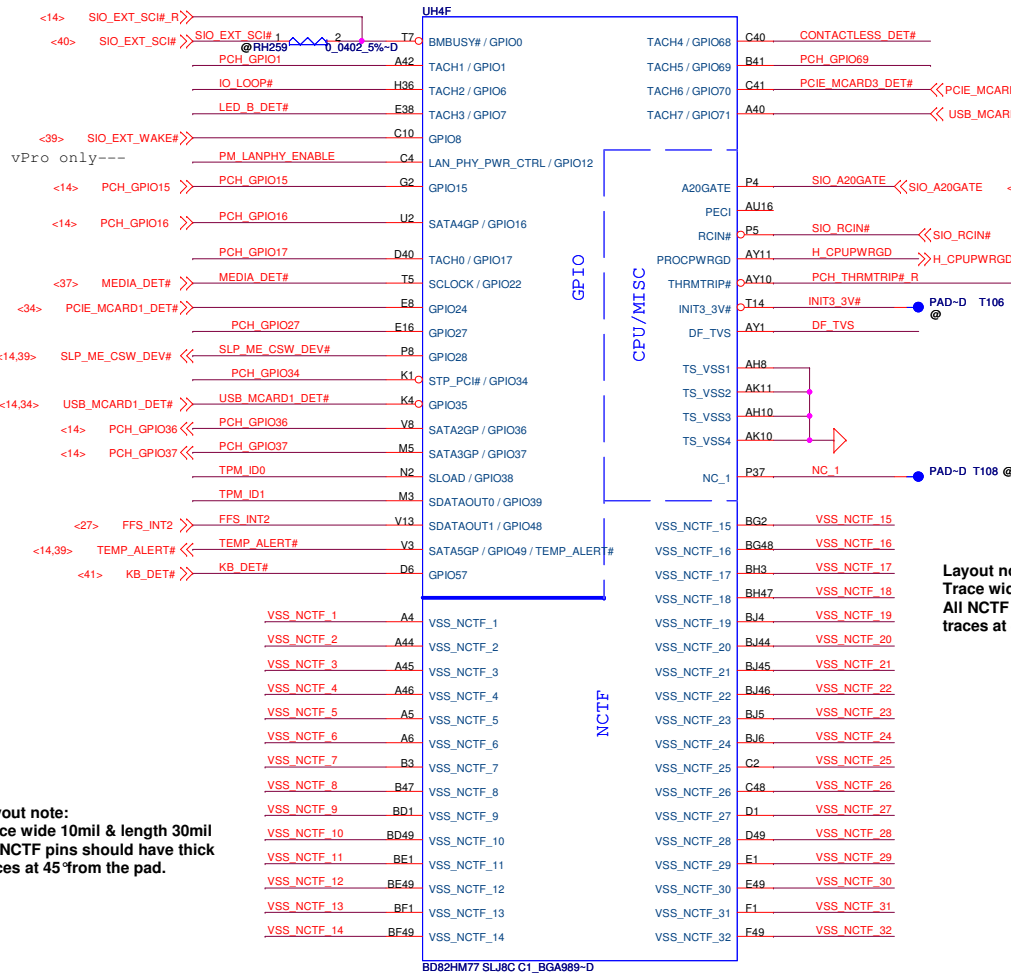


Note: PCH has internal pull up 20k ohm on E3_PAID_TS_DET# (GPIO27)

SLP_ME_CSW_DEV#	PLL ON DIE VR ENABLE
ENABLED - HIGH DEFAULT	
DISABLED - LOW	

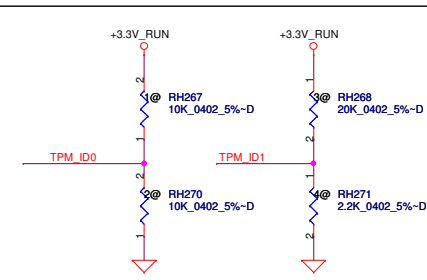


Intel review feedback in 0701

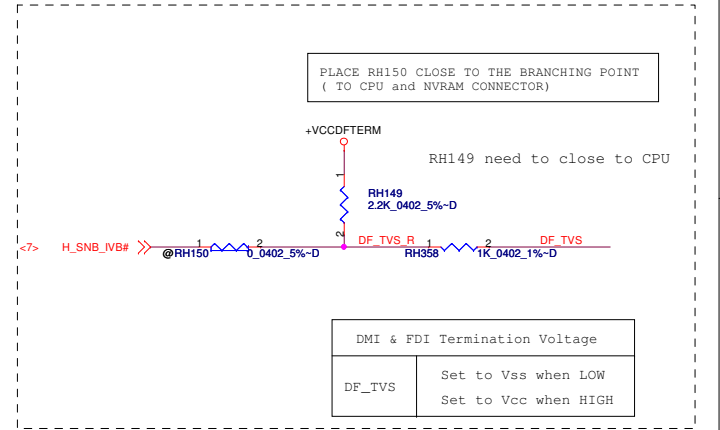
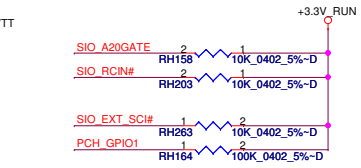
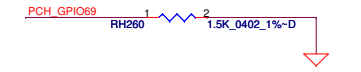
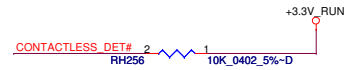


Layout note:
Trace wide 10mil & length 30mil
All NCTF pins should have thick traces at 45° from the pad.

Layout note:
Trace wide 10mil & length 30mil
All NCTF pins should have thick traces at 45° from the pad.



	TPM_ID0	TPM_ID1
China TPM	0	0
No TPM, No China TPM	0	1
TBD		
TPM	1	1



PLACE RH150 CLOSE TO THE BRANCHING POINT
(TO CPU and NVRAM CONNECTOR)

RH149 need to close to CPU

DMI & FDI Termination Voltage	
DF_TVS	Set to Vss when LOW Set to Vcc when HIGH

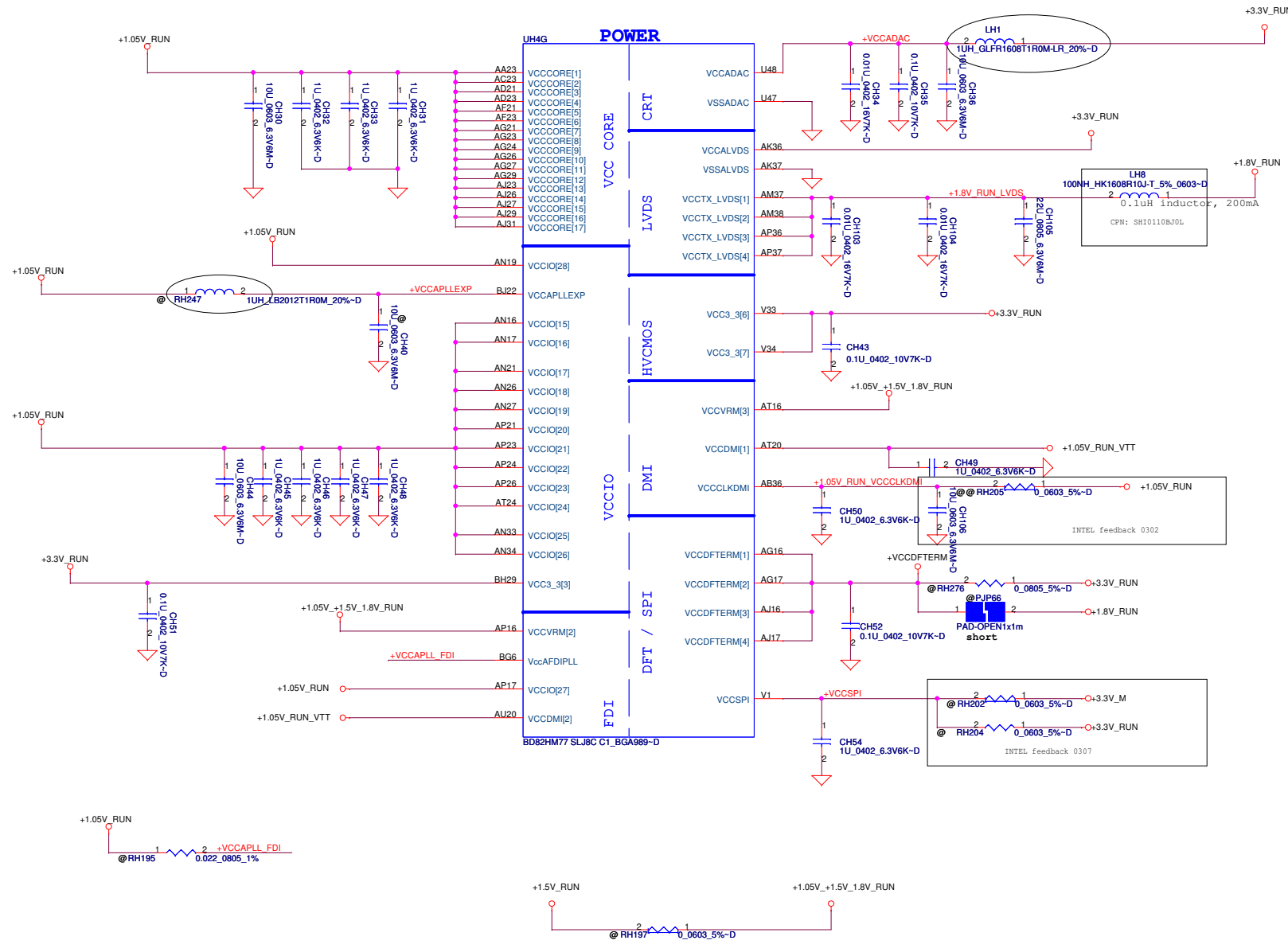
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Title: PCH (5/8)

Size: Document Number LA-7902P Rev 1.0

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PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.288
VccADAC3	3.3	0.063
VccADPFLLA	1.05	0.08
VccADPFLB	1.05	0.08
VccCore	1.05	1.7
VccDMI	1.05	0.047
VccIO	1.05	3.711
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW3_3	3.3	0.001
VCCDFTERM	1.8	0.002
VccRTC	3.3	6uA
VccSus3_3	3.3	0.126
VccSusHDA	3.3	0.01
VccVRM	1.8 / 1.5	0.167
VccClkDMI	1.05	0.07
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

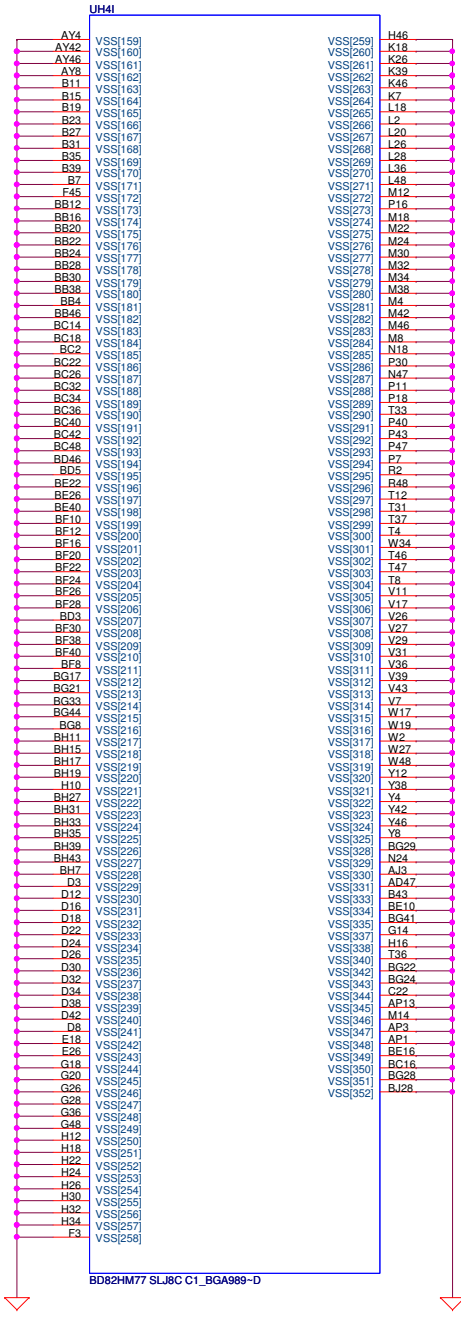
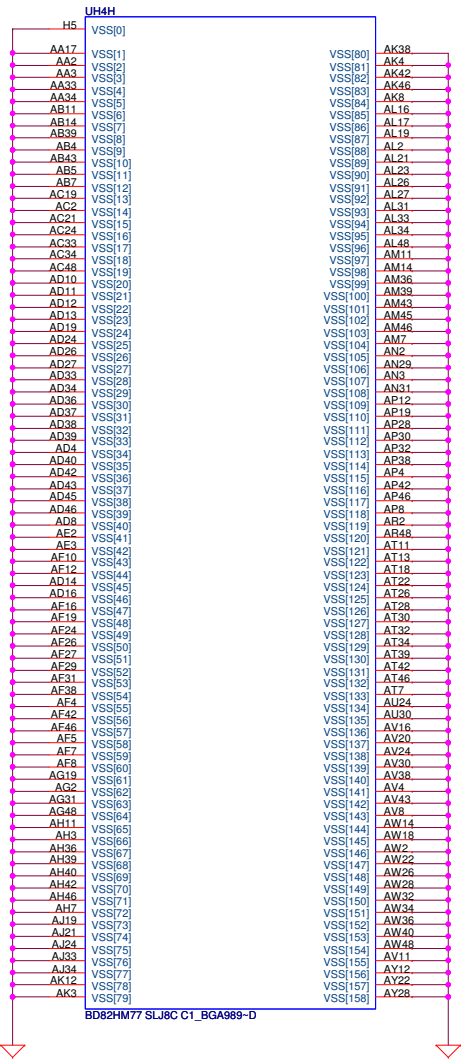
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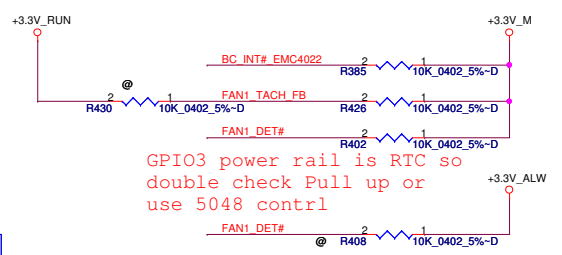
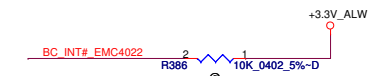
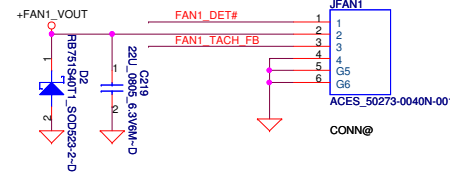
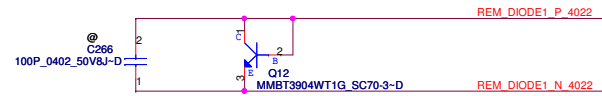
Compal Electronics, Inc.

Title: **PCH (8/8)**

Size: **LA-7902P** Rev: **1.0**

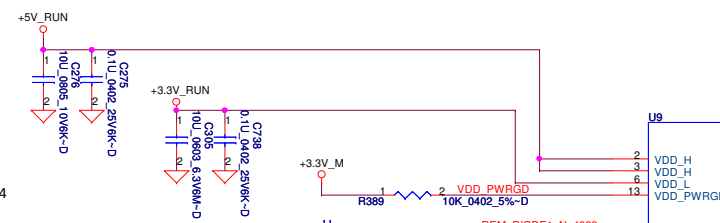
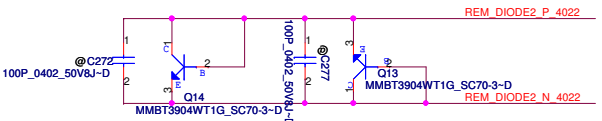
Date: **Wednesday, March 07, 2012** Sheet: **21** of **61**

Place under CPU
Place C266 close to the Q12 as possible



GPIO3 power rail is RTC so double check Pull up or use 5048 contrl

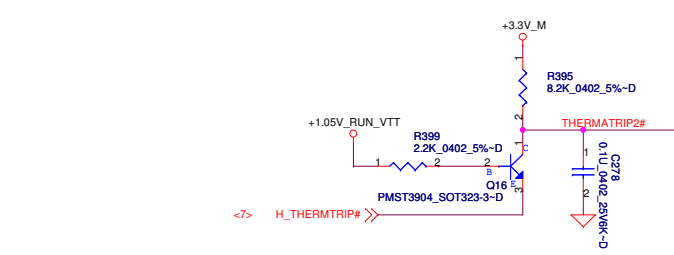
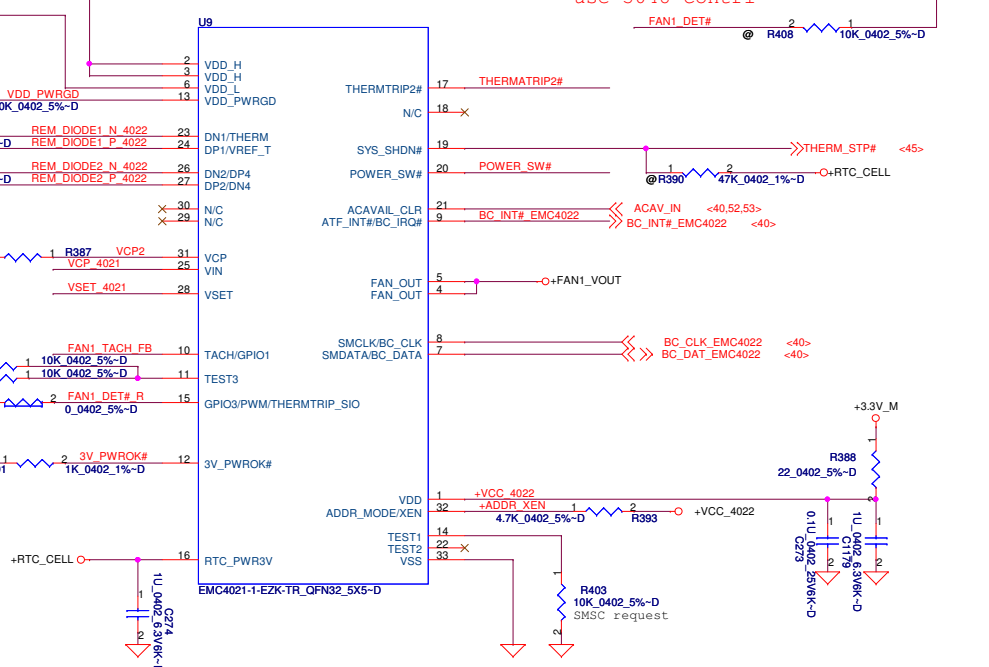
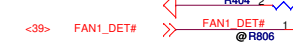
- (1) DP3/DN3 for SODIMM on Q14, place Q14 close to SODIMM and C272 close to Q14
- (2) DP5/DN5 for Skin on Q13, place Q13 close to Vcore VR choke.



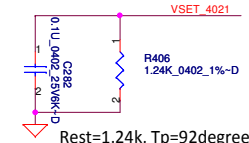
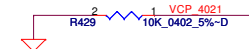
Test3

0 = 4021
1 = 4022

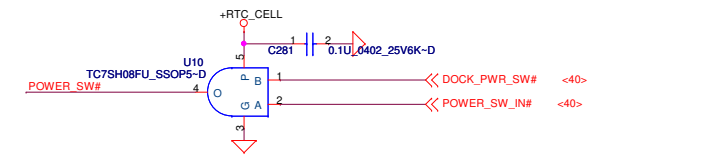
SMSC request



SMSC review in 6/22



Rest=1.24k, Tp=92degree

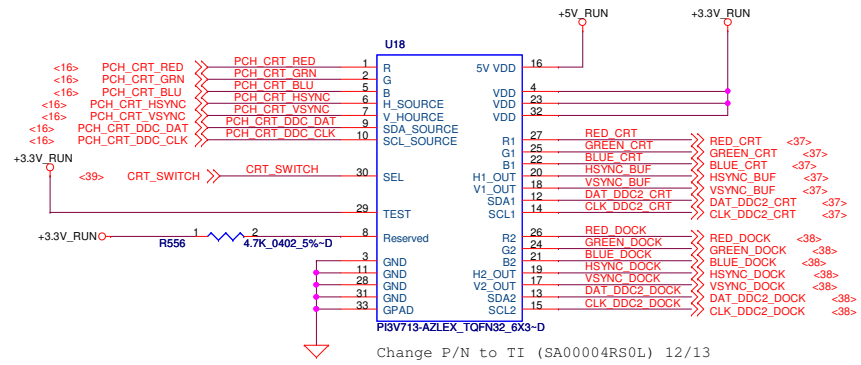


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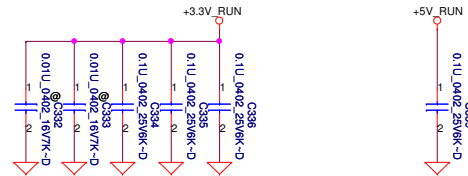
Compal Electronics, Inc.			
FAN & Thermal Sensor			
LA-7902P			
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SW for MB/DOCK

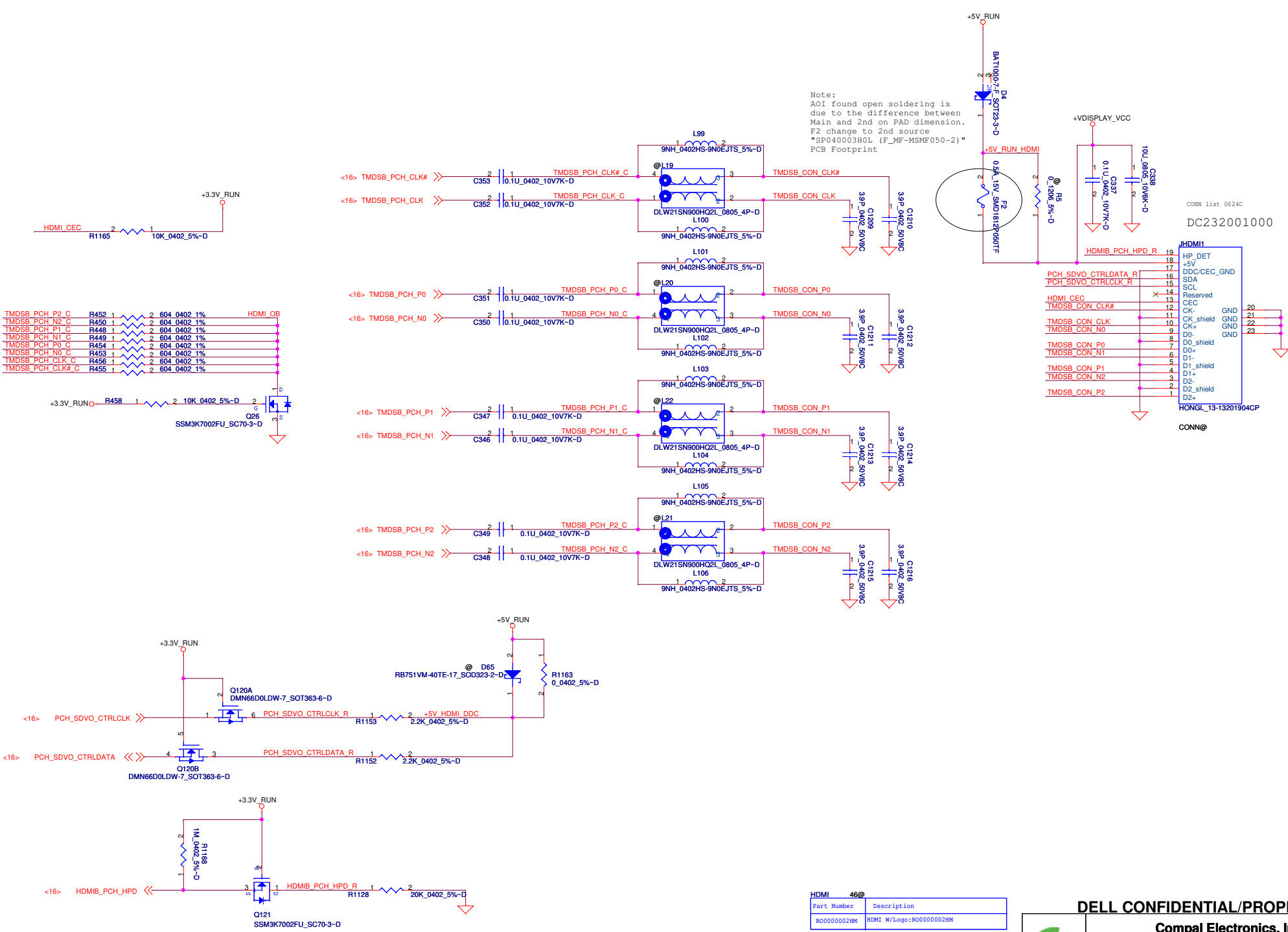


SEL1/SEL2	Chanel	Source
0	A=B1	MB
1	A=B2	APR/SPR

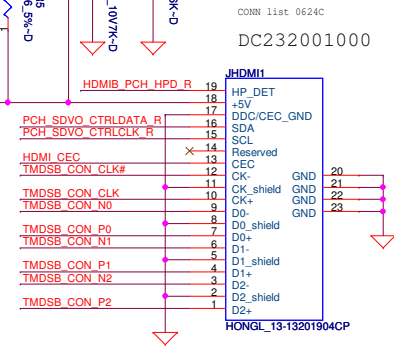


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	Compal Electronics, Inc.		
	CRT/Video switch		
	Size	Document Number	Rev
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Note:
AOI found open soldering is due to the difference between Main and 2nd on PAD dimension. F2 change to 2nd source "SP040003H0L (F_MF-MSMF050-2)" PCB Footprint



Part Number	Description
RO0000002HM	HDMI W/Logo:RO000002HM

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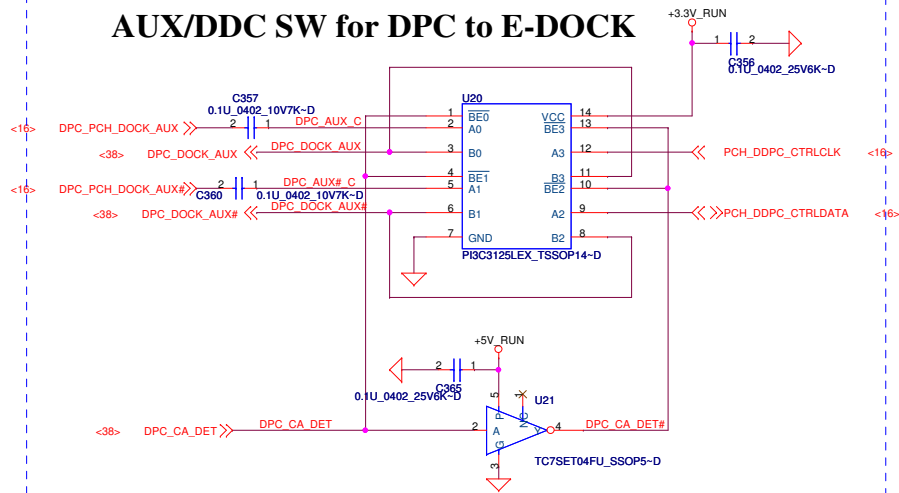
Compal Electronics, Inc.

HDMI port

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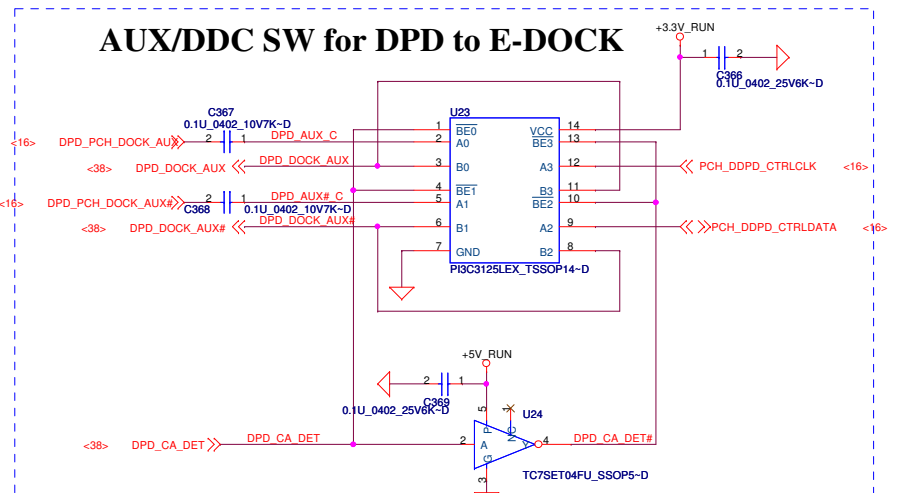
AUX/DDC SW for DPC to E-DOCK



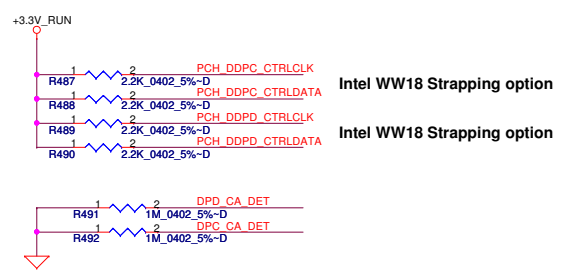
Note: When implement 2nd source, please check Vil and Vih spec is meet main source spec

There is a new die for PI3C3125. Sample available on May.

AUX/DDC SW for DPD to E-DOCK



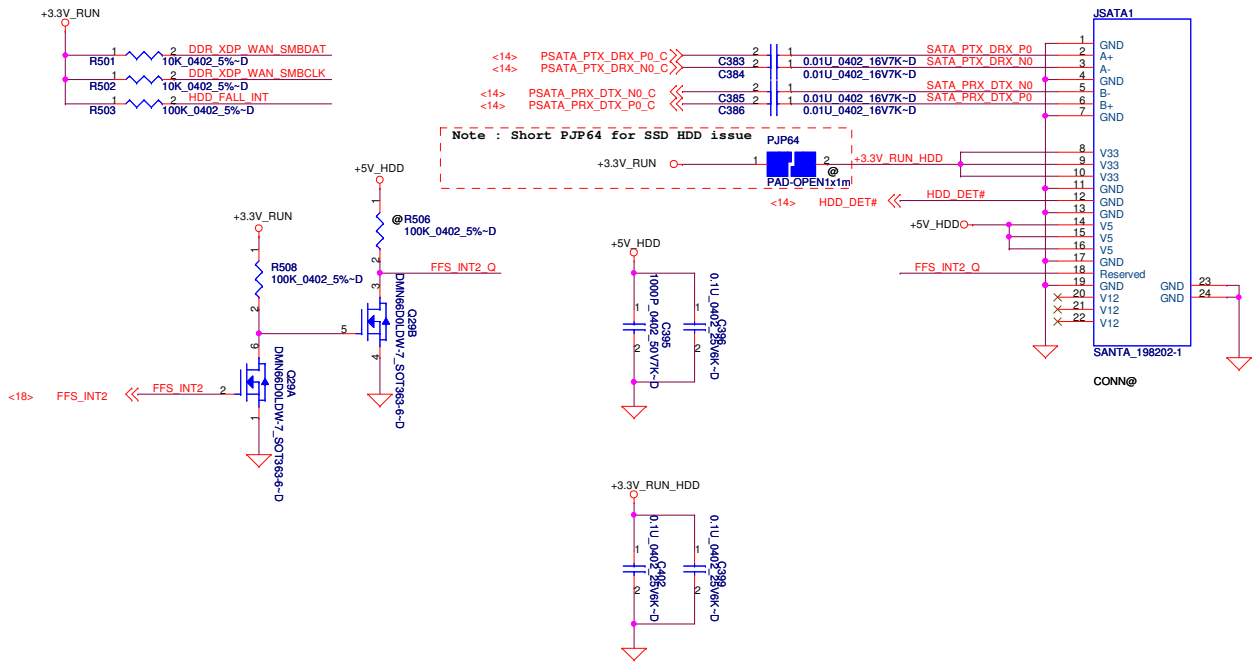
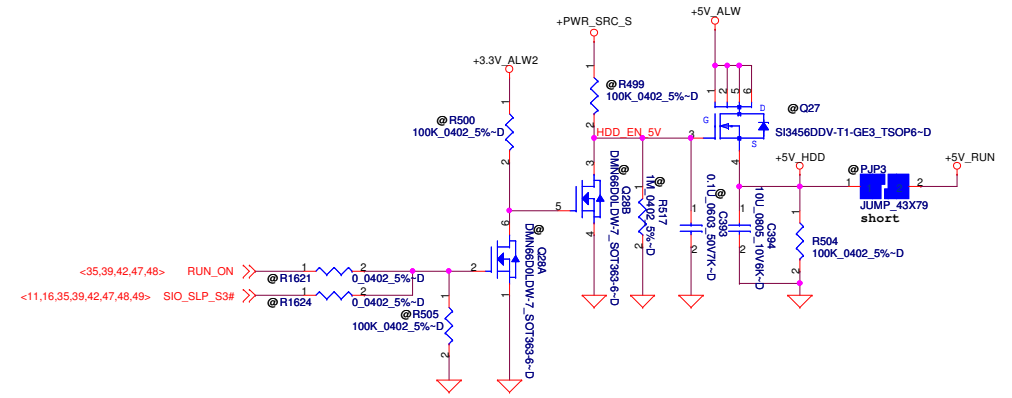
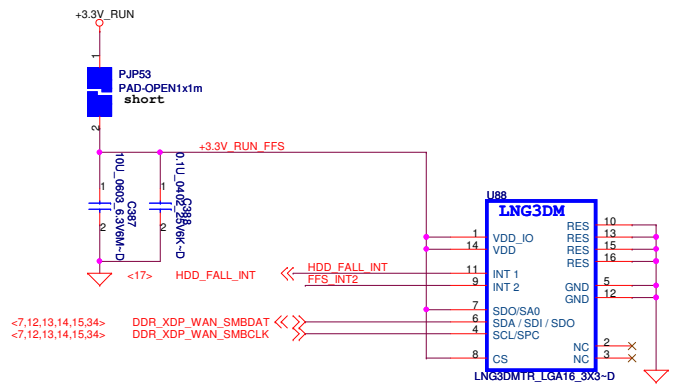
Note: When implement 2nd source, please check Vil and Vih spec is meet main source spec



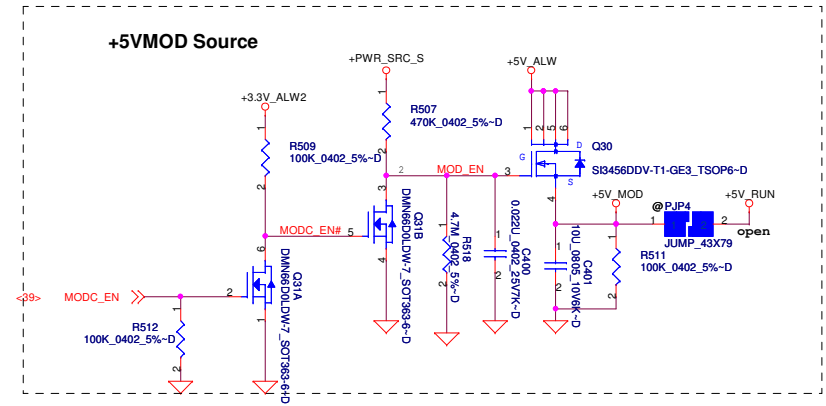
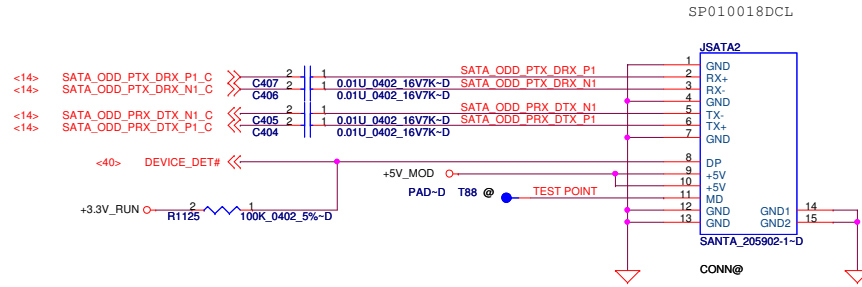
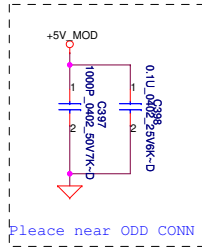
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Title DP SW		
Size	Document Number LA-7902P	Rev 1.0
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For ODD



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Title: **ODD CONNECTOR**

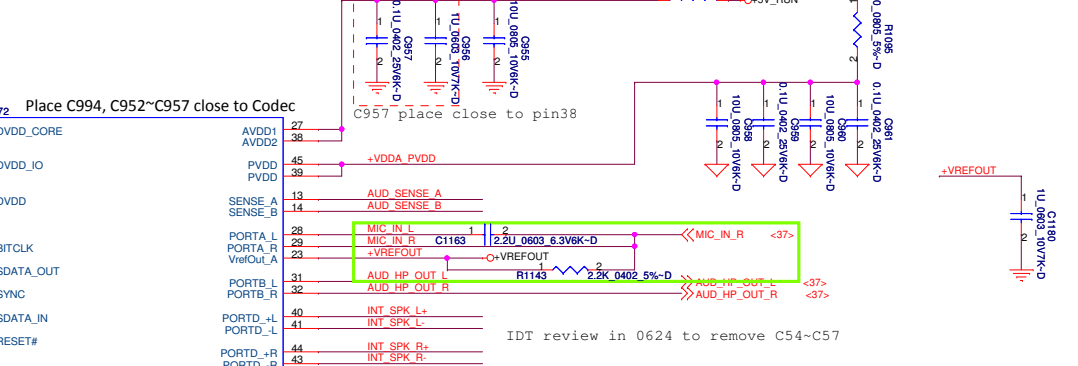
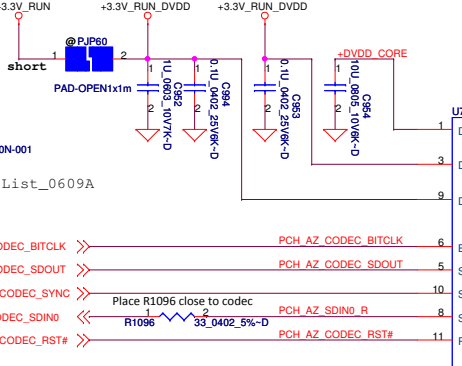
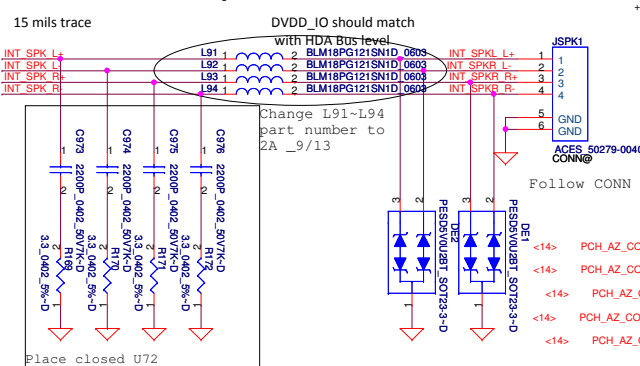
Size: **LA-7902P**

Date: **Wednesday, March 07, 2012**

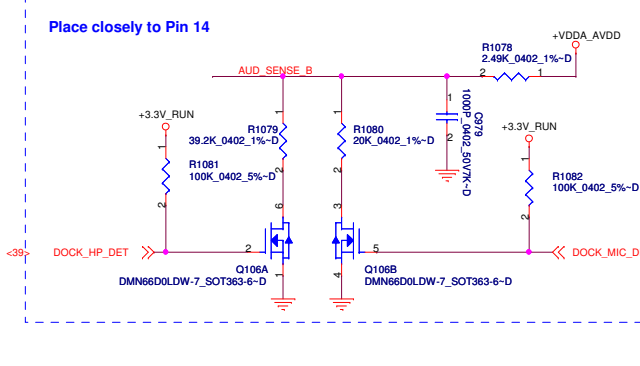
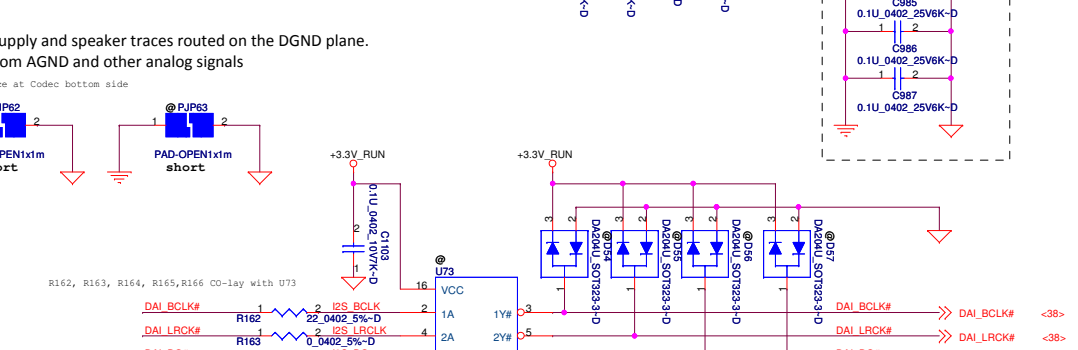
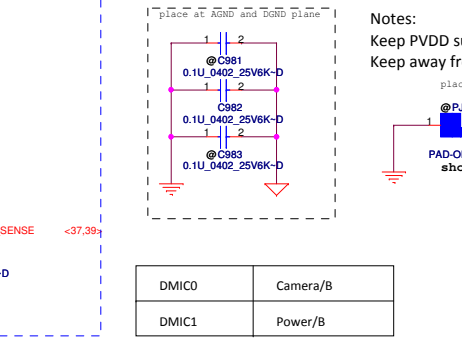
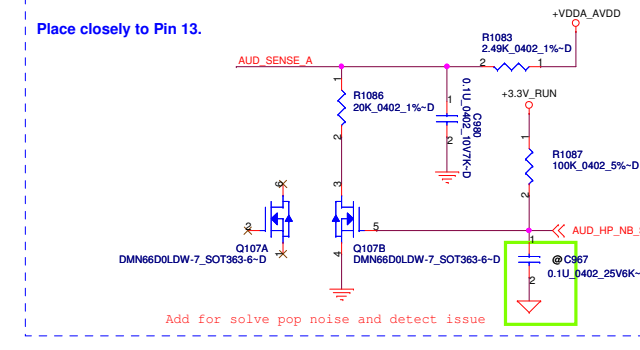
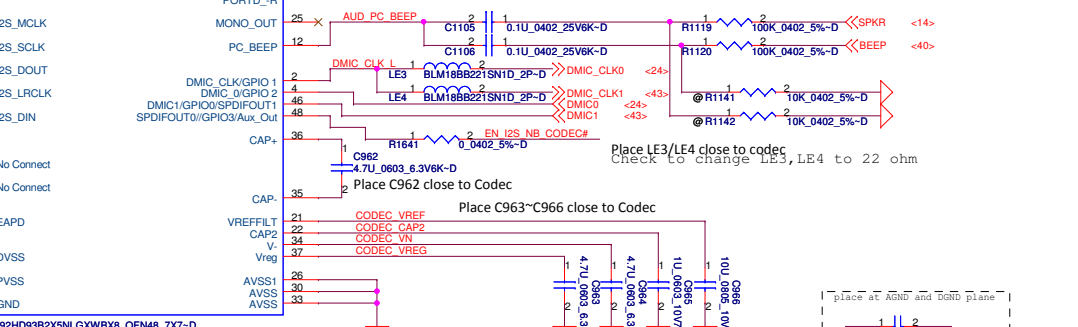
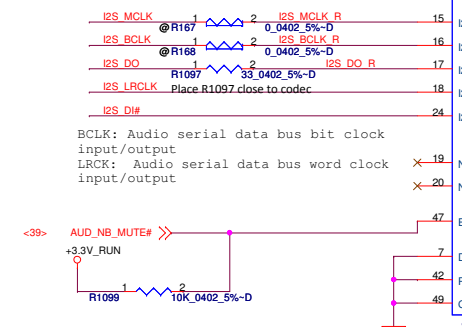
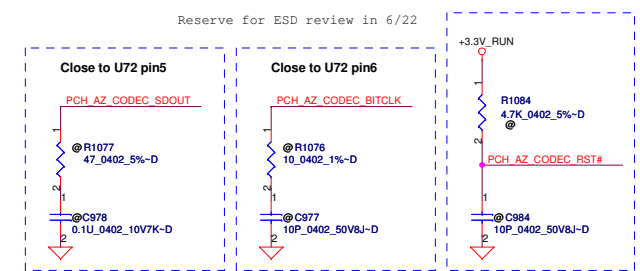
Rev: **1.0**

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Internal Speakers Header

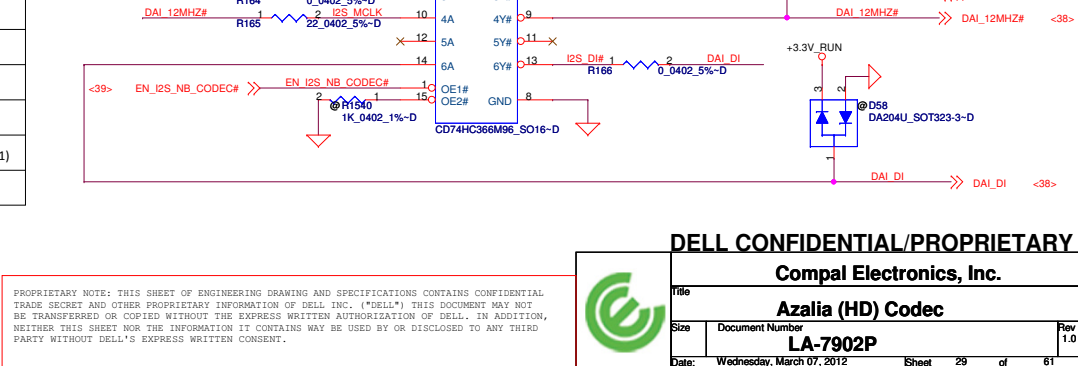


IDT review in 0624 to add R169-R172
IDT suggest exchange location R169-R172 & C973-C976._09/13

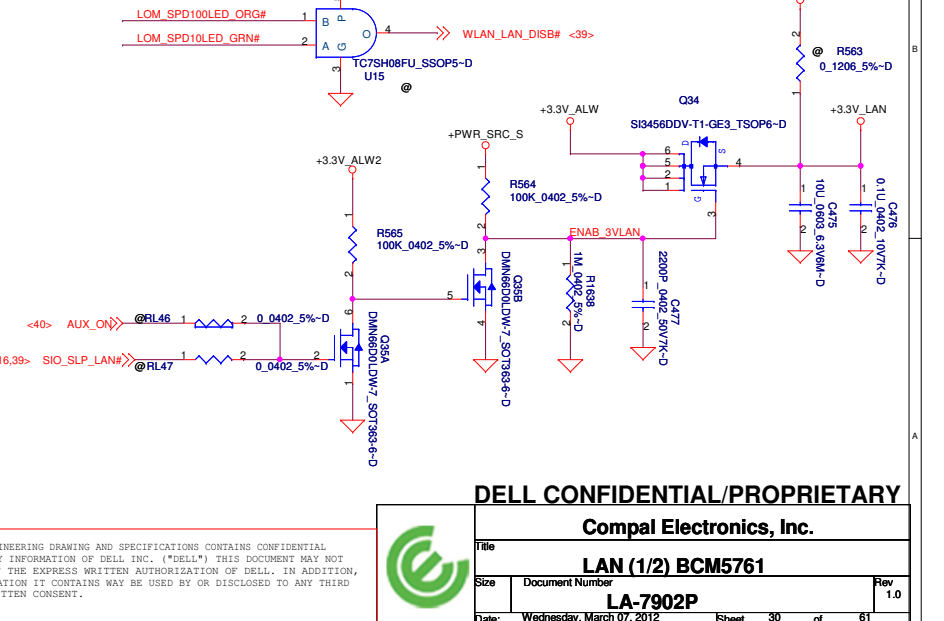
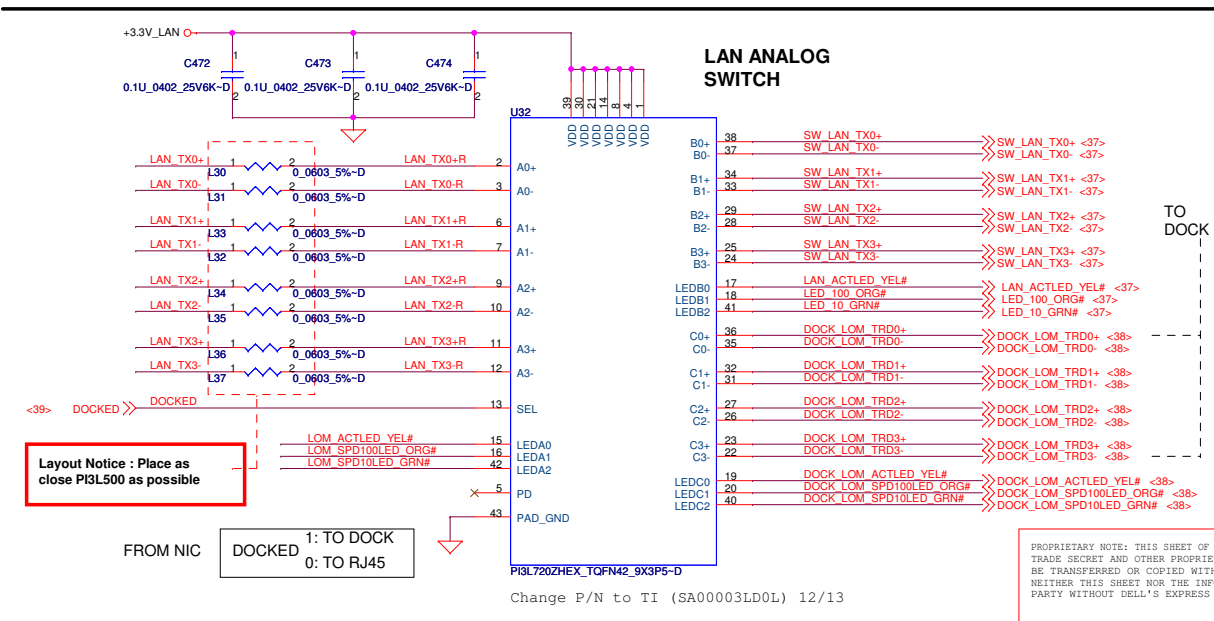
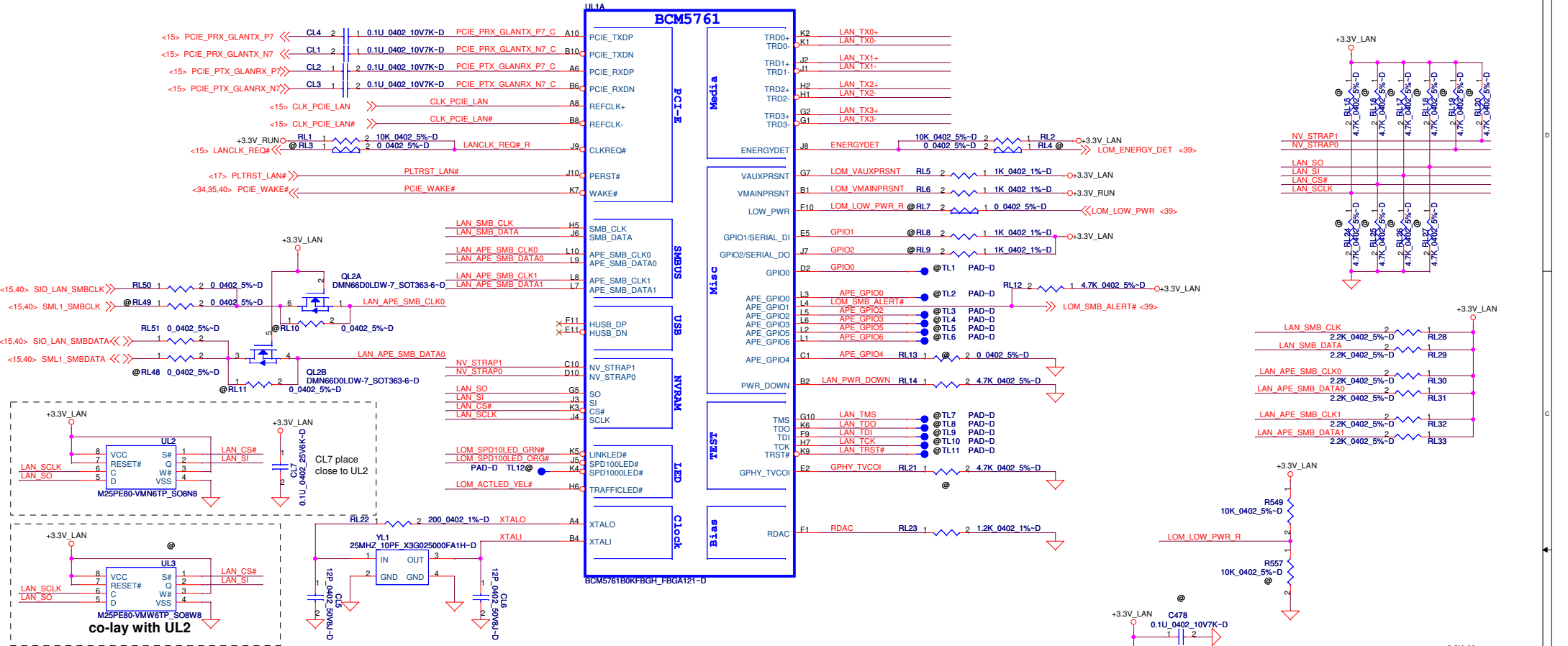


Resistor	SENSE_A	SENSE_B
39.2K	PORT A	PORT E
20K	PORT B	PORT F
10K	NA	DMIC0
5.11K	SPDIFOUT0	SPDIFOUT1 (DMIC1)
2.49K	Pull-up to AVDD	

PORT	Function
PORT A	External MIC
PORT B	HeadPhone Out
PORT C	Dock Audio
PORT D	Internal SPK



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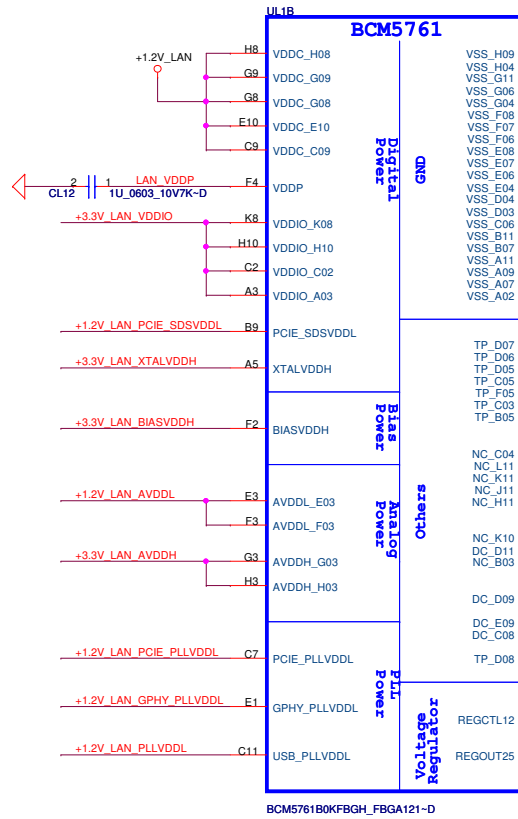
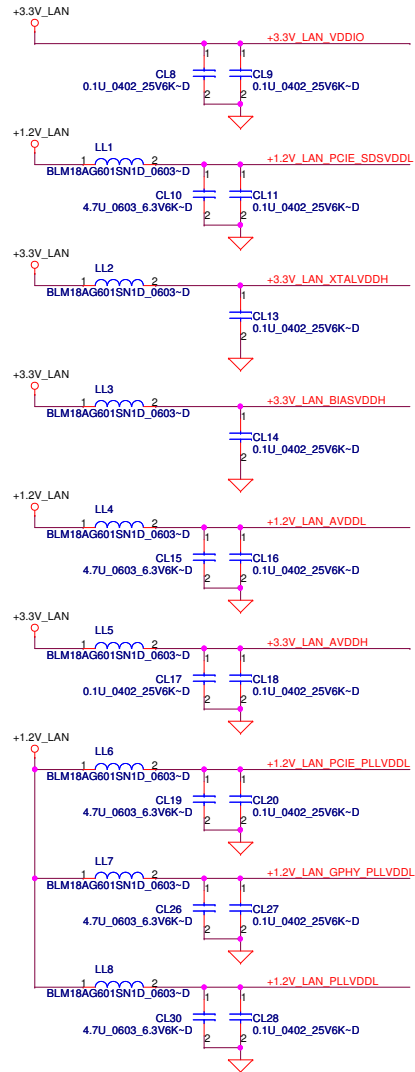
LAN (1/2) BCM5761

LA-7902P

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Change P/N to TI (SA00003LD0L) 12/13



BCM5761

VSS_H09, VSS_H04, VSS_G11, VSS_G06, VSS_G04, VSS_F08, VSS_F07, VSS_F06, VSS_E08, VSS_E07, VSS_E06, VSS_E04, VSS_D04, VSS_D03, VSS_C06, VSS_B11, VSS_B07, VSS_A11, VSS_A09, VSS_A07, VSS_A02

TP_D07, TP_D06, TP_D05, TP_C05, TP_F05, TP_C03, TP_B05, TP_D08

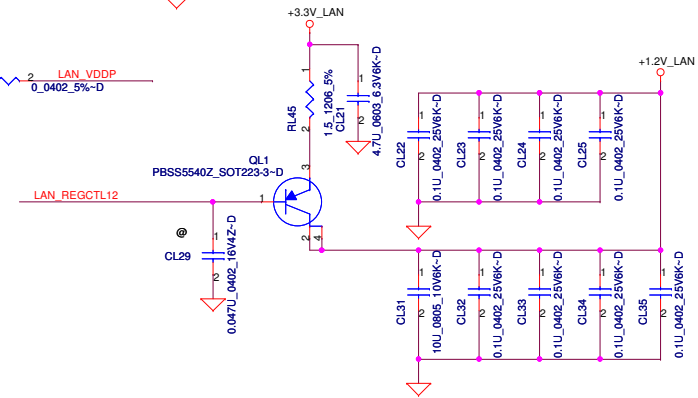
NC_C04, NC_L11, NC_K11, NC_J11, NC_H11

NC_K10, DC_D11, NC_B03

DC_D09, DC_E09, DC_C08

REGCTL12, REGOUT25

Cvdpp must have ESR < 1 Ohm.



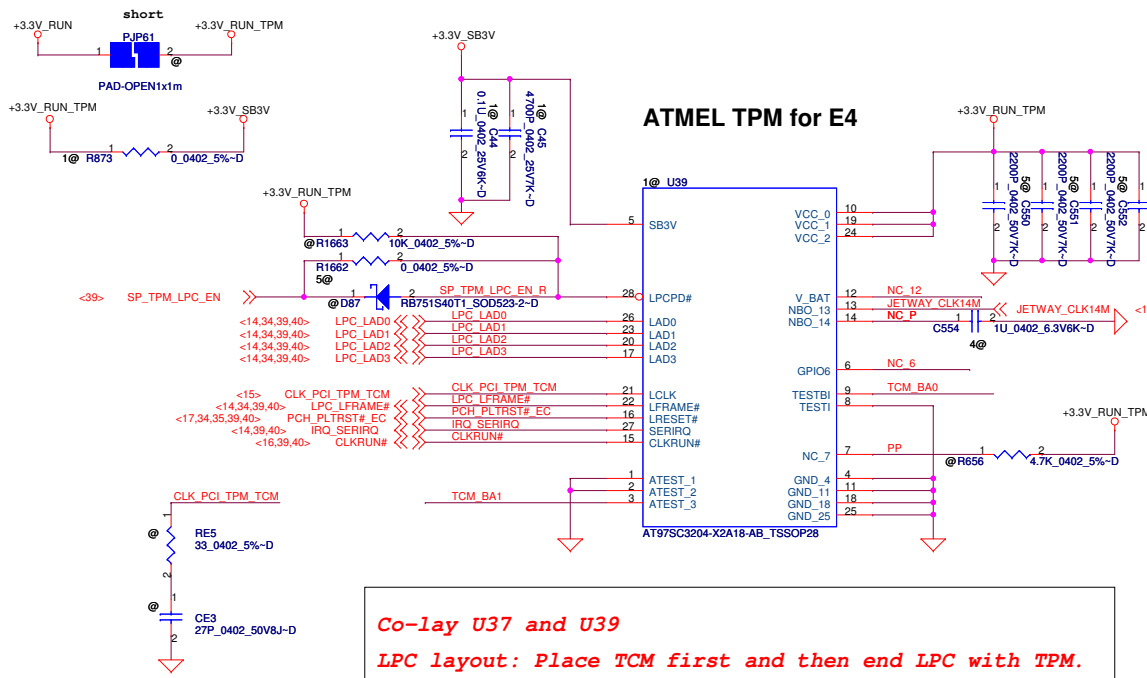
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LAN (2/2) BCM5761			
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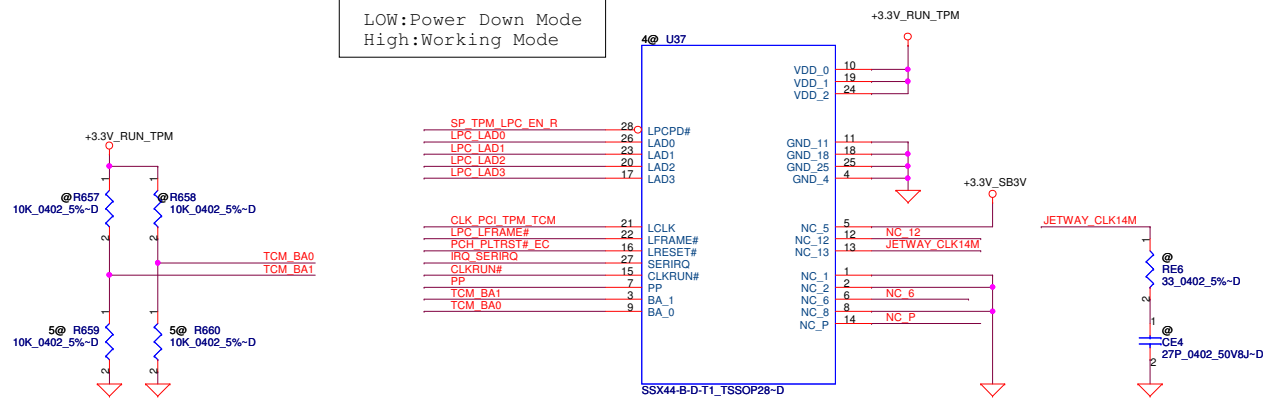
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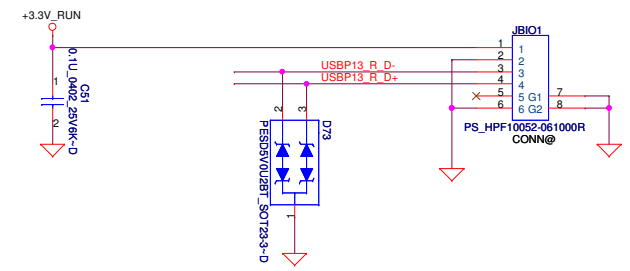
Co-lay U37 and U39
LPC layout: Place TCM first and then end LPC with TPM.

China TCM: NationZ & Jetway co-lay

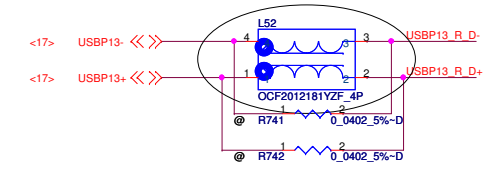
LOW:Power Down Mode
 High:Working Mode



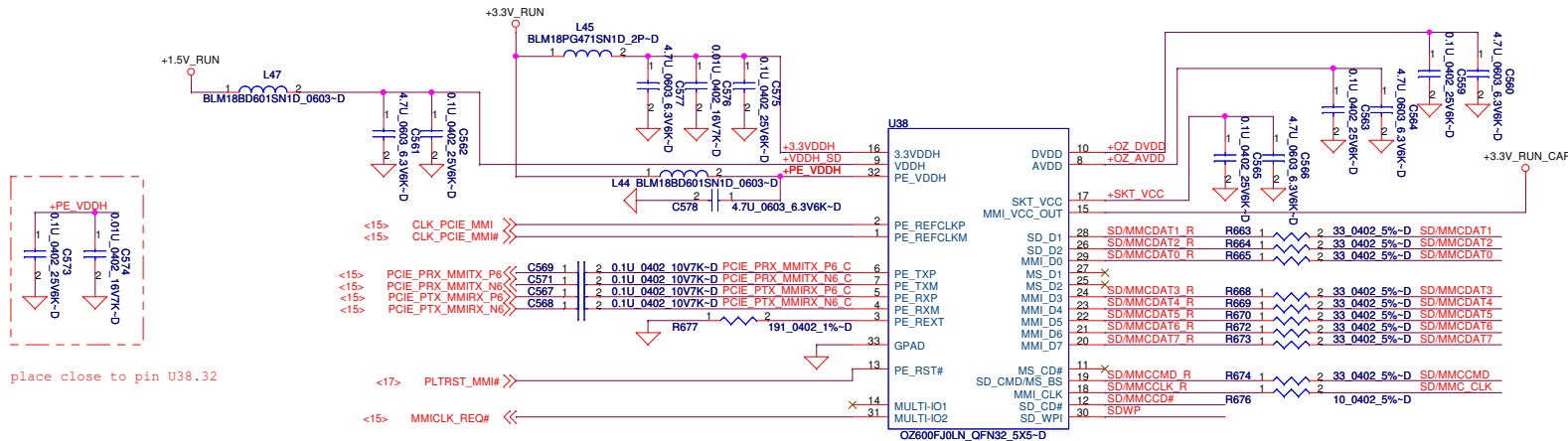
Change CONN to pitch 1.0_0815



Change CIS symbol_12/07



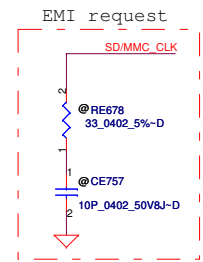
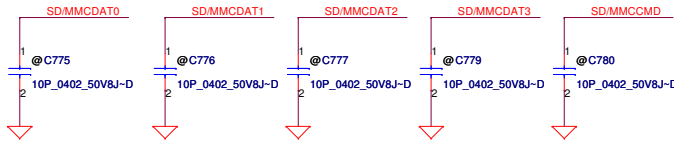
Vendor review in 6/22 and change C576 to 0.01uF



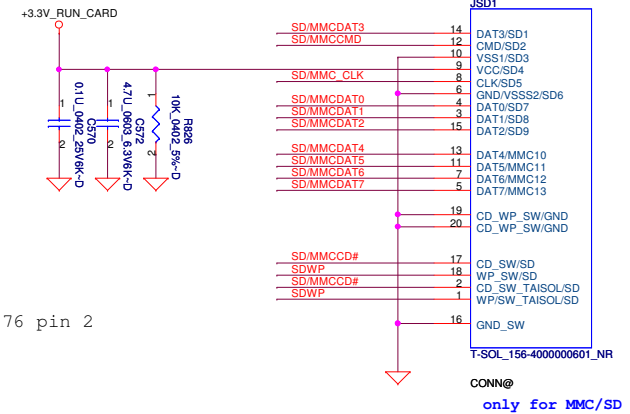
place close to pin U38.32

Note: The trace need to route as daisy-chain and the trace of SD signals need to route as short as possible

Vendor review in 6/22 and reserve for SD3.0 UHS-I 200MHz transfer

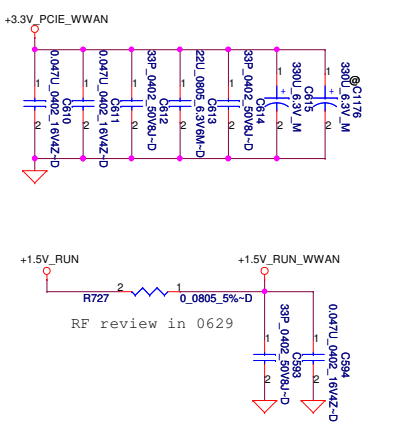
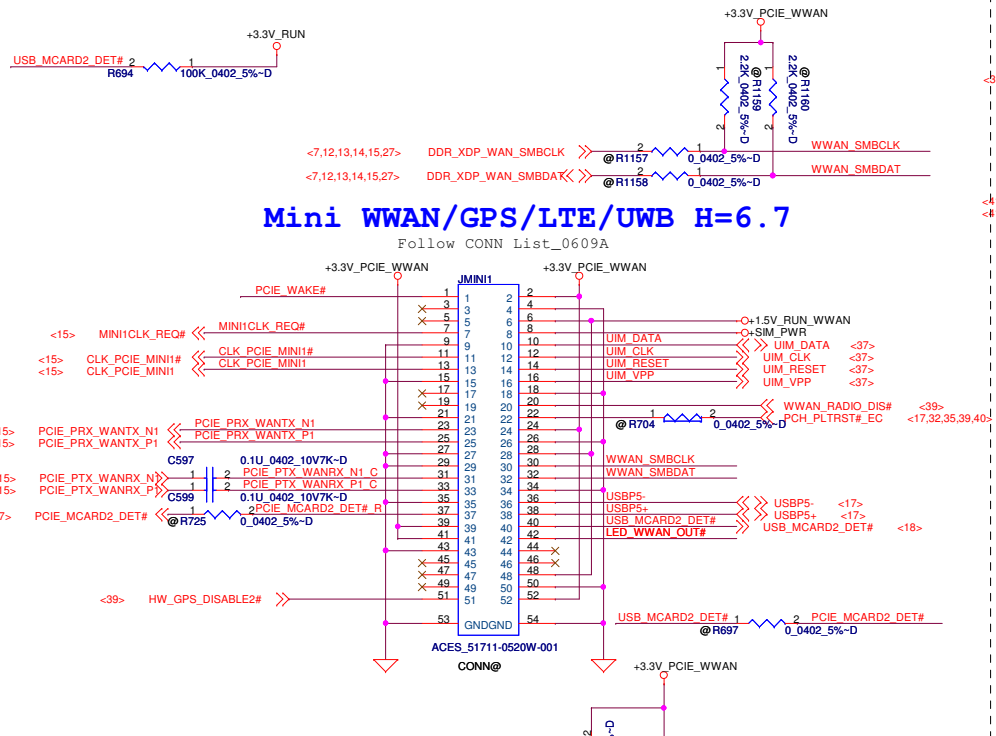


Place closed R676 pin 2

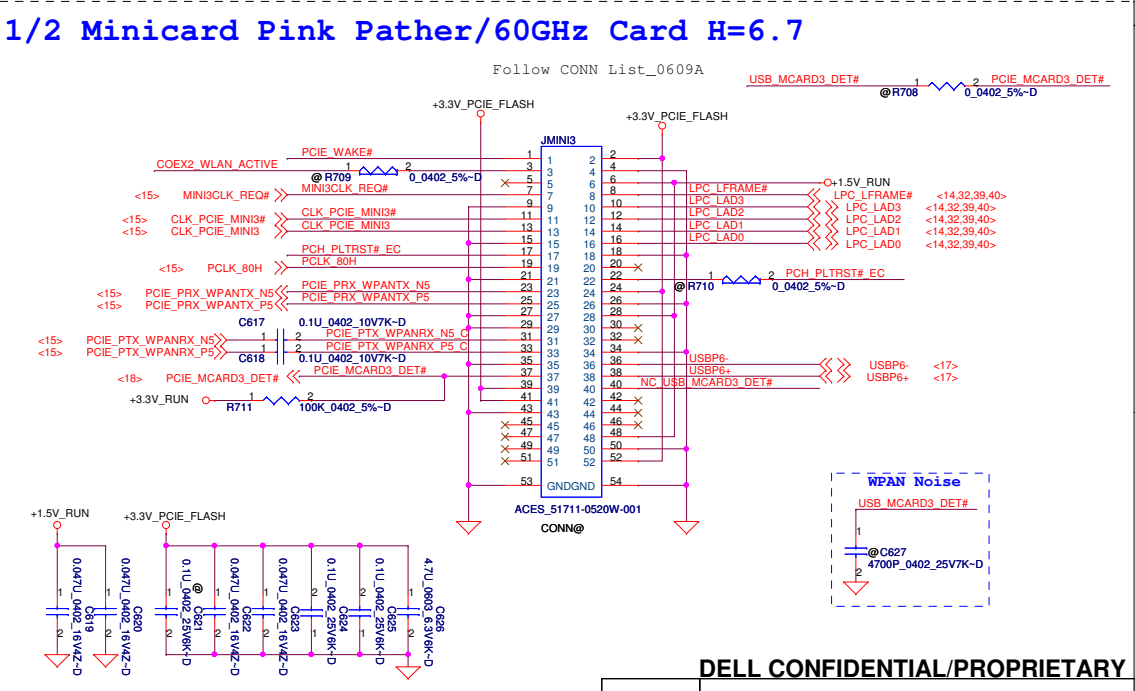
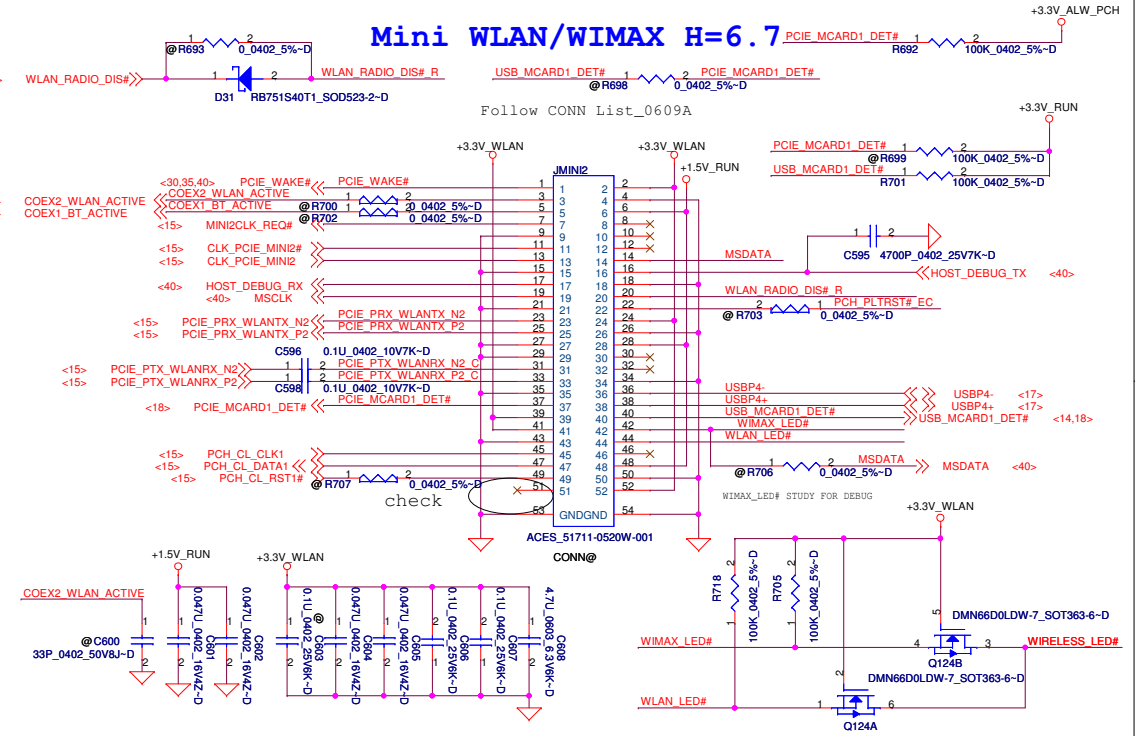


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Card Reader OZ600FJ0
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PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+9%	1000	750	
+3.3Vaux	+9%	330	250	250 (Wake enable) 5 (Not wake enable)
+1.5V	+5%	500	375	NA



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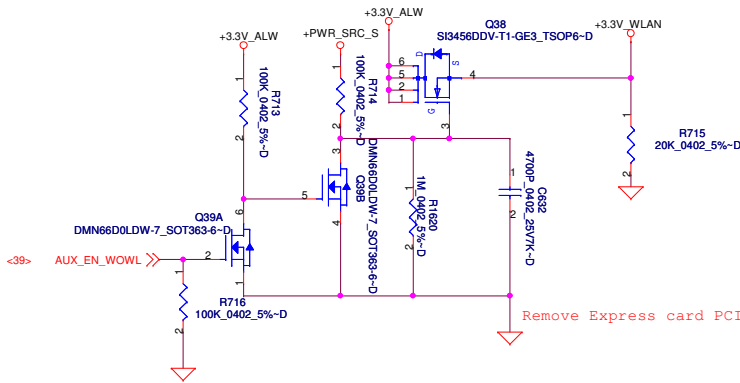
Compal Electronics, Inc.

Mini Card

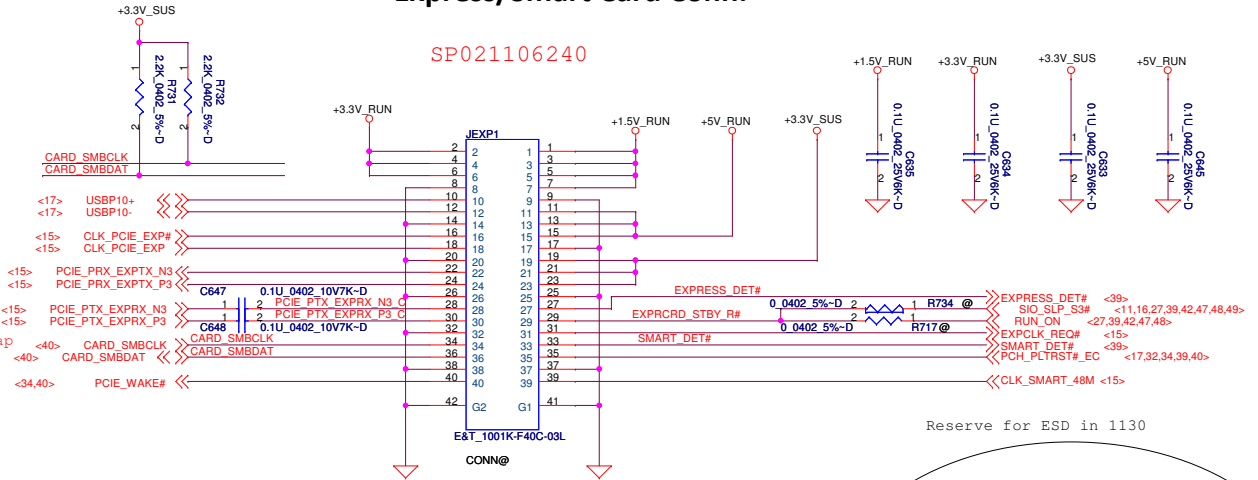
LA-7902P

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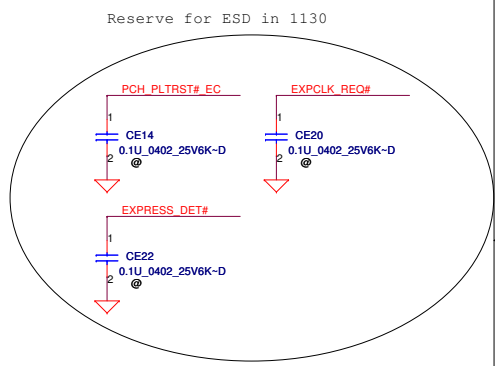
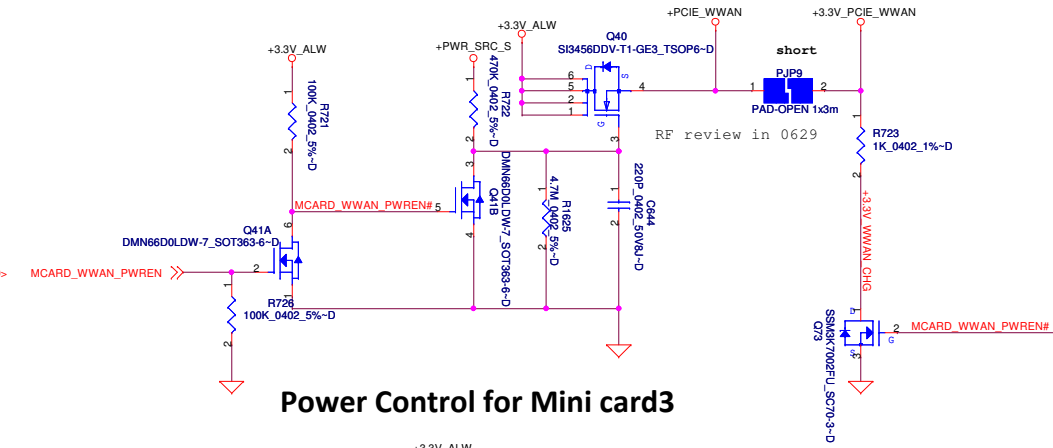
Power Control for Mini card2



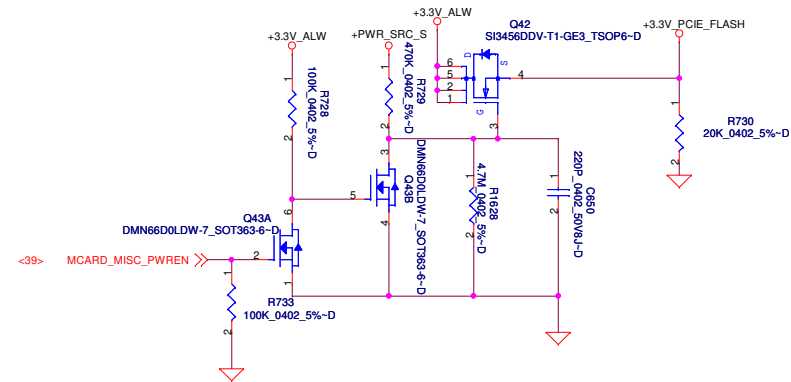
Express/Smart Card Conn.




Power Control for Mini card1

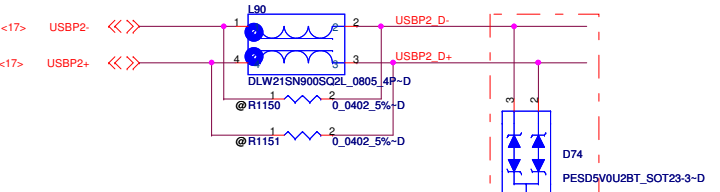
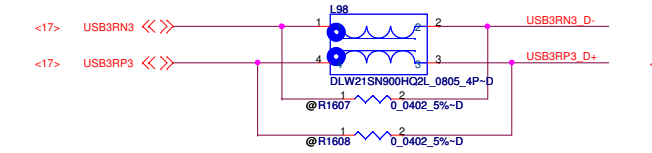
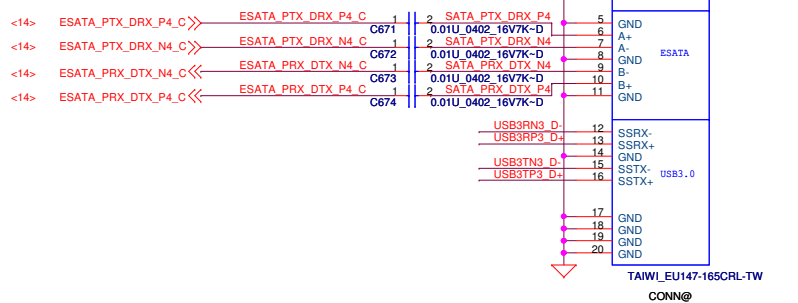
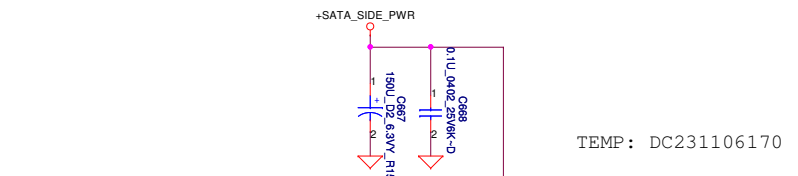
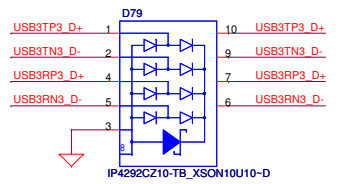
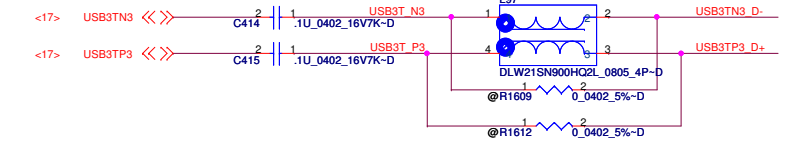
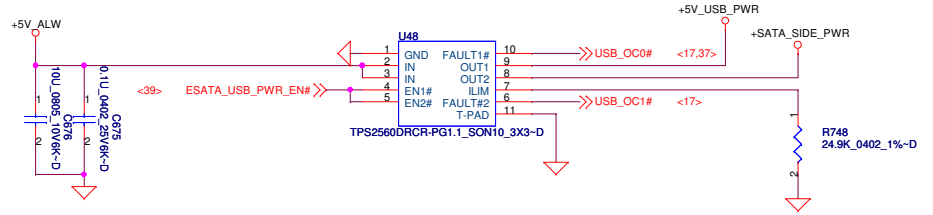
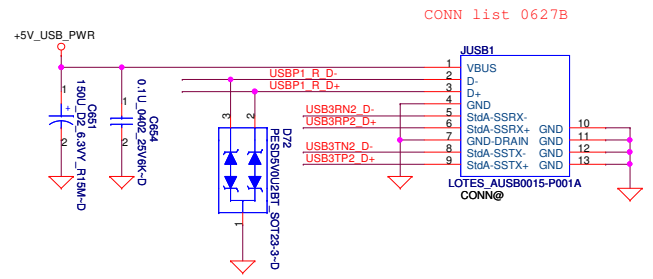
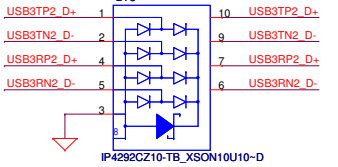
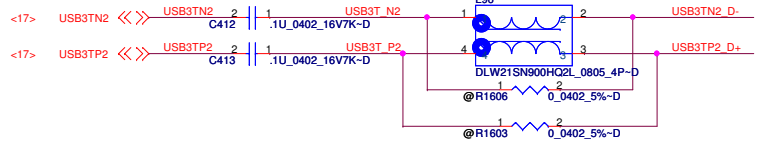
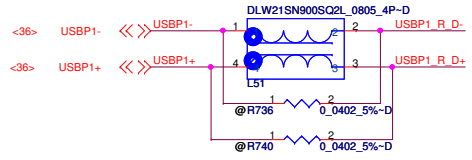
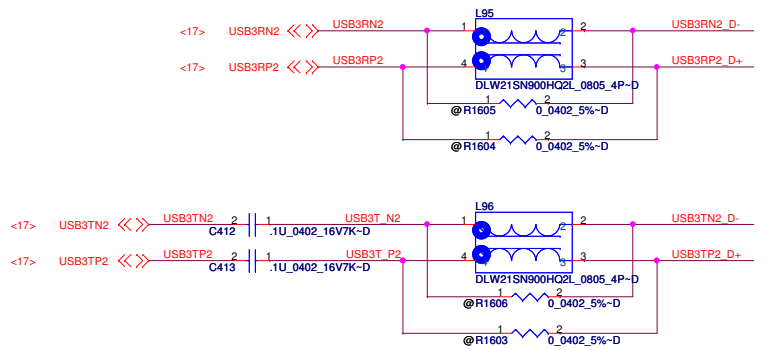


Power Control for Mini card3



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		Compal Electronics, Inc.	
MINI CARD PWR/EXP SC			
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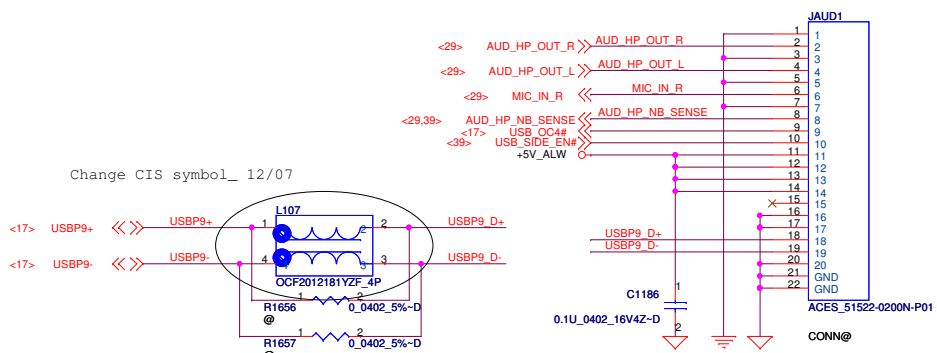
Place D74 close to JESATA1

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USB2.0/3.0 ESATA		
LA-7902P		
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AUDIO BOARD

Pitch=0.5

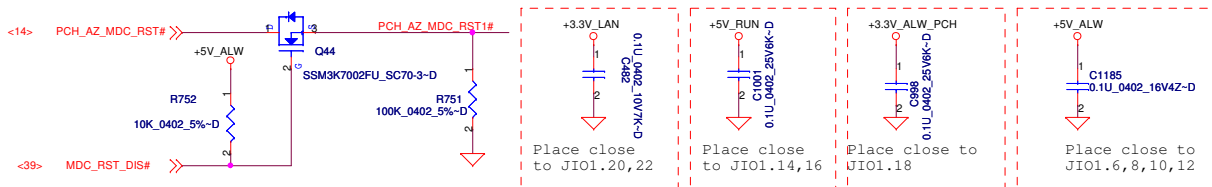
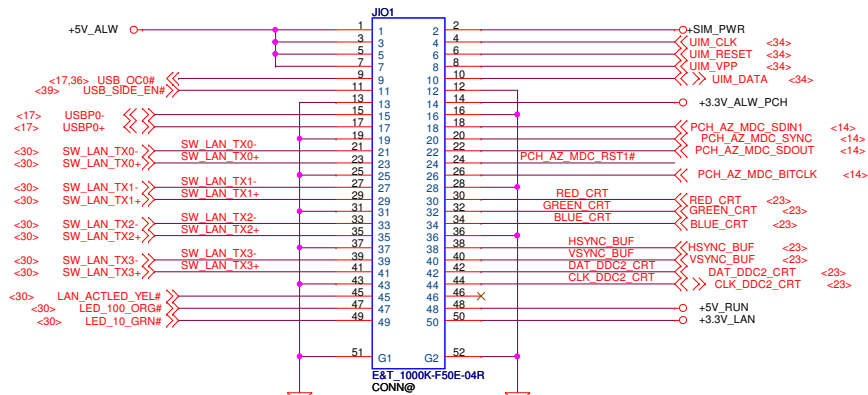
Follow CONN List_1130A



IO BOARD

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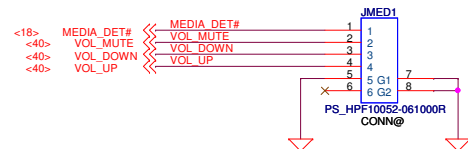
Follow CONN List_0609A



Follow CONN List_0616E

MEDIA BOARD

Follow CONN List_0621A

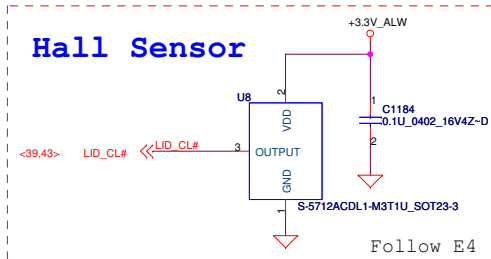


Sniffer Switch



Default on,
WIRELESS_ON/OFF#:
LOW: ON
HIGH: OFF
Follow E4

Hall Sensor

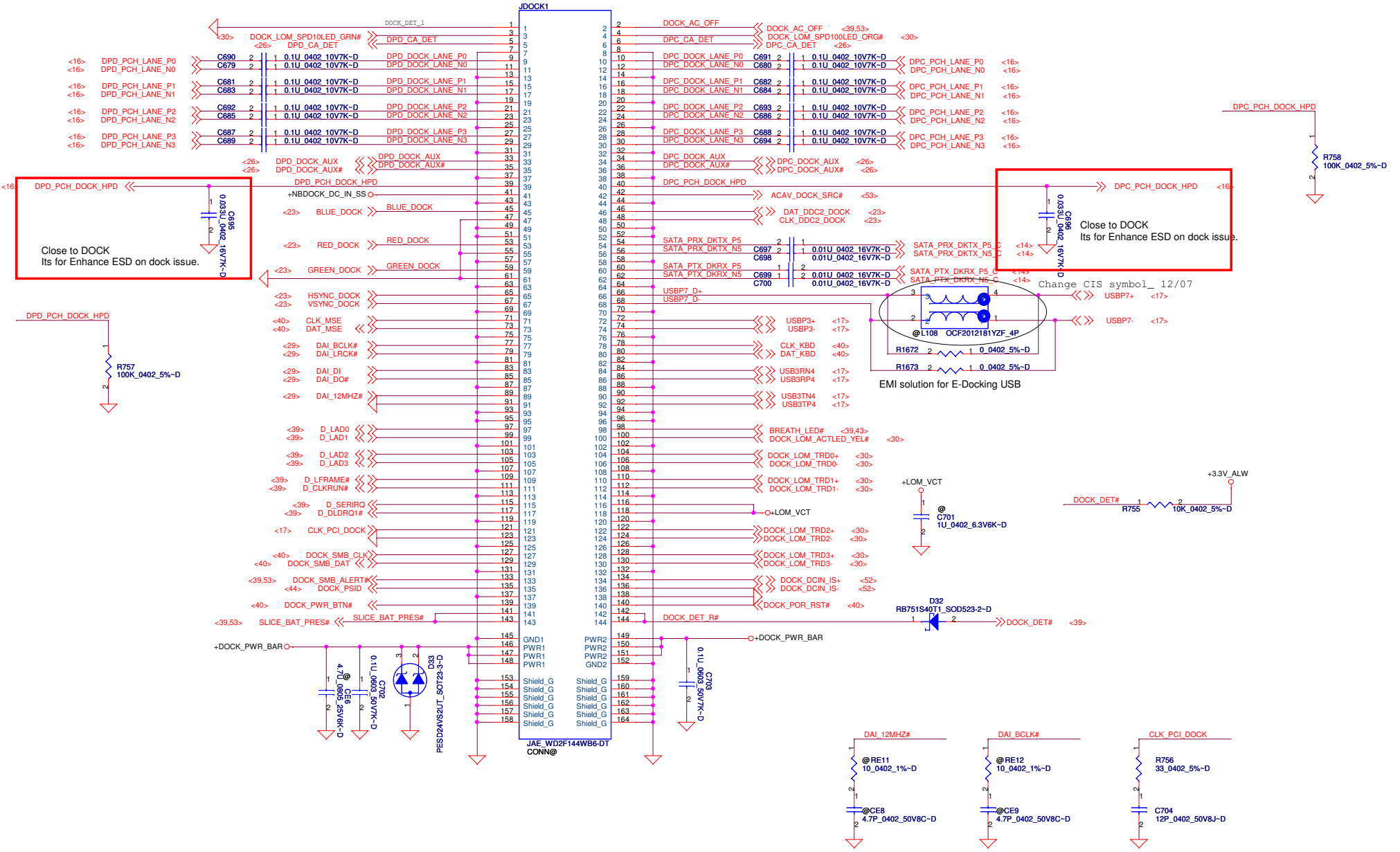


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IO/AUDIO/MEDIA/SNF			
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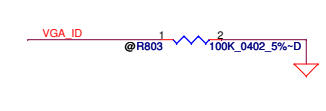
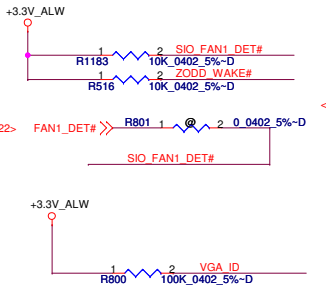
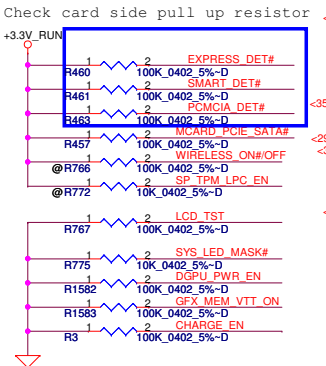
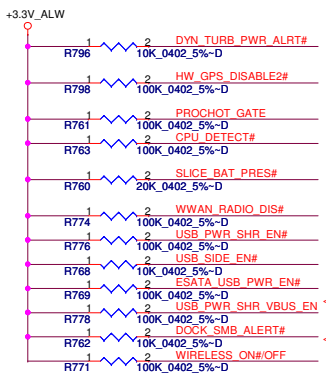
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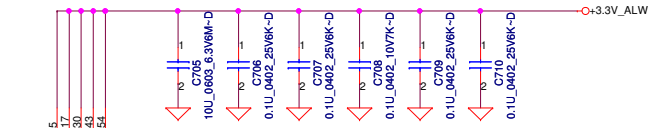
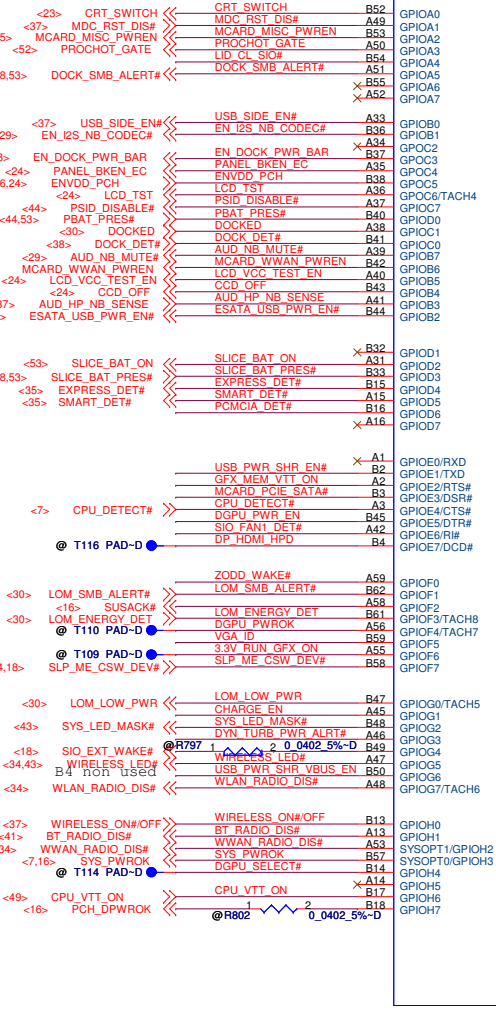
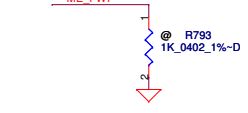
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Size	Document Number	Rev		1.0	
Date: Wednesday, March 07, 2012			Sheet	38	of 61

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	VGA_ID0
Discrete	0
UMA	1

ME_FWP PCH has internal 20K PD.
(suspend power rail)

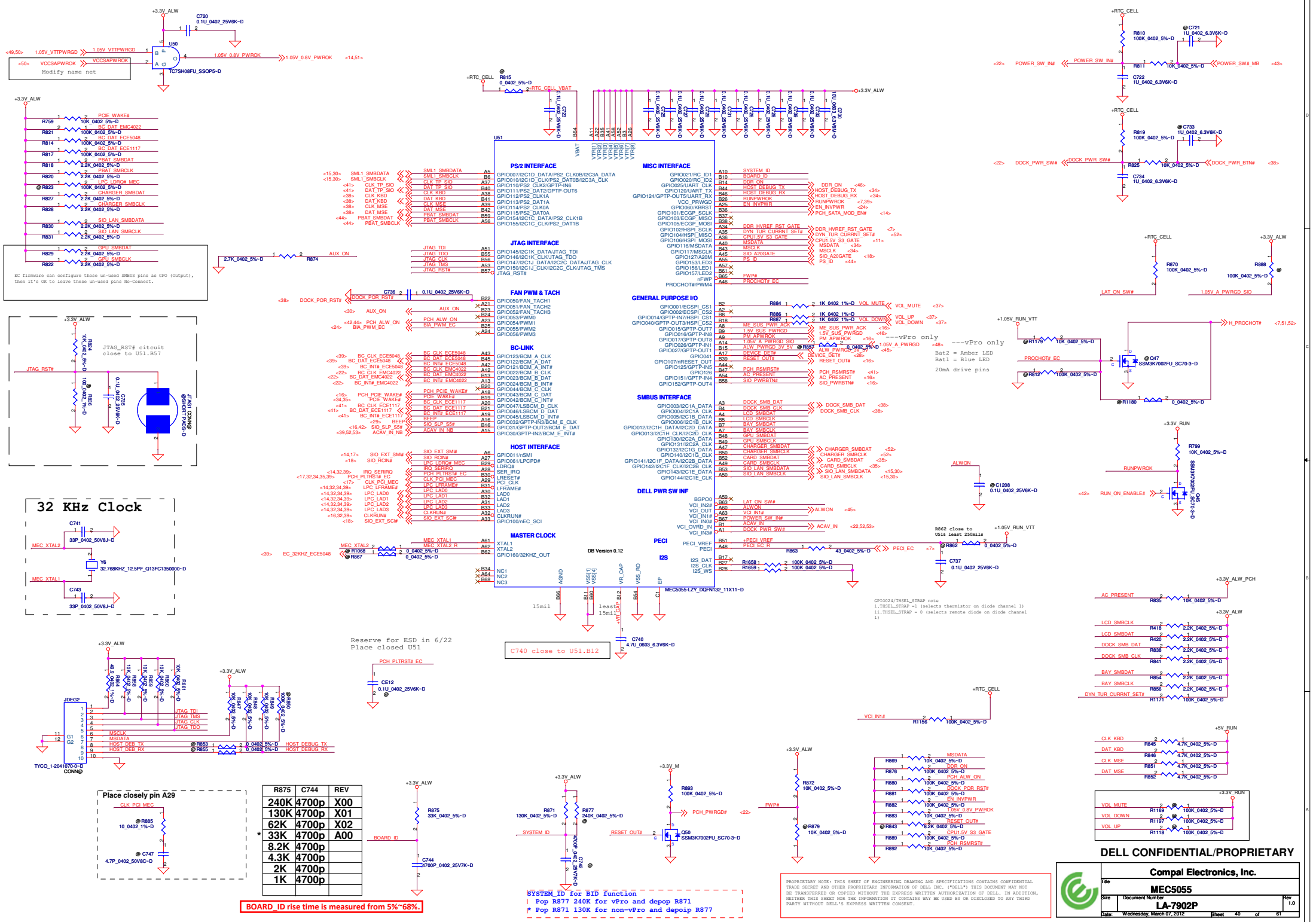


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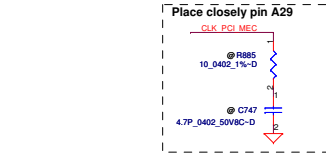
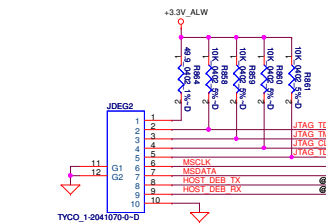
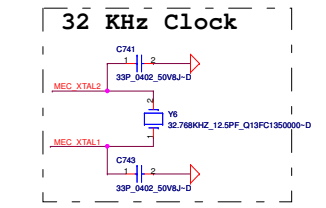
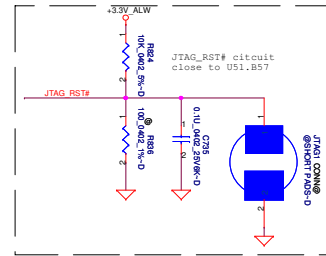


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ECE5048		
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BC firmware can configure those unused SMBUS pins as GPIO (Output), then it's OK to leave these unused pins No-Connect.



R875	C744	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	A00
8.2K	4700p	
4.3K	4700p	
2K	4700p	
1K	4700p	

BOARD_ID rise time is measured from 5%~68%.

C740 close to U51.B12

Reserve for ESD in 6/22 Place closed U51

SYSTEM ID for B1D function
 * Pop R877 240K for vPro and depop R871
 * Pop R871 130K for non-vPro and depop R877

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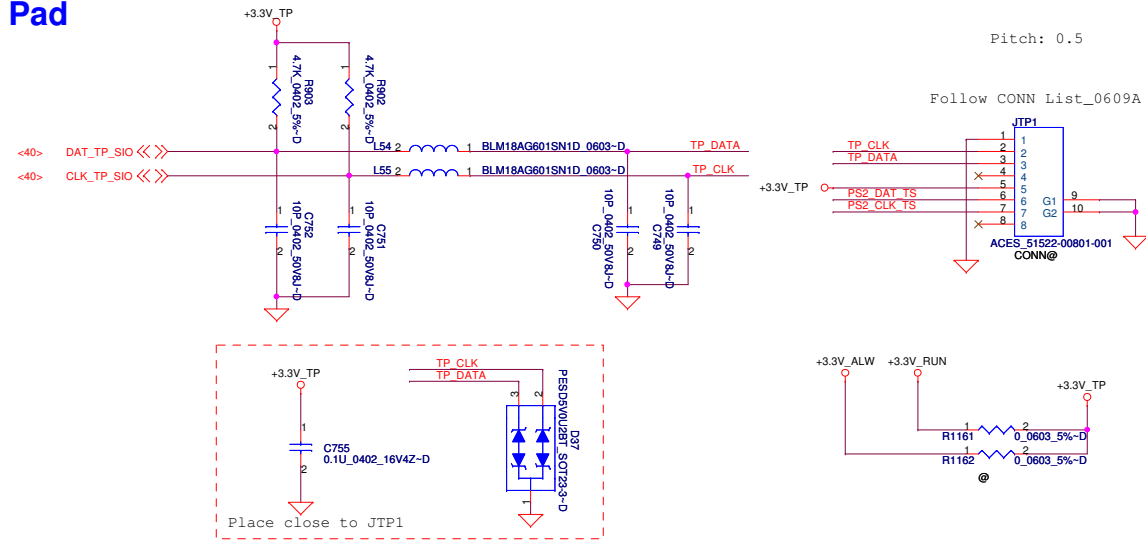
Compal Electronics, Inc.

File: **ME5055**

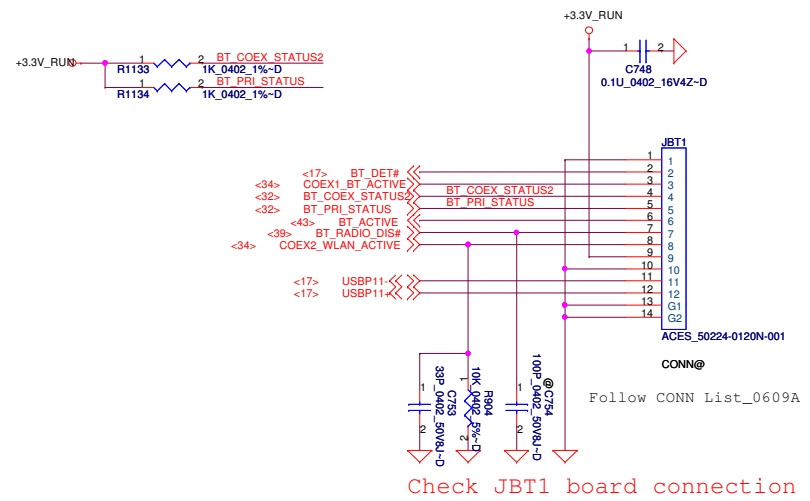
Size: **LA-7902P**

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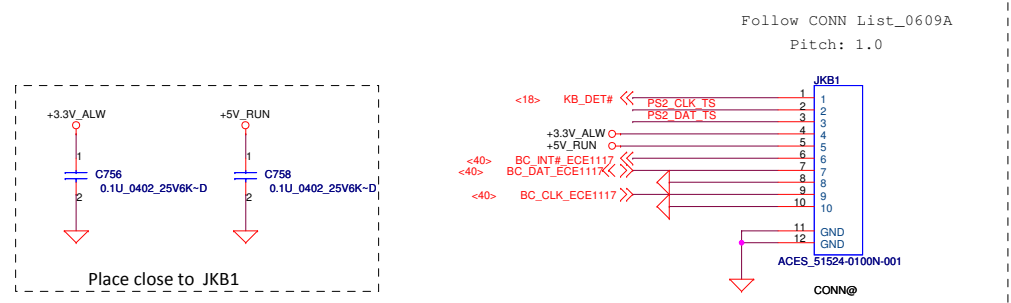
Touch Pad



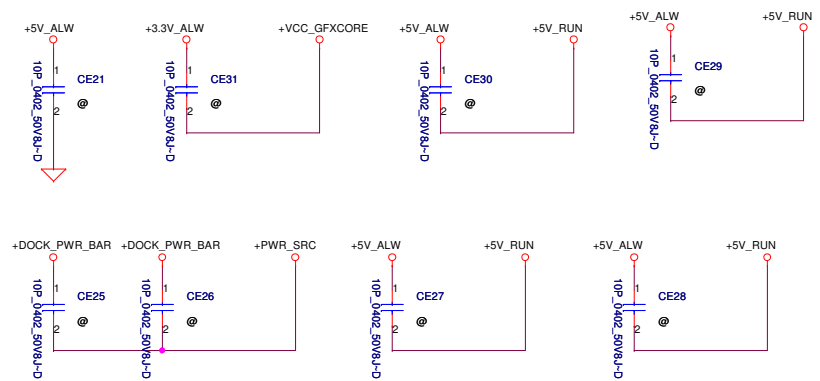
BlueTooth



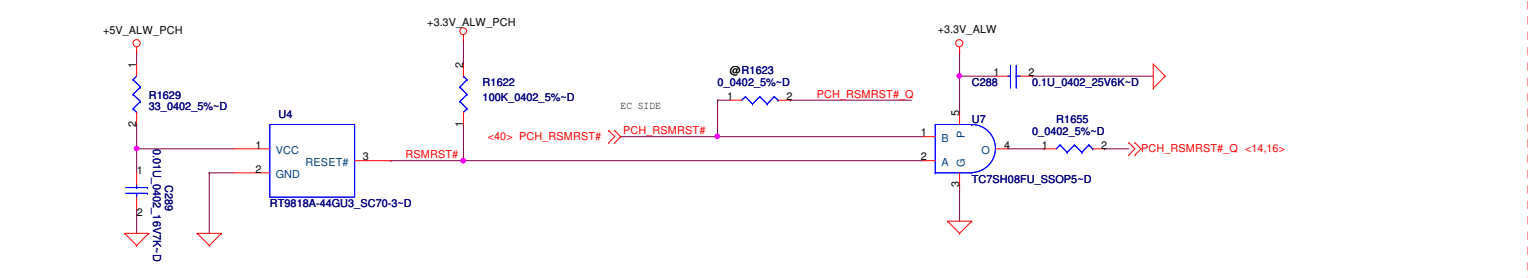
Keyboard



EMI/RF transition capacitors



RSMRST circuit

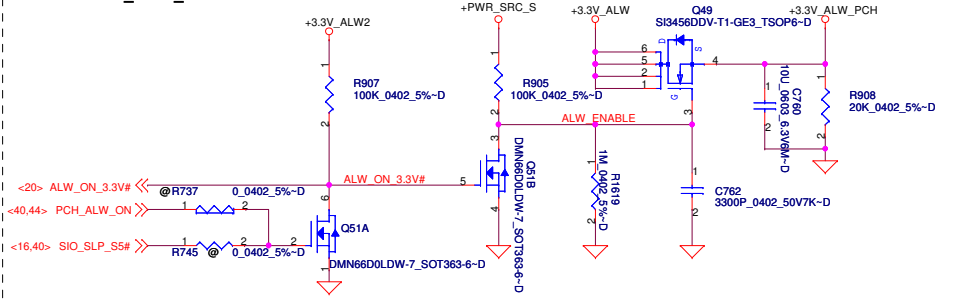


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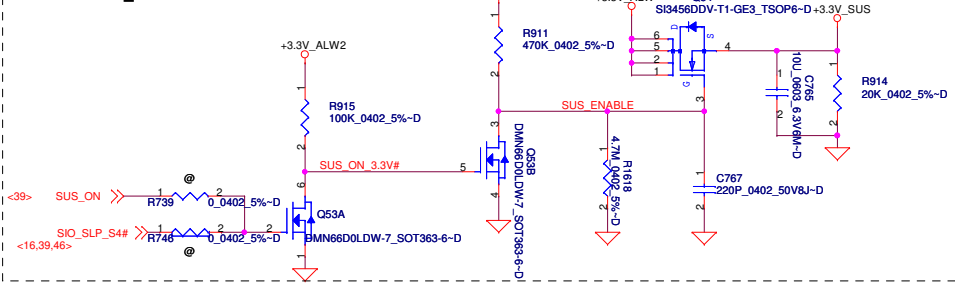
Compal Electronics, Inc.		
Title: Int KB/TP/BT/RSMRST		
Size: LA-7902P	Document Number: LA-7902P	Rev: 1.0
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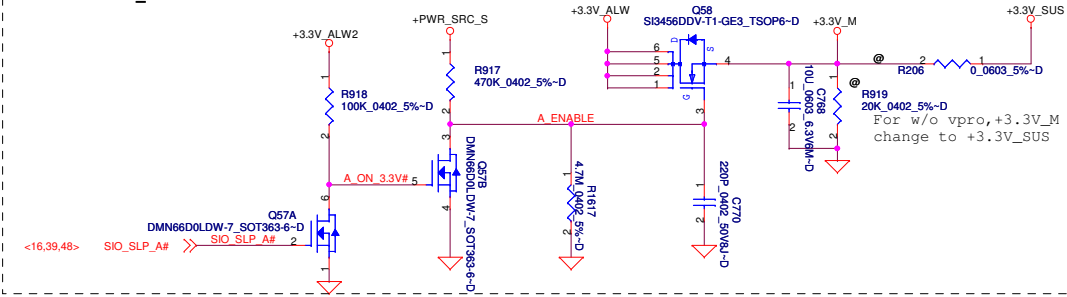
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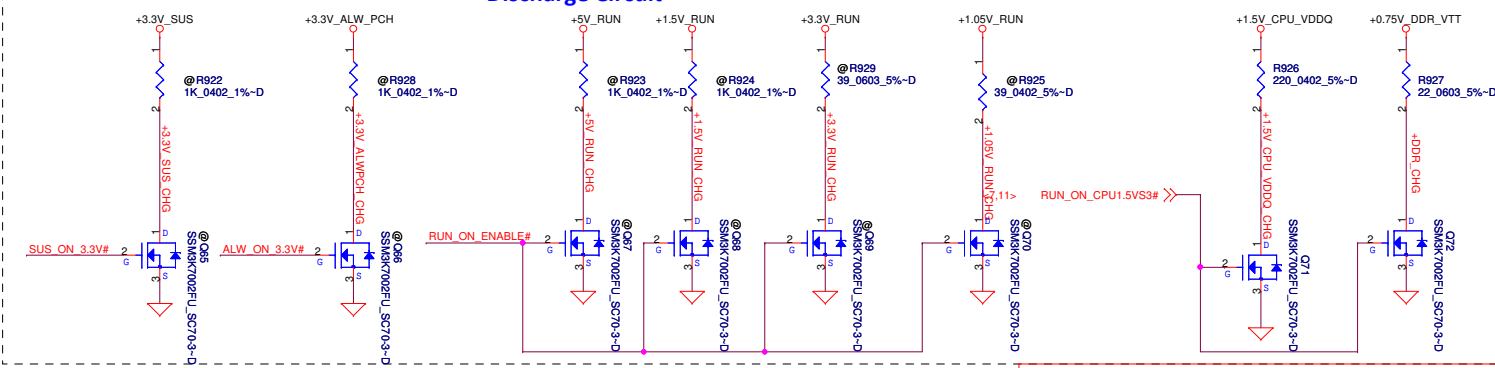
+3.3V_SUS Source



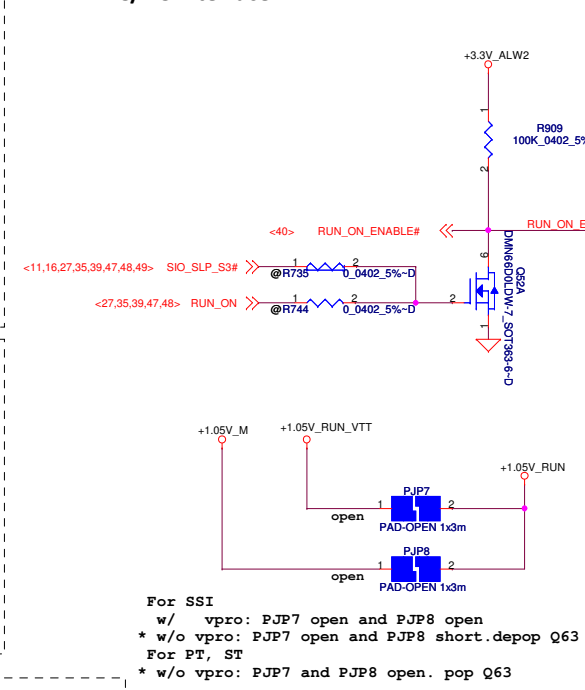
+3.3V_M Source



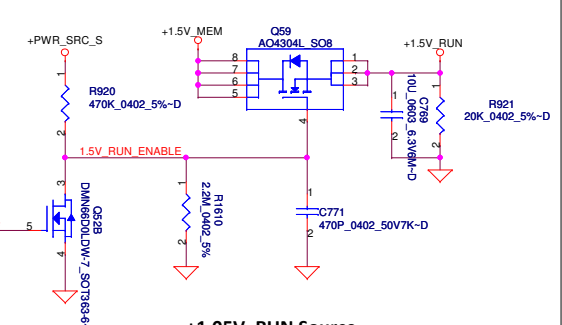
Discharge Circuit



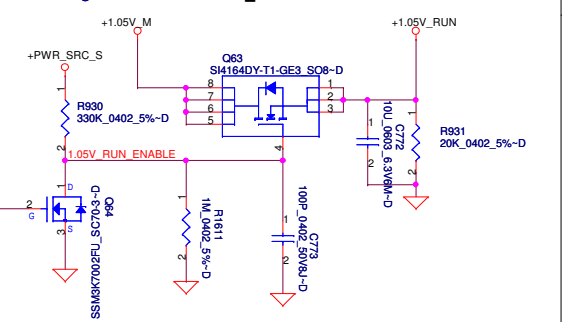
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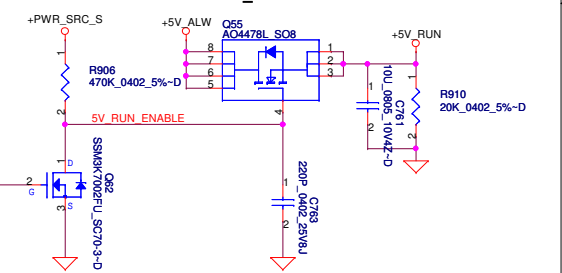
+1.5V_RUN Source



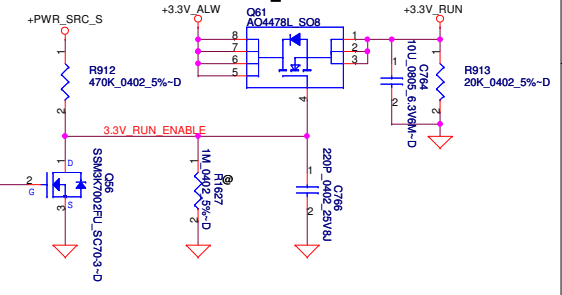
+1.05V_RUN Source



+5V_RUN Source



+3.3V_RUN Source

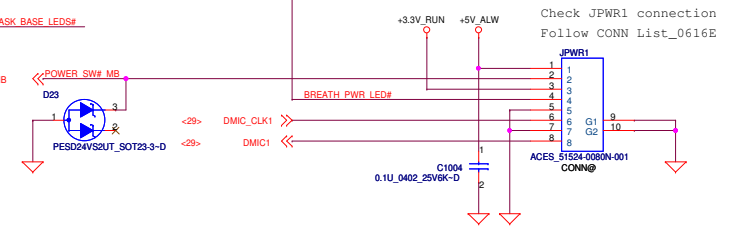
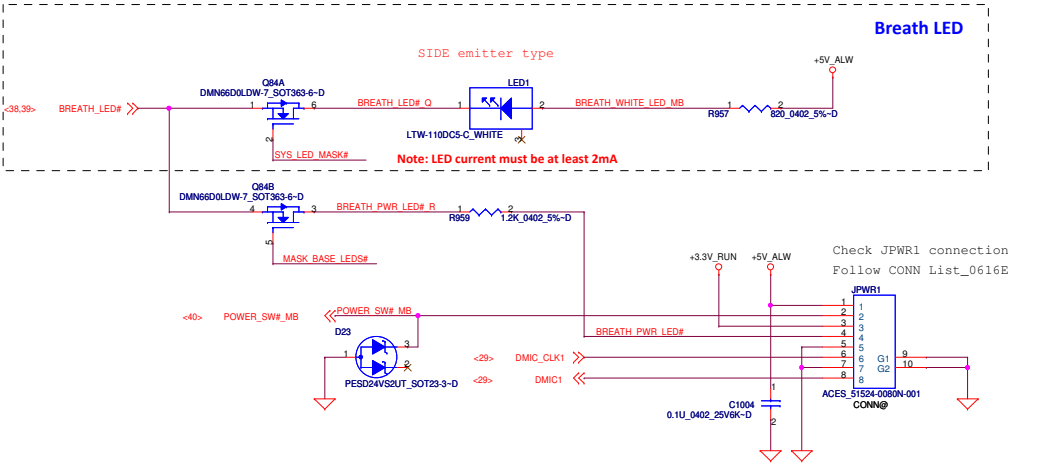
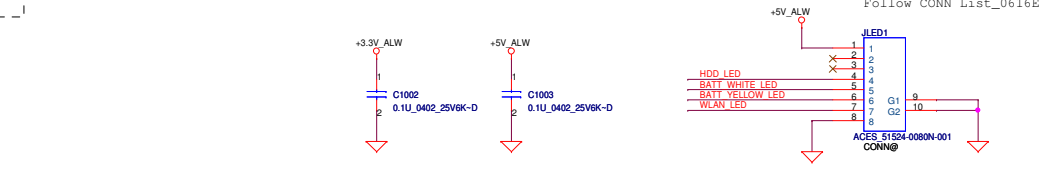
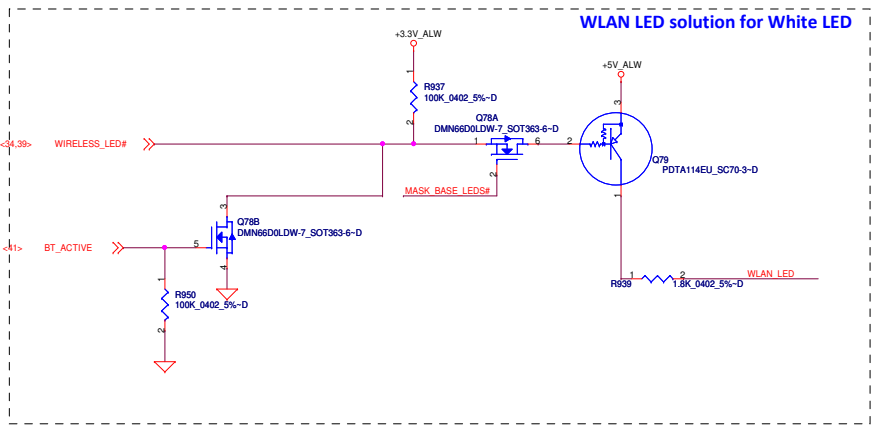
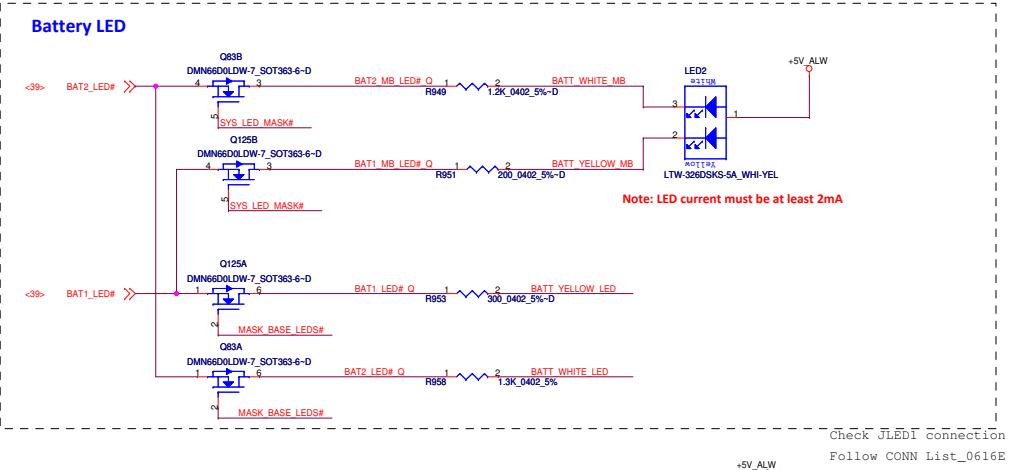
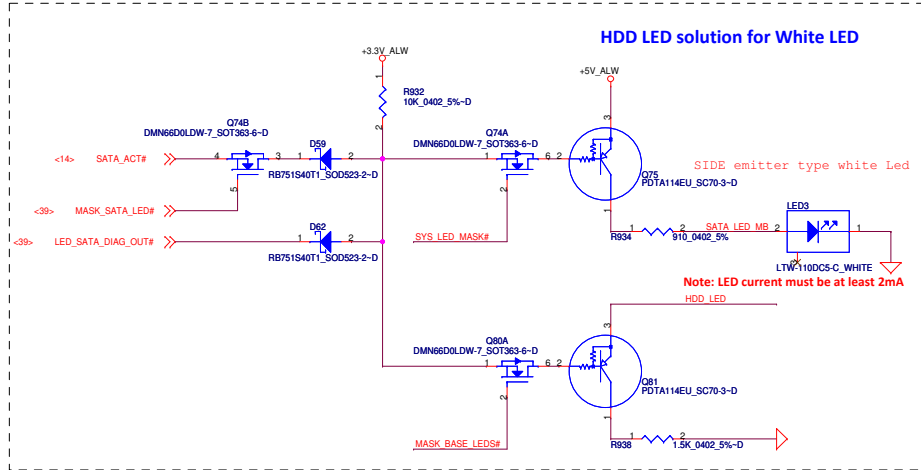


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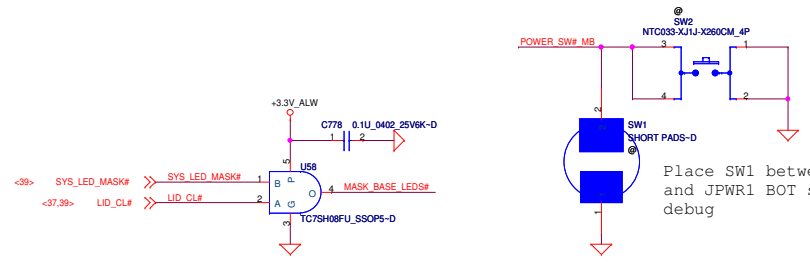
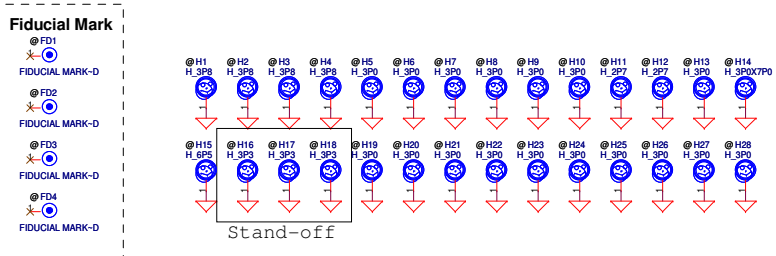


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POWER CONTROL		
LA-7902P	Rev 1.0	
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	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



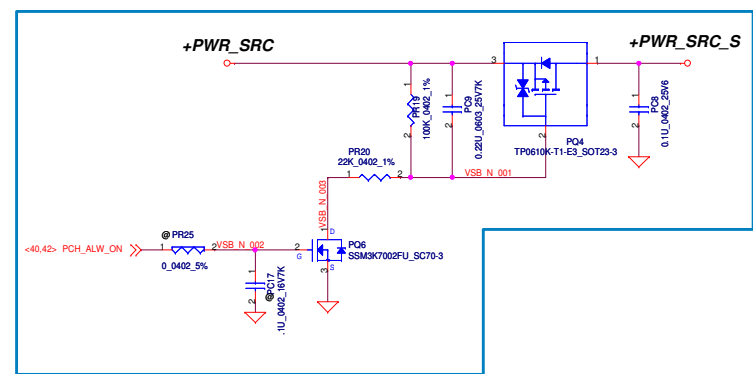
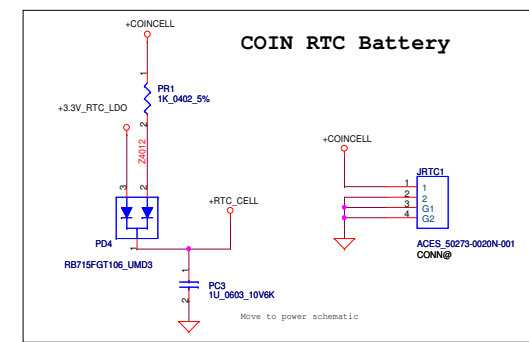
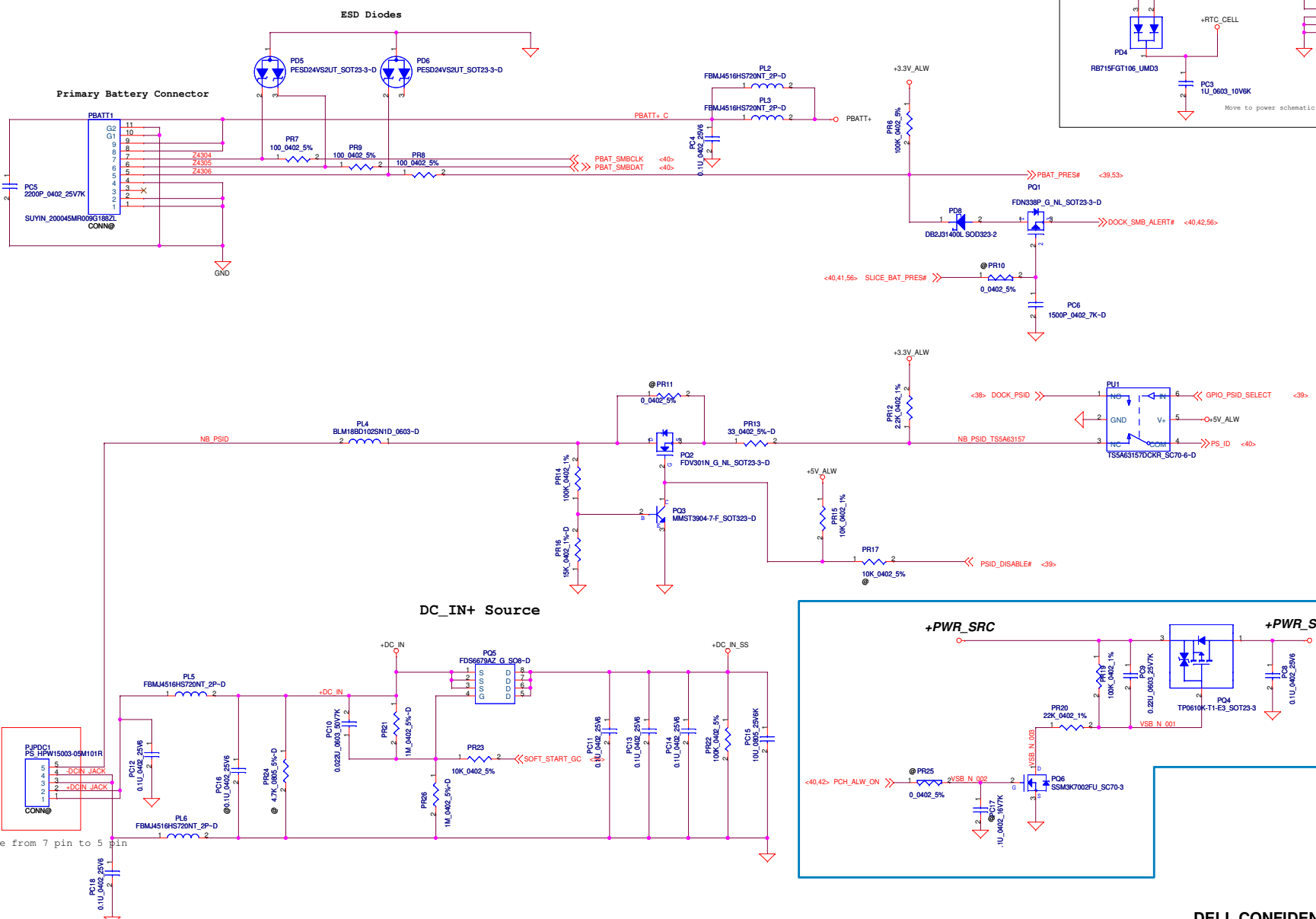
Place SW2 between D23 and JPWR1 Top side for debug

Place SW1 between D23 and JPWR1 BOT side for debug

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Compal Electronics, Inc.
PWR/LED Conn/PAD/ME
 Title
 Size Document Number
LA-7902P
 Date: Wednesday, March 07, 2012 Sheet 43 of 61 Rev 1.0

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8/18 change from 7 pin to 5 pin

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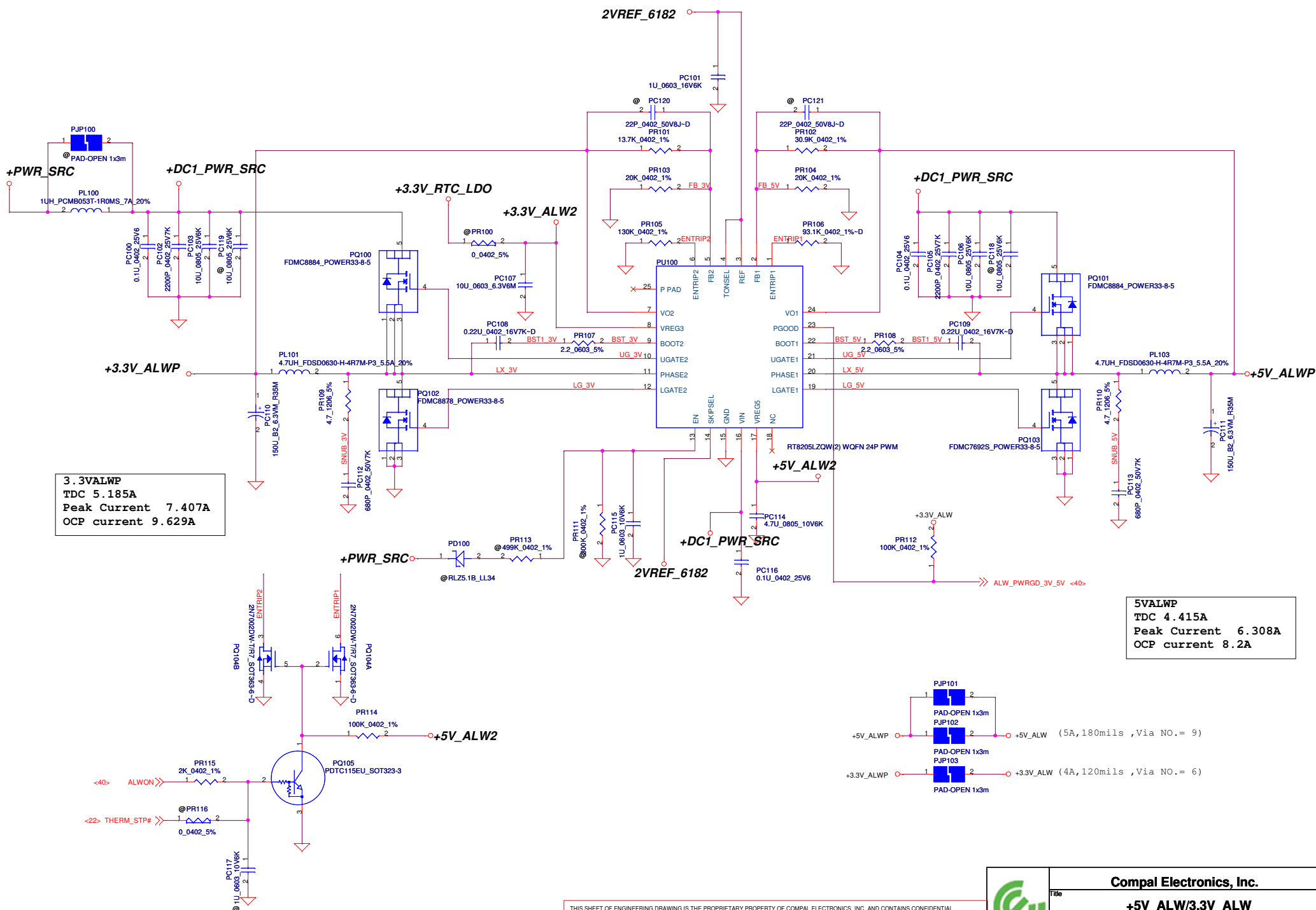
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Title: **+DCIN**

Size: **LA-7902P**

Date: **Wednesday, March 07, 2012** Sheet **44** of **61**



3.3VALWP
 TDC 5.185A
 Peak Current 7.407A
 OCP current 9.629A

5VALWP
 TDC 4.415A
 Peak Current 6.308A
 OCP current 8.2A

+5V_ALW (5A, 180mils, Via NO.= 9)
 +3.3V_ALW (4A, 120mils, Via NO.= 6)

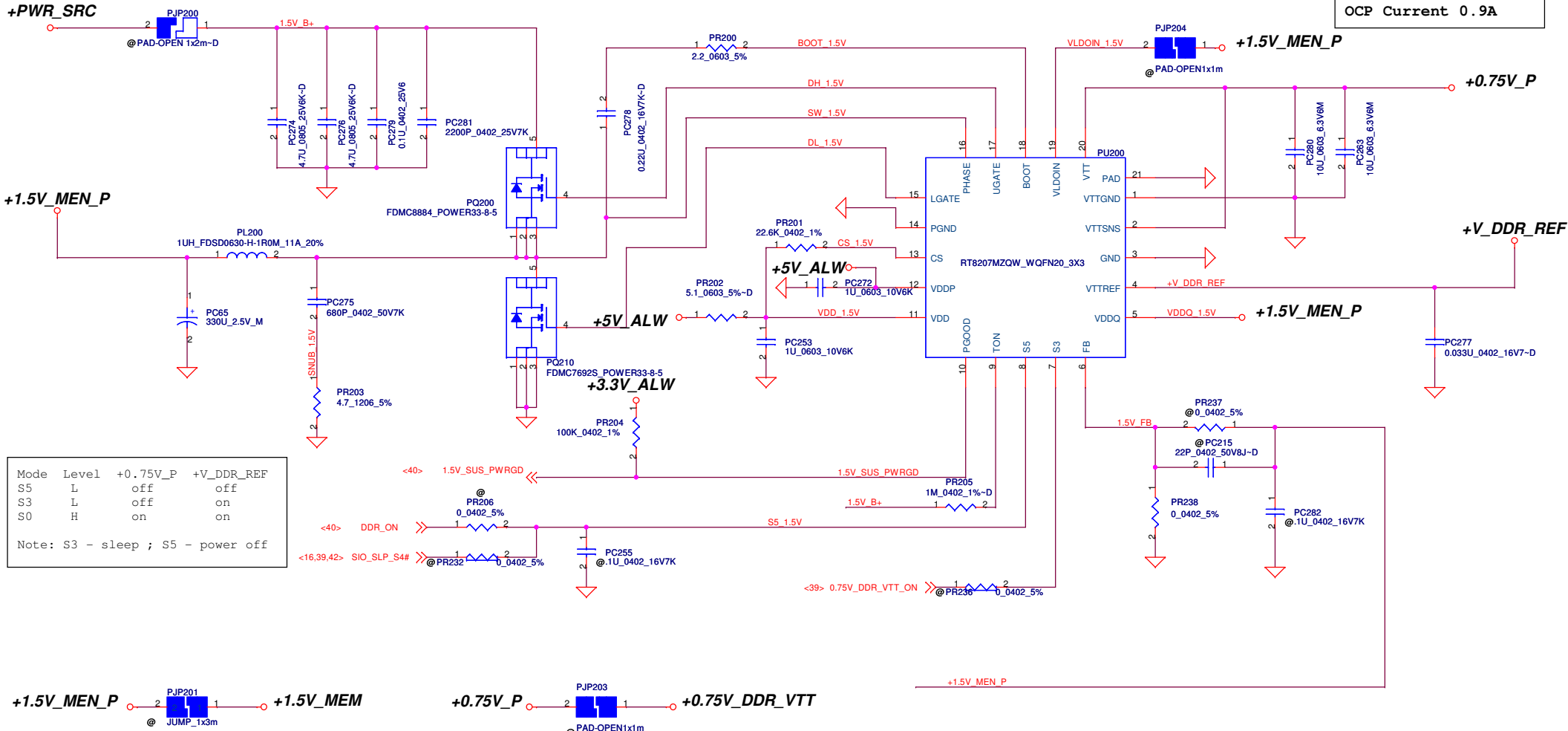
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Compal Electronics, Inc.		
Title		
+5V_ALW/3.3V_ALW		
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1.5Volt +/- 5%
 TDC 9.74A
 Peak Current 13.915A
 OCP current 16.698A

0.75Volt +/- 5%
 TDC 0.525A
 Peak Current 0.75A
 OCP Current 0.9A



Mode	Level	+0.75V_P	+V_DDR_REF
S5	L	off	off
S3	L	off	on
S0	H	on	on

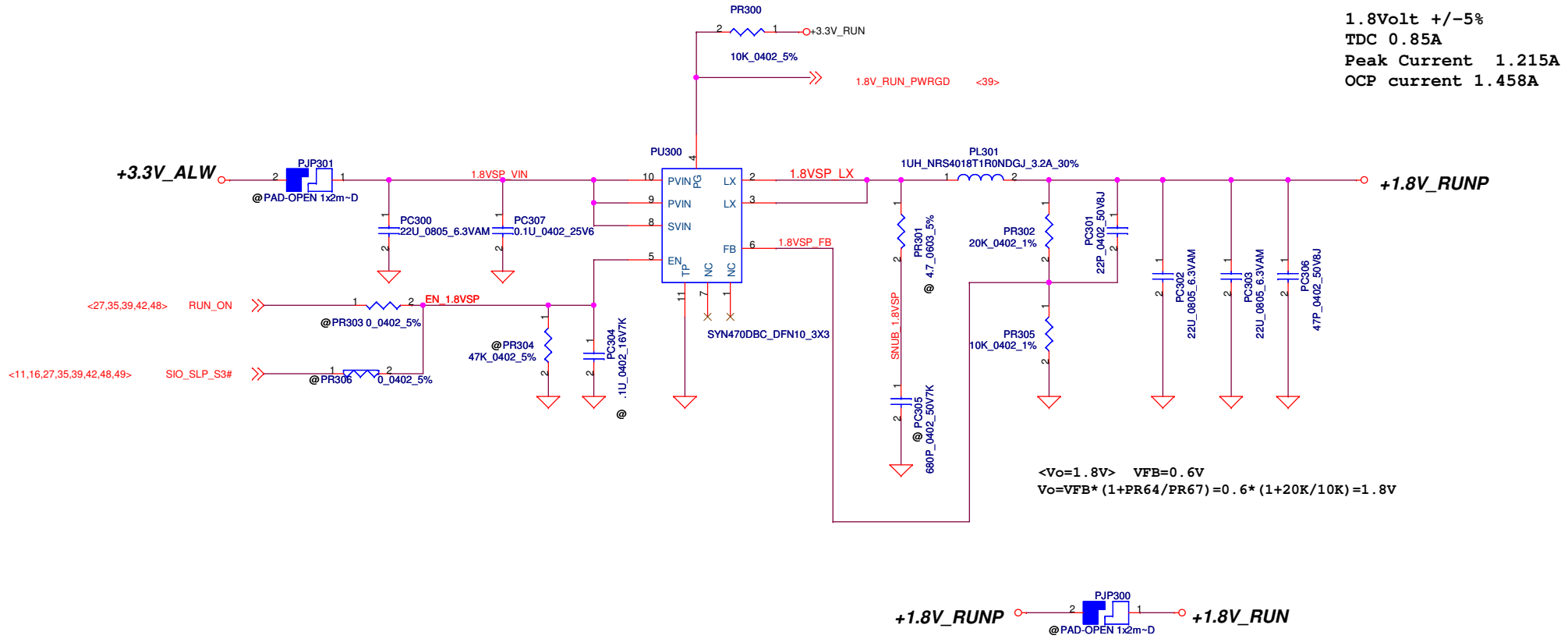
Note: S3 - sleep ; S5 - power off

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Compal Electronics, Inc.		
Title: +1.5V_MEN/+0.75V_DDR_VTT		
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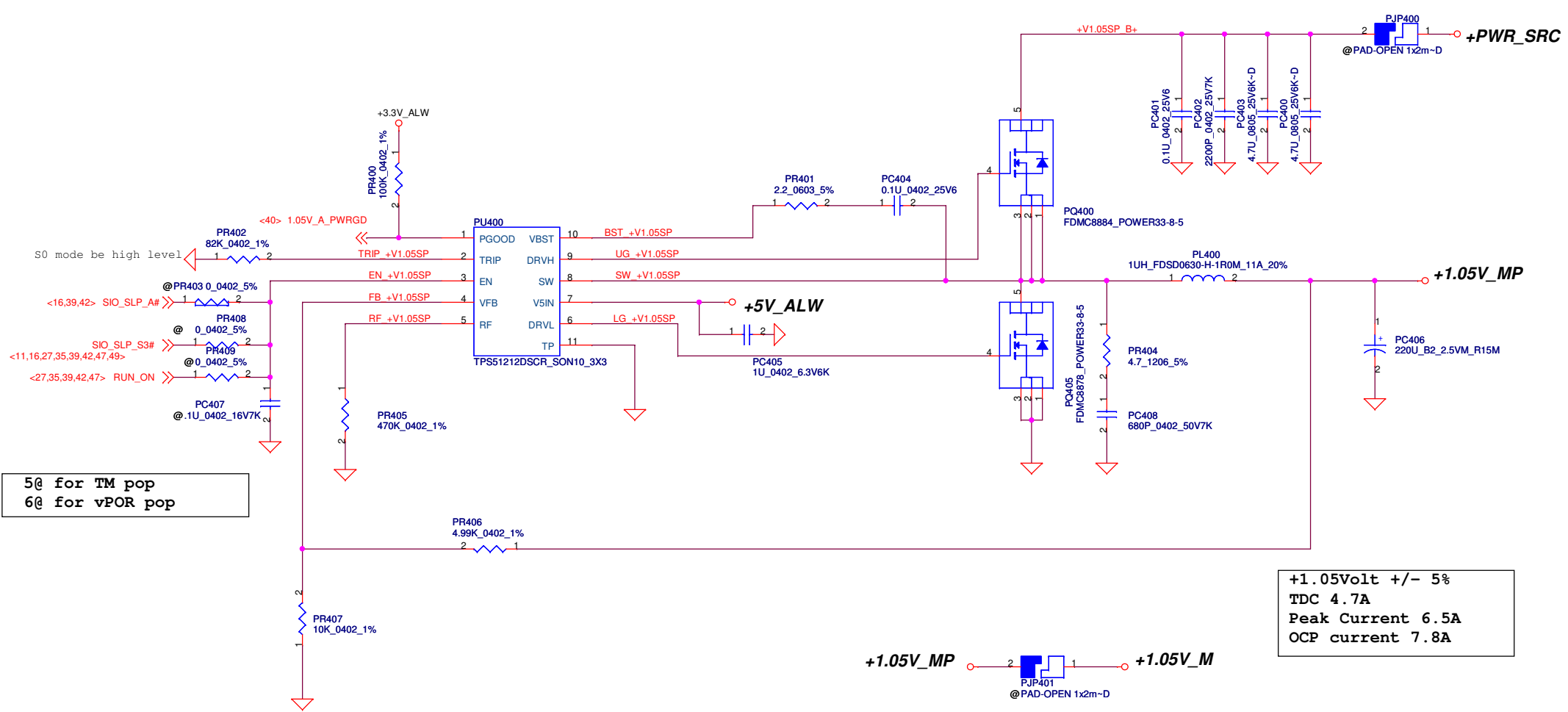
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Compal Electronics, Inc.		
Title		
+1.8V_RUN		
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5@ for TM pop
6@ for vPOR pop

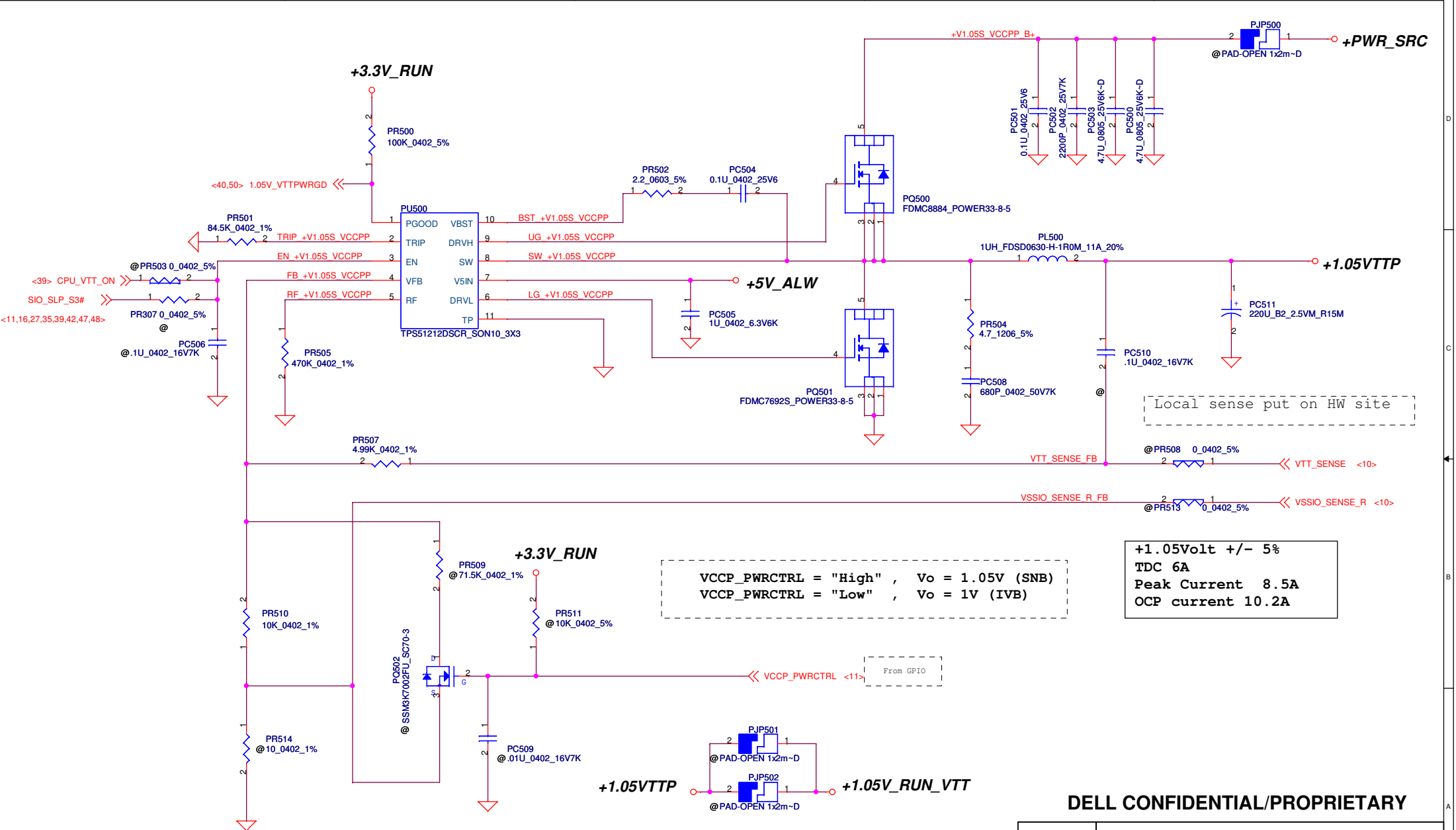
+1.05Volt +/- 5%
TDC 4.7A
Peak Current 6.5A
OCP current 7.8A

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Compal Electronics, Inc.			
+1.05V_M			
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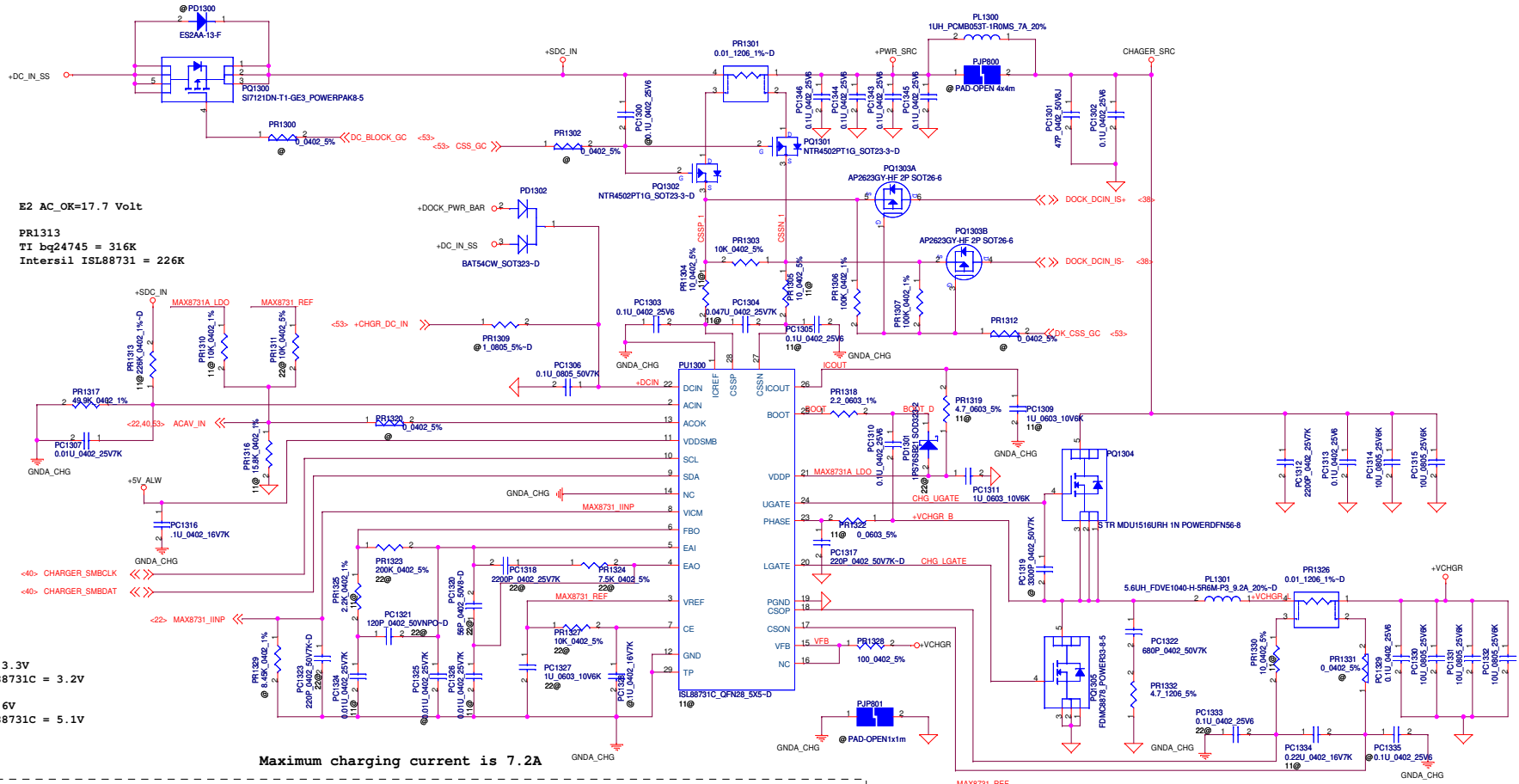
VCCP_PWRCTRL = "High" , Vo = 1.05V (SNB)
 VCCP_PWRCTRL = "Low" , Vo = 1V (IVB)

+1.05Volt +/- 5%
 TDC 6A
 Peak Current 8.5A
 OCP current 10.2A

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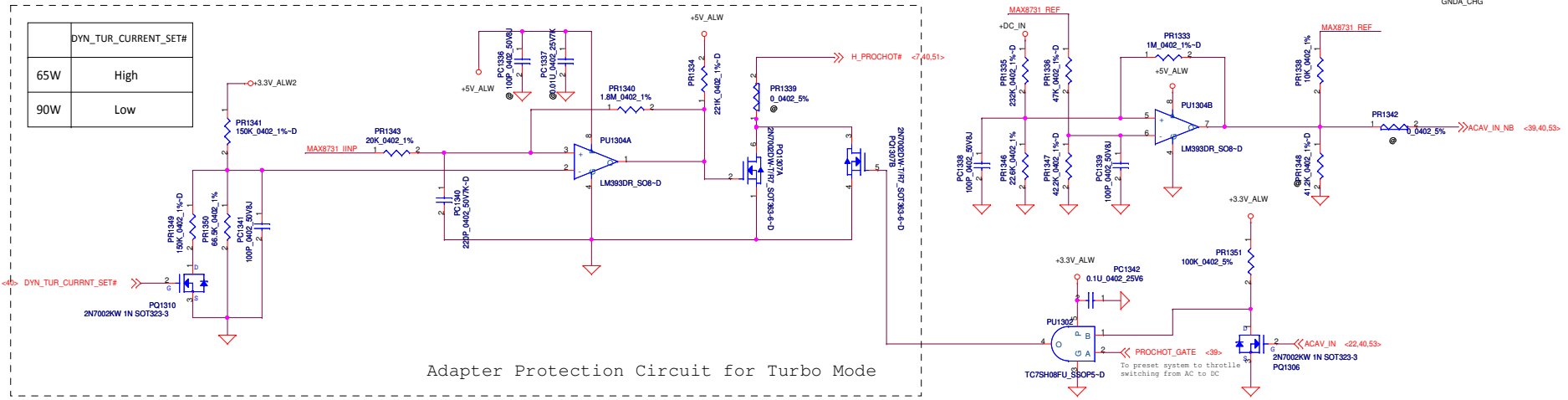
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			Compal Electronics, Inc.	
			+1.05V_RUN_VTT	
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Vref
TI bq24747 = 3.3V
Intersil ISL88731C = 3.2V
VDDP
TI bq24747 = 6V
Intersil ISL88731C = 5.1V

DYN_TUR_CURRENT_SET#	
65W	High
90W	Low

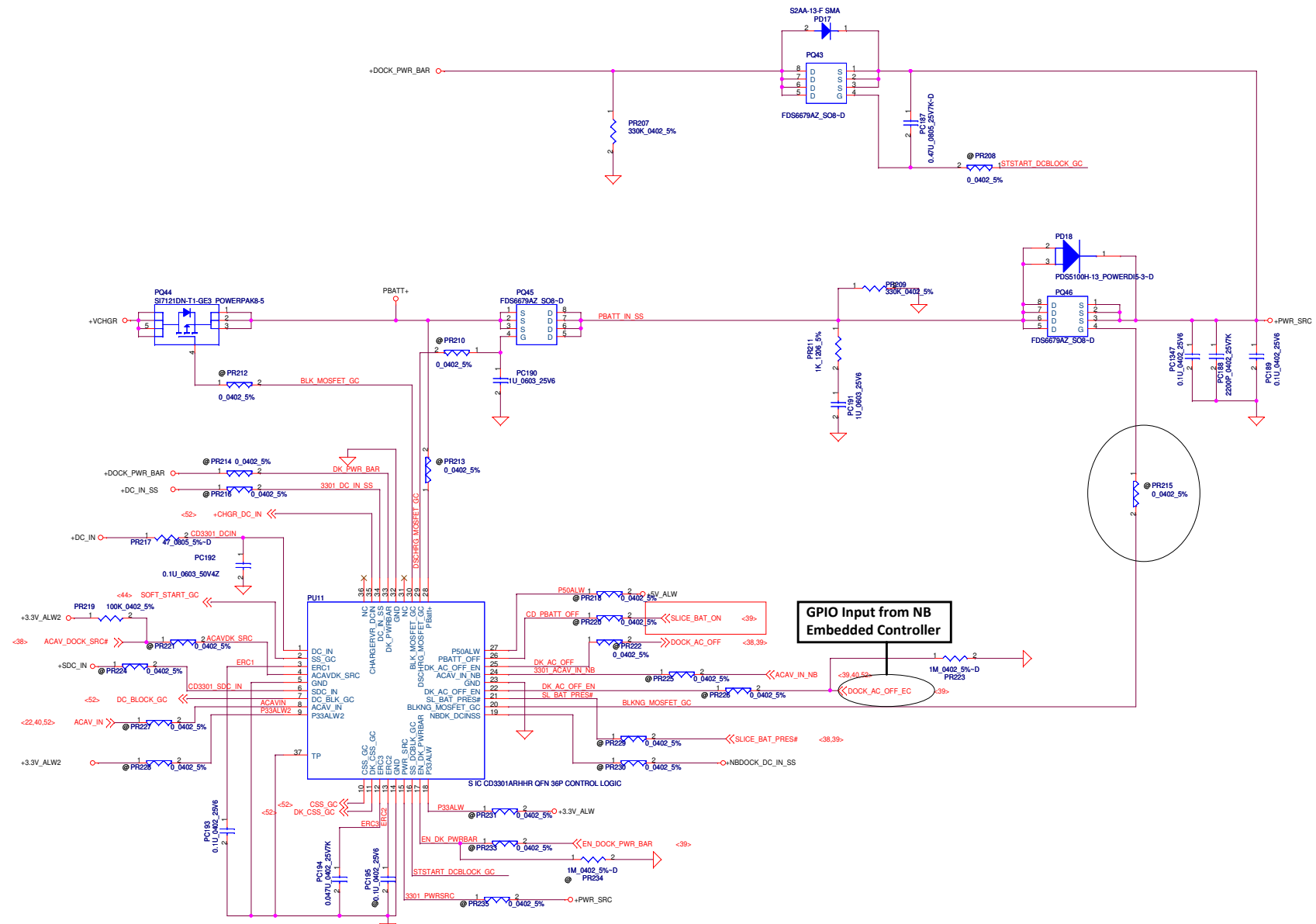


- PU1300 22@
BQ24747
- PR1313 22@
316k_0402_1%
- PR1325 22@
4.7k_0402_1%
- PC1334 22@
0.1U_0402_25V6
- PR1330 22@
0_0402_5%
- PR1304 22@
0_0402_5%
- PR1305 22@
0_0402_5%
- PC1304 22@
0.1U_0402_25V6 1+-5% 0603
- PR1322 22@
10k_0402_5%

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Charger	
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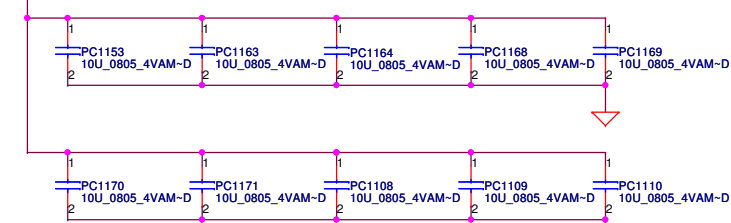
Selector



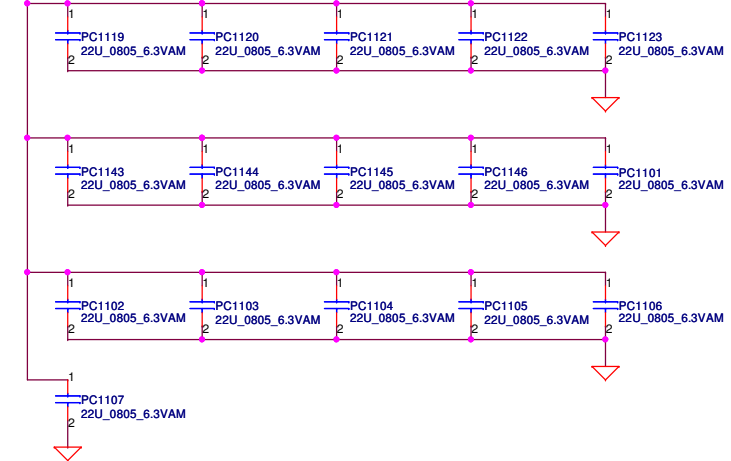
Title	Selector		
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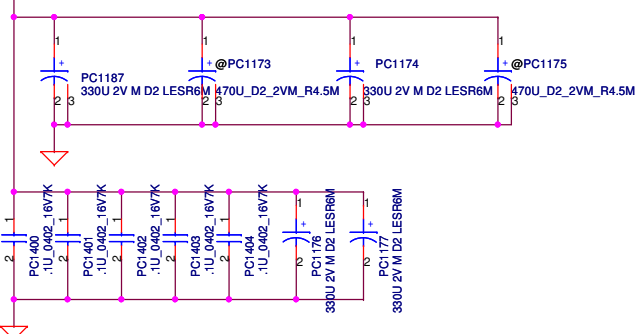
+VCC_CORE



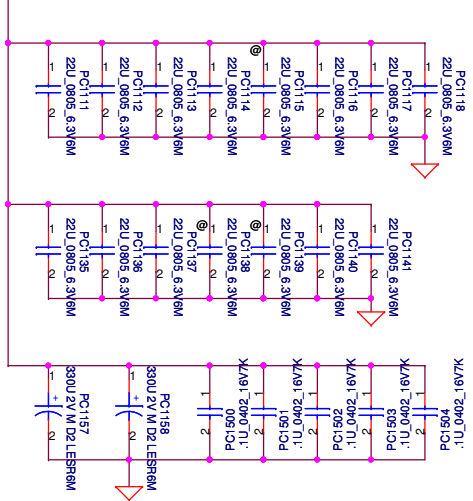
+VCC_CORE



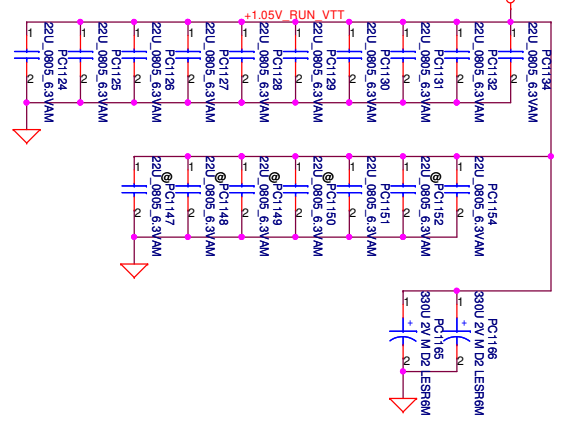
+VCC_CORE



+VCC GFXCORE



+1.05V_RUN_VTT



Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	44	Power	8/18	Compal	ME design change.	PJPDC1 change from 7pin to 5pin	X01
2	45	Power	8/18	Compal	Main and 2nd IC common setting.	De-pop PD100, PR113, PR111	X01
3	45 46	Power	8/18	Compal	Prevent Jitter issue.	Add PC120, PC121, PC215 parallel with PR101, PR102, PR207	X01
4	51	Power	8/18	Compal	Prevent output voltage glitch when power up.	PU700 VCCP and VDD change form +5V_RUN to +5V_ALW	X01
5	53	Power	8/18	Dell	Change net name PBATT to SLICE_BAT_ON.	Change net name same as E4.	X01
6	50	Power	8/18	Compal	Reserve 0 ohm resistance for test.	Add PR90, PR91	X01
7	54	Power	8/31	Compal	Reserve cap for improve transient response.	Reserve PC1176	X01
8	54	Power	8/31	Compal	Change to green P/N.	Change PQ4, PC1153, PC1163, PC1164, PC1168, PC1169, PC1170, PC1171, PC1108, PC1109, PC1110, PC1187, PC1173, PC1174, PC1175, PC1157, PC1158 PQ1310, PQ1306, PC719 to green P/N	X01
9	48	Power	9/1	Dell	For support TL+TM	Change 6@ to pop for PC400~PC406, PC408, PL400, PQ400, PQ405, PR400~PR407, PU400. 5@ to @ for PR408.	X01
10	49	Power	9/1	Compal	For fix 1.05V_RUN_VTT on 1.05V	Depop PR509, PR511, PQ502. Change PR507 to 4.99k.	X01
11	45 52	Power	8/30	Compal	For reduce EMI radiation.	Pop PL100, PL1300	X01
12	51	Power	9/5	Compal	For reduce EMI radiation.	Change PL700 to SM01000DJ00	X01
13	45 46	Power	9/6	Compal	Change to green P/N.	Change PC107, PC263, PC280, PC405, PC505 to HF P/N.	X01
14	52	Power	9/13	Compal	For reduce EMI radiation.	Pop PC1400~1404, PC1500~PC1504.	X01

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Compal Electronics, Inc.		
Title PWR PIR 1		
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
15	51	Power	9/14	Compal	For Vcore OCP setting	Change PC740 to 10nF, PR750 to 365 ohm.	X01
16	51	Power	9/14	Compal	For AXG OCP setting	Change PR702 to 2.61kohm, PR711 to 365ohm.	X01
17	51	Power	9/14	Compal	For Vender proposal	Change PC704 to 390pF, PC705 to 68pF, PC720 to 22pF, PC722 to 390pF, PC723 to 33pF, PR741 to 130kohm, PR703 to 130kohm, PC744 to 3300pF, PR754 to 649ohm.	X01
18	52	Power	11/17	Compal	Shortage issue	Change PQ1303 from NTGD416 to AP2623	X02
19	52	Power	11/17	Compal	Need ESD protected	Change PQ1306, PQ1310 from SB57002040L to SB000009Q80	X02
20	53	Power	11/17	Compal	IC version upgrade	Change PU11 from CD3301 to CD3301A	X02
21	45	Power	11/17	Compal	Shortage issue	Change PC110, PC111 from SGA00004E00 to SGA00002N80	X02
22	44	Power	11/21	Compal	HW requirement for S3 power consumption	PWR_SRC_S control signal change from +3.3V_ALW to PCH_ALW_ON	X02
23	52 53	Power	12/04	Compal	EMI requirement	add PC1343 PC1344 PC1345 PC1346 PC1347 (0.1U_0402_25V6)	X02
24	52	Power	12/04	Compal	EMI requirement	add PC1302 (0.1U_0402_25V6) PC1317 (220P_0402_50V7K~D)	X02
25	52	Power	12/04	Compal	Prevent COS.	change PD1301 from SCS00003M0L to SCS0000400L PD8 from SCS00004L0L to SCS00005C00	X02
26	54	Power	12/13	Compal	Prevent COS.	change PC1174 PC1176 PC1177 PC1187 PC1158 PC1157 PC1165 PC1166 to SGA00002U1L	X02
27	50	Power	12/13	Compal	Improve efficiency	change PR86 to 22K_0402_5%	X02
28	47	Power	12/16	Compal	Prevent COS.	change PL301 to SH00000MW00	X02

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Compal Electronics, Inc.		
Title PWR_PIR 2		
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Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	11	HW	08/15/2011	COMPAL	INTEL review feedback	Add CC178,CC179,CC149,CC150	X01
2	32	HW	08/15/2011	COMPAL	Finger Print connector changed	Change JBI01 to pitch 1.0mm	X01
3	37	HW	08/15/2011	COMPAL	Sniffer Switch location changed	Change JSF1 to SF1	X01
4	14, 39	HW	08/15/2011	COMPAL	SMSC request to delete LPC_LDRQ0#	Leave LDRQ0# no connection on both of 5048 and PCH side Removed R743	X01
5	22	HW	08/15/2011	COMPAL	Removed reserve circuit for EMC4022	Removed R405,C280,R392,R394	X01
6	42	HW	08/15/2011	COMPAL	Load SW sources output rising time mismatch and COS. cost concern	Change back to E3 +3.3V/5V_RUN discrete solution Removed U78 and add Q55,Q61 circuit	X01
7	1, 29	HW	08/15/2011	COMPAL	Codec is change to 92HD93	Pop R162~R166 and de-pop U73,R1540 add R1641 connect the codec pin48 to U73 pin1	X01
8	29	HW	08/15/2011	COMPAL	Reserve co-lay with ALC290	Pop option for 92HD93/ALC290=>R1646/C1164; R1644/R1643; C965/R1642; Q107/R171 Reserve for ALC290 only: C1204, C1205, R1647, C1165, R1648 Reserve for 92HD93 only: R1645, C963 Add R174 depop and R175 pop	X01
9	20, 42	HW	08/15/2011	COMPAL	Vgs less than cut-in voltage in battery mode	Add control circuit QH6,R279,CH107 for +5V_ALW_PCH	X01
10	27, 28	HW	08/15/2011	COMPAL	Vgs of 5V MOS maybe large than max rating	Add R517, R518	X01
11	11	HW	08/15/2011	COMPAL	Follow INTEL PDDG 0.8	De-pop RC140	X01
12	40	HW	08/15/2011	COMPAL	Change board ID to X01	Change R875 to 130Kohms	X01
13	34	HW	08/15/2011	COMPAL	PCH GPIO52 need 8.2~10K pull up +3.3VS	Change R695 from 100K to 10Kohms	X01
14	23	HW	08/15/2011	COMPAL	CRT SW 2nd source TI, TS3V713 pin29 is VDD	Connect U18 pin29 to +3.3V_RUN	X01
15	16	HW	08/15/2011	COMPAL	+1.05V_M turn off before APWROK de-assert	Add UH5,CH108 6@ circuit reserve for VPRO	X01
16	41	HW	08/15/2011	COMPAL	Reset IC threshold voltage issue	Change U4 to RT9801A (threshold adjustable) Add R1649~R1654;Reserve R1655 and pop R1623	X01
17	26	HW	08/15/2011	COMPAL	DPX_CA_DET voltage too low through dongle	Change U21 and U24 to SA000055G0L	X01
18	17, 18	HW	08/15/2011	COMPAL	Request from INTEL review feedback	Pop RH332 for PCH_GPIO3 and RH180 for GPIO27	X01
19	42	HW	08/15/2011	COMPAL	Material changed	Power team request Q59 change to SB00000L80L	X01
20	43	HW	08/15/2011	COMPAL	White light LED brightness is abnormal	Change R934, R938, R939, R949, R958, R957 and R959 to 2.2 Kohms	X01
21	40	HW	08/15/2011	COMPAL	Reserve C1208 for ESD backup plan	Reserve C1208 for ESD backup plan	X01
22	11	HW	08/15/2011	COMPAL	S3 can't resume issue	Control 1.5V_VDDQ by EC. Pop RC79 and de-pop RC82	X01
23	15	HW	08/15/2011	COMPAL	Fine tune CLK EA	Changed RH311,RH314 to 10 ohm	X01


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HW_PIR 1			
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
24	17,18	HW	08/16/2011	COMPAL	INTEL review feedback	Change RH331,RH272 to 10K ohm	X01
25	34	HW	08/16/2011	COMPAL	WWAN card request	JMINI1 pin 1 connect to PCIE_WAKE#	X01
26	1,14	HW	08/16/2011	COMPAL	ROM size changed	Change U52 to 8M and R936,R895,R897,R900 to 6@	X01
27	11	HW	08/17/2011	COMPAL	Material package changed	Change CC161~CC166 from 0402 to 0603	X01
28	42	HW	08/17/2011	COMPAL	BOM changed	Change Q60 to 6@	X01
29	31	HW	08/17/2011	COMPAL	Correct Lan power net name	Change LL1,LL4,LL6~LL8 pin 2 net from +3.3V* to +1.2V*	X01
30	39	HW	08/19/2011	COMPAL	GPIO signal name changed same as E/P	Change PBATT_OFF to SLICE_BAT_ON	X01
31	34	HW	08/19/2011	COMPAL	Material package changed	Changed C615,C1176	X01
32	37	HW	08/26/2011	COMPAL	Change audio connector pin definition.	Change JAUD1 pin15 to NC	X01
33	29	HW	08/29/2011	COMPAL	Remove reserve co-lay with ALC290 circuit	Remove below circuit: Pop option for 92HD93/ALC290=>R1646/C1164; R1644/R1643; C965/R1642; Q107/R171 Reserve for ALC290 only: C1204, C1205, R1647, C1165, R1648 Reserve for 92HD93 only: R1645, C963 Add R174 depop and R175 pop	X01
34	43	HW	08/29/2011	COMPAL	White light LED brightness is abnormal	Change R934, R938, R939, R949, R958, R957 and R959 to 1.2 Kohms	X01
35	25	HW	08/30/2011	COMPAL	Due to EMI HDMI test Fail, add EMI solution	Change resistor to Inductor Change R451, R459, R462, R466, R468, R469, R470, R471 to (Inductor CIS symbol is not ready) Add C1209, C1210, C1211, C1212, C1213, C1214, C1215 and C1216 between Inductor and HDMI connector	X01
36	37	HW	08/30/2011	COMPAL	Follow CONN List_0824 Change JAUD1 to ACES_51522-02001-001	Change JAUD1 to ACES_51522-02001-001 and swap pin because pin1 definition different	X01
37	24	HW	08/31/2011	COMPAL	Follow CONN List_0824 Change JLVDS1 to STARC_111H40-100000-G4-R	Change JLVDS1 to STARC_111H40-100000-G4-R	X01
38	25	HW	08/31/2011	COMPAL	For EMI solution de-pop L19~L22 and pop 0ohm resistors(need change to Inductor)	de-pop L19~L22 and pop R451, R459, R462, R466, R468, R469, R470, R471(need change to Inductor)	X01
39	30	HW	08/31/2011	COMPAL	Change RL23 to 1.2k for IEEE EA	Change RL23 to 1.2k for IEEE EA	X01
40	30	HW	08/31/2011	COMPAL	Change 3.3V LAN control signal pop option for TM/TL	Change RL46 to pop & RL47 to @	X01
41	14,16,19,22,30,40,42	HW	09/02/2011	COMPAL	Change pop option for TM/TL	Change 6@ to pop; 5@ to @ Change R871 pop, R877 depop	X01
42	37	HW	09/05/2011	COMPAL	Reserved 2 GND pins for Audio performance issue.	Add JAG1 2 pin connector.	X01
43	14,15	HW	09/06/2011	COMPAL	Change Cap value for Crystal EA	Change CH2, CH3 from 15pF to 18pF Change CH18, CH19 from 12pF to 10pF	X01
44	25	HW	09/06/2011	COMPAL	For EMI solution change resistor to Inductor	Change 0ohm (R451, R459, R462, R466, R468, R469, R470, R471) to 9nH (L99,L100,L101,L102,L103,L104, L105,L106)	X01

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45	15, 30, 40	HW	09/06/2011	COMPAL	Reserved TM LAN SMBus	Add QH8, RL48~RL51	X01
46	37	HW	09/07/2011	COMPAL	Change USB common choke from Audio/B to M/B	Add L107 & R1656,R1657	X01
47	07	HW	09/07/2011	COMPAL	PCH_PLTRST#_R & VCCPWRGOOD_0_R add 2 CAP to GND for ESD.	Add CC141 & CC142	X01
48	24	HW	09/08/2011	COMPAL	DMIC0 & DMIC_CLK0 add 100pF CAP close to JLVDS	Reserve C1217 & C1218	X01
49	36	HW	09/08/2011	COMPAL	Change USB3.0 CAP to 0.1uF	Change C412,C413,C414,C415 to 0.1uF	X01
50	29	HW	09/08/2011	COMPAL	Change AGND to DGND CAP to pop	Change C982,C985,C986,C987 to pop	X01
51	07	HW	09/09/2011	COMPAL	Change RC25 value for ESD	Change RC25 from 0ohm to 1kohm	X01
52	32	HW	09/09/2011	COMPAL	Swap JBIO1 pin define	Swap JBIO1 pin define	X01
53	29	HW	09/13/2011	COMPAL	IDT suggest exchange location R169~R172 & C973~C976. Change L91~L94 part number to 0ohm	IDT suggest exchange location R169~R172 & C973~C976. Change L91~L94 part number to 0ohm	X01
54	42	HW	09/13/2011	COMPAL	Change Q55,Q61 part for open soldering issue.	Change Q55,Q61 from DMN3030LSS-13 to AO4478L	X01
55	15	HW	09/13/2011	COMPAL	CLK_SMART_48M reserve 10pF CAP to GND for RF	Reserve CE18 to GND	X01
56	15, 30	HW	09/13/2011	COMPAL	Change LAN SMBus pop option.	Change QH8,RL50,RL51 to pop & RL48,RL49 to de-pop	X01
57	29	HW	09/15/2011	COMPAL	Follow EMI recommand	Change L91~L94 to 2A bead	X01
58	19	HW	09/15/2011	COMPAL	Change LH1 from bead to Inductor for CRT	Change LH1 to 1uH Inductor (SHI00007W0L)	X01
59	40	HW	11/28/2011	COMPAL	Crystal EA result, change CAP value.	Change C741,C743 to 33pF (PT Memo)	X02
60	39	HW	11/28/2011	COMPAL	EXPRESS card insert in 15" vPro can't power on issue	Change R760 to 20k ohm (PT Memo)	X02
61	40	HW	11/28/2011	COMPAL	Change board ID to X02	Change R875 to 62Kohms	X02
62	42	HW	11/28/2011	COMPAL	Rated Vgs of Q61 is 25V	De-pop R1627 (PT Memo)	X02
63	39	HW	11/28/2011	COMPAL	SMSC change 5048 pin A23 to GPIOIO	Re-link ECE 5048 symbol	X02
64	40	HW	11/28/2011	COMPAL	SMSC review feedback	Reserve R1658 and R1659 100Kohms to GND for I2S disabled	X02
65	41	HW	11/28/2011	COMPAL	Change reset IC to RT9818A-44GU3	Update U4 symbol and add R1629 for backup of inrush prevention. Change RSMRST# pull up with 100Koms. Pop R1655 and de-pop R1623.Delete R1649~R1654	X02
66	39	HW	11/28/2011	COMPAL	When suspend/resume cycles, wireless SW GPIO IRQs keeps giving	Add R771 pulling up to +3.3V_ALW for WIRELESS_ON#/OFF and de-pop R766	X02
67	27	HW	11/28/2011	COMPAL	Depop HDD control power circuit for cost down.	Depop R1624, Q28, R500, R499, R517, C393	X02

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68	30	HW	11/28/2011	COMPAL	Crystal EA result	Change YL1 to 3G025000FA1H, CL5,CL6 to 12pF. (PT Memo)	X02
69	11, 42	HW	11/28/2011	COMPAL	Change MOSFET to without Schottky Diode	Change QC3 and Q59 to AO4304L_S08	X02
70	34	HW	11/28/2011	COMPAL	S3 had leakage in +3/5V_RUN	De-pop R725, remove R695 and add +3.3V_RUN pull high at PCH side(RH361)	X02
71	32	HW	11/28/2011	COMPAL	TPM is changed to AT97SC3204-X2A18-AB	U39(TPM) is changed to SA00004WQ10(AT97SC3204-X2A18-AB) for WIN8 support	X02
72	32	HW	11/28/2011	COMPAL	+3.3V_RUN Giltch when AC plugin	Reserve D87, R1663 (pull high to +3.3V_RUN_TPM) and add R1662 for HW solution backup	X02
73	14~21	HW	11/28/2011	COMPAL	Change PCH to C1 version	Change UH4 to SA00005AG1L(HM77 for non vpro)	X02
74		HW	11/28/2011	COMPAL	Change RC value at Gate of MOS Load SW to modify power rail soft start timing	RC72 from 100K to 330K; RC143 form 330K to 1M; CC136 form 0.1u to 0.022u R412 from 100K to 470K; R1632 form 1M to 4.7M; C293 form 0.1u to 0.022u R507 from 100K to 470K; R517 form 1M to 4.7M; C400 form 0.1u to 0.022u R722 from 100K to 470K; R1625 form 1M to 4.7M; C644 form 4700p to 220p R729 from 100K to 470K; R1628 form 1M to 4.7M; C650 form 4700p to 220p R917 from 100K to 470K; R1617 form 1M to 4.7M; C770 form 4700p to 220p R920 from 100K to 470K; R1610 form 470K to 2.2M; C771 form 4700p to 470p R930 from 100K to 330K; R1611 form 470K to 1M; C773 form 2200p to 100p R906 from 100K to 470K; C763 form 2200p to 220p R912 from 100K to 470K; C766 form 470p to 220p	X02
75	36	HW	11/28/2011	COMPAL	Change P/N for HF	Change C412~C415 P/N to SE076104K8L	X02
76		HW	11/28/2011	COMPAL	For cost saving	Change 0 ohm to R-short	X02
77	37	HW	12/01/2011	COMPAL	Remove 2pin connector for Audio performance	Remove JAG1 2 pin connector.	X02
78	15	HW	12/01/2011	COMPAL	Add 10pF CAP to GND for RF request	SIO_14M add CE19(10pF) to GND	X02
79	35	HW	12/01/2011	COMPAL	Reserve 0.1uF CAP to GND for ESD request	PCH_PLTRST#_EC & EXPCLK_REQ# reserve 0.1uF CAP(CE14,CE20) to GND	X02
80	35	HW	12/02/2011	COMPAL	Reserve 0.1uF CAP to GND for ESD request	EXPRESS_DET# reserve 0.1uF CAP(CE22) to GND	X02
81	37	HW	12/05/2011	COMPAL	Follow CONN List_1130A Change JAUD1 to ACES_51522-0200N-P01	Change JAUD1 to ACES_51522-0200N-P01 and swap pin because pin1 definition different	X02
82	17, 38	HW	12/07/2011	COMPAL	EMI solution for E-Docking USB port	Swap USB Port7 and Port8 and reserve a choke(L108) at E-Docking side: Port7 from NA to E-docking ; Port8 from E-Docking to NA	X02
83	24, 32, 37	HW	12/07/2011	COMPAL	Change USB9,12,13 CMC to 180ohm for EMI request	Change L10,L52,L107 to SM070002X00(OCF2012181YZF)	X02
84	22	HW	12/09/2011	COMPAL	Thermal requests to change OTP from 88 to 92	Change R406 from 953ohm to 1.24Kohm	X02
85	41	HW	12/09/2011	COMPAL	To prevent inrush current at reset IC input	Change R1629 from 0ohms to 33ohm resistor	X02
86	25	HW	12/13/2011	COMPAL	Change HDMI R,C value for EMI request	Change R448,R449,R450,R452,R453,R454,R455,R456 from 680ohm to 604ohm; C1209~C1216 from 4.7pF to 3.9pF	X02
87	42	HW	12/15/2011	COMPAL	+3.3V_SUS sequence timing	R911 from 100K to 470K; R1618 from 1M to 4.7M; C767 from 4700p to 220p	X02
88	43	HW	12/15/2011	COMPAL	Change current limit resistors of LED	R934 from 1.2K to 910, R957 from 1.2K to 820, R951 from 330 to 200, R938 from 1.2K to 1.5K, R958 from 1.2K to 1K, R953 from 330 to 300 and R939 from 1.2K to 1.8K	X02

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89	38	HW	02/10/2012	COMPAL	Dalmore14 UMA hang on white screen issue when attached AC+media battery after hot dock.	Change R755 from 100k ohm to 10k ohm	A00
90	33	HW	02/10/2012	COMPAL	Change SD CLK damping resistor for EMI request	Change R676 from 33 ohm to 10 ohm	A00
91	43	HW	02/24/2012	COMPAL	Change current limit resistors of LED	Change R958 from 1K to 1.3K (ST Memo)	A00
92	40	HW	02/24/2012	COMPAL	SMSC creates a new catalog part number and IC marking for the MEC5055	Change U51 P/N to SA00003TZ2L	A00
93	40	HW	02/24/2012	COMPAL	Change board ID to A00	Change R875 to 33K ohm	A00
94	32	HW	02/24/2012	COMPAL	Change BOM option for TPM/TCM funtion	Change C550,C551,C552,C553,R659,R660,R1662,RH311 BOM option to 5@	A00
95	25	HW	03/02/2012	COMPAL	SMT request to change F2 footprint	For DFX conern of F2 2nd source, SP040003H0L, change F2 footprint to F_MF-MSMF050-2	A00
96	14~21, 30	HW	03/02/2012	COMPAL	Change PCH chip P/N for X-build	UH4 is changed to SA00005AG3L(wait confirm with PJE)	A00
97	14	HW	03/02/2012	COMPAL	De-pop resistor on PCH JTAG for power saving	De-pop RH288, RH47, RH48 and RH49	A00

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