

Cedar Schematic Beema

2014-03-05

REV : A00

DY : None Installed

UMA: UMA only installed

OPS: DISCRTE SG installed

Cedar UMA 14

緯創資通 **Wistron Corporation**
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Cover Page

Size
A3

Document Number

Rev

Cedar AMD BEEMA

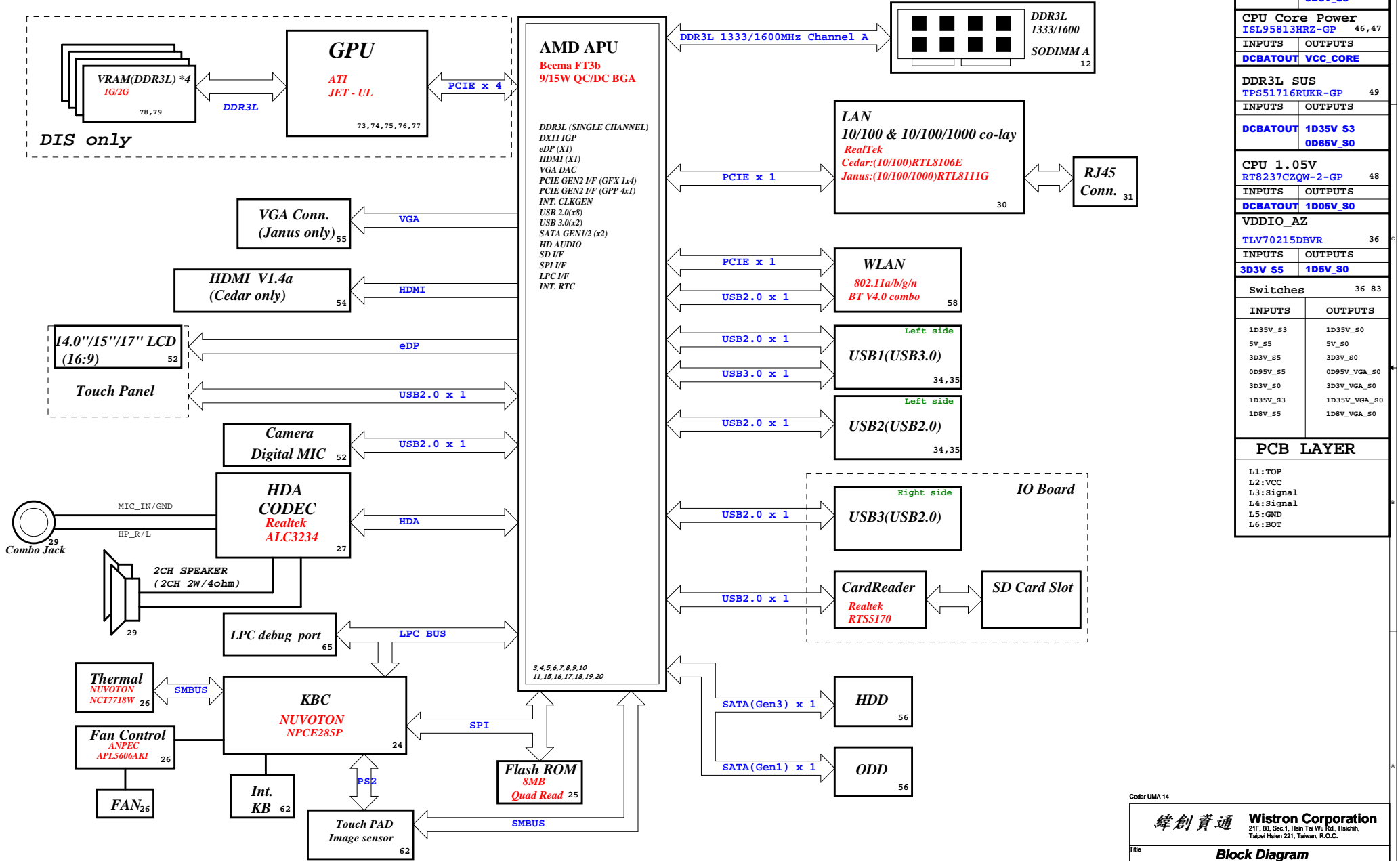
A00

Date: Wednesday, March 05, 2014

Sheet 1 of 104

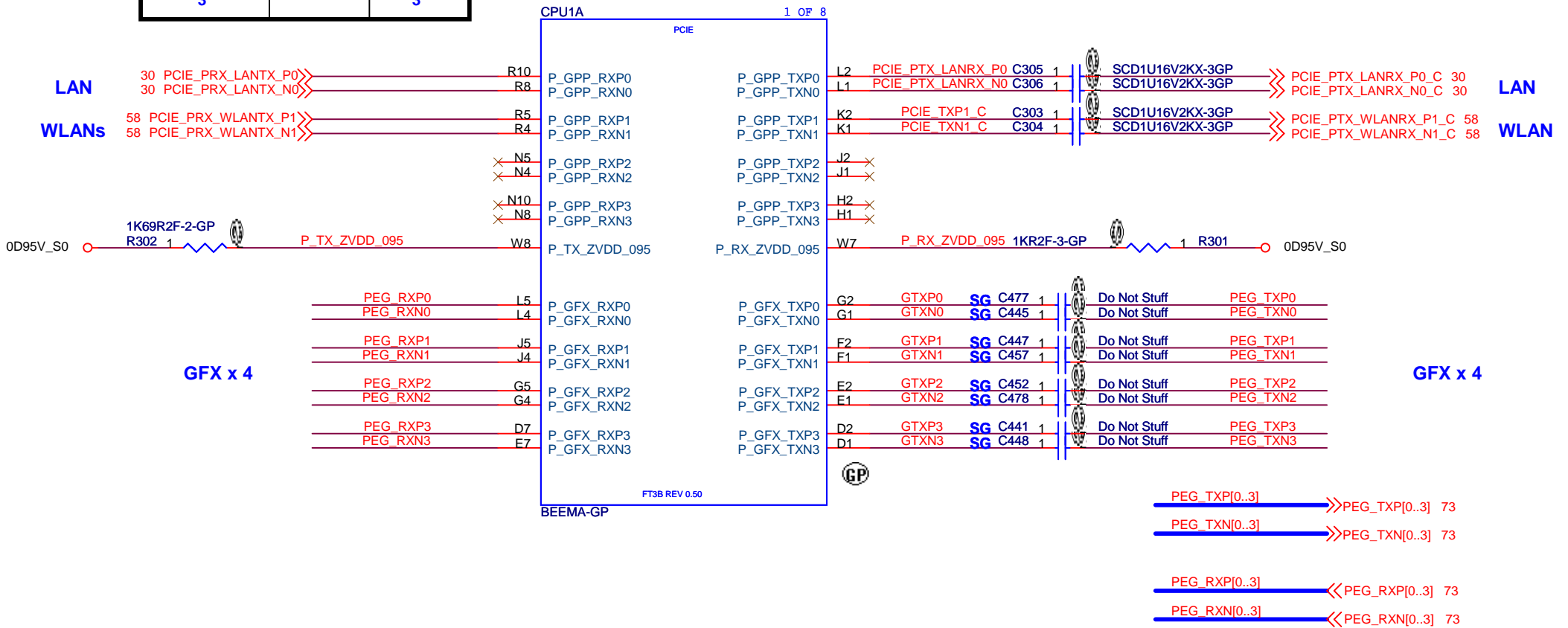
Cedar Block Diagram

Project code:4PD00G010001
 PCB P/N: 13283-1
 Revision: A00

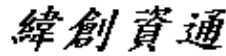


CHARGER		44
BQ24727RGR		
INPUTS	OUTPUTS	
AD+	DCBATOUT	
BT+		
SYSTEM DC/DC		45
TPS51225RUKR-GP		
INPUTS	OUTPUTS	
DCBATOUT	3D3V_AUX_S5	
	5V_AUX_S5	
	5V_S5	
	3D3V_S5	
CPU Core Power		46,47
ISL95813HRZ-GP		
INPUTS	OUTPUTS	
DCBATOUT	VCC_CORE	
DDR3L SUS		49
TPS51716RUKR-GP		
INPUTS	OUTPUTS	
DCBATOUT	1D35V_S3	
	0D65V_S0	
CPU 1.05V		48
RT8237CZQW-2-GP		
INPUTS	OUTPUTS	
DCBATOUT	1D05V_S0	
VDDIO_AZ		36
TLV70215DBVR		
INPUTS	OUTPUTS	
3D3V_S5	1D5V_S0	
Switches		36 83
INPUTS	OUTPUTS	
1D35V_S3	1D35V_S0	
5V_S5	5V_S0	
3D3V_S5	3D3V_S0	
0D95V_S5	0D95V_VGA_S0	
3D3V_S0	3D3V_VGA_S0	
1D35V_S3	1D35V_VGA_S0	
1D8V_S5	1D8V_VGA_S0	
PCB LAYER		
L1: TOP		
L2: VCC		
L3: Signal		
L4: Signal		
L5: GND		
L6: BOT		

GPP CLK port	Device	CLKREQ#
0	LAN	0
1	LAN	1
2	WLAN	2
3	WLAN	3

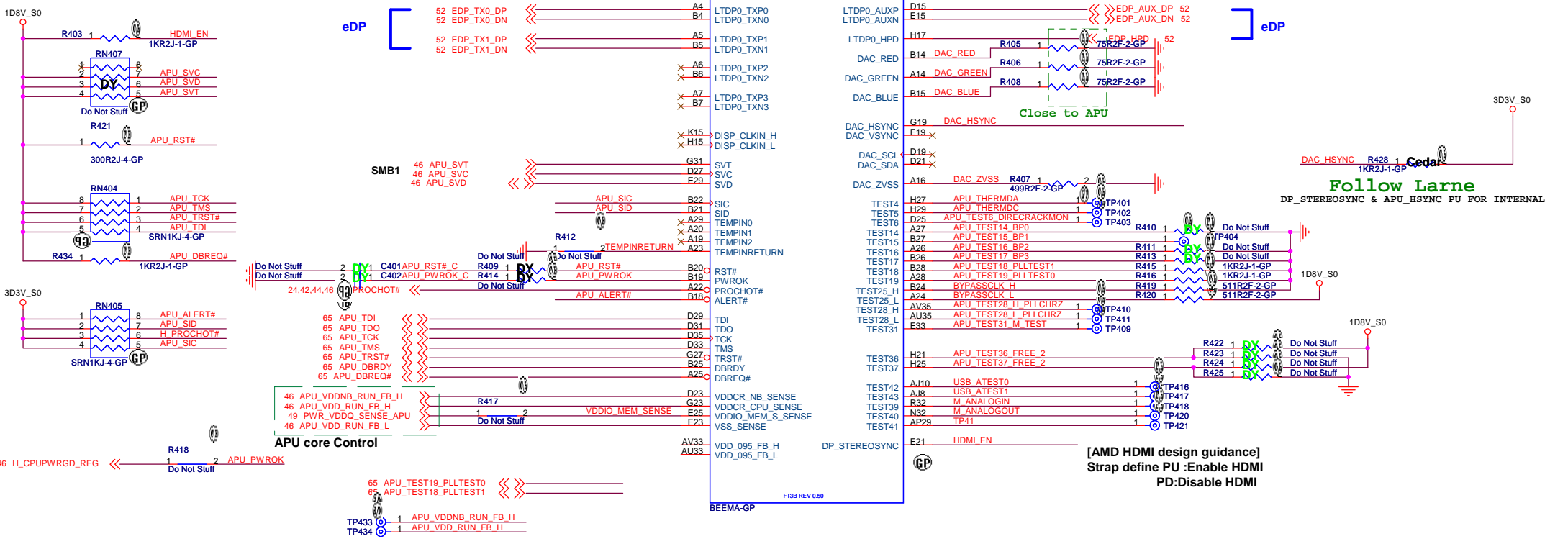


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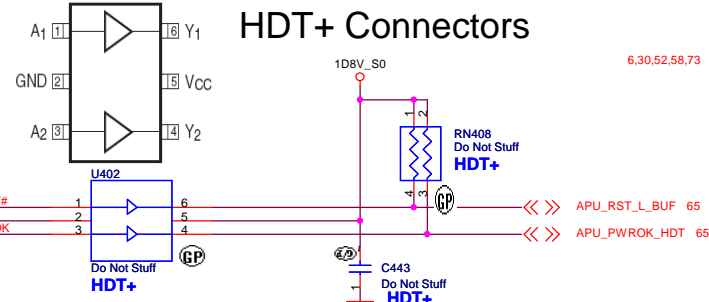
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CPU (PCIE)		
Size A4	Document Number	Rev
Cedar AMD BEEMA		A00
Date: Wednesday, March 05, 2014	Sheet 3 of 104	

Pre-PWROK METAL VID CODES

SVD	SVC	Output Voltage
0	0	1.1
1	0	1.0
0	1	0.9
1	1	0.8



HDT+ Connectors



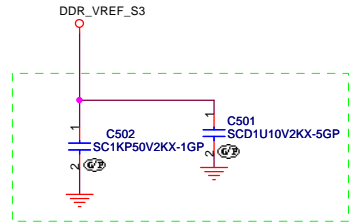
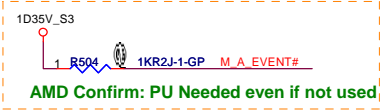
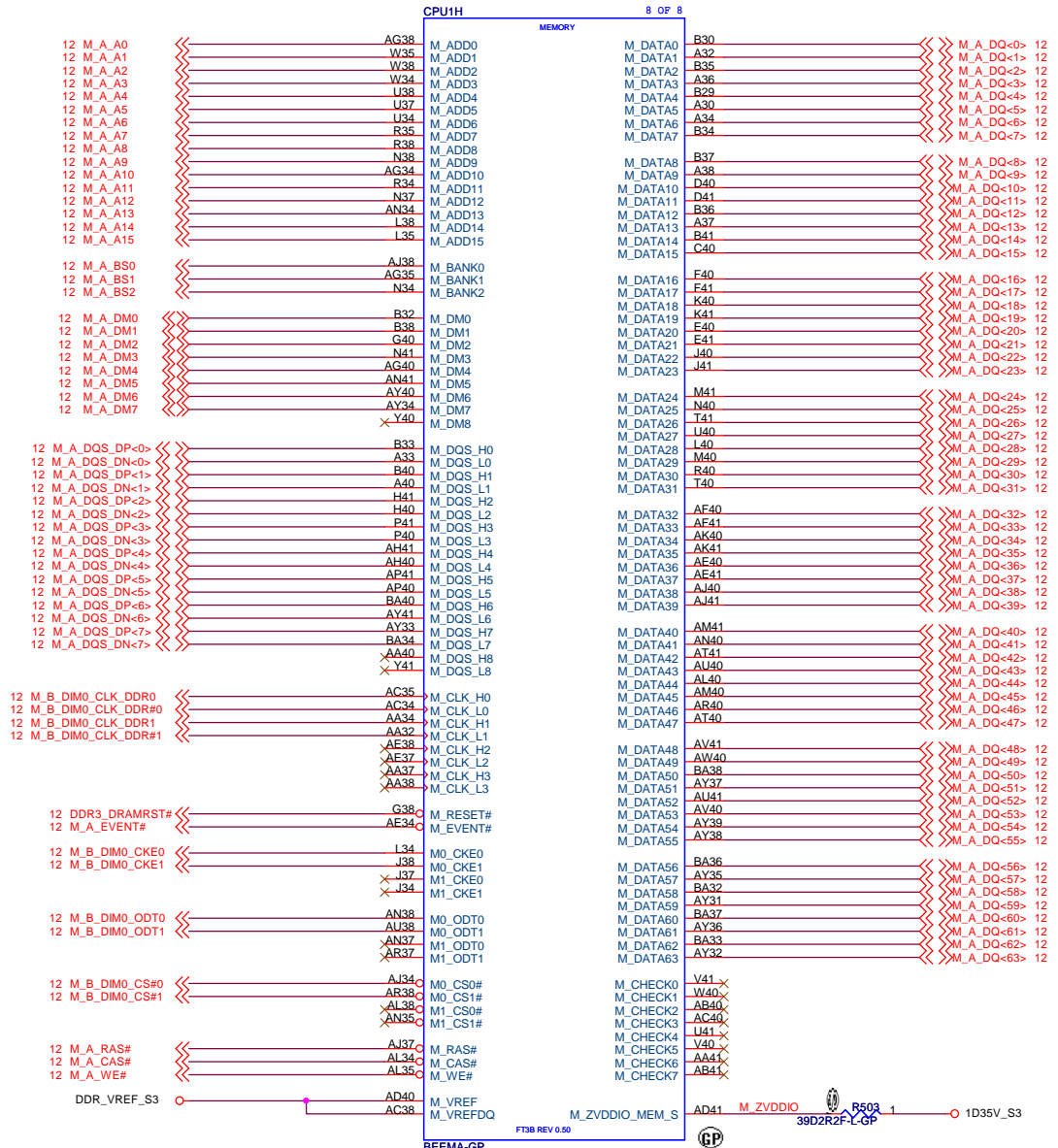
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Title: **CPU (DISPLAY/SVIZ/JTAG/TEST)**

Size A3 Document Number **Cedar AMD BEEMA** Rev **A00**

Date: Wednesday, March 05, 2014 Sheet 4 of 104



LAYOUT: place them close to APU

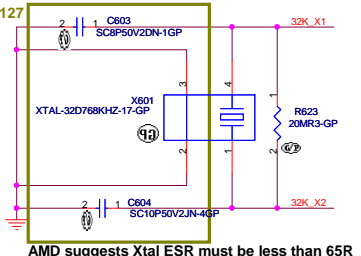
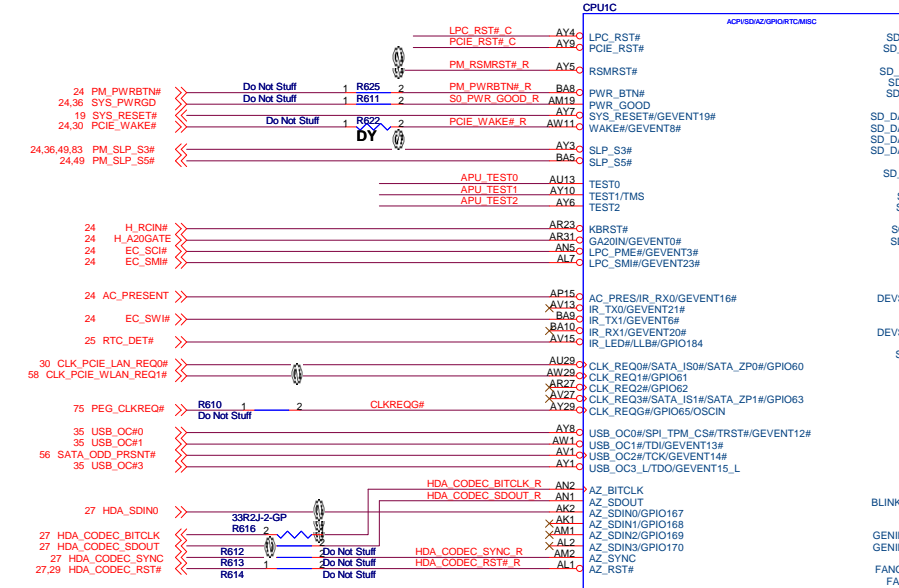
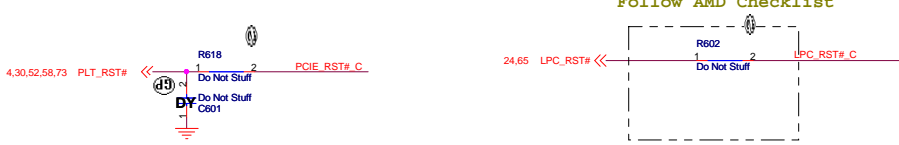
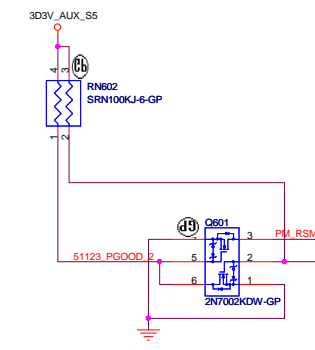
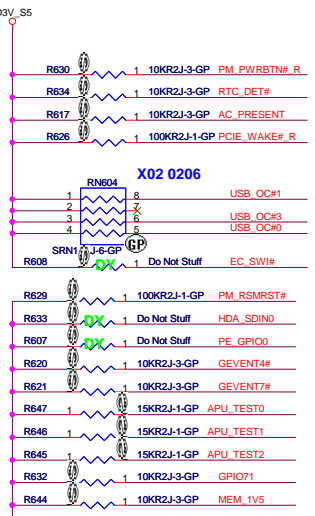
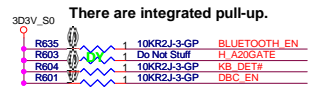
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Title: **CPU (DDR)**

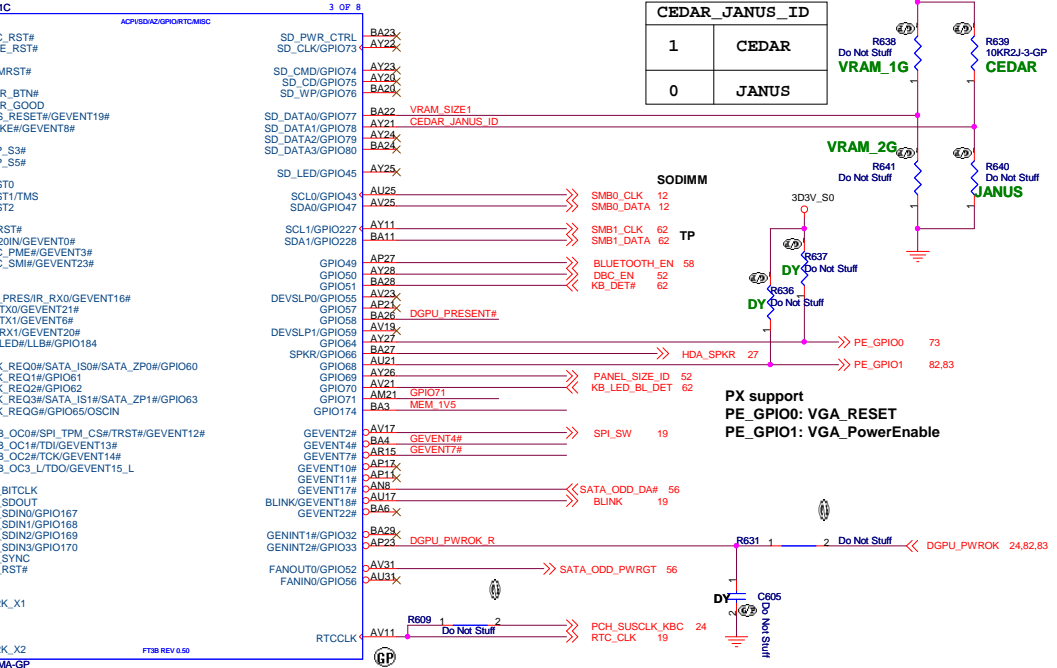
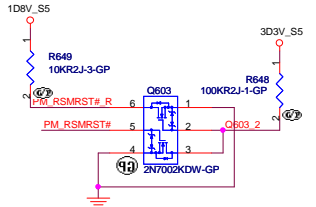
Size A3 Document Number: **Cedar AMD BEEMA** Rev: **A00**

Date: Wednesday, March 05, 2014 Sheet 5 of 104



XTAL	CLK, Hz
0	System & USB 48M
1	RTC 32.768K
2	LAN 25M
3	VGA 27M

AMD suggests Xtal ESR must be less than 65R

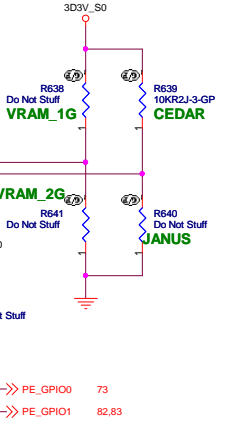


VRAM SIZE1

1	1G
0	2G

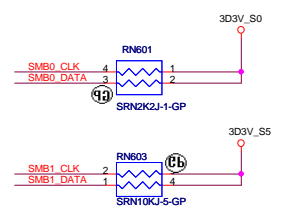
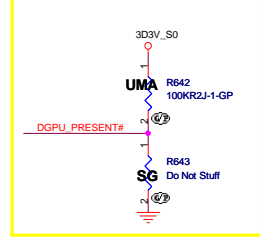
CEDAR_JANUS_ID

1	CEDAR
0	JANUS

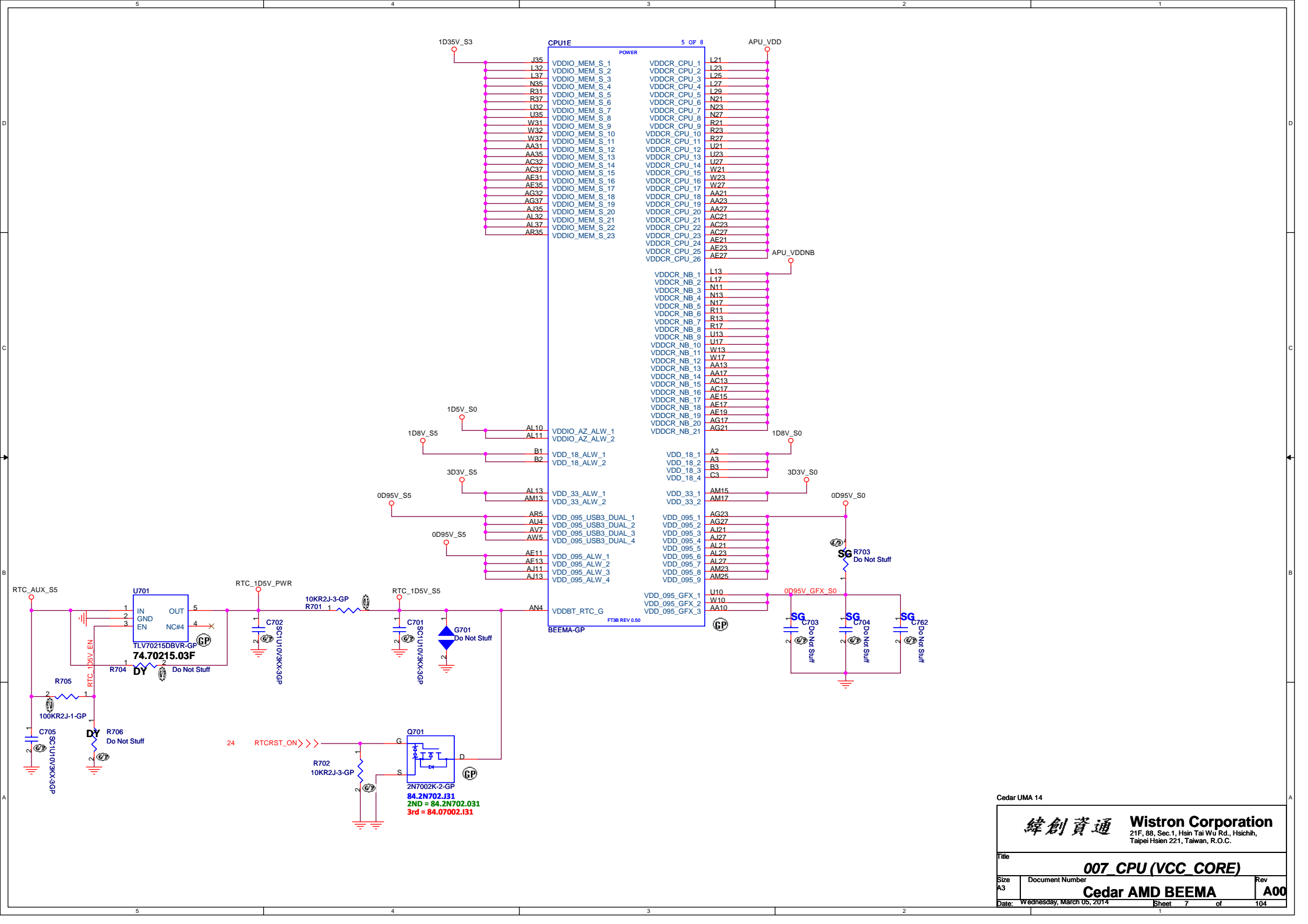


PX support
PE_GPIO0: VGA_RESET
PE_GPIO1: VGA_PowerEnable

Report APU
H=UMA L=DISCRETE



Cedar UMA 14



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Title			007 CPU (VCC CORE)		
Size	Document Number			Rev	
A3					A00
Date:	Wednesday, March 05, 2014	Sheet	7	of	104

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Cedar UMA 14

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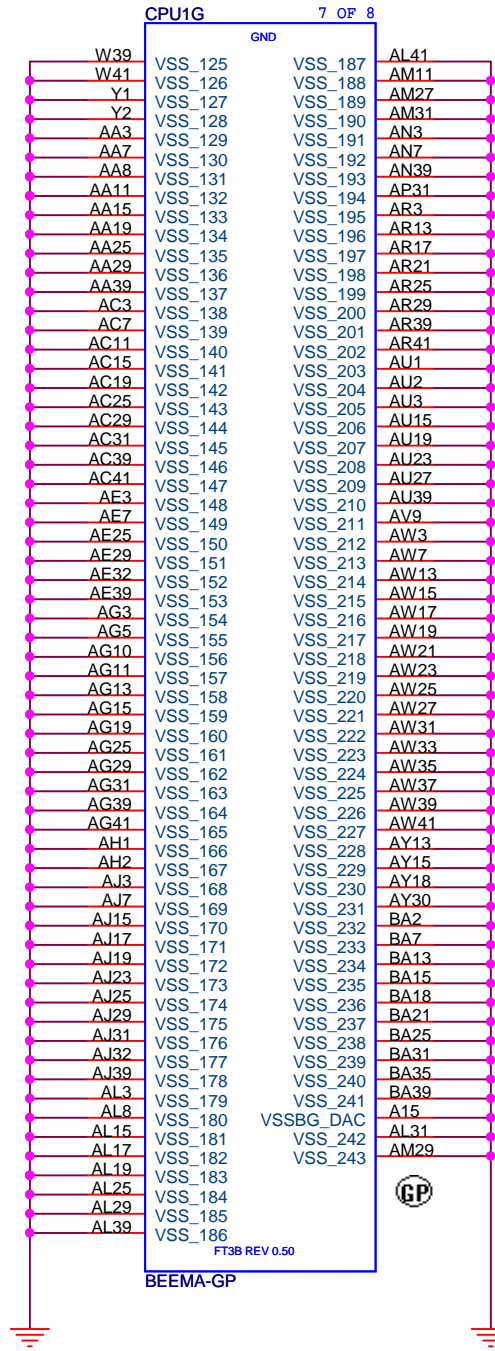
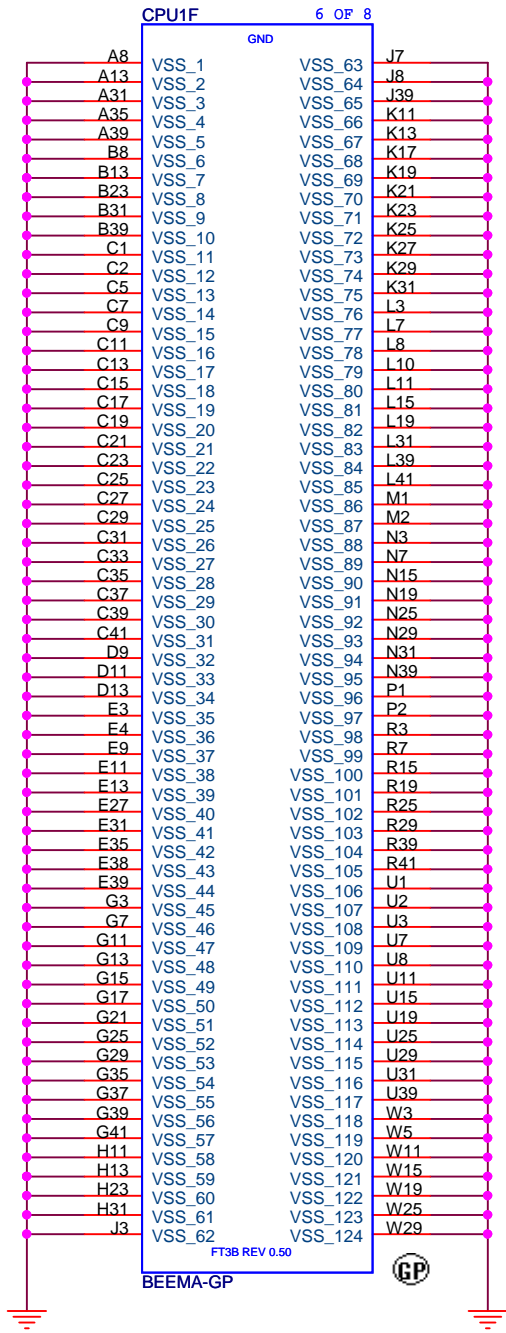
Cedar AMD BEEMA

Rev

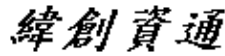
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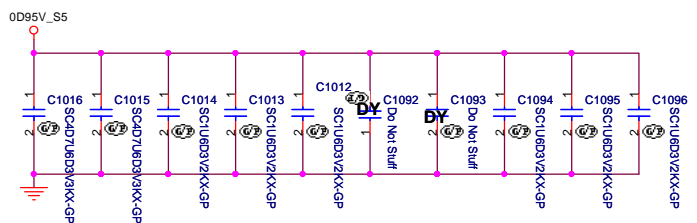
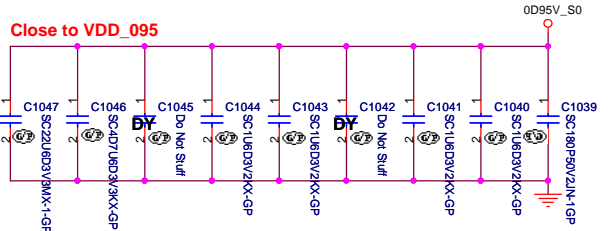
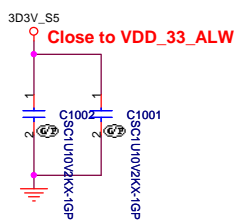
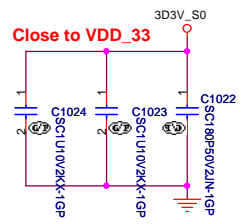
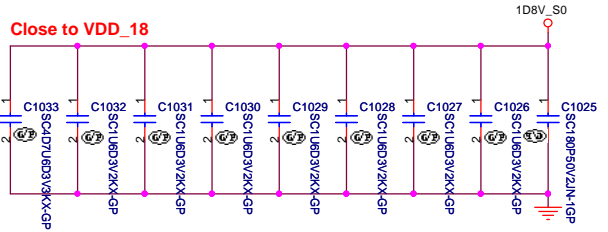
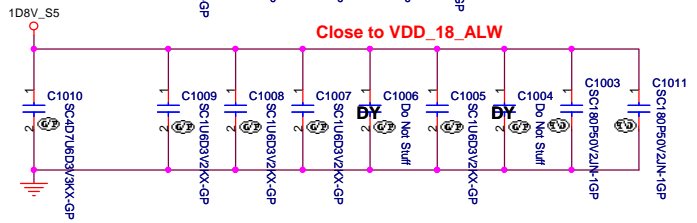
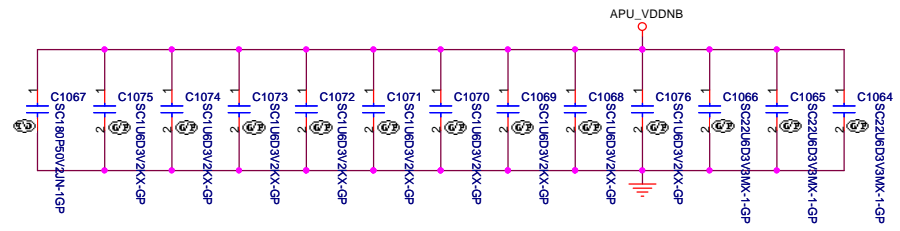
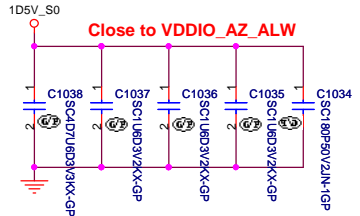
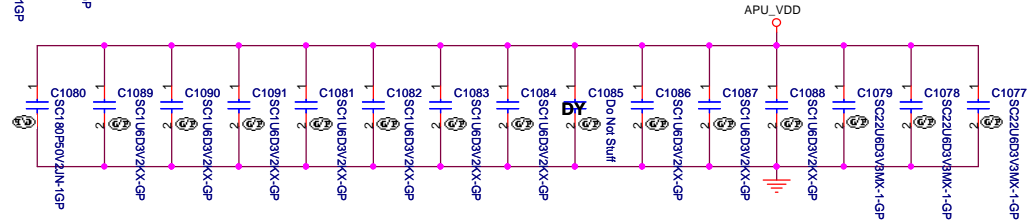
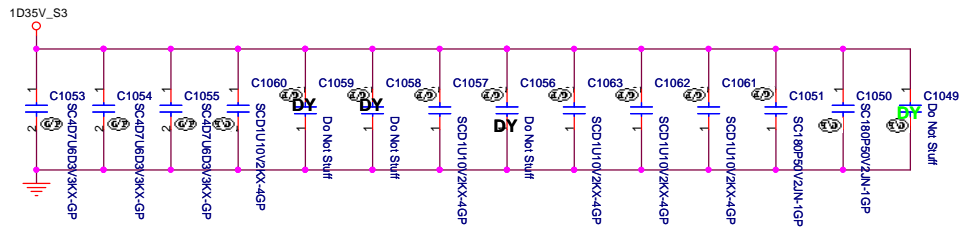
Sheet 8 of 104



Cedar UMA 14

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Title		
CPU (VSS)		
Size	Document Number	Rev
A4	Cedar AMD BEEMA	A00
Date	Wednesday, March 05, 2014	Sheet 9 of 104



Cedar UMA 14

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Title: **Reserved**

Size: A3 | Document Number: **Cedar AMD BEEMA** | Rev: **A00**

Date: Wednesday, March 05, 2014 | Sheet: 10 of 104

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Size
A4

Document Number

Cedar AMD BEEMA

Rev

A00

Date: Wednesday, March 05, 2014

Sheet 11 of 104

(Blanking)

Cedar UMA 14

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DDR3-SODIMM2

Size
A4

Document Number

Cedar AMD BEEMA

Rev

A00

Date: Wednesday, March 05, 2014

Sheet 13 of 104

5

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Cedar UMA 14

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Title

Reserved

Size
A4

Document Number

Cedar AMD BEEMA

Rev

A00

Date: Wednesday, March 05, 2014

Sheet 14 of 104

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Size A4	Document Number Cedar AMD BEEMA	Rev A00
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Date: Wednesday, March 05, 2014	Sheet 15 of	104
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Title

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Size

A4

Document Number

Cedar AMD BEEMA

Rev

A00

Date: Wednesday, March 05, 2014

Sheet 16 of 104

5

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<p>Date: Wednesday, March 05, 2014</p>	<p>Sheet 17 of 104</p>
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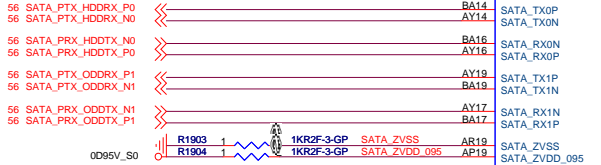
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Size A4	Document Number Cedar AMD BEEMA	Rev A00
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SATA HDD

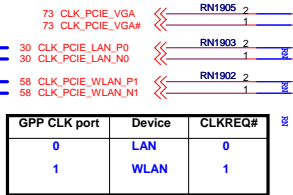
ODD



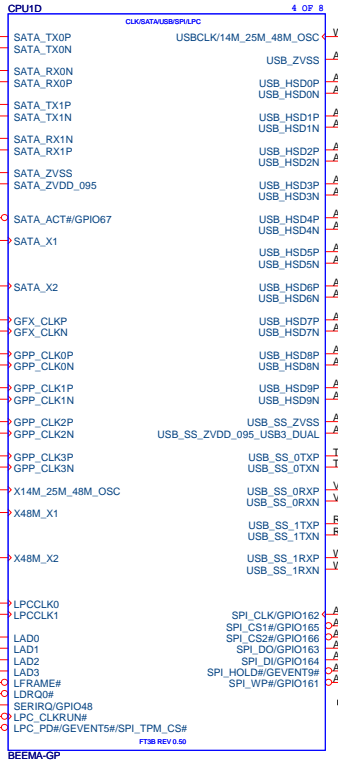
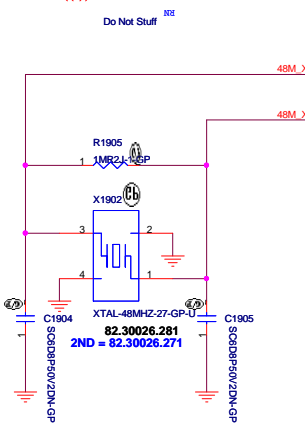
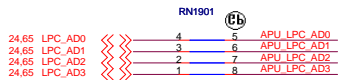
SATA	
Pair	Device
0	SATA HDD
1	ODD

LAN

WLAN



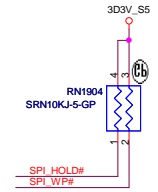
GPP CLK port	Device	CLKREQ#
0	LAN	0
1	WLAN	1



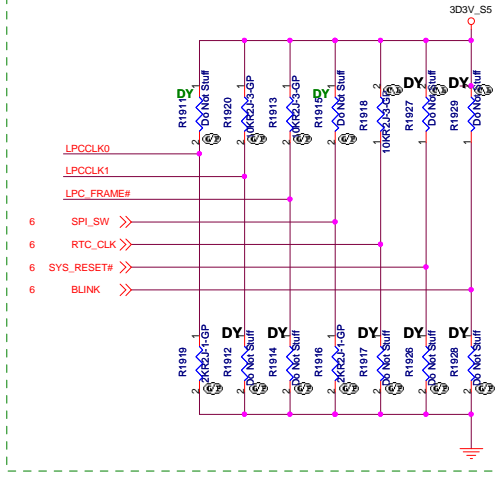
USB Table

Pair	Device
0	USB2.0 PORT1 Debug
1	USB2.0 PORT3 (DB Conn)
2	
3	NA
4	Card Reader
5	WLAN + BT (Mini PCI-E)
6	Touch Panel
7	CCD (CCD Conn)
0/8	USB3.0 & USB 2.0 (MB port2)
1/9	

XTAL	CLK, Hz
0	System & USB 48M
1	RTC 32.768K
2	LAN 25M
3	VGA 27M



SYSTEM STRAPPINGS



REQUIRED SYSTEM STRAPS

	LPC_CLK0	LPC_CLK1	LPC_FRAME#	SPI_SELECT	RTC_CLK	SYS_RESET#	BLINK
PULL HIGH	Boot Fail Timer Enabled	CLKGEN ENABLED DEFAULT	SPI ROM DEFAULT	1.8V SPI ROM DEFAULT	Coin Battery DEFAULT	NORMAL POWR UP /RESET TIMING DEFAULT	PWROK and RST_L pin routed to APU DEFAULT
PULL LOW	Boot Fail Timer Disabled DEFAULT	CLKGEN DISABLED	LPC ROM	3.3V SPI ROM	Direct DC	Reserved	Reserved

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Size

A4

Document Number

Cedar AMD BEEMA

Rev

A00

Date: Wednesday, March 05, 2014

Sheet 20 of 104

(Blanking)

Cedar UMA 14

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Reserved

Size
A4

Document Number

Cedar AMD BEEMA

Rev

A00

Date: Wednesday, March 05, 2014

Sheet 21 of 104

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A4

Document Number
Cedar AMD BEEMA

Rev
A00

Date: Wednesday, March 05, 2014

Sheet 22 of 104

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Cedar UMA 14

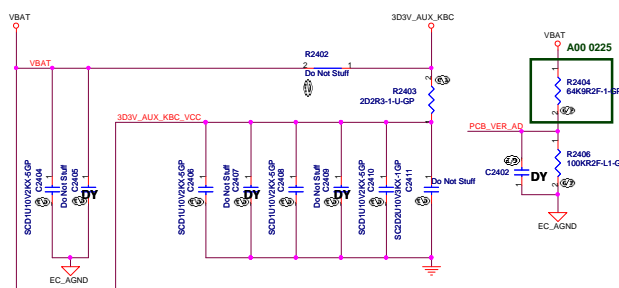
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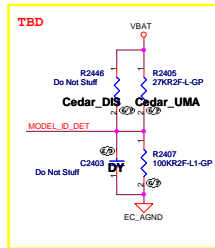
Size A4 Document Number **Cedar AMD BEEMA** Rev **A00**

Date: Wednesday, March 05, 2014 Sheet 23 of 104

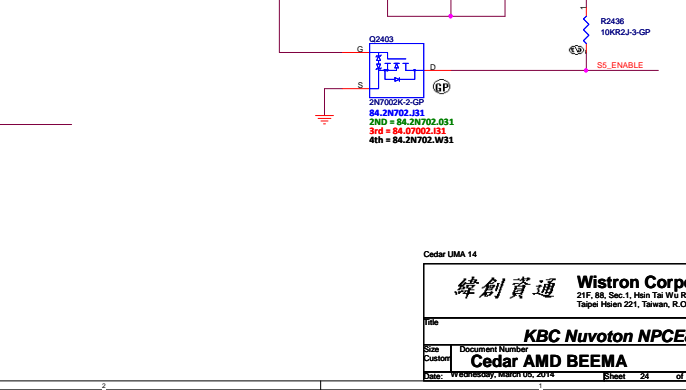
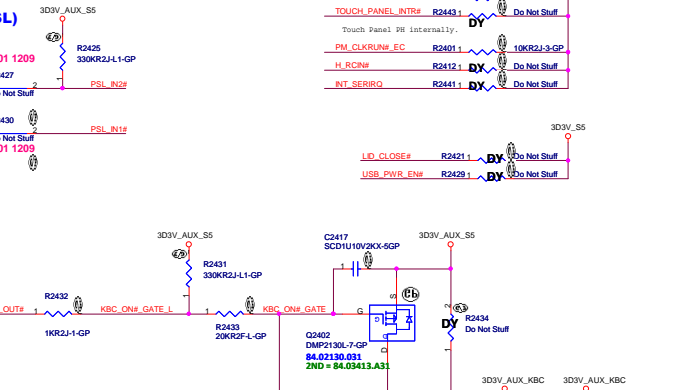
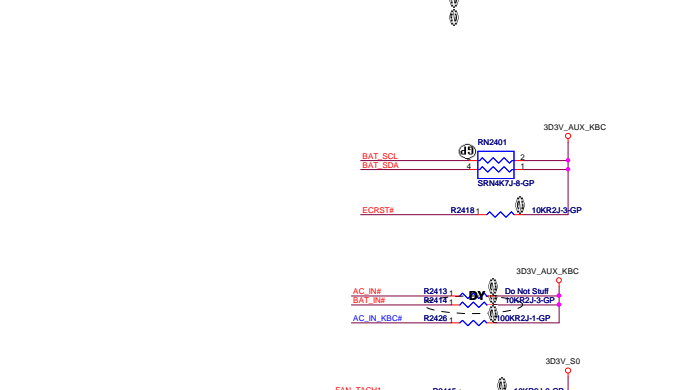
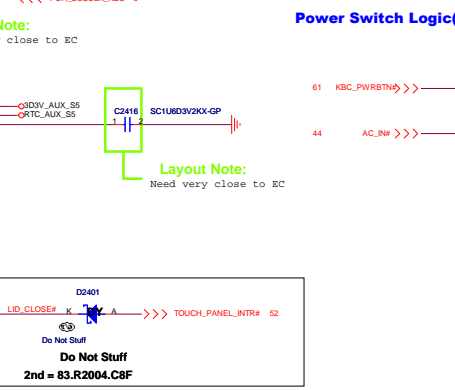
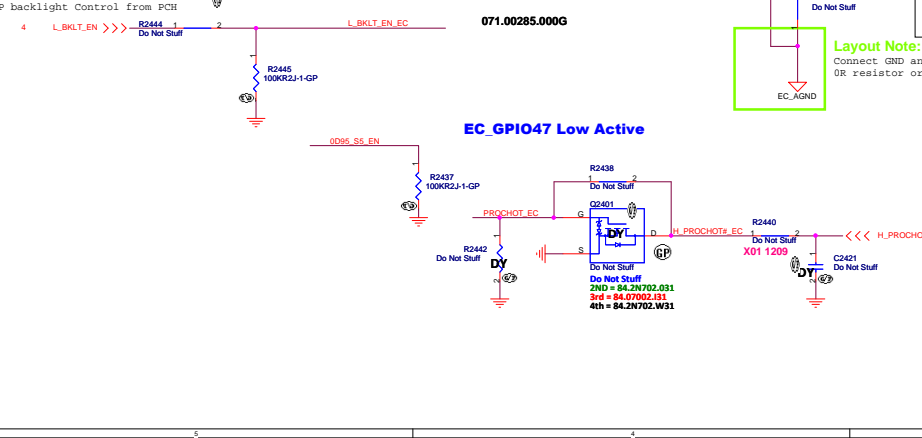
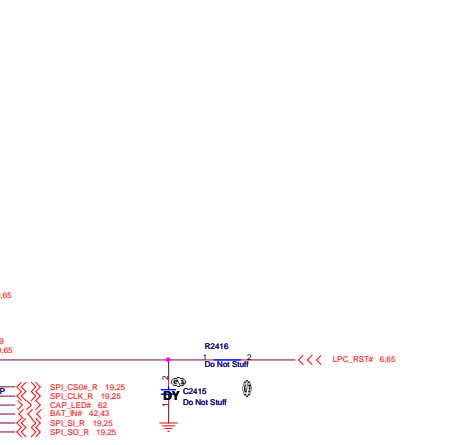
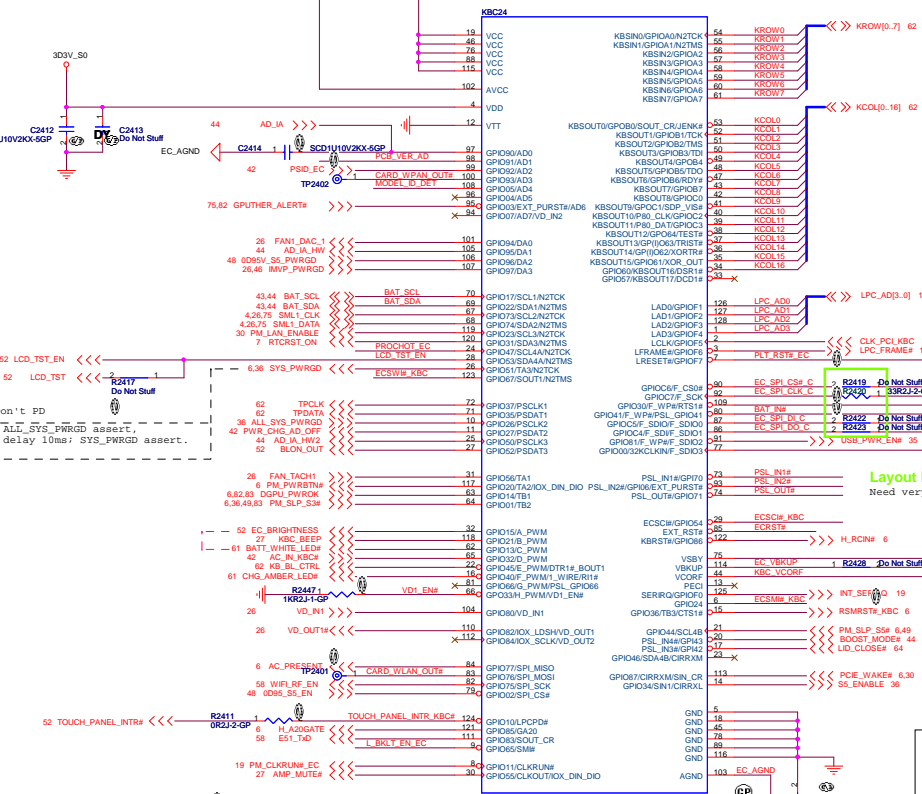
SSID = KBC



PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
X00	100.0K	10.0K	3.0V
X01	100.0K	20.0K	2.75V
X02	100.0K	33.0K	2.48V
X03	100.0K	47.0K	2.24V
A00	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

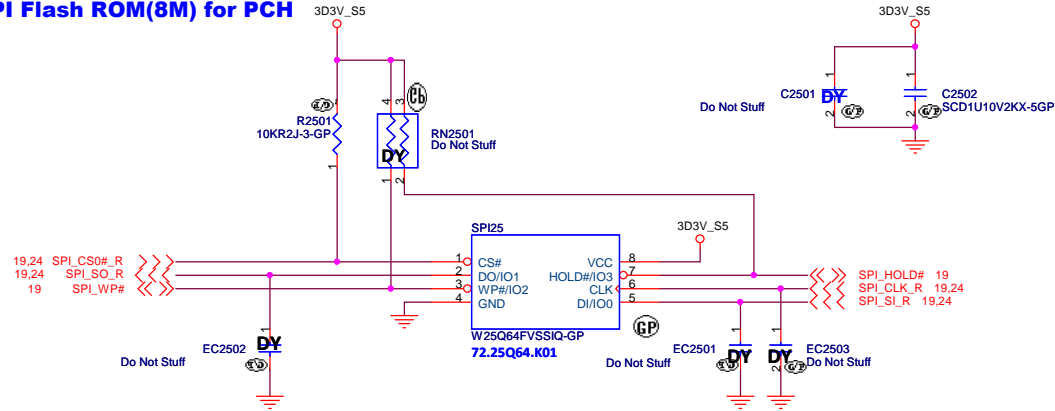


MODEL_ID_DET(GPIO07)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
James_LIMA	100.0K	10.0K(6.4.18025.GD1)	3.0V
TBD	100.0K	17.1K(6.4.1735.GD1)	2.901V
TBD	100.0K	17.8K(6.4.1725.GD1)	2.801V
TBD	100.0K	17.8K(6.4.1735.GD1)	2.702V
Cedar_LIMA	100.0K	37.0K(6.4.2705.GD1)	2.508V
TBD	100.0K	37.4K(6.4.2425.GD1)	2.402V
TBD	100.0K	37.4K(6.4.2125.GD1)	2.404V
James_DIS	100.0K	43.2K(6.4.4325.GD1)	2.301V
TBD	100.0K	49.0K(6.4.4925.GD1)	2.201V
Cedar_DIS	100.0K	57.6K(6.4.5765.GD1)	2.002V
TBD	100.0K	64.0K(6.4.6425.GD1)	1.801V
TBD	100.0K	71.2K(6.4.7125.GD1)	1.605V
TBD	100.0K	82.5K(6.4.8255.GD1)	1.400V
TBD	100.0K	93.1K(6.4.9315.GD1)	1.200V
TBD	100.0K	107.6K(6.4.10735.GD1)	1.150V
TBD	100.0K	120.0K(6.4.12035.GD1)	1.000V
TBD	100.0K	137.2K(6.4.13735.GD1)	1.002V
TBD	100.0K	154.0K(6.4.15435.GD1)	1.000V
TBD	100.0K	200.0K(6.4.20035.GD1)	1.000V
TBD	100.0K	232.0K(6.4.23235.GD1)	0.900V



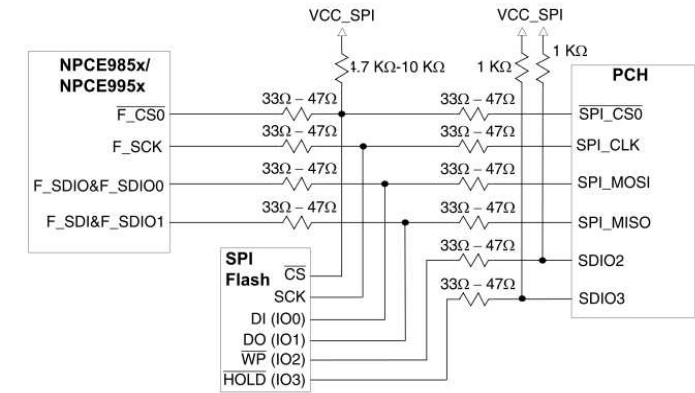
SSID = Flash.ROM

SPI Flash ROM(8M) for PCH



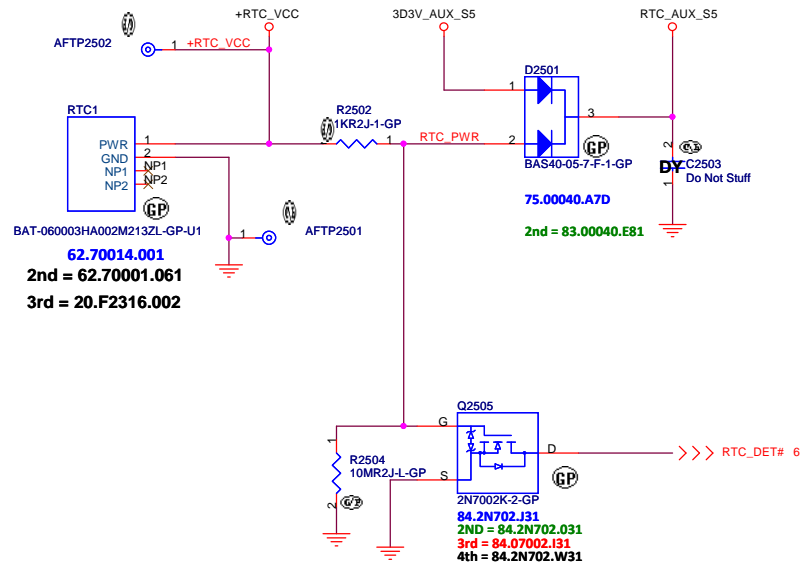
Source	QUAD/DUAL fast read	DUAL fast read
72.25Q64.K01	o	o
72.25647.00A	o	o

Single SPI shared flash connection (SPI Quad I/O mode)



Refer to "NPCE985x/ NPCE995x board design reference guide"

SSID = RBATT

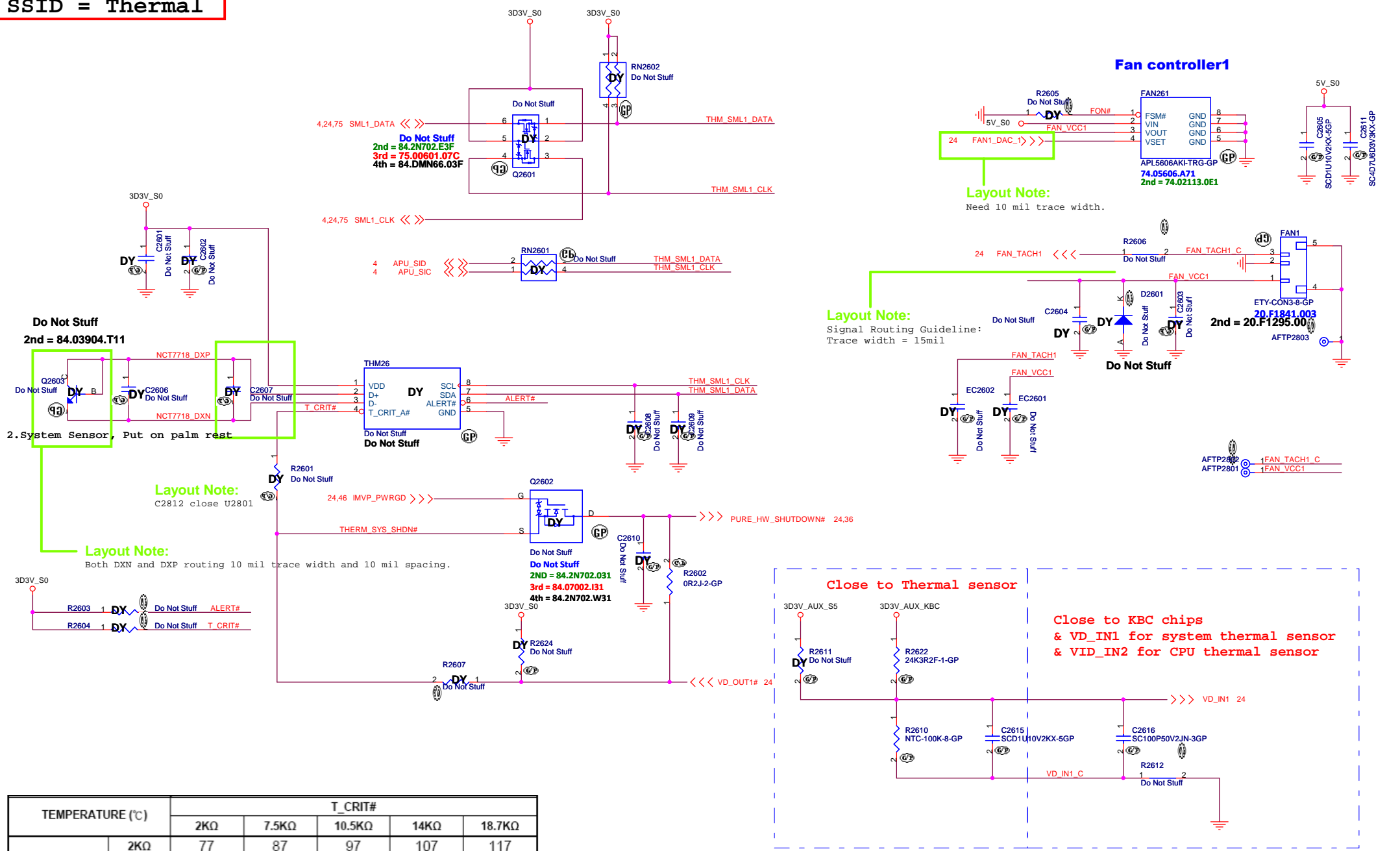


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Flash/RTC		
Title	Flash/RTC	
Size A3	Document Number	Rev
	Cedar AMD BEEMA	A00
Date: Wednesday, March 05, 2014	Sheet 25	of 104

SSID = Thermal



TEMPERATURE (°C)	T_CRIT#					
	2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ	
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

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Title: **THERMAL NCT7718W/Fan**

Size A3 Document Number: **Cedar AMD BEEMA** Rev: **A00**

Date: Wednesday, March 05, 2014 Sheet 26 of 104

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Title

Reserved

Size
A4

Document Number

Cedar AMD BEEMA

Rev
A00

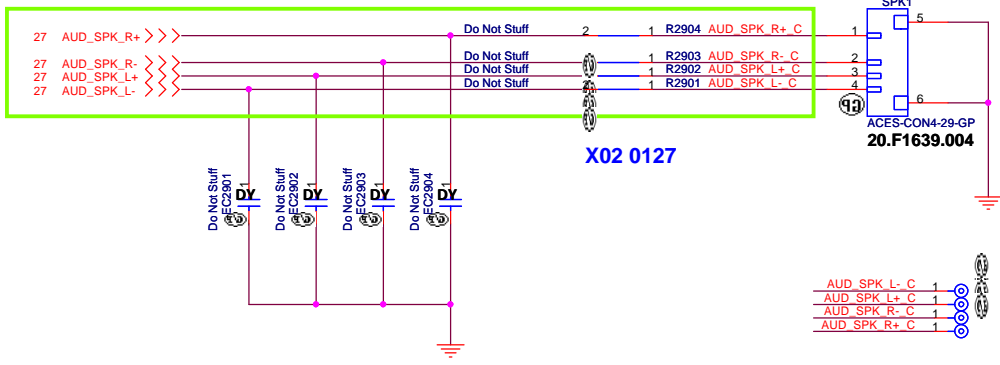
Date: Wednesday, March 05, 2014

Sheet 28 of 104

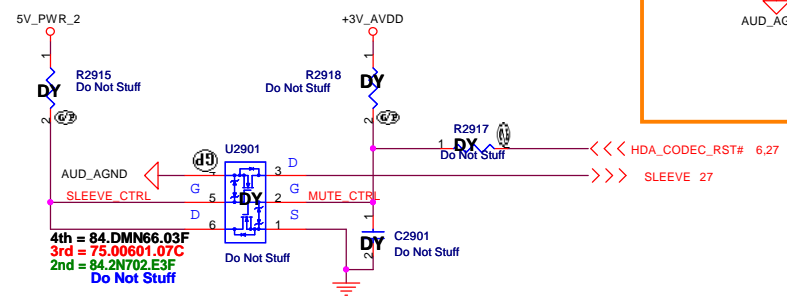
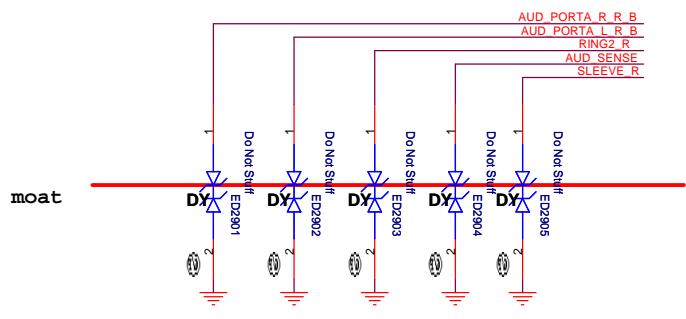
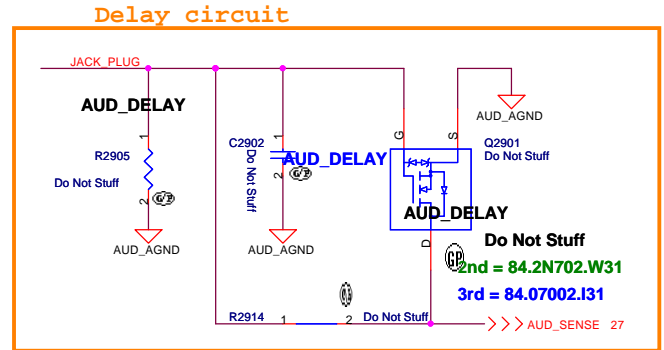
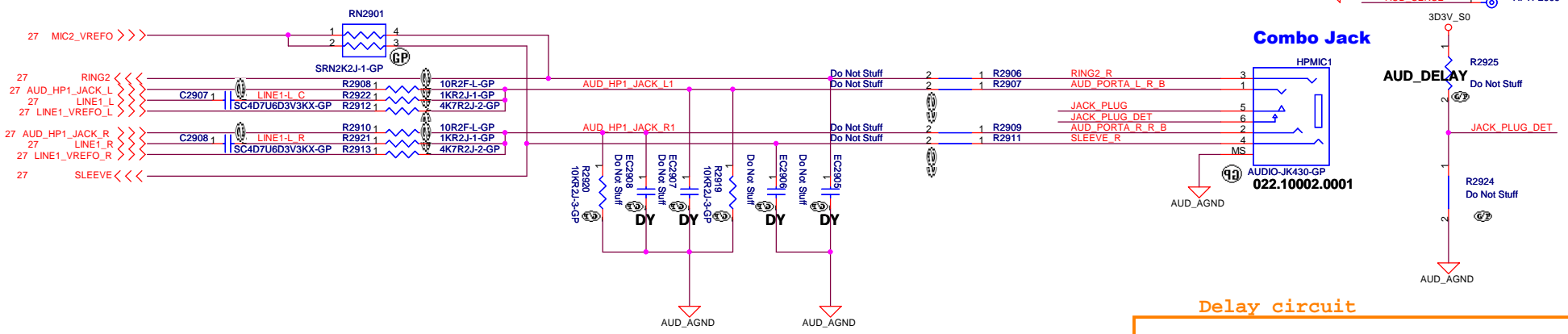
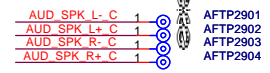
SSID = AUDIO

Layout Note:

Speaker trace width >40mil @ 2W4ohm speaker power



CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-



Cedar UMA 14

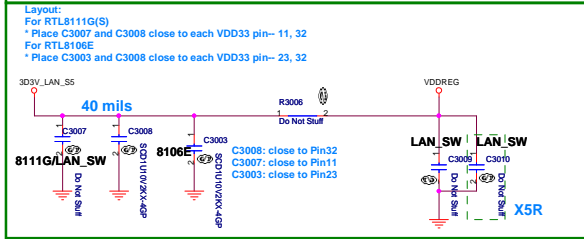
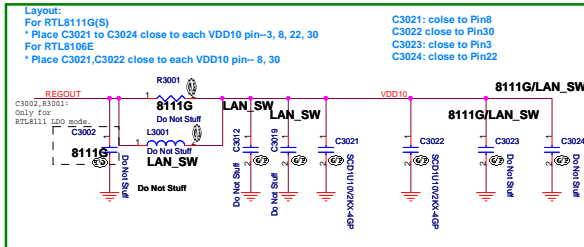
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Thermal NCT7718W/Fan Controller P2793**

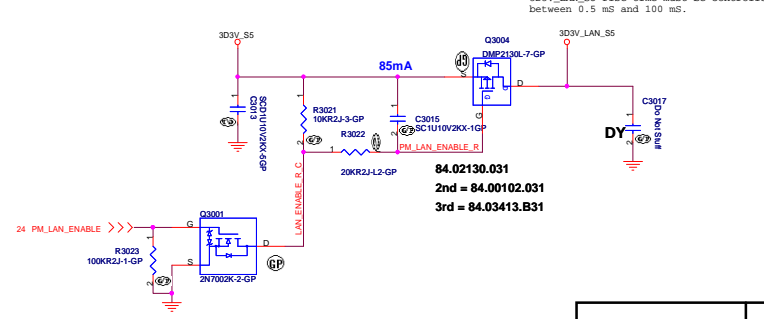
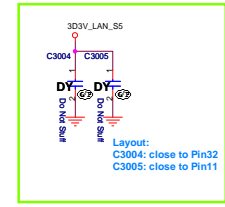
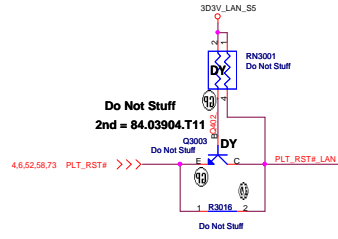
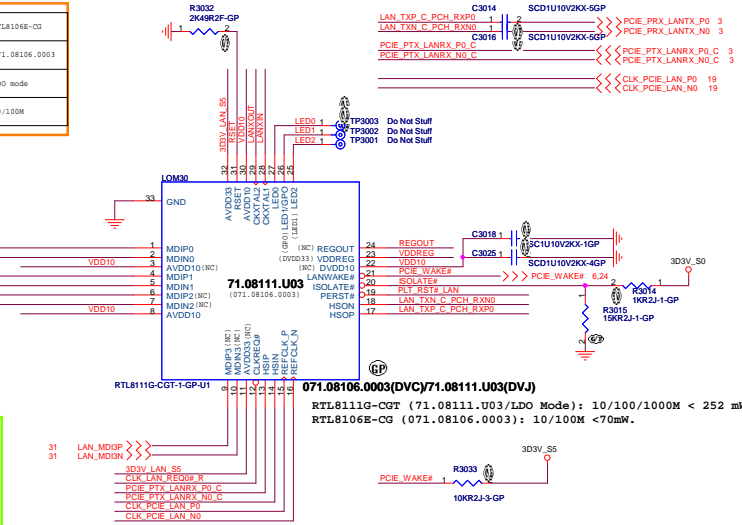
Size A3 Document Number Rev A00

Date: Wednesday, March 05, 2014 Sheet 29 of 104

LAN CHIP (10/100/1000M & 10/100M co-lay)



RTL811100B-CG	RTL81110-CGT	RTL8106EUS-CG	RTL8106E-CG
71.08111.W03	71.08111.003	71.08106.003	071.08106.0003
SWR mode	LDO mode	SWR mode	LDO mode
10/100/1000M	10/100/1000M	10/100M	10/100M

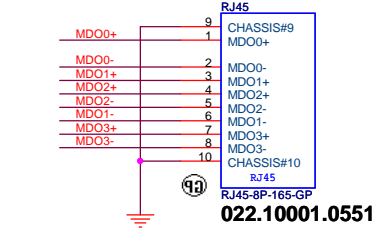
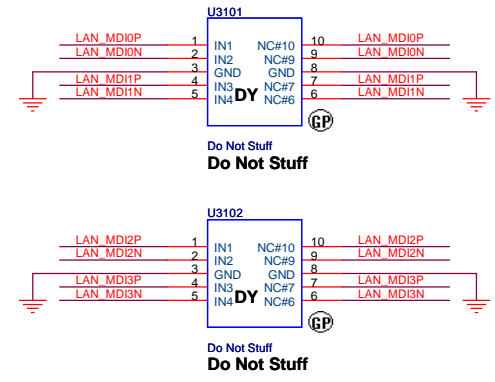
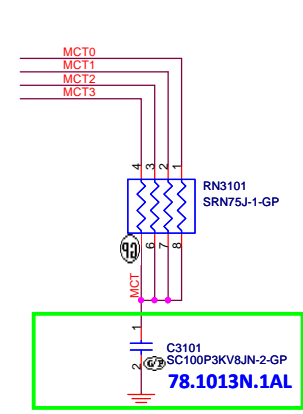
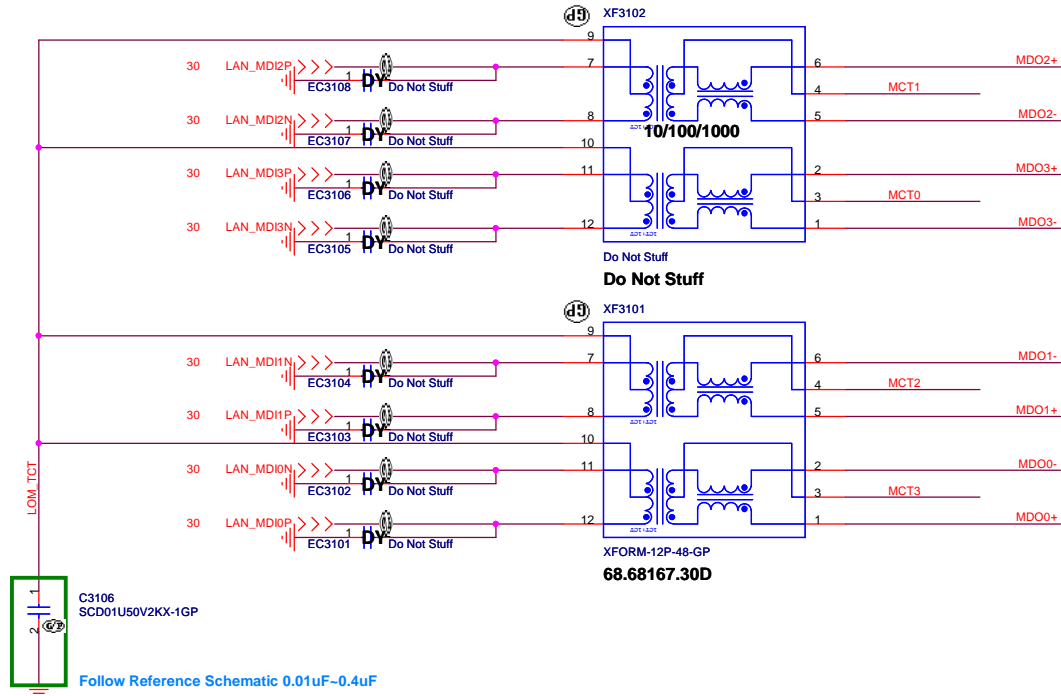


	1.0V Source	R3001	C3002	C3023	C3024	C3007	L3001	C3012	C3019	C3009	C3010	C3003
RTL8111G-CGT (71.08111.U03)	LDO	O	O	O	O	O	X	X	X	X	X	X
RTL8111GUS-CG (71.08111.W03) / RTL8106EUS-CG (71.08106.003)	SWR	X	X	O	O	O	O	O	O	O	O	X
RTL8106E-CG (071.08106.0003)	LDO	X	X	X	X	X	X	X	X	X	X	O

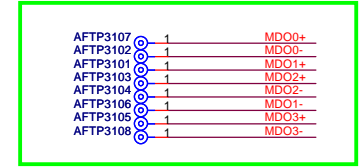
SSID = LOM

LAN Transformer (10/100/1000M & 10/100M co-lay)

Layout note:
30 mil spacing between MDI differential pairs.



Layout:
Place near RJ45



5

4

3

2

1

D

D

C

C

B

B

A

A

(Blanking)

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(Reserved)Card Reader		
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Size A4	Document Number Cedar AMD BEEMA	Rev A00
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Date: Wednesday, March 05, 2014	Sheet 32 of 104
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Document Number

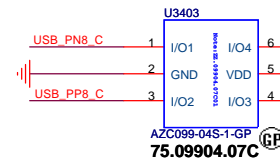
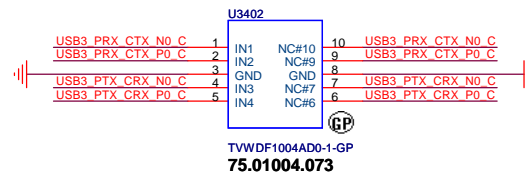
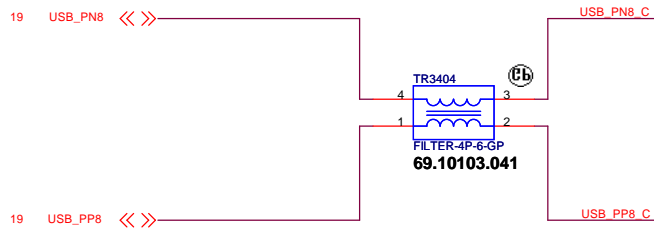
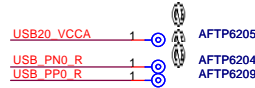
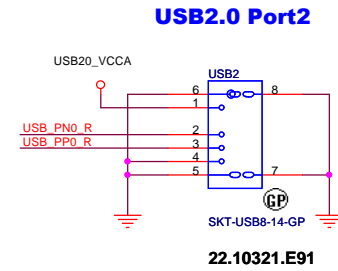
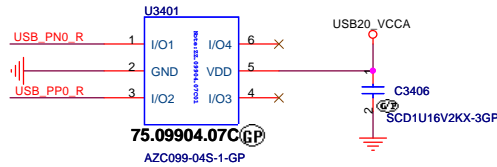
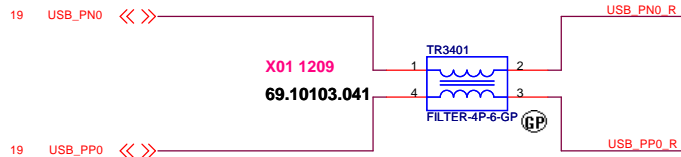
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Rev
A00

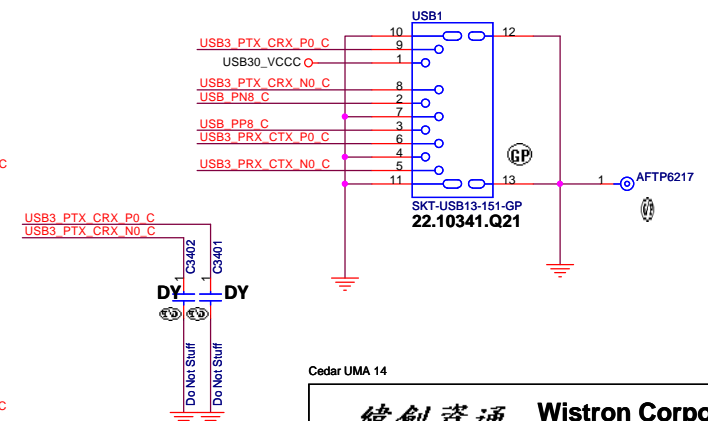
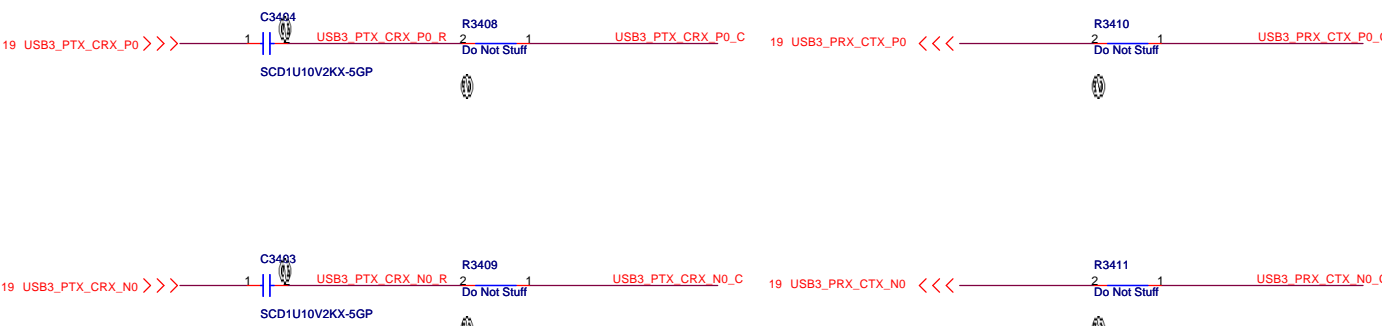
Date: Wednesday, March 05, 2014

Sheet 33 of 104

SSID = USB

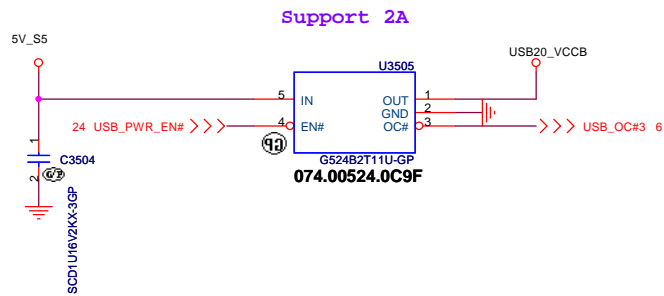
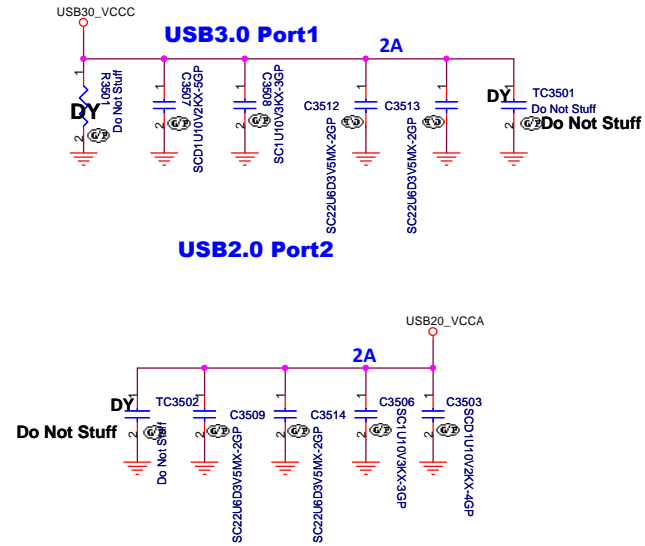
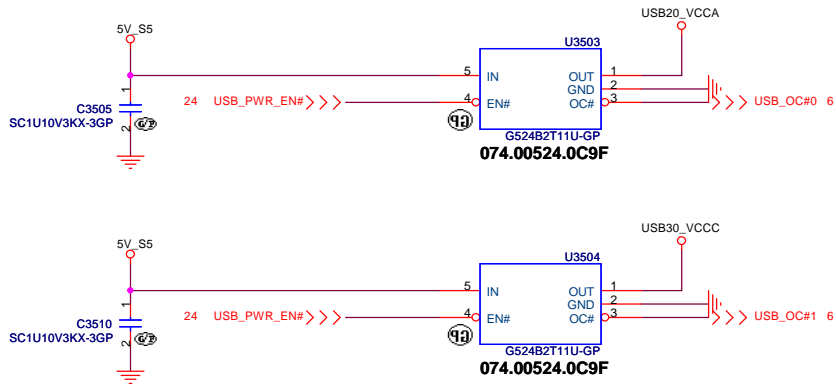


USB3.0 Port1

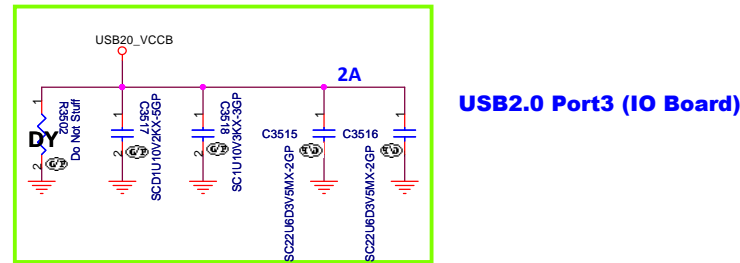


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USB 3.0			
Title			
Size A3	Document Number	Rev	
	Cedar AMD BEEMA	A00	
Date: Wednesday, March 05, 2014	Sheet 34	of 104	

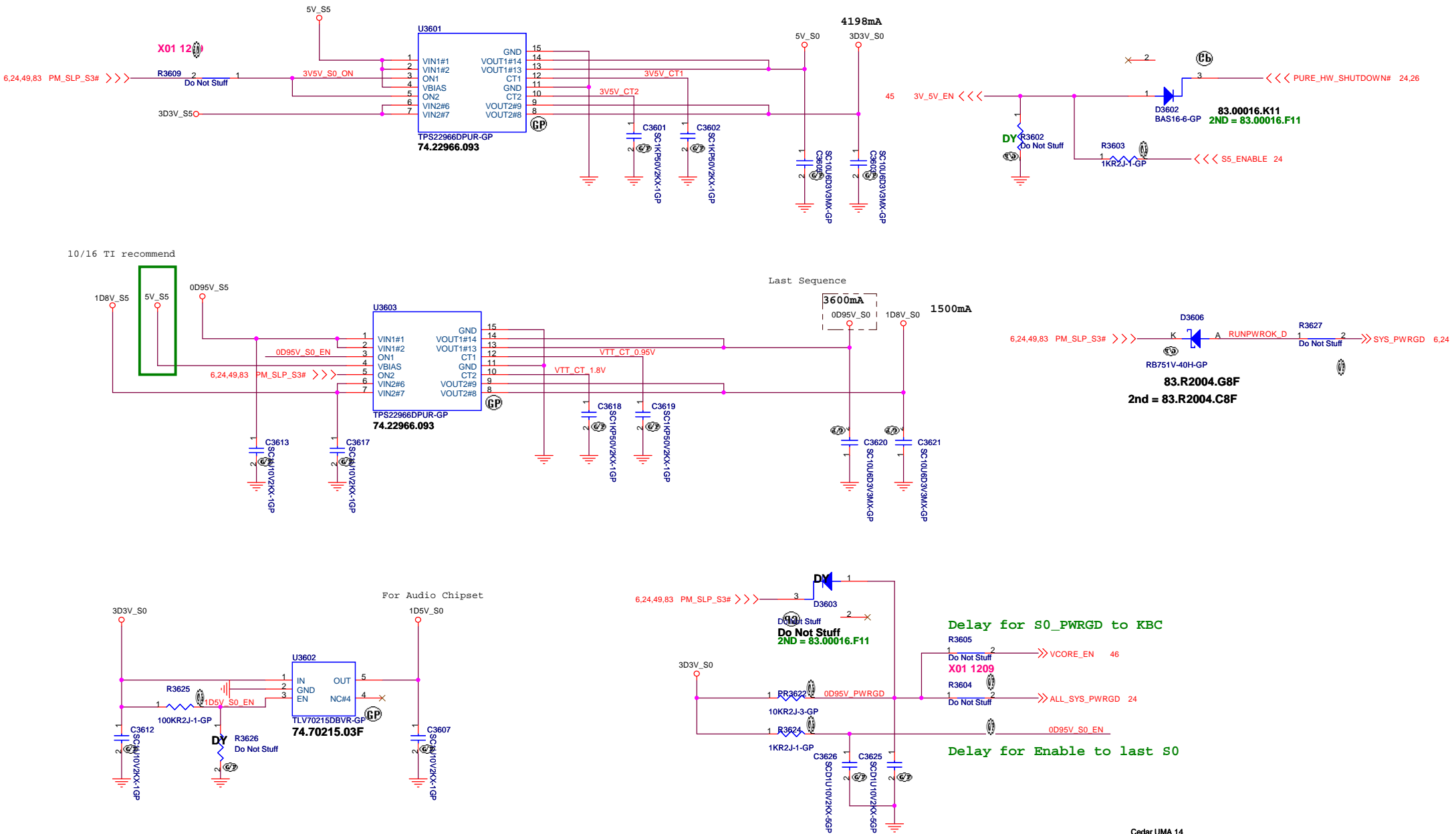


Layout Note: Close CON1



Cedar UMA 14

Power Sequence



Cedar UMA 14

SSID = Reset.Suspend

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Size
A3

Document Number

Cedar AMD BEEMA

Rev

A00

Date: Wednesday, March 05, 2014

Sheet 37 of 104

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Size A4	Document Number Cedar AMD BEEMA	Rev A00
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Date: Wednesday, March 05, 2014 Sheet 38 of 104

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Title
(Reserved) 1D05_M

Size A4	Document Number Cedar AMD BEEMA	Rev A00
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Date: Wednesday, March 05, 2014 Sheet 39 of 104

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Document Number

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Rev
A00

Date: Wednesday, March 05, 2014

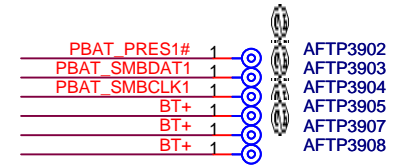
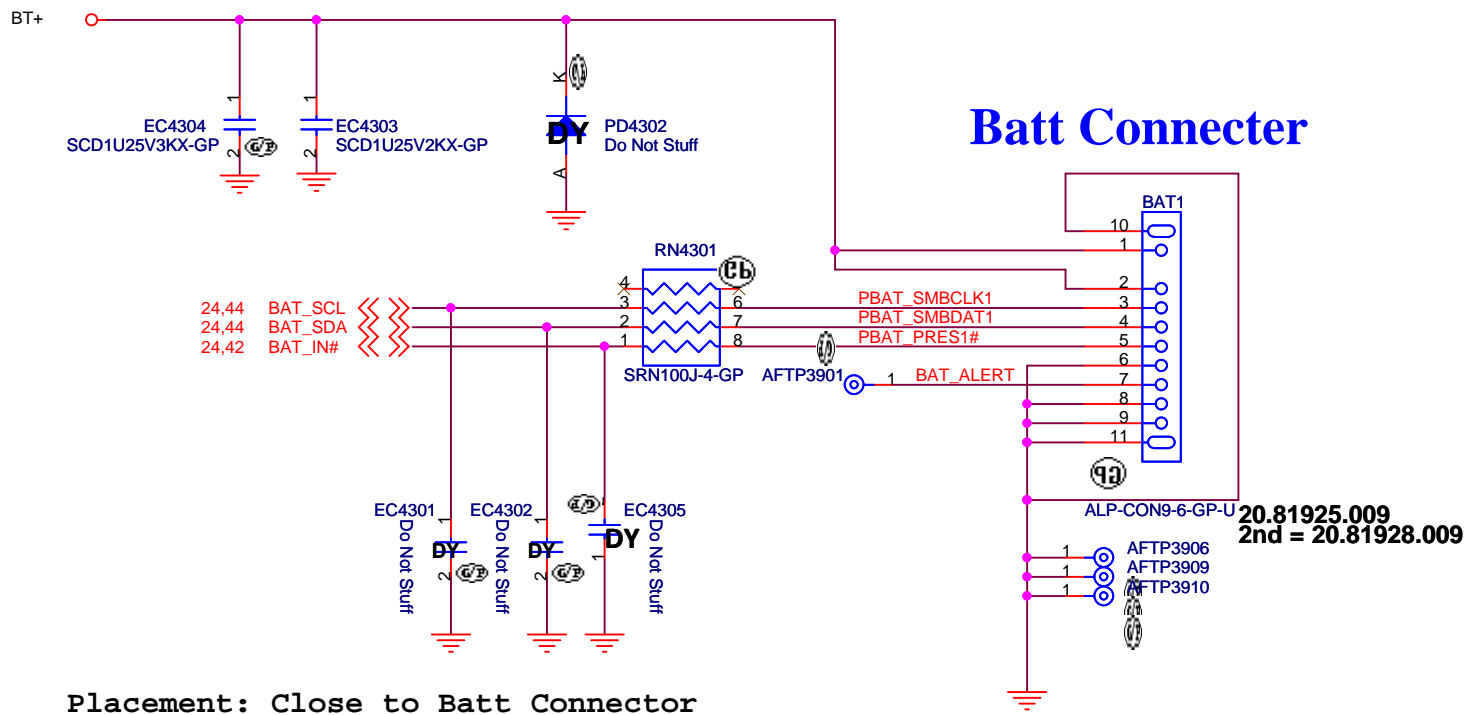
Sheet 40 of 104

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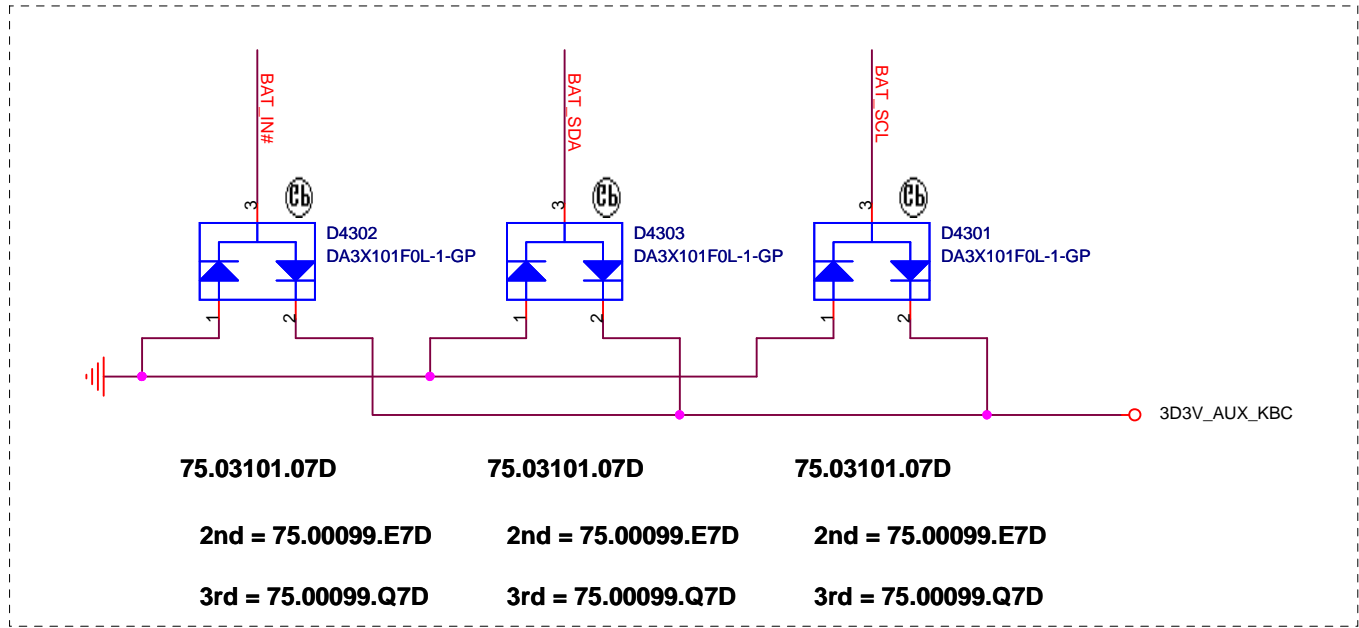
Cedar UMA 14

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Title			
Reserved			
Size A4	Document Number Cedar AMD BEEMA		Rev A00
Date: Wednesday, March 05, 2014		Sheet 41	of 104

SSID = PWR.Support




Placement: Close to Batt Connector

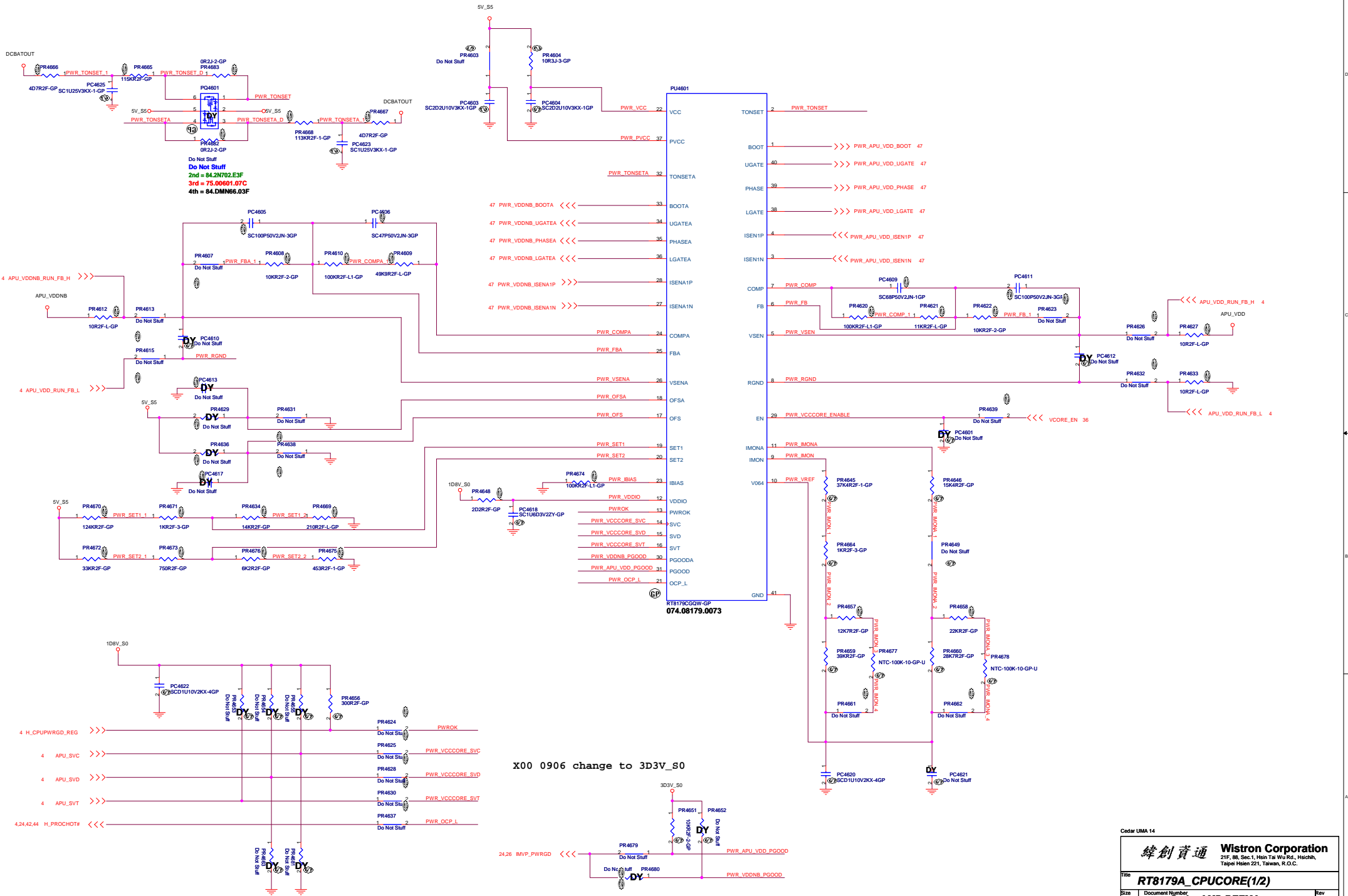


75.03101.07D	75.03101.07D	75.03101.07D
2nd = 75.00099.E7D	2nd = 75.00099.E7D	2nd = 75.00099.E7D
3rd = 75.00099.Q7D	3rd = 75.00099.Q7D	3rd = 75.00099.Q7D

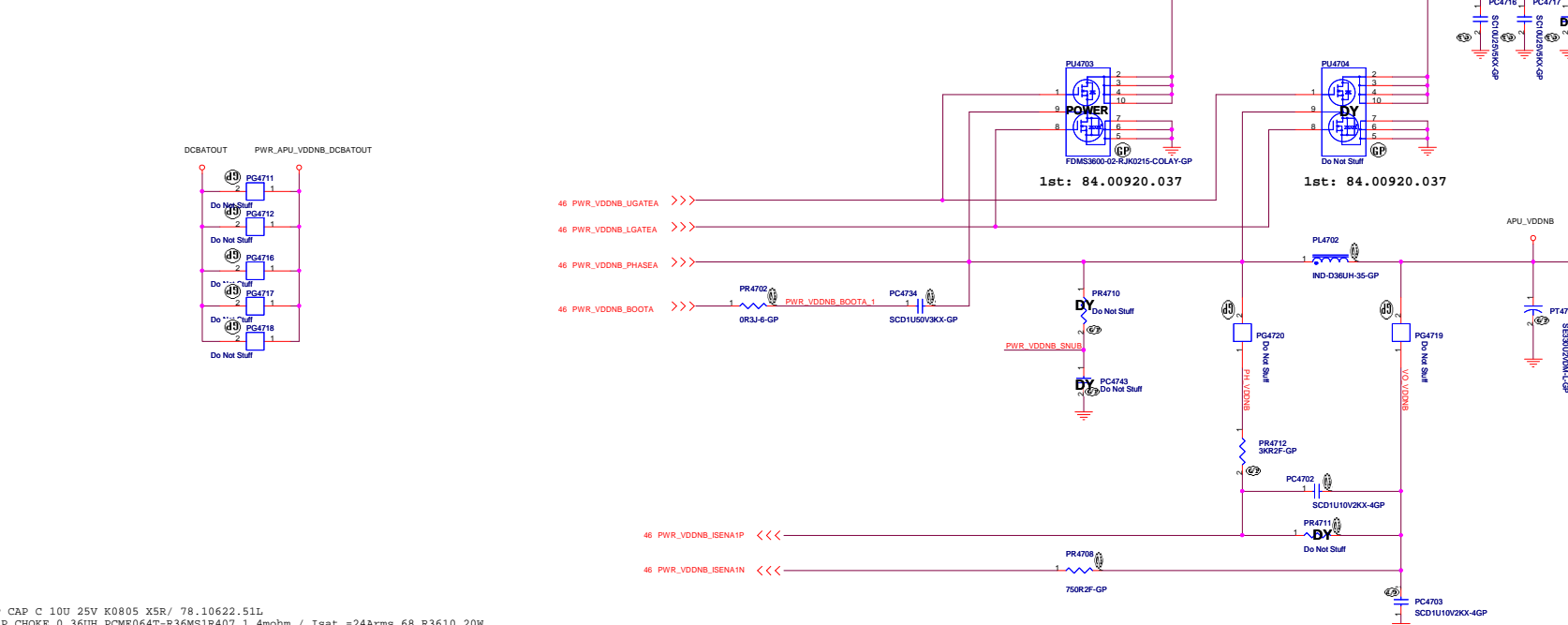
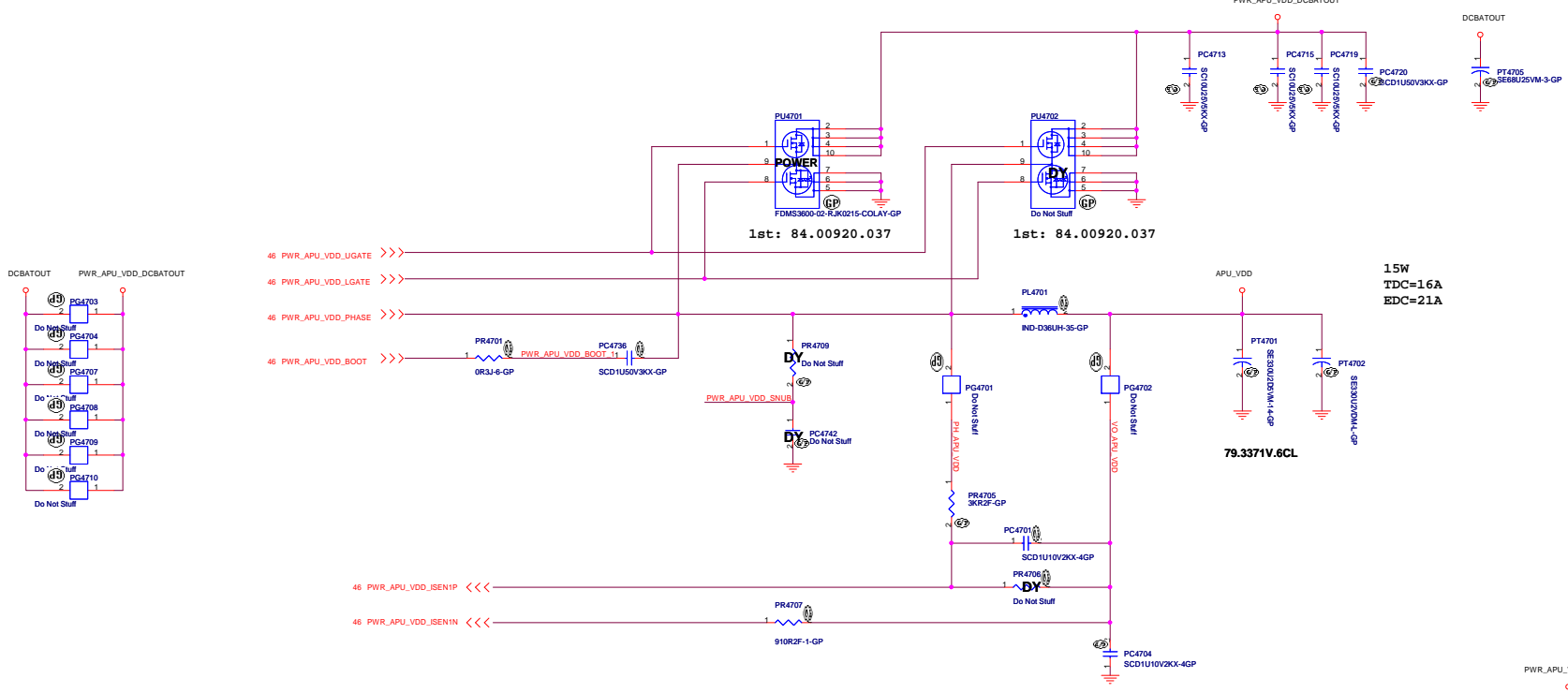
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Title BATT CONN	
Size A4	Document Number Cedar AMD BEEMA
Rev A00	
Date: Wednesday, March 05, 2014	
Sheet 43	of 104

SSID = CPU.Regulator

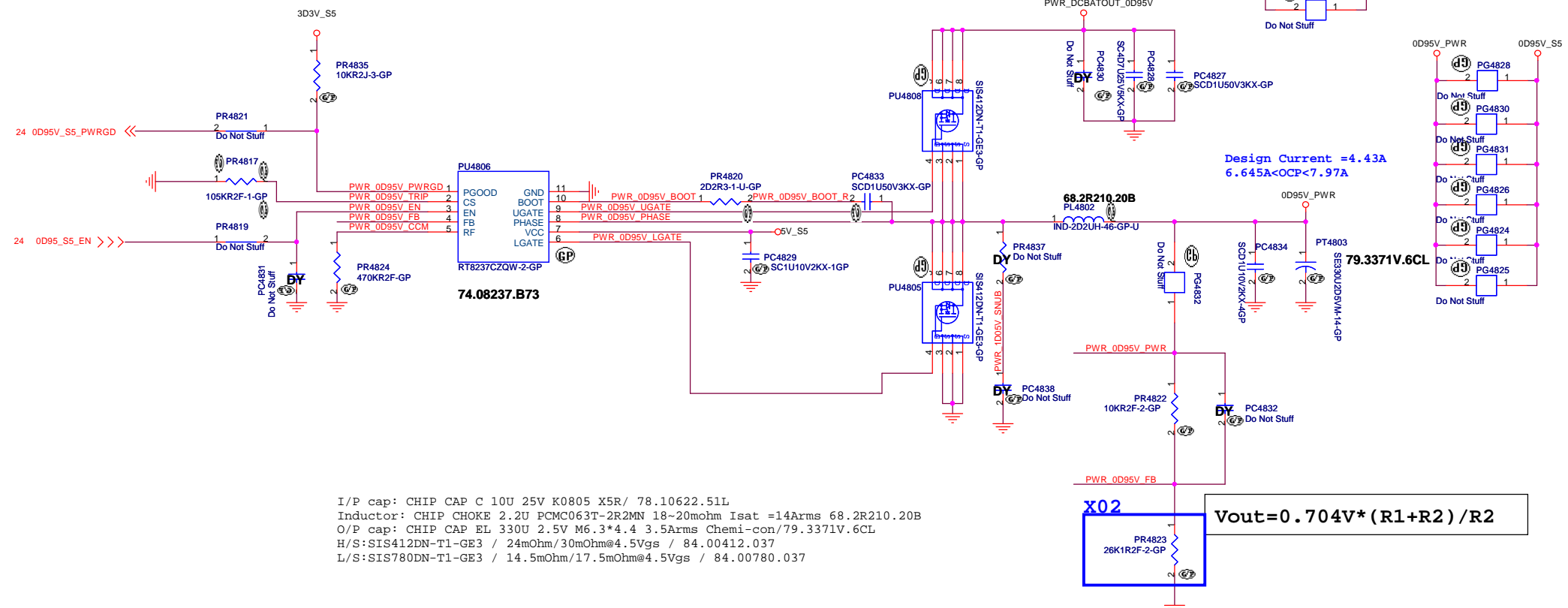


X00 0906 change to 3D3V_S0

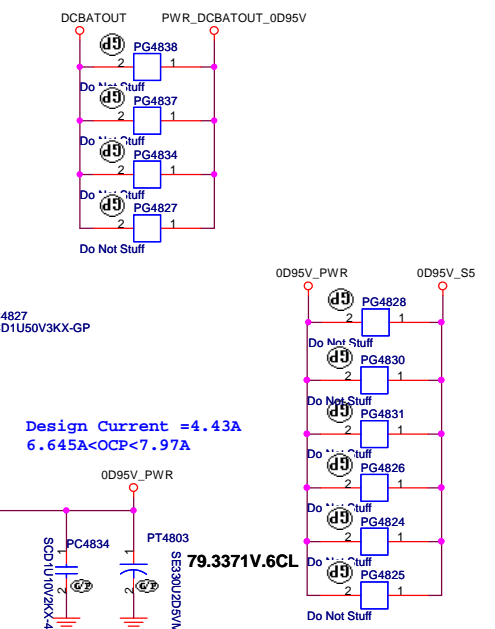


I/P cap: CHIP CAP C 10U 25V K0805 XSR/ 78.10622.51L
 Inductor: CHIP CHOKR 0.36UH PCMR064T-R36MS1R407 1.4mohm / Isat =24Arms 68.R3610.20W
 O/P cap:CHIP CAP 470UF 2V EFPSX0D471X /Panasonic/ 6mOhm / 79.47719.2BL
 Dual N FET MOS SI2920DT-T1-GE3 DUAL NC POWER 8P /H/S 7.4mohm/8.9mohm / L/S 2.9mOhm/3.5mohm@4.5Vgs / 84.00920.037

SSID = PWR.Plane.Regulator_1p05v

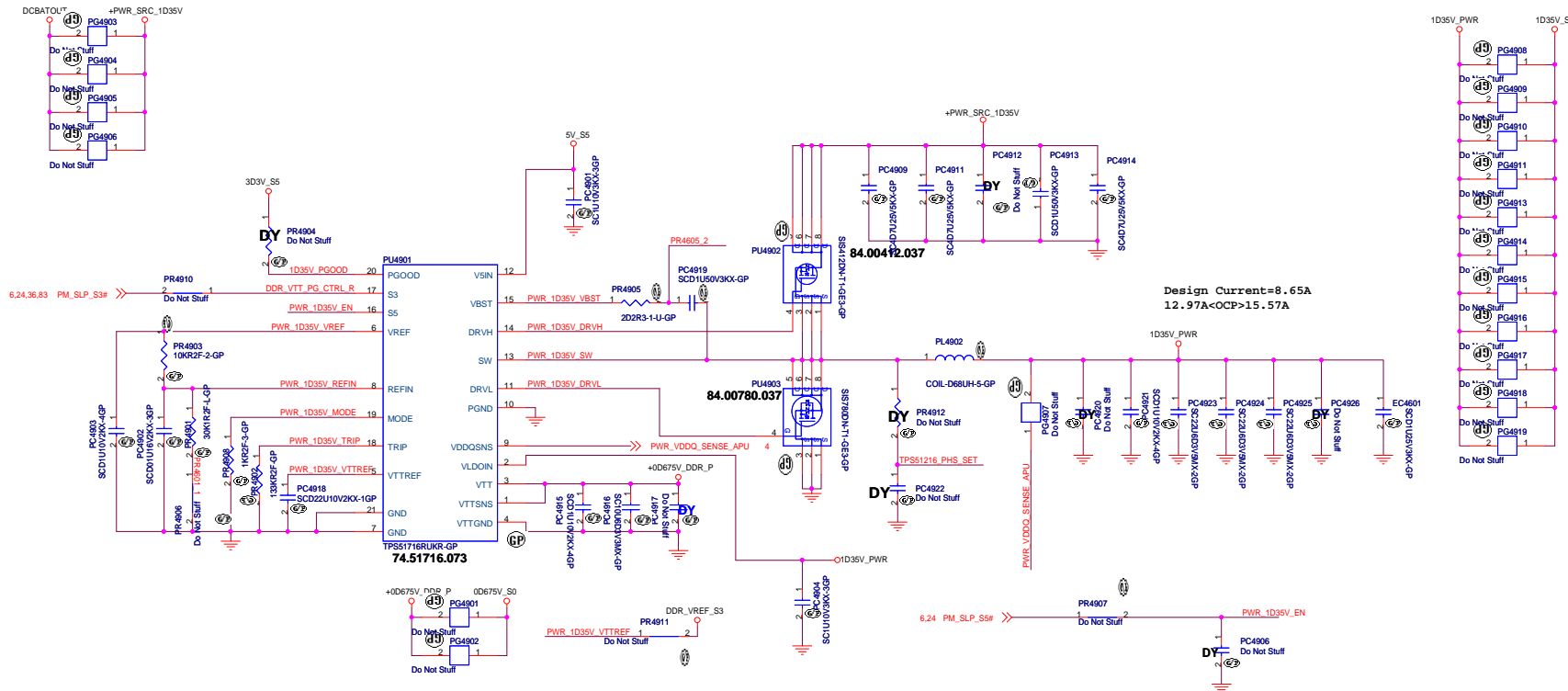


I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
 Inductor: CHIP CHOKE 2.2U PCMC063T-2R2MN 18~20mohm Isat =14Arms 68.2R210.20B
 O/P cap: CHIP CAP EL 330U 2.5V M6.3*4.4 3.5Arms Chemi-con/79.3371V.6CL
 H/S:SIS412DN-T1-GE3 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
 L/S:SIS780DN-T1-GE3 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037



$$V_{out} = 0.704V * (R1 + R2) / R2$$

SSID = PWR.Plane.Regulator 1p35v0p675v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

I/P cap: 10U 25V K0805 X5R / 78.10622.51L
 Inductor: CHIP IND 0.1UH M PCMC063T-R10MN 1.5-1.7mohm Isat =60Arms 68.R1010.10T
 O/P cap: CHIP CAP C 22U 6.3V M0805 X5R / 78.22610.51L
 H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
 L/S:SIS780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

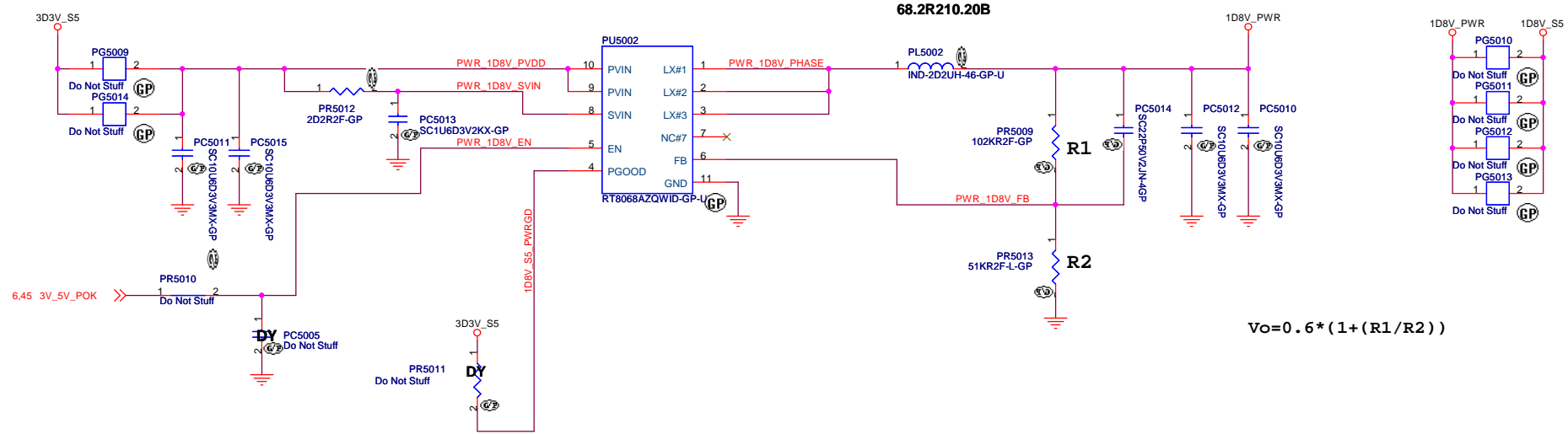
TPS51716 MODE

PR4608	Frequency	Discharge Mode
33k ohm	500kHz	Non-tracking Discharge
22k ohm	670kHz	
12k ohm	670kHz	Tracking Discharge
1k ohm	500kHz	

SSID = PWR.Plane.Regulator_1p8v

RT8068A for 1D8V_S5

Design Current=1.62A



$$V_o = 0.6 * (1 + (R1 / R2))$$

SSID = PWR.Plane.Regulator_1p5v

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Title			
TLV70215_1D5			
Size	Document Number	Rev	
A3	Cedar AMD BEEMA	A00	
Date: Wednesday, March 05, 2014		Sheet	51 of 104

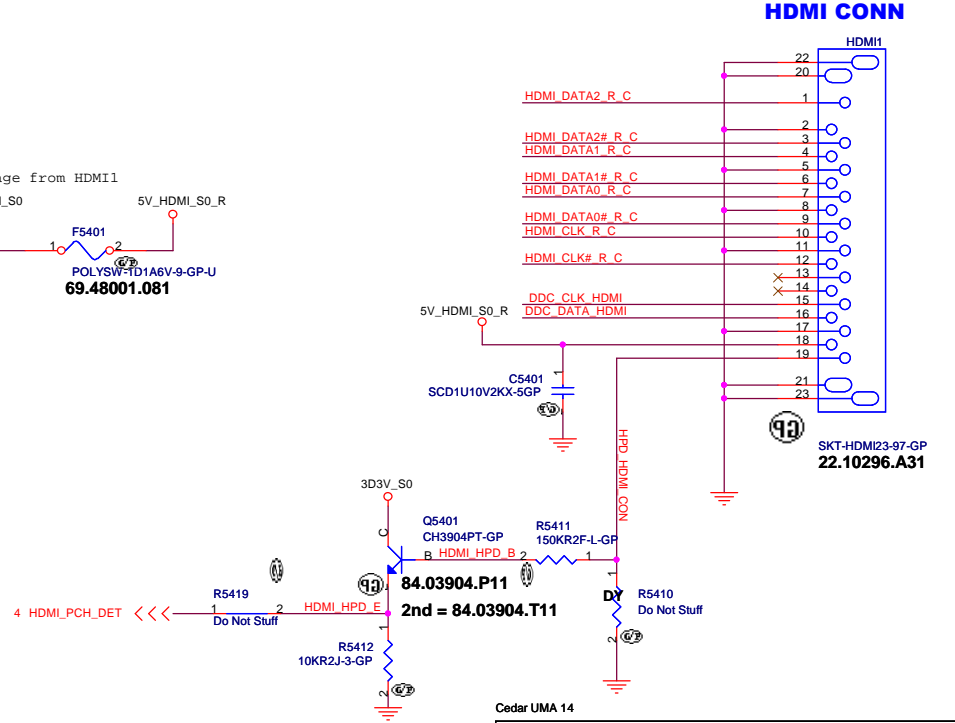
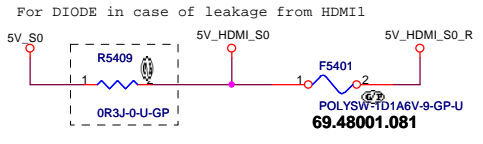
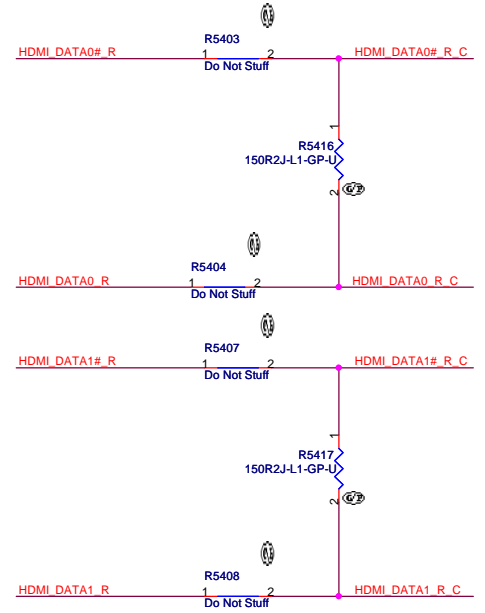
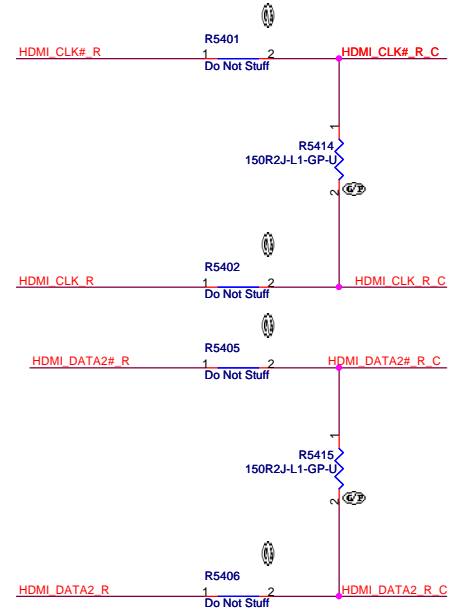
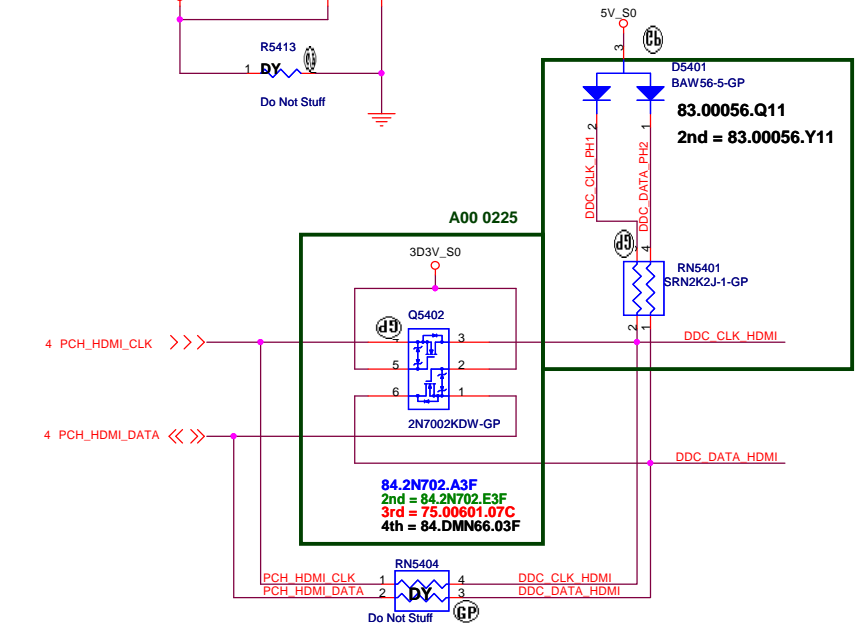
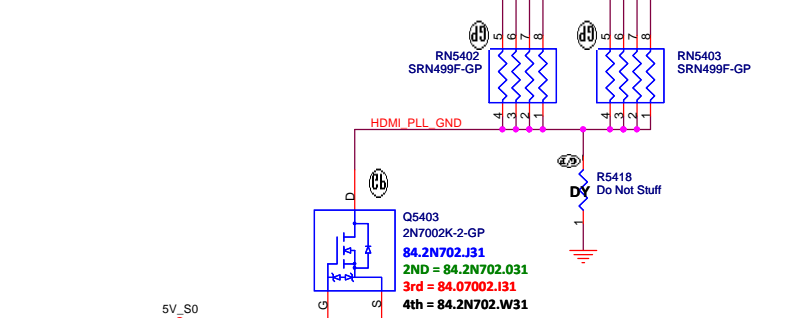
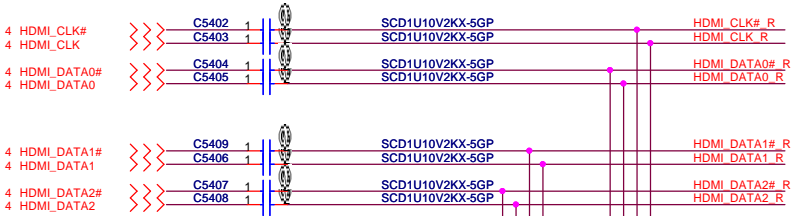
(Blanking)

Cedar UMA 14

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Title		
(Reserved)		
Size	Document Number	Rev
A3	Cedar AMD BEEMA	A00
Date: Wednesday, March 05, 2014		Sheet 53 of 104

SSID = VIDEO



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Taipei Hsien 221, Taiwan, R.O.C.

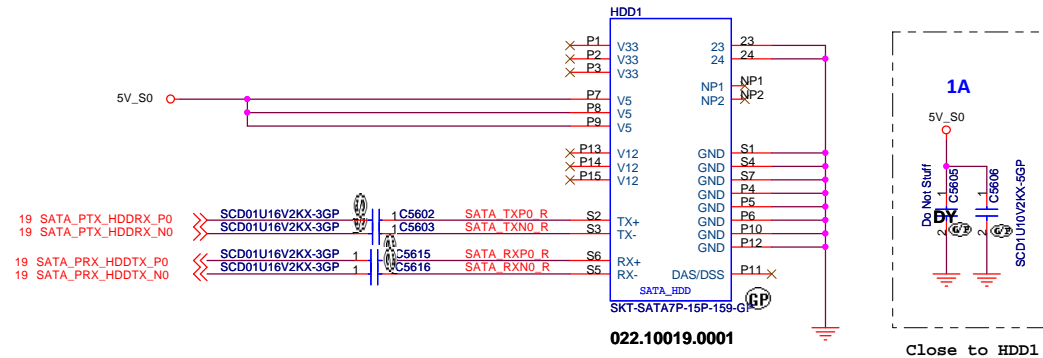
Title: HDMI Level Shifter/Connector
Size A3 Document Number: Cedar AMD BEEMA Rev A00
Date: Wednesday, March 05, 2014 Sheet 54 of 104

(Blanking)

Cedar UMA 14

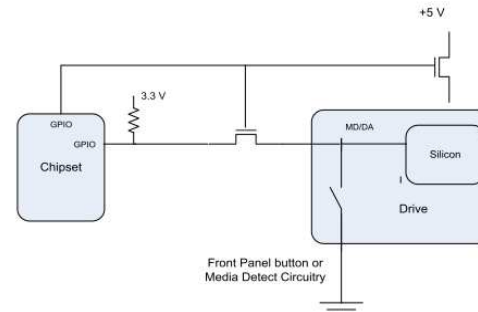
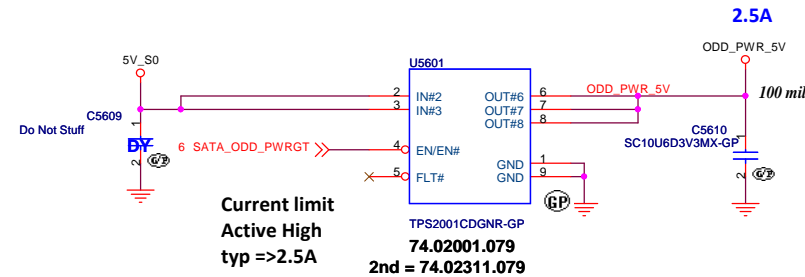
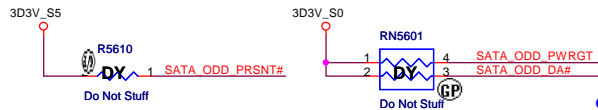
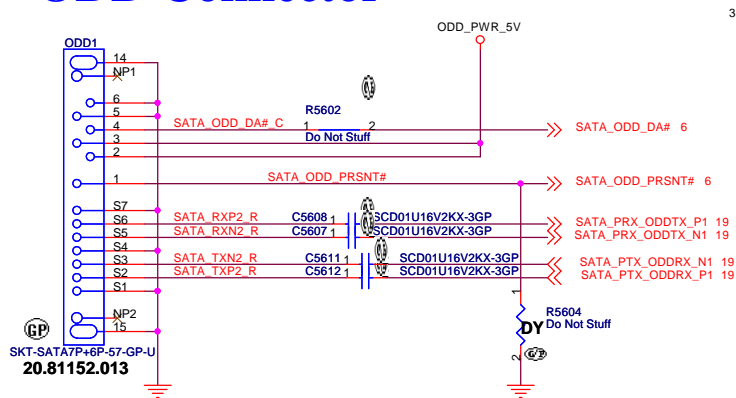
緯創資通			Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
VGA Con.(Reserve)					
Size	Document Number				Rev
A3	Cedar AMD BEEMA				A00
Date: Wednesday, March 05, 2014		Sheet 55		of 104	

SATA HDD Connector



ME Note: New HDD conn symbol is not ready, we will use original OAK HDD conn (22.10300.991) and shift to the correct position.

ODD Connector



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SSID = ESATA

(Blanking)

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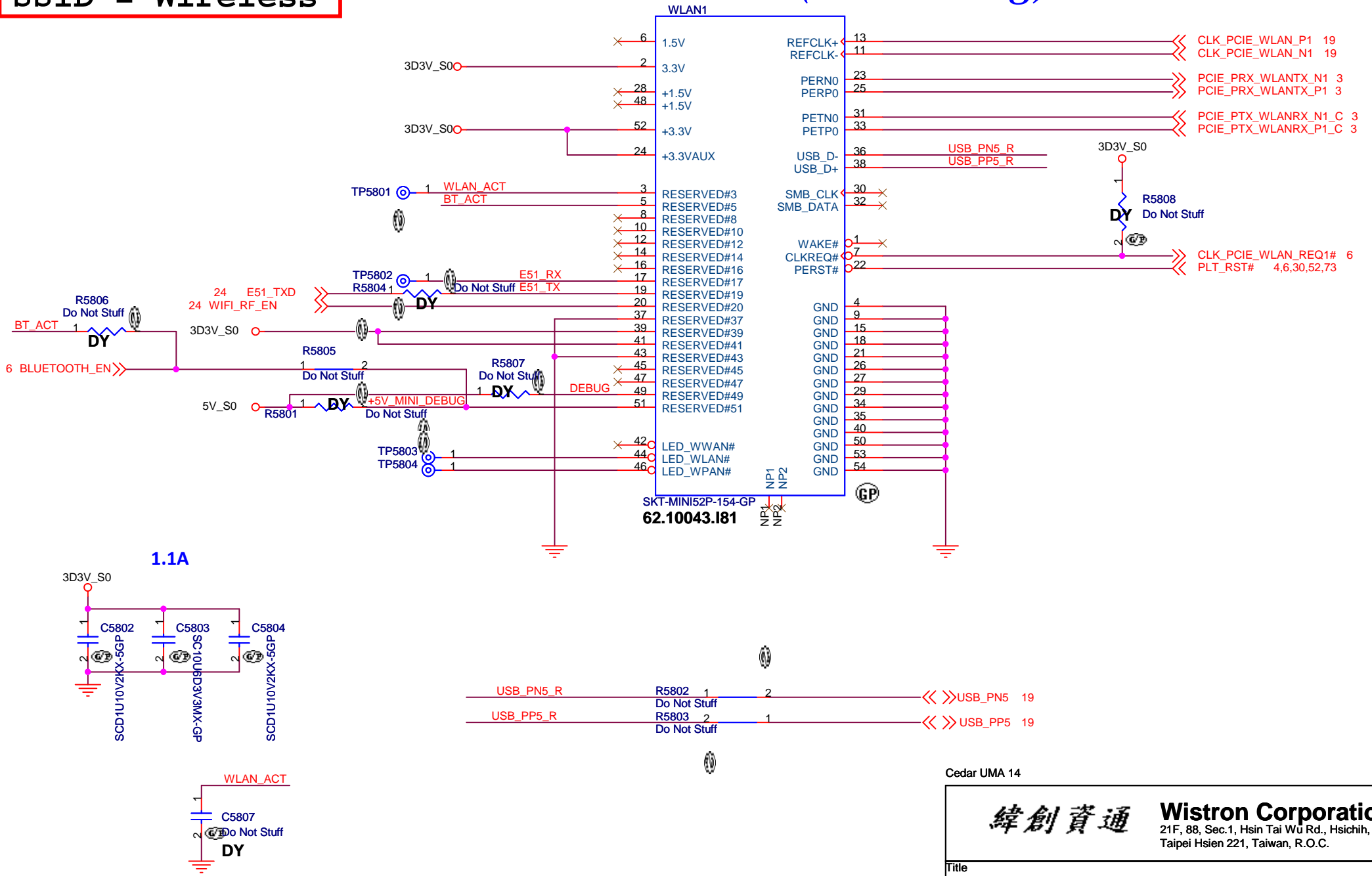
Title **ESATA**

Size A3 Document Number **Cedar AMD BEEMA** Rev **A00**

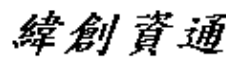
Date: Wednesday, March 05, 2014 Sheet 57 of 104

SSID = Wireless

Mini Card Connector(802.11a/b/g)



Cedar UMA 14

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Title WLAN CONN	
Size A4	Document Number Cedar AMD BEEMA
Rev A00	
Date: Wednesday, March 05, 2014	
Sheet 58	of 104

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Cedar UMA 14

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Title

Reserved

Size
A4

Document Number

Cedar AMD BEEMA

Rev
A00

Date: Wednesday, March 05, 2014

Sheet 59 of 104

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Cedar UMA 14

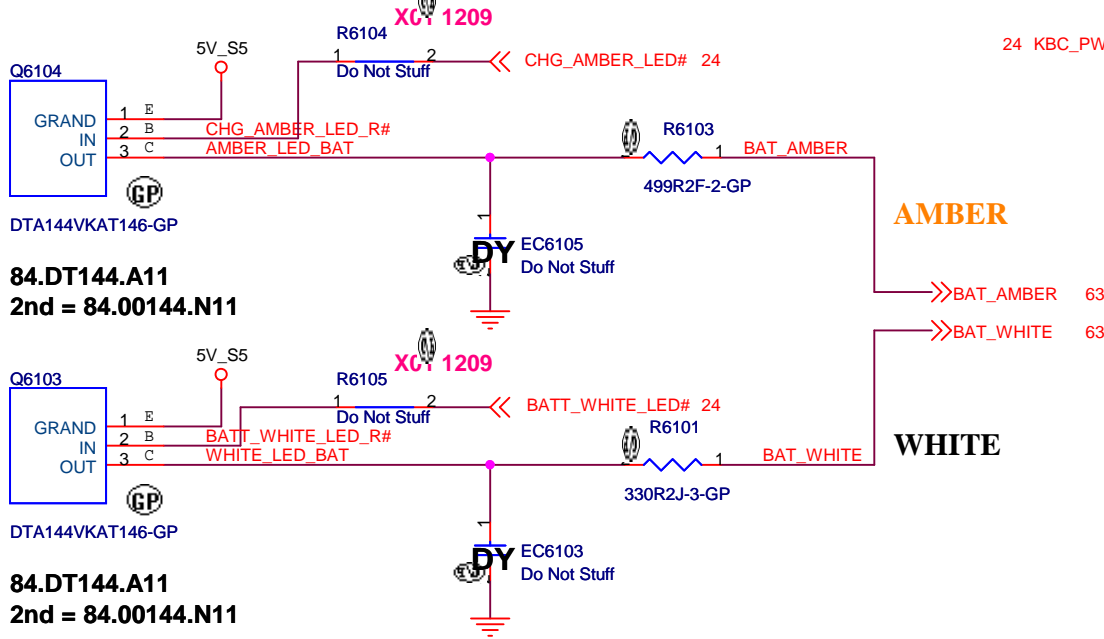
緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
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Title		
(Reserved)		

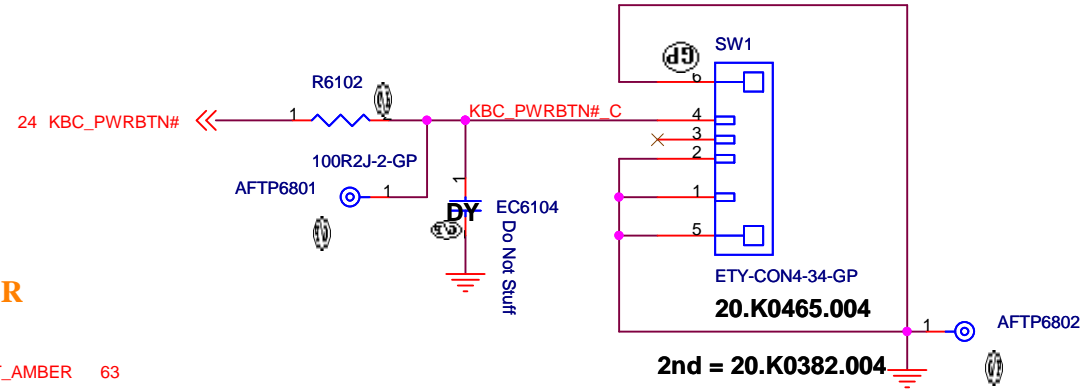
Size A4	Document Number Cedar AMD BEEMA	Rev A00
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Power button


Battery LED1 (AMBER_LED)
Low activated from KBC GPIO



Battery LED2 (WHITE_LED)
Low activated from KBC GPIO

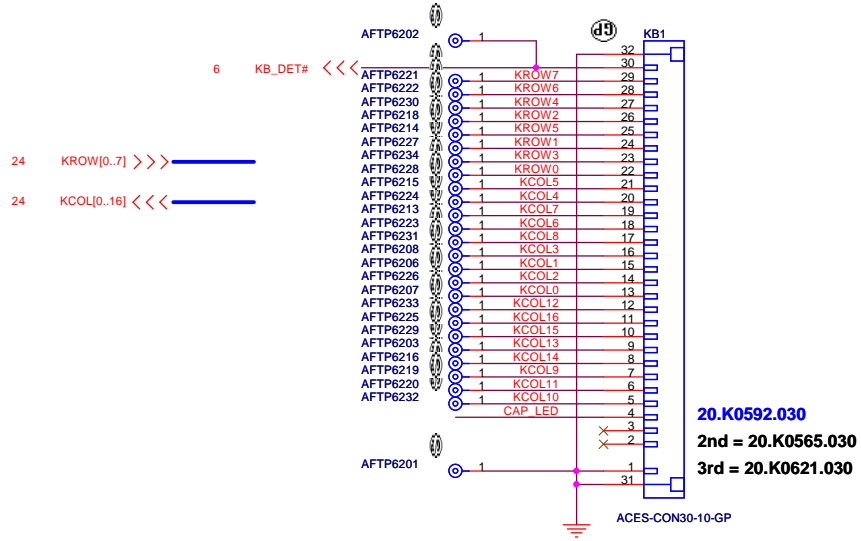


Cedar UMA 14

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LED Bard/Power Button	
Size A4	Document Number Cedar AMD BEEMA
Date: Wednesday, March 05, 2014	Rev A00
Sheet 61 of 104	

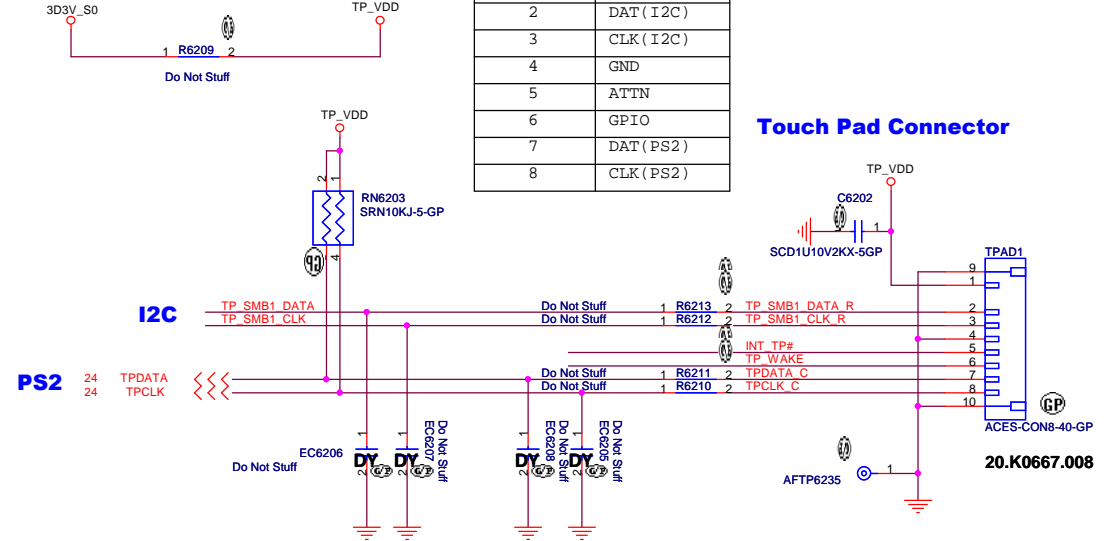
SSID = KBC

Internal Keyboard Connector (DVC40)

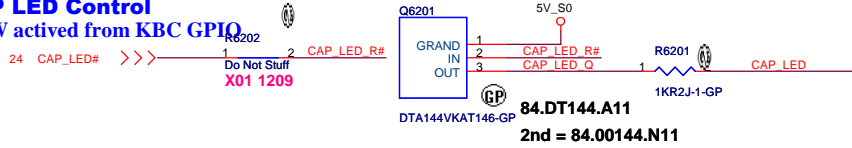


SSID = Touch.Pad

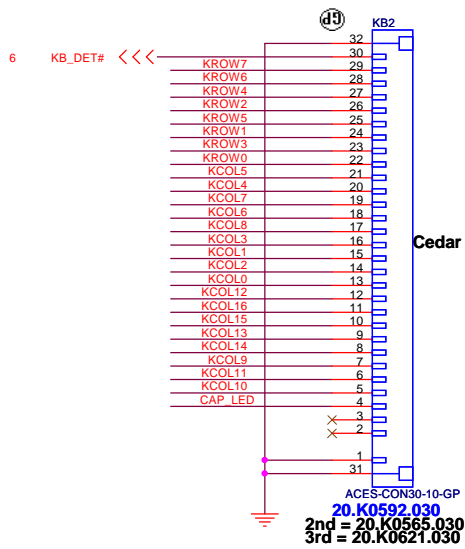
Pin number	Pin name
1	VDD
2	DAT (I2C)
3	CLK (I2C)
4	GND
5	ATTN
6	GPIO
7	DAT (PS2)
8	CLK (PS2)



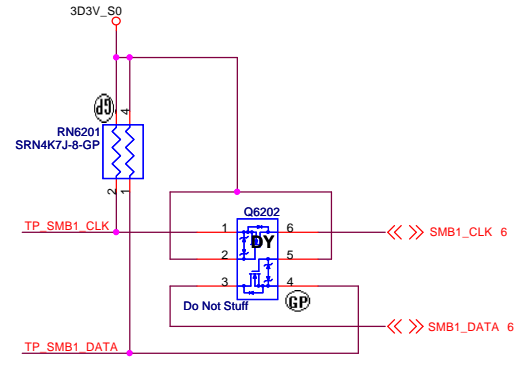
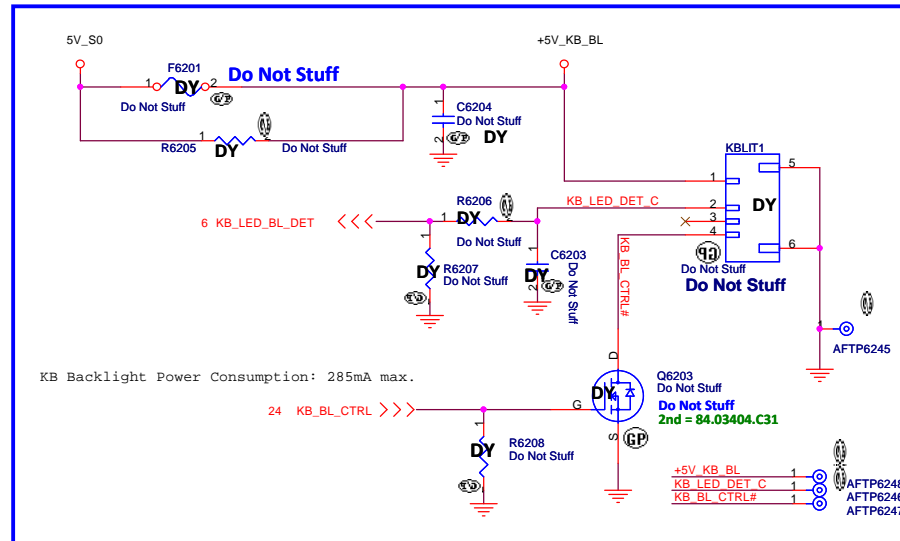
**CAP LED Control
LOW acted from KBC GPIO**



Internal Keyboard Connector (DVC50)



Keyboard Backlight



Cedar UMA 14

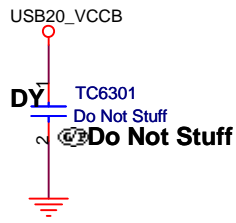
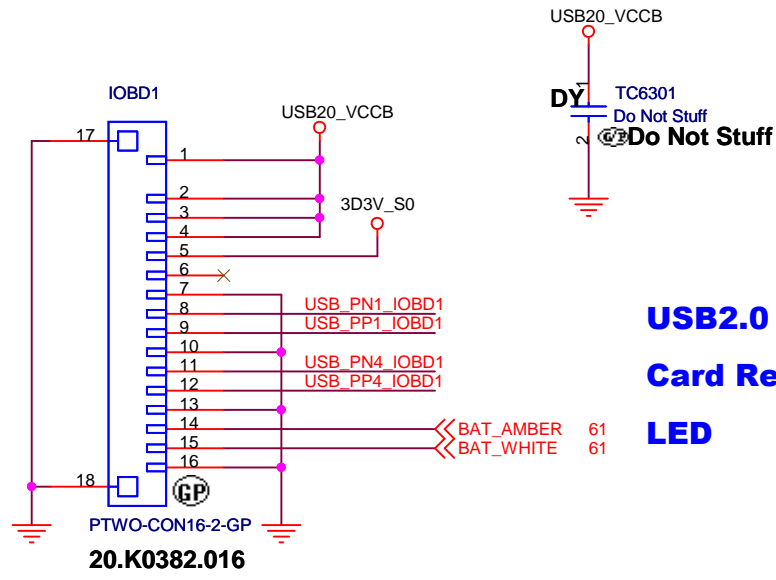
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Key Board/Touch Pad

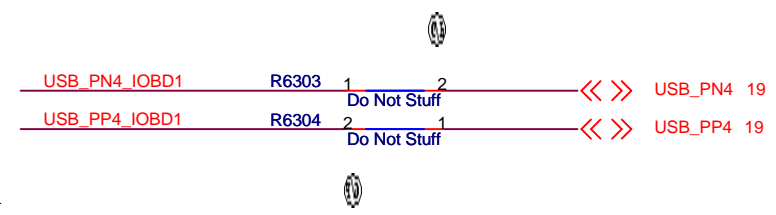
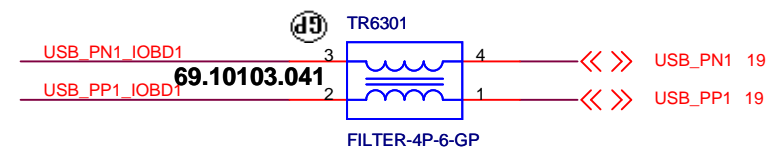
File: Cedar AMD BEEMA

Size: A3 Document Number: Rev: A00

Date: Wednesday, March 05, 2014 Sheet 62 of 104

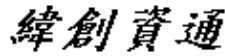


**USB2.0 Port3
Card Reader
LED**

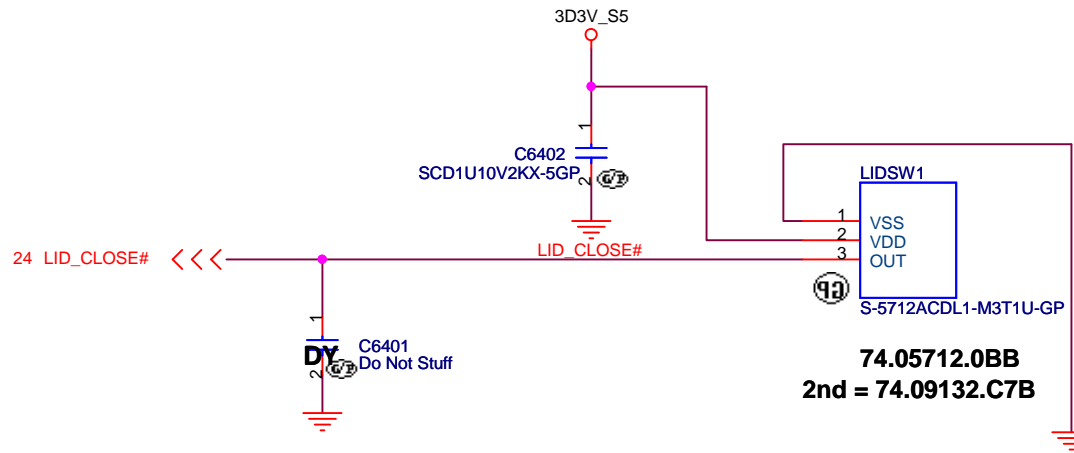


The maximum range of the PMOS output current in RTS5170 (Card Reader IC) is 400mA

Cedar UMA 14

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IO Board Connector	
Title IO Board Connector	Document Number Cedar AMD BEEMA
Size A4	Rev A00
Date: Wednesday, March 05, 2014	
Sheet 63 of 104	

SSID = User.Interface



74.05712.0BB
2nd = 74.09132.C7B

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Title

Hall Sensor

Size
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Document Number

Cedar AMD BEEMA

Rev
A00

Date: Wednesday, March 05, 2014

Sheet 64 of 104

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Cedar UMA 14

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Title

Reserved

Size
A4

Document Number

Cedar AMD BEEMA

Rev
A00

Date: Wednesday, March 05, 2014

Sheet 66 of 104

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Cedar UMA 14

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Title **Reserved**

Size A3	Document Number Cedar AMD BEEMA	Rev A00
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Date: Wednesday, March 05, 2014 Sheet 67 of 104

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Cedar UMA 14

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Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

Thunderbolt (1/5)

Size
A4

Document Number

Cedar AMD BEEMA

Rev

A00

Date: Wednesday, March 05, 2014

Sheet 68 of 104

5

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Title

Thunderbolt (2/5)

Size

A4

Document Number

Cedar AMD BEEMA

Rev

A00

Date: Wednesday, March 05, 2014

Sheet 69 of 104

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Taipei Hsien 221, Taiwan, R.O.C.

Title
Thunderbolt (3/5)

Size A4	Document Number Cedar AMD BEEMA	Rev A00
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Date: Wednesday, March 05, 2014 Sheet 70 of 104

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Cedar UMA 14

緯創資通

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

Thunderbolt (4/5)

Size
A4

Document Number

Cedar AMD BEEMA

Rev

A00

Date: Wednesday, March 05, 2014

Sheet 71 of 104

5

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Cedar UMA 14

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Thunderbolt (5/5)

Size

A4

Document Number

Cedar AMD BEEMA

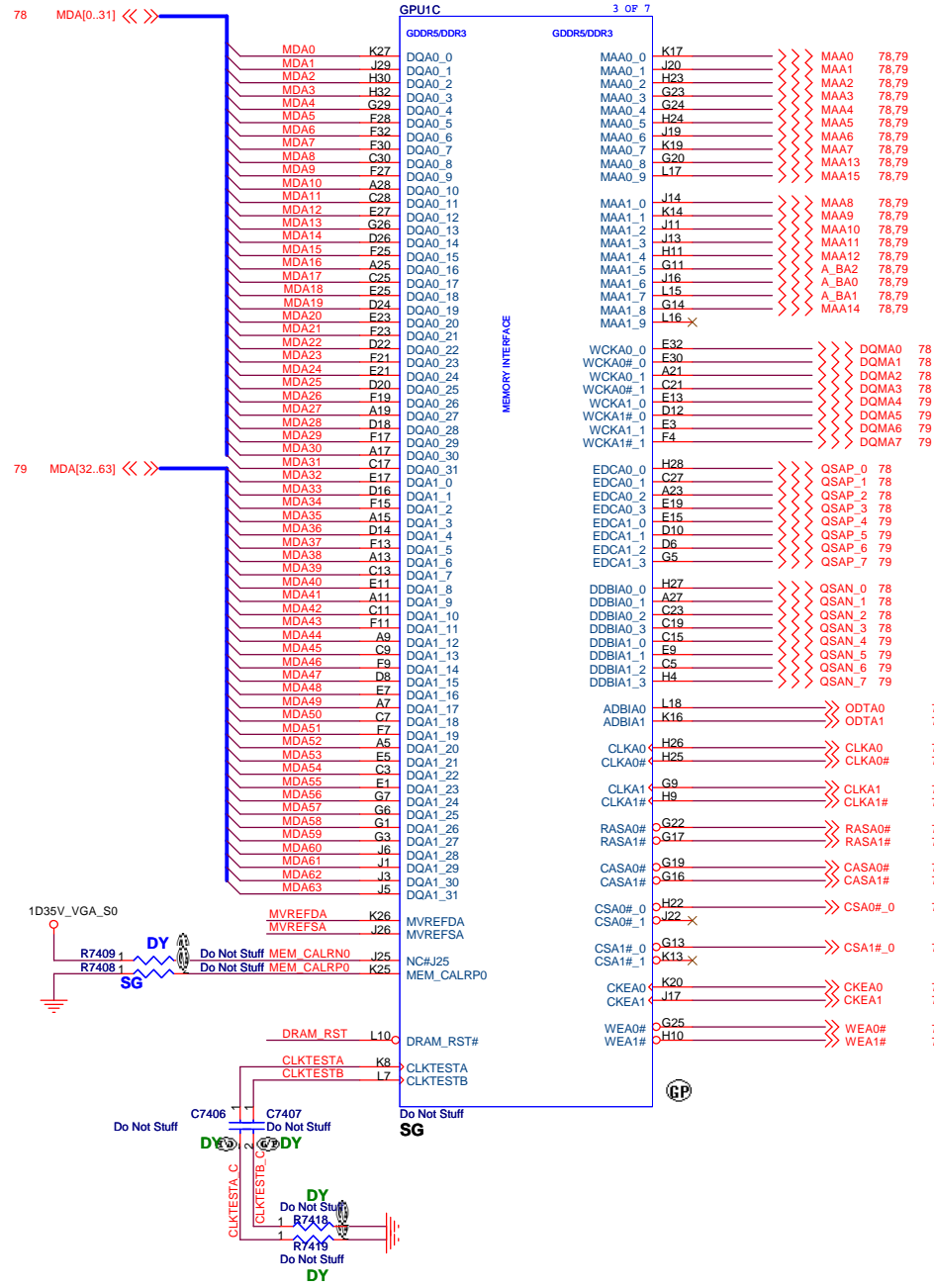
Rev

A00

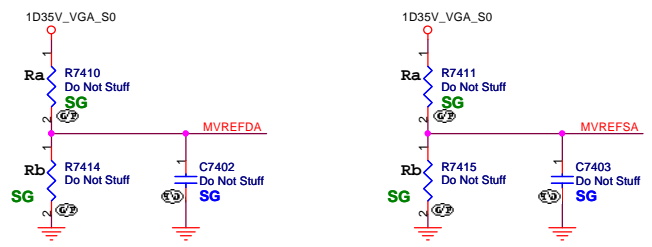
Date: Wednesday, March 05, 2014

Sheet 72 of 104

104

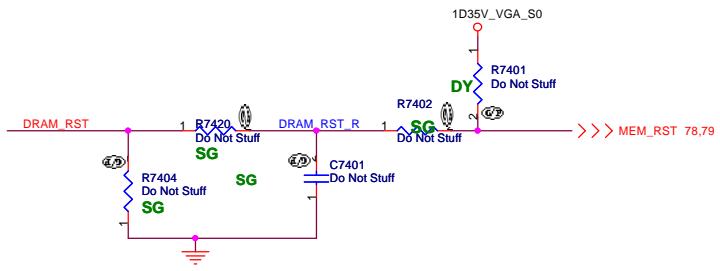


PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC



DDR3/GDDR3 Memory Stuff Option(Mad/Park)

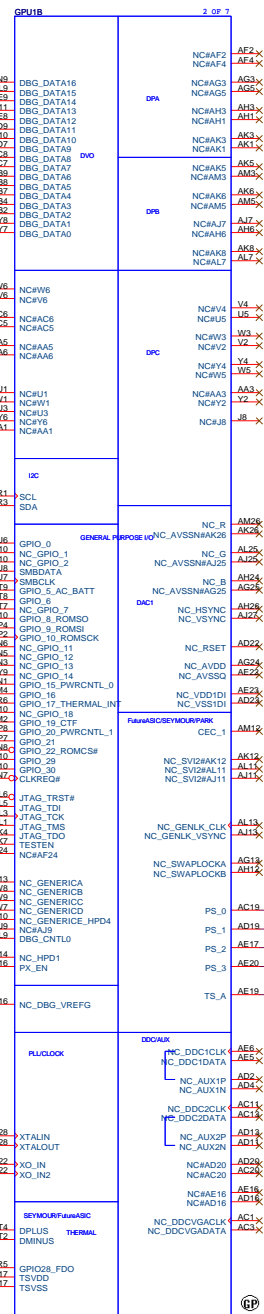
	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1.8V/1.5V	1.35V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R



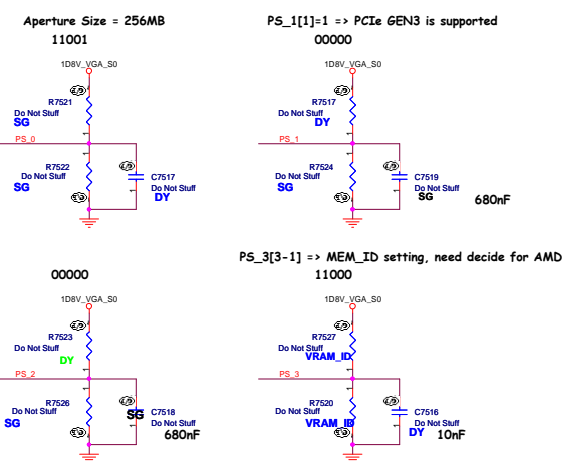
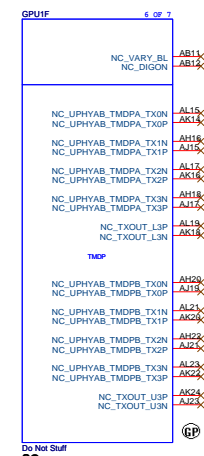
Cedar UMA 14

緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

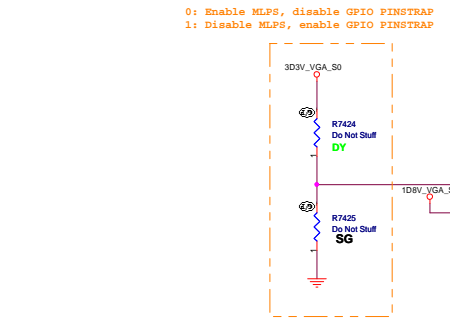
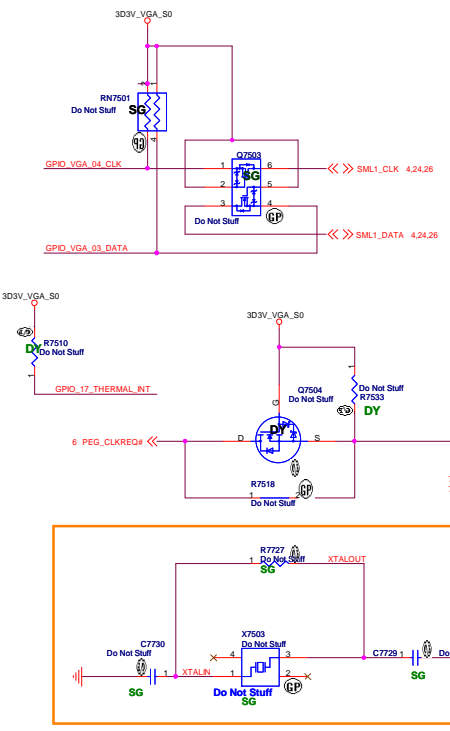
Title GPU Digitalout		
Size A3	Document Number Cedar AMD BEEMA	Rev A00
Date: Wednesday, March 05, 2014	Sheet 74	of 104



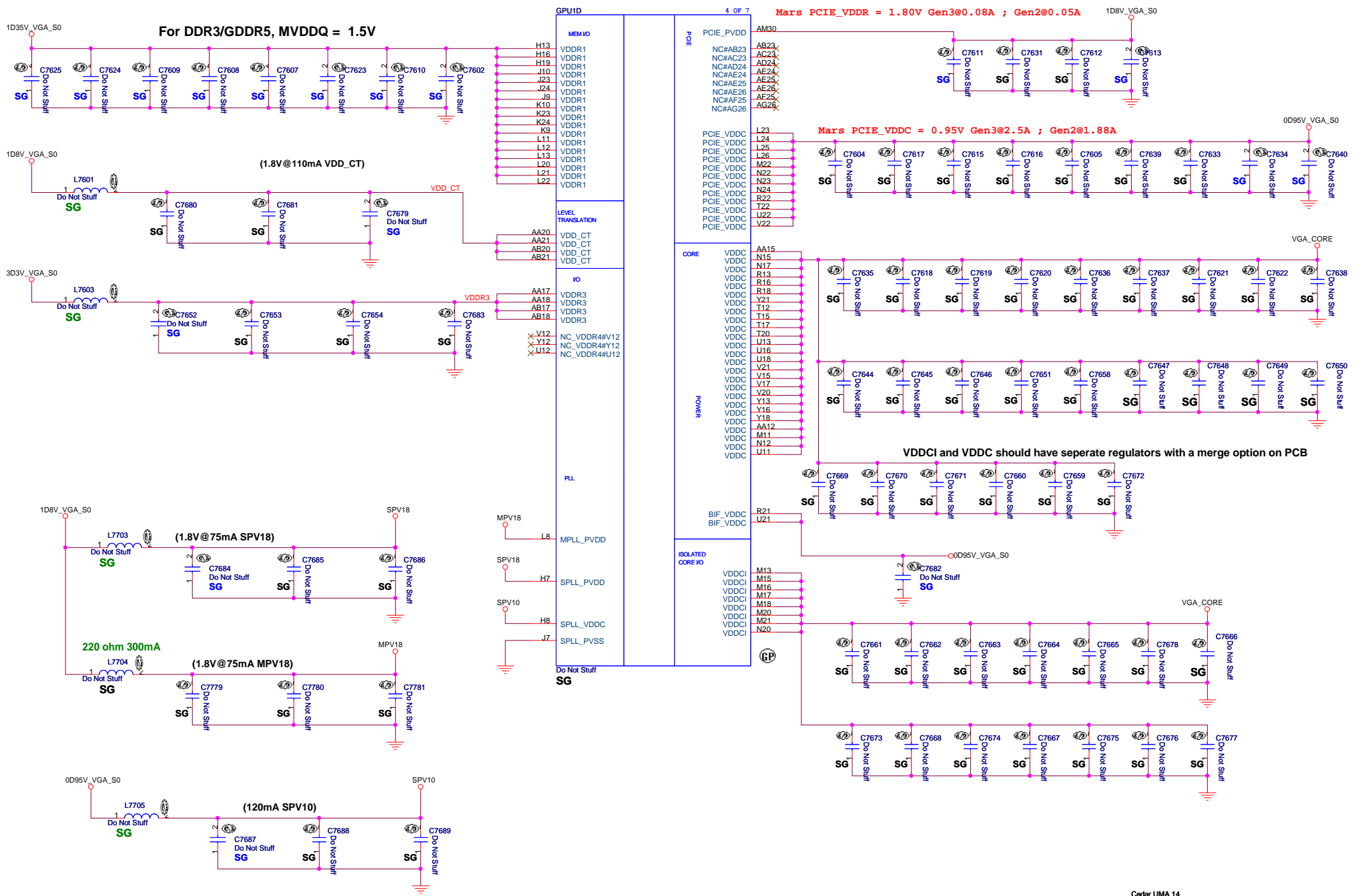
LVDS Interface



	Bit5,4		Bit3,2,1			
	C	nF	R _{pu}	K Ohm	R _{pd}	K Ohm
PS0	C8517	NC	R8521	8.45	R8522	2
PS1	C8519	680	R8517	NC	R8524	4.75
PS2	C8518	680	R8523	NC	R8526	4.75
PS3	C8516	NC	R8527	NC	R8520	4.75



0: Enable MLPS, disable GPIO PINSTRAP
 1: Disable MLPS, enable GPIO PINSTRAP



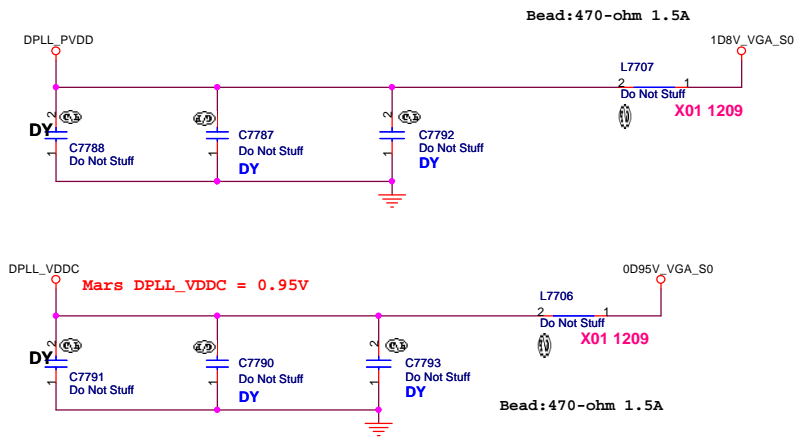
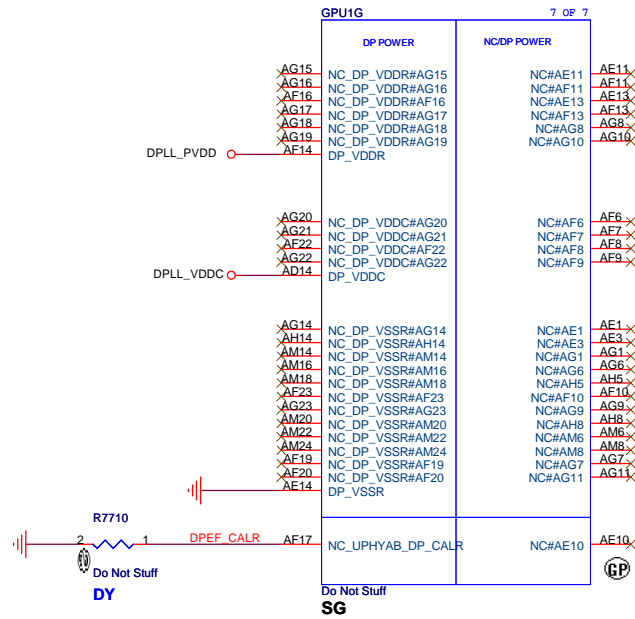
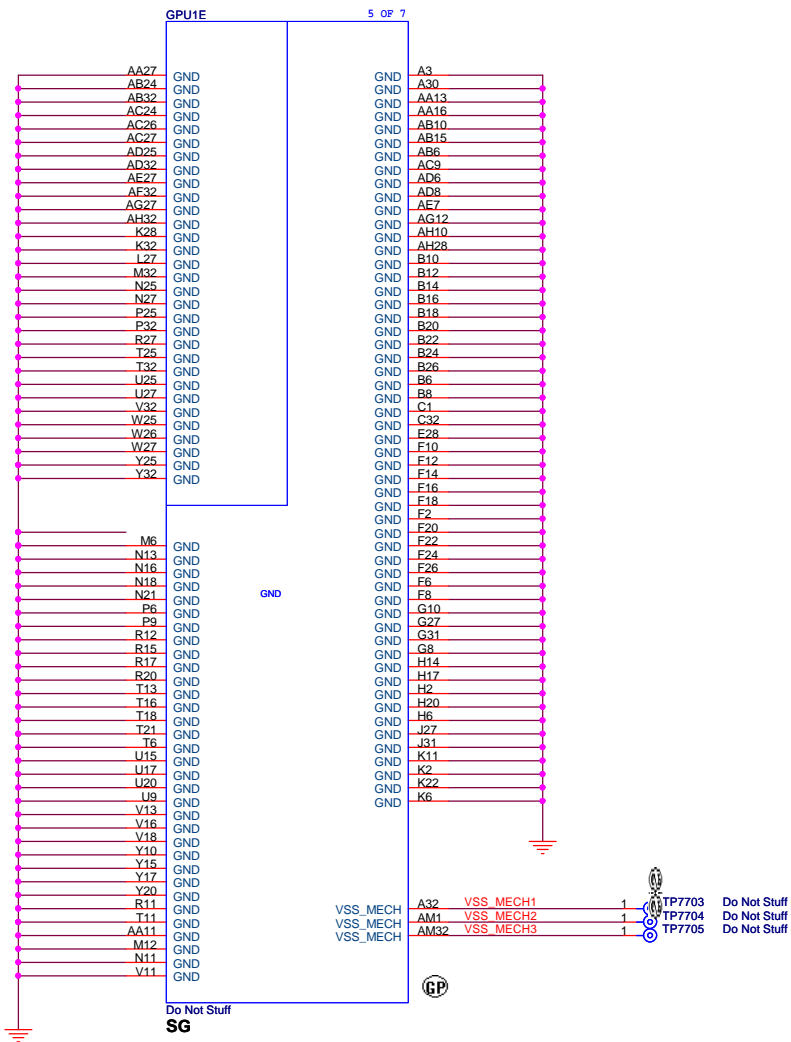
Mars PCIe_VDDR = 1.80V Gen3@0.08A ; Gen2@0.05A

Mars PCIe_VDDC = 0.95V Gen3@2.5A ; Gen2@1.88A

VDDCI and VDDC should have separate regulators with a merge option on PCB

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GPU_GPIO/STRAP	
Title	Document Number
Size	Custom
Cedar AMD BEEMA	
Date: Wednesday, March 05, 2014	Sheet 76 of 104
Rev	A00



Cedar UMA 14

緯創資通 Wistron Corporation	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title GPU_POWER/GND	
Size	Project Name <Project Name>
Date: Wednesday, March 05, 2014	Rev <Rev>
Sheet 77	of 104

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Cedar UMA 14

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Title

Reserved

Size

A4

Document Number

Cedar AMD BEEMA

Rev

A00

Date: Wednesday, March 05, 2014

Sheet 80 of 104

5

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Cedar UMA 14

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size

A4

Document Number

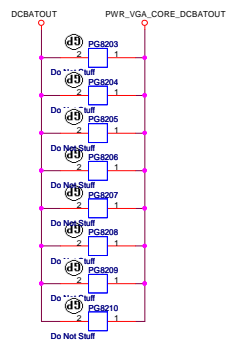
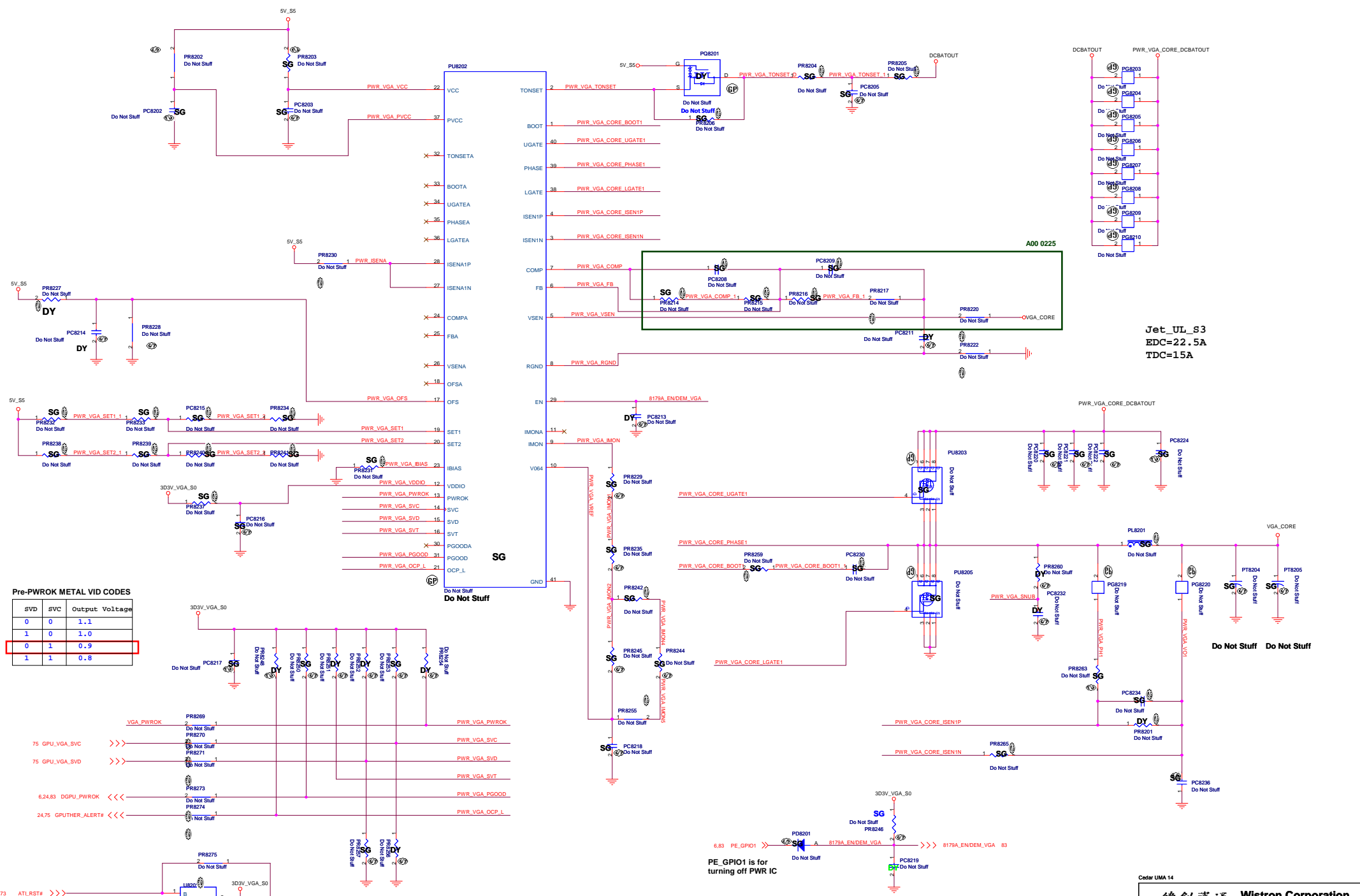
Cedar AMD BEEMA

Rev

A00

Date: Wednesday, March 05, 2014

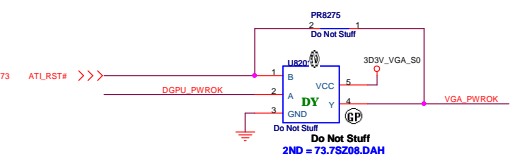
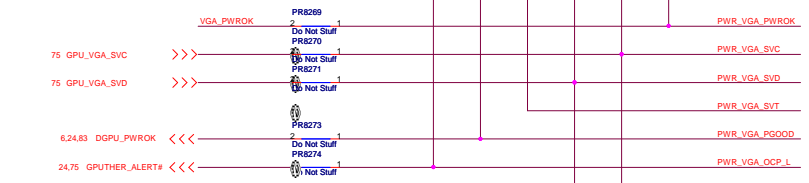
Sheet 81 of 104



Jet_UL_S3
EDC=22.5A
TDC=15A

Pre-PWROK METAL VID CODES

SVD	SVC	Output Voltage
0	0	1.1
1	0	1.0
0	1	0.9
1	1	0.8

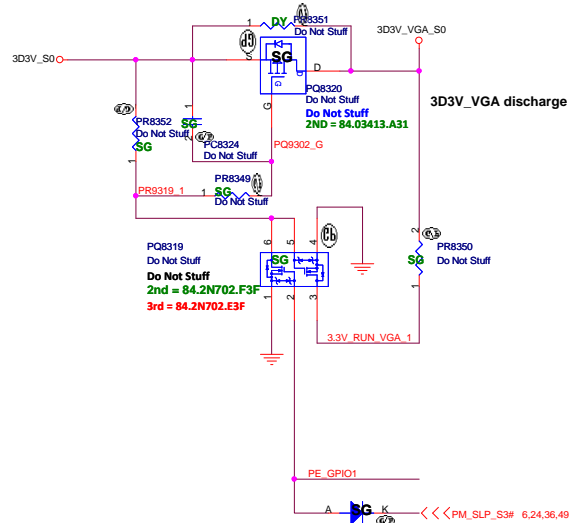


I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
 Inductor: CHIP CHOKR 0.36UH PCME064T-R36MS1R407 1.4mOhm / Isat =24Arms 68.R3610.20W
 O/P cap:CHIP CAP 470UF 2V EEPX0D471X /Panasonic/ 6mOhm / 79.47719.2BL
 CHIP CAP EL 330U 2.5V M6.3*4.4 3.5Arms Chemi-con/79.3371V.6CL
 FET MOS /H/S: SIRA14DP /6.8mohm/8.5mohm / 2.9mOhm/3.5mohm@4.5Vgs / 84.A14DP.037
 L/S: SIRA06DP /6.8mohm/8.5mohm / 2.75mOhm/3.5mohm@4.5Vgs / 84.SRA06.037

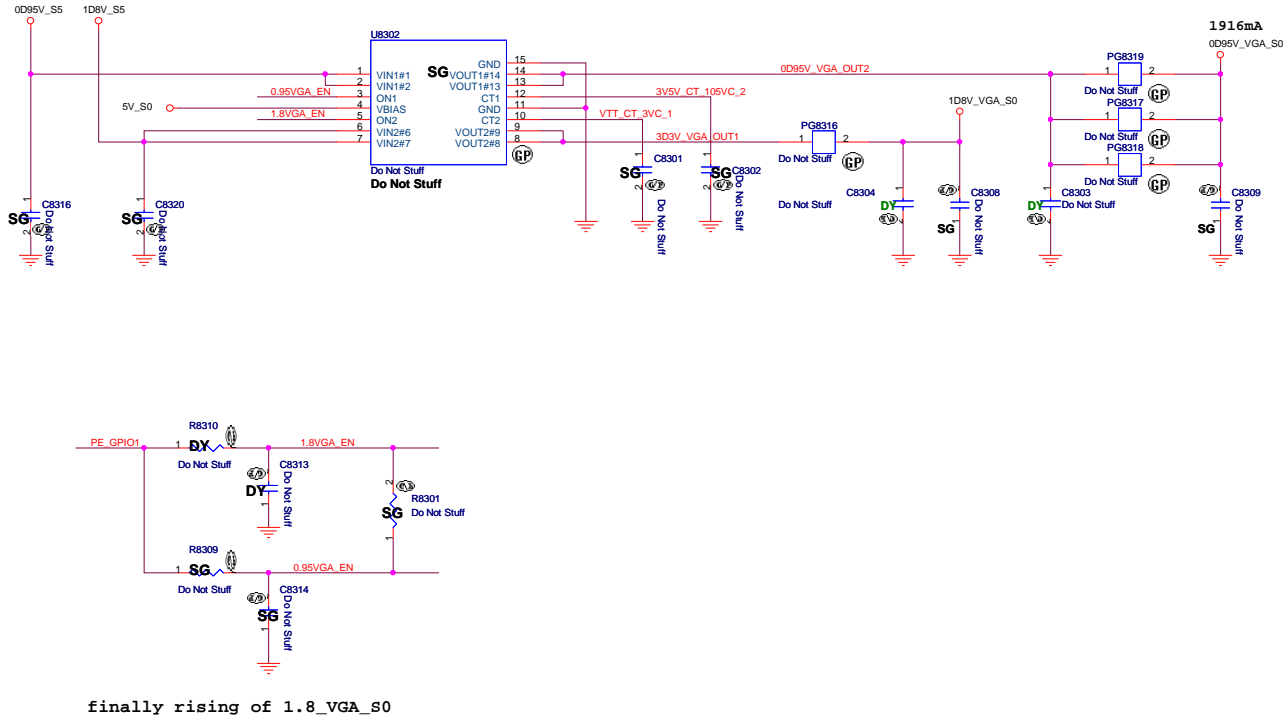
PE_GPIO1 is for turning off PWR IC

3D3V_S0 to 3D3V_VGA_S0 Transfer

Change DUMMY Reference Name to PX_BACO

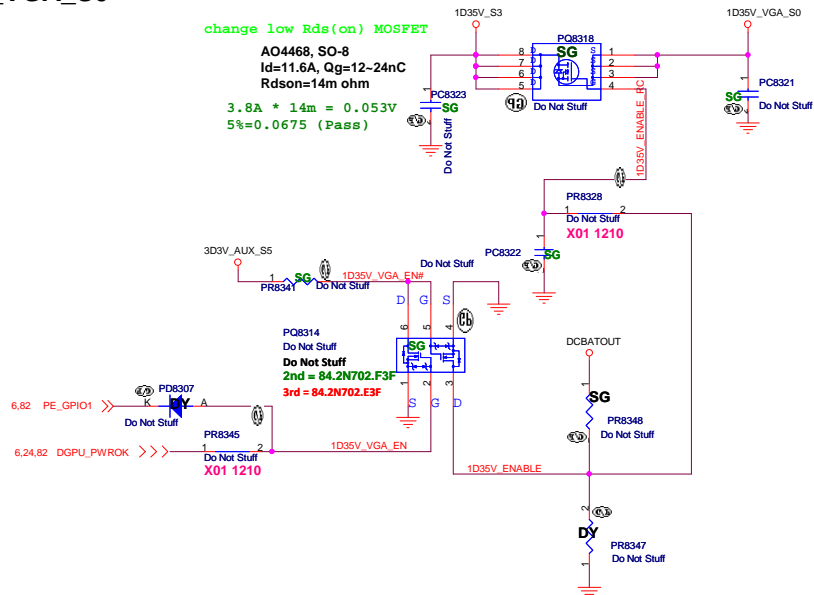


	PE_GPIO0	PE_GPIO1
dGPU mode	H	H
IGPU	L	L
IGPU with BACC	H	H

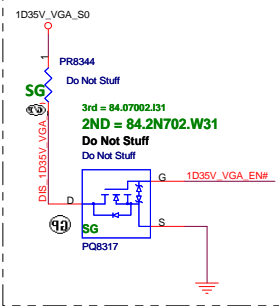


1D35V_VGA_S0

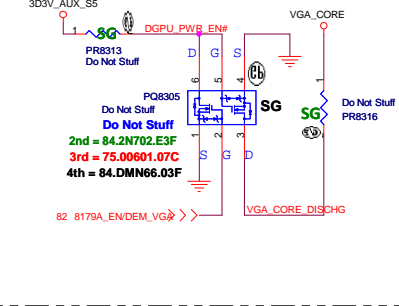
change low Rds(on) MOSFET
 AO4468, SO-8
 Id=11.6A, Qg=12-24nC
 Rdson=14m ohm
 $3.8A * 14m = 0.053V$
 $5\% = 0.0675$ (Pass)



Discharge Circuit



VGA_CORE Discharge Circuit



Cedar UMA 14

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Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size

A4

Document Number

Cedar AMD BEEMA

Rev

A00

Date: Wednesday, March 05, 2014

Sheet 84 of 104

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Cedar UMA 14

緯創資通

Wistron Corporation
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Title

(Reserved)

Size

A4

Document Number

Cedar AMD BEEMA

Rev

A00

Date: Wednesday, March 05, 2014

Sheet 85 of 104

5

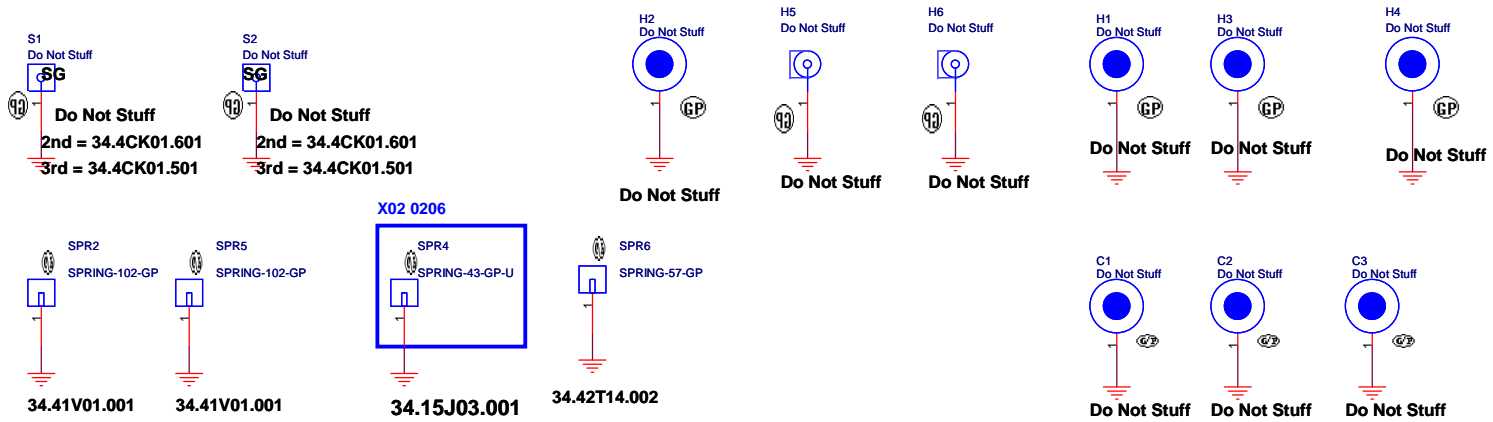
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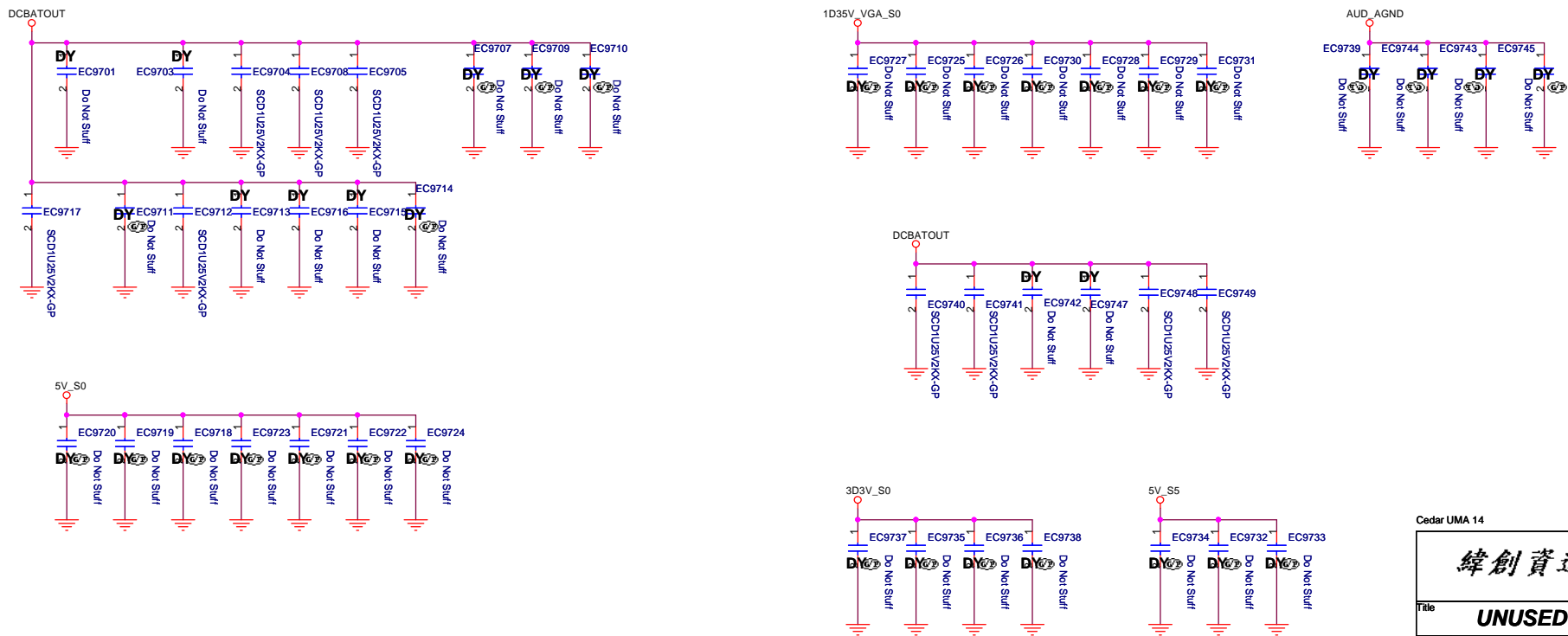
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SSID = Mechanical



SSID = EMI



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Cedar UMA 14

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
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Title **NFC(Reserved)**

Size A4	Document Number Cedar AMD BEEMA	Rev A00
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Date: Wednesday, March 05, 2014 Sheet 87 of 104

(Blanking)

Cedar UMA 14

緯創資通			Wistron Corporation		
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
TPM/TCM					
Size	Document Number				Rev
A3	Cedar AMD BEEMA				A00
Date:	Wednesday, March 05, 2014		Sheet	88	of 104

(Blanking)

Cedar UMA 14

緯創資通		Wistron Corporation	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichia, Taipei Hsien 221, Taiwan, R.O.C.		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichia, Taipei Hsien 221, Taiwan, R.O.C.	
Reserved K Series Connector			
Title			
Size	Document Number	Rev.	
A2	Cedar AMD BEEMA	A00	
Date:	Wednesday, March 05, 2014	Sheet	89 of 104

(Blanking)

Cedar UMA 14

緯創資通		Wistron Corporation	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
TEST PAD			
Size	Document Number	Rev	
C	Cedar AMD BEEMA	A00	
Date:	Wednesday, March 05, 2014	Sheet	90 of 104

5

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Cedar UMA 14

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size

A4

Document Number

Cedar AMD BEEMA

Rev

A00

Date: Wednesday, March 05, 2014

Sheet 91 of 104

5

4

3

2

1

(Blanking)

Cedar UMA 14

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size

A4

Document Number

Cedar AMD BEEMA

Rev

A00

Date: Wednesday, March 05, 2014

Sheet 92 of 104

5

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C

B

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(Blanking)

Cedar UMA 14

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size

A4

Document Number

Cedar AMD BEEMA

Rev

A00

Date: Wednesday, March 05, 2014

Sheet 93 of

104

5

4

3

2

1

(Blanking)

Cedar UMA 14

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size

A4

Document Number

Cedar AMD BEEMA

Rev

A00

Date: Wednesday, March 05, 2014

Sheet 94 of 104

5

4

3

2

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C

C

B

B

A

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(Blanking)

Cedar UMA 14

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size

A4

Document Number

Cedar AMD BEEMA

Rev

A00

Date: Wednesday, March 05, 2014

Sheet 95 of

104

5

4

3

2

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(Blanking)

Cedar UMA 14

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
MCP CPU XDP HDT+			
Size	Document Number	Rev	
A3	Cedar AMD BEEMA	A00	
Date: Wednesday, March 05, 2014		Sheet 96	of 104

(Blanking)

Cedar UMA 14

<p>緯創資通</p>	<p>Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>
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Title

Table of Content

Size A4	Document Number Cedar AMD BEEMA	Rev A00
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5

4

3

2

1

D

D

C

C

B

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Cedar UMA 14


Wistron Corporation
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 Taipei Hsien 221, Taiwan, R.O.C.

Title **Change History**

Size A3	Document Number Cedar AMD BEEMA	Rev A00
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Date: Wednesday, March 05, 2014 Sheet 98 of 104

5

4

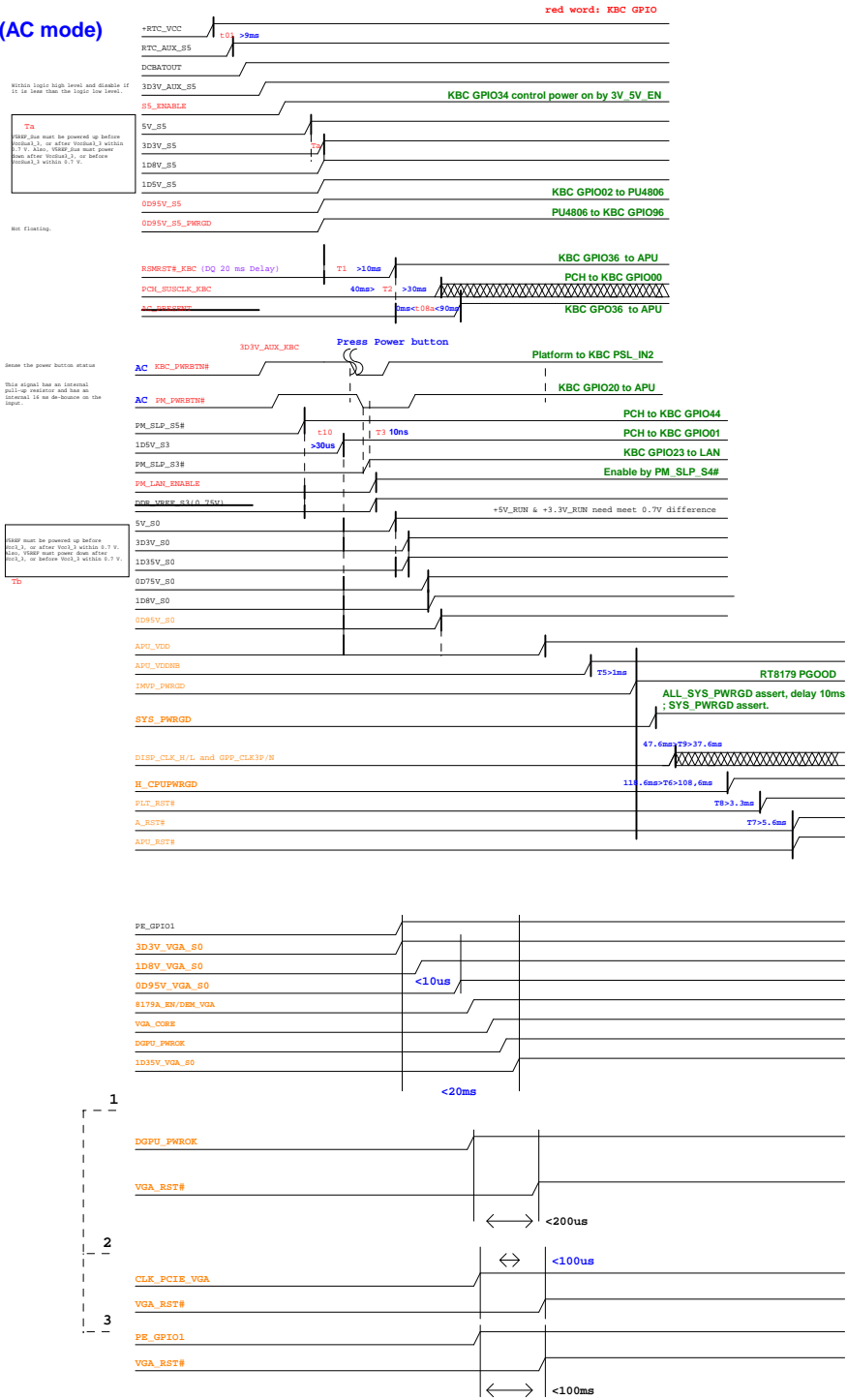
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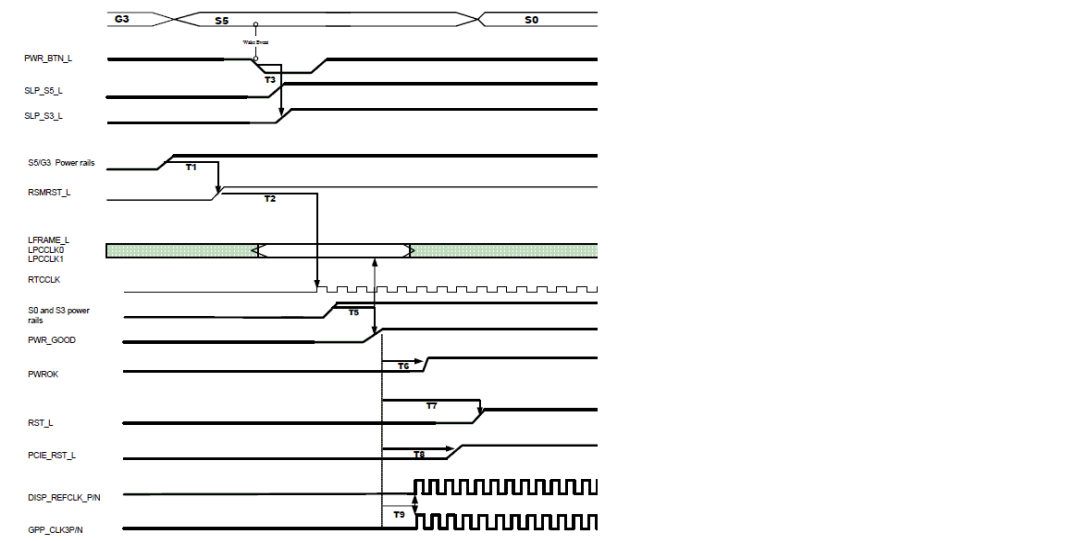
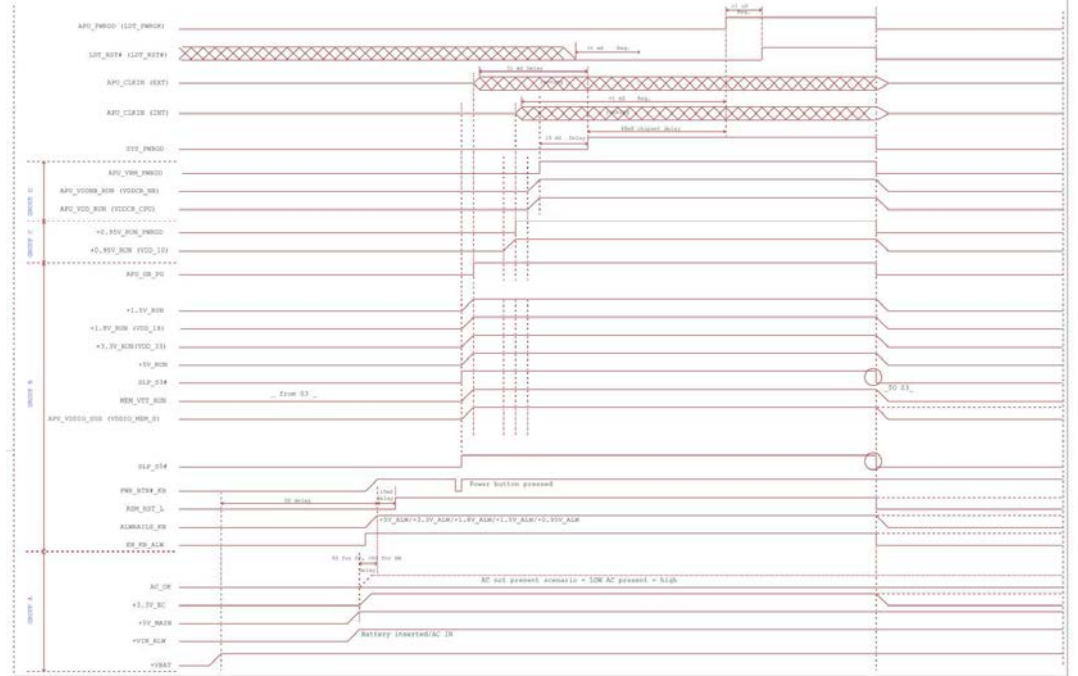
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Beema Platform Power Sequence

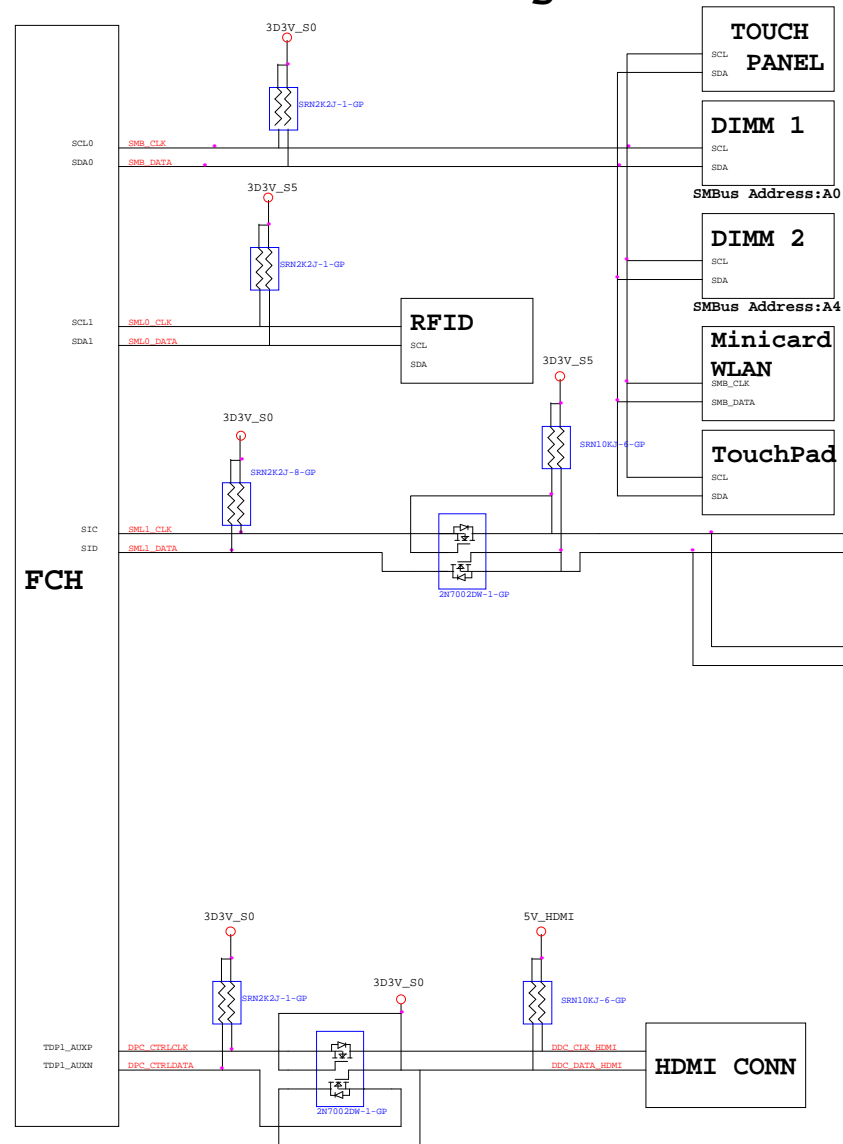
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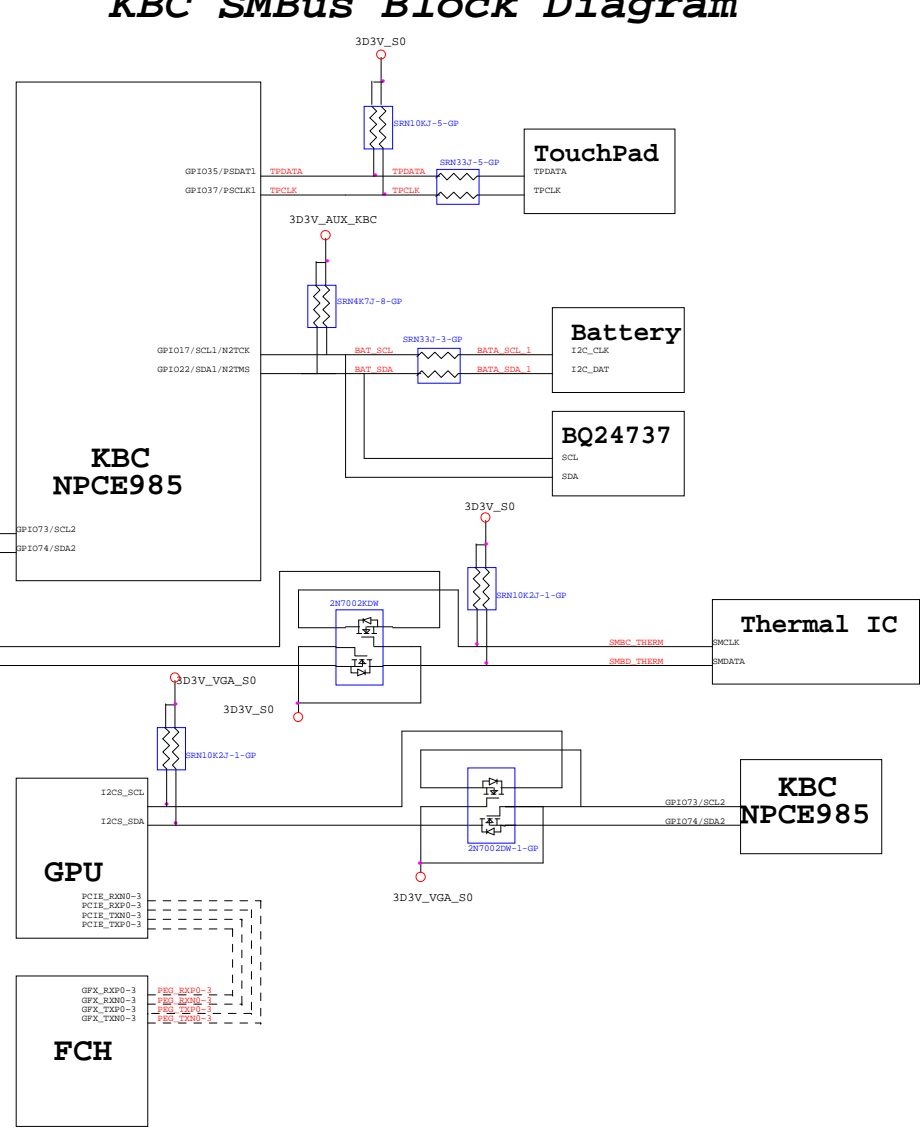
Power-up Sequencing for the KABINI Platform from Mechanical Off



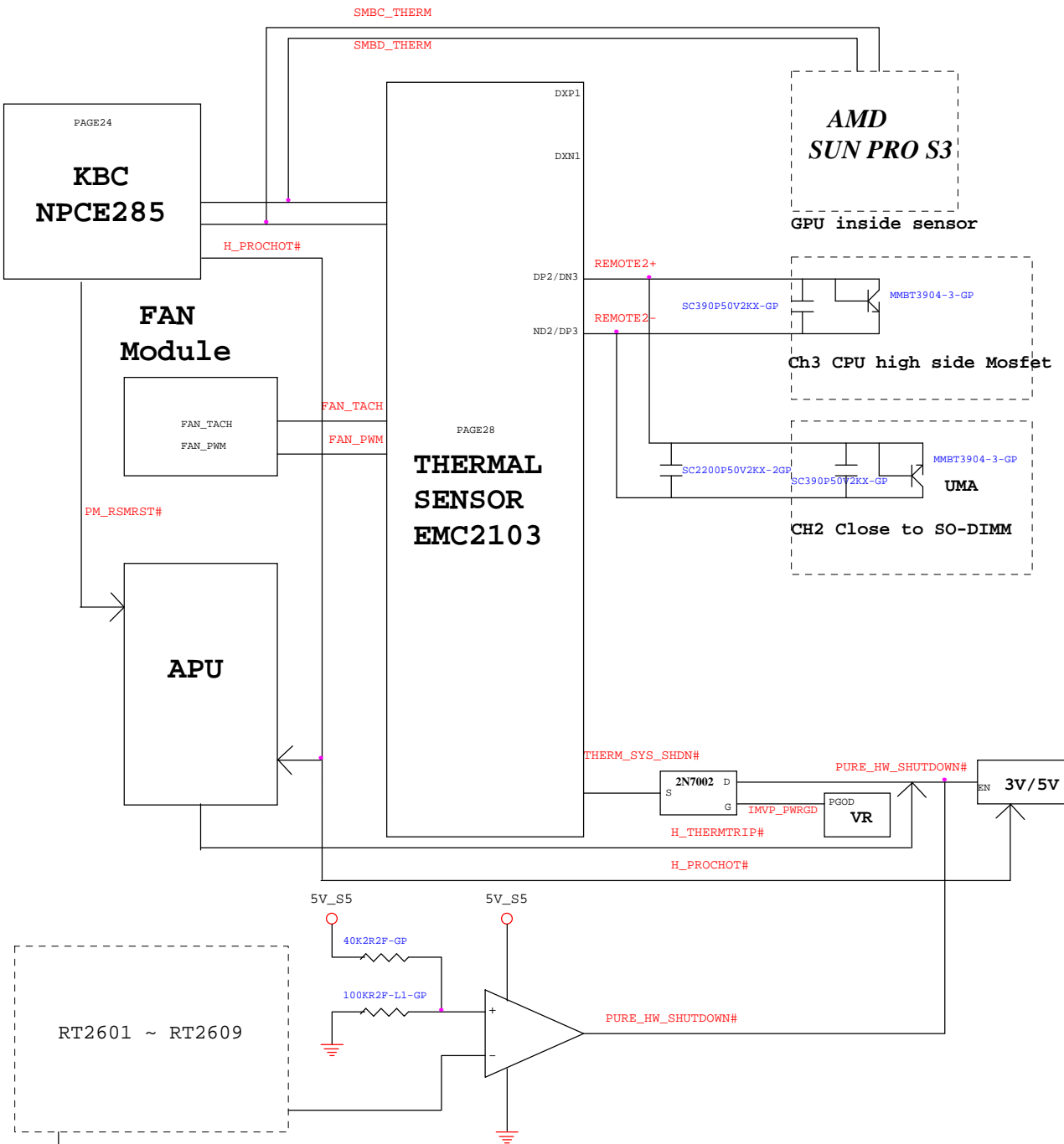
PCH SMBus Block Diagram



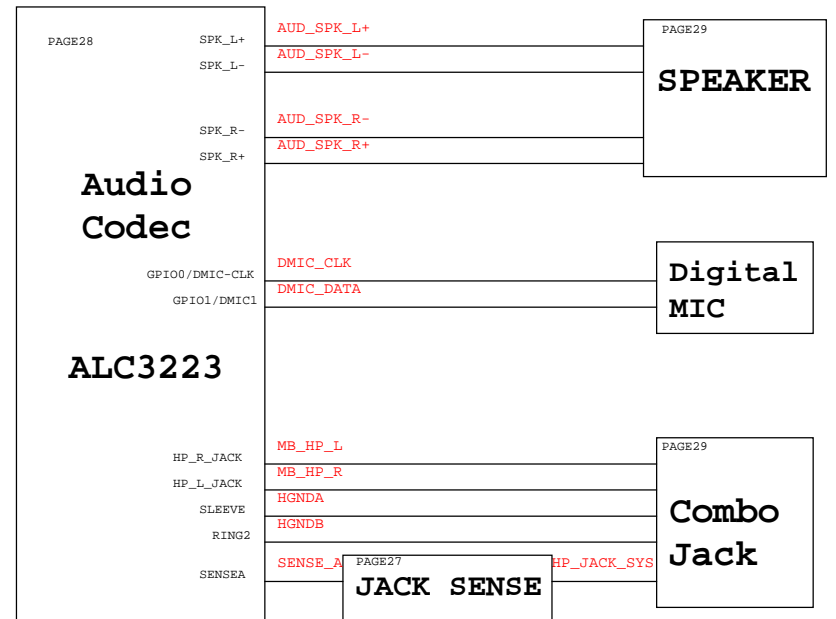
KBC SMBus Block Diagram



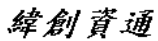
Thermal Block Diagram



Audio Block Diagram



Cedar UMA 14

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Thermal/Audio Block Diagram	
Size	Document Number
Custom	Cedar AMD BEEMA
Date: Wednesday, March 05, 2014	Sheet 102 of 104
Rev	A00

Change notes -

VERSON	DATE	Page	Modify List	OWNER
X01	2013/12/3	83	R8309 = 15Kohm ,C8301/C8313 = DY,C8302 = 1000pF	
X01	2013/12/3	43 44	RN4301 to 100ohm, AC_IN# change to Pull-H 3D3V_AUX_S5(PR4434)	
X01	2013/12/3	27	HDA27 change from ALS3223 to ALC3234	
X01	2013/12/3	24 25	Swap BATT_WHITE_LED# and EC_BRIGHTNESS. BATT_WHITE_LED# to GPIO13 and EC_BRIGHTNESS to GPIO15. Change R2404 from 10K to 20K ohm for PCB VERSION strap , Del SKT25	
X01	2013/12/3	52	Reserve 0805 0 ohm R5211 between LCDVDD and LCD1.F5201 change from 69.50007.A31 to 69.60040.001	
X01	2013/12/3	Power	Change C5205,EC4304,EC4601,PC4409,PC4419,PC4511.PC4518,PC4524,PC4720,PC4722,PC4827, PC4913 to 78.10422.2BL (0.1U 25V K0603 X7R) from 78.10424.2BL (0.1U 50V K0603 X7R).	
X01	2013/12/3	54 55	Add HDMI SMBUS use 0 ohm DUMMY co-lay ,Add Hsync Vsync 0ohm DUMMY co-lay	
X01	2013/12/3	29	Change HPMIC1 to 022.10002.0001 from 22.10270.G61 SPK1 change to 20.F1639.004	
X01	2013/12/3	34 63	Change USB1 to 22.10341.Q21 / Change KBLIT1 to 20.K0800.004	
X01	2013/12/3	19 26	Change C1904 and C1905 from 10pf to 6.8pf / Q2601 RN2602 DUMMY, RN2601 install	
X01	2013/12/3	30	R3004 CLK_LAN_REQ0#_R change pull high to 3D3V_S0	
X01	2013/12/3	EMI	DMIC_CLK mount R2716 100ohm resistance,Mount EC9749,Mount EC4304	
X01	2013/12/3	58	CARD_WLAN_OUT# and CARD_WPAN_OUT# modify to TP change WLAN1 to 62.10043.I81	
X01	2013/12/3	42 51	DCIN1 change to 20.F1783.007,Del 1D5V_S5 circuit	
X01	2013/12/4	24 34 35	R2447 change to 63.10334.1DL,Del U3502 and U3501,swap the net U3403.1 and U3403.3	
X01	2013/12/5	42 46 24 26	Del AFTP3804 AFTP3807, Modify AFTP6241 Add AFTP6242,Change R2447 to 1K , R2622 change to 24.3K	
X01	2013/12/6	24	R2411 DY D2401 install	
X01	2013/12/9	31 47 82	RJ45 connector change to 022.10001.0551, PT4701 /PT4704/PT8204 change to 79.3371V.6CL	
X01	2013/12/10	EMI	Mount EC4303 and change to 0.1u Mount EC9705 EC9748 EC9717 EC9740 EC9741 EC9712 EC9704 EC9708 and change to 0.1u Mount R5415、R5417、R5416、R5414 150ohm resistance Mount TR3401、TR3404、TR6301(69.10103.041、69.10080.011) Mount TR5208、TR5209(69.10103.041、69.10080.011) Mount EC2705、EC2703、EC9739、EC9743、EC9744 0.1u cap Mount SPR2、SPR5、SPR6	
X01	2013/12/10	0 ohm	change 0 ohm to short pad	
X01	2013/12/10	54 55	R5501/R5502 change to 33 ohm / Del D5402	
X01	2013/12/10	24 52 62	R2411 Install D2401 DUMMY ,R5207 BOM control ,BOM control DVC50 to Janus	
X01	2013/12/12	46 86 62	PR4609 change to 44.2K (64.44225.6DL) from short pad, EMI:Add SPR6(34.42T14.002),KBLIT DUMMY	
X01	2013/12/16	55 Power	Del CRT circuit / Modify power schematic BOM	
X01	2013/12/18	Power	PR8214 change to 499K (64.49935.6DL) / PR8215 change to 9.76K (64.97615.6DL)	

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Change List

Size

Document Number

A3

Cedar AMD BEEMA

Rev

A00

Date: Wednesday, March 05, 2014

Sheet 103 of 104

VERSON	DATE	Page	Modify List	OWNER
X02	2014/01/21	48	Change PR4823 to 26.1K. The voltage about 0.97V	
X02	2014/01/21	83	R8310 change 15Kohm /C8313 change 0.1uF /C8301 change 470pF Add R8301 for power sequence	
X02	2014/01/27	12, 46	EMC request:change EC4601,C1217,C1225,C1214 to 0.1u	
X02	2014/01/27		Change 0 ohm to short pad	
X02	2014/01/27	6	DGPU_PRESENT# pull hi to 3D3V_S0	
X02	2014/01/28	power	1. PD4201 change 1st source to 83.P6SEM.AAG and 2nd source to 83.P6SEM.DAG . 2. PC4202 PC4409 PC4419 PC4519 PC4524 PC4511 PC4513 PC4518 PC4734 PC4720 PC4722 PC4736 PC4833 PC4827 PC4919 PC4913 PC8230 change to 78.10424.2BL. 3. PC4201 change to 78.10594.41L. 4. PC4916,PC4917 change to 78.10610.5BL. 5. PC4408 change to 78.47522.51L (4.7U 25V K0805 X5R). 6. PC4425 change to 78.10324.2FL (0.01U 50V K0402 X7R). 7. PC4512 change to 78.47522.51L (4.7U 25V K0805 X5R). 8. Delete PC4814/PC4714. 9. Dummy PC4718/PC4912/PC4920/PC4204/PC4205/ PC4426/PC4416/PC4830 10.PC4828 change to 78.47522.51L (4.7U 25V K0805 X5R). 11.PC4909 and PC4911 change to 78.47522.51L (4.7U 25V K0805 X5R).	
X02	2014/01/28	31	change XF3101 and XF3102 to 68.68167.30D and Swap net	
X02	2014/02/06	06 19	Change RN1901 R1901 from short pad to 0 ohm Change RN604 to 66.10336.08L	
X02	2014/02/06	86	Change SPR4 P/N to 34.15J03.001	
X02	2014/02/07	26	THM26 DUMMY, Add R2602 for VD_OUT1# connect PURE_HW_SHUTDOWN#	
A00	2014/02/25		Change PR4911 PR4649 R3016 R6209 R1901 RN5404 RN1901 to short pad	
A00	2014/02/25	82	Modify schematic PWR_VGA_COMP connecte to PWR_VGA_FB	
A00	2014/02/25	24	PCB VERSION A/D(PIN98) R2404 change to 64.64925.6DL	
A00	2014/02/25	54	Install D5401 RN5401 Q5402, Dummy RN5404	

Cedar UMA 14

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Change List	
Size A3	Document Number Cedar AMD BEEMA
Date: Wednesday, March 05, 2014	Rev A00
Sheet 104 of 104	