MODEL NAME : *ZAW12*

PCB NO : *LA-A691P*

BOM P/N : *DA60012B000 LA-A691P M/B*
DA40001G410 LS-9105P POWER BUTTON/B
DA40001FP10 LS-9102P USB/B
DA40001FQ10 LS-9103P TP BUTTON/B
DA40001FR10 LS-9104P ODD/B

Dell / Compal Confidential

Schematic Document

AMD FP2 Richland Processor with DDRIII + Bolton M3 FCH
AMD VGA Sun XT

2013-05-23

Rev: 1.0

46@ : for 46 level
@ : Nopop Component
CONN@ : Connector Component
UMA@ : Only for UMA
DIS@ : Only for Discrete
GCLK@ : Green CLK implemented
NGCLK@ : Non Green CLK implemented
@3221: ALC 3221
@3223 : ALC 3223
EMC@ : EMC Parts
NEMC@ : EMC不上件

R1@ : R1 P/N for PCB
R3@ : R3 P/N for PCB
THR1@ : Thames-XT R1 P/N
THR3@ : Thames-XT R3 P/N
CHR1@ : Chelsea-Pro R1 P/N
CHR3@ : Chelsea-Pro R3 P/N
R@ : RTD2132-R
S@ : RTD2132-S
KBBL@ : KeyBoard Backlight

X76@ : VRAM Group
CH@ : Chelsea M2
SE@ : Seymour M2
TH@ : Thames-XT
Mars@ : Mars Pro M2
A4R1@ : A4 APU-R1
A6R1@ : A6 APU-R1
A8R1@ : A8 APU-R1
A8@ : A8 APU Symbol
Hud@ : HUDSON-M3
Bol@ : BOLTON-M3

Security Classification	Compal Secret Data		
Issued Date	2012/09/11	Deciphered Date	2014/03/12

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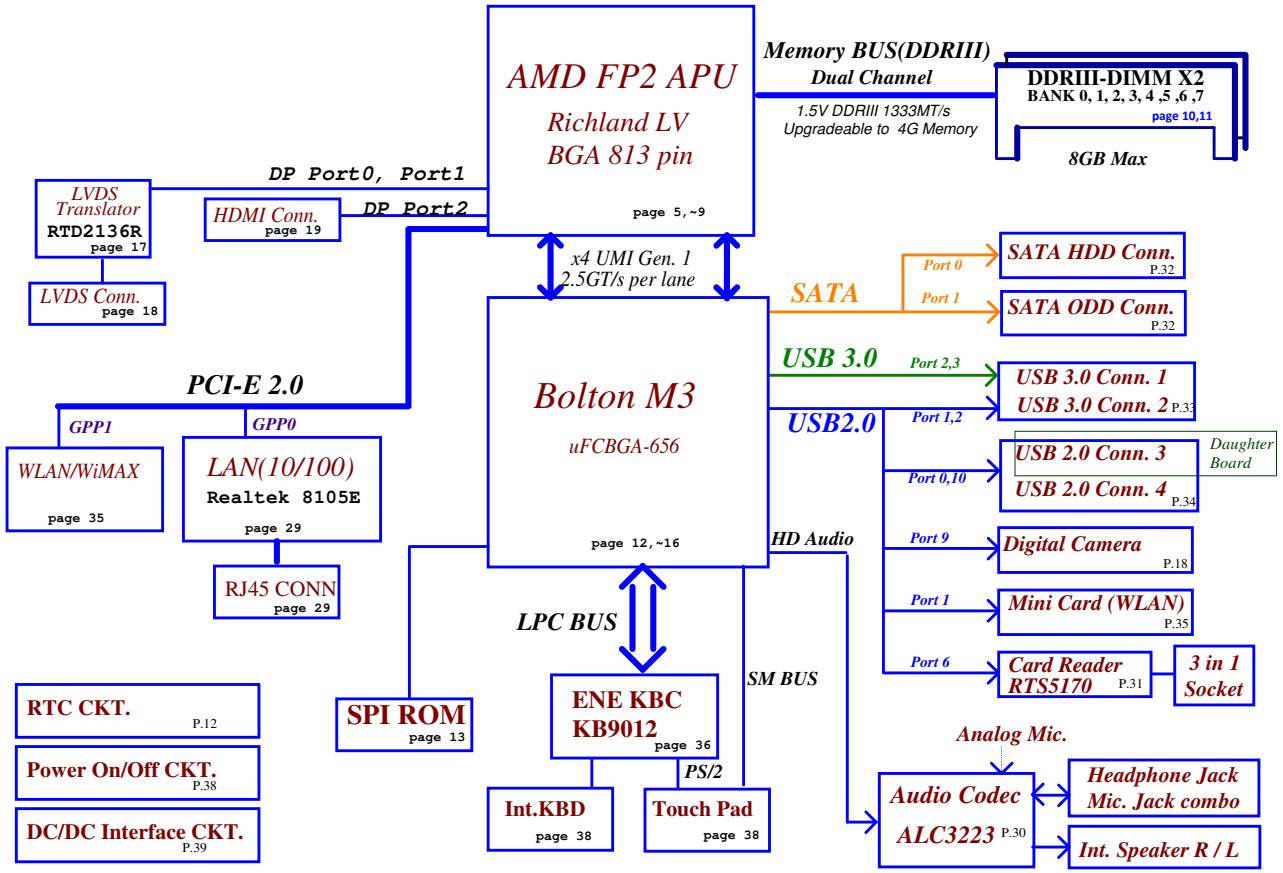
Title: *Cover Page*

Size: Custom | Document Number: *LA-9103P* | Rev: 1.0

Date: Wednesday, July 10, 2013 | Sheet 1 of 52

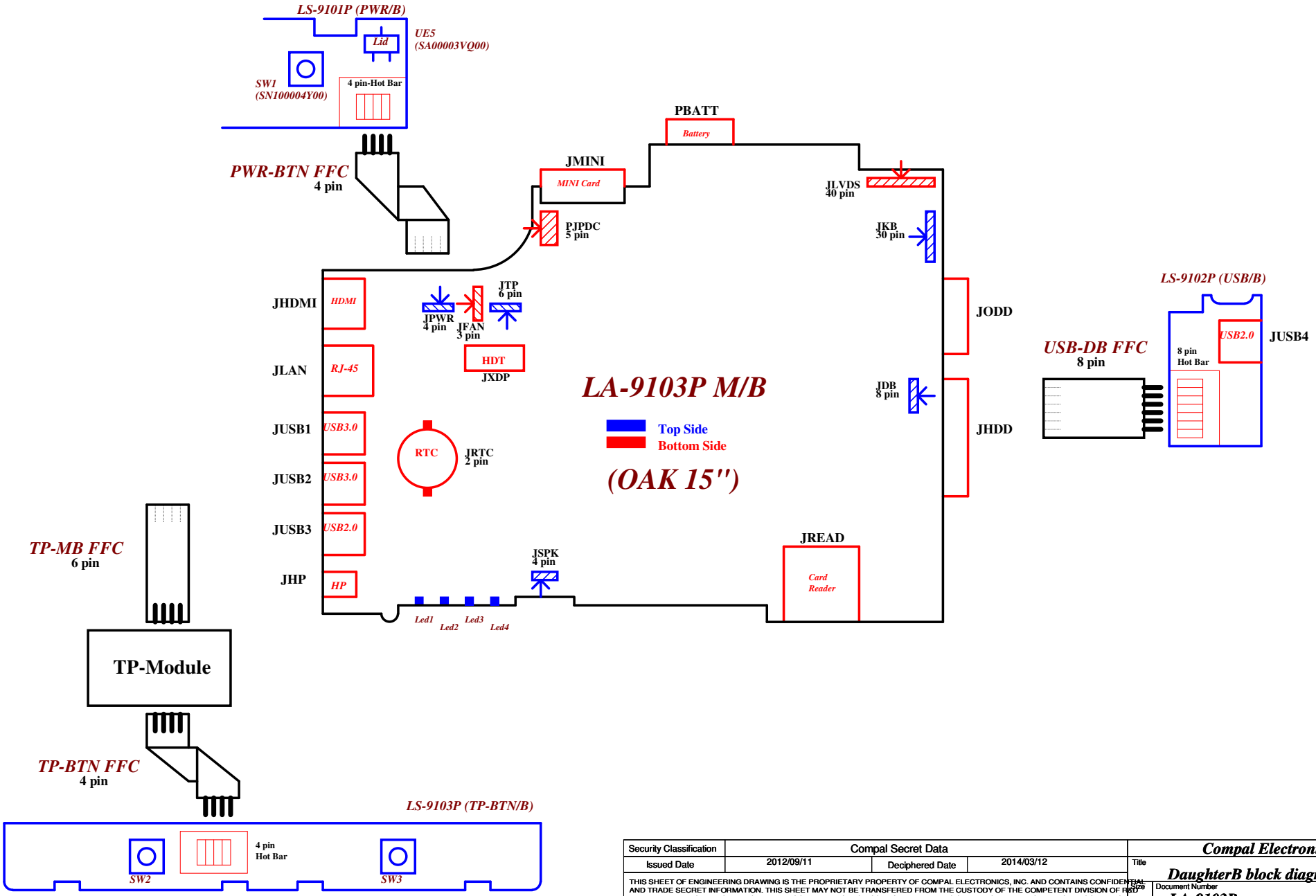


Security Classification	Compal Secret Data		
Issued Date	2012/09/11	Deciphered Date	2014/03/12

Compal Electronics, Inc.			
Title: Block diagram			
Size	Document Number: LA-9103P		Rev: 1.0
Date: Wednesday, July 10, 2013	Sheet 2 of 52		

Compal Confidential

Project Code : VAW03
File Name : LA-9103P



Security Classification	Compal Secret Data		
Issued Date	2012/09/11	Deciphered Date	2014/03/12

Compal Electronics, Inc.			
Title: DaughterB block diagram			
Size	Document Number: LA-9103P		Rev: 1.0
Date: Wednesday, July 10, 2013	Sheet 3 of 52		

Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

Board ID	PCB Revision	
0	0.1	
1	0.2	
2	0.3	
3	1.0	SD028330280
4		
5		
6		
7		

EC SM Bus1 address

Device	Address	HEX
Smart Battery	000 1011	11h 0x16
Charger IC	000 1001	09h 0x12

EC SM Bus2 address

Device	Address	HEX
ADM1032ARMZ	100 1101	4Dh 0x9A
SB-TSI	100 1100	4Ch 0x98
RTD2132	100 1010	4Ah 0x94
GPU	100 0001	41h 0x82

SM Bus Controller 0

(FCH_SMB1 ~ FCH_SMB4, SMB_ALERT#)

Device	Address	HEX
APU SIC/SID (FCH_SMB3)		

SM Bus Controller 1

(FCH_SMB0)

Device	Address	HEX
DDR DIMM1 (FCH_SMB0)	1001-000xb	90
DDR DIMM2 (FCH_SMB0)	1001-001xb	92
WLAN (FCH_SMB0)		

Symbol Note :

: means Digital Ground

: means Analog Ground

FCH	USB PORT#	DESTINATION
	0	USB conn.3 DEBUG PORT
	1	MINI CARD (WLAN)
	2	USB conn.4
	3	NC
	4	NC
	5	NC
	6	Card Reader
	7	NC
	8	NC
	9	Camera
	10	USB conn.2
	11	NC
	12	NC
	13	USB conn.1

CLK	DIFFERENTIAL	DESTINATION
	CLKOUT_PCIE0	None
	CLKOUT_PCIE1	None
	CLKOUT_PCIE2	10/100 LAN
	CLKOUT_PCIE3	MINI CARD WLAN
	CLKOUT_PCIE4	None
	CLKOUT_PCIE5	None
	CLKOUT_PCIE6	None
	CLKOUT_PCIE7	None
	CLKOUT_PEG_B	None

SATA	DESTINATION
SATA0	HDD
SATA1	ODD
SATA2	None
SATA3	None
SATA4	None
SATA5	None

PCI EXPRESS	DESTINATION
Lane 1	10/100 LAN
Lane 2	MINI CARD (WLAN)
Lane 3	None
Lane 4	None
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

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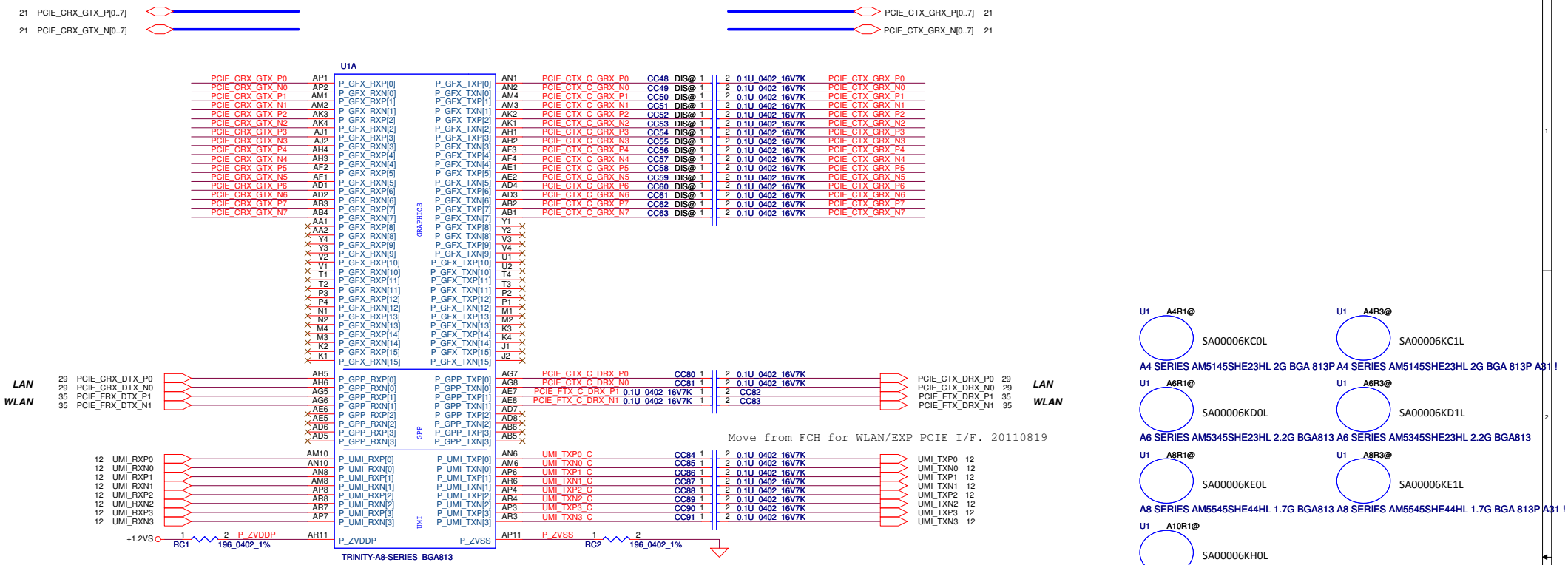
Title: Notes List

Size: Document Number: LA-9103P

Rev: 1.0

Date: Wednesday, July 10, 2013 Sheet 4 of 52



U1 A4R1@ SA00006KC0L
A4 SERIES AM5145SHE23HL 2G BGA 813P

U1 A4R3@ SA00006KC1L
A4 SERIES AM5145SHE23HL 2G BGA 813P A31 !

U1 A6R1@ SA00006KD0L
A6 SERIES AM5345SHE23HL 2.2G BGA813

U1 A6R3@ SA00006KD1L
A6 SERIES AM5345SHE23HL 2.2G BGA813

U1 A8R1@ SA00006KE0L
A8 SERIES AM5545SHE44HL 1.7G BGA813

U1 A8R3@ SA00006KE1L
A8 SERIES AM5545SHE44HL 1.7G BGA 813P A31 !

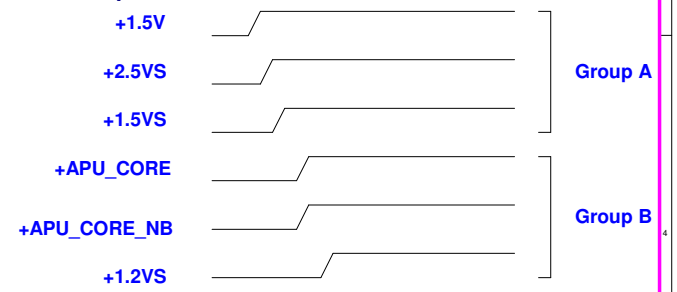
U1 A10R1@ SA00006KH0L
A10 SERIES AM5745SIE44HL 2.1G BGA 813P

ZZZ R1@
PCB 11R LA-A691P REV0 M/B 4
DA60012B000

ZZZ1 R3@
PCB VAW03 LA-9103P LS-9101P/9102P/9103P GOLD A31 !
DAZ0XO00101

Item	Material P/N	Model DELL PN	Description	Vender Contact Window
A4-5145M_Dual-Core,FP2(Group B),17W,Richland APU R1_ROH(Production)_HD 8310G	SA00006KC0L	VAW03	S IC A4 SERIES AM5145SHE23HL 2G BGA 813P	AMD
A4-5145M_Dual-Core,FP2(Group B),17W,Richland APU R3_ROH(Production)_HD 8310G	SA00006KC1L	8C6MV	S IC A4 SERIES AM5145SHE23HL 2G BGA 813P A31 !	AMD
A6-5345M_Dual-Core,FP2(Group B),17W,Richland APU R1_ROH(Production)_HD 8410G	SA00006KD0L	VAW03	S IC A6 SERIES AM5345SHE23HL 2.2G BGA 813P	AMD
A6-5345M_Dual-Core,FP2(Group B),17W,Richland APU R3_ROH(Production)_HD 8410G	SA00006KD1L	VGDH2	S IC A6 SERIES AM5345SHE23HL 2.2G BGA 813P A31 !	AMD
A8-5545M_Quad-Core,FP2(Group B),19W,Richland APU R1_ROH(Production)_HD 8510G	SA00006KE0L	VAW03	S IC A8 SERIES AM5545SHE44HL 1.7G BGA 813P	AMD
A8-5545M_Quad-Core,FP2(Group B),19W,Richland APU R3_ROH(Production)_HD 8510G	SA00006KE1L	Y53MJ	S IC A8 SERIES AM5545SHE44HL 1.7G BGA 813P A31 !	AMD
A10-5745M_Quad-Core,FP2(Group B),25W,Richland APU R1_ROH(Production)_HD 8610G	SA00006KH0L	VAW03	S IC A10 SERIES AM5745SIE44HL 2.1G BGA 813P	AMD
A10-5745M_Quad-Core,FP2(Group B),25W,Richland APU R3_ROH(Production)_HD 8610G		缺 DPN		AMD

Power Sequence of APU



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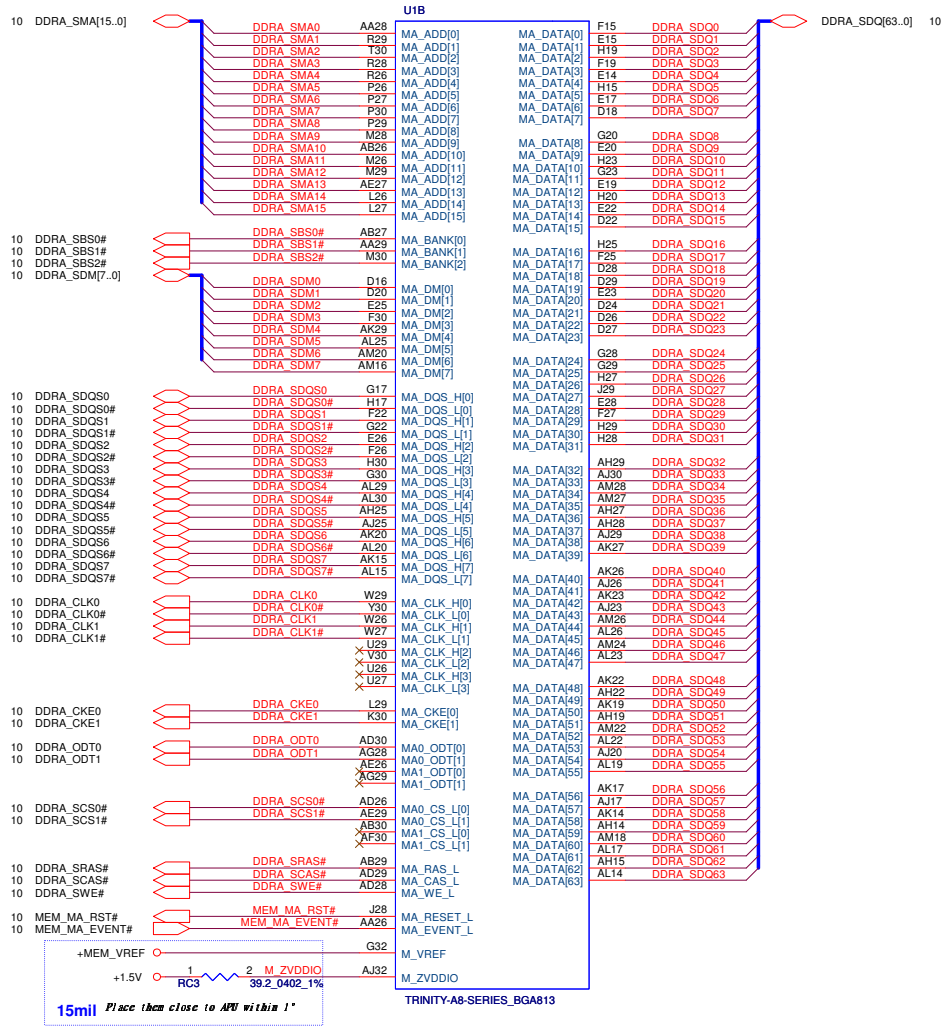
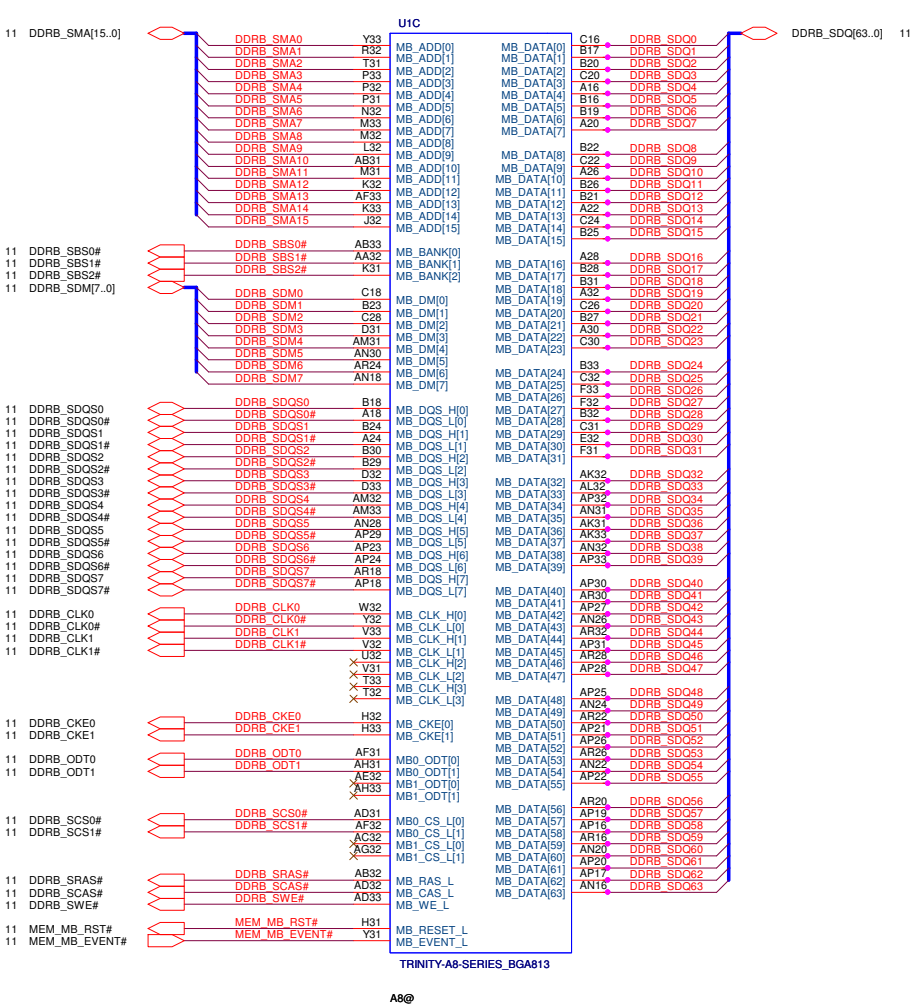
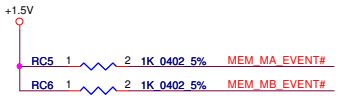
Issued Date	2012/09/11	Deciphered Date	2014/03/12
Title	FP2 PCIE/UMI		
Size Custom	Document Number LA-9103P		Rev 1.0
Date: Wednesday, July 10, 2013	Sheet 5 of 52		

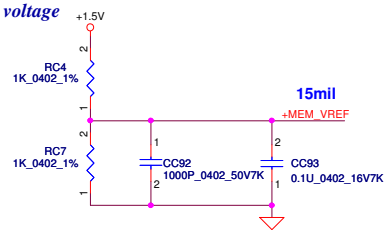




EVENT# pull high

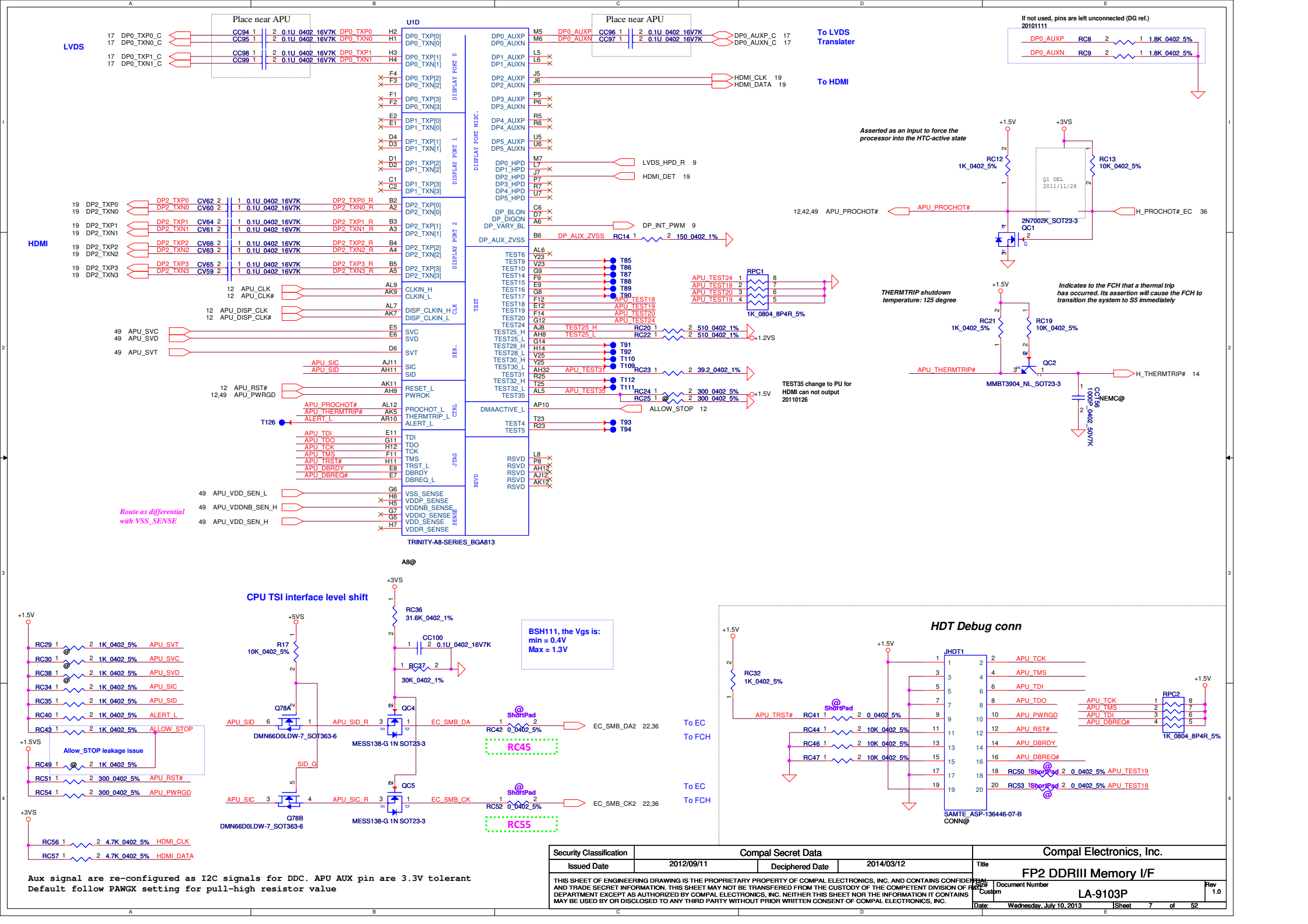


0.75V reference voltage



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/09/11	Deciphered Date 2014/03/12	Title: FP2 DDRIII Memory I/F

Size: Custom	Document Number: LA-9103P		Rev: 1.0
Date: Wednesday, July 10, 2013	Sheet 6 of 52		



Security Classification	Compal Secret Data		
Issued Date	2012/09/11	Deciphered Date	2014/03/12

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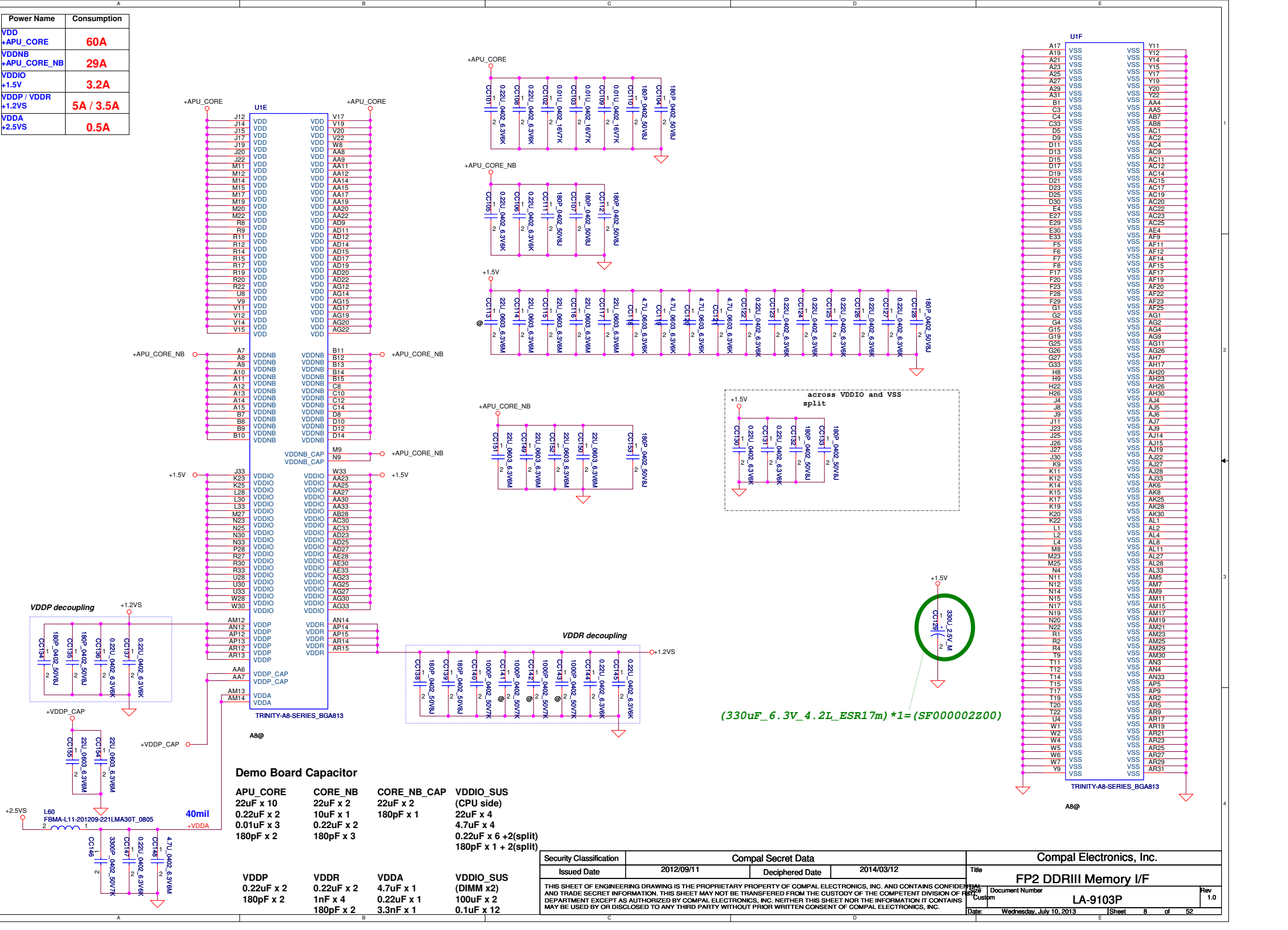
Compal Electronics, Inc.

Title: FP2 DDRIII Memory I/F

Size: Custom | Document Number: LA-9103P | Rev: 1.0

Date: Wednesday, July 10, 2013 | Sheet 7 of 52

Power Name	Consumption
VDD +APU_CORE	60A
VDDNB +APU_CORE_NB	29A
VDDIO +1.5V	3.2A
VDDP / VDDR +1.2VS	5A / 3.5A
VDDA +2.5VS	0.5A



Demo Board Capacitor

APU_CORE	CORE_NB	CORE_NB_CAP	VDDIO_SUS
22uF x 10	22uF x 2	22uF x 2	(CPU side)
0.22uF x 2	10uF x 1	180pF x 1	22uF x 4
0.01uF x 3	0.22uF x 2		4.7uF x 4
180pF x 2	180pF x 3		0.22uF x 6 +2(split)
			180pF x 1 + 2(split)

VDDP	VDDR	VDDA	VDDIO_SUS
0.22uF x 2	0.22uF x 2	4.7uF x 1	(DIMM x2)
180pF x 2	1nF x 4	0.22uF x 1	100uF x 2
	180pF x 2	3.3nF x 1	0.1uF x 12

Security Classification	Compal Secret Data		
Issued Date	2012/09/11	Deciphered Date	2014/03/12

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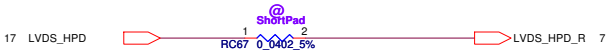
Title: FP2 DDRIII Memory I/F

Size: Custom | Document Number: LA-9103P | Rev: 1.0

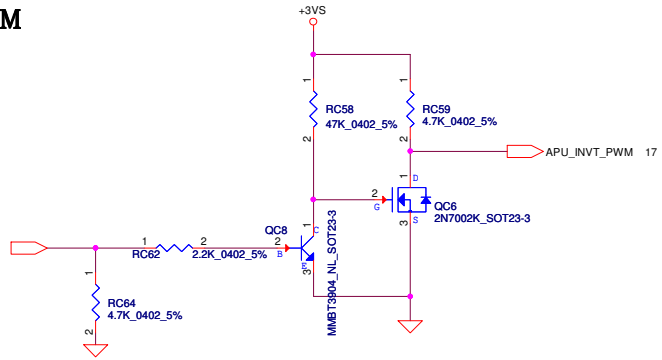
Date: Wednesday, July 10, 2013 | Sheet 8 of 52

HPD

Translator HPD



Panel PWM



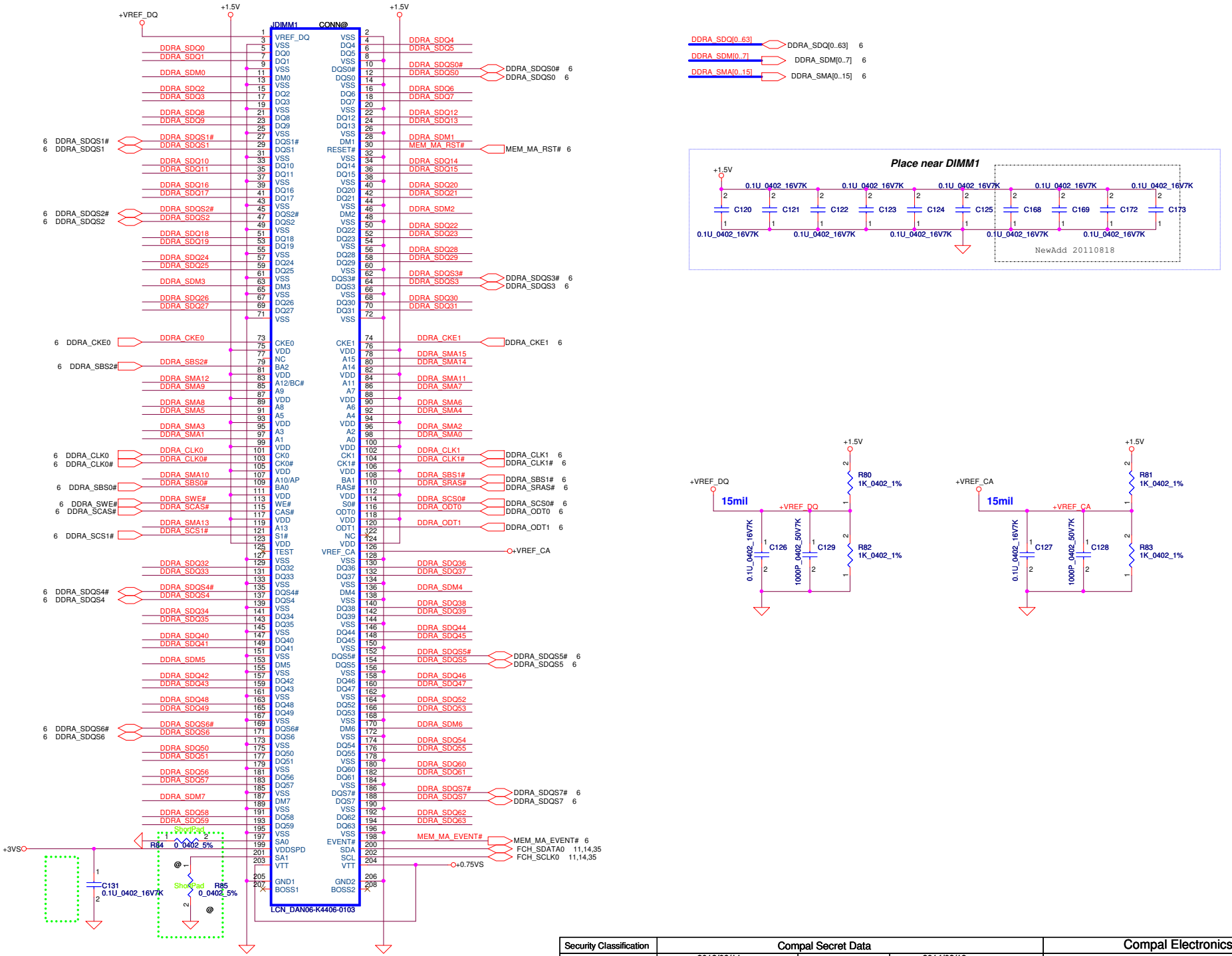
Security Classification	Compal Secret Data		
Issued Date	2012/09/11	Deciphered Date	2014/03/12

Compal Electronics, Inc.

Title: FP2 DDRIII Memory I/F

Size	Document Number	Rev
Custom	LA-9103P	1.0

Date: Wednesday, July 10, 2013 Sheet 9 of 52



DDRA_SDQ[0..63] → DDRA_SDQ[0..63] 6
DDRA_SDM[0..7] → DDRA_SDM[0..7] 6
DDRA_SMA[0..15] → DDRA_SMA[0..15] 6

Reverse H:4mm

<Address: 00>

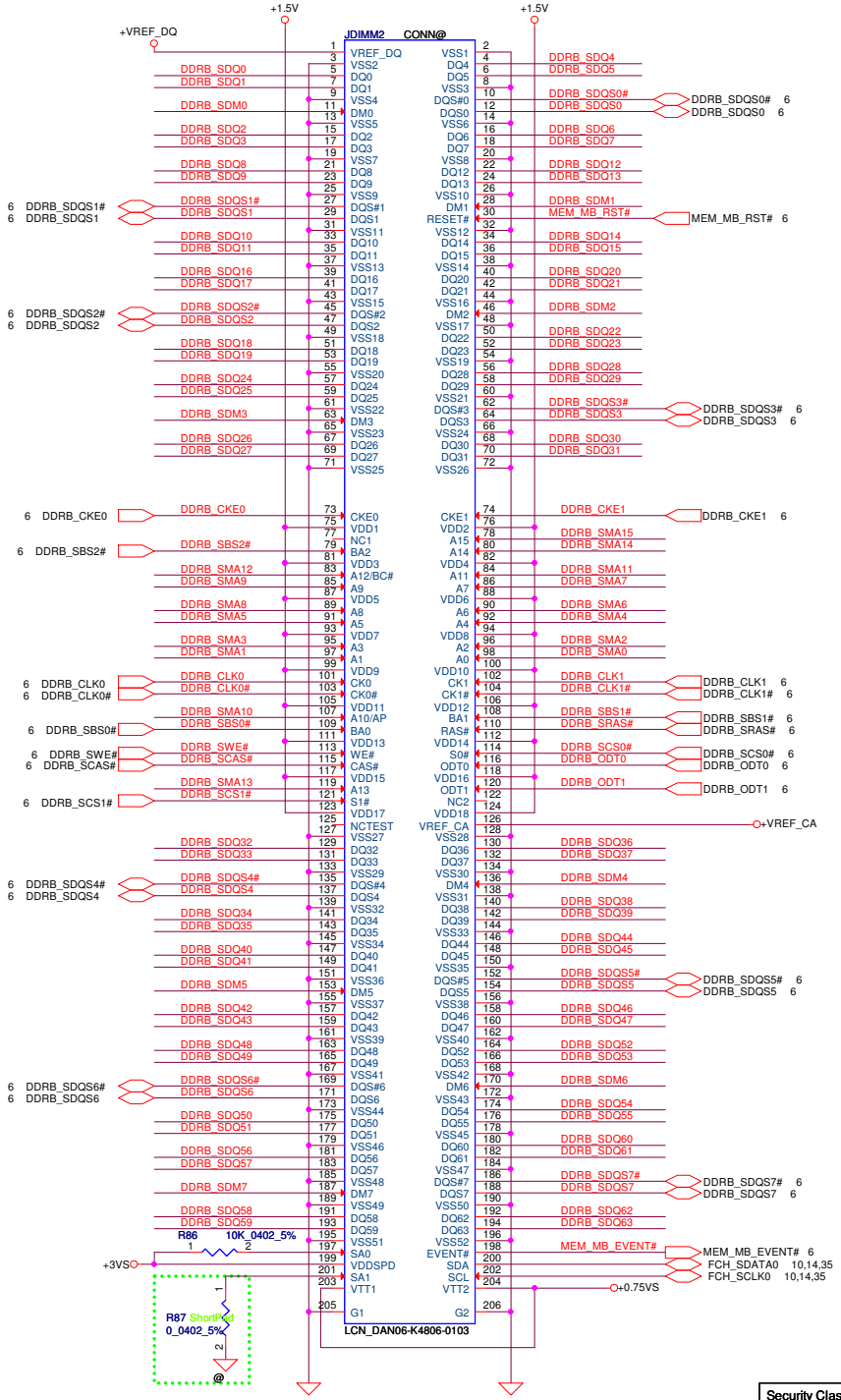
Security Classification	Compal Secret Data		
Issued Date	2012/09/11	Deciphered Date	2014/03/12

Compal Electronics, Inc.

Title: DDRIII SO-DIMM 1

Size	Document Number	Rev
Custom	LA-9103P	1.0

Date: Wednesday, July 10, 2013 | Sheet 10 of 52



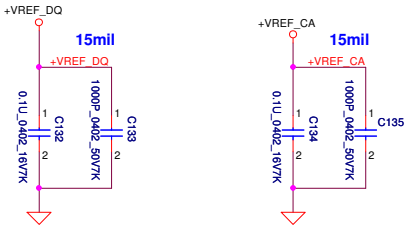
Reserve H:8mm

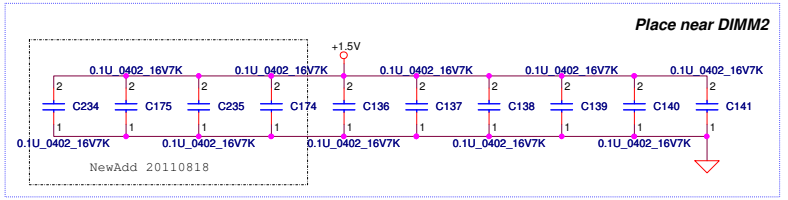
<Address: 01>

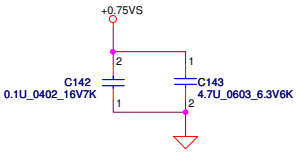
DDRB_SDQ[0..63] — DDRB_SDQ[0..63] 6

DDRB_SDM[0..7] — DDRB_SDM[0..7] 6

DDRB_SMA[0..15] — DDRB_SMA[0..15] 6







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Issued Date	2012/09/11	Deciphered Date 2014/03/12	Title: DDRIII SO-DIMM 2
Size: Custom	Document Number: LA-9103P		Rev: 1.0
Date: Wednesday, July 10, 2013	Sheet 11 of 52		

R90/ C146 close to FCH

Move PCIE device to APU. 20110819

SS

NSS

SS

APU DISP

APU

VGA

WLAN

LAN

For "EXT" CLK mode, input to PCIE,

For PCIE device reset on FS1 (GFX,GLAN,WLAN,LVDS Travis)

APU_PCIE_RST #: Reset PCIE device on APU

R692/ C790 close to FCH

CLOSE TO X1

CLOSE TO Y1

Close to HUDSON-M2/3

for Clear CMOS

APU_PG/APU_RST#/LDT_STP# : OD pin
DMA_ACTIVE# : IN/OD, 0.8V threshold
PROCHOT# : IN, 0.8V threshold
LDT_STP : No use, NC
DMA active. The FCH drives the DMA_ACTIVE# to APU to notify DMA activity. This will cause the APU to reestablish the UMI link quicker.

218-0844012 A1 BOLTON-M3 FCH 0FD

218-0844012 A1 BOLTON-M3 FCH A31!

21807-A13-HUDSON-M3_FCBGA656
Hud@

QCL10 LAN-APU,WLAN&ExCARD-FCH 20110803

Security Classification	Compal Secret Data		
Issued Date	2012/09/11	Deciphered Date	2014/03/12

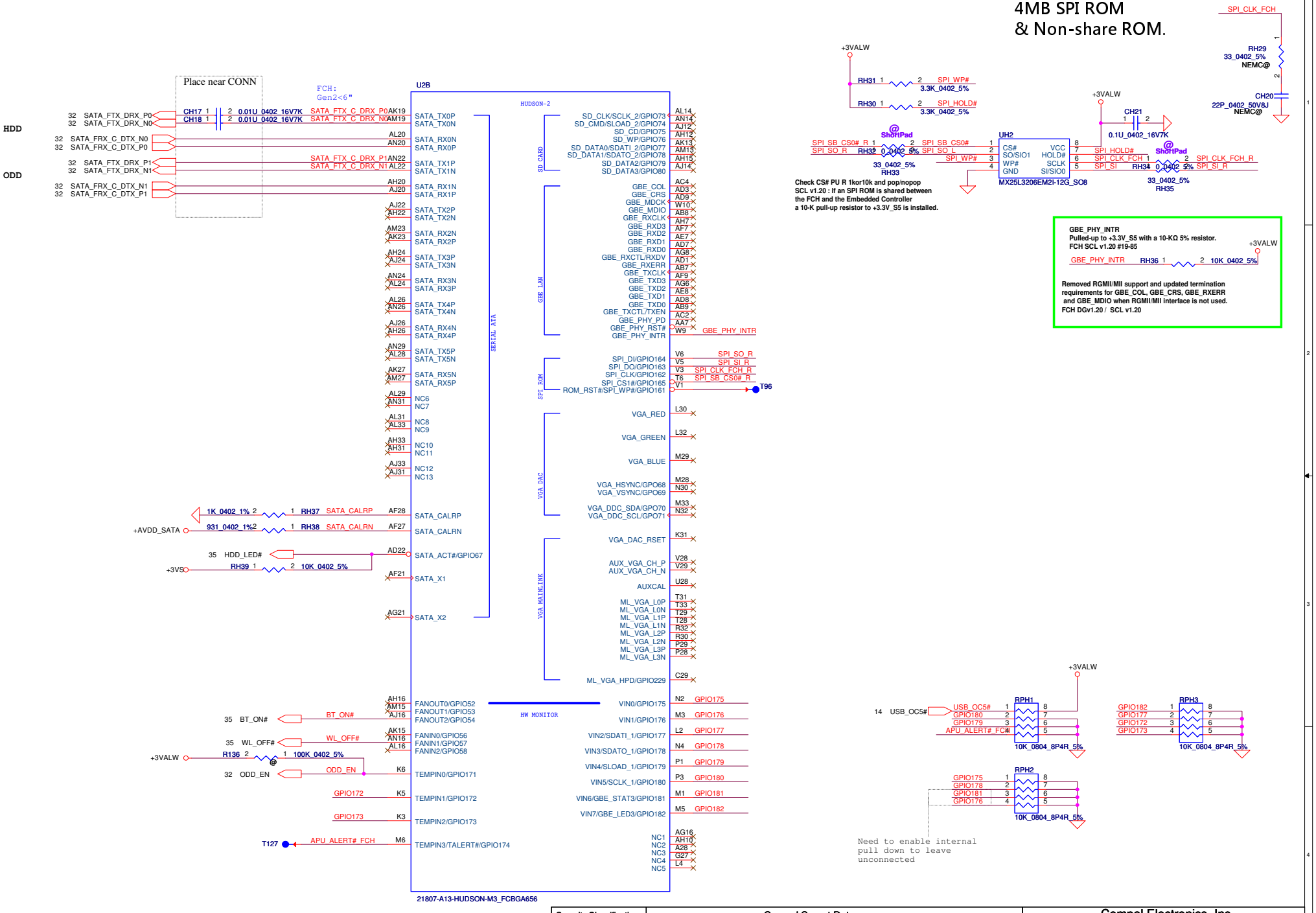
Compal Electronics, Inc.

Title: FCH PCIE/CLK/PCI/LPC/RTC

Size: Custom | Document Number: LA-9103P | Rev: 1.0

Date: Wednesday, July 10, 2013 | Sheet 12 of 52

4MB SPI ROM & Non-share ROM.



Check CS# PU R 1kor10k and pop/nopop
SCL v1.20 : If an SPI ROM is shared between the FCH and the Embedded Controller a 10-K pull-up resistor to +3.3V_S5 is installed.

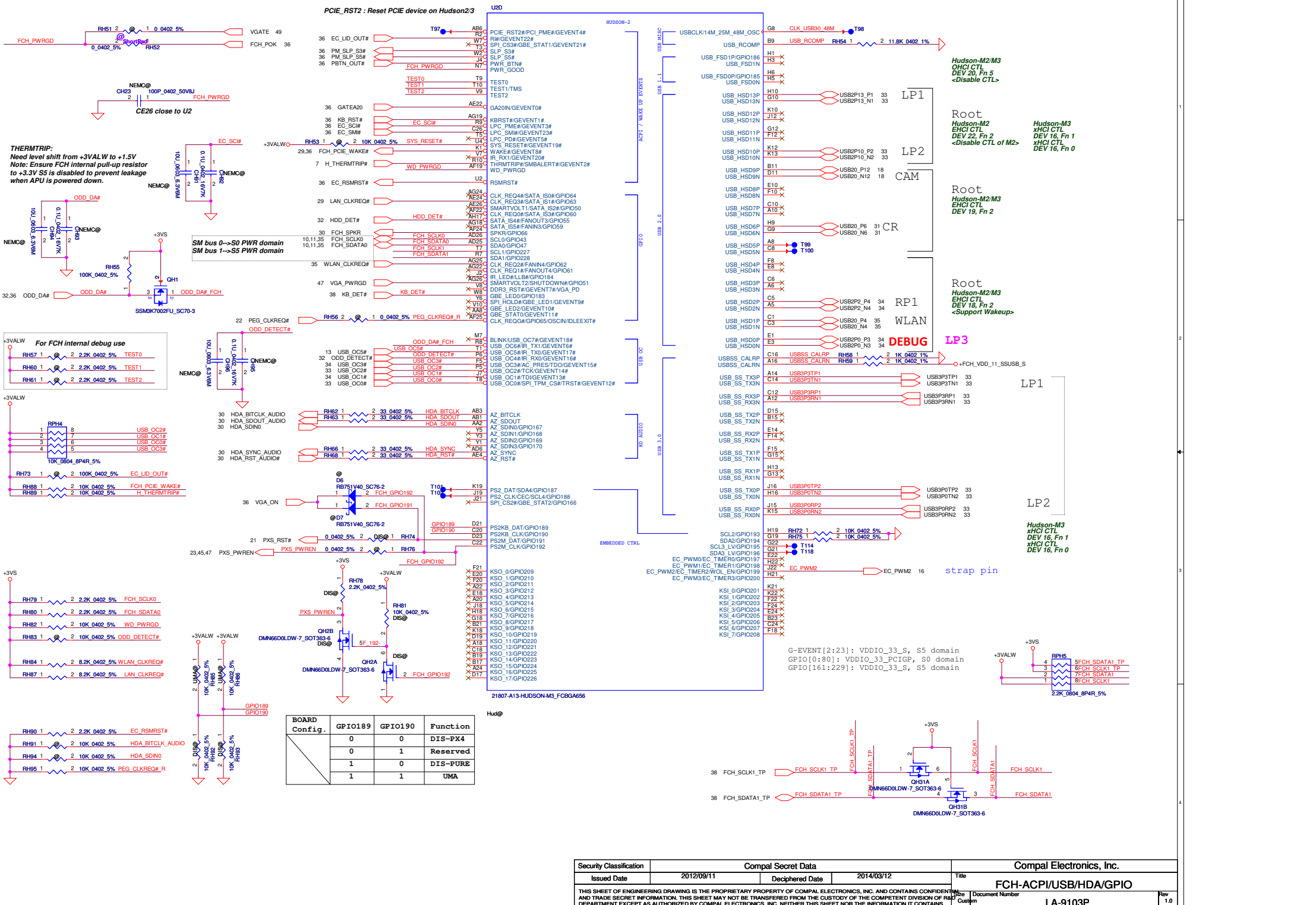
GBE_PHY_INTR
Pulled-up to +3.3V_S5 with a 10-KΩ 5% resistor.
FCH SCL v1.20 #19-85

Removed RGMII/MII support and updated termination requirements for GBE_COL, GBE_CRS, GBE_RXERR and GBE_MDIO when RGMII/MII interface is not used.
FCH DGv1.20 / SCL v1.20

Need to enable internal pull down to leave unconnected

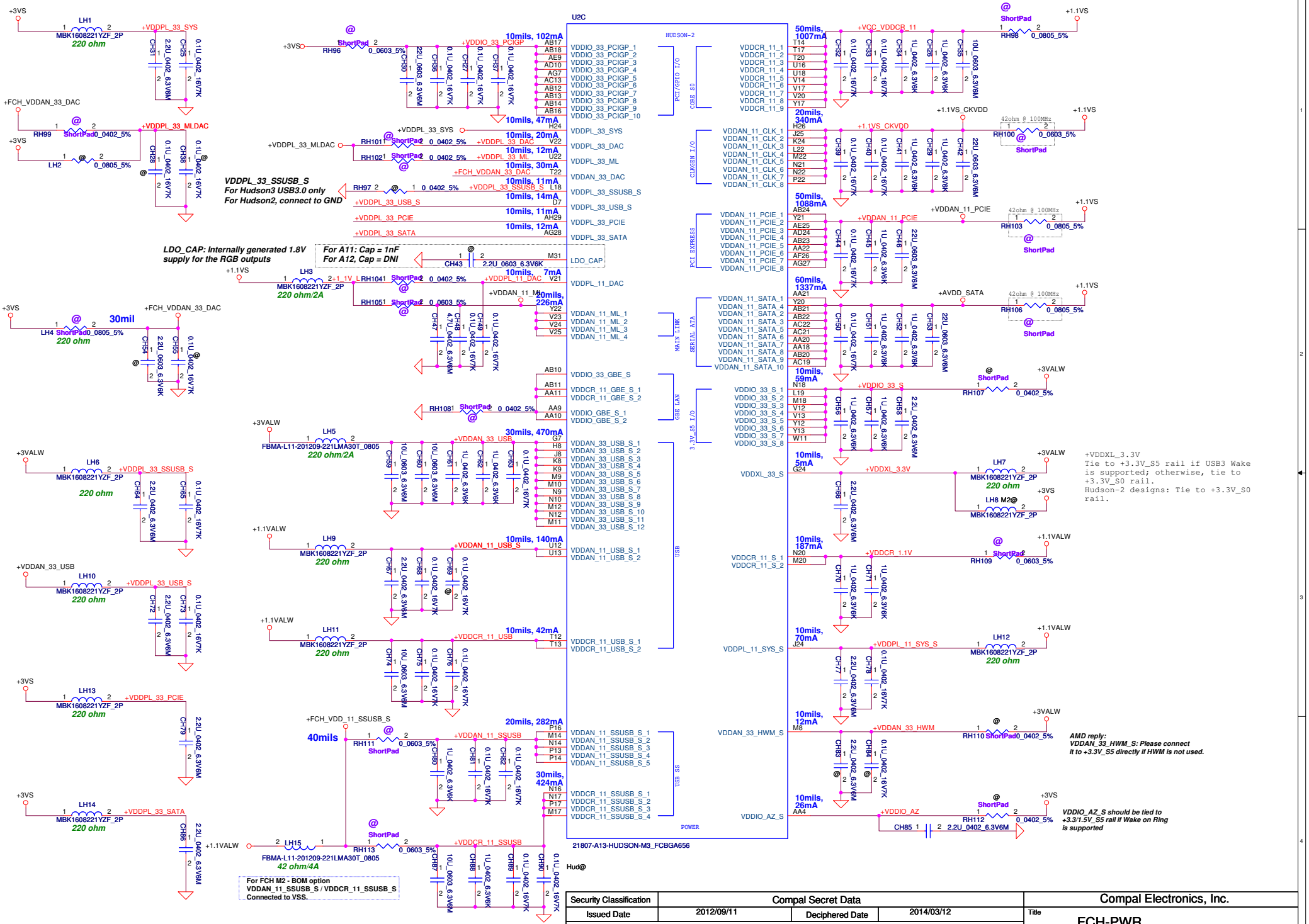
Security Classification	Compal Secret Data		
Issued Date	2012/09/11	Deciphered Date	2014/03/12

Compal Electronics, Inc.			
Title	FCH SATA/SPI/VGA/HWM/SD		
Size: Custom	Document Number: LA-9103P		Rev: 1.0
Date: Wednesday, July 10, 2013	Sheet 13 of 52		



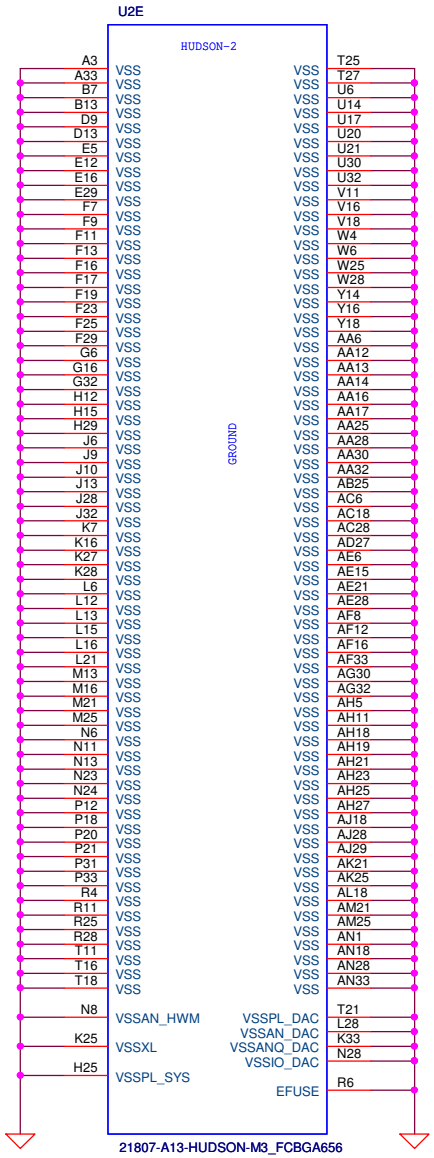
Security Classification	Compal Secret Data		
Issued Date	2012/09/11	Deciphered Date	2014/03/12

Compal Electronics, Inc.			
Title: FCH-ACPI/USB/HDA/GPIO			
Size: Custom	Document Number: LA-9103P		Rev: 1.0
Date: Wednesday, July 10, 2013	Sheet 14 of 52		



Security Classification	Compal Secret Data		
Issued Date	2012/09/11	Deciphered Date	2014/03/12

Compal Electronics, Inc.			
Title: FCH-PWR			
Size: Custom	Document Number: LA-9103P		Rev: 1.0
Date: Wednesday, July 10, 2013	Sheet 15 of 52		



Hud@

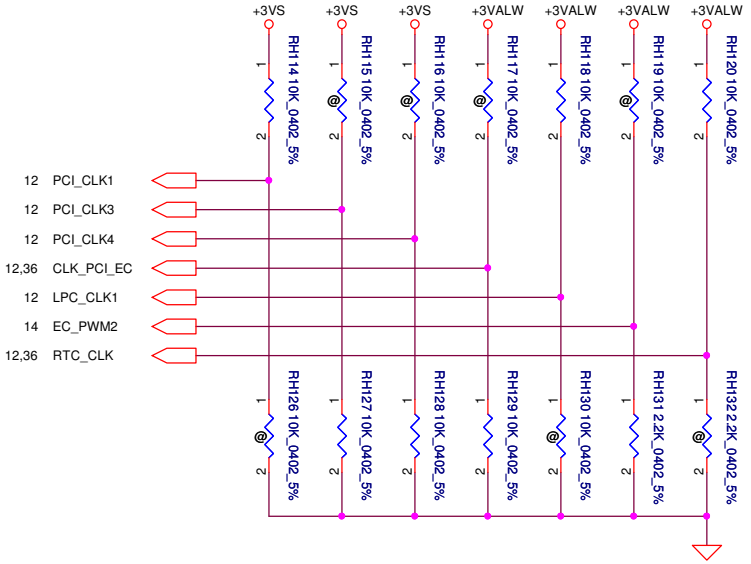
STRAP PINS

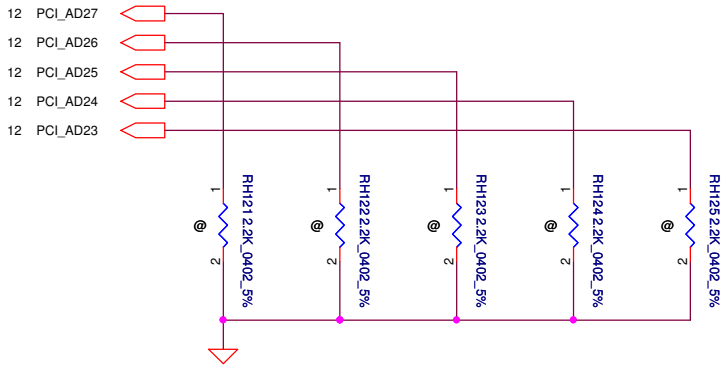
	PCI_CLK1	PCI_CLK3	PCI_CLK4	CLK_PCI_EC	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

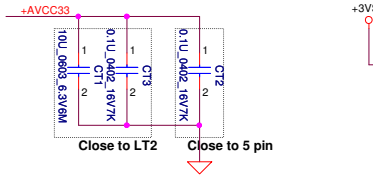


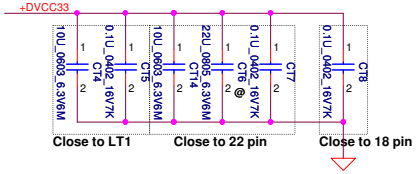


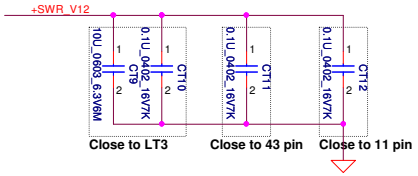
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/09/11	Deciphered Date 2014/03/12	Title: FCH-VSS/Strap
			Size: B; Document Number: LA-9103P; Rev: 1.0
			Date: Wednesday, July 10, 2013; Sheet 16 of 52

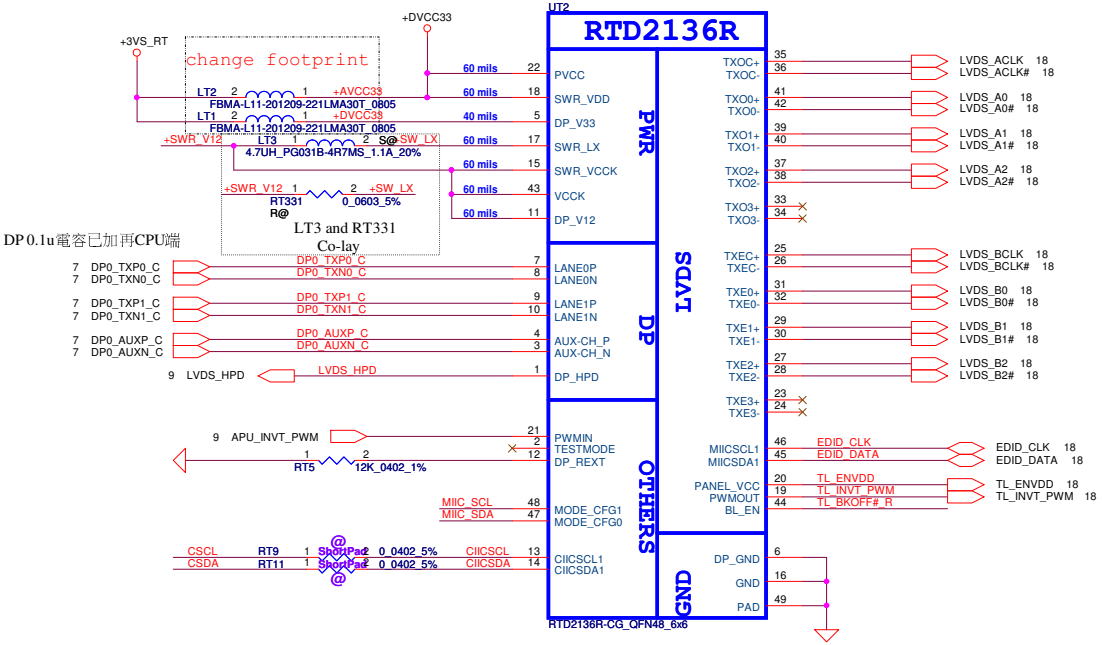
Power Consumption:

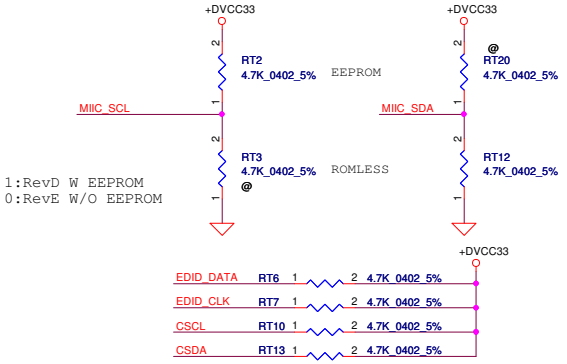
Pin22 (DPV33) < 20mA
Pin 11 (DP_V12) < 100mA
Pin 15 (SWR_VCCK) < 100mA (layout trace > 60 mil)
Pin 17 (SWR_LX) < 600mA (layout trace > 60 mil)
Pin 18 (SWR_VDD) < 200mA (layout trace > 40 mil)
Pin 22 (PVCC) < 50 mA
Pin 43 (VCCK) < 50mA



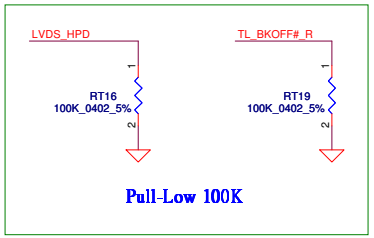


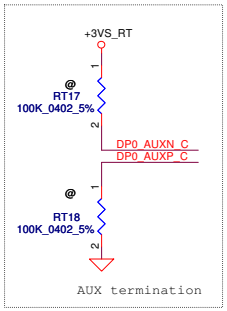


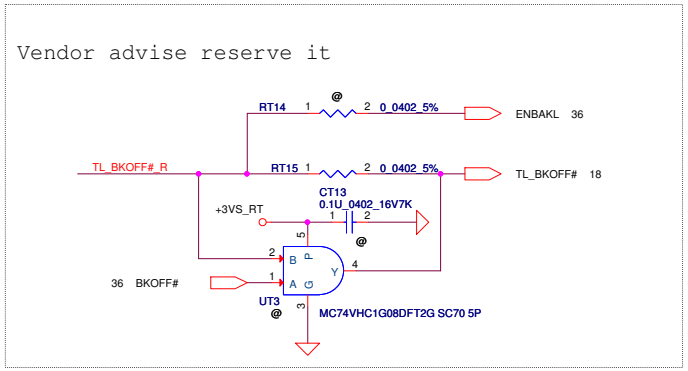


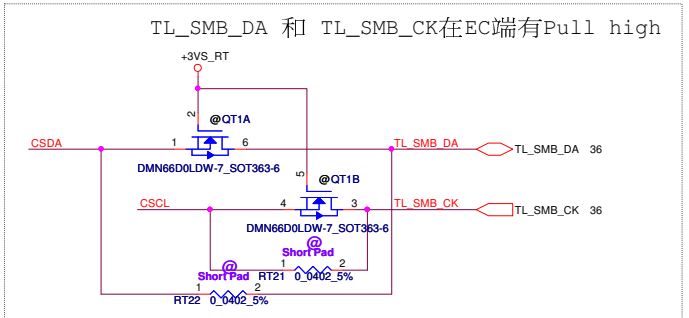


		Pin47 MIIC_SDA	
		0	1
Pin48 MIIC_SCL	0	x	EP MODE
	1	ROM	EEPROM



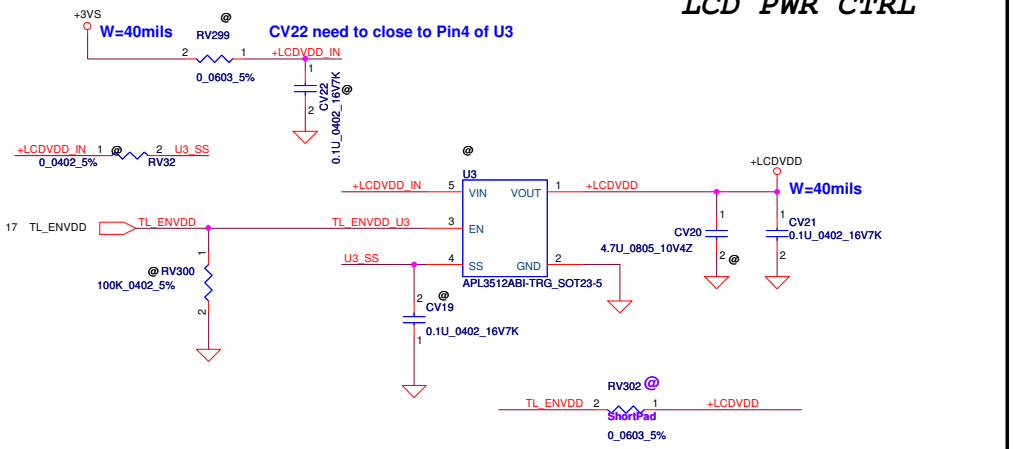




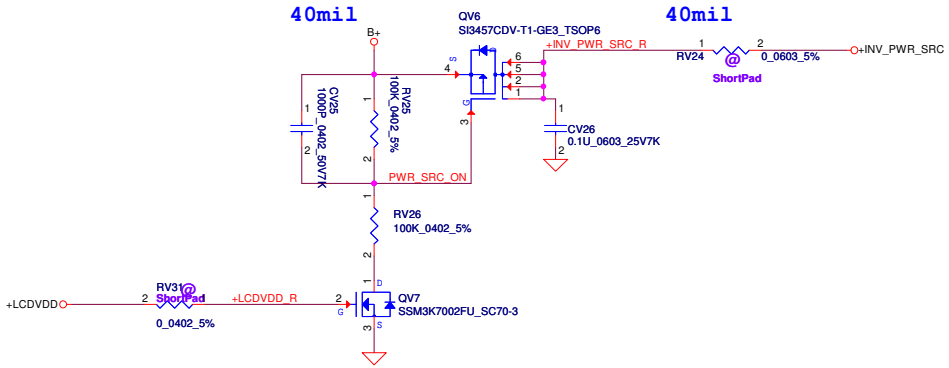


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/09/11	Deciphered Date 2014/03/12	Title: LVDS Translator - RTD2132R
			Size: Custom; Document Number: LA-9103P; Rev: 1.0
			Date: Wednesday, July 10, 2013; Sheet 17 of 52

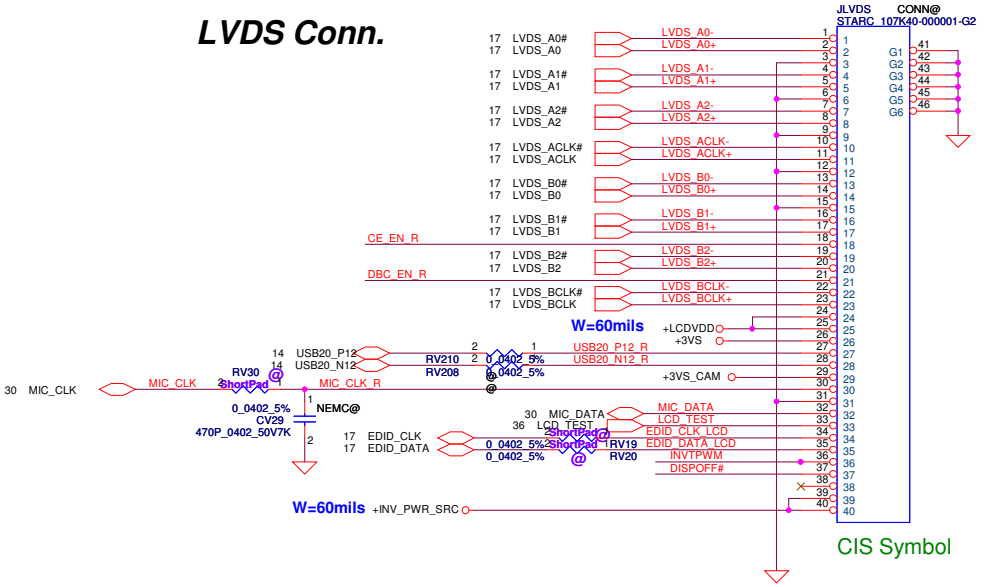
LCD PWR CTRL



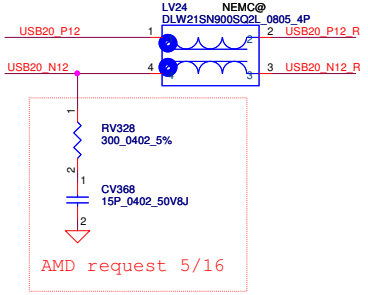
LCD backlight PWR CTRL

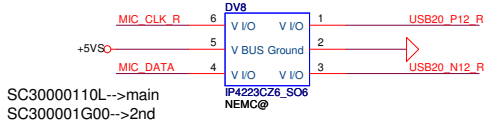


LVDS Conn.

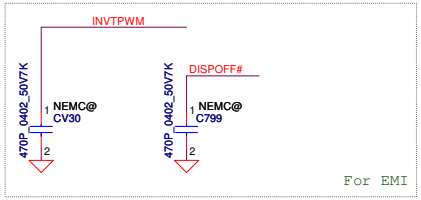


* Reserved for EMI/ESD/RF need to close to JLVDS

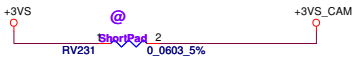


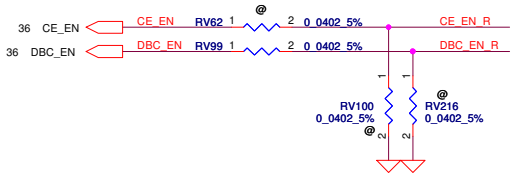


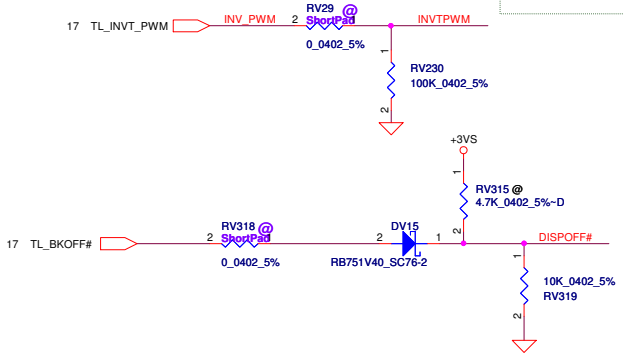
SC30000110L-->main
SC300001G00-->2nd



Wedcam PWR CTRL



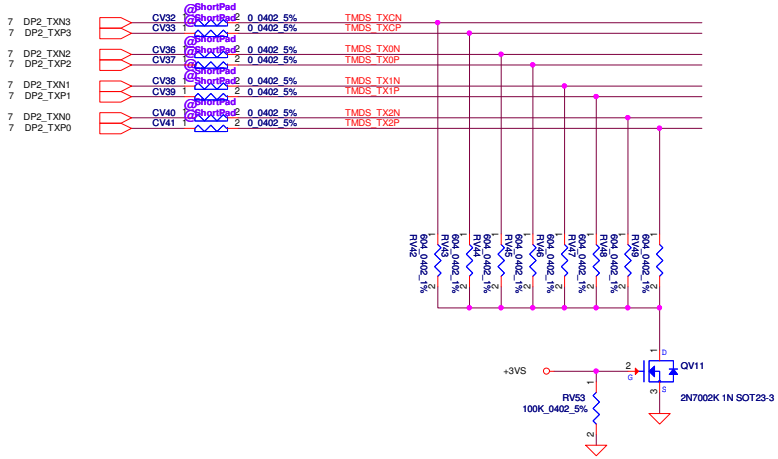


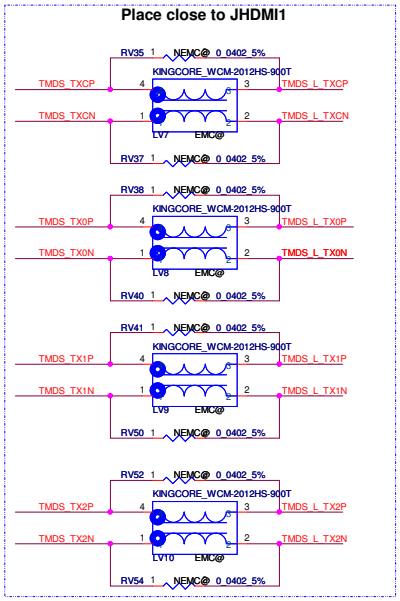


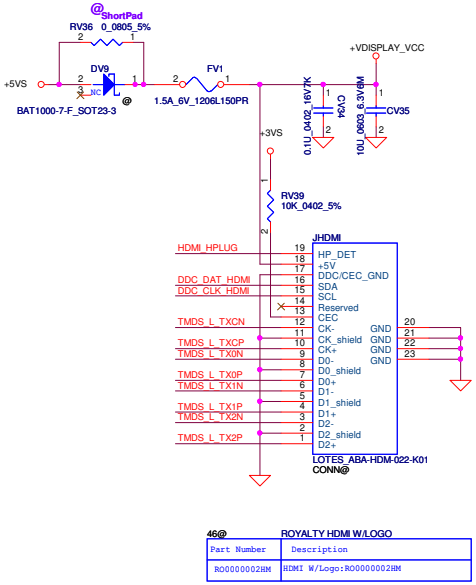
Security Classification	Compal Secret Data		
Issued Date	2012/09/11	Deciphered Date	2014/03/12

Compal Electronics, Inc.			
Title	LVDS/CAMERA		
Size B	Document Number LA-9103P		Rev 1.0
Date: Wednesday, July 10, 2013	Sheet 18 of 52		

W=40mils

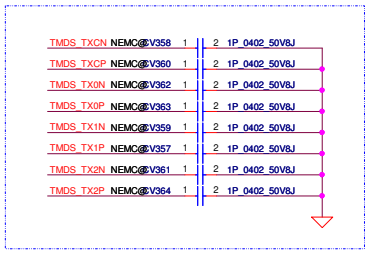


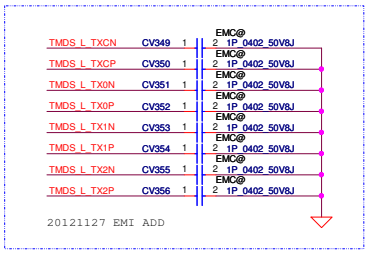


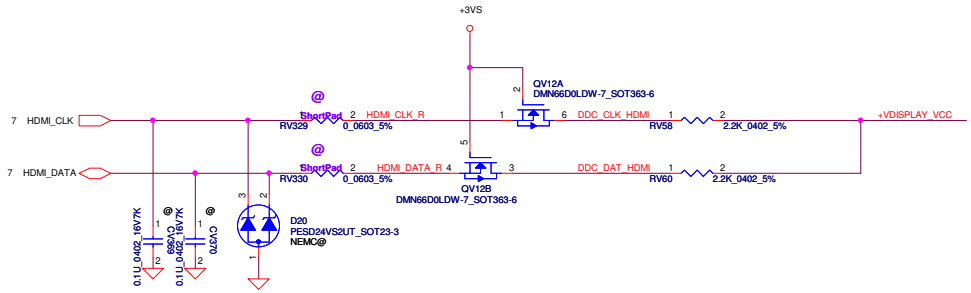


46@ ROYALTY HDMI W/LOGO

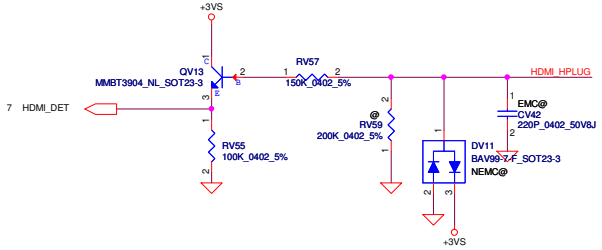
Part Number	Description
RO0000002HM	HDMI W/Logo:RO0000002HM







CV365, CV367
Please close APU side



Security Classification	Compal Secret Data		
Issued Date	2012/09/11	Deciphered Date	2014/03/12

Compal Electronics, Inc.

Title: HDMI

Size | Document Number: LA-9103P | Rev: 1.0

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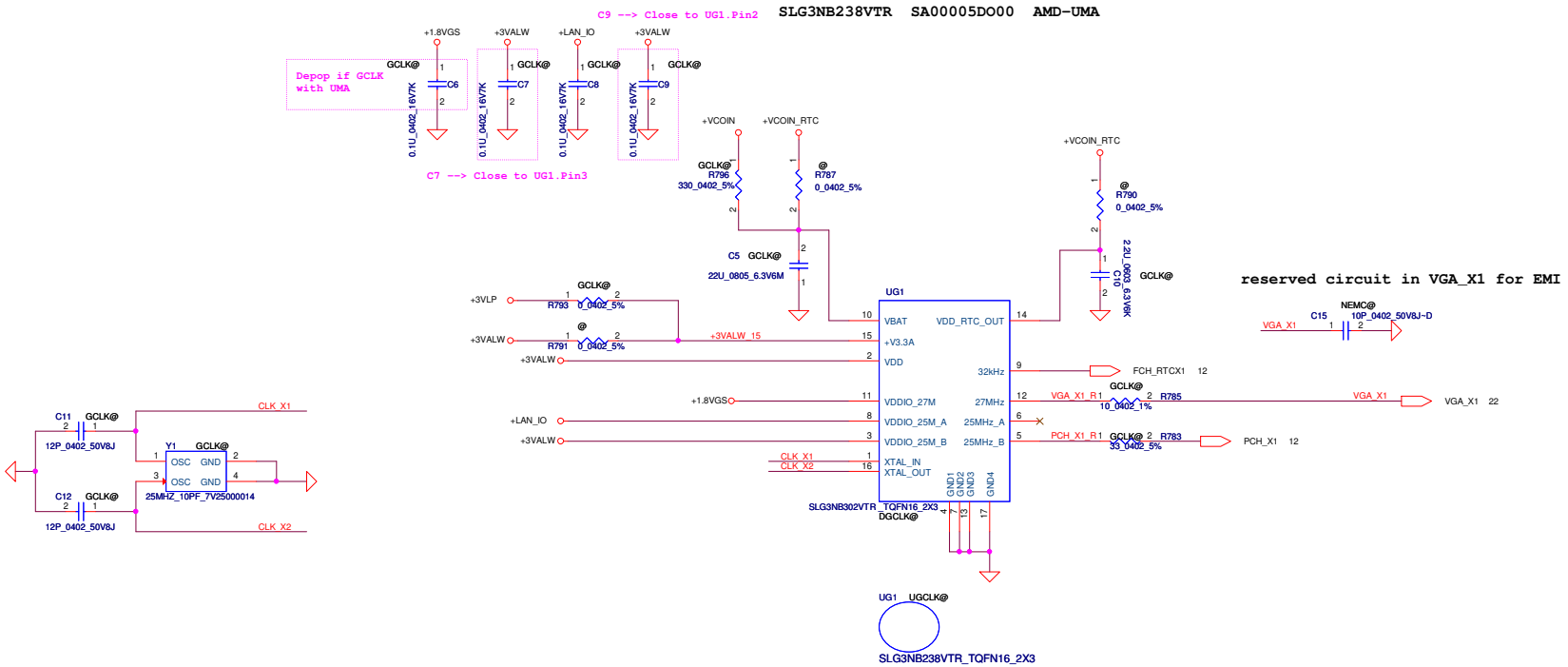
SLG3NB244VTR SA000057I00 Intel-UMA
SLG3NB300VTR SA00005RS00 Intel-DIS
SLG3NB302VTR SA00006D500 AMD-DIS
SLG3NB238VTR SA00005DO00 AMD-UMA



Security Classification	Compal Secret Data		
Issued Date	2012/09/11	Deciphered Date	2014/03/12

Compal Electronics, Inc.

Title: GCLK

Size | Document Number: LA-9103P | Rev: 1.0

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5 PCIE_CTX_GRX_P[7..0] PCIE_CTX_GRX_P[7..0]
5 PCIE_CTX_GRX_N[7..0] PCIE_CTX_GRX_N[7..0]

PCIE_CRX_GTX_P[7..0] PCIE_CRX_GTX_P[7..0] 5
PCIE_CRX_GTX_N[7..0] PCIE_CRX_GTX_N[7..0] 5

GFX PCIE LANE REVERSAL

UV1A

PCI EXPRESS INTERFACE

PCIE_CTX_GRX_P0	AA38	PCIE_RX0P	PCIE_TX0P	Y33	PCIE_CRX_C_GTX_P0	0.1U_0402_16V7K	2	1	CV43	DIS@	PCIE_CRX_GTX_P0
PCIE_CTX_GRX_N0	Y37	PCIE_RX0N	PCIE_TX0N	Y32	PCIE_CRX_C_GTX_N0	0.1U_0402_16V7K	2	1	CV44	DIS@	PCIE_CRX_GTX_N0
PCIE_CTX_GRX_P1	Y35	PCIE_RX1P	PCIE_TX1P	W33	PCIE_CRX_C_GTX_P1	0.1U_0402_16V7K	2	1	CV45	DIS@	PCIE_CRX_GTX_P1
PCIE_CTX_GRX_N1	W36	PCIE_RX1N	PCIE_TX1N	W32	PCIE_CRX_C_GTX_N1	0.1U_0402_16V7K	2	1	CV46	DIS@	PCIE_CRX_GTX_N1
PCIE_CTX_GRX_P2	W38	PCIE_RX2P	PCIE_TX2P	U33	PCIE_CRX_C_GTX_P2	0.1U_0402_16V7K	2	1	CV47	DIS@	PCIE_CRX_GTX_P2
PCIE_CTX_GRX_N2	V37	PCIE_RX2N	PCIE_TX2N	U32	PCIE_CRX_C_GTX_N2	0.1U_0402_16V7K	2	1	CV48	DIS@	PCIE_CRX_GTX_N2
PCIE_CTX_GRX_P3	V35	PCIE_RX3P	PCIE_TX3P	U30	PCIE_CRX_C_GTX_P3	0.1U_0402_16V7K	2	1	CV49	DIS@	PCIE_CRX_GTX_P3
PCIE_CTX_GRX_N3	U36	PCIE_RX3N	PCIE_TX3N	U29	PCIE_CRX_C_GTX_N3	0.1U_0402_16V7K	2	1	CV50	DIS@	PCIE_CRX_GTX_N3
PCIE_CTX_GRX_P4	U38	PCIE_RX4P	PCIE_TX4P	T33	PCIE_CRX_C_GTX_P4	0.1U_0402_16V7K	2	1	CV51	DIS@	PCIE_CRX_GTX_P4
PCIE_CTX_GRX_N4	T37	PCIE_RX4N	PCIE_TX4N	T32	PCIE_CRX_C_GTX_N4	0.1U_0402_16V7K	2	1	CV52	DIS@	PCIE_CRX_GTX_N4
PCIE_CTX_GRX_P5	T35	PCIE_RX5P	PCIE_TX5P	T30	PCIE_CRX_C_GTX_P5	0.1U_0402_16V7K	2	1	CV53	DIS@	PCIE_CRX_GTX_P5
PCIE_CTX_GRX_N5	R36	PCIE_RX5N	PCIE_TX5N	T29	PCIE_CRX_C_GTX_N5	0.1U_0402_16V7K	2	1	CV54	DIS@	PCIE_CRX_GTX_N5
PCIE_CTX_GRX_P6	R38	PCIE_RX6P	PCIE_TX6P	P33	PCIE_CRX_C_GTX_P6	0.1U_0402_16V7K	2	1	CV55	DIS@	PCIE_CRX_GTX_P6
PCIE_CTX_GRX_N6	P37	PCIE_RX6N	PCIE_TX6N	P32	PCIE_CRX_C_GTX_N6	0.1U_0402_16V7K	2	1	CV56	DIS@	PCIE_CRX_GTX_N6
PCIE_CTX_GRX_P7	P35	PCIE_RX7P	PCIE_TX7P	P30	PCIE_CRX_C_GTX_P7	0.1U_0402_16V7K	2	1	CV57	DIS@	PCIE_CRX_GTX_P7
PCIE_CTX_GRX_N7	N36	PCIE_RX7N	PCIE_TX7N	P29	PCIE_CRX_C_GTX_N7	0.1U_0402_16V7K	2	1	CV58	DIS@	PCIE_CRX_GTX_N7
	N38	PCIE_RX8P	PCIE_TX8P	N33							
	M37	PCIE_RX8N	PCIE_TX8N	N32							
	M35	PCIE_RX9P	PCIE_TX9P	N30							
	L36	PCIE_RX9N	PCIE_TX9N	N29							
	L38	PCIE_RX10P	PCIE_TX10P	L33							
	K37	PCIE_RX10N	PCIE_TX10N	L32							
	K35	PCIE_RX11P	PCIE_TX11P	L30							
	J36	PCIE_RX11N	PCIE_TX11N	L29							
	J38	PCIE_RX12P	PCIE_TX12P	K33							
	H37	PCIE_RX12N	PCIE_TX12N	K32							
	H35	PCIE_RX13P	PCIE_TX13P	J33							
	G36	PCIE_RX13N	PCIE_TX13N	J32							
	G38	PCIE_RX14P	PCIE_TX14P	K30							
	F37	PCIE_RX14N	PCIE_TX14N	K29							
	F35	PCIE_RX15P	PCIE_TX15P	H33							
	E37	PCIE_RX15N	PCIE_TX15N	H32							

CLOCK

12 CLK_PCIE_VGA CLK_PCIE_VGA AB35 PCIE_REFCLKP
12 CLK_PCIE_VGA# CLK_PCIE_VGA# AA36 PCIE_REFCLKN

CALIBRATION

PCIE_CALRP Y30 1.27K_0402_1% 1 RV63 2 TH@
PCIE_CALRN Y29 2K_0402_1% 1 RV65 2 TH@ +1.0VGS
1K_0402_1% 1 RV203 2 MARS@

MARS@
RV198 1 2 1.69K_0402_1%~D +1.0VGS

DIS@ RV64 1 2 1K_0402_5%
PWRGOOD AH16

GPU_RST# AA30 PERSTB

DIS@ RV66 100K_0402_5%

Install 2K for Thames/Seymour

THAMES XT M2 THR1@

UV1 MSR1@ SA00005X10L
MARS-PRO_FCBGA962~D
MARS Pro

UV1 SUNXTR1@ SA00006G60L
SUN XT M2_FCBGA962

UV1 SUNXTR3@ SA00006G61L
SUN XT M2_FCBGA962

LVDS Interface

UV1G

LVDS CONTROL
VARY_BL AK27
DIGON AJ27

TXCLK_UP_DPF3P	AK35	TXCLK_LP_DPE3P	AP34
TXCLK_UN_DPF3N	AL36	TXCLK_LN_DPE3N	AR34
TXOUT_U0P_DPF2P	AJ38	TXOUT_L0P_DPE2P	AW37
TXOUT_U0N_DPF2N	AK37	TXOUT_L0N_DPE2N	AU35
TXOUT_U1P_DPF1P	AH35	TXOUT_L1P_DPE1P	AR37
TXOUT_U1N_DPF1N	AJ36	TXOUT_L1N_DPE1N	AU38
TXOUT_U2P_DPF0P	AG38	TXOUT_L2P_DPE0P	AP35
TXOUT_U2N_DPF0N	AH37	TXOUT_L2N_DPE0N	AR36
TXOUT_U3P	AF35	TXOUT_L3P	AN36
TXOUT_U3N	AG36	TXOUT_L3N	AP37

LVTMDP

THAMES XT M2 @

RV61 2 @ 1 0_0402_5%
+3VGS

14 PXS_RST# 1 IN1
12 APU_PCIE_RST# 2 IN2
VCC 5
GND 3
OUT 4 GPU_RST#
UV13 MC74VHC1G08DFT2G_SC70-5
DIS@
SA000000H00

CV326 0.1U_0402_16V7K DIS@

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2012/09/11	Deciphered Date	2014/03/12	Title	ATI_ThamesXT_M2_PCIE/LVDS
				Size	Document Number LA-9103P Rev 1.0
				Date: Wednesday, July 10, 2013	Sheet 21 of 52

OPTIONAL FOR MEMORY ID ON HEATHROW/CHELSEA/VENUS/THAMES/SEYMOUR ONLY
No DVO or GPIO function on Mars

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING 0: 50% swing 1: Full swing	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS 0: disable 1: enable	X
RSVD	GPIO2	Advertises PCIE speed when compliance test 0: 2.5GT/s 1: 5GT/s	0
RSVD	GPIO8	RESERVED	0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0: disable 1: enable	X
ROMIDCFG[2:0]	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XXX
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD	H2SYNC		0
RSVD	GENERICC		0
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	11

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET

GPIO21	H2SYNC	GENERICC	GPIO2	GPIO8

ACIN_65W — RV250 Disc@ 0_0402_5% — AC_BATT
RV73 10K_0402_5%
RV74 4.7K_0402_5%
PACIN# — QV14B 2N7002DW-7-F_SOT363-6
QV14A 2N7002DW-7-F_SOT363-6

MLPS Setting please refer Page 24

	RV237	RV239	RV241
	8.45K_0402_1%	10K_0402_1%	10K_0402_1%
	RV238 4.75K_0402_1%	RV240 4.75K_0402_1%	RV242 4.75K_0402_1%
	MARS@	MARS@	MARS@
	CV329 0.68U_0402_10V	CV331 0.68U_0402_10V	CV333 0.68U_0402_10V

Add 12/6 for MLPS

TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Defalt setting for desktop)

MLPS Bit	AMD recommended setting			
	strap	R_PU	R_PD	C
PS0:	11001	RV243=8.45K	RV201=2K	CV335=NC
PS1:	11000	RV237=NC	RV238=4.75K	CV329=NC
PS2:	00000	RV239=NC	RV240=4.75K	CV331=0.68u

[ ] Via call back function: [V] Reading from GPIO/LCDDATA pins: PS_3

ID	Memory Type	Configuration	Row x Col x Bank bits	Channel Size
0	Samsung K4W2G1646E-BC11	128Mx16x8pcs	14*10*8	2G(SSI Only)
1	Samsung K4W2G1646E-BC11	128Mx16x4pcs	14*10*8	1G
2	Micron MT41K128M16JT-107G:K	128Mx16x4pcs	14*10*8	1G
3	Hynix H5TC2G63FFR-11C	128Mx16x4pcs	14*10*8	1G
4	Samsung K4W4G1646B-HC11	256Mx16x4pcs	15*10*8	2G
5	Micron MT41K256M16HA-107G:E	256Mx16x4pcs	15*10*8	2G
6	Hynix H5TC4G63AFR-11C	256Mx16x4pcs	15*10*8	2G
7				

PS_3 CONFIG[2:0]				Memory Configuration					
ID	RV241	RV242	Bits[3:1]	Memory Type	Configuration	Row x Col x Bank bits	Channel Size	VPN	DPN
0	NC	4750	000	Samsung-DDR3	128M x 16 8PCS	14 x 10 x 8	2G	K4W2G1646E-BC11	2488G
1	8450	2000	001	Samsung-DDR3	128M x 16 4PCS	14 x 10 x 8	1G	K4W2G1646E-BC11	
2	4530	2000	010	Micron-DDR3	128M x 16 4PCS	14 x 10 x 8	1G	MT41K128M16JT-107G:K	
3	6980	4990	011	Hynix-DDR3	128M x 16 4PCS	14 x 10 x 8	1G	H5TC2G63FFR-11C	
4	4530	4990	100	Samsung-DDR3	256M x 16 4PCS	15 x 10 x 8	2G	K4W4G1646B-HC11	
5	3240	5620	101	Micron-DDR3	256M x 16 4PCS	15 x 10 x 8	2G	MT41K256M16HA-107G:E	
6	3400	10000	110	Hynix-DDR3	256M x 16 4PCS	15 x 10 x 8	2G	H5TC4G63AFR-11C	
7	4750	NC	111						

VGA Thermal Sensor ADM1032ARMZ

Closed to GPU

Address:100_1101
SA00001Z710
12/12 Update

Internal VGA Thermal Sensor

Security Classification	Compal Secret Data		
Issued Date	2012/09/11	Deciphered Date	2014/03/12

Compal Electronics, Inc.
Title: ATI_ThamesXT_M2_Main_MSIC
Size: — Document Number: LA-9103P — Rev: 1.0
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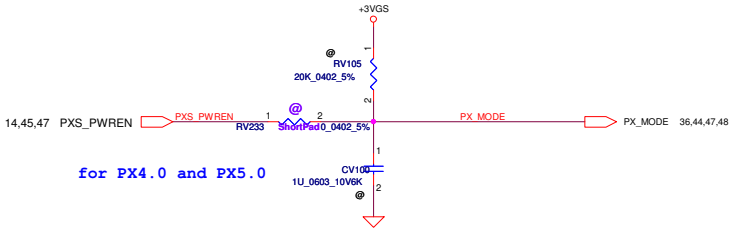
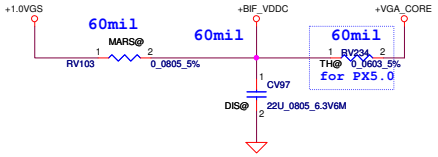
PX_MODE=1 for Normal Operation

PX_MODE=0 for BACO mode to shut down power rails expcept VDDR3,PCIE_VDDC and 1.8V rail

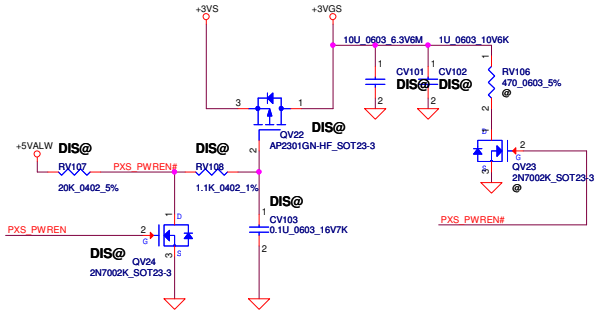
Switch circuits in BACO desingns for Thanes/Seymour only



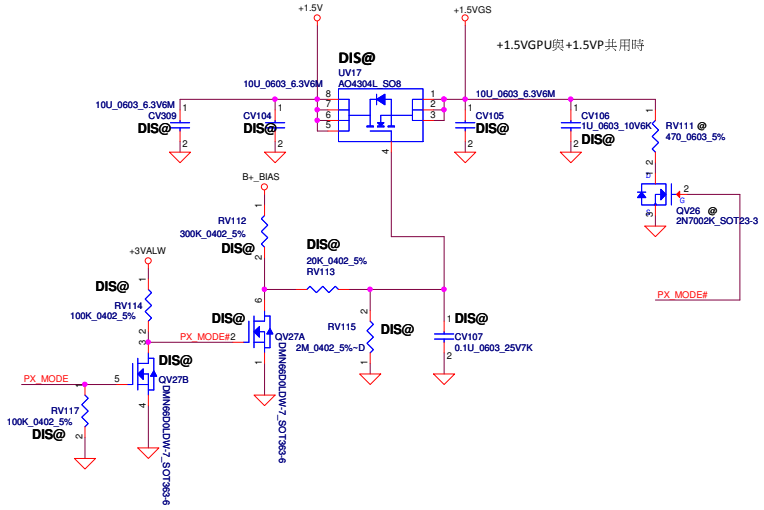
55mA@1.0V, in BACO mode



+3.3VS TO +3.3VGS



+1.5V TO +1.5VGS



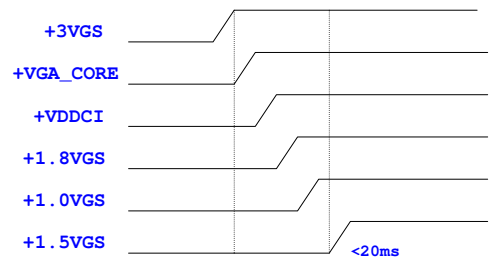
Note:

PX4.0 +VGA_CORE,VDDCI,+1.5VGS OFF

PX4.0 +3VGS, +1.0VGS,+1.8VGS ON

PX5.0 +3VGS,+VGA_CORE,VDDCI,+1.5VGV,+1.0VGS,+1.8VGS OFF

Power Seguence of Thames and Chelsea



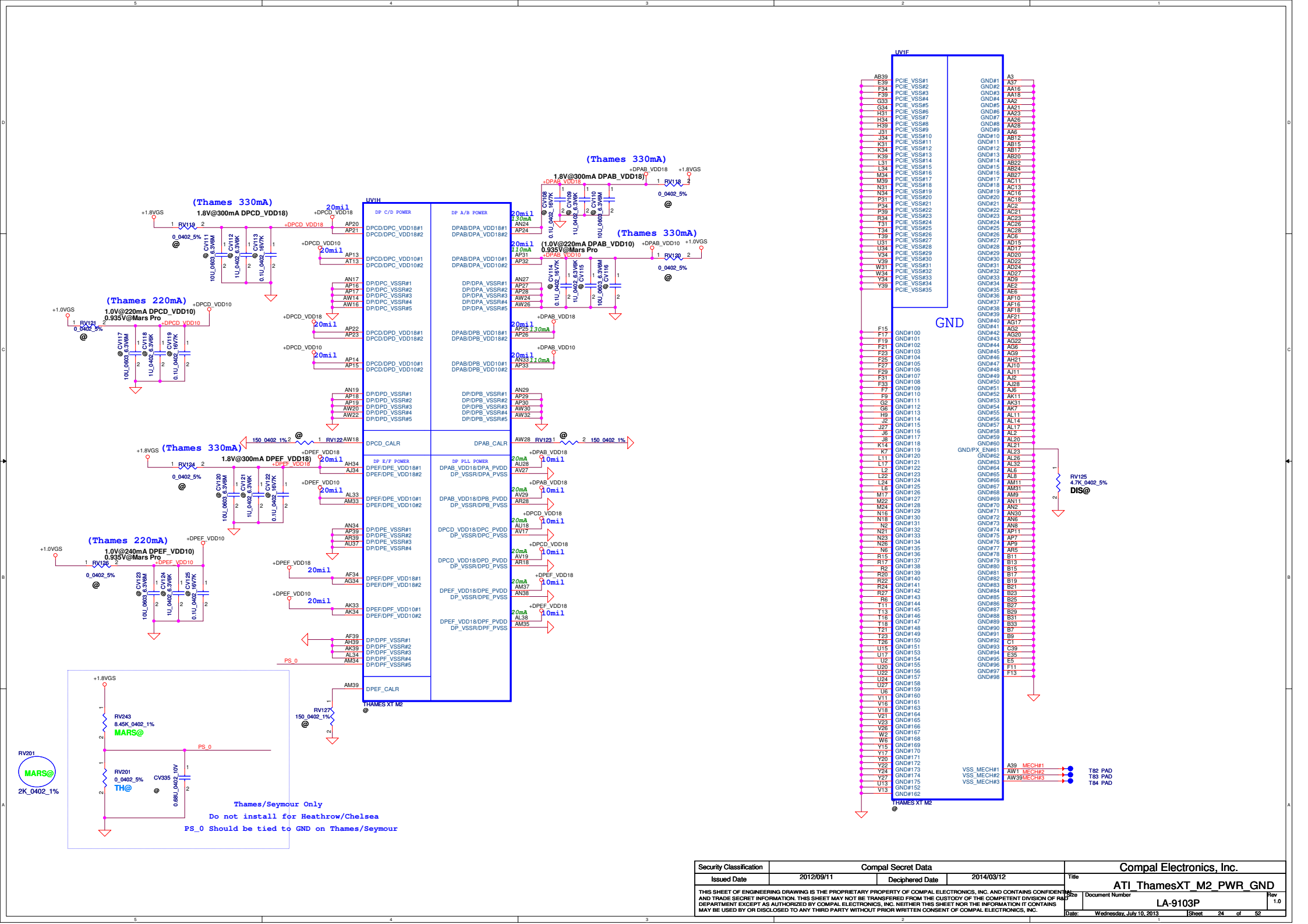
Security Classification	Compal Secret Data		
Issued Date	2012/09/11	Deciphered Date	2014/03/12

Compal Electronics, Inc.

Title: ATI_ThamesXT_M2_BACO POWER

Size | Document Number: LA-9103P | Rev: 1.0

Date: Wednesday, July 10, 2013 | Sheet 23 of 52



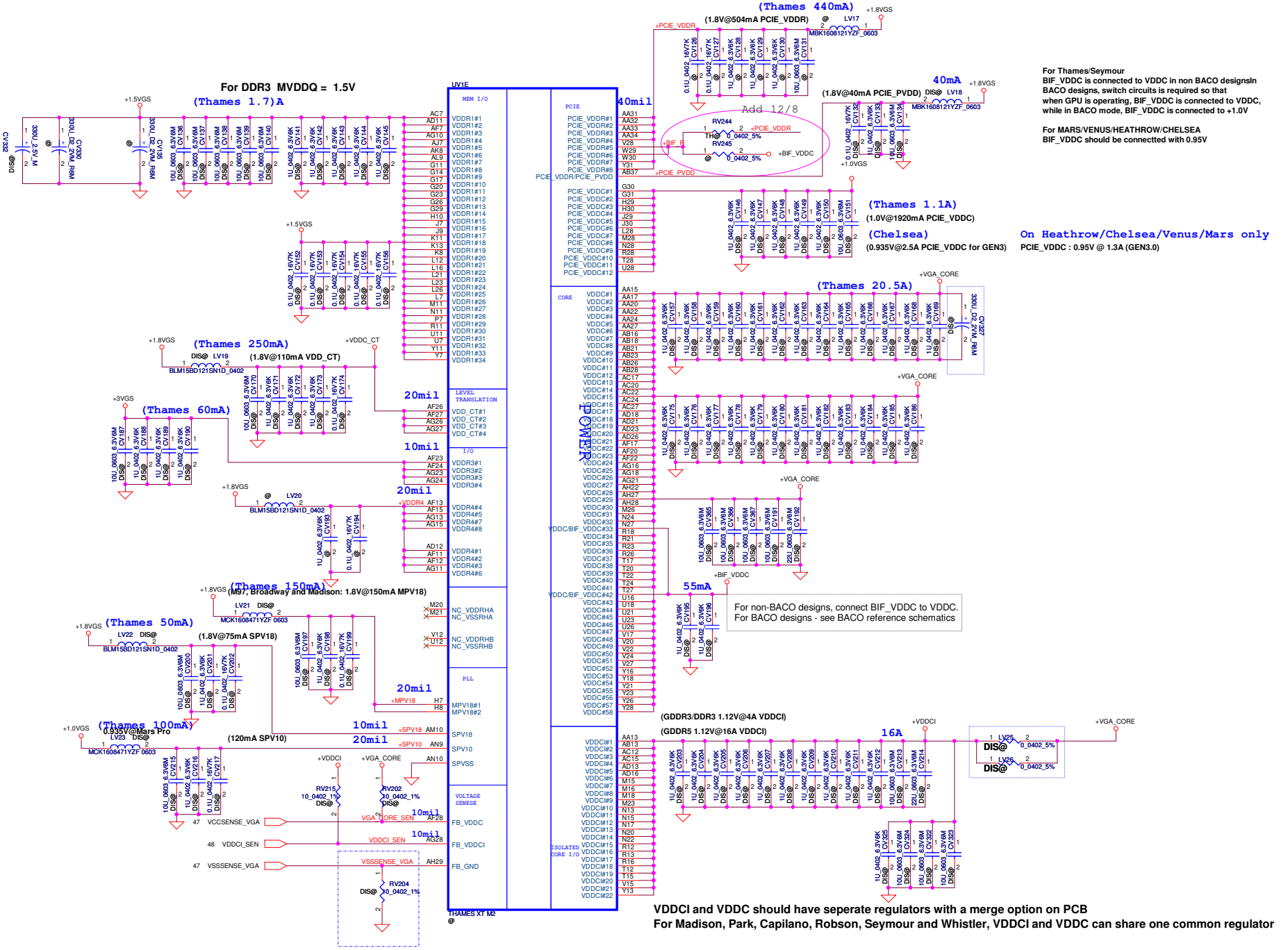
Security Classification	Compal Secret Data		
Issued Date	2012/09/11	Deciphered Date	2014/03/12

Compal Electronics, Inc.

Title: ATI_ThamesXT_M2_PWR_GND

Size: | Document Number: LA-9103P | Rev: 1.0

Date: Wednesday, July 10, 2013 | Sheet 24 of 52



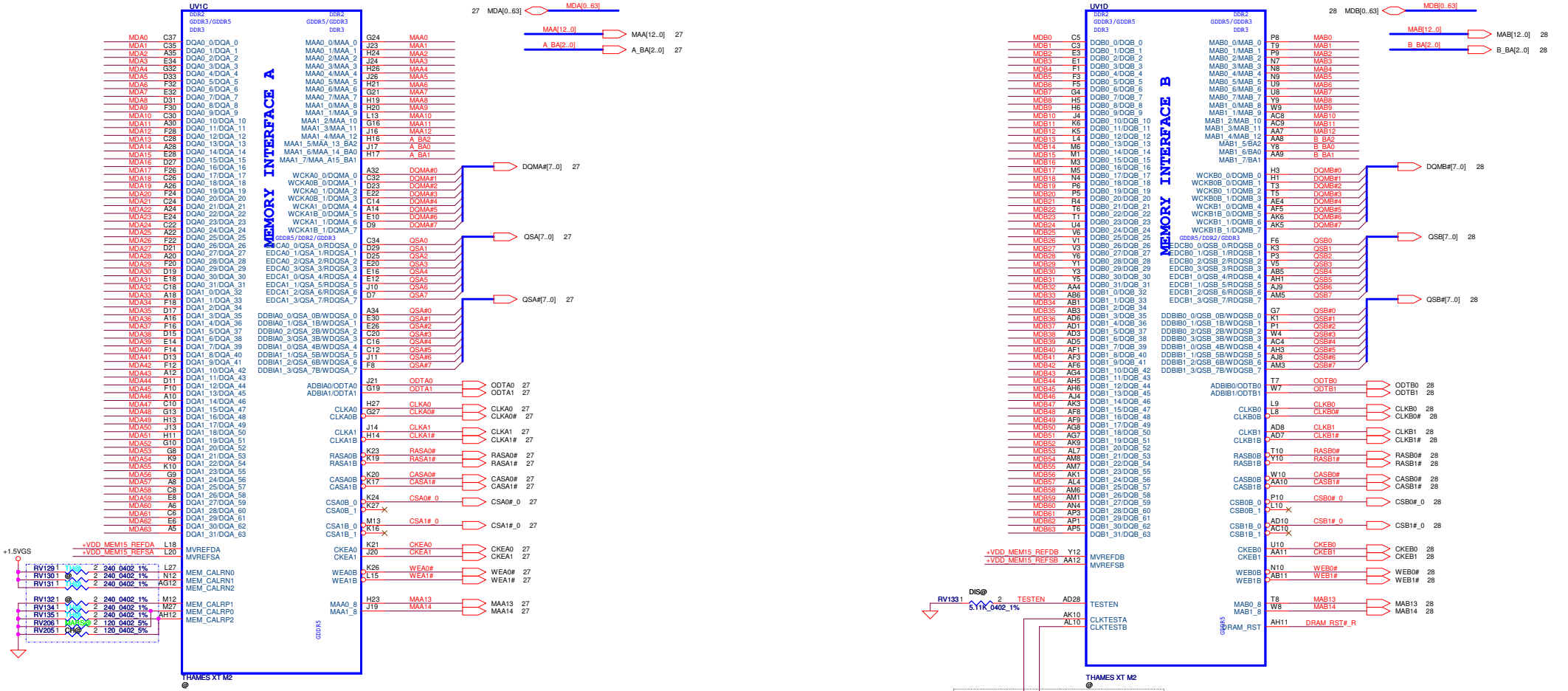
Security Classification	Compal Secret Data		
Issued Date	2012/09/11	Deciphered Date	2014/03/12

Compal Electronics, Inc.

Title: ATI_ThamesXT_M2_Power

Size: | Document Number: LA-9103P | Rev: 1.0

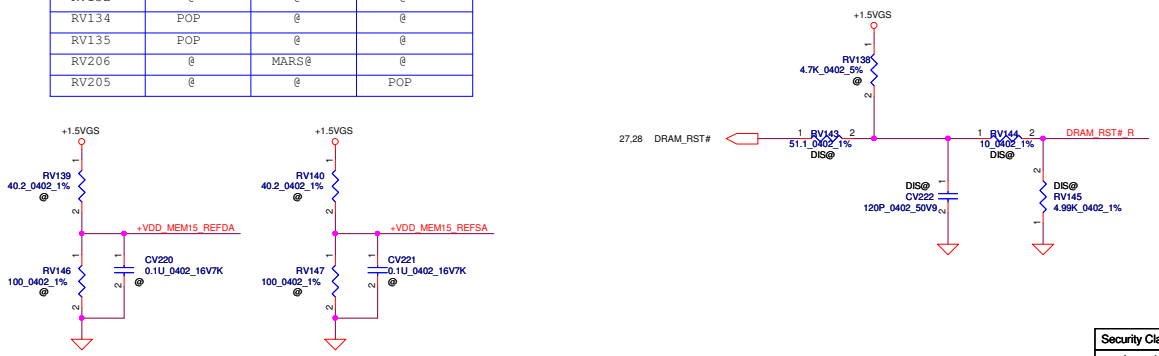
Date: Wednesday, July 10, 2013 | Sheet 25 of 52



Co-lay Thames/Mars Pro/Chelsea

	Thames M2	Mars Pro	Chelsea M2
RV129	POP	@	@
RV130	@	@	@
RV131	POP	@	@
RV132	@	@	@
RV134	POP	@	@
RV135	POP	@	@
RV206	@	MARS@	@
RV205	@	@	POP

This basic topology should be used for DRAM_RST for DDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM load and board to pass Reset Signal Spec.
Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2



Security Classification	Compal Secret Data		
Issued Date	2012/09/11	Deciphered Date	2014/03/12

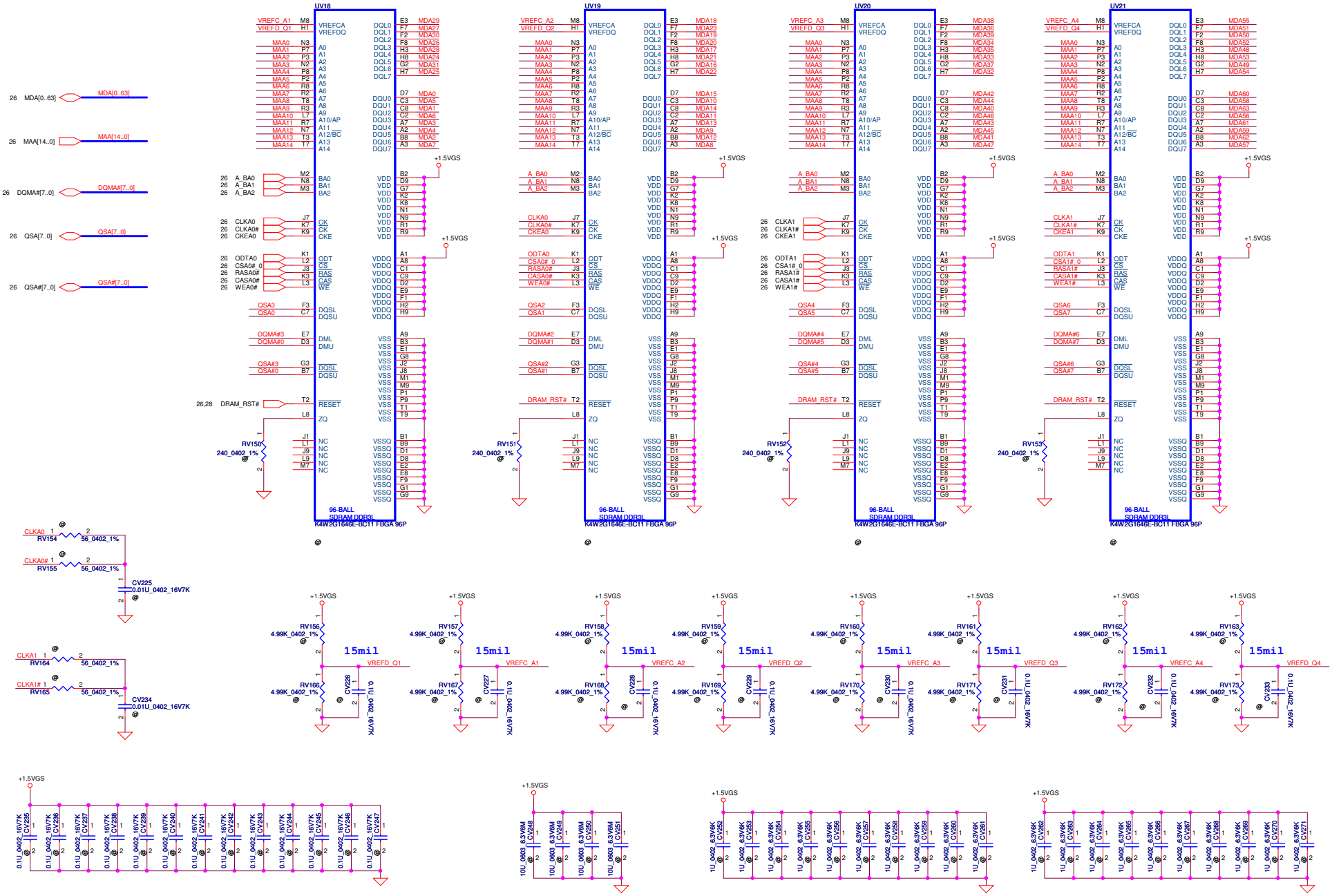
Compal Electronics, Inc.

Title: ATI_ThamesXT_M2_MEM IF

Size | Document Number: LA-9103P | Rev: 1.0

Date: Wednesday, July 10, 2013 | Sheet 26 of 52

CHANNEL A: 256MB/512MB DDR3



Security Classification	Compal Secret Data		
Issued Date	2012/09/11	Deciphered Date	2014/03/12

Compal Electronics, Inc.

Title: ATI_ThamesXT_M2_VRAM_A

Size	Document Number	Rev
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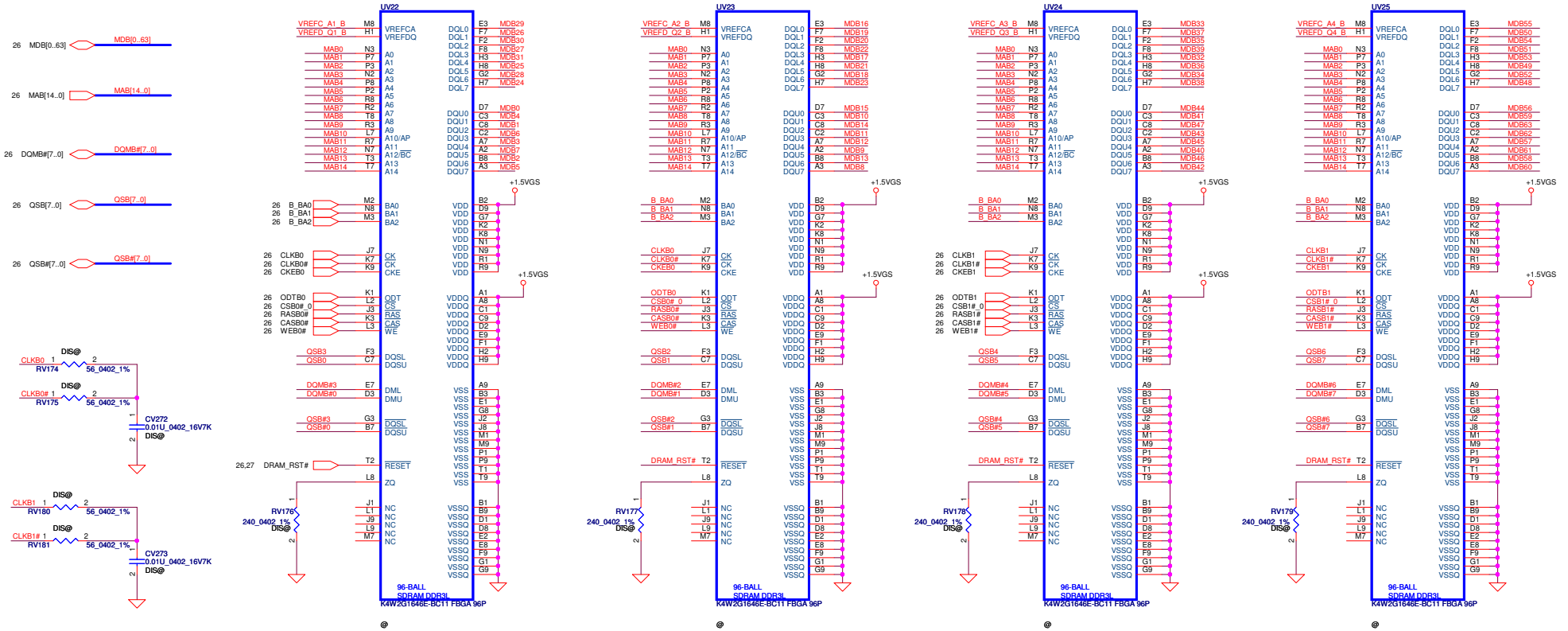
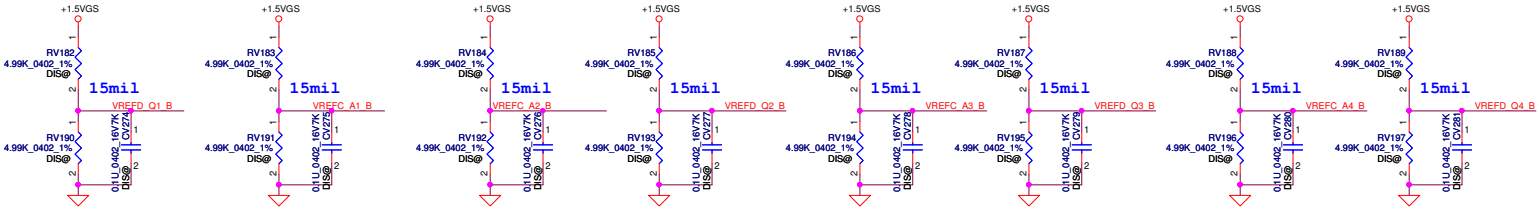
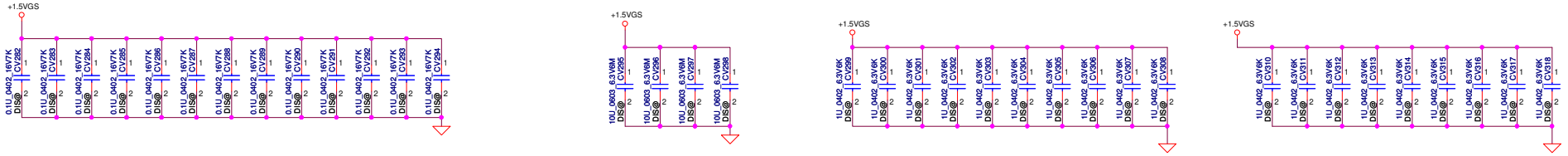
CHANNEL B: 256MB/512MB DDR3







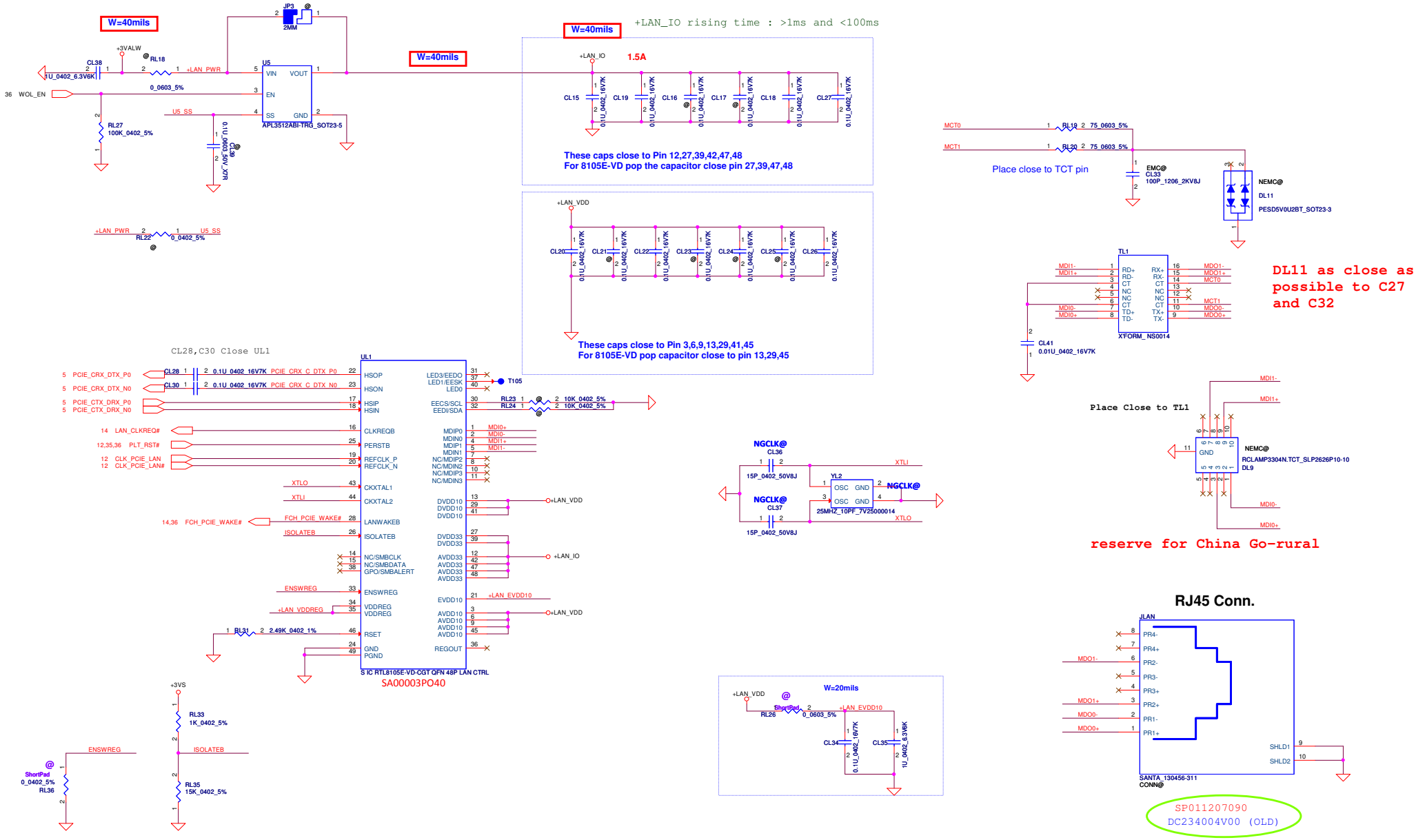
Security Classification	Compal Secret Data		
Issued Date	2012/09/11	Deciphered Date	2014/03/12

Compal Electronics, Inc.

Title: ATI_ThamesXT_M2_VRAM_B

Size: | Document Number: LA-9103P | Rev: 1.0

Date: Wednesday, July 10, 2013 | Sheet 26 of 52



Security Classification	Compal Secret Data		
Issued Date	2012/09/11	Deciphered Date	2014/03/12

Compal Electronics, Inc.			
Title	LAN RTL8105E		
Size	Document Number		Rev
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CA71, CA51 place close to Pin 26

CA59, CA60
Close to UA1
Pin36

SM01000BV00
need CIS symbol

JACK_PLUG Delay circutis

Reserve for cancel Delay circutis

RA1108, RA33 place close to Jack Conn

RA51, RA33 place close to UA1

Place on the moat between GND & GNDA.

EC Beep / FCH Beep / PC Beep

SP02000H300

close to Codec

Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R-

Speaker 4 ohm : 40mil

Speaker 8 ohm : 20mil

iPhone and Nokia type Combo Jack

40mil
40mil

CA33 and CA39 change to 9.31K
SD03493118L (S RES 1/16W 9.31K +-1% 0402)
Audio Vender request

Security Classification	Compal Secret Data		
Issued Date	2012/09/11	Deciphered Date	2014/03/12

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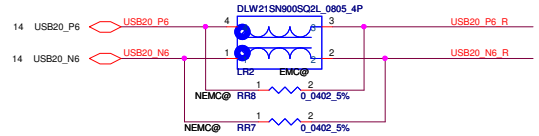
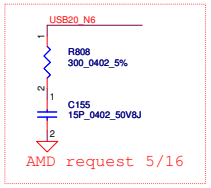
Compal Electronics, Inc.

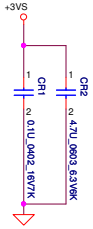
Title: **Audio Codec ALC3221**

Size | Document Number: **LA-9103P** | Rev: 1.0

Date: Wednesday, July 10, 2013 | Sheet 30 of 52



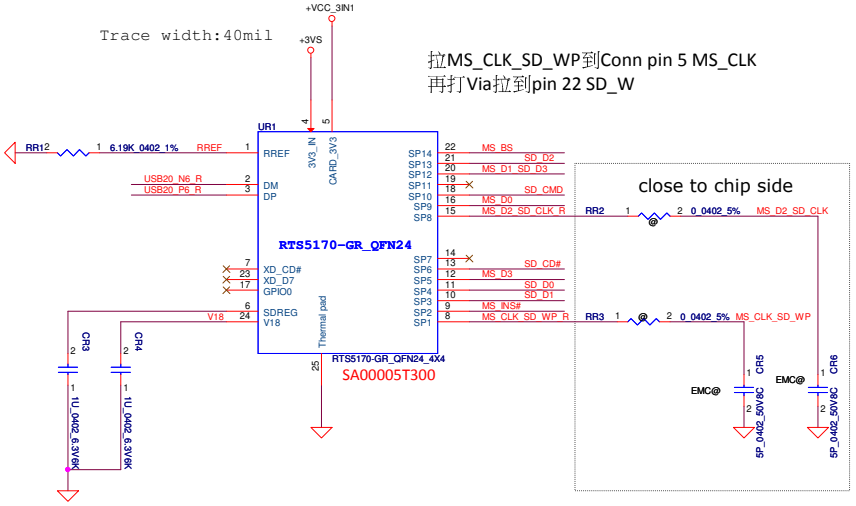


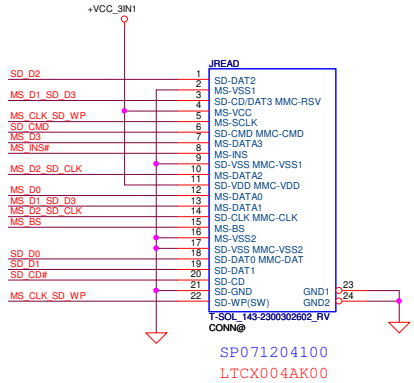


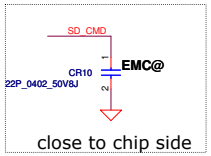
拉MS_D2_SD_CLK到Conn pin 14 SD_CLK
再打Via拉到pin 10 MS_D2

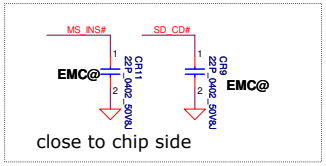
Trace width:40mil

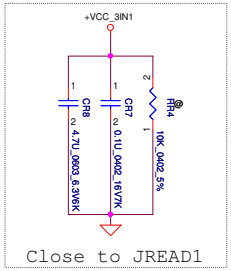
拉MS_CLK_SD_WP到Conn pin 5 MS_CLK
再打Via拉到pin 22 SD_W











Security Classification	Compal Secret Data		
Issued Date	2012/09/11	Deciphered Date	2014/03/12

Compal Electronics, Inc.	
Title	Card Reader RTS5179
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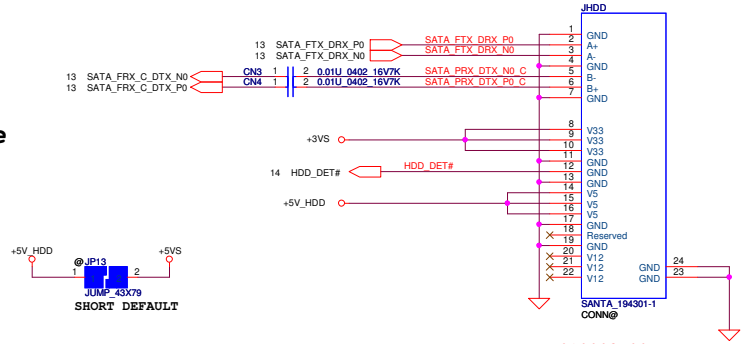
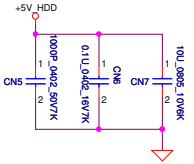
SATA HDD Conn.

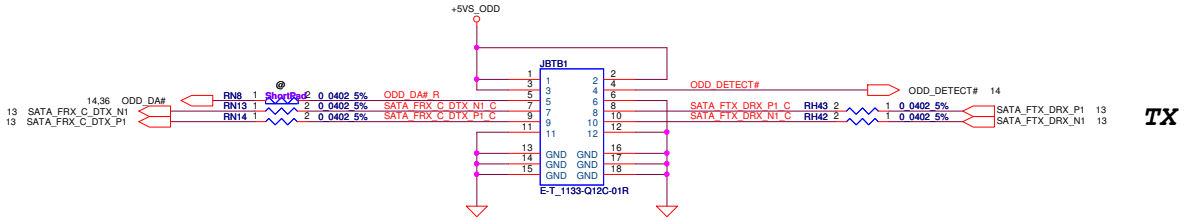
+5V_HDD Source



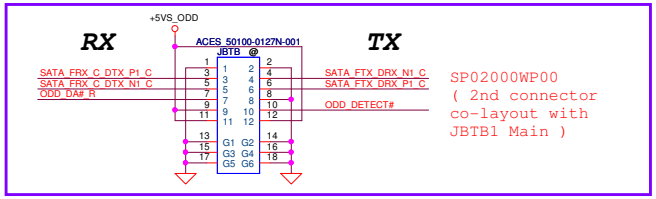


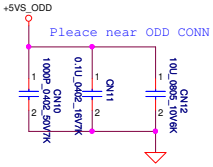
DC010003V00
DC010003Y00 (OLD)

ODD BTB Conn.

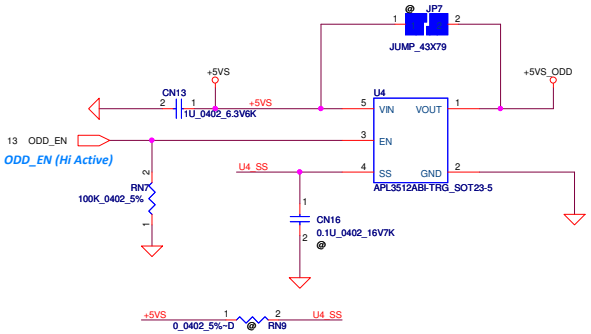


SP02000MJ00
SP02000G800 (OLD)





ODD Power Control



Security Classification	Compal Secret Data		
Issued Date	2012/09/11	Deciphered Date	2014/03/12

Compal Electronics, Inc.

Title: HDD/ODD

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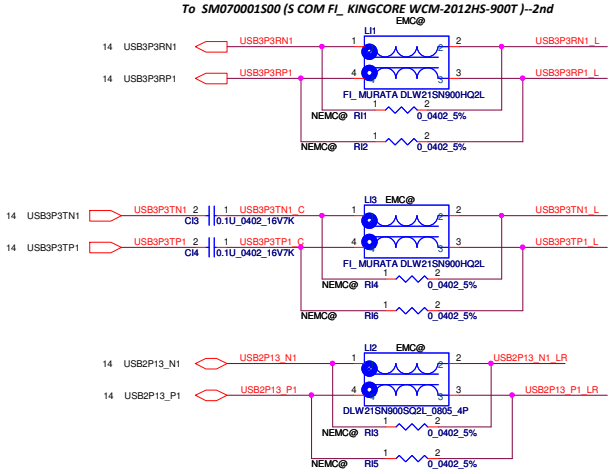
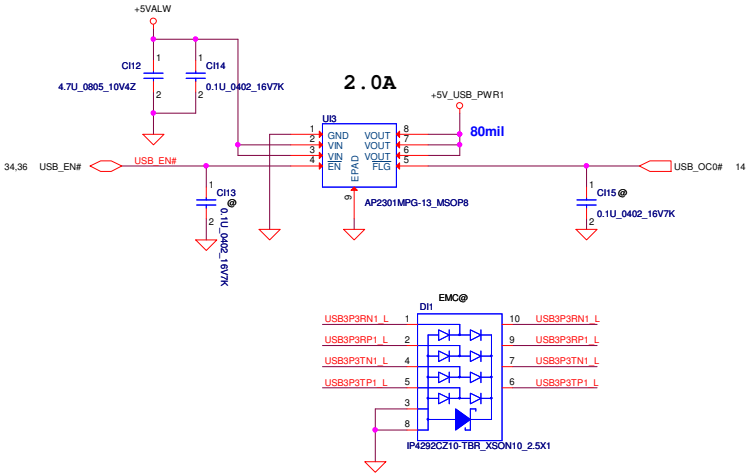
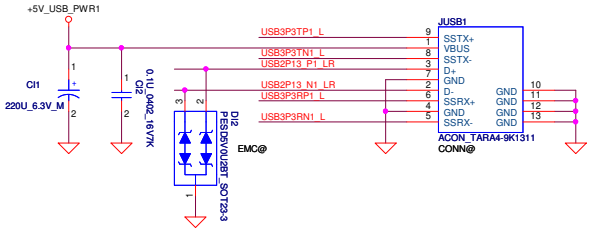
9/20 OAK Intel USB3.0 issue
Change LI1, LI3, LI4, LI6 Part
PN: from SM01002080L (S SUPPRE_ MURATA DLW21SN900SQ2L 0805)
To SM070000S80 (S COM FI_ CHENG HANN WCM2012F2SF-670T04)

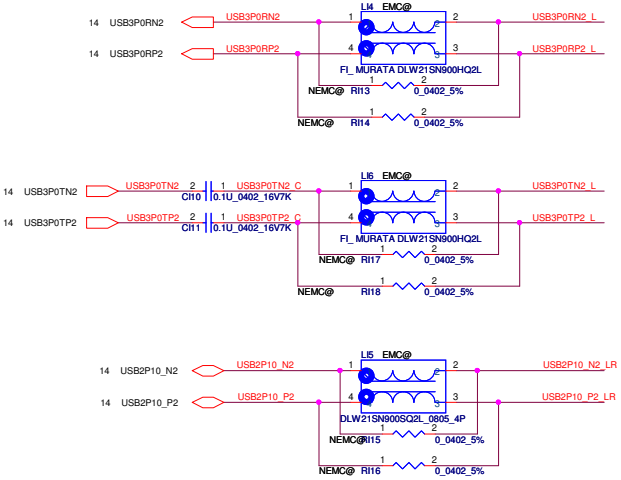
1/22 Change LI1, LI3, LI4, LI6 Part
PN: from SM070000S80 (S COM FI_ CHENG HANN WCM2012F2SF-670T04)
To SM070001E00 (S COM FI_ MURATA DLW21SN900HQ2L)--Main
To SM070001S00 (S COM FI_ KINGCORE WCM-2012HS-900T)--2nd

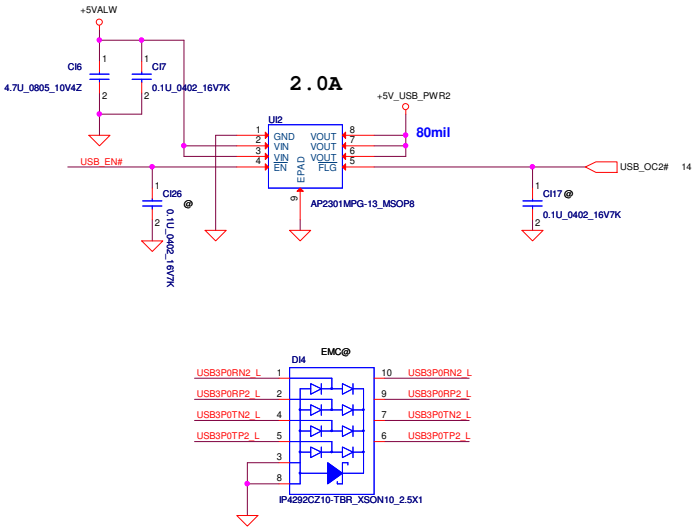




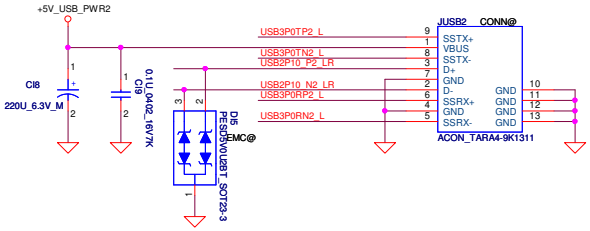
USB conn.1







USB conn.2



Security Classification	Compal Secret Data		
Issued Date	2012/09/11	Deciphered Date	2014/03/12

Compal Electronics, Inc.

Title: **USB3.0**

Size: Document Number: **LA-9103P** Rev: 1.0

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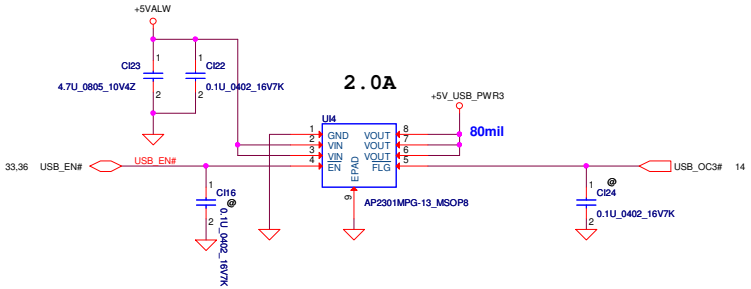
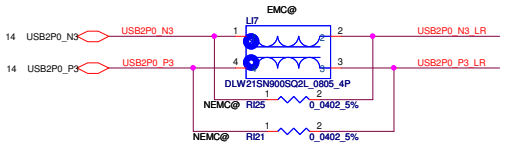
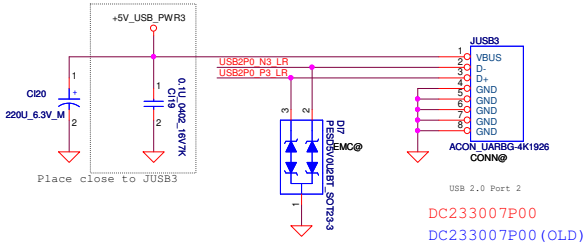
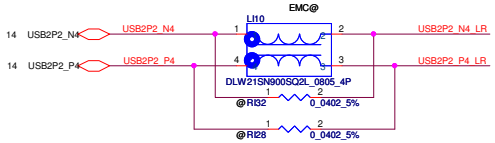
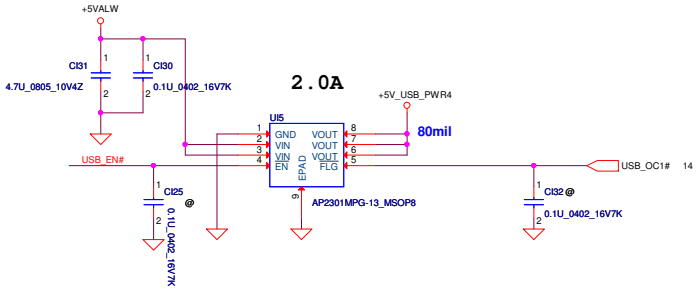




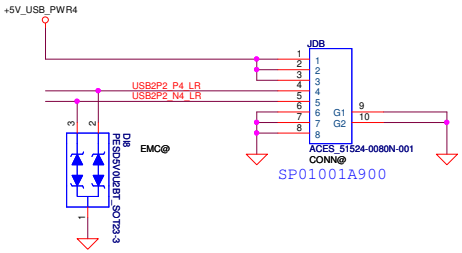
USB conn.3







USB conn.4



Security Classification	Compal Secret Data		
Issued Date	2012/09/11	Deciphered Date	2014/03/12

Compal Electronics, Inc.

Title: **MB to USB2.0 DB**

Size | Document Number: **LA-9103P** | Rev: 1.0

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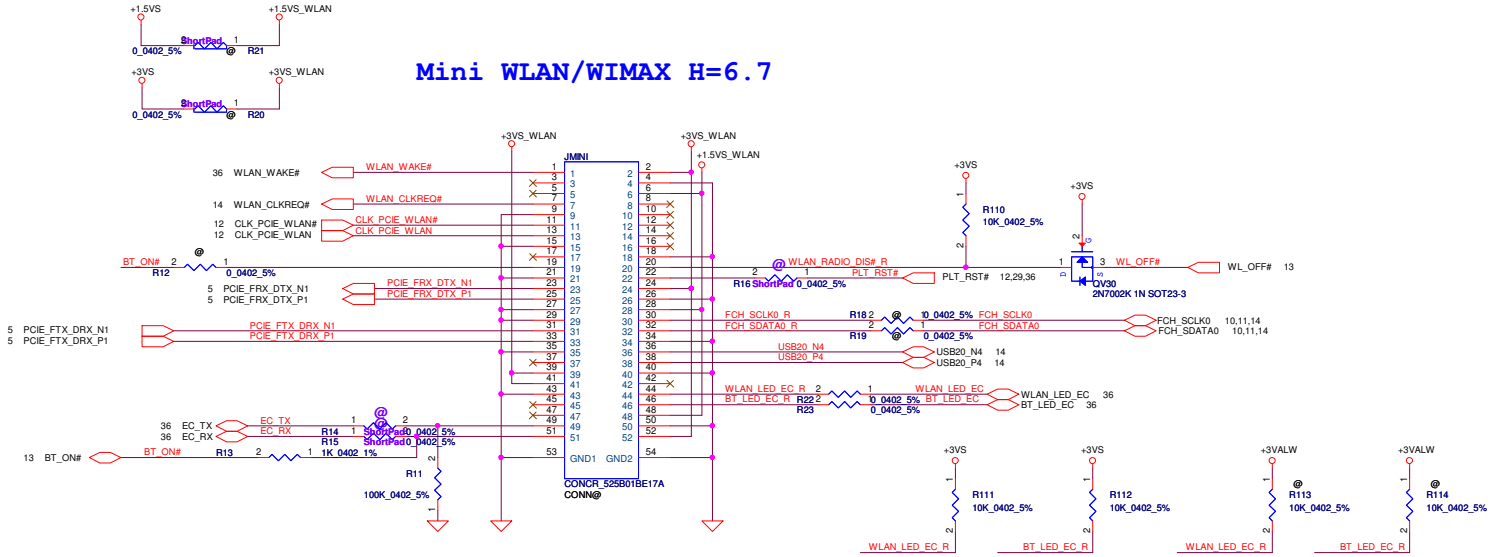
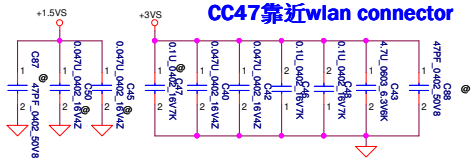
Mini WLAN/WIMAX H=6.7

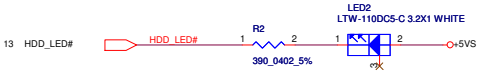


CC47靠近wlan connector



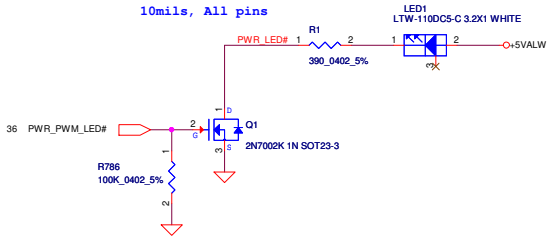
R111, R112
Please Close to JMINI

HDD LED

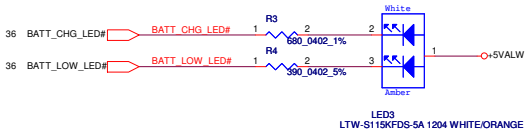


Power LED

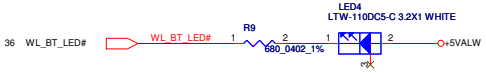
10mils, All pins



Battery LED



Wireless LED



Security Classification	Compal Secret Data		
Issued Date	2012/09/11	Deciphered Date	2014/03/12

Compal Electronics, Inc.	
Title	Mini Card/LED
Size	Document Number: LA-9103P
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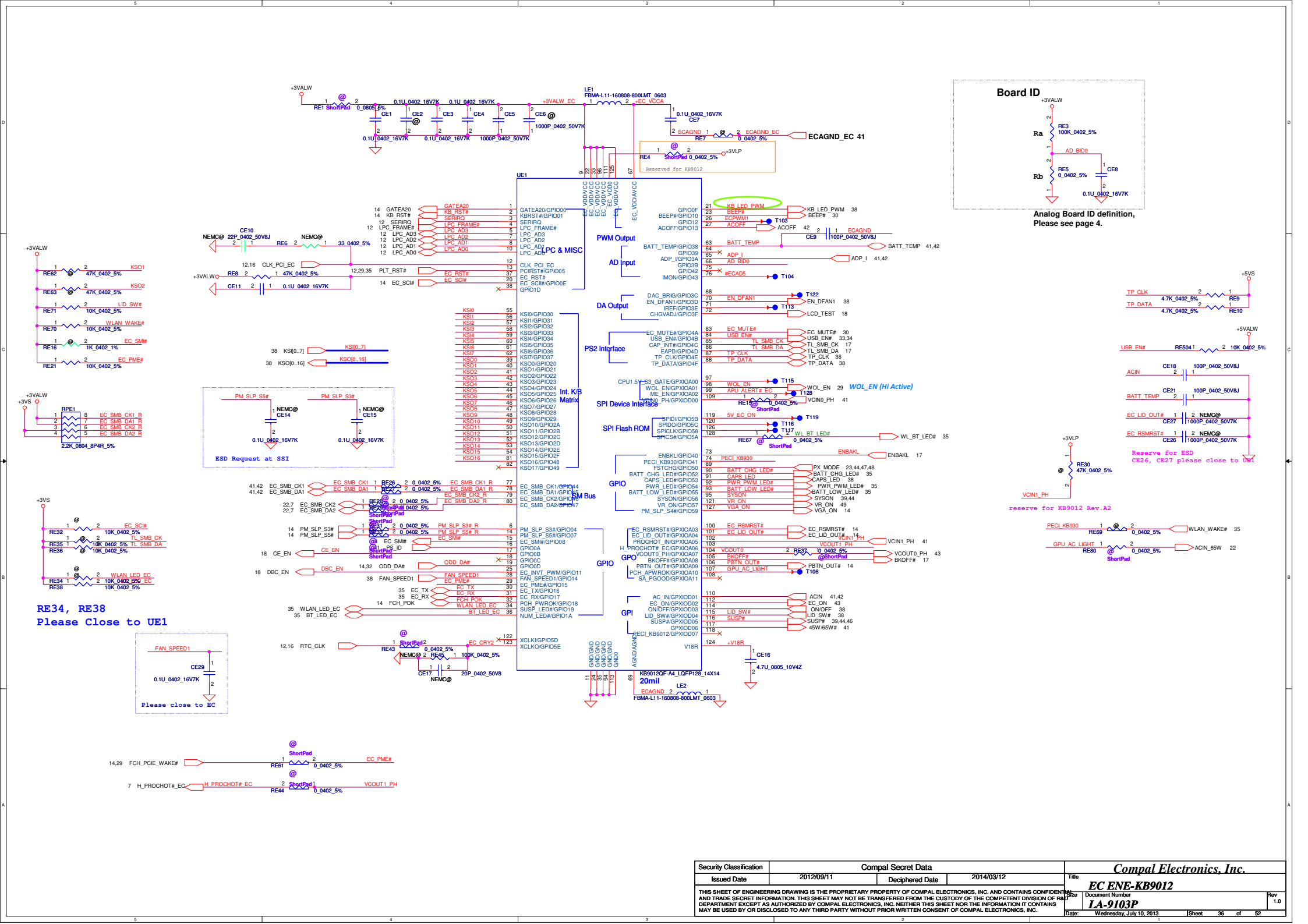
Board ID
Analog Board ID definition,
Please see page 4.
UE1
KB9012QF-A4_LQFP128_14X14
20mil
PWM Output
AD Input
LPC & MISC
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
GPIO
SM Bus
GPO
GPI
WOL_EN (Hi Active)
ESD Request at SSI
RE34, RE38
Please Close to UE1
Please close to EC
Reserve for KB9012 Rev.A2
Reserve for ESD
CE26, CE27 please close to UE1
ECAGND_EC 41
Reserved for KB9012
Security Classification
Compal Secret Data
Issued Date
2012/09/11
Deciphered Date
2014/03/12
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Compal Electronics, Inc.
Title
EC ENE-KB9012
Size
Document Number
LA-9103P
Rev
1.0
Date: Wednesday, July 10, 2013
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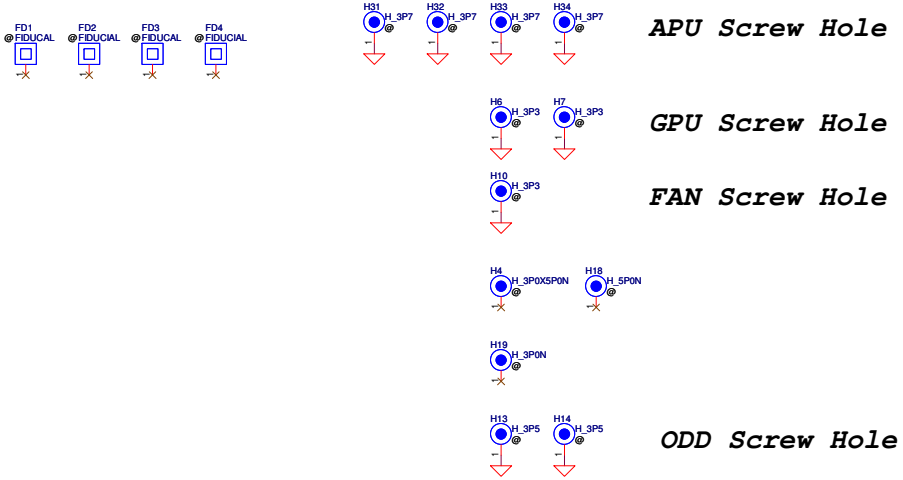
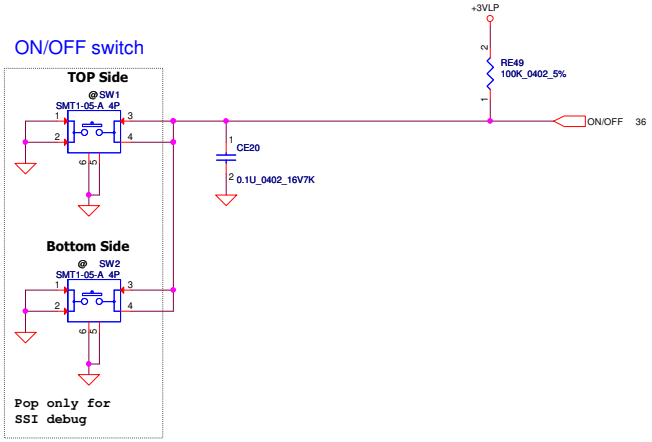
Screw Hole

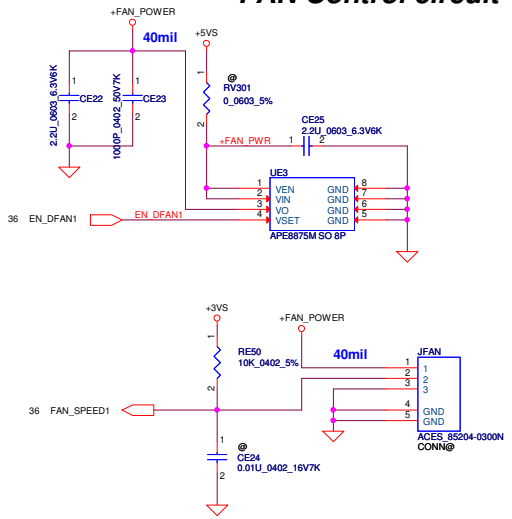


Compal Electronics, Inc.		
Title: Screw Hole		
Size	Document Number: LA-9101P	Rev: 1.0
Date: Wednesday, July 10, 2013	Sheet 37 of 52	

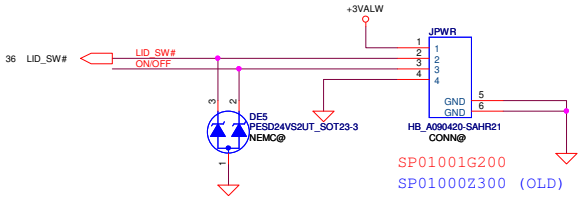
Power ON Circuit



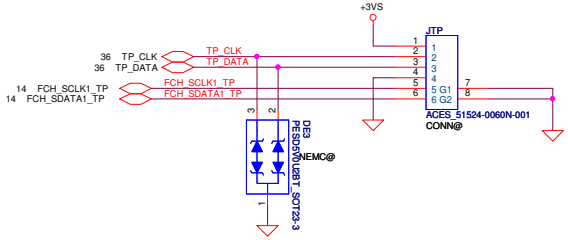
FAN Control circuit



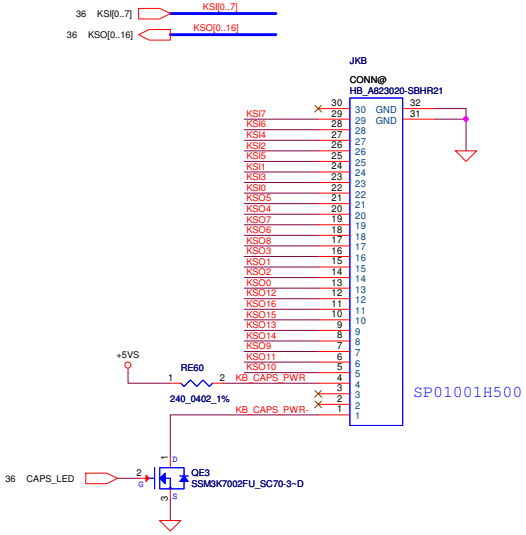
POWER/B



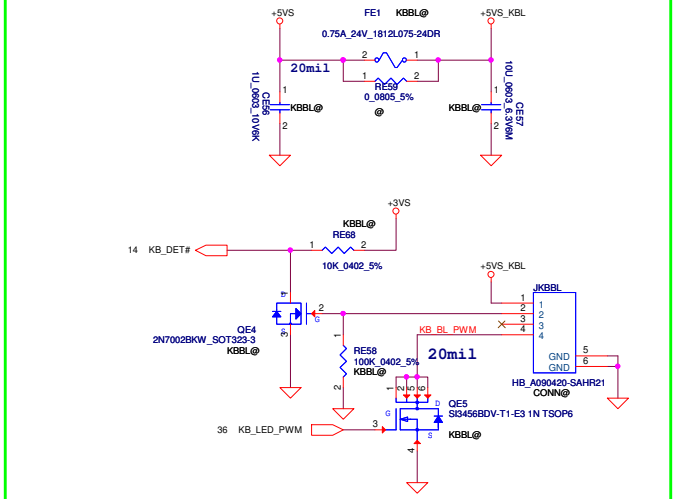
Touch pad



INT_KBD Conn.



* Key Board Back Light



Security Classification	Compal Secret Data		
Issued Date	2012/09/11	Deciphered Date	2014/03/12

Compal Electronics, Inc.			
Title: FAN/TP/KB/PWR SW			
Size	Document Number: LA-9103P		Rev: 1.0
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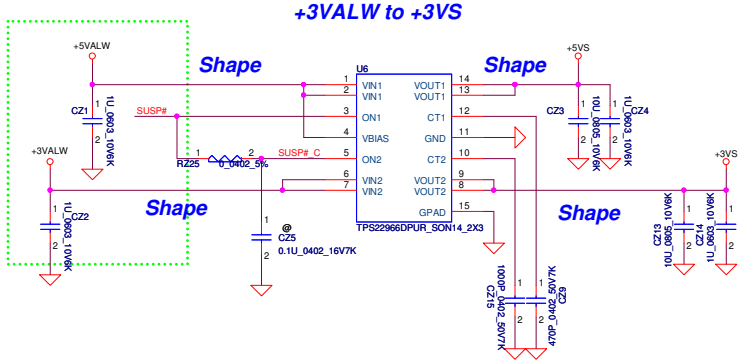
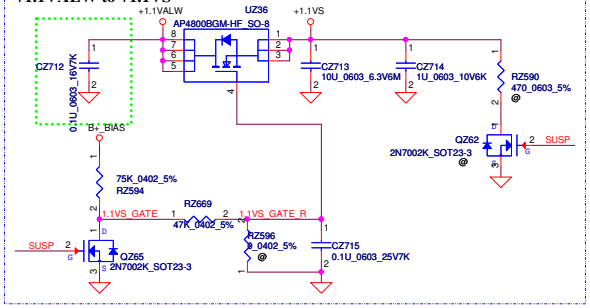
+5VALW to +5VS
+3VALW to +3VS

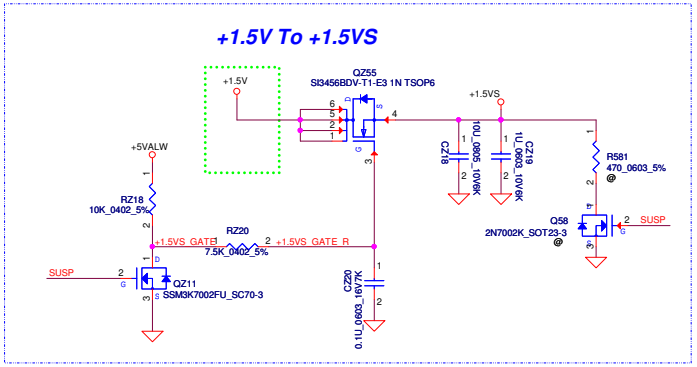


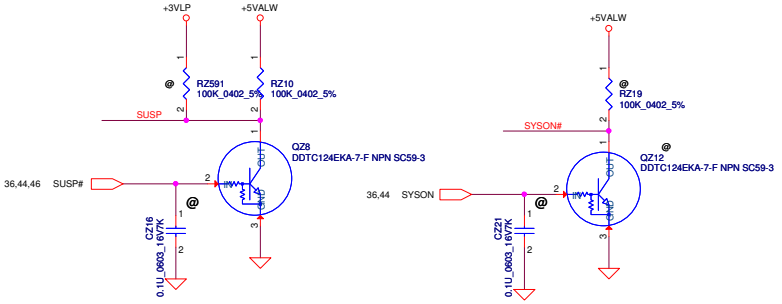
CTx(pF)	RISE TIME (µs)	
	5V	3.3V
0	124	88
220	481	323
470	855	603
1000	1724	1185
2200	3328	2240
4700	7459	4950
10000	16059	10835

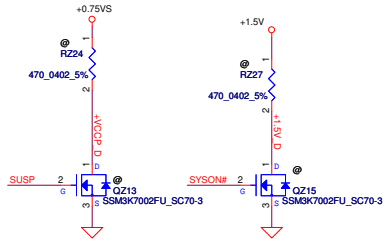
+1.1VALW to +1.1VS



+1.5V To +1.5VS







Security Classification	Compal Secret Data		
Issued Date	2012/09/11	Deciphered Date	2014/03/12

Compal Electronics, Inc.	
Title	DC/DC Interface
Size	Document Number: LA-9103P
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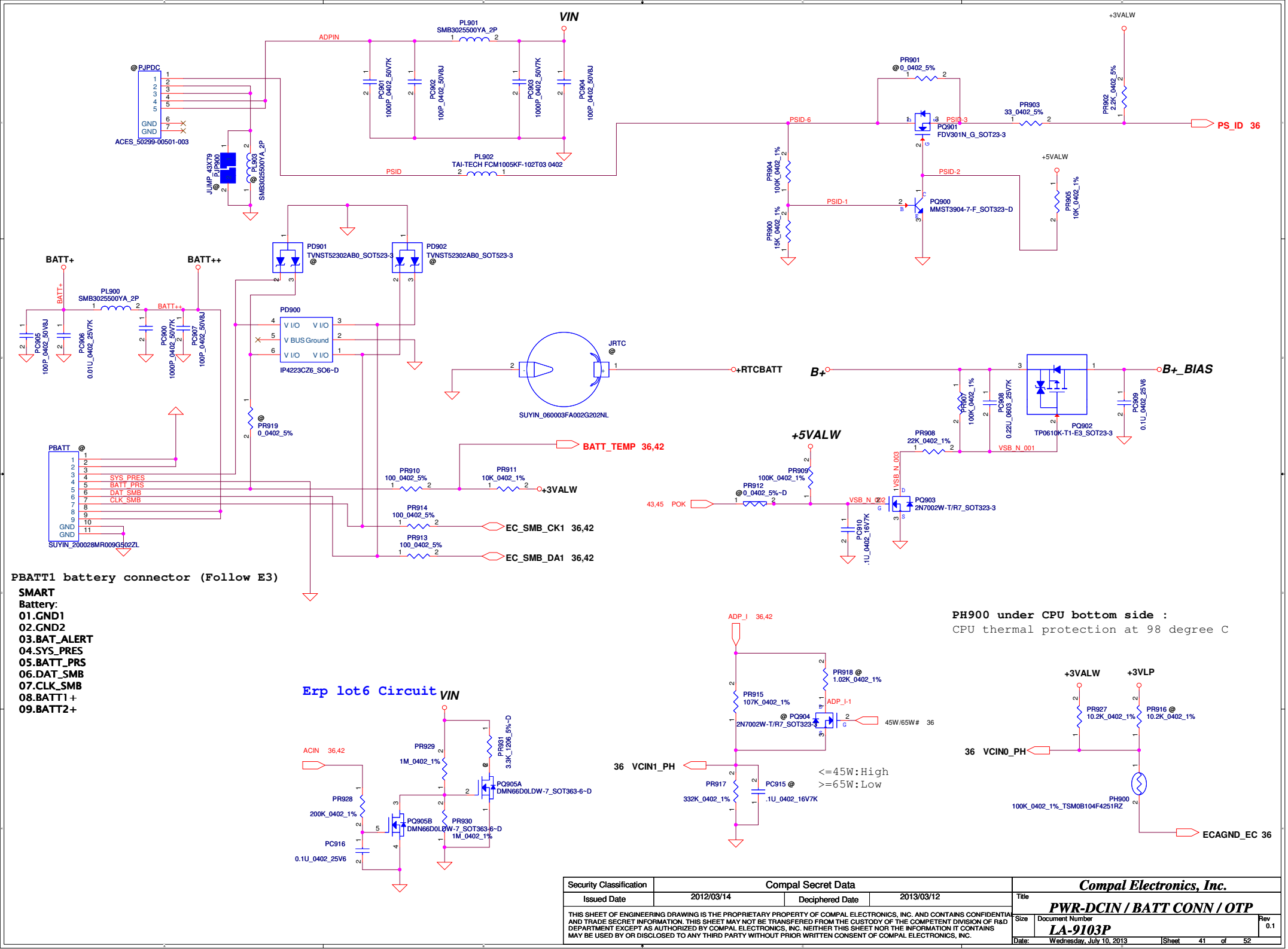
Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	08,11,12	DIMM	11/07/28	COMPAL	The M3 traces are routed to the Sandy Bridge Processor reserved pins for DDR3 VREF	Intel CHKLST Rev1.5 required	0.1
2							
3							
4							
5							
6							
7							
8							
9							
10							
11							
12							
13							
14							
15							
16							
17							
18							



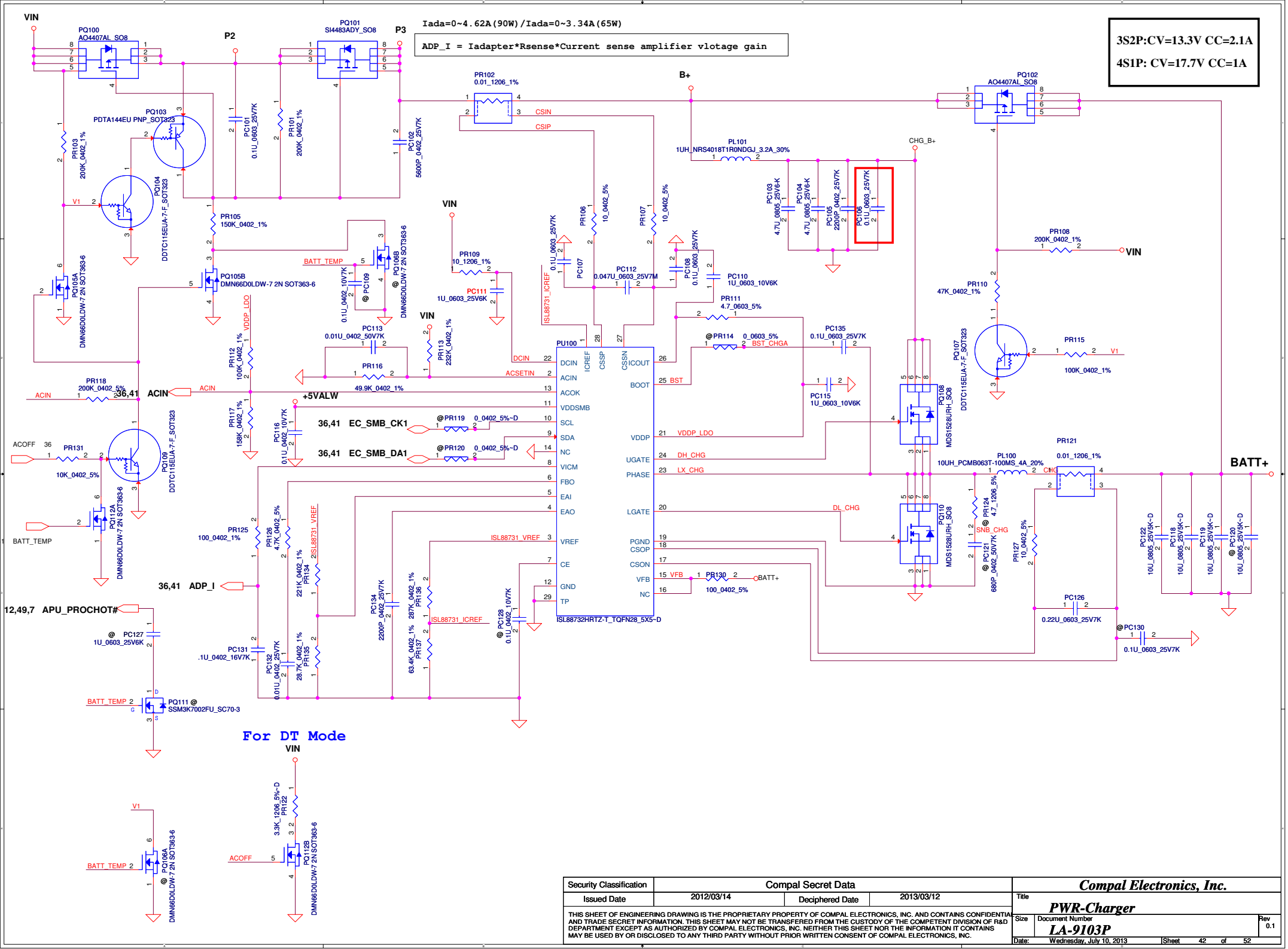
Security Classification	Compal Secret Data		
Issued Date	2012/03/14	Deciphered Date	2013/03/12

Compal Electronics, Inc.

Title: PWR-DCIN / BATT CONN / OTP

Size: | Document Number: LA-9103P | Rev: 0.1

Date: Wednesday, July 10, 2013 | Sheet 41 of 52



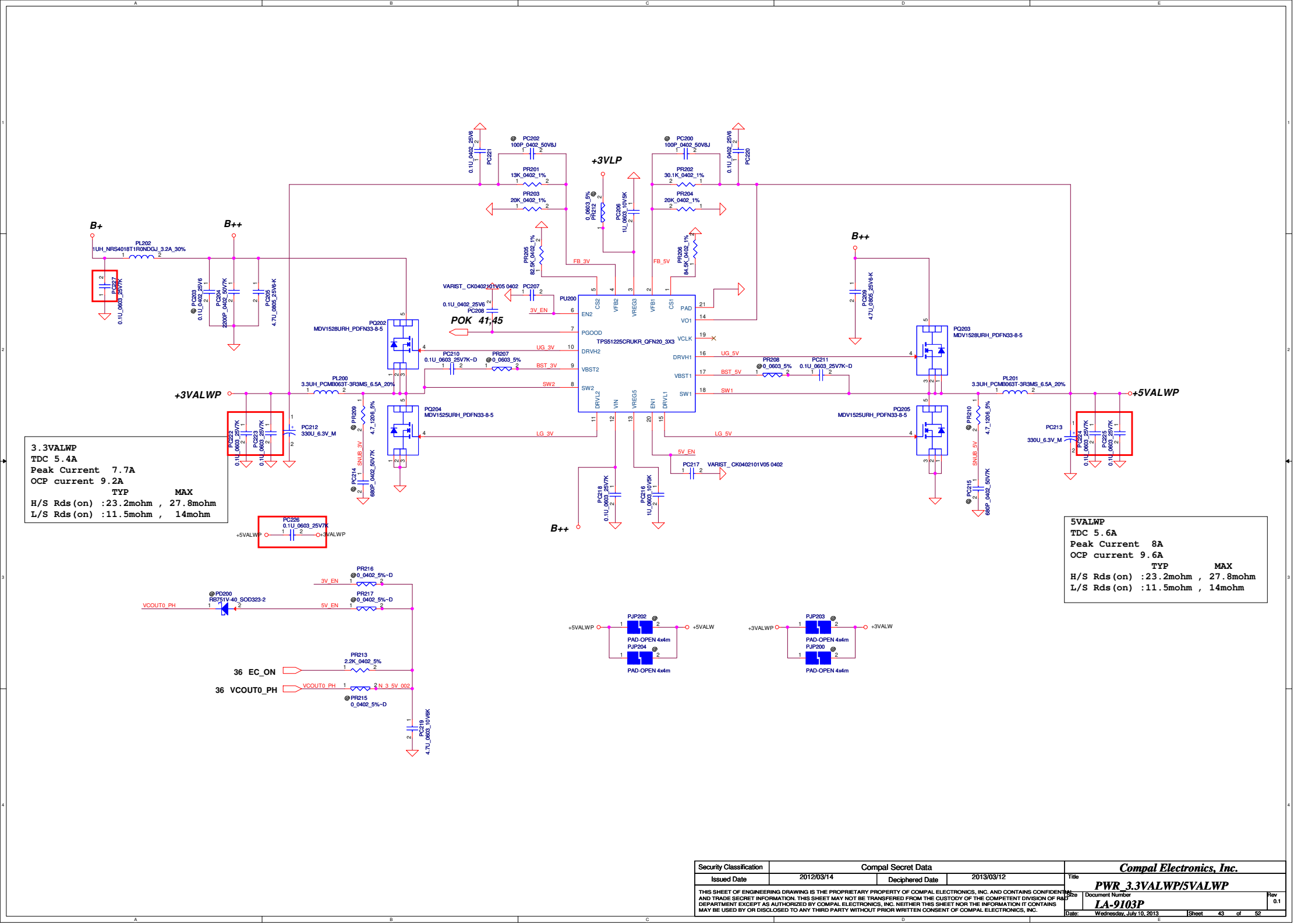
Security Classification	Compal Secret Data		
Issued Date	2012/03/14	Deciphered Date	2013/03/12

Compal Electronics, Inc.

Title: **PWR-Charger**

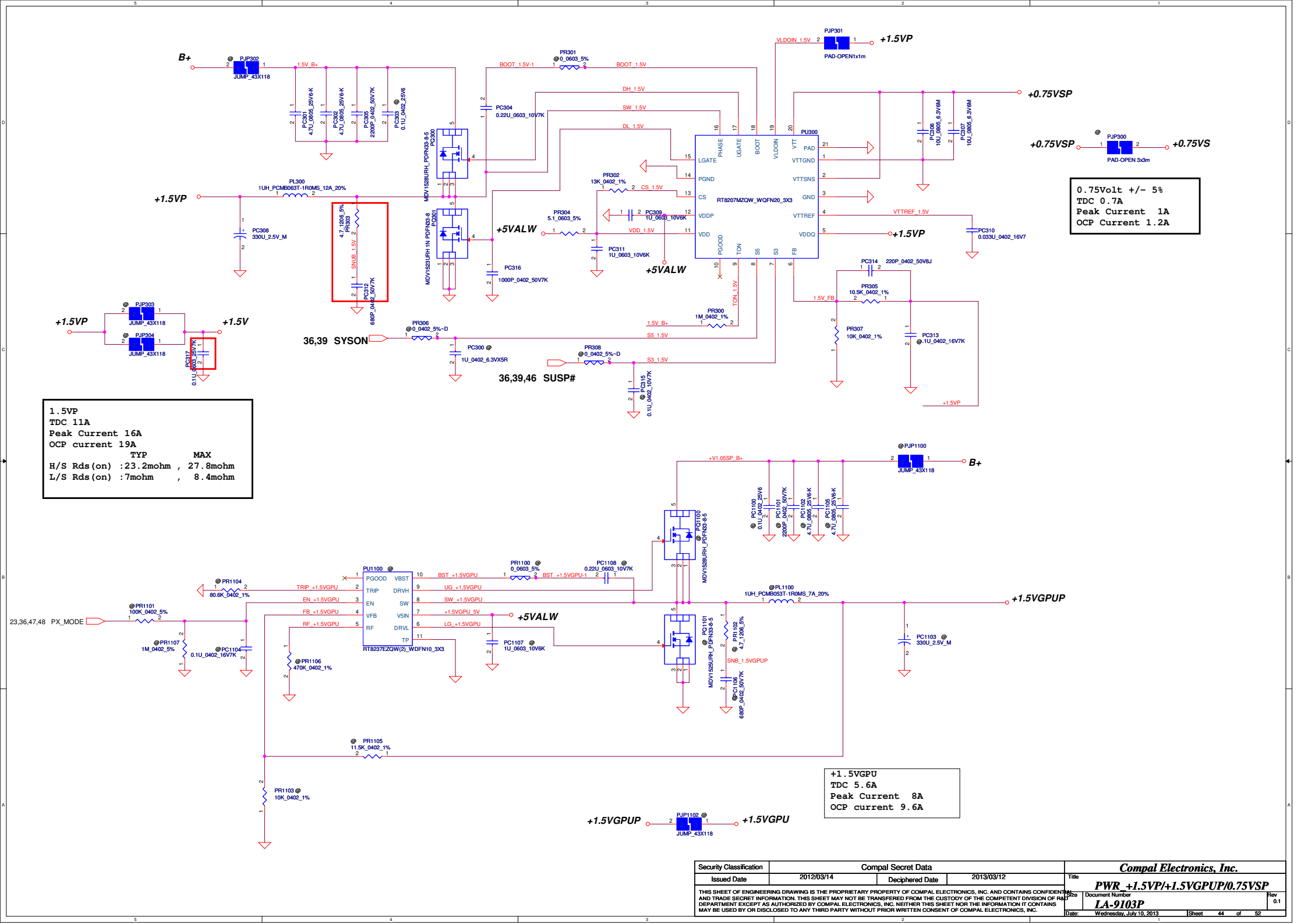
Size: | Document Number: **LA-9103P** | Rev: 0.1

Date: Wednesday, July 10, 2013 | Sheet 42 of 52



Security Classification	Compal Secret Data		
Issued Date	2012/03/14	Deciphered Date	2013/03/12

Compal Electronics, Inc.			
Title	PWR_3.3VALWP/5VALWP		
Size	Document Number	LA-9103P	Rev 0.1
Date: Wednesday, July 10, 2013	Sheet 43 of 52		


B+
PJP302
JUMP_43X118
1.5V_B+
PC301 4.7U_0805_25V6-K
PC302 4.7U_0805_25V6-K
PC305 2200P_0402_50V7K
PC303 0.1U_0402_25V6
PR301 @0_0603_5%
BOOT_1.5V-1
BOOT_1.5V
PC304 0.22U_0603_10V7K
DH_1.5V
SW_1.5V
DL_1.5V
MDV1528URH_PDFN33-8-5
PC300
MDV1523URH 1N PDFN33-8
PC301
PL300 1UH_PCMB063T-1R0MS_12A_20%
+1.5VP
PC308 330U_2.5V_M
PR303 4.7_1206_5%
SNUB_1.5V
PC312 680P_0402_50V7K
+5VALW
PR304 5.1_0603_5%
PR302 13K_0402_1%
CS_1.5V
PC309 1U_0603_10V6K
VDD_1.5V
PC311 1U_0603_10V6K
PC316 1000P_0402_50V7K
PU300
RT8207MZQW_WQFN20_3X3
PHASE
UGATE
BOOT
VLDOIN
VTT
PAD
VTTGND
VTTSNS
GND
VTTREF
VDDQ
LGATE
PGND
CS
VDDP
VDD
PGOOD
TON
S5
S3
FB
VLDOIN_1.5V
PJP301
PAD-OPEN1x1m
+0.75VSP
PC306 10U_0805_6.3V6M
PC307 10U_0805_6.3V6M
PJP300
PAD-OPEN 3x3m
+0.75VS
0.75Volt +/- 5%
TDC 0.7A
Peak Current 1A
OCP Current 1.2A
VTTREF_1.5V
PC310 0.033U_0402_16V7
PC314 220P_0402_50V8J
PR305 10.5K_0402_1%
1.5V_FB
PR307 10K_0402_1%
PC313 @1U_0402_16V7K
PR300 1M_0402_1%
TON_1.5V
1.5V_B+
S5_1.5V
S3_1.5V
PR306 @0_0402_5%~D
36,39 SYSON
PC300 @ 1U_0402_6.3V5R
PR308 @0_0402_5%~D
36,39,46 SUSP#
PC315 @ 0.1U_0402_10V7K
PJP303
JUMP_43X118
PJP304
JUMP_43X118
PC317 0.1U_0603_25V7K
1.5VP
TDC 11A
Peak Current 16A
OCP current 19A
TYP MAX
H/S Rds(on) :23.2mohm , 27.8mohm
L/S Rds(on) :7mohm , 8.4mohm
+V1.05SP_B+
@PJP1100
JUMP_43X118
PC1100 0.1U_0402_25V6
PC1101 2200P_0402_50V7K
PC1102 4.7U_0805_25V6-K
PC1105 4.7U_0805_25V6-K
PQ1100
MDV1528URH_PDFN33-8-5
PU1100 @
RT8237EZQW(2)_WDFN10_3X3
PGOOD
TRIP
EN
VFB
RF
VBST
DRVH
SW
VSIN
DRVL
TP
BST_+1.5VGPU
UG_+1.5VGPU
SW_+1.5VGPU
+1.5VGPU_5V
LG_+1.5VGPU
PR1100 @ 0_0603_5%
BST_+1.5VGPU-1
PC1108 @ 0.22U_0603_10V7K
@PR1104 80.6K_0402_1%
TRIP_+1.5VGPU
EN_+1.5VGPU
FB_+1.5VGPU
RF_+1.5VGPU
@PR1101 100K_0402_5%
23,36,47,48 PX_MODE
@PR1107 1M_0402_5%
@PC1104 0.1U_0402_16V7K
@PR1106 470K_0402_1%
PC1107 @ 1U_0603_10V6K
+5VALW
@PL1100 1UH_PCMB053T-1R0MS_7A_20%
+1.5VGPUP
PC1103 @ 330U_2.5V_M
PQ1101
MDV1525URH_PDFN33-8-5
PR1102 4.7_1206_5%
SNB_1.5VGPUP
@PC1106 680P_0402_50V7K
@PR1105 11.5K_0402_1%
PR1103 @ 10K_0402_1%
+1.5VGPU
TDC 5.6A
Peak Current 8A
OCP current 9.6A
PJP1102 @
JUMP_43X118
Security Classification
Compal Secret Data
Issued Date
2012/03/14
Deciphered Date
2013/03/12
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Compal Electronics, Inc.
Title
PWR_+1.5VP/+1.5VGPUP/0.75VSP
Size
Document Number
LA-9103P
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0.1
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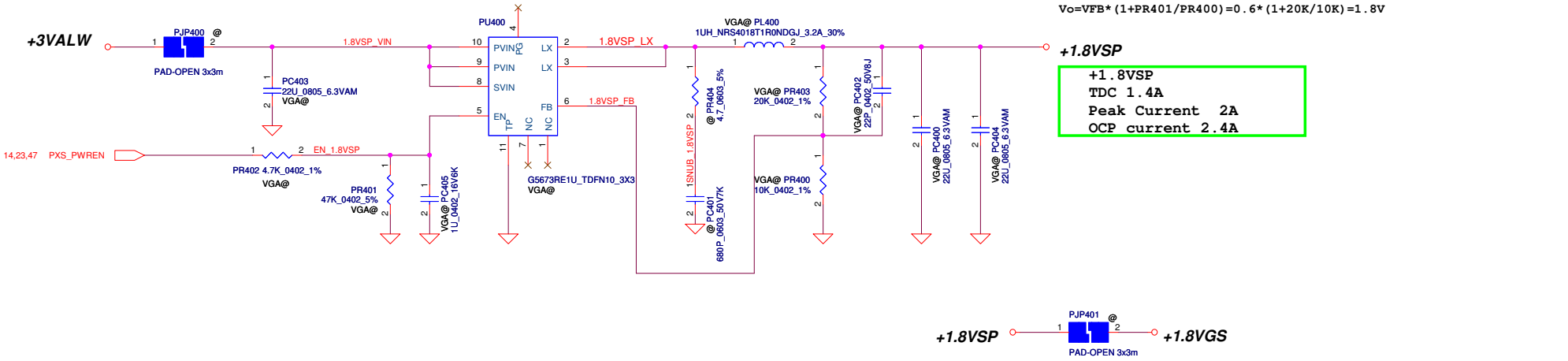
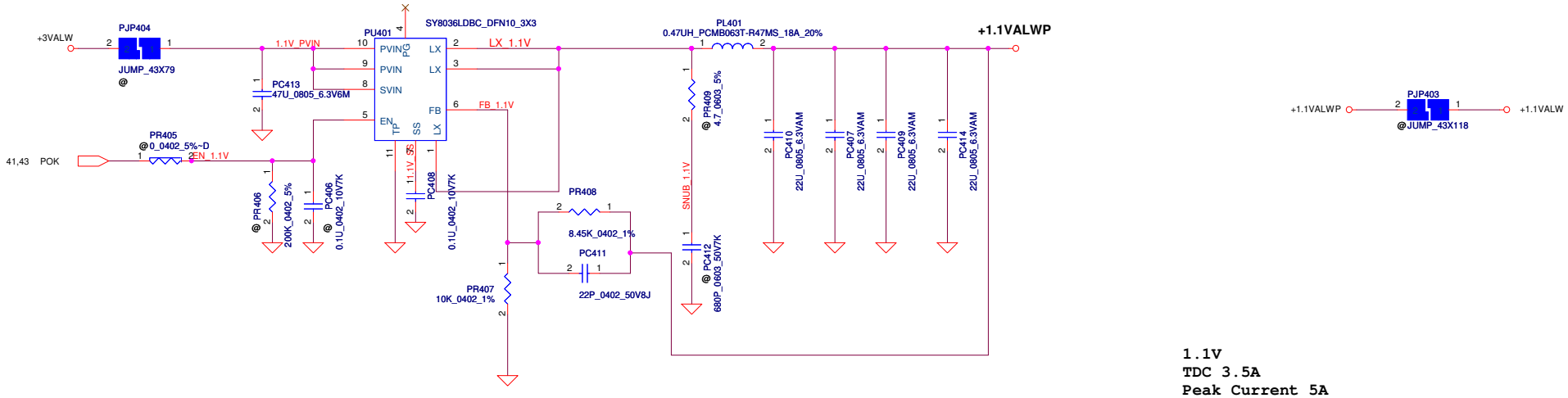




1.1V
TDC 3.5A
Peak Current 5A
OCP current 6A

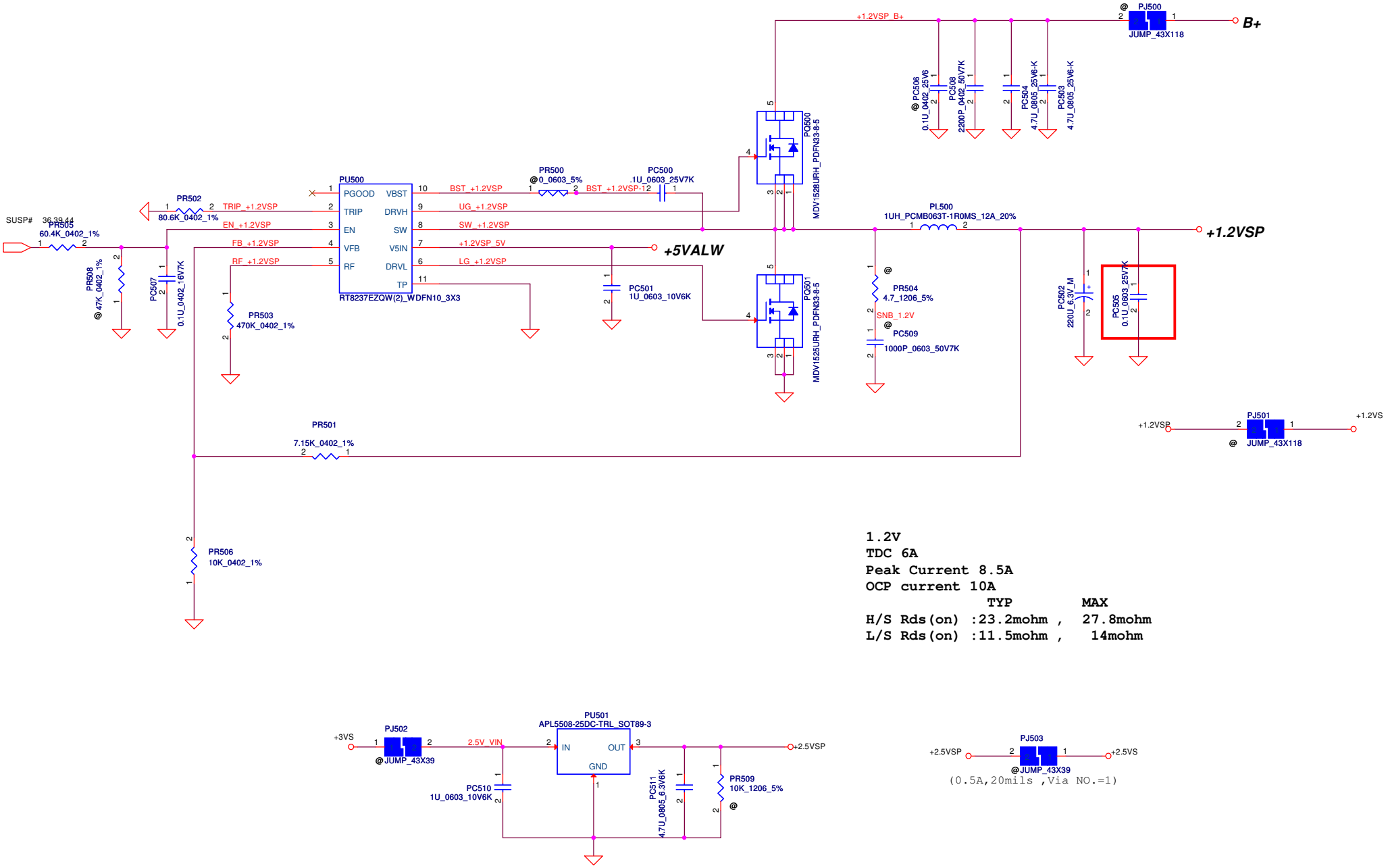
	TYP	MAX
H/S Rds(on)	:27mohm ,	34mohm
L/S Rds(on)	:11mohm ,	14mohm

Compal Electronics, Inc.

Title: PWR-1.8VSP/1.1VALWP

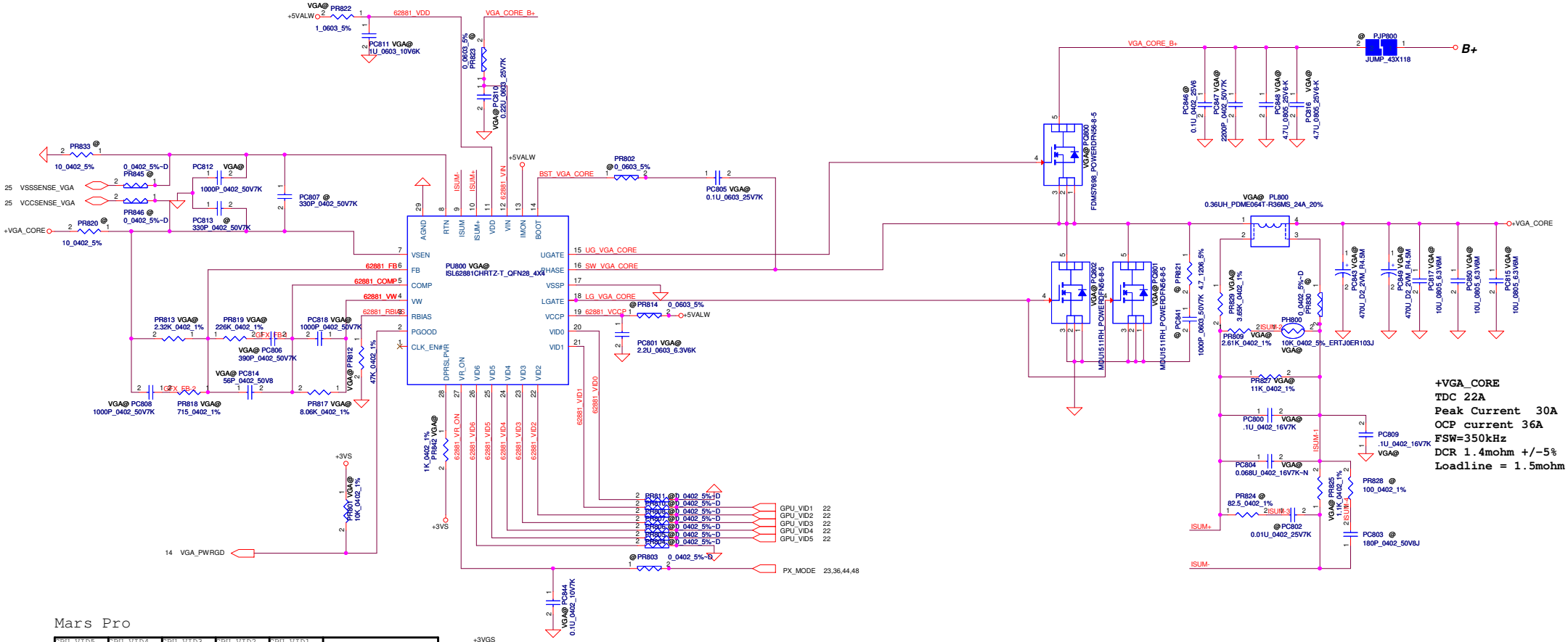
Size | Document Number: LA-9103P | Rev: 0.1

Date: Wednesday, July 10, 2013 | Sheet 45 of 52



Security Classification	Compal Secret Data		
Issued Date	2012/03/14	Deciphered Date	2013/03/12

Compal Electronics, Inc.			
Title	PWR-1.2VSP/2.5VSP		
Size	Document Number		Rev
	LA-9103P		0.1
Date:	Wednesday, July 10, 2013	Sheet	46 of 52



Mars Pro

GPU_VID5 (GPIO_10)	GPU_VID4 (GPIO_14)	GPU_VID3 (GPIO_15)	GPU_VID2 (GPIO_16)	GPU_VID1 (GPIO_20)	Core Voltage Level
0	1	1	1	1	1.125V
1	0	0	0	0	1.1V
1	0	0	0	1	1.075V
1	0	0	1	0	1.05V
1	0	0	1	1	1.025V
1	0	1	0	0	1V
1	0	1	0	1	0.975V
1	0	1	1	0	0.95V
1	0	1	1	1	0.925V
1	1	0	0	0	0.9V
1	1	0	0	1	0.875V
1	1	0	1	0	0.85V
1	1	0	1	1	0.825V
1	1	1	0	0	0.8V
1	1	1	0	1	0.775V

	Thames	Mars Pro
VGA_PCIE	1.0V	0.95V
PR832	6.81K	5.9K

Security Classification	Compal Secret Data		
Issued Date	2012/03/14	Deciphered Date	2013/03/12

Compal Electronics, Inc.

Title: PWR_VGA_CORE/VGA_PCIE

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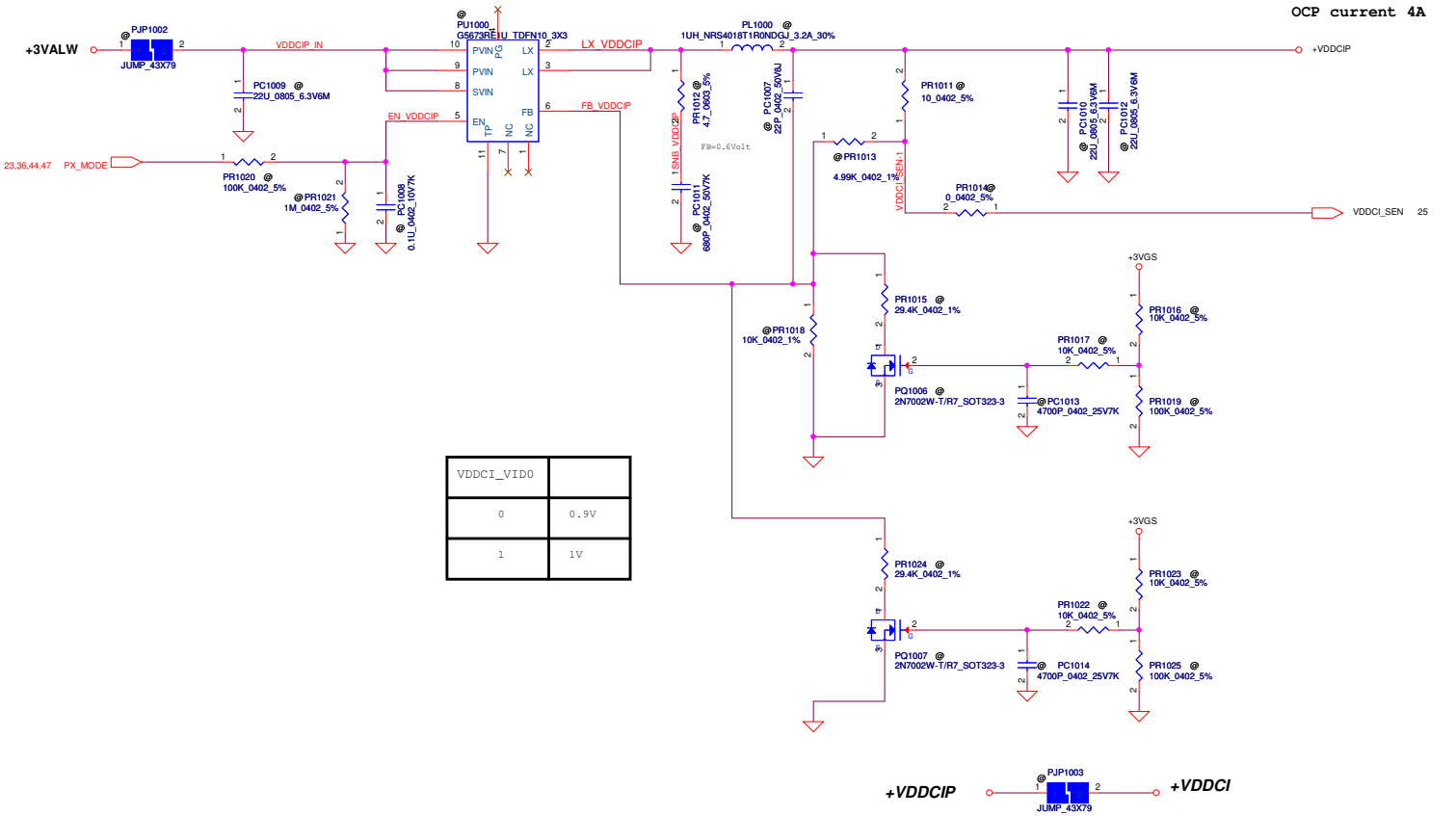
+VDDCI
TDC 1.5A
Peak Current 2.2A
OCP current 4A



VDDCI_VID0	
0	0.9V
1	1V

Compal Electronics, Inc.	
Title	PWR_+VDDCIP
Size	Document Number: LA-9103P
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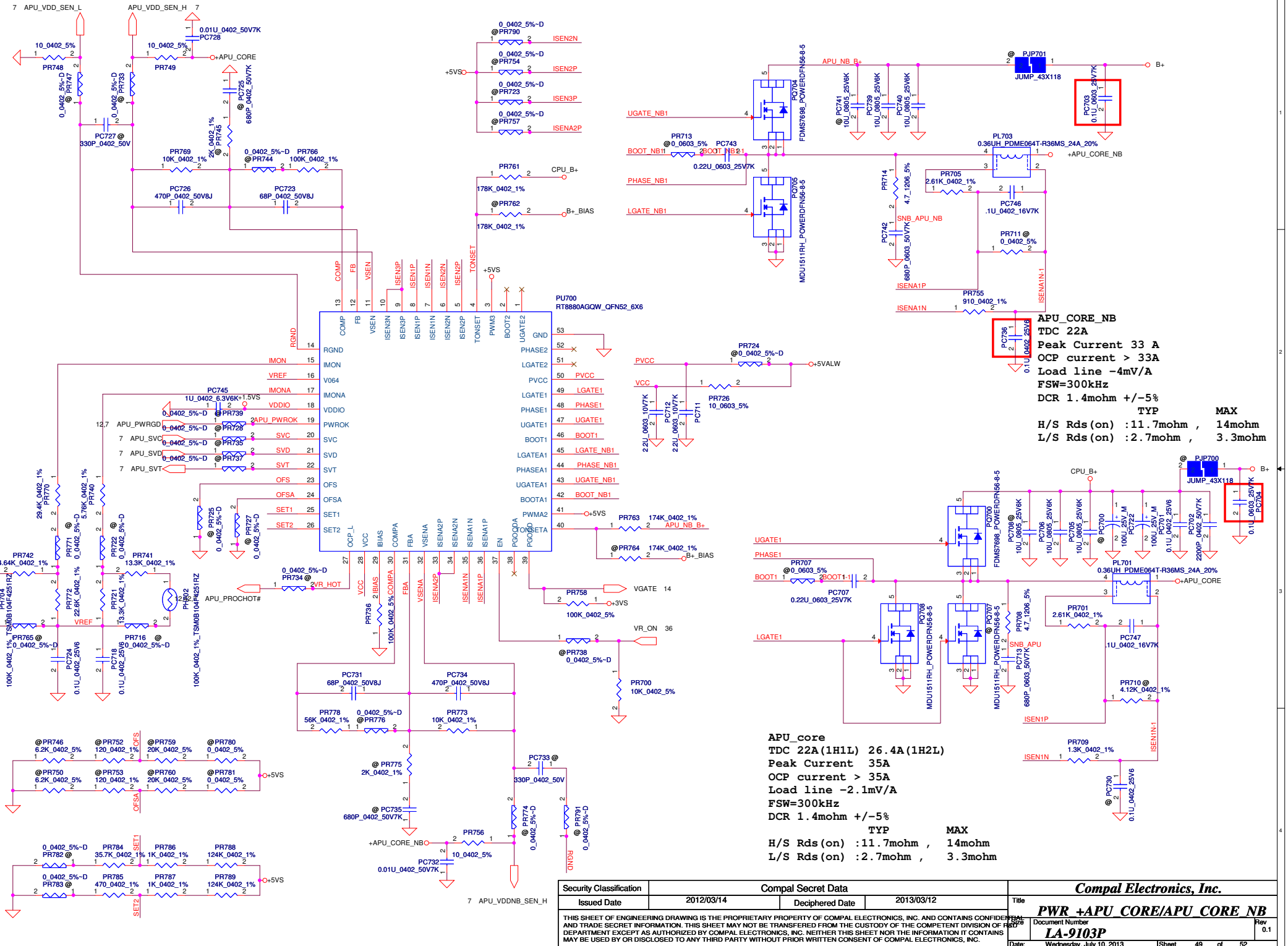

Security Classification	Compal Secret Data		
Issued Date	2012/03/14	Deciphered Date	2013/03/12

Compal Electronics, Inc.

Title: PWR_+APU_CORE/APU_CORE_NB

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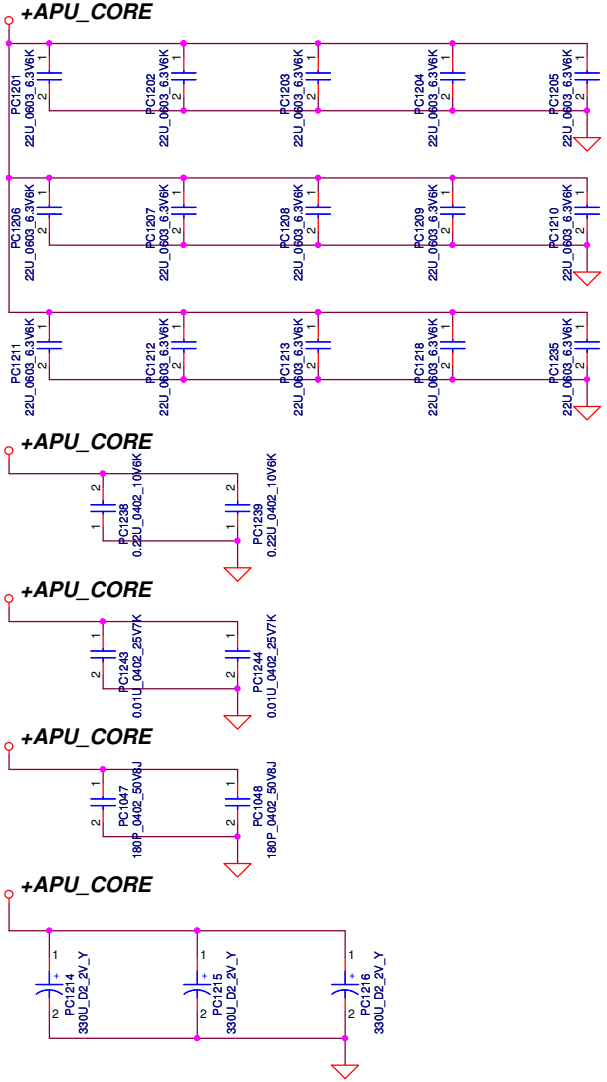
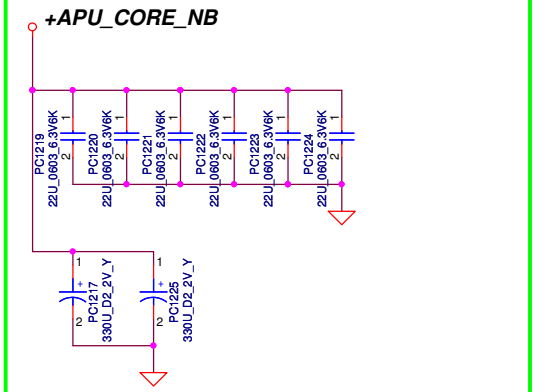
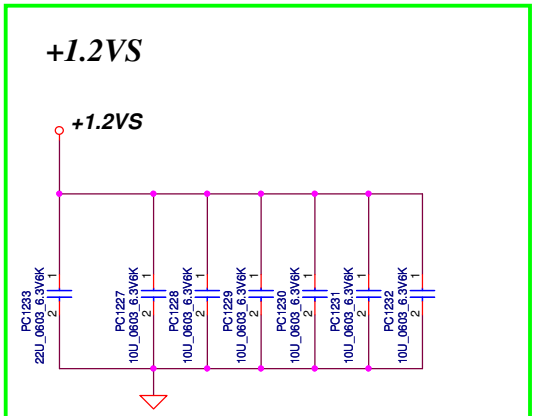
+APU_CORE



+APU_CORE_NB



+1.2VS



Security Classification	Compal Secret Data		
Issued Date	2012/03/14	Deciphered Date	2013/03/12

Compal Electronics, Inc.

Title: **PWR_PROCESSOR DECOUPLING**

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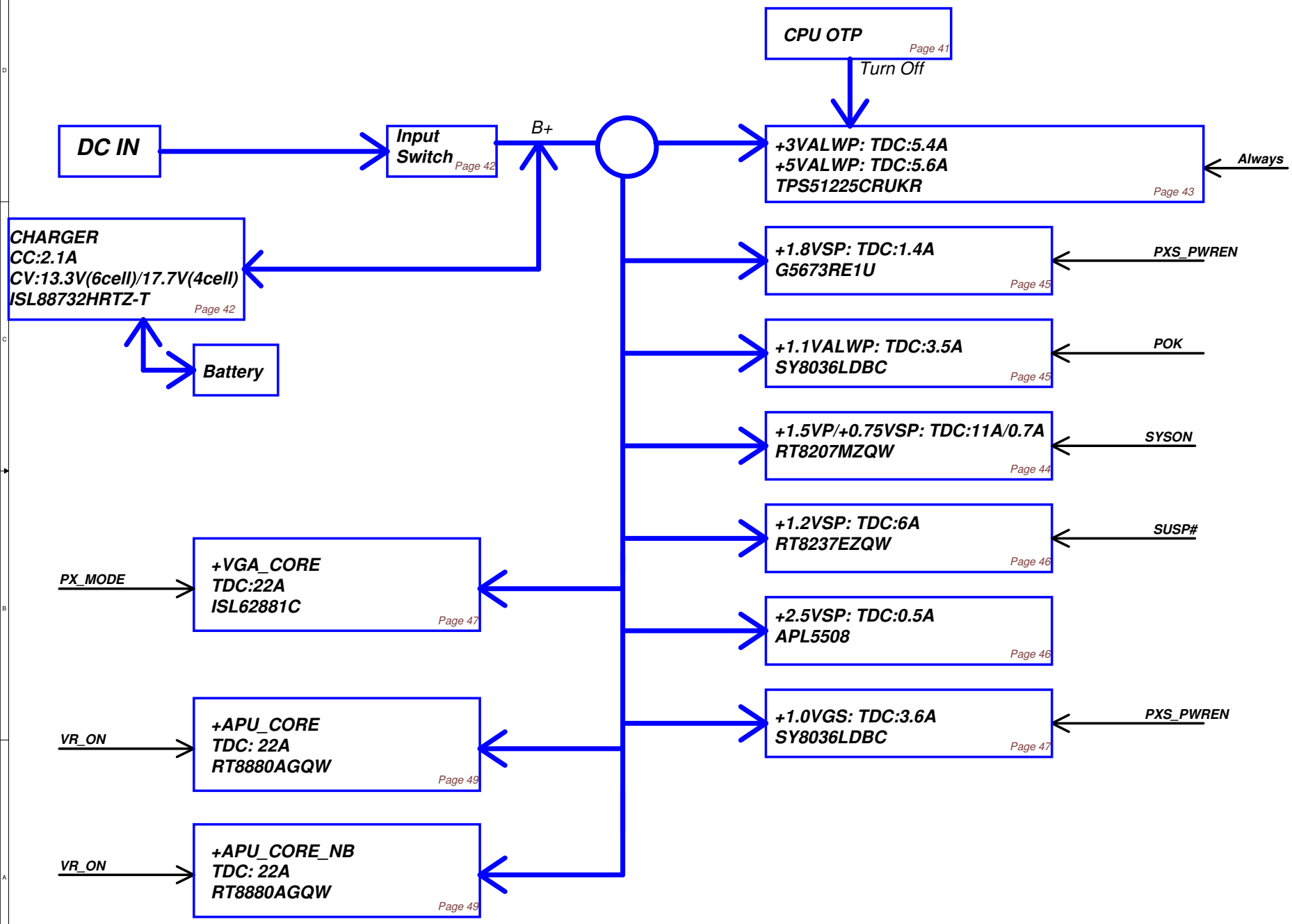
Power block



Security Classification	Compal Secret Data		
Issued Date	2012/03/14	Deciphered Date	2013/03/12

Compal Electronics, Inc.

Title: PWR_POWER BLOCK DIAGRAM

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Version Change List (P. I. R. List)

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	42	Charger	2013/07/08	Compal	EMI power noise.	Pop PC106 0.1uF for EMI requesst.	X01
2	44	+1.5VP	2013/07/08	Compal	EMI power noise/ESD issue.	Pop PR303 4.7ohm and PC312 680pF for EMI requesst. Add PC317 0.1uF for ESD request.	X01
3	49	+APU_CORE/APU_CORE_NB	2013/07/08	Compal	EMI power noise/ESD issue.	Add PR703 0.1uF and PC704 0.1uF for EMI requesst. Pop PC736 0.1uF for ESD request.	X01
4	46	+1.2VSP	2013/07/08	Compal	ESD issue.	Add PC505 0.1uF for ESD requesst.	X01
5	47	3.3VALWP/5VALWP	2013/07/08	Compal	ESD issue.	Add PC222,PC223,PC224,PC225,PC226,PC227 0.1uF for ESD requesst.	X01