Corsica\Gilligan - DISCRETE

M08 M/B PCB

VER : X02

POWER

- **SYSTEM RESET CIRCUIT** PG 38
- **BATT CHARGER** PG 40
- **RUN POWER SW** PG 39
  +3.3V_SUS/+5V_SUS/+3.3V_M
  +5V/+3.3V/+1.8V/+1.25_RUN
- **AC/BATT CONNECTOR** PG 41

Merom
(478 Micro-FCPGA)
PG 3,4
(Symbol Rev.09)

667/800 MHz FSB

POWER

- **REGULATOR** PG 43
  +1.5V_RUN/+1.05V_VCCP
- **REGULATOR** PG 42
  +1.25V/+1.8V_SUS/+0.9V_DDR_VTT
- **CPU VR** PG 45
- **DC/DC** PG 44
  +3.3V_ALW/+5V_ALW/+15V_ALW

CLOCK
CK505M+LP
PG 17

Crestline
1299 uFCBGA
PG 5,6,7,8,9,10
(Symbol Rev.09)

- **DDR2-SODIMM1** PG 15,16 — 533/667 MHZ DDR II
- **DDR2-SODIMM2** PG 15,16 — 533/667 MHZ DDR II

PCIEx16 → **VGA CONN. PCI EXPRESS GFX** PG 18

- LVDS → **Panel Connector**
- TVOUT → **S-Video** PG 19
- VGA → **CRT CONN.** PG 19

USB2.0 (P5) → **Camera** PG 33

DMI interface

ICH8-M
676 BGA
PG 11,12,13,14
(Symbol Rev.09)

- IDE → **CD-ROM** PG 23
- SATA0 → **SATA - HDD** PG 23
- SATA1 → **SATA - HDD** PG 23
- IHDA → **AUDIO/AMP** PG 32, **MDC**, **CONN** PG 26
  - **D-Micro** PG 33
  - **Audio Jacks** PG 33
  - **Tip Ring**

LAN
BCM4401 (B0)
+3.3V_LAN
PG 35
(Symbol Rev.09)

33MHz PCI → **RJ45/Magnetics** PG 36

33MHz PCI → **CARDBUS/1394**
R5C833
PG 20,21,22

PCIEx1 / USB2.0 (P6) → **EXPRESS-CARD**
R5538
PG 26

PCIEx1 / USB2.0 (P9) → **MINI-CARD x1**
WWAN
PG 25

PCIEx2 / USB2.0 (P7) → **MINI-CARD x2**
WLAN
PG 24

USB2.0 (P0,P2) (EXT SIDE)
USB2.0 (P3,P8) (EXT BACK) → **External USB** PG 27

SPI

LPC

SIO
MEC5025
128KB Flash
TMKBC
128 Pins VTQFP
PG 28

BC

SIO
ECE5011
Expander
USB 2.0 Hub(4)
128 Pins VTQFP
PG 29

SPI → **FLASH** PG 30

CIR PG 31

FAN & THERMAL
EMC4001
PG 34

BC
PS/2

- **Dash BD**
- **KB**
- **Touchpad**
- **Media BD**

TP/KB & Media/Dash BD Conn
PG 31

C G
31FM5MB0011 31GM2MB0004
41FM5SS0017 41GM2SS0000

QUANTA COMPUTER

Title	Schematic Block Diagram1	
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Pg#	Description	DNI LIST
1	Schematic Block Diagram	
2	Front Page	
3-4	Merom	
5-10	Crestline	
11-14	ICH8M	
15-16	DDRII SO-DIMM(200P)	
17	Clock Generator	
18-21	VGA	
22	LCD Conn. & SSP	
23	CRT Conn	
24	SATA & IDE Conn	
25	PCCARD/Conn & 1394	
26	Express Card & Smart Card	
27	Mini Card	
28	MDC Conn.	
29	SIO (MEC5004)	
30	SIO (MEC5018)	
31	SERIAL PORT & USB	
32	Flash ROM	
33	TP,BT & FIR	
34	Switch,Keyboard & LED	
35	FAN & Thermal	
36-37	Audio CODEC(STAC9200)/Phone Jack	
38-39	LOM (BCM5752)/Switch	
40-41	Docking Conn/Q-Switch	
42	System Reset Circuit	
43-44	Battery Selector & Charger	
45	DDR2_1.8VSUS, 0.9V	
46	1.5VSUS,1.05V(VTT)	
47	1.25V,1.05VM	
48	CPU_MAX8786(3phase)	
49	D/D Power	
50	RUN Power Switch	
51	VGA DC/DC	
52	DCIN/Batt Conn.	
53	PAD& SCREW	
54	EMI CAP	

Power & Ground

Label	Pg#	Description	Control Signal
DC_IN+		AC ADAPTER (19V)	
PBATT+		MAIN BATTERY + (10~17V)	
PBATT+		SECOND BATTERY + (10~17V)	
PWR_SRC		MAIN POWER (10~19V)	
RTC_PWR3_3V		RTC & +3.3V_RTC_LDO(3.3V)	
+VCC_CORE		CPU CORE POWER (1.5V)	RUNPWROK
+15V_ALW		LARGE POWER (15V)	SUS_ON
+3.3V_RUN		SLP_S3# CTRLD POWER	RUN_ON
+3.3V_SUS		SLP_S5# CTRLD POWER	SUS_ENABLE
+3.3V_ALW		8051 POWER (3.3V)	ALWON/THERM_STP#
+5V_RUN		SLP_S3# CTRLD POWER	RUN_ON
+5V_SUS		SLP_S5# CTRLD POWER	SUS_ON
+5V_HDD		HDD POWER (5V)	+5V_RUN
+5V_MOD		MODULE POWER (5V)	HDDC_EN
+5V_ALW		LCD/CHARGE POWER (5V)	
+VDDA		AUDIO ANALOG POWER (5V)	AUDIO_AVDD_ON
+1.5V_RUN		CALISTOGA/ICH7 POWER	RUN_ON
+1.05V_VCCP		CPU/CALISTOGA/ICH7 POWER	RUN_ON
+1_8V_SUS		SODIMM POWER	SUSPWROK_5V
+1.8V_RUN		SDVO POWER	RUN_ON
+0.9V_DDR_VTT		SODIMM POWER	RUN_ON
+3.3V_LAN		LAN POWER	AUX_EN
GND	ALL PAGES	DIGITAL GROUND	
AGND_ISL6260		CPU GND	
AGND_TPS51120		DC/DC POWER GND	
AGND1		VTT POWER GND	
AGND2		VTT POWER GND	
8731AGND		CHARGER GND	

QUANTA COMPUTER

Title	Index, DNI, Power & Ground	
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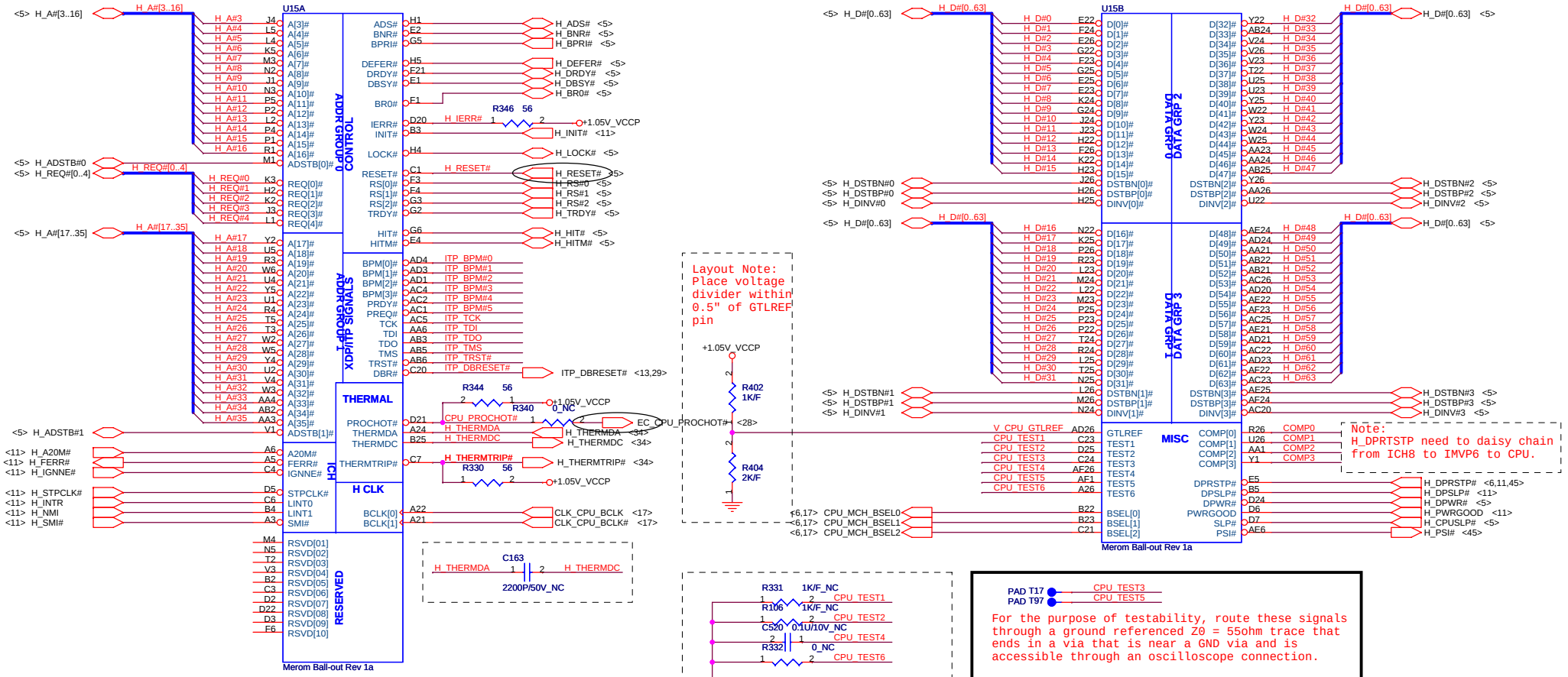

Populate ITP700Flex for bringup

For Support XDP:
1. ITP_BPM#5 need PU 51ohms to +1.05V_VCCP.
2. Change R4 & R361 to 51 ohms.
3. Changed R6 & R346 to 51 ohms.
4. Depopulate R2 and changed R8 to 1K/F.

Layout Note: Place couple 0.1uF Decoupling caps with in 0.1" ITP connector.

Layout Note: Place R8 close ITP.

Reserved for support XDP debug.

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

ITP700 layout guidelines

Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm ± 5%	VCCP	Place the pull-up near CPU
TMS	39 ohm ± 1%	VCCP	Within 200ps of ITP connector
TRST#	500 to 680 ohm ± 5%	GND	Place the pull-down near CPU
TCK	27 ohm ± 1%	GND	Connect to TCK pin of CPU and then connect it to FBO pin of ITP connector in daisy chain. Place the pull-down near TCK0 pin of ITP connector
TDO	51 ohm ± 5%	VCCP	Place the pull-up near ITP
RESET#	22.6 ohm ± 1% series resistor and pullup 51 ohm ± 1%.	VCCP	Connect to CPURST# pin of GMCH through the series resistor placed within 200ps of ITP connector. Place the pull-up after the series resistor from ITP connector.

DELL CONFIDENTIAL/PROPRIETARY

Title	Merom Processor (HOST BUS)	
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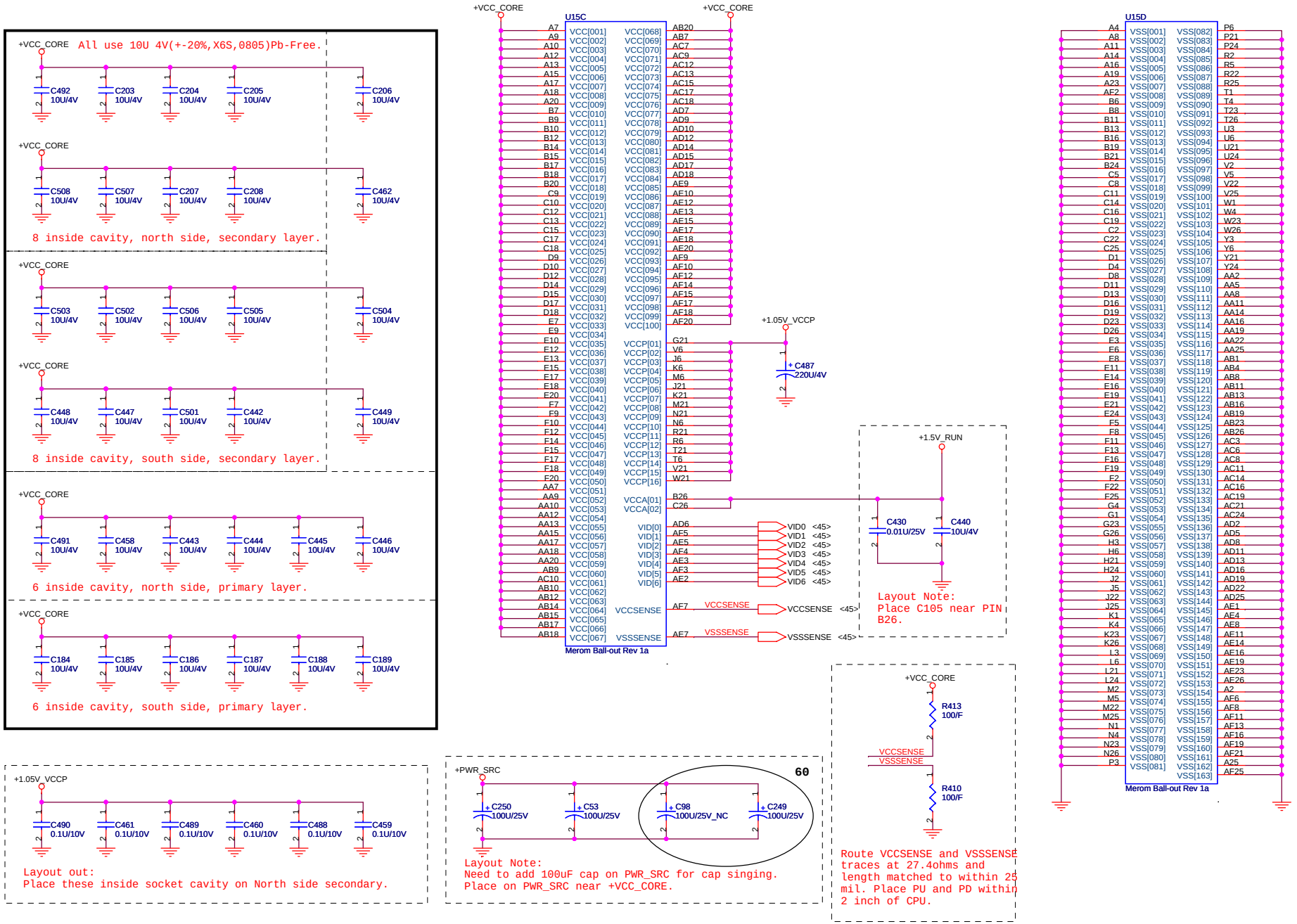
All use 10U 4V(+-20%,X6S,0805)Pb-Free.
8 inside cavity, north side, secondary layer.
8 inside cavity, south side, secondary layer.
6 inside cavity, north side, primary layer.
6 inside cavity, south side, primary layer.
Layout out:
Place these inside socket cavity on North side secondary.
U15C
Merom Ball-out Rev 1a
U15D
Merom Ball-out Rev 1a
Layout Note:
Place C105 near PIN B26.
Layout Note:
Need to add 100uF cap on PWR_SRC for cap singing.
Place on PWR_SRC near +VCC_CORE.
Route VCCSENSE and VSSSENSE traces at 27.4ohms and length matched to within 25 mil. Place PU and PD within 2 inch of CPU.
DELL CONFIDENTIAL/PROPRIETARY
Merom Processor (POWER)
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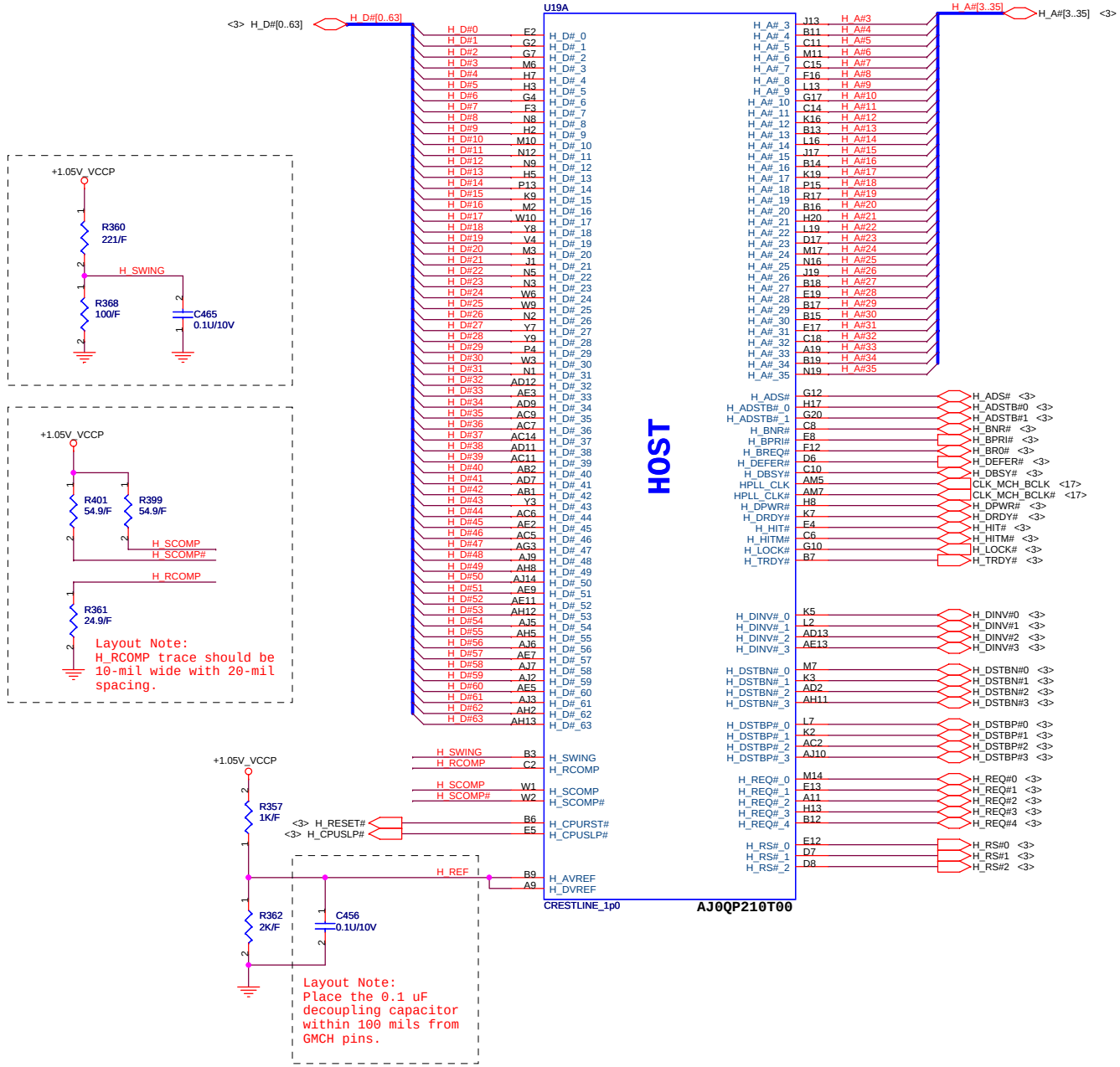

DELL CONFIDENTIAL/PROPRIETARY

Title: Crestline (HOST)		
Size	Document Number: M-08	Rev: 0.1
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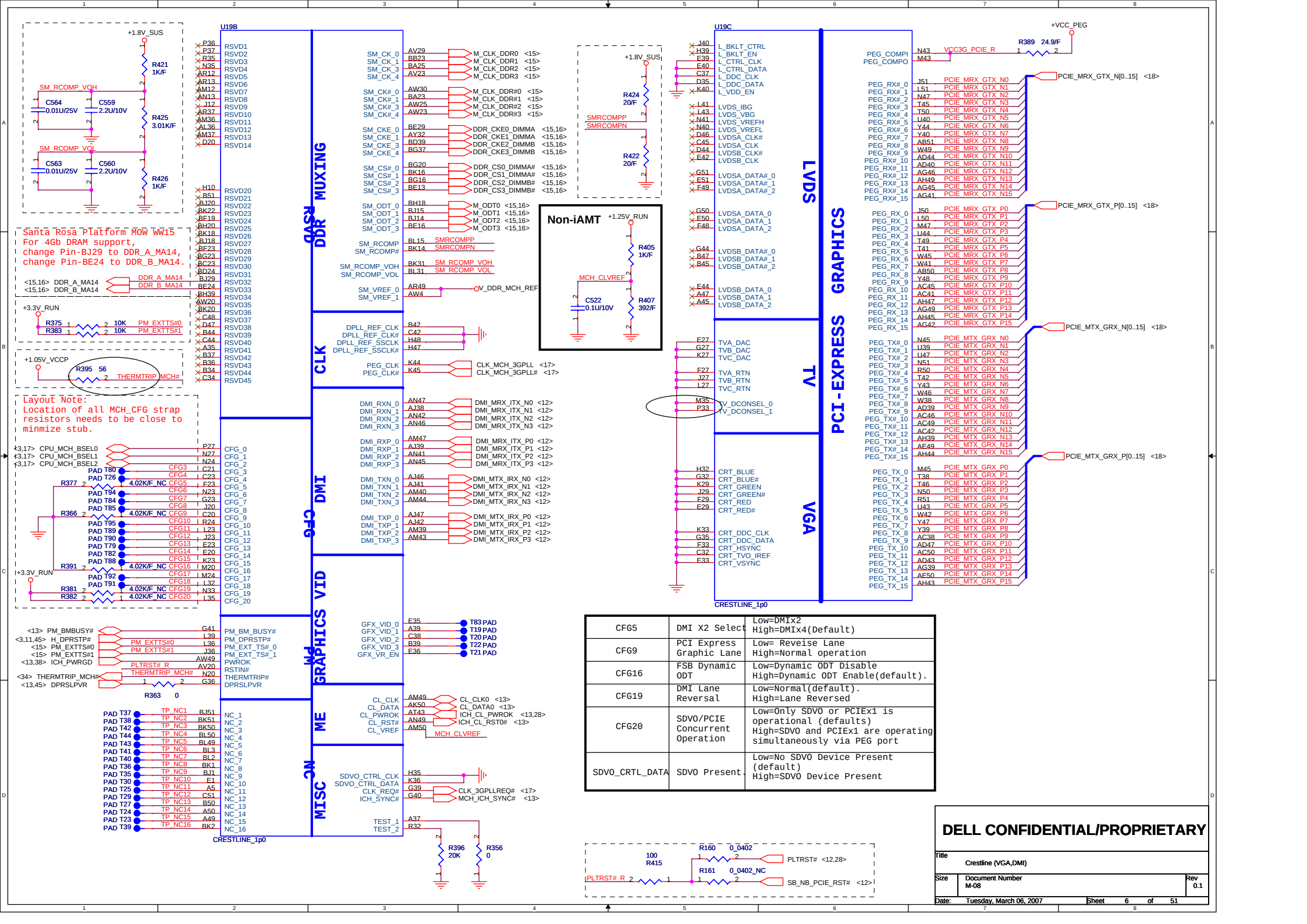
U19B
U19C
+1.8V_SUS
R421 1K/F
R425 3.01K/F
R426 1K/F
C564 0.01U/25V
C559 2.2U/10V
C563 0.01U/25V
C560 2.2U/10V
SM_RCOMP_VOH
SM_RCOMP_VOL
Santa Rosa Platform MOW WW15
For 4Gb DRAM support,
change Pin-BJ29 to DDR_A_MA14,
change Pin-BE24 to DDR_B_MA14.
+3.3V_RUN
R375 10K PM_EXTTS#0
R383 10K PM_EXTTS#1
+1.05V_VCCP
R395 56
THERMTRIP_MCH#
Layout Note:
Location of all MCH_CFG strap
resistors needs to be close to
minmize stub.
CFG_0
CFG_1
CFG_2
CFG_3
CFG_4
CFG_5
CFG_6
CFG_7
CFG_8
CFG_9
CFG_10
CFG_11
CFG_12
CFG_13
CFG_14
CFG_15
CFG_16
CFG_17
CFG_18
CFG_19
CFG_20
R377 4.02K/F_NC
R366 4.02K/F_NC
R391 4.02K/F_NC
R381 4.02K/F_NC
R382 4.02K/F_NC
PM_BM_BUSY#
PM_DPRSTP#
PM_EXT_TS#_0
PM_EXT_TS#_1
PWROK
RSTIN#
THERMTRIP#
DPRSLPVR
R363 0
NC_1
NC_2
NC_3
NC_4
NC_5
NC_6
NC_7
NC_8
NC_9
NC_10
NC_11
NC_12
NC_13
NC_14
NC_15
NC_16
CRESTLINE_1p0
RSVD1
RSVD2
RSVD3
RSVD4
RSVD5
RSVD6
RSVD7
RSVD8
RSVD9
RSVD10
RSVD11
RSVD12
RSVD13
RSVD14
RSVD20
RSVD21
RSVD22
RSVD23
RSVD24
RSVD25
RSVD26
RSVD27
RSVD28
RSVD29
RSVD30
RSVD31
RSVD32
RSVD33
RSVD34
RSVD35
RSVD36
RSVD37
RSVD38
RSVD39
RSVD40
RSVD41
RSVD42
RSVD43
RSVD44
RSVD45
DDR_A_MA14
DDR_B_MA14
DDR MUXING
CLK
DMI
CFG
GRAPHICS VID
PM
ME
MISC
NC
SM_CK_0
SM_CK_1
SM_CK_3
SM_CK_4
SM_CK#_0
SM_CK#_1
SM_CK#_3
SM_CK#_4
SM_CKE_0
SM_CKE_1
SM_CKE_3
SM_CKE_4
SM_CS#_0
SM_CS#_1
SM_CS#_2
SM_CS#_3
SM_ODT_0
SM_ODT_1
SM_ODT_2
SM_ODT_3
SM_RCOMP
SM_RCOMP#
SM_RCOMP_VOH
SM_RCOMP_VOL
SM_VREF_0
SM_VREF_1
M_CLK_DDR0 <15>
M_CLK_DDR1 <15>
M_CLK_DDR2 <15>
M_CLK_DDR3 <15>
M_CLK_DDR#0 <15>
M_CLK_DDR#1 <15>
M_CLK_DDR#2 <15>
M_CLK_DDR#3 <15>
DDR_CKE0_DIMMA <15,16>
DDR_CKE1_DIMMA <15,16>
DDR_CKE2_DIMMB <15,16>
DDR_CKE3_DIMMB <15,16>
DDR_CS0_DIMMA# <15,16>
DDR_CS1_DIMMA# <15,16>
DDR_CS2_DIMMB# <15,16>
DDR_CS3_DIMMB# <15,16>
M_ODT0 <15,16>
M_ODT1 <15,16>
M_ODT2 <15,16>
M_ODT3 <15,16>
SMRCOMPP
SMRCOMPN
SM_RCOMP_VOH
SM_RCOMP_VOL
V_DDR_MCH_REF
DPLL_REF_CLK
DPLL_REF_CLK#
DPLL_REF_SSCLK
DPLL_REF_SSCLK#
PEG_CLK
PEG_CLK#
CLK_MCH_3GPLL <17>
CLK_MCH_3GPLL# <17>
DMI_RXN_0
DMI_RXN_1
DMI_RXN_2
DMI_RXN_3
DMI_RXP_0
DMI_RXP_1
DMI_RXP_2
DMI_RXP_3
DMI_TXN_0
DMI_TXN_1
DMI_TXN_2
DMI_TXN_3
DMI_TXP_0
DMI_TXP_1
DMI_TXP_2
DMI_TXP_3
DMI_MRX_ITX_N0 <12>
DMI_MRX_ITX_N1 <12>
DMI_MRX_ITX_N2 <12>
DMI_MRX_ITX_N3 <12>
DMI_MRX_ITX_P0 <12>
DMI_MRX_ITX_P1 <12>
DMI_MRX_ITX_P2 <12>
DMI_MRX_ITX_P3 <12>
DMI_MTX_IRX_N0 <12>
DMI_MTX_IRX_N1 <12>
DMI_MTX_IRX_N2 <12>
DMI_MTX_IRX_N3 <12>
DMI_MTX_IRX_P0 <12>
DMI_MTX_IRX_P1 <12>
DMI_MTX_IRX_P2 <12>
DMI_MTX_IRX_P3 <12>
GFX_VID_0
GFX_VID_1
GFX_VID_2
GFX_VID_3
GFX_VR_EN
T83 PAD
T19 PAD
T20 PAD
T22 PAD
T21 PAD
CL_CLK
CL_DATA
CL_PWROK
CL_RST#
CL_VREF
CL_CLK0 <13>
CL_DATA0 <13>
ICH_CL_PWROK <13,28>
ICH_CL_RST0# <13>
MCH_CLVREF
SDVO_CTRL_CLK
SDVO_CTRL_DATA
CLK_REQ#
ICH_SYNC#
CLK_3GPLLREQ# <17>
MCH_ICH_SYNC# <13>
TEST_1
TEST_2
R396 20K
R356 0
Non-iAMT
+1.25V_RUN
R405 1K/F
MCH_CLVREF
C522 0.1U/10V
R407 392/F
R424 20/F
R422 20/F
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
L_BKLT_CTRL
L_BKLT_EN
L_CTRL_CLK
L_CTRL_DATA
L_DDC_CLK
L_DDC_DATA
L_VDD_EN
LVDS_IBG
LVDS_VBG
LVDS_VREFH
LVDS_VREFL
LVDSA_CLK#
LVDSA_CLK
LVDSB_CLK#
LVDSB_CLK
LVDSA_DATA#_0
LVDSA_DATA#_1
LVDSA_DATA#_2
LVDSA_DATA_0
LVDSA_DATA_1
LVDSA_DATA_2
LVDSB_DATA#_0
LVDSB_DATA#_1
LVDSB_DATA#_2
LVDSB_DATA_0
LVDSB_DATA_1
LVDSB_DATA_2
TVA_DAC
TVB_DAC
TVC_DAC
TVA_RTN
TVB_RTN
TVC_RTN
TV_DCONSEL_0
TV_DCONSEL_1
CRT_BLUE
CRT_BLUE#
CRT_GREEN
CRT_GREEN#
CRT_RED
CRT_RED#
CRT_DDC_CLK
CRT_DDC_DATA
CRT_HSYNC
CRT_TVO_IREF
CRT_VSYNC
PEG_COMPI
PEG_COMPO
+VCC_PEG
R389 24.9/F
VCC3G_PCIE_R
PCIE_MRX_GTX_N[0..15] <18>
PCIE_MRX_GTX_P[0..15] <18>
PCIE_MTX_GRX_N[0..15] <18>
PCIE_MTX_GRX_P[0..15] <18>
PEG_RX#_0
PEG_RX#_1
PEG_RX#_2
PEG_RX#_3
PEG_RX#_4
PEG_RX#_5
PEG_RX#_6
PEG_RX#_7
PEG_RX#_8
PEG_RX#_9
PEG_RX#_10
PEG_RX#_11
PEG_RX#_12
PEG_RX#_13
PEG_RX#_14
PEG_RX#_15
PEG_RX_0
PEG_RX_1
PEG_RX_2
PEG_RX_3
PEG_RX_4
PEG_RX_5
PEG_RX_6
PEG_RX_7
PEG_RX_8
PEG_RX_9
PEG_RX_10
PEG_RX_11
PEG_RX_12
PEG_RX_13
PEG_RX_14
PEG_RX_15
PEG_TX#_0
PEG_TX#_1
PEG_TX#_2
PEG_TX#_3
PEG_TX#_4
PEG_TX#_5
PEG_TX#_6
PEG_TX#_7
PEG_TX#_8
PEG_TX#_9
PEG_TX#_10
PEG_TX#_11
PEG_TX#_12
PEG_TX#_13
PEG_TX#_14
PEG_TX#_15
PEG_TX_0
PEG_TX_1
PEG_TX_2
PEG_TX_3
PEG_TX_4
PEG_TX_5
PEG_TX_6
PEG_TX_7
PEG_TX_8
PEG_TX_9
PEG_TX_10
PEG_TX_11
PEG_TX_12
PEG_TX_13
PEG_TX_14
PEG_TX_15
CRESTLINE_1p0
R160 0_0402
R161 0_0402_NC
R415 100
PLTRST# <12,28>
SB_NB_PCIE_RST# <12>
PLTRST# R
CFG5 | DMI X2 Select | Low=DMIx2 High=DMIx4(Default)
CFG9 | PCI Express Graphic Lane | Low= Reveise Lane High=Normal operation
CFG16 | FSB Dynamic ODT | Low=Dynamic ODT Disable High=Dynamic ODT Enable(default).
CFG19 | DMI Lane Reversal | Low=Normal(default). High=Lane Reversed
CFG20 | SDVO/PCIE Concurrent Operation | Low=Only SDVO or PCIEx1 is operational (defaults) High=SDVO and PCIEx1 are operating simultaneously via PEG port
SDVO_CRTL_DATA | SDVO Present. | Low=No SDVO Device Present (default) High=SDVO Device Present
DELL CONFIDENTIAL/PROPRIETARY
Title
Crestline (VGA,DMI)
Size
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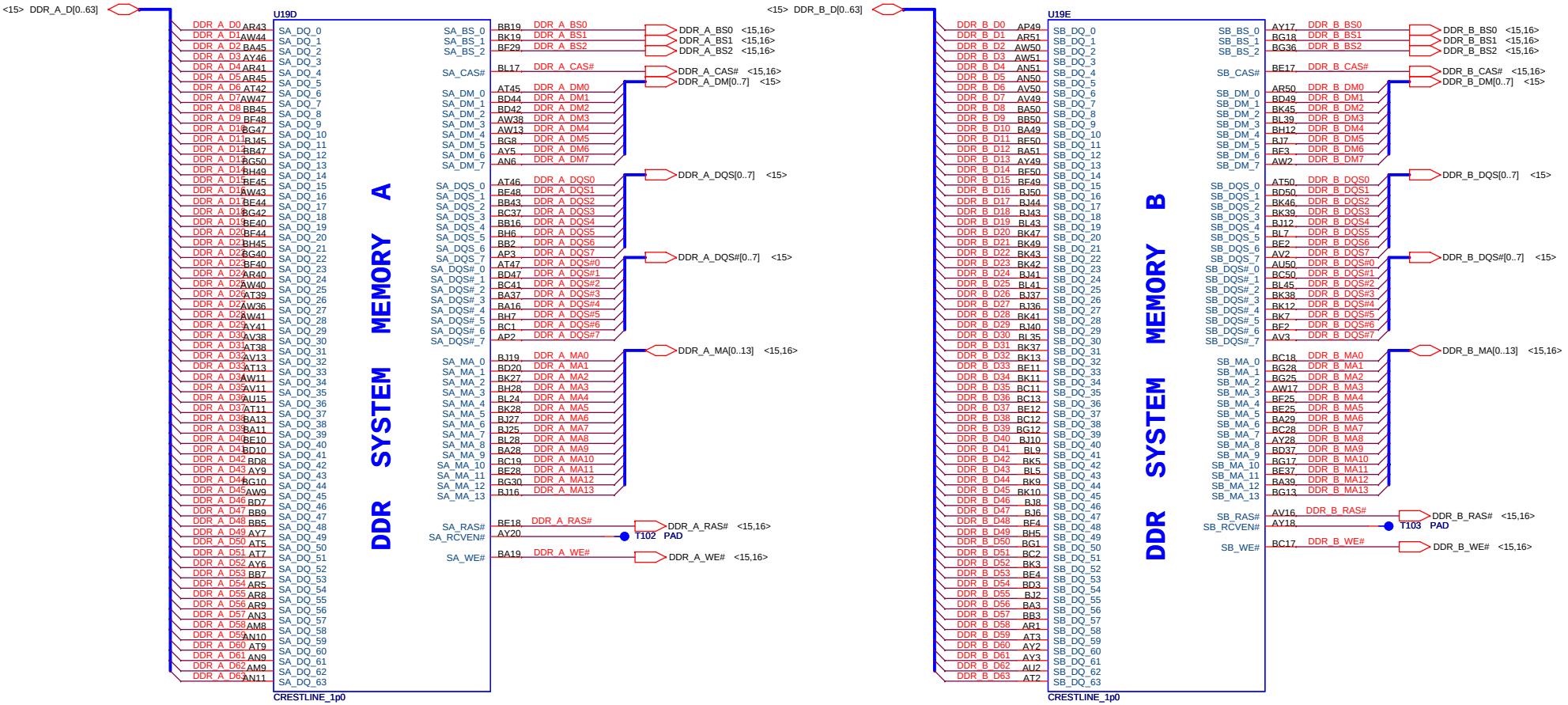

DELL CONFIDENTIAL/PROPRIETARY

Title	Crestline (DDR2)	
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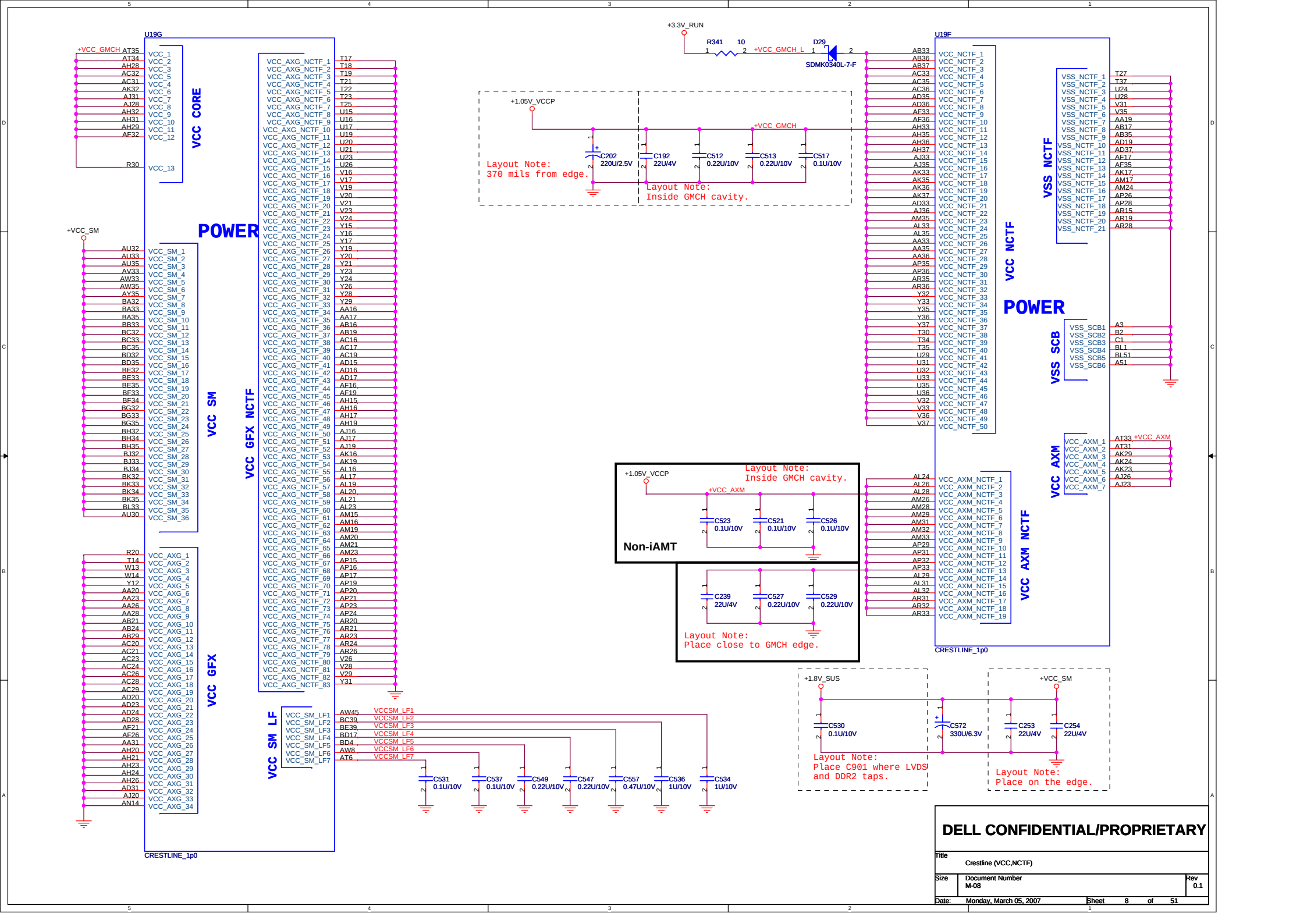
U19G
VCC CORE
POWER
VCC SM
VCC GFX NCTF
VCC GFX
VCC SM LF
CRESTLINE_1p0
U19F
VCC NCTF
VSS NCTF
VSS SCB
VCC AXM
VCC AXM NCTF
+3.3V_RUN
R341 10
D29
SDMK0340L-7-F
+VCC_GMCH_L
+1.05V_VCCP
+VCC_GMCH
Layout Note:
370 mils from edge.
Layout Note:
Inside GMCH cavity.
C202 220U/2.5V
C192 22U/4V
C512 0.22U/10V
C513 0.22U/10V
C517 0.1U/10V
+VCC_SM
+VCC_AXM
Non-iAMT
C523 0.1U/10V
C521 0.1U/10V
C526 0.1U/10V
C239 22U/4V
C527 0.22U/10V
C529 0.22U/10V
Layout Note:
Place close to GMCH edge.
+1.8V_SUS
C530 0.1U/10V
C572 330U/6.3V
C253 22U/4V
C254 22U/4V
Layout Note:
Place C901 where LVDS
and DDR2 taps.
Layout Note:
Place on the edge.
C531 0.1U/10V
C537 0.1U/10V
C549 0.22U/10V
C547 0.22U/10V
C557 0.47U/10V
C536 1U/10V
C534 1U/10V
DELL CONFIDENTIAL/PROPRIETARY
Title
Crestline (VCC,NCTF)
Size
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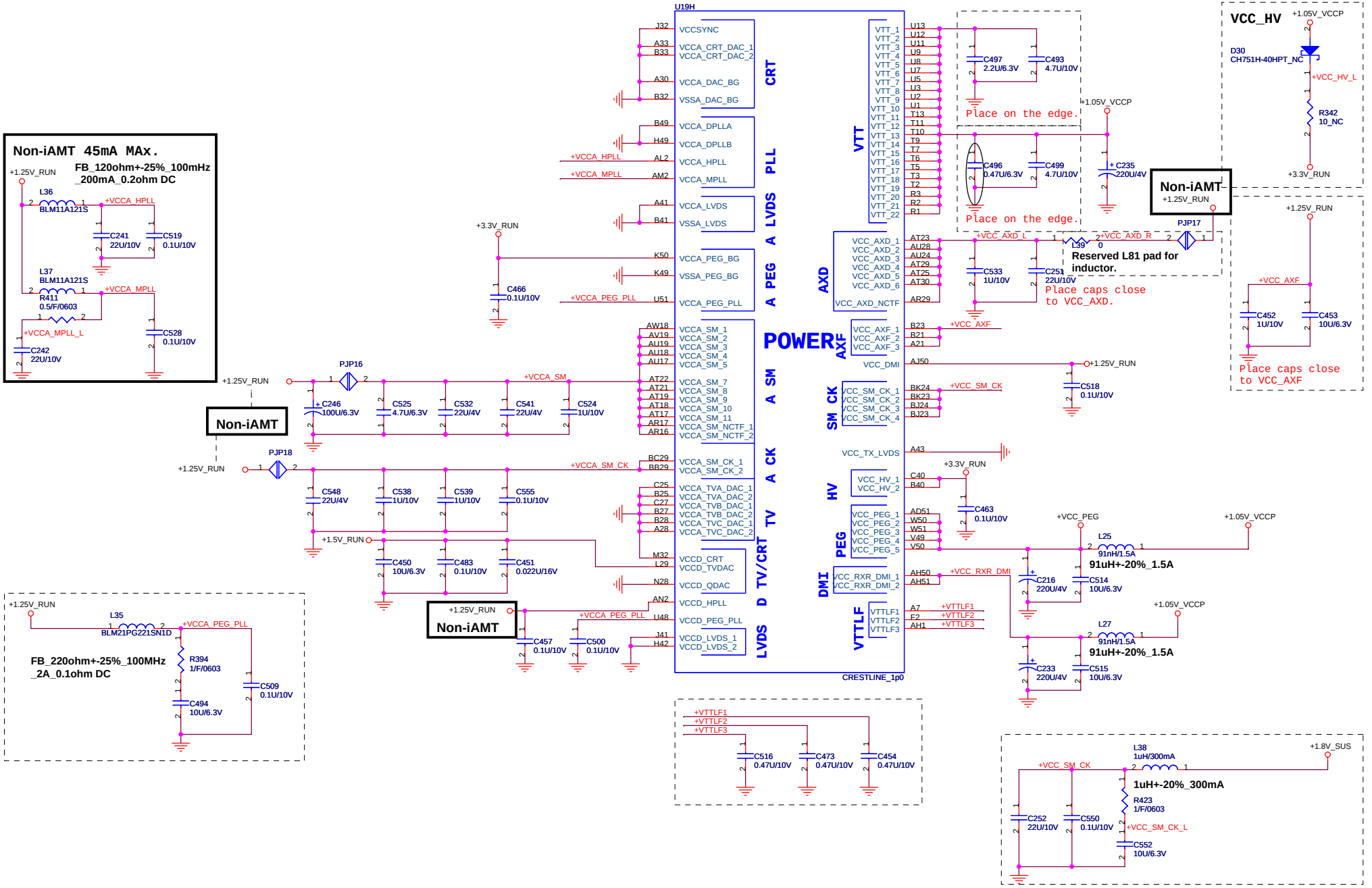
U19H
CRESTLINE_1p0
POWER
CRT
PLL
LVDS
PEG
SM CK
TV/CRT
DMI
VTTLF
VTT
AXD
AXF
HV
Non-iAMT 45mA MAx.
FB_120ohm+-25%_100mHz _200mA_0.2ohm DC
Non-iAMT
Non-iAMT
Non-iAMT
FB_220ohm+-25%_100MHz _2A_0.1ohm DC
Place on the edge.
Place on the edge.
Place caps close to VCC_AXD.
Place caps close to VCC_AXF
Reserved L81 pad for inductor.
VCC_HV
D30 CH751H-40HPT_NC
91uH+-20%_1.5A
91uH+-20%_1.5A
1uH+-20%_300mA
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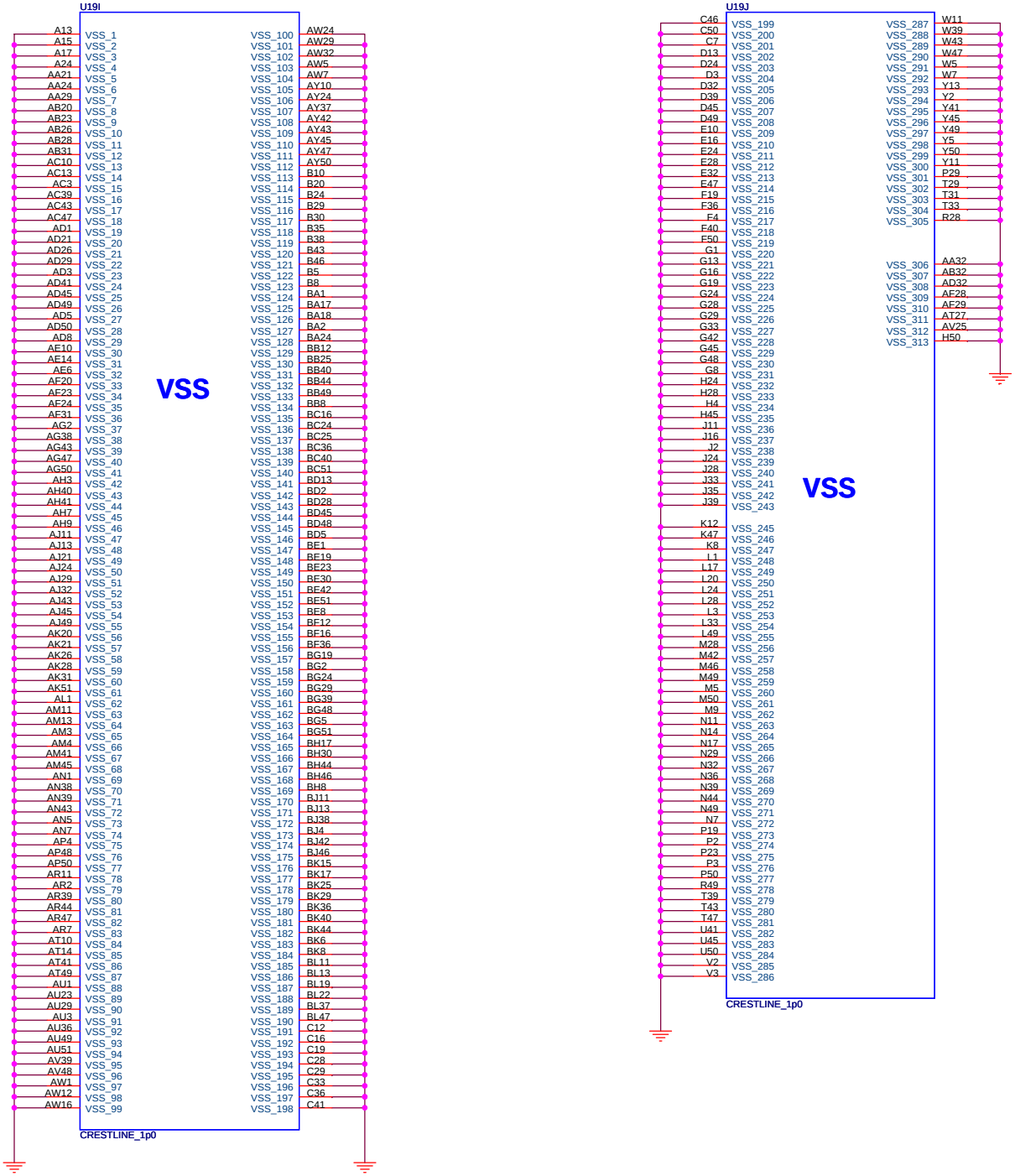

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Title	Crestline (VSS)	
Size	Document Number M-08	Rev 0.1
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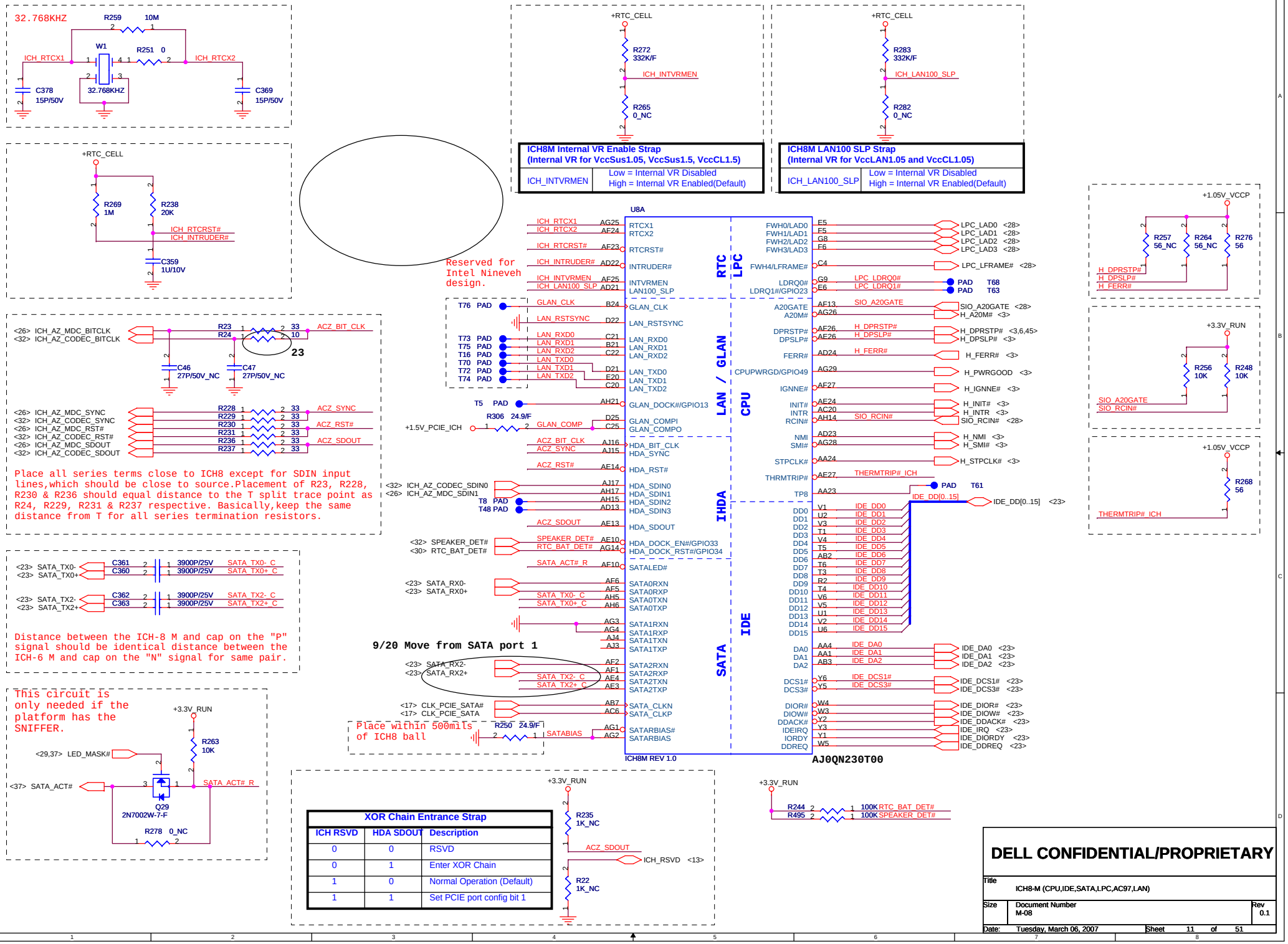
32.768KHZ
R259 10M
W1
R251 0
ICH_RTCX1
ICH_RTCX2
C378 15P/50V
32.768KHZ
C369 15P/50V
+RTC_CELL
R269 1M
R238 20K
ICH_RTCRST#
ICH_INTRUDER#
C359 1U/10V
+RTC_CELL
R272 332K/F
ICH_INTVRMEN
R265 0_NC
ICH8M Internal VR Enable Strap
(Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)
ICH_INTVRMEN
Low = Internal VR Disabled
High = Internal VR Enabled(Default)
+RTC_CELL
R283 332K/F
ICH_LAN100_SLP
R282 0_NC
ICH8M LAN100 SLP Strap
(Internal VR for VccLAN1.05 and VccCL1.05)
ICH_LAN100_SLP
Low = Internal VR Disabled
High = Internal VR Enabled(Default)
Reserved for Intel Nineveh design.
U8A
RTC
LPC
LAN / GLAN
CPU
IHDA
IDE
SATA
ICH8M REV 1.0
AJ0QN230T00
<26> ICH_AZ_MDC_BITCLK
<32> ICH_AZ_CODEC_BITCLK
R23 33
R24 10
23
ACZ_BIT_CLK
C46 27P/50V_NC
C47 27P/50V_NC
<26> ICH_AZ_MDC_SYNC
<32> ICH_AZ_CODEC_SYNC
<26> ICH_AZ_MDC_RST#
<32> ICH_AZ_CODEC_RST#
<26> ICH_AZ_MDC_SDOUT
<32> ICH_AZ_CODEC_SDOUT
R228 33
R229 33
R230 33
R231 33
R236 33
R237 33
ACZ_SYNC
ACZ_RST#
ACZ_SDOUT
Place all series terms close to ICH8 except for SDIN input lines,which should be close to source.Placement of R23, R228, R230 & R236 should equal distance to the T split trace point as R24, R229, R231 & R237 respective. Basically,keep the same distance from T for all series termination resistors.
T76 PAD
T73 PAD
T75 PAD
T16 PAD
T70 PAD
T72 PAD
T74 PAD
T5 PAD
R306 24.9/F
+1.5V_PCIE_ICH
T8 PAD
T48 PAD
<23> SATA_TX0-
<23> SATA_TX0+
C361 3900P/25V
C360 3900P/25V
SATA_TX0- C
SATA_TX0+ C
<23> SATA_TX2-
<23> SATA_TX2+
C362 3900P/25V
C363 3900P/25V
SATA_TX2- C
SATA_TX2+ C
Distance between the ICH-8 M and cap on the "P" signal should be identical distance between the ICH-6 M and cap on the "N" signal for same pair.
9/20 Move from SATA port 1
<23> SATA_RX2-
<23> SATA_RX2+
<17> CLK_PCIE_SATA#
<17> CLK_PCIE_SATA
Place within 500mils of ICH8 ball
R250 24.9/F
SATABIAS
This circuit is only needed if the platform has the SNIFFER.
+3.3V_RUN
R263 10K
<29,37> LED_MASK#
<37> SATA_ACT#
SATA_ACT# R
Q29 2N7002W-7-F
R278 0_NC
XOR Chain Entrance Strap
ICH RSVD
HDA SDOUT
Description
0 0 RSVD
0 1 Enter XOR Chain
1 0 Normal Operation (Default)
1 1 Set PCIE port config bit 1
+3.3V_RUN
R235 1K_NC
ACZ_SDOUT
ICH_RSVD <13>
R22 1K_NC
+3.3V_RUN
R244 100K RTC_BAT_DET#
R495 100K SPEAKER_DET#
+1.05V_VCCP
R257 56_NC
R264 56_NC
R276 56
H_DPRSTP#
H_DPSLP#
H_FERR#
+3.3V_RUN
R256 10K
R248 10K
SIO_A20GATE
SIO_RCIN#
+1.05V_VCCP
R268 56
THERMTRIP# ICH
LPC_LAD0 <28>
LPC_LAD1 <28>
LPC_LAD2 <28>
LPC_LAD3 <28>
LPC_LFRAME# <28>
LPC_LDRQ0#
LPC_LDRQ1#
PAD T68
PAD T63
SIO_A20GATE <28>
H_A20M# <3>
H_DPRSTP# <3,6,45>
H_DPSLP# <3>
H_FERR# <3>
H_PWRGOOD <3>
H_IGNNE# <3>
H_INIT# <3>
H_INTR <3>
SIO_RCIN# <28>
H_NMI <3>
H_SMI# <3>
H_STPCLK# <3>
THERMTRIP# ICH
PAD T61
IDE_DD[0..15]
IDE_DD[0..15] <23>
IDE_DA0 <23>
IDE_DA1 <23>
IDE_DA2 <23>
IDE_DCS1# <23>
IDE_DCS3# <23>
IDE_DIOR# <23>
IDE_DIOW# <23>
IDE_DDACK# <23>
IDE_IRQ <23>
IDE_DIORDY <23>
IDE_DDREQ <23>
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Place TX DC blocking caps close ICH8.

<25> PCIE_TX1-
<25> PCIE_TX1+
C90 0.1U/10V PCIE_TXN1_C
C97 0.1U/10V PCIE_TXP1_C

<24> PCIE_TX2-
<24> PCIE_TX2+
C101 0.1U/10V PCIE_TXN2_C
C106 0.1U/10V PCIE_TXP2_C

<24> PCIE_TX3-
<24> PCIE_TX3+
C114 0.1U/10V PCIE_TXN3_C
C116 0.1U/10V PCIE_TXP3_C

<26> PCIE_TX4-
<26> PCIE_TX4+
C127 0.1U/10V PCIE_TXN4_C
C120 0.1U/10V PCIE_TXP4_C

Non-iAMT

RP27 10P8R-10K
+3.3V_SUS
OC7# OC9# OC5# OC6#
USB_OC0_1# USB_OC2_3# OC4# USB_OC8#

Layout Note:
Place R313,R311 and R327 within 500 mils from ICH.

<28> ICH_EC_SPI_CLK — R313 15 — ICH_EC_SPI_CLK_R
<28> ICH_EC_SPI_DO — R311 15 — ICH_EC_SPI_DO_R
<28> ICH_EC_SPI_DIN

+3.3V_ALW
U11 7SH08_NC
R328 15_NC
R93 0
<30> SPI_CS0# — ICH_SPI_CS# — SIO_SPI_CS# <28>

<27> USB_OC0_1# — USB_OC0_1#
<27> USB_OC2_3# — USB_OC2_3#
<27> USB_OC8# — USB_OC8#
OC4# OC5# OC6# OC7# OC9#

U8D ICH8M REV 1.0

PCI-Express Direct Media Interface

WWAN: <25> PCIE_RX1- <25> PCIE_RX1+ — PCIE_TXN1_C PCIE_TXP1_C — PERN1 PERP1 PETN1 PETP1
WLAN: <24> PCIE_RX2- <24> PCIE_RX2+ — PCIE_TXN2_C PCIE_TXP2_C — PERN2 PERP2 PETN2 PETP2
WPAN: <24> PCIE_RX3- <24> PCIE_RX3+ — PCIE_TXN3_C PCIE_TXP3_C — PERN3 PERP3 PETN3 PETP3
Express Card: <26> PCIE_RX4- <26> PCIE_RX4+ — PCIE_TXN4_C PCIE_TXP4_C — PERN4 PERP4 PETN4 PETP4
PERN5 PERP5 PETN5 PETP5
PERN6/GLAN_RXN PERP6/GLAN_RXP PETN6/GLAN_TXN PETP6/GLAN_TXP

DMI0RXN DMI0RXP DMI0TXN DMI0TXP — DMI_MTX_IRX_N0 <6> DMI_MTX_IRX_P0 <6> DMI_MRX_ITX_N0 <6> DMI_MRX_ITX_P0 <6>
DMI1RXN DMI1RXP DMI1TXN DMI1TXP — DMI_MTX_IRX_N1 <6> DMI_MTX_IRX_P1 <6> DMI_MRX_ITX_N1 <6> DMI_MRX_ITX_P1 <6>
DMI2RXN DMI2RXP DMI2TXN DMI2TXP — DMI_MTX_IRX_N2 <6> DMI_MTX_IRX_P2 <6> DMI_MRX_ITX_N2 <6> DMI_MRX_ITX_P2 <6>
DMI3RXN DMI3RXP DMI3TXN DMI3TXP — DMI_MTX_IRX_N3 <6> DMI_MTX_IRX_P3 <6> DMI_MRX_ITX_N3 <6> DMI_MRX_ITX_P3 <6>
DMI_CLKN — CLK_PCIE_ICH# <17>
DMI_CLKP — CLK_PCIE_ICH <17>
DMI_ZCOMP
DMI_IRCOMP — DMI_COMP — R281 24.9/F — +1.5V_PCIE_ICH

Place within 500mils of ICH8

SPI
SPI_CLK SPI_CS0# SPI_CS1# SPI_MOSI SPI_MISO

USB
OC0# OC1#/GPIO40 OC2#/GPIO41 OC3#/GPIO42 OC4#/GPIO43 OC5#/GPIO29 OC6#/GPIO30 OC7#/GPIO31 OC8# OC9#

USBP0N USBP0P USBP1N USBP1P USBP2N USBP2P USBP3N USBP3P USBP4N USBP4P USBP5N USBP5P USBP6N USBP6P USBP7N USBP7P USBP8N USBP8P USBP9N USBP9P

ICH_USBP0- <27> ICH_USBP0+ <27> **USB[1B]**
ICH_USBP1- <27> ICH_USBP1+ <27> **USB[1A]**
ICH_USBP2- <27> ICH_USBP2+ <27> **USB[2B]**
ICH_USBP3- <27> ICH_USBP3+ <27> **USB[2A]**
ICH_USBP4- <24> ICH_USBP4+ <24> **3rd MINI CARD**
ICH_USBP5- <33> ICH_USBP5+ <33> **CAMERA**
ICH_USBP6- <26> ICH_USBP6+ <26> **Express Card**
ICH_USBP7- <37> ICH_USBP7+ <37> **BT**
ICH_USBP8- <27> ICH_USBP8+ <27> **USB[3A]**
ICH_USBP9- <25> ICH_USBP9+ <25> **WWAN USB**

USBRBIAS# USBRBIAS — USBRBIAS — R301 22.6/F

Short F2 and F3 at the package and keep length to less than 500mils. Trace Impedance should be 60ohms +/- 15%.

PCI Pullups
+3.3V_RUN
RP35 10P8R-8.2K — PCI_STOP# PCI_FRAME# PCI_REQ1#
RP34 10P8R-8.2K — PCI_SERR# SB_WLAN_PCIE_RST# PCI_TRDY# SB_MCARD3_PCIE_RST# — PCI_PIRQD# SB_NB_PCIE_RST# PCI_DEVSEL#
RP31 10P8R-8.2K — PCI_PERR# PCI_IRDY# PCI_PIRQA# PCI_REQ0# — PCI_PIRQC# PCI_PLOCK# PCI_PIRQB#

35

WWAN Noise - ICH improvements 18

OC4# C876 OC5# C871 OC6# C872 OC7# C873 OC9# C878 USB_OC8# C874 USB_OC0_1# C875 USB_OC2_3# C877 — 0.1U/10V

ICH_SPI_CS1# R — PCI_GNT0# — R304 1K — R292 1K_NC

Boot BIOS Strap

		GNT0#	SPI_CS1#
LPC	11	No stuff	No stuff
PCI	10	No stuff	Stuff
SPI	01	Stuff	No stuff

LOM	REQ0	GNT0	PIRQB
1394/MediaCard	REQ1	GNT1	PIRQC PIRQD

SB_NB_PCIE_RST# — R307 1K_NC

A16 away override strap.

SB_NB_PCIE_RST#	Low = A16 swap override enabled. High = Default.

Non-iAMT
Add Buffers as needed for Loading and fanout concerns.
+3.3V_SUS
C84 0.047U/10V — U10 7SH32 — PCI_RST# G — PCI_RST# <20,35>
C357 0.047U/10V — U28 7SH32 — PCI_PLTRST# — PLTRST# <6,28>
C355 0.047U/10V — U27 7SH32 — PCI_PLTRST# — PLTRST1# <24,25,26>

<20,35> PCI_AD[0..31]

U8B ICH8M REV 1.0

PCI

PCI_AD0 D20 PCI_AD1 E19 PCI_AD2 D19 PCI_AD3 A20 PCI_AD4 D17 PCI_AD5 A21 PCI_AD6 A19 PCI_AD7 C19 PCI_AD8 A18 PCI_AD9 B16 PCI_AD10 A12 PCI_AD11 E16 PCI_AD12 A14 PCI_AD13 G16 PCI_AD14 A15 PCI_AD15 B6 PCI_AD16 C11 PCI_AD17 A9 PCI_AD18 D11 PCI_AD19 B12 PCI_AD20 C12 PCI_AD21 D10 PCI_AD22 C7 PCI_AD23 F13 PCI_AD24 E11 PCI_AD25 E13 PCI_AD26 E12 PCI_AD27 D8 PCI_AD28 A6 PCI_AD29 E8 PCI_AD30 D6 PCI_AD31 A3

REQ0# A4 — PCI_REQ0# — PCI_REQ0# <35>
GNT0# D7 — PCI_GNT0# — PCI_GNT0# <35>
REQ1#/GPIO50 E18 — PCI_REQ1# — PCI_REQ1# <20>
GNT1#/GPIO51 C18 — PCI_GNT1# — PCI_GNT1# <20>
REQ2#/GPIO52 B19 — SB_WWAN_PCIE_RST# — SB_WWAN_PCIE_RST# <25>
GNT2#/GPIO53 F18
REQ3#/GPIO54 A11 — SB_LOM_PCIE_RST# — SB_LOM_PCIE_RST#
GNT3#/GPIO55 C10

C/BE0# C17 — PCI_C_BE0# — PCI_C_BE0# <20,35>
C/BE1# E15 — PCI_C_BE1# — PCI_C_BE1# <20,35>
C/BE2# E16 — PCI_C_BE2# — PCI_C_BE2# <20,35>
C/BE3# E17 — PCI_C_BE3# — PCI_C_BE3# <20,35>

IRDY# C8 — PCI_IRDY# — PCI_IRDY# <20,35>
PAR D9 — PCI_PAR — PCI_PAR <20,35>
PCIRST# G6 — PCI_RST# G
DEVSEL# D16 — PCI_DEVSEL# — PCI_DEVSEL# <20,35>
PERR# A7 — PCI_PERR# — PCI_PERR# <20,35>
PLOCK# B7 — PCI_PLOCK# — PCI_PLOCK#
SERR# E10 — PCI_SERR# — PCI_SERR# <20,35>
STOP# C16 — PCI_STOP# — PCI_STOP# <20,35>
TRDY# C9 — PCI_TRDY# — PCI_TRDY# <20,35>
FRAME# A17 — PCI_FRAME# — PCI_FRAME# <20,35>

PLTRST# AG24 — PCI_PLTRST#
PCICLK B10 — CLK_PCI_ICH — CLK_PCI_ICH <17>
PME# G7 — ICH_PME# <29>

SB_MCARD3_PCIE_RST# R291 20K_NC
SB_WWAN_PCIE_RST# R314 20K
SB_WLAN_PCIE_RST# R300 20K_NC
SB_LOM_PCIE_RST# R324 20K
SB_NB_PCIE_RST# R302 20K_NC

BIOS should not enable the internal GPIO pull up resistor.

CLK_PCI_ICH — R310 10 — C417 9P/50V

Reserved for EMI. Place resister and cap close to ICH.

Interrupt I/F

PCI_PIRQA# F9 PCI_PIRQB# B5 PCI_PIRQC# C5 PCI_PIRQD# A10

<35> PCI_PIRQB#
<20> PCI_PIRQC#
<20> PCI_PIRQD#

PIRQA# PIRQB# PIRQC# PIRQD#
PIRQE#/GPIO2 PIRQF#/GPIO3 PIRQG#/GPIO4 PIRQH#/GPIO5

SB_MCARD3_PCIE_RST# E8 — SB_MCARD3_PCIE_RST# — SB_MCARD3_PCIE_RST# <24>
SB_WLAN_PCIE_RST# G11 — SB_WLAN_PCIE_RST# — SB_WLAN_PCIE_RST# <24>
SB_NB_PCIE_RST# F12 — SB_NB_PCIE_RST# — SB_NB_PCIE_RST# <6>
PCIE_MCARD2_DET# B3 — PCIE_MCARD2_DET# — PCIE_MCARD2_DET# <25>

PCI_PIRQB: for LOM
PCI_PIRQC: for Media Card
PCI_PIRQD: for 1394

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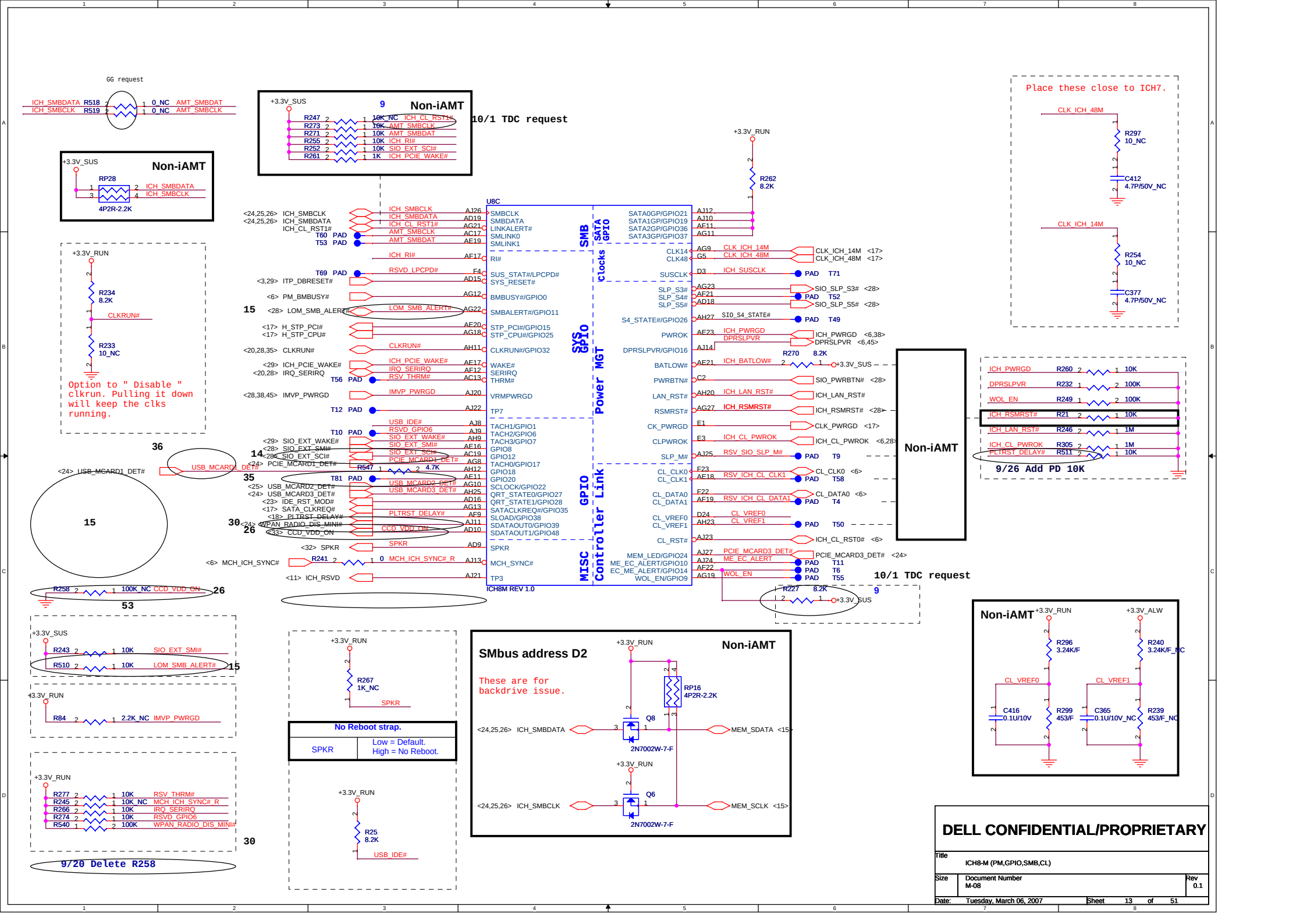
GG request
ICH_SMBDATA R518 2 1 0_NC AMT_SMBDAT
ICH_SMBCLK R519 2 1 0_NC AMT_SMBCLK
+3.3V_SUS
Non-iAMT
RP28
ICH_SMBDATA
ICH_SMBCLK
4P2R-2.2K
+3.3V_RUN
R234 8.2K
CLKRUN#
R233 10_NC
Option to " Disable " clkrun. Pulling it down will keep the clks running.
+3.3V_SUS
9
Non-iAMT
10/1 TDC request
R247 10K_NC ICH_CL_RST1#
R273 10K AMT_SMBCLK
R271 10K AMT_SMBDAT
R255 10K ICH_RI#
R252 10K SIO_EXT_SCI#
R261 1K ICH_PCIE_WAKE#
+3.3V_RUN
R262 8.2K
U8C
SMBCLK
SMBDATA
LINKALERT#
SMLINK0
SMLINK1
RI#
SUS_STAT#/LPCPD#
SYS_RESET#
BMBUSY#/GPIO0
SMBALERT#/GPIO11
STP_PCI#/GPIO15
STP_CPU#/GPIO25
CLKRUN#/GPIO32
WAKE#
SERIRQ
THRM#
VRMPWRGD
TP7
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
GPIO12
TACH0/GPIO17
GPIO18
GPIO20
SCLOCK/GPIO22
QRT_STATE0/GPIO27
QRT_STATE1/GPIO28
SATACLKREQ#/GPIO35
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
SPKR
MCH_SYNC#
TP3
ICH8M REV 1.0
SMB
SATA GPIO
Clocks
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA2GP/GPIO36
SATA3GP/GPIO37
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
S4_STATE#/GPIO26
PWROK
DPRSLPVR/GPIO16
BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
CK_PWRGD
CLPWROK
SLP_M#
CL_CLK0
CL_CLK1
CL_DATA0
CL_DATA1
CL_VREF0
CL_VREF1
CL_RST#
MEM_LED/GPIO24
ME_EC_ALERT/GPIO10
EC_ME_ALERT/GPIO14
WOL_EN/GPIO9
Place these close to ICH7.
CLK_ICH_48M
R297 10_NC
C412 4.7P/50V_NC
CLK_ICH_14M
R254 10_NC
C377 4.7P/50V_NC
Non-iAMT
ICH_PWRGD R260 10K
DPRSLPVR R232 100K
WOL_EN R249 100K
ICH_RSMRST# R21 10K
ICH_LAN_RST# R246 1M
ICH_CL_PWROK R305 1M
PLTRST_DELAY# R511 10K
9/26 Add PD 10K
R270 8.2K
+3.3V_SUS
R227 8.2K
+3.3V_SUS
9
10/1 TDC request
USB_MCARD1_DET#
USB_MCARD2_DET#
USB_MCARD3_DET#
R547 4.7K
IDE_RST_MOD#
SATA_CLKREQ#
PLTRST_DELAY#
WPAN_RADIO_DIS_MINI#
CCD_VDD_ON
SPKR
MCH_ICH_SYNC#
R241 0 MCH_ICH_SYNC#_R
ICH_RSVD
R258 100K_NC CCD_VDD_ON
53
+3.3V_SUS
R243 10K SIO_EXT_SMI#
R510 10K LOM_SMB_ALERT#
+3.3V_RUN
R84 2.2K_NC IMVP_PWRGD
+3.3V_RUN
R277 10K RSV_THRM#
R245 10K_NC MCH_ICH_SYNC#_R
R266 10K IRQ_SERIRQ
R274 10K RSVD_GPIO6
R540 100K WPAN_RADIO_DIS_MINI#
9/20 Delete R258
+3.3V_RUN
R267 1K_NC
SPKR
No Reboot strap.
SPKR
Low = Default.
High = No Reboot.
+3.3V_RUN
R25 8.2K
USB_IDE#
SMbus address D2
These are for backdrive issue.
Non-iAMT
+3.3V_RUN
RP16 4P2R-2.2K
Q8
2N7002W-7-F
ICH_SMBDATA
MEM_SDATA
Q6
2N7002W-7-F
ICH_SMBCLK
MEM_SCLK
Non-iAMT
+3.3V_RUN
+3.3V_ALW
R296 3.24K/F
R240 3.24K/F_NC
CL_VREF0
CL_VREF1
C416 0.1U/10V
R299 453/F
C365 0.1U/10V_NC
R239 453/F_NC
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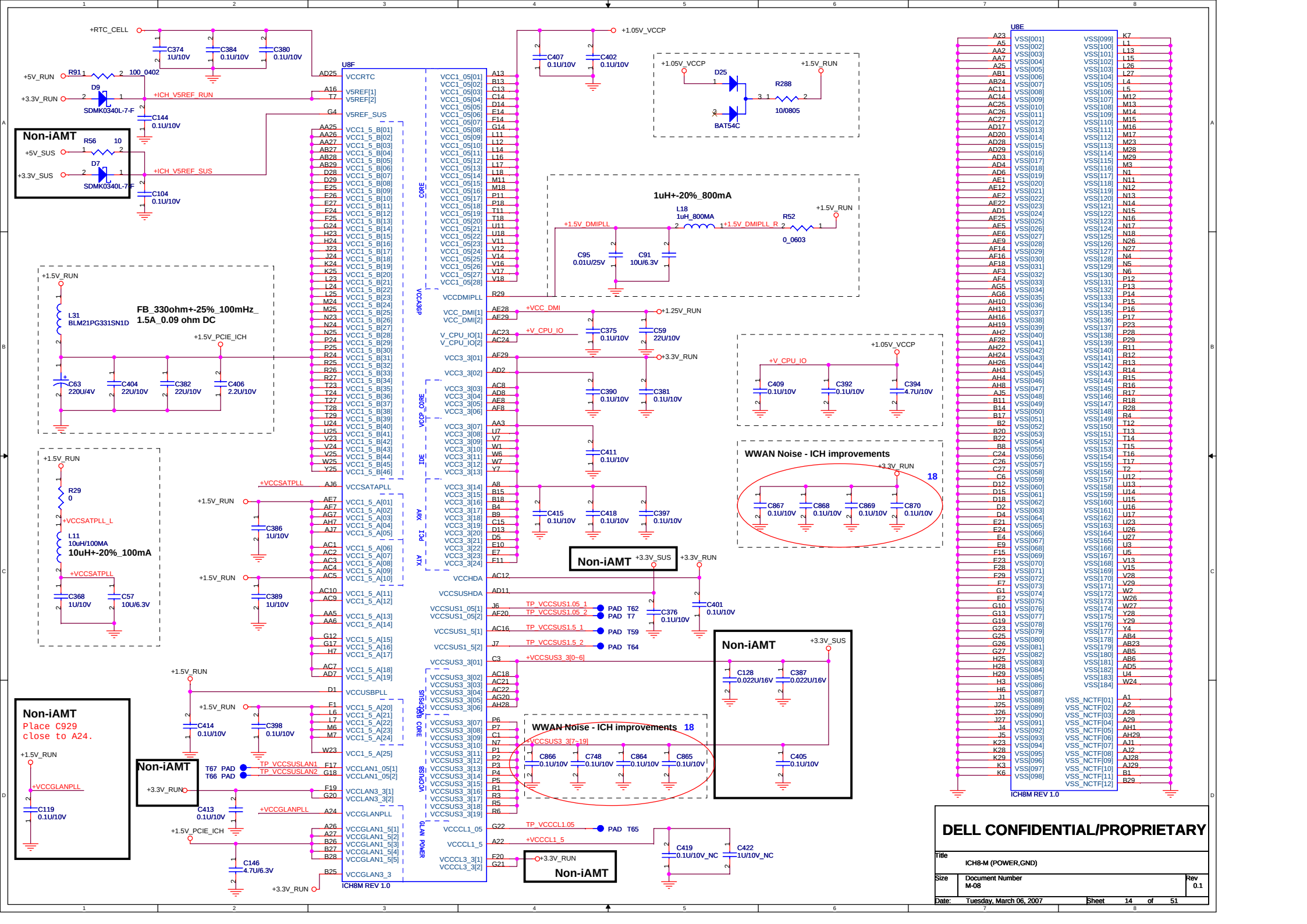
U8F
ICH8M REV 1.0
U8E
ICH8M REV 1.0
Non-iAMT
Non-iAMT
Place C929
close to A24.
Non-iAMT
Non-iAMT
Non-iAMT
Non-iAMT
Non-iAMT
WWAN Noise - ICH improvements 18
WWAN Noise - ICH improvements
1uH+-20%_800mA
FB_330ohm+-25%_100mHz_
1.5A_0.09 ohm DC
10uH+-20%_100mA
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Title
ICH8-M (POWER,GND)
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A is required to route to Top SoDIMM for AMTto function. Ch.A SODIMM needs to be populated for Intel AMT support.

TOP

JDIM1

PC4800 DDR2 SDRAM SO-DIMM (200P)

+1.8V_SUS, V_DDR_MCH_REF

DDR_A_DM[0..7] <7>
DDR_A_D[0..63] <7>
DDR_A_DQS[0..7] <7>
DDR_A_DQS#[0..7] <7>
DDR_A_MA[0..14] <6,7,16>

V_DDR_MCH_REF: C277 0.1U/10V, C276 2.2U/6.3V

M_CLK_DDR0 <6>
M_CLK_DDR#0 <6>
M_CLK_DDR1 <6>
M_CLK_DDR#1 <6>

PM_EXTTS#0 <6>

<6,16> DDR_CKE0_DIMMA
DDR_CKE1_DIMMA <6,16>
<6,16> DDR_CKE2_DIMMB

<7,16> DDR_A_BS2

DDR_A_BS1 <7,16>
DDR_A_RAS# <7,16>
DDR_CS0_DIMMA# <6,16>

<7,16> DDR_A_BS0
<7,16> DDR_A_WE#

M_ODT0 <6,16>

<7,16> DDR_A_CAS#
<6,16> DDR_CS1_DIMMA#

<6,16> M_ODT1

+3.3V_RUN: C580 2.2U/6.3V, C579 0.1U/10V — Non-iAMT

<13> MEM_SDATA
<13> MEM_SCLK
+3.3V_RUN

R169 10K, R170 10K

Non-iAMT

SMbus address A0

CLOCK 0,1
CKE 0,1

FOX_AS0A426-N2RN-7F

BOT

JDIM2

PC4800 DDR2 SDRAM SO-DIMM (200P)

+1.8V_SUS, V_DDR_MCH_REF

DDR_B_DM[0..7] <7>
DDR_B_D[0..63] <7>
DDR_B_DQS[0..7] <7>
DDR_B_DQS#[0..7] <7>
DDR_B_MA[0..14] <6,7,16>

V_DDR_MCH_REF: C274 0.1U/10V, C275 2.2U/6.3V

M_CLK_DDR2 <6>
M_CLK_DDR#2 <6>
M_CLK_DDR3 <6>
M_CLK_DDR#3 <6>

PM_EXTTS#1 <6>

DDR_CKE3_DIMMB <6,16>

<7,16> DDR_B_BS2

DDR_B_BS1 <7,16>
DDR_B_RAS# <7,16>
DDR_CS2_DIMMB# <6,16>

M_ODT2 <6,16>

<7,16> DDR_B_CAS#
<6,16> DDR_CS3_DIMMB#

<6,16> M_ODT3

+3.3V_RUN: C264 2.2U/6.3V, C268 0.1U/10V — Non-iAMT

R449 10K

Non-iAMT

SMbus address A4

CLOCK 2,3
CKE 2,3

FOX_ AS0A426-N2SN-7F

R448 10K

Place these Caps near So-Dimm1.

+1.8V_SUS: C270 2.2U/6.3V, C269 2.2U/6.3V, C279 2.2U/6.3V, C280 2.2U/6.3V, C281 2.2U/6.3V

Place these Caps near So-Dimm2.

+1.8V_SUS: C588 2.2U/6.3V, C575 2.2U/6.3V, C586 2.2U/6.3V, C587 2.2U/6.3V, C576 2.2U/6.3V

Place these Caps near So-Dimm1.

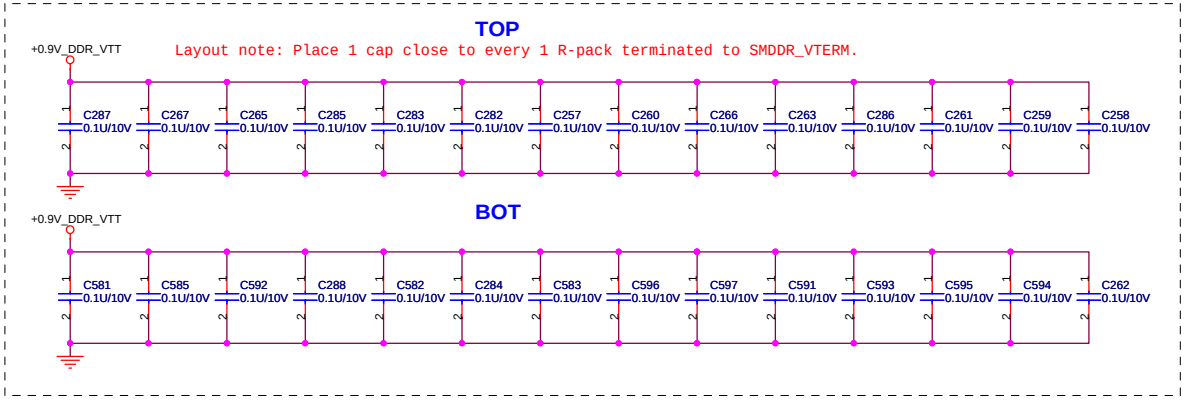
+1.8V_SUS: C272 0.1U/10V, C278 0.1U/10V, C271 0.1U/10V, C273 0.1U/10V

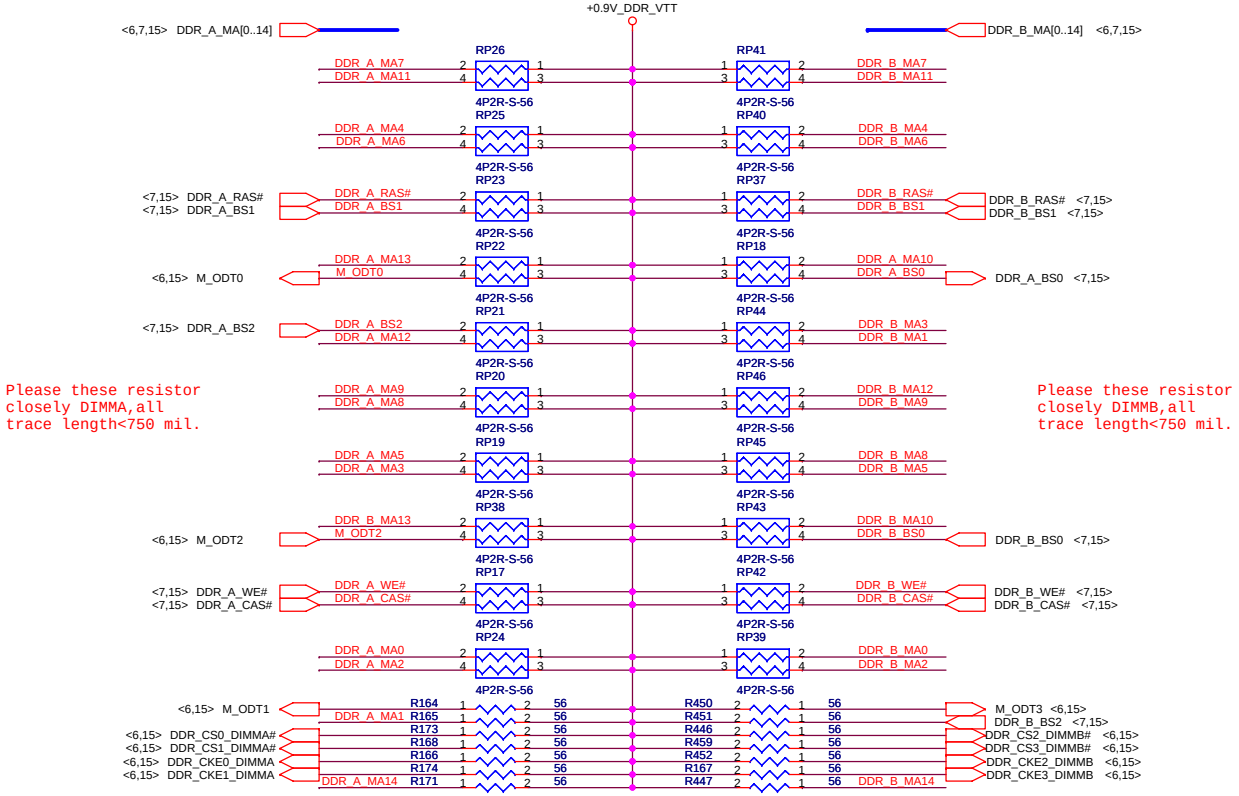
Place these Caps near So-Dimm2.

+1.8V_SUS: C574 0.1U/10V, C584 0.1U/10V, C578 0.1U/10V, C577 0.1U/10V

DELL CONFIDENTIAL/PROPRIETARY

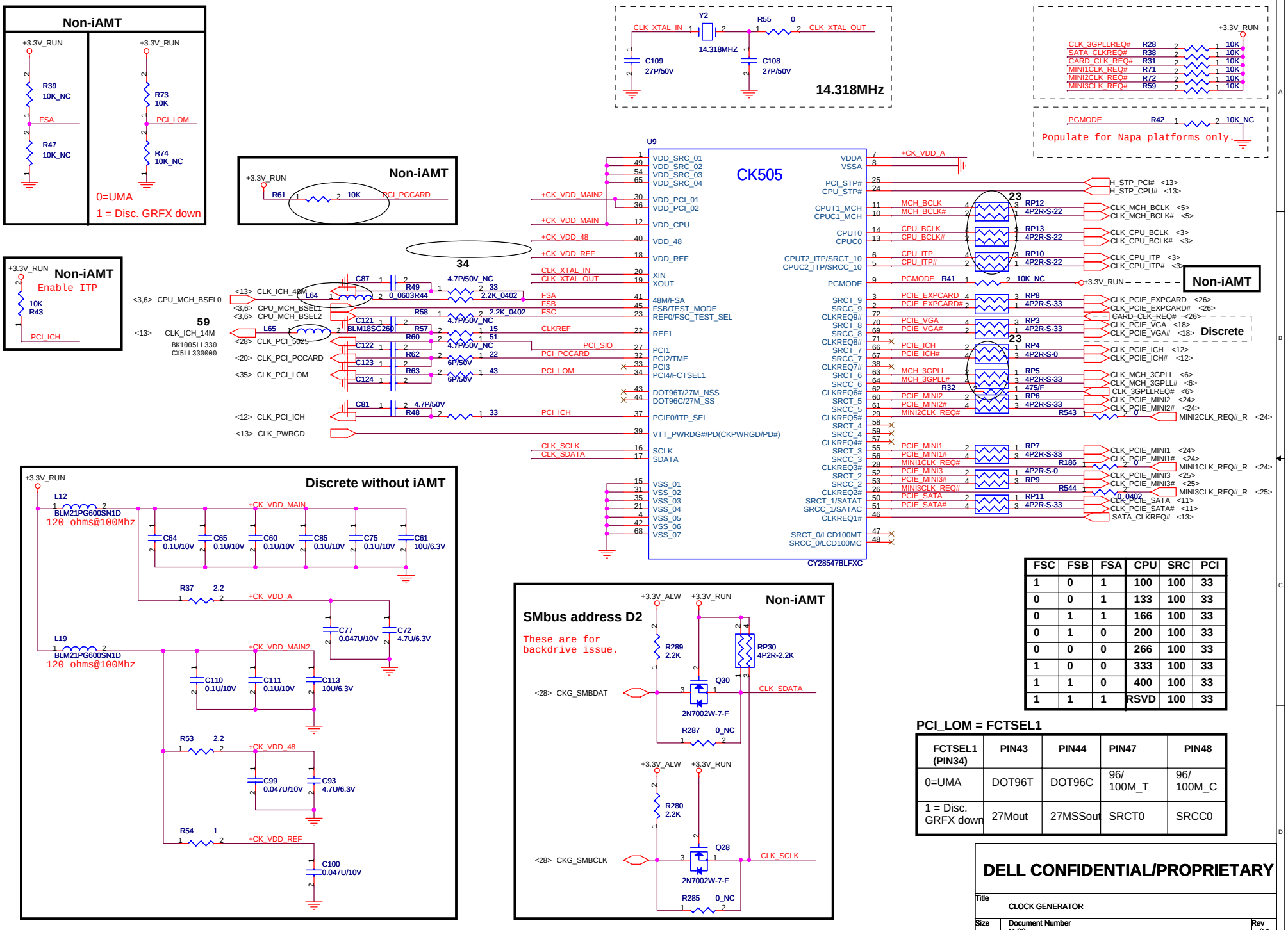
Title	DDR2 SO-DIMM (200P) X 2	
Size	Document Number M-08	Rev 0.1
Date: Monday, March 05, 2007	Sheet 15 of 51	





DELL CONFIDENTIAL/PROPRIETARY

Title	DDR2 RES ARRAY	
Size	Document Number M-08	Rev 0.1
Date: Monday, March 05, 2007	Sheet 16 of 51	



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

PCI_LOM = FCTSEL1

FCTSEL1 (PIN34)	PIN43	PIN44	PIN47	PIN48
0=UMA	DOT96T	DOT96C	96/ 100M_T	96/ 100M_C
1 = Disc. GRFX down	27Mout	27MSSout	SRCT0	SRCC0

DELL CONFIDENTIAL/PROPRIETARY

Title	CLOCK GENERATOR	
Size	Document Number M-08	Rev 0.1
Date: Wednesday, March 07, 2007	Sheet 17 of 51	

YPRPB_DET: SIGNAL FROM SVIDEO CONNECTOR,
TO SWICH TO COMPONENT OUT.

Delete R236,R247
pre ref schematic.

SMBUS Address 58 for Inverter.
SMBUS Address 98 for Temp.sensor.

JVDO1

HONDA_LPF-SC200SMYGA+

+3.3V_RUN

C372 .047U/10V/0402
C371 .047U/10V/0402
C373 .047U/10V/0402

YPRPB_DET# <19>
+5V_ALW
LCD_SMBCLK <28>
LCD_SMBDAT <28>
TV_Y <19>
TV_CVBS <19>
TV_C <19>
VSYNC <19>
HSYNC <19>
VGA_BLU <19>
VGA_GRN <19>
VGA_RED <19>
G_CLK_DDC2 <19>
G_DAT_DDC2 <19>
LCD_TST <29>
PLTRST_DELAY# <13>
CLK_PCIE_VGA <17>
CLK_PCIE_VGA# <17>

<6> PCIE_MTX_GRX_N[0..15]

PCIE_MTX_GRX_N0
PCIE_MTX_GRX_N1
PCIE_MTX_GRX_N2
PCIE_MTX_GRX_N3
PCIE_MTX_GRX_N4
PCIE_MTX_GRX_N5
PCIE_MTX_GRX_N6
PCIE_MTX_GRX_N7
PCIE_MTX_GRX_N8
PCIE_MTX_GRX_N9
PCIE_MTX_GRX_N10
PCIE_MTX_GRX_N11
PCIE_MTX_GRX_N12
PCIE_MTX_GRX_N13
PCIE_MTX_GRX_N14
PCIE_MTX_GRX_N15

<6> PCIE_MTX_GRX_P[0..15]

PCIE_MTX_GRX_P0
PCIE_MTX_GRX_P1
PCIE_MTX_GRX_P2
PCIE_MTX_GRX_P3
PCIE_MTX_GRX_P4
PCIE_MTX_GRX_P5
PCIE_MTX_GRX_P6
PCIE_MTX_GRX_P7
PCIE_MTX_GRX_P8
PCIE_MTX_GRX_P9
PCIE_MTX_GRX_P10
PCIE_MTX_GRX_P11
PCIE_MTX_GRX_P12
PCIE_MTX_GRX_P13
PCIE_MTX_GRX_P14
PCIE_MTX_GRX_P15

PCIE_MTX_GRX_P0 / PCIE_MTX_GRX_N0	C66	PCIE_MTX_C_GRX_P0	PCIE_MTX_C_GRX_N0
PCIE_MTX_GRX_P1 / PCIE_MTX_GRX_N1	C70	PCIE_MTX_C_GRX_P1	PCIE_MTX_C_GRX_N1
PCIE_MTX_GRX_P2 / PCIE_MTX_GRX_N2	C76	PCIE_MTX_C_GRX_P2	PCIE_MTX_C_GRX_N2
PCIE_MTX_GRX_P3 / PCIE_MTX_GRX_N3	C80	PCIE_MTX_C_GRX_P3	PCIE_MTX_C_GRX_N3
PCIE_MTX_GRX_P4 / PCIE_MTX_GRX_N4	C88	PCIE_MTX_C_GRX_P4	PCIE_MTX_C_GRX_N4
PCIE_MTX_GRX_P5 / PCIE_MTX_GRX_N5	C89	PCIE_MTX_C_GRX_P5	PCIE_MTX_C_GRX_N5
PCIE_MTX_GRX_P6 / PCIE_MTX_GRX_N6	C102	PCIE_MTX_C_GRX_P6	PCIE_MTX_C_GRX_N6
PCIE_MTX_GRX_P7 / PCIE_MTX_GRX_N7	C105	PCIE_MTX_C_GRX_P7	PCIE_MTX_C_GRX_N7
PCIE_MTX_GRX_P8 / PCIE_MTX_GRX_N8	C115	PCIE_MTX_C_GRX_P8	PCIE_MTX_C_GRX_N8
PCIE_MTX_GRX_P9 / PCIE_MTX_GRX_N9	C118	PCIE_MTX_C_GRX_P9	PCIE_MTX_C_GRX_N9
PCIE_MTX_GRX_P10 / PCIE_MTX_GRX_N10	C126	PCIE_MTX_C_GRX_P10	PCIE_MTX_C_GRX_N10
PCIE_MTX_GRX_P11 / PCIE_MTX_GRX_N11	C130	PCIE_MTX_C_GRX_P11	PCIE_MTX_C_GRX_N11
PCIE_MTX_GRX_P12 / PCIE_MTX_GRX_N12	C132	PCIE_MTX_C_GRX_P12	PCIE_MTX_C_GRX_N12
PCIE_MTX_GRX_P13 / PCIE_MTX_GRX_N13	C135	PCIE_MTX_C_GRX_P13	PCIE_MTX_C_GRX_N13
PCIE_MTX_GRX_P14 / PCIE_MTX_GRX_N14	C136	PCIE_MTX_C_GRX_P14	PCIE_MTX_C_GRX_N14
PCIE_MTX_GRX_P15 / PCIE_MTX_GRX_N15	C148	PCIE_MTX_C_GRX_P15	PCIE_MTX_C_GRX_N15

All: .1U/10V/0402

+3.3V_SUS

+1.8V_RUN

C429 .1U/10V/0402
C428 .1U/10V/0402

For Discrete:
Populate C178,C181

+15V_ALW
<28,29,38,45> RUNPWROK
+2.5V_RUN

PCIE_MRX_GTX_P0
PCIE_MRX_GTX_N0
PCIE_MRX_GTX_P1
PCIE_MRX_GTX_N1
PCIE_MRX_GTX_P2
PCIE_MRX_GTX_N2
PCIE_MRX_GTX_P3
PCIE_MRX_GTX_N3
PCIE_MRX_GTX_P4
PCIE_MRX_GTX_N4
PCIE_MRX_GTX_P5
PCIE_MRX_GTX_N5
PCIE_MRX_GTX_P6
PCIE_MRX_GTX_N6
PCIE_MRX_GTX_P7
PCIE_MRX_GTX_N7
PCIE_MRX_GTX_P8
PCIE_MRX_GTX_N8
PCIE_MRX_GTX_P9
PCIE_MRX_GTX_N9
PCIE_MRX_GTX_P10
PCIE_MRX_GTX_N10
PCIE_MRX_GTX_P11
PCIE_MRX_GTX_N11
PCIE_MRX_GTX_P12
PCIE_MRX_GTX_N12
PCIE_MRX_GTX_P13
PCIE_MRX_GTX_N13
PCIE_MRX_GTX_P14
PCIE_MRX_GTX_N14
PCIE_MRX_GTX_P15
PCIE_MRX_GTX_N15

PCIE_MRX_GTX_N[0..15] <6>

PCIE_MRX_GTX_N0
PCIE_MRX_GTX_N1
PCIE_MRX_GTX_N2
PCIE_MRX_GTX_N3
PCIE_MRX_GTX_N4
PCIE_MRX_GTX_N5
PCIE_MRX_GTX_N6
PCIE_MRX_GTX_N7
PCIE_MRX_GTX_N8
PCIE_MRX_GTX_N9
PCIE_MRX_GTX_N10
PCIE_MRX_GTX_N11
PCIE_MRX_GTX_N12
PCIE_MRX_GTX_N13
PCIE_MRX_GTX_N14
PCIE_MRX_GTX_N15

PCIE_MRX_GTX_P[0..15] <6>

PCIE_MRX_GTX_P0
PCIE_MRX_GTX_P1
PCIE_MRX_GTX_P2
PCIE_MRX_GTX_P3
PCIE_MRX_GTX_P4
PCIE_MRX_GTX_P5
PCIE_MRX_GTX_P6
PCIE_MRX_GTX_P7
PCIE_MRX_GTX_P8
PCIE_MRX_GTX_P9
PCIE_MRX_GTX_P10
PCIE_MRX_GTX_P11
PCIE_MRX_GTX_P12
PCIE_MRX_GTX_P13
PCIE_MRX_GTX_P14
PCIE_MRX_GTX_P15

+3.3V_RUN
GFX_PWRGD <38>
LCDVCC_TST_EN <28>
THERMATRIP_VGA# <34>
+5V_RUN
PANEL_BKEN <29>

+G_PWR_SRC

C166 .1U/50V/0402
C169 .1U/50V/0402
C175 .1U/50V/0402
C177 .1U/50V/0402
C425 10U/25V/1206

+3.3V_RUN

U13
7SH08_NC

CFX_PWR_LIMIT
SIO_GFX_PWR <34>
ACAV_IN <28,34,40>

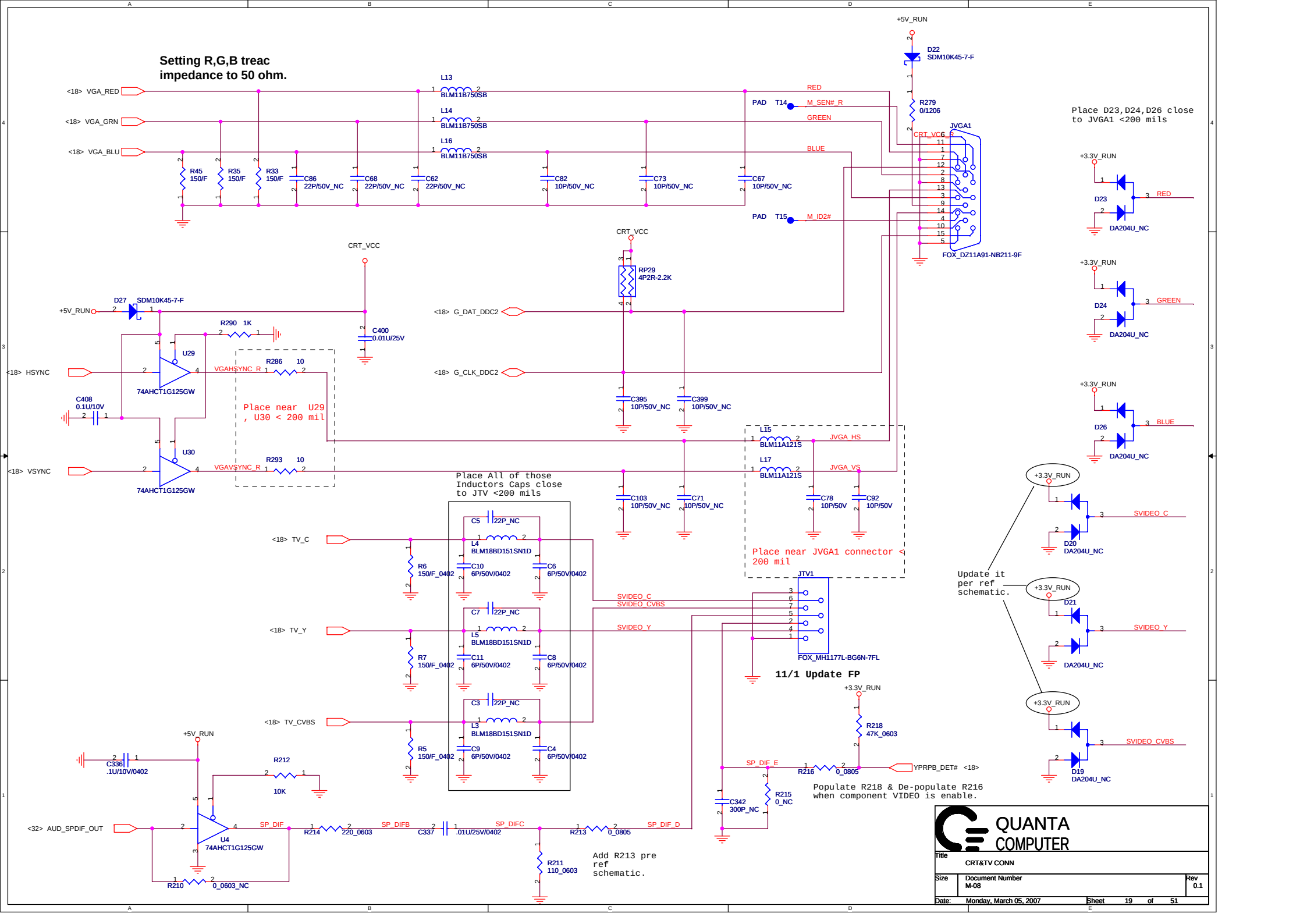
R109 0_NC

+PWR_SRC
+G_PWR_SRC
80 mil
80 mil
R94 100K_0402
C160 .1U/50V/0603
Q9 SI3457BDV-T1-E3
INV_PWR_SRC_ON
R103 100K_0402
INV_PWR_SRC_ON_R
RUN_ON <28,38,39>
Q11 2N7002W-7-F

QUANTA COMPUTER

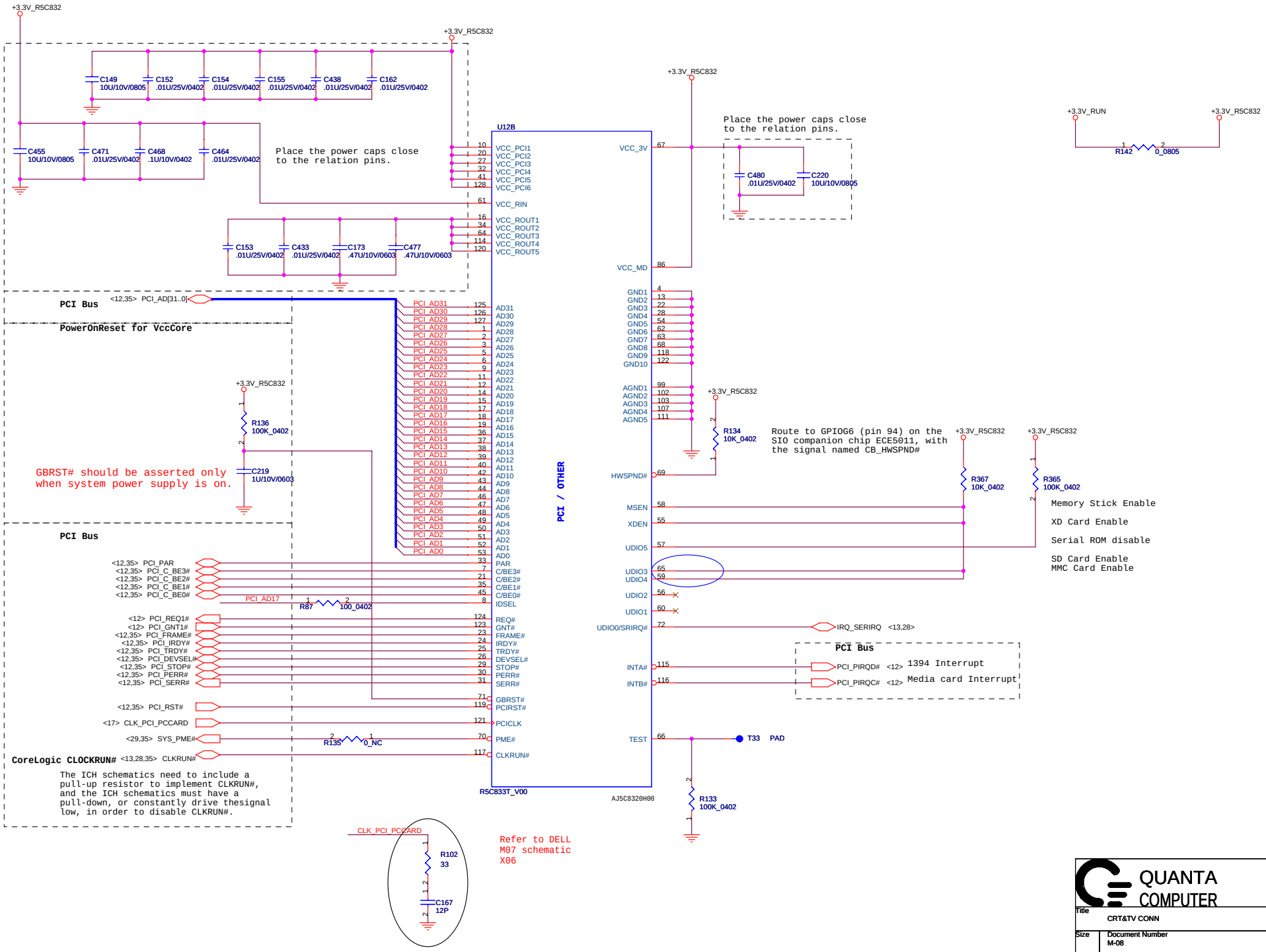
Title	VGA CARD Connector		
Size	Document Number FM1		Rev 0.1
Date: Monday, March 05, 2007		Sheet 18 of 51	

Setting R,G,B treac impedance to 50 ohm.

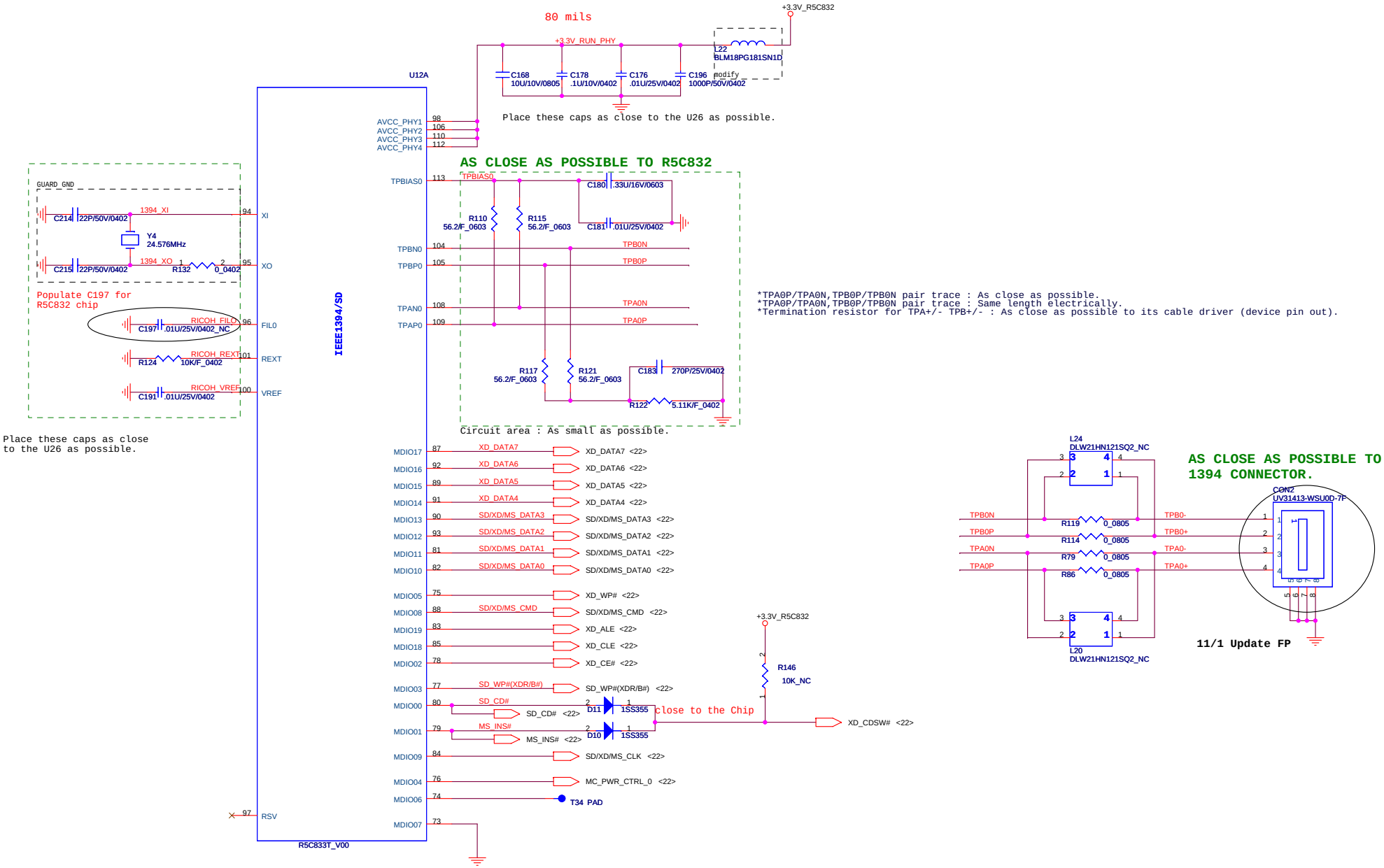


QUANTA COMPUTER

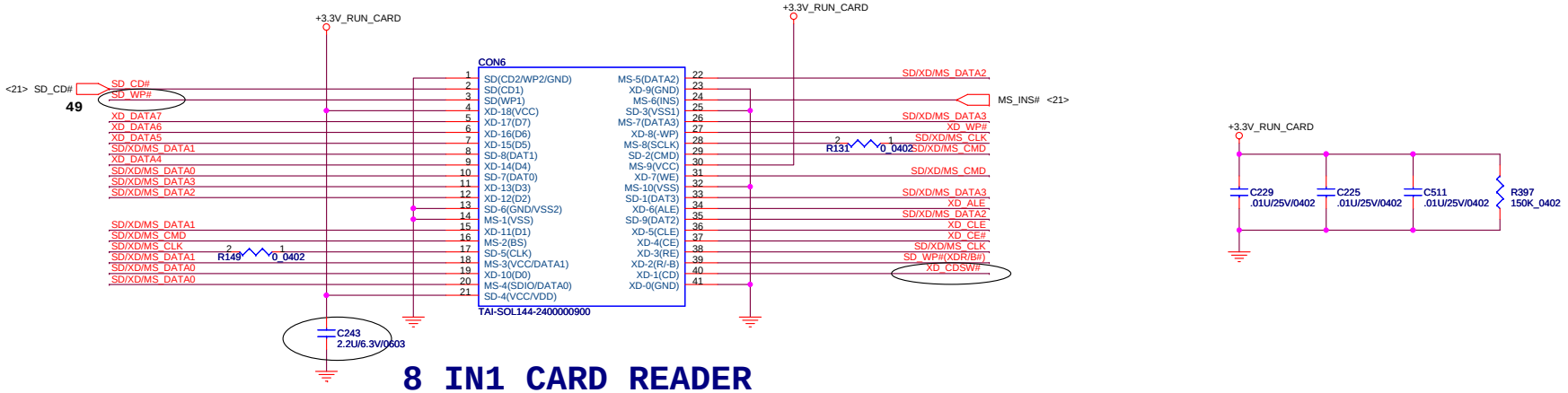
Title	CRT&TV CONN	
Size	Document Number M-08	Rev 0.1
Date: Monday, March 05, 2007	Sheet 19 of 51	



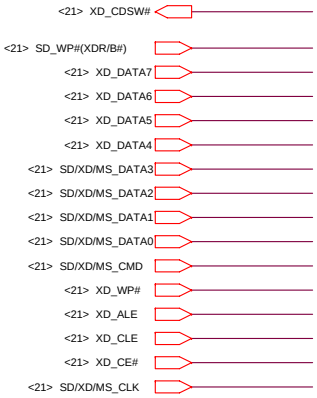
Title	CRT&TV CONN		
Size	Document Number M-08		Rev 0.1
Date:	Monday, March 05, 2007	Sheet 20 of 51	

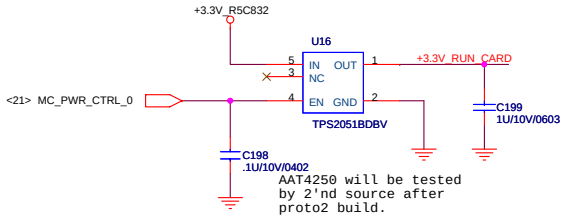


QUANTA COMPUTER		
Title	CRT&TV CONN	
Size	Document Number M-08	Rev 0.1
Date: Monday, March 05, 2007	Sheet 21 of 51	

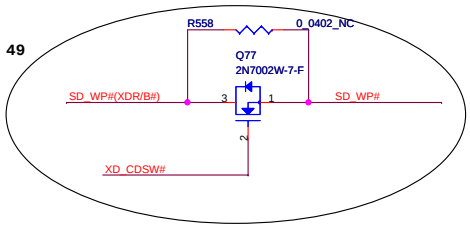


8 IN1 CARD READER





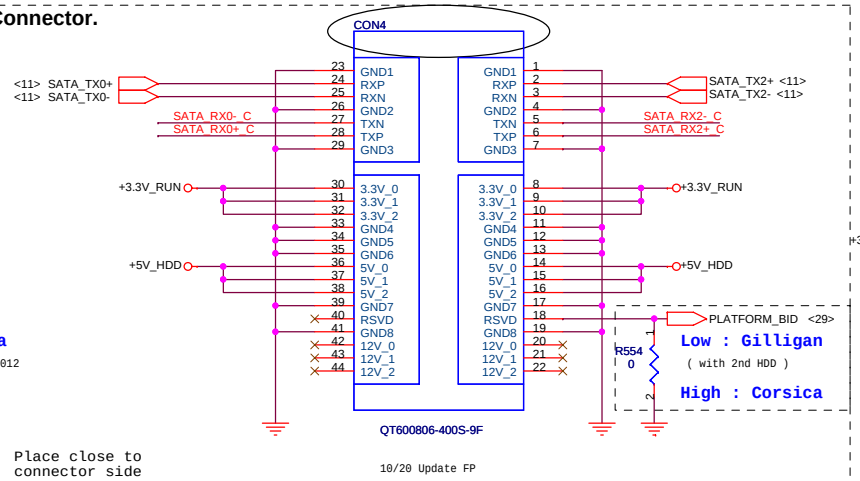
SD Protect



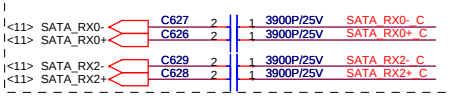
QUANTA COMPUTER

Title	CRT&TV CONN	
Size	Document Number M-08	Rev 0.1
Date: Monday, March 05, 2007	Sheet 22 of 51	

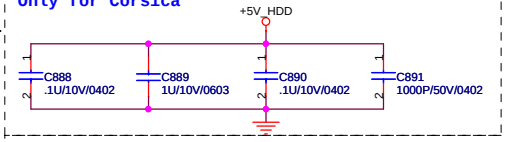
SATA 1 & 2 Connector.



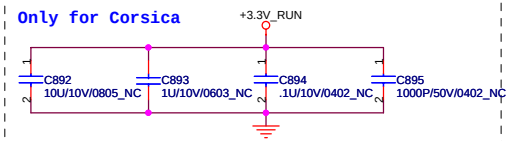
Locate caps C626, C627, C628, C629 near HDD Conn.
Length match SATA_C_RX0- & SATA_C_RX0+ within 0 mils.



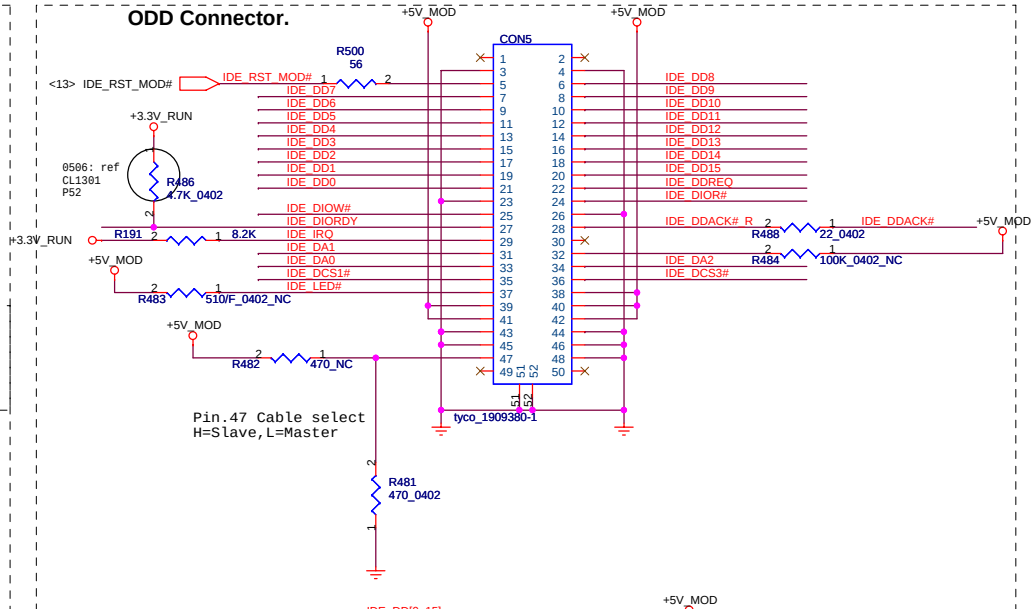
Only for Corsica

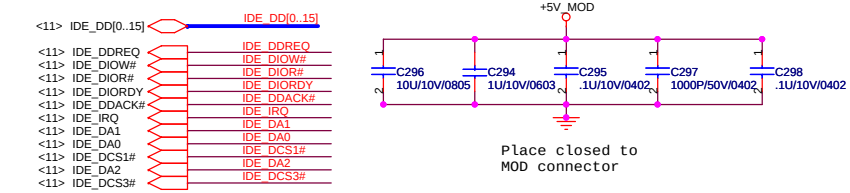


Only for Corsica

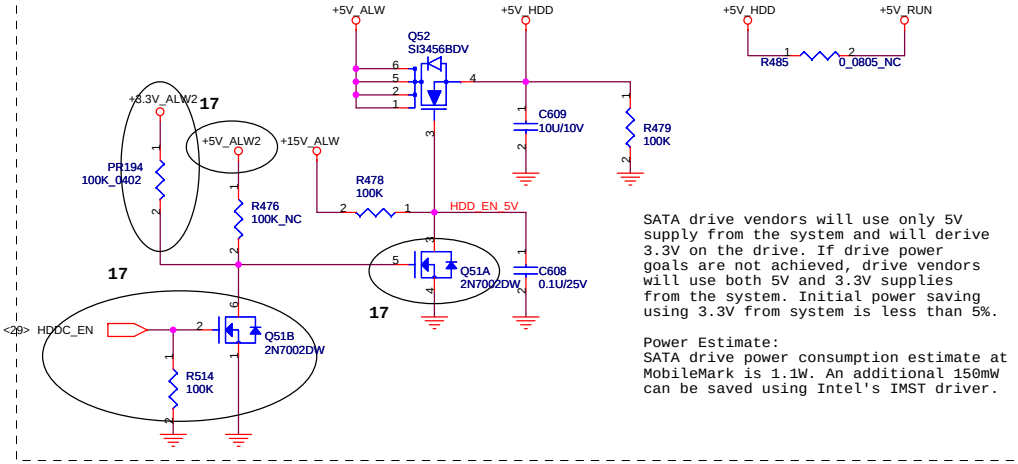


ODD Connector.





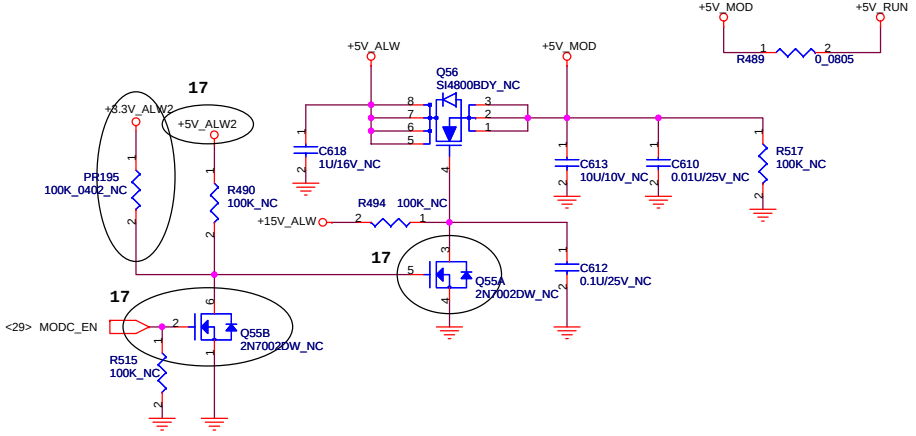
SATA PWR



SATA drive vendors will use only 5V supply from the system and will derive 3.3V on the drive. If drive power goals are not achieved, drive vendors will use both 5V and 3.3V supplies from the system. Initial power saving using 3.3V from system is less than 5%.

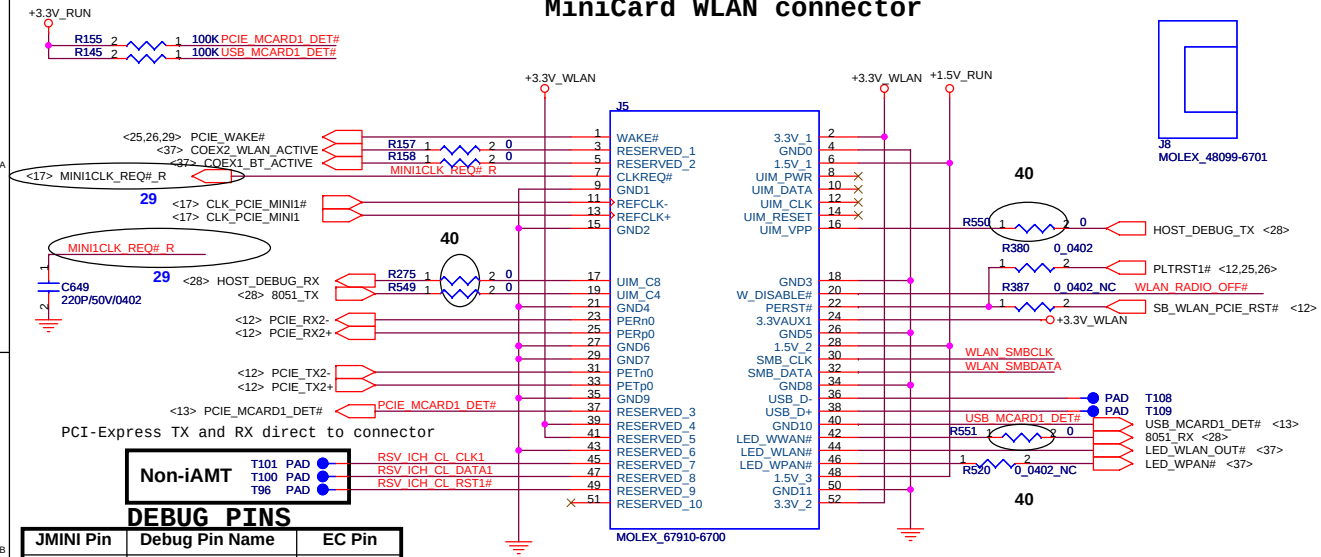
Power Estimate:
SATA drive power consumption estimate at MobileMark is 1.1W. An additional 150mW can be saved using Intel's IMST driver.

ODD PWR



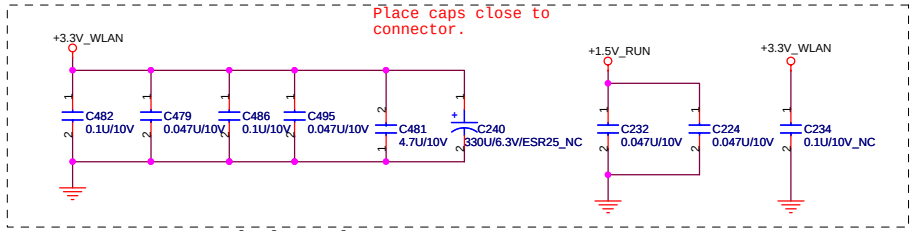
QUANTA COMPUTER		
Title: SATA (HDD&CD_ROM)		
Size	Document Number M-08	Rev 0.1
Date: Monday, March 05, 2007	Sheet 23 of 51	

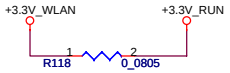
MiniCard WLAN connector



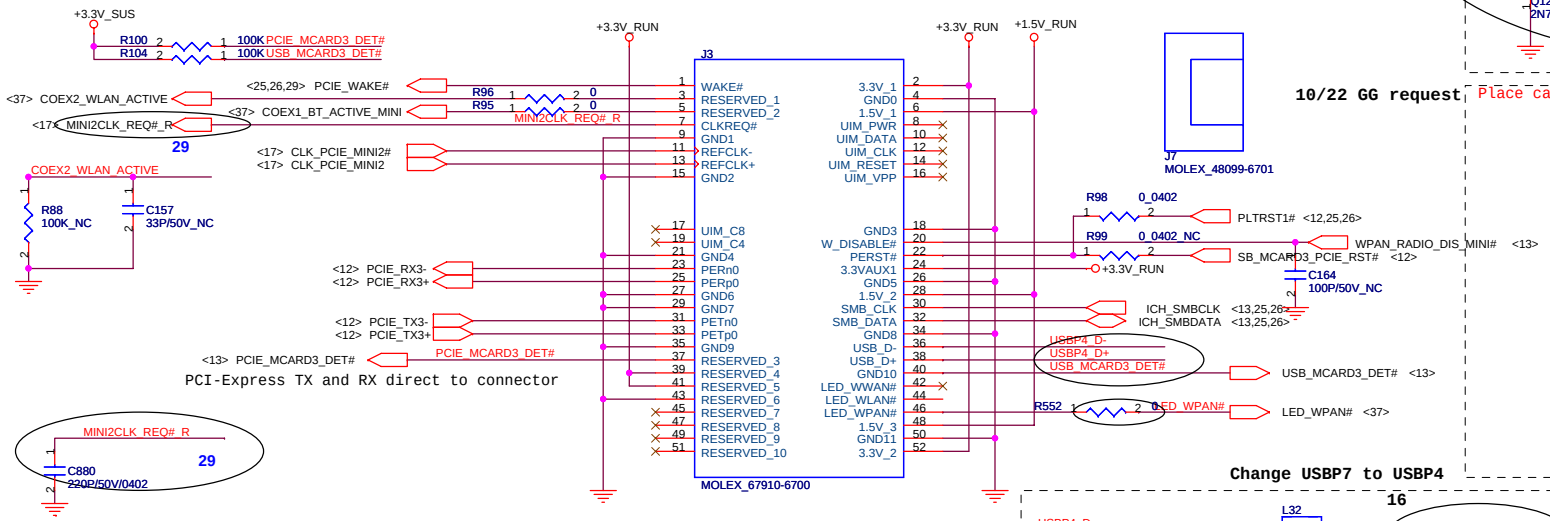
DEBUG_PINS

JMINI Pin	Debug Pin Name	EC Pin
16	HOST_DEBUG_TX	70
17	HOST_DEBUG_RX	71
19	8051_TX	82
42	8051_RX	81

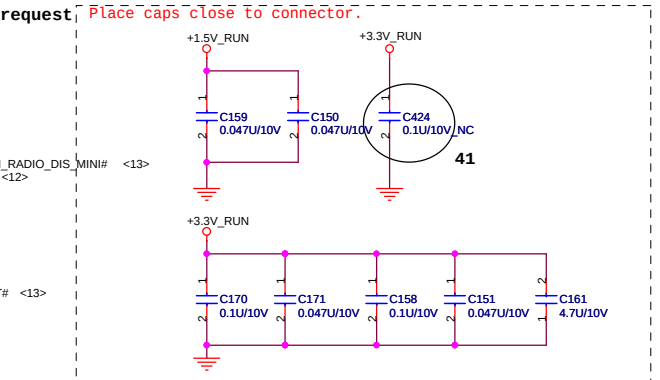




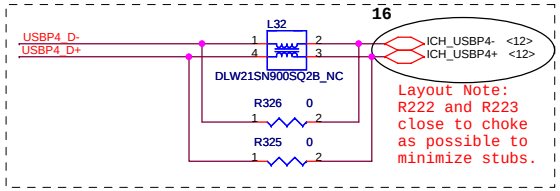
MiniCard WPAN connector

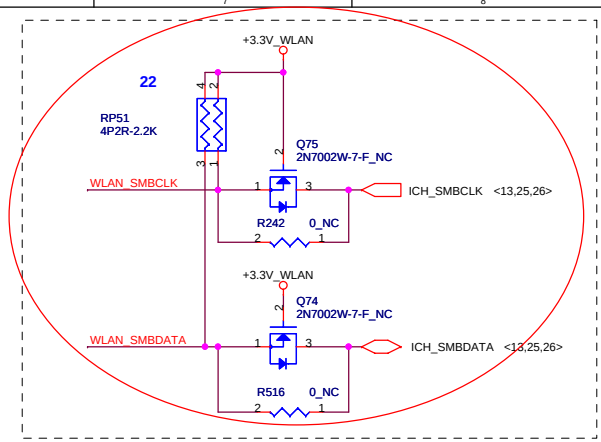


10/22 GG request

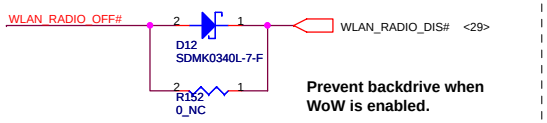


Change USBP7 to USBP4

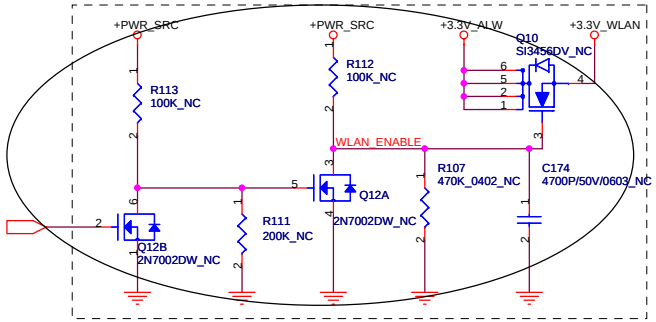




Suport for WoW



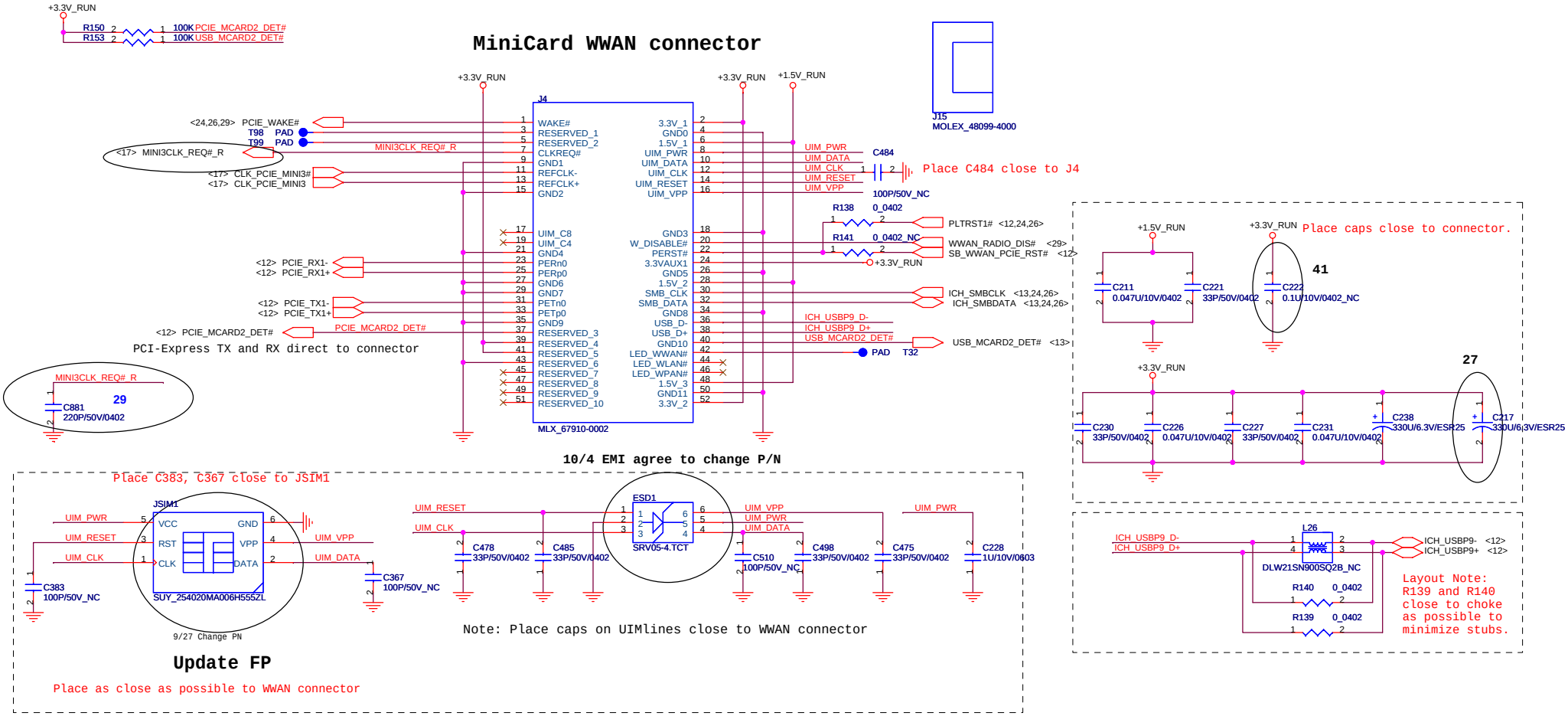
Prevent backdrive when WoW is enabled.



Title	MINI-PCI	
Size	Document Number M-08	Rev 0.1
Date: Monday, March 05, 2007	Sheet 24 of 51	

QUANTA COMPUTER

MiniCard WWAN connector



10/4 EMI agree to change P/N

QUANTA COMPUTER

Title	WWAN	
Size	Document Number VC-08B	Rev 0.1
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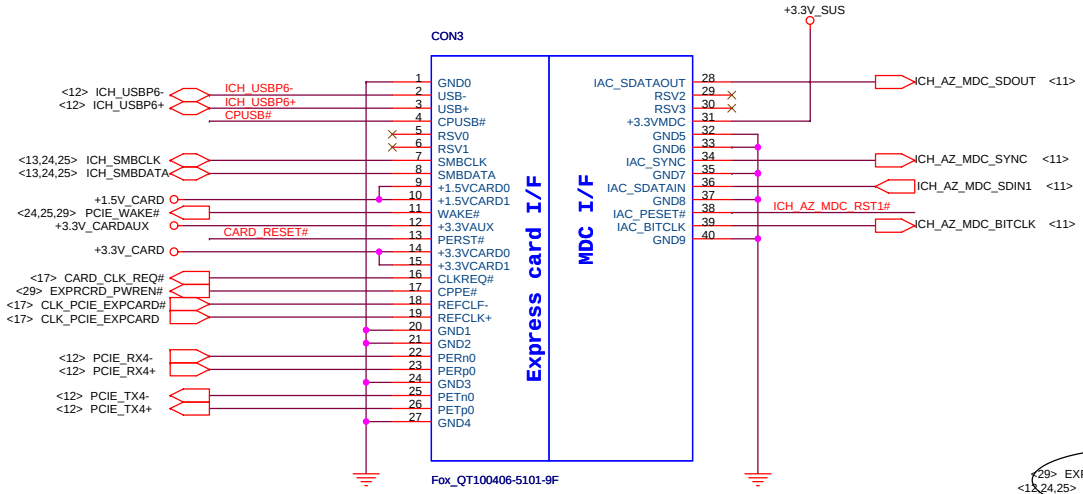
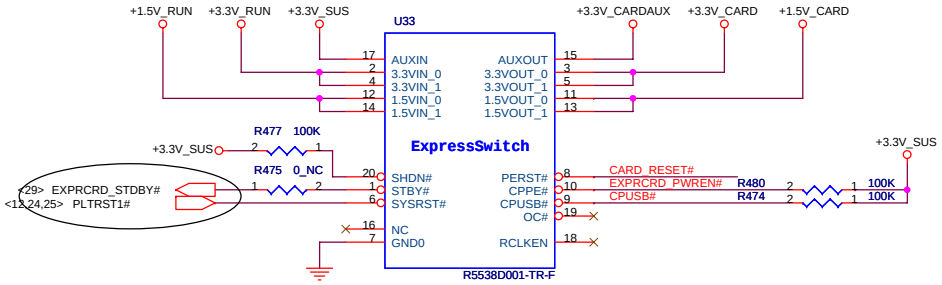
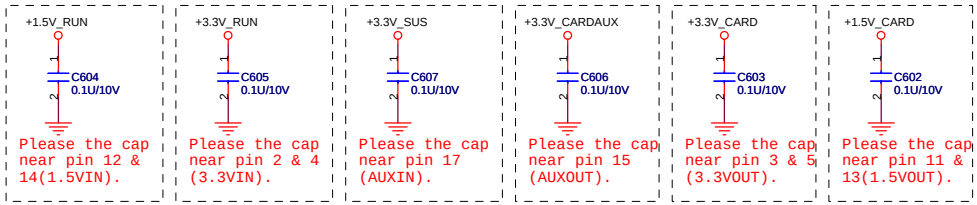
EXPRESS+MDC

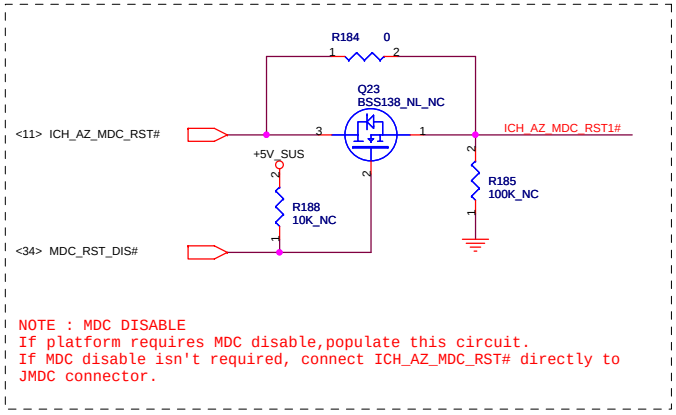


Update PN

+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.







QUANTA COMPUTER

Title	ExpressCard/SmartCard	
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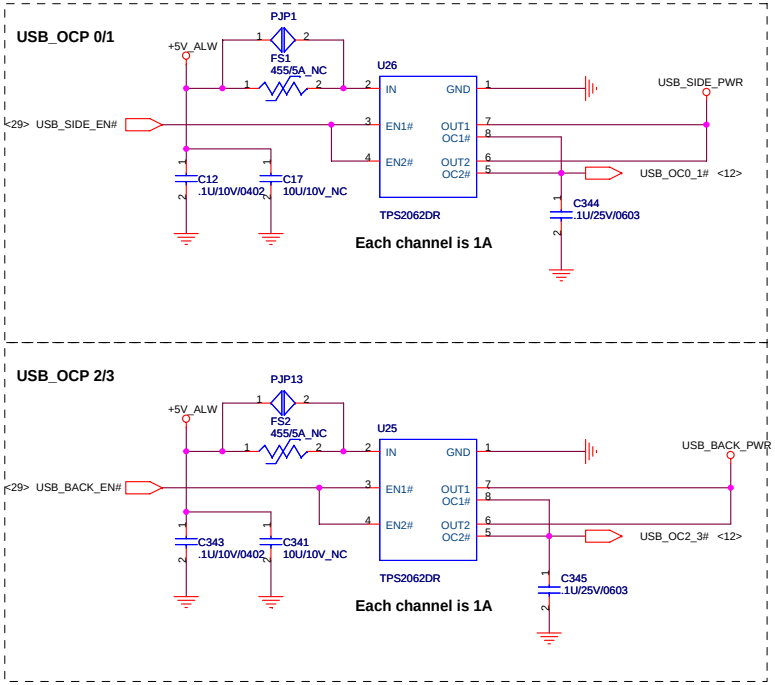
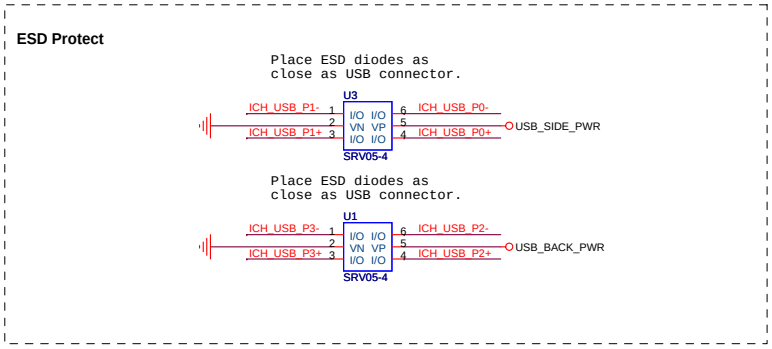
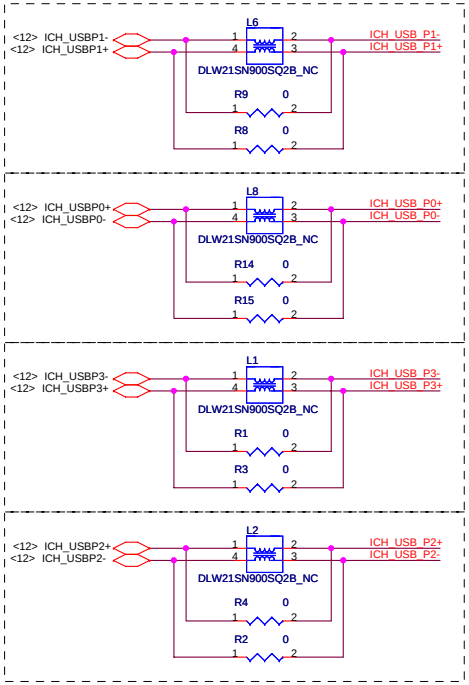
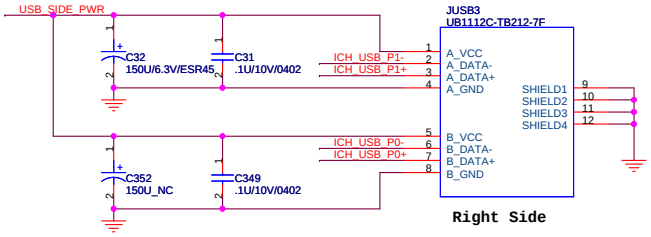
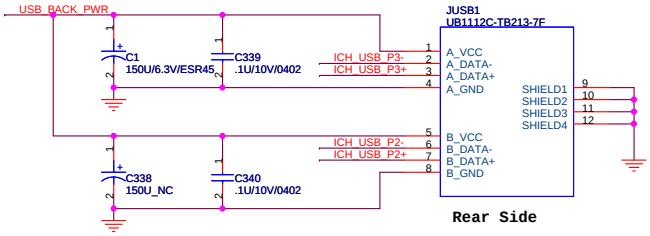
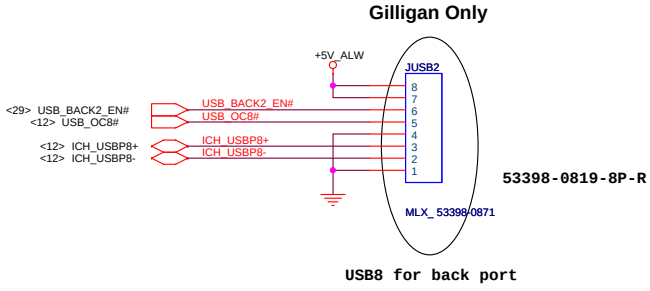






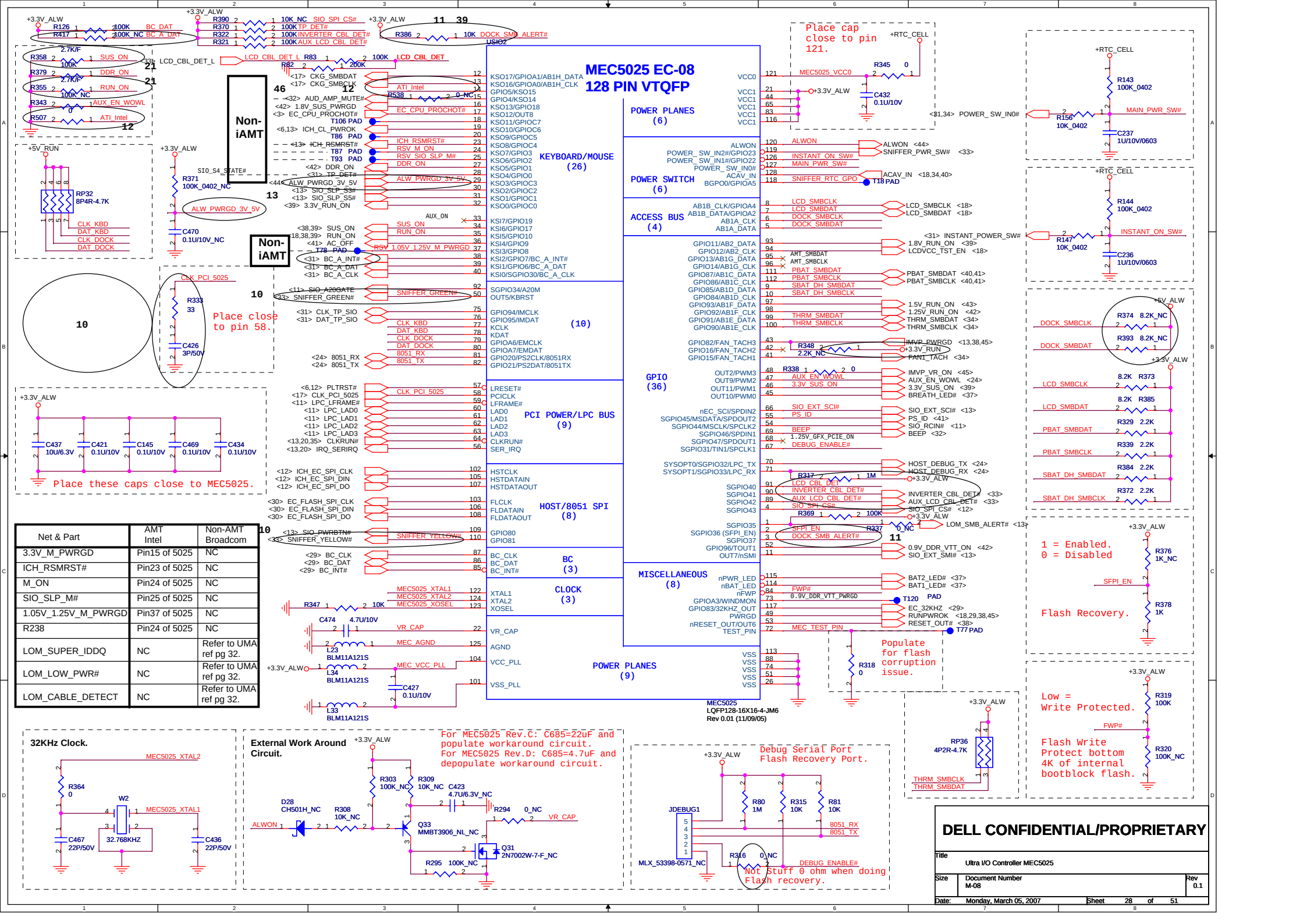






QUANTA COMPUTER

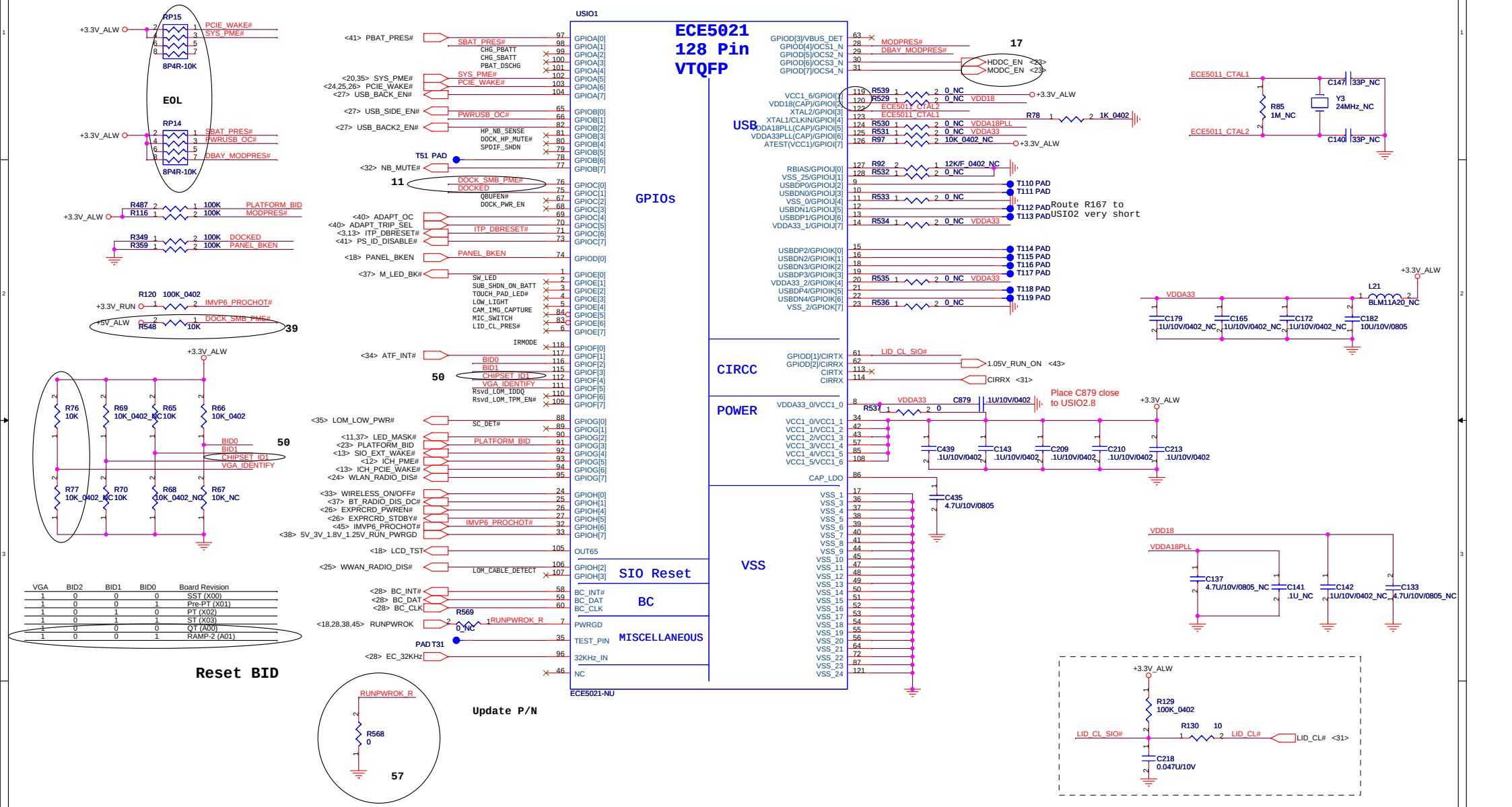
Title	USB & Flash	
Size	Document Number FM1	Rev 0.1
Date: Monday, March 05, 2007	Sheet 27 of 51	



Net & Part	AMT Intel	Non-AMT Broadcom
3.3V_M_PWRGD	Pin15 of 5025	NC
ICH_RSMRST#	Pin23 of 5025	NC
M_ON	Pin24 of 5025	NC
SIO_SLP_M#	Pin25 of 5025	NC
1.05V_1.25V_M_PWRGD	Pin37 of 5025	NC
R238	Pin24 of 5025	NC
LOM_SUPER_IDDQ	NC	Refer to UMA ref pg 32.
LOM_LOW_PWR#	NC	Refer to UMA ref pg 32.
LOM_CABLE_DETECT	NC	Refer to UMA ref pg 32.

Update to 5021

Depopulate R529, R530, R531, R532, R533, R534, R535, R536, R92, R97, C142, C133, C137, C141, C179, C165, C172, L21
Populate R537, C879.



Title	SIO (GPIO/BC/USB/CIRR)
Size	Document Number FM1 — Rev 0.1
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QUANTA COMPUTER

16Mbit (2M Byte), SPI

Non-iAMT +3.3V_SUS

Layout Note:
Place R471 within 500 mils from SPI flash.
Place R498 & R534 within 500 mils of the MEC5025.

55

<12> SPI_CS0#
<28> EC_FLASH_SPI_CLK
<28> EC_FLASH_SPI_DO
<28> EC_FLASH_SPI_DIN

R127 15
R128 15
R101 15

Non-iAMT

R105 10K
R125 10K

U14
CE# VDD
SCK
SI
SO HOLD#
WP# VSS
SST25VF016B

C896 22P/50V_NC
C201 0.1U/10V

22P : CH02206JB0K
2M : AKE28FP0K07

RTC BATTERY

+RTC_CELL
+3.3V_RTC_LDO
+PWR_SRC

D2 SDMK0340L-7-F
D1 SDMK0340L-7-F

U6
OUT IN
5/3#
GND SHDN
MAX1615_NC

C50 2.2U/6.3V
C43 1U/25V
C42 1U/25V

+RTC_1
<11> RTC_BAT_DET#
R20 1K
RTC_BAT_DET#
+RTC

J2
RTC-BATTERY_NC
MOLEX_53261-0371

TH1 H-E354X354D126p2-4
TH4 H-TC256BE354X354D126p2-4
TH22 H-E354X354D126p2-4
TH11 H-E276X315D126p2-4

Gfx

TH17 H-TC354BE354X354D126p2-4
TH23 H-TC354BE354X354D126p2-4
TH12 H-TC354BE354X354D126p2-4
TH5 H-TC354BE354X354D126p2-4

TH3 H-E354X354D126p2-4
TH20 H-C276D98p2-4
TH19 H-C276D98p2-4

SATA BTB Conn. Nut -- Only for Gilligan

TH18 H-C276D126p2-4
TH21 H-C276D126p2-4

10/18 EMI request

CPU

10/4 EMI request change to NPTH
11/28 EMI request change back to PTH

TH2 H-TC217BC236D126p2-4
TH6 H-TC354BE354X354D126p2-4
TH16 H-TC236BE354X354D126p2-3
TH13 H-TC217BC256D126p2-4

TH9 H-TC315BC236D102p2-4
TH10 H-TC315BC236D102p2-4
TH14 H-TC315BC236D102p2-4
TH15 H-TC315BC236D102p2-4

+PWR_SRC: C631 1U/25V/0603_NC → +DC_IN_SS; C632 1U/25V/0603_NC → +DC_IN_SS; C638 1U/25V/0603_NC → +5V_ALW; C639 1U/25V/0603_NC → +5V_ALW; C388 1U/25V/0603_NC → +1.5V_RUN
+3.3V_RUN: C634 1U/10V/0402_NC → +5V_ALW; C630 1U/25V/0603_NC → +5V_ALW; C633 1U/10V/0402_NC → +5V_ALW; C635 1U/10V/0402_NC → +5V_ALW; C636 1U/10V/0402_NC → +5V_ALW; C637 1U/10V/0402_NC → +5V_ALW; C642 1U/10V/0402_NC → +5V_ALW

+PWR_SRC: C356 1U/25V/0603_NC → +DC_IN_SS; C358 1U/25V/0603_NC → +DC_IN_SS; C52 1U/25V/0603_NC → +DC_IN_SS; C40 1U/25V/0603_NC → +3.3V_RUN; C370 1U/25V/0603_NC → +3.3V_RUN; C58 1U/25V/0603_NC → +3.3V_RUN; C396 1U/25V/0603_NC → +3.3V_RUN; C391 1U/25V/0603_NC → +3.3V_RUN
+3.3V_RUN: C353 1U/10V/0402_NC → +5V_ALW; C49 1U/10V/0402_NC → +5V_ALW
+1.05V_VCCP: C420 1U/10V/0402_NC → +3.3V_RUN; C410 1U/10V/0402_NC → +3.3V_RUN

TH24 h-R36X107DR16X87PB
TH25 h-R36X107DR16X87PB

DSUB
TH8 h-tc217bc256d126p2-4
TH7 h-tc217bc256d126p2-4

PV12 PAD195X130
PV13 PAD195X130
PV14 PAD195X130
PV16 PAD195X130
PV15 PAD195X130
PV9 PAD79X130
PV7 PAD79X130
PV2 PAD79X130
PV8 PAD79X130
PV6 PAD79X130
PV1 PAD79X130
PV5 PAD79X130
PV10 PAD79X130
PV11 PAD79X130
PV3 PAD79X130
PV19 PAD195X130
PV17 PAD195X130
PV18 PAD195X130
(all → GND)

QUANTA COMPUTER

Title	FLASH, RTC & KC	
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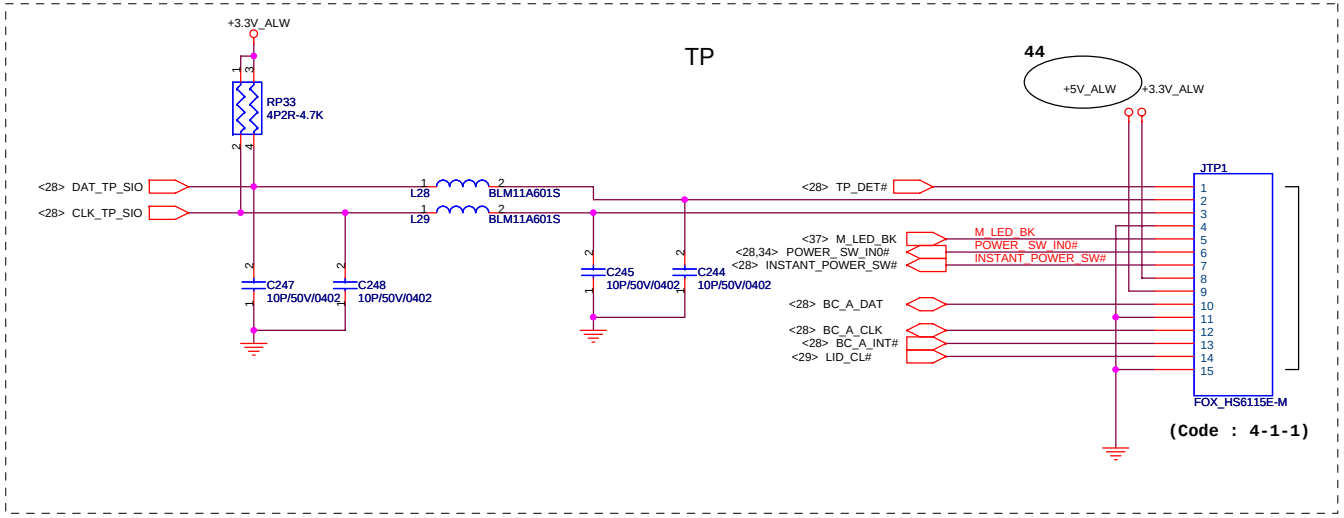

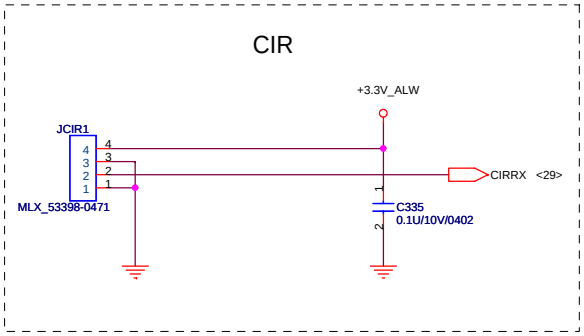

QUANTA COMPUTER

Title	TOUCH PAD, BULE TOOTH & FIR	
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INTERNAL SPEAKER AMP

Update PN

52

Package 1206 for THD+N performance for Vista Logo requirements.

AUD_LINE_OUT_L C306 .033U/25V/X7R/1206
AUD_LINE_OUT_R C307 .033U/25V/X7R/1206
AUD_HP_OUT_L C326 1uF/25V/X7R/1206
AUD_HP_OUT_R C329 1uF/25V/X7R/1206

10/18 Change 2.2u if necessary

C330 47P/50V_NC C327 47P/50V_NC C312 47P/50V_NC C311 47P/50V_NC

31

LIN- SPKR_LIN+
RIN- SPKR_RIN+

HP_OUT_L
HP_OUT_R

C334 1U/10V

AUD_SPK_ENABLE#
AMP_HP_EN
AUD_AMP_MUTE#
AUD_AMP_GAIN1
AUD_AMP_GAIN2

<28> AUD_AMP_MUTE#

32

U23

TPA6040A4 QFN 32PIN

SPKR_INL SPKR_INR HP_INL HP_INR BIAS SPKR_EN# HP_EN MUTE# GAIN1 GAIN2 HPVDD CPVDD C1P C1N CPGND PVSS CPVSS

OUTL+ OUTL- OUTR+ OUTR- HPL HPR REGEN SET VOUT VDD PVDD_8 PVDD_18 GND_28 PGND_5 PGND_21

AUD_SPK_L1 AUD_SPK_L2 AUD_SPK_R1 AUD_SPK_R2
AUD_HP_JACK_L <33>
AUD_HP_JACK_R <33>
REGEN SET SPKR_LIN- SPKR_RIN-
+VDDA
VDD +5V_SPK_AMP +5V_SPK_AMP

TPA6040A4

+5V_SPK_AMP

C318 10U/10V
10/18 Depop if not necessary
C328 1U/10V
C616 1U/10V
C324 1U/16V

R560 0_0603 <11> SPEAKER_DET# SPEAKER_DET#
R561 0_0603 R562 0_0603 R563 0_0603

JSPK1 MLX_53398-0671

C620 100P/50V_NC C621 100P/50V_NC C622 100P/50V_NC C623 100P/50V_NC

L35 FB_600ohm+-25%_100MHz _200mA_0.6ohm DC

+5V_SPK_AMP

VDD

C316 1U/10V C615 1U/10V C319 0.1U/10V

Layout Note: Place close U22.

+VDDA

C617 1U/10V C323 1U/10V

Layout Note: Place close U22.

For MAX9789A,depop R505,pop R506.

+5V_SPK_AMP

R506 100K_NC

R505 0

AUDIO_AVDD_ON AUD_AMP_MUTE#

+5V_SPK_AMP

C625 0.1U/10V

U34 NC7SZ08P5X_NL

+5V_SPK_AMP

U36 NC7SZ08P5X_NL_NC

NB_MUTE#
AUD_HP_NB_SENSE
AUD_HP_NB_SENSE_R
CODEC_GPIO_PIN_4
R545 0
AMP_HP_EN

AUDIO_AVDD_ON AUDIO_AVDD_ON <34>

R504 0_NC

REGEN

C619 0.033U/16V

C1425/C331 value need to match with C326/C290. This value be chosen in PT phase.

For MAX9789A,depop C619,pop R504.

+5V_SPK_AMP +5V_RUN +5V_SPK_AMP

L30 BLM21PG600SN1D

C310 1U/10V C315 10U/10V

Layout Note: Place close to pin 8.

C332 1U/10V C331 10U/10V C333 0.1U/10V

FB_60ohm+-25%_100MHz _3A_0.05ohm DC

Layout Note: Place close to pin 18.

+5V_SPK_AMP

R208 100K R209 100K

AUD_SPK_ENABLE#

AUD_EAPD# Q25 2N7002W-7-F

<29> NB_MUTE# Q24 2N7002W-7-F

+5V_SPK_AMP

R496 100K_NC R499 100K

AUD_AMP_GAIN1
AUD_AMP_GAIN2

R497 100K R199 100K_NC

GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

For MAX9789A,depop C614,pop R497.

R498

SET

+VDDA

2.2K_NC

C614 0.033U/16V

R497 0_NC

R501 0_0805
R207 0_0603
R189 0_0603
R198 0_0603
R202 0_0603

EMI Request

AZALIA (HD) CODEC

ICH_AZ_CODEC_BITCLK

R193 47_NC

Close to pin 6.

C305 0.1U/10V_NC

ICH_AZ_CODEC_SDOUT

R195 47_NC

Close to pin 5.

C308 0.1U/10V_NC

<11> ICH_AZ_CODEC_BITCLK
<11> ICH_AZ_CODEC_SDIN0
<11> ICH_AZ_CODEC_SDOUT
<11> ICH_AZ_CODEC_SYNC
<11> ICH_AZ_CODEC_RST#

ICH_AZ_CODEC_BITCLK
R192 33 SDIN
ICH_AZ_CODEC_SDOUT

49

<33> AUD_DMIC_CLK
<33> AUD_DMIC_IN0

AUD_DMIC_CLK
AUD_DMIC_IN0

R555 0
R556 0

CODEC_GPIO_PIN_4

For tuning.

<19> AUD_SPDIF_OUT

R204 0 AUD_EAPD# SPDIF_OUT

+3.3V_RUN

C317 10U/10V_NC C301 0.1U/10V C313 1U/10V

R203 0 R253 100K

+3.3V_RUN

C325 4.7U/10V_NC C321 0.1U/10V_NC C643 1000P/50V C309 0.1U/10V

AUD_DMIC_CLK

C647 4.7P/50V_NC

AUD_DMIC_IN0

C648 4.7P/50V_NC

49

37

+VDDA Depop R203 & pop C321 & C325 for AD1984.

C302 0.1U/16V C303 1U/10V C322 10U/10V_NC

U22 10/18 Check package

STAC9205 LQFP 48PIN

HDA_BITCLK HDA_SDI_CODEC HDA_SDO HDA_SYNC HDA_RST# DMIC_CLK DMIC0/VOL_UP/GPIO1 DMIC1/VOL_DN/GPIO2 SPDIF_IN/EAPD#/GPIO0 SPDIF_OUT NC_43 NC_44 NC_45 DVDD_CORE_1 DVDD_CORE_9 DVDD_CORE_40 DVDD_IO AVDD_25 AVDD_38 DVSS AVSS_26 AVSS_42

SENSE_A SENSE_B PORT_A_L PORT_A_R VREFOUT_A PORT_B_L PORT_B_R VREFOUT_B PORT_C_L PORT_C_R VREFOUT_C PORT_D_L PORT_D_R PORT_E_L PORT_E_R GPIO4/VREFOUT_E PORT_F_L PORT_F_R GPIO3/VREFOUT_F CD_L CD_GND CD_R PC_BEEP MONO_OUT VREFFILT CAP2

AUD_SENSE_A AUD_SENSE_B AUD_HP_OUT_L AUD_HP_OUT_R AUD_EXT_MIC_L <33> AUD_EXT_MIC_R <33> AUD_VREFOUT_B <33> AUD_MIC_IN_L AUD_MIC_IN_R AUD_LINE_OUT_L AUD_LINE_OUT_R DOCK_HP_MUTE# AUD_SPDIF_SHDN AUD_PC_BEEP AC97VREFI CAP2

STAC9205

+VDDA

R201 100K

R196 10K R194 10K

10_NC R200

C314 10U/10V C304 10U/10V C320 0.1U/10V_NC

C304 must be 1U & Pop C320 & R200 for AD1984.

Layout Note: Close to U22 Pin 13.

R493 5.1K/F +VDDA

AUD_SENSE_A

R491 39.2K/F R492 20K/F C611 1000P/50V

<33> AUD_HP_NB_SENSE AUD_HP_NB_SENSE AUD_MIC_SWITCH <33>

Q53 2N7002W-7-F Q54 2N7002W-7-F

Close to U22

+VDDA C300 0.1U/16V

C299 0.1U/10V R187 20K

AUD_PC_BEEP BEEP2 BEEP1

BEEP <28>
SPKR <13>

R190 10K

U21 74LVC1G86GW

DELL CONFIDENTIAL/PROPRIETARY

Title	Azelia CODEC(STAC9205))	
Size	Document Number M-08	Rev 0.1
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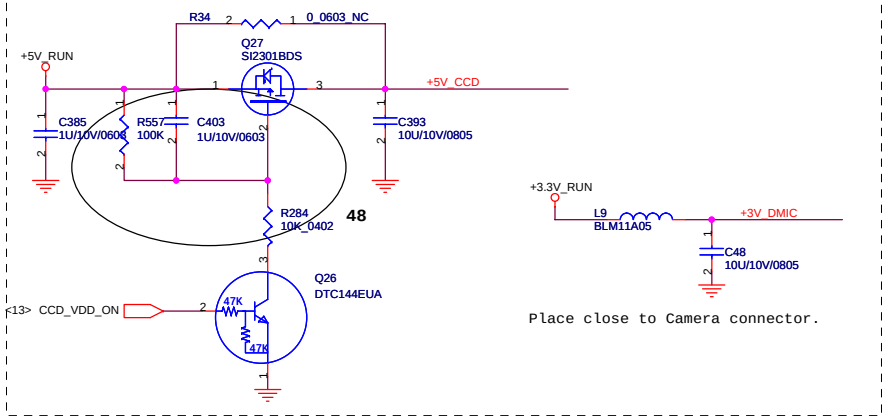
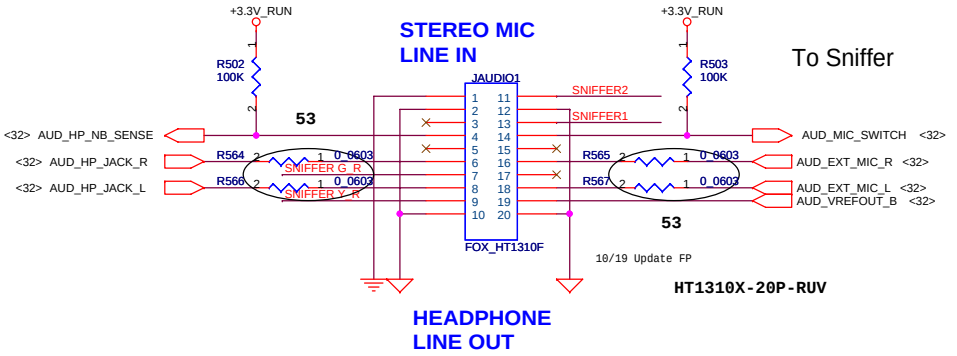
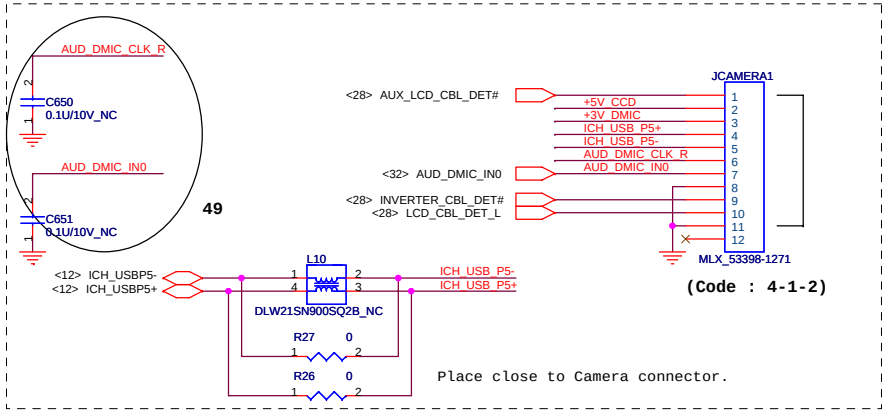
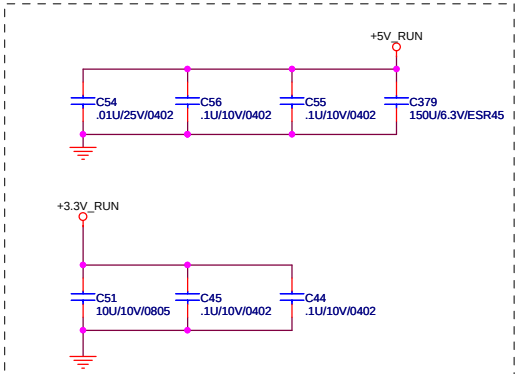
Digital Microphone & Camera

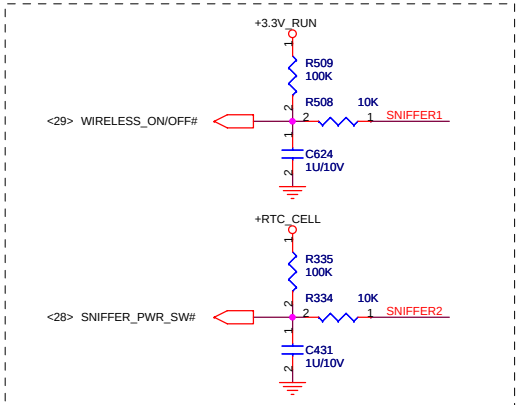


Update PN

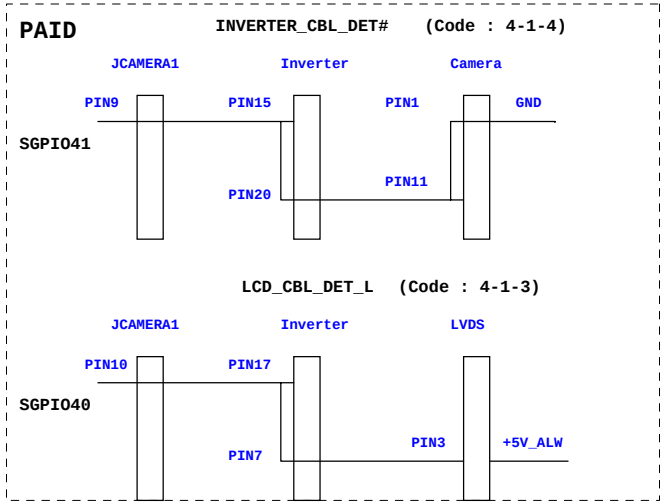


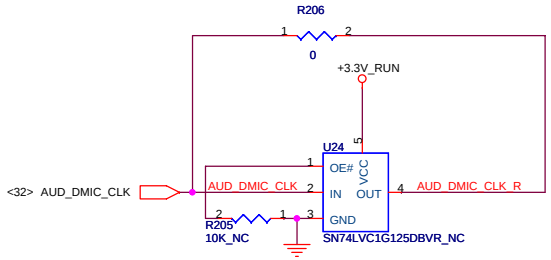


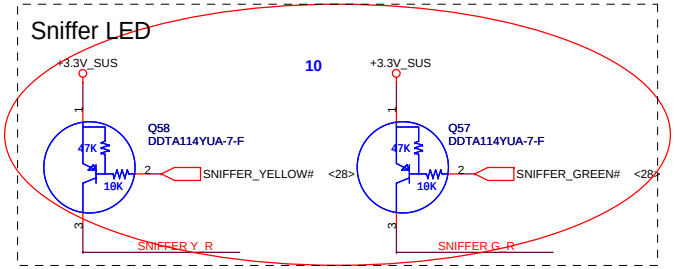




PAID







DELL CONFIDENTIAL/PROPRIETARY

Title	AUDIO CONN	
Size	Document Number M-08	Rev 0.1
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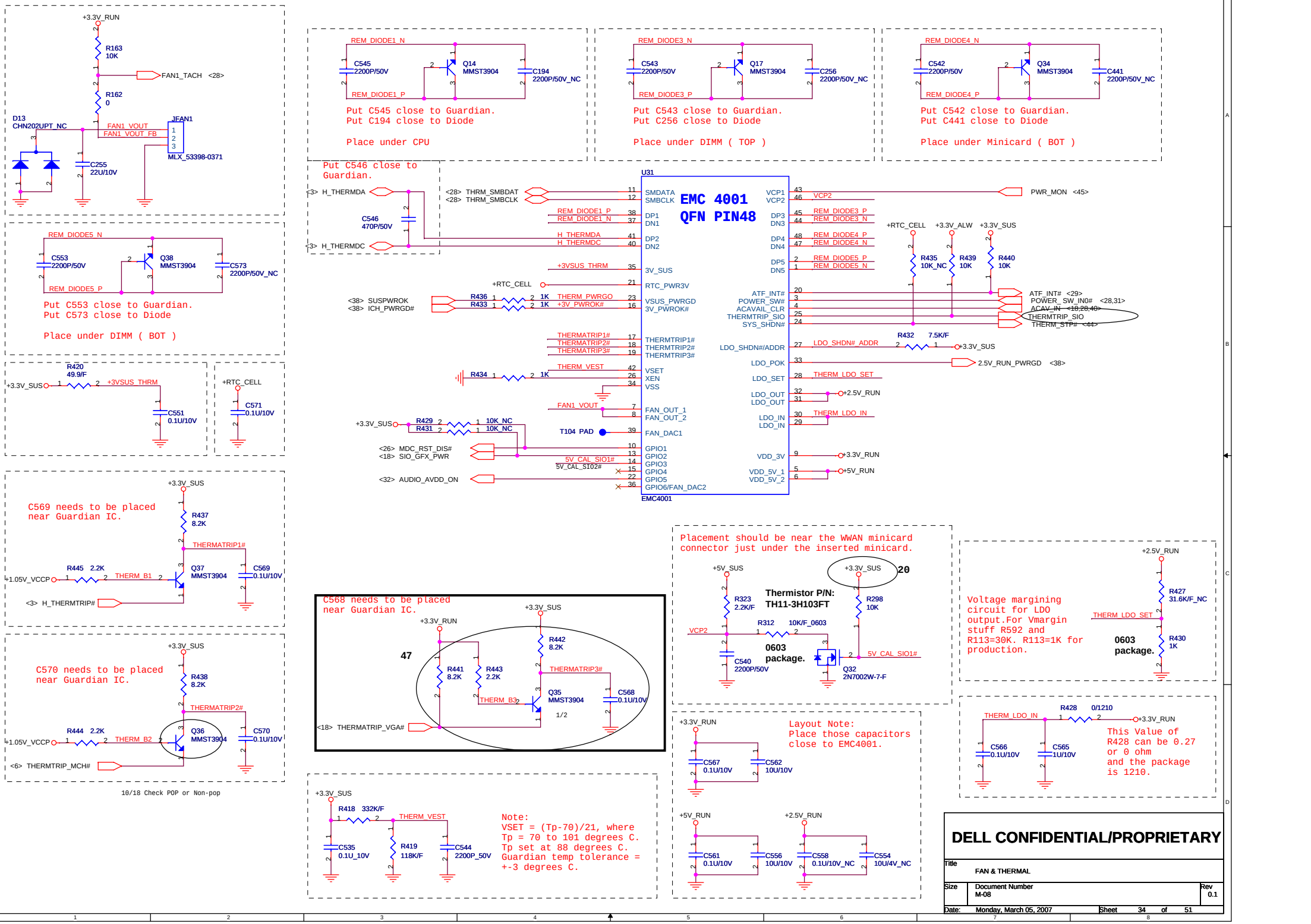

DELL CONFIDENTIAL/PROPRIETARY

Title	FAN & THERMAL	
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Refer to M07_LOM4401_X06 schematic.

Refer to M07_LOM4401_X06 schematic.

Close to power pins
0.1U*13 pcs

Place C1284 close to pin65

EMI requirement on 0812

Refer to M07_LOM4401_X06 schematic.
'+3VLAN should be sourced from +3VSUS instead of +3VSRC since WOL is not supported on C/G.

These three pin LINK_LED10#, LINK_LED100#, ACT_LED are open-drain type.

Place R219, C640, C347 close to pin69

Place L66, C29, C644 close to pin57.

Place R942 close to U62

Place L7, C22, C23 close to pin64.

Resistors must be rated at least 1/16W. Place termination resistors close to the ASIC.

Delete R630&R631 per 4401 ref schematic

Note: EXT_POR_L has a internl pull up.

Note: BCM4401 requires 16-bit R/W data width

Note: The BCM4401 has weak internal pulldown resistors on the following signals:
SPROM_CS, SPROM_CLK, SPROM_DOUT, SPROM_DIN.

Place R17, C33 close to U62.118

Refer to M07_LOM4401_X06 schematic.
R489 and R490 removed from schematic because of Bios can configure the state of CLKRUN# signal.

BCM4401 B0

Title	LAN (BCM4401)
Size	Document Number FM1
Rev	0.1
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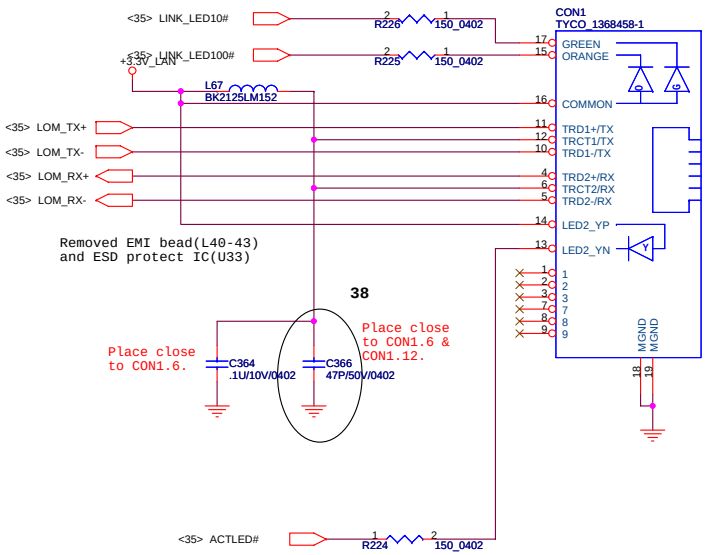

Title	LAN Jack	
Size	Document Number FM1	Rev 0.1
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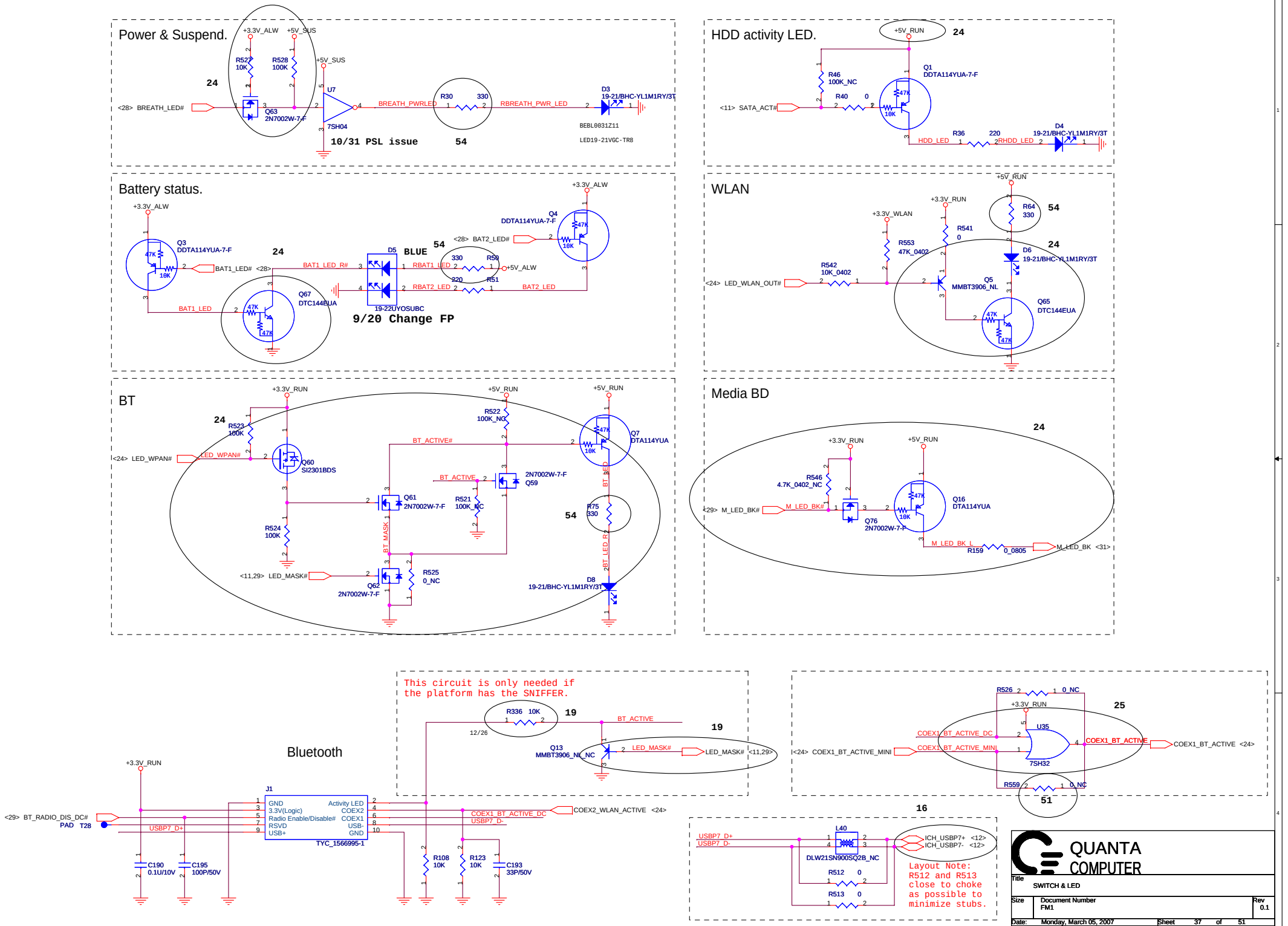
Power & Suspend.
+3.3V_ALW
+5V_SUS
R527 10K
R528 100K
24
<28> BREATH_LED#
Q63 2N7002W-7-F
U7
7SH04
BREATH_PWRLED
R30 330
RBREATH_PWR_LED
D3 19-21/BHC-YL1M1RY/3T
BEBL0031Z11
LED19-21VGC-TR8
10/31 PSL issue
54
HDD activity LED.
+5V_RUN
24
Q1 DDTA114YUA-7-F
R46 100K_NC
R40 0
<11> SATA_ACT#
HDD_LED
R36 220
RHDD_LED
D4 19-21/BHC-YL1M1RY/3T
Battery status.
+3.3V_ALW
Q3 DDTA114YUA-7-F
Q4 DDTA114YUA-7-F
24
D5 BLUE
54
<28> BAT2_LED#
BAT1_LED# <28>
BAT1_LED_R#
RBAT1_LED
RBAT2_LED
330 R50
220 R51
+5V_ALW
BAT2_LED
BAT1_LED
Q67 DTC144EUA
19-22UYOSUBC
9/20 Change FP
WLAN
+5V_RUN
+3.3V_RUN
+3.3V_WLAN
R64 330
54
R541 0
R553 47K_0402
24
D6 19-21/BHC-YL1M1RY/3T
R542 10K_0402
<24> LED_WLAN_OUT#
Q5 MMBT3906_NL
Q65 DTC144EUA
BT
+3.3V_RUN
+5V_RUN
24
R523 100K
<24> LED_WPAN#
LED_WPAN#
Q60 SI2301BDS
R522 100K_NC
BT_ACTIVE#
Q7 DTA114YUA
BT_ACTIVE
2N7002W-7-F Q59
Q61 2N7002W-7-F
R521 100K_NC
54
R75 330
R524 100K
BT_MASK
<11,29> LED_MASK#
Q62 2N7002W-7-F
R525 0_NC
D8 19-21/BHC-YL1M1RY/3T
Media BD
24
+3.3V_RUN
+5V_RUN
R546 4.7K_0402_NC
<29> M_LED_BK#
M_LED_BK#
Q16 DTA114YUA
Q76 2N7002W-7-F
M_LED_BK_L
R159 0_0805
M_LED_BK <31>
This circuit is only needed if the platform has the SNIFFER.
R336 10K
19
12/26
BT_ACTIVE
Q13 MMBT3906_NL_NC
LED_MASK#
<11,29>
Bluetooth
+3.3V_RUN
J1
<29> BT_RADIO_DIS_DC#
PAD T28
USBP7_D+
GND
3.3V(Logic)
Radio Enable/Disable#
RSVD
USB+
Activity LED
COEX2
COEX1
USB-
GND
TYC_1566995-1
C190 0.1U/10V
C195 100P/50V
R108 10K
R123 10K
C193 33P/50V
COEX1_BT_ACTIVE_DC
USBP7_D-
COEX2_WLAN_ACTIVE <24>
R526 0_NC
25
U35
7SH32
<24> COEX1_BT_ACTIVE_MINI
COEX1_BT_ACTIVE_DC
COEX1_BT_ACTIVE_MINI
COEX1_BT_ACTIVE
COEX1_BT_ACTIVE <24>
R559 0_NC
51
16
USBP7_D+
USBP7_D-
L40
DLW21SN900SQ2B_NC
ICH_USBP7+ <12>
ICH_USBP7- <12>
R512 0
R513 0
Layout Note:
R512 and R513
close to choke
as possible to
minimize stubs.
QUANTA COMPUTER
Title
SWITCH & LED
Size
Document Number
FM1
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0.1
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Non-iAMT

<42> 1.25V_RUN_PWRGD — R460 1 2 0

<43> 1.5V_RUN_PWRGD
<43> 1.05V_RUN_PWRGD
<34> 2.5V_RUN_PWRGD
<18> GFX_PWRGD
R462 1 2 0
R461 1 2 0
R467 1 2 0_NC
R463 1 2 0_NC
9/20 Depop R463

+5V_RUN — D33 SDMK0340L-7-F — R471 10K — Q49 MMBT3906_NL — C601 0.1U/10V — R473 200K — C600 2200P/50V — R472 4.7K — Q50 MMST3904

+5V_ALW

+1.8V_RUN — D32 SDMK0340L-7-F_NC — R468 10K_NC — Q45 MMBT3906_NL_NC — C598 0.1U/10V_NC — R469 200K_NC — C599 2200P/50V_NC — R466 4.7K_NC — Q47 MMST3904_NC

+1.8V_SUS

9/20 Depop Q47

+3.3V_RUN — D31 SDMK0340L-7-F — R453 10K — Q43 MMBT3906_NL — C590 0.1U/10V — R454 200K — C589 2200P/50V — R464 4.7K — Q46 MMST3904

+3.3V_ALW

5V_3V_1.8V_1.25V_RUN_PWRGD <29>

+3.3V_RUN — R154 2.2K_NC — U17D

<13,28,45> IMVP_PWRGD
<28> RESET_OUT#

74AHC08PW

+3.3V_SUS — R148 100K — Q15 2N7002W-7-F — ICH_PWRGD# <34>

ICH_PWRGD <6,13>

Keep Away from high speed buses

+3.3V_SUS — R137 20K — C223 0.01U/25V

+3.3V_ALW — C212 0.1U/10V — U18A — NC7WZ14P6X_NL

+3.3V_ALW — U18B — NC7WZ14P6X_NL

+3.3V_ALW — C200 0.1U/10V — U17A

<18,28,39> RUN_ON — R151 0

74AHC08PW

U17B — 74AHC08PW — RUNPWROK <18,28,29,45>

<28,39> SUS_ON — U17C — 74AHC08PW — SUSPWROK <34>

13

12

+3.3V_SUS — D17 SDMK0340L-7-F — R183 10K — Q22 MMBT3906_NL — C291 0.1U/10V — R182 200K — C292 2200P/50V — D16 SDMK0340L-7-F — R181 200K

+3.3V_ALW — C293 0.1U/10V — U20 — NC7SZ14P5X_NL

+5V_SUS — D14 SDMK0340L-7-F — R178 10K — Q21 MMBT3906_NL — C289 0.1U/10V — R179 200K — C290 2200P/50V — D15 SDMK0340L-7-F — R177 200K — R180 200K

+5V_ALW

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Title	System Reset Circuit	
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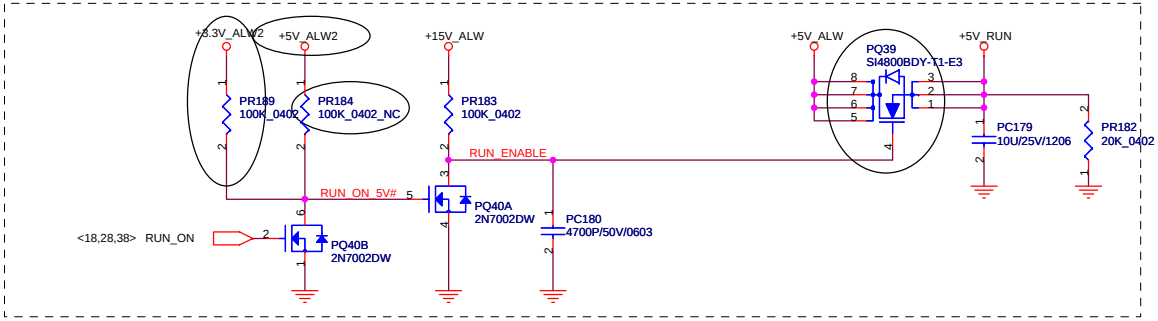

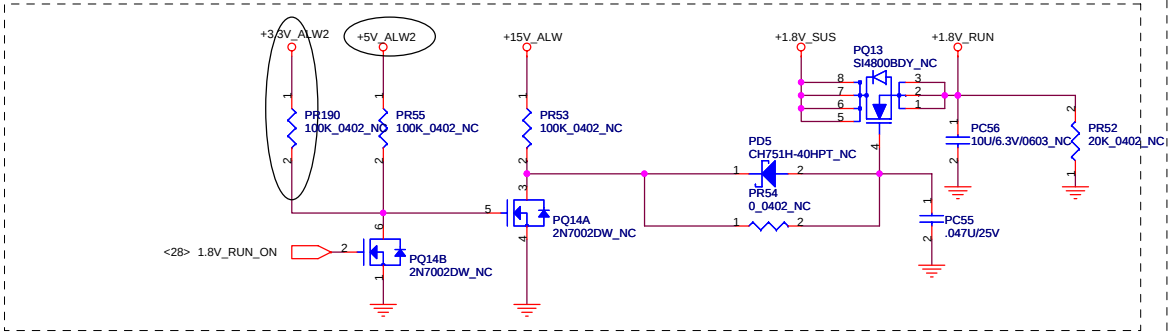

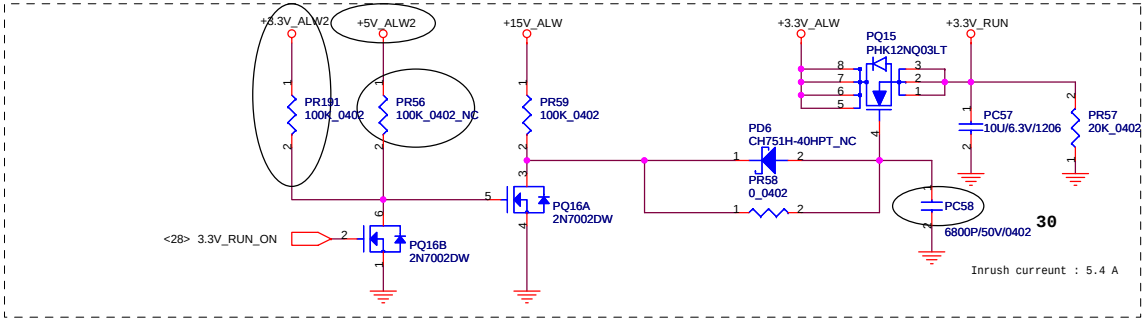

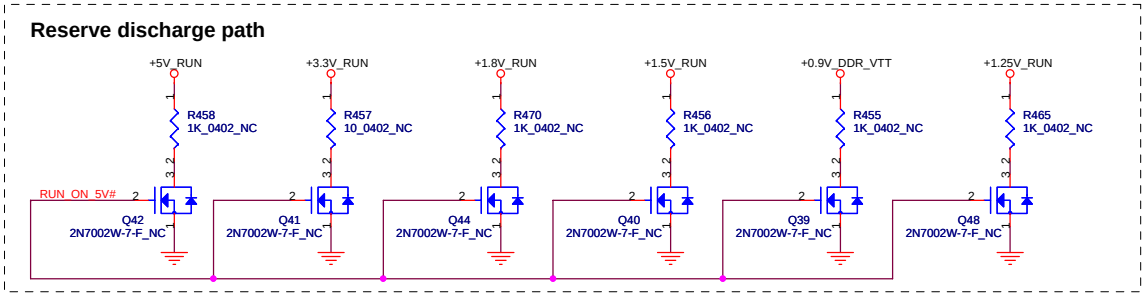

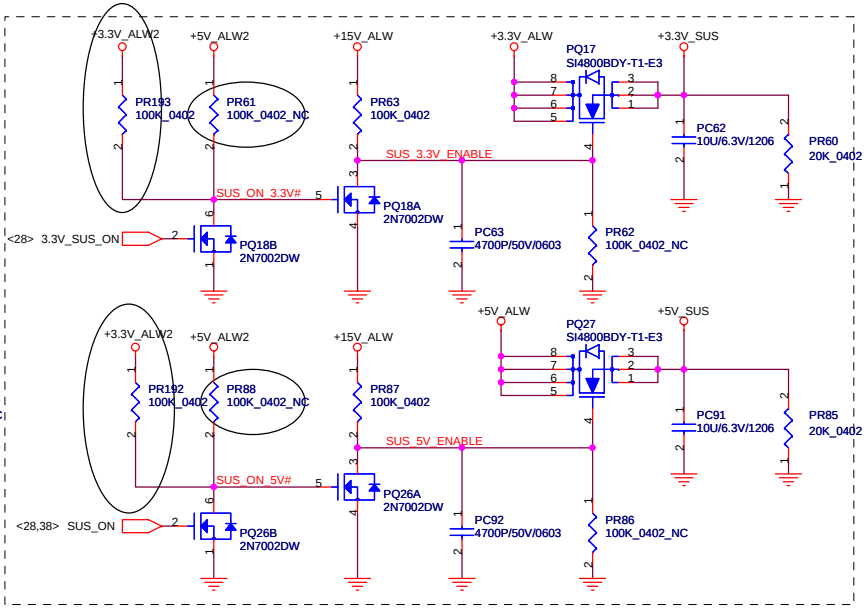

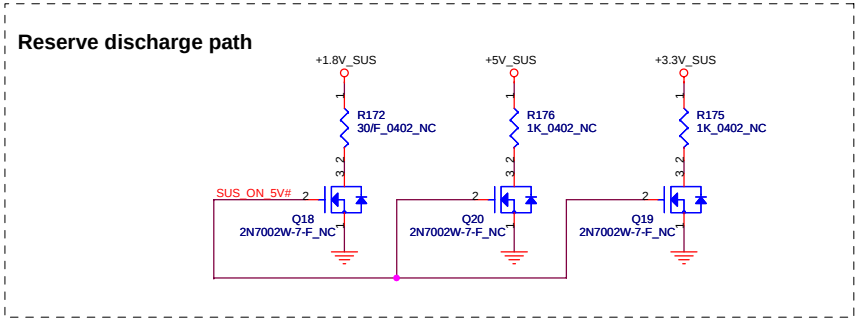

QUANTA COMPUTER

Title	RUN POWER SW	
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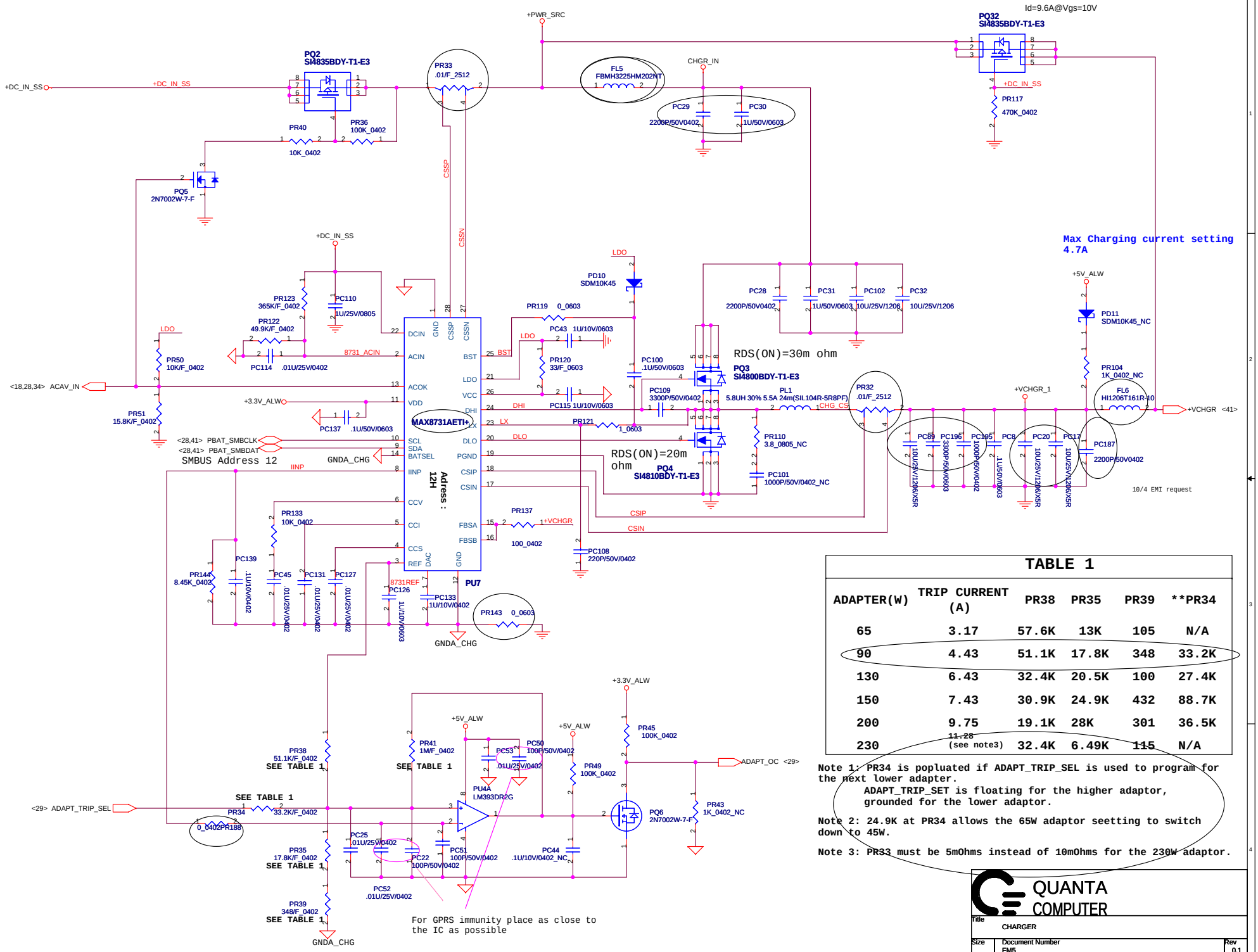

TABLE 1

ADAPTER(W)	TRIP CURRENT (A)	PR38	PR35	PR39	**PR34
65	3.17	57.6K	13K	105	N/A
90	4.43	51.1K	17.8K	348	33.2K
130	6.43	32.4K	20.5K	100	27.4K
150	7.43	30.9K	24.9K	432	88.7K
200	9.75	19.1K	28K	301	36.5K
230	11.28 (see note3)	32.4K	6.49K	115	N/A

Note 1: PR34 is popluated if ADAPT_TRIP_SEL is used to program for the next lower adapter.
ADAPT_TRIP_SET is floating for the higher adaptor, grounded for the lower adaptor.

Note 2: 24.9K at PR34 allows the 65W adaptor seetting to switch down to 45W.

Note 3: PR33 must be 5mOhms instead of 10mOhms for the 230W adaptor.

QUANTA COMPUTER

Title	CHARGER	
Size	Document Number FM5	Rev 0.1
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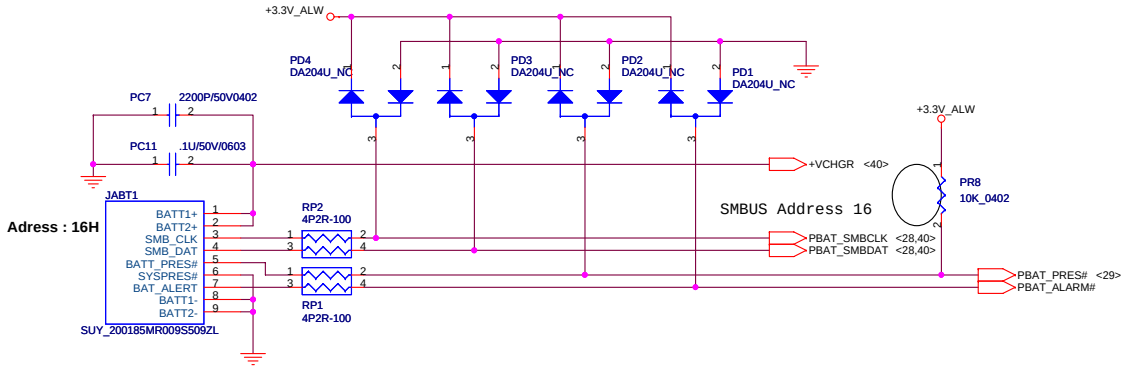

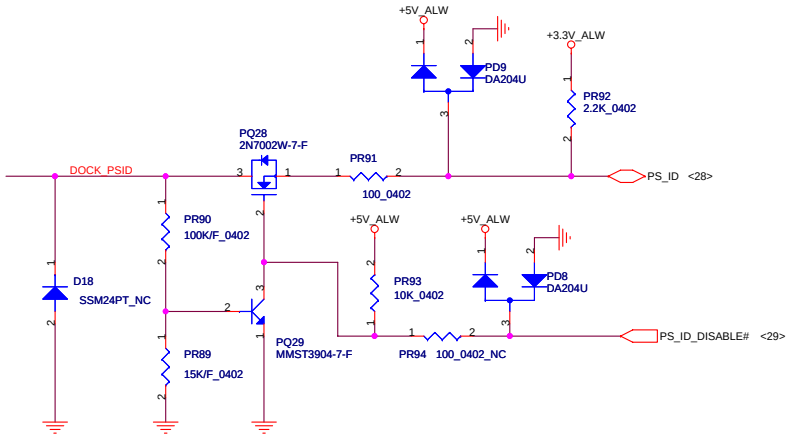

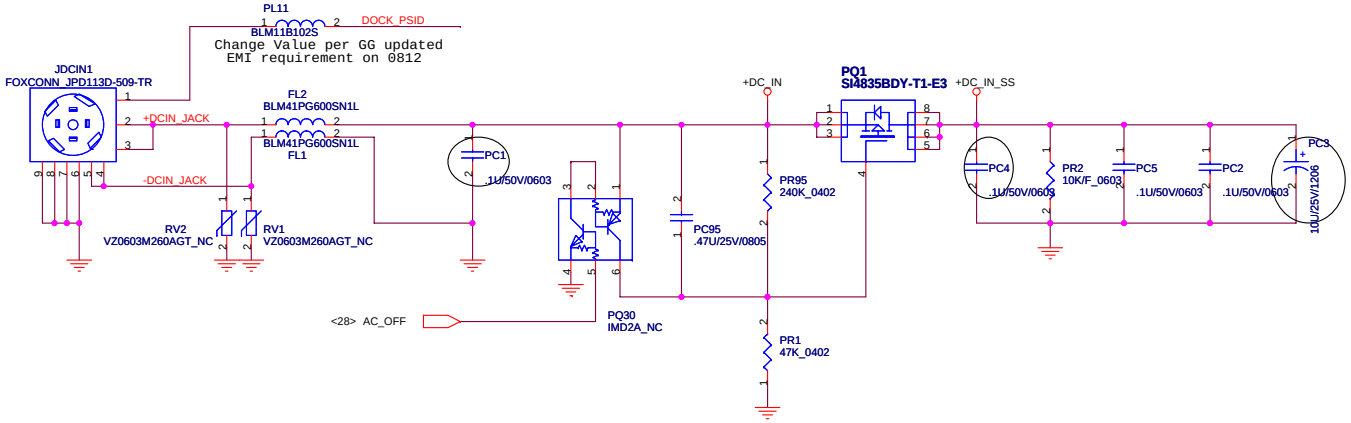

QUANTA COMPUTER

Title	DCIN,BATT CONNECTOR	
Size	Document Number FM5	Rev 0.1
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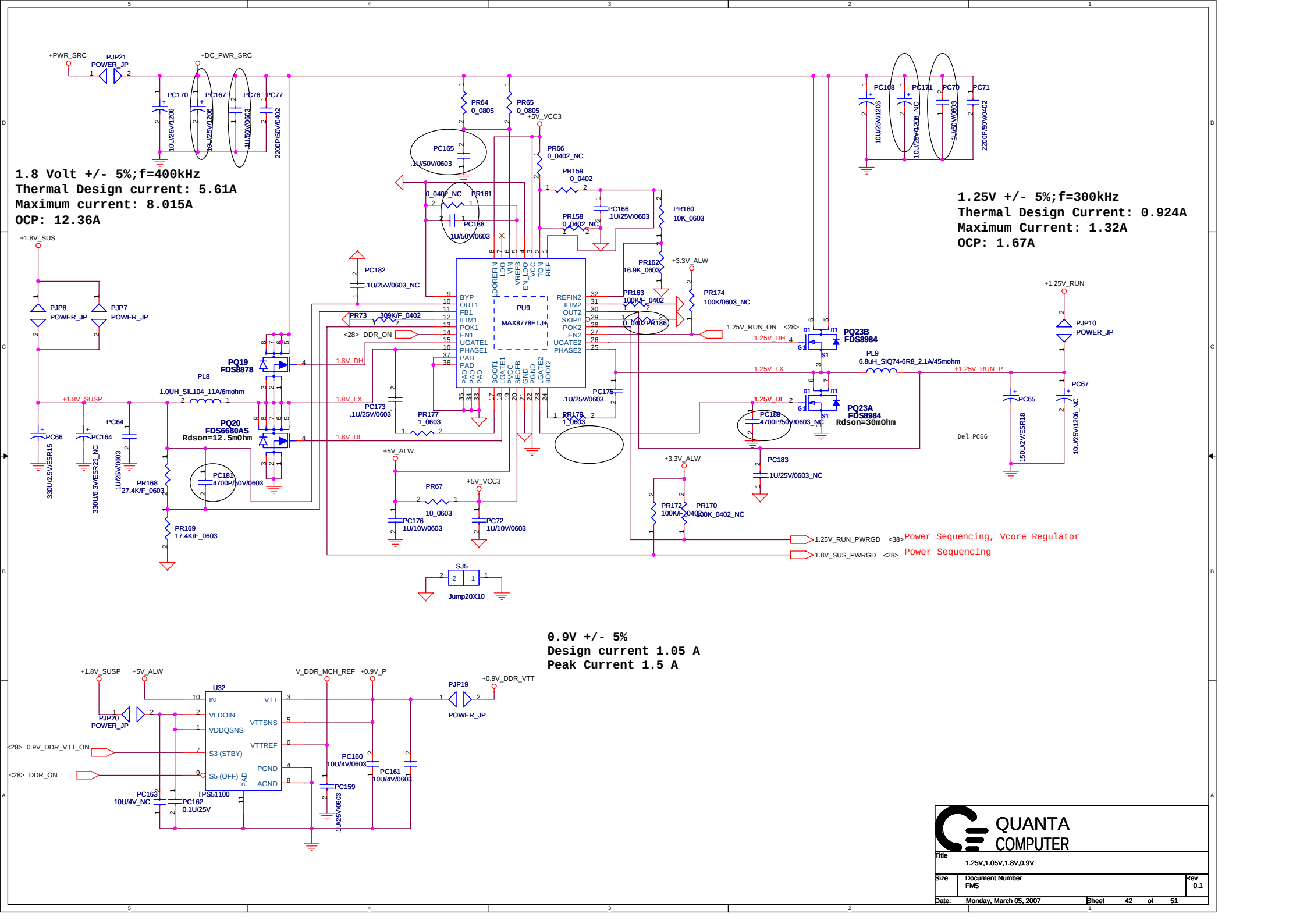
1.8 Volt +/- 5%;f=400kHz
Thermal Design current: 5.61A
Maximum current: 8.015A
OCP: 12.36A
1.25V +/- 5%;f=300kHz
Thermal Design Current: 0.924A
Maximum Current: 1.32A
OCP: 1.67A
0.9V +/- 5%
Design current 1.05 A
Peak Current 1.5 A
+PWR_SRC
+DC_PWR_SRC
PJP21
POWER_JP
+1.8V_SUS
+1.8V_SUSP
+5V_ALW
+5V_VCC3
+3.3V_ALW
+1.25V_RUN
PU9
MAX8778ETJ+
PQ19
FDS8878
PQ20
FDS6680AS
Rdson=12.5mOhm
PQ23B
FDS8984
PQ23A
FDS8984
Rdson=30mOhm
PL8
1.0UH_SIL104_11A/6mohm
PL9
6.8uH_SIQ74-6R8_2.1A/45mohm
1.8V_DH
1.8V_LX
1.8V_DL
1.25V_DH
1.25V_LX
1.25V_DL
1.25V_RUN_ON
1.25V_RUN_P
<28> DDR_ON
1.25V_RUN_PWRGD <38>
1.8V_SUS_PWRGD <28>
Power Sequencing, Vcore Regulator
Power Sequencing
SJ5
Jump20X10
U32
TPS51100
+0.9V_DDR_VTT
V_DDR_MCH_REF
+0.9V_P
<28> 0.9V_DDR_VTT_ON
Del PC66
QUANTA COMPUTER
Title
1.25V,1.05V,1.8V,0.9V
Size
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Rev
0.1
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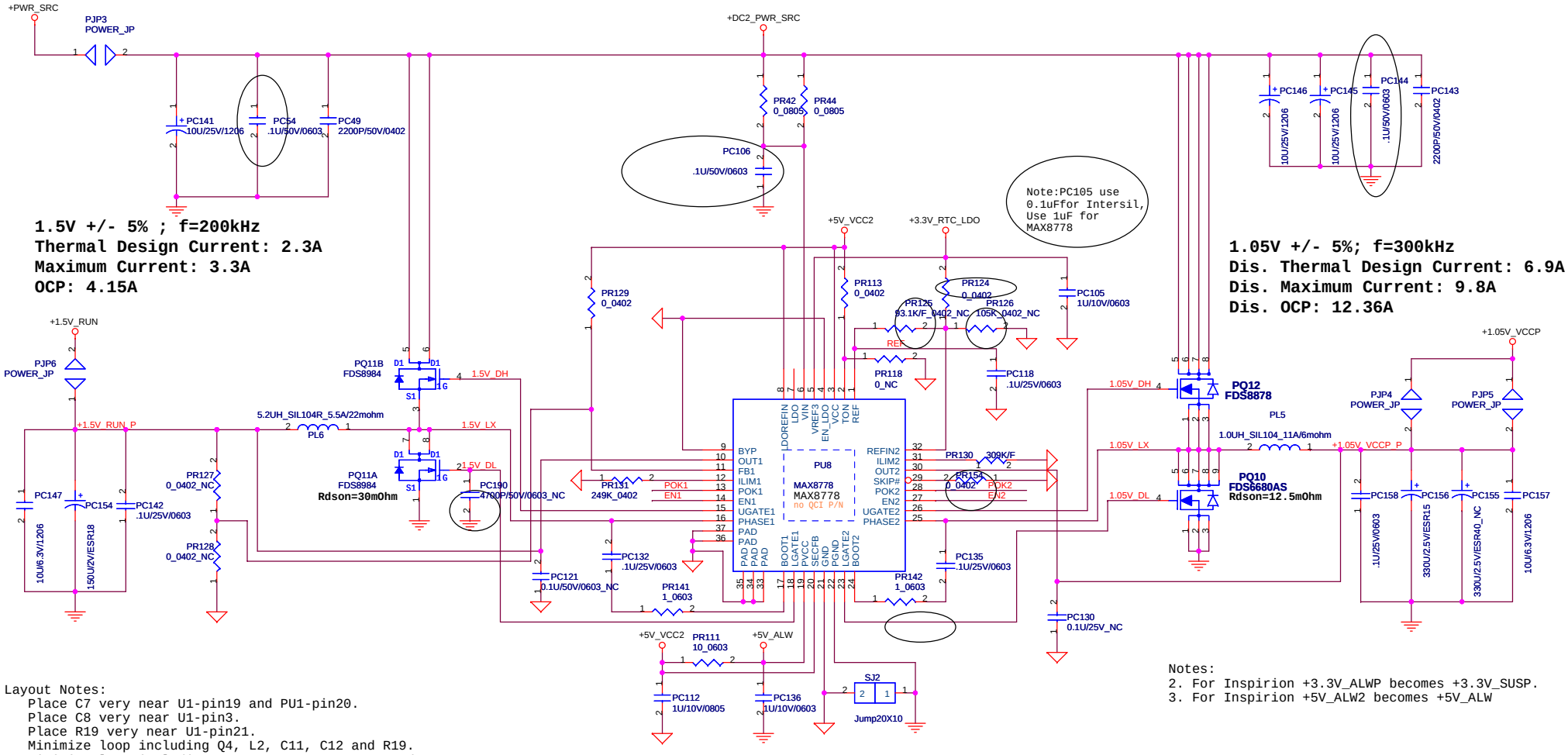
+1.5V_RUN /+1.05V_VCCP /+3.3V_ALW /+3.3_RTC_LDO



Layout Notes:
- Place C7 very near U1-pin19 and PU1-pin20.
- Place C8 very near U1-pin3.
- Place R19 very near U1-pin21.
- Minimize loop including Q4, L2, C11, C12 and R19.
- Minimize loop including Q2, L3, C17, C18, C19 and R19.
- Route GNDA_DC2 using at least 25 mil trace width.
- Minimize GNDA_DC2 trace length.
- Place C15 near U1-pin7.
- Place C20 near U1-pin5.
- Place R7 near U1-pin11.
- Place R12 near U1-pin31.
- Place R3, C10 near U1-pins 24 and 25.
- Place R2, C9 near U1-pins 16 and 17.
- Route +1.05V_BOOT, +1.05V_BOOST, +1.5V_BOOT, +1.5V_BOOST using 25mil trace width and minimize lengths.
- Connect large copper fill areas to PQ1, PQ2, PQ3 and Q4 signals for thermal improvement.
- Minimize length of +1.5V_RUN_PL and +1.05V_VCCP_PL.
- Place C1, C2, C3, C22 very near Q3-pins 5, 6, 7, 8.
- Place C4, C5, C6, C23 very near Q1-pins 5, 6, 7, 8.
- Route +DC2_PWR_SRC using 50 mil trace width and minimize length.
- Route OUT1 and OUT2 away from inductor and switch-node. Sense Vout directly at output bulk cap.

Notes:
2. For Inspirion +3.3V_ALWP becomes +3.3V_SUSP.
3. For Inspirion +5V_ALW2 becomes +5V_ALW

QUANTA COMPUTER		
Title: 1.5V,1.05V		
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DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

Ton:OUT1/OUT2 Switching Frequency
VDD 200kHz/300kHz
OPEN (REF): 400kHz/300kHz
GND: 400kHz/500kHz

Place these CAPs close to FETs

Place these CAPs close to FETs

No Install PR79 for ISL6236
Install PR79=0Ohm for MAX8778

No Install for ISL6236
Install 10 ohm for MAX8778

3.3 Volt +/- 5%
Design Current:7.18A
Maximum current:10.25A
OCP: 12.36A

5 Volt +/- 5%
Design Current: 7.43 A
Maximum current:10.6A
OCP: 12.96A

+PWR_SRC
PJP11 POWER_JP
PC172 10U/25V/1206
PC174 10U/25V/1206
PC177 10U/25V/1206
PC178 10U/25V/1206_NC
+DC1_PWR_SRC
PC82 .1U/50V/0603
PC85 2200P/50V/0402
PR180 0_0805
PR181 0_0805
PC84 .1U/50V/0603
+3.3V_ALW2
PR79 0_0402_NC
PC186 1U/10V/0603
+5V_ALW2
PR176 10_0603
+5V_VCC1
PC81 4.7U/10V/1206
PR173 0_0402_NC
PC80 1U/10V/0603
PC78 .1U/10V/0402
PR171 0_0402_NC
PR72 0_0402_NC
PR167 0_0402
PR68 0_0402_NC
PC83 .1U/50V/0603
PC79 2200P/50V/0402
+3.3V_ALW
FBMH4532HM681 FL10
FBMH4532HM681 FL12
FBMH4532HM681 FL11
+5V_ALW
PJP12 POWER_JP
PR185 240_0805_NC
PC93 330U/6.3V/ESR25
PC94 .1U/50V/0603
+5V_ALWP
PR80 0_0402_NC
PR84 0_0402
PL10 2.2uH_SIQH125A-13A/5.5mOhm
PQ25 FDS8878
PQ24 FDS6680AS Rdson=12.5mOhm
+5V_DH
+5V_LX
+5V_DL
PC88 .1U/50V/0603_NC
+5V_ALWP
PR81 324K/F_0402
POK1
PC90 .1U/50V/0603
PR83 1_0603
PU6
MAX8778ETJ+
MAX8778
LDOREFIN LDO VIN VREF3 EN_LDO VCC TON REF
BYP OUT1 FB1 ILIM1 POK1 EN1 UGATE1 PHASE1 PAD PAD PAD PAD
BOOT1 LGATE1 PVCC SECFB GND PGND LGATE2 BOOT2
REFIN2 ILIM2 OUT2 SKIP# POK2 EN2 UGATE2 PHASE2
PR71 309K/F_0402
POK2
PR187 0_0402
PC74 .1U/50V/0603
PR70 1_0603
+3.3V_DH
PQ22 FDS8878
+3.3V_LX
PL7 1.5uH_SIL1055RC-12.5A/7.6mOhm
+3.3V_ALWP
PC68 330U/6.3V/ESR25
PR164 0_0603
PR69 0_0603_NC
+3.3V_DL
PQ21 FDS6680AS Rdson=12.5mOhm
PC73 .1U/50V/0603_NC
+3.3V_ALWP +3.3V_ALWP
PR82 100K_0402
PR166 100K_0402_NC
POK2
PR165 0_0402
POK1
ALW_PWRGD_3V_5V <28>
PD13 BAT54S-7-F
PD12 BAT54S-7-F
PC87 .1U/50V/0603
PC86 .1U/50V/0603
PC75 .1U/50V/0603
PD7 SDM10K45
SJ4 Jump20X10
SJ3 Jump20X10
+15V_ALW
+15V_ALWP
PC169 .1U/50V/0603
PR175 200K/F_0402
PR178 39K/F_0402
PR76 1K/F_0402
<28> ALWON
<34> THERM_STP#
PR75 0_0402
PR77 200K_0402

LDO = 5V (LDOREFIN = GND) or
LDOREFIN RANGE: 0.3V to 2V
LDO = 2x LDOREFIN

REFIN2: DYNAMIC 0 to 2V
REFIN2 = RTC: 1.05V Fixed
REFIN2 = VCC: 3.3V Fixed

QUANTA COMPUTER

Title	3VALW,5V,3V, power on	
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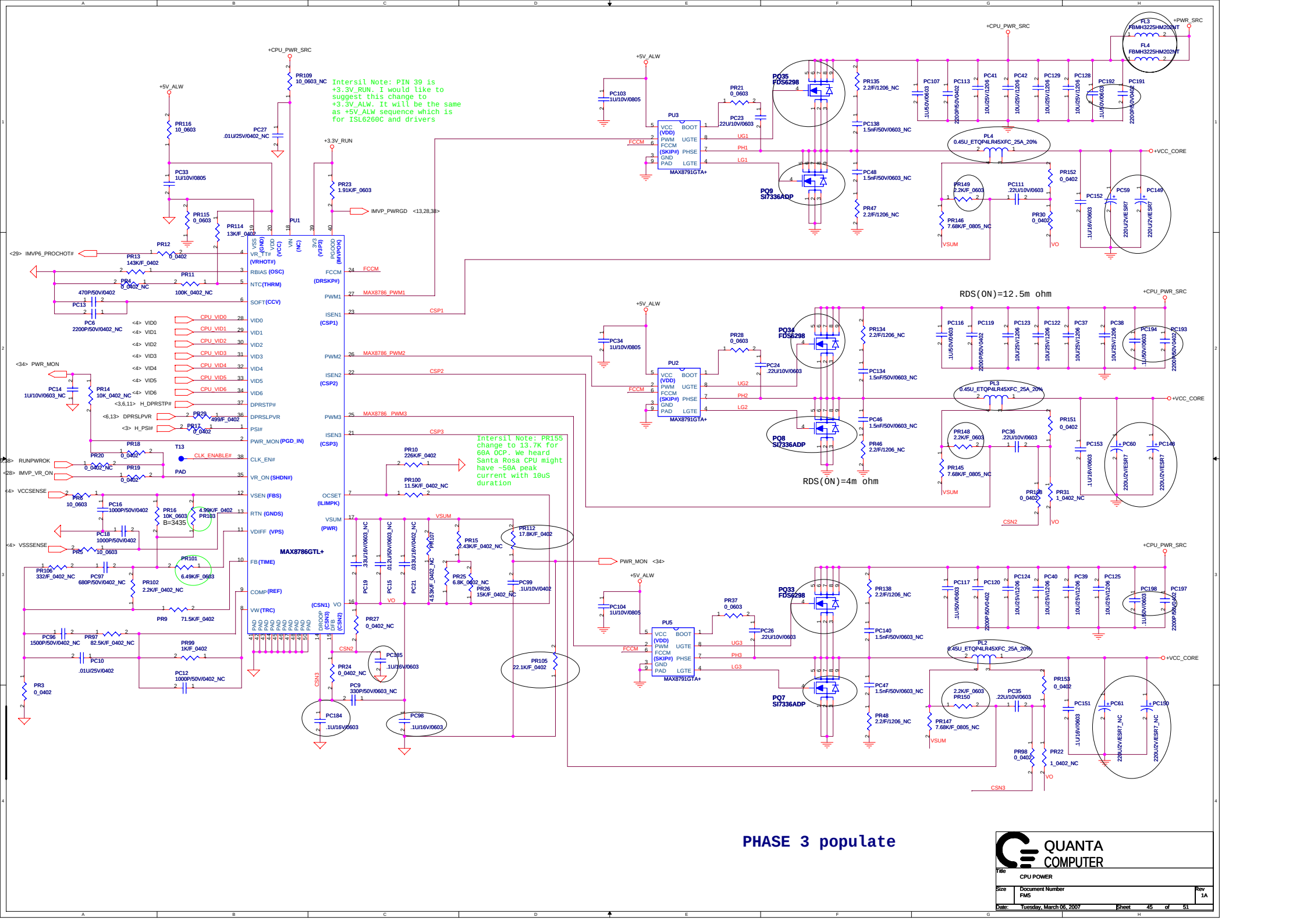
Intersil Note: PIN 39 is +3.3V_RUN. I would like to suggest this change to +3.3V_ALW. It will be the same as +5V_ALW sequence which is for ISL6260C and drivers
Intersil Note: PR155 change to 13.7K for 60A OCP. We heard Santa Rosa CPU might have ~50A peak current with 10uS duration
RDS(ON)=12.5m ohm
RDS(ON)=4m ohm
MAX8786GTL+
MAX8791GTA+
PHASE 3 populate
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POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	ON
S4 (Suspend to DISK) / M1	LOW	HIGH	HIGH	LOW	HIGH	ON	ON	ON	OFF	ON
S5 (SOFT OFF) / M1	LOW	HIGH	LOW	LOW	HIGH	ON	ON	ON	OFF	ON
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State \ power plane	+3.3V_ALW +3.3V_RTC_LDO +3.3V_WLAN +5V_ALW +15V_ALW	+1.8V_SUS +1.8V_LOM +3.3V_LAN +3.3V_SUS +5V_SUS	+0.9V_DDR_VTT +1.05V_VCCP +1.25V_RUN +1.5V_CARD +1.5V_RUN +3.3V_CARD +3.3V_CARDAUX +3.3V_R5C832 +3.3V_RUN	+3.3V_RUN_CARD +2.5V_RUN +5V_MOD +5V_RUN +5V_SPK_AMP +CPU_PWR_SRC +VCC_CORE +VDDA	+DC_IN +DC_IN_SS +PWR_SRC +RTC_CELL
S0	ON	ON	ON		ON
S3	ON	ON	OFF		ON
S5 S4/AC	ON	OFF	OFF		ON
S5 S4/AC don't exist	OFF	OFF	OFF		ON

PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
BCM4401B	AD16	REQ#0 / GNT#0	PIRQB
R5C833	AD17	REQ#1 / GNT#1	PIRQC: Card reader PIEQD: 1394

	USB PORT#	DESTINATION
ICH8-M	0	Right Top
	1	Right Bottom
	2	Side TOP
	3	Side Bottom
	4	Ext. USB TOP
	5	DIgital Camera
	6	Express Card
	7	WPAN/Bluetooth
	8	Ext. USB Bottom
	9	WWAN
ECE 5011	1	None
	2	None
	3	None
	4	None

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	MINI CARD-3 WPAN
Lane 4	Express Card
Lane 5	None
Lane 6	None

QUANTA COMPUTER

Title	Schematic Block Diagram1	
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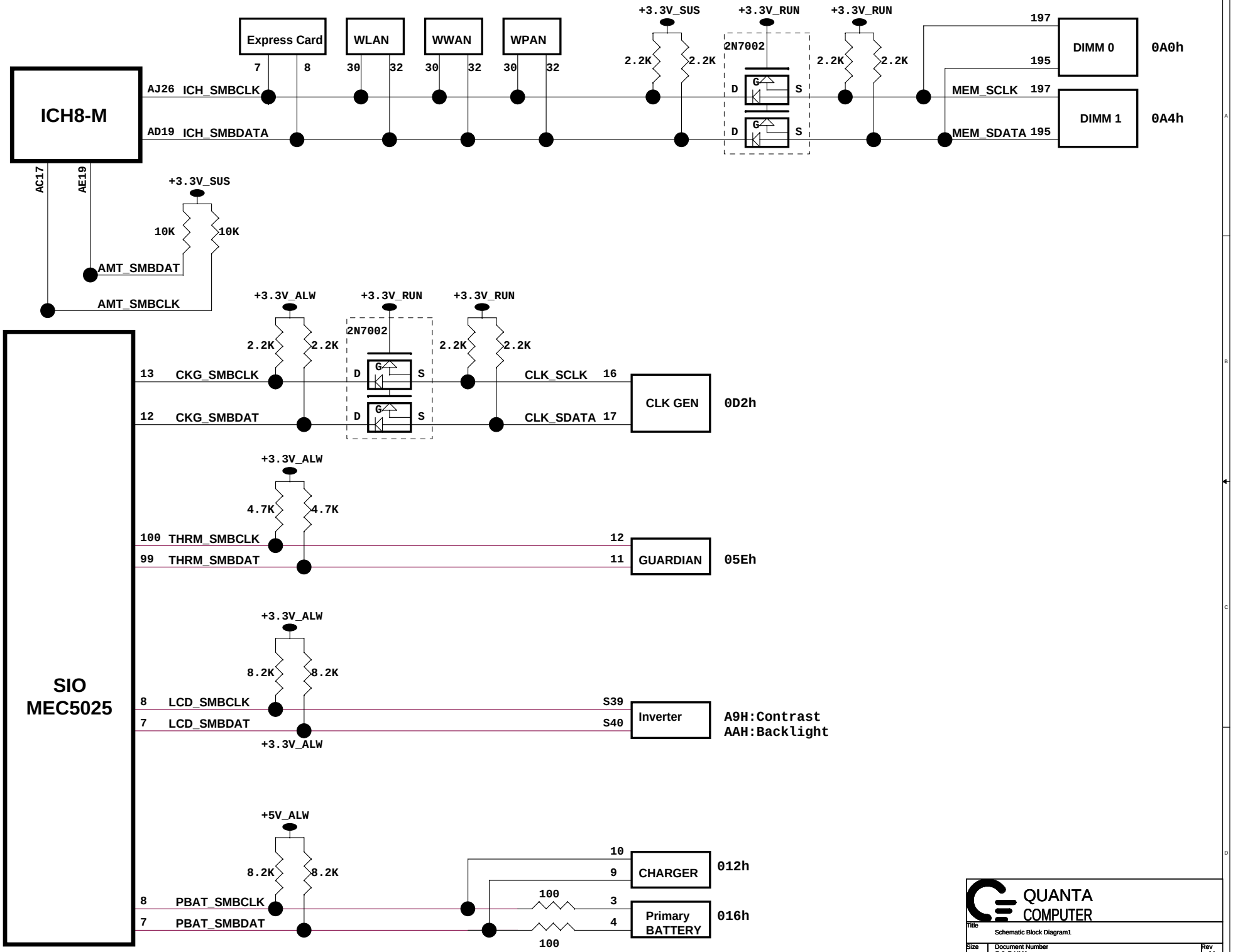

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Title	Schematic Block Diagram1	
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Model	Item	Page	Date	ECN Number	Item Id	Rev.	Issue Description	Solution Description
C/G *DISCRETE*	1	39-45	7/13/2006					Update PWR schematics
	2	13,29	9/20/2006				S3 resume fail	Move PLTRST_DELAY# from EC to ICH8
	3	11	9/20/2006				2nd SATA HDD can't recognize	Move 2nd SATA from port 1 to port 2
	4	38	9/20/2006				Gfx card timing error	Disconnect GFX_PWRGD to system (Delete R463)
	5	38	9/20/2006				Gfx card timing error	Disconnect +1.8V_RUN detect circuit to system (Delete Q47)
	6	39-45	9/21/2006					Update PWR schematics
	7	23	9/21/2006					Add +1.8V_RUN for SATA buffer test (CON4.20-21-22-42-43-44)
	8	37	10/2/2006				Update WLAN LED implementation.With the current implementation, there is a possibility for backdrive from the WLAN LED control signal to +3.3V_RUN while in S3 / S4 / S5. With the voltage rail being +3.3V_WLAN, there is a high probability that the LED will be illuminated while in S3 / S4 / S5.	Please change the WLAN LED implementation to advice from Dell.
	9	13	10/2/2006				Intel has advised that the pull-up on LINKALERT# be depopulated and that the pull-up on GPIO14 be 8.2k. Please update.	Depop R247 & change R227 from 10K ohm to 8.2K ohm
	10	28,33	10/11/2006				In order to leverage the M07 implementation, the sniffer LED circuit needs to be modified. The MEC5025 pins are being changed from active high to active low.	Change back VC08 design, rename SNIFFER_YELLOW to SNIFFER_YELLOW#, SNIFFER_GREEN to SNIFFER_GREEN# and remove R507 and R510.
	11	28,29	10/11/2006				Move DOCK_SMB_PME from MEC5025 SGPIO37 to ECE5018/5011 GPIOC0.Move DOCK_SMB_ALERT# from ECE5018/5011 GPIOC0 to MEC5025 SGPIO37	DOCK_SMB_PME# should be pulled up to +3.3V_ALW DOCK_SMB_ALERT# should be pulled up to +5V_ALW
	12	28,38	10/11/2006				Add ATI_Intel to MEC5025 pin 14 and tie to GND.This connection should be labeled ATI_Intel.	Remove 3.3V_LAN_PWRGD circuit from page 38 Delete 3.3V_LAN_PWRGD from MEC5025 pin 14 Add a connection from the MEC5025 pin 14 and tie to GND.
	13	28	10/11/2006					Move ALW_PWRGD_3V_5V from MEC5025 pin 18 to pin 29
	14	13	10/11/2006					1) Move SIO_EXT_SCI# from ICH pin AG22 to ICH pin AC19 2) Delete R242 (delete DOCKED# signal)
	15	13	10/11/2006					Reserve LOM_SMBALERT# (ICH8 AG22) & PU resister
	16	24	10/16/2006					Change WPAN USB port from USBP7 to USBP4
	17	23,29	10/18/2006				Modify HDDC_EN and MODC_EN Circuits to Resolve Glitch Issue. unintentionally for a brief moment.With the current Dawson design, it has been shown that the +15V_ALW rail comes up before the +3V_ALW rail on the original HDDC_EN and MODC_EN circuits. This can cause a momentary glitch at the gate of the power FET, which may cause the FET to turn on unintentionally for a brief moment.	To resolve this issue, please use the HDDC_EN and MODC_EN circuits that are attached below. These new circuits resemble closely our other load switch circuits, but require an additional FET and changes the sense of the HDDC_EN and MODC_EN signals to active high. Please note the use of +5V_ALW2 on these circuits. The +5V_ALW2 voltage comes directly from the LDO output on the 3V/5V switcher in your M08 design.
	18	12,14	10/18/2006				WWAN Noise - ICH improvements. Add one .1 uF cap on each USB OC (over current) trace near the ICH. Add four .1uF caps in parellel to C813 close to the ICH pins. Add four .1uF caps in parellel to C825 close to the ICH pins.	Add C871~C878 for USB OC. Add C867~C870 in parellel to C825. Add C748,C864~C866 in parellel to C813.
	19	37	10/23/2006				Use LED_MASK# to control BT LED to prevent leakage	Add R336 & change Q13 to BJT
	20	34	10/23/2006				Change pull-up rail on 5V_CAL_SIO1# to +3.3V_SUS. Feedback from SMSC has indicated that the pull-up rail on 5V_CAL_SIO1# needs to change from +5V_SUS to +3.3V_SUS.This is necessary because the GPIO on the EMC4001 is 3V tolerant, not 5V.	Pullup is at reference designator R298.
	21	28	10/23/2006				Due to the power on defaults of the MEC5025, the pull-downs on the KSI lines of the MEC5025 need to be stronger, to avoid pulses from powering on certain power rails. Please do the following: 1. Change pull-down on SUS_ON to 2.7k 2. Change pull-down on RUN_ON to 2.7k	Change R355,R358 to 2.7K
	22	24	10/23/2006				Add SMBus isolation circuitry for WLAN.Add isolation circuitry for SMBus on WLAN.	

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Title	Change List		
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Model	Item	Page	Date	ECN Number	Item Id	Rev.	Issue Description	Solution Description
C/G *DISCRETE*	23	17	10/26/2006				Chipset side spec. Differetial CLK raise/fall slew rate is 2.5~8 V/ns, only express card and mini card is 0.6~4V/ns. BITCLK rise/fall slew rate in 1-3 V/ns &	Change serial resistors (PR4,PR5,PR10,PR12,PR13) to meet the CLK SPEC
	24	37	10/26/2006				Change LED control method	
	25	37	10/26/2006				Add OR gate for BT_ACTIVE	
	26	13	10/26/2006				M08 GPIO A14 update. Original EC5011 pin66 CCD_VDD_ON move to IC8 pinAD10 GPIO48 and add 100K ohm pull down.	Move CCD_VDD_ON from EC5011 pin66to IC8 pin AD10 GPIO48 and add 100K ohm pull down.
	27	25	10/26/2006				For Comm team suggestion (GG list), pop C217 for WWAN	
	28	39 - 45	10/31/2006				PWR team updat schemtics - 10/23	

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Title	Change List	
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Model	Item	Page	Date	ECN Number	Item Id	Rev.	Issue Description	
C/G *DISCRETE*	29	24 - 25	11/1/2006				For EMI request, add RC circuit for Mini card clk request	Add R543, C880, R186, C649, R544, C181
	30	39	11/1/2006				For +3.3V_RUN inrush current, it may over OCP (12.36 A)	Change PC58 from 470 pF to 6800 pF
	31	32	11/3/2006				For AP - THN+D fail, change C306, 307 to 0.033uF/16V/X7R/1206 & C326, C329 to 1uF/16V/X7R/1206	Change C306, 307 to 0.033uF/16V/X7R/1206 & C326, C329 to 1uF/16V/X7R/1207
	32	32	11/3/2006				'PO' noise in resume from S3,S4,S5	Reserved the AUD_AMP_MUTE# for 'PO' noise
	33	39 - 45	11/09/2006				PWR team updat schemtics - 11/08	
	34	17	11/09/2006				Change R44 to 2.2K per Intel recommend value.	
	35	12 - 13	11/21/2006				Due to Intel-ICH8 uses GPIO20 pin AE11 as an Internal Strapping at power up	Move PCIE_MCARD2_DET# from GPIO20 to ICH8 GPIO5/PIRQH# pin B3.
	36	13	11/21/2006				GPIO18 is default as an output at power up, it will drive 1Hz output at power up. Per Intel this GPIO could not be connected to GND	Add 4.7K series - R547 resistor to separate it
	37	32	11/22/2006				There is potential back drive from the codec DVdd back to the AVdd supply due to an internal ESD diode	add 100kohm resistor (R253) between pin 40 and +3.3V_RUN and a 1000pF cap (C643 below) from Pin 40 to ground
	38	35 - 36	11/28/2006				GG list -- COMM team request	1.Change capacitor for U5 pin 79, 94,106 (VDDIO) (C18, C16, C25) to 47pF. 2.Change those three capacitors (C27, C37,C34) to 47pF 3.Add C644 - 47pF capacitor by the pin 57 of U5 4.Change L7 to 0805 package -BK2125LM152. & C23 to 47 pF 5.Add Ferrite Bead BK1608LM152 on 1.8V to EPHY_AVDD pin 57
	39	28-29	11/28/2006				Move DOCK_SMB_PME from MEC5025 SGPIO37 to ECE5018/5011 GPIOC0.Move DOCK_SMB_ALERT# from ECE5018/5011 GPIOC0 to MEC5025 SGPIO37	DOCK_SMB_PME# should be pulled up to +5V_ALW DOCK_SMB_ALERT# should be pulled up to +3.3V_ALW
	40	24	12/01/2006				GG list -- Seperate debug port with MINI-PCI if not necessary	Add 4 0ohm resistors for these pins
	41	24 - 25	12/01/2006				GG list -- Delete decoupling cap	Delete C222 & C424
	42	39 - 45	12/04/2006				PWR team updat schemtics - 12/04	
	43	32	12/08/2006				GG List -- Change audio AMP to TI solution	1.Change codec to TPA9040A4 2.Pop R505, C619 & C614; depop R506, R504 & R497
	44	31	12/13/2006				GG List -- Change power source for LED of dash board	Change JTP1.9 from +3.3V_RUN to +5V_ALW
	45	39 - 45	12/19/2006				PWR team updat schemtics - 12/19	
	46	28	12/25/2006				GG List -- Remove EC5025 pin15 GPIO4 AUD_AMP_MUTE# circuit.	NC R538
	47	34	12/25/2006				GG List -- Add THERMATRIP_VGA# function	Pop R441,442,443 and Q35, C568 for THERMATRIP_VGA# trip.
	48	33	12/28/2006				Modify CCD power control soft start function	Change C403 , R284 connect method

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Title	EMI & Screw hole	
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Model	Item	Page	Date	ECN Number	Item Id	Rev.	Issue Description	
C/G *DISCRETE*	49	22	1/11/2006				XD card detect function error	
	50	29	1/11/2006				Base on A16 GPIO : Change net name from BID2 to CHIPSET_ID1	
	51	37	1/24/2007				Add 0ohm_NC(R571) resistor pad connected from Coex1_BT_Active_MINI to Coex1_BT_Active	
	52	32	1/24/2007				Audio solution for pass EMI 225MHz and 451MHz radiation emission test.	Added R560, R561, R562 and R563 on AUD_SPK_L1, AUD_SPK_L2, AUD_SPK_R1, AUD_SPK_R2 trace
	52	33	1/24/2007				Audio solution for pass EMI 225MHz and 451MHz radiation emission test.	Added R564, R565, R566 and R567 on AUD_LINE_OUT,AUD_HP_OUT
	53	13	1/24/2007				GG List -- CCD_ON pull down R258 100K NC.	
	54	37	2/5/2007				Blue LED brightness is too high	Change R30,R50,R75,R64 & R36 from 220 ohm to 330 ohm
	55	30	2/12/2007				Prevent SPI CLK overshoot/undershoot issue	Add C896 for RC circuit but not pop it
	56	39 - 45	2/12/2007				PWR team updat schemtics - 2/12	
	57	29	2/12/2007				GG List -- CIR function intermidiate issue	ECE5021 pin7 PWRGD need to pull-down to GND with 0 ohm - Add R568 PD resistor & R569 series resistor (NC)
	58	44	3/1/2007				PWR team updat schemtics - 3/1	
	59	17	3/2/2007				Per TDC COMM team request - Change L65 to	Fine tune 14M CLK - Change R57 from 33 to 15 ohm & L65 to BLM18SG260
	60	04	3/2/2007				Per reliability issue - Move C98 to C249	De-pop C98 & pop C249

QUANTA COMPUTER

Title	EMI & Screw hole	
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